

Chapter 29 Image Enhancement Processor (IEP)

29.1 Overview

The Image Enhancement Processor (IEP) receives data from and transmits data to system main memory by AXI bus, or output the data to LCD controller directly.

The features of IEP are as follow:

- **Image format**
 - Input data: XRGB/RGB565/YUV420/YUV422
 - Output data: ARGB/RGB565/YUV420/YUV422
 - ARGB/XRGB/RGB565/YUV swap
 - YUV semi-planar/planar
 - BT601_l/BT601_f/BT709_l/BT709_f color space conversion
 - RGB dither up/down conversion
 - YUV up/down sampling conversion
 - Max source image resolution: 8192x8192
 - Max scaled image resolution: 4096x4096
- **Enhancement**
 - Gamma adjustment with programmable mapping table
 - Hue/Saturation/Brightness/Contrast enhancement
 - Color enhancement with programmable coefficient
 - Detail enhancement with filter matrix up to 9x9
 - Edge enhancement with filter matrix up to 9x9
 - Programmable difference table for detail enhancement
 - Programmable distance table for detail and edge enhancement
- **Noise reduction**
 - Compression noise reduction with filter matrix up to 9x9
 - Programmable difference table for compression noise reduction
 - Programmable distance table for compression noise reduction
 - Spatial sampling noise reduction
 - Temporal sampling noise reduction
 - Optional coefficient for sampling noise reduction
- **High quality scaling**
 - Horizontal down-scaling with vertical down-scaling
 - Horizontal down-scaling with vertical up-scaling
 - Horizontal up-scaling with vertical down-scaling
 - Horizontal up-scaling with vertical up-scaling
 - Arbitrary non-integer scaling ratio, from 1/16 to 16
- **De-interlace**
 - Input 4 fields, output 2 frames mode
 - Input 4 fields, output 1 frames mode
 - Input 2 fields, output 1 frames mode
 - Programmable motion detection coefficient
 - Programmable high frequency factor
 - Programmable edge interpolation parameter

- Source width up to 1920
- **Interface**
 - Programmable direct path to VOP
 - 32bit AHB bus slave
 - 64bit AXI bus master
 - Combined interrupt output

29.2 Block Diagram

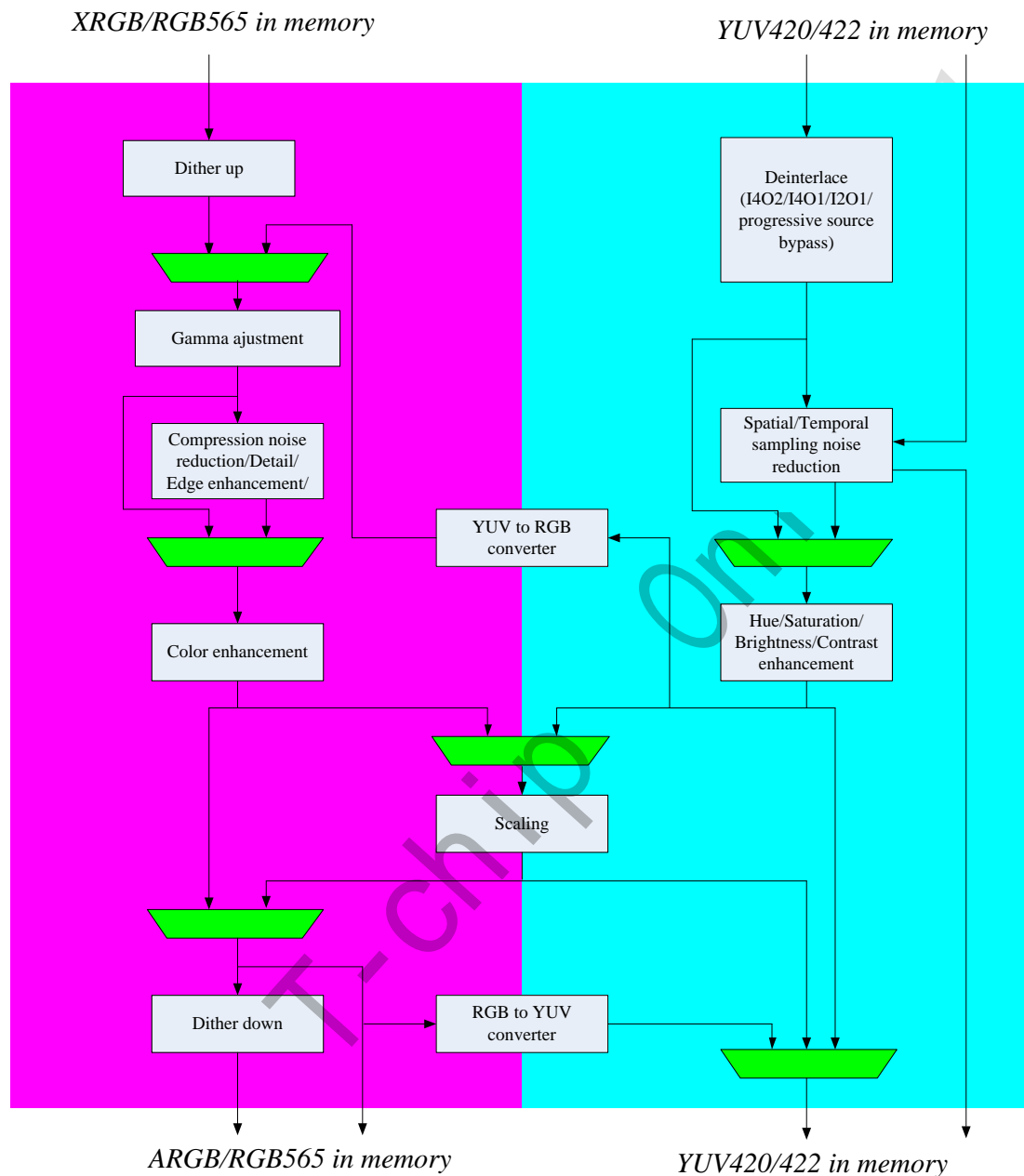


Fig. 29-1 IEP block diagram

The data path in IEP is in the previously diagram. The IEP comprises with:

- Deinterlace
There are five deinterlace mode including I4O2 (input 4 fields and output 2 frames once), I4O1B, I4O1T, I2O1B, I2O1T in the deinterlace block. YUV bypass is also supported.
- Enhancement

Not only hue, saturation, brightness, contrast enhancement, but also blue screen, black screen and color bar are supported in YUV domain enhancement block. Gamma adjustment, edge enhancement, detail enhancement and color enhancement are supported in RGB domain enhancement block.

- Noise Reduction

Spatial and temporal sampling noise can be reduced in YUV domain noise reduction block. Compression noise can be reduced in RGB domain noise reduction block.

- Scaling

There are four types of scaling modes.

- Horizontal down-scaling with vertical down-scaling
- Horizontal down-scaling with vertical up-scaling
- Horizontal up-scaling with vertical down-scaling
- Horizontal up-scaling with vertical up-scaling

29.3 Function description

29.3.1 Deinterlace

There are five deinterlace mode including I4O2, I4O1B, I4O1T, I2O1B and I2O1T in the deinterlace block. The I4O2 mode represents for 4 fields of input images and 2 frames of output images, so all of the two groups of source address registers and two groups of destination address registers need to be configured. For example, if source and destination format are both YUV420, the source address register IEP_SRC_ADDR_YRGB, IEP_SRC_ADDR_CBCR are used for source field0 and field 1, the source address register IEP_SRC_ADDR_Y1, IEP_SRC_ADDR_CBCR1 are used for source field2 and field3. The I4O1B and I4O1T mode have the same input images as the I4O2 mode, but only one frame output is generated once. The I2O1B and I2O1T mode have the same output as I4O1B and I4O1T mode, but only two fields input are needed. If bypass mode is selected, there are not any deinterlace operations. The parameter dil_ei_sel, dil_ei_radius, dil_ei_smooth, dil_ei_mode, dil_hf_en and dil_hf_fct in register IEP_CONFIG0 and registers IEP_DIL_MTN_TAB0~7 may have different influence in deinterlace effect depend on the type of the image source.

29.3.2 Noise reduction

Both of spatial and temporal sampling noise reduction are enabled when the 3D denoise bit is set. This function is used for reducing the noise generated at video or picture capturing in the camera sensor. There are four groups of optional noise reduction effect coefficients for luminance and chrominance in spatial and temporal segment.

Compression noise reduction is used for reducing the noise after the decompression of picture or video. Before the compression noise reduction is enabled, the IEP_ENH_DDE_COE0/1 from address 0x400 to 0x5FC for difference and distance coefficients must be written firstly. The filter matrix can be selected from 3x3/5x5/7x7/9x9 and the filter weight can be programmed by configuring IEP_ENH_RGB_CNFG.

29.3.3 Enhancement

Not only hue, saturation, brightness, contrast enhancement, but also blue screen, black screen and color bar are supported in this block. IEP_ENH_YUV_CNFG_0/1/2 registers can be configured to modify the YUV enhance parameters to satisfied with the requirement.

Before the gamma adjustment or contrast enhancement is enabled in RGB domain, the IEP_ENH_CG_TAB from address 0x100 to 0x3FC for B, G, R mapping must be written firstly. If the color enhancement is enabled, the IEP_ENH_C_COE must be written the required value.

Before the edge or detail enhancement is enabled, the IEP_ENH_DDE_COE0/1 from address

0x400 to 0x5FC for difference and distance coefficients must be written firstly. The filter matrix can be selected from 3x3/5x5/7x7/9x9 and the filter weight can be programmed by configuring IEP_ENH_RGB_CNFG.

29.3.4 Scaling

There are four types of scaling modes: horizontal down & vertical down-scaling, horizontal down & vertical up-scaling, horizontal up & vertical down-scaling, horizontal up & vertical up-scaling. The down-scaling and up-scaling factor can be got from different way. The detail calculated method is the following:

- $vrt_up_scl_fct = \text{floor}(\text{src_image_height} / \text{dst_image_height})$
- $vrt_dn_scl_fct = \text{ceiling}((\text{dst_image_height} + 1) / (\text{src_image_height} + 1))$
- $hrz_up_scl_fct = \text{floor}(\text{src_image_width} / \text{dst_image_width})$
- $hrz_dn_scl_fct = \text{ceiling}((\text{dst_image_width} + 1) / (\text{src_image_width} + 1))$

There are four up-scaling type (Hermite, Spline, Catrom and Mitchell) can be selected for difference requirement.

29.3.5 Format conversion

The color space conversion either from RGB to YUV or from YUV to RGB has the selections including BT601/709_L/F mode, and the input can be clipped or not.

If the source format is RGB565, dither up must be enabled. In contrary to the destination format is RGB565, dither down must be enabled.

29.3.6 Shadow registers

The configuration registers can be configured at any time, but they cannot have any effect immediately unless config_done is available and a new frame_start is enabled. The registers IEP_RAW_CONFIG0/1, IEP_RAW_VIR_IMG_WIDTH, IEP_RAW_IMG_SCL_FCT, IEP_RAW_SRC_IMG_SIZE, IEP_RAW_ENH_YUV_CNFG_0/1/2 corresponding to the registers have the similar names but without letters _RAW. They are used for raw register value reading before the configurations really have effect on the new frame.

29.3.7 VOP direct path

The IEP_DST_ADDR for DMA writing is useless if vop_path_en bit is set, because all RGB or YUV data is supplied for VOP directly from local bus via VOP and IEP.

29.4 Register description

29.4.1 Register Summary

Name	Offset	Size	Reset Value	Description
IEP_CONFIG0	0x00000	W	0x00000000	configuration register0
IEP_CONFIG1	0x00004	W	0x00000000	configuration register1
IEP_STATUS	0x00008	W	0x00000000	status register
IEP_INT	0x0000c	W	0x00000000	interrupt register
IEP_FRM_START	0x00010	W	0x00000000	frame start
IEP_CONFIG_DONE	0x00018	W	0x00000000	configuration done
IEP_FRM_CNT	0x0001c	W	0x00000000	frame counter

Name	Offset	Size	Reset Value	Description
IEP_VIR_IMG_WIDTH_H	0x00020	W	0x01400140	Image virtual width
IEP_IMG_SCL_FCT	0x00024	W	0x20002000	scaling factor
IEP_SRC_IMG_SIZE	0x00028	W	0x00f00140	Source image width/height
IEP_DST_IMG_SIZE	0x0002c	W	0x00f00140	Destination image width/height
IEP_DST_IMG_WIDTH_TILE0	0x00030	W	0x00000000	Destination image tile0 width
IEP_DST_IMG_WIDTH_TILE1	0x00034	W	0x00000000	Destination image tile1 width
IEP_DST_IMG_WIDTH_TILE2	0x00038	W	0x00000000	Destination image tile2 width
IEP_DST_IMG_WIDTH_TILE3	0x0003c	W	0x00000000	Destination image tile3 width
IEP_ENH_YUV_CNFG_0	0x00040	W	0x00000000	brightness,contrast,saturation adjustment
IEP_ENH_YUV_CNFG_1	0x00044	W	0x00000000	Hue configuration
IEP_ENH_YUV_CNFG_2	0x00048	W	0x00000000	color bar configuration
IEP_ENH_RGB_CNFG	0x0004c	W	0x00000000	enhancement RGB configuration
IEP_ENH_C_COE	0x00050	W	0x00000000	rgb color enhancement coefficient
IEP_RAW_CONFIG0	0x00058	W	0x00000000	configuration register0
IEP_RAW_CONFIG1	0x0005c	W	0x00000000	configuration register1
IEP_RAW_VIR_IMG_WIDTH	0x00060	W	0x01400140	Image virtual width
IEP_RAW_IMG_SCL_FCT	0x00064	W	0x20002000	scaling factor
IEP_RAW_SRC_IMG_SIZE	0x00068	W	0x00f00140	Source image width/height
IEP_RAW_DST_IMG_SIZE	0x0006c	W	0x00f00140	Destination image width/height
IEP_RAW_ENH_YUV_CNFG_0	0x00070	W	0x00000000	brightness,contrast,saturation adjustment
IEP_RAW_ENH_YUV_CNFG_1	0x00074	W	0x00000000	Hue configuration
IEP_RAW_ENH_YUV_CNFG_2	0x00078	W	0x00000000	color bar configuration
IEP_RAW_ENH_RGB_CNFG	0x0007c	W	0x00000000	enhancement RGB configuration

Name	Offset	Size	Reset Value	Description
IEP_SRC_ADDR_YRGB	0x00080	W	0x00000000	Start address of source image(Y/RGB)
IEP_SRC_ADDR_CBCR	0x00084	W	0x00000000	Start address of source image(Cb/Cr)
IEP_SRC_ADDR_CR	0x00088	W	0x00000000	Start address of source image(Cr)
IEP_SRC_ADDR_Y1	0x0008c	W	0x00000000	Start address of source image(Y)
IEP_SRC_ADDR_CBCR1	0x00090	W	0x00000000	Start address of source image(Cb/Cr)
IEP_SRC_ADDR_CR1	0x00094	W	0x00000000	Start address of source image(Cr)
IEP_SRC_ADDR_Y_I TEMP	0x00098	W	0x00000000	Start address of source image(Y integer part)
IEP_SRC_ADDR_CBCR_I TEMP	0x0009c	W	0x00000000	Start address of source image(CBCR integer part)
IEP_SRC_ADDR_CR_I TEMP	0x000a0	W	0x00000000	Start address of source image(CR integer part)
IEP_SRC_ADDR_Y_F TEMP	0x000a4	W	0x00000000	Start address of source image(Y fraction part)
IEP_SRC_ADDR_CBCR_F TEMP	0x000a8	W	0x00000000	Start address of source image(CBCR fraction part)
IEP_SRC_ADDR_CR_F TEMP	0x000ac	W	0x00000000	Start address of source image(CR fraction part)
IEP_DST_ADDR_YRGB	0x000b0	W	0x00000000	Start address of destination image(Y/RGB)
IEP_DST_ADDR_CBCR	0x000b4	W	0x00000000	Start address of destination image(Cb/Cr)
IEP_DST_ADDR_CR	0x000b8	W	0x00000000	Start address of destination image(Cr)
IEP_DST_ADDR_Y1	0x000bc	W	0x00000000	Start address of destination image(Y)
IEP_DST_ADDR_CBCR1	0x000c0	W	0x00000000	Start address of destination image(Cb/Cr)
IEP_DST_ADDR_CR1	0x000c4	W	0x00000000	Start address of destination image(Cr)
IEP_DST_ADDR_Y_I TEMP	0x000c8	W	0x00000000	Start address of destination image(Y integer part)

Name	Offset	Size	Reset Value	Description
IEP_DST_ADDR_CBCR_ITEMP	0x000cc	W	0x00000000	Start address of destination image(CBCR integer part)
IEP_DST_ADDR_CR_ITEMP	0x000d0	W	0x00000000	Start address of destination image(CR integer part)
IEP_DST_ADDR_Y_FTEMP	0x000d4	W	0x00000000	Start address of destination image(Y fraction part)
IEP_DST_ADDR_CBCR_FTEMP	0x000d8	W	0x00000000	Start address of destination image(CBCR fraction part)
IEP_DST_ADDR_CR_FTEMP	0x000dc	W	0x00000000	Start address of destination image(CR fraction part)
IEP_DIL_MTN_TAB0	0x000e0	W	0x00000000	Deinterlace motion table0
IEP_DIL_MTN_TAB1	0x000e4	W	0x00000000	Deinterlace motion table1
IEP_DIL_MTN_TAB2	0x000e8	W	0x00000000	Deinterlace motion table2
IEP_DIL_MTN_TAB3	0x000ec	W	0x00000000	Deinterlace motion table3
IEP_DIL_MTN_TAB4	0x000f0	W	0x00000000	Deinterlace motion table4
IEP_DIL_MTN_TAB5	0x000f4	W	0x00000000	Deinterlace motion table5
IEP_DIL_MTN_TAB6	0x000f8	W	0x00000000	Deinterlace motion table6
IEP_DIL_MTN_TAB7	0x000fc	W	0x00000000	Deinterlace motion table7
IEP_ENH_CG_TAB	0x00100	W	0x00000000	contrast and gamma enhancement table
IEP_ENH_DDE_COE0	0x00400	W	0x00000000	denoise,detail and edge enhancement coefficient
IEP_ENH_DDE_COE1	0x00500	W	0x00000000	denoise,detail and edge enhancement coefficient
IEP_MMU_DTE_ADDR	0x00800	W	0x00000000	MMU current page table address
IEP_MMU_STATUS	0x00804	W	0x00000018	MMU status register
IEP_MMU_CMD	0x00808	W	0x00000000	MMU command register
IEP_MMU_PAGE_FAULT_ADDR	0x0080c	W	0x00000000	MMU logic address of last page fault

Name	Offset	Size	Reset Value	Description
IEP_MMU_ZAP_ONE_LINE	0x00810	W	0x00000000	MMU zap cache line register
IEP_MMU_INT_RAW_STAT	0x00814	W	0x00000000	MMU raw interrupt status register
IEP_MMU_INT_CLEAR	0x00818	W	0x00000000	MMU interrupt clear register
IEP_MMU_INT_MASK	0x0081c	W	0x00000000	MMU interrupt mask register
IEP_MMU_INT_STAT_US	0x00820	W	0x00000000	MMU interrupt status register
IEP_MMU_AUTO_GATING	0x00824	W	0x00000001	MMU clock auto gating register

Notes: **Size** : **B** - Byte (8 bits) access, **HW** - Half WORD (16 bits) access, **W** -WORD (32 bits) access

29.4.2 Detail Register Description

IEP_CONFIG0

Address: Operational Base + offset (0x00000)
configuration register0

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	scl_en image scaling enable 0:disable 1:enable
27:26	RW	0x0	scl_sel Scaling select 00: horizontal down-scaling & vertical down-scaling; 01: horizontal down-scaling & vertical up-scaling; 10: horizontal up-scaling & vertical down-scaling; 11: horizontal up-scaling & vertical up-scaling;
25:24	RW	0x0	scl_up_coe_sel scale up coefficient select 00:hermite 01:spline 10:catrom 11:mitchell
23	RW	0x0	dil_ei_sel deinterlace edge interpolation select

Bit	Attr	Reset Value	Description
22:21	RW	0x0	dil_ei_radius deinterlace edge interpolation radius
20	RW	0x0	rgb_con_gam_order RGB contrast enhancement and gamma adjustment operation order select. 0:CG prior to DDE 1:DDE prior to CG (CG represent for contrast & gamma operation, and DDE represent for denoise, detail or edge enhancement operation)
19:18	RW	0x0	rgb_enh_sel RGB enhancement select 00: no operation 01: denoise 10: detail enhancement 11: edge enhancement
17	RW	0x0	rgb_con_gam_en RGB contrast enhancement and gamma adjustment enable 0:disable 1:enable
16	RW	0x0	rgb_color_enh_en RGB color enhancement enable 0:disable 1:enable
15	RW	0x0	dil_ei_smooth deinterlace edge interpolation for smooth effect 0: disable 1: enable
14	RW	0x0	yuv_enh_en yuv enhancement enable 0:disable 1:enable
13	RW	0x0	yuv_dns_en YUV 3D denoise enable 0:disable 1:enable
12	RW	0x0	dil_ei_mode deinterlace edge interpolation 0: disable 1: enable

Bit	Attr	Reset Value	Description
11	RW	0x0	dil_hf_en deinterlace high frequency calculation enable 0: disable 1: enable
10:8	RW	0x0	dil_mode Deinterlace mode select: 000: YUV deinterlace and bypass path disable; 001: I4O2 mode 010: I4O1B mode 011: I4O1T mode 100: I2O1B mode 101: I2O1T mode 110: bypass mode
7:1	RW	0x00	dil_hf_fct deinterlace high frequency factor
0	RW	0x0	vop_path_en VOP direct path enable 0:disable 1:enable

IEP_CONFIG1

Address: Operational Base + offset (0x00004)
configuration register1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	glb_alpha global alpha value only valid when destination format is ARGB
23	RW	0x0	rgb2yuv_input_clip RGB to YUV input range 0:R/G/B=[0,255] 1:R/G/B=[16,235]
22	RW	0x0	yuv2rgb_input_clip YUV to RGB input range 0:Y/U/V=[0,255] 1:Y=[16,235],U/V=[16,240]
21	RW	0x0	rgb_to_yuv_en RGB to YUV conversion enable 0: disable 1: enable
20	RW	0x0	yuv_to_rgb_en YUV to RGB conversion enable 0: disable 1: enable

Bit	Attr	Reset Value	Description
19:18	RW	0x0	rgb2yuv_coe_sel rgb2yuv coefficient select 00:bt601_1 01:bt601_f 10:bt709_1 11:bt709_f
17:16	RW	0x0	yuv2rgb_coe_sel yuv2rgb coefficient select 00:bt601_1 01:bt601_f 10:bt709_1 11:bt709_f
15	RW	0x0	dthr_down_en dither down enable 0: disable 1: enable
14	RW	0x0	dthr_up_en dither up enable 0: disable 1: enable
13:12	RW	0x0	dst_yuv_swap destination YUV swap 00:SP UV 01:SP VU 10, 11:P
11:10	RW	0x0	dst_rgb_swap destination RGB swap ARGB destination 00:ARGB 01:ABGR 10:RGBA 11:BGRA RGB565 destination 00,10:RGB 01,11:BGR
9:8	RW	0x0	dst_fmt Output image Format 00 : ARGB 01 : RGB565 10 : YUV422 11 : YUV420
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:4	RW	0x0	src_yuv_swap source YUV swap 00:SP UV 01:SP VU 10, 11:P
3:2	RW	0x0	src_rgb_swap source RGB swap XRGB source 00:XRGB 01:XBGR 10:RGBX 11:BGRX RGB565 source 00,10:RGB 01,11:BGR
1:0	RW	0x0	src_fmt Input image Format 00 : XRGB 01 : RGB565 10 : YUV422 11 : YUV420

IEP_STATUS

Address: Operational Base + offset (0x00008)

status register

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19	RW	0x0	rrgb_idle_ack RGB read DMA idle acknowlege
18	RW	0x0	wrgb_idle_ack RGB write DMA idle acknowlege
17	RW	0x0	ryuv_idle_ack YUV read DMA idle acknowlege
16	RW	0x0	wyuv_idle_ack YUV write DMA idle acknowlege
15:9	RO	0x0	reserved
8	RO	0x0	voi_sts vop direct path status 00:idle 01:working

Bit	Attr	Reset Value	Description
7	RO	0x0	rrgb_sts RGB DMA read status 00:idle 01:working
6	RO	0x0	wrgb_sts RGB DMA write status 00:idle 01:working
5	RO	0x0	ryuv_sts YUV DMA read status 00:idle 01:working
4	RO	0x0	wyuv_sts YUV DMA write status 00:idle 01:working
3	RO	0x0	dde_sts RGB denoise/enhancement status 00:idle 01:working
2	RO	0x0	dil_sts de-interlace or yuv bypass status 00:idle 01:working
1	RO	0x0	scl_sts scaling status 00:idle 01:working
0	RO	0x0	dns_sts YUV 3D denoise status 00:idle 01:working

IEP_INT

Address: Operational Base + offset (0x0000c)
interrupt register

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	W1C	0x0	frm_done_int_clr Frame process done interrupt clear After be set to 1, this bit will be clear automatically.
15:9	RO	0x0	reserved

Bit	Attr	Reset Value	Description
8	RW	0x0	frm_done_int_en Frame process done interrupt enable: 0: disable; 1: enable;
7:1	RO	0x0	reserved
0	RO	0x0	frm_done_int Frame process done interrupt 0: inactive; 1: active;

IEP_FRM_START

Address: Operational Base + offset (0x00010)

frame start

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	W1C	0x0	frm_start frame start Write 1, self clear.

IEP_CONFIG_DONE

Address: Operational Base + offset (0x00018)

configuration done

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	config_done configuration done Wait for frame start to update raw register configuration to really used registers.

IEP_FRM_CNT

Address: Operational Base + offset (0x0001c)

frame counter

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	frm_cnt frame counter Self increase one after a frame operation is finished. Write arbitrary value to clear to zero.

IEP_VIR_IMG_WIDTH

Address: Operational Base + offset (0x00020)

Image virtual width

Bit	Attr	Reset Value	Description
31:16	RW	0x0140	dst_vir_image_width Destination virtual image width

Bit	Attr	Reset Value	Description
15:0	RW	0x0140	src_vir_image_width Source virtual image width

IEP_IMG_SCL_FCT

Address: Operational Base + offset (0x00024)

scaling factor

Bit	Attr	Reset Value	Description
31:16	RW	0x2000	vrt_scl_fct Vertical scale factor up scaling: $vrt_scl_fct = \text{floor}(src_image_height / dst_image_height)$; down scaling: $vrt_scl_fct = \text{ceiling}((dst_image_height + 1) / (src_image_height + 1))$;
15:0	RW	0x2000	hrz_scl_fct Horizontal scale factor up scaling: $hrz_scl_fct = \text{floor}(src_image_width / dst_image_width)$; down scaling: $hrz_scl_fct = \text{ceiling}((dst_image_width + 1) / (src_image_width + 1))$;

IEP_SRC_IMG_SIZE

Address: Operational Base + offset (0x00028)

Source image width/height

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x00f0	src_image_height source image height
15:13	RO	0x0	reserved
12:0	RW	0x0140	src_image_width source image width

IEP_DST_IMG_SIZE

Address: Operational Base + offset (0x0002c)

Destination image width/height

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

Bit	Attr	Reset Value	Description
28:16	RW	0x00f0	dst_image_height Destination image height
15:13	RO	0x0	reserved
12:0	RW	0x0140	dst_image_width Destination image width

IEP_DST_IMG_WIDTH_TILE0

Address: Operational Base + offset (0x00030)

Destination image tile0 width

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	dst_image_width_tile0 Destination image tile0 width

IEP_DST_IMG_WIDTH_TILE1

Address: Operational Base + offset (0x00034)

Destination image tile1 width

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:0	RW	0x000	dst_image_width_tile1 Destination image tile1 width

IEP_DST_IMG_WIDTH_TILE2

Address: Operational Base + offset (0x00038)

Destination image tile2 width

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:0	RW	0x000	dst_image_width_tile2 Destination image tile2 width

IEP_DST_IMG_WIDTH_TILE3

Address: Operational Base + offset (0x0003c)

Destination image tile3 width

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:0	RW	0x000	dst_image_width_tile3 Destination image tile3 width

IEP_ENH_YUV_CNFG_0

Address: Operational Base + offset (0x00040)

brightness,contrast,saturation adjustment

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	sat_con YUV saturation and contrast adjustment saturation * contrast range from 0 to 1.992*1.992, and this value is saturation* contrast * 128
15:8	RW	0x00	contrast YUV contrast adjustment contrast value range from 0 to 1.992, and this value is contrast*128.
7:6	RO	0x0	reserved
5:0	RW	0x00	brightness YUV brightness adjustment range from -32 to 31 000000:0; 000001:1; 011111:31; 100000:-32; 100001:-31; 111110:-2; 111111:-1;

IEP_ENH_YUV_CNFG_1

Address: Operational Base + offset (0x00044)

Hue configuration

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:8	RW	0x00	cos_hue the cos function value for hue adjustment sin function value range from 0.866 to 1 ,and this value is cos * 128 ,no sign bit
7:0	RW	0x00	sin_hue the sin function value for hue adjustment sin function value range from -0.5 to 0.5 ,and this value is sin * 128 ,and the high bit is sign bit

IEP_ENH_YUV_CNFG_2

Address: Operational Base + offset (0x00048)

color bar configuration

Bit	Attr	Reset Value	Description
-----	------	-------------	-------------

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:24	RW	0x0	video_mode video mode 00:black screen 01:blue screen 10:color bars 11:normal video
23:16	RW	0x00	color_bar_v color bar v value
15:8	RW	0x00	color_bar_u color bar u value
7:0	RW	0x00	color_bar_y color bar y value

IEP_ENH_RGB_CNFG

Address: Operational Base + offset (0x0004c)

enhancement RGB configuration

Bit	Attr	Reset Value	Description
31:30	RW	0x0	luma_spat_sel 3D denoise luma spatial coefficient select
29:28	RW	0x0	luma_temp_sel 3D denoise luma temporal coefficient select
27:26	RW	0x0	chroma_spat_sel 3D denoise chroma spatial coefficient select
25:24	RW	0x0	chroma_temp_sel 3D denoise chroma temporal coefficient select
23:16	RW	0x00	enh_threshold enhancement threshold In denoise and detail enhancement operation, more than the threshold, considering as detail; but if less than the threshold, considering as noise, need to to be filtered.
15	RO	0x0	reserved

Bit	Attr	Reset Value	Description
14:8	RW	0x00	enh_alpha enhancement alpha value 0000000:0 0000001:1/16 0000010:2/16 0001111:15/16 0010000:1 0010001:1+1/16; 0010010:1+2/16; 0010011:1+3/16; 0100000:2; 0110000:3; 1000000:4; 1010000:5; 1100000:6; other : reserved
7:2	RO	0x0	reserved
1:0	RW	0x0	enh_radius enhancement radius 00:R=1 01:R=2 10:R=3 11:R=4

IEP_ENH_C_COE

Address: Operational Base + offset (0x00050)

rgb color enhancement coefficient

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6:5	RW	0x0	c_int_coe color enhancement integer coefficient
4:0	RW	0x00	c_frac_coe color enhancement fraction coefficient

IEP_RAW_CONFIG0

Address: Operational Base + offset (0x00058)

configuration register0

Bit	Attr	Reset Value	Description
31	RW	0x0	vrt_inv vertical inverse display 0:normal display 1:inverse display
30	RW	0x0	hrz_inv horizontal inverse display 0:normal display 1:inverse display
29	RO	0x0	reserved
28	RW	0x0	scl_en image scaling enable 0:disable 1:enable
27:26	RW	0x0	scl_sel Scaling select 00: horizontal down-scaling & vertical down-scaling; 01: horizontal down-scaling & vertical up-scaling; 10: horizontal up-scaling & vertical down-scaling; 11: horizontal up-scaling & vertical up-scaling;
25:24	RW	0x0	scl_up_coe_sel scale up coefficient select 00:hermite 01:spline 10:catrom 11:mitchell
23	RW	0x0	dil_ei_sel deinterlace edge interpolation select
22:21	RW	0x0	dil_ei_radius deinterlace edge interpolation radius
20	RW	0x0	rgb_con_gam_order RGB contrast enhancement and gamma adjustment operation order select. 0:CG prior to DDE 1:DDE prior to CG (CG represent for contrast & gamma operation, and DDE represent for denoise, detail or edge enhancement operation)

Bit	Attr	Reset Value	Description
19:18	RW	0x0	rgb_enh_sel RGB enhancement select 00: no operation 01: denoise 10: detail enhancement 11: edge enhancement
17	RW	0x0	rgb_con_gam_en RGB contrast enhancement and gamma adjustment enable 0:disable 1:enable
16	RW	0x0	rgb_color_enh_en RGB color enhancement enable 0:disable 1:enable
15	RW	0x0	dil_ei_smooth deinterlace edge interpolation for smooth effect 0: disable 1: enable
14	RW	0x0	yuv_enh_en yuv enhancement enable 0:disable 1:enable
13	RW	0x0	yuv_dns_en YUV 3D denoise enable 0:disable 1:enable
12	RW	0x0	dil_ei_mode deinterlace edge interpolation 0: disable 1: enable
11	RW	0x0	dil_hf_en deinterlace high frequency calculation enable 0: disable 1: enable

Bit	Attr	Reset Value	Description
10:8	RW	0x0	dil_mode Deinterlace mode select: 000: YUV deinterlace and bypass path disable; 001: I4O2 mode 010: I4O1B mode 011: I4O1T mode 100: I2O1B mode 101: I2O1T mode 110: bypass mode
7:1	RW	0x00	dil_hf_fct deinterlace high frequency factor
0	RW	0x0	vop_path_en VOP direct path enable 0:disable 1:enable

IEP_RAW_CONFIG1

Address: Operational Base + offset (0x0005c)
configuration register1

Bit	Attr	Reset Value	Description
31:24	RO	0x00	glb_alpha global alpha value only valid when destination format is ARGB
23	RO	0x0	rgb2yuv_input_clip RGB to YUV input range 0:R/G/B=[0,255] 1:R/G/B=[16,235]
22	RO	0x0	yuv2rgb_input_clip YUV to RGB input range 0:Y/U/V=[0,255] 1:Y=[16,235],U/V=[16,240]
21	RO	0x0	rgb_to_yuv_en RGB to YUV conversion enable 0: disable 1: enable
20	RO	0x0	yuv_to_rgb_en YUV to RGB conversion enable 0: disable 1: enable

Bit	Attr	Reset Value	Description
19:18	RO	0x0	rgb2yuv_coe_sel rgb2yuv coefficient select 00:bt601_1 01:bt601_f 10:bt709_1 11:bt709_f
17:16	RO	0x0	yuv2rgb_coe_sel yuv2rgb coefficient select 00:bt601_1 01:bt601_f 10:bt709_1 11:bt709_f
15	RO	0x0	dthr_down_en dither down enable 0: disable 1: enable
14	RO	0x0	dthr_up_en dither up enable 0: disable 1: enable
13:12	RO	0x0	dst_yuv_swap destination YUV swap 00:SP UV 01:SP VU 10, 11:P
11:10	RO	0x0	dst_rgb_swap destination RGB swap ARGB destination 00:ARGB 01:ABGR 10:RGBA 11:BGRA RGB565 destination 00,10:RGB 01,11:BGR
9:8	RO	0x0	dst_fmt Output image Format 00 : ARGB 01 : RGB565 10 : YUV422 11 : YUV420
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:4	RO	0x0	src_yuv_swap source YUV swap 00:SP UV 01:SP VU 10, 11:P
3:2	RO	0x0	src_rgb_swap source RGB swap XRGB source 00:XRGB 01:XBGR 10:RGBX 11:BGRX RGB565 source 00,10:RGB 01,11:BGR
1:0	RO	0x0	src_fmt Input image Format 00 : XRGB 01 : RGB565 10 : YUV422 11 : YUV420

IEP_RAW_VIR_IMG_WIDTH

Address: Operational Base + offset (0x00060)

Image virtual width

Bit	Attr	Reset Value	Description
31:16	RO	0x0140	dst_vir_image_width Destination virtual image width
15:0	RO	0x0140	src_vir_image_width Source virtual image width

IEP_RAW_IMG_SCL_FCT

Address: Operational Base + offset (0x00064)

scaling factor

Bit	Attr	Reset Value	Description
-----	------	-------------	-------------

Bit	Attr	Reset Value	Description
31:16	RO	0x2000	vrt_scl_fct Vertical scale factor up scaling: $\text{vrt_scl_fct} = \text{floor}(\text{src_image_height} / \text{dst_image_height});$ down scaling: $\text{vrt_scl_fct} = \text{ceiling}((\text{dst_image_height} + 1) / (\text{src_image_height} + 1));$
15:0	RO	0x2000	hrz_scl_fct Horizontal scale factor up scaling: $\text{hrz_scl_fct} = \text{floor}(\text{src_image_width} / \text{dst_image_width});$ down scaling: $\text{hrz_scl_fct} = \text{ceiling}((\text{dst_image_width} + 1) / (\text{src_image_width} + 1));$

IEP_RAW_SRC_IMG_SIZE

Address: Operational Base + offset (0x00068)

Source image width/height

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RO	0x00f0	src_image_height source image height
15:13	RO	0x0	reserved
12:0	RO	0x0140	src_image_width source image width

IEP_RAW_DST_IMG_SIZE

Address: Operational Base + offset (0x0006c)

Destination image width/height

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RO	0x00f0	dst_image_height Destination image height
15:13	RO	0x0	reserved
12:0	RO	0x0140	dst_image_width Destination image width

IEP_RAW_ENH_YUV_CNFG_0

Address: Operational Base + offset (0x00070)

brightness,contrast,saturation adjustment

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RO	0x000	sat_con YUV saturation and contrast adjustment saturation * contrast range from 0 to 1.992*1.992, and this value is saturation* contrast * 128
15:8	RO	0x00	contrast YUV contrast adjustment contrast value range from 0 to 1.992, and this value is contrast*128.
7:6	RO	0x0	reserved
5:0	RO	0x00	brightness YUV brightness adjustment range from -32 to 31 000000:0; 000001:1; 011111:31; 100000:-32; 100001:-31; 111110:-2; 111111:-1;

IEP_RAW_ENH_YUV_CNFG_1

Address: Operational Base + offset (0x00074)

Hue configuration

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:8	RO	0x00	cos_hue the cos function value for hue adjustment sin function value range from 0.866 to 1 ,and this value is cos * 128 ,no sign bit
7:0	RO	0x00	sin_hue the sin function value for hue adjustment sin function value range from -0.5 to 0.5 ,and this value is sin * 128 ,and the high bit is sign bit

IEP_RAW_ENH_YUV_CNFG_2

Address: Operational Base + offset (0x00078)

color bar configuration

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved

Bit	Attr	Reset Value	Description
25:24	RO	0x0	video_mode video mode 00:black screen 01:blue screen 10:color bars 11:normal video
23:16	RO	0x00	color_bar_v color bar v value
15:8	RO	0x00	color_bar_u color bar u value
7:0	RO	0x00	color_bar_y color bar y value

IEP_RAW_ENH_RGB_CNFG

Address: Operational Base + offset (0x0007c)

enhancement RGB configuration

Bit	Attr	Reset Value	Description
31:30	RW	0x0	luma_spat_sel 3D denoise luma spatial coefficient select
29:28	RW	0x0	luma_temp_sel 3D denoise luma temporal coefficient select
27:26	RW	0x0	chroma_spat_sel 3D denoise chroma spatial coefficient select
25:24	RW	0x0	chroma_temp_sel 3D denoise chroma temporal coefficient select
23:16	RW	0x00	enh_threshold enhancement threshold In denoise and detail enhancement operation, more than the threshold, considering as detail; but if less than the threshold, considering as noise, need to to be filtered.
15	RO	0x0	reserved

Bit	Attr	Reset Value	Description
14:8	RW	0x00	enh_alpha enhancement alpha value 0000000:0 0000001:1/16 0000010:2/16 0001111:15/16 0010000:1 0010001:1+1/16; 0010010:1+2/16; 0010011:1+3/16; 0100000:2; 0110000:3; 1000000:4; 1010000:5; 1100000:6; other : reserved
7:2	RO	0x0	reserved
1:0	RW	0x0	enh_radius enhancement radius 00:R=1 01:R=2 10:R=3 11:R=4

IEP_SRC_ADDR_YRGB

Address: Operational Base + offset (0x00080)

Start address of source image(Y/RGB)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_image_yrgb_mst Source image data YRGB start address in Memory

IEP_SRC_ADDR_CBCR

Address: Operational Base + offset (0x00084)

Start address of source image(Cb/Cr)

Bit	Attr	Reset Value	Description
-----	------	-------------	-------------

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_image_cbcr_mst Source image data CbCr start address in Memory

IEP_SRC_ADDR_CR

Address: Operational Base + offset (0x00088)

Start address of source image(Cr)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_image_cr_mst Source image data Cr start address in Memory

IEP_SRC_ADDR_Y1

Address: Operational Base + offset (0x0008c)

Start address of source image(Y)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_image_y_mst Source image data Y start address in Memory

IEP_SRC_ADDR_CBCR1

Address: Operational Base + offset (0x00090)

Start address of source image(Cb/Cr)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_image_cbcr_mst Source image data CbCr start address in Memory

IEP_SRC_ADDR_CR1

Address: Operational Base + offset (0x00094)

Start address of source image(Cr)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_image_cr_mst Source image data Cr start address in Memory

IEP_SRC_ADDR_Y_ITEMP

Address: Operational Base + offset (0x00098)

Start address of source image(Y integer part)

Bit	Attr	Reset Value	Description
-----	------	-------------	-------------

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_image_y_mst_itemp Interger part source image data Y start address in Memory

IEP_SRC_ADDR_CBCR_ITEMP

Address: Operational Base + offset (0x0009c)

Start address of source image(CBCR integer part)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_image_cbc_r_mst_cbc_r_itemp Interger part source image data CBCR start address in Memory

IEP_SRC_ADDR_CR_ITEMP

Address: Operational Base + offset (0x000a0)

Start address of source image(CR integer part)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_image_cr_mst_cr_itemp Interger part source image data CR start address in Memory

IEP_SRC_ADDR_Y_FTEMP

Address: Operational Base + offset (0x000a4)

Start address of source image(Y fraction part)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_image_y_mst_ftemp Fraction part source image data Y start address in Memory

IEP_SRC_ADDR_CBCR_FTEMP

Address: Operational Base + offset (0x000a8)

Start address of source image(CBCR fraction part)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_image_cbc_r_mst_ftemp Fraction part source image data CBCR start address in Memory

IEP_SRC_ADDR_CR_FTEMP

Address: Operational Base + offset (0x000ac)

Start address of source image(CR fraction part)

Bit	Attr	Reset Value	Description
-----	------	-------------	-------------

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_image_cr_mst_ftemp Fraction part source image data CR start address in Memory

IEP_DST_ADDR_YRGB

Address: Operational Base + offset (0x000b0)

Start address of destination image(Y/RGB)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_image_yrgb_mst Destination image data YRGB start address in Memory

IEP_DST_ADDR_CBCR

Address: Operational Base + offset (0x000b4)

Start address of destination image(Cb/Cr)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_image_cbc_r_mst Destination image data CBCR start address in Memory

IEP_DST_ADDR_CR

Address: Operational Base + offset (0x000b8)

Start address of destination image(Cr)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_image_cr_mst Destination image data CR start address in Memory

IEP_DST_ADDR_Y1

Address: Operational Base + offset (0x000bc)

Start address of destination image(Y)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_image_y_mst Destination image data Y start address in Memory

IEP_DST_ADDR_CBCR1

Address: Operational Base + offset (0x000c0)

Start address of destination image(Cb/Cr)

Bit	Attr	Reset Value	Description
-----	------	-------------	-------------

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_image_cbcr_mst Destination image data CbCr start address in Memory

IEP_DST_ADDR_CR1

Address: Operational Base + offset (0x000c4)

Start address of destination image(Cr)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_image_cr_mst Destination image data Cr start address in Memory

IEP_DST_ADDR_Y_ITEMP

Address: Operational Base + offset (0x000c8)

Start address of destination image(Y integer part)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_image_y_mst_itemp Interger part destination image data Y start address in Memory

IEP_DST_ADDR_CBCR_ITEMP

Address: Operational Base + offset (0x000cc)

Start address of destination image(CBCR integer part)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_image_cbcr_mst_itemp Int part destination image data CBCR start address in Memory

IEP_DST_ADDR_CR_ITEMP

Address: Operational Base + offset (0x000d0)

Start address of destination image(CR integer part)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_image_cr_mst_itemp Interger part destination image data CR start address in Memory

IEP_DST_ADDR_Y_FTEMP

Address: Operational Base + offset (0x000d4)

Start address of destination image(Y fraction part)

Bit	Attr	Reset Value	Description
-----	------	-------------	-------------

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_image_y_mst_ftemp Fraction part destination image data Y start address in Memory

IEP_DST_ADDR_CBCR_FTEMP

Address: Operational Base + offset (0x000d8)

Start address of destination image(CBCR fraction part)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_image_cbc_r_mst_ftemp Fraction part destination image data CBCR start address in Mem

IEP_DST_ADDR_CR_FTEMP

Address: Operational Base + offset (0x000dc)

Start address of destination image(CR fraction part)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_image_cr_mst_ftemp Fraction part destination image data CR start address

IEP_DIL_MTN_TAB0

Address: Operational Base + offset (0x000e0)

Deinterlace motion table0

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	mtn_sub_tab3 motion sub table3
23	RO	0x0	reserved
22:16	RW	0x00	mtn_sub_tab2 motion sub table2
15	RO	0x0	reserved
14:8	RW	0x00	mtn_sub_tab1 motion sub table1
7	RO	0x0	reserved
6:0	RW	0x00	mtn_sub_tab0 motion sub table0

IEP_DIL_MTN_TAB1

Address: Operational Base + offset (0x000e4)

Deinterlace motion table1

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	mtn_sub_tab3 motion sub table3
23	RO	0x0	reserved
22:16	RW	0x00	mtn_sub_tab2 motion sub table2
15	RO	0x0	reserved
14:8	RW	0x00	mtn_sub_tab1 motion sub table1
7	RO	0x0	reserved
6:0	RW	0x00	mtn_sub_tab0 motion sub table0

IEP_DIL_MTN_TAB2

Address: Operational Base + offset (0x000e8)

Deinterlace motion table2

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	mtn_sub_tab3 motion sub table3
23	RO	0x0	reserved
22:16	RW	0x00	mtn_sub_tab2 motion sub table2
15	RO	0x0	reserved
14:8	RW	0x00	mtn_sub_tab1 motion sub table1
7	RO	0x0	reserved
6:0	RW	0x00	mtn_sub_tab0 motion sub table0

IEP_DIL_MTN_TAB3

Address: Operational Base + offset (0x000ec)

Deinterlace motion table3

Bit	Attr	Reset Value	Description
-----	------	-------------	-------------

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	mtn_sub_tab3 motion sub table3
23	RO	0x0	reserved
22:16	RW	0x00	mtn_sub_tab2 motion sub table2
15	RO	0x0	reserved
14:8	RW	0x00	mtn_sub_tab1 motion sub table1
7	RO	0x0	reserved
6:0	RW	0x00	mtn_sub_tab0 motion sub table0

IEP_DIL_MTN_TAB4

Address: Operational Base + offset (0x000f0)

Deinterlace motion table4

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	mtn_sub_tab3 motion sub table3
23	RO	0x0	reserved
22:16	RW	0x00	mtn_sub_tab2 motion sub table2
15	RO	0x0	reserved
14:8	RW	0x00	mtn_sub_tab1 motion sub table1
7	RO	0x0	reserved
6:0	RW	0x00	mtn_sub_tab0 motion sub table0

IEP_DIL_MTN_TAB5

Address: Operational Base + offset (0x000f4)

Deinterlace motion table5

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

Bit	Attr	Reset Value	Description
30:24	RW	0x00	mtn_sub_tab3 motion sub table3
23	RO	0x0	reserved
22:16	RW	0x00	mtn_sub_tab2 motion sub table2
15	RO	0x0	reserved
14:8	RW	0x00	mtn_sub_tab1 motion sub table1
7	RO	0x0	reserved
6:0	RW	0x00	mtn_sub_tab0 motion sub table0

IEP_DIL_MTN_TAB6

Address: Operational Base + offset (0x000f8)

Deinterlace motion table6

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	mtn_sub_tab3 motion sub table3
23	RO	0x0	reserved
22:16	RW	0x00	mtn_sub_tab2 motion sub table2
15	RO	0x0	reserved
14:8	RW	0x00	mtn_sub_tab1 motion sub table1
7	RO	0x0	reserved
6:0	RW	0x00	mtn_sub_tab0 motion sub table0

IEP_DIL_MTN_TAB7

Address: Operational Base + offset (0x000fc)

Deinterlace motion table7

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	mtn_sub_tab3 motion sub table3

Bit	Attr	Reset Value	Description
23	RO	0x0	reserved
22:16	RW	0x00	mtn_sub_tab2 motion sub table2
15	RO	0x0	reserved
14:8	RW	0x00	mtn_sub_tab1 motion sub table1
7	RO	0x0	reserved
6:0	RW	0x00	mtn_sub_tab0 motion sub table0

IEP_ENH_CG_TAB

Address: Operational Base + offset (0x00100)
contrast and gamma enhancement table

Bit	Attr	Reset Value	Description
31:24	RW	0x00	cg_tab_3 cg table 3 pixel value 3,7,11,15,.....mapping
23:16	RW	0x00	cg_tab_2 cg table 2 pixel value 2,6,10,14,.....mapping
15:8	RW	0x00	cg_tab_1 cg table 1 pixel value 1,5,9,13,.....mapping
7:0	RW	0x00	cg_tab_0 cg table 0 256x8bit contrast & gamma mapping table pixel value 0,4,8,12,.....mapping

IEP_ENH_DDE_COE0

Address: Operational Base + offset (0x00400)
denoise,detail and edge enhancement coefficient

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	dde_coe_3 dde coefficient 3 coefficient number 3,7,11,15,.....
23:22	RO	0x0	reserved
21:16	RW	0x00	dde_coe_2 dde coefficient 2 coefficient number 2,6,10,14,.....
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:8	RW	0x00	dde_coe_1 dde coefficient 1 coefficient number 1,5,9,13,.....
7:6	RO	0x0	reserved
5:0	RW	0x00	dde_coe_0 dde coefficient 0 256x6bit coefficient for denoise and detail enhancement coefficient number 0,4,8,12,.....

IEP_ENH_DDE_COE1

Address: Operational Base + offset (0x00500)

denoise,detail and edge enhancement coefficient

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	dde_coe_3 dde coefficient 3 coefficient number 3,7,11,15,.....
23:22	RO	0x0	reserved
21:16	RW	0x00	dde_coe_2 dde coefficient 3 coefficient number 2,6,10,14,.....
15:14	RO	0x0	reserved
13:8	RW	0x00	dde_coe_1 dde coefficient 1 coefficient number 1,5,9,13,.....
7:6	RO	0x0	reserved
5:0	RW	0x00	dde_coe_0 dde coefficient 1 81x6bit coefficient for denoise and detail enhancement coefficient number 0,4,8,12,.....

IEP_MMU_DTE_ADDR

Address: Operational Base + offset (0x00800)

MMU current page table address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_dte_addr page table address

IEP_MMU_STATUS

Address: Operational Base + offset (0x00804)

MMU status register

Bit	Attr	Reset Value	Description
-----	------	-------------	-------------

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:6	RW	0x00	mmu_page_fault_bus_id Index of master responsible for the last page fault
5	RW	0x0	mmu_page_fault_is_write The direction of access for last page fault: 0: read 1:write
4	RW	0x1	mmu_replay_buffer_empty The MMU replay buffer is empty.
3	RW	0x1	mmu_idle the MMU is idle when accesses are being translated and there are no unfinished translated access. The MMU_IDLE signal only reports idle when the MMU processor is idle and accesses are active on the external bus. Note: the MMU can be idle in page fault mode.
2	RW	0x0	mmu_stall_active MMU stall mode currently enabled. The mode is enabled by command.
1	RW	0x0	mmu_page_fault_active MMU page fault mode currently enabled.The mode is enabled by command
0	RW	0x0	mmu_paging_enabled mmu paging is enabled

IEP_MMU_CMD

Address: Operational Base + offset (0x00808)

MMU command register

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved

Bit	Attr	Reset Value	Description
2:0	RW	0x0	mmu_cmd 0: MMU_ENABLE_PAGING. enable paging. 1: MMU_DISABLE_PAGING. disable paging. 2: MMU_ENABLE_STALL. turn on stall mode. 3: MMU_DISABLE_STALL. turn off stall mode. 4: MMU_ZAP_CACHE. zap the entire page table cache. 5: MMU_PAGE_FAULT_DONE. leave page fault mode. 6: MMU_FORCE_RESET. reset the mmu. The MMU_ENABLE_STALL command can always be issued. Other commands are ignored unless the MMU is idle or stalled.

IEP_MMU_PAGE_FAULT_ADDR

Address: Operational Base + offset (0x0080c)
 MMU logic address of last page fault

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_page_fault_addr address of last page fault

IEP_MMU_ZAP_ONE_LINE

Address: Operational Base + offset (0x00810)
 MMU zap cache line register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	mmu_zap_one_line address to be invalidated from the page table cache.

IEP_MMU_INT_RAWSTAT

Address: Operational Base + offset (0x00814)
 MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	read_bus_error read bus error
0	RW	0x0	page_fault page fault

IEP_MMU_INT_CLEAR

Address: Operational Base + offset (0x00818)

MMU interrupt clear register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	read_bus_error_clear read bus error interrupt clear. write 1 to this register can clear read bus error interrupt.
0	RW	0x0	page_fault_clear page fault interrupt clear, write 1 to this register can clear page fault interrupt.

IEP_MMU_INT_MASK

Address: Operational Base + offset (0x0081c)

MMU interrupt mask register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	read_bus_error_int_en read bus error interrupt enable
0	RW	0x0	page_fault_int_en page fault interrupt enable

IEP_MMU_INT_STATUS

Address: Operational Base + offset (0x00820)

MMU interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	read_bus_error read bus error interrupt
0	RW	0x0	page_fault page fault interrupt

IEP_MMU_AUTO_GATING

Address: Operational Base + offset (0x00824)

MMU clock auto gating register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x1	mmu_auto_gating mmu clock auto gating when it is 1, the mmu will auto gating itself

29.5 Application Notes

29.5.1 VOP path disabled configure flow

1. Keep IEP direct path disabled.
2. Configure all registers which are needed at any time.
3. Configure IEP_CONFIG_DONE.
4. Configure IEP_FRM_START.

29.5.2 VOP path enabled configure flow

1. Keep IEP direct path enabled.
2. Configure all IEP registers which are needed.
3. Configure VOP related registers which are needed.
4. Configure CONFIG_DONE register in VOP only.
5. Wait for frame start from VOP and IEP direct path.

29.5.3 VOP path turn on flow

1. Configure all IEP registers which are needed.
2. Configure VOP related registers which are needed.
3. Enable IEP direct path.
4. Enable VOP direct path.
5. Configure CONFIG_DONE register in VOP only.
6. Wait for frame start from VOP and IEP direct path.

29.5.4 VOP path turn off flow

1. Disable VOP direct path.
2. Disable IEP direct path, so IEP do not receive any other CONFIG_DONE and frame start from VOP immediately.
3. Configure CONFIG_DONE register in VOP.
4. Wait for frame start from VOP and IEP direct path, so VOP quit direct path mode completely.
5. Configure IEP registers which are needed at any time.
6. Configure IEP_CONFIG_DONE.
7. Configure IEP_FRM_START, IEP is working at write back mode now.