

Chapter 36 MIPI CSI-2 Host Controller

36.1 Overview

The CSI-2 Host Controller implements the CSI-2 protocol on the host side. The CSI-2 link protocol specification is a part of communication protocols defined by MIPI Alliance standards intended for mobile system chip-to-chip communications. The CSI-2 specification is for the image application processor communication in cameras.

The CSI-2 Host Controller is designed to receive data from a CSI-2 compliant camera sensor. A D-PHY configured as a Slave acts as the physical layer.

The MIPI CSI-2 Host Controller supports the following features:

- Compliant with MIPI Alliance Specification for CSI-2, Version 1.01.00-9 November 2010
- Interface with MIPI D-PHY following PHY Protocol Interface, as defined in MIPI Alliance Specification for D-PHY, Version 1.1-7 November 2011
- Up to four D-PHY RX data lanes
- Dynamically configurable multi-lane merging
- Long and Short packet decoding
- Timing accurate signaling of Frame and Line synchronization packets
- Several Frame formats
 - General Frame or Digital Interlaced Video with or without accurate sync timing
 - Data Type (Packet or Frame Level) and Virtual Channel interleaving
- 32-bit Image Data Interface delivering data formatted as recommended in CSI-2 Specification
- All primary and secondary data formats
 - RGB, YUV, and RAW color space definitions
 - From 24-bit down to 6-bit per pixel
 - Generic or user-defined byte-based data types
- Error detection and correction
 - PHY level
 - Packet level
 - Line level
 - Frame level

36.2 Block Diagram

The following diagram shows the MIPI CSI-2 Host Controller architecture.

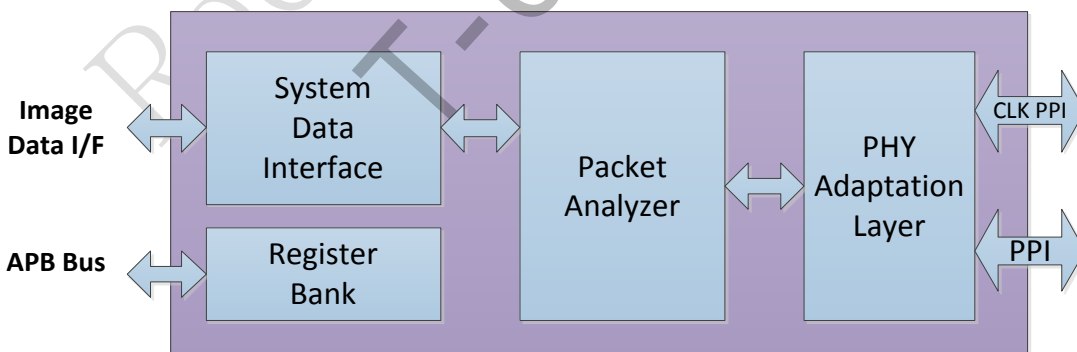


Fig. 36-1 MIPI CSI-2 Host Controller architecture

PHY Adaptation Layer: Manages the D-PHY PPI interface

Packet Analyzer: Merges the data from the different lanes

Image Data Interface: Reorders pixels into 32-bit data for memory storage and generates

timing accurate video synchronization signals

AMBA-APB Register Bank: Provides access to configuration and control registers

36.3 Function Description

36.3.1 Supported Resolutions and Frame Rates

The CSI-2 specification does not define the supported standard resolutions or frame rates. Camera sensor resolution, blanking periods, synchronization events, frame rates, and pixel color depth play a fundamental role in the required bandwidth. All these variables make it difficult to define a standard procedure to estimate the minimum lane rate and the minimum number of lanes that support a specific CSI-2 device.

Table 37-1 presents some predefined and supported camera settings, assuming the following:

- Clock lane frequency is 500 MHz or 750 MHz that results in a bandwidth of 1 Gbps or 1.5 Gbps respectively, for each data lane.
- No significant control/reserved traffic is present on the link when pixel data is being transmitted.

The last column of Table 37-1 presents the minimum number of lanes required for each configuration.

Table 36-1 Supported Camera Settings

Mega Pixels	Mega Pixels with Overhead	Refresh Rate (Hz)	Color Depth (bpp)	CSI2 BW (Mbits)	D-PHY at 1 Gbps Number of Lanes	D-PHY at 1.5Gbps Number of Lanes
2MP	2560000	15	24	922	1	1
2MP	2560000	30	24	1843	2	2
3MP	3840000	15	16	922	1	1
3MP	3840000	30	16	1843	2	2
3MP	3840000	30	24	2765	3	2
5MP	6400000	15	16	1536	2	2
5MP	6400000	15	24	2304	3	2
5MP	6400000	30	16	3072	4	3
8MP	10240000	15	16	2458	3	2
8MP	10240000	15	24	3686	4	3
8MP	10240000	30	12	3686	4	3
12MP	15360000	15	12	2765	3	2
12MP	15360000	15	16	3686	4	3
14MP	17920000	15	12	3226	4	3
16MP	20480000	15	12	3686	4	3
Video Formats						
1280x720 pixels(720p)	921600	30	24	664	1	1
1280x720 pixels(720p)	921600	60	24	1327	2	1
1920x1080 pixels(1080p)	2073600	60	24	2986	3	2

36.3.2 Error Detection

The CSI-2 Host Controller analyzes the received packets and determines if there are protocol errors. It is possible to monitor the following errors:

- Frame errors such as incorrect Frame sequence, reception of a CRC error in the most recent frame, and the mismatch between Frame Start and Frame End
- Line errors such as incorrect line sequence and mismatch between Line Start and Line End
- Packet errors such as ECC or CRC mismatch
- D-PHY errors such as synchronization pattern mismatch

Table 37-2 shows all the errors that CSI-2 Host Controller can identify.

Table 36-2 Errors Identified by the CSI-2 Host Controller

Error	Description	Level	Action
-------	-------------	-------	--------

phy_errsotsynchs_*	Start of transmission error on data lane* with no synchronization achieved	PHY	Packets with this error are not delivered in IDI interface
phy_erresc_*	Escape entry error (ULPM) on data lane*	PHY	Informative only. Error is acknowledged in the register and the interrupt pin is raised.
phy_errsoths_*	Start of transmission error on data lane* but synchronization can still be achieved	PHY	Informative only since PHY can recover from this error. Error is acknowledged in register and the interrupt pin is raised.
vc*_err_crc	Checksum error detected on virtual channel*	Packet	Informative only. Error is acknowledged in the register and Interrupt pin is raised.
vc*_err_crc	Header ECC contains one error detected on virtual channel*	Packet	Informative only since controller can recover the correct header. Error is acknowledged in the register and the interrupt pin is raised.
err_ecc_double	Header ECC contains two errors. Unrecoverable.	Packet	Packets with this error are not delivered in IDI.s
err_id_vc*	Unrecognized or unimplemented data type detected in virtual channel*	Packet	Informative only. Error is acknowledged in the register and the interrupt pin is raised
err_f_bndry_match_vc*	Error matching Frame Start with Frame End for virtual channel*	Frame	Informative only. Error is acknowledged in register and the interrupt pin is raised if not masked.
err_f_seq_vc*	Incorrect Frame Sequence detected in virtual channel*	Frame	Informative only. Error is acknowledged in register and the interrupt pin is raised if not masked.
err_frame_data_vc*	Last received frame, in virtual channel*, had at least one CRC error	Frame	Informative only. Error is acknowledged in the register and the interrupt pin is raised.

36.4 Register Description

This section describes the control/status registers of the design.

36.4.1 Register Summary

Name	Offset	Size	Reset Value	Description
CSIHOST_VERSION	0x0000	W	0x00000000	Version of the CSI2 Host
CSIHOST_N_LANES	0x0004	W	0x00000001	Number of active data lanes
CSIHOST_PHY_SHUT DOWNZ	0x0008	W	0x00000000	PHY shutdown control
CSIHOST_DPHY_RST Z	0x000c	W	0x00000000	DPHY reset control
CSIHOST_CSI2_RES ETN	0x0010	W	0x00000000	CSI-2 Controller reset
CSIHOST_PHY_STAT E	0x0014	W	0x00000000	General settings for all blocks
CSIHOST_ERR1	0x0020	W	0x00000000	Error state register 1
CSIHOST_ERR2	0x0024	W	0x00000000	Error state register 2
CSIHOST_MSK1	0x0028	W	0x00000000	Masks for errors 1
CSIHOST_MSK2	0x002c	W	0x00000000	Masks for errors 2
CSIHOST_PHY_TEST _CTRL0	0x0030	W	0x00000000	D-PHY test interface control 0

Name	Offset	Size	Reset Value	Description
CSIHOST_PHY_TEST_CTRL1	0x0034	W	0x00000000	D-PHY test interface control 1

Notes: **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access

36.4.2 Detail Register Description

CSIHOST_VERSION

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	VERSION Version of the mipi csi2 host

CSIHOST_N_LANES

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1:0	RW	0x1	N_LANES Number of active data lanes 00: 1 data lane (lane 0) 01: 2 data lanes (lanes 0 and 1) 10: 3 data lanes (lanes 0, 1, and 2) 11: 4 data lanes (All) Can only be updated when the D-PHY lane is in Stop state.

CSIHOST_PHY_SHUTDOWNZ

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	PHY_SHUTDOWNZ D-PHY shutdown input. active low

CSIHOST_DPHY_RSTZ

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	DPHY_RSTZ D-PHY reset output. active low

CSIHOST_CSI2_RESETN

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	CSI2_RESETN CSI-2 controller reset output. active low

CSIHOST_PHY_STATE

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10	RO	0x0	PHY_STOPSTATECLK Clock lane in stop state
9	RO	0x0	PHY_RXULPSCLKNOT This signal indicates that the clock lane module has entered the Ultra Low Power state, active low
8	RO	0x0	PHY_RXCLKACTIVEHS Indicates that the clock lane is actively receiving a DDR clock
7	RO	0x0	PHY_STOPSTATEDATA_3 Data lane 3 in stop state
6	RO	0x0	PHY_STOPSTATEDATA_2 Data lane 2 in stop state
5	RO	0x0	PHY_STOPSTATEDATA_1 Data lane 1 in stop state
4	RO	0x0	PHY_STOPSTATEDATA_0 Data lane 0 in stop state
3	RO	0x0	PHY_RXULPSESC_3 lane module 3 has entered the Ultra Low Power mode
2	RO	0x0	PHY_RXULPSESC_2 lane module 2 has entered the Ultra Low Power mode
1	RO	0x0	PHY_RXULPSESC_1 lane module 1 has entered the Ultra Low Power mode
0	RO	0x0	PHY_RXULPSESC_0 lane module 0 has entered the Ultra Low Power mode

CSIHOST_ERR1

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RO	0x0	err_ecc_double Header ECC contains 2 errors, unrecoverable
27	RO	0x0	vc3_err_crc Checksum error detected on virtual channel 3
26	RO	0x0	vc2_err_crc Checksum error detected on virtual channel 2
25	RO	0x0	vc1_err_crc Checksum error detected on virtual channel 1
24	RO	0x0	vc0_err_crc Checksum error detected on virtual channel 0

Bit	Attr	Reset Value	Description
23	RO	0x0	err_l_seq_di3 Error in the sequence of lines for vc3 and dt3
22	RO	0x0	err_l_seq_di2 Error in the sequence of lines for vc2 and dt2
21	RO	0x0	err_l_seq_di1 Error in the sequence of lines for vc1 and dt1
20	RO	0x0	err_l_seq_di0 Error in the sequence of lines for vc0 and dt0
19	RO	0x0	err_l_bndry_match_di3 Error matching line start with line end for vc3 and dt3
18	RO	0x0	err_l_bndry_match_di2 Error matching line start with line end for vc2 and dt2
17	RO	0x0	err_l_bndry_match_di1 Error matching line start with line end for vc1 and dt1
16	RO	0x0	err_l_bndry_match_di0 Error matching line start with line end for vc0 and dt0
15	RO	0x0	err_frame_data_vc3 Last received frame, in virtual channel 3, had at least one CRC error
14	RO	0x0	err_frame_data_vc2 Last received frame, in virtual channel 2 had at least one CRC error
13	RO	0x0	err_frame_data_vc1 Last received frame, in virtual channel 1, had at least one CRC error
12	RO	0x0	err_frame_data_vc0 Last received frame, in virtual channel 0, had at least one CRC error
11	RO	0x0	err_f_seq_vc3 Error in the sequence of lines for vc3 and dt3
10	RO	0x0	err_f_seq_vc2 Error in the sequence of lines for vc2 and dt2
9	RO	0x0	err_f_seq_vc1 Error in the sequence of lines for vc1 and dt1
8	RO	0x0	err_f_seq_vc0 Error in the sequence of lines for vc0 and dt0
7	RO	0x0	err_f_bndry_match_vc3 Error matching frame start with frame end for virtual channel 3

Bit	Attr	Reset Value	Description
6	RO	0x0	err_f_bndry_match_vc2 Error matching frame start with frame end for virtual channel 2
5	RO	0x0	err_f_bndry_match_vc1 Error matching frame start with frame end for virtual channel 1
4	RO	0x0	err_f_bndry_match_vc0 Error matching frame start with frame end for virtual channel 0
3	RO	0x0	phy_errsotsynchs_3 Start of transmission error on data lane 3(no synchronization achieved)
2	RO	0x0	phy_errsotsynchs_2 Start of transmission error on data lane 2 (no synchronization achieved)
1	RO	0x0	phy_errsotsynchs_1 Start of transmission error on data lane 1 (no synchronization achieved)
0	RO	0x0	phy_errsotsynchs_0 Start of transmission error on data lane 0 (no synchronization achieved)

CSIHOST_ERR2

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23	RO	0x0	err_l_seq_di7 Error in the sequence of lines for vc7 and dt7
22	RO	0x0	err_l_seq_di6 Error in the sequence of lines for vc6 and dt6
21	RO	0x0	err_l_seq_di5 Error in the sequence of lines for vc5 and dt5
20	RO	0x0	err_l_seq_di4 Error in the sequence of lines for vc4 and dt4
19	RO	0x0	err_l_bndry_match_di7 Error matching line start with line end for vc7 and dt7
18	RO	0x0	err_l_bndry_match_di6 Error matching line start with line end for vc6 and dt6
17	RO	0x0	err_l_bndry_match_di5 Error matching line start with line end for vc5 and dt5
16	RO	0x0	err_l_bndry_match_di4 Error matching line start with line end for vc4 and dt4

Bit	Attr	Reset Value	Description
15	RO	0x0	err_id_vc3 Unrecognized or unimplemented data type detected in virtual channel 3
14	RO	0x0	err_id_vc2 Unrecognized or unimplemented data type detected in virtual channel 2
13	RO	0x0	err_id_vc1 Unrecognized or unimplemented data type detected in virtual channel 1
12	RO	0x0	err_id_vc0 Unrecognized or unimplemented data type detected in virtual channel 0
11	RO	0x0	vc3_err_ecc_corrected Header error detected and corrected on virtual channel 3
10	RO	0x0	vc2_err_ecc_corrected Header error detected and corrected on virtual channel 2
9	RO	0x0	vc1_err_ecc_corrected Header error detected and corrected on virtual channel 1
8	RO	0x0	vc0_err_ecc_corrected Header error detected and corrected on virtual channel 0
7	RO	0x0	phy_errsoths_3 Start of transmission error on data lane 3 (synchronization can still be achieved)
6	RO	0x0	phy_errsoths_2 Start of transmission error on data lane 2 (synchronization can still be achieved)
5	RO	0x0	phy_errsoths_1 Start of transmission error on data lane 1 (synchronization can still be achieved)
4	RO	0x0	phy_errsoths_0 Start of transmission error on data lane 0 (synchronization can still be achieved)
3	RO	0x0	phy_erresc_3 Escape entry error (ULPM) on data lane 3
2	RO	0x0	phy_erresc_2 Escape entry error (ULPM) on data lane 2
1	RO	0x0	phy_erresc_1 Escape entry error (ULPM) on data lane 1
0	RO	0x0	phy_erresc_0 Escape entry error (ULPM) on data lane 0

CSIHOST_MSK1

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	mask_err_ecc_double Mask for err_ecc_double
27	RW	0x0	mask_vc3_err_crc Mask for vc3_err_crc
26	RW	0x0	mask_vc2_err_crc Mask for vc2_err_crc
25	RW	0x0	mask_vc1_err_crc Mask for vc1_err_crc
24	RW	0x0	mask_vc0_err_crc Mask for vc0_err_crc
23	RW	0x0	mask_err_l_seq_di3 Mask fro err_l_seq_di3
22	RW	0x0	mask_err_l_seq_di2 Mask fro err_l_seq_di2
21	RW	0x0	mask_err_l_seq_di1 Mask fro err_l_seq_di1
20	RW	0x0	mask_err_l_seq_di0 Mask fro err_l_seq_di0
19	RW	0x0	mask_err_l_bndry_match_di3 Mask for err_I_bndry_match_di3
18	RW	0x0	mask_err_l_bndry_match_di2 Mask for err_I_bndry_match_di2
17	RW	0x0	mask_err_l_bndry_match_di1 Mask for err_I_bndry_match_di1
16	RW	0x0	mask_err_l_bndry_match_di0 Mask for err_I_bndry_match_di0
15	RW	0x0	mask_err_frame_data_vc3 Mask for err_frame_data_vc3
14	RW	0x0	mask_err_frame_data_vc2 Mask for err_frame_data_vc2
13	RW	0x0	mask_err_frame_data_vc1 Mask for err_frame_data_vc1
12	RW	0x0	mask_err_frame_data_vc0 Mask for err_frame_data_vc0
11	RW	0x0	mask_err_f_seq_vc3 Mask for err_f_seq_vc3
10	RW	0x0	mask_err_f_seq_vc2 Mask for err_f_seq_vc2
9	RW	0x0	mask_err_f_seq_vc1 Mask for err_f_seq_vc1
8	RW	0x0	mask_err_f_seq_vc0 Mask for err_f_seq_vc0

Bit	Attr	Reset Value	Description
7	RW	0x0	mask_err_f_bndry_match_vc3 Mask for err_f_bndry_match_vc1
6	RW	0x0	mask_err_f_bndry_match_vc2 Mask for err_f_bndry_match_vc1
5	RW	0x0	mask_err_f_bndry_match_vc1 Mask for err_f_bndry_match_vc1
4	RW	0x0	mask_err_f_bndry_match_vc0 Mask for err_f_bndry_match_vc0
3	RW	0x0	mask_phy_errsotsynchs_3 Mask for phy_errsotsynchs_3
2	RW	0x0	mask_phy_errsotsynchs_2 Mask for phy_errsotsynchs_2
1	RW	0x0	mask_phy_errsotsynchs_1 Mask for phy_errsotsynchs_1
0	RW	0x0	mask_phy_errsotsynchs_0 Mask for phy_errsotsynchs_0

CSIHOST_MSK2

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23	RO	0x0	err_l_seq_di7 Error in the sequence of lines for vc7 and dt7
22	RO	0x0	err_l_seq_di6 Error in the sequence of lines for vc6 and dt6
21	RO	0x0	err_l_seq_di5 Error in the sequence of lines for vc5 and dt5
20	RO	0x0	err_l_seq_di4 Error in the sequence of lines for vc4 and dt4
19	RO	0x0	err_l_bndry_match_di7 Error matching line start with line end for vc7 and dt7
18	RO	0x0	err_l_bndry_match_di6 Error matching line start with line end for vc6 and dt6
17	RO	0x0	err_l_bndry_match_di5 Error matching line start with line end for vc5 and dt5
16	RO	0x0	err_l_bndry_match_di4 Error matching line start with line end for vc4 and dt4
15	RO	0x0	err_id_vc3 Unrecognized or unimplemented data type detected in virtual channel 3

Bit	Attr	Reset Value	Description
14	RO	0x0	err_id_vc2 Unrecognized or unimplemented data type detected in virtual channel 2
13	RO	0x0	err_id_vc1 Unrecognized or unimplemented data type detected in virtual channel 1
12	RO	0x0	err_id_vc0 Unrecognized or unimplemented data type detected in virtual channel 0
11	RO	0x0	vc3_err_ecc_corrected Header error detected and corrected on virtual channel 3
10	RO	0x0	vc2_err_ecc_corrected Header error detected and corrected on virtual channel 2
9	RO	0x0	vc1_err_ecc_corrected Header error detected and corrected on virtual channel 1
8	RO	0x0	vc0_err_ecc_corrected Header error detected and corrected on virtual channel 0
7	RO	0x0	phy_errsoths_3 Start of transmission error on data lane 3 (synchronization can still be achieved)
6	RO	0x0	phy_errsoths_2 Start of transmission error on data lane 2 (synchronization can still be achieved)
5	RO	0x0	phy_errsoths_1 Start of transmission error on data lane 1 (synchronization can still be achieved)
4	RO	0x0	phy_errsoths_0 Start of transmission error on data lane 0 (synchronization can still be achieved)
3	RW	0x0	mask_phy_erresc_3 Mask for phy_erresc_3
2	RW	0x0	mask_phy_erresc_2 Mask for phy_erresc_2
1	RW	0x0	mask_phy_erresc_1 Mask for phy_erresc_1
0	RW	0x0	mask_phy_erresc_0 Mask for phy_erresc_0

CSIHST_PHY_TEST_CTRL0

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1	RW	0x0	phy_testclk D-PHY test interface strobe signal It is used to clock TESTDIN bus into the D-PHY. In conjunction with TESTEN signal controls the operation selection
0	RW	0x0	phy_testclr D-PHY test interface clear It is used when active performs vendor specific interface initialization (active high)

CSIHOST_PHY_TEST_CTRL1

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	RW	0x0	phy_testen D-PHY test interface operation selector: 1: configures address write operation on the falling edge of TESTCLK 0: configures a data write operation on the rising edge of TESTCLK
15:8	RO	0x00	phy_testdout D-PHY output 8-bit data bus for read-back and internal probing functionalities
7:0	RW	0x00	phy_testdin D-PHY test interface input 8-bit data bus for internal register programming and test functionalities access

36.5 Application Notes