Chapter 46 Temperature-Sensor ADC(TS-ADC)

46.1 Overview

TS-ADC Controller module supports user-defined mode and automatic mode. User-defined mode refers, TSADC all the control signals entirely by software writing to register for direct control. Automatic mode refers to the module automatically poll TSADC output, and the results were checked. If you find that the temperature High in a period of time, an interrupt is generated to the processor down-measures taken; if the temperature over a period of time High, the resulting TSHUT gave CRU module, let it reset the entire chip, or via GPIO give PMIC.

TS-ADC Controller supports the following features:

- Support User-Defined Mode and Automatic Mode
- In User-Defined Mode, start_of_conversion can be controlled completely by software, and also can be generated by hardware.
- In Automatic Mode, the temperature of alarm interrupt can be configurable
- In Automatic Mode, the temperature of system reset can be configurable
- Support to 4 channel TS-ADC, the temperature criteria of each channel can be configurable
- In Automatic Mode, the time interval of temperature detection can be configurable
- In Automatic Mode, when detecting a high temperature, the time interval of temperature detection can be configurable
- High temperature debounce can be configurable

46.2 Block Diagram

TS-ADC controller comprises with:

- APB Interface
- TS-ADC control logic

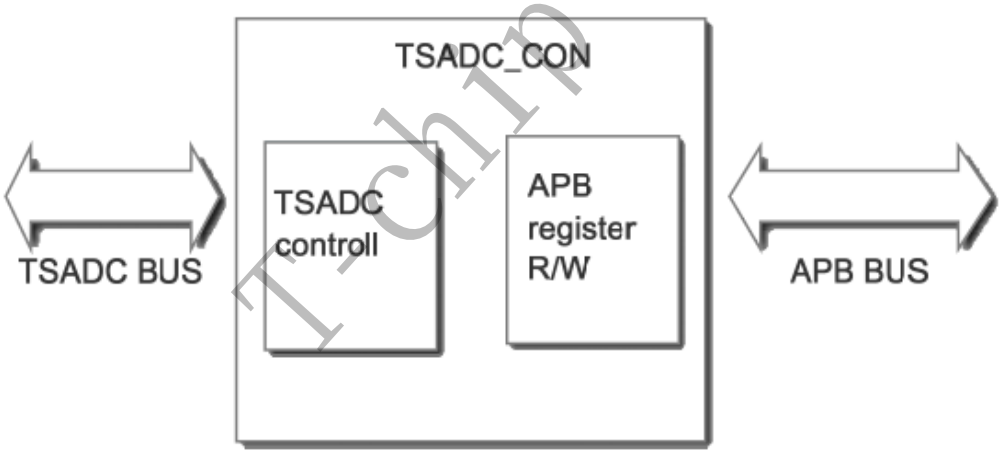

Fig. 46-1 TS-ADC Controller Block Diagram

46.3 Function Description

46.3.1 APB Interface

There is an APB Slave interface in TS-ADC Controller, which is used to configure the TS-ADC Controller registers and look up the temperature from the temperature sensor.

46.3.2 TS-ADC Controller

This block is exploited to realize binary search algorithm, storing the intermediate result and generate control signal for analog block. This block compares the analog input with the voltage generated from D/A Converter, and output the comparison result to SAR and Control Logic Block for binary search. Three level amplifiers are employed in this comparator to provide enough gain.

46.4 Register Description

46.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
TSADC_USER_CON	0x0000	W	0x00000208	The control register of A/D Converter.
TSADC_AUTO_CON	0x0004	W	0x00000000	TSADC auto mode control register
TSADC_INT_EN	0x0008	W	0x00000000	Interrupt enable
TSADC_INT_PD	0x000c	W	0x00000000	Interrupt Status
TSADC_DATA0	0x0020	W	0x00000000	This register contains the data after A/D Conversion.
TSADC_DATA1	0x0024	W	0x00000000	This register contains the data after A/D Conversion.
TSADC_DATA2	0x0028	W	0x00000000	This register contains the data after A/D Conversion.
TSADC_DATA3	0x002c	W	0x00000000	This register contains the data after A/D Conversion.
TSADC_COMP0_INT	0x0030	W	0x00000000	TSADC high temperature level for source 0
TSADC_COMP1_INT	0x0034	W	0x00000000	TSADC high temperature level for source 1
TSADC_COMP2_INT	0x0038	W	0x00000000	TSADC high temperature level for source 2
TSADC_COMP3_INT	0x003c	W	0x00000000	TSADC high temperature level for source 3
TSADC_COMP0_SHUT	0x0040	W	0x00000000	TSADC high temperature level for source 0
TSADC_COMP1_SHUT	0x0044	W	0x00000000	TSADC high temperature level for source 1
TSADC_COMP2_SHUT	0x0048	W	0x00000000	TSADC high temperature level for source 2
TSADC_COMP3_SHUT	0x004c	W	0x00000000	TSADC high temperature level for source 3
TSADC_HIGHT_INT_DEBOUNCE	0x0060	W	0x00000003	high temperature debounce

Name	Offset	Size	Reset Value	Description
TSADC_HIGHT_TSHUT_DEBOUNCE	0x0064	W	0x00000003	high temperature debounce
TSADC_AUTO_PERIOD	0x0068	W	0x00010000	TSADC auto access period
TSADC_AUTO_PERIOD_HT	0x006c	W	0x00010000	TSADC auto access period when temperature is high

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

46.4.2 Detail Register Description

TSADC_USER_CON

Address: Operational Base + offset (0x0000)

The control register of A/D Converter.

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12	RO	0x0	adc_status ADC status (EOC) 0: ADC stop; 1: Conversion in progress.
11:6	RW	0x08	inter_pd_soc interleave between power down and start of conversion
5	RW	0x0	start When software write 1 to this bit , start_of_conversion will be assert. This bit will be cleared after TSADC access finishing.
4	RW	0x0	start_mode start mode. 0: tsadc controller will asert start_of_conversion after "inter_pd_soc" cycles. 1: the start_of_conversion will be controlled by TSADC_USER_CON[5].
3	RW	0x1	adc_power_ctrl ADC power down control bit 0: ADC power down; 1: ADC power up and reset.
2:0	RW	0x0	adc_input_src_sel ADC input source selection(CH_SEL[2:0]). 111 : Input source 0 (SARADC_AIN[0]) 110 : Input source 1 (SARADC_AIN[1]) 101 : Input source 2 (SARADC_AIN[2]) 100 : Input source 3 (SARADC_AIN[3]) Others : Reserved

TSADC_AUTO_CON
Address: Operational Base + offset (0x0004)
TSADC auto mode control register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	last_tshut TSHUT status. This bit will set to 1 when tshut is valid, and only be cleared when application write 1 to it. This bit will not be cleared by system reset.
23:18	RO	0x0	reserved
17	RO	0x0	sample_dly_sel 0: AUTO_PERIOD is used. 1: AUTO_PERIOD_HT is used.
16	RO	0x0	auto_status 0: auto mode stop; 1: auto mode in progress.
15:9	RO	0x0	reserved
8	RW	0x0	tshut polarity 0: low active 1: high active
7	RW	0x0	src3_en 0: do not care the temperature of source 3 1: if the temperature of source 3 is too high , TSHUT will be valid
6	RW	0x0	src2_en 0: do not care the temperature of source 2 1: if the temperature of source 2 is too high , TSHUT will be valid
5	RW	0x0	src1_en 0: do not care the temperature of source 1 1: if the temperature of source 1 is too high , TSHUT will be valid
4	RW	0x0	src0_en 0: do not care the temperature of source 0 1: if the temperature of source 0 is too high , TSHUT will be valid
3:1	RO	0x0	reserved
0	RW	0x0	auto_en 0: TSADC controller works at user-define mode 1: TSADC controller works at auto mode

TSADC_INT_EN
Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12	RW	0x0	eoc_int_en eoc_Interrupt enable. eoc_interrupt enable in user defined mode 0: Disable; 1: Enable
11	RW	0x0	tshut_2cru_en_src3 0: TSHUT output to cru disabled. TSHUT output will always keep low . 1: TSHUT output works.
10	RW	0x0	tshut_2cru_en_src2 0: TSHUT output to cru disabled. TSHUT output will always keep low . 1: TSHUT output works.
9	RW	0x0	tshut_2cru_en_src1 0: TSHUT output to cru disabled. TSHUT output will always keep low . 1: TSHUT output works.
8	RW	0x0	tshut_2cru_en_src0 0: TSHUT output to cru disabled. TSHUT output will always keep low . 1: TSHUT output works.
7	RW	0x0	tshut_2gpio_en_src3 0: TSHUT output to gpio0b2 disabled. TSHUT output will always keep low . 1: TSHUT output works.
6	RW	0x0	tshut_2gpio_en_src2 0: TSHUT output to gpio0b2 disabled. TSHUT output will always keep low . 1: TSHUT output works.
5	RW	0x0	tshut_2gpio_en_src1 0: TSHUT output to gpio0b2 disabled. TSHUT output will always keep low . 1: TSHUT output works.
4	RW	0x0	tshut_2gpio_en_src0 0: TSHUT output to gpio0b2 disabled. TSHUT output will always keep low . 1: TSHUT output works.
3	RW	0x0	ht_inten_src3 high temperature interrupt enable for src3 0: disable 1: enable

Bit	Attr	Reset Value	Description
2	RW	0x0	ht_inten_src2 high temperature interrupt enable for src2 0: disable 1: enable
1	RW	0x0	ht_inten_src1 high temperature interrupt enable for src1 0: disable 1: enable
0	RW	0x0	ht_inten_src0 high temperature interrupt enable for src0 0: disable 1: enable

TSADC_INT_PD
Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8	RW	0x0	eoc_int_pd Interrupt status. This bit will be set to 1 when end-of-conversion. Set 0 to clear the interrupt.
7	RW	0x0	tshut_o_src3 TSHUT output status
6	RW	0x0	tshut_o_src2 TSHUT output status
5	RW	0x0	tshut_o_src1 TSHUT output status
4	RW	0x0	tshut_o_src0 TSHUT output status
3	RW	0x0	ht_irq_src3 When TSADC output is smaller than COMP_INT, this bit will be valid, which means temperature is high, and the application should in charge of this. write 1 to it , this bit will be cleared.
2	RW	0x0	ht_irq_src2 When TSADC output is smaller than COMP_INT, this bit will be valid, which means temperature is high, and the application should in charge of this. write 1 to it , this bit will be cleared.

Bit	Attr	Reset Value	Description
1	RW	0x0	ht_irq_src1 When TSADC output is smaller than COMP_INT, this bit will be valid, which means temperature is high, and the application should in charge of this. write 1 to it , this bit will be cleared.
0	RW	0x0	ht_irq_src0 When TSADC output is smaller than COMP_INT, this bit will be valid, which means temperature is high, and the application should in charge of this. write 1 to it , this bit will be cleared.

TSADC_DATA0
Address: Operational Base + offset (0x0020)
This register contains the data after A/D Conversion.

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RO	0x000	adc_data A/D value of the channel 0 last conversion (DOUT[9:0]).

TSADC_DATA1
Address: Operational Base + offset (0x0024)
This register contains the data after A/D Conversion.

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RO	0x000	adc_data A/D value of the channel 1 last conversion (DOUT[9:0]).

TSADC_DATA2
Address: Operational Base + offset (0x0028)
This register contains the data after A/D Conversion.

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RO	0x000	adc_data A/D value of the channel 2 last conversion (DOUT[9:0]).

TSADC_DATA3
Address: Operational Base + offset (0x002c)
This register contains the data after A/D Conversion.

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RO	0x000	adc_data A/D value of the channel 3 last conversion (DOUT[9:0]).

TSADC_COMP0_INT
Address: Operational Base + offset (0x0030)
TSADC high temperature level for source 0

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	tsadc_comp_src0 TSADC high temperature level. TSADC output is smaller than tsadc_comp, means the temperature is high. TSADC_INT will be valid.

TSADC_COMP1_INT
Address: Operational Base + offset (0x0034)
TSADC high temperature level for source 1

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	tsadc_comp_src1 TSADC high temperature level. TSADC output is smaller than tsadc_comp, means the temperature is high. TSADC_INT will be valid.

TSADC_COMP2_INT
Address: Operational Base + offset (0x0038)
TSADC high temperature level for source 2

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	tsadc_comp_src2 TSADC high temperature level. TSADC output is smaller than tsadc_comp, means the temperature is high. TSADC_INT will be valid.

TSADC_COMP3_INT
Address: Operational Base + offset (0x003c)
TSADC high temperature level for source 3

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	tsadc_comp_src3 TSADC high temperature level. TSADC output is smaller than tsadc_comp, means the temperature is high. TSADC_INT will be valid.

TSADC_COMP0_SHUT
Address: Operational Base + offset (0x0040)
TSADC high temperature level for source 0

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:0	RW	0x000	tsadc_comp_src0 TSADC high temperature level. TSADC output is smaller than tsadc_comp, means the temperature is too high. TSHUT will be valid.

TSADC_COMP1_SHUT
Address: Operational Base + offset (0x0044)
TSADC high temperature level for source 1

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	tsadc_comp_src1 TSADC high temperature level. TSADC output is smaller than tsadc_comp, means the temperature is too high. TSHUT will be valid.

TSADC_COMP2_SHUT
Address: Operational Base + offset (0x0048)
TSADC high temperature level for source 2

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	tsadc_comp_src2 TSADC high temperature level. TSADC output is smaller than tsadc_comp, means the temperature is too high. TSHUT will be valid.

TSADC_COMP3_SHUT
Address: Operational Base + offset (0x004c)
TSADC high temperature level for source 3

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	tsadc_comp_src3 TSADC high temperature level. TSADC output is smaller than tsadc_comp, means the temperature is too high. TSHUT will be valid.

TSADC_HIGHT_INT_DEBOUNCE
Address: Operational Base + offset (0x0060)
high temperature debounce

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x03	debounce TSADC controller will only generate interrupt or TSHUT when temperature is higher than COMP_INT for "debounce" times.

TSADC_HIGHT_TSHUT_DEBOUNCE
Address: Operational Base + offset (0x0064)
high temperature debounce

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x03	debounce TSADC controller will only generate interrupt or TSHUT when temperature is higher than COMP_SHUT for "debounce" times.

TSADC_AUTO_PERIOD
Address: Operational Base + offset (0x0068)
TSADC auto access period

Bit	Attr	Reset Value	Description
31:0	RW	0x00010000	auto_period when auto mode is enabled, this register controls the interleave between every two accessing of TSADC.

TSADC_AUTO_PERIOD_HT
Address: Operational Base + offset (0x006c)
TSADC auto access period when temperature is high

Bit	Attr	Reset Value	Description
31:0	RW	0x00010000	auto_period This register controls the interleave between every two accessing of TSADC after the temperature is higher than COMP_SHUT or COMP_INT

46.5 Application Notes

46.5.1 Channel Select

The system has three Temperature Sensors, channel0 is reserve, and channel 1is for CPU, and channel 2 is for GPU.

46.5.2 Single-sample conversion

To saving power, the TS-ADC used single-sample conversion. The timing as flowing picture:

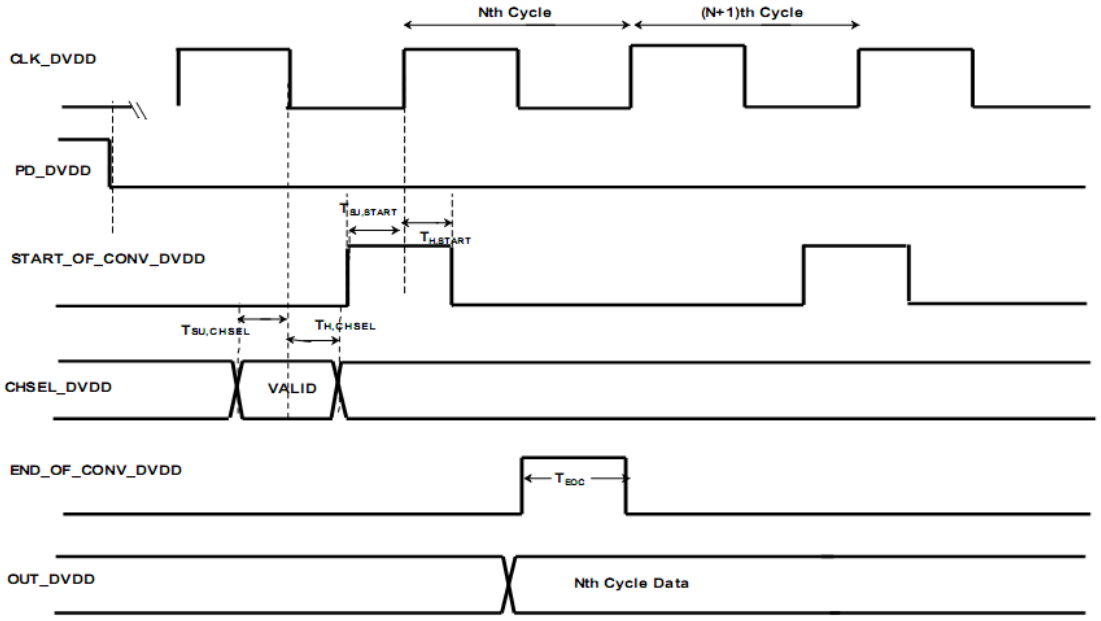

Fig. 46-2 Single-sample conversion

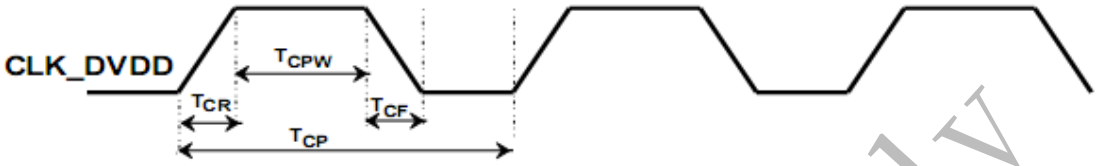

Fig. 46-3 Clock Timing Diagram

The below timing constraints are applicable for single-sample conversion mode.

Table 46-1 Timing parameters

Timing	Symbol	Value			Unit	Description
		Min	Typ	Max		
START_OF_CONV Setup time	TSU,START	5			ns	Set Up time for START_OF_CONV w.r.t CLKIN rising edge
START_OF_CONV Hold time	TH,START	5			ns	Hold time for START_OF_CONV w.r.t CLKIN rising edge
CHSEL setup time	TSU,CHSEL	5			ns	Set Up time for CHSEL w.r.t CLKIN falling edge
CHSEL Hold time	TH,CHSEL	5			ns	Hold time for CHSEL w.r.t CLKIN falling edge
Data Setup	TSU,DATA	11		15	us	Set Up time for output data w.r.t either CLKIN rising edge or END_OF_CONV falling edge
Data Hold	TH,DATA	5		9	us	Hold time for output data w.r.t either CLKIN rising edge or END_OF_CONV falling edge
Data access time	TDAC	5		9	us	Valid data w.r.t CLKIN rising edge
Delay time	TDelay			5	ns	Delay between Valid data and EOC_DVDD rising edge
EOC Pulse Width (max frequency)	TEOC	11		15	us	Pulse width of EOC
CLKIN Rise Time	TCR			2	ns	CLKIN Rise Time
CLKIN Fall Time	TCF			2	ns	CLKIN Fall Time
CLK Pulse Width(Duty Cycle)	TCPW	45		55	%	CLKIN High/Low Time Period
CLK Period	TCP	20			us	CLKIN Time Period

Note: The time from negedge of PD_DVDD to posedge of START_OF_CONV_DVDD is more than 8 cycles of CLK_DVDD, and less than 500us at same time.

46.5.3 Temperature-to-code mapping

Table 46-2 Temperature Code Mapping

temp (C)	Code
-40	3800
-35	3792
-30	3783
-25	3774
-20	3765
-15	3756
-10	3747
-5	3737
0	3728
5	3718
10	3708
15	3698
20	3688
25	3678
30	3667
35	3656
40	3645
45	3634
50	3623
55	3611
60	3600
65	3588
70	3575
75	3563
80	3550
85	3537
90	3524
95	3510
100	3496
105	3482
110	3467
115	3452
120	3437
125	3421

Note:

1. Code to Temperature mapping of the Temperature sensor is a piece wise linear curve. Any temperature, code faling between to 2 give temperatures can be linearly interpolated.

2. Code to Temperature mapping should be updated based on sillcon results.

46.5.4 User-Define Mode

1. In user-define mode, the PD_DVDD and CHSEL_DVDD are generate by setting register TSADC_USER_CON, bit[3] and bit[2:0]. In order to ensure timing between PD_DVDD and CHSEL_DVDD, the CHSEL_DVDD must be set before the PD_DVDD.

2. In user-define mode, you can choose the method to control the START_OF_CONVERSION by setting bit[4] of TSADC_USER_CON. If set to 0, the start_of_conversion will be assert after "inter_pd_soc" cycles, which could be set by bit[11:6] of TSADC_USER_CON. And if start_mode was set 1, the start_of_conversion will be controlled by bit[5] of TSADC_USER_CON.

3. Software can get the four channel temperature from TSADC_DATAn (n=0,1,2,3).

46.5.5 Automatic Mode

You can use the automatic mode with the following step:

1. Set TSADC_AUTO_PERIOD，configure the interleave between every two accessing of TSADC in normal operation.

2. Set TSADC_AUTO_PERIOD_HT. configure the interleave between every two accessing of TSADC after the temperature is higher than COMP_SHUT or COMP_INT.

3. Set TSADC_COMPn_INT(n=0,1,2,3), configure the high temperature level, if tsadc output is smaller than the value, means the temperature is high, tsadc_int will be asserted.

4. Set TSADC_COMPn_SHUT(n=0,1,2,3), configure the super high temperature level, if tsadc output is smaller than the value, means the temperature is too high, TSHUT will be asserted.

5. Set TSADC_INT_EN, you can enable the high temperature interrupt for all channel; and you can also set TSHUT output to gpio to reset the whole chip; and you can set TSHUT output to cru to reset the whole chip.

6. Set TSADC_HIGHT_INT_DEBOUNCE and TSADC_HIGHT_TSHUT_DEBOUNCE, if the temperature is higher than COMP_INT or COMP_SHUT for "debounce" times, TSADC controller will generate interrupt or TSHUT.

7. Set TSADC_AUTO_CON, enable the TSADC controller.