



























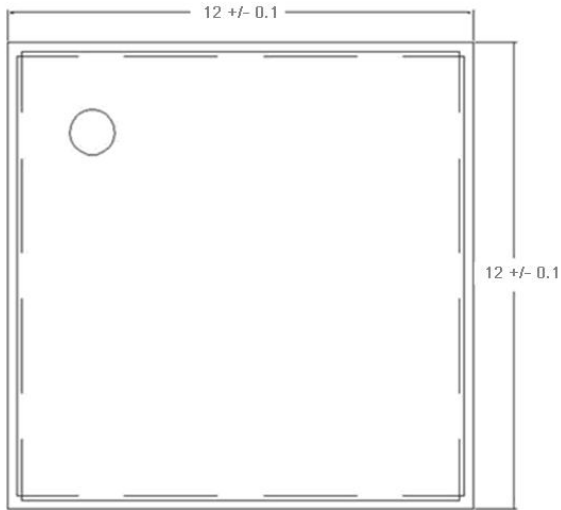


# 8. Dimensions

## 8.1 Physical Dimensions

(Unit: mm)

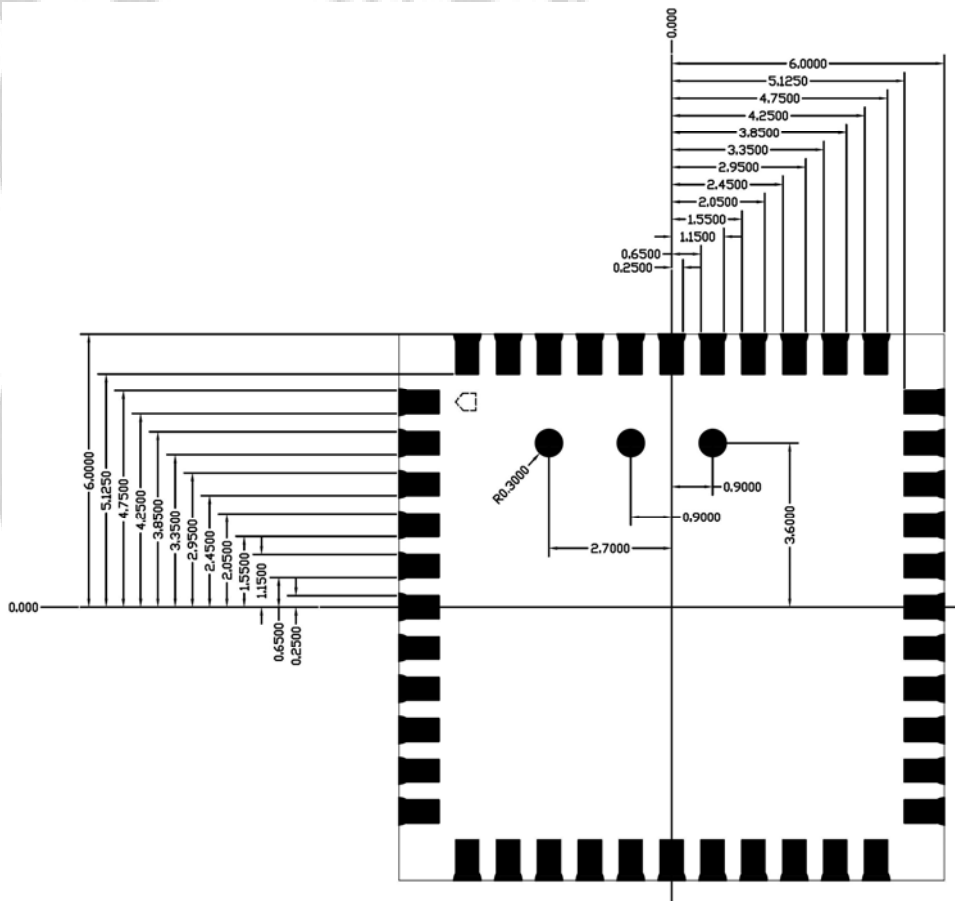
< TOP VIEW >



< Side View >



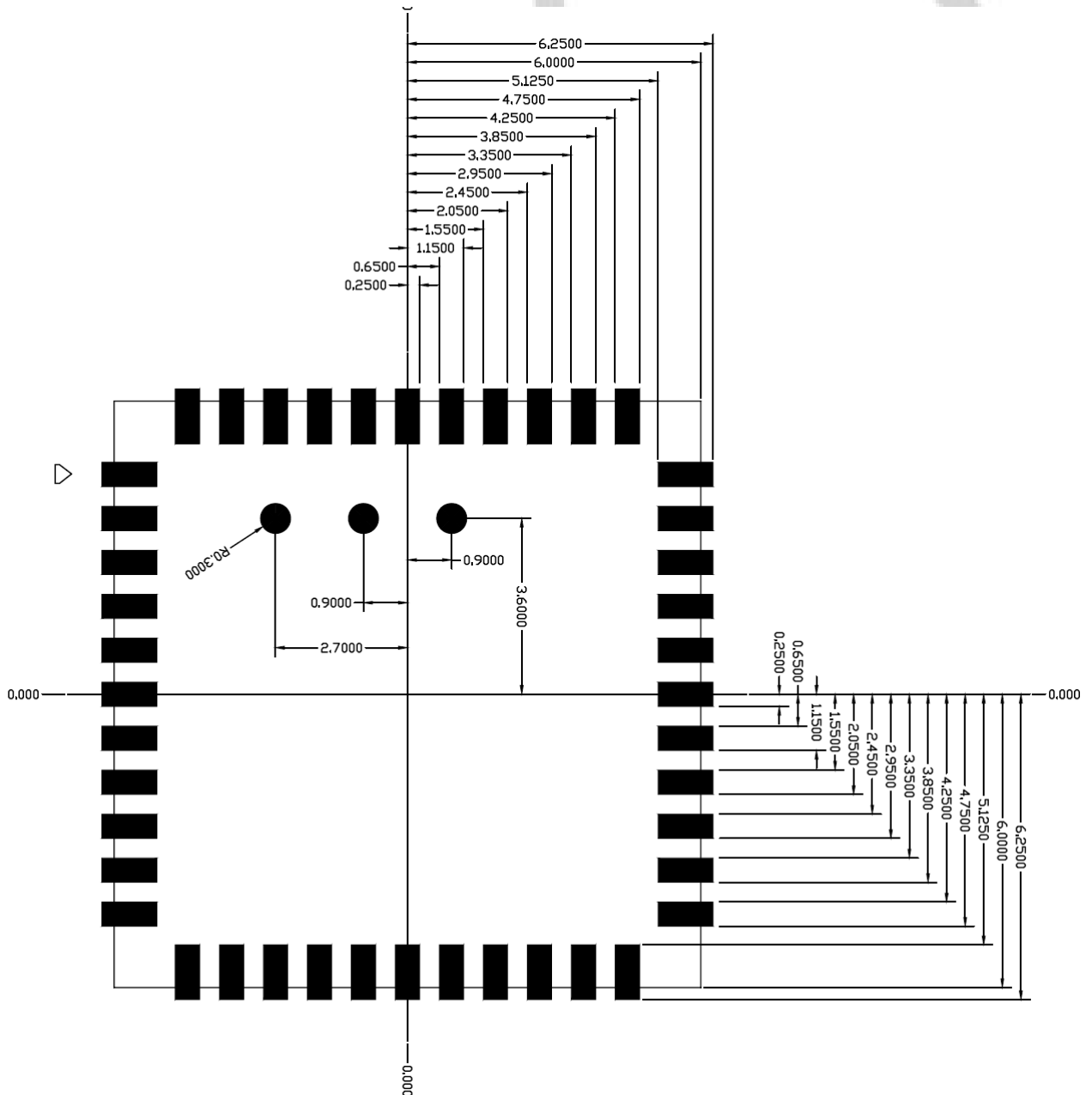
< TOP VIEW >



## 8.2 Layout Recommendation

(Unit: mm)

< TOP VIEW >



## 9. External clock reference

External LPO signal characteristics

Parameter	Specification	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	±30	ppm
Duty cycle	30 - 70	%
Input signal amplitude	1600 to 3300	mV, p-p
Signal type	Square-wave or sine-wave	-
Input impedance	>100k	Ω
	<5	pF
Clock jitter (integrated over 300Hz – 15KHz)	<1	Hz
Output high voltage	0.7V <sub>io</sub> - V <sub>io</sub>	V

External Ref\_CLK signal characteristics

No.	Item	Symb.	Electrical Specification				Remark
			Min.	Type	Max.	Units	
1	Nominal Frequency	F0	26.00000			MHz	
2	Mode of Vibration		Fundamental				
3	Frequency Tolerance	ΔF/F0	-10	-	10	ppm	at 25°C±3°C
4	Operating Temperature Range	T <sub>OPR</sub>	-30	-	85	°C	
5	Frequency Stability	TC	-10	-	10	ppm	
6	Storage Temperature	T <sub>STG</sub>	-55	-	125	°C	
7	Load capacitance	CL	-	16		pF	
8	Equivalent Series Resistance	ESR	-	-	50	Ω	
9	Drive Level	DL	-	100	200	μW	
10	Insulation Resistance	IR	500	-	-	MΩ	At 100V <sub>DC</sub>
11	Shunt Capacitance	C0	-	-	3	pF	
12	Aging Per Year	Fa	-2	-	2	ppm	First Year

### 9.1 SDIO Pin Description

The module supports SDIO version 2.0 for 4-bit modes. It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This 'out-of-band' interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.



- ❖ Function 0 Standard SDIO function (Max BlockSize / ByteCount = 32B)
- ❖ Function 1 Backplane Function to access the internal System On Chip (SOC) address space (Max BlockSize / ByteCount = 64B)
- ❖ Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max BlockSize/ByteCount=512B)

SDIO Pin Description

SDIO 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

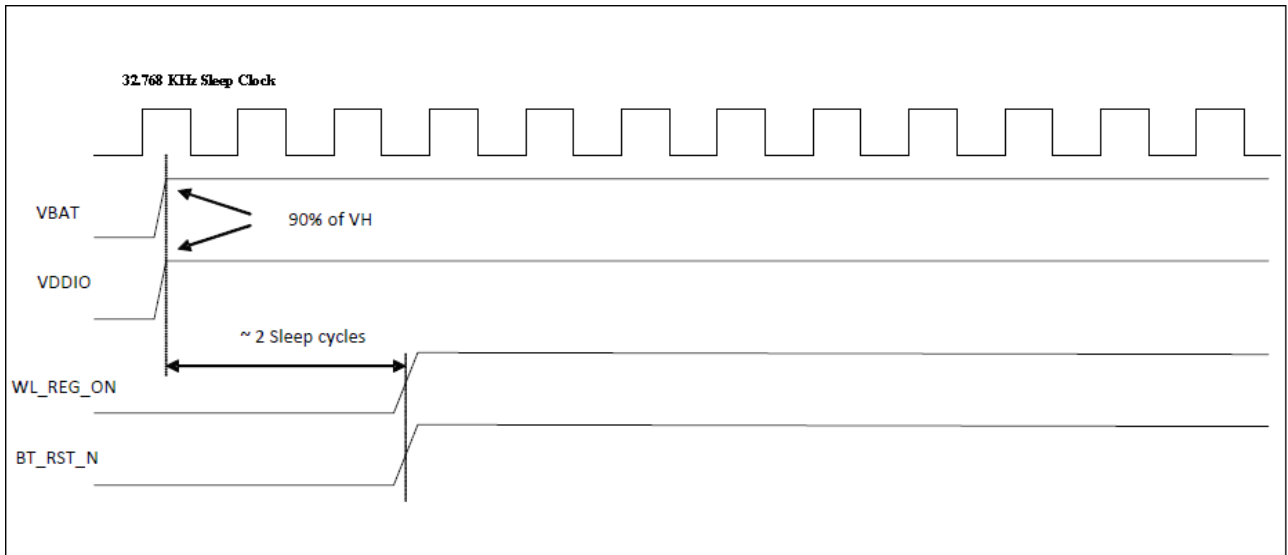
## 10. Host Interface Timing Diagram

### 10.1 Power-up Sequence Timing Diagram

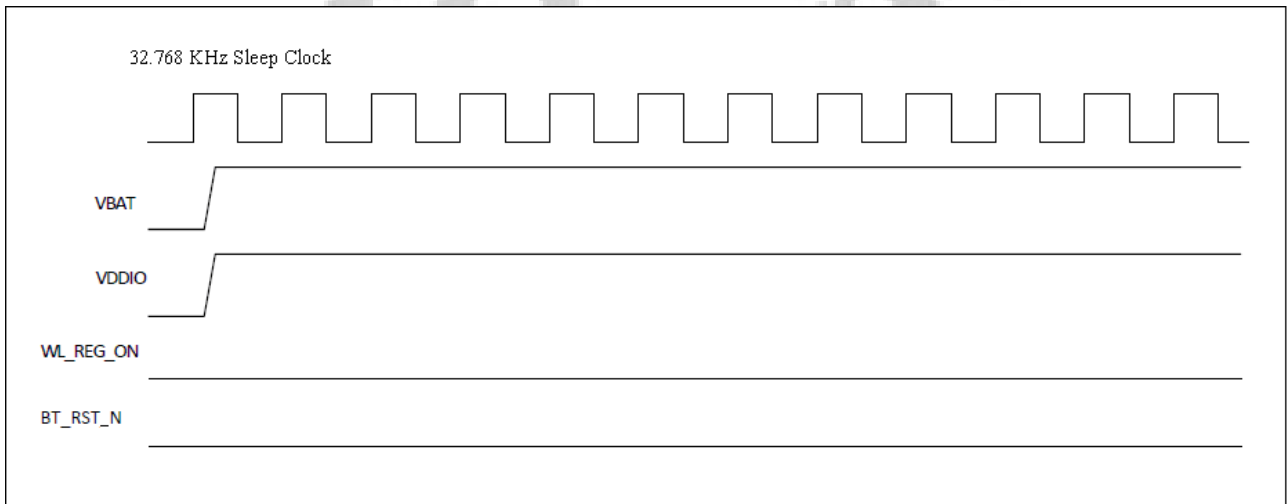
The module has two signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below.

Additionally, diagrams are provided to indicate proper sequencing of the signals for various operating states. The timing values indicated are minimum required values; longer delays are also acceptable.

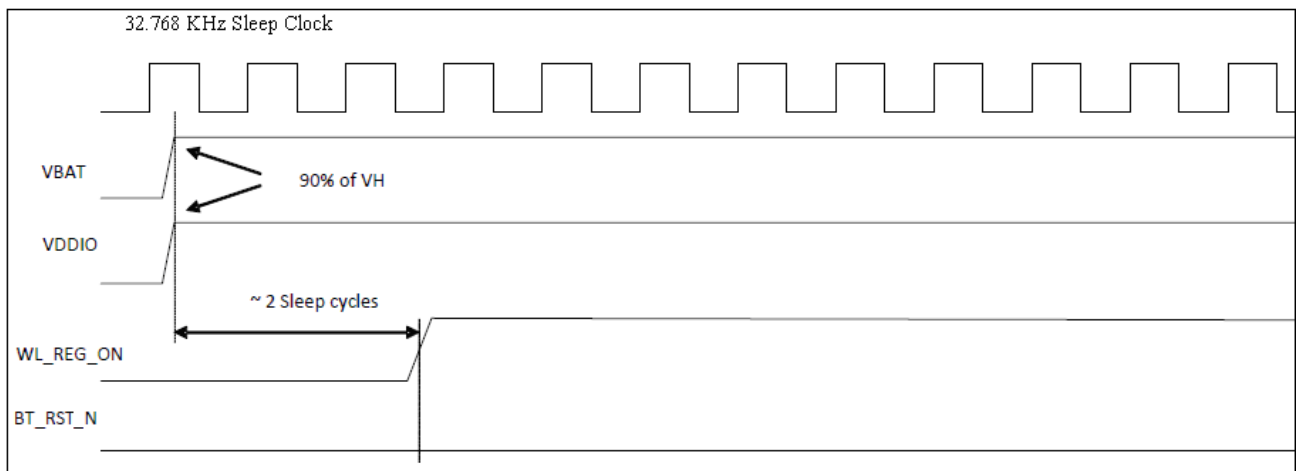
- ※ WL\_REG\_ON: Used by the PMU to power up the WLAN section. It is input to control the internal WLAN regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset.
- ※ BT\_RST\_N: Used by the PMU to power up the internal Bluetooth regulators. If the BT\_RST\_N pins are low, the regulators are disabled.



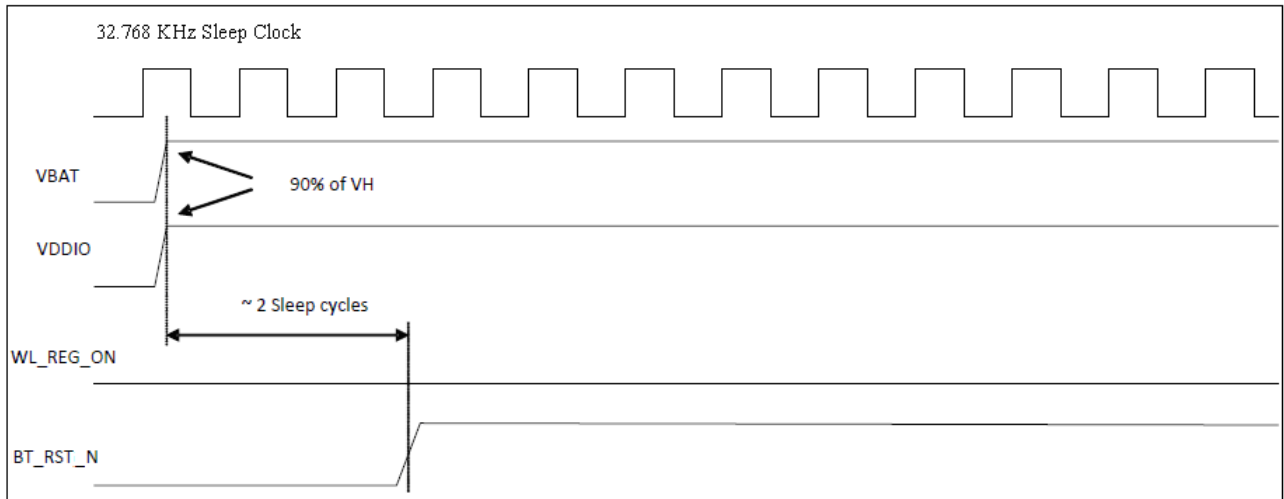
WLAN=ON, Bluetooth =ON



WLAN=OFF, Bluetooth =OFF

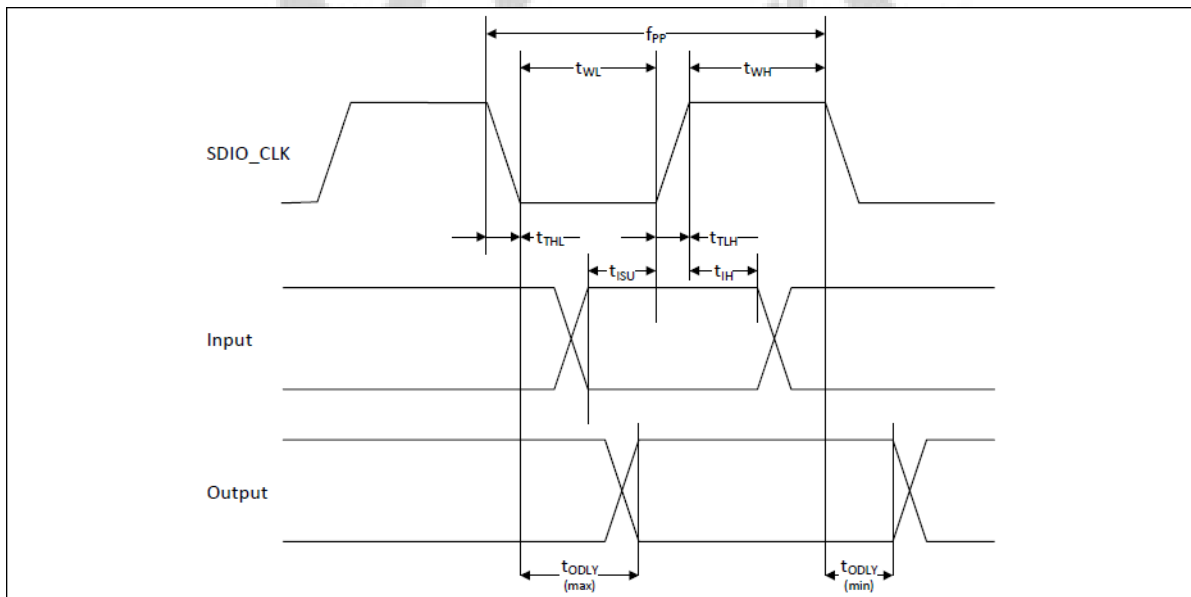


WLAN=ON, Bluetooth =OFF



WLAN=OFF, Bluetooth=ON

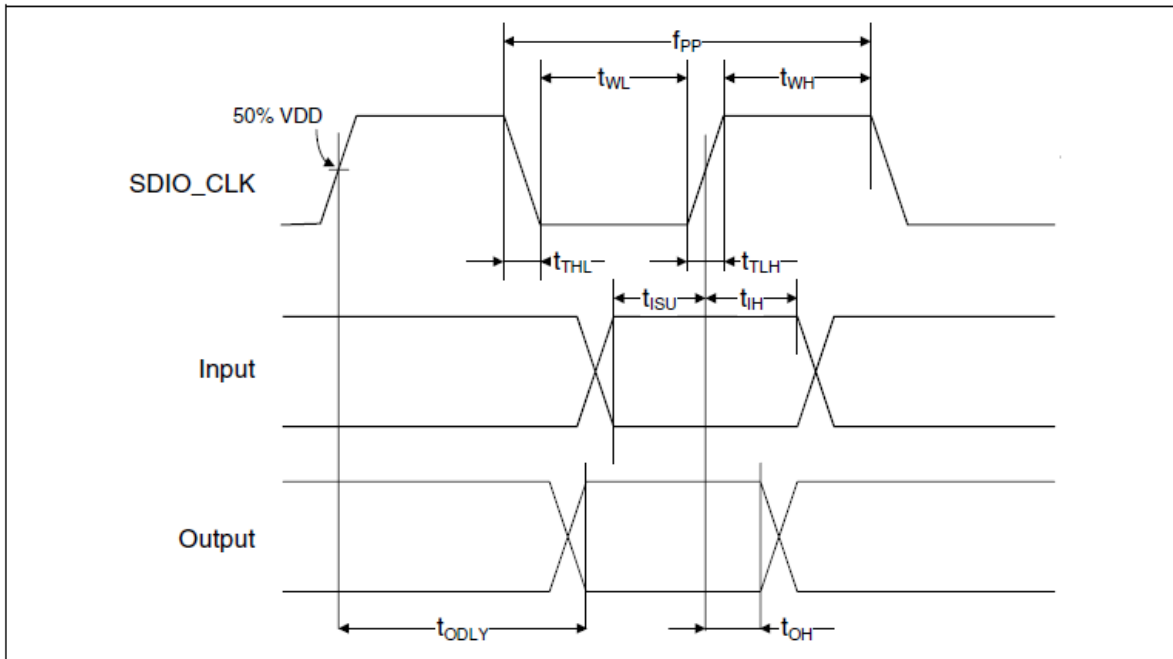
### 10.2 SDIO Default Mode Timing Diagram



Parameter	Symbol	Minimum	Typical	Maximum	Unit
<b>SDIO CLK (All values are referred to minimum V<sub>IH</sub> and maximum V<sub>IL</sub><sup>b</sup>)</b>					
Frequency-Data Transfer mode	f <sub>PP</sub>	0	-	25	MHz
Frequency-Identification mode	f <sub>OD</sub>	0	-	400	kHz
Clock low time	t <sub>WL</sub>	10	-	-	ns
Clock high time	t <sub>WH</sub>	10	-	-	ns
Clock rise time	t <sub>TLH</sub>	-	-	10	ns
Clock low time	t <sub>THL</sub>	-	-	10	ns
<b>Inputs: CMD, DAT (referenced to CLK)</b>					
Input setup time	t <sub>ISU</sub>	5	-	-	ns
Input hold time	t <sub>IH</sub>	5	-	-	ns
<b>Outputs: CMD, DAT (referenced to CLK)</b>					
Output delay time - Data Transfer mode	t <sub>ODLY</sub>	0	-	14	ns
Output delay time - Identification mode	t <sub>ODLY</sub>	0	-	50	ns

a. Timing is based on CL ≤ 40pF load on CMD and Data.  
 b. min(V<sub>IH</sub>) = 0.7 × V<sub>DDIO</sub> and max(V<sub>IL</sub>) = 0.2 × V<sub>DDIO</sub>.

### 10.3 SDIO High Speed Mode Timing Diagram



Parameter	Symbol	Minimum	Typical	Maximum	Unit
<b>SDIO CLK (All values are referred to minimum VIH and maximum VIL<sup>b</sup>)</b>					
Frequency-Data Transfer mode	$f_{PP}$	0	-	50	MHz
Frequency-Identification mode	$f_{OD}$	0	-	400	kHz
Clock low time	$t_{WL}$	7	-	-	ns
Clock high time	$t_{WH}$	7	-	-	ns
Clock rise time	$t_{TLH}$	-	-	3	ns
Clock low time	$t_{THL}$	-	-	3	ns
<b>Inputs: CMD, DAT (referenced to CLK)</b>					
Input setup time	$t_{ISU}$	6	-	-	ns
Input hold time	$t_{IH}$	2	-	-	ns
<b>Outputs: CMD, DAT (referenced to CLK)</b>					
Output delay time - Data Transfer mode	$t_{ODLY}$	-	-	14	ns
Output hold time	$t_{OH}$	2.5	-	-	ns
Total system capacitance (each line)	CL	-	-	40	pF

a. Timing is based on  $CL \leq 40\text{pF}$  load on CMD and Data.

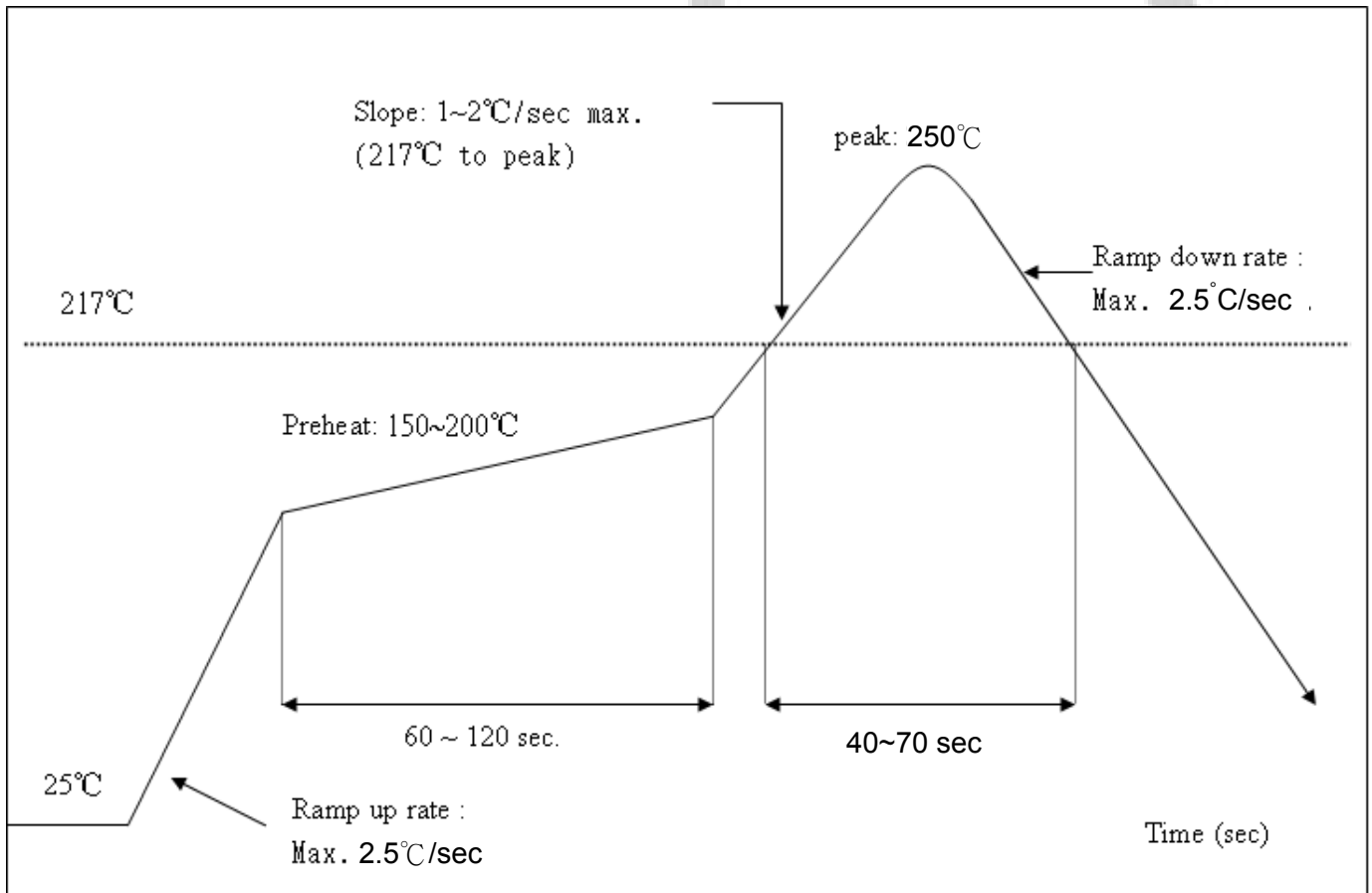
b.  $\min(V_{ih}) = 0.7 \times V_{DDIO}$  and  $\max(V_{il}) = 0.2 \times V_{DDIO}$ .

# 11. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <250°C

Number of Times : ≤2 times



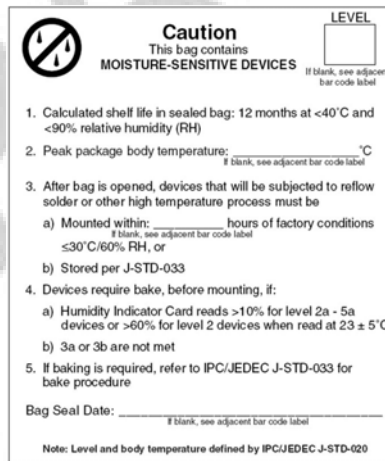
# 12. Package Information

## 12.1 Label

Label A → Anti-static and humidity notice



Label B → MSL caution / Storage Condition



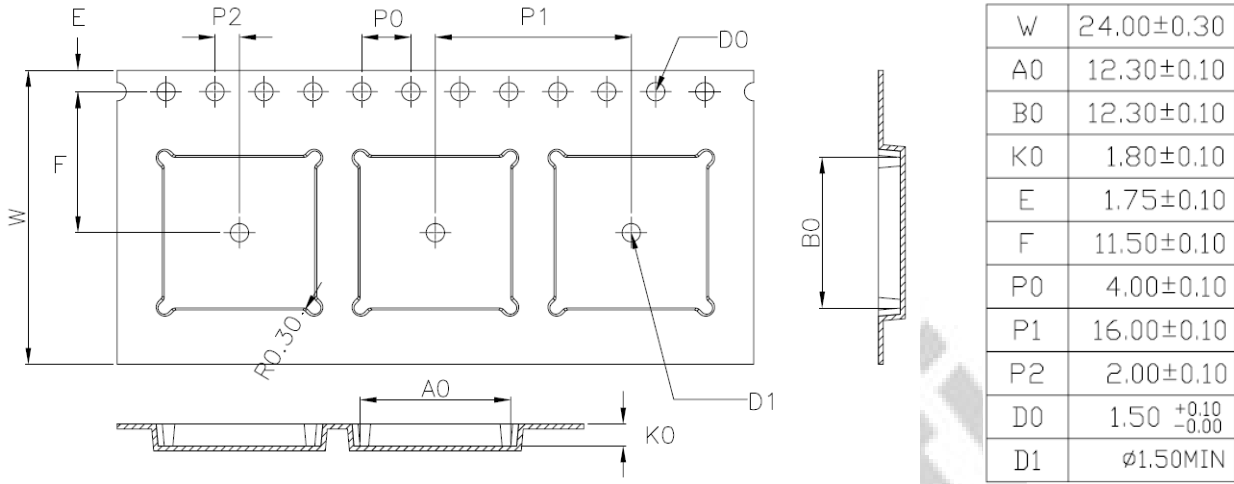
Label C → Inner box label .



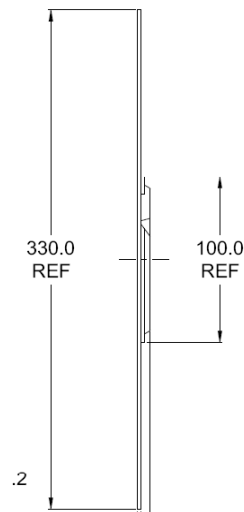
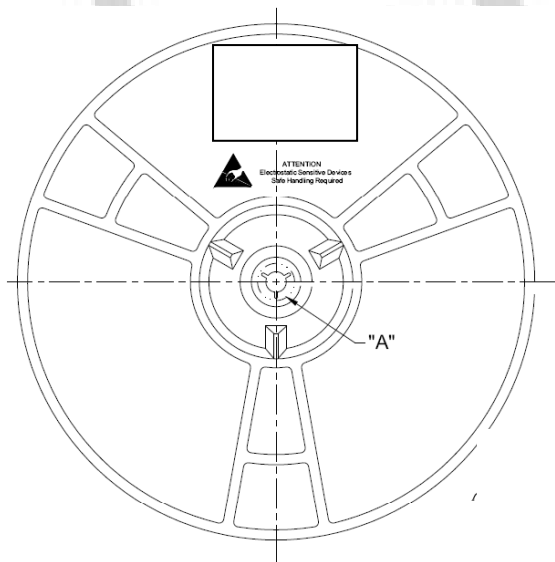
Label D → Carton box label .

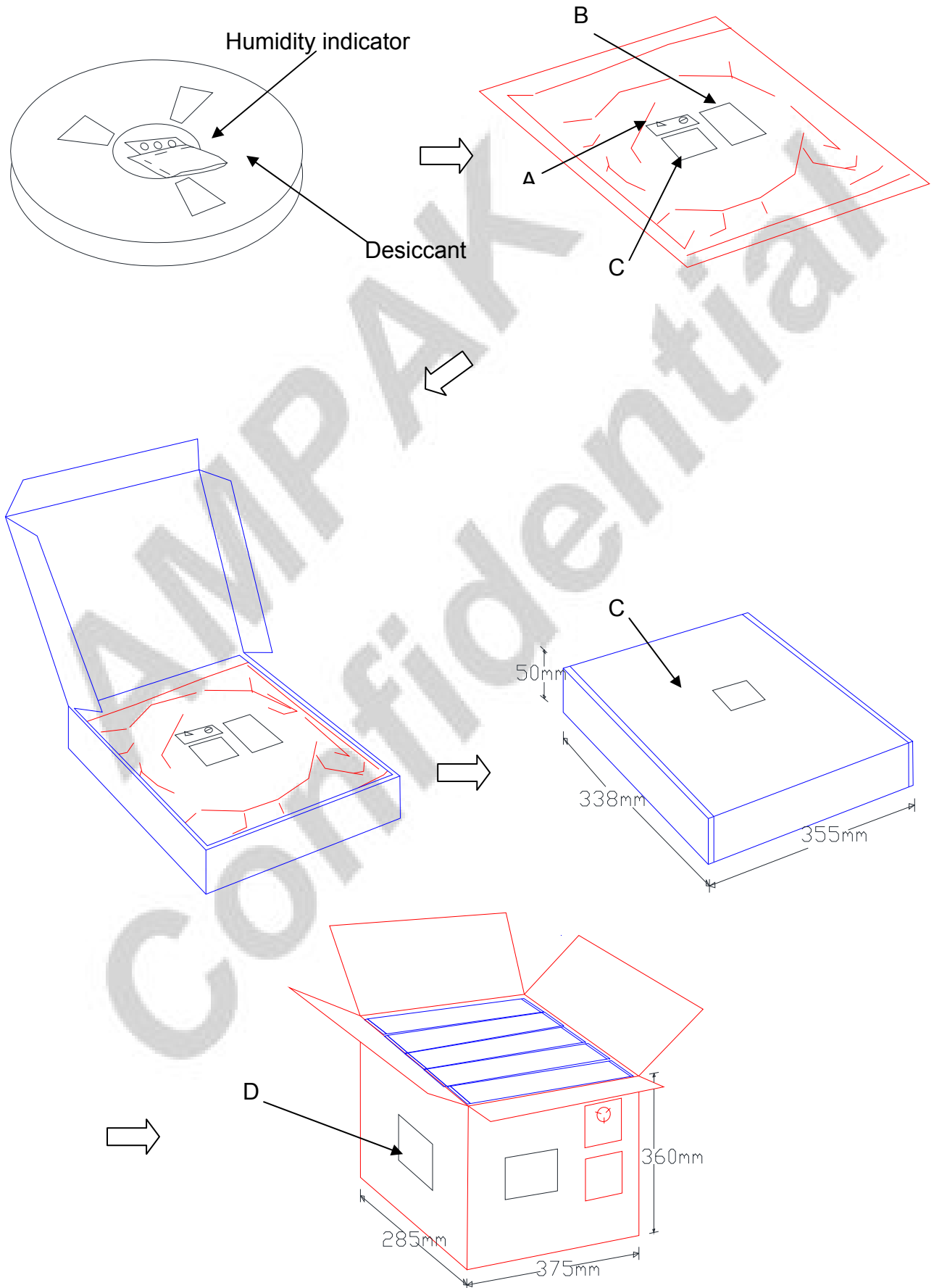


### 12.2 Dimension




1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-D requirements.
5. Thickness : 0.30±0.05mm.
6. Packing length per 22" reel : 98.5 Meters.(1:3)
7. Component load per 13" reel : 1500 pcs.







### 12.3 MSL Level / Storage Condition

	<p><b>Caution</b> This bag contains <b>MOISTURE-SENSITIVE DEVICES</b></p> <p>Do not open except under controlled conditions</p> <p>1. Calculated shelf life in sealed bag: 12 months at &lt; 40°C and &lt; 90% relative humidity(RH)</p> <p>2. Peak package body temperature:      225°C   240°C   250°C   260°C  <input type="checkbox"/>            <input type="checkbox"/>            <input checked="" type="checkbox"/>            <input type="checkbox"/></p> <p>3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must  a) Mounted within: 48 hours of factory conditions            &lt;30°C/60% RH, OR  b) Stored at &lt;10% RH</p> <p>4. Devices require bake, before mounting, if:  a) Humidity Indicator Card is &gt;10% when read at 23±5°C  b) 3a or 3b not met</p> <p>5. If baking is required, devices may be baked for 24 hours at 125±5°C</p> <p>Note : If device containers cannot be subjected to high temperature or shorter bake times are desired, reference IPC/JEDEC J-STD-033 for bake procedure</p> <p>Bag Seal Date: _____ <b>See-SEAL DATE LABEL</b> _____</p> <p>Note: Level and body temperature defined by IPC/JEDEC J-STD-020</p>	<p>LEVEL</p> <div style="border: 1px solid black; padding: 10px; width: 60px; margin: 0 auto;"> <p style="font-size: 2em; font-weight: bold;">4</p> </div>
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**※NOTE : Accumulated baking time should not exceed 96hrs**