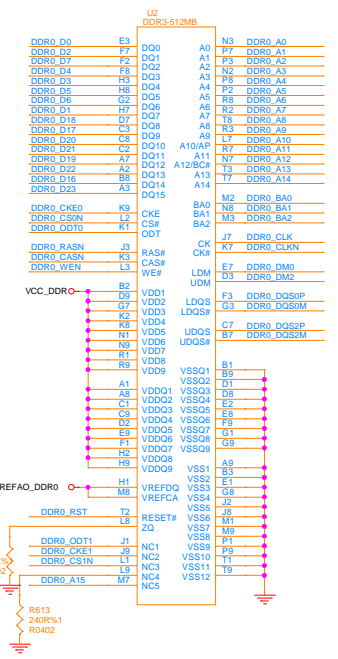
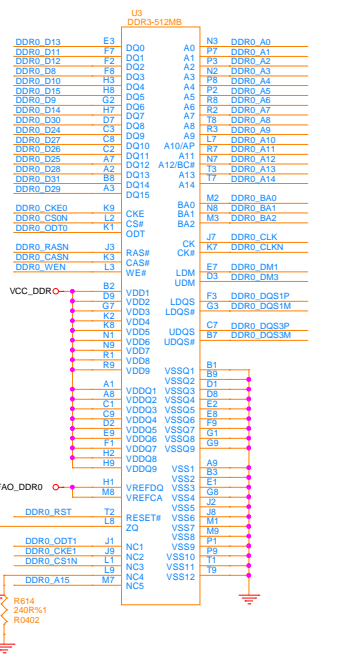


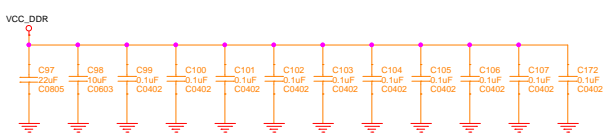
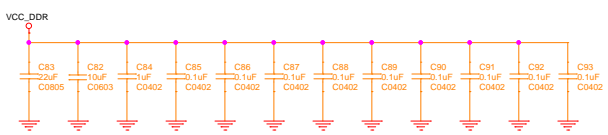
RK3288_K



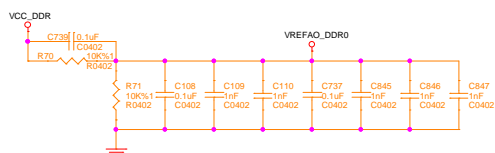
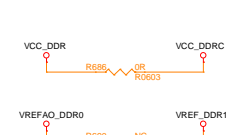
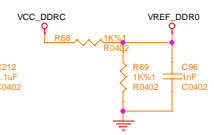
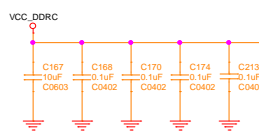
DDR3



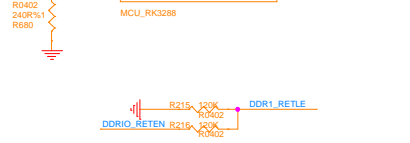
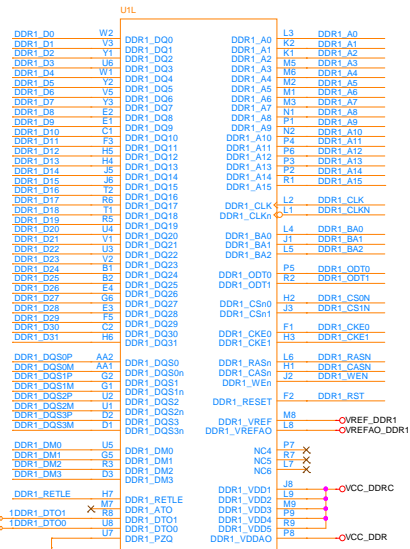
DDR0_RETEN <<DDR0_RETEN 2.4



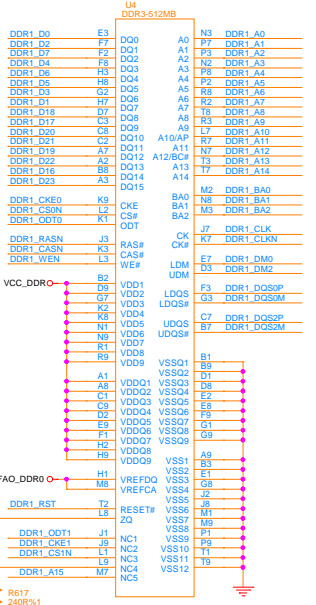
DDR0 FILTER



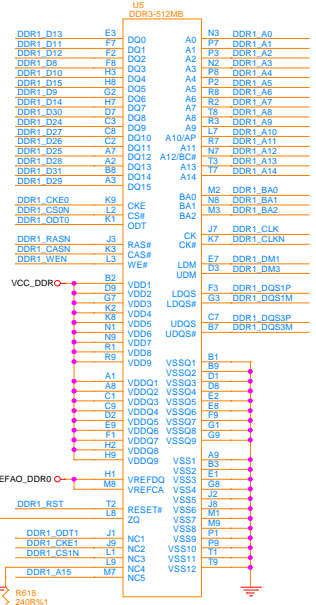
Rockchip 福州瑞芯微电子股份有限公司	
Title: DDR3	
File: RK3288_SDK_DDR3_4X16bit	
Create Date: Wednesday, August 13, 2014	Page: Num:1
Modify Date: Saturday, September 27, 2014	Page: Total:8



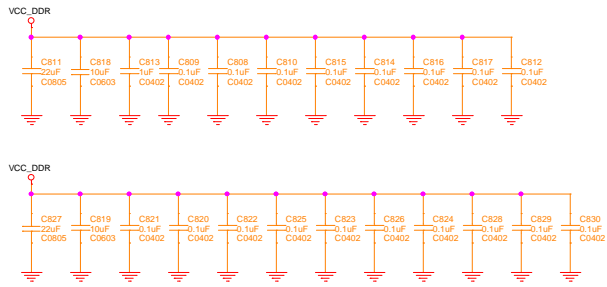
RK3288_L



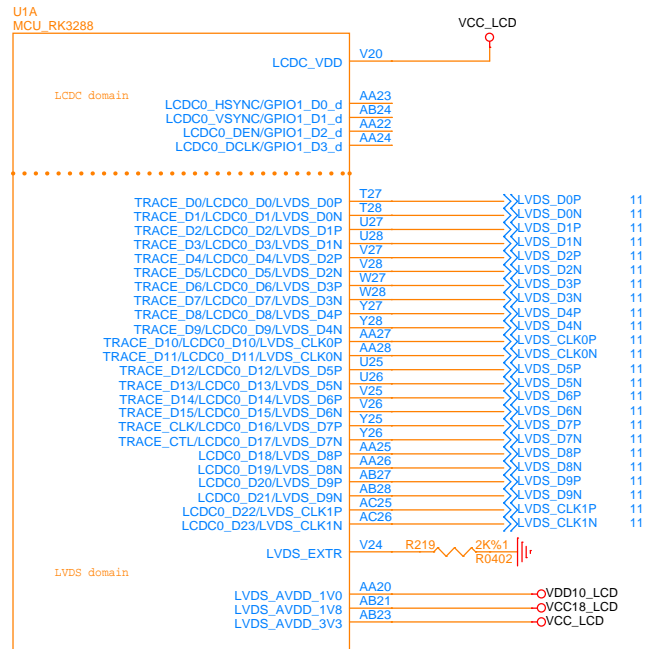
DDR3



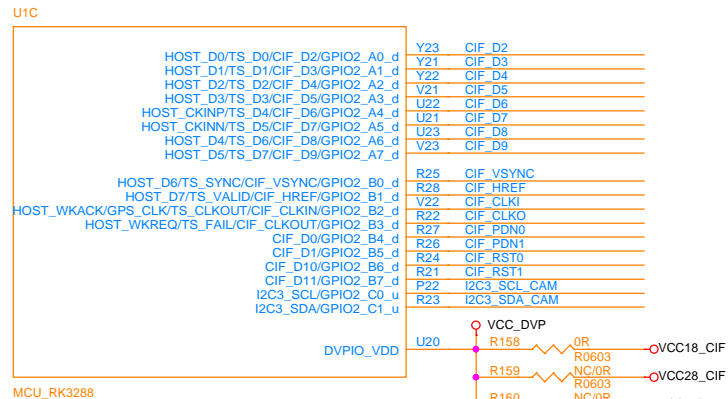
DDRIO_RETEN 1.4



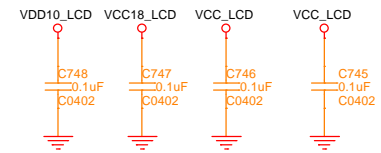
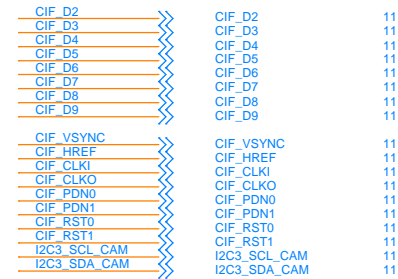
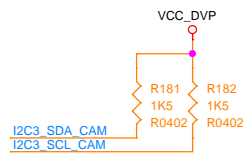
DDR FILTER



RK3288_A

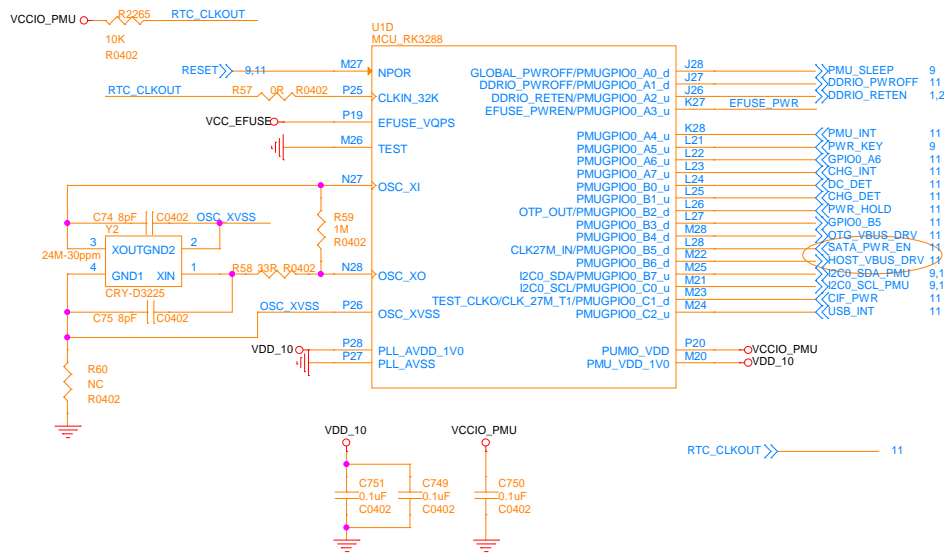


RK3288_C

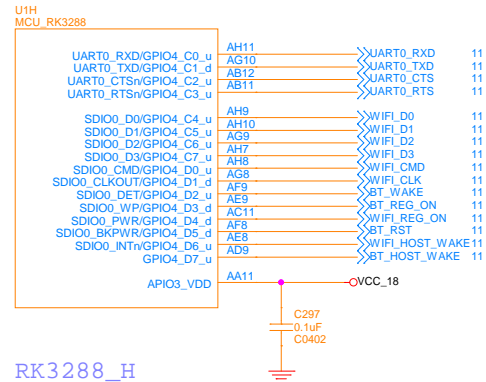


RADXA_ROCK2

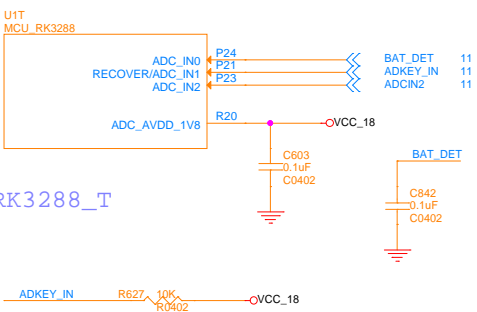
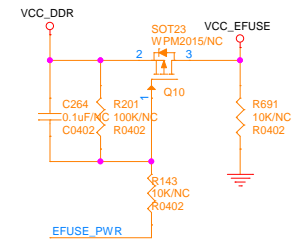
Design Name			RADXA_ROCK2		
Size	Page Name	Rev			
B	INTERFACE1	1.0			
Date:	Saturday, September 27, 2014	Sheet	3	of 11	



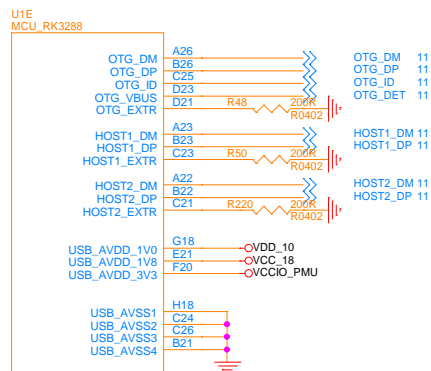
RK3288_D



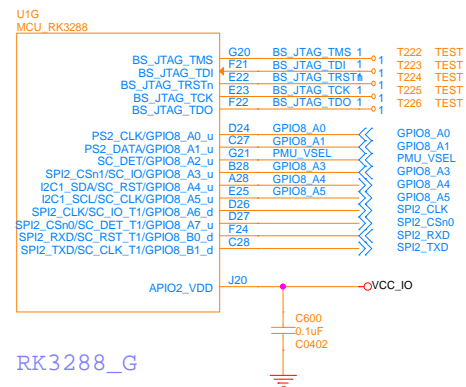
RK3288_H



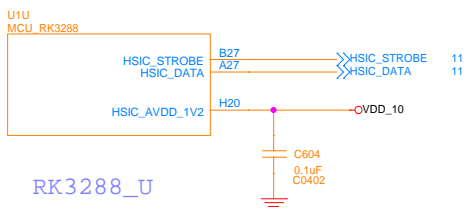
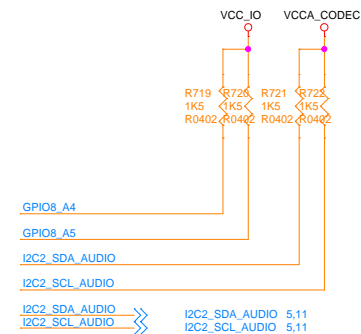
RK3288_T



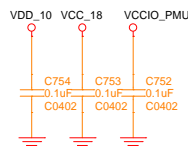
RK3288_E



RK3288_G



RK3288_U



Design Name **RADXA_ROCK2**

RADXA_ROCK2

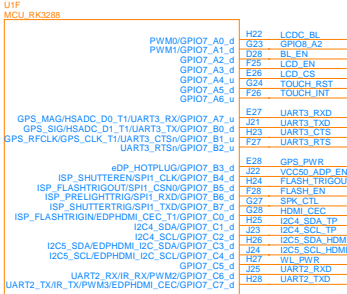
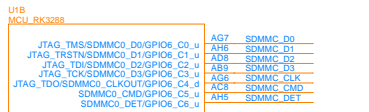
Size **A3**

Page Name **INTERFACE2**

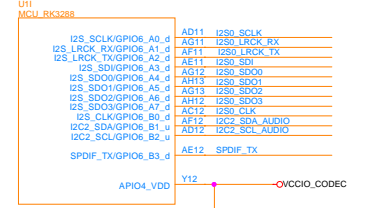
Rev **1.0**

Date: **Saturday, September 27, 2014**

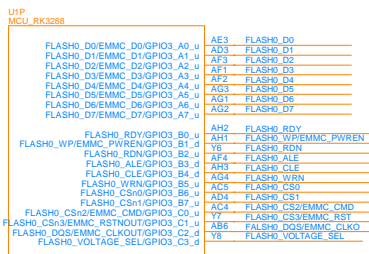
Sheet **4** of **11**



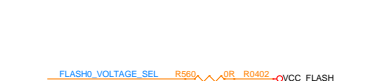
RK3288_B



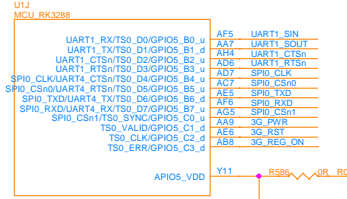
RK3288_I



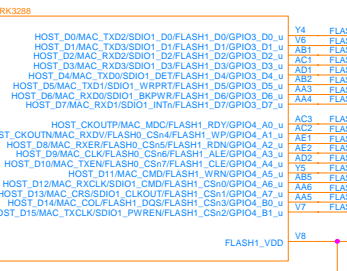
RK3288_P



RK3288_F

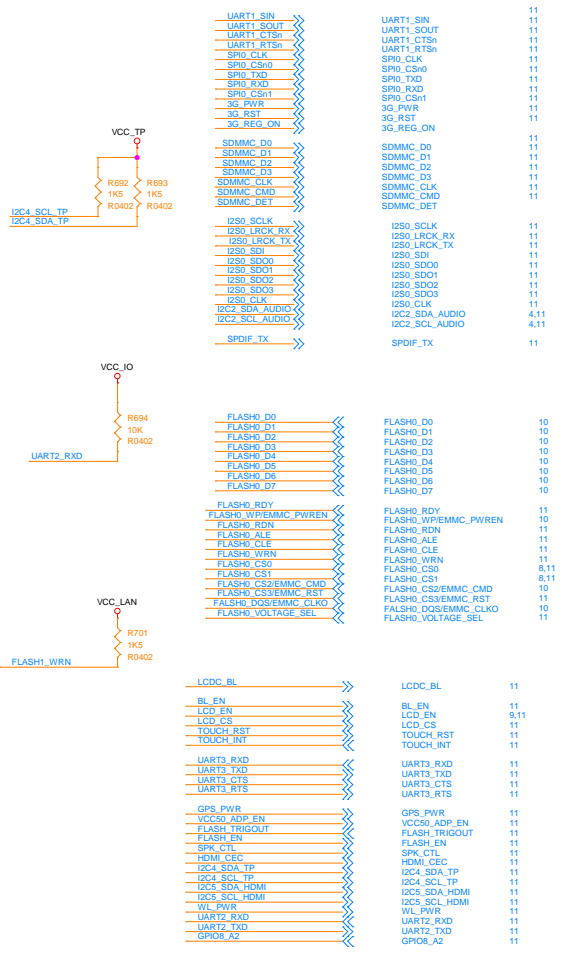


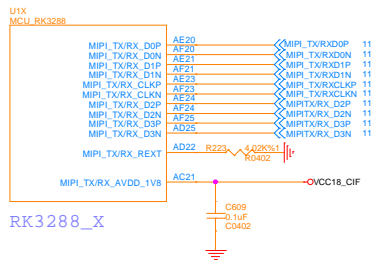
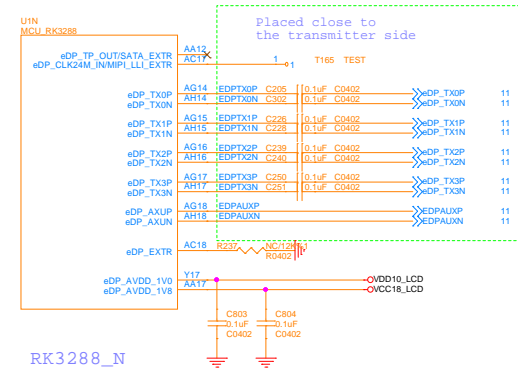
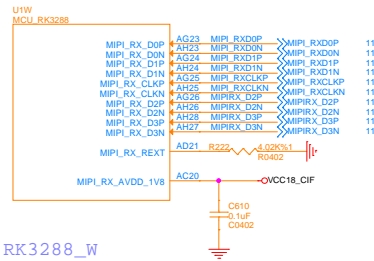
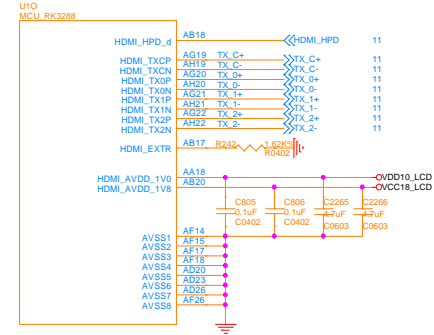
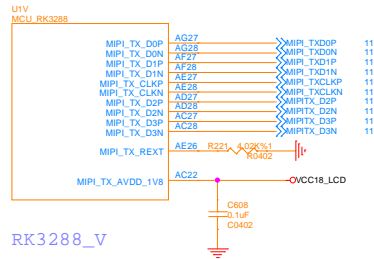
RK3288_J

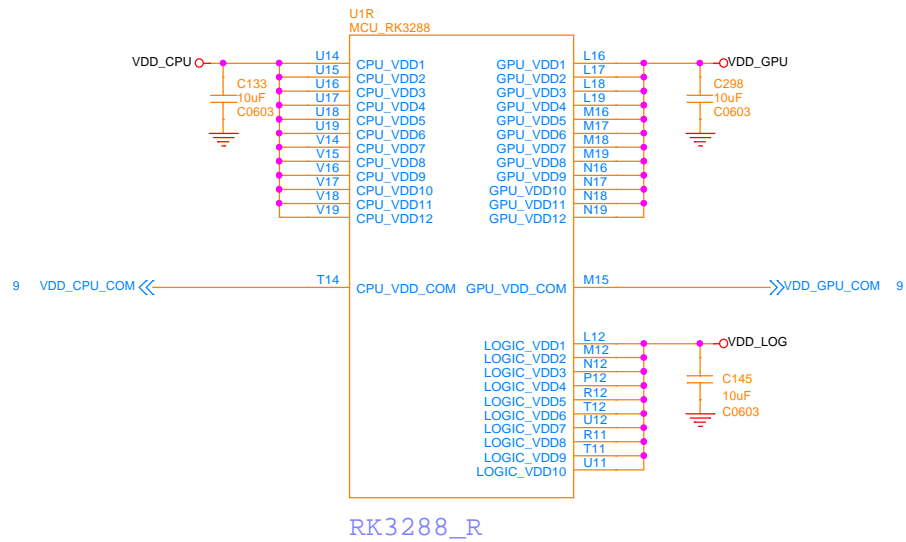


RK3288_Q

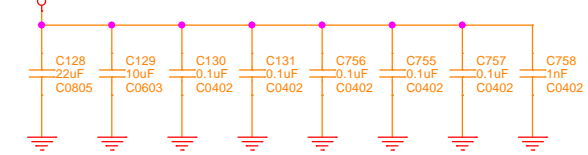
RK3188_G



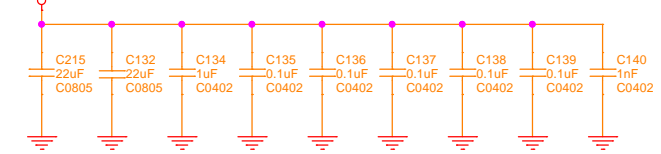




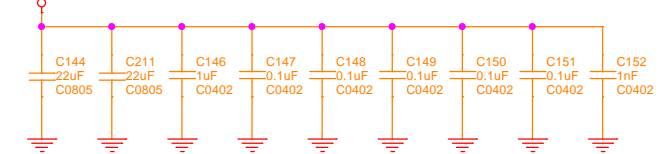
VDD_LOG **RK3288 FILTER**



VDD_CPU



VDD_GPU

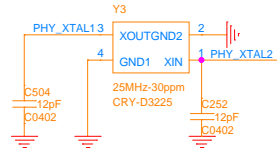


RADXA_ROCK2

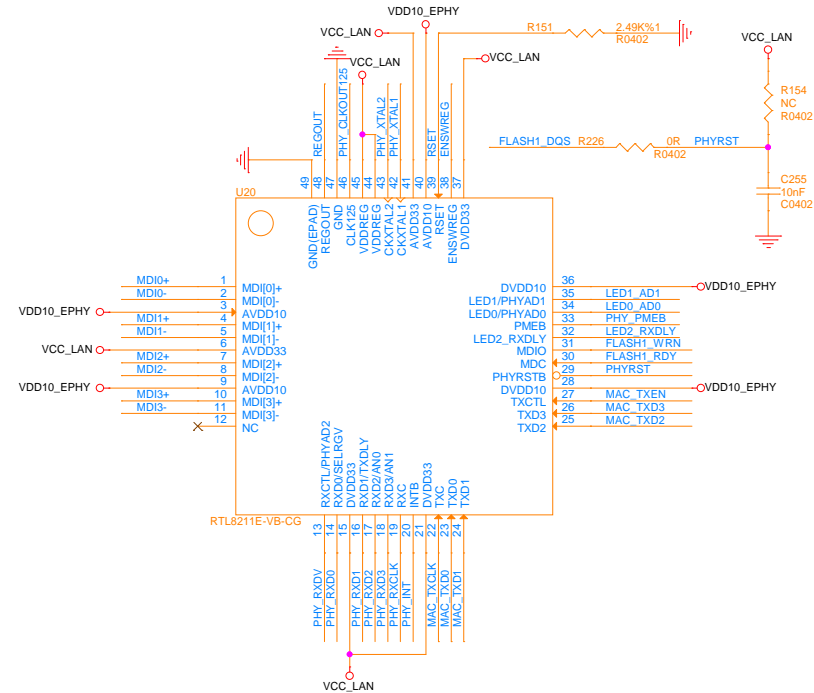
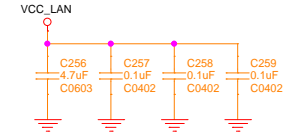
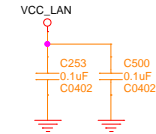
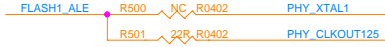
Design Name		RADXA_ROCK2
Size	Page Name	INTERFACE4&POWER
B		Rev 1.0
Date:	Saturday, September 27, 2014	Sheet 7 of 11

MAC_TXD0	MAC_TXD0	5
MAC_TXD1	MAC_TXD1	5
MAC_TXD2	MAC_TXD2	5
MAC_TXD3	MAC_TXD3	5
MAC_TXEN	MAC_TXEN	5
MAC_TXCLK	MAC_TXCLK	5
FLASH1_DQS	FLASH1_DQS	5
FLASH1_CS#0	FLASH1_CS#0	5
FLASH1_ALE	FLASH1_ALE	5
FLASH1_WP	FLASH1_WP	5
FLASH1_WRN	FLASH1_WRN	5
FLASH1_RDY	FLASH1_RDY	5
FLASH1_D2	FLASH1_D3	5
FLASH1_D3	FLASH1_D6	5
FLASH1_D6	FLASH1_D7	5
FLASH1_D7	FLASH1_D7	5
FLASH0_CS0	FLASH0_CS0	5,11
FLASH0_CS1	FLASH0_CS1	5,11

PHY_PMEB	R506	OR	R0402	FLASH0_CS0
PHY_INT	R505	OR	R0402	FLASH0_CS1

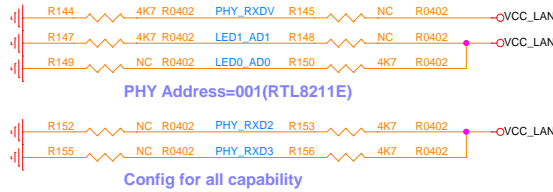


If use external clock then the XTAL2 need connect to GND for RTL8211E.

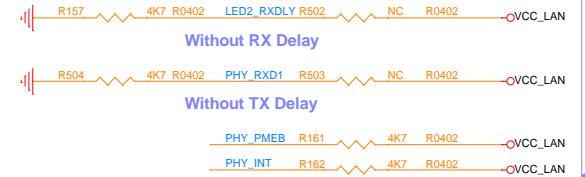


PHY_RXD0	R169	22R	R0402	FLASH1_D6
PHY_RXD1	R169	22R	R0402	FLASH1_D7
PHY_RXD2	R170	22R	R0402	FLASH1_D2
PHY_RXD3	R171	22R	R0402	FLASH1_D3
PHY_RXCLK	R172	22R	R0402	FLASH1_CS#0
PHY_RXDV	R173	22R	R0402	FLASH1_WP

Close to PHY

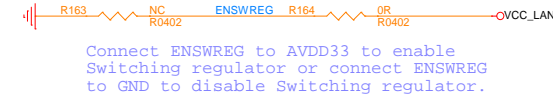


Config for all capability



Without RX Delay

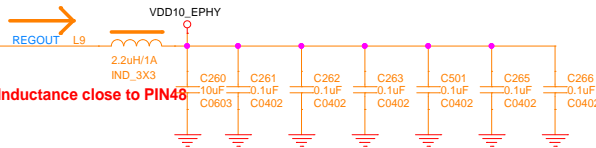
Without TX Delay



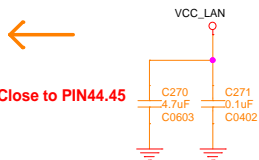
Connect ENSWREG to AVDD33 to enable Switching regulator or connect ENSWREG to GND to disable Switching regulator.



Pull down for 2.5V RGMII(RTL8211D/8211E)
Pull up for 3.3V RGMII (RTL8211D/8211E)
Pull up 1.5 / 1.8V RGMII (RTL8211E-VL only)



Inductance close to PIN48

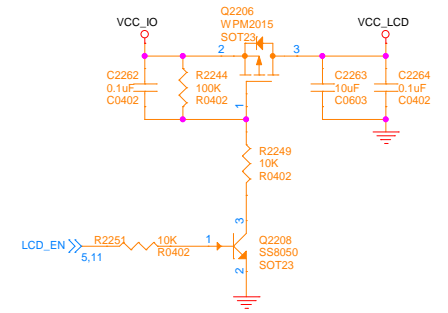
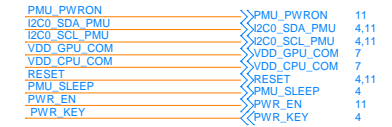
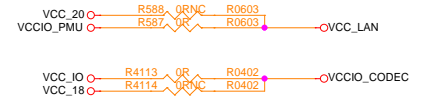
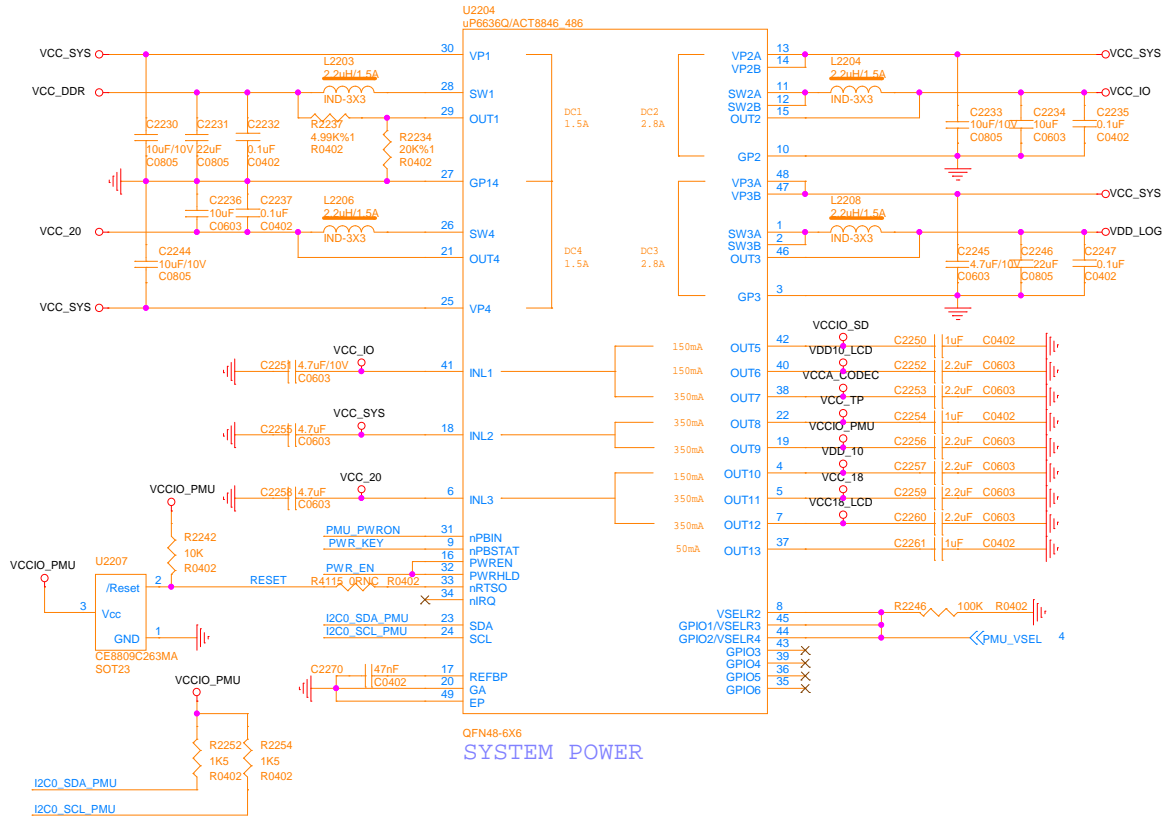


Close to PIN44.45



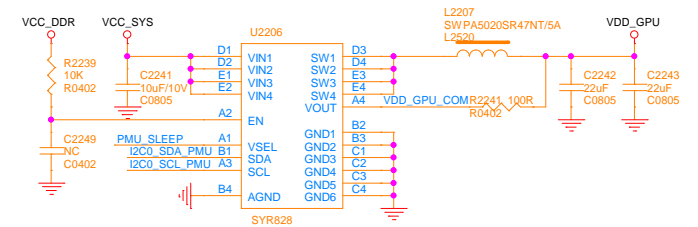
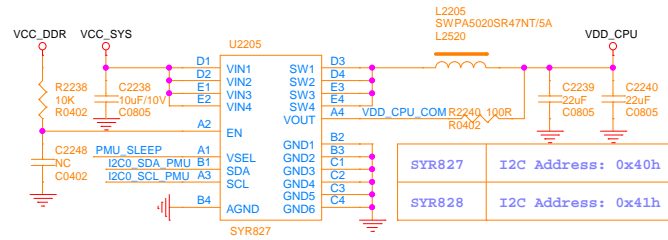
Design Name			
RADXA_ROCK2			
Size	Page Name	Rev	
A3	ETH PHY	1.0	
Date:	Saturday, September 27, 2014	Sheet	8 of 11

Note: The ACT8846-2cell Solution only for 9.7" eDP Panel.



SYSTEM POWER

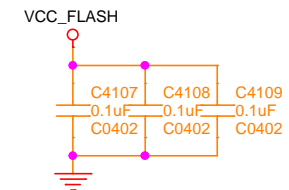
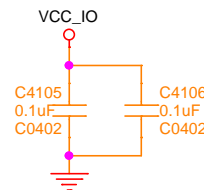
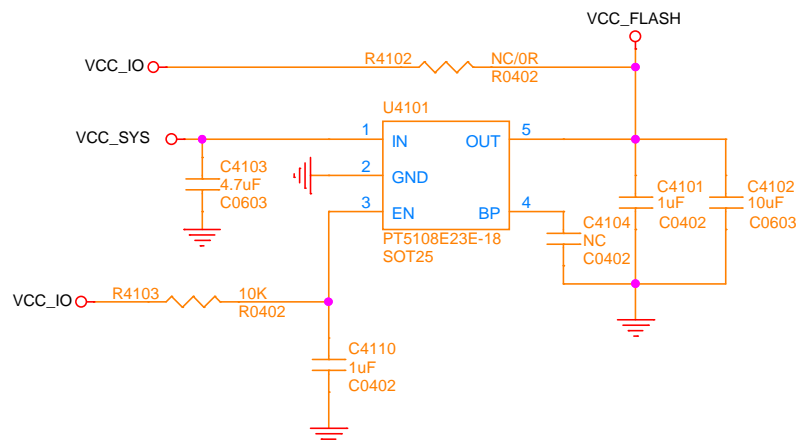
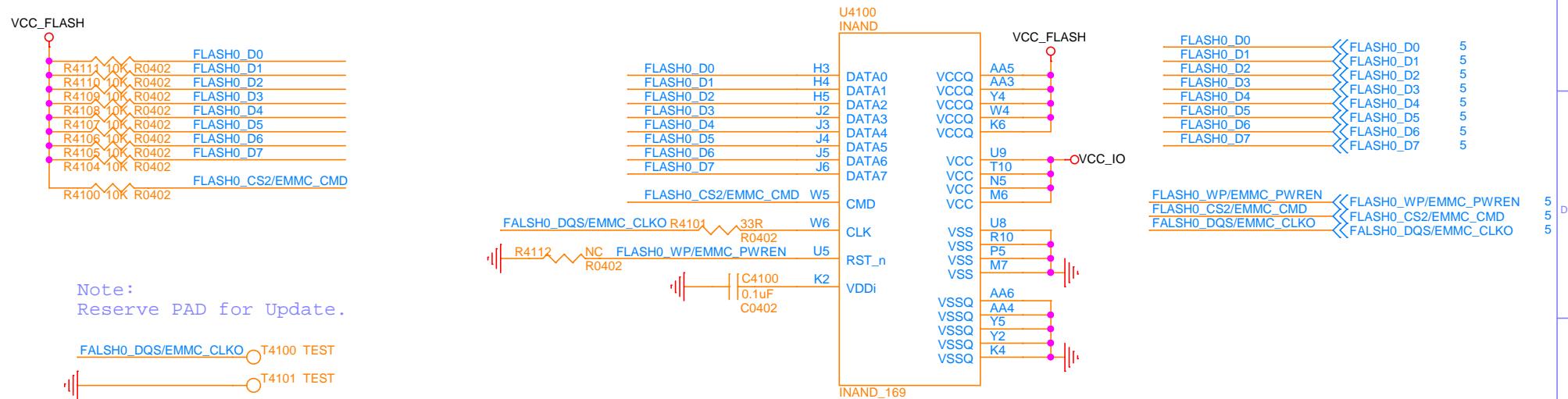
PowerName	PMU Channel	TIMER (1ms)	OutPut voltage
VCC_10	DCDC2	sol1:6	3.3V
VCC_20	DCDC4	sol1:0	2.0V
VCCIO_LCD	ExMos	DFP	3.3V
VCC_LOG	DCDC3	sol1:3	1.0V
VCC_DDR	DCDC1	sol1:2	1.2V
VDD_ARM	EXDCDC1	sol1:2A	1.0V
VDD_GPU	EXDCDC2	sol1:2B	1.0V
VCCA_TP	OUT8	DFP	3.3V
VCC_SD	ExMos	sol1:6A	3.3V
VCCIO_WL	ExMos	DFP	1.8V
VDD10_LCD	OUT6	DFP	1.0V
VCCIO_SD	OUT5	sol1:6	3.3V
VCC18_LCD	OUT12	DFP	1.8V
VDD_10	OUT10	sol1:1	1.0V
VCC_18	OUT11	sol1:4	1.8V
VCC_PMU10	OUT9	sol1:5	3.3V
VCCA_CODEC	OUT7	DFP	3.3V
RESET	sol1:6+40ms		



RADXA ROCK2

Design Name	RADXA ROCK2		
Size	Page Name	ACT8846	
Date	Saturday, September 27, 2014	Sheet	9 of 11

INAND FLASH



RADXA_ROCK2

Design Name

RADXA_ROCK2

Size
A4

Page Name

EMMC

Rev
1.0

Date:

Saturday, September 27, 2014

Sheet

10

of

11

