Rockchip RK1820/ RK1828 Datasheet

Revision 1.5
Apr. 2026

Revision History

Date	Revision	Description
2026-04-15	1.5	Update recommended minimum and maximum supply power of TOP, LOGIC and PMU in Table 3-2 Add maximum NPU frequency in Table 3-2
2025-12-04	1.4	Update package dimension pictures in 2.3 Correct minimum supply voltage for DRAM VPPEX in Table 3-2
2025-11-25	1.3	Confirm ambient operating temperature in Table 3-2
2025-11-20	1.2	Change overview description, highlighting its AI feature and applications in LLM and VLM Update description of PCIe 2.1 interface
2025-09-22	1.1	Add features and package information of RK1828
2025-07-28	1.0	Initial release

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Chapter 1 Introduction

1.1 Overview

RK1820 and RK1828 is a high-performance AI co-processor SoC for machine learning application, especially for Large Language Model (LLM) and Vision Language Model (VLM) related application.

It is based on three 64-bit independent RISC-V cores with FPU. There is a 32KB I-cache、32KB D-cache and 128KB L2 cache for each core.

The build-in NPU Support INT4/INT8/INT16/FP8/FP16/BF16 hybrid operation and computing power is up to 20TOPs. In addition, with its strong compatibility, network models based on a series of frameworks such as TensorFlow/MXNet/PyTorch/Caffe can be easily converted.

RK1820 and RK1828 have extreme high bandwidth build-in DRAM.

To communicate with the host processor, RK1820 and RK1828 integrate two PCIe 2.0/ USB 3.0 combo PHYs.

1.2 Features

1.2.1 Application Processor

- Three RISC-V cores abbreviated as SRV, VRV0 and VRV1
- SRV is implemented with RV64GCB ISA and VR0/VRV1 is implemented with RV64GCBV ISA
- All cores are integrated FPU with RISC-V H/F/D precision
- Each core has 32KB L1 I-Cache, 32KB L1 D-Cache and 128KB L2 cache
- VRV0 and VRV1 is integrated with 128-bit vector unit

1.2.2 Memory Organization

- Internal on-chip memory
  - Bootrom
    - Support system boot from the following device:
      - SPI interface
      - eMMC interface
      - SD/MMC interface
    - Support system code download by the following interface:
      - USB2.0 interface
      - UART interface
      - PCIe interface
  - 512KB system SRAM
  - Build-in Dynamic Memory Interface
    - Capacity is 2.5GB (RK1820)/ 5GB (RK1828)

- External off-chip memory
  - Combo SDMMC Interface, work at only one of the following modes
    - eMMC
      - Fully compliant with JEDEC eMMC 4.51 specification
      - Support HS200, but not support CMD Queue
      - Support three data bus width mode: 1bit, 4bits and 8bits
    - SD/MMC Interface
      - Compatible with SD3.0, MMC ver4.51
      - Support 1bit, 4bits data bus width
    - SDIO Interface
      - Compatible with SDIO3.0 protocol
      - 4-bit data bus widths

- Flexible Serial Flash Interface (FSPI)
  - Support transfer data from/to serial flash device
  - Support 1bit, 2bits or 4bits data bus width
  - Support 2 chips select

1.2.3 System Component

- CRU (clock & reset unit)
  - Support total 4 PLLs to generate all clocks
  - One oscillator with 24MHz clock input
  - Support clock gating control for individual components
  - Support global soft-reset control for whole chip, also individual soft-reset for each component

- PMU (power management unit)
  - Multiple configurable work modes to save power by different frequency or automatic clock gating control
  - Support 3 separate voltage domains
    VDD_TOP, VDD_LOGIC, VDD_PMU

- Timer
  - Support 6 timers with 64bits counter and interrupt-based operation
  - Support two operation modes: free-running and user-defined count for each timer
  - Support timer work state checkable

- Watchdog
  - 32-bit watchdog counter
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - Generate a system reset
    - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
  - Three Watchdogs

- Interrupt Controller
  - Support 160 interrupt sources input from different components inside SoC for SRV and 64 interrupt sources input for VRV
  - Support 1 software-triggered interrupt in m-mode and s-mode each
  - Input interrupt level is fixed, high-level sensitive
  - Support different interrupt priority for each interrupt source, and they are always software-programmable

- DMAC
  - Support 2 physical channels
  - Support 22 groups of peripheral request interfaces
  - Support 24 logic channels, each logic channel support the following feature
    - Support the data transfer of memory-to-memory, memory-to-peripherals, peripherals-to-memory
    - Support Linked list DMA function to complete scatter-gather transfer
    - Support three kinds of multi-block transfer: contiguous address, auto reload, link list

- Secure System
  - Support one cipher engine
    - Support Symmetrical algorithms
      - AES-128, AES-192, AES-256, SM4
      - ECB/CBC/OFB/CFB/CTR/CTS/XTS/CCM/GCM/CBC-MAC/CMAC mode for AES

and SM4
- Hash algorithm
  - SHA-1, SHA-256/224, MD5, SM3 with hardware padding
  - HMAC of SHA-1, SHA-256, MD5, SM3 with hardware padding
- Asymmetrical algorithms
  - RSA (up to 4096 bits), ECC (up to 256 bits), SM2
- Key-ladder (KL)
  - Support obtaining the root key from OTP or RKRNG and deriving it
  - Support writes out root key or derived key to some specific modules
  - Number of stages can be configured

- Mailbox
  - Twelve mailboxes in SoC used to service different RISC-V communication

1.2.4 JPEG CODEC

- JPEG encoder
  - Supports Baseline (DCT sequential)
  - Supports JPEG file interchange format (JFIF) 1.02
  - Supports image size is from 16x16 to 65520x65520
  - Supports YUV400/YUV420/YUV422/YUV444

- JPEG Decoder
  - Support Baseline (DCT sequential)
  - Support JPEG file interchange format (JFIF) 1.02
  - Support image size is from 48x48 to 65520x65520
  - Support YUV400/YUV420/YUV422/YUV440/YUV411/YUV444/RG888/RGB565

1.2.5 Neural Process Unit

- Rockchip NPU engine:
  - Up to 20 TOPS for INT8
  - Support INT4/INT8/INT16/FP8/FP16/BF16 operation
  - Support deep learning frameworks: TensorFlow, Caffe, Tflite, Pytorch, Onnx NN, Android NN, etc.

1.2.6 2D Graphics Engine

- 2D Graphics Engine (RGA)
- Data format
  - SRC0 Input data format:
    - ARGB8888/RGBA8888/RGBA4444/RGBA5551
    - RGB888P/RGB565
    - YUV422-P/YUV422-SP-8bit/10bit (clip to 8bit after input)
    - YUV420-P/YUV420-SP-8bit/10bit (clip to 8bit after input)
    - YUV444I/YUV444SP-8bit
    - YVYU422-8bit
    - YUV400-8bit
    - TILE4X4 YUV420/422/444-8bit
    - TILE4X4 YUV420/422/444-10bit (clip to 8bit after input)
    - BPP1/2/4/8
  - SRC1 Input data format:
    - ARGB8888/RGBA8888/RGBA4444/RGBA5551/A8
    - RGB888P/RGB565
  - Output data format (all YUV format is 8bit):
    - ARGB8888/RGBA8888/ARGB4444/RGBA4444/ARGB5551/RGBA5551
    - RGB888/RGB565
    - YUV420/YUV422 P/SP
    - YUV400/Y4
    - YUV444SP/444I
  - Pixel Format conversion, BT.601/BT.709

- Dither operation
- Max resolution : 8192x8192 source, 4096x4096 destination

- Scaling
  - Down-scaling: Average/Bilinear filter
  - Up-scaling: Bi-cubic filter(source>1992 would use Bi-linear)
  - Arbitrary non-integer scaling ratio, from 1/16 to 16
- Rotation
  - 0, 90, 180, 270-degree rotation
  - x-mirror, y-mirror operation
  - Mirroring and rotation co-operation
- BitBLT
  - Block transfer
  - Color palette/Color fill, support with alpha
  - Transparency mode (color keying/stencil test, specified value/value range)
  - Two source BitBLT
  - A+B=B only BitBLT, A support rotate & scale when B fixed
  - A+B=C second source (B) has same attribute with (C) plus rotation function
- Alpha Blending
  - Comprehensive per-pixel alpha (color/alpha channel separately)
  - Fading
  - Support SRC1(R2Y) +SRC0(YUV) -> DST(YUV)
  - Support DST Full CSC convert for YUV2YUV
- OSD Automatic Inversion
  - Support OSD sources in ARGB8888/ARGB1555/ARGB444/ARGB2BPP format
  - Support SRC0 and OSD overlay

1.2.7 Serial Audio Interface (SAI)

- Support 1 SAI interfaces
  - Support 4 TX lanes and 4 RX lanes
  - Support audio protocol: I2S, PCM, TDM
  - Support up to 128 slots available with configurable size
  - Support slot length 8 to 32 bits configurable
  - Support slot valid data length 8 to 32 bits configurable

1.2.8 Connectivity

- MAC 10/100/1000M Ethernet
  - Support one Ethernet controllers
  - Support 10/100/1000-Mbps data transfer rates with the RGMII interfaces
  - Support both full-duplex and half-duplex operation
  - Support for TCP Segmentation Offload (TSO) and UDP Segmentation Offload (USO) network acceleration
  - Support Ethernet packet timestamping as described in IEEE 1588-2002 and IEEE 1588-2008

- USB 2.0 DRD (Dual-Role Device)
  - Support one USB2.0 DRD (Dual-Role Device)
  - Compatible with USB 2.0 specification
  - Support high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Support Enhanced Host Controller Interface Specification (EHCI), Revision 1.0
  - Support Open Host Controller Interface Specification (OHCI), Revision 1.0a

- Multi-PHY Interface
  - Support two multi-PHY with two PCIe2.1 controller and one USB3.0 controller (multiplex to one of the PHY)
  - Support one of the following interfaces for each multi-PHY
    - USB3.0 Host

    - PCIe2.1
  - USB 3.0 Dual-Role Device (DRD) Controller
    - Static USB3.0 Device
    - Static USB3.0 xHCI host
    - USB3.0/USB2.0 OTG A device and B device basing on ID
  - PCIe2.1 interface
    - Compatible with PCI Express Base Specification Revision 2.1
    - Support one lane
    - Support dual mode
    - Support 5.0GT/s serial data transmission rate per lane per direction

- SPI interface
  - Support 2 SPI Controllers
  - Support two chip-select output
  - Support serial-master and serial-slave mode, software-configurable

- I2C Master controller
  - Support 5 I2C ports in Master mode
  - Support 7bits and 10bits address mode
  - Software programmable clock frequency
  - Data on the I2C-bus can be transferred at rates of up to 100k bits/s in the Standard-mode, up to 400K bits/s in the Fast-mode and up to 1M bit/s in high-speed mode

- SMBus slave interface
  - Support 1 independent SMBus
  - Supports slave mode of SMBus bus
  - Support SMBus protocol: write byte/read byte/read word/read 32 protocol/write 32 protocol/block write/block read
  - Support PEC
  - Support Alert
  - Support directed get UDID command
  - Clock stretching and wait state generation

- UART interface
  - Support 3 UART ports
  - Embedded two 64-byte FIFO for TX and RX operation respectively
  - Support 5bit, 6bit, 7bit, 8bit serial data transmit or receive
  - Standard asynchronous communication bits such as start, stop and parity
  - Support different input clock for UART operation to get up to 4Mbps baud rate
  - Support auto flow control mode for UART2
  - Support RS485 function for UART2

- PWM
  - Support 1 PWM interface, total 8 channels
  - Support input capture mode
  - Support continuous mode and one-shot output mode
  - Support two-stage frequency division of working clock
  - Support power key capture mode
  - Support clock frequency meter
  - Support clock counter

1.2.9 Others

- Multiple groups of GPIO
  - All of GPIOs can be used to generate interrupt
  - Support level trigger and edge trigger interrupt
  - Support configurable polarity of level trigger interrupt
  - Support configurable rising edge, falling edge and both edge trigger interrupt

- Support configurable pull direction (a weak pull-up and a weak pull-down)
- Support configurable drive strength

- Temperature Sensor (TS-ADC)
  - Support User-Defined Mode and Automatic Mode
  - In User-Defined Mode, start_of_conversion can be controlled completely by software, and also can be generated by hardware.
  - In Automatic Mode, the temperature of alarm (high/low temperature) interrupt can be configurable
  - In Automatic Mode, the temperature of system reset can be configurable
  - Support 3 channel TS-ADC
  - -40~125°C temperature range and +/-3.5°C temperature accuracy
  - Resolution: 0.01°C

- Successive approximation ADC (SARADC)
  - Support 1 SARADC, each support 2 single-ended input channels
  - 13-bit resolution
  - Up to 2MS/s sampling rate
  - Support single mode and series conversion mode

- OTP
  - Support 8K bits size, 6.5K bits for secure application
  - Support Program/Read/Idle mode

- Package Type
  - **RK1820**: FCBGA 746L (body size:19mm x 19mm; ball size: 0.35mm; ball pitch: 0.65mm)
  - **RK1828**: FCBGA 746L (body size:19mm x 19mm; ball size: 0.35mm; ball pitch: 0.65mm)

1.3 Block Diagram

The following figure shows the basic block diagram.

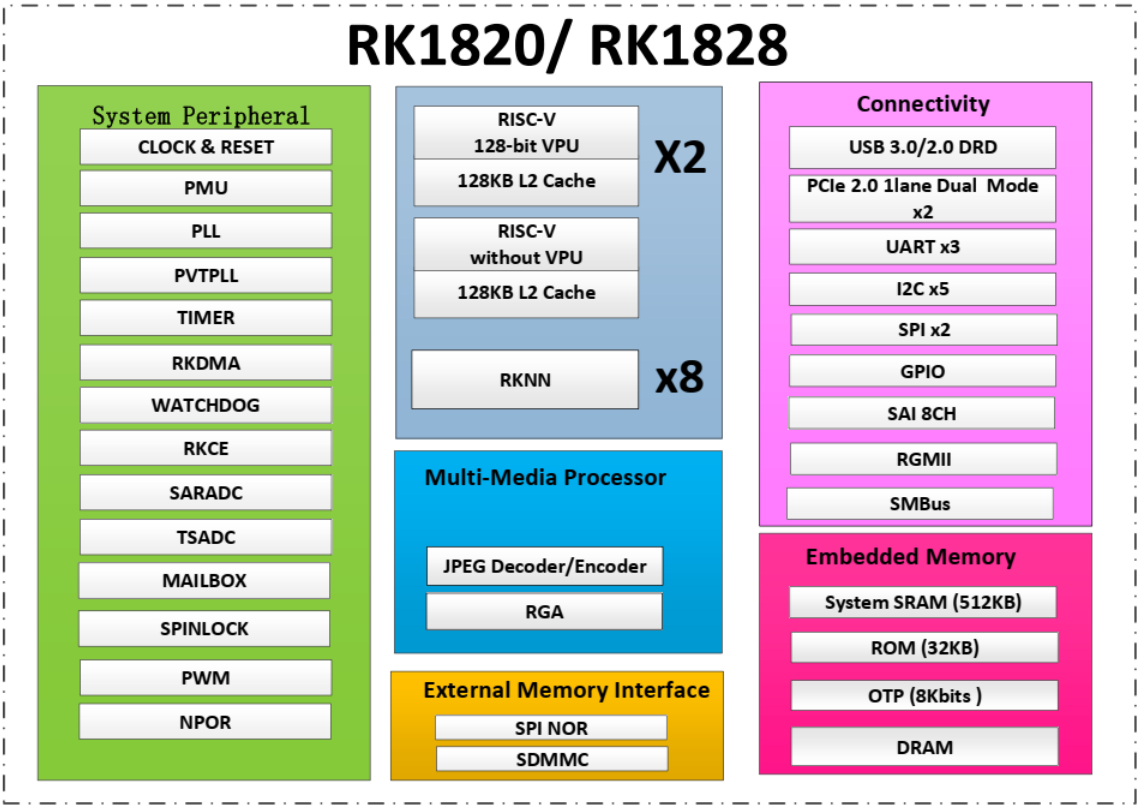

Fig. 1-1 Block Diagram

Chapter 2 Package Information

2.1 Order Information

Orderable Device	RoHS status	Package	Package Q'ty	Device Feature
RK1820	RoHS	FCBGA 746L	420pcs	AI Co-processor
RK1828	RoHS	FCBGA 746L	420pcs	AI Co-processor

2.2 Top Marking

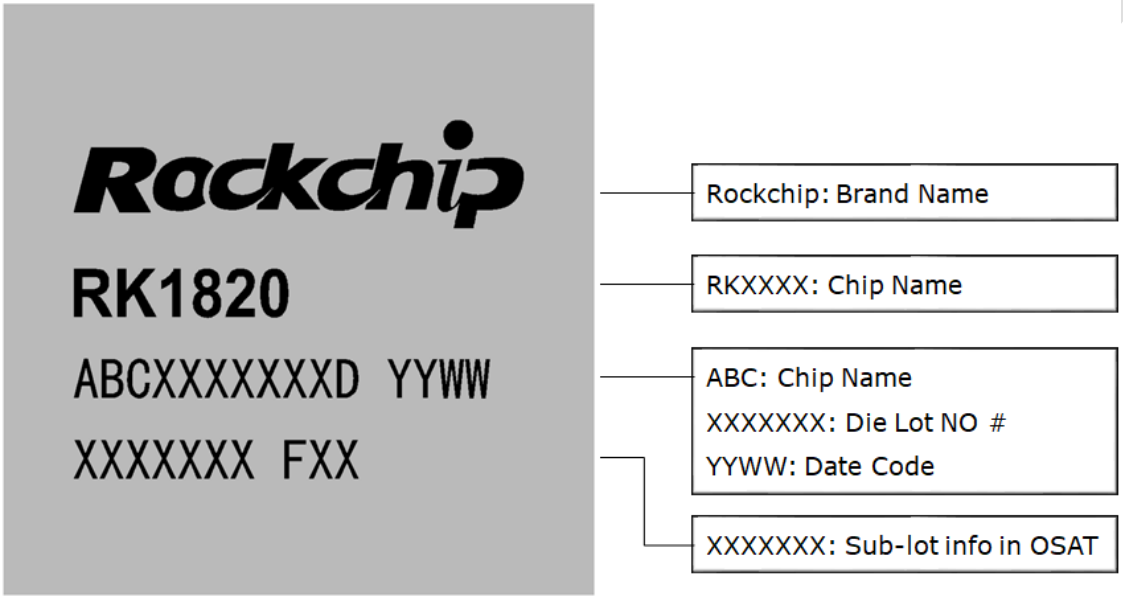

Fig. 2-1 RK1820 Package Definition

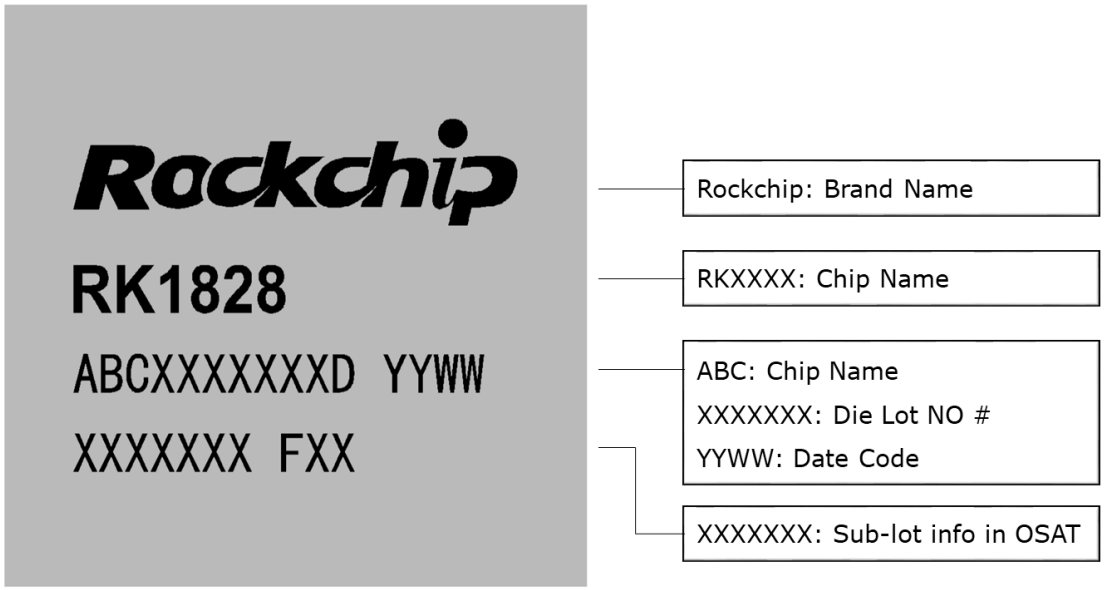

Fig. 2-2 RK1828 Package Definition

2.3 Package Dimension

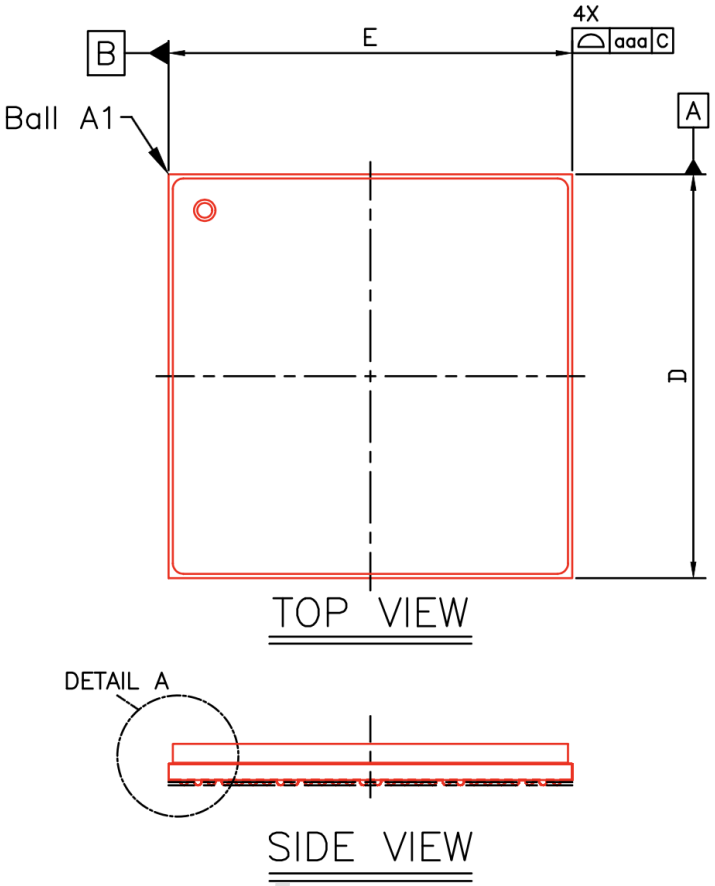

Fig. 2-3 RK1820/ RK1828 Package Top View and Side View

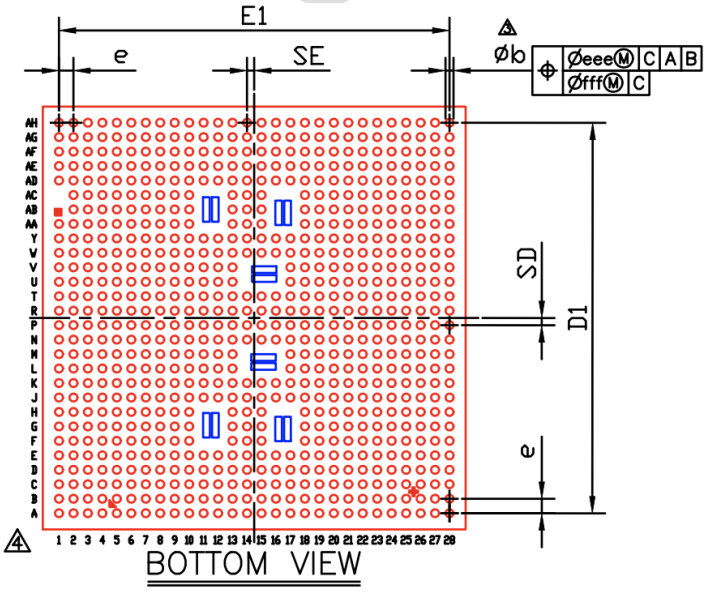

Fig. 2-4 RK1820/ RK1828 Package Bottom View

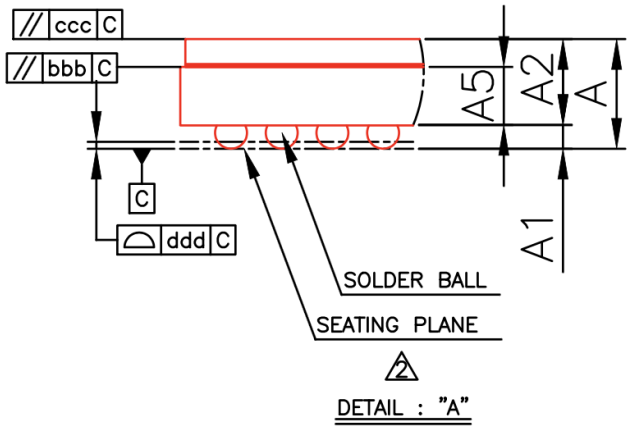

Fig. 2-5 RK1820/ RK1828 PKG Detail A

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.858	1.969	2.083	0.073	0.078	0.082
A1	0.200	0.260	0.320	0.008	0.010	0.013
A2	1.600	1.699	1.801	0.063	0.067	0.071
A5	0.654	0.754	0.854	0.026	0.030	0.034
E	18.850	19.000	19.150	0.742	0.748	0.754
D	18.850	19.000	19.150	0.742	0.748	0.754
E1	---	17.550	---	---	0.691	---
D1	---	17.550	---	---	0.691	---
e	---	0.650	---	---	0.026	---
b	0.310	0.360	0.410	0.012	0.014	0.016
aaa	0.150			0.006		
bbb	0.100			0.004		
ccc	0.350			0.014		
ddd	0.100			0.004		
eee	0.200			0.008		
fff	0.080			0.003		
MD/ME	28/28					
SE	0.325			0.013		
SD	0.325			0.013		

NOTE :
1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
5. BALL PLACEMENT USE 0.350 mm SOLDER BALL. BGA PAD SOLDER MASK OPENING = 0.300 mm.

Fig. 2-6 RK1820/ RK1828 Package Dimension

2.4 MSL Information

Moisture sensitivity Level: MSL3

2.5 Lead Finish/Ball Material Information

Lead Finish/Ball material: SnAgCu

2.6 Pin Number List

Table 2-1 RK1820/ RK1828 Pin Number Order Information

Pin Name	Pin#	Pin Name	Pin#
VSS_0	A1	VSS_177	P28
I2C2_SDA_M0/UART1_RTSN_M0/PCIE0_PERSTN_M0/SAI_SCLK_M0/GPIO0_B6_d	A2	ETH_TXD3/I2C0_SDA_M1/SPI1_MISO_M2/GPIO1_B1_d	R1

Pin Name	Pin#	Pin Name	Pin#
JTAG_TMS_M0/UART1_RX_M0/SAI_SDI3_M0/SAI_SDO0_M0/GPIO0_C1_d	A3	ETH_TXD2/I2C0_SCL_M1/SPI1_MOSI_M2/GPIO1_B0_d	R2
JTAG_TMS_M1/UART0_RX/GPIO0_C3_u	A4	ETH_MDC/PCIE0_PERSTN_M2/GPIO1_C2_d	R3
VSS_1	A5	ETH_MDIO/PCIE0_CLKREQN_M2/GPIO1_C3_d	R4
VDD_LOGIC_0	A6	VSS_178	R5
VSS_2	A7	VSS_179	R6
VDD_LOGIC_1	A8	VSS_180	R7
VSS_3	A9	VSS_181	R8
DRAM_VEQ_1V4_0	A10	VDD_TOP_9	R9
VSS_4	A11	VSS_182	R10
DRAM_VEQ_1V4_1	A12	VSS_183	R11
VSS_5	A13	VSS_184	R12
DRAM_VPPEX_2V5_0	A14	VSS_185	R13
DRAM_VDD_1V2_0	A15	VSS_186	R14
VSS_6	A16	VSS_187	R15
DRAM_VCC_1V1_0	A17	VSS_188	R16
VSS_7	A18	VSS_189	R17
DRAM_VCC_1V1_1	A19	VSS_190	R18
VSS_8	A20	VSS_191	R19
VSS_SENSE_N	A21	VSS_192	R20
VDD_LOGIC_2	A22	VSS_193	R21
VSS_9	A23	VSS_194	R22
VDD_LOGIC_3	A24	VSS_195	R23
VSS_10	A25	VSS_196	R24
VDD_LOGIC_4	A26	VSS_197	R25
VSS_11	A27	VSS_198	R26
VSS_12	A28	VSS_199	R27
I2C3_SDA_M0/PWM_CH7_M0/SPI1_MOSI_M0/SMBUS_SDA_M0/SAI_SDI1_M0/SAI_SDO2_M0/GPIO0_B4_d	B1	VSS_200	R28
I2C2_SCL_M0/UART1_CTSN_M0/PCIE0_WAKEN_M0/SMBUS_ALERT_M0/SAI_SDI0_M0/SAI_SDO3_M0/GPIO0_B5_d	B2	ETH_CLK_25M_OUT/I2C2_SCL_M1/SAI_SDO2_M2/UART2_CTSN_M0/SPI1_CS1N_M1/GPIO1_C4_d	T1
JTAG_TCK_M0/UART1_TX_M0/SAI_MCLK_M0/GPIO0_C0_d	B3	ETH_MCLK/I2C2_SDA_M1/SAI_SDO1_M2/UART2_RTSN_M0/PWM_CH0_M2/SPI1_MOSI_M1/GPIO1_C5_d	T2
JTAG_TCK_M1/UART0_TX/GPIO0_C2_u	B4	ETH_PTP_REFCLK/SAI_MCLK_M2/PWM_CH1_M2/SPI1_MISO_M1/GPIO1_C6_d	T3
VSS_13	B5	VSS_201	T4
VDD_LOGIC_5	B6	VSS_202	T5
VSS_14	B7	VSS_203	T6
VDD_LOGIC_6	B8	VSS_204	T7
VSS_15	B9	VSS_205	T8
DRAM_VEQ_1V4_2	B10	VDD_TOP_10	T9
VSS_16	B11	VSS_206	T10
DRAM_VEQ_1V4_3	B12	VDD_LOGIC_87	T11
VSS_17	B13	VDD_LOGIC_88	T12
DRAM_VPPEX_2V5_1	B14	VDD_LOGIC_89	T13
DRAM_VDD_1V2_1	B15	VSS_207	T14
VSS_18	B16	VSS_208	T15

Pin Name	Pin#	Pin Name	Pin#
DRAM_VCC_1V1_2	B17	VSS_209	T16
VSS_19	B18	VDD_LOGIC_90	T17
DRAM_VCC_1V1_3	B19	VDD_LOGIC_91	T18
VSS_20	B20	VDD_LOGIC_92	T19
VDD_LOGIC_SENSE_P	B21	VDD_LOGIC_93	T20
VSS_21	B22	VDD_LOGIC_94	T21
VDD_LOGIC_7	B23	VDD_LOGIC_95	T22
VSS_22	B24	VDD_LOGIC_96	T23
VDD_LOGIC_8	B25	VDD_LOGIC_97	T24
VSS_23	B26	VDD_LOGIC_98	T25
VDD_LOGIC_9	B27	VDD_LOGIC_99	T26
VSS_24	B28	VDD_LOGIC_100	T27
PWM_CH4_M0/SPI1_CS0N_M0/GPIO0_B1_d	C1	VDD_LOGIC_101	T28
PWM_CH5_M0/SPI1_MISO_M0/GPIO0_B2_d	C2	ETH_PPSCLK/PCIE1_WAKEN_M0/SAI_SCLK_M2/PWM_CH2_M2/SPI1_CS0N_M1/GPIO1_C7_d	U1
I2C3_SCL_M0/PWM_CH6_M0/SPI1_CLK_M0/SMBUS_SCL_M0/SAI_SDI2_M0/SAI_SDO1_M0/GPIO0_B3_d	C3	ETH_PPSTRIG/PCIE1_PERSTN_M0/SAI_LRCK_M2/PWM_CH3_M2/SPI1_CLK_M1/GPIO1_D0_d	U2
PCIE0_CLKREQN_M0/SAI_LRCK_M0/GPIO0_B7_d	C4	PCIE1_CLKREQN_M0/SAI_SDI0_M2/UART1_RTSN_M1/PWM_CH4_M2/SPI0_CLK_M1/GPIO1_D1_d	U3
VSS_25	C5	SARADC_IN2/SMBUS_SCL_M1/I2C3_SCL_M1/SAI_SDO3_M2/UART1_TX_M1/PWM_CH6_M1/SPI0_MOSI_M1/GPIO1_D2_d	U4
VDD_LOGIC_10	C6	VSS_210	U5
VSS_26	C7	OSC_AVDD1V8	U6
VDD_LOGIC_11	C8	PLL_AVDD1V8	U7
VSS_27	C9	SARADC_AVDD1V8	U8
DRAM_VEQ_1V4_4	C10	VSS_211	U9
VSS_28	C11	VSS_212	U10
DRAM_VEQ_1V4_5	C12	VSS_213	U11
VSS_29	C13	VSS_214	U12
DRAM_VPPEX_2V5_2	C14	VSS_215	U13
DRAM_VDD_1V2_2	C15	VSS_216	U17
VSS_30	C16	VSS_217	U18
DRAM_VCC_1V1_4	C17	VSS_218	U19
VSS_31	C18	VSS_219	U20
DRAM_VCC_1V1_5	C19	VSS_220	U21
VSS_32	C20	VSS_221	U22
VSS_33	C21	VSS_222	U23
VDD_LOGIC_12	C22	VSS_223	U24
VSS_34	C23	VSS_224	U25
VDD_LOGIC_13	C24	VSS_225	U26
VSS_35	C25	VSS_226	U27
VDD_LOGIC_14	C26	VSS_227	U28
VSS_36	C27	SARADC_IN3/SMBUS_SDA_M1/I2C3_SDA_M1/UART1_RX_M1/PWM_CH7_M1/SPI0_MISO_M1/GPIO1_D3_d	V1
VDD_LOGIC_15	C28	SARADC_IN4/SMBUS_ALERT_M1/SAI_SDO0_M2/UART1_CTSN_M1/SPI0_CS0N_M1/GPIO1_D4_d	V2

Pin Name	Pin#	Pin Name	Pin#
I2C0_SCL_M0/SPI0_CS0N_M0/GPIO0_A5_d	D1	SARADC_IN5/PCIE0_CLKREQN_M1/SAI_SDI1_M2/PWM_CH5_M2/SPI0_CS1N_M1/GPIO1_D5_d	V3
I2C0_SDA_M0/SPI0_MISO_M0/GPIO0_A6_d	D2	SARADC_IN6/PCIE0_PERSTN_M1/I2C4_SCL_M0/SAI_SDI2_M2/UART2_TX_M0/PWM_CH6_M2/ETH_TESTRXCLK_OUT/GPIO1_D6_d	V4
I2C1_SCL_M0/PWM_CH2_M0/SPI0_CLK_M0/GPIO0_A7_d	D3	VSS_228	V5
I2C1_SDA_M0/PWM_CH3_M0/SPI0_MOSI_M0/GPIO0_B0_d	D4	VDD_PMU_0V9	V6
VSS_37	D5	PLL_AVDD0V9	V7
VDD_LOGIC_16	D6	PLL_AVSS	V8
VSS_38	D7	VSS_229	V9
VDD_LOGIC_17	D8	VDD_LOGIC_102	V10
VSS_39	D9	VDD_LOGIC_103	V11
DRAM_VEQ_1V4_6	D10	VDD_LOGIC_104	V12
VSS_40	D11	VSS_230	V13
DRAM_VEQ_1V4_7	D12	VSS_231	V17
VSS_41	D13	VDD_LOGIC_105	V18
DRAM_VPPEX_2V5_3	D14	VDD_LOGIC_106	V19
DRAM_VDD_1V2_3	D15	VDD_LOGIC_107	V20
VSS_42	D16	VDD_LOGIC_108	V21
DRAM_VCC_1V1_6	D17	VDD_LOGIC_109	V22
DRAM_VCC_1V1_7	D18	VDD_LOGIC_110	V23
VSS_43	D19	VDD_LOGIC_111	V24
VSS_44	D20	VDD_LOGIC_112	V25
VDD_LOGIC_18	D21	VDD_LOGIC_113	V26
VSS_45	D22	VDD_LOGIC_114	V27
VDD_LOGIC_19	D23	VDD_LOGIC_115	V28
VSS_46	D24	SARADC_IN0_BOOT	W1
VDD_LOGIC_20	D25	SARADC_IN1	W2
VSS_47	D26	VSS_232	W3
VDD_LOGIC_21	D27	SARADC_IN7/PCIE0_WAKEN_M1/I2C4_SDA_M0/SAI_SDI3_M2/UART2_RX_M0/PWM_CH7_M2/ETH_TESTRXD_OUT/GPIO1_D7_d	W4
VSS_48	D28	AVSS_0	W5
PWR_CTRL0/TEST_CLK_OUT1/GPIO0_A2_z	E1	AVSS_1	W6
PWR_CTRL1/PWM_CH0_M0/SPI1_CS1N_M0/PCIE1_BUTTONRSTN/GPIO0_A3_d	E2	Combo_PHY_AVDD1V8	W7
PWR_CTRL2/PWM_CH1_M0/SPI0_CS1N_M0/PCIE0_BUTTONRSTN/GPIO0_A4_d	E3	Combo_PHY_AVDD0V9_0	W8
REF_CLK_OUT/TEST_CLK_OUT0/GPIO0_A0_d	E4	VSS_233	W9
VSS_49	E5	VSS_234	W10
VSS_50	E6	VSS_235	W11
VDD_LOGIC_22	E7	VSS_236	W12
VDD_LOGIC_23	E8	VSS_237	W13
VSS_51	E9	VDD_TOP_11	W14
DRAM_VEQ_1V4_8	E10	VDD_TOP_12	W15
DRAM_VEQ_1V4_9	E11	VSS_238	W16
VSS_52	E12	VSS_239	W17
VSS_53	E13	VSS_240	W18

Pin Name	Pin#	Pin Name	Pin#
DRAM_VPPEX_2V5_4	E14	VSS_241	W19
DRAM_VDD_1V2_4	E15	VSS_242	W20
VSS_54	E16	VSS_243	W21
DRAM_VCC_1V1_8	E17	VSS_244	W22
DRAM_VCC_1V1_9	E18	VSS_245	W23
VSS_55	E19	VSS_246	W24
VDD_LOGIC_24	E20	VSS_247	W25
VDD_LOGIC_25	E21	VSS_248	W26
VDD_LOGIC_26	E22	VSS_249	W27
VDD_LOGIC_27	E23	VSS_250	W28
VDD_LOGIC_28	E24	VSS_251	Y1
VDD_LOGIC_29	E25	VSS_252	Y2
VDD_LOGIC_30	E26	VSS_253	Y3
VDD_LOGIC_31	E27	AVSS_2	Y4
VDD_LOGIC_32	E28	AVSS_3	Y5
NPOR_DET	F1	AVSS_4	Y6
TSADC_CTRL/GPIO0_A1_z	F2	USB_AVDD0V9	Y7
VSS_56	F3	Combo_PHY_AVDD0V9_1	Y8
FSPI_D3/UART2_RX_M1/GPIO0_C7_u	F4	VSS_254	Y9
VSS_57	F5	DRAM_VCC_1V1_16	Y10
VSS_58	F6	DRAM_VCC_1V1_17	Y11
VDD_LOGIC_33	F7	DRAM_VCC_1V1_18	Y12
VDD_LOGIC_34	F8	VSS_255	Y13
VSS_59	F9	VDD_TOP_13	Y14
DRAM_VEQ_1V4_10	F10	VSS_256	Y15
VSS_60	F13	DRAM_VEQ_1V4_16	Y16
VDD_LOGIC_35	F14	DRAM_VEQ_1V4_17	Y17
VDD_LOGIC_36	F15	DRAM_VEQ_1V4_18	Y18
DRAM_VCC_1V1_10	F18	VSS_257	Y19
VSS_61	F19	VDD_LOGIC_116	Y20
VDD_LOGIC_37	F20	VDD_LOGIC_117	Y21
VSS_62	F21	VDD_LOGIC_118	Y22
VSS_63	F22	VDD_LOGIC_119	Y23
VSS_64	F23	VDD_LOGIC_120	Y24
VSS_65	F24	VDD_LOGIC_121	Y25
VSS_66	F25	VDD_LOGIC_122	Y26
VSS_67	F26	VDD_LOGIC_123	Y27
VSS_68	F27	VDD_LOGIC_124	Y28
VSS_69	F28	OSC_XIN	AA1
FSPI_D1/UART2_RTSN_M1/GPIO0_C5_u	G1	OSC_XOUT	AA2
FSPI_D2/UART2_TX_M1/GPIO0_C6_u	G2	AVSS_5	AA3
FSPI_CLK_OUT/GPIO0_D1_d	G3	PCIE1_REFCLKP	AA4
FSPI_CSN1_u	G4	AVSS_6	AA5
VSS_70	G5	USB_AVDD3V3	AA6
VSS_71	G6	AVSS_7	AA7
VSS_72	G7	AVSS_8	AA8
VDD_LOGIC_38	G8	VSS_258	AA9
VSS_73	G9	DRAM_VCC_1V1_19	AA10
DRAM_VEQ_1V4_11	G10	VSS_259	AA13

Pin Name	Pin#	Pin Name	Pin#
VSS_74	G13	VDD_TOP_14	AA14
VSS_75	G14	VSS_260	AA15
VSS_76	G15	DRAM_VEQ_1V4_19	AA18
DRAM_VCC_1V1_11	G18	VSS_261	AA19
VSS_77	G19	VDD_LOGIC_125	AA20
VDD_LOGIC_39	G20	VSS_262	AA21
VDD_LOGIC_40	G21	VSS_263	AA22
VDD_LOGIC_41	G22	VSS_264	AA23
VDD_LOGIC_42	G23	VSS_265	AA24
VDD_LOGIC_43	G24	VSS_266	AA25
VDD_LOGIC_44	G25	VSS_267	AA26
VDD_LOGIC_45	G26	VSS_268	AA27
VDD_LOGIC_46	G27	VSS_269	AA28
VDD_LOGIC_47	G28	AVSS_9	AB2
VSS_78	H1	AVSS_10	AB3
FSPI_CSN0/GPIO0_D0_u	H2	PCIE1_REFCLKN	AB4
VSS_79	H3	AVSS_11	AB5
FSPI_D0/UART2_CTSN_M1/GPIO0_C4_u	H4	OTP_AVDD1V8	AB6
SDMMC_DETN/I2C3_SDA_M2/SAI_MCLK_M1/PCIE1_CLKREQN_M1/SDMMC_TESTCLK_OUT/GPIO1_A5_u	H5	USB_AVDD1V8	AB7
VSS_80	H6	VSS_270	AB8
VSS_81	H7	VSS_271	AB9
VSS_82	H8	DRAM_VCC_1V1_20	AB10
VSS_83	H9	VSS_272	AB13
DRAM_VEQ_1V4_12	H10	VSS_273	AB14
VSS_84	H13	VSS_274	AB15
VDD_TOP_0	H14	DRAM_VEQ_1V4_20	AB18
VSS_85	H15	VSS_275	AB19
DRAM_VCC_1V1_12	H18	VDD_LOGIC_126	AB20
VSS_86	H19	VDD_LOGIC_127	AB21
VDD_LOGIC_48	H20	VDD_LOGIC_128	AB22
VSS_87	H21	VDD_LOGIC_129	AB23
VSS_88	H22	VDD_LOGIC_130	AB24
VSS_89	H23	VDD_LOGIC_131	AB25
VSS_90	H24	VDD_LOGIC_132	AB26
VSS_91	H25	VDD_LOGIC_133	AB27
VSS_92	H26	VDD_LOGIC_134	AB28
VSS_93	H27	DRAM_VCC_1V1_21	AC10
VSS_94	H28	VSS_278	AC13
SDMMC_D3/SAI_SDI3_M1/UART1_RX_M2/GPIO0_D5_u	J1	VDD_LOGIC_136	AC14
SDMMC_D5/I2C4_SDA_M2/SAI_LRCK_M1/UART2_RX_M2/SMBUS_SDA_M2/GPIO0_D7_u	J2	VDD_LOGIC_137	AC15
SDMMC_CLK_OUT/SAI_SDO1_M1/FSPI_TESTCLK_OUT/GPIO1_A3_d	J3	DRAM_VEQ_1V4_21	AC18
VSS_95	J4	VSS_279	AC19
VSS_96	J5	PCIE1_TXN/USB0_DRD_SSTXN_M1	AC2
VSS_97	J6	VDD_LOGIC_138	AC20
VSS_98	J7	VSS_280	AC21
VSS_99	J8	VSS_281	AC22

Pin Name	Pin#	Pin Name	Pin#
VSS_100	J9	VSS_282	AC23
DRAM_VEQ_1V4_13	J10	VSS_283	AC24
DRAM_VEQ_1V4_14	J11	VSS_284	AC25
DRAM_VEQ_1V4_15	J12	VSS_285	AC26
VSS_101	J13	VSS_286	AC27
VDD_TOP_1	J14	VSS_287	AC28
VSS_102	J15	PCIE1_TXP/USB0_DRD_SSTXP_M1	AC3
DRAM_VCC_1V1_13	J16	AVSS_12	AC4
DRAM_VCC_1V1_14	J17	PCIE0_REFCLKP	AC5
DRAM_VCC_1V1_15	J18	AVSS_13	AC6
VSS_103	J19	VSS_276	AC7
VDD_LOGIC_49	J20	VDD_LOGIC_135	AC8
VDD_LOGIC_50	J21	VSS_277	AC9
VDD_LOGIC_51	J22	PCIE1_RXN/USB0_DRD_SSRXN_M1	AD1
VDD_LOGIC_52	J23	DRAM_VCC_1V1_22	AD10
VDD_LOGIC_53	J24	DRAM_VCC_1V1_23	AD11
VDD_LOGIC_54	J25	VSS_290	AD12
VDD_LOGIC_55	J26	VSS_291	AD13
VDD_LOGIC_56	J27	DRAM_VDD_1V2_5	AD14
VDD_LOGIC_57	J28	DRAM_VPPEX_2V5_5	AD15
SDMMC_D0/SAI_SDO2_M1/UART1_CTSN_M2/GPIO0_D2_u	K1	VSS_292	AD16
SDMMC_D4/I2C4_SCL_M2/SAI_SCLK_M1/UART2_TX_M2/SMBUS_SCL_M2/GPIO0_D6_u	K2	DRAM_VEQ_1V4_22	AD17
VSS_104	K3	DRAM_VEQ_1V4_23	AD18
SDMMC_CMD/FSPI_TESTDATA_OUT/GPIO1_A2_u	K4	VSS_293	AD19
VSS_105	K5	PCIE1_RXP/USB0_DRD_SSRXP_M1	AD2
VSS_106	K6	VDD_LOGIC_141	AD20
VCCIO0_VCC3V3	K7	VDD_LOGIC_142	AD21
VSS_107	K8	VDD_LOGIC_143	AD22
VSS_108	K9	VDD_LOGIC_144	AD23
VSS_109	K10	VDD_LOGIC_145	AD24
VSS_110	K11	VDD_LOGIC_146	AD25
VSS_111	K12	VDD_LOGIC_147	AD26
VSS_112	K13	VDD_LOGIC_148	AD27
VDD_TOP_2	K14	VDD_LOGIC_149	AD28
VDD_TOP_3	K15	AVSS_14	AD3
VSS_113	K16	PCIE0_REFCLKN	AD4
VSS_114	K17	AVSS_15	AD5
VSS_115	K18	VSS_288	AD6
VSS_116	K19	VDD_LOGIC_139	AD7
VSS_117	K20	VDD_LOGIC_140	AD8
VSS_118	K21	VSS_289	AD9
VSS_119	K22	PCIE0_TXP/USB0_DRD_SSTXP_M0	AE1
VSS_120	K23	DRAM_VCC_1V1_24	AE10
VSS_121	K24	VSS_297	AE11
VSS_122	K25	DRAM_VCC_1V1_25	AE12
VSS_123	K26	VSS_298	AE13
VSS_124	K27	DRAM_VDD_1V2_6	AE14

Pin Name	Pin#	Pin Name	Pin#
VSS_125	K28	DRAM_VPPEX_2V5_6	AE15
SDMMC_D2/SAI_SDI2_M1/UART1_TX_M2/GPIO0_D4_u	L1	VSS_299	AE16
SDMMC_D1/SAI_SDO3_M1/UART1_RTSN_M2/GPIO0_D3_u	L2	DRAM_VEQ_1V4_24	AE17
SDMMC_RSTN/I2C3_SCL_M2/SAI_SDI1_M1/PCIE1_PERSTN_M1/SDMMC_TESTDATA_OUT/GPIO1_A4_u	L3	DRAM_VEQ_1V4_25	AE18
ETH_RXCLK/I2C4_SDA_M1/GPIO1_C1_d	L4	VSS_300	AE19
VSS_126	L5	PCIE0_TXN/USB0_DRD_SSTXN_M0	AE2
VSS_127	L6	VSS_301	AE20
VCCIO1	L7	VDD_LOGIC_152	AE21
TVSS	L8	VSS_302	AE22
VSS_128	L9	VDD_LOGIC_153	AE23
VDD_LOGIC_58	L10	VSS_303	AE24
VDD_LOGIC_59	L11	VDD_LOGIC_154	AE25
VDD_LOGIC_60	L12	VSS_304	AE26
VSS_129	L13	VDD_LOGIC_155	AE27
VSS_130	L17	VSS_305	AE28
VDD_LOGIC_61	L18	AVSS_16	AE3
VDD_LOGIC_62	L19	USB0_DRD_ID	AE4
VDD_LOGIC_63	L20	VSS_294	AE5
VDD_LOGIC_64	L21	VDD_LOGIC_150	AE6
VDD_LOGIC_65	L22	VSS_295	AE7
VDD_LOGIC_66	L23	VDD_LOGIC_151	AE8
VDD_LOGIC_67	L24	VSS_296	AE9
VDD_LOGIC_68	L25	AVSS_17	AF1
VDD_LOGIC_69	L26	PCIE0_RXP/USB0_DRD_SSRXP_M0	AF2
VDD_LOGIC_70	L27	AVSS_18	AF3
VDD_LOGIC_71	L28	USB0_DRD_VBUSDET	AF4
SDMMC_D6/I2C2_SCL_M2/SAI_SDI0_M1/UART2_CTSN_M2/SMBUS_ALERT_M2/GPIO1_A0_u	M1	VSS_306	AF5
SDMMC_D7/I2C2_SDA_M2/SAI_SDO0_M1/UART2_RTSN_M2/PCIE1_WAKEN_M1/GPIO1_A1_u	M2	VDD_LOGIC_PDN_0	AF6
ETH_RXD1/PWM_CH4_M1/SPI0_CS1N_M2/GPIO1_B5_d	M3	VSS_307	AF7
ETH_RXCTL/PCIE0_WAKEN_M2/PWM_CH5_M1/GPIO1_C0_d	M4	VDD_LOGIC_156	AF8
VSS_131	M5	VSS_308	AF9
VSS_132	M6	DRAM_VCC_1V1_26	AF10
VSS_133	M7	VSS_309	AF11
VSS_134	M8	DRAM_VCC_1V1_27	AF12
VSS_135	M9	VSS_310	AF13
VSS_136	M10	DRAM_VDD_1V2_7	AF14
VSS_137	M11	DRAM_VPPEX_2V5_7	AF15
VSS_138	M12	VSS_311	AF16
VSS_139	M13	DRAM_VEQ_1V4_26	AF17
VSS_140	M17	VSS_312	AF18
VSS_141	M18	DRAM_VEQ_1V4_27	AF19
VSS_142	M19	VSS_313	AF20
VSS_143	M20	VSS_314	AF21
VSS_144	M21	VDD_LOGIC_157	AF22

Pin Name	Pin#	Pin Name	Pin#
VSS_145	M22	VSS_315	AF23
VSS_146	M23	VDD_LOGIC_158	AF24
VSS_147	M24	VSS_316	AF25
VSS_148	M25	VDD_LOGIC_159	AF26
VSS_149	M26	VSS_317	AF27
VSS_150	M27	VDD_LOGIC_160	AF28
VSS_151	M28	PCIE0_RXN/USB0_DRD_SSRXN_M0	AG1
ETH_TXCTL/PCIE1_CLKREQN_M2/PWM_CH2_M1/ SPI0_CLK_M2/GPIO1_B2_d	N1	USB0_DRD_DP	AG2
ETH_TXCLK/I2C1_SCL_M1/SPI1_CLK_M2/GPIO1_ B3_d	N2	USB1_DRD_DP	AG3
VSS_152	N3	AVSS_19	AG4
ETH_RXD0/PWM_CH3_M1/SPI0_CS0N_M2/GPIO1 _B4_d	N4	VSS_318	AG5
VSS_153	N5	VDD_LOGIC_161	AG6
VSS_154	N6	VSS_319	AG7
VCCIO2	N7	VDD_LOGIC_162	AG8
VCCIO2	N7	VSS_320	AG9
VSS_155	N8	DRAM_VCC_1V1_28	AG10
VDD_TOP_4	N9	VSS_321	AG11
VSS_156	N10	DRAM_VCC_1V1_29	AG12
VDD_LOGIC_72	N11	VSS_322	AG13
VDD_LOGIC_73	N12	DRAM_VDD_1V2_8	AG14
VDD_LOGIC_74	N13	DRAM_VPPEX_2V5_8	AG15
VSS_157	N14	VSS_323	AG16
VSS_158	N15	DRAM_VEQ_1V4_28	AG17
VSS_159	N16	VSS_324	AG18
VDD_LOGIC_75	N17	DRAM_VEQ_1V4_29	AG19
VDD_LOGIC_76	N18	VSS_325	AG20
VDD_LOGIC_77	N19	VDD_LOGIC_163	AG21
VDD_LOGIC_78	N20	VSS_326	AG22
VDD_LOGIC_79	N21	VDD_LOGIC_164	AG23
VDD_LOGIC_80	N22	VSS_327	AG24
VDD_LOGIC_81	N23	VDD_LOGIC_165	AG25
VDD_LOGIC_82	N24	VSS_328	AG26
VDD_LOGIC_83	N25	VDD_LOGIC_166	AG27
VDD_LOGIC_84	N26	VSS_329	AG28
VDD_LOGIC_85	N27	AVSS_20	AH1
VDD_LOGIC_86	N28	USB0_DRD_DM	AH2
ETH_TXD1/PCIE1_PERSTN_M2/PWM_CH1_M1/SP I0_MISO_M2/GPIO1_A7_d	P1	USB1_DRD_DM	AH3
ETH_TXD0/PCIE1_WAKEN_M2/PWM_CH0_M1/SPI 0_MOSI_M2/GPIO1_A6_d	P2	AVSS_21	AH4
ETH_RXD2/I2C1_SDA_M1/SPI1_CS0N_M2/GPIO1 _B6_d	P3	VSS_330	AH5
VSS_160	P4	VDD_LOGIC_167	AH6
ETH_RXD3/I2C4_SCL_M1/SPI1_CS1N_M2/GPIO1 _B7_d	P5	VSS_331	AH7
VSS_161	P6	VDD_LOGIC_PDN_1	AH8
VCCIO3	P7	VSS_332	AH9
VSS_162	P8	DRAM_VCC_1V1_30	AH10
VDD_TOP_5	P9	VSS_333	AH11

Pin Name	Pin#	Pin Name	Pin#
VSS_163	P10	DRAM_VCC_1V1_31	AH12
VSS_164	P11	VSS_334	AH13
VSS_165	P12	DRAM_VDD_1V2_9	AH14
VSS_166	P13	DRAM_VPPEX_2V5_9	AH15
DRAM_VMONI	P14	VSS_335	AH16
VDD_TOP_6	P15	DRAM_VEQ_1V4_30	AH17
VDD_TOP_7	P16	VSS_336	AH18
VSS_167	P17	DRAM_VEQ_1V4_31	AH19
VSS_168	P18	VSS_337	AH20
VDD_TOP_8	P19	VSS_338	AH21
VSS_169	P20	VDD_LOGIC_168	AH22
VSS_170	P21	VSS_339	AH23
VSS_171	P22	VDD_LOGIC_169	AH24
VSS_172	P23	VSS_340	AH25
VSS_173	P24	VDD_LOGIC_170	AH26
VSS_174	P25	VSS_341	AH27
VSS_175	P26	VSS_342	AH28
VSS_176	P27		

Chapter 3 Electrical Specification

3.1 Absolute Ratings

The below table provides the absolute ratings.

Absolute maximum or minimum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

Table 3-1 Absolute Ratings

Parameters	Related Power Group	Min	Max	Unit
Supply voltage for DRAM VEQ	DRAM_VEQ_1V4	-0.3	1.75	V
Supply voltage for DRAM VCC	DRAM_VCC_1V1	-0.3	1.54	V
Supply voltage for DRAM VPPEX	DRAM_VPPEX_2V5	-0.3	3.0	V
Supply voltage for DRAM VDD	DRAM_VDD_1V2	-0.3	1.54	V
0.9V supply voltage	VDD_TOP VDD_PMU_0V9 VDD_LOGIC PLL_AVDD_0V9 USB_AVDD_0V9 Combo_PHY_AVDD0V9_0 Combo_PHY_AVDD0V9_1	-0.3	1.1	V
1.8V supply voltage	SARADC_AVDD1V8 USB_AVDD1V8 Combo_PHY_AVDD1V8 PLL_AVDD1V8 OTP_AVDD1V8 OSC_AVDD1V8	-0.3	2.0	V
3.3V supply voltage	USB_AVDD3V3	-0.3	3.8	V
3.3V supply voltage for VCCIO	VCCIO0_VCC3V3	-0.3	3.8	V
1.8V supply voltage for VCCIO	VCCIO1	-0.3	2.5	V
1.8V/3.3V supply voltage for VCCIO	VCCIO2 VCCIO3	-0.3	3.8	V
Storage Temperature	Tstg	-40	125	℃
Max Conjunction Temperature	Tj	NA	125	℃

3.2 Recommended Operating Condition

Following table describes the recommended operating condition.

Table 3-2 Recommended Operating Condition

Parameters	Related Power Group	Min	Typ	Max	Unit
Supply voltage for DRAM VEQ	DRAM_VEQ_1V4	1.365	1.4	1.435	V
Supply voltage for DRAM VCC	DRAM_VCC_1V1	1.073	1.1	1.128	V
Supply voltage for DRAM VPPEX	DRAM_VPPEX_2V5	2.438	2.5	2.563	V
Supply voltage for DRAM VDD	DRAM_VDD_1V2	1.17	1.2	1.23	V
0.9V supply voltage	VDD_TOP	0.81	0.9	1.05	V
0.9V supply voltage	VDD_LOGIC	0.81	0.9	1.05	V
0.9V supply voltage	VDD_PMU_0V9	0.855	0.9	0.945	V
0.9V supply voltage	PLL_AVDD_0V9 USB_AVDD_0V9 Combo_PHY_AVDD0V9_0 Combo_PHY_AVDD0V9_1	0.81	0.9	0.99	V
1.8V supply voltage	SARADC_AVDD1V8 USB_AVDD1V8 Combo_PHY_AVDD1V8 PLL_AVDD1V8 OTP_AVDD1V8 OSC_AVDD1V8	1.62	1.8	1.98	V
3.3V supply voltage	USB_AVDD3V3	2.97	3.3	3.63	V
3.3V supply voltage for VCCIO	VCCIO0_VCC3V3	2.97	3.3	3.63	
1.8V supply voltage for VCCIO	VCCIO1	1.62	1.8	1.98	
1.8V/3.3V supply voltage for VCCIO	VCCIO2 VCCIO3	1.62 2.97	1.8 3.3	1.98 3.63	V

Parameters	Related Power Group	Min	Typ	Max	Unit
Max NPU Frequency		NA	NA	1000	MHz
Ambient Operating Temperature	Ta	0	25	85	℃

3.3 DC Characteristics

Table 3-3 DC Characteristics

Parameters		Symbol	Min	Typ	Max	Unit
Digital GPIO @3.3V	Input Low Voltage	Vil	-0.3	NA	0.8	V
	Input High Voltage	Vih	2.0	NA	VCCIO+0.3	V
	Output Low Voltage	Vol	-0.3	NA	0.4	V
	Output High Voltage	Voh	2.4	NA	VCCIO+0.3	V
	Pullup Resistor	Rpu	16	NA	43	Kohm
	Pulldown Resistor	Rpd	16	NA	43	Kohm
Digital GPIO @1.8V	Input Low Voltage	Vil	-0.3	NA	0.35*VCCIO	V
	Input High Voltage	Vih	0.65*VCCIO	NA	VCCIO+0.3	V
	Output Low Voltage	Vol	-0.3	NA	0.4	V
	Output High Voltage	Voh	1.4	NA	VCCIO+0.3	V
	Pullup Resistor	Rpu	16	NA	43	Kohm
	Pulldown Resistor	Rpd	16	NA	43	Kohm

3.4 Electrical Characteristics for General IO

Table 3-4 Electrical Characteristics for Digital General IO

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
Digital GPIO @3.3V	Input leakage current	Ii	Vin = 3.3V or 0V	NA	NA	10	uA
	Tri-state output leakage current	Ioz	Vout = 3.3V or 0V	NA	NA	10	uA
	High level input current	Iih	Vin = 3.3V, pulldown disabled	NA	NA	10	uA
			Vin = 3.3V, pulldown enabled	NA	NA	10	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	NA	NA	10	uA
			Vin = 0V, pullup enabled	NA	NA	10	uA
Digital GPIO @1.8V	Input leakage current	Ii	Vin = 1.8V or 0V	NA	NA	10	uA
	Tri-state output leakage current	Ioz	Vout = 1.8V or 0V	NA	NA	10	uA
	High level input current	Iih	Vin = 1.8V, pulldown disabled	NA	NA	10	uA
			Vin = 1.8V, pulldown enabled	NA	NA	10	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	NA	NA	10	uA
			Vin = 0V, pullup enabled	NA	NA	10	uA

Note: VCCIO and DVDD are both IO power Supply

3.5 Electrical Characteristics for PLL

Table 3-5 Electrical Characteristics for FRAC PLL

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
Frac PLL	Input clock frequency (Frac)	F_{in}	Fin = FREF @1.8V/0.99V	1	NA	1200	MHz
	VCO operating range	F_{vco}	Fvco = Fref * FBDIV @3.3V/0.99V	950	NA	3800	MHz

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
	Output clock frequency	F_{out}	Fout = Fvco/POSTDIV @3.3V/0.99V	19	NA	3800	MHz
	Lock time	T_{lt}	@ 3.3V/0.99V, FREF=24M,REFDIV=1	NA	250	500	Input clock cycles

Notes:

① REFDIV is the input divider value;
② FBDIV is the feedback divider value;
③ POSTDIV is the output divider value

3.6 Electrical Characteristics for USB2.0 Interface

Table 3-6 Electrical Characteristics for USB2.0 Interface

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Transmitter						
Output resistance	ROUT	Classic mode (Vout = 0 or 3.3V)	40.5	45	49.5	ohms
		HS mode (Vout = 0 to 800mV)	40.5	45	49.5	ohms
Output Capacitance	COUT	seen from D+ or D-			3	pF
Output Common Mode Voltage	VM	Classic (LS/FS) mode	1.45	1.65	1.85	V
		HS mode	0.175	0.2	0.225	V
Differential output signal high	VOH	Classic (LS/FS); Io=0mA	2.97	3.3	3.63	V
		Classic (LS/FS); Io=6mA	2.2	2.7	NA	V
		HS mode; Io=0mA	360	400	440	mV
Differential output signal low	VOL	Classic (LS/FS); Io=0mA	-0.33	0	0.33	V
		Classic (LS/FS); Io=6mA	NA	0.3	0.8	V
		HS mode; Io=0mA	-40	0	40	mV
Receiver						
Receiver sensitivity	RSENS	Classic mode	NA	+-250	NA	mV
		HS mode	NA	+-25	NA	mV
Receiver common mode	RCM	Classic mode	0.8	1.65	2.5	V
		HS mode (differential and squelch comparator)	0.1	0.2	0.3	V
		HS mode (disconnect comparator)	0.5	0.6	0.7	V
Input capacitance (seen at D+ or D-)			NA	NA	3	pF
Squelch threshold			100	NA	150	mV
Disconnect threshold			570	600	664	mV

3.7 Electrical Characteristics for SARADC

Table 3-7 Electrical Characteristics for SARADC

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Resolution	ENOB	f_S=1MS/s fclk=24MHz	NA	11.2	13	bit
Analog Input Channel			NA	NA	8	
Analog Input Range	VIN		0	NA	1.8	V
Analog Input maximum voltage					3.3	V
Differential Non-Linearity	DNL		NA	±1	±3	LSB
Integral Non-Linearity	INL		NA	±2	±6	LSB
Conversion Rage	f_S		NA	1	NA	MS/s
Signal to Noise and Distortion Ratio	SINAD	f_S=1MS/s f_{OUT}=1.17KHz	NA	69.2	NA	dB
Total Harmonic Distortion	THD		NA	77.3	NA	dB

3.8 Electrical Characteristics for TSADC

Table 3-8 Electrical Characteristics for TSADC

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Accuracy from -40℃ to 125℃	T_{JACC}		NA	NA	±3.5	℃
Sensing Temperature Range	T_{RANGE}		-40	NA	125	℃
Resolution	T_{LSB}		NA	0.01	NA	℃

3.9 Electrical Characteristics for Multi-PHY

Table 3-9 Electrical Characteristics for PCIe PHY

Parameters	Symbol	Condition	Min	Typ	Max	Unit
Transmitter						
Differential p-pTx voltage swing	$V_{TX-DIFF-PP}$		0.8	NA	1.2	V
Low power differential p-p Tx voltage swing	$V_{TX-DIFF-PP-LOW}$		0.4	NA	1.2	V
Tx de-emphasis level ratio	$R_{TX-DIFF-DC}$		80	NA	120	ohm
Single Ended Output Resistance Matching	$R_{TX-DC-OFFSET}$		NA	NA	5	%
The amount of voltage change allowed during Receiver Detection	$V_{TX-RCV-DETECT}$		NA	NA	600	mV
Output rising time for 20% to 80%	Tr		25	NA	NA	ps
Output falling time for 20% to 80%	Tf		25	NA	NA	ps
AC Coupling Capacitor(USB3.0/PCIE)	C_{TX}		75	NA	200	nF
Unit Interval	UI		399.88	NA	400.12	ps
Input Voltage Swing	$V_{rxdpp-c}$		250	NA	1200	mV
Input differential impedance	R_{rxd-c}		80	NA	120	ohm
Single Ended input Resistance Matching	$T_{rxd-c-ms}$		NA	NA	5	%

Chapter 4 Thermal Management

4.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature has to be below 125℃.

4.2 Package Thermal Characteristics

Table 4-1 provides the thermal resistance characteristics for the package used on the SoC. The resulting simulation data for reference only, please prevail in kind test.

Table 4-1 Thermal Resistance Characteristics

Parameter	Symbol	Value	Unit	Note
Junction-to-ambient thermal resistance	θ_{JA}	11.72	(℃/W)	(1)
Junction-to-board thermal resistance	θ_{JB}	4.38	(℃/W)	(2)
Junction-to-case thermal resistance	θ_{JC}	0.06	(℃/W)	(3)
Thermal characterization parameter	ψ_{JT}	0.19	(℃/W)	(4)

*Note (1): The package-board system is placed in the natural convection (JEDEC JESD51-2 standard), and the 2S2P test-board is designed in accordance with JESD 51-7/JESD 51-9. The actual system design and environment may be different.（The PCB is 4 layers, 114.5 mm*101.5 mm）*

Note (2): ϑ_{JB} is measured in the special environment (JEDEC JESD51-8 standard), and the printed circuit board used to mount the devices is specified in JESD51-7.

Note (3): The thermal resistance ϑ_{JC} is provided in compliance with the JEDEC JESD51-14.

Note (4): ψ_{JT} - The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package, ψ_{JT} is measured in the test environment of ϑ_{JA} (JEDEC JESD51-2 standard).