Rockchip RK2108D Datasheet

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Revision History

Date	Revision	Description
2021-10-20	1.1	Update the max frequency information
2020-06-15	1.0	Initial released

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Chapter 1 Introduction

1.1 Overview

RK2108D is an ultra low power consumption application processor with integrated ARM Cortex-M4F and HiFi3 DSP, and designed for smart home and IoT applications.

1.2 Features

The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

1.2.1 Microprocessor

- ARM Cortex-M4F processor
- Integrated 16KB instruction cache, 16KB data cache
- Nested Vectored Interrupt Controller closely integrated with processor core to achieve low latency interrupt processing, support 64 external interrupts
- Include Floating Point Unit (FPU)

1.2.2 DSP

- HiFi3 with 4 24-bit MAC or dual 32-bit MAC architecture
- 3 VLIW slots, 2-Way SIMD Vector FPU
- Voice noise reduction optimization
- Integrated 64KB/512KB I/D TCM
- Integrated 16KB/16KB I/D Cache

1.2.3 Memory Organization

- Internal on-chip memory
  - BootRom
  - Share Memory

- External off-chip memory
  - FSPI NorFlash
  - FSPI pSRAM

1.2.4 System SRAM

- Internal BootRom
  - Support system boot from the following device:
    - FSPI NorFlash interface
  - Support system code download by the following interface:
    - USB2 interface (Device mode)

- Share Memory
  - Size: 1MB

1.2.5 External Storage device

- FSPI Serial flash interface
  - Support transfer data from/to serial flash device
  - Support x1,x2,x4 data bits mode
  - Support 1 chip select

- FSPI pSRAM interface
  - Support transfer data from/to pSRAM
  - Support x1,x2,x4 data bits mode
  - Support 1 chip select

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1.2.6 System Component

- CRU (clock & reset unit)
  - Support 2 PLLs to generate all clocks
  - Support 1 32KPLL to generate 26MHz clock from 32.768KHz input
  - One oscillator with 24MHz clock input
  - Support clock gating control for individual components
  - Support global soft-reset control for whole chip, also individual soft-reset for each component

- PMU(power management unit)
  - Support 4 separate power domains, which can be power up/down by software based on different application scenes
  - Multiple configurable work modes to save power by different frequency or automatic clock gating control or power domain on/off control
  - Support DSP auto power down mode

- Timer
  - Support 6 64bits timers with interrupt-based operation
  - Support two operation modes: free-running and user-defined count
  - Support timer work state checkable

- PWM
  - Support 4 on-chip PWMs(PWM0~PWM3) with interrupt-based operation
  - Programmable pre-scaled operation to bus clock and then further scaled
  - Embedded 32-bit timer/counter facility
  - Support capture mode
  - Support continuous mode or one-shot mode
  - Provides reference mode and output various duty-cycle waveform
  - Optimized for IR application for PWM3

- Watchdog
  - 32-bit watchdog counter
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - Generate a system reset
    - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
  - One Watchdog for CM4, the other for DSP

- Interrupt Controller
  - Support 2 interrupt controllers for DSP and AP
  - Support 50 SPI interrupt sources input from different components inside RK2108
  - Input interrupt level is fixed, only high-level sensitive
  - Support different interrupt priority for each interrupt source, and they are always software-programmable

- DMAC
  - Micro-code programming based DMA
  - The specific instruction set provides flexibility for programming DMA transfers
  - Linked list DMA function is supported to complete scatter-gather transfer
  - Support internal instruction cache
  - Support data transfer types including memory-to-memory, memory-to-peripherals, peripherals-to-memory
  - DMAC features:
    - Support 8 channels

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- 17 hardware request from peripherals
- 2 interrupt output

1.2.7 Video input interface

- VIP
  - Support BT601 YCbCr 422 8-bit input
  - Support BT656 YCbCr 422 8-bit input
  - Support UYVY/VYUY/YUYV/YVYU configurable
  - Support RAW 8/10/12-bit input
  - Support window cropping
  - Support virtual stride when write to internal memory
  - Support different stored address for Y and UV

1.2.8 Display interface

- Display interface
  - Support RGB Parallel Display interface
  - Support MIPI DSI interface

- RGB Parallel Display interface
  - Up to serial 8-bit

- MIPI DSI interface
  - Compatible with MIPI Alliance Interface specification v1.0
  - Support 2 data lanes, 1.5Gbps maximum data rate per lane

1.2.9 Video Output Processor

- Display interface
  - MIPI interface
  - Parallel RGB LCD interface
  - Max input/output resolution
    - Max input size: 512KB
    - Max output: 2048x4096
- Display process
  - Background layer
    - programmable 24-bit color
  - Win0 layer and Win1 layer
    - Format :
      1BPP/2BPP/4BPP/8BPP
      RGB888, ARGB888, RGB565, RGB444
      YUV422, YUV420, YUV444 4-bit/8-bit
      YUYV422 4-bit/8-bit
    - Support virtual display
    - 256 level alpha blending (pre-multiplied alpha support)
    - Transparency color key
    - YCbCr2RGB(rec601-mpeg/ rec601-jpeg/rec709)
    - RGB2YCbCr(BT601/BT709)
  - Win2 layer
    - Format :
      RGB888, ARGB888, RGB565, RGB444
      YUV422, YUV420, YUV444 4-bit/8-bit
      YUYV422 4-bit/8-bit
    - Support virtual display
    - 256 level alpha blending (pre-multiplied alpha support)
    - Transparency color key
    - YCbCr2RGB(rec601-mpeg/ rec601-jpeg/rec709)
    - RGB2YCbCr(BT601/BT709)
- Overlay

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  - RGB/YUV overlay
  - Layer1/2/3 exchange
- POST process
  - BCSH
  - Y-gamma
  - Post scale up: 2/3/4
  - Color matrix
- Support some dsc1.1 encoding mechanisms
  - MMAP, BP, MPP predictions and ICH
  - Flatness detection and signaling
  - Standard 2:1 and 3:1 compression ratio for MIPI DSI standard
  - Support maximum 2kx4k image resolution
  - Support 1 or 2 slices per line
  - Support 8bits/component (24 bits/pixel)

1.2.10 Audio Interface

- I2S0
  - Up to 2 channels TX and 4 channels RX path
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal, left-justified, right-justified)

- I2S1
  - Up to 2 channels for TX and 6 channels RX path
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal, left-justified, right-justified)
  - Support 4 PCM formats (early, late1, late2, late3)
  - I2S and PCM cannot be used at the same time

- PDM
  - Up to 6 channels
  - Audio resolution from 16bits to 24bits
  - Sample rate up to 192KHz
  - Support PDM master receive mode

- Codec ADC
  - Up to 2 channels
  - Support I2S 2 channels or PDM 2 channels
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable

- Audio Bypass
  - Support I2SIN interface bypass to AP by I2SOUT interface
  - Support PDMIN interface bypass to AP by PDMOUT interface
  - Support I2S from Codec ADC bypass to AP by I2SOUT interface
  - Support PDM from Codec ADC bypass to AP by PDMOUT interface

- VAD(Voice Activity Detection)
  - Support read voice data from I2S/PDM
  - Support voice amplitude detection
  - Support Multi-Mic array data storing
  - Support a level combined interrupt

- Audio PWM

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- Support 2 channels audio PWM
- Audio data width from 16bits to 32bits
- Support up to 16 oversampling
- Support audio resolution 8/9/10/11bits
- Support linear interpolation by 2/4/6/8 oversampling

1.2.11 Connectivity

- SDIO interface
  - Compatible with SDIO3.0 protocol
  - 4-bit data bus widths

- USB 2.0 for Device
  - Compatible with USB 2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode

- SPI interface
  - Support 2 SPI Controllers, both support one chip-select output
  - Support serial-master and serial-slave mode, software-configurable

- SPI2APB interface
  - Support slave mode SPI protocol
  - Support serial-slave mode only
  - Embedded a APB master interface

- I2C Master controller
  - Support 3 I2C Master(I2C0-I2C2)
  - Support 7bits and 10bits address mode
  - Software programmable clock frequency
  - Data on the I2C-bus can be transferred at rates of up to 100k bits/s in the Standard-mode, up to 400k bits/s in the Fast-mode

- I2C Slave controller
  - One on-chip I2C slave controller
  - Software programmable clock frequency and transfer rate 400Kbit/s in the fast mode
  - Serial 8bits oriented and bidirectional data transfers can be made at 100Kbit/s in the standard mode

- UART interface
  - Support 3 UART interfaces(UART0-UART2)
  - Embedded two 64-byte FIFO for TX and RX operation respectively
  - Support 5bit, 6bit, 7bit, 8bit serial data transmit or receive
  - Standard asynchronous communication bits such as start, stop and parity
  - Support different input clock for UART operation to get up to 4Mbps baud rate
  - Support auto flow control mode for UART0/UART2

1.2.12 Others

- Multiple group of GPIO
  - All of GPIOs can be used to generate interrupt
  - Support level trigger and edge trigger interrupt
  - Support configurable polarity of level trigger interrupt
  - Support configurable rising edge, falling edge and both edge trigger interrupt
  - Support configurable pull direction(a weak pull-up and a weak pull-down)
  - Support configurable drive strength

- LDO
  - Support input 1.8V power supply

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- Output 3 power supply: digital 0.9V, analog 0.9V, codec 1.6V

- Package Type
  - FCCSP116L (body: 3.8mm x 4.5mm; ball size: 0.22mm; ball pitch: 0.35mm)

1.3 Block Diagram

The following diagram shows the basic block diagram.

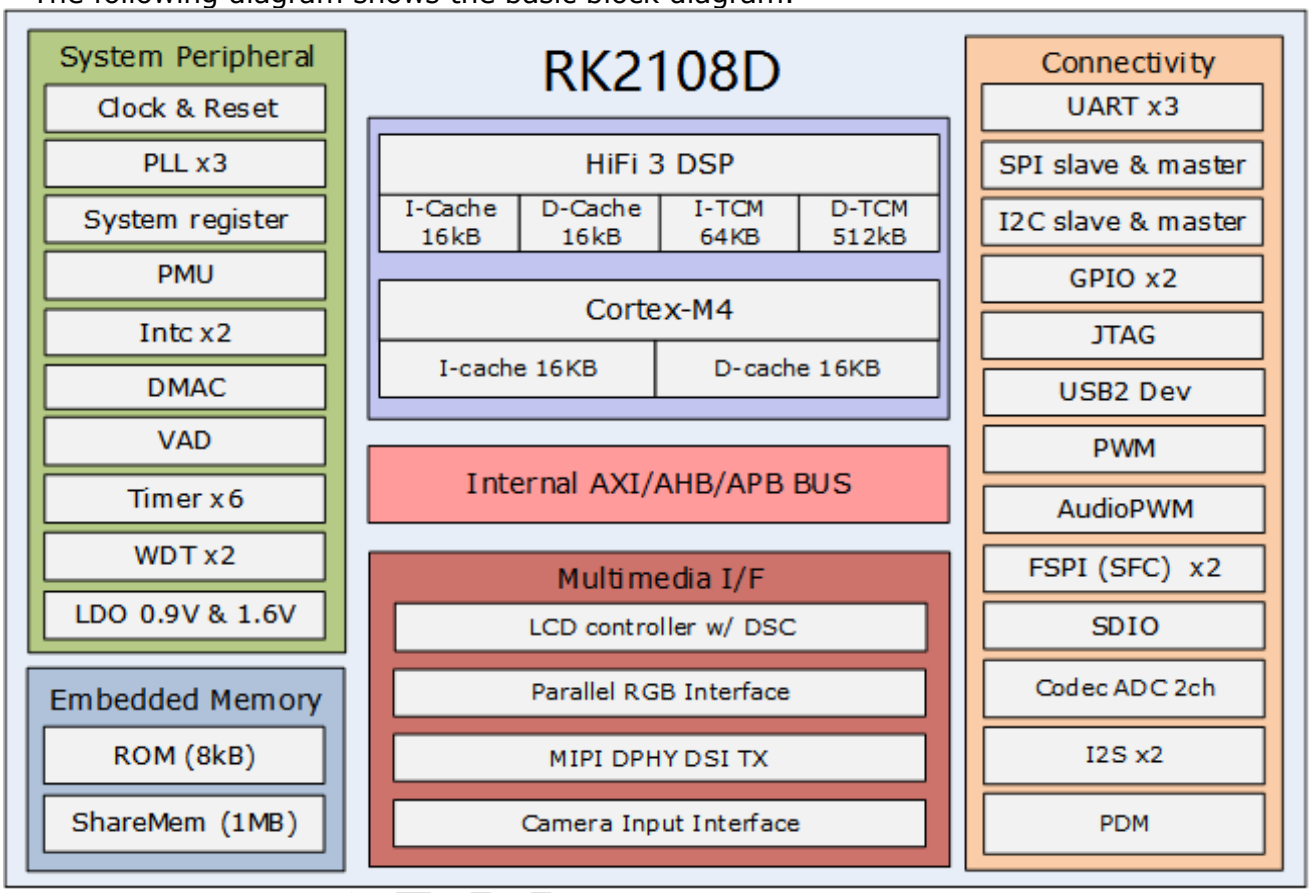

Fig.1-1 Block Diagram

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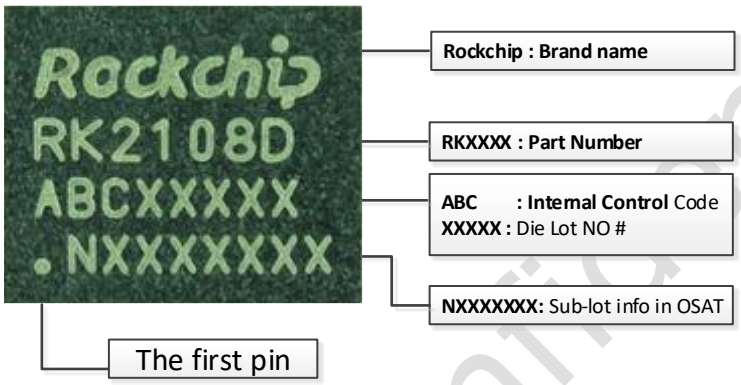
Chapter 2 Package Information

2.1 Order Information

Orderable Device	RoHS status	Package	Package Qty	Device Feature
RK2108D	RoHS	FCCSP116L	TBD	Audio application processor includes Cortex-M4F and HiFi3 DSP

2.2 Top Marking



2.3 FCCSP 116L Dimension

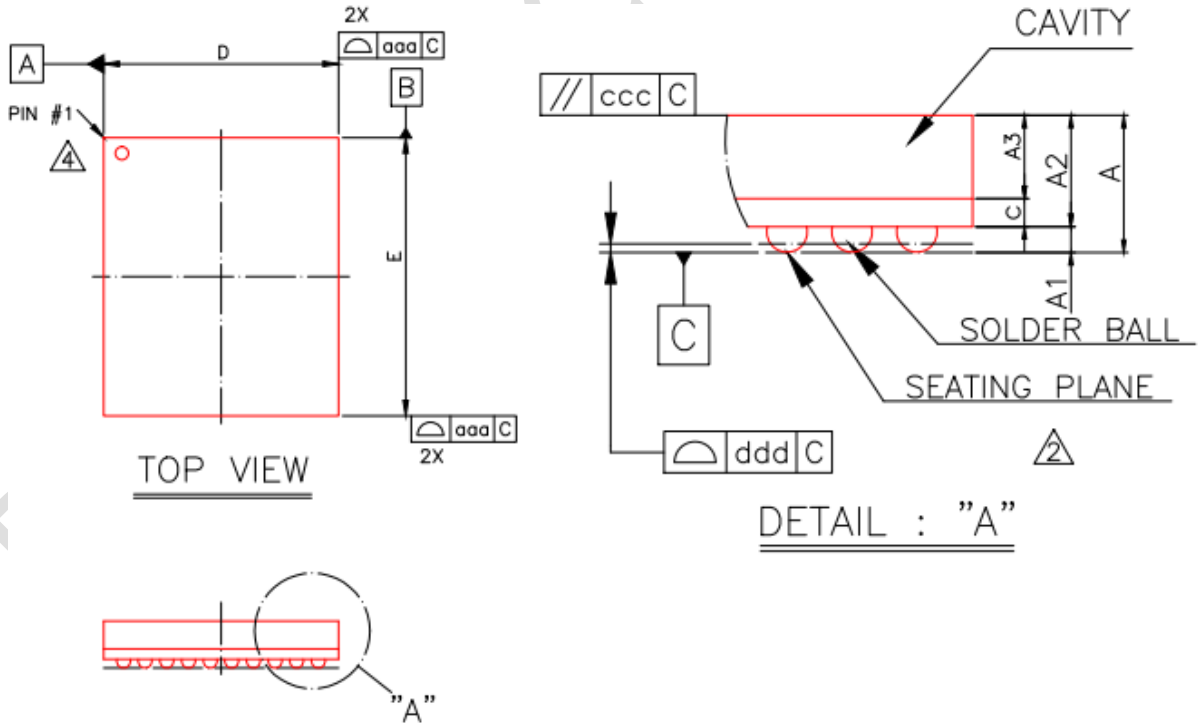


Fig.2-1 Package Top And Side View

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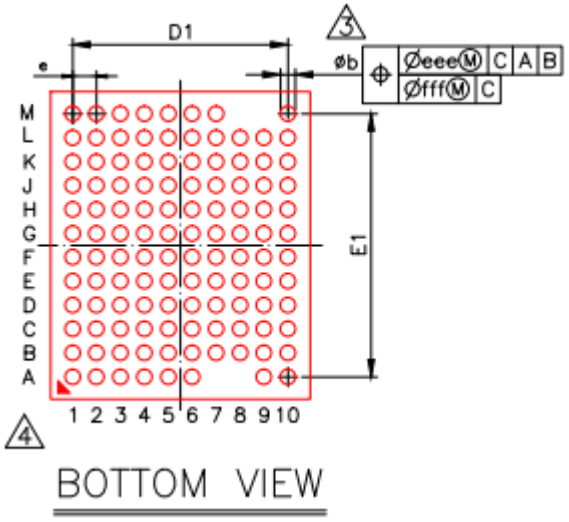

Fig.2-2 Package Bottom View

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.69	0.76	0.83	0.027	0.030	0.033
A1	0.09	0.14	0.19	0.004	0.006	0.007
A2	0.57	0.62	0.67	0.022	0.024	0.026
A3	0.42	0.45	0.48	0.017	0.018	0.019
c	0.14	0.17	0.20	0.006	0.007	0.008
D	3.70	3.80	3.90	0.146	0.150	0.154
E	4.40	4.50	4.60	0.173	0.177	0.181
D1	---	3.15	---	---	0.124	---
E1	---	3.85	---	---	0.152	---
e	---	0.35	---	---	0.014	---
b	0.17	0.22	0.27	0.007	0.009	0.011
aaa	0.10			0.004		
ccc	0.10			0.004		
ddd	0.08			0.003		
eee	0.15			0.006		
fff	0.05			0.002		
MD/ME	10/12					

Fig.2-3 Package Dimension

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2.4 Ball Map

116	1	2	3	4	5	6	7	8	9	10	
A	GPIO1_C2_u/SPIMST1_MOSI_M1/I2CMST2_SCL_M2/SFC1_SIO3	GPIO1_C5_d/SPIMST2_CLK_M1/SFC1_CLK	GPIO1_C4_u/SPIMST2_CS0_M1/SFC1_CS	GPIO1_C7_u/SPIMST2_MISO_M1/SFC1_SIO1	GPIO1_C3_u/SPIMST1_MISO_M1/I2CMST2_SDA_M2/SFC1_SIO2	GPIO1_C6_u/SPIMST2_MOSI_M1/SFC1_SIO0	NP	NP	GPIO1_C1_d/SPIMST1_CLK_M1/I2CMST1_SDA_M2	GPIO1_C0_u/SPIMST1_CS_M1/I2CMST1_SCL_M2	A
B	VSS_1	GPIO0_B6_u/I2CSLV_SCL/SFC_SIO0	GPIO0_B5_d/SPISLV0_MISO/I2CMST2_SDA_M1/SFC_CLK	GPIO0_C5_d/SPIMST1_MOSI_M0/I2CMST2_SCL_M0/SDIO_D3	GPIO0_B7_u/I2CSLV_SDA/SFC_SIO1	NC10	NC9	NC6	NC5	VSS_2	B
C	GPIO1_A6_d/M4_DSP_JTAG_SEL	GPIO0_D2_u/UART0_RTS/UART1_TX_M0/AUDIO_ROUT_M0/PWM2	GPIO1_A3_d/PMU_DEBUG3/SPIMST2_MOSI_M0/UART2_RTS/I2CMST0_SDA_M2	NPOR_u	GPIO0_B2_u/SPISLV0_CS/I2CMST1_SCL_M1/SFC_SIO3	GPIO0_C4_d/SPIMST1_MISO_M0/I2CMST2_SDA_M0/DSP_JTAG0_TDO/SDIO_D2	NC8	NC7	NC2	NC4	C
D	GPIO0_C7_u/UART0_RX/M4_JTAG1_TCK	GPIO1_A0_u/PMU_DEBUG0/SPIMST2_CS0_M0/UART2_RX	GPIO1_A2_d/LCD_OUT_RESET_N/PMU_DEBUG2/SPIMST2_MISO_M0/UART2_CTS/I2CMST0_SCL_M2	VCCIO1	GPIO0_B3_u/SPISLV0_CLK/I2CMST1_SDA_M1/SFC_SIO2	GPIO0_C6_u/I2CSLV_ADDR_SEL	VSS_5	AVSS_1	NC1	NC3	D
E	GPIO0_D0_u/UART0_TX/M4_JTAG1_TMS	GPIO0_D1_u/UART0_CTS/UART1_RX_M0/AUDIO_LOUT_M0/PWM1	GPIO1_A1_d/LCD_IN_TE/PMU_DEBUG1/SPIMST2_CLK_M0/UART2_TX	GPIO0_B4_u/SPISLV0_MOSI/I2CMST2_SCL_M1/SFC_CS	GPIO0_C3_d/SPIMST1_CLK_M0/I2CMST1_SCL_M0/DSP_JTAG0_TDI/SDIO_D1	GPIO0_C1_u/I2CMST0_SDA_M0/TEST_CLK_OUT3/DSP_JTAG0_TMS/SDIO_CMD	GPIO0_C0_u/I2CMST0_SCL_M0/TEST_CLK_OUT0/DSP_JTAG0_TCK/SDIO_CLK	GPIO0_C2_u/SPIMST1_CSN_M0/I2CMST1_SDA_M0/DSP_JTAG0_TRSTN/SDIO_D0	NC12	NC14	E
F	GPIO1_A5_d/BOOTDEV_SEL/LCD_CS/SPIMST2_CS1/PWM0/AUDIO_ROUT_M1	GPIO1_A7_d/CLK_OUT/PCM_CLK_M1/32K_CLK_OUT	TEST_d	CORE_VDD_1	CORE_VDD_2	VSS_7	DVDD_1V8_2	VSS_8	NC11	NC13	F
G	GPIO0_D4_u/TP_INTN/I2CMST0_SDA_M1/I2S1_SDIO_M1/PCM_SYNC_M0/CIF_D11	GPIO0_D7_d/OLPC_AP_INT/CIF_PCLK/I2S1_MCLK_M1	GPIO0_B1_d/PDM_OUT_SD01/I2S_OUT_SD01/LCD_RD/UART1_TX_M3/CIF_D9	VSS_9	CORE_VDD_OUT	VSS_10	DVDD_1V8_1	AVSS_2	MIPI_OUT_D1N	MIPI_OUT_CLKN	G
H	GPIO1_A4_d/LDO_OUT_PWR_EN/LCD_CMD/CIF_MCLK/PWM3/AUDIO_LOUT_M1	GPIO0_D3_u/TP_RESETN/I2CMST0_SCL_M1/I2S1_SDO0_M1/PCM_CLK_M0/CIF_D10	GPIO0_A5_d/I2S_OUT_MCLK/UART1_RX_M1_M3/TEST_CLK_OUT2/I2S1_IN_SDI2/CIF_D5/LCD_D5	VSS_11	VSS_12	VSS_13	AVDD_0V9_OUT	AVDD_1V8	MIPI_OUT_D1P	MIPI_OUT_CLKP	H
J	GPIO0_D6_d/AUD_BY_CTRL/CIF_VSYNC/I2S1_SCLK_M1/PCM_OUT_M0	GPIO0_D5_d/MIPISWITCH_CTRL/CIF_HREF/I2S1_LRCK_M1/PCM_IN_M0	VCCIO0	GPIO0_A3_d/PDM_IN_SDI1/I2S_IN_SDI1/LCD_D3/I2S1_IN_SDI1/CIF_D3	GPIO0_A1_d/PDM_IN_CLK1/I2S_IN_LRCK/LCD_D1/I2S1_IN_LRCK_M0/CIF_D1	VREF	AVDD_0V9	CODEC_1V6	AVSS_3	MIPI_OUT_D0N	J
K	GPIO1_B1_d/AP_WAKEUP_OLPC/PCM_IN_M1/UART1_RX_M2	GPIO1_B0_d/CLK_OUT_EN/PCM_SYNC_M1/UART1_TX_M2	GPIO0_B0_d/PDM_OUT_SD00/I2S_OUT_SD00/LCD_WR/I2S1_OUT_SD00_M0/CIF_D8	GPIO0_A4_d/I2S_IN_MCLK/UART1_TX_M1/TEST_CLK_OUT1/I2S1_MCLK_M0/CIF_D4/LCD_D4	GPIO0_A0_d/PDM_IN_CLK0/I2S_IN_SCLK/LCD_D0/I2S1_IN_SCLK_M0/CIF_D0	AVSS_4	MIC_IN2_N	MIC_IN2_P	AVSS_5	MIPI_OUT_D0P	K
L	VSS_3	GPIO1_B2_d/CLK_IN_SEL0/PCM_OUT_M1	GPIO0_A7_d/PDM_OUT_CLK1/I2S_OUT_LRCK/LCD_D7/I2S1_OUT_LRCK_M0/CIF_D7	GPIO0_A6_d/PDM_OUT_CLK0/I2S_OUT_SCLK/LCD_D6/I2S1_OUT_SCLK_M0/CIF_D6	GPIO0_A2_d/PDM_IN_SDIO/I2S_IN_SDIO/LCD_D2/I2S1_IN_SDIO_M0/CIF_D2	MAIN_CLK_IN	VSS_6	MIC_IN1_N	MIC_IN1_P	VSS_4	L
M	CLKSRC_SEL_u	GPIO1_B3_u/BOOT_SEL	USB_DM	USB_DP	USB_AVDD_3V3	XOUT_24M	XIN_24M	NP	NP	VSS_14	M
	1	2	3	4	5	6	7	8	9	10	
	FCCSP										

Fig.2-4 Ball Map

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2.5 Pin Number List

Table 2-1 Pin Number Order Information

Pin name	Pin#	Pin name	Pin#
SPIMST1_MOSI_M1/I2CMST2_SCL_M2/SFC1_SIO3/GPIO1_C2_u	A1	TP_INTN/I2CMST0_SDA_M1/I2S1_SDI0_M1/PCM_SYNC_M0/CIF_D11/GPIO0_D4_u	G1
SPIMST2_CLK_M1/SFC1_CLK/GPIO1_C5_d	A2	OLPC_AP_INT/CIF_PCLK/I2S1_MCLK_M1/GPIO0_D7_d	G2
SPIMST2_CS0_M1/SFC1_CS/GPIO1_C4_u	A3	PDM_OUT_SDO1/I2S_OUT_SDO1/LCD_RD/UART1_TX_M3/ CIF_D9/GPIO0_B1_d	G3
SPIMST2_MISO_M1/SFC1_SIO1/GPIO1_C7_u	A4	VSS_9	G4
SPIMST1_MISO_M1/I2CMST2_SDA_M2/SFC1_SIO2/GPIO1_C3_u	A5	CORE_VDD_OUT	G5
SPIMST2_MOSI_M1/SFC1_SIO0/GPIO1_C6_u	A6	VSS_10	G6
SPIMST1_CLK_M1/I2CMST1_SDA_M2/GPIO1_C1_d	A9	DVDD_1V8_1	G7
SPIMST1_CS_M1/I2CMST1_SCL_M2/GPIO1_C0_u	A10	AVSS_2	G8
VSS_1	B1	MIPI_OUT_D1N	G9
I2CSLV_SCL/SFC_SIO1/GPIO0_B6_u	B2	MIPI_OUT_CLKN	G10
SPISLV0_MISO/I2CMST2_SDA_M1/SFC_CLK/GPIO0_B5_d	B3	LDO_OUT_PWR_EN/LCD_CMD/CIF_MCLK/PWM3/AUDIO_LOUT_M1/GPIO1_A4_d	H1
SPIMST1_MOSI_M0/I2CMST2_SCL_M0/SDIO_D3/GPIO0_C5_d	B4	TP_RESETN/I2CMST0_SCL_M1/I2S1_SDO0_M1/PCM_CLK_M0/CIF_D10/GPIO0_D3_u	H2
I2CSLV_SDA/SFC_SIO1/GPIO0_B7_u	B5	I2S_OUT_MCLK/UART1_RX_M1_M3/TEST_CLK_OUT2/I2S1_IN_SDI2/CIF_D5/LCD_D5/GPIO0_A5_d	H3
NC	B6	VSS_11	H4
NC	B7	VSS_12	H5
NC	B8	VSS_13	H6
NC	B9	AVDD_0V9_OUT	H7
VSS_2	B10	AVDD_1V8	H8
M4_DSP_JTAG_SEL/GPIO1_A6_d	C1	MIPI_OUT_D1P	H9
UART0_RTS/UART1_TX_M0/AUDIO_ROUT_M0/PWM2/GPIO0_D2_u	C2	MIPI_OUT_CLKP	H10
PMU_DEBUG3/SPIMST2_M0SI_M0/UART2_RTS/I2CMST0_SDA_M2/GPIO1_A3_d	C3	AUD_BY_CTRL/CIF_VSYNC/I2S1_SCLK_TX_RX_M1/PCM_OUT_M0/GPIO0_D6_d	J1
NPOR_u	C4	CIF_HREF/I2S1_LRCK_M1/PCM_IN_M0/GPIO0_D5_d	J2
SPISLV0_CS/I2CMST1_SCL_M1/SFC_SIO3/GPIO0_B2_u	C5	VCCIO0	J3
SPIMST1_MISO_M0/I2CMST2_SDA_M0/DSP_JTAG0_TDO/ SDIO_D2/GPIO0_C4_d	C6	PDM_IN_SDI1/I2S_IN_SDI1/LCD_D3/I2S1_IN_SDI1/CIF_D3/GPIO0_A3_d	J4
NC	C7	PDM_IN_CLK1/I2S_IN_LRCK/LCD_D1/I2S1_IN_LRCK_M0/CIF_D1/GPIO0_A1_d	J5
NC	C8	VREF	J6
NC	C9	AVDD_0V9	J7
NC	C10	CODEC_1V6	J8
UART0_RX/M4_JTAG1_TCK/GPIO0_C7_u	D1	AVSS_3	J9
PMU_DEBUG0/SPIMST2_CS0_M0/UART2_RX/GPIO1_A0_u	D2	MIPI_OUT_D0N	J10
LCD_OUT_RESET_N/PMU_DEBUG2/SPIMST2_MISO_M0/UART2_CTS/I2CMST0_SCL_M2/ GPIO1_A2_d	D3	AP_WAKEUP_OLPC/PCM_IN_M1/UART1_RX_M2/GPIO1_B1_d	K1
VCCIO1	D4	CLK_OUT_EN/PCM_SYNC_M1/UART1_TX_M2/GPIO1_B0_d	K2
SPISLV0_CLK /I2CMST1_SDA_M1/SFC_SIO2/GPIO0_B3_u	D5	PDM_OUT_SDO0/I2S_OUT_SDO0/LCD_WR/I2S1_OUT_SDO0_M0/CIF_D8/GPIO0_B0_d	K3
I2CSLV_ADDR_SEL/GPIO0_C6_u	D6	I2S_IN_MCLK/UART1_TX_M1/TEST_CLK_OUT1/I2S1_MCLK_M0/CIF_D4/LCD_D4/GPIO0_A4_d	K4

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Pin name	Pin#	Pin name	Pin#
VSS_5	D7	PDM_IN_CLK0/I2S_IN_SCLK/LCD_D0/I2S1_IN_SCLK_M0/CIF_D0/GPIO0_A0_d	K5
AVSS_1	D8	AVSS_4	K6
NC	D9	MIC_IN2_N	K7
NC	D10	MIC_IN2_P	K8
UART0_TX/M4_JTAG1_TMS/GPIO0_D0_u	E1	AVSS_5	K9
UART0_CTS/UART1_RX_M0/AUDIO_LOUT_M0/PWM1/GPIO0_D1_u	E2	MIPI_OUT_D0P	K10
LCD_IN_TE/PMU_DEBUG1/SPIMST2_CLK_M0/UART2_TX/GPIO1_A1_d	E3	VSS_3	L1
SPISLV0_MOSI/I2CMST2_SCL_M1/SFC_CS/GPIO0_B4_u	E4	CLK_IN_SEL0/PCM_OUT_M1/GPIO1_B2_d	L2
SPIMST1_CLK_M0/I2CMST1_SCL_M0/DSP_JTAG0_TDI / SDIO_D1/GPIO0_C3_d	E5	PDM_OUT_CLK1/I2S_OUT_LRCK/LCD_D7/I2S1_OUT_LRCK_M0/CIF_D7/GPIO0_A7_d	L3
I2CMST0_SDA_M0/TES_CLK_OUT3/DSP_JTAG0_TMS/SDIO_CMD/GPIO0_C1_u	E6	PDM_OUT_CLK0/I2S_OUT_SCLK/LCD_D6/I2S1_OUT_SCLK_M0/CIF_D6/GPIO0_A6_d	L4
I2CMST0_SCL_M0/TEST_CLK_OUT0/DSP_JTAG0_TCK/SDIO_CLK/GPIO0_C0_u	E7	PDM_IN_SDI0/I2S_IN_SDI0/LCD_D2/I2S1_IN_SDI0_M0/CIF_D2/GPIO0_A2_d	L5
SPIMST1_CSN_M0/I2CMST1_SDA_M0/DSP_JTAG0_TRSTN/SDIO_D0/GPIO0_C2_u	E8	MAIN_CLK_IN	L6
NC	E9	VSS_6	L7
NC	E10	MIC_IN1_N	L8
BOOT_DEV_SEL/LCD_CS/SPIMST2_CS1/PWM0/AUDIO_ROUT_M1/GPIO1_A5_d	F1	MIC_IN1_P	L9
CLK_OUT/PCM_CLK_M1/32K_CLK_OUT/GPIO1_A7_d	F2	VSS_4	L10
TEST_d	F3	CLKSRC_SEL	M1
CORE_VDD_1	F4	BOOT_SEL/GPIO1_B3	M2
CORE_VDD_2	F5	USB_DM	M3
VSS_7	F6	USB_DP	M4
DVDD_1V8_2	F7	USB_AVDD_3V3	M5
VSS_8	F8	XOUT_24M	M6
NC	F9	XIN_24M	M7
NC	F10	VSS_14	M10

2.6 Power/Ground IO Description

Table 2-2 Power/Ground IO information

Group	Ball#	Descriptions
VSS	B1 B10 D7 L7 F6 F8 G4 G6 H4 H5 H6 L1 L10 M10	Internal Core Ground Digital IO Ground
AVSS	D8 G8 J9 K6 K9	Analog Ground
CORE_VDD	F4 F5	Digital Logic Power
CORE_VDD_OUT	G5	CORE LDO output power
DVDD_1V8	F7 G7	CORE LDO input power
AVDD_1V8	H8	MIPI LDO input power AUDIO LDO input power MIPI TX Analog Power OSC IO Analog Power FRAC PLL Analog Power
AVDD_0V9	J7	MIPI TX Analog Power FRAC PLL Analog Power INT PLL Analog Power 32K PLL Analog Power
AVDD_0V9_OUT	H7	MIPI LDO output power

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Group	Ball#	Descriptions
CODEC_1V6	J8	Codec ADC Analog Power
VCCIO	D4 J3	1.8V IO Power
USB_AVDD_3V3	M5	USB2 3.3V Analog Power
VREF	J6	Codec ADC VREF

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2.7 Function IO Description

Table 2-3 Function IO description

Pin#	Pin Name	Func1	Func2	Func3	Func4	Func5	Func6	Func7	PAD Type	Def	Driver Strength	Pull up /Pull down	IO Domain
K5	PDM_IN_CLK0/I2S_IN_SCLK/LCD_D0/I2S1_IN_SCLK_M0/CIF_D0/GPIO0_A0_d	GPIO0_A0_d	PDM_IN_CLK0	I2S_IN_SCLK	LCD_D0	I2S1_IN_SCLK_M0	CIF_D0		I/O	O	4	down	VCCIO
J5	PDM_IN_CLK1/I2S_IN_LRCK/LCD_D1/I2S1_IN_LRCK_M0/CIF_D1/GPIO0_A1_d	GPIO0_A1_d	PDM_IN_CLK1	I2S_IN_LRCK	LCD_D1	I2S1_IN_LRCK_M0	CIF_D1		I/O	O	4	down	
L5	PDM_IN_SDI0/I2S_IN_SDI0/LCD_D2/I2S1_IN_SDI0_M0/CIF_D2/GPIO0_A2_d	GPIO0_A2_d	PDM_IN_SDI0	I2S_IN_SDI0	LCD_D2	I2S1_IN_SDI0_M0	CIF_D2		I/O	I	4	down	
J4	PDM_IN_SDI1/I2S_IN_SDI1/LCD_D3/I2S1_IN_SDI1/CIF_D3/GPIO0_A3_d	GPIO0_A3_d	PDM_IN_SDI1	I2S_IN_SDI1	LCD_D3	I2S1_IN_SDI1	CIF_D3		I/O	I	4	down	
K4	I2S_IN_MCLK/UART1_TX_M1/TEST_CLK_OUT1/I2S1_MCLK_M0/CIF_D4/LCD_D4/GPIO0_A4_d	GPIO0_A4_d	I2S_IN_MCLK	UART1_TX_M1	TEST_CLK_OUT1	I2S1_MCLK_M0	CIF_D4	LCD_D4	I/O	I	4	down	
H3	I2S_OUT_MCLK/UART1_RX_M1_M3/TEST_CLK_OUT2/I2S1_IN_SDI2/CIF_D5/LCD_D5/GPIO0_A5_d	GPIO0_A5_d	I2S_OUT_MCLK	UART1_RX_M1_M3	TEST_CLK_OUT2	I2S1_IN_SDI2	CIF_D5	LCD_D5	I/O	I	4	down	
L4	PDM_OUT_CLK0/I2S_OUT_SCLK/LCD_D6/I2S1_OUT_SCLK_M0/CIF_D6/GPIO0_A6_d	GPIO0_A6_d	PDM_OUT_CLK0	I2S_OUT_SCLK	LCD_D6	I2S1_OUT_SCLK_M0	CIF_D6		I/O	I	4	down	
L3	PDM_OUT_CLK1/I2S_OUT_LRCK/LCD_D7/I2S1_OUT_LRCK_M0/CIF_D7/GPIO0_A7_d	GPIO0_A7_d	PDM_OUT_CLK1	I2S_OUT_LRCK	LCD_D7	I2S1_OUT_LRCK_M0	CIF_D7		I/O	I	4	down	
K3	PDM_OUT_SDO0/I2S_OUT_SDO0/LCD_WR/I2S1_OUT_SDO0_M0/CIF_D8/GPIO0_B0_d	GPIO0_B0_d	PDM_OUT_SDO0	I2S_OUT_SDO0	LCD_WR	I2S1_OUT_SDO0_M0	CIF_D8		I/O	O	4	down	
G3	PDM_OUT_SDO1/I2S_OUT_SDO1/LCD_RD/UART1_TX_M3/CIF_D9/GPIO0_B1_d	GPIO0_B1_d	PDM_OUT_SDO1	I2S_OUT_SDO1	LCD_RD	UART1_TX_M3	CIF_D9		I/O	O	4	down	
C5	SPISLV0_CS/I2CMST1_SCL_M1/SFC_SIO3/GPIO0_B2_u	GPIO0_B2_u	SPISLV0_CS	I2CMST1_SCL_M1	SFC_SIO3				I/O	I	4	up	
D5	SPISLV0_CLK /I2CMST1_SDA_M1/SFC_SIO2/GPIO0_B3_u	GPIO0_B3_u	SPISLV0_CLK	I2CMST1_SDA_M1	SFC_SIO2				I/O	I	4	up	
E4	SPISLV0_MOSI/I2CMST2_SCL_M1/SFC_CS/GPIO0_B4_u	GPIO0_B4_u	SPISLV0_MOSI	I2CMST2_SCL_M1	SFC_CS				I/O	I	4	up	
B3	SPISLV0_MISO/I2CMST2_SDA_M1/SFC_CLK/GPIO0_B5_d	GPIO0_B5_d	SPISLV0_MISO	I2CMST2_SDA_M1	SFC_CLK				I/O	I	4	down	
B2	I2CSLV_SCL/SFC_SIO1/GPIO0_B6_u	GPIO0_B6_u	I2CSLV_SCL	SFC_SIO0					I/O	I	4	up	
B5	I2CSLV_SDA/SFC_SIO1/GPIO0_B7_u	GPIO0_B7_u	I2CSLV_SDA	SFC_SIO1					I/O	I	4	up	
E7	I2CMST0_SCL_M0/TEST_CLK_OUT0/DSP_JTAG0_TCK/SDIO_CLK/GPIO0_C0_u	GPIO0_C0_u	I2CMST0_SCL_M0	TEST_CLK_OUT0	DSP_JTAG0_TCK	SDIO_CLK			I/O	I	4	up	
E6	I2CMST0_SDA_M0/TES_CLK_OUT3/DSP_JTAG0_TMS/SDIO_CMD/GPIO0_C1_u	GPIO0_C1_u	I2CMST0_SDA_M0	TEST_CLK_OUT3	DSP_JTAG0_TMS	SDIO_CMD			I/O	I	4	up	
E8	SPIMST1_CSN_M0/I2CMST1_SDA_M0/DSP_JTAG0_TRSTN/SDIO_D0/GPIO0_C2_u	GPIO0_C2_u	SPIMST1_CSN_M0	I2CMST1_SDA_M0	DSP_JTAG0_TRSTN	SDIO_D0			I/O	O	4	up	
E5	SPIMST1_CLK_M0/I2CMST1_SCL_M0/DSP_JTAG0_TDI/SDIO_D1/GPIO0_C3_d	GPIO0_C3_d	SPIMST1_CLK_M0	I2CMST1_SCL_M0	DSP_JTAG0_TDI	SDIO_D1			I/O	O	4	down	
C6	SPIMST1_MISO_M0/I2CMST2_SDA_M0/DSP_JTAG0_TDO/SDIO_D2/GPIO0_C4_d	GPIO0_C4_d	SPIMST1_MISO_M0	I2CMST2_SDA_M0	DSP_JTAG0_TDO	SDIO_D2			I/O	I	4	down	
B4	SPIMST1_MOSI_M0/I2CMST2_SCL_M0/SDIO_D3/GPIO0_C5_d	GPIO0_C5_d	SPIMST1_MOSI_M0	I2CMST2_SCL_M0	SDIO_D3				I/O	I	4	down	
D6	I2CSLV_ADDR_SEL/GPIO0_C6_u	GPIO0_C6_u	I2CSLV_ADDR_SEL						I/O	I	4	up	
D1	UART0_RX/M4_JTAG1_TCK/GPIO0_C7_u	GPIO0_C7_u	UART0_RX	M4_JTAG1_TCK					I/O	I	4	up	
E1	UART0_TX/M4_JTAG1_TMS/GPIO0_D0_u	GPIO0_D0_u	UART0_TX	M4_JTAG1_TMS					I/O	O	4	up	
E2	UART0_CTS/UART1_RX_M0/AUDIO_LOUT_M0/PWM1/GPIO0_D1_u	GPIO0_D1_u	UART0_CTS	UART1_RX_M0	AUDIO_LOUT_M0	PWM1			I/O	I	4	up	
C2	UART0_RTS/UART1_TX_M0/AUDIO_ROUT_M0/PWM2/GPIO0_D2_u	GPIO0_D2_u	UART0_RTS	UART1_TX_M0	AUDIO_ROUT_M0	PWM2			I/O	O	4	up	
H2	TP_RESETN/I2CMST0_SCL_M1/I2S1_SDO0_M1/PCM_CLK_M0/CIF_D10/GPIO0_D3_u	GPIO0_D3_u	TP_RESETN	I2CMST0_SCL_M1	I2S1_SDO0_M1	PCM_CLK_M0	CIF_D10		I/O	O	4	up	

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Pin#	Pin Name	Func1	Func2	Func3	Func4	Func5	Func6	Func7	PAD Type	Def	Driver Strength	Pull up /Pull down	IO Domain
G1	TP_INTN/I2CMST0_SDA_M1/I2S1_SDI0_M1/PCM_SYNC_M0/CIF_D11/GPIO0_D4_u	GPIO0_D4_u	TP_INTN	I2CMST0_SDA_M1	I2S1_SDI0_M1	PCM_SYNC_M0	CIF_D11		I/O	I	4	up	
J2	CIF_HREF/I2S1_LRCK_M1/PCM_IN_M0/GPIO0_D5_d	GPIO0_D5_d		CIF_HREF	I2S1_LRCK_M1	PCM_IN_M0			I/O	I	4	down	
J1	AUD_BY_CTRL/CIF_VSYNC/I2S1_SCLK_TX_RX_M1/PCM_OUT_M0/GPIO0_D6_d	GPIO0_D6_d	AUD_BY_CTRL	CIF_VSYNC	I2S1_SCLK_M1	PCM_OUT_M0			I/O	I	4	down	
G2	OLPC_AP_INT/CIF_PCLK/I2S1_MCLK_M1 /GPIO0_D7_d	GPIO0_D7_d	OLPC_AP_INT	CIF_PCLK	I2S1_MCLK_M1				I/O	O	4	down	
D2	PMU_DEBUG0/SPIMST2_CS0_M0/UART2_RX/GPIO1_A0_u	GPIO1_A0_u		PMU_DEBUG0	SPIMST2_CS0_M0	UART2_RX			I/O	I	4	up	
E3	LCD_IN_TE/PMU_DEBUG1/SPIMST2_CLK_M0/UART2_TX/GPIO1_A1_d	GPIO1_A1_d	LCD_IN_TE	PMU_DEBUG1	SPIMST2_CLK_M0	UART2_TX			I/O	I	4	down	
D3	LCD_OUT_RESET_N/PMU_DEBUG2/SPIMST2_MISO_M0/UART2_CTS/I2CMST0_SCL_M2/ GPIO1_A2_d	GPIO1_A2_d	LCD_OUT_RESET_N	PMU_DEBUG2	SPIMST2_MISO_M0	UART2_CTS	I2CMST0_SCL_M2		I/O	O	4	down	
C3	PMU_DEBUG3/SPIMST2_M0SI_M0/UART2_RTS/I2CMST0_SDA_M2/GPIO1_A3_d	GPIO1_A3_d		PMU_DEBUG3	SPIMST2_MOSI_M0	UART2_RTS	I2CMST0_SDA_M2		I/O	O	4	down	
H1	LDO_OUT_PWR_EN/LCD_CMD/CIF_MCLK/PWM3/AUDIO_LOUT_M1/GPIO1_A4_d	GPIO1_A4_d	LDO_OUT_PWR_EN	LCD_CMD	CIF_MCLK	PWM3	AUDIO_LOUT_M1		I/O	O	4	down	
F1	BOOT_DEV_SEL/LCD_CS/SPIMST2_CS1/PWM0/AUDIO_ROUT_M1/GPIO1_A5_d	GPIO1_A5_d	BOOTDEV_SEL	LCD_CS	SPIMST2_CS1	PWM0	AUDIO_ROUT_M1		I/O	I	4	down	
C1	M4_DSP_JTAG_SEL/GPIO1_A6_d	GPIO1_A6_d	M4_DSP_JTAG_SEL						I/O	I	4	down	
F2	CLK_OUT/PCM_CLK_M1/32K_CLK_OUT/GPIO1_A7_d	GPIO1_A7_d	CLK_OUT	PCM_CLK_M1	32K_CLK_OUT				I/O	O	4	down	
K2	CLK_OUT_EN/PCM_SYNC_M1/UART1_TX_M2/GPIO1_B0_d	GPIO1_B0_d	CLK_OUT_EN	PCM_SYNC_M1	UART1_TX_M2				I/O	I	4	down	
K1	AP_WAKEUP_OLPC/PCM_IN_M1/UART1_RX_M2/GPIO1_B1_d	GPIO1_B1_d	AP_WAKEUP_OLPC	PCM_IN_M1	UART1_RX_M2				I/O	I	4	down	
L2	CLK_IN_SEL0/PCM_OUT_M1/GPIO1_B2_d	GPIO1_B2_d	CLK_IN_SEL0	PCM_OUT_M1					I/O	I	4	down	
A10	SPIMST1_CS_M1/I2CMST1_SCL_M2/GPIO1_C0_u	GPIO1_C0_u	SPIMST1_CS_M1	I2CMST1_SCL_M2					I/O	I	4	up	
A9	SPIMST1_CLK_M1/I2CMST1_SDA_M2/GPIO1_C1_d	GPIO1_C1_d	SPIMST1_CLK_M1	I2CMST1_SDA_M2					I/O	I	4	down	
A1	SPIMST1_MOSI_M1/I2CMST2_SCL_M2/SFC1_SIO3/GPIO1_C2_u	GPIO1_C2_u	SPIMST1_MOSI_M1	I2CMST2_SCL_M2	SFC1_SIO3				I/O	I	4	up	
A5	SPIMST1_MISO_M1/I2CMST2_SDA_M2/SFC1_SIO2/GPIO1_C3_u	GPIO1_C3_u	SPIMST1_MISO_M1	I2CMST2_SDA_M2	SFC1_SIO2				I/O	I	4	up	
A3	SPIMST2_CS0_M1/SFC1_CS/GPIO1_C4_u	GPIO1_C4_u	SPIMST2_CS0_M1	SFC1_CS					I/O	I	4	up	
A2	SPIMST2_CLK_M1/SFC1_CLK/GPIO1_C5_d	GPIO1_C5_d	SPIMST2_CLK_M1	SFC1_CLK					I/O	I	4	down	
A6	SPIMST2_MOSI_M1/SFC1_SIO0/GPIO1_C6_u	GPIO1_C6_u	SPIMST2_MOSI_M1	SFC1_SIO0					I/O	I	4	up	
A4	SPIMST2_MISO_M1/SFC1_SIO1/GPIO1_C7_u	GPIO1_C7_u	SPIMST2_MISO_M1	SFC1_SIO1					I/O	I	4	up	
C4	NPOR_u	NPOR_u							I	I	4	up	
F3	TEST_d	TEST_d							I	I	4	down	
M1	CLKSRC_SEL_u	CLKSRC_SEL_u							I	I	4	up	
M2	BOOT_SEL/GPIO1_B3_u	GPIO1_B3_u	BOOT_SEL						I/O	I	2	up	VCCIO
L6	MAIN_CLK_IN	MAIN_CLK_IN							I	I		down	
M7	XIN24M	XIN24M							I	I		NA	OSC

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Pin#	Pin Name	Func1	Func2	Func3	Func4	Func5	Func6	Func7	PAD Type	Def	Driver Strength	Pull up /Pull down	IO Domain
M6	XOUT24M	XOUT24M							O	O		NA	
G9	MIPI_OUT_D1N	MIPI_OUT_D1N							A			NA	MIPI OUT
J10	MIPI_OUT_D0N	MIPI_OUT_D0N							A			NA	
G10	MIPI_OUT_CLKN	MIPI_OUT_CLKN							A			NA	
K10	MIPI_OUT_D0P	MIPI_OUT_D0P							A			NA	
H10	MIPI_OUT_CLKP	MIPI_OUT_CLKP							A			NA	
H9	MIPI_OUT_D1P	MIPI_OUT_D1P							A			NA	
L8	MIC_IN1_N	MIC_IN1_N							A			NA	
K8	MIC_IN2_P	MIC_IN2_P							A			NA	CODEC
K7	MIC_IN2_N	MIC_IN2_N							A			NA	
L9	MIC_IN1_P	MIC_IN1_P							A			NA	
M3	USB_DM	USB_DM							A			NA	USB
M4	USB_DP	USB_DP							A			NA	

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Notes:
①:Type: I = input, O = output, I/O = input/output (bidirectional), A = Analog
②:Output Drive Unit is mA, only Digital IO has driver strength value;
③:Def: I = input without any pull resistor, O = output without any pull resistor;

2.8 IO Pin Name Description

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 2-4 IO function description list

Interface	Pin Name	Direction	Description
Misc	XIN24M	I	Clock input of 24MHz crystal
	XOUT24M	O	Clock output of 24MHz crystal
	MAIN_CLK_IN	I	Main clock input
	NPOR_u	I	Chip hardware reset
	TEST_d	I	Test mode enable
	CLKSRC_SEL_u	I	Control to select OSC or Main clock Input Low Voltage: From 24MHz OSC Input High Voltage: From IO directly or from 32K PLL
	BOOT_SEL_u	I	Boot select Input Low Voltage: Boot from SFC0/USB Input High Voltage: Boot from SPISLV0/I2CSLV/SPIMST1
	BOOT_DEV_SEL_d	I	When BOOT_SEL_u input High Voltage Input Low Voltage: Boot from SPISLV0/I2CSLV Input High Voltage: Boot from SPIMST1
	CLK_IN_SEL0_d	I	Clock frequency select for MAIN_CLK_IN (When CLKSRC_SEL=1) Input Low Voltage：high frequency clock Input High Voltage：32.768KHz clock

Interface	Pin Name	Direction	Description
M4 SWJ-DP	M4_JTAG1_TCK	I	M4 JTAG interface clock input/SWD interface clock input
	M4_JTAG1_TMS	I/O	M4 JTAG interface TMS input/SWD interface data out

Interface	Pin Name	Direction	Description
DSP JTAG	DSP_JTAG0_TCK	I	DSP JTAG interface clock input
	DSP_JTAG0_TMS	I	DSP JTAG interface tms input
	DSP_JTAG0_TRSTN	I	DSP JTAG interface reset input
	DSP_JTAG0_TDI	I	DSP JTAG interface data in
	DSP_JTAG0_TDO	O	DSP JTAG interface data out

Interface	Pin Name	Direction	Description
SDIO Host Controller	SDIO_CLK	O	SDIO card clock
	SDIO_CMD	I/O	SDIO card command output and response input
	SDIO_D*i* (*i*=0~3)	I/O	SDIO card data input and output

Interface	Pin Name	Direction	Description
FSPI Controller	SFC(1)_CLK	I/O	SFC serial clock
	SFC(1)_CS	I/O	SFC chip select signal, low active
	SFC(1)_Di*(i=0~3)*	O	SFC serial data output

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Interface	Pin Name	Direction	Description
LCDC	LCDC_RS	O	LCDC RGB interface display clock out, MCU i80 interface RS signal
	LCDC_CS	O	LCDC RGB interface vertical sync pulse, MCU i80 interface CSN signal
	LDDC_WR	O	LCDC RGB interface horizontal sync pulse, MCU i80 interface WEN signal
	LCDC_RD	O	LCDC RGB interface data enable, MCU i80 interface REN signal
	LCDC_D*i* (*i*=0~7)	O	LCDC data output

Interface	Pin Name	Direction	Description
I2S0	I2S_IN_MCLK	I/O	I2SIN clock from or to external device
	I2S_IN_SCLK	I/O	I2SIN serial clock
	I2S_IN_LRCK	I/O	I2SIN left & right channel signal for receiving serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	I2S_IN_DAT*i* (*i*=0~1)	I	I2SIN input serial data
	I2S_OUT_MCLK	I/O	I2SOUt clock from or to external device
	I2S_OUT_SCLK	I/O	I2SOUT serial clock
	I2S_OUT_LRCK	I/O	I2SOUT left & right channel signal for receiving serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	I2S_OUT_DAT*i* (*i*=0~1)	O	I2SOUT output serial data

Interface	Pin Name	Direction	Description
I2S1	I2S1_MCLK	I/O	I2S1 clock from or to external device
	I2S1_SCLK_RX	I/O	I2S1 receiving serial clock
	I2S1_LRCK_RX	I/O	I2S1 left & right channel signal for receiving serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	I2S1_SDI*i* (*i*=0~2)	I	I2S1 receiving serial data
	I2S1_SCLK_TX	I/O	I2S1 transmitting serial clock
	I2S1_LRCK_TX	I/O	I2S1OUT left & right channel signal for transmitting serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	I2S1_SDO0	O	I2S1 transmitting serial data

Interface	Pin Name	Direction	Description
PDM	PDM_IN_CLK*i* (*i*=0~1)	O	PDMIN serial output clock
	PDM_IN_DAT*i* (*i*=0~1)	I	PDMIN serial input data
	PDM_OUT_CLK*i* (*i*=0~1)	I/O	PDMOUT serial input or output clock
	PDM_OUT_DAT*i* (*i*=0~1)	O	PDMOUT serial output data

Interface	Pin Name	Direction	Description
SPI	SPI_MST*i*_CLK(*i*=0,1,2)	I/O	SPI serial clock
	SPI_MST*i*_CS(*i*=0,1,2)	I/O	SPI chip select signal, low active

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Interface	Pin Name	Direction	Description
	SPI_MST*i*_MOSI(*i*=0,1,2)	I/O	SPI serial data output in master mode, and input in slave mode
	SPI_MST*i*_MISO(*i*=0,1,2)	I/O	SPI serial data input in master mode, and output in slave mode

Interface	Pin Name	Direction	Description
SPI2APB	SPI_SLV0_CLK	I	SPI2APB serial clock
	SPI_SLV0_CS	I	SPI2APB chip select signal, low active
	SPI_SLV0_MOSI	I	SPI2APB serial data input
	SPI_SLV0_MISO	O	SPI2APB serial data output

Interface	Pin Name	Direction	Description
I2C2APB	I2CSLV_SCL	I/O	I2C2APB clock
	I2CSLV_SDA	I/O	I2C2APB data

Interface	Pin Name	Direction	Description
PWM	PWM0	I/O	Pulse Width Modulation input or output
	PWM1	I/O	Pulse Width Modulation input or output
	PWM2	I/O	Pulse Width Modulation input or output
	PWM3	I/O	Pulse Width Modulation input or output, used for IR application recommended

Interface	Pin Name	Direction	Description
AUDIO PWM	AUDIO_LOUT	O	AUDIO PWM left channel output data
	AUDIO_ROUT	O	AUDIO PWM right channel output data

Interface	Pin Name	Direction	Description
I2C	I2C_MST*i*_SDA (*i*=0,1,2)	I/O	I2C data
	I2C_MST*i*_SCL (*i*=0,1,2)	I/O	I2C clock

Interface	Pin Name	Direction	Description
UART	UART*i*_RX (*i*=0,1,2)	I	UART serial data input
	UART*i*_TX (*i*=0,1,2)	O	UART serial data output
	UART*i*_CTS (*i*=0,2)	I	UART clear to send modem status input
	UART*i*_RTS (*i*=0,2)	O	UART modem control request to send output

Interface	Pin Name	Direction	Description
USB2	USB_DP	I/O	USB 2.0 Data signal DP
	USB_DM	I/O	USB 2.0 Data signal DM

Interface	Pin Name	Direction	Description
VIP (Camera IF)	CIF_D*i*(*i*=0~11)	I	Camera interface input pixel data
	CIF_VSYNC	I	Camera interface vertical sync signal
	CIF_PCLK	I	Camera interface input pixel clock
	CIF_HREF	I	Camera interface horizontial sync signal

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Interface	Pin Name	Direction	Description
MIPI_DSI	MIPI_OUT_D*i*N(*i*=0~1)	O	MIPI DSI negative differential data line transceiver output
	MIPI_OUT_D*i*P(*i*=0~1)	O	MIPI DSI positive differential data line transceiver output
	MIPI_OUT_CLKP	O	MIPI DSI positive differential clock line transceiver output
	MIPI_OUT_CLKN	O	MIPI DSI negative differential clock line transceiver output

Interface	Pin Name	Direction	Description
Codec ADC	MIC_IN1_P	I	Codec channel1 positive differential data
	MIC_IN1_N	I	Codec channel1 negative differential data
	MIC_IN2_P	I	Codec channel2 positive differential data
	MIC_IN2_N	I	Codec channel2 negative differential data

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Chapter 3 Electrical Specification

3.1 Absolute Ratings

The below table provides the absolute ratings.

Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

Table 3-1 Absolute ratings

Parameters	Related Power Group	Min	Max	Unit
Digital logic supply voltage	CORE_VDD	-0.3	1.26	V
Analog 0.9V supply voltage	AVDD_0V9	-0.3	1.26	V
1.8V supply voltage	DVDD_1V8 AVDD_1V8 VCCIO_1V8 VCCIO	-0.3	2.16	V
3.3V supply voltage	USB_AVDD_3V3	-0.3	3.96	V
Storage Temperature	Tstg	-40	125	℃
Max Conjunction Temperature	Tj	NA	125	℃

3.2 Recommended Operating Condition

Following table describes the recommended operating condition.

Table 3-2 Recommended operating condition

Parameters	Symbol	Min	Typ	Max	Unit
Max frequency of M4F			297	396	MHz
Max frequency of HiFi-3			396	594	MHz
CORE LDO power	DVDD_1V8	1.74	1.80	1.86	V
MIPI LOO and AUDIO LDO power	AVDD_1V8	1.74	1.80	1.86	V
Digital Logic power	CORE_VDD	0.81	0.90	0.99	V
Analog 0.9V power	AVDD_0V9	0.81	0.90	0.99	V
Digital GPIO Power (1.8V)	VCCIO_1V8	1.62	1.80	1.98	V
USB 2.0 Analog Power (3.3V)	USB_AVDD_3V3	3.0	3.30	3.60	V
OSC input clock frequency		NA	24	NA	MHz
Main clock input frequency		32.768	26000	38400	KHz
Ambient Operating Temperature	T_A	0	25	85	℃

Notes:① *Symbol name is same as the pin name in the io descriptions*

3.3 DC Characteristics

Table 3-3 DC Characteristics

Parameters		Symbol	Min	Typ	Max	Unit
Digital GPIO @1.8V	Input Low Voltage	Vil	NA	NA	0.3*VCC	V
	Input High Voltage	Vih	0.7*VCC	NA	NA	V
	Output Low Voltage	Vol	NA	NA	0.4	V
	Output High Voltage	Voh	0.75*VCC	NA	NA	V
	Pull-up Resistor	Rpu	10	22	55	KΩ
	Pull-down Resistor	Rpd	10	22	55	KΩ

Parameters		Symbol	Min	Typ	Max	Unit
MIPI DPHY	Input Low Voltage	Vil	NA	NA	0.2*VCC09D	V
	Input High Voltage	Vih	0.8*VCC09D	NA	NA	V
	Output Low Voltage	Vol	NA	NA	0.1*VCC09D	V
	Output High Voltage	Voh	0.9*VCC09D	NA	NA	V

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Parameters		Symbol	Min	Typ	Max	Unit
USB2	Input Low Voltage	Vil	NA	NA	0.8	V
	Input High Voltage	Vih	2.0	NA	NA	V
	Output Low Voltage	Vol	NA	NA	0.2	V
	Output High Voltage	Voh	VCC-0.2	NA	NA	V

3.4 Electrical Characteristics for General IO

Table 3-4 Electrical Characteristics for Digital General IO

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
Digital GPIO @1.8V	Input leakage current	Ii	Vin = 1.8V or 0V	NA	1.0	10	uA
	Tri-state output leakage current	Ioz	Vout = 1.8V or 0V	NA	1.0	10	uA
	High level input current	Iih	Vin = 1.8V, pull down disabled	NA	NA	NA	uA
			Vin = 1.8V, pull down enabled	NA	NA	NA	uA
	Low level input current	Iil	Vin = 0V, pull up disabled	NA	NA	NA	uA
			Vin = 0V, pull up enabled	NA	NA	NA	uA

3.5 Electrical Characteristics for PLL

Table 3-5 Electrical Characteristics for INT PLL

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
INT PLL(GPLL)	Reference frequency Range	Fref		5	NA	800	MHz
	VCO Frequency Range	Fvco		625	NA	2500	MHz
	PFD Frequency Range	Fpfd		5	NA	Fvco/16	MHz
	Output Frequency Range	Fout		12	NA	2500	MHz
	Lock time	Tlt	Input clock cycle is REFDIV/Fref. Example: Fref=25MHz REFDIV=1, Lock time is 40us	NA	1000	1500	Input clock cycles

Table 3-6 Electrical Characteristics for FRAC PLL

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
FRAC PLL(GPLL)	Reference frequency Range (Int)	Fref		1	NA	1200	MHz
	Reference frequency Range (Frac)	Fref		10	NA	1200	MHz
	VCO Frequency Range	Fvco		800	NA	3200	MHz
	PFD Frequency Range (Int)	Fpfd		1	NA	Fvco/16	MHz
	PFD Frequency Range (Frac)	Fpfd		10	NA	Fvco/16	MHz
	Output Frequency Range	Fout		16	NA	3200	MHz
	Lock time	Tlt	Input clock cycle is REFDIV/Fref. Example: Fref=25MHz REFDIV=1, Lock time is 10us	NA	250	500	Input clock cycles

Table 3-7 Electrical Characteristics for 32K PLL

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
32K PLL(SPLL)	Reference frequency Range	Fref		30	NA	900000	KHz
	VCO Frequency Range	Fvco		60	NA	900	MHz
	Output Frequency Range	Fout		3.75	NA	900	MHz

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Parameters		Symbol	Test condition	Min	Typ	Max	Unit
	Lock time	Tlt	Input clock cycle is REFDIV/Fref. Example: Fref=32.768KHz REFDIV=1, Lock time is 15.26ms	NA	500	NA	Input clock cycles

Notes:

① *REFDIV is the input divider value*

3.6 Electrical Characteristics for USB 2.0 Interface

Table 3-8 Electrical Characteristics for USB 2.0 Interface

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Data signaling common mode voltage range	Vhscm		-50	NA	500	mV
Squelch detection threshold	Vhssq	Squelch detected	NA	NA	100	mV
		No squelch detected	200	NA	NA	
Disconnect detection threshold	Vhsdsc		525	NA	625	mV
High-speed idle level output voltage	Vhsoi		-10	NA	10	mV
High-speed low level output voltage	Vhsol		-10	NA	10	mV
High-speed high level output voltage	Vhsoh		360	400	440	mV
Chirp-J output voltage(Differential)	Vchirpj		700	NA	1100	mV
Chirp-K output voltage(Differential)	Vchirpk		-900	NA	-500	mV
Slew rate of rising edge	Thsrlew		NA	NA	1600	V/usec
Slew rate of falling edge	Thsflew		NA	NA	1600	V/usec
Differential cable impedance	Zo		76.5	90	103.5	Ω
Common mode cable impedance	Zcm		21	30	39	Ω
Cable skew	Tskew		NA	NA	100	ps
Unmated contact capacitance	Cuc		NA	NA	2	ps
High input level	Vih		2.0	NA	NA	V
Low input level	Vil		NA	NA	0.8	V
High output level	Voh		VCC-0.2	NA	NA	V
Low output level	Vol		NA	NA	0.2	V

3.7 Electrical Characteristics for MIPI DPHY TX

Table 3-9 Electrical Characteristics for MIPI DPHY TX

Parameters	Symbol	Test condition	Min	Typ	Max	Units
HS TX static common-mode	Vcmtx		150	200	250	mV
Vcmtx mismatch when output is Differential-1 or Differential-0	ΔVcmtx(1,0)		NA	NA	5	mV
HS Transmit differential voltage	Vod		140	200	270	mV
Vod mismatch when output is Differential-1 or Differential-0	ΔVod		NA	NA	14	mV
HS output high voltage	Vohhs		NA	NA	360	mV
Single ended output impedance	Zos		40	50	60	Ω
Single ended output impedance mismacth	ΔZos		NA	NA	10	%
The venin output high level	Voh	To pass V1.1 LSTX Voh spec	1.1	NA	1.3	V
		To pass V1.2 LSTX Voh spec	0.95	NA	1.3	V
The venin output low level	Vol		-50	NA	50	mV
Output impedance of LP	Zolp		110	NA	NA	Ω
High-level output voltage	Voh		0.9*VCC09A	NA	NA	V
Low-level output voltage	Vol		NA	NA	0.1*VCC09A	V
Common-mode variations above 450 MHz	ΔVcmtx(HF)		NA	NA	15	mVrms

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Parameters	Symbol	Test condition	Min	Typ	Max	Units
Common-mode variations between 50MHz – 450MHz	ΔVcmtx(LF)		NA	NA	25	mVpeak
20%-80% rise time and fall time	Tr and Tf		NA	NA	0.3(<=1Gbps) 0.35(>1Gbps)	UI
			100	NA	NA	ps
15%-85% rise time and fall time	Trlp/Tflp		NA	NA	25	ns
30%-85% rise time and fall time	Treot		NA	NA	35	ns
Slew rate	SR		25	NA	150	mV/ns

3.8 Electrical Characteristics for Codec ADC

Table 3-10 Electrical Characteristics for Codec ADC

Parameters	Symbol	Test condition	Min	Typ	Max	Units
ADC Performance (16K Sample)						
Resolution				24		bit
Full Scale Input Range		0dB Gain in PGA stage		0.82		Vrms
Dynamic Range		A-Weight filter open, No boost in PGA stage, -60dBFs input, 20-8K Bandwidth		90		dB
THD+N		A-Weight filter open, No boost in PGA stage, -3dBFs input, 20-20K Bandwidth		-70		dB
ADC Digital Filter Pass Band			20		7.2K	Hz
ADC Digital Filter Pass Band Ripple				0.1		dB
Crosstalk		One channel drive 100mVrms signal		85		dB
Noise Floor		PGA 21db		-103		dB
ADC Performance (48K Sample)						
Resolution				24		bit
Full Scale Input Range		0dB Gain in PGA stage		0.82		Vrms
Dynamic Range		A-Weight filter open, No boost in PGA stage, -60dBFs input, 20-20K Bandwidth		88		dB
THD+N		A-Weight filter open, No boost in PGA stage, -3dBFs input, 20-20K Bandwidth		-70		dB
ADC Digital Filter Pass Band			20		20K	Hz
ADC Digital Filter Pass Band Ripple				0.1		dB
Crosstalk		One channel drive 100mVrms signal		85		dB
Noise Floor		PGA 21db		-99		dB

3.9 Electrical Characteristics for LDO

Table 3-11 Electrical Characteristics for LDO

Parameters	Symbol	Test condition	Min	Typ	Max	Units
LDO Input Voltage			1.74	1.8	1.86	V
AUDIO LDO						
V_{OUT} Output Voltage Adjustable Range (step=50mV)			1.5	NA	1.65	V
V_{OUT} Output Voltage Default value(Tj=25℃)	VOUT1		NA	1.6	NA	V
Power Supply Reject Ratio	PSRR		NA	70	NA	dB
Dropout voltage @ 20mA	V_{DROP}		NA	100	NA	mV
Operating Quiescent Current, No load	I_Q		NA	20	NA	uA
Rated output current	I_{MAX}		NA	10	NA	mA
Current Limit, VOUT1= V_{OUT1}x 0.95	I_{CLimit}		20	30	NA	mA
Soft-start Time	t_{SS}		NA	200	NA	us
V_{OUT} Discharge Switch ON Resistance	R_{DIS}		NA	400	NA	Ω
CORE LDO						

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Parameters	Symbol	Test condition	Min	Typ	Max	Units
V_{OUT} Output Voltage Adjustable range (step=50mV)			0.75	NA	1.05	V
V_{OUT} Output Voltage Default value(Tj=25℃)	VOUT2		0.877	0.9	0.923	V
V_{OUT} Load Regulation, I_{OUT} = 1mA to 200mA			NA	0.01	NA	%/mA
Power Supply Reject Ratio	PSRR		NA	50@1k	NA	dB
Dropout voltage @ 200mA	V_{DROP}		NA	500	NA	mV
Operating Quiescent Current, No load	I_Q		NA	40	NA	uA
Rated output current	I_{MAX}		NA	200	NA	mA
Current Limit, VOUT1= V_{OUT1}x 0.95	I_{CLimit}		250	300	NA	mA
Soft-start Time	t_{SS}		NA	200	NA	us
MIPI LDO						
V_{OUT} Output Voltage Adjustable range (step=50mV)			0.75	NA	1.05	V
V_{OUT} Output Voltage Default value(Tj=25℃)	VOUT3		0.877	0.9	0.923	V
V_{OUT} Load Regulation, I_{OUT} = 1mA to 100mA			NA	0.01	NA	%/mA
Power Supply Reject Ratio	PSRR		NA	50@1k	NA	dB
Dropout voltage @ 100mA	V_{DROP}		NA	500	NA	mV
Operating Quiescent Current, No load,	I_{Q1}		NA	40	NA	uA
Rated output current	I_{MAX}		NA	100	NA	mA
Current Limit, VOUT1= V_{OUT1}x 0.95	I_{CLimit}		150	200	NA	mA
Soft-start Time	t_{SS}		NA	200	NA	us
V_{OUT} Discharge Switch ON Resistance	R_{DIS}		NA	400	NA	Ω

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