Rockchip RK2116M2 Datasheet

Revision 1.6
Feb. 2026

Revision History

Date	Revision	Description
2026-02-10	1.6	Update package dimension in Fig 2.4 to compatible with different package venders. Update pin name in Table 2-1 according to the latest hardware schematic. Add MSL information and Lead Finish/Ball Material Information in Chapter 2 Change FSPI SCLK and data timing diagram in Fig. 4-1. Correct maximum FSPI clock frequency and minimum time of t_{rsu} in Table 4-1, and update related notes in Table 4-1. Update note(1) of thermal resistance characteristics in Table 5-1.
2026-01-13	1.5	Add timing parameters in Table 4-7 to Table 4-22 Modify SCLK frequency in Table 4-15 to Table 4-22
2025-12-12	1.4	Delete pSRAM interface in 1.2.5 and update block diagram accordingly Add Timing Chapter Delete TX description of PWM in 1.2.6
2025-11-21	1.3	Update description in 1.2.9 Connectivity Update conjunction temperature in Table 3-1 Update voltage data in Table 3-2 Update package thermal characteristics in Table 4-1
2025-10-18	1.2	Update block diagram Update package dimension in Fig.2 4 Update the description of NPOR in Table 2-9 Update voltage data in Table 3-1 and Table 3-2
2025-10-09	1.1	Update the description of CAN
2025-07-25	1.0	Initial release

Table of Content

Figure Index

Table Index

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Chapter 1 Introduction

1.1 Overview

RK2116M2 is a high-performance dual core HiFi4 DSP processor designed for intelligent voice interaction, audio input/output processing and other digital multimedia applications.

RK2116M2 integrates one N320 RISC-V processor to run operating system, UI rendering and application protocol stack and so on. Embedded 768KB system memory and eXecute In Place (XIP) Flash interface make RK2116M2 flexible for different application development.

RK2116M2 integrates rich peripheral interfaces, such as VOP, SAI, PDM, SPDIF, USB2 OTG, RMII, CAN, CEC and so on, can meet different application development, reduce hardware development complexity and development cost.

1.2 Features

1.2.1 Microprocessor

- One N320 RISC-V processor
- Support Zc*, Zicond and Bit-Manipulation Instruction Set Architecture Extension
- Support Private Timer Unit
- Support Enhanced Core Level Interrupt Controller
- Support one Multiplier, one Divider and one Floating Point Unit
- Support configurable Physical Memory Protection
- Support configurable Trust Execution Environment
- Support 16KB I-Cache and 16KB D-Cache
- Support standard 2-wire cJTAG debug interface

1.2.2 DSP

- Dual core HiFi4 DSP processor (DSP0, DSP1)
- Dual Load/Store, 4 VLIW Slots, 64-bit SIMD
- 4 MAC 32x32, 4 MAC 24x24, 8 MAC 32x16, 8 MAC 16x16 per cycle
- Two 2-Way SIMD VFPU
- 64KB ITCM, 256KB DTCM, 64KB I-Cache, 64KB D-Cache for DSP0
- 64KB ITCM, 128KB DTCM, 64KB I-Cache, 64KB D-Cache for DSP1
- One isolated voltage domain for DSP DVFS

1.2.3 Memory Organization

- Internal on-chip memory
  - BootROM
  - System SRAM
  - PMU SRAM
- External off-chip memory
  - SPI Nor/Nand Flash
  - SDMMC (eMMC/SD Card)

1.2.4 Internal Memory

- Internal BootRom
  - Support system boot from the following device:
    - SPI Flash interface
    - SDMMC(eMMC/SD Card) interface
  - Support system code download by the following interface:
    - USB OTG interface (Device mode)
    - SPI0 inteprface (Slave mode)
    - UART0 interface

- Internal SRAM
  - 768KB System SRAM
  - 16KB PMU SRAM

1.2.5 External Memory or Storage device

- Serial Flash Interface
  - Support transfer data from/to SPI flash device
  - Support x1, x2, x4 data bits mode
  - Support SDR mode
  - Support XIP (eXecute In Place)
  - Support up to 1 chip select

- SD/MMC Interface
  - Compatible with standard iNAND interface
  - Compatible with eMMC specification 4.51
  - Compatible with SD3.0, MMC ver4.51
  - Compatible with SDIO3.0 protocol
  - Data bus width is 4bits

1.2.6 System Component

- CRU (clock & reset unit)
  - One oscillator with external crystal input
  - One internal low frequency RC clock
  - One internal power on reset circuit
  - Support single-end 32.768KHz clock input/output from/to GPIO
  - Support PLL control and generate various clock frequency for chip
  - Support reference clock of PLL come from GPIO single-end clock input
  - Support clock gating control for individual components
  - Support global soft-reset control for whole chip, also individual soft-reset for each component

- PMU(power management unit)
  - Three separate digital voltage domains (DSP_DVDD/CORE_DVDD/PMU_DVDD)
  - Multiple configurable work sleep modes to save power consumption by different frequency or automatic clock gating control or external power on/off control

- Timer
  - Twelve 64bits timers with interrupt-based operation
  - One 64bits timer for low power mode application
  - Support two operation modes: free-running and user-defined count
  - Support timer work state checkable

- PWM
  - 8-channels PWM with interrupt-based operation
  - Support capture mode
  - Provides reference mode and output various duty-cycle waveform
  - Support continuous mode or one-shot mode
  - Support one channel IR RX application
  - Support one clock frequency calculation engine and one clock free running counter
  - Support three channels as waveform generation through lookup table
  - Support three channels as led controller

- Watchdog
  - Support three 32-bit watchdog counter
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout

- WDT can perform two types of operations when timeout occurs:
  - Generate a system reset
  - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
- Programmable reset pulse length
- Totally 16 defined ranges of main timeout period

- Mailbox
  - One Mailbox to service different core's communication
  - Support sixteen mailbox elements, each element includes one data word, one command word register and one flag bit that can represent one interrupt

- Spinlock
  - Support spinlock registers for software to realize resource management

- DMA
  - Support two embedded DMA controllers
  - Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory
  - Support 36 logic channels and 4 physical channels for each DMA controller

- Secure System
  - Cipher engine
    - Support SHA-1, SHA-256/224, MD5 with hardware padding
    - Support HMAC of SHA-1, SHA-256, MD5 with hardware padding
    - Support AES-128, AES-192, AES-256 encrypt & decrypt cipher
    - Support AES ECB/CBC/OFB/CFB/CTR/CTS/XTS/CCM/GCM/CBC-MAC/CMAC mode
    - Support up to 4096 bits PKA mathematical operations for RSA
  - Support two 256 bits RNG output
  - Support secure boot
  - Support secure debug
  - Support secure OTP
  - Support secure OS
  - Support bus firewall

1.2.7 Video Output Processor

- Support RGB888/RGB565 source data format
- Support RGB888/RGB565/RGB666 display data format
- Support i8080 MCU serial interface
- Support max output resolution 480x480

1.2.8 Audio Interface

- SAI
  - Support eight SAI components
  - Support audio protocol: I2S, PCM, TDM
  - Support up to 128 slots available with configurable size
  - Support slot length 8 to 32 bits configurable
  - Support slot valid data length 8 to 32 bits configurable
  - SAI0 support up to four lane transmitter and four lane parallel receiver
  - SAI1~3 support up to two lane transmitter and two lane parallel receiver
  - SAI4~7 support up to one lane transmitter and one lane receiver
  - Support combine different SAI component to meet more transmitter and receiver lane

- PDM
  - Support PDM master receive mode

- Support 5 wire PDM interface with one is clock and 4 data line
- Support up to 8 mono microphones
- Support 16~24 bits sample resolution

- SPDIF
  - Support SPDIF TX x 1
  - Support SPDIF RX x 1
  - Support 16bits/20bits/24bits resolution
  - Support linear PCM mode (IEC-60958)
  - Support non-linear PCM transfer (IEC-61937)

- ASRC
  - Support eight ASRC components
  - Support fixed length conversion mode and real time conversion mode
  - Support asynchronous sample rate clock for real time conversion mode
  - ASRC0 support 8 channel sample rate converter
  - ASRC1 support 4 channel sample rate converter
  - ASRC2~7 support 2 channel sample rate converter
  - Support combine different ASRC component to meet more channel sample rate converter

1.2.9 Connectivity

- RMII 10/100 Ethernet Controller
  - Support one Ethernet Controller
  - Supports 10/100-Mbps data transfer rates with the RMII interfaces
  - Supports both full-duplex and half-duplex operation
  - Support IEEE 1588-2002 (version 1) and IEEE 1588-2008 (version 2) Timestamp
  - Support Flexible Pulse-Per-Second (PPS) Output

- USB 2.0 OTG
  - Support one USB 2.0 OTG port
  - Compatible with USB 2.0 specification
  - Supports high-speed (480Mbps), full-speed (12Mbps) and low-speed (1.5Mbps) mode

- FLEXBUS interface
  - High Speed Interface
    - Support transfer data from internal memory to GPIO by DMA
    - Support transfer data from GPIO to internal memory by DMA
    - Support Multiplexing TX clock and RX clock and Multiplexing TX data and RX data
    - Support TX only mode, RX only mode, TX then RX mode
    - Support clock free running mode and following data mode
    - Support TX data width 1, 2, 4 bit configurable
    - Support RX data width 1, 2, 4 bit configurable
    - Support continue transmission mode and fix length transmission mode
    - Support one chip selection function
    - Support TX clock auto gating
  - Low Speed Interface
    - Support two channels low speed interface
    - Support software configurable as I2C, UART, SPI and SAI interface protocol for each channel

- SPI interface
  - Support four SPI interface
  - SPI0/SPI3 support serial-slave mode

- SPI1/SPI2 support serial-master and serial-slave mode, software-configurable
- Support direct connection from SPI0 interface to Serial Flash Interface

- I2C interface
  - Support seven I2C interface
  - I2C0 support as slave mode
  - I2C1~6 support as master mode
  - Support data rate up to Standard-mode 100 Kbit/s , Fast-mode 400 Kbit/s and Fast-mode Plus 1 Mbit/s

- UART Controller
  - Support four UART interface
  - Embedded two 64-byte FIFO for TX and RX operation respectively
  - Support 5bit, 6bit, 7bit, 8bit serial data transmit or receive
  - Standard asynchronous communication bits such as start, stop and parity
  - Support different input clock for UART operation to get up to 4Mbps baud rate
  - Support auto flow control mode

- CAN Controller
  - Support one CAN interface
  - Compatible with ISO 11898-1-2003 specification
  - Support transmit or receive standard frame
  - Support transmit or receive extended frame

- CEC Controller
  - Support one HDMI CEC interface
  - Support Initiator Mode and Follower Mode

1.2.10 Others

- Multiple groups of GPIO
  - All of GPIOs can be used to generate interrupt
  - Support level trigger and edge trigger interrupt
  - Support configurable polarity of level trigger interrupt
  - Support configurable rising edge, falling edge and both edge trigger interrupt
  - Support configurable pull direction (pullup or pulldown)
  - Support configurable drive strength
  - Support configurable slew rate

- Temperature Sensor (TS-ADC)
  - Up to 50KS/s sampling rate
  - Support one temperature sensor
  - -40~125℃ temperature range and +/-5℃ temperature accuracy

- Successive Approximation ADC (SARADC)
  - 10-bit resolution
  - Up to 1MS/s sampling rate
  - 4 single-ended input channels
  - GPIO multiplexed

- OTP
  - Support 8K bits Size, 6.5K bit for secure application
  - Support Program/Read/Idle mode

- Package Type
  - RK2116M2: QFP128L(body: 14mm x 14mm; lead pitch: 0.4mm)
    - ◆ Not MCP CODEC and pSRAM

1.3 Block Diagram

The following diagram shows the basic block diagram.

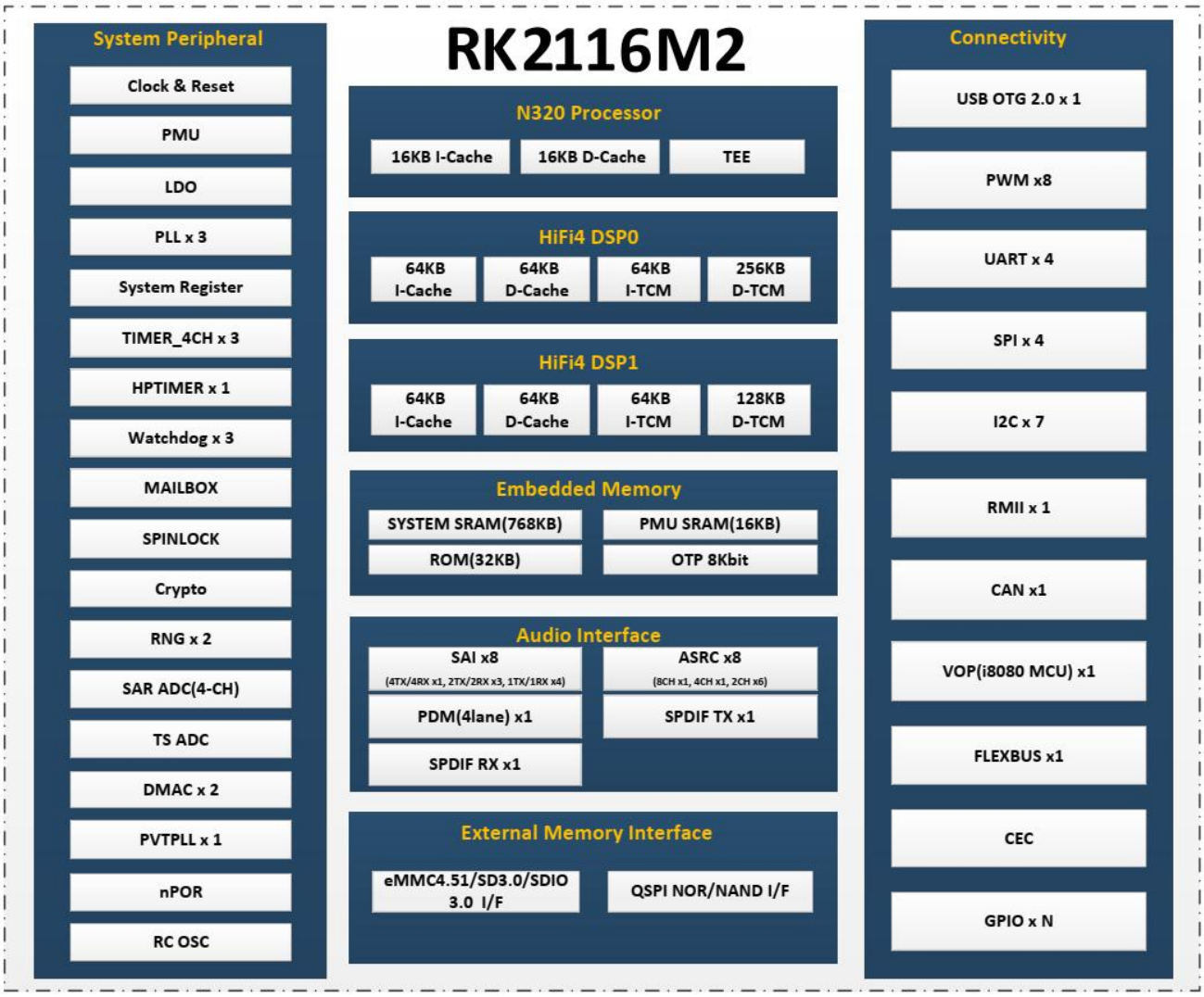

Fig.1-1 RK2116M2 Block Diagram

Chapter 2 Package Information

2.1 Order Information

Orderable Device	RoHS status	Package	Package Qty	Device Feature
RK2116M2	RoHS	QFP128L	900	Smart audio processor

2.2 Top Marking

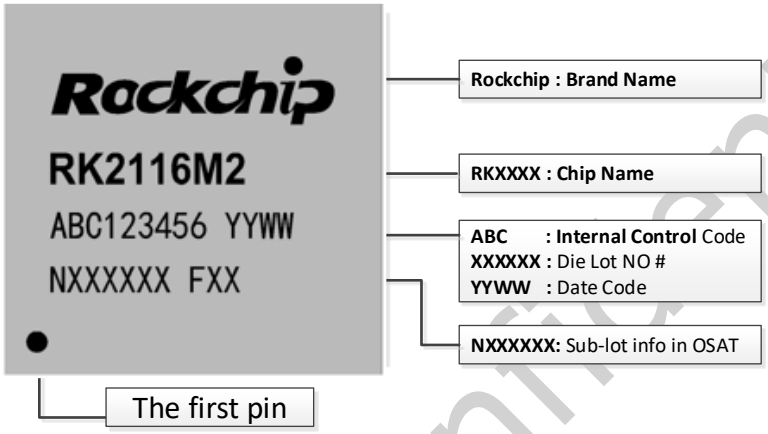

Fig.2-1 RK2116M2 Package Definition

2.3 Package Dimension

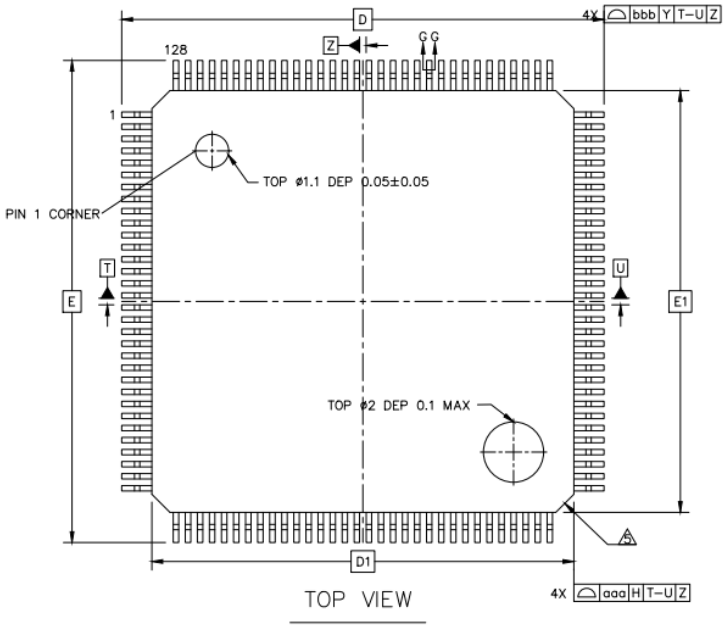

Fig.2-2 RK2116M2 Package Top View

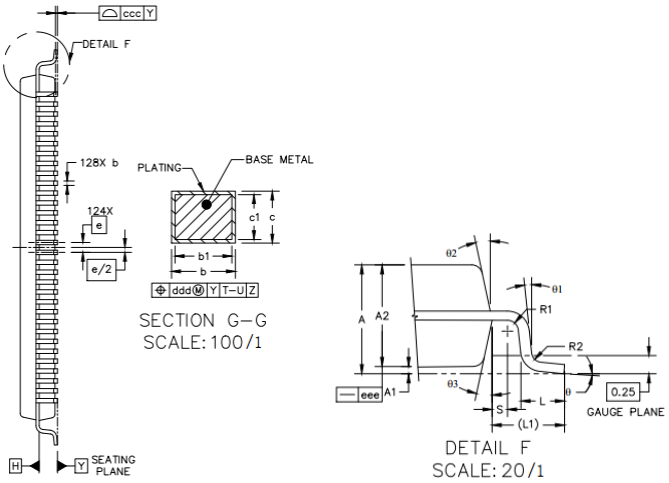

Fig.2-3 RK2116M2 Package Side View

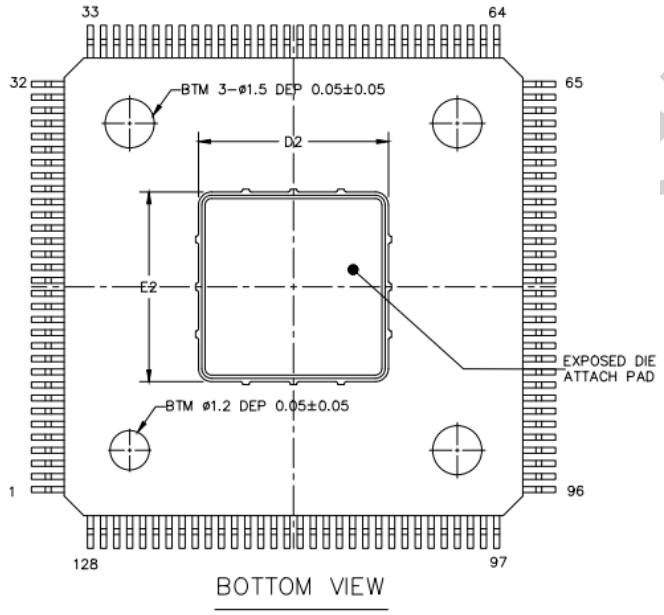

Fig. 2-4 RK2116M2 Package Bottom View

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.025	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	0.14	0.20
L/F THICKNESS		c1	0.09	0.12	0.16
BODY SIZE	X	D	15.85	16.00	16.15
	Y	E	15.85	16.00	16.15
	X	D1	13.90	14.00	14.10
	Y	E1	13.90	14.00	14.10
EP SIZE	X	D2	5.70	5.75	5.80
	Y	E2	5.70	5.75	5.80
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.08		
MOLD FLATNESS		eee	0.05		

Fig.2-5 RK2116M2 Package Dimension

2.4 MSL Information

Moisture sensitivity Level: MSL3

2.5 Lead Finish/Ball Material Information

Lead Finish/Ball material: Sn

2.6 Pin Number List

Table 2-1 RK2116M2 Pin Number Order Information

Pin	Pin Name	Abbreviated Pin Name
1	USB2_OTG_VBUSDET	USB2_OTG_VBUSDET
2	LDO2_3V3_VIN	LDO2_3V3_VIN
3	LDO2_1V8_COUT	LDO2_1V8_COUT
4	SARADC_IN2/GPIO5_C4_z	SARADC_IN2/GPIO5_C4
5	SARADC_IN3/GPIO5_C5_z	SARADC_IN3/GPIO5_C5
6	SARADC_IN0_BOOT	SARADC_IN0_BOOT
7	SARADC_IN1/GPIO5_C3_z	SARADC_IN1/GPIO5_C3
8	CORE_DVDD_0	CORE_DVDD
9	RM2_IO16/GPIO3_A0_d	GPIO3_A0
10	RM2_IO17/GPIO3_A1_d	GPIO3_A1
11	RM2_IO18/GPIO3_A2_d	GPIO3_A2
12	RM2_IO19/GPIO3_A3_d	GPIO3_A3
13	RM1_IO0/RM2_IO20/GPIO3_A4_d	GPIO3_A4
14	VCCIO3_VCC	VCCIO3_VCC
15	RM1_IO1/RM2_IO21/GPIO3_A5_d	GPIO3_A5
16	RM1_IO2/RM2_IO22/GPIO3_A6_d	GPIO3_A6
17	RM1_IO3/RM2_IO23/GPIO3_A7_d	GPIO3_A7
18	ETH_RMII_RXD0/RM1_IO4/GPIO3_B0_d	GPIO3_B0
19	ETH_RMII_RXD1/RM1_IO5/GPIO3_B1_d	GPIO3_B1
20	ETH_RMII_CLK/RM1_IO6/GPIO3_B2_d	GPIO3_B2
21	ETH_RMII_TXD0/RM1_IO7/GPIO3_B3_d	GPIO3_B3
22	ETH_RMII_TXEN/RM1_IO9/GPIO3_B5_d	GPIO3_B5
23	ETH_RMII_TXD1/RM1_IO8/GPIO3_B4_d	GPIO3_B4
24	ETH_RMII_MDC/RM1_IO10/GPIO3_B6_d	GPIO3_B6
25	ETH_RMII_MDIO/RM1_IO11/GPIO3_B7_d	GPIO3_B7
26	ETH_RMII_RXDV_CRS/RM1_IO12/GPIO3_C0_d	GPIO3_C0
27	FSPI_D3/RM2_IO24/GPIO4_A0_d	GPIO4_A0
28	FSPI_D1/RM2_IO25/GPIO4_A1_d	GPIO4_A1
29	VCCIO4_VCC	VCCIO4_VCC
30	FSPI_CSN/RM2_IO26/GPIO4_A2_u	GPIO4_A2
31	FSPI_D0/RM2_IO27/GPIO4_A3_d	GPIO4_A3
32	FSPI_CLK/RM2_IO28/GPIO4_A4_d	GPIO4_A4
33	FSPI_D2/RM2_IO29/GPIO4_A5_d	GPIO4_A5
34	CORE_DVDD_1	CORE_DVDD
35	RM1_IO13/RM2_IO30/GPIO4_A6_d	GPIO4_A6
36	RM1_IO14/RM2_IO31/GPIO4_A7_d	GPIO4_A7
37	RM1_IO15/RM2_IO32/GPIO4_B0_d	GPIO4_B0
38	RM1_IO16/RM2_IO33/GPIO4_B1_d	GPIO4_B1

Pin	Pin Name	Abbreviated Pin Name
39	RM1_IO17/RM2_IO34/GPIO4_B2_d	GPIO4_B2
40	RM1_IO18/RM2_IO35/GPIO4_B3_d	GPIO4_B3
41	DSP_DVDD_0	DSP_DVDD
42	VSS_0	VSS
43	DSP_DVDD_1	DSP_DVDD
44	VSS_1	VSS
45	DSP_DVDD_2	DSP_DVDD
46	VSS_2	VSS
47	DSP_DVDD_3	DSP_DVDD
48	NC_0	NC
49	VSS_3	VSS
50	NC_1	NC
51	DSP_DVDD_4	DSP_DVDD
52	VSS_3	VSS
53	DSP_DVDD_5	DSP_DVDD
54	CORE_DVDD_2	CORE_DVDD
55	RM2_IO0/GPIO1_A0_d	GPIO1_A0
56	RM2_IO1/GPIO1_A1_d	GPIO1_A1
57	RM2_IO2/GPIO1_A2_d	GPIO1_A2
58	RM2_IO3/GPIO1_A3_d	GPIO1_A3
59	RM2_IO4/GPIO1_A4_d	GPIO1_A4
60	RM2_IO5/GPIO1_A5_d	GPIO1_A5
61	VCCIO1_VCC	VCCIO1_VCC
62	RM0_IO9/RM2_IO8/GPIO1_B0_d	GPIO1_B0
63	RM0_IO10/RM2_IO9/GPIO1_B1_d	GPIO1_B1
64	RM0_IO11/RM2_IO10/GPIO1_B2_d	GPIO1_B2
65	RM2_IO6/GPIO1_A6_d	GPIO1_A6
66	RM2_IO7/GPIO1_A7_d	GPIO1_A7
67	RM0_IO12/RM2_IO11/GPIO1_B3_d	GPIO1_B3
68	SDMMC_CLK/RM0_IO13/GPIO2_A0_d	GPIO2_A0
69	SDMMC_D0/RM0_IO15/GPIO2_A2_d	GPIO2_A2
70	SDMMC_CMD/RM0_IO14/GPIO2_A1_d	GPIO2_A1
71	SDMMC_D1/DSP_JTAG_TRSTN_M0/TEST_CLK_OUT/RM0_IO16/GPIO2_A3_d	GPIO2_A3
72	SDMMC_D2/MCU_JTAG_TCK_M0/DSP_JTAG_TCK_M0/RM0_IO17/GPIO2_A4_d	GPIO2_A4
73	VCCIO2_VCC	VCCIO2_VCC
74	SDMMC_D3/MCU_JTAG_TMS_M0/DSP_JTAG_TMS_M0/RM0_IO18/GPIO2_A5_d	GPIO2_A5
75	SPI0_CSN/RM0_IO19/GPIO2_A6_u	GPIO2_A6
76	SPI0_MISO/RM0_IO20/GPIO2_A7_u	GPIO2_A7
77	SPI0_CLK/RM0_IO21/GPIO2_B0_u	GPIO2_B0
78	SPI0_MOSI/RM0_IO22/GPIO2_B1_d	GPIO2_B1
79	GPIO2_B6_z	GPIO2_B6
80	CORE_DVDD_3	CORE_DVDD
81	DSP_JTAG_TDI_M0/RM2_IO12/GPIO2_B2_d	GPIO2_B2
82	DSP_JTAG_TDO_M0/RM2_IO13/GPIO2_B3_d	GPIO2_B3
83	RM2_IO14/GPIO2_B4_d	GPIO2_B4
84	RM2_IO15/GPIO2_B5_d	GPIO2_B5
85	HDMI_HPD/GPIO0_C0_z	GPIO0_C0
86	HDMI_CEC/GPIO0_B7_u	GPIO0_B7
87	HDMI_I2C3_SDA/GPIO0_B4_z	GPIO0_B4

Pin	Pin Name	Abbreviated Pin Name
88	HDMI_I2C3_SCL/GPIO0_B3_z	GPIO0_B3
89	UART0_RX_M0/MCU_JTAG_TMS_M2/GPIO0_B2_u	GPIO0_B2
90	UART0_TX_M0/MCU_JTAG_TCK_M2/GPIO0_B1_u	GPIO0_B1
91	PWR_CTRL3/PWM0_CH3_M1/RM0_IO8/GPIO0_B0_u	GPIO0_B0
92	PWR_CTRL2/PWM0_CH2_M1/RM0_IO7/GPIO0_A7_u	GPIO0_A7
93	TSADC_CTRL/RM0_IO0/GPIO0_A0_z	GPIO0_A0
94	NPOR_DET	NPOR_DET
95	PMU_DVDD0V9	PMU_DVDD0V9
96	PMUIO_VCC3V3	PMUIO_VCC3V3
97	PWR_CTRL0/PWM0_CH0_M1/RM0_IO5/GPIO0_A5_d	GPIO0_A5
98	PWR_CTRL1/PWM0_CH1_M1/RM0_IO6/GPIO0_A6_d	GPIO0_A6
99	REF_CLK_OUT/PWM0_CH3_M0/RM0_IO4/GPIO0_A4_d	GPIO0_A4
100	AUPLL_CLK_IN/PWM0_CH2_M0/RM0_IO3/GPIO0_A3_d	GPIO0_A3
101	ETH_CLK_25M_OUT/PWM0_CH1_M0/RM0_IO2/GPIO0_A2_d	GPIO0_A2
102	CLK_32K/PWM0_CH0_M0/RM0_IO1/GPIO0_A1_d	GPIO0_A1
103	LDO0_3V3_VIN	LDO1_3V3_VIN
104	OSC_XIN	OSC_XIN
105	OSC_XOUT	OSC_XOUT
106	VSS_5	VSS
107	VO_LCDC_RDN/RM1_IO19/GPIO5_A0_d	GPIO5_A0
108	VO_LCDC_CSN/RM1_IO20/GPIO5_A1_u	GPIO5_A1
109	VO_LCDC_RS/RM1_IO21/GPIO5_A2_u	GPIO5_A2
110	VO_LCDC_WRN/RM1_IO22/RM2_IO36/GPIO5_A3_d	GPIO5_A3
111	VO_LCDC_D0/RM1_IO23/RM2_IO37/GPIO5_A4_d	GPIO5_A4
112	VO_LCDC_D1/RM1_IO24/RM2_IO38/GPIO5_A5_d	GPIO5_A5
113	VO_LCDC_D2/FLEXBUS0_CLK/RM2_IO39/GPIO5_A6_d	GPIO5_A6
114	VO_LCDC_D3/FLEXBUS0_CSN/RM2_IO40/GPIO5_A7_d	GPIO5_A7
115	VO_LCDC_D4/FLEXBUS0_D3/RM2_IO41/GPIO5_B0_d	GPIO5_B0
116	CORE_DVDD_4	CORE_DVDD
117	VCCIO5_VCC	VCCIO5_VCC
118	VO_LCDC_D5/FLEXBUS0_D2/RM2_IO42/GPIO5_B1_d	GPIO5_B1
119	VO_LCDC_D6/FLEXBUS0_D1/RM2_IO43/GPIO5_B2_d	GPIO5_B2
120	VO_LCDC_D7/FLEXBUS0_D0/RM2_IO44/GPIO5_B3_d	GPIO5_B3
121	FLEXBUS_LS_D0/RM2_IO45/GPIO5_B4_d	GPIO5_B4
122	FLEXBUS_LS_D1/RM2_IO46/GPIO5_B5_d	GPIO5_B5
123	FLEXBUS_LS_D2/RM2_IO47/GPIO5_B6_d	GPIO5_B6
124	FLEXBUS_LS_D3/RM2_IO48/GPIO5_B7_d	GPIO5_B7
125	FLEXBUS_LS_D5/RM2_IO50/GPIO5_C1_d	GPIO5_C1
126	FLEXBUS_LS_D4/RM2_IO49/GPIO5_C0_d	GPIO5_C0
127	USB2_OTG_DM	USB2_OTG_DM
128	USB2_OTG_DP	USB2_OTG_DP
EPAD	VSS	VSS

2.7 Power/Ground IO Description

Table 2-2 RK2116M2 Power/Ground IO information

Group	Pin#	Descriptions
VSS	42,44,46,49,52,106,EPAD	Digital Ground

Group	Pin#	Descriptions
CORE_DVDD	8,34,54,80,116	Logic Power
DSP_DVDD	41,43,45,47,51,53	DSP0 Power
PMU_DVDD0V9	95	PMU Power
PMUIO_VCC3V3	96	PMU IO Power
VCCIO1_VCC	61	VCCIO1 IO Power
VCCIO2_VCC	73	VCCIO2 IO Power
VCCIO3_VCC	14	VCCIO3 IO Power
VCCIO4_VCC	29	VCCIO4 IO Power
VCCIO5_VCC	117	VCCIO5 IO Power
LDO1_3V3_VIN	103	Analog Power
LDO2_3V3_VIN	2	Analog Power

2.8 Function IO Description

Table 2-3 RK2116M2 Function IO description

Pin	Pin Name	Func0	Func1	Func2	Func3	Func4	Func5	Pad Type①	Def②	Pull	Power Domain
104	OSC_XIN	OSC_XIN						I	I	N/A	LDO1_3V3_IN
105	OSC_XOUT	OSC_XOUT						O	O	N/A	
94	NPOR_DET	NPOR_DET						I	I	N/A	PMUIO_VCC3V3
93	TSADC_CTRL/RM0_IO0/GPIO0_A0_Z	GPIO0_A0	TSADC_CTRL				RM0_IO0	IO	I	z	
102	CLK_32K/PWM0_CH0_M0/RM0_IO1/GPIO0_A1_D	GPIO0_A1	CLK_32K	PWM0_CH0_M0			RM0_IO1	IO	I	down	
101	ETH_CLK_25M_OUT/PWM0_CH1_M0/RM0_IO2/GPIO0_A2_D	GPIO0_A2	ETH_CLK_25M_OUT	PWM0_CH1_M0			RM0_IO2	IO	I	down	
100	AUPLL_CLK_IN/PWM0_CH2_M0/RM0_IO3/GPIO0_A3_D	GPIO0_A3	AUPLL_CLK_IN	PWM0_CH2_M0			RM0_IO3	IO	I	down	
99	REF_CLK_OUT/PWM0_CH3_M0/RM0_IO4/GPIO0_A4_D	GPIO0_A4	REF_CLK_OUT	PWM0_CH3_M0			RM0_IO4	IO	I	down	
97	PWR_CTRL0/PWM0_CH0_M1/RM0_IO5/GPIO0_A5_D	GPIO0_A5	PWR_CTRL0	PWM0_CH0_M1			RM0_IO5	IO	I	down	
98	PWR_CTRL1/PWM0_CH1_M1/RM0_IO6/GPIO0_A6_D	GPIO0_A6	PWR_CTRL1	PWM0_CH1_M1			RM0_IO6	IO	I	up	
92	PWR_CTRL2/PWM0_CH2_M1/RM0_IO7/GPIO0_A7_U	GPIO0_A7	PWR_CTRL2	PWM0_CH2_M1			RM0_IO7	IO	I	up	
91	PWR_CTRL3/PWM0_CH3_M1/RM0_IO8/GPIO0_B0_U	GPIO0_B0	PWR_CTRL3	PWM0_CH3_M1			RM0_IO8	IO	I	up	
90	UART0_TX_M0/MCU_JTAG_TCK_M2/GPIO0_B1_U	GPIO0_B1	UART0_TX_M0		MCU_JTAG_TCK_M2			IO	I	up	
89	UART0_RX_M0/MCU_JTAG_TMS_M2/GPIO0_B2_U	GPIO0_B2	UART0_RX_M0		MCU_JTAG_TMS_M2			IO	I	up	
88	HDMI_I2C_SCL		HDMI_I2C_SCL					IO	I	z	
87	HDMI_I2C_SDA		HDMI_I2C_SDA					IO	I	z	
86	HDMI_CEC/GPIO0_B7_U	GPIO0_B7	HDMI_CEC					IO	I	up	
85	HDMI_HPD/GPIO0_C0_Z	GPIO0_C0	HDMI_HPD					IO	I	z	
55	RM2_IO0/GPIO1_A0_D	GPIO1_A0					RM2_IO0	IO	I	down	VCCIO1_VCC
56	RM2_IO1/GPIO1_A1_D	GPIO1_A1					RM2_IO1	IO	I	down	
57	RM2_IO2/GPIO1_A2_D	GPIO1_A2					RM2_IO2	IO	I	down	
58	RM2_IO3/GPIO1_A3_D	GPIO1_A3					RM2_IO3	IO	I	down	
59	RM2_IO4/GPIO1_A4_D	GPIO1_A4					RM2_IO4	IO	I	down	
60	RM2_IO5/GPIO1_A5_D	GPIO1_A5					RM2_IO5	IO	I	down	
65	RM2_IO6/GPIO1_A6_D	GPIO1_A6					RM2_IO6	IO	I	down	
66	RM2_IO7/GPIO1_A7_D	GPIO1_A7					RM2_IO7	IO	I	down	
62	RM0_IO9/RM2_IO8/GPIO1_B0_D	GPIO1_B0				RM0_IO9	RM2_IO8	IO	I	down	
63	RM0_IO10/RM2_IO9/GPIO1_B1_D	GPIO1_B1				RM0_IO10	RM2_IO9	IO	I	down	

Pin	Pin Name	Func0	Func1	Func2	Func3	Func4	Func5	Pad Type①	Def②	Pull	Power Domain
64	RM0_IO11/RM2_IO10/GPIO1_B2_D	GPIO1_B2				RM0_IO11	RM2_IO10	IO	I	down	
67	RM0_IO12/RM2_IO11/GPIO1_B3_D	GPIO1_B3				RM0_IO12	RM2_IO11	IO	I	down	
68	SDMMC_CLK/RM0_IO13/GPIO2_A0_D	GPIO2_A0	SDMMC_CLK				RM0_IO13	IO	I	down	
70	SDMMC_CMD/RM0_IO14/GPIO2_A1_D	GPIO2_A1	SDMMC_CMD				RM0_IO14	IO	I	down	
69	SDMMC_D0/RM0_IO15/GPIO2_A2_D	GPIO2_A2	SDMMC_D0				RM0_IO15	IO	I	down	
71	SDMMC_D1/DSP_JTAG_TRSTN_M0/TEST_CLK_OUT/RM0_IO16/GPIO2_A3_D	GPIO2_A3	SDMMC_D1		DSP_JTAG_TRSTN_M0	TEST_CLK_OUT	RM0_IO16	IO	I	down	
72	SDMMC_D2/MCU_JTAG_TCK_M0/DSP_JTAG_TCK_M0/RM0_IO17/GPIO2_A4_D	GPIO2_A4	SDMMC_D2	MCU_JTAG_TCK_M0	DSP_JTAG_TCK_M0		RM0_IO17	IO	I	down	
74	SDMMC_D3/MCU_JTAG_TMS_M0/DSP_JTAG_TMS_M0/RM0_IO18/GPIO2_A5_D	GPIO2_A5	SDMMC_D3	MCU_JTAG_TMS_M0	DSP_JTAG_TMS_M0		RM0_IO18	IO	I	down	
75	SPI0_CSN/RM0_IO19/GPIO2_A6_U	GPIO2_A6	SPI0_CSN				RM0_IO19	IO	I	up	
76	SPI0_MISO/RM0_IO20/GPIO2_A7_U	GPIO2_A7	SPI0_MISO				RM0_IO20	IO	I	up	VCCIO2_VCC
77	SPI0_CLK/RM0_IO21/GPIO2_B0_U	GPIO2_B0	SPI0_CLK				RM0_IO21	IO	I	up	
78	SPI0_MOSI/RM0_IO22/GPIO2_B1_D	GPIO2_B1	SPI0_MOSI				RM0_IO22	IO	I	down	
81	DSP_JTAG_TDI_M0/RM2_IO12/GPIO2_B2_D	GPIO2_B2			DSP_JTAG_TDI_M0		RM2_IO12	IO	I	down	
82	DSP_JTAG_TDO_M0/RM2_IO13/GPIO2_B3_D	GPIO2_B3			DSP_JTAG_TDO_M0		RM2_IO13	IO	I	down	
83	RM2_IO14/GPIO2_B4_D	GPIO2_B4					RM2_IO14	IO	I	down	
84	RM2_IO15/GPIO2_B5_D	GPIO2_B5					RM2_IO15	IO	I	down	
79	GPIO2_B6_Z	GPIO2_B6						IO	I	z	
9	RM2_IO16/GPIO3_A0_D	GPIO3_A0					RM2_IO16	IO	I	down	
10	RM2_IO17/GPIO3_A1_D	GPIO3_A1					RM2_IO17	IO	I	down	
11	RM2_IO18/GPIO3_A2_D	GPIO3_A2					RM2_IO18	IO	I	down	
12	RM2_IO19/GPIO3_A3_D	GPIO3_A3					RM2_IO19	IO	I	down	
13	RM1_IO0/RM2_IO20/GPIO3_A4_D	GPIO3_A4				RM1_IO0	RM2_IO20	IO	I	down	
15	RM1_IO1/RM2_IO21/GPIO3_A5_D	GPIO3_A5				RM1_IO1	RM2_IO21	IO	I	down	
16	RM1_IO2/RM2_IO22/GPIO3_A6_D	GPIO3_A6				RM1_IO2	RM2_IO22	IO	I	down	VCCIO3_VCC
17	RM1_IO3/RM2_IO23/GPIO3_A7_D	GPIO3_A7				RM1_IO3	RM2_IO23	IO	I	down	
18	ETH_RMII_RXD0/RM1_IO4/GPIO3_B0_D	GPIO3_B0	ETH_RMII_RXD0			RM1_IO4		IO	I	down	
19	ETH_RMII_RXD1/RM1_IO5/GPIO3_B1_D	GPIO3_B1	ETH_RMII_RXD1			RM1_IO5		IO	I	down	
20	ETH_RMII_CLK/RM1_IO6/GPIO3_B2_D	GPIO3_B2	ETH_RMII_CLK			RM1_IO6		IO	I	down	
21	ETH_RMII_TXD0/RM1_IO7/GPIO3_B3_D	GPIO3_B3	ETH_RMII_TXD0			RM1_IO7		IO	I	down	
23	ETH_RMII_TXD1/RM1_IO8/GPIO3_B4_D	GPIO3_B4	ETH_RMII_TXD1			RM1_IO8		IO	I	down	

Pin	Pin Name	Func0	Func1	Func2	Func3	Func4	Func5	Pad Type①	Def②	Pull	Power Domain
22	ETH_RMII_TXEN/RM1_IO9/GPIO3_B5_D	GPIO3_B5	ETH_RMII_TXEN			RM1_IO9		IO	I	down	
24	ETH_RMII_MDC/RM1_IO10/GPIO3_B6_D	GPIO3_B6	ETH_RMII_MDC			RM1_IO10		IO	I	down	
25	ETH_RMII_MDIO/RM1_IO11/GPIO3_B7_D	GPIO3_B7	ETH_RMII_MDIO			RM1_IO11		IO	I	down	
26	ETH_RMII_RXDV_CRS/RM1_IO12/GPIO3_C0_D	GPIO3_C0	ETH_RMII_RXDV_CRS			RM1_IO12		IO	I	down	
27	FSPI_D3/RM2_IO24/GPIO4_A0_D	GPIO4_A0	FSPI_D3				RM2_IO24	IO	I	down	VCCIO4_VCC
28	FSPI_D1/RM2_IO25/GPIO4_A1_D	GPIO4_A1	FSPI_D1				RM2_IO25	IO	I	down	
30	FSPI_CSN/RM2_IO26/GPIO4_A2_U	GPIO4_A2	FSPI_CSN				RM2_IO26	IO	I	up	
31	FSPI_D0/RM2_IO27/GPIO4_A3_D	GPIO4_A3	FSPI_D0				RM2_IO27	IO	I	down	
32	FSPI_CLK/RM2_IO28/GPIO4_A4_D	GPIO4_A4	FSPI_CLK				RM2_IO28	IO	I	down	
33	FSPI_D2/RM2_IO29/GPIO4_A5_D	GPIO4_A5	FSPI_D2				RM2_IO29	IO	I	down	
35	RM1_IO13/RM2_IO30/GPIO4_A6_D	GPIO4_A6				RM1_IO13	RM2_IO30	IO	I	down	
36	RM1_IO14/RM2_IO31/GPIO4_A7_D	GPIO4_A7				RM1_IO14	RM2_IO31	IO	I	down	
37	RM1_IO15/RM2_IO32/GPIO4_B0_D	GPIO4_B0				RM1_IO15	RM2_IO32	IO	I	down	
38	RM1_IO16/RM2_IO33/GPIO4_B1_D	GPIO4_B1				RM1_IO16	RM2_IO33	IO	I	down	
39	RM1_IO17/RM2_IO34/GPIO4_B2_D	GPIO4_B2				RM1_IO17	RM2_IO34	IO	I	down	
40	RM1_IO18/RM2_IO35/GPIO4_B3_D	GPIO4_B3				RM1_IO18	RM2_IO35	IO	I	down	
107	VO_LCDC_RDN/RM1_IO19/GPIO5_A0_D	GPIO5_A0	VO_LCDC_RDN			RM1_IO19		IO	I	down	VCCIO5_VCC
108	VO_LCDC_CSN/RM1_IO20/GPIO5_A1_U	GPIO5_A1	VO_LCDC_CSN			RM1_IO20		IO	I	up	
109	VO_LCDC_RS/RM1_IO21/GPIO5_A2_U	GPIO5_A2	VO_LCDC_RS			RM1_IO21		IO	I	up	
110	VO_LCDC_WRN/RM1_IO22/RM2_IO36/GPIO5_A3_D	GPIO5_A3	VO_LCDC_WRN			RM1_IO22	RM2_IO36	IO	I	down	
111	VO_LCDC_D0/RM1_IO23/RM2_IO37/GPIO5_A4_D	GPIO5_A4	VO_LCDC_D0			RM1_IO23	RM2_IO37	IO	I	down	
112	VO_LCDC_D1/RM1_IO24/RM2_IO38/GPIO5_A5_D	GPIO5_A5	VO_LCDC_D1			RM1_IO24	RM2_IO38	IO	I	down	
113	VO_LCDC_D2/FLEXBUS0_CLK/RM2_IO39/GPIO5_A6_D	GPIO5_A6	VO_LCDC_D2	FLEXBUS0_CLK			RM2_IO39	IO	I	down	
114	VO_LCDC_D3/FLEXBUS0_CSN/RM2_IO40/GPIO5_A7_D	GPIO5_A7	VO_LCDC_D3	FLEXBUS0_CSN			RM2_IO40	IO	I	down	
115	VO_LCDC_D4/FLEXBUS0_D3/RM2_IO41/GPIO5_B0_D	GPIO5_B0	VO_LCDC_D4	FLEXBUS0_D3			RM2_IO41	IO	I	down	
118	VO_LCDC_D5/FLEXBUS0_D2/RM2_IO42/GPIO5_B1_D	GPIO5_B1	VO_LCDC_D5	FLEXBUS0_D2			RM2_IO42	IO	I	down	
119	VO_LCDC_D6/FLEXBUS0_D1/RM2_IO43/GPIO5_B2_D	GPIO5_B2	VO_LCDC_D6	FLEXBUS0_D1			RM2_IO43	IO	I	down	
120	VO_LCDC_D7/FLEXBUS0_D0/RM2_IO44/GPIO5_B3_D	GPIO5_B3	VO_LCDC_D7	FLEXBUS0_D0			RM2_IO44	IO	I	down	
121	FLEXBUS_LS_D0/RM2_IO45/GPIO5_B4_D	GPIO5_B4		FLEXBUS_LS_D0			RM2_IO45	IO	I	down	
122	FLEXBUS_LS_D1/RM2_IO46/GPIO5_B5_D	GPIO5_B5		FLEXBUS_LS_D1			RM2_IO46	IO	I	down	

Pin	Pin Name	Func0	Func1	Func2	Func3	Func4	Func5	Pad Type①	Def②	Pull	Power Domain
123	FLEXBUS_LS_D2/RM2_IO47/GPIO5_B6_D	GPIO5_B6		FLEXBUS_LS_D2			RM2_IO47	IO	I	down	
124	FLEXBUS_LS_D3/RM2_IO48/GPIO5_B7_D	GPIO5_B7		FLEXBUS_LS_D3			RM2_IO48	IO	I	down	
126	FLEXBUS_LS_D4/RM2_IO49/GPIO5_C0_D	GPIO5_C0		FLEXBUS_LS_D4			RM2_IO49	IO	I	down	
125	FLEXBUS_LS_D5/RM2_IO50/GPIO5_C1_D	GPIO5_C1		FLEXBUS_LS_D5			RM2_IO50	IO	I	down	
6	SARADC_IN0_BOOT/GPIO5_C2_Z	GPIO5_C2	SARADC_IN0_BOOT					IO	I	z	LDO2_3V3_VIN
7	SARADC_IN1/GPIO5_C3_Z	GPIO5_C3	SARADC_IN1					IO	I	z	
4	SARADC_IN2/GPIO5_C4_Z	GPIO5_C4	SARADC_IN2					IO	I	z	
5	SARADC_IN3/GPIO5_C5_Z	GPIO5_C5	SARADC_IN3					IO	I	z	
1	USB2_OTG_VBUSDET	USB2_OTG_VBUSDET						A			
127	USB2_OTG_DM	USB_DP						A			
128	USB2_OTG_DP	USB_DM						A			
3	LDO2_1V8_COUT	LDO2_1V8_COUT						A			

Notes:
□: Pad types: I = input, O = output, I/O = input/output (bidirectional)
AP = Analog Power, AG = Analog Ground
DP = Digital Power, DG = Digital Ground
A = Analog
□: Reset state: I = input, O = output;

2.9 IO Pin Name Description

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 2-4 IO function description list

Interface	Pin Name	Direction	Description
Misc	OSC_XIN	I	Clock input of crystal XO
	OSC_XOUT	O	Clock output of crystal XO
	NPOR	I	Chip hardware reset input
	REF_CLK_OUT	O	REF Clock Output for external function module
	ETH_CLK_25M_OUT	O	REF Clock Output for external function module
	AUPLL_CLK_IN	I	REF Clock Input for internal PLL
	TEST_CLK_OUT	O	Chip internal clock output for measurement
	PWR_CTRL0	O	Chip low power mode output indication signal
	PWR_CTRL1	O	Chip low power mode output indication signal
	PWR_CTRL2	O	Chip low power mode output indication signal
	PWR_CTRL3	O	Chip low power mode output indication signal
	TSADC_CTRL	O	Chip high temperature output indication signal
	CLK_32K	I/O	32K clock If configured as input，clock is provided from external circuit； If configured as output，clock is provided from internal circuit of chip；

Interface	Pin Name	Direction	Description
SWJ-DP	MCU_JTAG_TCK_M*i* (*i*=0~3)	I	SWD interface clock input for MCU
	MCU_JTAG_TMS_M*i* (*i*=0~3)	I/O	SWD interface data input/output for MCU

Interface	Pin Name	Direction	Description
JTAG-DP	DSP_JTAG_TCK*i* (*i*=0~2)	I	JTAG interface for DSP
	DSP_JTAG_TMS*i* (*i*=0~2)	I	
	DSP_JTAG_TDI*i* (*i*=0~2)	I	
	DSP_JTAG_TDO*i* (*i*=0~2)	O	
	DSP_JTAG_TRSTN*i* (*i*=0~2)	I	

Interface	Pin Name	Direction	Description
SD/MMC Controller	SDMMC_CLK	O	sdmmc card clock
	SDMMC_CMD	I/O	sdmmc card command output and response input
	SDMMC_D[*i*] (*i*=0~3)	I/O	sdmmc card data input and output

Interface	Pin Name	Direction	Description
FSPI Controller	FSPI_CLK	O	fspi serial clock
	FSPI_CSN	O	fspi chip select signal, low active
	FSPI_D*i*(*i=0~3)*	I/O	fspi serial data input/output signal

Interface	Pin Name	Direction	Description
MCU Display Interface	VO_LCDC_CSN	O	MCU interface CSN signal
	VO_LCDC_RS	O	MCU interface RS signal
	VO_LCDC_WRN	O	MCU interface WRN signal
	VO_LCDC_RDN	I	MCU interface RDN signal
	VO_LCDC_D*i*(*i*=0~7)	O	MCU interface data input/output

Interface	Pin Name	Direction	Description
SAI0 Controller	SAI*i*_SCLK(*i*=0)	I/O	I2S/PCM/TDM serial clock
	SAI*i*_LRCK(*i*=0)	I/O	I2S/PCM/TDM channel indication signal
	SAI*i*_SDO0(*i*=0)	O	I2S/PCM/TDM serial data output
	SAI*i*_SDO1(*i*=0)	O	I2S/PCM/TDM serial data output
	SAI*i*_SDO2(*i*=0)	O	I2S/PCM/TDM serial data output
	SAI*i*_SDO3(*i*=0)	O	I2S/PCM/TDM serial data output
	SAI*i*_SDI0(*i*=0)	I	I2S/PCM/TDM serial data input
	SAI*i*_SDI1(*i*=0)	I	I2S/PCM/TDM serial data input
	SAI*i*_SDI2(*i*=0)	I	I2S/PCM/TDM serial data input
	SAI*i*_SDI3(*i*=0)	I	I2S/PCM/TDM serial data input

Interface	Pin Name	Direction	Description
SAI1~3 Controller	SAI*i*_SCLK(*i*=1~3)	I/O	I2S/PCM/TDM serial clock
	SAI*i*_LRCK(*i*=1~3)	I/O	I2S/PCM/TDM channel indication signal
	SAI*i*_SDO0(*i*=1~3)	O	I2S/PCM/TDM serial data output
	SAI*i*_SDO1(*i*=1~3)	O	I2S/PCM/TDM serial data output
	SAI*i*_SDI0(*i*=1~3)	I	I2S/PCM/TDM serial data input
	SAI*i*_SDI1(*i*=1~3)	I	I2S/PCM/TDM serial data input

Interface	Pin Name	Direction	Description
SAI4~7 Controller	SAI*i*_SCLK(*i*=4~7)	I/O	I2S/PCM/TDM serial clock
	SAI*i*_LRCK(*i*=4~7)	I/O	I2S/PCM/TDM channel indication signal
	SAI*i*_SDO(*i*=4~7)	O	I2S/PCM/TDM serial data output
	SAI*i*_SDI(*i*=4~7)	I	I2S/PCM/TDM serial data input

Interface	Pin Name	Direction	Description
PDM	PDM_CLK0	O	PDM sampling clock
	PDM_CLK1	O	PDM sampling clock
	PDM_SDI*i*(*i*=0~3)	I	PDM data

Interface	Pin Name	Direction	Description
SPI0/SPI3	SPI*i*_CLK(*i*=0,3)	I	SPI serial clock
	SPI*i*_CSN(*i*=0,3)	I	SPI chip select signal, low active
	SPI*i*_MOSI(*i*=0,3)	I	SPI serial data input
	SPI*i*_MISO(*i*=0,3)	O	SPI serial data output

Interface	Pin Name	Direction	Description
SPI1/SPI2	SPI*i*_CLK(*i*=1~2)	I/O	SPI serial clock
	SPI*i*_CSN0(*i*=1~2)	I/O	SPI chip select signal, low active
	SPI*i*_CSN1(*i*=1~2)	O	SPI chip select signal, low active
	SPI*i*_MISO(*i*=1~2)	I/O	SPI serial data input/output
	SPI*i*_MOSI(*i*=1~2)	I/O	SPI serial data input/output

Interface	Pin Name	Direction	Description
PWM	PWM0_CH*i*_M*j*(*i*=0~3, *j*=0~1)	I/O	Pulse Width Modulation input and output
	PWM1_CH*i*(*i*=0~3)	I/O	Pulse Width Modulation input and output

Interface	Pin Name	Direction	Description
I2C0	I2C0_SDA	I/O	Slave I2C data
	I2C0_SCL	I/O	Slave I2C clock

Interface	Pin Name	Direction	Description
I2C1~6	I2C*i*_SDA(*i*=1~6)	I/O	Master I2C data
	I2C*i*_SCL(*i*=1~6)	I/O	Master I2C clock

Interface	Pin Name	Direction	Description
UART	UART0_RX	I	UART serial data input
	UART0_TX	O	UART serial data output
	UART*i*_RX (*i*=1~3)	I	UART serial data input
	UART*i*_TX (*i*=1~3)	O	UART serial data output
	UART*i*_CTSN (*i*=1~3)	I	UART clear to send modem status input
	UART*i*_RTSN (*i*=1~3)	O	UART modem control request to send output

Interface	Pin Name	Direction	Description
HDMI CEC	HDMI_CEC	I/O	HDMI CEC data
	HDMI_HPD	I	HDMI HPD indication signal

Interface	Pin Name	Direction	Description
RMII	ETH_RMII_CLK	I/O	RMII REC_CLK output or external clock input
	ETH_RMII_MDC	O	RMII management interface clock
	ETH_RMII_MDIO	I/O	RMII management interface data
	ETH_RMII_TXD*i*(*i*=0~1)	O	RMII TX data
	ETH_RMII_RXD*i*(*i*=0~1)	I	RMII RX data
	ETH_RMII_TXEN	O	RMII TX data enable
	ETH_RMII_CRSDV	I	RMII RX indication signal

Interface	Pin Name	Direction	Description
FLEXBUS	FLEXBUS0_CLK	O	FLEXBUS0 clock output
	FLEXBUS0_D*i*(*i*=0~3)	I/O	FLEXBUS0 data input/output
	FLEXBUS0_CSN	O	FLEXBUS0 chip selection output
	FLEXBUS_LS_D*i*(*i*=0~5)	I/O	FLEXBUS low speed data

Interface	Pin Name	Direction	Description
Rockchip matrix IO	RM0_IO*i*(*i*=0~22)	I/O	IO matrix0
	RM1_IO*i*(*i*=0~24)	I/O	IO matrix1
	RM2_IO*i*(*i*=0~50)	I/O	IO matrix2

Interface	Pin Name	Direction	Description
USB 2.0	USB2_OTG_DP	I/O	USB 2.0 Data signal DP

	USB2_OTG_DM	I/O	USB 2.0 Data signal DM
	USB2_OTG_VBUSDET	I	Insert detect when act as USB device

2.10 Rockchip Matrix IO Function List

RK2116M2 support three Rockchip Matrix IO (RM_IO) which are designed to let numerous functional signals share limited pin interfaces. Within the same matrix, any function signal can be mapped to any pin interface by software configurable.

- RM0_IO support 19 function signals map to 23 pin interfaces (GPIO0_A0 ~ GPIO0_B0, GPIO1_B0 ~ GPIO1_B3, GPIO2_A0 ~ GPIO2_B1)
- RM1_IO support 31 function signals map to 25 pin interfaces (GPIO3_A4 ~ GPIO3_C0, GPIO4_A6 ~ GPIO4_B3, GPIO5_A0 ~ GPIO5_A5)
- RM2_IO support 64 function signals map to 51 pin interfaces (GPIO1_A0 ~ GPIO1_B3, GPIO2_B2 ~ GPIO2_B5, GPIO3_A0 ~ GPIO3_A7, GPIO4_A0 ~ GPIO4_B3, GPIO5_A3 ~ GPIO5_C1)

Table 2-5 RK2116M2 Rockchip Matrix IO function list

Function Index	RM0_IO	RM1_IO	RM2_IO
1	PWM0_CH0	UART2_TX	SAI0_SCLK
2	PWM0_CH1	UART2_RX	SAI0_LRCK
3	PWM0_CH2	UART2_CTSN	SAI0_SDO0
4	PWM0_CH3	UART2_RTSN	SAI0_SDO1
5	UART1_TX	UART3_TX	SAI0_SDO2
6	UART1_RX	UART3_RX	SAI0_SDO3
7	UART1_CTSN	UART3_CTSN	SAI0_SDI0
8	UART1_RTSN	UART3_RTSN	SAI0_SDI1
9	I2C1_SCL	I2C4_SCL	SAI0_SDI2
10	I2C1_SDA	I2C4_SDA	SAI0_SDI3
11	I2C2_SCL	I2C5_SCL	SAI_LRCKXN_0
12	I2C2_SDA	I2C5_SDA	SAI_LRCKXN_1
13	I2C3_SCL	I2C6_SCL	SAI1_SCLK
14	I2C3_SDA	I2C6_SDA	SAI1_LRCK
15	SPI1_CLK	PWM1_CH0	SAI1_SDO0
16	SPI1_MOSI	PWM1_CH1	SAI1_SDO1
17	SPI1_MISO	PWM1_CH2	SAI1_SDI0
18	SPI1_CSN0	PWM1_CH3	SAI1_SDI1
19	SPI1_CSN1	CAN_RX	SAI2_SCLK
20		CAN_TX	SAI2_LRCK
21		SPI2_CSN1	SAI2_SDO0

Function Index	RM0_IO	RM1_IO	RM2_IO
22		SPI2_CSN0	SAI2_SDO1
23		SPI2_MISO	SAI2_SDI0
24		SPI2_MOSI	SAI2_SDI1
25		SPI2_CLK	SAI3_SCLK
26		ETH_PPSCLK	SAI3_LRCK
27		ETH_PPSTRIG	SAI3_SDO0
28		SPI3_CSN	SAI3_SDO1
29		SPI3_MISO	SAI3_SDI0
30		SPI3_MOSI	SAI3_SDI1
31		SPI3_CLK	PDM_CLK0
32			PDM_CLK1
33			PDM_SDI0
34			PDM_SDI1
35			PDM_SDI2
36			PDM_SDI3
37			SAI4_SCLK
38			SAI4_LRCK
39			SAI4_SDO
40			SAI4_SDI
41			SAI5_SCLK
42			SAI5_LRCK
43			SAI5_SDO
44			SAI5_SDI
45			SAI6_SCLK
46			SAI6_LRCK
47			SAI6_SDO
48			SAI6_SDI
49			SAI7_SCLK
50			SAI7_LRCK
51			SAI7_SDO
52			SAI7_SDI
53			SPDIF_TX
54			SPDIF_RX

Function Index	RM0_IO	RM1_IO	RM2_IO
55			MCLK0
56			MCLK1
57			MCLK2
58			MCLK3
59			MCLK4
60			MCLK5
61			MCLK6
62			MCLK7
63			UART0_TX
64			UART0_RX

Chapter 3 Electrical Specification

3.1 Absolute Ratings

The below table provides the absolute ratings.
Absolute maximum or minimum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

Table 3-1 Absolute ratings

Parameters	Related Power Group	Min	Max	Unit
Supply voltage for DSP	DSP_DVDD	-0.3	1.05	V
Supply voltage for LOGIC	CORE_DVDD	-0.3	1.05	V
Supply voltage for PMU	PMU_DVDD0V9	-0.3	1.10	V
3.3V supply voltage	PMUIO_VCC3V3 LDO1_3V3_VIN LDO2_3V3_VIN	-0.3	3.80	V
1.8V/3.3V supply voltage	VCCIO1_VCC VCCIO2_VCC VCCIO3_VCC VCCIO4_VCC VCCIO5_VCC	-0.3	3.80	V
Storage Temperature	Tstg	-40	125	℃
Max Conjunction Temperature	Tj	-40	125	℃

3.2 Recommended Operating Condition

Following table describes the recommended operating condition.

Table 3-2 Recommended operating condition

Parameters	Symbol	Min	Typ	Max	Unit
Voltage for DSP	DSP_DVDD	0.85	0.95	1.0	V
Voltage for LOGIC	CORE_DVDD	0.85	0.95	1.0	V
Voltage for PMU	PMU_DVDD0V9	0.85	0.90	1.025	V
Voltage for GPIO (3.3V only)	PMUIO_VCC3V3	3.00	3.30	3.63	V
Voltage for GPIO (1.8V/3.3V)	VCCIO1_VCC VCCIO2_VCC VCCIO3_VCC VCCIO4_VCC VCCIO5_VCC	1.62 3.00	1.80 3.30	1.98 3.63	V
Voltage for Analog (3.3V)	LDO1_3V3_VIN LDO2_3V3_VIN	3.00	3.30	3.63	V
OSC input clock frequency	F_{osc}		24.576		MHz

3.3 DC Characteristics

Table 3-3 DC Characteristics

Parameters		Symbol	Min	Typ	Max	Unit
Digital GPIO @3.3V	Input Low Voltage	Vil	-0.3	NA	0.8	V
	Input High Voltage	Vih	2.0	NA	VDDO+0.3	V
	Output Low Voltage	Vol	-0.3	NA	0.4	V
	Output High Voltage	Voh	2.4	NA	VDDO+0.3	V
	Pullup Resistor	Rpu	16	30	43	Kohm
	Pulldown Resistor	Rpd	16	30	43	Kohm
Digital GPIO @1.8V	Input Low Voltage	Vil	-0.3	NA	0.35*VDDO	V
	Input High Voltage	Vih	0.65*VDDO	NA	VDDO+0.3	V
	Output Low Voltage	Vol	-0.3	NA	0.4	V
	Output High Voltage	Voh	1.4	NA	VDDO+0.3	V
	Pullup Resistor	Rpu	16	30	43	Kohm
	Pulldown Resistor	Rpd	16	30	43	Kohm

3.4 Electrical Characteristics for General IO

Table 3-4 Electrical Characteristics for Digital General IO

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
Digital GPIO @3.3V	Input leakage current	Ii	Vin = 3.3V or 0V	NA	NA	15	uA
	Tri-state output leakage current	Ioz	Vout = 3.3V or 0V	NA	NA	15	uA
	High level input current	Iih	Vin = 3.3V, pulldown disabled	NA	NA	15	uA
			Vin = 3.3V, pulldown enabled	NA	NA	250	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	NA	NA	15	uA
			Vin = 0V, pullup enabled	NA	NA	250	uA
Digital GPIO @1.8V	Input leakage current	Ii	Vin = 1.8V or 0V	NA	NA	15	uA
	Tri-state output leakage current	Ioz	Vout = 1.8V or 0V	NA	NA	15	uA
	High level input current	Iih	Vin = 1.8V, pulldown disabled	NA	NA	15	uA
			Vin = 1.8V, pulldown enabled	NA	NA	150	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	NA	NA	15	uA
			Vin = 0V, pullup enabled	NA	NA	150	uA

3.5 Electrical Characteristics for PLL

Table 3-5 Electrical Characteristics for FRAC PLL

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
	Input clock frequency(Frac)	F_{in}	Fin = FREF	10	NA	1200	MHz
	VCO operating range	F_{vco}	Fvco = FREF * FBDIV	950	NA	3800	MHz
	Output clock frequency	F_{out}	Fout = Fvco/POSTDIV	19	NA	3800	MHz
	Lock time	T_{lt}	FREF=24M,REFDIV=1	NA	250	500	Input clock cycles

Notes:

① *REFDIV is the input divider value;*

② *FBDIV is the feedback divider value;*

③ *POSTDIV is the output divider value*

3.6 Electrical Characteristics for USB2.0 Interface

Table 3-6 Electrical Characteristics for USB2.0 Interface

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Transmitter						
Output Resistance	ROUT	Classic mode (Vout = 0 or 3.3V)	40.5	45	49.5	ohms
		HS mode (Vout = 0 to 800mV)	40.5	45	49.5	ohms
Output Capacitance	COUT	seen from D+ or D-			3	pF
Output Common Mode Voltage	VM	Classic (LS/FS) mode	1.45	1.65	1.85	V
		HS mode	0.175	0.2	0.225	V
Differential output signal high	VOH	Classic (LS/FS); Io=0mA	2.97	3.3	3.63	V
		Classic (LS/FS); Io=6mA	2.2	2.7	NA	V
		HS mode; Io=0mA	360	400	440	mV
Differential output signal low	VOL	Classic (LS/FS); Io=0mA	-0.33	0	0.33	V
		Classic (LS/FS); Io=6mA	NA	0.3	0.8	V
		HS mode; Io=0mA	-40	0	40	mV
Receiver						
Receiver sensitivity	RSENS	Classic mode	NA	+-250	NA	mV
		HS mode	NA	+-25	NA	mV
Receiver common mode	RCM	Classic mode	0.8	1.65	2.5	V
		HS mode (differential and squelch comparator)	0.1	0.2	0.3	V
		HS mode (disconnect comparator)	0.5	0.6	0.7	V
Input capacitance (seen at D+ or D-)			NA	NA	3	pF

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Squelch threshold			100	NA	150	mV
Disconnect threshold			570	600	664	mV

3.7 Electrical Characteristics for SARADC

Table 3-7 Electrical Characteristics for SARADC

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Resolution			NA	10	NA	bit
Effective Number of Bit	ENOB		NA	9	NA	bit
Differential Non-Linearity	DNL		-1	NA	+1	LSB
Integral Non-Linearity	INL		-2	NA	+2	LSB
Reference voltage	VREFP		NA	1.8	NA	V
Input Capacitance	C_{IN}		NA	8	NA	pF
Sampling Rate	f_S		NA	NA	1	MS/s
Spurious Free Dynamic Range	SFDR	f_S=1MS/s f_{OUT}=1.17KHz	NA	61	NA	dB
Signal to Noise and Harmonic Ratio	SNDR		NA	56	NA	dB

3.8 Electrical Characteristics for TSADC

Table 3-8 Electrical Characteristics for TSADC

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Accuracy from -40℃ to 125℃	T_{JACC}		NA	NA	±5	℃
Sensing Temperature Range	T_{RANGE}		-40	NA	125	℃
Resolution	T_{LSB}		NA	0.6	NA	℃

Chapter 4 Timing Specification

4.1 FSPI

The following table gives the FSPI electrical characteristics.
Test conditions: maximum output load 15 pF, input transition time 2 ns, drive strength set to 6'b000111, and Slew Rate set to 2'b11.

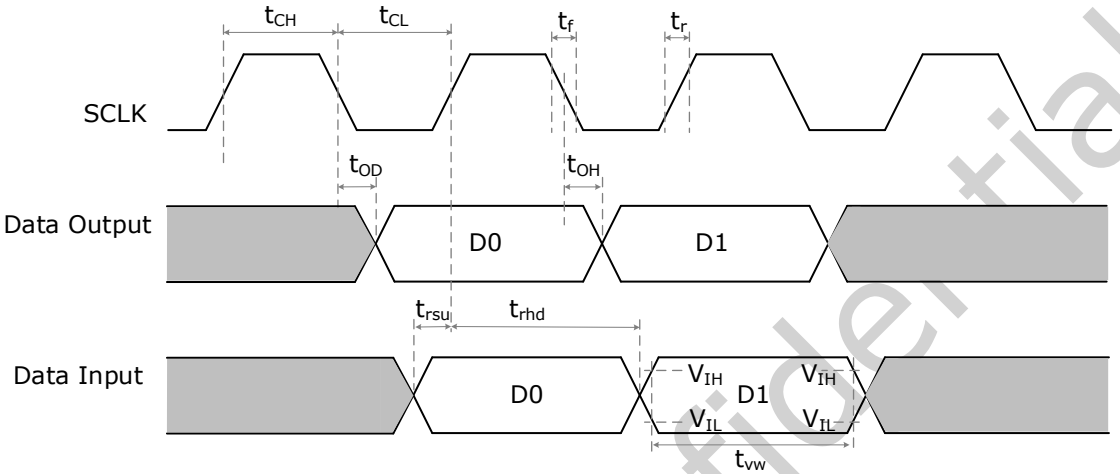

Fig. 4-1 FSPI SCLK and data timing diagram (SDR read mode and write mode)

Table 4-1 FSPI Electrical Specification in VDDxx SDR Read Mode and Write Mode

Parameter		Min	Typ	Max	Min	Typ	Max	Unit
		1.8V			3.3V			
f_{SCLK}	FSPI Clock Frequency			125			125	MHz
t_{CH}	Clock High	t_{CK}*45%		t_{CK}*55%	t_{CK}*45%		t_{CK}*55%	ns
t_{CL}	Clock Low	t_{CK}*45%		t_{CK}*55%	t_{CK}*45%		t_{CK}*55%	ns
t_{OD}	Data output valid time	-1		1	-1		1	ns
t_{OH}	Data output hold time	-1		1	-1		1	ns
t_{rsu}*1	Data input setup time for rise edge sampling	6.1			5.8			ns
t_{rhd}	Data input hold time for rise edge sampling	0			0			ns
t_{vw}	Data valid window	0.5* t_{CK}			0.5* t_{CK}			

NOTE (1):
1. When the signal rate exceeds 50 MHz, it is acceptable as long as it meets the t_{vw} specification requirements.
2. Supports delaying the sampling edge by 180 degrees to reduce the setup time requirement. In addition, a Delayline module is also support which can adjust the phase of the signal passing through the module to achieve phase calibration in high-frequency scenarios

4.2 SDMMC

The following table gives the SDMMC electrical characteristics.
Test conditions: maximum output load 15 pF, input transition time 2 ns, drive strength set to 6'b000111, and Slew Rate set to 2'b11.I

4.2.1 Default Speed Mode

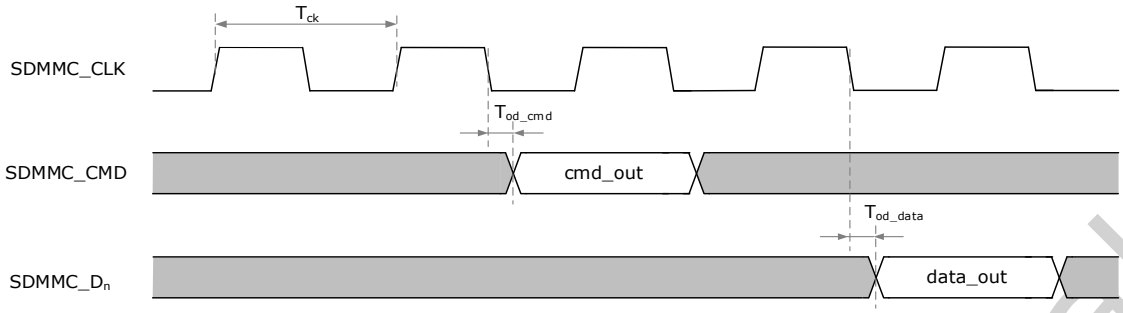

Fig. 4-2 SDMMC Default Speed Mode Output Timing

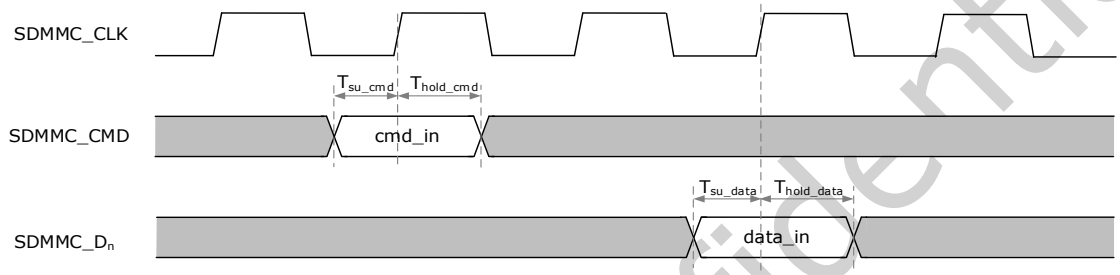

Fig. 4-3 SDMMC Default Speed Mode Input Timing

Table 4-2 SDMMC Default Speed Mode Timing Parameter

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
		1.8V			3.3V			
CMD Interface								
T_{su_cmd}	Command input setup time	8.3			8			ns
T_{hold_cmd}	Command input hold time	0			0			ns
T_{od_cmd}	Command output delay time	-2		2	-2		2	ns
DATA Interface								
T_{su_data}	Data input setup time	8.3			8			ns
T_{hold_data}	Data input hold time	0			0			ns
T_{od_data}	Data output delay time	-2		2	-2		2	ns
Clock Interface								
T_{ck}	Clock cycle time	20			40			ns

4.2.2 High Speed Mode

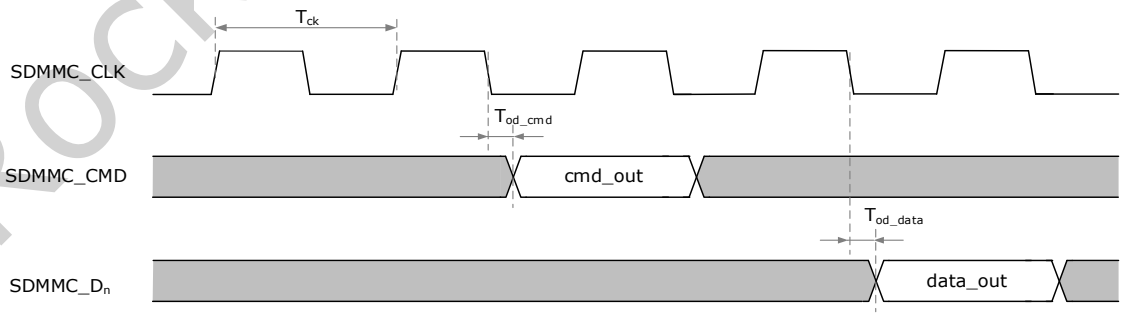

Fig. 4-4 SDMMC High Speed Mode Output Timing

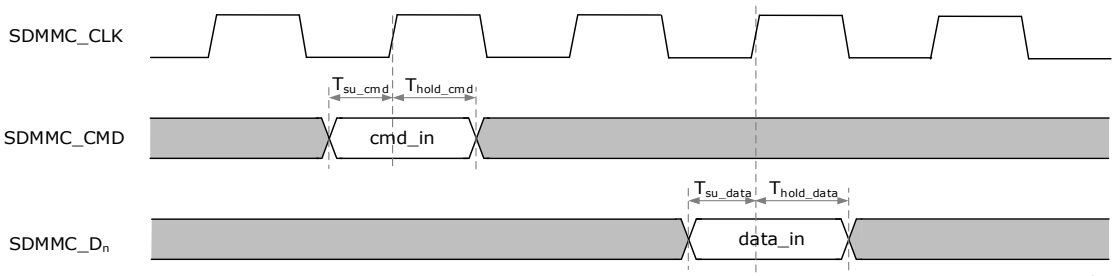

Fig. 4-5 SDMMC High Speed Mode Input Timing

Table 4-3 SDMMC High Speed Mode Timing Parameter

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
		1.8V			3.3V			
CMD Interface								
T_{su_cmd}	Command input setup time	8.3			8			ns
T_{hold_cmd}	Command input hold time	0			0			ns
T_{od_cmd}	Command output delay time	-2		2	-2		2	ns
DATA Interface								
T_{su_data}	Data input setup time	8.3			8			ns
T_{hold_data}	Data input hold time	0			0			ns
T_{od_data}	Data output delay time	-2		2	-2		2	ns
Clock Interface								
T_{ck}	Clock cycle time	10			20			ns

4.3 RMII

The following table gives the RMII electrical characteristics.
Test conditions: maximum output load 15 pF, input transition time 2 ns, drive strength set to 6'b000111, and Slew Rate set to 2'b11.

4.3.1 RMII

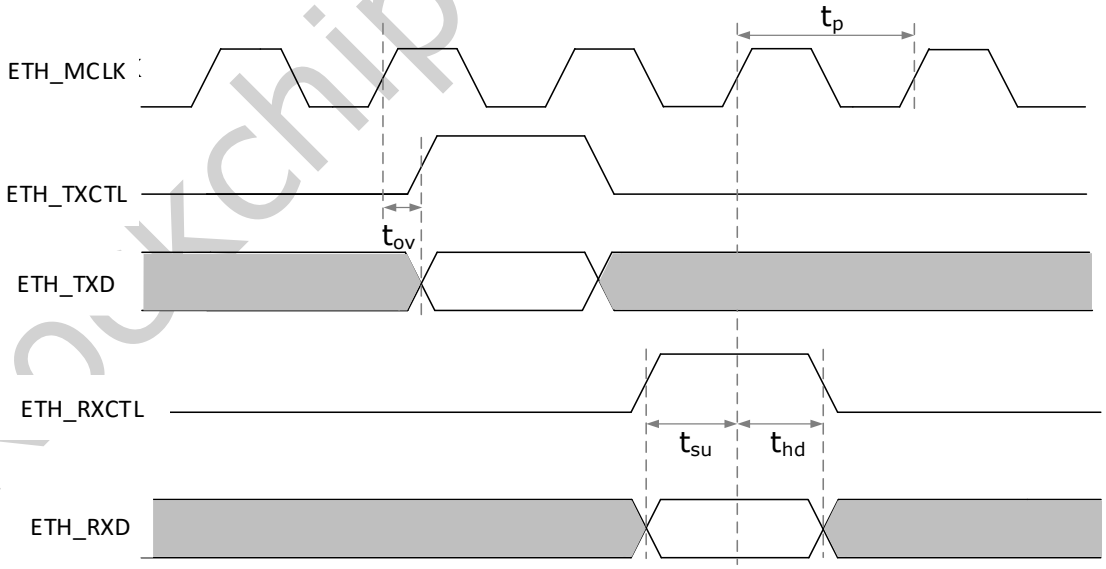

Fig. 4-6 RMII Interface Timing Diagram

Table 4-4 MAC Timing in RMII Mode and Internal Clock Mode

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
		1.8V			3.3V			

t_p	REF_CLK Period		20			20		ns
t_{su}	RXD Setup Time	3.6			3.5			ns
t_{hd}	RXD Hold Time	0.4			0			ns
t_{ov}	TXD Output Delay	3		7	3		7	ns

Table 4-5 MAC Timing in RMII Mode and External Clock Mode

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
		1.8V			3.3V			
t_p	REF_CLK Period		20			20		ns
t_{su}	RXD Setup Time	0			0			ns
t_{hd}	RXD Hold Time	0.6			0.6			ns
t_{ov}	TXD Output Delay	3		8.2	3		8.2	ns

4.3.2 MDIO

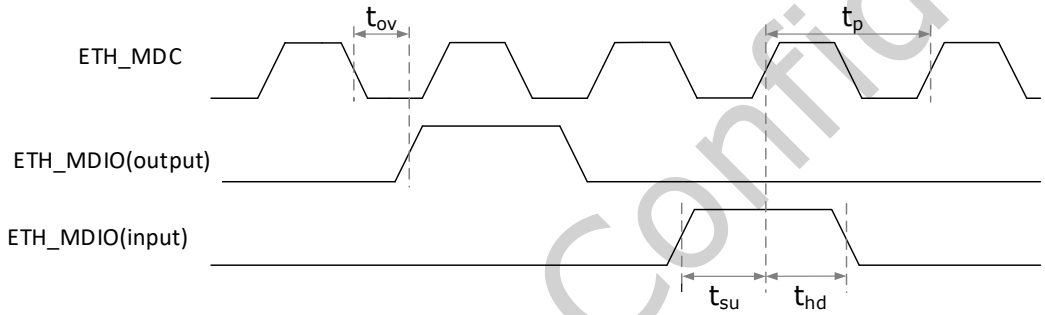

Fig. 4-7 MDIO Timing Diagram

Table 4-6 MAC MDIO Timing in 1.8V

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
		1.8V			3.3V			
t_{su}	MDIO Setup Time(Read)	13			13			ns
t_{hd}	MDIO Hold Time(Read)	0			0			ns
t_{ov}	MDIO Output Delay(Write)	-2		10	-2		10	ns
t_{su}	MDIO Setup Time(Read)	13			13			ns

4.4 SAI

The following table gives the SAI electrical characteristics.
Test conditions: maximum output load 15 pF, input transition time 2 ns, drive strength set to 6'b000111, and Slew Rate set to 2'b11.

4.4.1 Master Mode

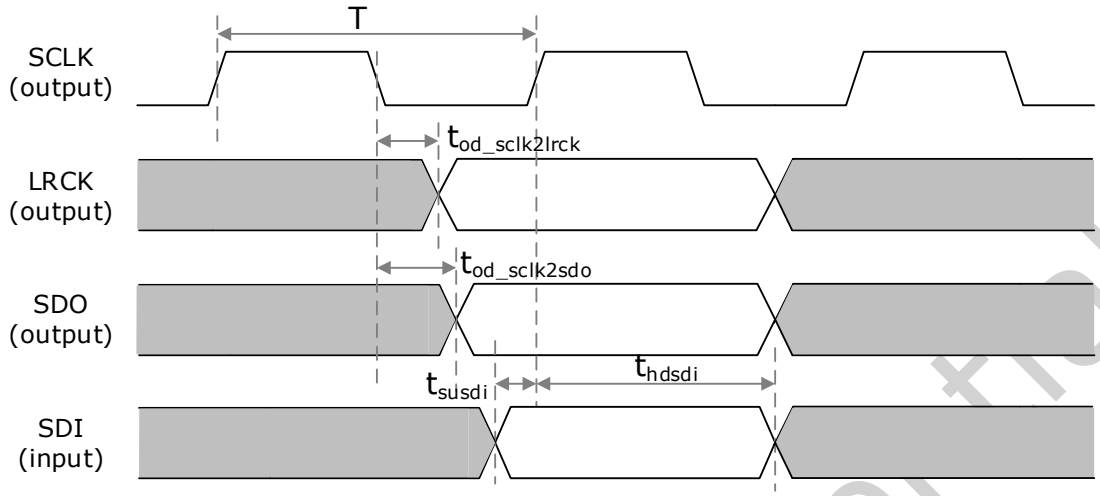

Fig. 4-8 SAI Master PAD Interface Timing Diagram

Table 4-7 SAI0 Master Timing

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
		1.8V			3.3V			
Fsclk	Frequency of SCLK	0.256		49.152	0.256		49.152	MHz
Fsclk	Duty cycle of SCLK	45%	50%	55%	45%	50%	55%	
LRCK	Duty cycle	45%	50%	55%	45%	50%	55%	
$t_{od\_sclk2lrck}$	LRCK delay time from SCLK falling edge	-2		2	-1.5		1.5	ns
$t_{od\_sclk2sdo}$	SDO propagation delay from SCLK falling edge	-2		2	-1.5		1.5	ns
t_{susdi}	SDI setup time to SCLK rising edge	11.5			11.3			ns
t_{hdsdi}	SDI hold time from SCLK rising edge	0			0			ns
t_{susdi_hs}*2	SDI setup time to SCLK rising edge for high speed	11.5-T/2			11.3-T/2			ns
t_{hdsdi_hs}*2	SDI hold time from SCLK rising edge for high speed mode	T/2-7.2			T/2-7			ns

Table 4-8 SAI1 Master Timing

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
		1.8V			3.3V			
Fsclk	Frequency of SCLK	0.256		49.152	0.256		49.152	MHz
Fsclk	Duty cycle of SCLK	45%	50%	55%	45%	50%	55%	
LRCK	Duty cycle	45%	50%	55%	45%	50%	55%	
$t_{od\_sclk2lrck}$	LRCK delay time from SCLK falling edge	-2		2	-1.5		1.5	ns
$t_{od\_sclk2sdo}$	SDO propagation delay from SCLK falling edge	-2		2	-1.5		1.5	ns
t_{susdi}	SDI setup time to SCLK rising edge	9.4			11.9			ns
t_{hdsdi}	SDI hold time from SCLK rising edge	0			0			ns
t_{susdi_hs}*2	SDI setup time to SCLK rising edge for high speed	9.4-T/2			11.9-T/2			ns
t_{hdsdi_hs}*2	SDI hold time from SCLK rising edge for high speed mode	T/2-7.8			T/2-7.6			ns

Table 4-9 SAI2 Master Timing

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
		1.8V			3.3V			
Fsclk	Frequency of SCLK	0.256		49.152	0.256		49.152	MHz
Fsclk	Duty cycle of SCLK	45%	50%	55%	45%	50%	55%	
LRCK	Duty cycle	45%	50%	55%	45%	50%	55%	
$t_{od\_sclk2lrck}$	LRCK delay time from SCLK falling edge	-2		2	-1.5		1.5	ns
$t_{od\_sclk2sdo}$	SDO propagation delay from SCLK falling edge	-2		2	-1.5		1.5	ns
t_{susdi}	SDI setup time to SCLK rising edge	12.1			11.9			ns
t_{hdsdi}	SDI hold time from SCLK rising edge	0			0			ns
t_{susdi_hs}*2	SDI setup time to SCLK rising edge for high speed	12.1-T/2			11.9-T/2			ns
t_{hdsdi_hs}*2	SDI hold time from SCLK rising edge for high speed mode	T/2-7.9			T/2-7.6			ns

Table 4-10 SAI3 Master Timing

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
		1.8V			3.3V			
Fsclk	Frequency of SCLK	0.256		49.152	0.256		49.152	MHz
Fsclk	Duty cycle of SCLK	45%	50%	55%	45%	50%	55%	
LRCK	Duty cycle	45%	50%	55%	45%	50%	55%	
$t_{od\_sclk2lrck}$	LRCK delay time from SCLK falling edge	-2		2	-1.5		1.5	ns
$t_{od\_sclk2sdo}$	SDO propagation delay from SCLK falling edge	-2		2	-1.5		1.5	ns
t_{susdi}	SDI setup time to SCLK rising edge	11.1			10.9			ns
t_{hdsdi}	SDI hold time from SCLK rising edge	0			0			ns
t_{susdi_hs}*2	SDI setup time to SCLK rising edge for high speed	11.1-T/2			10.9-T/2			ns
t_{hdsdi_hs}*2	SDI hold time from SCLK rising edge for high speed mode	T/2-6.9			T/2-6.7			ns

Table 4-11 SAI4 Master Timing

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
		1.8V			3.3V			
Fsclk	Frequency of SCLK	0.256		49.152	0.256		49.152	MHz
Fsclk	Duty cycle of SCLK	45%	50%	55%	45%	50%	55%	
LRCK	Duty cycle	45%	50%	55%	45%	50%	55%	
$t_{od\_sclk2lrck}$	LRCK delay time from SCLK falling edge	-2		2	-1.5		1.5	ns
$t_{od\_sclk2sdo}$	SDO propagation delay from SCLK falling edge	-2		2	-1.5		1.5	ns
t_{susdi}	SDI setup time to SCLK rising edge	11.8			11.6			ns
t_{hdsdi}	SDI hold time from SCLK rising edge	0			0			ns
t_{susdi_hs}*2	SDI setup time to SCLK rising edge for high speed	11.8-T/2			11.6-T/2			ns
t_{hdsdi_hs}*2	SDI hold time from SCLK rising edge for high speed mode	T/2-7.6			T/2-7.4			ns

Table 4-12 SAI5 Master Timing

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit

		1.8V			3.3V			
Fsclk	Frequency of SCLK	0.256		49.152	0.256		49.152	MHz
Fsclk	Duty cycle of SCLK	45%	50%	55%	45%	50%	55%	
LRCK	Duty cycle	45%	50%	55%	45%	50%	55%	
$t_{od\_sclk2lrck}$	LRCK delay time from SCLK falling edge	-2		2	-1.5		1.5	ns
$t_{od\_sclk2sdo}$	SDO propagation delay from SCLK falling edge	-2		2	-1.5		1.5	ns
t_{susdi}	SDI setup time to SCLK rising edge	11.9			11.7			ns
t_{hdsdi}	SDI hold time from SCLK rising edge	0			0			ns
t_{susdi_hs}*2	SDI setup time to SCLK rising edge for high speed	11.9-T/2			11.7-T/2			ns
t_{hdsdi_hs}*2	SDI hold time from SCLK rising edge for high speed mode	T/2-8			T/2-7.7			ns

Table 4-13 SAI6 Master Timing

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
		1.8V			3.3V			
Fsclk	Frequency of SCLK	0.256		49.152	0.256		49.152	MHz
Fsclk	Duty cycle of SCLK	45%	50%	55%	45%	50%	55%	
LRCK	Duty cycle	45%	50%	55%	45%	50%	55%	
$t_{od\_sclk2lrck}$	LRCK delay time from SCLK falling edge	-2		2	-1.5		1.5	ns
$t_{od\_sclk2sdo}$	SDO propagation delay from SCLK falling edge	-2		2	-1.5		1.5	ns
t_{susdi}	SDI setup time to SCLK rising edge	11.8			11.7			ns
t_{hdsdi}	SDI hold time from SCLK rising edge	0			0			ns
t_{susdi_hs}*2	SDI setup time to SCLK rising edge for high speed	11.8-T/2			11.7-T/2			ns
t_{hdsdi_hs}*2	SDI hold time from SCLK rising edge for high speed mode	T/2-7.9			T/2-7.4			ns

Table 4-14 SAI7 Master Timing

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
		1.8V			3.3V			
Fsclk	Frequency of SCLK	0.256		49.152	0.256		49.152	MHz
Fsclk	Duty cycle of SCLK	45%	50%	55%	45%	50%	55%	
LRCK	Duty cycle	45%	50%	55%	45%	50%	55%	
$t_{od\_sclk2lrck}$	LRCK delay time from SCLK falling edge	-2		2	-1.5		1.5	ns
$t_{od\_sclk2sdo}$	SDO propagation delay from SCLK falling edge	-2		2	-1.5		1.5	ns
t_{susdi}	SDI setup time to SCLK rising edge	11.5			11.3			ns
t_{hdsdi}	SDI hold time from SCLK rising edge	0			0			ns
t_{susdi_hs}*2	SDI setup time to SCLK rising edge for high speed	11.5-T/2			11.3-T/2			ns
t_{hdsdi_hs}*2	SDI hold time from SCLK rising edge for high speed mode	T/2-7.7			T/2-7.4			ns

Note：

1. The maximum frequency of the interface is 49.152 MHz. Whether the actual data transmission rate can reach this

level depends on t_{od_slave} *(output delay of the slave device) ,* t_{pd_clk} *(popagation delay of CLK) and* t_{pd_data}*(popagation delay of data). It should meet* $t_{susdi}+ t_{od\_slave+} t_{pd\_clk} + t_{pd\_data} <T/2$ in normal mode or $t_{susdi\_hs}+ t_{od\_slave+} t_{pd\_clk} + t_{pd\_data} <T/2$ in high speed mode.

2.The SAI supports configure the RX_TIMING_SHIFT register to change sampling edges in high speed mode. so the minimum setup time on the SoC side can subtract T/2 from $t_{susdi.}$ *The minimum hold time on the SoC side is the value that subtract an interval from T/2*

4.4.2 Slave Mode

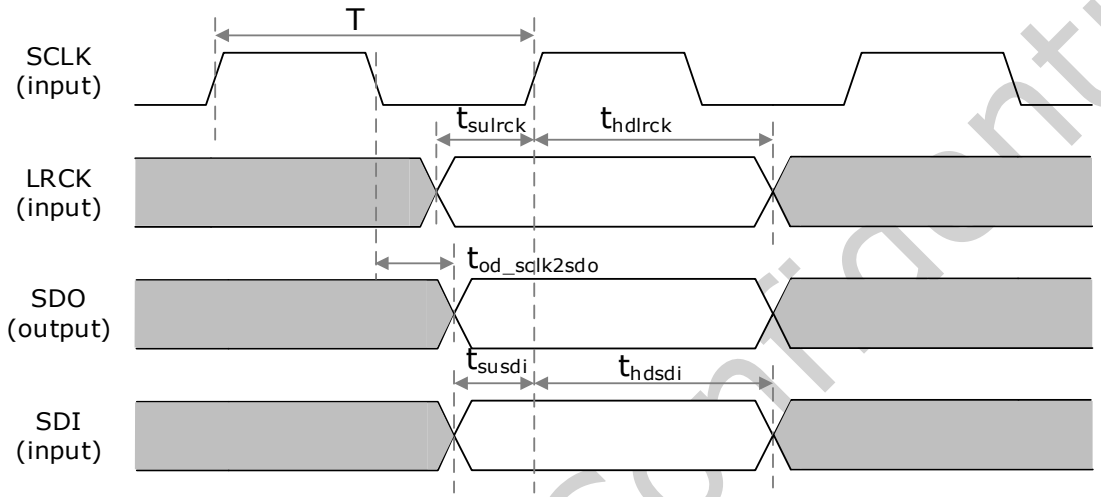

Fig. 4-9 SAI Slave PAD Interface Timing Diagram

Table 4-15 SAI0 Slave Timing

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
		1.8V			3.3V			
Fsclk	Frequency of SCLK	0.256		49.152	0.256		49.152	MHz
Fsclk	Duty cycle of SCLK	45%	50%	55%	45%	50%	55%	
LRCK	Duty cycle	45%	50%	55%	45%	50%	55%	
$t_{od\_sclk2lrck}$	LRCK delay time from SCLK falling edge	2.2			2.2			ns
$t_{od\_sclk2sdo}$	SDO propagation delay from SCLK falling edge	2.1			2.1			ns
$t_{od\_sclk2sdo}$	SDO propagation delay from SCLK falling edge	2.9		11.1	3.2		10.9	ns
t_{susdi}	SDI setup time to SCLK rising edge	2.2			2.2			ns
t_{hdsdi}	SDI hold time from SCLK rising edge	2			2			ns
$t_{od\_sclk2sdo\_hs}$*2	SDO propagation delay from SCLK falling edge for high speed mode	2.9-T/2		11.1-T/2	3.2-T/2		10.9-T/2	ns

Table 4-16 SAI1 Slave Timing

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
		1.8V			3.3V			
Fsclk	Frequency of SCLK	0.256		49.152	0.256		49.152	MHz

Fsclk	Duty cycle of SCLK	45%	50%	55%	45%	50%	55%	
LRCK	Duty cycle	45%	50%	55%	45%	50%	55%	
$t_{od\_sclk2lrck}$	LRCK delay time from SCLK falling edge	2.1			2.1			ns
$t_{od\_sclk2sdo}$	SDO propagation delay from SCLK falling edge	2.1			2.1			ns
$t_{od\_sclk2sdo}$	SDO propagation delay from SCLK falling edge	3.4		12	3.7		11.8	ns
t_{susdi}	SDI setup time to SCLK rising edge	2.2			2.2			ns
t_{hdsdi}	SDI hold time from SCLK rising edge	2.1			2.1			ns
$t_{od\_sclk2sdo\_hs}$*2	SDO propagation delay from SCLK falling edge for high speed mode	3.4-T/2		12-T/2	3.7-T/2		11.8-T/2	ns

Table 4-17 SAI2 Slave Timing

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
		1.8V			3.3V			
Fsclk	Frequency of SCLK	0.256		49.152	0.256		49.152	MHz
Fsclk	Duty cycle of SCLK	45%	50%	55%	45%	50%	55%	
LRCK	Duty cycle	45%	50%	55%	45%	50%	55%	
$t_{od\_sclk2lrck}$	LRCK delay time from SCLK falling edge	2.1			2.1		NA	ns
$t_{od\_sclk2sdo}$	SDO propagation delay from SCLK falling edge	2.2			2.2		NA	ns
$t_{od\_sclk2sdo}$	SDO propagation delay from SCLK falling edge	3.4		11.6	3		11.6	ns
t_{susdi}	SDI setup time to SCLK rising edge	2			2			ns
t_{hdsdi}	SDI hold time from SCLK rising edge	2.2			2.2			ns
$t_{od\ sclk2sdo\_hs}$*2	SDO propagation delay from SCLK falling edge for high speed mode	3.4-T/2		11.6-T/2	3-T/2		11.6-T/2	ns

Table 4-18 SAI3 Slave Timing

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
		1.8V			3.3V			
Fsclk	Frequency of SCLK	0.256		49.152	0.256		49.152	MHz
Fsclk	Duty cycle of SCLK	45%	50%	55%	45%	50%	55%	
LRCK	Duty cycle	45%	50%	55%	45%	50%	55%	
$t_{od\_sclk2lrck}$	LRCK delay time from SCLK falling edge	2.1			2.1			ns
$t_{od\_sclk2sdo}$	SDO propagation delay from SCLK falling edge	2.1			2.1			ns
$t_{od\_sclk2sdo}$	SDO propagation delay from SCLK falling edge	2.6		10.5	3		10.3	ns
t_{susdi}	SDI setup time to SCLK rising edge	2.4			2.4			ns
t_{hdsdi}	SDI hold time from SCLK rising edge	1.9			1.9			ns
$t_{od\ sclk2sdo\_hs}$*2	SDO propagation delay from SCLK falling edge for high speed mode	2.6-T/2		10.5-T/2	3-T/2		10.3-T/2	ns

Table 4-19 SAI4 Slave Timing

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
		1.8V			3.3V			
Fsclk	Frequency of SCLK	0.256		49.152	0.256		49.152	MHz
Fsclk	Duty cycle of SCLK	45%	50%	55%	45%	50%	55%	
LRCK	Duty cycle	45%	50%	55%	45%	50%	55%	
$t_{od\_sclk2lrck}$	LRCK delay time from SCLK falling edge	2			2			ns
$t_{od\_sclk2sdo}$	SDO propagation delay from SCLK falling edge	2.2			2.2			ns
$t_{od\_sclk2sdo}$	SDO propagation delay from SCLK falling edge	3.2		11.6	3.5		11.4	ns
t_{susdi}	SDI setup time to SCLK rising edge	2			2			ns
t_{hdsdi}	SDI hold time from SCLK rising edge	2.3			2.3			ns
$t_{od\ sclk2sdo\_hs}$*2	SDO propagation delay from SCLK falling edge for high speed mode	3.2-T/2		11.6-T/2	3.5-T/2		11.4-T/2	ns

Table 4-20 SAI5 Slave Timing

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
		1.8V			3.3V			
Fsclk	Frequency of SCLK	0.256		49.152	0.256		49.152	MHz
Fsclk	Duty cycle of SCLK	45%	50%	55%	45%	50%	55%	
LRCK	Duty cycle	45%	50%	55%	45%	50%	55%	
$t_{od\_sclk2lrck}$	LRCK delay time from SCLK falling edge	2.1			2.1			ns
$t_{od\_sclk2sdo}$	SDO propagation delay from SCLK falling edge	2.2			2.2			ns
$t_{od\_sclk2sdo}$	SDO propagation delay from SCLK falling edge	3.3		11.7	3.6		11.5	ns
t_{susdi}	SDI setup time to SCLK rising edge	2			2			ns
t_{hdsdi}	SDI hold time from SCLK rising edge	2.4			2.4			ns
$t_{od\ sclk2sdo\_hs}$*2	SDO propagation delay from SCLK falling edge for high speed mode	-T/2		-T/2	3.6-T/2		11.5-T/2	ns

Table 4-21 SAI6 Slave Timing

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
		1.8V			3.3V			
Fsclk	Frequency of SCLK	0.256		49.152	0.256		49.152	MHz
Fsclk	Duty cycle of SCLK	45%	50%	55%	45%	50%	55%	
LRCK	Duty cycle	45%	50%	55%	45%	50%	55%	
$t_{od\_sclk2lrck}$	LRCK delay time from SCLK falling edge	1.8			2.1			ns
$t_{od\_sclk2sdo}$	SDO propagation delay from SCLK falling edge	2.2			2.2			ns
$t_{od\_sclk2sdo}$	SDO propagation delay from SCLK falling edge	3.4		11.5	3.7		11.3	ns
t_{susdi}	SDI setup time to SCLK rising edge	2.3			2.3			ns
t_{hdsdi}	SDI hold time from SCLK rising edge	2.2			2.2			ns
t_{od}	SDO propagation delay from	3.4-		11.5-	3.7-		11.3-	ns

$t_{sclk2sdo\_hs}$*2	SCLK falling edge for high speed mode	T/2		T/2	T/2		T/2	

Table 4-22 SAI7 Slave Timing

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
		1.8V			3.3V			
Fsclk	Frequency of SCLK	0.256		49.152	0.256		49.152	MHz
Fsclk	Duty cycle of SCLK	45%	50%	55%	45%	50%	55%	
LRCK	Duty cycle	45%	50%	55%	45%	50%	55%	
$t_{od\_sclk2lrck}$	LRCK delay time from SCLK falling edge	2.2			2.2			ns
$t_{od\_sclk2sdo}$	SDO propagation delay from SCLK falling edge	2			2			ns
$t_{od\_sclk2sdo}$	SDO propagation delay from SCLK falling edge	3.1		11.2	3.4		11	ns
t_{susdi}	SDI setup time to SCLK rising edge	2			2.1			ns
t_{hdsdi}	SDI hold time from SCLK rising edge	2.2			2.2			ns
$t_{od\ sclk2sdo\_hs}$*2	SDO propagation delay from SCLK falling edge for high speed mode	3.1-T/2		11.2-T/2	3.4-T/2		11-T/2	ns

Note：

1. The maximum frequency of the interface is 49.152 MHz. Whether the actual data transmission rate can reach this level depends on $t_{od\_sclk2sdo\_hs}$ */* $t_{od\_sclk2sdo}$ *and the receiving capability of the master.*

2.The SAI supports configure the TX_TIMING_SHIFT register to change drive edges in high speed mode, so the maximum SDO propagation delay on *the SoC side can subtract T/2 from* $t_{od\_sclk2sdo}$.

4.5 PDM

The following table gives the PDM electrical characteristics.
Test conditions: maximum output load 15 pF, input transition time 2 ns, drive strength set to 6'b000111, and Slew Rate set to 2'b11.

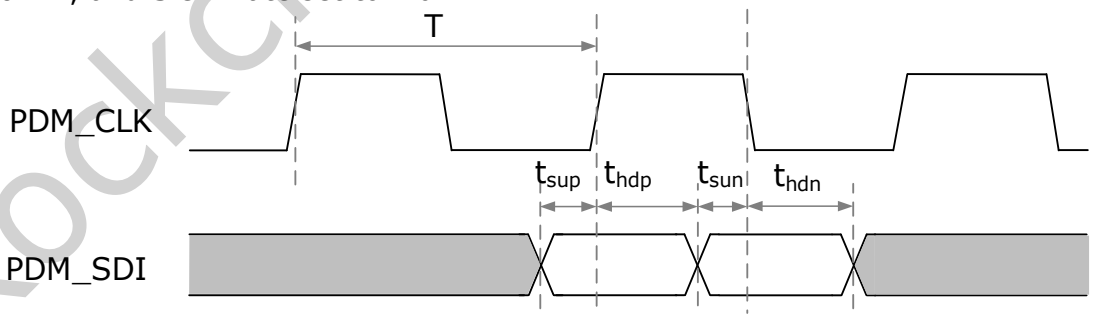

Fig. 4-10 PDM Timing Diagram

Table 4-23 PDM Timing

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
		1.8V			3.3V			
T	Frequency of PDM_CLK	1.024	4.096	6.144	1.024	4.096	6.144	MHz
T_{duty}	Duty cycle of PDM_CLK	45%	50%	55%	45%	50%	55%	N/A
t_{sup}	Input SDI setup time to PDM_CLK rising edge	11.2			11			ns

t_{hdp}	Input SDI hold time to PDM_CLK rising edge	0			0			ns
t_{sun}	Input SDI setup time to PDM_CLK falling edge	11.2			11			ns
t_{hdn}	Input SDI hold time to PDM_CLK falling edge	0			0			ns

4.6 SPI

The following table gives the SPI electrical characteristics.
Test conditions: maximum output load 15 pF, input transition time 2 ns, drive strength set to 6'b000111, and Slew Rate set to 2'b11.

4.6.1 SPI Master

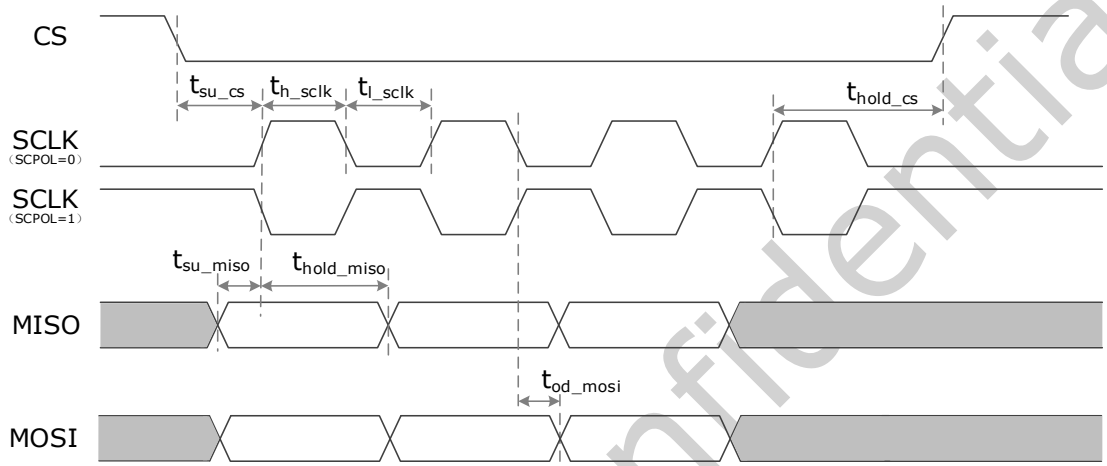

Fig. 4-11 SPI Master Mode Timing Diagram

Table 4-24 SPI1 Timing in Master Mode 1.8V

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
	1.8V			3.3V			
F_{sclk}			50			50	MHz
t_{h_sclk}	10			10			ns
t_{l_sclk}	10			10			ns
t_{hold_cs}	9			9			ns
t_{su_cs}	9			9			ns
t_{su_miso}	10.2-(rsd+1)*5			10-(rsd+1)*5			ns
t_{hold_miso}	(rsd+1)*5- 3.8			(rsd+1)*5- 4.4			ns
t_{od_mosi}	-2		2	-2		2	ns
1.rsd=0,1,2,3							

Table 4-25 SPI2 Timing in Master Mode 1.8V

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
	1.8V			3.3V			
F_{sclk}			50			50	MHz
t_{h_sclk}	10			10			ns
t_{l_sclk}	10			10			ns
t_{hold_cs}	9			9			ns
t_{su_cs}	9			9			ns
t_{su_miso}	11.5-(rsd+1)*5			11-(rsd+1)*5			ns
t_{hold_miso}	(rsd+1)*5- 5.8			(rsd+1)*5- 6.3			ns
t_{od_mosi}	-2		2	-2		2	ns
1.rsd=0,1,2,3							

4.6.2 SPI Slave

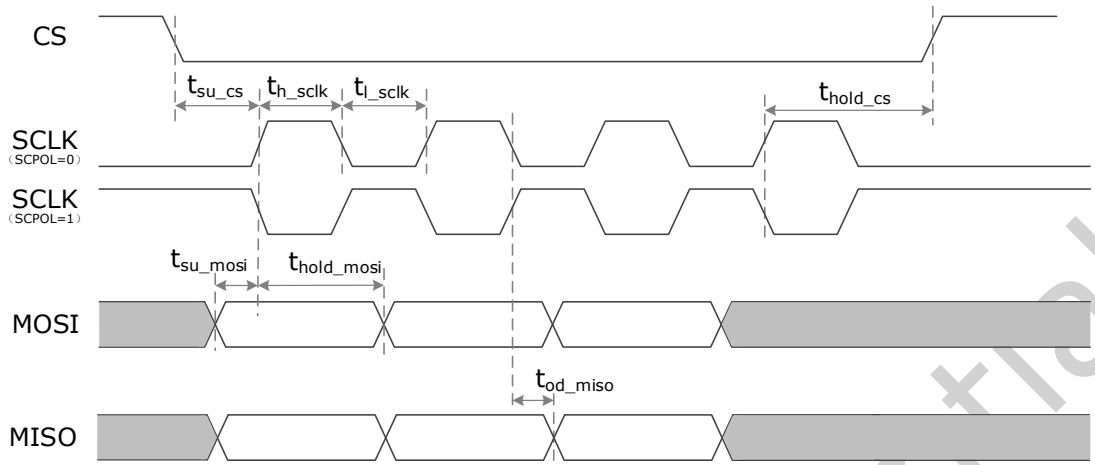

Fig. 4-12 SPI Slave Mode Timing Diagram

Table 4-26 SPI0 Timing in Slave Mode

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
	1.8V			3.3V			
F_{sclk}			50			50	MHz
t_{h_sclk}		10			10		ns
t_{l_sclk}		10			10		ns
t_{su_cs}	5			5			ns
t_{hold_cs}	25			25			ns
t_{su_mosi}	0.5			0.4			ns
t_{hold_mosi}	0.0			0.2			ns
t_{od_miso}	2.5		9.6	2.8		8.9	ns

Table 4-27 SPI1 Timing in Slave Mode

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
	1.8V			3.3V			
F_{sclk}			50			50	MHz
t_{h_sclk}		10			10		ns
t_{l_sclk}		10			10		ns
t_{su_cs}	5			5			ns
t_{hold_cs}	25			25			ns
t_{su_mosi}	1.5			1.5			ns

t_{hold_mosi}	0.9			0.9			ns
t_{od_miso}	3.0		10.5	3.2	NA	10.2	ns

Table 4-28 SPI2 Timing in Slave Mode

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
	1.8V			3.3V			
F_{sclk}			50			50	MHz
t_{h_sclk}		10			10		ns
t_{l_sclk}		10			10		ns
t_{su_cs}	5			5			ns
t_{hold_cs}	25			25			ns
t_{su_mosi}	2.2			2.2			ns
t_{hold_mosi}	1.8			2.1			ns
t_{od_miso}	2.5		12.6	2.8		11.9	ns

Table 4-29 SPI3 Timing in Slave Mode

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
	1.8V			3.3V			
F_{sclk}			50			50	MHz
t_{h_sclk}		10			10		ns
t_{l_sclk}		10			10		ns
t_{su_cs}	5			5			ns
t_{hold_cs}	25			25			ns
t_{su_mosi}	1.7			1.7			ns
t_{hold_mosi}	1.6			1.6			ns
t_{od_miso}	2.4		13.2	3.7		12.5	ns

4.6.3 SPI Through

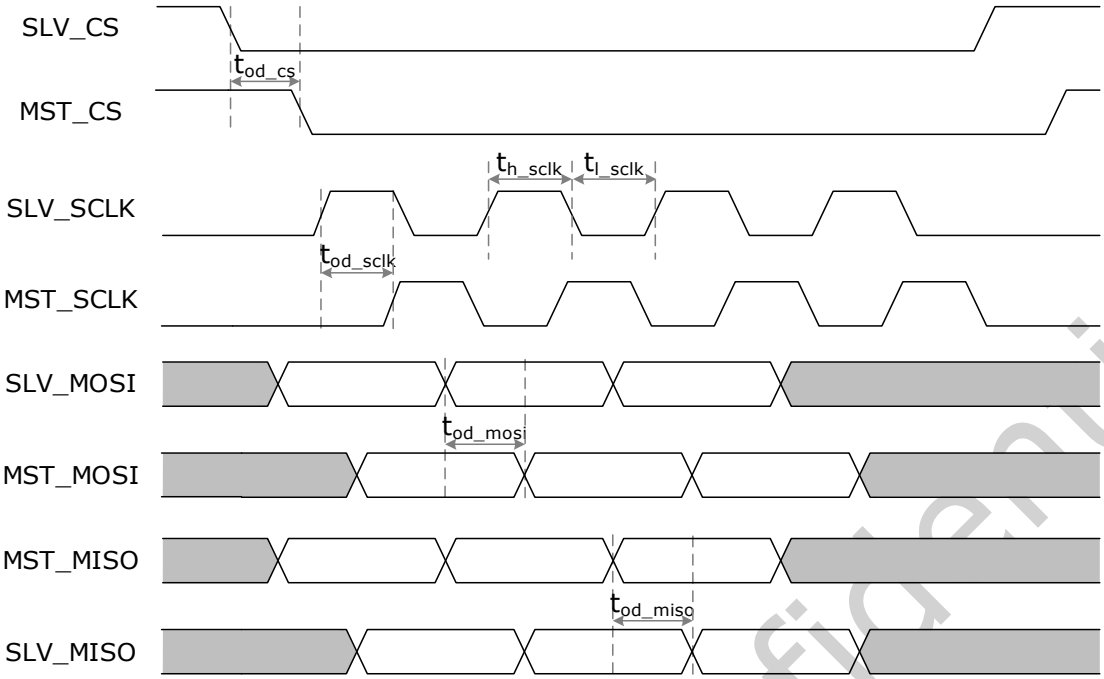

Fig. 4-13 SPI Through Mode Timing Diagram

Table 4-30 SPI0 Timing in Slave Mode

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
	1.8V			3.3V			
F_{sclk}			50			50	MHz
t_{h_sclk}		10			10		ns
t_{l_sclk}		10			10		ns
t_{od_cs}	3.0			3.0			ns
t_{od_sclk}	3.0		8.0	3.0		8.0	ns
t_{od_mosi}	3.0		10.0	3.0		10.0	ns
t_{od_miso}	3.0		10.0	3.0		10.0	ns

4.7 Flexbus

The following table gives the SPI electrical characteristics.
Test conditions: maximum output load 15 pF, input transition time 2 ns, drive strength set to 6'b000111, and Slew Rate set to 2'b11.

4.7.1 HS_Flexbus Master Mode

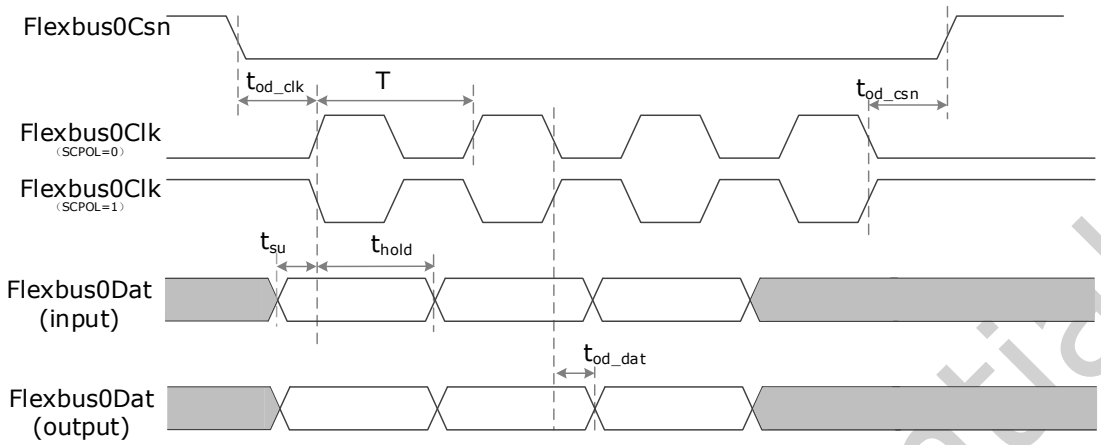

Fig. 4-14 HS_Flexbus Master Mode Timing Diagram

Table 4-31 HS_Flexbus Master Mode

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
		1.8V			3.3V			
F_{clk}	Flexbus clock Frequency		txclk/2	100		txclk/2	100	MHz
t_{od_clk}	Flexbus0Csn active to Flexbus0Clk valid	(1-scph)*tcycle-1.2		(1-scph)*tcycle+1.4	(1-scph)*tcycle -1.3		(1-scph)*tcycle+1.5	ns
t_{od_csn}	Flexbus0Clk stop to Flexbus0Csn inactive	scph*tcycle-1.4		scph*tcycle+1.2	scph*tcycle –1.5		(scph)*tcycle+1.3	ns
t_{su}	Data input setup time	7.6-tcycle			7.4-tcycle			ns
t_{hold}	Data input hold time	tcycle-1.6			tcycle–2			ns
t_{od_dat}	Data output delay	-1.1		0.8	-1.2		0.8	ns
1.scph=0 or 1								

4.7.2 LS_Flexbus

LS_Flexbus Master Mode

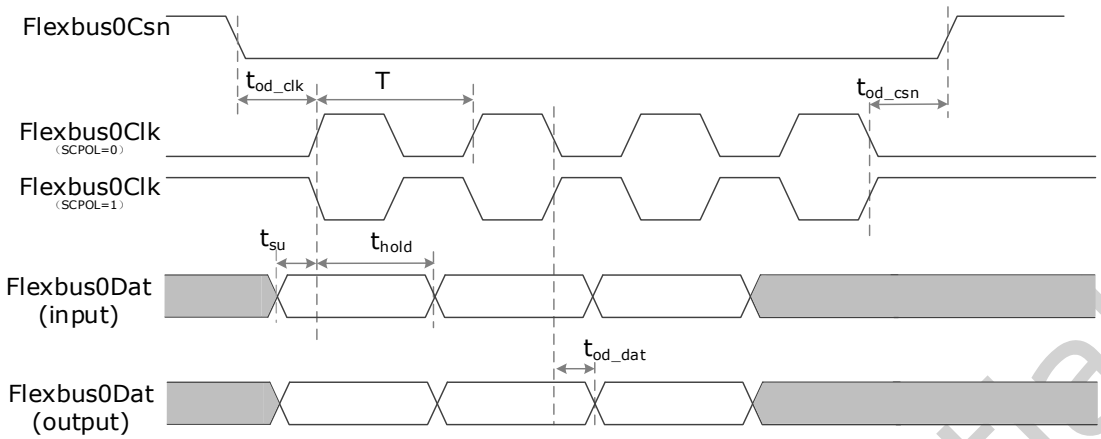

Fig. 4-15 LS_Flexbus Master Mode

Table 4-32 LS_Flexbus Master Mode

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
		1.8V			3.3V			
F_{clk}	Flexbus clock Frequency			34			34	MHz
D_{clk}	Flexbus0Csn active to Flexbus0Clk valid	t_{CK}*45%		t_{CK}*55%	t_{CK}*45%		t_{CK}*55%	ns
t_{od_clk}	Flexbus0Clk stop to Flexbus0Csn inactive	(3*(1-pol)+0.5)*tcycle - 1.6		(3*(1-pol)+0.5)*tcycle + 1.7	(3*(1-pol)+0.5)*tcycle - 1.7		(3*(1-pol)+0.5)*tcycle + 1.7	ns
t_{od_csn}	Data input setup time	(3*pol-0.5)*tcycle - 1.7		(3*pol-0.5)*tcycle + 1.6	(3*pol-0.5)*tcycle - 1.7		(3*pol-0.5)*tcycle + 1.6	ns
t_{su}	Data input hold time	0.5*tcycle + 9.3-ctl			0.5*tcycle+ 9.3-ctl			ns
t_{hold}	Data output delay	-0.5*tcycle - 1.4+ctl			-0.5*tcycle- 1.9+ctl			ns
t_{od_dat}	Data output delay	-1.1-0.5*tcycle		0	-1.2-0.5*tcycle		0	ns
1.pol=0 or 1 2.ctl=0.125*T*n (0<=n<4)								

4.7.3 LS_Flexbus Slave Mode

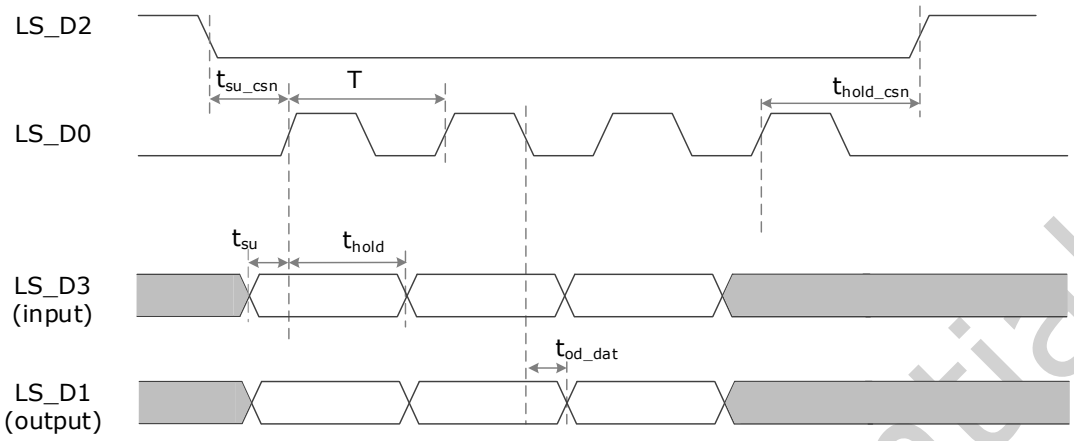

Fig. 4-16 LS_Flexbus Slave Mode

Table 4-33 LS_Flexbus Slave Mode

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
		1.8V			3.3V			
F_{clk}	SClk frequency		1/T	20		1/T	20	MHz
D_{clk}	SClk duty cycle	t_{CK}*45%		t_{CK}*55%	t_{CK}*45%		t_{CK}*55%	ns
t_{su_csn}	Csn active to SClk valid	0.5T			0.5T			ns
t_{hold_csn}	SClk stop to Csn inactive	T			T			ns
t_{su}	Data input setup time	0			0			ns
t_{hold}	Data input hold time	16.6			16.7			ns
t_{od_dat}	Data output delay	22.8			22.9			ns

4.8 I2C

Refer to the I2C protocol of 'UM10204-I2C-bus specification and user manual'

Chapter 5 Thermal Management

5.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature has to be below 125℃.

5.2 Package Thermal Characteristics

Table 4-1 provides the thermal resistance characteristics for the package used on the SoC. The resulting simulation data for reference only, please prevail in kind test.

Table 5-1 RK2116M2 Thermal Resistance Characteristics

Symbol	Description	Value	Unit	Note
θ_{JA}	Junction-to-ambient thermal resistance	19.7	(℃/W)	(1)
θ_{JB}	Junction-to-board thermal resistance	7.5	(℃/W)	(2)
θ_{JC}	Junction-to-case thermal resistance	16.7	(℃/W)	(3)
ψ_{JT}	Thermal characterization parameter	0.4	(℃/W)	(4)

Note (1): The package-board system is placed in the natural convection (JEDEC JESD51-2 standard), and the 2S2P test-board is designed in accordance with JESD 51-7/JESD 51-9. The actual system design and environment may be different. (The PCB is 4 layers, 114.5 mm*76.2 mm)
Note (2): θ_{JB} is measured in the special environment (JEDEC JESD51-8 standard), and the printed circuit board used to mount the devices is specified in JESD51-7.
Note (3): The thermal resistance θ_{JC} is provided in compliance with the JEDEC JESD51-14.
Note (4): ψ_{JT} - The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package, $\psi_{JT}$is measured in the test environment of θ_{JA} (JEDEC JESD51-2 standard).

