Rockchip RK2118G Datasheet

Revision 1.9
Mar. 2026

Revision History

Date	Revision	Description
2026-03-19	1.9	Correct the descriptions of SAI parameters, t_{sulrck} and t_{hdlrck} in Table 4-13
2026-02-11	1.8	Update NPU information in 1.2.3. Update block diagram. Update package dimension in Fig 2.6 to compatible with different package venders. Change FSPI SCLK and data timing diagram in Fig. 4-1. Update maximum FSPI clock frequency in Table 4-2 and delete information of parameter t_{fsu} and $t_{rhd.}$ Update maximum FSPI clock frequency in 3.3V in Table 4-3. Add related notes in Table 4-2, while deleting notes in Table 4-4. Update note(1) of thermal resistance characteristics in Table 5-1.
2026-01-05	1.7	Add timing parameters and related notes in Table 4-12 and Table 4-13. Correct maximum frequency of SCLK at 1.8V in Table 4-12 and maximum frequency of SCLK at both 1.8V and 3.3V in Table 4-13
2025-12-12	1.6	Update maximum frequency of SCLK of SAI Timing in Table 4-12 and Table 4-13
2025-11-21	1.5	Update Chapter 4 Update description in 1.2.11 Connectivity Update voltage data in Table 3-1 and Table 3-2 Update conjunction temperature in Table 3-1 Add parameter of clock frequency and input voltage in Table 3-7
2025-10-09	1.4	Update the description of CAN
2025-04-28	1.3	Update the electrical parameters in 3.1 and 3.2; Update the DDR frequency
2024-11-27	1.2	Add the part numbers RK2118G-Y and RK2118G-YX in Chapter 2; Add Chapter 4 Timing Specification to describe the timing specification of interfaces; Update the max. voltage values for DSP and logic core in 3.1 and 3.2
2024-05-31	1.1	Update some description and parameters
2024-04-28	1.0	Initial release

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Chapter 1 Introduction

1.1 Overview

RK2118G is a high-performance triple-core HiFi4 DSP processor designed for intelligent voice interaction, audio input/output processing and other digital multimedia applications. Embedded FIR/IIR accelerator and asynchronous sample rate converter hardware engine for minimizing DSP overhead to meet audio processing requirements. Also one NPU, specially designed for audio is integrated for potential audio AI processing.

RK2118G integrates dual-core STAR processor to run operating system, UI rendering and application protocol stack and so on. It is embedded with 1024KB system memory and eXecute In Place (XIP) Flash interface make RK2118G flexible for different application development. It is embedded with DDR2 capable of sustaining demanding memory bandwidths.

RK2118G integrates rich peripheral interfaces, such as VOP, SAI, PDM, SPDIF, USB2 OTG, RMII, CAN, and so on. It can meet different needs of application development, reduce hardware development complexity and development cost.

1.2 Features

1.2.1 Microprocessor

- Dual core Star-SE processor, ARM-V8M Architecture
- Support Thumb-2 technology
- Nested Vectored Interrupt Controller (NVIC) closely integrated with the processor
- Support single-precision Floating Point Unit
- Support Enhanced Memory Protection Unit
- Support TrustZone technology
- 16KB I-Cache and 16KB D-Cache
- Serial wire debug port (SW-DP) debug access

1.2.2 DSP

- Three core HiFi4 DSP processor (DSP0, DSP1, DSP2)
- Dual Load/Store, 4 VLIW Slots, 64-bit SIMD
- 4 MAC 32x32, 4 MAC 24x24, 8 MAC 32x16, 8 MAC 16x16 per cycle
- Two 2-Way SIMD VFPU
- 256KB ITCM, 768KB DTCM, 64KB I-Cache, 64KB D-Cache for DSP0
- 64KB ITCM, 256KB DTCM, 64KB I-Cache, 64KB D-Cache for DSP1/DSP2
- One isolated voltage domain for DSP0 DVFS

1.2.3 Neural Process Unit

- Support float point 16bit convolution operation
- 32 float point 16bit MAC operations per cycle
- Inference Engine: TensorFlow, Caffe, Tflite, Pytorch, Onnx NN, Android NN, etc.

1.2.4 FIR/IIR Accelerator

- Support simultaneous operation of FIR and IIR
- Support TCB chain structure
- Support legacy mode and max up to 32 TCB
- Support auto configuration mode (ACM), and keep working until TCB pointer is empty
- Support 4096 order FIR filter
- Support Transposed Direct Form II Biquads for IIR, and max 64 biquads cascade

1.2.5 Memory Organization

- Internal on-chip memory
  - BootROM
  - System SRAM
  - PMU SRAM
  - DDR2

- External off-chip memory①
  - SPI Nor/Nand Flash
  - eMMC
  - SD Card

1.2.6 Internal Memory

- Internal BootRom
  - Support system boot from the following device:
    - SPI Flash interface
    - eMMC interface
    - SDMMC interface
  - Support system code download by the following interface:
    - USB OTG interface (Device mode)
    - SPI interface (Slave mode)
    - UART interface

- Internal SRAM
  - 1024KB System SRAM
  - 16KB PMU SRAM

- Integrated 64MB DDR2, which supports up to 903 frequency.

1.2.7 External Memory or Storage device

- Serial Flash Interface
  - Support transfer data from/to SPI flash device
  - Support x1, x2, x4, x8 data bits mode
  - Support SDR, DDR mode
  - Support XIP (eXecute In Place)
  - Support up to 1 chip select

- eMMC Interface
  - Compatible with standard iNAND interface
  - Compatible with eMMC specification 4.51
  - Data bus width is 8bits

- SD/MMC Interface
  - Compatible with SD3.0, MMC ver4.51
  - Compatible with SDIO3.0 protocol
  - Data bus width is 4bits

1.2.8 System Component

- CRU (clock & reset unit)
  - One oscillator with external crystal input
  - One internal low frequency RC clock
  - One internal power on reset circuit
  - Support single-end 32.768KHz clock input/output from/to GPIO
  - Support PLL control and generate various clock frequency for chip
  - Support clock gating control for individual components
  - Support global soft-reset control for whole chip, also individual soft-reset for each

component

- PMU(power management unit)
  - Three separate digital voltage domains (DSP0_DVDD/CORE_DVDD/PMU_DVDD)
  - Multiple configurable work sleep modes to save power consumption by different frequency or automatic clock gating control or external power on/off control

- Timer
  - Twenty 64bits timers with interrupt-based operation
  - One 64bits timer for low power mode application
  - Support two operation modes: free-running and user-defined count
  - Support timer work state checkable

- PWM
  - 8-channels PWM with interrupt-based operation
  - Support capture mode
  - Provides reference mode and output various duty-cycle waveform
  - Support continuous mode or one-shot mode
  - Support one channel IR TX and one channel IR RX application
  - Support one clock frequency calculation engine and one clock free running counter
  - Support four channel waveform generation through lookup table

- Watchdog
  - Support five 32-bit watchdog counter
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - Generate a system reset
    - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
  - Programmable reset pulse length
  - Totally 16 defined ranges of main timeout period

- Mailbox
  - One Mailbox to service different core's communication
  - Support sixteen mailbox elements, each element includes one data word, one command word register and one flag bit that can represent one interrupt

- Spinlock
  - Support spinlock registers for software to realize resource management

- DMA
  - Support five embedded DMA controllers
  - Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory
  - Support TrustZone technology and programmable secure state for each DMA channel
  - Support 8 channels for each DMA controller

- Secure System
  - Cipher engine
    - Support SHA-1, SHA-256/224, MD5 with hardware padding
    - Support HMAC of SHA-1, SHA-256, MD5 with hardware padding
    - Support AES-128, AES-192, AES-256 encrypt & decrypt cipher
    - Support AES ECB/CBC/OFB/CFB/CTR/CTS/XTS/CCM/GCM/CBC-MAC/CMAC mode
    - Support up to 4096 bits PKA mathematical operations for RSA
  - Support two 256 bits RNG output

- Support secure boot
- Support secure debug
- Support secure OTP
- Support secure OS
- Support bus firewall

1.2.9 Video Output Processor

- Support RGB888/RGB565 source data format
- Support RGB888/RGB565/RGB666 display data format
- Support i8080 MCU serial interface
- Support max output resolution 480x480

1.2.10 Audio Interface

- SAI
  - Support eight SAI components
  - Support audio protocol: I2S, PCM, TDM
  - Support up to 128 slots available with configurable size
  - Support slot length 8 to 32 bits configurable
  - Support slot valid data length 8 to 32 bits configurable
  - SAI0/SAI4 support up to four lane transmitter and four lane parallel receiver
  - SAI1/2/3/5/6/7 support up to two lane transmitter and two lane receiver
  - Support combine different SAI component to meet more transmitter and receiver lane

- PDM
  - Support PDM master receive mode
  - Support 5 wire PDM interface with one is clock and 4 data line
  - Support up to 8 mono microphones
  - Support 16~24 bits sample resolution

- SPDIF
  - Support SPDIF TX x 1
  - Support SPDIF RX x 2
  - Support 16bits/20bits/24bits resolution
  - Support linear PCM mode (IEC-60958)
  - Support non-linear PCM transfer (IEC-61937)

- ASRC
  - Support eight ASRC components
  - Support fixed length conversion mode and real time conversion mode
  - Support asynchronous sample rate clock for real time conversion mode
  - ASRC0/ASRC4 support 8 channel sample rate converter
  - ASRC1/2/3/5/6/7 support 4 channel sample rate converter
  - Support combine different ASRC component to meet more channel sample rate converter

1.2.11 Connectivity

- RMII 10/100 Ethernet Controller
  - Support one Ethernet Controller
  - Supports 10/100-Mbps data transfer rates with the RMII interfaces
  - Supports both full-duplex and half-duplex operation
  - Support IEEE 1588-2002 (version 1) and IEEE 1588-2008 (version 2) Timestamp
  - Support Flexible Pulse-Per-Second (PPS) Output

- USB 2.0 OTG
  - Support one USB 2.0 OTG port

- Compatible with USB 2.0 specification
- Supports high-speed (480Mbps), full-speed (12Mbps) and low-speed (1.5Mbps) mode

- FLEXBUS interface
  - Support transfer data from internal memory to GPIO by DMA
  - Support transfer data from GPIO to internal memory by DMA
  - Support multiple operating modes
    - Multiplexing TX clock and RX clock, Multiplexing TX data and RX data
      - Support TX only mode, RX only mode, TX then RX mode
    - Multiplexing TX clock and RX clock, Separating TX data and RX data
      - Support TX only mode, RX only mode, TX and RX mode, TX then RX mode
    - Separating TX clock and RX clock, Separating TX data and RX data
      - Support TX only mode, RX only mode, TX and RX mode
  - Support clock free running mode and following data mode
  - Support TX data width 1, 2, 4, 8, 16 bit configurable
  - Support RX data width 1, 2, 4, 8, 16 bit configurable
  - Support continue transmission mode and fix length transmission mode
  - Support one chip selection function for multiplexing TX clock and RX clock mode
  - Support two chip selection function for separating TX clock and RX clock mode, one for TX direction, the other for RX direction
  - Support TX clock auto gating
  - Support DVP (RGB888, RGB565, YUV422) interface for camera sensor

- SPI interface
  - Support three SPI Controllers
  - SPI0 support serial-slave mode
  - SPI1/SPI2 support serial-master and serial-slave mode, software-configurable

- I2C interface
  - Support six I2C interface
  - Support 7bits and 10bits address mode
  - Software programmable clock frequency
  - Data on the I2C-bus can be transferred at rates of up to 100 Kbit/s in the Standard-mode, up to 400 Kbit/s in the Fast-mode or up to 1 Mbit/s in Fast-mode Plus

- UART Controller
  - Support four UART interface
  - Embedded two 64-byte FIFO for TX and RX operation respectively
  - Support 5bit, 6bit, 7bit, 8bit serial data transmit or receive
  - Standard asynchronous communication bits such as start, stop and parity
  - Support different input clock for UART operation to get up to 4Mbps baud rate
  - Support auto flow control mode

- CAN Controller
  - Support one CAN interface
  - Compatible with ISO 11898-1-2003 specification
  - Support transmit or receive standard frame
  - Support transmit or receive extended frame

- Touch Key Controller
  - Support muti-channel CapSense monitor
  - Support trigger interrupt waterline configurable
  - Support LPF and DC elimination

1.2.12 Others

- Multiple groups of GPIO
  - All of GPIOs can be used to generate interrupt
  - Support level trigger and edge trigger interrupt
  - Support configurable polarity of level trigger interrupt
  - Support configurable rising edge, falling edge and both edge trigger interrupt
  - Support configurable pull direction (pullup or pulldown)
  - Support configurable drive strength
  - Support configurable slew rate

- Temperature Sensor (TS-ADC)
  - Up to 50KS/s sampling rate
  - Support one temperature sensor
  - -40~125℃ temperature range and +/-5℃ temperature accuracy

- Successive Approximation ADC (SARADC)
  - 10-bit resolution
  - Up to 1MS/s sampling rate
  - 4 single-ended input channels
  - GPIO multiplexed

- OTP
  - Support 8K bits Size, 7K bit for secure application
  - Support Program/Read/Idle mode

- Package Type
  - QFP128L(body: 14mm x 14mm; lead pitch: 0.4mm)
    - Embedded with 64MB DDR2

1.3 Block Diagram

The following figure shows the basic block diagram.

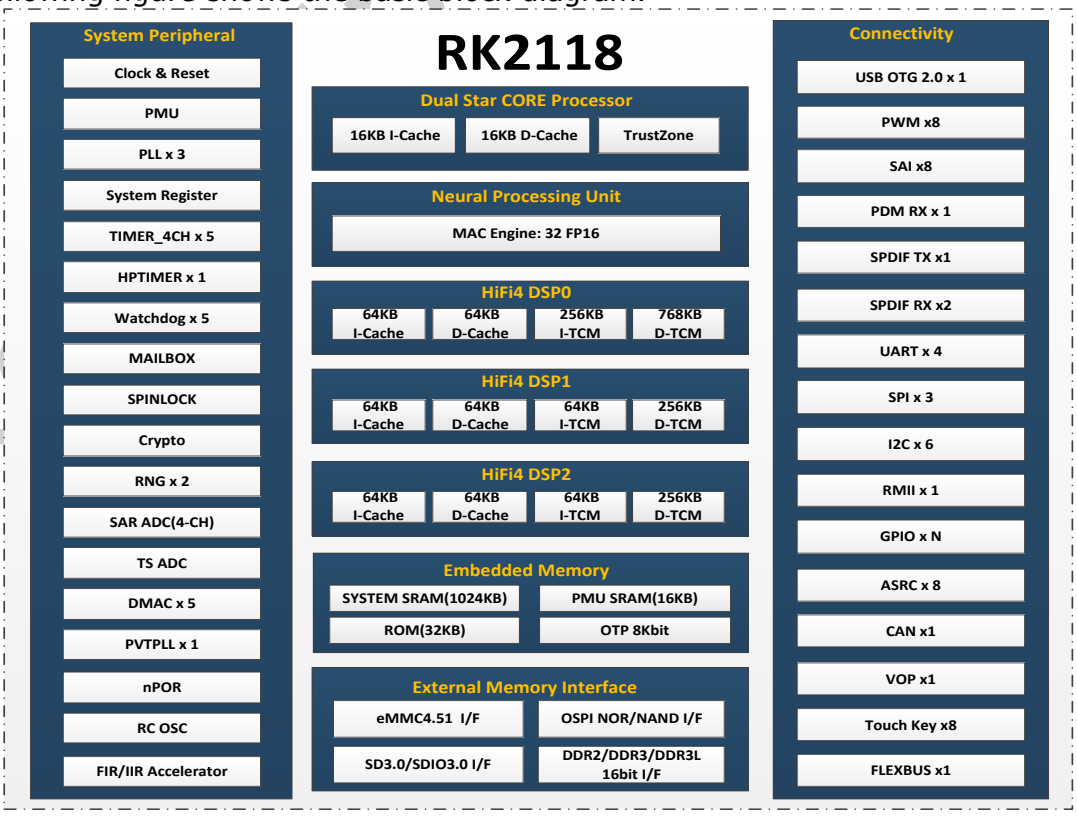


Fig.1-1 Block Diagram

Chapter 2 Package Information

2.1 Order Information

Orderable Device	RoHS status	Package	Package Qty	Device Feature
RK2118G	RoHS	QFP128L	900pcs	Smart audio processor
RK2118G-Y	RoHS	QFP128L	900pcs	Smart audio processor supporting Dolby Atmos
RK2118G-YX	RoHS	QFP128L	900pcs	Smart audio processor supporting Dolby Atmos and DTS-X

2.2 Top Marking

- RK2118G

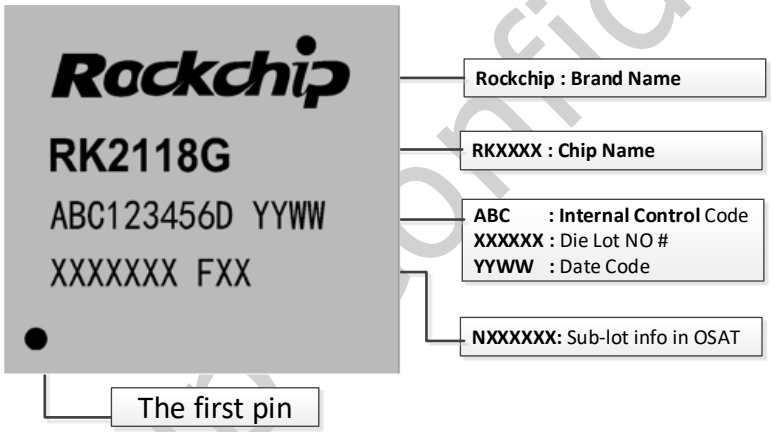


Fig.2-1 RK2118G Package Definition

- RK2118G-Y

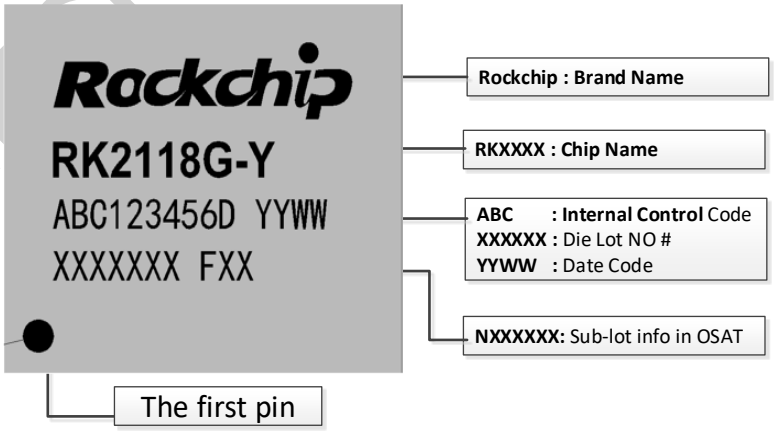


Fig.2-2 RK2118G-Y Package Definition

- RK2118G-YX

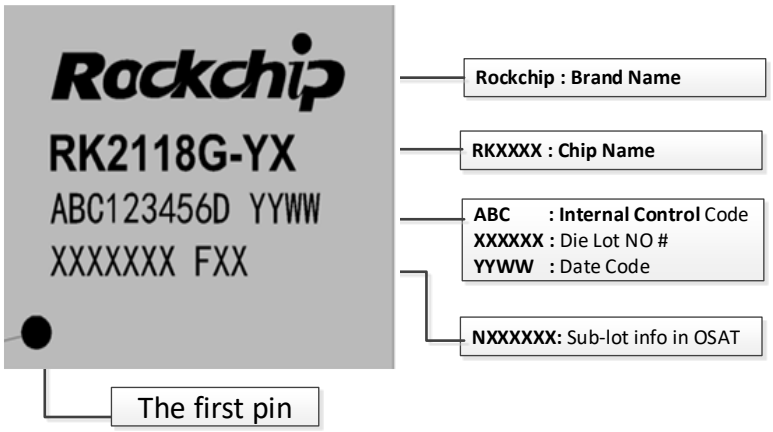


Fig.2-3 RK2118G-YX Package Definition

2.3 Package Dimension

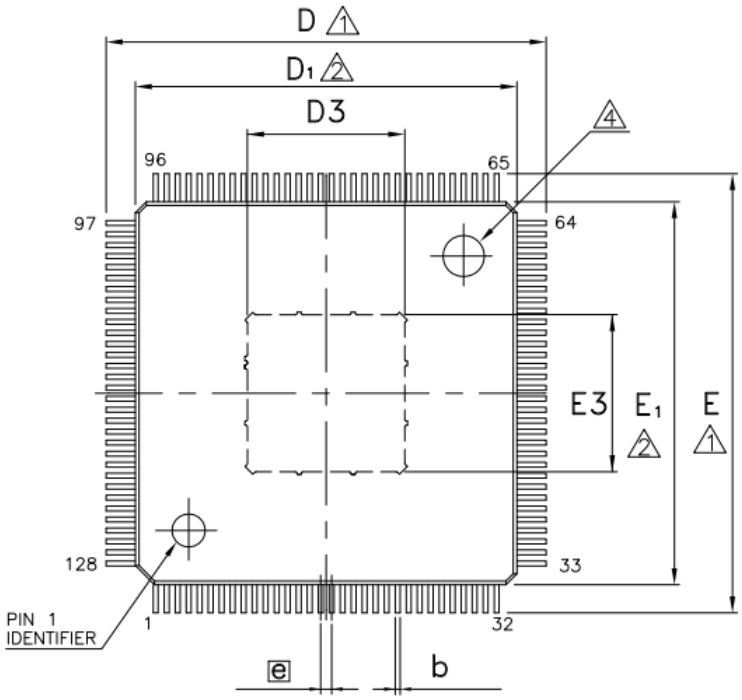
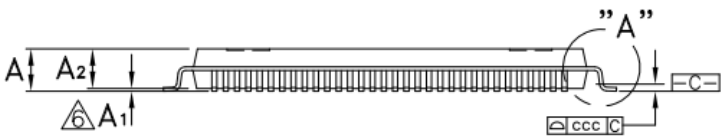


Fig.2-4 Package Top View



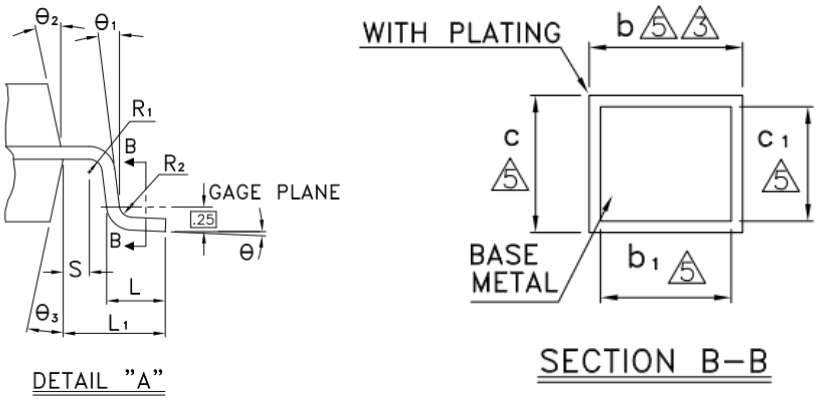


Fig.2-5 Package Side View

Symbol	Dimension in mm		
	Min	Nom	Max
A	——	——	1.60
A1	0.025	——	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
b1	0.13	0.16	0.19
c	0.09	0.14	0.20
c1	0.09	0.12	0.16
D	15.85	16.00	16.15
E	15.85	16.00	16.15
D1	13.90	14.00	14.10
E1	13.90	14.00	14.10
D3	8.00 REF		
E3	8.00 REF		
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 'REF		
θ	0°	3.5°	7°
θ1	0°	/	/
θ2	11°	12°	13°
θ3	11°	12°	13°
R1	0.08	——	——
R2	0.08	——	0.20
S	0.20	——	——
ccc	0.08		

Fig.2-6 Package Dimension

2.4 MSL Information

Moisture sensitivity Level: 3

2.5 Lead Finish/Ball Material Information

Lead Finish/Ball material: Sn

2.6 Pin Number List

Table 2-1 Pin Number Order Information

Pin	Pin Name	Pin	Pin Name
1	VSS	65	FLEXBUS1_D8/FLEXBUS0_CSN_M0/RM1_IO19/GPIO3_C3_D
2	DSP0_DVDD	66	FLEXBUS1_D7/RM1_IO20/GPIO3_C4_D
3	UART2_TX_RM/RM4_IO0/GPIO4_C0_D	67	FLEXBUS1_D6/RM1_IO21/GPIO3_C5_D
4	UART2_RX_RM/RM4_IO1/GPIO4_C1_D	68	SDMMC_D1/FLEXBUS1_D5/TEST_CLK_OUT/JTAG_MCU_SWO_M0/RM1_IO22/GPIO3_C6_D
5	UART2_CTSN_RM/RM4_IO2/GPIO4_C2_D	69	SDMMC_D0/FLEXBUS1_D4/RM1_IO23/GPIO3_C7_D
6	UART2_RTSN_RM/RM4_IO3/GPIO4_C3_D	70	SDMMC_CLK/FLEXBUS1_D3/RM1_IO24/GPIO3_D0_D
7	PWM1_CH0_RM/RM4_IO4/GPIO4_C4_D	71	SDMMC_CMD/FLEXBUS1_D2/RM1_IO25/GPIO3_D1_D
8	CORE_DVDD	72	SDMMC_D3/FLEXBUS1_D1/JTAG_MCU_TMS_M0/RM1_IO26/GPIO3_D2_D
9	VCCIO5_VCC	73	SDMMC_D2/FLEXBUS1_D0/JTAG_MCU_TCK_M0/RM1_IO27/GPIO3_D3_D
10	PWM1_CH1_RM/RM4_IO5/GPIO4_C5_D	74	VCCIO3_VCC
11	PWM1_CH2_RM/RM4_IO6/GPIO4_C6_D	75	CORE_DVDD
12	PWM1_CH3_RM/TOUCH_KEY_DRIVE_RM/RM4_IO7/GPIO4_C7_D	76	USB2_OTG_DM
13	UART3_TX_RM/TOUCH_KEY_IN0_RM/RM4_IO8/GPIO4_D0_D	77	USB2_OTG_DP
14	UART3_RX_RM/TOUCH_KEY_IN1_RM/RM4_IO9/GPIO4_D1_D	78	USB2_OTG_AVDD3V3
15	I2C3_SCL_RM/UART3_CTSN_RM/TOUCH_KEY_IN2_RM/RM4_IO10/GPIO4_D2_D	79	SARADC_IN0_BOOT/GPIO2_B1_Z
16	I2C3_SDA_RM/UART3_RTSN_RM/TOUCH_KEY_IN3_RM/RM4_IO11/GPIO4_D3_D	80	SARADC_IN1/GPIO2_B2_Z
17	I2C4_SCL_RM/TOUCH_KEY_IN4_RM/RM4_IO12/GPIO4_D4_D	81	SARADC_IN2/GPIO2_B3_Z
18	I2C4_SDA_RM/TOUCH_KEY_IN5_RM/RM4_IO13/GPIO4_D5_D	82	SARADC_IN3/GPIO2_B4_Z
19	CORE_DVDD	83	AVDD_1V8
20	NPOR	84	EMMC_D5/FSPI_D5/SPI0_CLK_M1/GPIO1_A0_U
21	PMU_DVDD0V9	85	EMMC_D3/FSPI_D7/SPI0_CSN_M1/GPIO1_A1_U
22	PMUIO_VCC3V3	86	EMMC_D4/FSPI_D6/SPI0_MOSI_M1/GPIO1_A2_U
23	TSADC_CTRL/RM0_IO0/GPIO0_A0_Z	87	EMMC_D0/FSPI_D4/SPI0_MISO_M1/GPIO1_A3_U
24	AUPLL_CLK_IN/RM0_IO1/GPIO0_A1_D	88	EMMC_D1/FSPI_D3/GPIO1_A4_U
25	ETH_CLK_25M_OUT/RM0_IO2/GPIO0_A2_D	89	FSPI_CLK/GPIO1_A5_D
26	REF_CLK1_OUT/DSP_AVS/RM0_IO3/GPIO0_A3_D	90	CORE_DVDD
27	CLK_32K/RM0_IO4/GPIO0_A4_D	91	VCCIO1_VCC
28	PWR_CTRL0/RM0_IO5/GPIO0_A5_D	92	EMMC_D2/FSPI_D0/GPIO1_A6_U
29	PWR_CTRL1/RM0_IO6/GPIO0_A6_U	93	EMMC_D7/FSPI_D2/GPIO1_A7_U
30	PWR_CTRL2/RM0_IO7/GPIO0_A7_U	94	EMMC_D6/FSPI_D1/GPIO1_B0_U
31	UART0_TX/JTAG_MCU_TCK_M1/RM0_IO9/GPIO0_B1_U	95	EMMC_CMD/FSPI_CSN/GPIO1_B1_U
32	UART0_RX/JTAG_MCU_TMS_M1/RM0_IO10/GPIO0_B2_U	96	FSPI_RSTN/GPIO1_B2_D
33	SYS_PLL_AVDD1V8	97	VCCIO1_VCC
34	OSC_XIN	98	EMMC_CLK/FSPI_DQS/GPIO1_B3_D

Pin	Pin Name	Pin	Pin Name
35	OSC_XOUT	99	ETH_RMII_CRSDV/SPI0_CLK_M0/RM2_IO0/GPIO2_A0_D
36	SYS_PLL_AVDD0V9	100	ETH_RMII_MDIO/SPI0_CSN_M0/RM2_IO1/GPIO2_A1_D
37	OSC_CLK_OUT/REF_CLK0_OUT/GPIO0_B3_D	101	ETH_RMII_MDC/SPI0_MOSI_M0/RM2_IO2/GPIO2_A2_D
38	DDR_VDDQ	102	ETH_RMII_TXEN/SPI0_MISO_M0/RM2_IO3/GPIO2_A3_D
39	VSS	103	CORE_DVDD
40	DDR_VDDQ	104	VCCIO2_VCC
41	VSS	105	ETH_RMII_TXD1/JTAG_DSP_TDO/RM2_IO4/GPIO2_A4_D
42	DDR_VDDQ	106	ETH_RMII_TXD0/JTAG_DSP_TCK/RM2_IO5/GPIO2_A5_D
43	FLEXBUS0_D0/VO_LCDC_CSN/RM1_IO0/GPIO3_A0_D	107	ETH_RMII_CLK/JTAG_DSP_TMS/RM2_IO6/GPIO2_A6_D
44	FLEXBUS0_D1/VO_LCDC_RS/RM1_IO1/GPIO3_A1_D	108	ETH_RMII_RXD1/JTAG_DSP_TDI/RM2_IO7/GPIO2_A7_D
45	FLEXBUS0_D2/VO_LCDC_WRN/RM1_IO2/GPIO3_A2_D	109	ETH_RMII_RXD0/JTAG_DSP_TRSTN/RM2_IO8/GPIO2_B0_D
46	FLEXBUS0_D3/VO_LCDC_D0/RM1_IO3/GPIO3_A3_D	110	CORE_DVDD
47	FLEXBUS0_D4/VO_LCDC_D1/RM1_IO4/GPIO3_A4_D	111	VO_LCDC_RDN_M1/RM3_IO0/GPIO4_A0_D
48	FLEXBUS0_D5/VO_LCDC_D2/RM1_IO5/GPIO3_A5_D	112	I2C0_SCL_RM/ETH_PPSCLK_RM/RM3_IO1/GPIO4_A1_D
49	FLEXBUS0_D6/VO_LCDC_D3/RM1_IO6/GPIO3_A6_D	113	I2C0_SDA_RM/ETH_PPSTRIG_RM/RM3_IO2/GPIO4_A2_D
50	FLEXBUS0_D7/VO_LCDC_D4/RM1_IO7/GPIO3_A7_D	114	I2C1_SCL_RM/RM3_IO3/GPIO4_A3_D
51	CORE_DVDD	115	VCCIO4_VCC
52	VCCIO3_VCC	116	I2C1_SDA_RM/RM3_IO4/GPIO4_A4_D
53	CORE_DVDD	117	I2C2_SCL_RM/RM3_IO5/GPIO4_A5_D
54	FLEXBUS0_D8/FLEXBUS1_CSN_M5/VO_LCDC_D5/RM1_IO8/GPIO3_B0_D	118	I2C2_SDA_RM/RM3_IO6/GPIO4_A6_D
55	FLEXBUS0_D9/FLEXBUS0_CSN_M5/VO_LCDC_D6/RM1_IO9/GPIO3_B1_D	119	PWM0_CH0_RM/RM3_IO7/GPIO4_A7_D
56	FLEXBUS0_CLK/FLEXBUS1_CSN_M4/VO_LCDC_D7/RM1_IO10/GPIO3_B2_D	120	PWM0_CH1_RM/RM3_IO8/GPIO4_B0_D
57	FLEXBUS1_CLK/FLEXBUS0_CSN_M4/VO_LCDC_RDN_M0/RM1_IO11/GPIO3_B3_D	121	PWM0_CH2_RM/RM3_IO9/GPIO4_B1_D
58	FLEXBUS0_D10/FLEXBUS1_D15/FLEXBUS1_CSN_M3/RM1_IO12/GPIO3_B4_D	122	UART1_TX_RM/RM3_IO11/GPIO4_B3_D
59	FLEXBUS0_D11/FLEXBUS1_D14/FLEXBUS0_CSN_M3/RM1_IO13/GPIO3_B5_D	123	UART1_RX_RM/RM3_IO12/GPIO4_B4_D
60	FLEXBUS0_D12/FLEXBUS1_D13/FLEXBUS1_CSN_M2/RM1_IO14/GPIO3_B6_D	124	UART1_CTSN_RM/RM3_IO13/GPIO4_B5_D
61	FLEXBUS0_D13/FLEXBUS1_D12/FLEXBUS0_CSN_M2/RM1_IO15/GPIO3_B7_D	125	RM3_IO15/GPIO4_B7_D
62	FLEXBUS0_D14/FLEXBUS1_D11/FLEXBUS1_CSN_M1/RM1_IO16/GPIO3_C0_D	126	TSADC_AVDD1V8
63	FLEXBUS0_D15/FLEXBUS1_D10/FLEXBUS0_CSN_M1/RM1_IO17/GPIO3_C1_D	127	VSS
64	FLEXBUS1_D9/FLEXBUS1_CSN_M0/RM1_IO18/GPIO3_C2_D	128	DSP0_DVDD
		EPAD	VSS

2.7 Power/Ground IO Description

Table 2-2 Power/Ground IO information

Group	Pin#	Description
VSS	1, 39, 41, 127, EPAD	Digital Ground

Group	Pin#	Description
CORE_DVDD	8, 19, 51, 53, 75, 90, 103, 110	Logic Power
DSP0_DVDD	2, 128	DSP0 Power
PMU_DVDD0V9	20	PMU Power
PMUIO_VCC3V3	22	PMU IO Power
VCCIO1_VCC	91, 97	VCCIO1 IO Power
VCCIO2_VCC	104	VCCIO2 IO Power
VCCIO3_VCC	52, 74	VCCIO3 IO Power
VCCIO4_VCC	115	VCCIO4 IO Power
VCCIO5_VCC	9	VCCIO5 IO Power
SYS_PLL_AVDD0V9	36	PLL Power
SYS_PLL_AVDD1V8	33	PLL Power
USB2_OTG_AVDD3V3	78	USB OTG2.0 Power
TSADC_AVDD1V8	126	TSADC Analog Power
AVDD_1V8	83	SarADC/OTP Analog Power USB OTG2.0 Power
DDR_VDDQ	38, 40, 42	DDR Power

2.8 Function IO Description

Table 2-3 Function IO description

Pin	Pin Name	Func0	Func1	Func2	Func3	Func4	Func5	Pad Type ①	Def ③	Pull	Drive Strength ②	INT	Power Domain
34	OSC_XIN	OSC_XIN						I	I	N/A	N/A		PLL
35	OSC_XOUT	OSC_XOUT						O	O	N/A	N/A		
37	OSC_CLK_OUT/REF_CLK0_OUT/GPIO0_B3_D	GPIO0_B3	OSC_CLK_OUT	REF_CLK0_OUT				IO	I	down	Level1	√	
20	NPOR	NPOR						I	I	N/A	N/A		PMUIO_VCC3V3
23	TSADC_CTRL/RM0_IO0/GPIO0_A0_Z	GPIO0_A0	TSADC_CTRL				RM0_IO0	IO	I	Z	Level2	√	
24	AUPLL_CLK_IN/RM0_IO1/GPIO0_A1_D	GPIO0_A1	AUPLL_CLK_IN				RM0_IO1	IO	I	down	Level2	√	
25	ETH_CLK_25M_OUT/RM0_IO2/GPIO0_A2_D	GPIO0_A2	ETH_CLK_25M_OUT				RM0_IO2	IO	I	down	Level2	√	
26	REF_CLK1_OUT/DSP_AVS/RM0_IO3/GPIO0_A3_D	GPIO0_A3	REF_CLK1_OUT	DSP_AVS			RM0_IO3	IO	I	down	Level2	√	
27	CLK_32K/RM0_IO4/GPIO0_A4_D	GPIO0_A4	CLK_32K				RM0_IO4	IO	I	down	Level2	√	
28	PWR_CTRL0/RM0_IO5/GPIO0_A5_D	GPIO0_A5	PWR_CTRL0				RM0_IO5	IO	I	down	Level2	√	
29	PWR_CTRL1/RM0_IO6/GPIO0_A6_U	GPIO0_A6	PWR_CTRL1				RM0_IO6	IO	I	up	Level2	√	
30	PWR_CTRL2/RM0_IO7/GPIO0_A7_U	GPIO0_A7	PWR_CTRL2				RM0_IO7	IO	I	up	Level2	√	
31	UART0_TX/JTAG_MCU_TCK_M1/RM0_IO9/GPIO0_B1_U	GPIO0_B1	UART0_TX	JTAG_MCU_TCK_M1			RM0_IO9	IO	I	up	Level2	√	
32	UART0_RX/JTAG_MCU_TMS_M1/RM0_IO10/GPIO0_B2_U	GPIO0_B2	UART0_RX	JTAG_MCU_TMS_M1			RM0_IO10	IO	I	up	Level2	√	
84	EMMC_D5/FSPI_D5/SPI0_CLK_M1/GPIO1_A0_U	GPIO1_A0	EMMC_D5	FSPI_D5	SPI0_CLK_M1			IO	I	up	Level2	√	VCCIO1_VCC
85	EMMC_D3/FSPI_D7/SPI0_CSN_M1/GPIO1_A1_U	GPIO1_A1	EMMC_D3	FSPI_D7	SPI0_CSN_M1			IO	I	up	Level2	√	
86	EMMC_D4/FSPI_D6/SPI0_MOSI_M1/GPIO1_A2_U	GPIO1_A2	EMMC_D4	FSPI_D6	SPI0_MOSI_M1			IO	I	up	Level2	√	
87	EMMC_D0/FSPI_D4/SPI0_MISO_M1/GPIO1_A3_U	GPIO1_A3	EMMC_D0	FSPI_D4	SPI0_MISO_M1			IO	I	up	Level2	√	
88	EMMC_D1/FSPI_D3/GPIO1_A4_U	GPIO1_A4	EMMC_D1	FSPI_D3				IO	I	up	Level2	√	
89	FSPI_CLK/GPIO1_A5_D	GPIO1_A5		FSPI_CLK				IO	I	down	Level3	√	
92	EMMC_D2/FSPI_D0/GPIO1_A6_U	GPIO1_A6	EMMC_D2	FSPI_D0				IO	I	up	Level2	√	
93	EMMC_D7/FSPI_D2/GPIO1_A7_U	GPIO1_A7	EMMC_D7	FSPI_D2				IO	I	up	Level2	√	
94	EMMC_D6/FSPI_D1/GPIO1_B0_U	GPIO1_B0	EMMC_D6	FSPI_D1				IO	I	up	Level2	√	
95	EMMC_CMD/FSPI_CSN/GPIO1_B1_U	GPIO1_B1	EMMC_CMD	FSPI_CSN				IO	I	up	Level2	√	
96	FSPI_RSTN/GPIO1_B2_D	GPIO1_B2		FSPI_RSTN				IO	I	down	Level2	√	
98	EMMC_CLK/FSPI_DQS/GPIO1_B3_D	GPIO1_B3	EMMC_CLK	FSPI_DQS				IO	I	down	Level3	√	
99	ETH_RMII_CRSDV/SPI0_CLK_M0/RM2_IO0/GPIO2_A0_D	GPIO2_A0	ETH_RMII_CRSDV	SPI0_CLK_M0			RM2_IO0	IO	I	down	Level2	√	VCCIO2_VCC

Pin	Pin Name	Func0	Func1	Func2	Func3	Func4	Func5	Pad Type ①	Def ③	Pull	Drive Strength ②	INT	Power Domain
100	ETH_RMII_MDIO/SPI0_CSN_M0/RM2_IO1/GPIO2_A1_D	GPIO2_A1	ETH_RMII_MDIO	SPI0_CSN_M0			RM2_IO1	IO	I	down	Level2	√	
101	ETH_RMII_MDC/SPI0_MOSI_M0/RM2_IO2/GPIO2_A2_D	GPIO2_A2	ETH_RMII_MDC	SPI0_MOSI_M0			RM2_IO2	IO	I	down	Level2	√	
102	ETH_RMII_TXEN/SPI0_MISO_M0/RM2_IO3/GPIO2_A3_D	GPIO2_A3	ETH_RMII_TXEN	SPI0_MISO_M0			RM2_IO3	IO	I	down	Level2	√	
105	ETH_RMII_TXD1/JTAG_DSP_TDO/RM2_IO4/GPIO2_A4_D	GPIO2_A4	ETH_RMII_TXD1	JTAG_DSP_TDO			RM2_IO4	IO	I	down	Level2	√	
106	ETH_RMII_TXD0/JTAG_DSP_TCK/RM2_IO5/GPIO2_A5_D	GPIO2_A5	ETH_RMII_TXD0	JTAG_DSP_TCK			RM2_IO5	IO	I	down	Level2	√	
107	ETH_RMII_CLK/JTAG_DSP_TMS/RM2_IO6/GPIO2_A6_D	GPIO2_A6	ETH_RMII_CLK	JTAG_DSP_TMS			RM2_IO6	IO	I	down	Level2	√	
108	ETH_RMII_RXD1/JTAG_DSP_TDI/RM2_IO7/GPIO2_A7_D	GPIO2_A7	ETH_RMII_RXD1	JTAG_DSP_TDI			RM2_IO7	IO	I	down	Level2	√	
109	ETH_RMII_RXD0/JTAG_DSP_TRSTN/RM2_IO8/GPIO2_B0_D	GPIO2_B0	ETH_RMII_RXD0	JTAG_DSP_TRSTN			RM2_IO8	IO	I	down	Level2	√	
43	FLEXBUS0_D0/VO_LCDC_CSN/RM1_IO0/GPIO3_A0_D	GPIO3_A0	FLEXBUS0_D0			VO_LCDC_CSN	RM1_IO0	IO	I	down	Level2	√	
44	FLEXBUS0_D1/VO_LCDC_RS/RM1_IO1/GPIO3_A1_D	GPIO3_A1	FLEXBUS0_D1			VO_LCDC_RS	RM1_IO1	IO	I	down	Level2	√	
45	FLEXBUS0_D2/VO_LCDC_WRN/RM1_IO2/GPIO3_A2_D	GPIO3_A2	FLEXBUS0_D2			VO_LCDC_WRN	RM1_IO2	IO	I	down	Level2	√	
46	FLEXBUS0_D3/VO_LCDC_D0/RM1_IO3/GPIO3_A3_D	GPIO3_A3	FLEXBUS0_D3			VO_LCDC_D0	RM1_IO3	IO	I	down	Level2	√	
47	FLEXBUS0_D4/VO_LCDC_D1/RM1_IO4/GPIO3_A4_D	GPIO3_A4	FLEXBUS0_D4			VO_LCDC_D1	RM1_IO4	IO	I	down	Level2	√	
48	FLEXBUS0_D5/VO_LCDC_D2/RM1_IO5/GPIO3_A5_D	GPIO3_A5	FLEXBUS0_D5			VO_LCDC_D2	RM1_IO5	IO	I	down	Level2	√	
49	FLEXBUS0_D6/VO_LCDC_D3/RM1_IO6/GPIO3_A6_D	GPIO3_A6	FLEXBUS0_D6			VO_LCDC_D3	RM1_IO6	IO	I	down	Level2	√	
50	FLEXBUS0_D7/VO_LCDC_D4/RM1_IO7/GPIO3_A7_D	GPIO3_A7	FLEXBUS0_D7			VO_LCDC_D4	RM1_IO7	IO	I	down	Level2	√	
54	FLEXBUS0_D8/FLEXBUS1_CSN_M5/VO_LCDC_D5/RM1_IO8/GPIO3_B0_D	GPIO3_B0	FLEXBUS0_D8		FLEXBUS1_CSN_M5	VO_LCDC_D5	RM1_IO8	IO	I	down	Level2	√	
55	FLEXBUS0_D9/FLEXBUS0_CSN_M5/VO_LCDC_D6/RM1_IO9/GPIO3_B1_D	GPIO3_B1	FLEXBUS0_D9		FLEXBUS0_CSN_M5	VO_LCDC_D6	RM1_IO9	IO	I	down	Level2	√	
56	FLEXBUS0_CLK/FLEXBUS1_CSN_M4/VO_LCDC_D7/RM1_IO10/GPIO3_B2_D	GPIO3_B2	FLEXBUS0_CLK		FLEXBUS1_CSN_M4	VO_LCDC_D7	RM1_IO10	IO	I	down	Level2	√	VCCIO3_VCC
57	FLEXBUS1_CLK/FLEXBUS0_CSN_M4/VO_LCDC_RDN_M0/RM1_IO11/GPIO3_B3_D	GPIO3_B3		FLEXBUS1_CLK	FLEXBUS0_CSN_M4	VO_LCDC_RDN_M0	RM1_IO11	IO	I	down	Level2	√	
58	FLEXBUS0_D10/FLEXBUS1_D15/FLEXBUS1_CSN_M3/RM1_IO12/GPIO3_B4_D	GPIO3_B4	FLEXBUS0_D10	FLEXBUS1_D15	FLEXBUS1_CSN_M3		RM1_IO12	IO	I	down	Level2	√	
59	FLEXBUS0_D11/FLEXBUS1_D14/FLEXBUS0_CSN_M3/RM1_IO13/GPIO3_B5_D	GPIO3_B5	FLEXBUS0_D11	FLEXBUS1_D14	FLEXBUS0_CSN_M3		RM1_IO13	IO	I	down	Level2	√	
60	FLEXBUS0_D12/FLEXBUS1_D13/FLEXBUS1_CSN_M2/RM1_IO14/GPIO3_B6_D	GPIO3_B6	FLEXBUS0_D12	FLEXBUS1_D13	FLEXBUS1_CSN_M2		RM1_IO14	IO	I	down	Level2	√	
61	FLEXBUS0_D13/FLEXBUS1_D12/FLEXBUS0_CSN_M2/RM1_IO15/GPIO3_B7_D	GPIO3_B7	FLEXBUS0_D13	FLEXBUS1_D12	FLEXBUS0_CSN_M2		RM1_IO15	IO	I	down	Level2	√	
62	FLEXBUS0_D14/FLEXBUS1_D11/FLEXBUS1_CSN_M1/RM1_IO16/GPIO3_C0_D	GPIO3_C0	FLEXBUS0_D14	FLEXBUS1_D11	FLEXBUS1_CSN_M1		RM1_IO16	IO	I	down	Level2	√	
63	FLEXBUS0_D15/FLEXBUS1_D10/FLEXBUS0_CSN_M1/RM1_IO17/GPIO3_C1_D	GPIO3_C1	FLEXBUS0_D15	FLEXBUS1_D10	FLEXBUS0_CSN_M1		RM1_IO17	IO	I	down	Level2	√	
64	FLEXBUS1_D9/FLEXBUS1_CSN_M0/RM1_IO18/GPIO3_C2_D	GPIO3_C2		FLEXBUS1_D9	FLEXBUS1_CSN_M0		RM1_IO18	IO	I	down	Level2	√	
65	FLEXBUS1_D8/FLEXBUS0_CSN_M0/RM1_IO19/GPIO3_C3_D	GPIO3_C3		FLEXBUS1_D8	FLEXBUS0_CSN_M0		RM1_IO19	IO	I	down	Level2	√	
66	FLEXBUS1_D7/RM1_IO20/GPIO3_C4_D	GPIO3_C4		FLEXBUS1_D7			RM1_IO20	IO	I	down	Level2	√	

Pin	Pin Name	Func0	Func1	Func2	Func3	Func4	Func5	Pad Type ①	Def ③	Pull	Drive Strength ②	INT	Power Domain
67	FLEXBUS1_D6/RM1_IO21/GPIO3_C5_D	GPIO3_C5		FLEXBUS1_D6			RM1_IO21	IO	I	down	Level2	√	
68	SDMMC_D1/FLEXBUS1_D5/TEST_CLK_OUT/JTAG_MCU_SWO_M0/RM1_IO22/GPIO3_C6_D	GPIO3_C6	SDMMC_D1	FLEXBUS1_D5	TEST_CLK_OUT	JTAG_MCU_SWO_M0	RM1_IO22	IO	I	down	Level2	√	
69	SDMMC_D0/FLEXBUS1_D4/RM1_IO23/GPIO3_C7_D	GPIO3_C7	SDMMC_D0	FLEXBUS1_D4			RM1_IO23	IO	I	down	Level2	√	
70	SDMMC_CLK/FLEXBUS1_D3/RM1_IO24/GPIO3_D0_D	GPIO3_D0	SDMMC_CLK	FLEXBUS1_D3			RM1_IO24	IO	I	down	Level3	√	
71	SDMMC_CMD/FLEXBUS1_D2/RM1_IO25/GPIO3_D1_D	GPIO3_D1	SDMMC_CMD	FLEXBUS1_D2			RM1_IO25	IO	I	down	Level2	√	
72	SDMMC_D3/FLEXBUS1_D1/JTAG_MCU_TMS_M0/RM1_IO26/GPIO3_D2_D	GPIO3_D2	SDMMC_D3	FLEXBUS1_D1		JTAG_MCU_TMS_M0	RM1_IO26	IO	I	down	Level2	√	
73	SDMMC_D2/FLEXBUS1_D0/JTAG_MCU_TCK_M0/RM1_IO27/GPIO3_D3_D	GPIO3_D3	SDMMC_D2	FLEXBUS1_D0		JTAG_MCU_TCK_M0	RM1_IO27	IO	I	down	Level2	√	
111	VO_LCDC_RDN_M1/RM3_IO0/GPIO4_A0_D	GPIO4_A0	VO_LCDC_RDN_M1				RM3_IO0	IO	I	down	Level2	√	VCCIO4_VCC
112	I2C0_SCL_RM/ETH_PPSCLK_RM/RM3_IO1/GPIO4_A1_D	GPIO4_A1	I2C0_SCL_RM	ETH_PPSCLK_RM			RM3_IO1	IO	I	down	Level2	√	
113	I2C0_SDA_RM/ETH_PPSTRIG_RM/RM3_IO2/GPIO4_A2_D	GPIO4_A2	I2C0_SDA_RM	ETH_PPSTRIG_RM			RM3_IO2	IO	I	down	Level2	√	
114	I2C1_SCL_RM/RM3_IO3/GPIO4_A3_D	GPIO4_A3	I2C1_SCL_RM				RM3_IO3	IO	I	down	Level2	√	
116	I2C1_SDA_RM/RM3_IO4/GPIO4_A4_D	GPIO4_A4	I2C1_SDA_RM				RM3_IO4	IO	I	down	Level2	√	
117	I2C2_SCL_RM/RM3_IO5/GPIO4_A5_D	GPIO4_A5	I2C2_SCL_RM				RM3_IO5	IO	I	down	Level2	√	
118	I2C2_SDA_RM/RM3_IO6/GPIO4_A6_D	GPIO4_A6	I2C2_SDA_RM				RM3_IO6	IO	I	down	Level2	√	
119	PWM0_CH0_RM/RM3_IO7/GPIO4_A7_D	GPIO4_A7	PWM0_CH0_RM				RM3_IO7	IO	I	down	Level2	√	
120	PWM0_CH1_RM/RM3_IO8/GPIO4_B0_D	GPIO4_B0	PWM0_CH1_RM				RM3_IO8	IO	I	down	Level2	√	
121	PWM0_CH2_RM/RM3_IO9/GPIO4_B1_D	GPIO4_B1	PWM0_CH2_RM				RM3_IO9	IO	I	down	Level2	√	
122	UART1_TX_RM/RM3_IO11/GPIO4_B3_D	GPIO4_B3	UART1_TX_RM				RM3_IO11	IO	I	down	Level2	√	
123	UART1_RX_RM/RM3_IO12/GPIO4_B4_D	GPIO4_B4	UART1_RX_RM				RM3_IO12	IO	I	down	Level2	√	
124	UART1_CTSN_RM/RM3_IO13/GPIO4_B5_D	GPIO4_B5	UART1_CTSN_RM				RM3_IO13	IO	I	down	Level2	√	
125	RM3_IO15/GPIO4_B7_D	GPIO4_B7					RM3_IO15	IO	I	down	Level2	√	
3	UART2_TX_RM/RM4_IO0/GPIO4_C0_D	GPIO4_C0	UART2_TX_RM				RM4_IO0	IO	I	down	Level2	√	VCCIO5_VCC
4	UART2_RX_RM/RM4_IO1/GPIO4_C1_D	GPIO4_C1	UART2_RX_RM				RM4_IO1	IO	I	down	Level2	√	
5	UART2_CTSN_RM/RM4_IO2/GPIO4_C2_D	GPIO4_C2	UART2_CTSN_RM				RM4_IO2	IO	I	down	Level2	√	
6	UART2_RTSN_RM/RM4_IO3/GPIO4_C3_D	GPIO4_C3	UART2_RTSN_RM				RM4_IO3	IO	I	down	Level2	√	
7	PWM1_CH0_RM/RM4_IO4/GPIO4_C4_D	GPIO4_C4	PWM1_CH0_RM				RM4_IO4	IO	I	down	Level2	√	
10	PWM1_CH1_RM/RM4_IO5/GPIO4_C5_D	GPIO4_C5	PWM1_CH1_RM				RM4_IO5	IO	I	down	Level2	√	
11	PWM1_CH2_RM/RM4_IO6/GPIO4_C6_D	GPIO4_C6	PWM1_CH2_RM				RM4_IO6	IO	I	down	Level2	√	
12	PWM1_CH3_RM/TOUCH_KEY_DRIVE_RM/RM4_IO7/GPIO4_C7_D	GPIO4_C7	PWM1_CH3_RM		TOUCH_KEY_DRIVE_RM		RM4_IO7	IO	I	down	Level2	√	

Pin	Pin Name	Func0	Func1	Func2	Func3	Func4	Func5	Pad Type ①	Def ③	Pull	Drive Strength ②	INT	Power Domain
13	UART3_TX_RM/TOUCH_KEY_IN0_RM/RM4_IO8/GPIO4_D0_D	GPIO4_D0	UART3_TX_RM		TOUCH_KEY_IN0_RM		RM4_IO8	IO	I	down	Level2	√	
14	UART3_RX_RM/TOUCH_KEY_IN1_RM/RM4_IO9/GPIO4_D1_D	GPIO4_D1	UART3_RX_RM		TOUCH_KEY_IN1_RM		RM4_IO9	IO	I	down	Level2	√	
15	I2C3_SCL_RM/UART3_CTSN_RM/TOUCH_KEY_IN2_RM/RM4_IO10/GPIO4_D2_D	GPIO4_D2	I2C3_SCL_RM	UART3_CTSN_RM	TOUCH_KEY_IN2_RM		RM4_IO10	IO	I	down	Level2	√	
16	I2C3_SDA_RM/UART3_RTSN_RM/TOUCH_KEY_IN3_RM/RM4_IO11/GPIO4_D3_D	GPIO4_D3	I2C3_SDA_RM	UART3_RTSN_RM	TOUCH_KEY_IN3_RM		RM4_IO11	IO	I	down	Level2	√	
17	I2C4_SCL_RM/TOUCH_KEY_IN4_RM/RM4_IO12/GPIO4_D4_D	GPIO4_D4	I2C4_SCL_RM		TOUCH_KEY_IN4_RM		RM4_IO12	IO	I	down	Level2	√	
18	I2C4_SDA_RM/TOUCH_KEY_IN5_RM/RM4_IO13/GPIO4_D5_D	GPIO4_D5	I2C4_SDA_RM		TOUCH_KEY_IN5_RM		RM4_IO13	IO	I	down	Level2	√	
79	SARADC_IN0_BOOT/GPIO2_B1_Z	GPIO2_B1	SARADC_IN0_BOOT					IO	I	z	Level1	√	AVDD_1V8
80	SARADC_IN1/GPIO2_B2_Z	GPIO2_B2	SARADC_IN1					IO	I	z	Level1	√	
81	SARADC_IN2/GPIO2_B3_Z	GPIO2_B3	SARADC_IN2					IO	I	z	Level1	√	
82	SARADC_IN3/GPIO2_B4_Z	GPIO2_B4	SARADC_IN3					IO	I	z	Level1	√	
76	USB2_OTG_DM	USB_DP						A					USB
77	USB2_OTG_DP	USB_DM						A					

Notes:
□: Pad types: I = input, O = output, I/O = input/output (bidirectional)
AP = Analog Power, AG = Analog Ground
DP = Digital Power, DG = Digital Ground
A = Analog
□: Output Drive Unit is mA, only Digital IO has drive value;
□: Reset state: I = input, O = output;

2.9 IO Pin Name Description

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 2-4 IO Function Description List

Interface	Pin Name	Direction	Description
Misc	OSC_XIN	I	Clock input of crystal XO
	OSC_XOUT	O	Clock output of crystal XO
	NPOR	I	Chip hardware reset input
	OSC_CLK_OUT	O	OSC Clock Output for external function module
	REF_CLK0_OUT	O	REF Clock Output for external function module
	REF_CLK1_OUT	O	REF Clock Output for external function module
	ETH_CLK_25M_OUT	O	REF Clock Output for external function module
	AUPLL_CLK_IN	I	REF Clock Input for internal PLL
	TEST_CLK_OUT	O	Chip internal clock output for measurement
	PWR_CTRL0	O	Chip low power mode output indication signal
	PWR_CTRL1	O	Chip low power mode output indication signal
	PWR_CTRL2	O	Chip low power mode output indication signal
	PWR_CTRL3	O	Chip low power mode output indication signal
	TSADC_CTRL	O	Chip high temperature output indication signal
	CLK_32K	I/O	32K clock If configured as input，clock is provided from external circuit； If configured as output，clock is provided from internal circuit of chip；

Interface	Pin Name	Direction	Description
SWJ-DP	JTAG_MCU_TCK_M*i* (*i*=0~1)	I	SWD interface clock input for MCU
	JTAG_MCU_TMS_M*i* (*i*=0~1)	I/O	SWD interface data input/output for MCU
	JTAG_MCU_SWO_M*i* (*i*=0~1)	O	Serial wire output for trace debug

Interface	Pin Name	Direction	Description
JTAG-DP	JTAG_DSP_TCK	I	JTAG interface for DSP
	JTAG_DSP_TMS	I	
	JTAG_DSP_TDI	I	
	JTAG_DSP_TDO	O	
	JTAG_DSP_TRSTN	I	

Interface	Pin Name	Direction	Description
SD/MMC/SDIO Host Controller	SDMMC_CLK	O	sdmmc card clock
	SDMMC_CMD	I/O	sdmmc card command output and response input
	SDMMC_D[*i*] (*i*=0~3)	I/O	sdmmc card data input and output

Interface	Pin Name	Direction	Description
eMMC Interface	EMMC_CLK	O	emmc card clock
	EMMC_CMD	I/O	emmc card command output and response input
	EMMC_D[*i*] (*i*=0~7)	I/O	emmc card data input and output

Interface	Pin Name	Direction	Description
FSPI Controller	FSPI_CLK	O	fspi serial clock
	FSPI_CSN	O	fspi chip select signal, low active
	FSPI_D*i(i=0~7)*	I/O	fspi serial data input/output signal
	FSPI_DQS	I/O	fspi dqs input/output signal
	FSPI_RSTN	O	fspi reset signal, low active

Interface	Pin Name	Direction	Description
MCU Display Interface	VO_LCDC_CSN	O	MCU interface CSN signal
	VO_LCDC_RS	O	MCU interface RS signal
	VO_LCDC_WRN	O	MCU interface WRN signal
	VO_LCDC_RDN_M*i* (*i*=0~1)	I	MCU interface RDN signal
	VO_LCDC_D*i*(*i*=0~7)	O	MCU interface data input/output

Interface	Pin Name	Direction	Description
SAI0/SAI4 Controller	SAI*i*_SCLK(*i*=0,4)	I/O	I2S/PCM/TDM serial clock
	SAI*i*_LRCK(*i*=0,4)	I/O	I2S/PCM/TDM channel indication signal
	SAI*i*_SDO0(*i*=0,4)	O	I2S/PCM/TDM serial data output
	SAI*i*_SDO1(*i*=0,4)	O	I2S/PCM/TDM serial data output
	SAI*i*_SDO2(*i*=0,4)	O	I2S/PCM/TDM serial data output
	SAI*i*_SDO3(*i*=0,4)	O	I2S/PCM/TDM serial data output
	SAI*i*_SDI0(*i*=0,4)	I	I2S/PCM/TDM serial data input
	SAI*i*_SDI1(*i*=0,4)	I	I2S/PCM/TDM serial data input
	SAI*i*_SDI2(*i*=0,4)	I	I2S/PCM/TDM serial data input
	SAI*i*_SDI3(*i*=0,4)	I	I2S/PCM/TDM serial data input

Interface	Pin Name	Direction	Description
SAI1~3	SAI*i*_SCLK(*i*=1,2,3,5,6,7)	I/O	I2S/PCM/TDM serial clock

Interface	Pin Name	Direction	Description
SAI5~7 Controller	SAI*i*_LRCK(*i*=1,2,3,5,6,7)	I/O	I2S/PCM/TDM channel indication signal
	SAI*i*_SDO0(*i*=1,2,3,5,6,7)	O	I2S/PCM/TDM serial data output
	SAI*i*_SDO1(*i*=1,2,3,5,6,7)	O	I2S/PCM/TDM serial data output
	SAI*i*_SDI0(*i*=1,2,3,5,6,7)	I	I2S/PCM/TDM serial data input
	SAI*i*_SDI1(*i*=1,2,3,5,6,7)	I	I2S/PCM/TDM serial data input

Interface	Pin Name	Direction	Description
PDM	PDM_CLK0	O	PDM sampling clock
	PDM_CLK1	O	PDM sampling clock
	PDM_SDI*i*(*i*=0~3)	I	PDM data

Interface	Pin Name	Direction	Description
SPI0	SPI0_CLK_M*i*(*i*=0~1)	I	SPI serial clock
	SPI0_CSN_M*i*(*i*=0~1)	I	SPI chip select signal, low active
	SPI0_MOSI_M*i*(*i*=0~1)	I	SPI serial data input
	SPI0_MISO_M*i*(*i*=0~1)	O	SPI serial data output

Interface	Pin Name	Direction	Description
SPI1/SPI2	SPI*i*_CLK(*i*=1~2)	I/O	SPI serial clock
	SPI*i*_CSN0(*i*=1~2)	I/O	SPI chip select signal, low active
	SPI*i*_CSN1(*i*=1~2)	O	SPI chip select signal, low active
	SPI*i*_MISO(*i*=1~2)	I/O	SPI serial data input/output
	SPI*i*_MOSI(*i*=1~2)	I/O	SPI serial data input/output

Interface	Pin Name	Direction	Description
PWM	PWM0_CH*i*_RM(*i*=0~3)	I/O	Pulse Width Modulation input and output
	PWM1_CH*i*_RM(*i*=0~3)	I/O	Pulse Width Modulation input and output

Interface	Pin Name	Direction	Description
I2C	I2C*i*_SDA_RM (*i*=0,1,2,3,4,5)	I/O	I2C data
	I2C*i*_SCL_RM (*i*=0,1,2,3,4,5)	I/O	I2C clock

Interface	Pin Name	Direction	Description
UART	UART0_RX	I	UART serial data input
	UART0_TX	O	UART serial data output
	UART*i*_RX_RM (*i*=1,2,3)	I	UART serial data input
	UART*i*_TX_RM (*i*=1,2,3)	O	UART serial data output
	UART*i*_CTSN_RM (*i*=1,2,3)	I	UART clear to send modem status input
	UART*i*_RTSN_RM (*i*=1,2,3)	O	UART modem control request to send output

Interface	Pin Name	Direction	Description
Touch Key	TOUCH_KEY_IN*i*_RM(*i*=0~7)	I	Touch Key data input
	TOUCH_KEY_DRIVE_RM	O	Touch Key drive clock output

Interface	Pin Name	Direction	Description
RMII	ETH_RMII_CLK	I/O	RMII REC_CLK output or external clock input
	ETH_RMII_MDC	O	RMII management interface clock
	ETH_RMII_MDIO	I/O	RMII management interface data
	ETH_RMII_TXD*i*(*i*=0~1)	O	RMII TX data
	ETH_RMII_RXD*i*(*i*=0~1)	I	RMII RX data
	ETH_RMII_TXEN	O	RMII TX data enable
	ETH_RMII_CRSDV	I	RMII RX indication signal

Interface	Pin Name	Direction	Description
FLEXBUS	FLEXBUS0_CLK	O	FLEXBUS0 clock output
	FLEXBUS0_D*i*(*i*=0~15)	I/O	FLEXBUS0 data input/output
	FLEXBUS1_CLK	I/O	FLEXBUS1 clock input/output DVP mode, acted as VICAP_CLK input
	FLEXBUS1_D*i*(*i*=0~15)	I	FLEXBUS0 data input DVP mode, FLEXBUS1_D6 and FLEXBUS1_D7 acted as VICAP_VSYNC and VICAP_HREF input signal separately. FLEXBUS1_D8~FLEXBUS1_D16 acted as VICAP_DATA0~VICAP_DATA7 input signal.
	FLEXBUS0_CSN_M*i*(*i*=0~5)	O	FLEXBUS0 chip selection output
	FLEXBUS1_CSN_M*i*(*i*=0~5)	O	FLEXBUS1 chip selection output

Interface	Pin Name	Direction	Description

Rockchip matrix IO	RM0_IO*i*(*i*=0~10)	I/O	IO matrix0
	RM1_IO*i*(*i*=0~27)	I/O	IO matrix1
	RM2_IO*i*(*i*=0~8)	I/O	IO matrix2
	RM3_IO*i*(*i*=0~15)	I/O	IO matrix3
	RM4_IO*i*(*i*=0~15)	I/O	IO matrix4

Interface	Pin Name	Direction	Description
USB 2.0	USB2_OTG_DP	I/O	USB 2.0 Data signal DP
	USB2_OTG_DM	I/O	USB 2.0 Data signal DM

2.10 Rockchip Matrix IO Function List

RK2118G support five Rockchip Matrix IO (RM_IO) which are designed to let numerous functional signals share limited pin interfaces. Within the same matrix, any function signal can be mapped to any pin interface by software configurable.

- RM0_IO support 20 function signals map to 11 pin interfaces (GPIO0_A0~GPIO0_B2)
- RM1_IO support 40 function signals map to 28 pin interfaces (GPIO3_A0~GPIO3_D3)
- RM2_IO support 16 function signals map to 9 pin interfaces (GPIO2_A0~GPIO2_B0)
- RM3_IO support 41 function signals map to 14 pin interfaces (GPIO4_A0~GPIO4_B7)
- RM4_IO support 36 function signals map to 14 pin interfaces (GPIO4_C0~GPIO4_D5)

Table 2-5 Rockchip Matrix IO Function List

Function Index	RM0_IO	RM1_IO	RM2_IO	RM3_IO	RM4_IO
1	I2C0_SCL	UART1_TX_RM1	UART1_TX_RM2	SPDIF_RX0	SPDIF_TX
2	I2C0_SDA	UART1_RX_RM1	UART1_RX_RM2	PDM_CLK0	SPDIF_RX1
3	I2C1_SCL	UART1_CTSN_RM1	UART1_CTSN_RM2	PDM_CLK1	MCLK4
4	I2C1_SDA	UART1_RTSN_RM1	UART1_RTSN_RM2	PDM_SDI0	MCLK5
5	PWM0_CH0	UART2_TX_RM1	UART2_TX_RM2	PDM_SDI1	MCLK6
6	PWM0_CH1	UART2_RX_RM1	UART2_RX_RM2	PDM_SDI2	MCLK7
7	PWM0_CH2	UART2_CTSN_RM1	UART2_CTSN_RM2	PDM_SDI3	SAI7_SCLK
8	PWM0_CH3	UART2_RTSN_RM1	UART2_RTSN_RM2	MCLK0	SAI7_LRCK
9	TOUCH_KEY_DRIVE_RM0	UART3_CTSN	I2C2_SCL_RM2	MCLK1	SAI7_SDI0
10	TOUCH_KEY_IN0_RM0	UART3_RX	I2C2_SDA_RM2	MCLK2	SAI7_SDI1
11	TOUCH_KEY_IN1_RM0	UART3_TX	I2C3_SCL_RM2	MCLK3	SAI7_SDO0
12	TOUCH_KEY_IN2_RM0	UART3_RTSN	I2C3_SDA_RM2	SAI3_SCLK	SAI7_SDO1
13	TOUCH_KEY_IN3_RM0	I2C2_SCL_RM1	I2C4_SCL_RM2	SAI3_LRCK	SAI6_SCLK
14	SPI1_CLK	I2C2_SDA_RM1	I2C4_SDA_RM2	SAI3_SDI0	SAI6_LRCK
15	SPI1_MOSI	I2C3_SCL_RM1	I2C5_SCL_RM2	SAI3_SDI1	SAI6_SDI0
16	SPI1_MISO	I2C3_SDA_RM1	I2C5_SDA_RM2	SAI3_SDO0	SAI6_SDI1
17	SPI1_CSN0	I2C4_SCL_RM1		SAI3_SDO1	SAI6_SDO0
18	SPI1_CSN1	I2C4_SDA_RM1		SAI2_SCLK	SAI6_SDO1

Function Index	RM0_IO	RM1_IO	RM2_IO	RM3_IO	RM4_IO
19	ETH_PPSCLK	I2C5_SCL_RM1		SAI2_LRCK	SAI5_SCLK
20	ETH_PPSTRIG	I2C5_SDA_RM1		SAI2_SDI0	SAI5_LRCK
21		CAN_TX		SAI2_SDI1	SAI5_SDI0
22		CAN_RX		SAI2_SDO0	SAI5_SDI1
23		PWM1_CH0		SAI2_SDO1	SAI5_SDO0
24		PWM1_CH1		SAI1_SCLK	SAI5_SDO1
25		PWM1_CH2		SAI1_LRCK	SAI4_SCLK
26		PWM1_CH3		SAI1_SDI0	SAI4_LRCK
27		TOUCH_KEY_DRIVE_RM1		SAI1_SDI1	SAI4_SDI0
28		TOUCH_KEY_IN0_RM1		SAI1_SDO0	SAI4_SDI1
29		TOUCH_KEY_IN1_RM1		SAI1_SDO1	SAI4_SDI2
30		TOUCH_KEY_IN2_RM1		SAI0_SCLK	SAI4_SDI3
31		TOUCH_KEY_IN3_RM1		SAI0_LRCK	SAI4_SDO0
32		TOUCH_KEY_IN4_RM1		SAI0_SDI0	SAI4_SDO1
33		TOUCH_KEY_IN5_RM1		SAI0_SDI1	SAI4_SDO2
34		TOUCH_KEY_IN6_RM1		SAI0_SDI2	SAI4_SDO3
35		TOUCH_KEY_IN7_RM1		SAI0_SDI3	SAI4_LRCKXN_0
36		SPI2_CLK		SAI0_SDO0	SAI4_LRCKXN_1
37		SPI2_MOSI		SAI0_SDO1	
38		SPI2_MISO		SAI0_SDO2	
39		SPI2_CSN0		SAI0_SDO3	
40		SPI2_CSN1		SAI0_LRCKXN_0	
41				SAI0_LRCKXN_1	

2.11 FLEXBUS Interface Typical Application Example

RK2118G FLEXBUS can be adapted to certain timing interface through software programming. In this section, we will list the pin mapping relationship for some typical application interfaces, such as ADC, DAC, DVP, QSPI LCD panel.

Table 2-6 Pin Mapping between FLEXBUS and ADC

FLEXBUS Interface	Direction	ADC Application Interface
FLEXBUS1_D0	Input	ADC_D0
FLEXBUS1_D1	Input	ADC_D1
FLEXBUS1_D2	Input	ADC_D2
FLEXBUS1_D3	Input	ADC_D3
FLEXBUS1_D4	Input	ADC_D4
FLEXBUS1_D5	Input	ADC_D5

FLEXBUS1_D6	Input	ADC_D6
FLEXBUS1_D7	Input	ADC_D7
FLEXBUS1_D8	Input	ADC_D8
FLEXBUS1_D9	Input	ADC_D9
FLEXBUS1_D10	Input	ADC_D10
FLEXBUS1_D11	Input	ADC_D11
FLEXBUS1_D12	Input	ADC_D12
FLEXBUS1_D13	Input	ADC_D13
FLEXBUS1_D14	Input	ADC_D14
FLEXBUS1_D15	Input	ADC_D15
FLEXBUS1_CLK	Input Output	ADC_CLK_IN(from ADC) ADC_CLK_OUT(To ADC)

Table 2-7 Pin Mapping between FLEXBUS and DAC

FLEXBUS Interface	Direction	DAC Application Interface
FLEXBUS0_D0	Output	DAC_D0
FLEXBUS0_D1	Output	DAC_D1
FLEXBUS0_D2	Output	DAC_D2
FLEXBUS0_D3	Output	DAC_D3
FLEXBUS0_D4	Output	DAC_D4
FLEXBUS0_D5	Output	DAC_D5
FLEXBUS0_D6	Output	DAC_D6
FLEXBUS0_D7	Output	DAC_D7
FLEXBUS0_D8	Output	DAC_D8
FLEXBUS0_D9	Output	DAC_D9
FLEXBUS0_D10	Output	DAC_D10
FLEXBUS0_D11	Output	DAC_D11
FLEXBUS0_D12	Output	DAC_D12
FLEXBUS0_D13	Output	DAC_D13
FLEXBUS0_D14	Output	DAC_D14
FLEXBUS0_D15	Output	DAC_D15
FLEXBUS0_CLK	Output	DAC_CLK
FLEXBUS0_CSN	Output	DAC_CS

Table 2-8 Pin Mapping between FLEXBUS and DVP Camera

FLEXBUS Interface	Direction	DVP Application Interface
FLEXBUS1_D6	Input	VI_CIF_VSYNC
FLEXBUS1_D7	Input	VI_CIF_HREF
FLEXBUS1_D8	Input	VI_CIF_D0

FLEXBUS1_D9	Input	VI_CIF_D1
FLEXBUS1_D10	Input	VI_CIF_D2
FLEXBUS1_D11	Input	VI_CIF_D3
FLEXBUS1_D12	Input	VI_CIF_D4
FLEXBUS1_D13	Input	VI_CIF_D5
FLEXBUS1_D14	Input	VI_CIF_D6
FLEXBUS1_D15	Input	VI_CIF_D7
FLEXBUS1_CLK	Input	VI_CIF_CLK

Table 2-9 Pin Mapping between FLEXBUS and QSPI LCD Panel

FLEXBUS Interface	Direction	QSPI LCD Application Interface
FLEXBUS0_D0	Inout	QSPI_D0
FLEXBUS0_D1	Inout	QSPI_D1
FLEXBUS0_D2	Inout	QSPI_D2
FLEXBUS0_D3	Inout	QSPI_D3
FLEXBUS0_CLK	Output	QSPI_CLK
FLEXBUS0_CS	Output	QSPI_CS

Chapter 3 Electrical Specification

3.1 Absolute Ratings

The below table provides the absolute ratings.
Absolute maximum or minimum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

Table 3-1 Absolute Ratings

Parameters	Related Power Group	Min	Max	Unit
Supply voltage for DSP0	DSP0_DVDD	-0.3	1.20	V
Supply voltage for LOGIC	CORE_DVDD	-0.3	1.10	V
Supply voltage for PMU	PMU_DVDD0V9	-0.3	1.10	V
0.9V supply voltage	SYS_PLL_AVDD0V9	-0.3	1.10	V
1.8V supply voltage	SYS_PLL_AVDD1V8 TSADC_AVDD1V8 AVDD_1V8	-0.3	2.10	V
3.3V supply voltage	PMUIO_VCC3V3 USB2_OTG_AVDD3V3	-0.3	3.80	V
1.8V/3.3V supply voltage	VCCIO1_VCC VCCIO2_VCC VCCIO3_VCC VCCIO4_VCC VCCIO5_VCC	-0.3	3.80	V
Supply voltage for DDR IO	DDR_VDDQ	0	2.00	V
Storage Temperature	Tstg	-40	125	℃
Max Conjunction Temperature	Tj	0	125	℃

3.2 Recommended Operating Condition

The following table describes the recommended operating conditions.

Table 3-2 Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
Voltage for DSP0	DSP0_DVDD	0.85	1.10	1.15	V
Voltage for LOGIC	CORE_DVDD	0.85	0.975	1.025	V
Voltage for PMU	PMU_DVDD0V9	0.85	0.90	1.025	V
Voltage for PLL Analog (0.9V)	SYS_PLL_AVDD0V9	0.85	0.90	1.025	V
Voltage for PLL Analog (1.8V)	SYS_PLL_AVDD1V8	1.62	1.80	1.98	V
Voltage for GPIO (3.3V only)	PMUIO_VCC3V3	3.00	3.30	3.63	V
Voltage for GPIO (1.8V/3.3V)	VCCIO1_VCC VCCIO2_VCC VCCIO3_VCC	1.62 3.00	1.80 3.30	1.98 3.63	V

Parameters	Symbol	Min	Typ	Max	Unit
	VCCIO4_VCC VCCIO5_VCC				
Voltage for SarADC/OTP Analog (1.8V)	AVDD_1V8	1.62	1.8	1.98	V
Voltage for TSADC Analog (1.8V)	TSADC_AVDD1V8	1.62	1.8	1.98	V
Voltage for USB Analog (1.8V)	USB2_OTG_AVDD1V8	1.62	1.80	1.98	V
Voltage for USB Analog (3.3V)	USB2_OTG_AVDD3V3	3.00	3.30	3.63	V
DDR2 IO power	DDR_VDDQ	1.71	1.80	1.89	V
DDR3 IO power	DDR_VDDQ	1.425	1.50	1.575	V
OSC input clock frequency	F_{osc}	N/A	24/ 24.576	N/A	MHz
Ambient Operating Temperature	T_A	-20	25	80	℃

3.3 DC Characteristics

Table 3-3 DC Characteristics

Parameters		Symbol	Min	Typ	Max	Unit
Digital GPIO @3.3V	Input Low Voltage	Vil	-0.3	NA	0.8	V
	Input High Voltage	Vih	2.0	NA	VDDO+0.3	V
	Output Low Voltage	Vol	-0.3	NA	0.4	V
	Output High Voltage	Voh	2.4	NA	VDDO+0.3	V
	Pullup Resistor	Rpu	16	30	43	Kohm
	Pulldown Resistor	Rpd	16	30	43	Kohm
Digital GPIO @1.8V	Input Low Voltage	Vil	-0.3	NA	0.35*VDDO	V
	Input High Voltage	Vih	0.65*VDDO	NA	VDDO+0.3	V
	Output Low Voltage	Vol	-0.3	NA	0.4	V
	Output High Voltage	Voh	1.4	NA	VDDO+0.3	V
	Pullup Resistor	Rpu	16	30	43	Kohm
	Pulldown Resistor	Rpd	16	30	43	Kohm

3.4 Electrical Characteristics for General IO

Table 3-4 Electrical Characteristics for Digital General IO

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
Digital GPIO @3.3V	Input leakage current	Ii	Vin = 3.3V or 0V	NA	NA	15	uA
	Tri-state output leakage current	Ioz	Vout = 3.3V or 0V	NA	NA	15	uA
	High level input current	Iih	Vin = 3.3V, pulldown disabled	NA	NA	15	uA

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
			Vin = 3.3V, pulldown enabled	NA	NA	250	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	NA	NA	15	uA
			Vin = 0V, pullup enabled	NA	NA	250	uA
Digital GPIO @1.8V	Input leakage current	Ii	Vin = 1.8V or 0V	NA	NA	15	uA
	Tri-state output leakage current	Ioz	Vout = 1.8V or 0V	NA	NA	15	uA
	High level input current	Iih	Vin = 1.8V, pulldown disabled	NA	NA	15	uA
			Vin = 1.8V, pulldown enabled	NA	NA	150	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	NA	NA	15	uA
			Vin = 0V, pullup enabled	NA	NA	150	uA

3.5 Electrical Characteristics for PLL

Table 3-5 Electrical Characteristics for FRAC PLL

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
	Input clock frequency(Frac)	F_{in}	Fin = FREF	10	NA	1200	MHz
	VCO operating range	F_{vco}	Fvco = FREF * FBDIV	950	NA	3800	MHz
	Output clock frequency	F_{out}	Fout = Fvco/POSTDIV	19	NA	3800	MHz
	Lock time	T_{lt}	FREF=24M,REFDIV=1	NA	250	500	Input clock cycles

Notes:

① *REFDIV is the input divider value;*

② *FBDIV is the feedback divider value;*

③ *POSTDIV is the output divider value*

3.6 Electrical Characteristics for USB2.0 Interface

Table 3-6 Electrical Characteristics for USB2.0 Interface

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Transmitter						
Output Resistance	ROUT	Classic mode (Vout = 0 or 3.3V)	40.5	45	49.5	ohms

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
		HS mode (Vout = 0 to 800mV)	40.5	45	49.5	ohms
Output Capacitance	COUT	seen from D+ or D-			3	pF
Output Common Mode Voltage	VM	Classic (LS/FS) mode	1.45	1.65	1.85	V
		HS mode	0.175	0.2	0.225	V
Differential output signal high	VOH	Classic (LS/FS); Io=0mA	2.97	3.3	3.63	V
		Classic (LS/FS); Io=6mA	2.2	2.7	NA	V
		HS mode; Io=0mA	360	400	440	mV
Differential output signal low	VOL	Classic (LS/FS); Io=0mA	-0.33	0	0.33	V
		Classic (LS/FS); Io=6mA	NA	0.3	0.8	V
		HS mode; Io=0mA	-40	0	40	mV
Receiver						
Receiver sensitivity	RSENS	Classic mode	NA	+-250	NA	mV
		HS mode	NA	+-25	NA	mV
Receiver common mode	RCM	Classic mode	0.8	1.65	2.5	V
		HS mode (differential and squelch comparator)	0.1	0.2	0.3	V
		HS mode (disconnect comparator)	0.5	0.6	0.7	V
Input capacitance (seen at D+ or D-)			NA	NA	3	pF
Squelch threshold			100	NA	150	mV
Disconnect threshold			570	600	664	mV

3.7 Electrical Characteristics for SARADC

Table 3-7 Electrical Characteristics for SARADC

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Resolution			NA	10	NA	bit
Effective Number of Bit	ENOB		NA	9	NA	bit
Differential Non-Linearity	DNL		-1	NA	+1	LSB
Integral Non-Linearity	INL		-2	NA	+2	LSB
Reference voltage	VREFP		NA	1.8	NA	V
Input Capacitance	C_{IN}		NA	8	NA	pF
Clock Frequency	f_{adc}		NA	NA	12	MHz
Sampling Rate	f_S		NA	NA	1	MS/s
Input Voltage	VADC		0	NA	1.8	V
Spurious Free Dynamic Range	SFDR	f_S=1MS/s f_{OUT}=1.17KHz	NA	61	NA	dB
Signal to Noise and Harmonic Ratio	SNDR		NA	56	NA	dB

3.8 Electrical Characteristics for TSADC

Table 3-8 Electrical Characteristics for TSADC

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Accuracy from -40℃ to 125℃	T_{JACC}		NA	NA	±5	℃
Sensing Temperature Range	T_{RANGE}		-40	NA	125	℃
Resolution	T_{LSB}		NA	0.6	NA	℃

Chapter 4 Timing Specification

4.1 AUPLL_CLK_IN

Table 4-1 AUPLL_CLK_IN Clock Requirements

Parameters	Min	Typ	Max	Unit
Clock Frequency	1		125	Mhz
Clock duty cycle	45	50	55	%

4.2 FSPI

The following table gives the FSPI electrical characteristics.
Test conditions: maximum output load 15 pF, input transition time 2 ns, drive strength set to 6'b000111, and Slew Rate set to 2'b11.

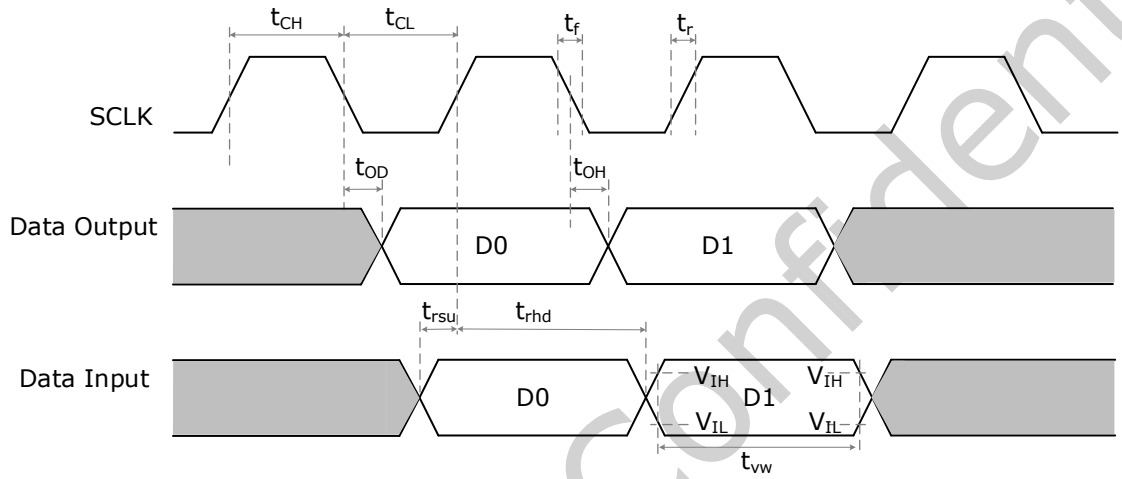


Fig. 4-1 FSPI SCLK and data timing diagram (SDR read mode and write mode)

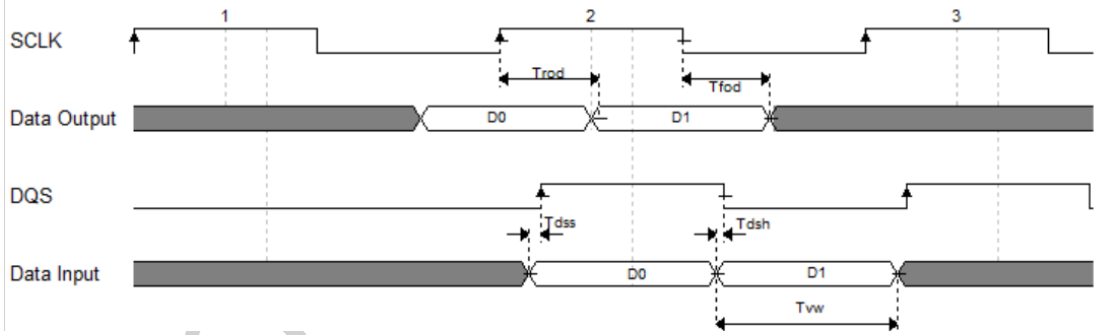


Fig. 4-2 FSPI SCLK and data timing diagram (DDR read with DQS mode and DDR write mode)

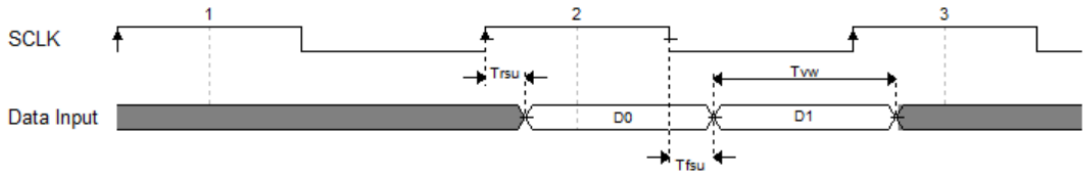


Fig. 4-3 FSPI SCLK and data timing diagram (DDR read without DQS mode)

Table 4-2 FSPI Electrical Specification in VDDxx SDR read mode and write mode

Parameter		Min	Typ	Max	Min	Typ	Max	Unit
		1.8V			3.3V			
f_{SCLK}	FSPI Clock Frequency			120			120	MHz
t_{CH}	Clock High	t_{CK}*45%		t_{CK}*55	t_{CK}*45		t_{CK}*55%	ns

				%	%			
t_{CL}	Clock Low	t_{CK}*45%		t_{CK}*55 %	t_{CK}*45 %		t_{CK}*55%	ns
t_{OD}	Data output valid time	-2		2	-2		2	ns
t_{OH}	Data output hold time	-2		2	-2		2	ns
t_{rsu}*1	Data input setup time for rise edge sampling	8.5			7.7			ns
t_{rhd}	Data input hold time for rise edge sampling	0			0			ns
t_{vw}	Data valid window	0.5* t_{CK}			0.5* t_{CK}			

Note (1):
1. When the signal rate exceeds 50 MHz, it is acceptable as long as it meets the tvw specification requirements.
2. Supports delaying the sampling edge by 180 degrees to reduce the setup time requirement. In addition, a Delayline module is also support which can adjust the phase of the signal passing through the module to achieve phase calibration in high-frequency scenarios

Table 4-3 FSPI Electrical Specification in VDDxx DDR read with DQS mode and DDR write mode

Parameter		Min	Typ	Max	Min	Typ	Max	Unit
		1.8V			3.3V			
f_{SCLK}	FSPI Clock Frequency			50			80	MHz
t_{CH}	Clock High	t_{CK}*45%		t_{CK}*55%	t_{CK}*45%		t_{CK}*55%	ns
t_{CL}	Clock Low	t_{CK}*45%		t_{CK}*55%	t_{CK}*45%		t_{CK}*55%	ns
Trod	Rise Output Delay Time	-1+0.25*tcycle		2+0.25*tcycle	-1+0.25*tcycl		2+0.25*tcycl	ns
Tfod	Fall Output Delay Time	-1+0.25*tcycle		2+0.25*tcycle	-2+0.25*tcycl		2+0.25*tcycl	ns
Tdss	DQS transition to DQ Valid	0.5			0.5			ns
Tdsh	DQS transition to DQ Invalid	1.5			1.5			ns
t_{vw}	Data valid window	0.25* t_{CK}			0.25* t_{CK}			

Table 4-4 FSPI Electrical Specification in VDDxx DDR READ without DQS mode

Parameter		Min	Typ	Max	Min	Typ	Max	Unit
		1.8V			3.3V			
f_{SCLK}	FSPI Clock Frequency			50			50	MHz
t_{CH}	Clock High	t_{CK}*45%		t_{CK}*55%	t_{CK}*45%		t_{CK}*55%	ns
t_{CL}	Clock Low	t_{CK}*45%		t_{CK}*55%	t_{CK}*45%		t_{CK}*55%	ns
Trsu	data input setup time for rise edge sampling	0		1.5*tcycle -8.5	0		1.5*tcycle -7.7	ns
Tfsu	Data input setup time for fall edge sampling	0		1.5*tcycle -8.5	0		1.5*tcycle -7.7	ns
t_{vw}	Data valid window	0.25* t_{CK}			0.25* t_{CK}			

4.3 eMMC

The following table gives the eMMC electrical characteristics.
Test conditions: maximum output load 15 pF, input transition time 2 ns, drive strength set to 6'b000111, and Slew Rate set to 2'b11.I

4.3.1 EMMC Backward Mode

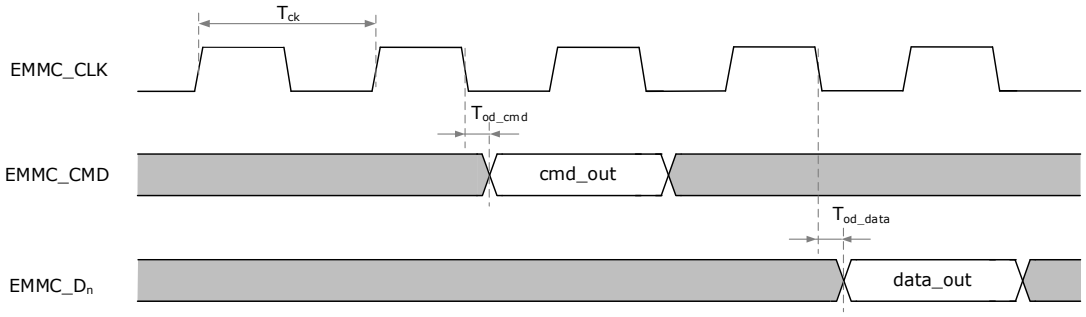


Fig. 4-4 eMMC Backward Mode Output Timing

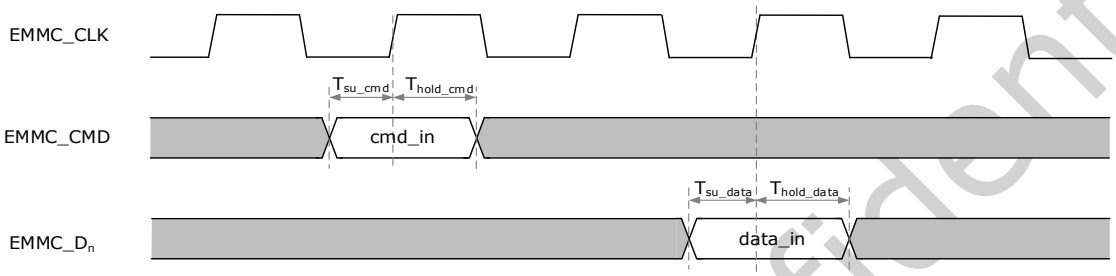


Fig. 4-5 eMMC Backward Mode input Timing

Table 4-5 EMMC Backward Mode Timing

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
		1.8V			3.3V			
CMD Interface								
Tsu_cmd	Command input setup time	9			8			ns
Thold_cmd	Command input hold time	0			0			ns
Tod_cmd	Command output delay time	-2		2	-2		2	ns
DATA Interface								
Tsu_data	Data input setup time	9			8			ns
Thold_data	Data input hold time	0			0			ns
Tod_data	Data output delay time	-2		2	-2		2	ns
Clock Interface								
Tck	Clock cycle time	40			40			ns

4.3.2 EMMC High Speed Mode

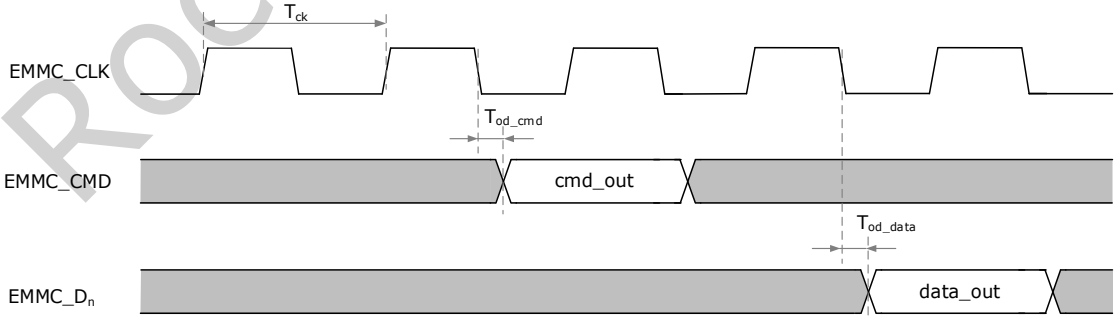


Fig. 4-6 EMMC High Speed Mode Output Timing

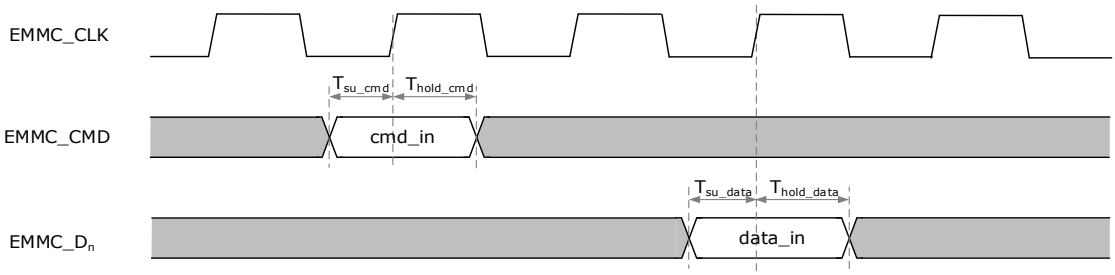


Fig. 4-7 EMMC High Speed Mode Input Timing

Table 4-6 EMMC High Speed Mode Timing

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
		1.8V			3.3V			
CMD Interface								
Tsu_cmd	Command input setup time	9			8			ns
Thold_cmd	Command input hold time	0			0			ns
Tod_cmd	Command output delay time	-2		2	-2		2	ns
DATA Interface								
Tsu_data	Data input setup time	9			8			ns
Thold_data	Data input hold time	0			0			ns
Tod_data	Data output delay time	-2		2	-2		2	ns
Clock Interface								
Tck	Clock cycle time	20						ns

4.4 SDMMC

The following table gives the SDMMC electrical characteristics.
Test conditions: maximum output load 15 pF, input transition time 2 ns, drive strength set to 6'b000111, and Slew Rate set to 2'b11.I.

4.4.1 Default Speed Mode

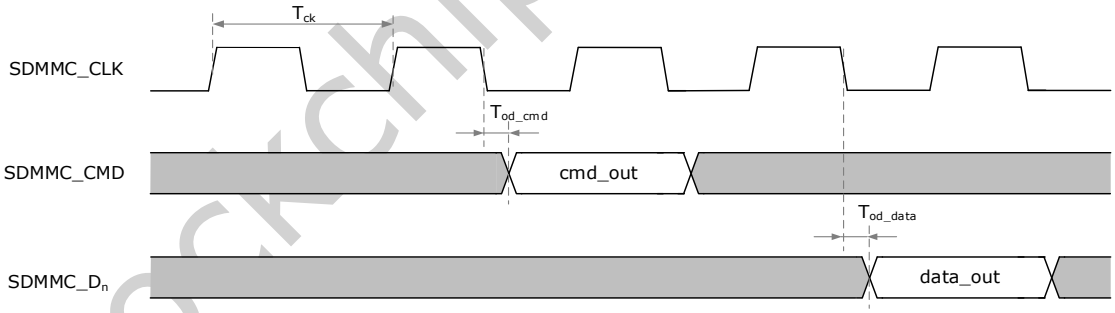


Fig. 4-8 SDMMC Default Speed Mode Output Timing

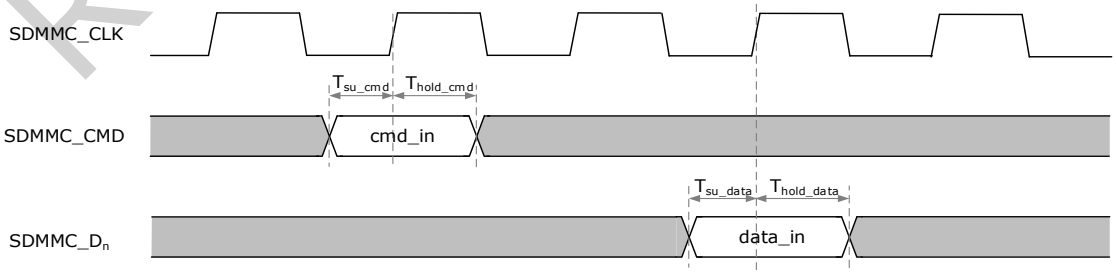


Fig. 4-9 SDMMC Default Speed Mode Input Timing

Table 4-7 SDMMC High Speed Mode Timing

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
		1.8V			3.3V			
CMD Interface								
Tsu_cmd	Command input setup time	8			8			ns
Thold_cmd	Command input hold time	0			0			ns
Tod_cmd	Command output delay time	-2		2	-2		2	ns
DATA Interface								
Tsu_data	Data input setup time	9			8			ns
Thold_data	Data input hold time	0			0			ns
Tod_data	Data output delay time	-2		2	-2		2	ns
Clock Interface								
Tck	Clock cycle time	20			40			ns

4.4.2 High Speed Mode

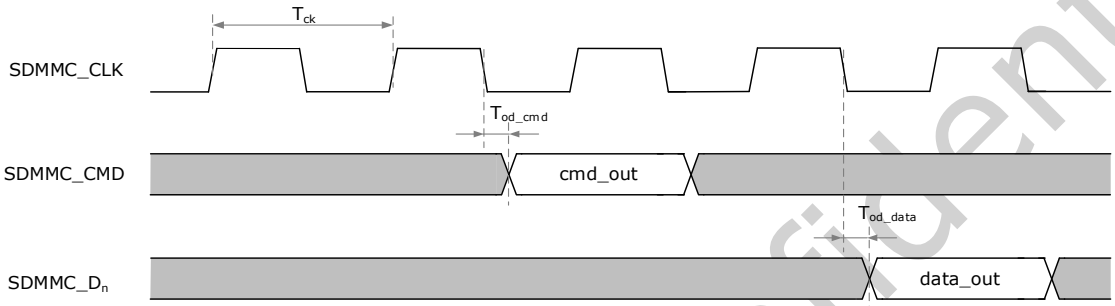


Fig. 4-10 SDMMC High Speed Mode Output Timing

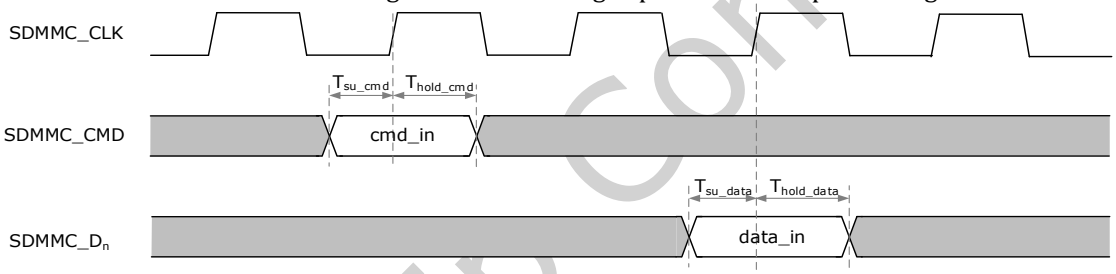


Fig. 4-11 SDMMC High Speed Mode Output Timing

Table 4-8 SDMMC High Speed Mode Timing

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
		1.8V			3.3V			
CMD Interface								
Tsu_cmd	Command input setup time	9			8			ns
Thold_cmd	Command input hold time	0			0			ns
Tod_cmd	Command output delay time	-2		2	-2		2	ns
DATA Interface								
Tsu_data	Data input setup time	9			8			ns
Thold_data	Data input hold time	0			0			ns
Tod_data	Data output delay time	-2		2	-2		2	ns
Clock Interface								
Tck	Clock cycle time	20			20			ns

4.5 RMII

The following table gives the RMII electrical characteristics.
Test conditions: maximum output load 15 pF, input transition time 2 ns, drive strength set to 6'b000111, and Slew Rate set to 2'b11.

4.5.1 RMII

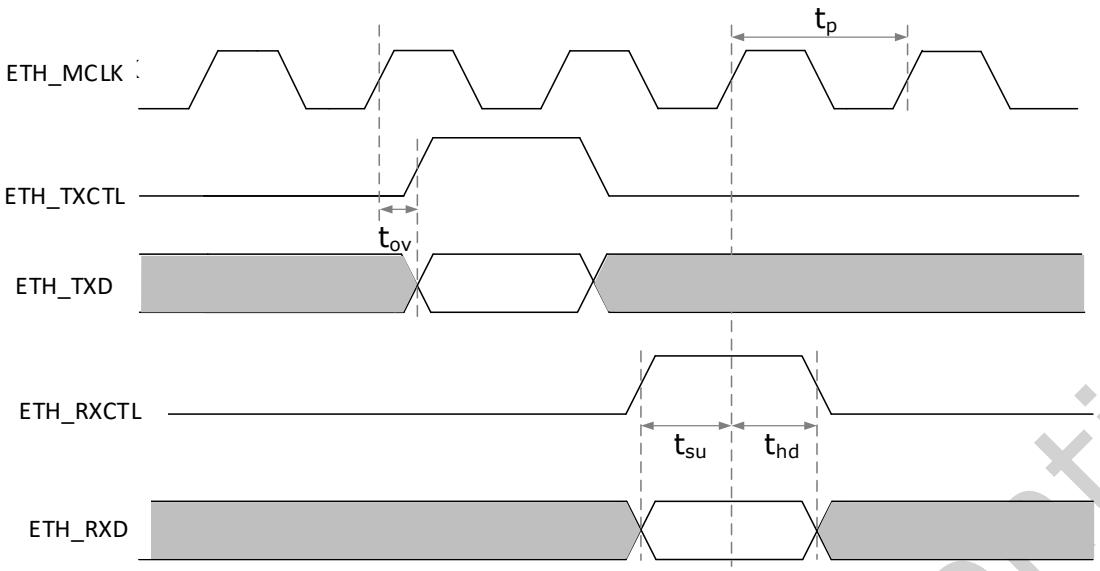


Fig. 4-12 RMII Interface Timing

Table 4-9 MAC Timing in RMII Mode and Internal Clock Mode

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
		1.8V			3.3V			
tp	REF_CLK Period		20			20		ns
tsu	RXD Setup Time	6			6			ns
thd	RXD Hold Time	0			0			ns
tov	TXD Output Delay	3		10	3		10	ns

Table 4-10 MAC Timing in RMII Mode and External Clock Mode

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
		1.8V			3.3V			
tp	REF_CLK Period		20			20		ns
tsu	RXD Setup Time	6			6			ns
thd	RXD Hold Time	0			0			ns
tov	TXD Output Delay	3		10	3		10	ns

4.5.2 MDIO

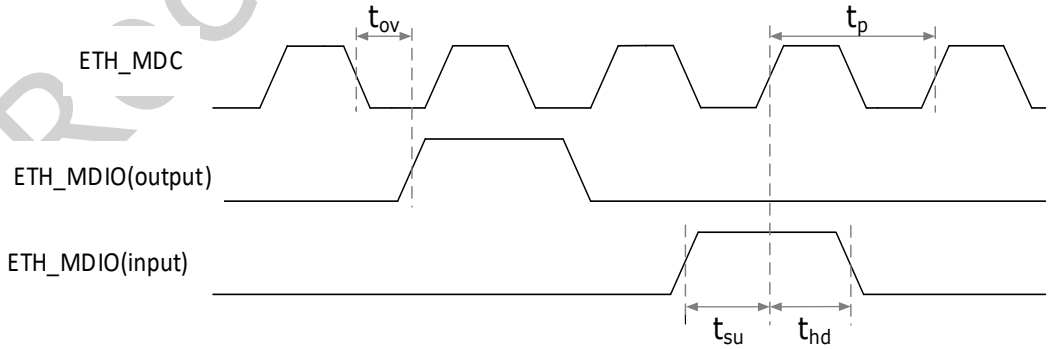


Fig. 4-13 MDIO Timing

Table 4-11 MAC MDIO Timing in 1.8V

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit

	1.8V	3.3V						
tp	MDC Period	400			400			ns
tsu	MDIO Setup Time(Read)	8			8			ns
thd	MDIO Hold Time(Read)	0			0			ns
tov	MDIO Output Delay(Write)	-1		3	-1		3	ns

4.6 SAI

The following table gives the SAI electrical characteristics.
Test conditions: maximum output load 15 pF, input transition time 2 ns, drive strength set to 6'b000111, and Slew Rate set to 2'b11.

4.6.1 Master Mode

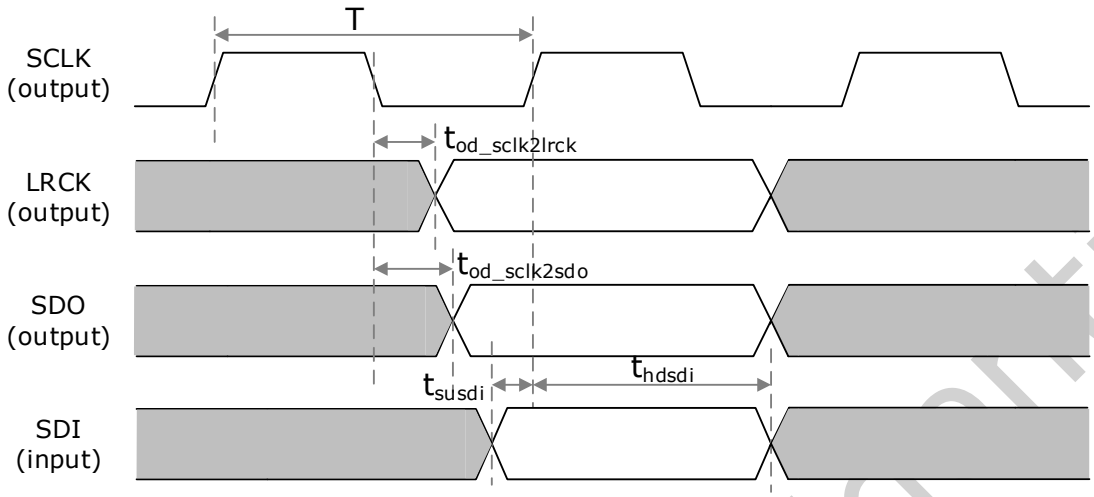


Fig. 4-14 SAI Master PAD Interface Timing Diagram

Table 4-12 SAI Master Mode Timing

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
			1.8V			3.3V		
Fsclk*1	Frequency of SCLK	0.256		49.152	0.256		49.152	MHz
Fsclk*1	Duty cycle of SCLK	45%	50%	55%	45%	50%	55%	
LRCK*1	Duty cycle	45%	50%	55%	45%	50%	55%	
$t_{od\_sclk2lrck}$*1	LRCK delay time from SCLK falling edge	-1.5		1.5	-1.5		1.5	ns
$t_{od\_sclk2sdo}$*1	SDO propagation delay from SCLK falling edge	-1.5		1.5	-1.5		1.5	ns
t_{susdi}*1	SDI setup time to SCLK rising edge	10			11			ns
t_{hdsdi}*1	SDI hold time from SCLK rising edge	0			0			ns
t_{susdi_hs}*1,2	SDI setup time to SCLK rising edge for high speed	10-T/2			11-T/2			ns
t_{hdsdi_hs}*2	SDI hold time from SCLK rising edge for high speed mode	T/2-5			T/2-5.5			ns

1. The maximum frequency of the interface is 49.152 MHz. Whether the actual data transmission rate can reach this level depends on t_{od_slave} (output delay of the slave device) , t_{pd_clk} (propagation delay of CLK) and t_{pd_data}(propagation delay of data). It should meet $t_{susdi}+ t_{od\_slave}+ t_{pd\_clk} + t_{pd\_data} < T/2$ in normal mode or $t_{susdi\_hs}+ t_{od\_slave}+ t_{pd\_clk} + t_{pd\_data} < T/2$ in high speed mode.

2.The SAI supports configure the RX_TIMING_SHIFT register to change sampling edges in high speed mode. so the minimum setup time on the SoC side can subtract T/2 from t_{susdi}. *The minimum hold time on the SoC side is the value that subtract an interval from T/2.*

4.6.2 Slave Mode

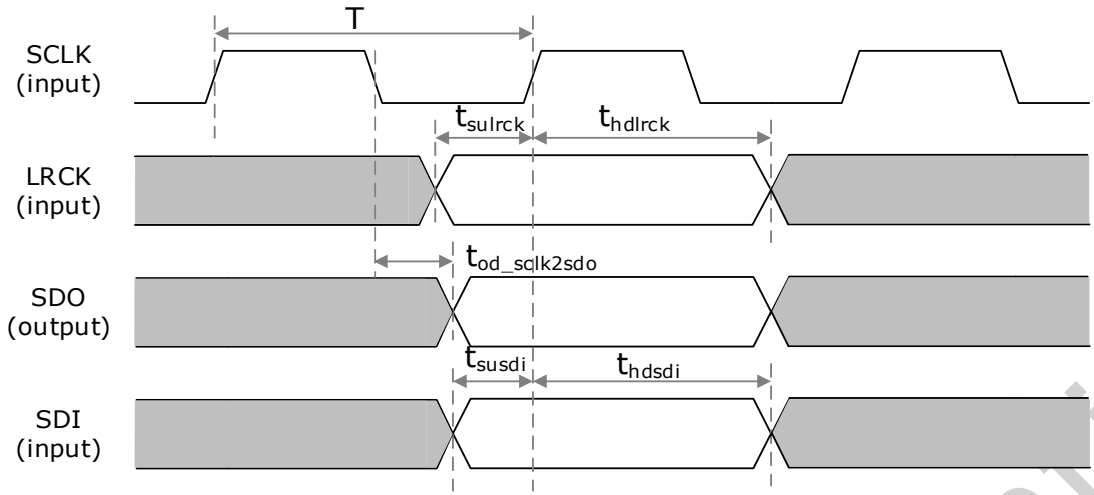


Fig. 4-15 SAI Slave PAD Interface Timing Diagram

Table 4-13 SAI Slave Mode Timing

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
		1.8V			3.3V			
Fsclk*1	Frequency of SCLK	0.256		49.152	0.256		49.152	MHz
Fsclk*1	Duty cycle of SCLK	45%	50%	55%	45%	50%	55%	
LRCK*1	Duty cycle	45%	50%	55%	45%	50%	55%	
t_{sulrck}*1	LRCK setup time to SCLK rising edge	1.5			1.5			ns
t_{hdlrck}*1	LRCK hold time from SCLK rising edge	1.5			1.5			ns
$t_{od\_sclk2sdo}$*1	SDO propagation delay from SCLK falling edge			13			13	
t_{susdi}*1	SDI setup time to SCLK rising edge	1.5			1.5			ns
t_{hdsdi}*1	SDI hold time from SCLK rising edge	1.5			1.5			ns
$t_{od\_sclk2sdo\_hs}$*2	SDO propagation delay from SCLK falling edge for high speed mode			13-T/2			13-T/2	ns

1. The maximum frequency of the interface is 49.152 MHz. Whether the actual data transmission rate can reach this level depends on $t_{od\_sclk2sdo\_hs}$ */* $t_{od\_sclk2sdo}$ *and the receiving capability of the master.*
2.The SAI supports configure the TX_TIMING_SHIFT register to change drive edges in high speed mode, so the maximum SDO propagation delay on *the SoC side can subtract T/2 from* $t_{od\_sdk2sdo}$.

4.7 PDM

The following table gives the PDM electrical characteristics.
Test conditions: maximum output load 15 pF, input transition time 2 ns, drive strength set to 6'b000111, and Slew Rate set to 2'b11

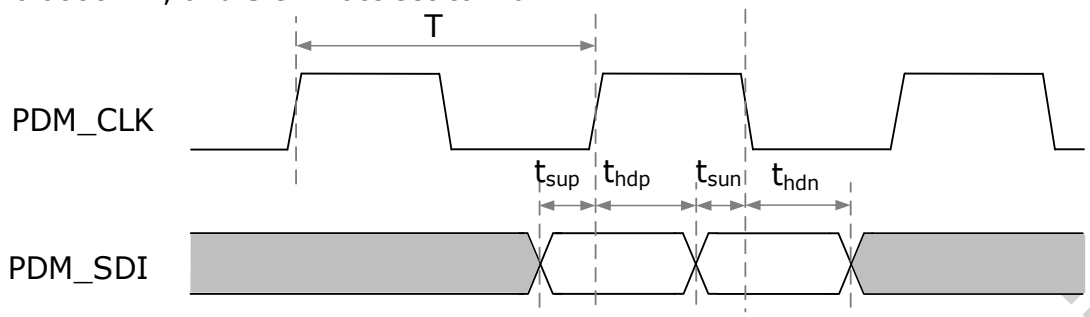


Fig. 4-16 PDM Timing Diagram

Table 4-14 PDM Timing

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
		1.8V			3.3V			
T	Frequency of PDM_CLK	1.024	4.096	6.144	1.024	4.096	6.144	MHz
Tduty	Duty cycle of PDM_CLK	45%	50%	55%	45%	50%	55%	N/A
tsup	Input SDI setup time to PDM_CLK rising edge	9.5			8.6			ns
thdp	Input SDI hold time to PDM_CLK rising edge	0			0			ns
tsun	Input SDI setup time to PDM_CLK falling edge	9.5			8.5			ns
thdn	Input SDI hold time to PDM_CLK falling edge	0			0			ns

4.8 SPI

The following table gives the SPI electrical characteristics.
Test conditions: maximum output load 15 pF, input transition time 2 ns, drive strength set to 6'b000111, and Slew Rate set to 2'b11.

4.8.1 SPI MASTER

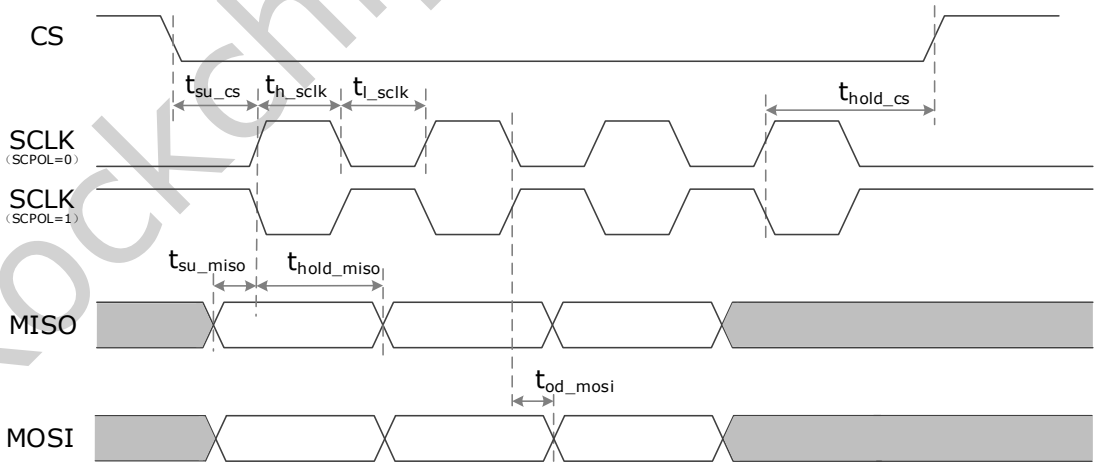


Fig. 4-17 SPI Master Mode Timing Diagram

Table 4-15 SPI1 Timing in Master Mode 1.8V

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
	1.8V			3.3V			
Fsclk			50			50	MHz
th_sclk	10			10			ns

tl_sclk	10			10			ns
thold_cs	9.7			9.8			ns
tsu_cs	9.6			9.6			ns
tsu_miso	9.5-(rsd+1)*5			10.1-(rsd+1)*5			ns
thold_miso	(rsd+1)*5- 8.3			(rsd+1)*5- 8.9			ns
tod_mosi	-1		3	-2		3	ns
1.rsd=0,1,2,3.Default rsd=1							

Table 4-16 SPI2 Timing in Master Mode 1.8V

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
	1.8V			3.3V			
Fsclk			50			50	MHz
th_sclk	10			10			ns
tl_sclk	10			10			ns
thold_cs	9.7			9.7			ns
tsu_cs	9.7			9.7			ns
tsu_miso	8.6-(rsd+1)*5			9.2-(rsd+1)*5			ns
thold_miso	(rsd+1)*5- 7.6			(rsd+1)*5- 8.3			ns
tod_mosi	-1		3	-2		3	ns
1.rsd=0,1,2,3.Default rsd=1							

4.8.2 SPI Slave

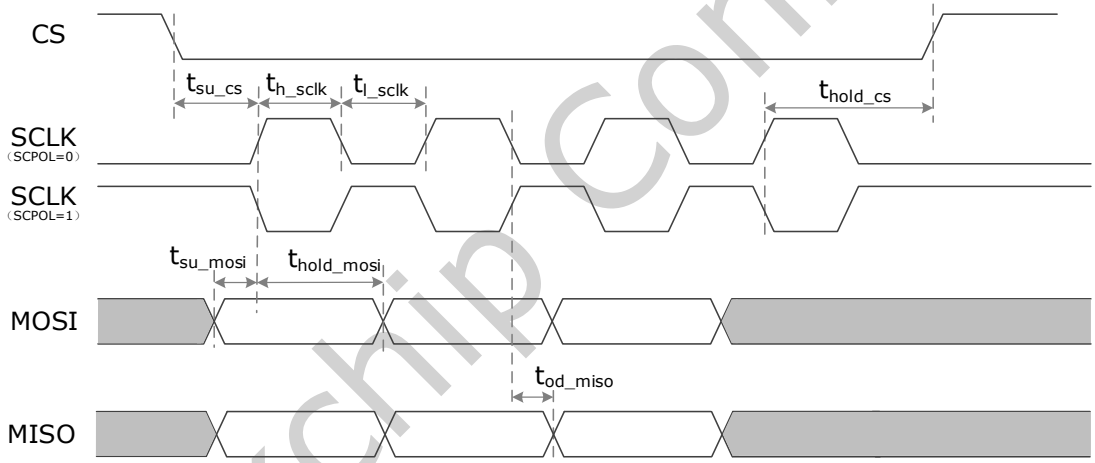


Fig. 4-18 SPI Slave Mode Timing Diagram

Table 4-17 SPI0 M0 Timing in Slave Mode

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
	1.8V			3.3V			
Fsclk			50			50	MHz
th_sclk	10			10			ns
tl_sclk	10			10			ns
tsu_cs	0.3			0.5			ns
thold_cs	0.5			0.5			ns
tsu_mosi	0.4			0.6			ns
thold_mosi	0.9			0.9			ns

tod_miso	3		9	5		11	ns

Table 4-18 SPI0 M1 Timing in Slave Mode

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
	1.8V			3.3V			
Fsclk			50			50	MHz
th_sclk	10			10			ns
tl_sclk	10			10			ns
tsu_cs	0.2			0.4			ns
thold_cs	0.5			0.5			ns
tsu_mosi	0			0.3			ns
thold_mosi	1			1			ns
tod_miso	3		9	5		11	ns

Table 4-19 SPI1 Timing in Slave Mode

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
	1.8V			3.3V			
Fsclk			50			50	MHz
th_sclk	10			10			ns
tl_sclk	10			10			ns
tsu_cs	5			5			ns
thold_cs	25			25			ns
tsu_mosi	0.4			0.6			ns
thold_mosi	1			1			ns
tod_miso	3.2		9.7	3.1		9.7	ns

Table 4-20 SPI2 Timing in Slave Mode

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
	1.8V			3.3V			
Fsclk			50			50	MHz
th_sclk	10			10			ns
tl_sclk	10			10			ns
tsu_cs	5			5			ns

thold_cs	25			25			ns
tsu_mosi	0.3			0.5			ns
thold_mosi	0.8			0.8			ns
tod_miso	2.6		9.5	2.5		9.4	ns

4.9 Flexbus

The following table gives the SPI electrical characteristics.
Test conditions: maximum output load 15 pF, input transition time 2 ns, drive strength set to 6'b000111, and Slew Rate set to 2'b11.

4.9.1 Flexbus Master Mode

4.9.1.1 TX Timing and RX Timing (Flexbus0Clk Output and Flexbus0Dat Modes)

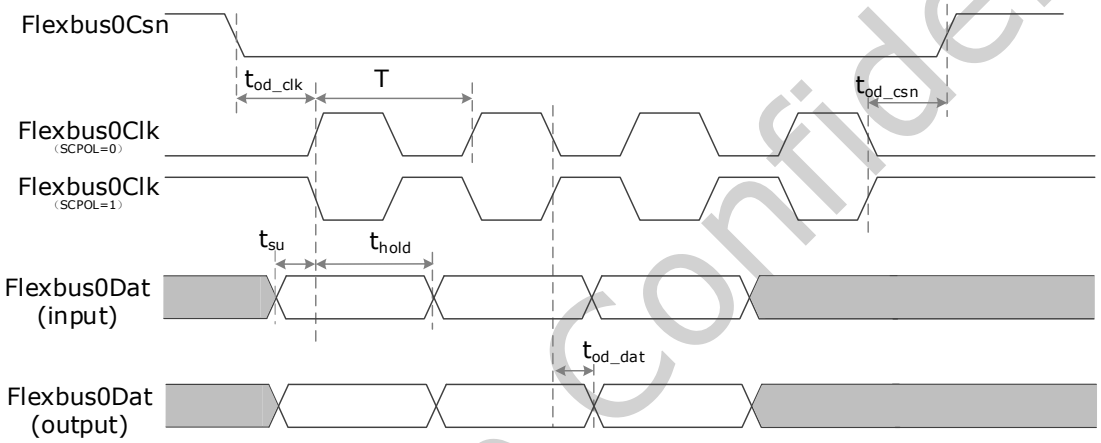


Fig. 4-19 Flexbus TX&RX Timing Diagram in Master Mode

Table 4-21 Flexbus0 Timing in Master Mode

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
		1.8V			3.3V			
Fclk	Flexbus clock Frequency		txclk/2	100		txclk/2	100	MHz
tod_clk	Flexbus0Csn active to Flexbus0Clk valid	(1-cpha)*tcycle -0.7		(1-cpha)*tcycle +0.2	(1-cpha)*tcycle - 0.4		(1-cpha)*tcycle +0.3	ns
tod_csn	Flexbus0Clk stop to Flexbus0Csn inactive	cpha*tcycle-0.2		cpha*tcycle + 0.7	cpha*tcycle – 0.3		(cpha)*tcycle+0.4	ns
tsu	Data input setup time	9.1-tcycle			8-tcycle			ns
thold	Data input hold time	tcycle - 2.4			tcycle – 3.3			ns
tod_dat	Data output delay	-2		2	-2		2	ns

1.cpha=0 or 1

4.9.1.2 TX Timing and RX Timing (Flexbus0Clk Output and Flexbus0Dat Modes)

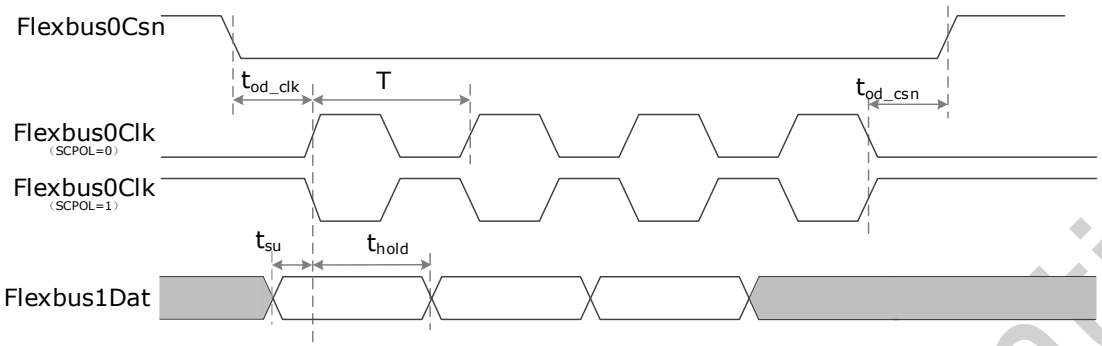


Fig. 4-20 Flexbus RX Timing Diagram 1 in Master Mode

Table 4-22 Flexbus1 Timing in Master Mode

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
		1.8V			3.3V			
Fclk	Flexbus clock Frequency		txclk/2	100		txclk/2	100	MHz
tod_clk	Flexbus0Csn active to Flexbus0Clk valid	(1-cpha)*tcycle -0.7		(1-cpha)*tcycle +0.2	(1-cpha)*tcycle -0.4		(1-cpha)*tcycle +0.3	ns
tod_csn	Flexbus0Clk stop to Flexbus0Csn inactive	cpha*tcycle – 0.2		cpha*tcycle +0.7	cpha*tcycle – 0.3		cpha*tcycle +0.4	ns
tsu	Data input setup time	9.1-cycle			8.1-tcycle			ns
thold	Data input hold time	tcycle - 2.4			tcycle - 3.3			ns
1.cpha=0 or 1								

4.9.1.3 RX Timing (Flexbus1Clk Output and Flexbus1Dat Input Mode)

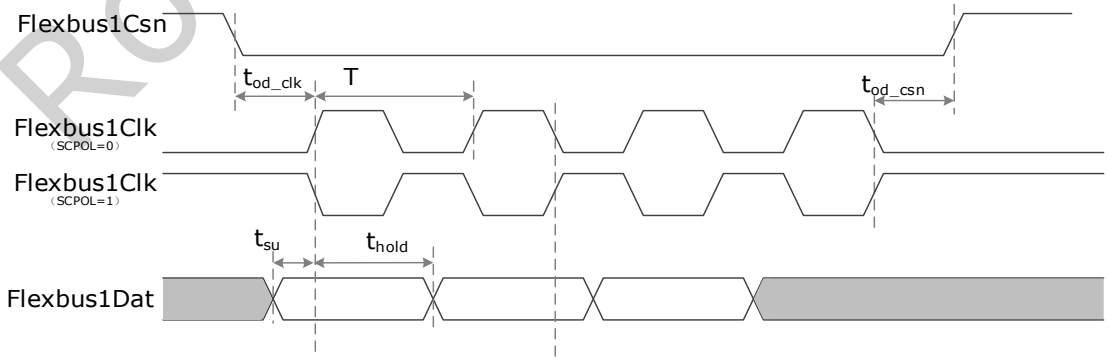


Fig. 4-21 Flexbus RX Timing Diagram 2 in Master Mode

Table 4-23 Flexbus1 Timing in Master Mode

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
		1.8V			3.3V			
Fclk	Flexbus clock Frequency		txclk/2	100		txclk/2	100	MHz
tod_clk	Flexbus0Csn active to Flexbus0Clk valid	(1-cpha)*tcycle -1.1		(1-cpha)*tcycle +0.1	(c1-cpha)*tcycle -0.8	NA	(1-cpha)*tcycle +0.1	ns
tod_csn	Flexbus0Clk stop to Flexbus0Csn inactive	cpha*tcycle – 0.1		cpha*tcycle +1.1	cpha*tcycle – 0.1	NA	cpha*tcycle +0.8	ns
tsu	Data input setup time	9.1-tcycle			8-tcycle			ns
thold	Data input hold time	tcycle - 2.4			tcycle - 3.3			ns
1.cpha=0 or 1								

4.9.2 Flexbus Slave Mode

4.9.2.1 RX Timing (Flexbus1Dat Input Mode)

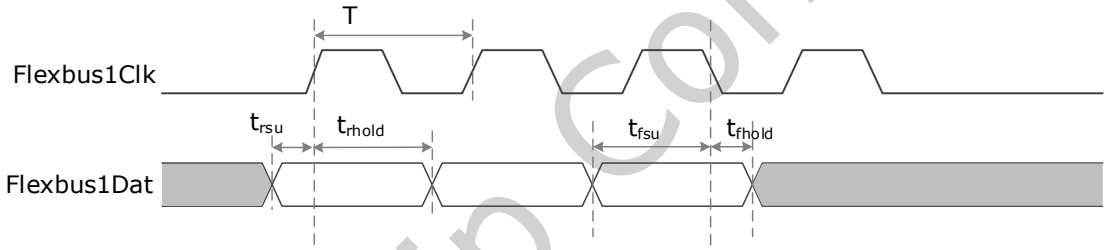


Fig. 4-22 Flexbus RX Timing Diagram 1 in Slave Mode

Table 4-24 Flexbus1 timing in Slave Mode

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
		1.8V			3.3V			
Fclk	Flexbus clock Frequency			100			100	MHz
trsu	Data input setup time for rise edge sampling	0.8			0.7			ns
trhold	Data input hold time for rise edge sampling	0.3			0.4			ns
tfsu	Data input setup time for fall edge sampling	0.8			0.7			ns
tfhold	Data input hold time for fall edge sampling	0.3			0.4			ns

4.9.2.2 RX Timing (Flexbus0Dat Input Mode)

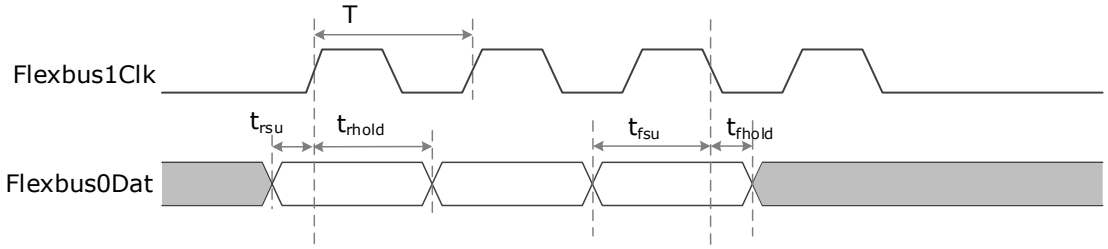


Fig. 4-23 Flexbus RX Timing Diagram 1 in Slave Mode

Table 4-25 Flexbus1 Timing in Slave Mode

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
		1.8V			3.3V			
Fclk	Flexbus clock Frequency			100			100	MHz
trsu	Data input setup time for rise edge sampling	0.7			0.6			ns
trhold	Data input hold time for rise edge sampling	0.3			0.4			ns
tfsu	Data input setup time for fall edge sampling	0.7			0.6			ns
tfhold	Data input hold time for fall edge sampling	0.3			0.4			ns

4.10I2C

Refer to the I2C protocol of 'UM10204-I2C-bus specification and user manual'

Chapter 5 Thermal Management

5.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature has to be below 125℃.

5.2 Package Thermal Characteristics

Table 5-1 provides the thermal resistance characteristics for the package used on the SoC. The resulting simulation data for reference only, please prevail in kind test.

Table 5-1 RK2118G Thermal Resistance Characteristics

Parameter	Symbol	Typical	Unit	Note
Junction-to-ambient thermal resistance	θ_{JA}	13	(℃/W)	(1)
Junction-to-board thermal resistance	θ_{JB}	4.5	(℃/W)	(2)
Junction-to-case thermal resistance	θ_{JC}	4	(℃/W)	(3)
Thermal characterization parameter	ψ_{JT}	0.5	(℃/W)	(4)

Note (1): The package-board system is placed in the natural convection (JEDEC JESD51-2 standard), and the 2S2P test-board is designed in accordance with JESD 51-7/JESD 51-9. The actual system design and environment may be different. (The PCB is 4 layers, 114.5 mm*76.2 mm)

Note (2): θ_{JB} is measured in the special environment (JEDEC JESD51-8 standard), and the printed circuit board used to mount the devices is specified in JESD51-7.

Note (3): The thermal resistance θ_{JC} is provided in compliance with the JEDEC JESD51-14.

Note (4): ψ_{JT} - The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package, $\psi_{JT}$is measured in the test environment of θ_{JA} (JEDEC JESD51-2 standard).