

Rockchip RK3028 Datasheet

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Chapter 1 Introduction

1.1 Overview

RK3028 is a low power, high performance processor for mobile phones, personal mobile internet device and other digital multimedia applications, and integrates dual-core Cortex-A9 with separately NEON and FPU coprocessor.

Many embedded powerful hardware engines provide optimized performance for high-end application. RK3028 supports almost full-format video decoder by 1080p@30fps, also support H.264 encoder by 1080p@30fps, high-quality JPEG encoder/decoder, special image preprocessor and postprocessor .

Embedded 3D GPU makes RK3028 completely compatible with OpenGL ES2.0 and 1.1, OpenVG 1.1. Special 2D hardware engine with MMU will maximize display performance and provide very smoothly operation.

RK3028 has high-performance external memory interface(DDR3/LVDDR3) capable of sustaining demanding memory bandwidths, also provides a complete set of peripheral interface to support very flexible applications as follows :

- Support async NAND Flash, Sync Toggle NAND Flash, LBA NAND Flash and sync ONFI NAND Flash, 4 banks, all up to 60bits hardware ECC
- Totally 2GB memory space for 2 ranks, 16bits DDR3-800 , LVDDR3-800
- Totally 2-channels SD/MMC interface to support MMC4.41, SD3.0 or SDIO3.0
- One-channels TFT LCD interface with 4-layers, 1920x1080 maximum display size
- One-channels, 8bits CCIR656 interface with image preprocessor
- One USB OTG 2.0 and one USB Host2.0 interface
- High-speed ADC interface
- Lots of low-speed peripheral interface : 3 I2C, 4 UART, 1 SPI, 3 PWM
- HDMI 1.4/1.3/1.2/1.1, HDCP 1.2 and DVI 1.0 standard compliant transmitter
- LVDS support VGA, SVGA, XGA and single pixel SXGA, and comply with the Standard TIA/EIA-644-A LVDS stand
- Audio Codec with Mono Microphone interface

This document will provide guideline on how to use RK3028 correctly and efficiently. The chapter 1 and chapter 2 will introduce the features, block diagram, signal descriptions and system usage of RK3028, the chapter 3 through chapter 6 will describe the full function of each module in detail.

1.2 Features

1.2.1 MicroProcessor

- Dual-core ARM Cortex-A9 MPCore, a high-performance, low-power and cached application processor
- Full implementation of the ARM architecture v7-A instruction set, ARM Neon Advanced SIMD (single instruction, multiple data) support for accelerated media and signal processing computation
- Superscalar, variable length, out-of-order pipeline with dynamic branch prediction, 8-stage pipeline
- Include VFPv3 hardware to support single and double-precision add, subtract, divide, multiply and accumulate, and square root operations
- SCU ensures memory coherency between the two CPUs
- Integrated timer and watchdog timer per CPU
- Integrated 32KB L1 instruction cache , 32KB L1 data cache with 4-way set associative
- 256KB unified L2 Cache
- TrustZone technology support
- Full coresight debug solution

- Debug and trace visibility of whole systems
- ETM trace support
- Invasive and non-invasive debug
- One separate power domain for secondary core to support internal power switch and externally turn on/off based on different application scenario
 - PD_A9_1: 2nd Cortex-A9 + Neon + FPU + L1 I/D Cache
- One isolated voltage domain to support DVFS
- Maximum frequency can be up to 1GHz@1.0V(Worst Case)

1.2.2 Memory Organization

- Internal on-chip memory
 - 10KB BootRom
 - 16KB internal SRAM for security and non-security access, detailed size is programmable
 - 128KB or 256KB internal SRAM shared with L2 Cache Memory
- External off-chip memory^①
 - DDR3-800, 16bits data widths, 2 ranks, totally 2GB(max) address space, maximum address space for one rank is also 2GB.
 - Async NAND Flash, 8bits data width, 4 banks, 60bits ECC
 - Sync Toggle NAND Flash, 8bits data width, 4 banks, 60bits ECC
 - Sync ONFI NAND Flash , 8bits data width, 4 banks, 60bits ECC
 - Support LBA NAND Flash

1.2.3 Internal Memory

- Internal BootRom
 - Size : 10KB
 - Support system boot from the following device :
 - ◆ 8bits Async NAND Flash
 - ◆ 8bits ONFI NAND Flash
 - ◆ SPI interface
 - ◆ eMMC interface
 - Support system code download by the following interface:
 - ◆ USB OTG interface
- Internal SRAM
 - Size : 16KB
 - Support security and non-security access
 - Security or non-security space is software programmable
 - Security space can be 0KB,4KB,8KB,12KB,16KB continuous size
- 128KB or 256KB internal SRAM shared with L2 Cache for Cortex-A9, size is configurable by software.

1.2.4 External Memory or Storage device

- Dynamic Memory Interface (DDR3)
 - Compatible with JEDEC standard DDR3 SDRAM
 - Data rates up to 800Mbps(400MHz) for DDR3
 - Support up to 2 ranks (chip selects), totally 2GB(max) address space, maximum address space for one rank is also 2GB, which is software-configurable.
 - 16bits data width is software programmable
 - 5 host ports with 64bits AXI bus interface for system access, AXI bus clock is asynchronous with DDR clock
 - Programmable timing parameters to support DDR3 SDRAM from various vendor
 - Advanced command reordering and scheduling to maximize bus utilization
 - Low power modes, such as power-down and self-refresh for DDR3 SDRAM
 - Compensation for board delays and variable latencies through programmable pipelines
 - Embedded dynamic drift detection in the PHY to get dynamic drift compensation with the controller

- Programmable output and ODT impedance with dynamic PVT compensation
- Support one low-power work mode: power down DDR PHY and most of DDR IO except two cs and cke output signals , make SDRAM still in self-refresh state to prevent data missing.
- NAND Flash Interface
 - Support 8bits async NAND Flash, up to 4 banks
 - Support 8bits sync Toggle NAND Flash, up to 4 banks
 - Support 8bits sync ONFI NAND Flash, up to 4 banks
 - Support LBA NAND Flash
 - Up to 60bits hardware ECC
 - For DDR NAND Flash, support DLL bypass and 1/4 or 1/8 clock adjust, maximum clock rate is 75MHz
 - For async NAND Flash, support configurable interface timing , maximum data rate is 8bit/cycle
 - Embedded special DMA interface to do data transfer
 - Also support data transfer together with general DMAC1 in SoC system
- eMMC Interface
 - Compatible with standard iNAND interface
 - Support MMC4.41 protocol
 - Provide eMMC boot sequence to receive boot data from external eMMC device
 - Support combined single FIFO(32x32bits) for both transmit and receive operations
 - Support FIFO over-run and under-run prevention by stopping card clock automatically
 - Support CRC generation and error detection
 - Embedded clock frequency division control to provide programmable baud rate
 - Support block size from 1 to 65535Bytes
 - 8bits data bus width
- SD/MMC Interface
 - Compatible with SD3.0, MMC ver4.41
 - Support combined single FIFO(32x32bits) for both transmit and receive operations
 - Support FIFO over-run and under-run prevention by stopping card clock automatically
 - Support CRC generation and error detection
 - Embedded clock frequency division control to provide programmable baud rate
 - Support block size from 1 to 65535Bytes
 - Data bus width is 4bits

1.2.5 System Component

- CRU (clock & reset unit)
 - Support clock gating control for individual components inside RK3028
 - One oscillator with 24MHz clock input and 4 embedded PLLs
 - Up to 2.2GHz clock output for all PLLs
 - Support global soft-reset control for whole SOC, also individual soft-reset for every components
- Timer
 - 3 on-chip 32bits Timers in SoC with interrupt-based operation
 - Provide two operation modes: free-running and user-defined count
 - Support timer work state checkable
 - Fixed 24MHz clock input
- PWM
 - Three on-chip PWMs with interrupt-based operation
 - Programmable 4-bit pre-scalar from apb bus clock
 - Embedded 32-bit timer/counter facility
 - Support single-run or continuous-run PWM mode

- Provides reference mode and output various duty-cycle waveform
- WatchDog
 - 32 bits watchdog counter width
 - Counter clock is from apb bus clock
 - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
 - WDT can perform two types of operations when timeout occurs:
 - ◆ Generate a system reset
 - ◆ First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
 - Programmable reset pulse length
 - Totally 16 defined-ranges of main timeout period
- Bus Architecture
 - 64-bit multi-layer AXI/AHB/APB composite bus architecture
 - 5 embedded AXI interconnect
 - ◆ CPU interconnect with three 64-bits AXI masters, two 64-bits AXI slaves, one 32-bits AHB master and lots of 32-bits AHB/APB slaves
 - ◆ PERI interconnect with two 64-bits AXI masters, one 64-bits AXI slave, one 32-bits AXI slave, four 32-bits AHB masters and lots of 32-bits AHB/APB slaves
 - ◆ Display interconnect with six 64-bits AXI masters and one 32-bits AHB slave
 - ◆ GPU interconnect with one 128-bits AXI master and 64-bits AXI slave ,they are point-to-point AXI-lite architecture
 - ◆ VCODEC interconnect also with one 64-bits AXI master and one 32-bits AHB slave ,they are point-to-point AXI-lite architecture
 - For each interconnect with AXI/AHB/APB composite bus, clocks for AXI/AHB/APB domains are always synchronous, and different integer ratio is supported for them.
 - Flexible different QoS solution to improve the utility of bus bandwidth
- Interrupt Controller
 - Support 3 PPI interrupt source and 76 SPI interrupt sources input from different components inside RK3028
 - Support 16 software-triggered interrupts
 - Input interrupt level is fixed , only high-level sensitive
 - Two interrupt outputs (nFIQ and nIRQ) separately for each Cortex-A9, both are low-level sensitive
 - Support different interrupt priority for each interrupt source, and they are always software-programmable
- DMAC
 - Micro-code programming based DMA
 - The specific instruction set provides flexibility for programming DMA transfers
 - Linked list DMA function is supported to complete scatter-gather transfer
 - Support internal instruction cache
 - Embedded DMA manager thread
 - Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory
 - Signals the occurrence of various DMA events using the interrupt output signals
 - Mapping relationship between each channel and different interrupt outputs is software-programmable
 - Two embedded DMA controller , DMAC0 is for cpu system, DMAC1 is for peri system
 - DMAC0 features:
 - ◆ 6 channels totally
 - ◆ 11 hardware request from peripherals
 - ◆ 2 interrupt output
 - ◆ Dual APB slave interface for register config, designated as secure and non-secure
 - ◆ Support TrustZone technology and programmable secure state for each DMA

channel

- DMAC1 features:
 - ◆ 7 channels totally
 - ◆ 13 hardware request from peripherals
 - ◆ 2 interrupt output
 - ◆ Not support TrustZone technology
- Security system
 - Support TrustZone technology for the following components inside RK3028
 - ◆ Cortex-A9, support security and non-security mode, switch by software
 - ◆ DMAC0, support some dedicated channels work only in security mode
 - ◆ eFuse, only accessed by Cortex-A9 in security mode
 - ◆ Internal memory , part of space is addressed only in security mode, detailed size is software-programmable together with TZMA(TrustZone memory adapter) and TZPC(TrustZone protection controller)

1.2.6 Video CODEC

- Shared internal memory and bus interface for video decoder and encoder[®]
- Video Decoder
 - Real-time video decoder of MPEG-1, MPEG-2, MPEG-4, H.263, H.264 , RV , VP6/VP8 , Sorenson Spark
 - Error detection and concealment support for all video formats
 - Output data format is YUV420 semi-planar, and YUV400(monochrome) is also supported for H.264
 - H.264 up to HP level 4.2 : 1080p@30fps (1920x1088)[®]
 - MPEG-4 up to ASP level 5 : 1080p@30fps (1920x1088)
 - MPEG-2 up to MP : 1080p@30fps (1920x1088)
 - MPEG-1 up to MP : 1080p@30fps (1920x1088)
 - H.263 : 576p@60fps (720x576)
 - Sorenson Spark : 1080p@30fps (1920x1088)
 - RV8/RV9/RV10 : 1080p@30fps (1920x1088)
 - VP6/VP8 : 1080p@30fps (1920x1088)
 - For H.264, Image cropping not supported
 - For MPEG-4, GMC(global motion compensation) not supported
 - For MPEG-4 SP/H.263/Sorenson spark, using a modified H.264 in-loop filter to implement deblocking filter in post-processor unit
- Video Encoder
 - Support video encoder for H.264 ([BP@level4.0](#), [MP@level4.0](#), [HP@level4.0](#)), MVC and VP8
 - Only support I and P slices, not B slices
 - Support error resilience based on constrained intra prediction and slices
 - Input data format :
 - ◆ YCbCr 4:2:0 planar
 - ◆ YCbCr 4:2:0 semi-planar
 - ◆ YCbYCr 4:2:2
 - ◆ CbYCrY 4:2:2 interleaved
 - ◆ RGB444 and BGR444
 - ◆ RGB555 and BGR555
 - ◆ RGB565 and BGR565
 - ◆ RGB888 and BRG888
 - ◆ RGB101010 and BRG101010
 - Image size is from 96x96 to 1920x1088(Full HD)
 - Maximum frame rate is up to 30fps@1920x1080[®]
 - Bit rate supported is from 10Kbps to 20Mbps

1.2.7 JPEG CODEC

- JPEG decoder
 - Input JPEG file : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 sampling formats
 - Output raw image : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar
 - Decoder size is from 48x48 to 8176x8176(66.8Mpixels)
 - Maximum data rate[®] is up to 76million pixels per second

- JPEG encoder
 - Input raw image :
 - ◆ YCbCr 4:2:0 planar
 - ◆ YCbCr 4:2:0 semi-planar
 - ◆ YCbYCr 4:2:2
 - ◆ CbYCrY 4:2:2 interleaved
 - ◆ RGB444 and BGR444
 - ◆ RGB555 and BGR555
 - ◆ RGB565 and BGR565
 - ◆ RGB888 and BRG888
 - ◆ RGB101010 and BRG101010
 - Output JPEG file : JFIF file format 1.02 or Non-progressive JPEG
 - Encoder image size up to 8192x8192(64million pixels) from 96x32
 - Maximum data rate[®] up to 90million pixels per second

1.2.8 Image Enhancement

- Image Post-Processor(embedded inside video decoder)
 - Combined with HD video decoder and JPEG decoder, post-processor can read input data directly from decoder output to reduce bus bandwidth
 - Also work as a stand-alone mode, its input data is from a camera interface or other image data stored in external memory
 - Input data format :
 - ◆ any format generated by video decoder in combined mode
 - ◆ YCbCr 4:2:0 semi-planar
 - ◆ YCbCr 4:2:0 planar
 - ◆ YCbYCr 4:2:2
 - ◆ YCrYCb 4:2:2
 - ◆ CbYCrY 4:2:2
 - ◆ CrYCbY 4:2:2
 - Output data format:
 - ◆ YCbCr 4:2:0 semi-planar
 - ◆ YCbYCr 4:2:2
 - ◆ YCrYCb 4:2:2
 - ◆ CbYCrY 4:2:2
 - ◆ CrYCbY 4:2:2
 - ◆ Fully configurable ARGB channel lengths and locations inside 32bits, such as ARGB8888,RGB565,ARGB4444 etc.
 - Input image size:
 - ◆ Combined mode : from 48x48 to 8176x8176 (66.8Mpixels)
 - ◆ Stand-alone mode : width from 48 to 8176,height from 48 to 8176, and maximum size limited to 16.7Mpixels
 - ◆ Step size is 16 pixels
 - Output image size: from 16x16 to 1920x1088 (horizontal step size 8,vertical step size 2)
 - Support image up-scaling :
 - ◆ Bicubic polynomial interpolation with a four-tap horizontal kernel and a two-tap vertical kernel
 - ◆ Arbitrary non-integer scaling ratio separately for both dimensions
 - ◆ Maximum output width is 3x input width

- ◆ Maximum output height is 3x input height
 - Support image down-scaling:
 - ◆ Arbitrary non-integer scaling ratio separately for both dimensions
 - ◆ Unlimited down-scaling ratio
 - Support YUV to RGB color conversion, compatible with BT.601-5, BT.709 and user definable conversion coefficient
 - Support dithering (2x2 ordered spatial dithering for 4,5,6bit RGB channel precision)
 - Support programmable alpha channel and alpha blending operation with the following overlay input formats:
 - ◆ 8bit alpha +YUV444, big endian channel order with AYUV8888
 - ◆ 8bit alpha +24bit RGB, big endian channel order with ARGB8888
 - Support RGB image contrast / brightness / color saturation adjustment
 - Support image cropping & digital zoom only for JPEG or stand-alone mode
 - Support picture in picture
 - Support image rotation (horizontal flip, vertical flip, rotation 90,180 or 270 degrees)
- Image Post-Processor (IPP)(standalone)
 - memory to memory mode
 - input data format and size
 - ◆ RGB888 : 16x16 to 8191x8191
 - ◆ RGB565 : 16x16 to 8191x8191
 - ◆ YUV422/YUV420 : 16x16 to 8190x8190
 - ◆ YUV444 : 16x16 to 8190x8190
 - pre scaler
 - ◆ integer down-scaling(ratio: 1/2,1/3,1/4,1/5,1/6,1/7,1/8) with linear filter
 - ◆ deinterlace(up to 1080i) to support YUV422&YUV420 input format
 - post scaler
 - ◆ down-scaling with 1/2 ~ 1 arbitrary non-integer ratio
 - ◆ up-scaling with 1~4 arbitrary non-integer ratio
 - ◆ 4-tap vertical, 2-tap horizontal filter
 - ◆ The max output image width of post scaler is 4096
 - Support rotation with 90/180/270 degrees and x-mirror, y-mirror

1.2.9 Graphics Engine

- 2D Graphics Engine :
 - Pixel rate: 500Mpix/s without scale, 250Mpix/s with bilinear scale, 125Mpix/s with bicubic scale.
 - Bit Blit with Stretch Blit, Simple Blit and Filter Blit
 - Color fill with gradient fill , and pattern fill
 - Line drawing with anti-aliasing and specified width
 - High-performance stretch and shrink
 - Monochrome expansion for text rendering
 - ROP2, ROP3, ROP4 full alpha blending and transparency
 - Alpha blending modes including Java 2 Porter-Duff compositing blending rules, chroma key, and pattern mask
 - 8K x 8K raster 2D coordinate system
 - Arbitrary degrees rotation with anti-aliasing on every 2D primitive
 - Programmable bicubic filter to support image scaling
 - Blending, scaling and rotation are supported in one pass for stretch blit
 - Source format:
 - ◆ ABGR8888, XBGR888, ARGB8888, XRGB888
 - ◆ RGB888, RGB565
 - ◆ RGBA5551, RGBA4444
 - ◆ YUV420 planar, YUV420 semi-planar
 - ◆ YUV422 planar, YUV422 semi-planar
 - ◆ BPP8, BPP4, BPP2, BPP1
 - Destination formats :

- ◆ ABGR8888, XBGR8888, ARGB8888, XRGB8888
- ◆ RGB888, RGB565
- ◆ RGBA5551, RGBA4444
- ◆ YUV420 planar, YUV420 semi-planar only in filter and pre-scale mode
- ◆ YUV422 planar, YUV422 semi-planar only in filter and pre-scale mode

1.2.10 Video IN/OUT

- Camera Interface
 - Support up to 5M pixels
 - 8bits CCIR656(PAL/NTSC) interface
 - 8bits raw data interface
 - YUV422 data input format with adjustable YUV sequence
 - YUV422, YUV420 output format with separately Y and UV space
 - Support picture in picture (PIP)
 - Support simple image effects such as Arbitrary(sepia), Negative, Art freeze, Embossing etc.
 - Support static histogram statistics and white balance statistics
 - Support image crop with arbitrary windows
 - Support scale up/down from 1/8 to 8 with arbitrary non-integer ratio
- Display Interface
 - Support RGB, LVDS and HDMI up to 1920x1080
 - Parallel RGB LCD Interface: RGB666(18bits), RGB565(15bits)
 - Serial RGB LCD Interface: 3x8bits with RGB delta support, 3x8bits followed by dummy data, 16bits followed by 8bits
 - MCU LCD Interface: i-8080 with up to 18bits RGB
 - 4 display layers :
 - ◆ One background layer with programmable 24bits color
 - ◆ One video layer (win0)
 - RGB888, ARGB888, RGB565, YUV422, YUV420, AYUV
 - maximum resolution is 1920x1080
 - 1/8 to 8 scaling up/down engine with arbitrary non-integer ratio
 - 256 level alpha blending
 - Support transparency color key
 - Support 3D display
 - ◆ One video layer (win1)
 - RGB888, ARGB888, RGB565, YUV422, YUV420, AYUV
 - maximum resolution is 1920x1080
 - 1/8 to 8 scaling up/down engine with arbitrary non-integer ratio
 - 256 level alpha blending
 - Support transparency color key
 - ◆ Hardware cursor(HWC)
 - 32x32x2bpp
 - 3-color and transparent mode
 - 2-color + transparency + tran_invert mode
 - 16 level alpha blending
 - 3 x 256 x 8 bits display LUTs
 - Win0 and Win1 layer overlay exchangeable
 - Support color space conversion :
 - YUV2RGB(rec601-mpeg/rec601-jpeg/rec709) and RGB2YUV
 - Support replication(16bits to 24bits) and dithering(24bits to 16bits/ 18bits) operation
 - Blank and black display
 - Standby mode
- HDMI
 - Very low power operation, less than 60mW during 1080P HD display
 - HDMI 1.4/1.3/1.2/1.1, HDCP 1.2 and DVI 1.0 standard compliant transmitter

- Supports data rate from 25MHz, 1.65Gbps up to 3.4Gbps over a single channel HDMI support 3D function defined in HDMI 1.4 spec
 - TMDS Tx Drivers with programmable output swing, resistor values and pre-emphasis supports all DTV resolutions including 480i/576i/480p/576p/720p/1080i/1080p
 - Digital video interface supports a pixel size of 24 bits color depth in RGB, YCbCr 4:4:4 or YCbCr 4:2:2 (ITU.656)
 - Multiphase 4MHz fixed bandwidth PLL with low jitter
 - DDC Bus I2C master interface at 3.3V
 - HDCP encryption and decryption engine contains all the necessary logic to encrypt the incoming audio and video data
 - Support HDMI LipSync
 - Lower power operation with optimal power management feature
- LVDS
 - 85MHz clock support
 - 28:4 data channel compression at data rates up to 595 Mbps per hannel
 - Support VGA,SVGA,XGA and single pixel SXGA
 - Comply with the Standard TIA/EIA-644-A LVDS stand
 - Support 8bit format-1, format-2, format-3 display mode, Support 6bit display mode
 - Low power mode

1.2.11 Audio Interface

- Audio Codec
 - Less than -80dB out-of-band Noise
 - 256 x Fs/384 x Fs Master clock rates, up to 24MHz
 - Audio sample rates up to 96KHz
 - ADC SNR 95dB('A'Weighted), THD -85dB at 48KHz, 3.3V
 - ◆ >20mW output power on 32Ω/3.3V
 - ◆ THD+N at 20mW, SNR>95dB with 32Ω load

1.2.12 Connectivity

- SDIO interface
 - Compatible with SDIO 3.0 protocol
 - Support FIFO over-run and under-run prevention by stopping card clock automatically
 - 4bits data bus widths
- High-speed ADC stream interface
 - Support single-channel 8bits/10bits interface
 - DMA-based and interrupt-based operation
 - Support PID filter operation
 - ◆ Combined with high-speed ADC interface to implement filter from original TS data
 - ◆ Provide PID filter up to 64 channels PID simultaneously
 - ◆ Support sync-byte detection in transport packet head
 - ◆ Support packet lost mechanism in condition of limited bandwidth
- SPI Controller
 - One on-chip SPI controller inside RK3028
 - Support serial-master and serial-slave mode, software-configurable
 - DMA-based or interrupt-based operation
 - Embedded two 32x16bits FIFO for TX and RX operation respectively
- Uart Controller
 - 4 on-chip uart controller inside RK3028
 - DMA-based or interrupt-based operation
 - For UART1/UART2/UART3, Embedded two 32Bytes FIFO for TX and RX operation

- respectively
 - For UART0, two 64Bytes FIFOs are embedded for TX/RX operation
 - Support 5bit,6bit,7bit,8bit serial data transmit or receive
 - Standard asynchronous communication bits such as start,stop and parity
 - Support different input clock for uart operation to get up to 4Mbps or other special baud rate
 - Support non-integer clock divides for baud clock generation
 - Auto flow control mode is only for UART0, UART1, UART3
- I2C controller
 - 3 on-chip I2C controller in RK3028
 - Multi-master I2C operation
 - Support 7bits and 10bits address mode
 - Software programmable clock frequency and transfer rate up to 400Kbit/s in the fast mode
 - Serial 8bits oriented and bidirectional data transfers can be made at up to 100Kbit/s in the standard mode
- GPIO
 - 4 groups of GPIO (GPIO0~GPIO3,) , 32 GPIOs per group, totally have 128 GPIOs
 - All of GPIOs can be used to generate interrupt to Cortex-A9
 - All of GPIOs are always in input direction in default after power-on-reset
 - The drive strength for all of GPIOs is software-programmable
- USB Host2.0
 - Supports USB 2.0 protocol and backward compatible with the USB 1.1 protocol
 - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
 - Provides 16 host mode channels
 - Support periodic out channel in host mode
- USB OTG2.0
 - Supports USB 2.0 protocol and backward compatible with the USB 1.1 protocol
 - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
 - Support up to 9 device mode endpoints in addition to control endpoint 0
 - Support up to 6 device mode IN endpoints including control endpoint 0
 - Endpoints 1/3/5/7 can be used only as data IN endpoint
 - Endpoints 2/4/6 can be used only as data OUT endpoint
 - Endpoints 8/9 can be used as data OUT and IN endpoint
 - Provides 9 host mode channels

1.2.13 Others

- SAR-ADC(Successive Approximation Register)
 - 3-channel single-ended 10-bit SAR analog-to-digital converter
 - Conversion speed range is up to 1 MSPS
 - SAR-ADC clock must be less than 1MHz
 - DNL is less than ± 1 LSB , INL is less than ± 2.0 LSB
 - Power down current is about 0.5uA for analog and digital logic
 - Power supply is 1.8V ($\pm 10\%$) for analog interface
- eFuse
 - 256bits (32x8) high-density electrical Fuse
 - Programming condition : VQPS must be 1.5($\pm 10\%$)
 - Program time is about 10us(± 1 us)
 - Read condition : VQPS must be 0V
 - Support standby mode

- Operation Temperature Range
 - -10°C to+85°C
- Operation Voltage Range
 - Core supply: 1.0V ($\pm 10\%$)
 - IO supply : 3.3V ($\pm 10\%$)
- Package Type
 - TFBGA313 (body: 19mm x 19mm ; ball size : 0.4mm ; ball pitch : 0.8mm)
- Power
 - TBA

Notes :^① : *DDR3 are not used simultaneously as well as async and sync ddr and flash*
^② : *In RK3028, Video decoder and encoder are not used simultaneously because of shared internal buffer*
^③ : *Actual maximum frame rate will depend on the clock frequency and system bus performance*
^④ : *Actual maximum data rate will depend on the clock frequency and JPEG compression rate*

1.3 Block Diagram

The following diagram shows the basic block diagram for RK3028.

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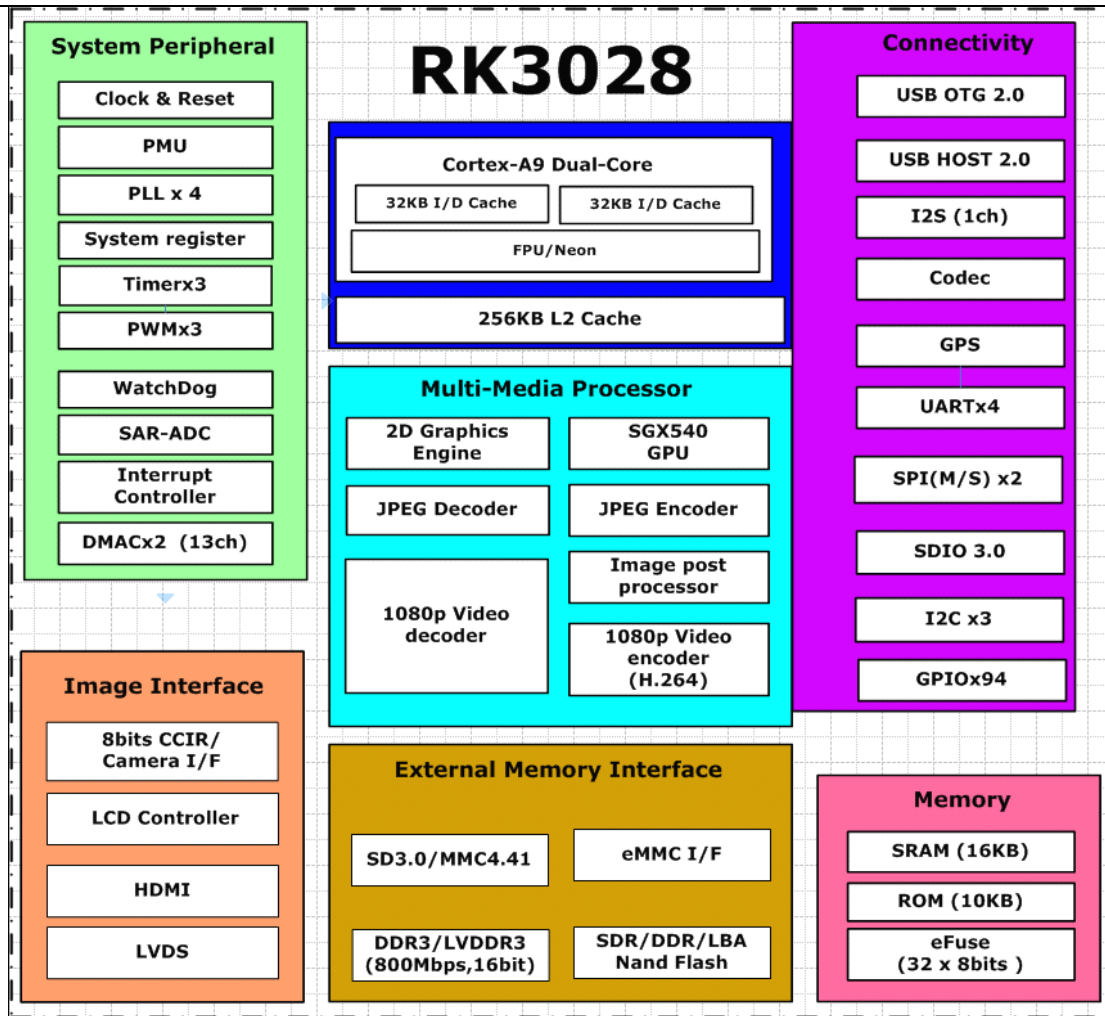


Fig. 01 RK3028 Block Diagram

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