Chapter 2 System Overview

2.1 Address Mapping

RKaudi support to boot from internal bootrom, which support remap function by software programming. Remap is controlled by GRF_SOC_CON0[12].

Addr	IP	Addr	IP	Addr	IP	Addr	IP
	Reserved		MIPI-ANA		Reserved		Reserved
		20038000	16K	10504000		20094000	
	Reserved		HDMI-ANA		NANDC		eFuse
		20034000	16K	10500000	16K	20090000	16K
	Reserved		ACODEC-ANA		GPS		GMAC
		20030000	16K	10400000	1024K	2008C000	16K
	Reserved		DBG		PERI BUS		GPIO3
1013e000		20020000	64K	10300000	1024k	20088000	16K
	Reserved		Reserved		AHB ARB1		GPIO2
1013d000	4K	20010000	64K	1023C000	784K	20084000	16K
	Reserved		DDR_PHY		AHB ARB0		GPIO1
1013c000	8k	2000a000	24K	10234000	32K	20080000	16K
	GIC		GRF		Reserved		GPI0
10138000	16K	20008000	8K	10224000	64K	2007C000	16K
	Reserved		DDR_PCTL		I2S_2ch		DMAC
10130000	32K	20004000	16K	10220000	16K	20078000	16K
	CPU BUS		CRU		eMMC		SPI
10128000	32K	20000000	16K	1021C000	16K	20074000	16K
	Reserved				SDIO		I2C0
10118000	64K			10218000	16K	20070000	16K
	EBC				SDMMC		SARADC
10114000	16k			10214000	16K	2006C000	16K
	Reserved				SFC		UART2
10112000	8K			1020c000	32k	20068000	16K
	MIPI_ctrl				TSP		UART1
10110000	8K			10208000	16k	20064000	16K
	LCDC0				SPDIF		UART0
1010e000	8K			10204000	16k	20060000	16K
	RGA				I2S_8ch		I2C3
1010c000	8K			10200000	16k	2005C000	16K
	CIF				USB HOST OHCI		I2C2
1010a000	8K			101E0000	128K	20058000	16K
	IEP				USB HOST ECHI		I2C1
10108000	8K			101C0000	128K	20054000	16K
	VCODEC				USB OTG		PWM0
10104000	16K			10180000	256K	20050000	16K
	ROM						WDT
10100000	16K					2004C000	16K
	crypto						SCR
100fc000	16K					20048000	16K
	Reserved						TIMER0-5
100b0000	304K					20044000	16K
	PMU						
100a0000	64K						
	GPU						
10090000	64K						
			before remap		after remap		
			IMEM		IMEM		
		10080000	8k	10080000 / 00000000	8k		

Fig. 2-1 RKaudi Address Mapping

2.2 System Boot

RKaudi provides system boot from off-chip devices such as SDMMC card, 8bits async nand flash or toggle nand flash, SPI nor or nand, and eMMC memory.

When boot code is not ready in these devices, also provide system code download into them by USB OTG interface. All of the boot code will be stored in internal bootrom. The following is the whole boot procedure for boot code, which will be stored in bootrom in advance.

The following features are supports.

- Support secure boot mode and non-secure boot mode
- Support system boot from the following device:
  - 8bits Async Nand Flash
  - 8bits Toggle Nand Flash
  - SFC interface
  - eMMC interface
  - SDMMC Card
- Support system code download by USB OTG

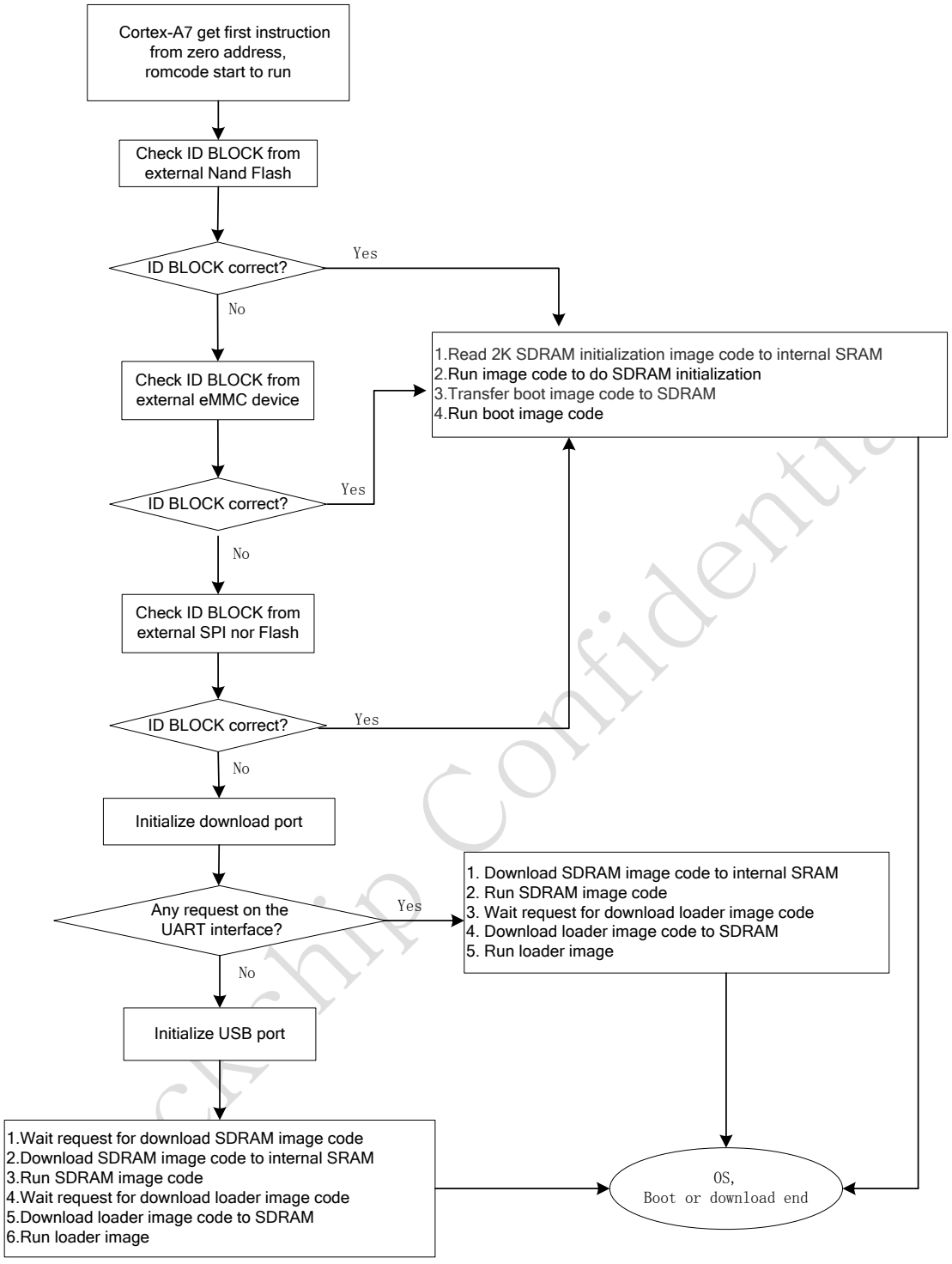

Fig. 2-2 RKaudi boot procedure flow

2.3 System Interrupt connection

RKaudi provides an general interrupt controller(GIC) for Cortex-A7 MPCore processor, which has 112 SPI (shared peripheral interrupts) interrupt sources and 3 PPI(Private peripheral interrupt) interrupt source and separately generates one nIRQ and one nFIQ to CPU. The triggered type for each interrupts is high level sensitive, not programmable. The detailed interrupt sources connection is in the following table. For detailed GIC setting, please refer to

Chapter 12.

Table 2-1 RKaudi Interrupt connection list

	IRQ ID	Source	Polarity
PPI	27	VIRTUAL TIMER	High level
	29	SECURE PHYSICAL TIMER	High level
	30	NON-SECURE PHY TIMER	High level
Source(spi)	32	DMAC2(0)	High level
	33	DMAC2(1)	High level
	34	DDR_PCTL	High level
	35	gpu_irqgp	High level
	36	gpu_irqmmu	High level
	37	gpu_irqpp	High level
	38	Video encoder	High level
	39	Video decoder	High level
	40	CIF	High level
	41	LCDC	High level
	42	USB OTG	High level
	43	USB Host EHCI	High level
	44	gps_irq	High level
	45	gps_timer_irq	High level
	46	SD/MMC0	High level
	47	SDIO	High level
	48	eMMC	High level
	49	SAR-ADC	High level
	50	NandC	High level
	51	I2S_2ch	High level
	52	UART0	High level
	53	UART1	High level
	54	UART2	High level
	55	SPI0	High level
	56	I2C0	High level
	57	I2C1	High level
	58	I2C2	High level
	59	I2C3	High level
	60	Timer0	High level
	61	Timer1	High level
	62	PWM	High level
	63	PMU	High level
	64	USB Host OHCI	High level
	65	MIPI_controller	High level
	66	WDT	High level
	67	otg_bvalid_irq	High level
	68	GPIO0	High level

	69	GPIO1	High level
	70	GPIO2	High level
	71	GPIO3	High level
	72	CRYPTO	High level
	73	reserved	High level
	74	peri_ahb_usb arbiter	High level
	75	reserved	High level
	76	RGA	High level
	77	hdmi	High level
	78	SD/MMC detect	High level
	79	SDIO detect	High level
	80	IEP	High level
	81	EBC	High level
	82	sfc	High level
	83	otg0_id_irq	High level
	84	otg0_linestate_irq	High level
	85	otg1_linestate_irq	High level
	86	sd_detectn_irq	High level
	87	spdif	High level
	88	gmac	High level
	89	gmac_tmc	High level
	90	tsp	High level
	91	timer2	High level
	92	timer3	High level
	93	timer4	High level
	94	timer5	High level
	95	sim_card	High level
	96	acodec_detectn_irq	High level
	97	hevc_mmu_irq	High level
	98	hevc_dec_irq	High level
	99	vpu_mmu_irq	High level
	100	i2s_8ch	High level
	101	Reserved	High level
	102	Reserved	High level
	103	Reserved	High level
	104	Reserved	High level
	105	Reserved	High level
	106	Reserved	High level
	107	Reserved	High level
	108	pmuirq_a7_0	High level
	109	pmuirq_a7_1	High level
	110	pmuirq_a7_2	High level

	111	pmuirq_a7_3	High level
	112	axierrirq	High level

2.4 System DMA hardware request connection

RKaudi provides one DMA controller: DMAC inside peripheral system. 15 hardware request ports are used in DMAC_PERI, the trigger type for each of them is high level, not programmable. For detailed descriptions of DMAC, please refer to Chapter 11.

Table 2-2 RKaudi DMAC_BUS Hardware request connection list

Req Number	Source	Polarity
0	I2S_2ch tx	High level
1	I2S_2ch rx	High level
2	Uart0 tx	High level
3	Uart0 rx	High level
4	Uart1 tx	High level
5	Uart1 rx	High level
6	Uart2 tx	High level
7	Uart2 rx	High level
8	SPI tx	High level
9	SPI rx	High level
10	SD/MMC	High level
11	SDIO	High level
12	eMMC	High level
13	SPDIF	High level
14	I2S_8ch tx	High level
15	I2S_8ch rx	High level