Chapter 19 RGA1_plus

19.1 Overview

RGA is a separate 2D raster graphic acceleration unit. It accelerates 2D graphics operations, such as point/line drawing, image scaling, rotation, BitBLT, alpha blending and image blur/sharpness.

19.1.1 Features

- **Data format**
  - Input data: ARGB/RGB888/RGB565/YUV420/YUV422
  - Output data: ARGB/RGB888/RGB565 (YUV420/YUV422 for blur/sharpness);
  - Pixel Format conversion, BT.601/BT.709
  - Dither operation
  - Max resolution: 8192x8192 source image, 2048x2048 frame buffer
- **Scaling**
  - Down-scaling and up-scaling
  - Three sampling modes: Nearest sampling (Stretched BitBLT), Bi-linear filter or Bi-cubic filter
  - Arbitrary non-integer scaling ratio, from 1/2 to 8
  - Average filter pre-scaling (2's Down-scaling bypass path, not avaliable with other 2D operation)
- **Rotation**
  - Arbitrary rotation, minimum 1 degree step
  - No per-pixel alpha in arbitrary ratation (without 90, 180, 270)
  - x-mirror, y-mirror
- **BitBLT**
  - Block transfer
  - Color palette (with transparency mode)/Color fill
  - Transparency mode (color keying/stencil test, specified value/range)
- **Alpha Blending**
  - Per-pixel/user-specified alpha blending (Porter-duff alpha support)
  - Fading
  - Anti-aliasing (for rotation)
- **Raster operation**
  - ROP2/ROP3/ROP4
  - No ROP in arbitrary rotation (except 90/180/270 degree)
- **YUV_Output**
  - Output data: YUV422SP/YUV420SP, not used in Pre_scaling Line/point drawing and Blur/sharp, Alpha and ROP.
  - ColorPalette alpha 1/8bit mode
- **RW_Align**
  - AXI read/write can be DDR-Align in Line scan mode, high performance.
- ~~**Line/Point drawing**~~
  - ~~Bresonham algorithm, Specified width~~
  - ~~Anti-aliasing~~
- ~~**Blur/sharpness**~~
  - ~~Bypass post processing path (not avaliable with other 2D operation)~~
  - ~~Tile_based~~

19.2 Block Diagram

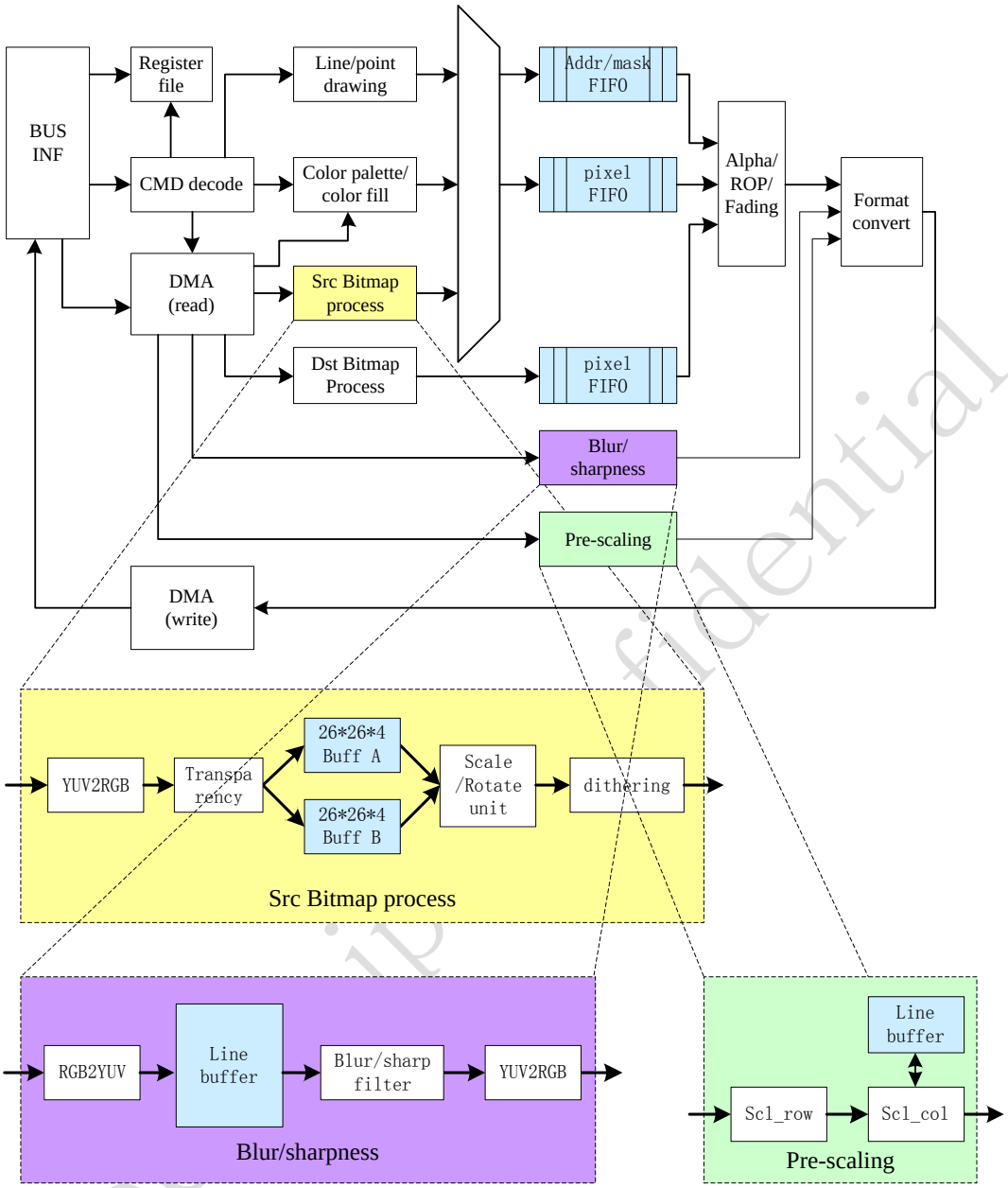

Fig. 19-1 RGA Block Diagram

19.3 Function Description

19.3.1 Data Format

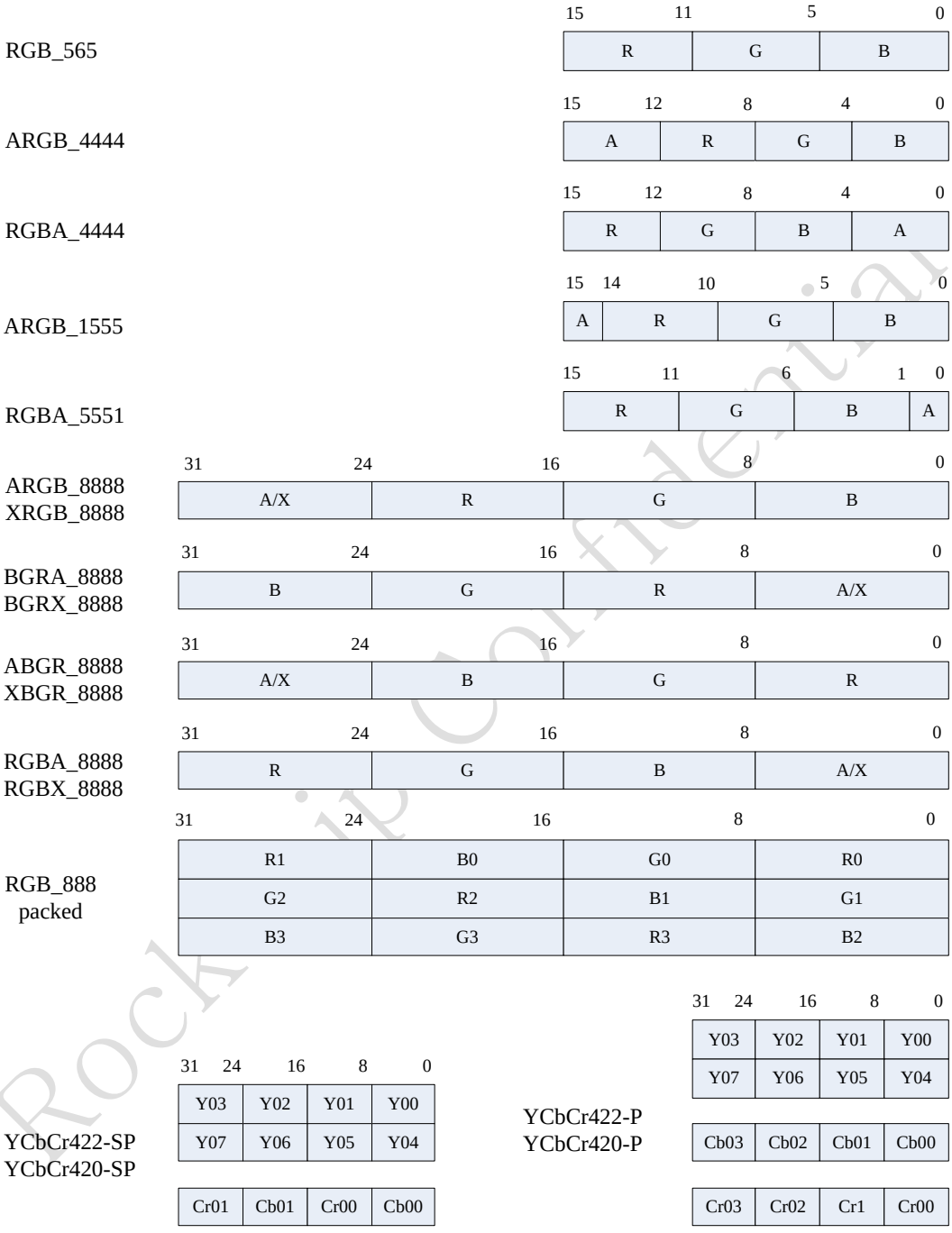

Fig. 19-2 RGA Input Data Format

All input datas (defined by SRC_IN_FMT/DST_IN_FMT) are converted to ABGR8888. The results are converted to the output data format (defined by DST_OUT_FMT).

19.3.2 Dithering

There could have dithering operation for source image when the source image format is not RGB565 and the destination format is RGB565.

The down-dithering is done using Dither Matrix.

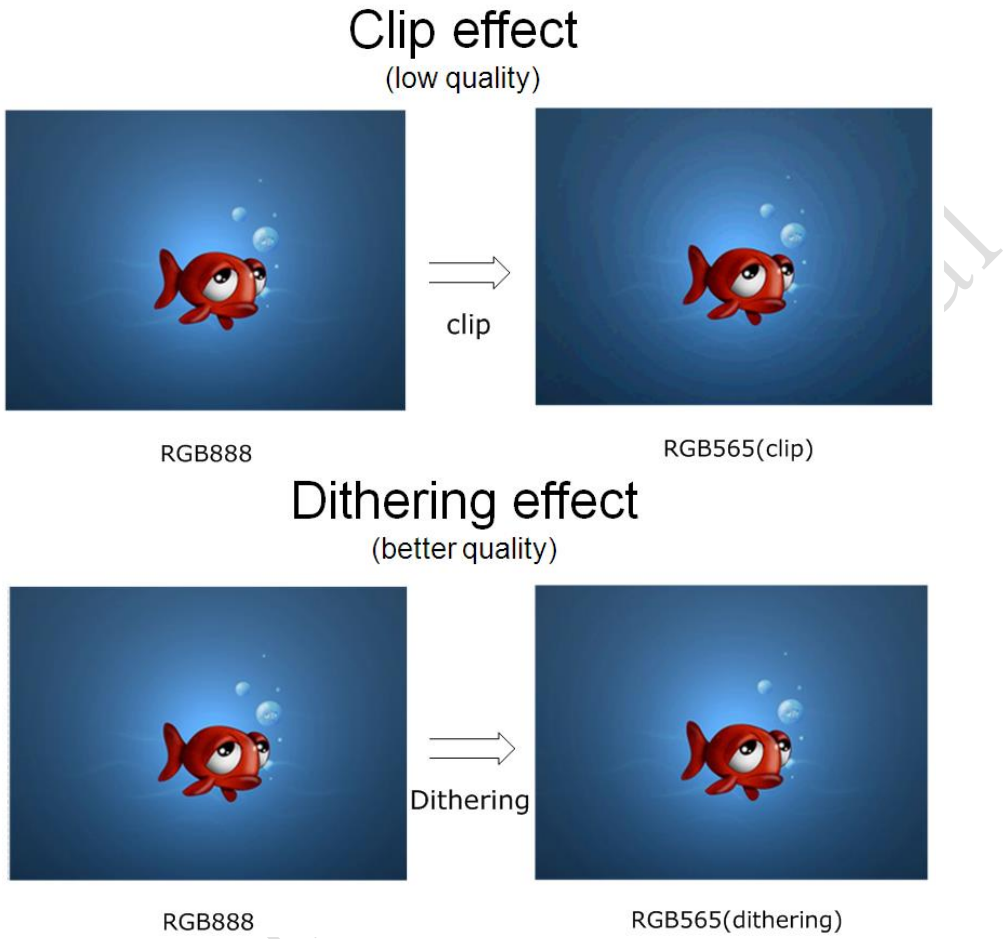

Fig. 19-3 RGA Dither effect

19.3.3 Scaling

The scaling operation is the imageresizing processing of source image. Scaling is done base on ARGB8888 format.

There are three sampling modes: Nearest sampling (Stretched BitBLT), Bi-linear filter or Bi-cubic filter.

19.3.4 Rotation

Arbitrary rotation and x-mirror, y-mirror operation is supported in RGA. The rotation operation is combined with scaling operation.

Alpha is avaliable only if there is no rotation or 90-degree/180-degree /270-degree rotation or x-mirror/y-mirror. Anti-aliasing is done by the alpha blending of the boundary pixels.

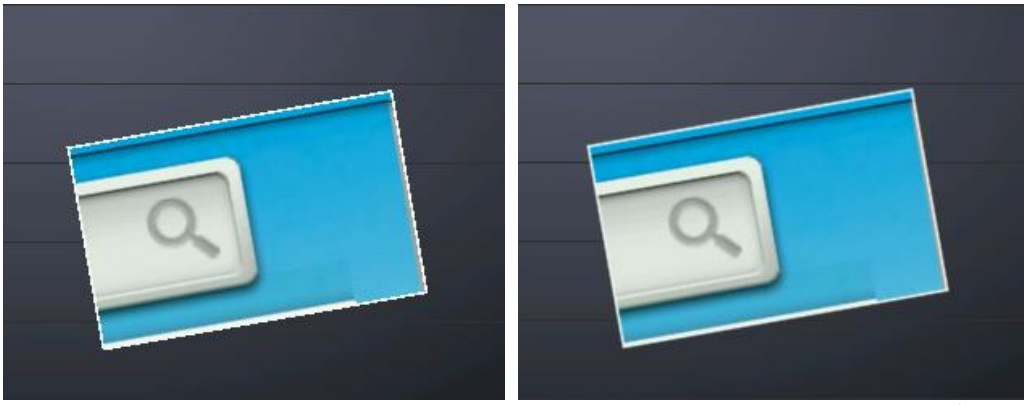

Fig. 19-4 RGA Rotation AA effect

19.3.5 Bitmap Block Transfer

BitBlt is a computer graphics operation in which several bitmaps are combined into one using a raster operator. The bitmap rectangular block is transfered from source frame buffer to destination frame buffer. There are three bitmap block transfer type: bitmap block transfer (RGB/YCbCr), color expansion, and solid fill.

RGA also supports transparency mode in BitBLT. There are two transparency modes (stencil test): normal mode and inverted mode.

There are 4 enable control bits for ARGB color channel for stencil test, which can be set independently.

1. Transparency mode

(1) Normal Stencil test (Color keying)

Pixels with the same color or in the range of user-specified colors are discarded.

(2) Inverted stencil test

Pixels with the different color or out the range of user-specified colors are discarded.

2. Color palette

1bpp/2bpp/4bpp/8bpp palette data formats are support in RGA source layer. 1bpp color expansion can be BG color and FG color, transparency and FG color according the alpha enable bit. There is a 256x25bit LUT in RGA for 2bpp/4bpp/8bpp color palette. The following is the table of 8bpp with alpha enable bit in the MSB.

Table 19-1 RGA 8bpp color palette LUT

INDEX\ Bit Pos.	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00H	AEN	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
01H	AEN	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
.....	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…
FFH	AEN	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0

3. Color fill

Two modes of color fill can be done by RGA: solid fill and gradient fill.

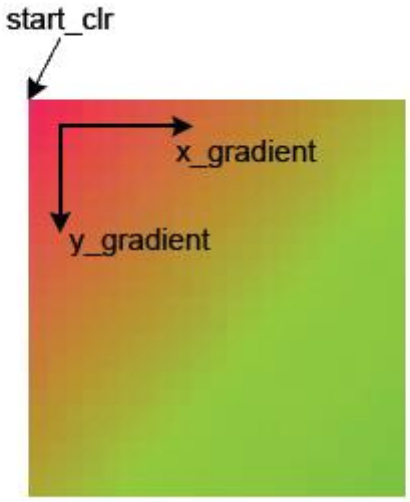

Fig. 19-5 RGA Gradient Fill

Gradient fill using following equations for ARGB calculation of every pixel in different coordinary.

A_cur = (A_start + x*x_A_gradient) +y*y_A_gradient;
R_cur = (R_start + x*x_R_gradient) +y*y_R_gradient;
G_cur = (G_start + x*x_G_gradient) +y*y_G_gradient;
B_cur = (B_start + x*x_B_gradient) +y*y_B_gradient;

A_start, R_start, G_start, B_start is the ARGB value of start point. There are four pairs of values for horizontal and vertical gradient. Saturation operation could be enabled or disabled if the color overflows 255 or underflows 0.

19.3.6 Alpha Blending

Alpha blending is devided to two stages. The first stage is mix alpha

(per-pixel/user-specified), where Porter-Duff (pre-multiplied) alpha is supported. The second stage is fading.

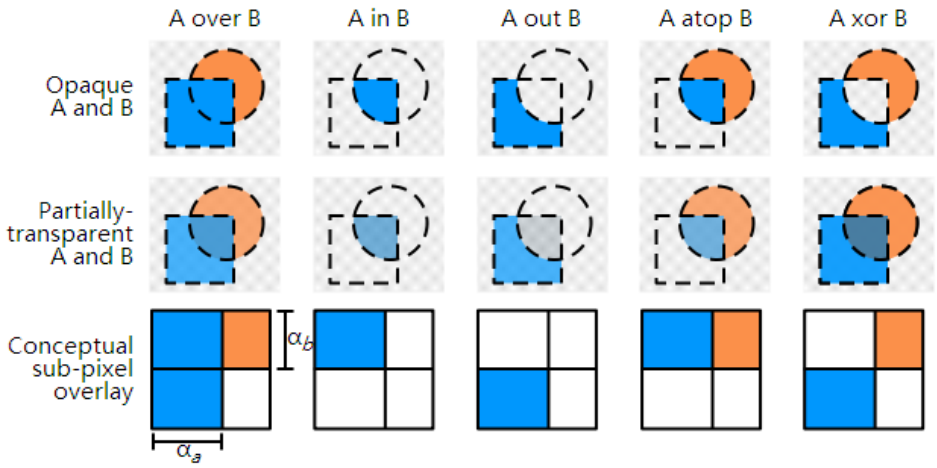

Fig. 19-6 RGA Alpha blanding

1. Mix (per-pixel/user-specified) alpha

$$data = (source \times (ALPHA + 1) + destination \times (255 - ALPHA)) >> 8$$

2. Porter-Duff

Porter-Duff alpha is a premultiplied alpha between two layers。

Porter-Duff formula:

$$C_r = C_s * F_s + C_d * F_d$$

$$A_r = A_s * F_s + A_d * F_d$$

(C – color, A – alpha, s – source, d – destination, r – result, F – factor)

There are 12 diferent mix types for Fs and Fd factor.

Table 19-2 RGA Porter-Duff alpha factor

NO.	type	Source factor	Destination factor
1	CLEAR	0	0
2	SRC	1	0
3	DST	0	1
4	SRC OVER	1	(1-As)
5	DST OVER	(1-Ad)	1
6	SRC IN	Ad	0
7	DST IN	0	As
8	SRC OUT	(1-Ad)	0
9	DST OUT	0	(1-As)
10	SRC ATOP	Ad	(1-As)
11	DST ATOP	(1-Ad)	As
12	XOR	(1-Ad)	(1-As)

3. Fading

$$data = ((source \times (ALPHA + 1) >> 8) + fading\_offset$$

19.3.7 Raster Operation (ROP)

Raster operation (ROP) is a Boolean operation between operands, which involve AND, OR, XOR, and NOT operations. For ROP2, operands are P (select pan) and D (Destination bitmap). For ROP3, operands are P (pattern), S (source bitmap) and D (Destination bitmap). For ROP4, operands are P (pattern), S (source bitmap), D (Destination bitmap) and MASK.

Table 19-3 RGA ROP Boolean operations

Operator	Meaning
a	Bitwise AND
n	Bitwise NOT (inverse)
o	Bitwise OR
x	Bitwise exclusive OR (XOR)

~~19.3.8 Line/Point Drawing~~

Line operation draws a line, which coordinates for two points are given: start point and end point. The end point can be drawn or not drawn. Lines are rendered using the Bresenham algorithm.

The width of the line can be user-specified. Anti-aliasing is done to improve the display quality.

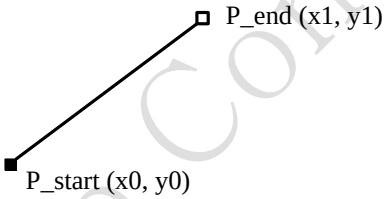

Fig. 19-7 RGA Line drawing

~~19.3.9 Blur/sharpness~~

Blur and sharpness is a post processing for destination image. A 8x8 matrix filter is used.

Blur/sharpness unit is also a bypass unit, which is not avaliable when doing other 2D graphic operations.

19.4 Register Description

19.4.1 Register Summary

Name	Offset	Size	Reset Value	Description

Name	Offset	Size	Reset Value	Description
RGA_SYS_CTRL	0x0000	W	0x00000000	RGA system control register
RGA_CMD_CTRL	0x0004	W	0x00000000	RGA command code control
RGA_CMD_ADDR	0x0008	W	0x00000000	RGA command codes start address register
RGA_STATUS	0x000c	W	0x00000000	RGA status register
RGA_INT	0x0010	W	0x00000000	RGA interrupt register
RGA_AXI_ID	0x0014	W	0x49850210	RGA AXI ID setting register
RGA_MMU_STA_CTRL	0x0018	W	0x00000000	RGA MMU statistic ctrl
RGA_MMU_STA	0x001c	W	0x00000000	RGA MMU statistic data
RGA_WORK_CNT	0x0020	W	0x00000000	RGA work cycle counter
RGA_VERSION	0x0028	W	0x02018632	RGA version num
RGA_MODE_CTRL	0x0100	W	0x00000000	RGA mode control register
RGA_SRC_Y_MST	0x0104	W	0x00000000	Source image Y/RGB/line drawing start addr
RGA_SRC_CB_MST	0x0108	W	0x00000000	Source image Cb/Cbr start addr
RGA_SRC_CR_MST	0x010c	W	0x00000000	Source image Cr/color palette start addr
RGA_SRC_VIR_INFO	0x0110	W	0x00000000	Source image virtual width
RGA_SRC_ACT_INFO	0x0114	W	0x00000000	Source image active width/height
RGA_SRC_X_PARA	0x0118	W	0x00000000	Source image horizontal scaling/rotation parameter
RGA_SRC_Y_PARA	0x011c	W	0x00000000	Source image vertical scaling/rotation parameter
RGA_SRC_TILE_XINFO	0x0120	W	0x00000000	Source tile start point coordinate,Source tile width
RGA_SRC_TILE_YINFO	0x0124	W	0x00000000	Source tile start point coordinate,Source tile height
RGA_SRC_TILE_H_INCR	0x0128	W	0x00000000	Source tile horizontal X/Y increment value
RGA_SRC_TILE_V_INCR	0x012c	W	0x00000000	Source tile vertical X/Y increment value
RGA_SRC_TILE_OFFSETX	0x0130	W	0x00000000	Source tile start point x for DST tile start point remap
RGA_SRC_TILE_OFFSETY	0x0134	W	0x00000000	Source tile start point y for DST tile start point remap
RGA_SRC_BG_COLOR	0x0138	W	0x00000000	Source image background color

Name	Offset	Size	Reset Value	Description
RGA_SRC_FG_COLOR	0x013c	W	0x00000000	Source image foreground color
RGA_SRC_TR_COLOR0	0x0140	W	0x00000000	Source image transparency color min value
RGA_CP_GR_A	0x0140	W	0x00000000	RGA color gradient fill step register (color fill mode)
RGA_SRC_TR_COLOR1	0x0144	W	0x00000000	Source image transparency color max value,Color gradient fill st
RGA_CP_GR_B	0x0144	W	0x00000000	RGA color gradient fill step register (color fill mode)
RGA_LINE_DRAW	0x0148	W	0x00000000	Point/line drawing setting
RGA_PAT_ST_POINT	0x0148	W	0x00000000	RGA pattern start point
RGA_DST_MST	0x014c	W	0x00000000	Destination image start addr
RGA_DST_VIR_INFO	0x0150	W	0x00000000	Destination image virtual width
RGA_DST_CTR_INFO	0x0154	W	0x00000000	Destination image control window active width/height
RGA_ALPHA_CON	0x0158	W	0x00000000	Alpha blending/ROP mode register
RGA_PAT_CON	0x015c	W	0x00000000	Pattern size/offset
RGA_DST_VIR_WIDTH	0x015c	W	0x00000000	Register0000 Abstract
RGA_ROP_CON0	0x0160	W	0x00000000	Raster operation code0 control register
RGA_CP_GR_G	0x0160	W	0x00000000	Color gradient fill step of green
RGA_PRESCL_CB_MST	0x0160	W	0x00000000	RGA pre-scale Cb destination start addr
RGA_ROP_CON1	0x0164	W	0x00000000	Raster operation code1 control register
RGA_CP_GR_R	0x0164	W	0x00000000	Color gradient fill step of red
RGA_PRESCL_CR_MST	0x0164	W	0x00000000	RGA pre-scale Cr destination start addr
RGA_MMU_CTRL	0x0168	W	0x00000000	MMU control register
RGA_MMU_TLB	0x016c	W	0x00000000	RGA MMU TLB base address
RGA_YUV_OUT_CFG	0x0170	W	0x00000000	Destination YUV output configuration
RGA_DST_UV_MST	0x0174	W	0x00000000	Destination image UV start add

*Notes: Size : **B** - Byte (8 bits) access, **HW** - Half WORD (16 bits) access, **W** -WORD (32 bits) access*

19.4.2 Detail Register Description

RGA_SYS_CTRL
Address: Operational Base + offset (0x0000)
RGA system control register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	acg_en RGA auto clock gating enable bit 0：disable 1：enable
2	RW	0x0	cmd_mode RGA command mode 0：slave mode 1：master mode
1	W1C	0x0	op_st RGA operation start bit Only used in passive (slave) control mode
0	W1C	0x0	soft_reset RGA soft reset write '1' to this would reset the RGA engine except config registers.

RGA_CMD_CTRL
Address: Operational Base + offset (0x0004)
RGA command code control

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:3	RW	0x000	cmd_incr_num RGA command increment number
2	RW	0x0	cmd_stop RGA command stop mode Command execution would stop after the current graphic operation finish if set this bit to '1'.
1	W1C	0x0	cmd_incr_valid RGA command increment valid (Auto cleared) When setting this bit, 1. The total cmd number would increase by the RGA_INCR_CMD_NUM. 2. RGA would continue running if idle.
0	W1C	0x0	cmd_line_fet_st RGA command line fetch start (command line reset) (Auto cleared) When fetch start, the total cmd number would reset to RGA_INCR_CMD_NUM.

RGA_CMD_ADDR
Address: Operational Base + offset (0x0008)

RGA command codes start address register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cmd_addr RGA command codes start address

RGA_STATUS

Address: Operational Base + offset (0x000c)

RGA status register

Bit	Attr	Reset Value	Description
31:20	RO	0x000	cmd_total_num RGA command total number
19:8	RO	0x000	cur_cmd_num RGA current command number
7:1	RO	0x0	reserved
0	RO	0x0	engine_status RGA engine status 0: idle 1: working

RGA_INT

Address: Operational Base + offset (0x0010)

RGA interrupt register

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10	RW	0x0	all_cmd_finish_int_en All command finished interrupt enable
9	RW	0x0	mmu_int_en MMU interrupt enable
8	RW	0x0	error_int_en Error interrupt enable
7	W1C	0x0	cur_cmd_finish_int_clr Current command finished interrupt clear(auto clear)
6	W1C	0x0	all_cmd_finish_int_clr All command finished interrupt clear(auto clear)
5	W1C	0x0	mmu_int_clr MMU interrupt clear(auto clear)
4	W1C	0x0	error_int_clr Error interrupt clear(auto clear)

Bit	Attr	Reset Value	Description
3	RO	0x0	cur_cmd_finish_int_flag Current command finished interrupt flag
2	RO	0x0	all_cmd_finish_int_flag All command finished interrupt flag
1	RO	0x0	mmu_int_flag MMU interrupt flag
0	RO	0x0	error_int_flag Error interrupt flag

RGA_AXI_ID

Address: Operational Base + offset (0x0014)

RGA AXI ID setting register

Bit	Attr	Reset Value	Description
31:30	RW	0x1	mmu_rid MMU read channel address maping axi bus ID Note: Don't use the same ID with RGA axi bus ID.2'b11, [31:30].
29:28	RW	0x0	mmu_wid MMU write channel address maping axi bus ID Note: Don't use the same ID with RGA axi bus ID.2'b11, [29:28].
27:24	RW	0x9	mask_rid mask read AXI ID
23:20	RW	0x8	cmd_rid CMD fetch AXI ID
19:16	RW	0x5	dst_wid DST write AXI ID
15:12	RW	0x4	dst_rid DST/LUT/PAT read AXI ID
11:8	RW	0x2	src_cr_rid SRC Cr read AXI ID
7:4	RW	0x1	src_cb_rid SRC Cb read AXI ID
3:0	RW	0x0	src_yrgb_rid SRC YRGB read AXI ID

RGA_MMU_STA_CTRL

Address: Operational Base + offset (0x0018)

RGA MMU statistic ctrl

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	W1C	0x0	mmu_sta_cnt_clr TLB statistic counter clear(auto clear) 0: no clear 1: clear After be set to 1, this bit will clear by itself 1 cycle later
2	W1C	0x0	mmu_sta_resume TLB statistic resume(auto clear) After be set to 1, this bit will clear by itself 1 cycle later.
1	RW	0x0	mmu_sta_pause TLB statistic pause Note: before reading MMU_TLB_STATISTIC, this bit must be set to 1.
0	RW	0x0	mmu_sta_en TLB statistic enable 0: disable 1: enable

RGA_MMU_STA
Address: Operational Base + offset (0x001c)
RGA MMU statistic data

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	tlb_miss_sta_cnt TLB miss statistic counter
15:0	RO	0x0000	tlb_hit_sta_cnt TLB hit statistic counter

RGA_WORK_CNT
Address: Operational Base + offset (0x0020)
RGA work cycle counter

Bit	Attr	Reset Value	Description
31:27	RO	0x0000	Reserved
26:0	RO	0x0000	Rga_work_cnt Rga work cycle counter

RGA_VERSION
Address: Operational Base + offset (0x0028)
RGA Version num

Bit	Attr	Reset Value	Description
31:24	RO	0x0002	MAJOR: RGA1: 1; RGA1_Plus: 2; RGA2: 3; RGA2_Lite: 4;
23:16	RO	0x0001	MINOR; 1: for AUDI;

Bit	Attr	Reset Value	Description
15:0	RO	0x8632	ASCII code: mmip svn num=8632

RGA_MODE_CTRL

Address: Operational Base + offset (0x0100)

RGA mode control register

Bit	Attr	Reset Value	Description
31	RW	0x0	alpha_source_sel alpha select for alpha mix mode 0: SRC alpha: SRC*As+DST*(1-As) 1: DST alpha: SRC*(1-Ad)+DST*Ad
30	RW	0x0	alpha_zero_key_mode ARGB888 alpha zero key mode 0x000000 would be changed to 0x000100(RGB888)/0x0020(RGB565)for ARGB888 to RGBX/RGB565 color key 0: disable 1: enable
29	RW	0x0	cur_cmd_finish_int_en Current command finished interrupt enable
28	RW	0x0	endian_swap Color palette endian swap 0: big endian 1: little endian
27	RW	0x0	dst_alpha_swap Destination bitmap data alpha swap 0: ABGR 1: BGRA
26	RW	0x0	dst_rb_swap Destination bitmap data RB swap 0: BGR 1: RGB
25	RW	0x0	dst_rgb_pack Destination bitmap BGR packed 0: ABGR 1: BGR packed
24:23	RW	0x0	dst_data_fmt Destination bitmap data format(Collor fill/ROP pattern data format) 00: XBGR888/ABGR888 01: RGB565 10: ARGB1555 11: ARGB4444
22	RW	0x0	pat_mode Color fill/ROP4 pattern 0: solid color 1: pattern color

Bit	Attr	Reset Value	Description
21:20	RW	0x0	src_filter_type SRC rotation/mirror mode[3:2]: filter type 00: nearest neighbor 01: bi-linear 10: bi-cubic
19:18	RW	0x0	src_rotate_mode SRC rotation/mirror mode[1:0] 00: bypass 01: rotation 10: x mirror 11: y mirror
17:14	RW	0x0	src_trans_en Source transparency enable bits [3]: A value stencil test enable bit [2]: B value stencil test enable bit [1]: G value stencil test enable bit [0]: R value stencil test enable bit
13	RW	0x0	src_trans_mode Source color key mode 0: normal stencil test 1: inverted stencil test
12:11	RW	0x0	src_yuv2rgb_mode Source bitmap YUV2RGB conversion mode 00: BT.601-MPEG 01: BT.601-JPEG 10: BT.709 11: BT.601-MPEG
10	RW	0x0	src_uv_swap Source Cb-Cr swap 0: CrCb 1: CbCr
9	RW	0x0	src_alpha_swap Source bitmap data alpha swap 0: ABGR 1: BGRA
8	RW	0x0	src_rb_swap Source bitmap data RB swap 0: BGR 1: RGB
7:4	RW	0x0	src_data_fmt Source bitmap data format 0000: XBGR888/ABGR888 0001: RGB565 0010: ARGB1555 0011: ARGB4444 0100: YUV422SP 0101: YUV422P 0110: YUV420SP 0111: YUV420P 1000: 1BPP (color palette) 1001: 2BPP (color palette) 1010: 4BPP (color palette) 1011: 8BPP (color palette)

Bit	Attr	Reset Value	Description
3	RW	0x0	src_rga_pack Source bitmap RGB packed 0: ABGR 1: BGR packed
2:0	RW	0x0	render_mode RGA 2D render mode 000: Bitblt 001: Color palette 010: Color fill（pattern fill） 011: Line/point drawing 100: Blur/sharp filter 101: Pre-scaling 110: Update palette LUT 111: Update pattern buffer

RGA_SRC_Y_MST
Address: Operational Base + offset (0x0104)
Source image Y/RGB/line drawing start addr

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_y_mst RGA source image Y/RGB start address register

RGA_SRC_CB_MST
Address: Operational Base + offset (0x0108)
Source image Cb/Cbr start addr

Bit	Attr	Reset Value	Description

31:0	RW	0x00000000	src_cb_mst
			RGA source image Cb/Cbr start address register
			source image Cb start address(YUV422/420-P);
			source image Cb/Cr start address(YUV422/420-SP);
			mask start address in ROP4 mode

RGA_SRC_CR_MST
Address: Operational Base + offset (0x010c)
Source image Cr/color palette start addr

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_cr_mst source image Cr start address(YUV422/420-P)

RGA_SRC_VIR_INFO
Address: Operational Base + offset (0x0110)

Source image virtual width

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:0	RW	0x0000	src_vir_stride source image virtual stride(words)

RGA_SRC_ACT_INFO

Address: Operational Base + offset (0x0114)

Source image active width/height

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	src_act_height source image active height
15:13	RO	0x0	reserved
12:0	RW	0x0000	src_act_width source image active width

RGA_SRC_X_PARA

Address: Operational Base + offset (0x0118)

Source image horizontal scaling/rotation parameter

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	src_h_para1 Source image horizontal scaling/rotation parameter1 sin(a)/ZoomX (signed 2.14)
15:0	RW	0x0000	src_h_para0 Source image horizontal scaling/rotation parameter0 cos(a)/ZoomX (signed 2.14)

RGA_SRC_Y_PARA

Address: Operational Base + offset (0x011c)

Source image vertical scaling/rotation parameter

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	src_v_para1 Source image vertical scaling/rotation parameter1 cos(a)/ZoomY (signed 2.14)
15:0	RW	0x0000	src_v_para0 Source image vertical scaling/rotation parameter0 -sin(a)/ZoomY (signed 2.14)

RGA_SRC_TILE_XINFO

Address: Operational Base + offset (0x0120)
Source tile start point coordinate,Source tile width

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	src_tile_width Source tile width (unsigned 5.11)
15:0	RW	0x0000	src_tile_xst Source tile start point x coordinate (signed13.3)

RGA_SRC_TILE_YINFO
Address: Operational Base + offset (0x0124)
Source tile start point coordinate,Source tile height

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	src_tile_height Source tile height (unsigned 5.11)
15:0	RW	0x0000	src_tile_yst Source tile start point y coordinate (signed13.3)

RGA_SRC_TILE_H_INCR
Address: Operational Base + offset (0x0128)
Source tile horizontal X/Y increment value

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	src_h_tile_y_incr Source horizontal tile Y increment value (signed 6.10)
15:0	RW	0x0000	src_h_tile_x_incr Source horizontal tile X increment value (signed 6.10)

RGA_SRC_TILE_V_INCR
Address: Operational Base + offset (0x012c)
Source tile vertical X/Y increment value

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	src_v_tile_y_incr Source vertical tile Y increment value (signed 6.10)
15:0	RW	0x0000	src_v_tile_x_incr Source vertical tile X increment value (signed 6.10)

RGA_SRC_TILE_OFFSETX
Address: Operational Base + offset (0x0130)
Source tile start point x for DST tile start point remap

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x00000	src_tile_xoff Source tile start point offset X for DST tile start point remap(unsigned 5.14)

RGA_SRC_TILE_OFFSETY
Address: Operational Base + offset (0x0134)
Source tile start point y for DST tile start point remap

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RW	0x00000	src_tile_yoff Source tile start point offset Y for DST tile start point remap(unsigned 5.14)

RGA_SRC_BG_COLOR
Address: Operational Base + offset (0x0138)
Source image background color

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_bg_color Source image background color "0" bit color for mono expansion.

RGA_SRC_FG_COLOR
Address: Operational Base + offset (0x013c)
Source image foreground color

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_fg_color Source image foreground color "1" bit color for mono expansion. Line/point color, Color fill color, Pan color

RGA_SRC_TR_COLOR0
Address: Operational Base + offset (0x0140)
Source image transparency color min value

Bit	Attr	Reset Value	Description
31:24	RW	0x00	src_trans_a_min source image transparency color A min value
23:16	RW	0x00	src_trans_b_min source image transparency color B min value

Bit	Attr	Reset Value	Description
15:8	RW	0x00	src_trans_g_min source image transparency color G min value
7:0	RW	0x00	src_trans_r_min source image transparency color R min value

RGA_CP_GR_A
Address: Operational Base + offset (0x0140)
RGA color gradient fill step register (color fill mode)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	a_gr_y Y gradient value of Alpha (signed 8.8)
15:0	RW	0x0000	a_gr_x X gradient value of Alpha (signed 8.8)

RGA_SRC_TR_COLOR1
Address: Operational Base + offset (0x0144)
Source image transparency color max value,Color gradient fill st

Bit	Attr	Reset Value	Description
31:24	RW	0x00	src_trans_a_max source image transparency color A max value
23:16	RW	0x00	src_trans_b_max source image transparency color B max value
15:8	RW	0x00	src_trans_g_max source image transparency color G max value
7:0	RW	0x00	src_trans_r_max source image transparency color R max value

RGA_CP_GR_B
Address: Operational Base + offset (0x0144)
RGA color gradient fill step register (color fill mode)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	b_gr_y Y gradient value of Blue (signed 8.8)
15:0	RW	0x0000	b_gr_x X gradient value of Blue (signed 8.8)

~~**RGA_LINE_DRAW**~~
Address: Operational Base + offset (0x0148)

Point/line drawing setting

Bit	Attr	Reset Value	Description
31	RW	0x0	line_draw_aa Line drawing Anti-alising operation 0: disable 1: enable
30	RW	0x0	line_draw_last_point_en Line drawing last point drawing 0: Don't draw 1: Draw
29	RW	0x0	line_draw_semi_dir Direction of semi-major axis 0: Increase 1: Decrease
28	RW	0x0	line_draw_major_dir Direction of major axis 0: Increase 1: Decrease
27:16	RW	0x000	line_draw_incr Line drawing X/Y delta step (unsigned 0.12) X delta step value if X is major axis; Y delta step value if Y is major axis;
15:12	RW	0x0	line_draw_width Line width (1~16 pixel)
11	RW	0x0	line_draw_dir Line drawing direction 0: X is major axis 1: Y is major axis
10:0	RW	0x000	line_draw_length Line drawing X/Y length of line (unigned 11) X length if X is major axis Y length if Y is major axis

RGA_PAT_ST_POINT

Address: Operational Base + offset (0x0148)

RGA pattern start point

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	pat_st_point Pattern start point in pattern ram

RGA_DST_MST

Address: Operational Base + offset (0x014c)

Destination image start addr

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_mst destiniation image RGB start address source image color palette table start address(color palette mode)

RGA_DST_VIR_INFO
Address: Operational Base + offset (0x0150)
Destination image virtual width

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	mask_vir_stride mask image virtual stride[6:0] (words) destination image virtual height[11:0] for line point drawing
15:12	RO	0x0	reserved
11:0	RW	0x000	dst_vir_stride destination image virtual stride(words)

RGA_DST_CTR_INFO
Address: Operational Base + offset (0x0154)
Destination image control window active width/height

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	dst_ctrl_win_height destination image control window height (11bits) Start Y in line drawing mode (11bits) Pre_scaling active height in pre_scaling mode (12bits)
15:12	RO	0x0	reserved
11:0	RW	0x000	dst_ctrl_win_width destination image control window width (11bits) Start X in line drawing mode (11bits) Pre_scaling active width in pre_scaling mode (12bits)

RGA_ALPHA_CON
Address: Operational Base + offset (0x0158)
Alpha blending/ROP mode register

Bit	Attr	Reset Value	Description
31	RW	0x0	ratate_aa Rotation AA mode 0:no AA 1:AA

Bit	Attr	Reset Value	Description
30	RW	0x0	gr_cal_mode Gradient calculation mode 0:clip 1:not-clip
29	RW	0x0	dither_down_en Dither_down_en 0:disable 1:enable
28	RW	0x0	alpah_cal_sel Alpha_cal_sel 0:alpha' = alpha + (alpha>>7) 1:alpha' = alpha
27:26	RW	0x0	bs_filter_type Blur/sharp Filter type 00:weakest 01:weaker 10:stronger 11:strongest
25	RW	0x0	bs_mode Blur/sharp filter mode 0: Blur 1: sharp
24	RW	0x0	pre_scl_yuv_out_fmt Pre-scale YCbCr output format 0: The same with source format 1: all is semi-planar
23:22	RW	0x0	pre_scl_v_ratio Pre_scaler vertical scaling ratio: 00: 1 01: 1/2 10: 1/4 11: 1/8
21:20	RW	0x0	pre_scl_h_ratio Pre_scaler horizontal scaling ratio: 00: 1 01: 1/2 10: 1/4 11: 1/8
19:18	RW	0x0	rop_mode ROP mode select 00: ROP 2 01: ROP 3 10: ROP 4
17	RW	0x0	fading_en Fading enable 0: disable 1: enable
16	RW	0x0	mix_alpha_mode Mix alpha mode or porter-duff alpha mode

Bit	Attr	Reset Value	Description
15:8	RW	0x00	user_set_alpha User set alpha constant value/fading_alpha_value
7:4	RW	0x0	port_duff_mode Porter-duff mode 0: CLEAR 1: SRC 2: DST 3: SRC OVER 4: DST OVER 5: SRC IN 6: DST IN 7: SRC OUT 8: DST OUT 9: SRC ATOP 10: DST ATOP 11: XOR
3:2	RW	0x0	alpah_mode Per pixel alpha or user set alpha 00: user set alpha 01: per pixel alpha 10: per pixel alpha & user set alpha 11: un-defined
1	RW	0x0	alpha_rop_sel Alpha or ROP sel: 0: alpha 1: ROP
0	RW	0x0	alpha_rop_en Alpha or ROP enable 0: disable 1: enable

RGA_PAT_CON

Address: Operational Base + offset (0x015c)

Pattern size/offset

Bit	Attr	Reset Value	Description
31:24	RW	0x00	pat_yoff Pattern y offset
23:16	RW	0x00	pat_xoff Pattern x offset
15:8	RW	0x00	pat_height Pattern height
7:0	RW	0x00	pat_width Pattern width Pattern total number when doing pattern load

RGA_DST_VIR_WIDTH
Address: Operational Base + offset (0x015c)
Register0000 Abstract

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	dst_vir_width_pixel destination image virtual width(pixel)

RGA_ROP_CON0
Address: Operational Base + offset (0x0160)
Raster operation code0 control register

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:0	RW	0x000000	rop3_code0 Rop3 code 0 control bits

RGA_CP_GR_G
Address: Operational Base + offset (0x0160)
Color gradient fill step of green

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	g_gr_y Y gradient value of Green (signed 8.8)
15:0	RW	0x0000	g_gr_x X gradient value of Green (signed 8.8)

RGA_PRESCL_CB_MST
Address: Operational Base + offset (0x0160)
RGA pre-scale Cb destination start addr

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pre_scl_uv_dst_mst Pre-scale Cb/Cr destination start addr

RGA_ROP_CON1
Address: Operational Base + offset (0x0164)
Raster operation code1 control register

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:0	RW	0x000000	rop3_code1 Rop3 code 1 control bits

RGA_CP_GR_R
Address: Operational Base + offset (0x0164)
Color gradient fill step of red

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	r_gr_y X gradient value of Red (signed 8.8)
15:0	RW	0x0000	r_gr_x X gradient value of Red (signed 8.8)

RGA_PRESCL_CR_MST
Address: Operational Base + offset (0x0164)
RGA pre-scale Cr destination start addr

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pre_scl_v_dst_mst Pre-scale Cr destination start addr

RGA_MMU_CTRL
Address: Operational Base + offset (0x0168)
MMU control register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	fading_b Fading offset B value
23:16	RW	0x00	fading_g Fading offset G value
15:8	RW	0x00	fading_r Fading offset R value
7:6	RO	0x0	reserved
5:4	RW	0x0	mmu_page_table_size RGA MMU Page table size 00: 1KB page 01: 2KB page 10: 4KB page 11: 8KB page
3	RW	0x0	cmd_flush_en MMU TLB CMD channel flush enable bit (auto clear) 00: 1KB page 01: 2KB page 10: 4KB page 11: 8KB page
2	RW	0x0	dst_flush_en MMU TLB DST channel flush enable bit (auto clear) 0: no flush 1: flush
1	RW	0x0	src_flush_en MMU TLB SRC channel flush enable bit (auto clear) 0: no flush 1: flush

Bit	Attr	Reset Value	Description
0	RW	0x0	mmu_en RGA MMU enable

RGA_MMU_TLB
Address: Operational Base + offset (0x016c)
RGA MMU TLB base address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_tlb_addr RGA MMU TLB base address(word)

RGA_YUV_OUT_CFG
Address: Operational Base + offset (0x170)
RGA Destination output configuration

bit	Attr	Reset Value	Description
31:15	RO	0x0	Reserved
14:8	RW	0x0	sw_axi_rw_align_e_n AXI WR/RD Align in line scan; Suggested value=7'b0, Align enable; [6:0] each bit value: 0, enable; 1: disable; [6]: DST BGR565/4444/1555 Read align disable [5]: DST ABGR888 Read align disable [4]: DST BGR565/4444/1555 Write align disable [3]: DST ABGR888 Write align disable [2]: SRC Y channel read Rlign disable [1]: SRC BGR565/4444/1555 Read align disable [0]: SRC ABGR888 Read align disable
7	RW	0x0	sw_cp_alpha_bit_sel alpha bits width select for ColorPalette; default=1'b0; 1: 1bit alpha; 0: 8bit alpha;
6	RW	0x0	sw_dst_csc_clip BGR2YUV Clip mode(from 0~255 clip to 36~235) 1: clip enable; 0: unclip
5:4	RW	0x1	sw_dst_csc_mode DST bitmap RGB2YUV conversion mode 00: Bypass mode, only used in y2y mode 01: BT.601-range0 10: BT.601-range1 11: BT.709-range0
3	RW	0x0	sw_dst_uv_swap Destination Cb-Cr swap 0: CrCb 1: CbCr
2	RW	0x0	reserved
1	RW	0x0	sw_dst_yuv_fmt Destination bitmap data format 0: YUV422SP 1: YUV420SP
0	RW	0x0	sw_dst_yuv_en Destination YUV output enable, Could not used

			Pre_scaling/Line-point drawing and Blur/Sharp, Alpha and ROP. 1: enable; 0: disable;

RGA_DST_UV_MST
Address: Operational Base + offset (0x174)
RGA Destination image UV start addr

bit	Attr	Reset Value	Description
31:0	RW	0x0	sw_dst_uv_mst destiniation image UV start address

19.5 Programming Guide

19.5.1 Register Partition

There are two types of register in RGA. The first 8 registers (0x0 - 0x1C) are general registers for system configuration including command mode, command parameter, RGA status, general interrupts. The other registers (range from 0x100~0x178) are command registers for command codes.

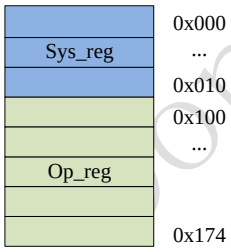

Fig. 19-8 HDMI TX Software Main Sequence Diagram

19.5.2 Command Modes

RGA has two command modes: slave mode and master mode. In salve mode (RGA_SYS_CTRL[2] = 1'b0), 2D graphic command only could be run one by one. CPU set all the command registers in RGA and then start RGA running by setting RGA_SYS_CTRL[2] to '1'. In master mode (RGA_SYS_CTRL[2] = 1'b1), 2D graphic commands could be run sequentially. After setting command's number to RGA_CMD_CTRL[12:3], writing '1' to RGA_CMD_CTRL[0] will start the command fetch, then Internal command DMA fetch commands from external command line.

Command line is a collection of several command codes with continuous address. At the first start, the command start address (RGA_CMD_ADDR) and command number (RGA_CMD_CTRL[12:3]) should be set, then write '1' to cmd_line_st (RGA_CMD_CTRL[0]) to start the command line fetch. Incremental command is supported by setting cmd_incr_num (RGA_CMD_CTRL[12:3]) and cmd_incr_valid (RGA_CMD_CTRL[1]=1'b1)

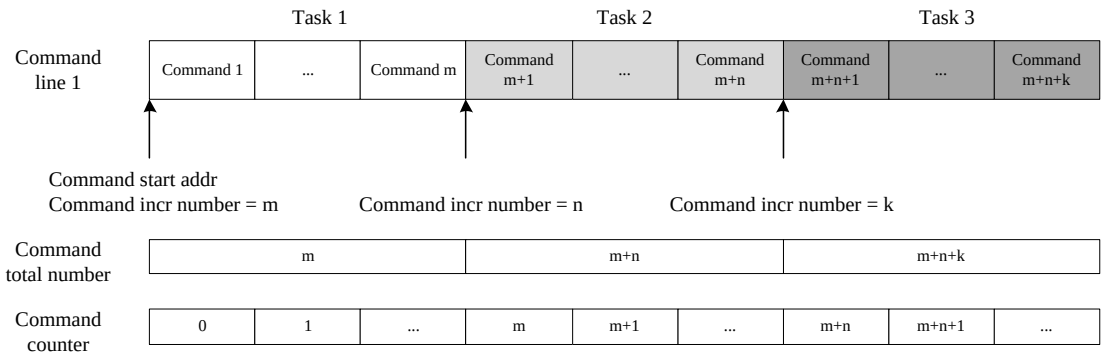

Fig. 19-9 RGA command line and command counter

19.5.3 Command Sync

In slave command mode, command sync is controlled by CPU.

In master command mode, user can enable the current_cmd_int (RGA_MODE_CTRL[25] = 1'b1) command by command to generate a interrupt at the end point of target command operation.

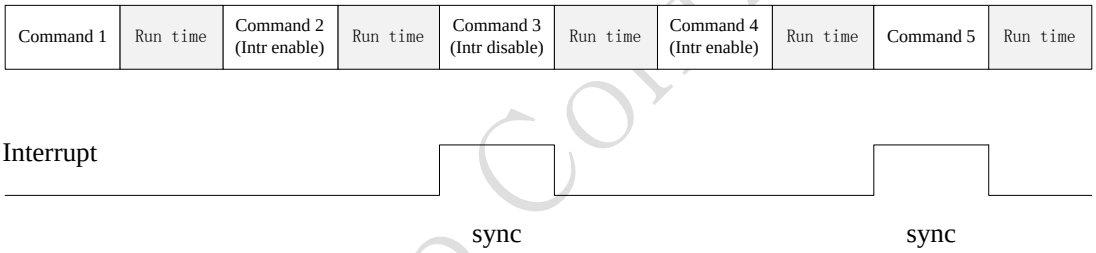

Fig. 19-10 RGA command sync generation