Chapter 23 LVDS

23.1 Overview

LVDS IP is integrated into MIPI D-PHY. LVDS transmitter converts a CMOS signal into a low-voltage differential signal. Usinga differential signal reduces the system's susceptibility to noise and EMI emissions. Inaddition, using a differential signal can deliver high speeds. This results in a verycost-effective solution to some of the greatest bandwidth bottlenecks in manytransmission applications.

23.1.1 Features

- 150MHz clock support
- LVDS 24bits or 18bits color data output
- PLL requires no external components
- Combine LVTTL IO, support LVDS/LVTTL data output
- Comply with the Standard TIA/EIA-644-A LVDS standard
- Support 8bit format-1, format-2, format-3 display mode, Support 6bit displaymode.
- Display mode can be select by input MUX
- Consumes Less Than 1mW When Disabled

23.2 Block Diagram

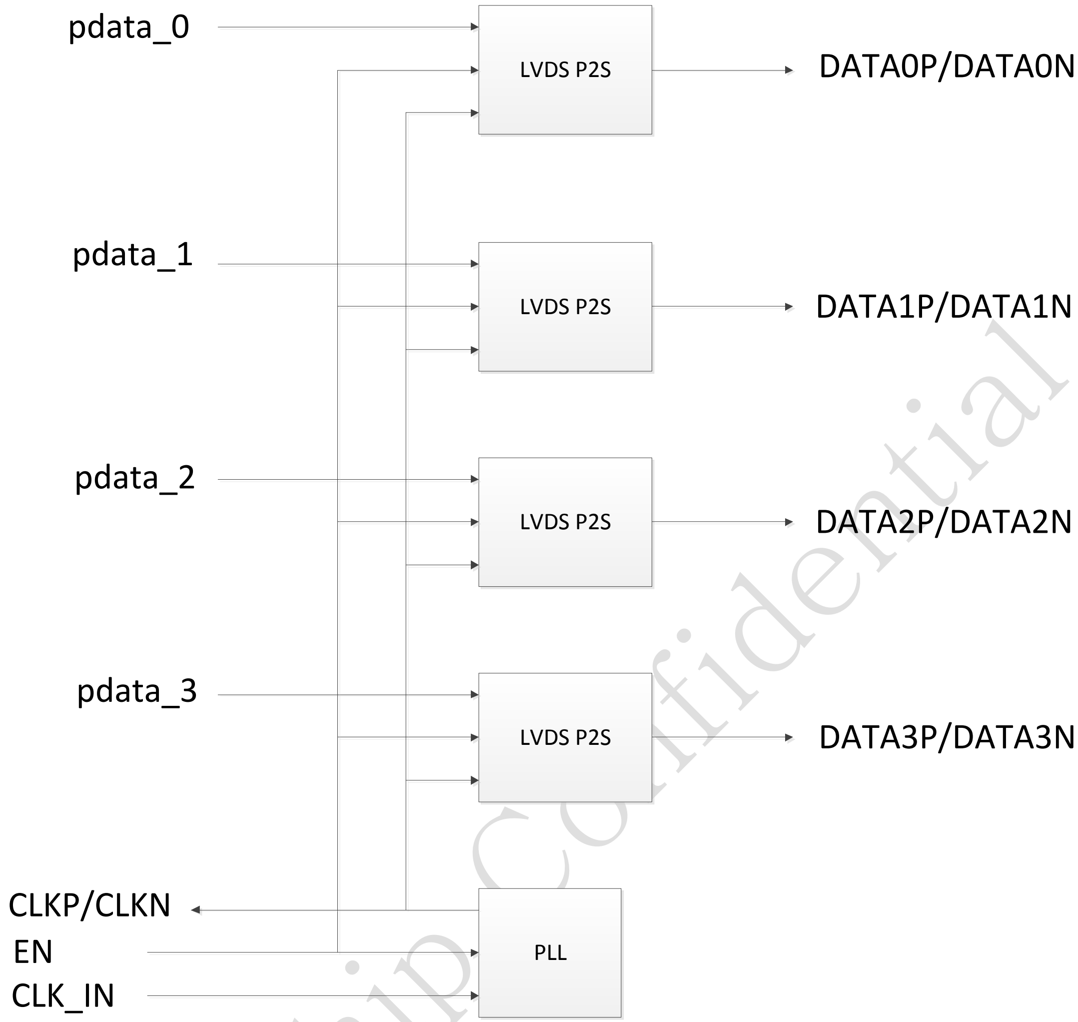

Fig.23-1LVDS TX Block Diagram

23.3 Function description

23.3.1 Video Data Processing

LVDS PHY implements LVDS TIA/EIA protocol. LVDS PHY contains four 7-bit parallel-load serial-out shift registers, a 7X clock PLL, and five LowVoltage Differential Signaling (LVDS) line drivers in a single integrated circuit. These functions allow 28 bits of single-ended LVTTLdata to be synchronously transmitted over five balanced-pair conductors for receipt by a compatible receiver.

When transmitting, parallel data, pdata0/1/2/3 are each loaded into registers upon the edge of the input clock signal (CLKIN). The frequency of CLKIN is multiplied seven times, and then used to unload the data registers in7-bit slices and serially. The four serial streams and a phase-locked clock (CLKOUT) are then output to LVDS output drivers.

The frequency of CLKOUT is the same as the input clock, CLKIN.

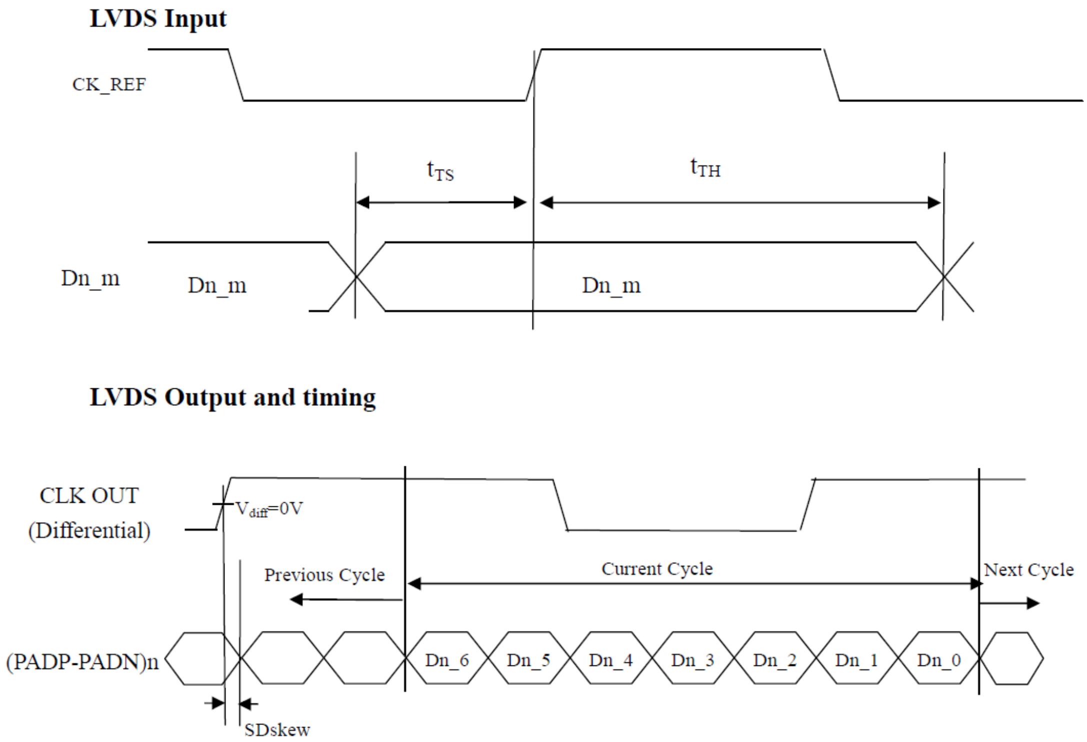

Fig.23-2LVDS TX InterfaceTiming

23.3.2 LVDSFORMAT

LVDSFORMAT converts LCDC RGB interface to LVDS format data, only support 8-bit/6-bit mode. Table 23-4 is LVDSFORMAT input data format.

Table 23-1 is LVDSFORMAT Input Data Format

Serial Channel	Data Bits	8-Bit			6-Bit	4-Bit	
		Format-1 [1]	Format-2 [2]	Format-3 [3]		Non-Linear Step Size [4]	Linear Step Size [5]
Y0	D0	R0	R2	R2	R0	R2	VCC
	D1	R1	R3	R3	R1	R3	GND
	D2	R2	R4	R4	R2	R0	R0
	D3	R3	R5	R5	R3	R1	R1
	D4	R4	R6	R6	R4	R2	R2
	D6	R5	R7	R7	R5	R3	R3
	D7	G0	G2	G2	G0	G2	VCC

Serial Channel	Data Bits	8-Bit			6-Bit	4-Bit	
		Format-1 [1]	Format-2 [2]	Format-3 [3]		Non-Linear Step Size [4]	Linear Step Size [5]
Y1	D8	G1	G3	G3	G1	G3	GND
	D9	G2	G4	G4	G2	G0	G0
	D12	G3	G5	G5	G3	G1	G1
	D13	G4	G6	G6	G4	G2	G2
	D14	G5	G7	G7	G5	G3	G3
	D15	B0	B2	B2	B0	B2	VCC
	D18	B1	B3	B3	B1	B3	GND
Y2	D19	B2	B4	B4	B2	B0	B0
	D20	B3	B5	B5	B3	B1	B1
	D21	B4	B6	B6	B4	B2	B2
	D22	B5	B7	B7	B5	B3	B3
	D24	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
	D25	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
	D26	ENABLE	ENABLE	ENABLE	ENABLE	ENABLE	ENABLE
Y3	D27	R6	R0	GND	GND	GND	GND
	D5	R7	R1	GND	GND	GND	GND
	D10	G6	G0	GND	GND	GND	GND
	D11	G7	G1	GND	GND	GND	GND
	D16	B6	B0	GND	GND	GND	GND
	D17	B7	B1	GND	GND	GND	GND
	D23	RSVD	RSVD	GND	GND	GND	GND
CLKOUT	CLKIN	CLK	CLK	CLK	CLK	CLK	CLK

[1] *Format-1:* 2-MSBs of each color transmitted over 4th serial data channel (Y3). Dominant data format for LCD panel.
[2] *Format-2:* 2-LSBs of each color transmitted over 4th serial data channel. System designer needs to verify the data format by checking with the LCD display data sheet.
[3] *Format-3:* 24-bit color host to 18-bit color LCD panel display application.
[4] Increased dynamic range of the entire color space at the expense of non-linear step sizes between each step.
[5] Linear step size with less dynamic range.

23.4 Register Description

23.4.1 Register Summary

Name	Offset	Size	Reset Value	Description
MIPI_reg03	0x000c	B	0x03	Register03
MIPI_reg04	0x0010	B	0x7d	Register04
MIPI_rege0	0x0380	B	0x45	Registere0
MIPI_rege1	0x0384	B	0x12	Registere1
MIPI_rege3	0x038c	B	0x01	Registere3
GRF_LVDS_CON0	0X0150	W	0x0100	GRF_LVDS_CON0

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

23.4.2 Detail Register Description

MIPI_reg03

Address: Operational Base + offset (0x000c)

Register03

Bit	Attr	Reset Value	Description
7:6	RW	0x0	reserved
5	RW	0x0	Reg_fbdiv[8] PLL input reference clock divider
4:0	RW	0x3	Reg_prediv[4:0] Integer value programmed into feedback divider

MIPI_reg04

Address: Operational Base + offset (0x0010)

Register04

Bit	Attr	Reset Value	Description
7:0	RW	0x7d	Reg_fbdiv[7:0] PLL input reference clock divider

MIPI_rege0

Address: Operational Base + offset (0x0380)

Registere0

Bit	Attr	Reset Value	Description
7:3	RW	0x00	reserved
2	RW	0x1	Digital internal reset Active low, default high
1	RW	0x0	reserved
0	RW	0x1	Selection for MSB and LSB 1'b1: MSB 1'b0: LSB

MIPI_rege1

Address: Operational Base + offset (0x0384)

Registere1

Bit	Attr	Reset Value	Description
7	RW	0x0	Digital internal enable Active high, default low.
6:0	RW	0x12	reserved

MIPI_rege3

Address: Operational Base + offset (0x038c)

Registere3

Bit	Attr	Reset Value	Description
7:3	RW	0x0	reserved
2	RW	0x0	TTL mode enable 1'b1: enable TTL mode 1'b0: disable TTL mode
1	RW	0x0	LVDS mode enable 1'b1: enable LVDS mode 1'b0: disable LVDS mode
0	RW	0x1	Mipi mode enable 1'b1: enable mipi mode 1'b0: disable mipi mode

GRF_LVDS_CON0

Address: Operational Base + offset (0x0150)

GRF_LVDS_CON0

Bit	Attr	Reset Value	Description
31:16	RW	0x0	Write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ...... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
13	RW	0x0	Mipiphylane3forcexmode 1'b1: enable 1'b0: disable
12	RW	0x0	Mipiphylane2 forcexmode 1'b1: enable 1'b0: disable
11	RW	0x0	Mipiphylane1 forcexmode 1'b1: enable 1'b0: disable
10	RW	0x0	Mipiphylane0 forcexmode 1'b1: enable 1'b0: disable
9	RW	0x0	Mipidsiforcexmode 1'b1: enable 1'b0: disable

Bit	Attr	Reset Value	Description
8	RW	0x0	Mipiphylane0turndisable 1’b1: enable 1’b0: disable
7	RW	0x0	Mipiphyttlmode 1’b1: enable 1’b0: disable
6	RW	0x0	lvds_mode 1’b1: enable 1’b0: disable
5	RW	0x0	Mipictrldpicoloorm 1’b1: enable 1’b0: disable
4	RW	0x0	Mipictrldpishutdown 1’b1: enable 1’b0: disable
3	RW	0x0	Lvdsmsbsel 1’b0: MSB is on D0 1’b1: MSB is on D7
2:1	RW	0x0	Lvdsselect 2’b00: 8bit mode format-1 2’b01: 8bit mode format-2 2’b10: 8bit mode format-3 2’b11: 6bit mode
0	RW	0x0	Ebc and lcdc_datasel 1'b0 : lcdc_data[9:0] 1'b1 : ebc

23.5 Interface Description

23.5.1 Video Input Source

In RKaudi, the LVDS TX video source comes from VOP.

23.6 ApplicationNotes

23.6.1 LVDS mode

When used in lvds mode, LVDS transmitter source from VOP, vop_dclk need get invert, then input to LVDS.

When lvds panel is LSB receive mode, lvds_msbsel =1, otherwiselvds_msbsel =0.

When LVDS output format is 8bit mode format-1/8bit mode format-2, configure grf_lvds_con0 in 24-bit color mode.

When LVDS output format is 8bit mode format-3/6bit mode,configure grf_lvds_con0 in 18-bit color mode.

Step1: configure GRF_LVDS_CON0

configure MIPI:

Step2: configure PLL

MIPI_reg03 = 0x01;

MIPI_reg04 = 0x07;

Step3: MIPI_rege0 = 0x45;

MIPI_rege1 = 0x92;

MIPI_rege3 = 0x02;

23.6.2 TTL mode

When used in lvttl mode, lvds_dclk and rgb_dclk need get invert.
ebc_sel = 1'b0: LVDS transmitter source from lcdc_data[9:0].
ebc_sel = 1'b1: LVDS transmitter source from EBC.

Step1: configure GRF_LVDS_CON0

Step2: configure PLL

MIPI_reg03 = 0x01;

MIPI_reg04 = 0x07;

Step3: MIPI_rege0 = 0x45;

MIPI_rege1 = 0x92;

MIPI_rege3 = 0x04;