

Rockchip RK3502G2 Datasheet

**Revision 1.1
Dec. 2025**

Revision History

Date	Revision	Description
2025-12-08	1.1	Update the POD thickness and update package dimension in 2.3
2024-10-10	1.0	Initial release

Rockchip Confidential

Table of Content

Table of Content	3
Figure Index	4
Table Index.....	5
Warranty Disclaimer.....	6
Chapter 1 Introduction	7
1.1 Overview	7
1.2 Features	7
1.3 Block Diagram	12
Chapter 2 Package Information.....	14
2.1 Order Information	14
2.2 Top Marking	14
2.3 Package Dimension	14
2.4 MSL Information	15
2.5 Lead Finish/Ball material Information	16
2.6 Pin Number List	16
2.7 Power/Ground IO Description	18
2.8 Function IO Description.....	20
2.9 IO Pin Name Description	23
2.10 Rockchip Matrix IO Function List	29
2.11 FLEXBUS Interface Typical Application Example.....	30
Chapter 3 Electrical Specification	32
3.1 Absolute Ratings	32
3.2 Recommended Operating Condition	32
3.3 DC Characteristics.....	33
3.4 Electrical Characteristics for General IO	34
3.5 Electrical Characteristics for PLL	34
3.6 Electrical Characteristics for USB2.0 Interface	35
3.7 Electrical Characteristics for SARADC	35
3.8 Electrical Characteristics for TSADC.....	36
3.9 Electrical Characteristics for CODEC ADC	36
Chapter 4 Thermal Management.....	37
4.1 Overview	37
4.2 Package Thermal Characteristics	37

Figure Index

Fig.1-1 RK3502G2 Block Diagram 13
Fig.2-1 RK3502G2 Package Definition 14
Fig.2-2 Package Top View 14
Fig.2-3 Package Bottom View 15
Fig.2-4 Package Side View 15
Fig.2-5 Package Dimension 15

Rockchip Confidential

Table Index

Table 2-1 Pin Number Order Information 16

Table 2-2 Power/Ground IO information 18

Table 2-3 Function IO description 20

Table 2-4 IO function description list 23

Table 2-5 Matrix IO function list 29

Table 2-6 Pin Mapping between FLEXBUS and ADC 30

Table 2-7 Pin Mapping between FLEXBUS and DAC 31

Table 2-8 Pin Mapping between FLEXBUS and DVP Camera 31

Table 3-1 Absolute ratings..... 32

Table 3-2 Recommended operating condition 32

Table 3-3 DC Characteristics..... 33

Table 3-4 Electrical Characteristics for Digital General IO 34

Table 3-5 Electrical Characteristics for FRAC PLL..... 34

Table 3-6 Electrical Characteristics for USB2.0 Interface 35

Table 3-7 Electrical Characteristics for SARADC 35

Table 3-8 Electrical Characteristics for TSADC 36

Table 3-9 Electrical Characteristics for CODEC ADC 36

Table 4-1 Thermal Resistance Characteristics 37

Warranty Disclaimer

Copyright © 2025 Rockchip Electronics Co., Ltd. All rights reserved.

No part of this document may be reproduced, transmitted or used in any form or by any means without the written prior consent of Rockchip Electronics Co., Ltd.

Trademark

Rockchip is a registered trademark of Rockchip Electronics Co., Ltd. in the People's Republic of China and other countries/areas. Other brands, product names mentioned in this document are the property of their respective owners.

Disclaimer

Rockchip Electronics Co., Ltd. ("Rockchip") may make changes to any information in this document at any time without any prior notice.

Information in this document is provided just as a reference or typical applications. All or part of product features described in this document may not be within the purchase scope or the usage scope, and may be subject to the third party licensing requirements. All statements, information in this document is provided "AS IS" without warranties of any kind, either express or implied. Actual performance of Rockchip products may vary in different applications. Third party licenses maybe required to use some features supported by Rockchip products. Customers shall be solely and exclusively responsible to obtain all appropriately required third party licenses prior to its such use. Should customers use the features supported by Rockchip products without any required third party license, customers shall indemnify and hold Rockchip and its subsidiaries, affiliates as well as distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of any claim associated with such unauthorized use.

Rockchip products are not intended for use in military, airplane, medical devices, lifesaving or life sustaining applications ("Unintended Uses"). Customers shall take any and all actions to ensure using Rockchip products in a lawful manner and shall be liable for Unintended Uses.

Chapter 1 Introduction

1.1 Overview

RK3502G2 is a high-performance triple-core Cortex-A7 processor designed for applications such as robot vacuums.

It is embedded with rich peripheral interfaces, such as UART, PWM, SARADC, Audio ADC, USB2 OTG, etc., to meet the requirements to develop different applications and reduce the complexity and cost of hardware development.

RK3502G2 has high-performance external memory interface capable of sustaining demanding memory bandwidths. Integrated 128MB DDR3 is available for customer.

1.2 Features

1.2.1 Microprocessor

- Triple-core ARM Cortex-A7 CPU
- ARM architecture v7-A instruction set
- ARM Neon Advanced SIMD (single instruction, multiple data) support for accelerated media and signal processing computation
- Include VFPv4-D32 hardware to support single and double-precision operations
- Integrated 16KB L1 instruction cache, 16KB L1 data cache
- 128KB unified system L2 cache
- TrustZone technology support
- One isolated voltage domain to support DVFS

1.2.2 Memory Organization

- Internal on-chip memory
 - BootROM
 - System SRAM
- External off-chip memory
 - SPI Nor/Nand Flash
 - SDMMC(eMMC/SD Card)

1.2.3 Internal Memory

- Internal BootRom
 - Support system boot from the following device:
 - ◆ SPI Flash interface
 - ◆ SDMMC(eMMC/SD Card) interface
 - Support system code download by the following interface:
 - ◆ USB OTG interface (Device mode)
 - ◆ SPI interface(Slave mode)
- Internal SRAM
 - 48KB System SRAM
- Integrated 128MB DDR is available.

1.2.4 External Memory or Storage device

- Serial Flash Interface
 - Support transfer data from/to SPI flash device
 - Support x1,x2,x4 data bits mode
 - Support up to 1 chip select
- SD/MMC Interface
 - Compatible with standard iNAND interface
 - Compatible with eMMC specification 4.51
 - Compatible with SD3.0, MMC ver4.51

- Compatible with SDIO3.0 protocol
- Data bus width is 4bits

1.2.5 System Component

- Cortex-M0
 - The ARMv6-M Thumb instruction set
 - Thumb-2 technology
 - Nested Vectored Interrupt Controller (NVIC)
 - Serial wire debug port (SW-DP) debug access
- CRU (clock & reset unit)
 - One oscillator with external 24MHz crystal input
 - One internal low frequency RC clock
 - One internal power on reset circuit
 - Support single-end 32.768KHz clock input/output from/to GPIO
 - Support PLL control and generate various clock frequency for chip
 - Support clock gating control for individual components
 - Support global soft-reset control for whole chip, also individual soft-reset for each component
- PMU(power management unit)
 - Three separate voltage domains(CPU_DVDD/LOGIC_DVDD/PMU_DVDD)
 - Multiple configurable work sleep modes to save power consumption by different frequency or automatic clock gating control or external power on/off control
- Timer
 - Twelve 64-bit timers with interrupt-based operation
 - One 64-bit timer with interrupt-based operation for low power mode application
 - Support two operation modes: free-running and user-defined count
 - Support timer work state checkable
- PWM0
 - 4-channel PWM with interrupt-based operation
 - Support capture mode
 - Provides reference mode and output various duty-cycle waveform
 - Support continuous mode or one-shot mode
 - Support one channel IR RX application
 - Support four channel waveform generation through lookup table
- PWM1
 - 8-channels PWM with interrupt-based operation
 - Support capture mode
 - Provides reference mode and output various duty-cycle waveform
 - Support continuous mode or one-shot mode
 - Support one channel IR TX application
 - Support one clock frequency calculation engine and one clock free running counter
 - Support six channel biphasic counter
- Watchdog
 - Support two 32-bit watchdog counter
 - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
 - WDT can perform two types of operations when timeout occurs:
 - ◆ Generate a system reset
 - ◆ First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
 - Programmable reset pulse length

- Totally 16 defined ranges of main timeout period
- Mailbox
 - One Mailbox to service Cortex-A7 and Cortex-M0 communication
 - Support four mailbox elements, each element includes one data word, one command word register and one flag bit that can represent one interrupt
- Spinlock
 - Support spinlock registers for software to realize resource management
- DMA
 - Support two embedded DMA controllers
 - Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory
 - Support TrustZone technology and programmable secure state for each DMA channel
 - DMAC0 support 6 channels in total
 - DMAC1 support 8 channels in total
- Secure System
 - Cipher engine
 - ◆ Support SHA-1, SHA-256/224, MD5 with hardware padding
 - ◆ Support HMAC of SHA-1, SHA-256, MD5 with hardware padding
 - ◆ Support AES-128, AES-192, AES-256 encrypt & decrypt cipher
 - ◆ Support AES ECB/CBC/OFB/CFB/CTR/CTS/XTS/CCM/GCM/CBC-MAC/CMAC mode
 - ◆ Support up to 4096 bits PKA mathematical operations for RSA
 - Support two 256 bits RNG output
 - Support secure boot
 - Support secure debug
 - Support secure OTP
 - Support secure OS
 - Support bus firewall

1.2.6 Graphics Engine

- 2D Graphics Engine
 - SRC0 Input data format:
 - ◆ ARGB8888/RGBA8888/RGBA4444/RGBA5551
 - ◆ RGB888P/RGB565
 - ◆ YUV422-P/YUV422-SP-8bit/10bit(clip to 8bit after input)
 - ◆ YUV420-P/YUV420-SP-8bit/10bit(clip to 8bit after input)
 - ◆ YVYU422-8bit
 - ◆ YUV400-8bit
 - ◆ BPP1/2/4/8
 - SRC1 Input data format:
 - ◆ ARGB8888/RGBA8888/RGBA4444/RGBA5551/A8
 - ◆ RGB888P/RGB565
 - Output data format(all YUV format is 8bit):
 - ◆ ARGB8888/RGBA8888/ARGB4444/RGBA4444/ARGB5551/RGBA5551
 - ◆ RGB888/RGB565
 - ◆ YUV420/YUV422 P/SP
 - ◆ YUV400
 - Pixel Format conversion, BT.601/BT.709
 - Dither operation
 - Max resolution: 1280x1280 source, 1280x1280 destination
 - Scaling
 - ◆ Down-scaling: Average filter

- ◆ Up-scaling: Bi-cubic filter(Horizontal, Vertical), Bi-linear filter(Vertical)
- ◆ Arbitrary non-integer scaling ratio, from 1/16 to 16
- Rotation
 - ◆ 0, 90, 180, 270 degree rotation
 - ◆ x-mirror, y-mirror operation
 - ◆ Mirroring and rotation co-operation
- BitBLT
 - ◆ Block transfer
 - ◆ Color palette/Color fill, support with alpha
 - ◆ Transparency mode (color keying/stencil test, specified value/value range)
 - ◆ Two source BitBLT
 - ◆ A+B=B only BitBLT, A support rotate & scale when B fixed
 - ◆ A+B=C second source (B) has same attribute with (C) plus rotation function
- Alpha Blending
 - ◆ Comprehensive per-pixel alpha(color/alpha channel separately)
 - ◆ Fading
 - ◆ Support SRC1(R2Y)+SRC0(YUV) -> DST(YUV)
 - ◆ Support DST Full CSC convert for YUV2YUV
- Others
 - ◆ Supports Gaussian filters with a window size of 3 * 3

1.2.7 Audio Interface

- SAI
 - Support five SAI components
 - Support audio protocol: I2S, PCM, TDM
 - Support up to 128 slots available with configurable size
 - Support slot length 8 to 32 bits configurable
 - Support master and slave mode, software configurable
 - Sample rate up to 192KHz
 - Support slot valid data length 8 to 32 bits configurable
 - SAI0 support up to one lane transmitter and four lane parallel receivers
 - SAI1 support up to four lane parallel transmitters and one lane receiver
 - SAI2 support up to one lane transmitter and one lane receiver
 - SAI0/1/2 connected to chip GPIO
 - SAI3 support up to one lane transmitter and one lane receiver
 - SAI4 support up to one lane receiver
 - SAI3 connected to internal Audio DSM modulator and chip GPIO optional, and SAI4 connected to internal Audio ADC
- PDM
 - Support PDM master receive mode
 - Support 5 wire PDM interface with one is clock and 4 data line
 - Support up to 8 mono microphones
 - Support 16~24 bits sample resolution
 - Sample rate up to 192KHz
- ASRC
 - Support two ASRC components
 - Support fixed length conversion mode and real time conversion mode
 - Support asynchronous sample rate clock for real time conversion mode
 - Support 4 channel sample rate converter for each ASRC
 - Support combine two ASRC component to meet 8 channel sample rate converter
- Audio DSM
 - Support 2-channel digital DAC
 - Support I2S/PCM master and slave mode
 - Support 16 bit sample resolution

- Support volume control
- Sample rate up to 192KHz
- Audio ADC
 - One channel 24 bit ADC microphone input
 - Support one differential microphone input
 - Support I2S as the digital signal interface
 - Support both master and slave mode
 - Support 16bits/24bits resolution
 - Support I2S normal, left and right justified mode
 - Sample rate up to 192KHz

1.2.8 Connectivity

- USB 2.0 OTG
 - Support two USB 2.0 OTG ports
 - Compatible with USB 2.0 specification
 - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
- FLEXBUS interface
 - Support transfer data from internal memory to GPIO by DMA
 - Support transfer data from GPIO to internal memory by DMA
 - Support multiple operating modes
 - ◆ Multiplexing TX clock and RX clock, Multiplexing TX data and RX data
 - Support TX only mode, RX only mode, TX then RX mode
 - ◆ Multiplexing TX clock and RX clock, Separating TX data and RX data
 - Support TX only mode, RX only mode, TX and RX mode, TX then RX mode
 - ◆ Separating TX clock and RX clock, Separating TX data and RX data
 - Support TX only mode, RX only mode, TX and RX mode
 - Support clock free running mode and following data mode
 - Support TX data width 1, 2, 4, 8, 16 bit configurable
 - Support RX data width 1, 2, 4, 8, 16 bit configurable
 - Support continue transmission mode and fix length transmission mode
 - Support one chip selection function for multiplexing TX clock and RX clock mode
 - Support two chip selection function for separating TX clock and RX clock mode, one for TX direction, the other for RX direction
 - Support TX clock auto gating
 - Support DVP (RGB888, RGB565, YUV422) interface for camera sensor
- SPI interface
 - Support three SPI Controllers
 - SPI0/SPI1 support serial-master and serial-slave mode, software-configurable
 - Support 2 chip-selects output in serial-master mode
 - SPI2 support serial-slave mode
- I2C interface
 - Support three I2C interface
 - Support 7bits and 10bits address mode
 - Software programmable clock frequency
 - Data on the I2C-bus can be transferred at rates of up to 100 Kbit/s in the Standard-mode, up to 400 Kbit/s in the Fast-mode or up to 1 Mbit/s in Fast-mode Plus
- UART Controller
 - Support six UART interface
 - Embedded two 64-byte FIFO for TX and RX operation respectively
 - Support 5bit, 6bit, 7bit, 8bit serial data transmit or receive
 - Standard asynchronous communication bits such as start, stop and parity

- Support different input clock for UART operation to get up to 4Mbps baud rate
- Support auto flow control mode
- Touch Key Controller
 - Support multi-channel CapSense monitor
 - Support trigger interrupt waterline configurable
 - Support LPF and DC elimination

1.2.9 Others

- Multiple groups of GPIO
 - All of GPIOs can be used to generate interrupt
 - Support level trigger and edge trigger interrupt
 - Support configurable polarity of level trigger interrupt
 - Support configurable rising edge, falling edge and both edge trigger interrupt
 - Support configurable pull direction (pullup or pulldown)
 - Support configurable drive strength
 - Support configurable slew rate
- Temperature Sensor (TS-ADC)
 - Up to 50KS/s sampling rate
 - Support one temperature sensor
 - -40~125°C temperature range and +/-5°C temperature accuracy
- Successive Approximation ADC (SARADC)
 - 10-bit resolution
 - Up to 1MS/s sampling rate
 - 4 single-ended input channels
 - GPIO multiplexed
- OTP
 - Support 8K bits Size, 7K bit for secure application
 - Support Program/Read/Idle mode
- Package Type
 - RK3502G2: QFN128L(body: 12.3mm x 12.3mm; lead pitch: 0.35mm)
 - ◆ Embedded with 128MB DDR3L

1.3 Block Diagram

The following figure shows the basic block diagram.

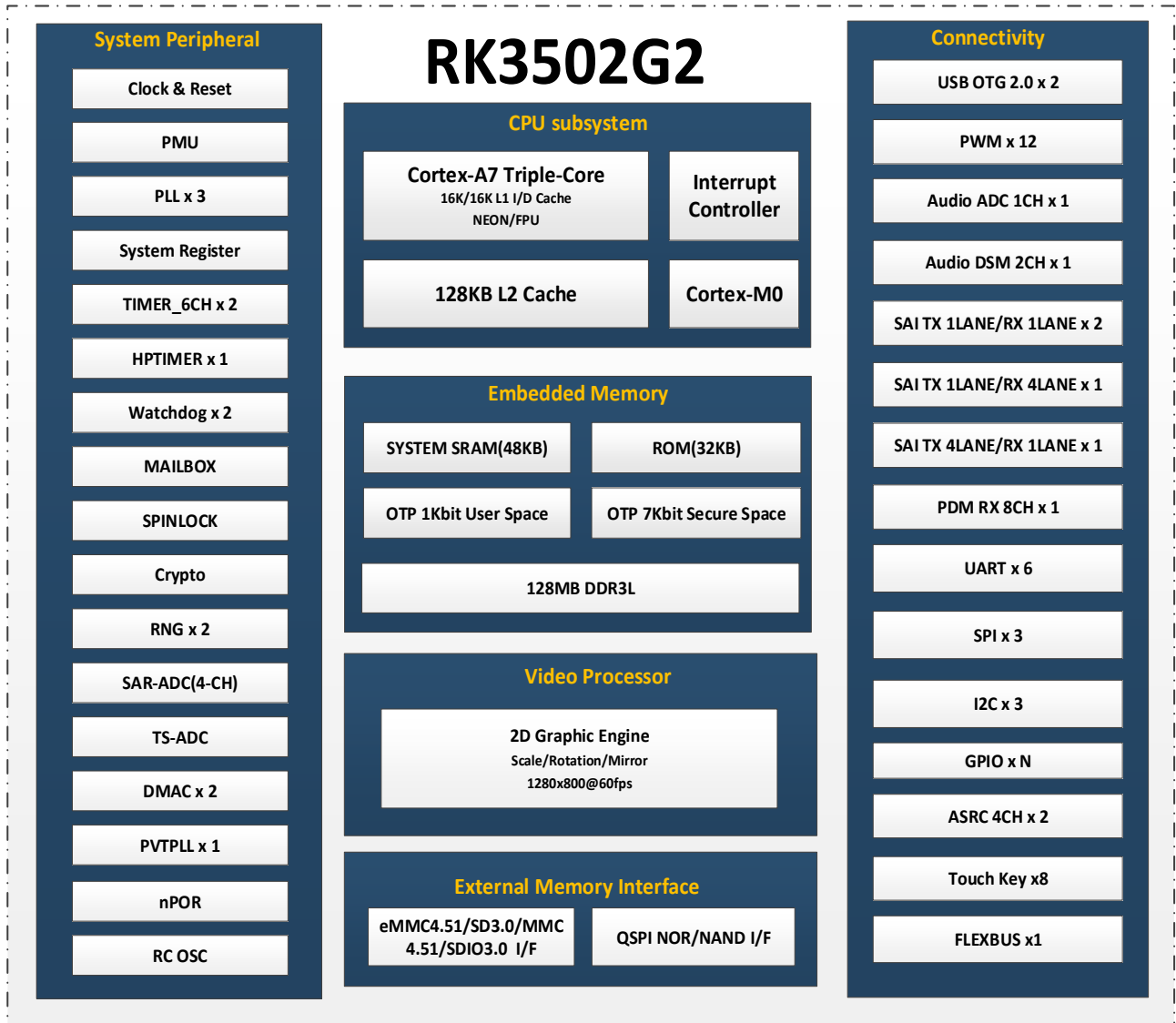


Fig.1-1 RK3502G2 Block Diagram

Chapter 2 Package Information

2.1 Order Information

Orderable Device	RoHS status	Package	Package Qty	Device Feature
RK3502G2	RoHS	QFN128L	1520 pcs	Audio Application Processor

2.2 Top Marking

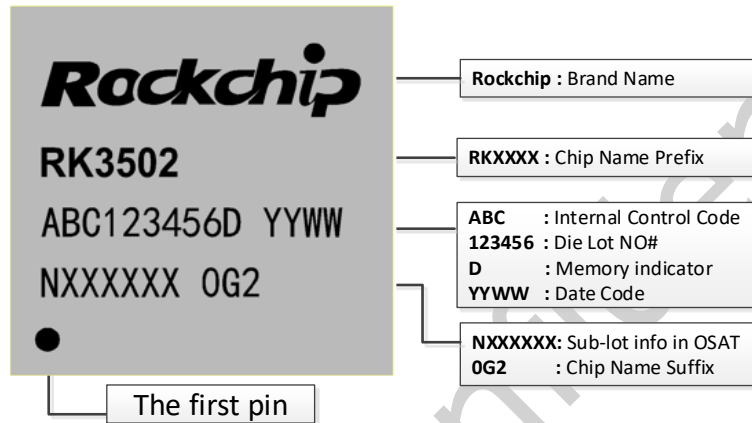


Fig.2-1 RK3502G2 Package Definition

2.3 Package Dimension

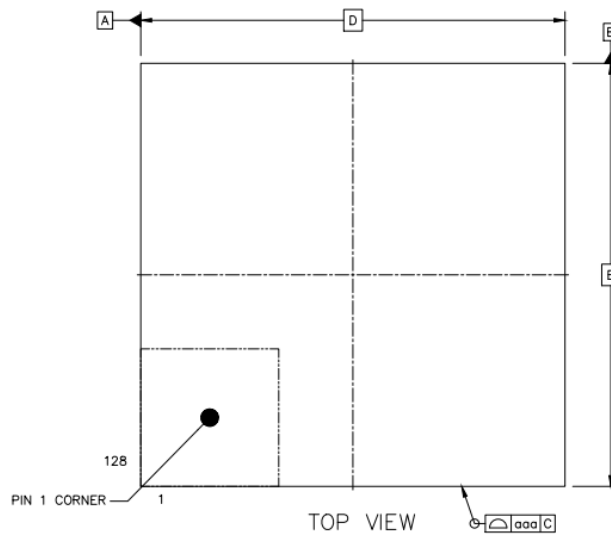


Fig.2-2 Package Top View

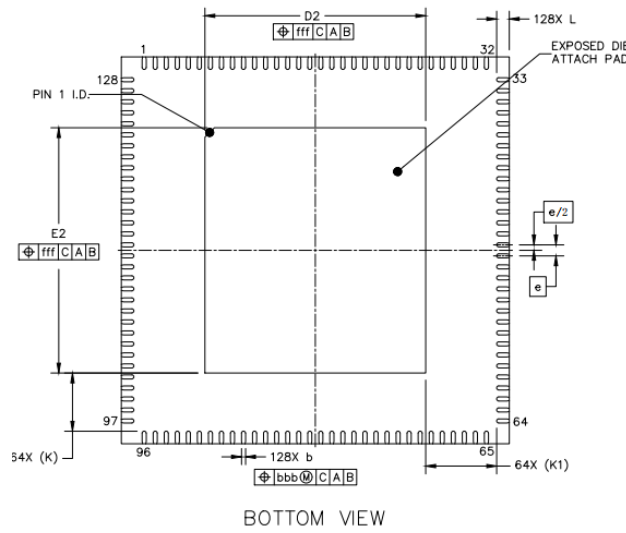


Fig.2-3 Package Bottom View

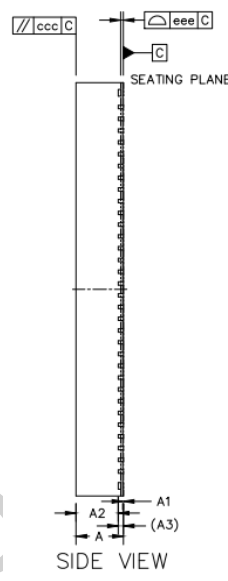


Fig.2-4 Package Side View

	SYMBOL	MIN	NOM	MAX	
TOTAL THICKNESS	A	1.35	1.4	1.45	
STAND OFF	A1	0	0.02	0.05	
MOLD THICKNESS	A2	---	1.25	---	
L/F THICKNESS	A3		0.152 REF		
LEAD WIDTH	b	0.08	0.13	0.18	
BODY SIZE	X	D 12.3 BSC			
	Y	E 12.3 BSC			
LEAD PITCH	e	0.35 BSC			
EP SIZE	X	D2	6.9	7	7.1
	Y	E2	7.7	7.8	7.9
LEAD LENGTH	L	0.3	0.4	0.5	
LEAD TIP TO EXPOSED PAD EDGE	K	1.85 REF			
	K1	2.25 REF			
PACKAGE EDGE TOLERANCE	aaa	0.1			
MOLD FLATNESS	ccc	0.1			
COPLANARITY	eee	0.08			
LEAD OFFSET	bbb	0.07			
EXPOSED PAD OFFSET	fff	0.1			

Fig.2-5 Package Dimension

2.4 MSL Information

Moisture sensitivity Level: 3

2.5 Lead Finish/Ball material Information

Lead Finish/Ball material: Sn

2.6 Pin Number List

Table 2-1 Pin Number Order Information

Pin	Pin Name	Abbreviated Pin Name
1	SPI0_MOSI/RM_IO17/GPIO0_C1_d	GPIO0_C1
2	SPI0_CLK/RM_IO16/GPIO0_C0_d	GPIO0_C0
3	SAI1_SDO3/SPI0_CSN1/RM_IO15/GPIO0_B7_d	GPIO0_B7
4	SAI1_SDO2/SPI1_CSN0/RM_IO14/GPIO0_B6_d	GPIO0_B6
5	SAI1_SDO1/RM_IO13/GPIO0_B5_d	GPIO0_B5
6	SAI1_SDO0/RM_IO12/GPIO0_B4_d	GPIO0_B4
7	SAI1_SDI/RM_IO11/GPIO0_B3_d	GPIO0_B3
8	SAI1_LRCK/SPI1_MISO/RM_IO10/GPIO0_B2_d	GPIO0_B2
9	PMUIO_VCC3V3	PMUIO_VCC3V3
10	NPOR	NPOR
11	PMU_LOGIC_DVDD0V9	PMU_LOGIC_DVDD0V9
12	SAI1_SCLK/SPI1_MOSI/RM_IO9/GPIO0_B1_d	GPIO0_B1
13	SAI1_MCLK/SPI1_CLK/RM_IO8/GPIO0_B0_d	GPIO0_B0
14	SAI0_SDI3/SPI1_CSN1/RM_IO7/GPIO0_A7_d	GPIO0_A7
15	SAI0_SDI2/RM_IO6/GPIO0_A6_d	GPIO0_A6
16	SAI0_SDI1/RM_IO5/GPIO0_A5_d	GPIO0_A5
17	SAI0_SDI0/RM_IO4/GPIO0_A4_d	GPIO0_A4
18	SAI0_SDO/RM_IO3/GPIO0_A3_d	GPIO0_A3
19	SAI0_MCLK/RM_IO2/GPIO0_A2_u	GPIO0_A2
20	SAI0_SCLK/RM_IO1/GPIO0_A1_d	GPIO0_A1
21	SAI0_LRCK/RM_IO0/GPIO0_A0_u	GPIO0_A0
22	DDR_VDDQ	DDR_VDDQ
23	DDR_VDDQ	DDR_VDDQ
24	VSS	VSS
25	DDR_VDDQ	DDR_VDDQ
26	SAI2_MCLK_M0/GPIO3_B6_d	GPIO3_B6
27	UART5_RTSN_M0/GPIO3_B5_d	GPIO3_B5
28	UART5_TX_M0/GPIO3_B4_d	GPIO3_B4
29	UART5_RX_M0/GPIO3_B3_d	GPIO3_B3
30	UART5_CTSN_M0/GPIO3_B2_d	GPIO3_B2
31	SAI2_LRCK_M0/GPIO3_B1_d	GPIO3_B1
32	SAI2_SDO_M0/GPIO3_B0_d	GPIO3_B0
33	SAI2_SCLK_M0/GPIO3_A7_d	GPIO3_A7
34	SAI2_SDI_M0/GPIO3_A6_d	GPIO3_A6
35	SDMMC_D1/TEST_CLK_OUT/GPIO3_A3_d	GPIO3_A3
36	SDMMC_D0/GPIO3_A2_d	GPIO3_A2
37	SDMMC_CLK/GPIO3_A0_d	GPIO3_A0
38	SDMMC_CMD/GPIO3_A1_d	GPIO3_A1
39	VCCIO4_VCC	VCCIO4_VCC
40	SDMMC_D3/JTAG_TMS_M0/GPIO3_A5_d	GPIO3_A5
41	SDMMC_D2/JTAG_TCK_M0/GPIO3_A4_d	GPIO3_A4

Pin	Pin Name	Abbreviated Pin Name
42	SAI3_MCLK/GPIO2_C0_d	GPIO2_C0
43	DSM_AUD_LP_M1/SAI3_SDO/GPIO2_B7_d	GPIO2_B7
44	DSM_AUD_LN_M1/SAI3_SDI/GPIO2_B6_d	GPIO2_B6
45	DSM_AUD_RP_M1/SAI3_LRCK/GPIO2_B5_d	GPIO2_B5
46	DSM_AUD_RN_M1/SAI3_SCLK/GPIO2_B4_d	GPIO2_B4
47	SPI2_MISO/GPIO2_B3_d	GPIO2_B3
48	SPI2_MOSI/GPIO2_B2_d	GPIO2_B2
49	SPI2_CSN/GPIO2_B1_d	GPIO2_B1
50	SPI2_CLK/GPIO2_B0_d	GPIO2_B0
51	LOGIC_DVDD	LOGIC_DVDD
52	VCCIO3_VCC	VCCIO3_VCC
53	FSPI_D3/GPIO2_A5_u	GPIO2_A5
54	FSPI_CLK/GPIO2_A1_d	GPIO2_A1
55	FSPI_D0/GPIO2_A2_u	GPIO2_A2
56	VCCIO2_VCC	VCCIO2_VCC
57	FSPI_D2/GPIO2_A4_u	GPIO2_A4
58	FSPI_D1/GPIO2_A3_u	GPIO2_A3
59	FSPI_CSN/GPIO2_A0_u	GPIO2_A0
60	SARADC_IN3/GPIO4_B3_z	SARADC_IN3/GPIO4_B3_z
61	SARADC_IN2/GPIO4_B2_z	SARADC_IN2/GPIO4_B2_z
62	SARADC_IN1/GPIO4_B1_z	SARADC_IN1/GPIO4_B1_z
63	SARADC_IN0/GPIO4_B0_z	SARADC_IN0/GPIO4_B0_z
64	AVCC_1V8	AVCC_1V8
65	ACODEC_ADC_AVDD1V6	ACODEC_ADC_AVDD1V6
66	ACODEC_ADC_VCM	ACODEC_ADC_VCM
67	ACODEC_ADC_INN	ACODEC_ADC_INN
68	ACODEC_ADC_INP	ACODEC_ADC_INP
69	ACODEC_ADC_AVSS	ACODEC_ADC_AVSS
70	USB20_OTG_AVDD3V3	USB20_OTG_AVDD3V3
71	USB20_OTG0_DM	USB20_OTG0_DM
72	USB20_OTG0_DP	USB20_OTG0_DP
73	USB20_OTG1_DM	USB20_OTG1_DM
74	USB20_OTG1_DP	USB20_OTG1_DP
75	AVDD_0V9	AVDD_0V9
76	AVDD_1V8	AVDD_1V8
77	GPO4_A4_z	GPO4_A4_z
78	GPO4_A5_z	GPO4_A5_z
79	GPO4_A2_z	GPO4_A2_z
80	GPO4_A3_z	GPO4_A3_z
81	GPO4_A0_z	GPO4_A0_z
82	GPO4_A1_z	GPO4_A1_z
83	FLEXBUS1_D0/GPIO1_A0_d	GPIO1_A0
84	FLEXBUS1_D1/GPIO1_A1_d	GPIO1_A1
85	CPU_DVDD	CPU_DVDD
86	VSS	VSS
87	LOGIC_DVDD	LOGIC_DVDD
88	FLEXBUS1_D2/GPIO1_A2_d	GPIO1_A2
89	FLEXBUS1_D3/GPIO1_A3_d	GPIO1_A3
90	FLEXBUS1_D4/GPIO1_A4_d	GPIO1_A4

Pin	Pin Name	Abbreviated Pin Name
91	FLEXBUS1_D5/GPIO1_A5_d	GPIO1_A5
92	VCCIO1_VCC	VCCIO1_VCC
93	FLEXBUS1_D6/GPIO1_A6_d	GPIO1_A6
94	FLEXBUS1_D7/GPIO1_A7_d	GPIO1_A7
95	FLEXBUS1_D8/FLEXBUS0_CSN_M0/GPIO1_B0_d	GPIO1_B0
96	FLEXBUS1_D9/FLEXBUS1_CSN_M0/UART5_CTSN_M1/RM_IO24/GPIO1_B1_d	GPIO1_B1
97	FLEXBUS1_D10/FLEXBUS0_D15/FLEXBUS0_CSN_M1/SAI2_SCLK_M1/RM_IO25/GPIO1_B2_d	GPIO1_B2
98	FLEXBUS1_D11/FLEXBUS0_D14/FLEXBUS1_CSN_M1/SAI2_LRCK_M1/RM_IO26/GPIO1_B3_d	GPIO1_B3
99	FLEXBUS1_D12/FLEXBUS0_D13/FLEXBUS0_CSN_M2/GPIO1_B4_d	GPIO1_B4
100	FLEXBUS1_D13/FLEXBUS0_D12/FLEXBUS1_CSN_M2/GPIO1_B5_d	GPIO1_B5
101	FLEXBUS1_D14/FLEXBUS0_D11/FLEXBUS0_CSN_M3/GPIO1_B6_d	GPIO1_B6
102	FLEXBUS1_D15/FLEXBUS0_D10/FLEXBUS1_CSN_M3/GPIO1_B7_d	GPIO1_B7
103	VCCIO1_VCC	VCCIO1_VCC
104	FLEXBUS1_CLK/FLEXBUS0_CSN_M4/GPIO1_C0_d	GPIO1_C0
105	FLEXBUS0_CLK/DSM_AUD_RN_M0/FLEXBUS1_CSN_M4/SAI2_MCLK_M1/GPIO1_C1_d	GPIO1_C1
106	FLEXBUS0_D9/DSM_AUD_RP_M0/FLEXBUS0_CSN_M5/SAI2_SDI_M1/RM_IO27/GPIO1_C2_d	GPIO1_C2
107	FLEXBUS0_D8/FLEXBUS1_CSN_M5/SAI2_SDO_M1/RM_IO28/GPIO1_C3_d	GPIO1_C3
108	FLEXBUS0_D7/GPIO1_C4_d	GPIO1_C4
109	FLEXBUS0_D6/GPIO1_C5_d	GPIO1_C5
110	LOGIC_DVDD	LOGIC_DVDD
111	VSS	VSS
112	CPU_DVDD	CPU_DVDD
113	FLEXBUS0_D5/GPIO1_C6_d	GPIO1_C6
114	FLEXBUS0_D4/GPIO1_C7_d	GPIO1_C7
115	FLEXBUS0_D3/DSM_AUD_LN_M0/GPIO1_D0_d	GPIO1_D0
116	FLEXBUS0_D2/DSM_AUD_LP_M0/UART5_RTSN_M1/RM_IO29/GPIO1_D1_d	GPIO1_D1
117	FLEXBUS0_D1/UART5_TX_M1/RM_IO30/GPIO1_D2_d	GPIO1_D2
118	FLEXBUS0_D0/UART5_RX_M1/RM_IO31/GPIO1_D3_d	GPIO1_D3
119	OSC_CLK_OUT/REF_CLK0_OUT/GPIO0_D0_d	GPIO0_D0
120	SYS_PLL_AVDD1V8	SYS_PLL_AVDD1V8
121	OSC_XIN	OSC_XIN
122	OSC_XOUT	OSC_XOUT
123	UART0_RX/JTAG_TMS_M1/RM_IO23/GPIO0_C7_u	GPIO0_C7
124	UART0_TX/JTAG_TCK_M1/RM_IO22/GPIO0_C6_u	GPIO0_C6
125	CPU_AVS/RM_IO21/GPIO0_C5_z	GPIO0_C5
126	AUPLL_CLK_IN/RM_IO20/GPIO0_C4_d	GPIO0_C4
127	SPI0_CSN0/RM_IO19/GPIO0_C3_d	GPIO0_C3
128	REF_CLK1_OUT/SPI0_MISO/RM_IO18/GPIO0_C2_d	GPIO0_C2
EPA D	VSS	VSS

2.7 Power/Ground IO Description

Table 2-2 Power/Ground IO information

Group	Pin#	Descriptions
VSS	24, 86, 111, EPAD	Digital Ground

Group	Pin#	Descriptions
ACODEC_ADC_AVSS	69	ACODEC ADC Analog Ground
CPU_DVDD	85, 112	Logic Power
LOGIC_DVDD	51, 87, 110	DSP0 Power
PMU_LOGIC_DVDD0V9	11	PMU Power
PMUIO_VCC3V3	9	PMU IO Power
VCCIO1_VCC	92, 103	VCCIO1 IO Power
VCCIO2_VCC	56	VCCIO2 IO Power
VCCIO3_VCC	52	VCCIO3 IO Power
VCCIO4_VCC	39	VCCIO4 IO Power
SYS_PLL_AVDD1V8	120	PLL Power
USB20_OTG_AVDD3V3	70	USB OTG2.0 Power
AVDD_0V9	75	USB OTG2.0
AVDD_1V8	76	USB OTG2.0
AVCC_1V8	64	ACODEC ADC/SARADC/OTP Analog Power
DDR_VDDQ	22, 23, 25	DDR Power

2.8 Function IO Description

Table 2-3 Function IO description

Pin	Pin Name	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Pad Type ^①	Def ^③	Pull	Drive Strength ^②	INT	Power Domain	
121	OSC_XIN	OSC_XIN									I	I	N/A	N/A		PLL	
122	OSC_XOUT	OSC_XOUT									O	O	N/A	N/A			
119	OSC_CLK_OUT/REF_CLK0_OUT/GPIO0_D0_d	GPIO0_D0	OSC_CLK_OUT	REF_CLK0_OUT							IO	I	down	Level1	√		
10	NPOR	NPOR									I	I	N/A	N/A		PMUIO_VCC3V3	
21	SAI0_LRCK/RM_IO0/GPIO0_A0_u	GPIO0_A0	SAI0_LRCK						RM_IO0		IO	I	up	Level2	√		
20	SAI0_SCLK/RM_IO1/GPIO0_A1_d	GPIO0_A1	SAI0_SCLK						RM_IO1		IO	I	down	Level2	√		
19	SAI0_MCLK/RM_IO2/GPIO0_A2_u	GPIO0_A2	SAI0_MCLK						RM_IO2		IO	I	up	Level2	√		
18	SAI0_SDO/RM_IO3/GPIO0_A3_d	GPIO0_A3	SAI0_SDO						RM_IO3		IO	I	down	Level2	√		
17	SAI0_SDI0/RM_IO4/GPIO0_A4_d	GPIO0_A4	SAI0_SDI0						RM_IO4		IO	I	down	Level2	√		
16	SAI0_SDI1/RM_IO5/GPIO0_A5_d	GPIO0_A5	SAI0_SDI1						RM_IO5		IO	I	down	Level2	√		
15	SAI0_SDI2/RM_IO6/GPIO0_A6_d	GPIO0_A6	SAI0_SDI2						RM_IO6		IO	I	down	Level2	√		
14	SAI0_SDI3/SPI1_CSN1/RM_IO7/GPIO0_A7_d	GPIO0_A7	SAI0_SDI3	SPI1_CSN1					RM_IO7		IO	I	down	Level2	√		
13	SAI1_MCLK/SPI1_CLK/RM_IO8/GPIO0_B0_d	GPIO0_B0	SAI1_MCLK	SPI1_CLK					RM_IO8		IO	I	down	Level2	√		
12	SAI1_SCLK/SPI1_MOSI/RM_IO9/GPIO0_B1_d	GPIO0_B1	SAI1_SCLK	SPI1_MOSI					RM_IO9		IO	I	down	Level2	√		
8	SAI1_LRCK/SPI1_MISO/RM_IO10/GPIO0_B2_d	GPIO0_B2	SAI1_LRCK	SPI1_MISO					RM_IO10		IO	I	down	Level2	√		
7	SAI1_SDI/RM_IO11/GPIO0_B3_d	GPIO0_B3	SAI1_SDI						RM_IO11		IO	I	down	Level2	√		
6	SAI1_SDO0/RM_IO12/GPIO0_B4_d	GPIO0_B4	SAI1_SDO0						RM_IO12		IO	I	down	Level2	√		
5	SAI1_SDO1/RM_IO13/GPIO0_B5_d	GPIO0_B5	SAI1_SDO1						RM_IO13		IO	I	down	Level2	√		
4	SAI1_SDO2/SPI1_CSN0/RM_IO14/GPIO0_B6_d	GPIO0_B6	SAI1_SDO2	SPI1_CSN0					RM_IO14		IO	I	down	Level2	√		
3	SAI1_SDO3/SPI0_CSN1/RM_IO15/GPIO0_B7_d	GPIO0_B7	SAI1_SDO3	SPI0_CSN1					RM_IO15		IO	I	down	Level2	√		
2	SPI0_CLK/RM_IO16/GPIO0_C0_d	GPIO0_C0		SPI0_CLK					RM_IO16		IO	I	down	Level2	√		
1	SPI0_MOSI/RM_IO17/GPIO0_C1_d	GPIO0_C1		SPI0_MOSI					RM_IO17		IO	I	down	Level2	√		
128	REF_CLK1_OUT/SPI0_MISO/RM_IO18/GPIO0_C2_d	GPIO0_C2	REF_CLK1_OUT	SPI0_MISO					RM_IO18		IO	I	down	Level2	√		
127	SPI0_CSN0/RM_IO19/GPIO0_C3_d	GPIO0_C3		SPI0_CSN0					RM_IO19		IO	I	down	Level2	√		
126	AUPLL_CLK_IN/RM_IO20/GPIO0_C4_d	GPIO0_C4		AUPLL_CLK_IN					RM_IO20		IO	I	down	Level2	√		
125	CPU_AVS/RM_IO21/GPIO0_C5_z	GPIO0_C5	CPU_AVS						RM_IO21		IO	I	z	Level2	√		
124	UART0_TX/JTAG_TCK_M1/RM_IO22/GPIO0_C6_u	GPIO0_C6	UART0_TX	JTAG_TCK_M1					RM_IO22		IO	I	up	Level2	√		
123	UART0_RX/JTAG_TMS_M1/RM_IO23/GPIO0_C7_u	GPIO0_C7	UART0_RX	JTAG_TMS_M1					RM_IO23		IO	I	up	Level2	√		
83	FLEXBUS1_D0/GPIO1_A0_d	GPIO1_A0		FLEXBUS1_D0							IO	I	down	Level2	√		VCCIO1_VCC
84	FLEXBUS1_D1/GPIO1_A1_d	GPIO1_A1		FLEXBUS1_D1							IO	I	down	Level2	√		
88	FLEXBUS1_D2/GPIO1_A2_d	GPIO1_A2		FLEXBUS1_D2							IO	I	down	Level2	√		
89	FLEXBUS1_D3/GPIO1_A3_d	GPIO1_A3		FLEXBUS1_D3							IO	I	down	Level2	√		
90	FLEXBUS1_D4/GPIO1_A4_d	GPIO1_A4		FLEXBUS1_D4							IO	I	down	Level2	√		
91	FLEXBUS1_D5/GPIO1_A5_d	GPIO1_A5		FLEXBUS1_D5							IO	I	down	Level2	√		
93	FLEXBUS1_D6/GPIO1_A6_d	GPIO1_A6		FLEXBUS1_D6							IO	I	down	Level2	√		
94	FLEXBUS1_D7/GPIO1_A7_d	GPIO1_A7		FLEXBUS1_D7							IO	I	down	Level2	√		
95	FLEXBUS1_D8/FLEXBUS0_CSN_M0/GPIO1_B0_d	GPIO1_B0		FLEXBUS1_D8		FLEXBUS0_CSN_M0					IO	I	down	Level2	√		
96	FLEXBUS1_D9/FLEXBUS1_CSN_M0/UART5_CTSN_M1/RM_IO24/GPIO1_B1_d	GPIO1_B1		FLEXBUS1_D9		FLEXBUS1_CSN_M0	UART5_CTSN_M1	RM_IO24			IO	I	down	Level2	√		
97	FLEXBUS1_D10/FLEXBUS0_D15/FLEXBUS0_CSN_M1/SAI2_SCLK_M1/RM_IO25/GPIO1_B2_d	GPIO1_B2		FLEXBUS1_D10	FLEXBUS0_D15	FLEXBUS0_CSN_M1	SAI2_SCLK_M1	RM_IO25			IO	I	down	Level2	√		
98	FLEXBUS1_D11/FLEXBUS0_D14/FLEXBUS1_CSN_M1/SAI2_LRCK_M1/RM_IO26/GPIO1_B3_d	GPIO1_B3		FLEXBUS1_D11	FLEXBUS0_D14	FLEXBUS1_CSN_M1	SAI2_LRCK_M1	RM_IO26			IO	I	down	Level2	√		
99	FLEXBUS1_D12/FLEXBUS0_D13/FLEXBUS0_CSN_M2/GPIO1_B4_d	GPIO1_B4		FLEXBUS1_D12	FLEXBUS0_D13	FLEXBUS0_CSN_M2					IO	I	down	Level2	√		
100	FLEXBUS1_D13/FLEXBUS0_D12/FLEXBUS1_CSN_M2/GPIO1_B5_d	GPIO1_B5		FLEXBUS1_D13	FLEXBUS0_D12	FLEXBUS1_CSN_M2					IO	I	down	Level2	√		
101	FLEXBUS1_D14/FLEXBUS0_D11/FLEXBUS0_CSN_M3/GPIO1_B6_d	GPIO1_B6		FLEXBUS1_D14	FLEXBUS0_D11	FLEXBUS0_CSN_M3					IO	I	down	Level2	√		

Pin	Pin Name	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Pad Type ^①	Def ^③	Pull	Drive Strength ^②	INT	Power Domain	
102	FLEXBUS1_D15/FLEXBUS0_D10/FLEXBUS1_CSN_M3/GPIO1_B7_d	GPIO1_B7		FLEXBUS1_D15	FLEXBUS0_D10	FLEXBUS1_CSN_M3					IO	I	down	Level2	✓	VCCIO1_VCC	
104	FLEXBUS1_CLK/FLEXBUS0_CSN_M4/GPIO1_C0_d	GPIO1_C0		FLEXBUS1_CLK		FLEXBUS0_CSN_M4					IO	I	down	Level2	✓		
105	FLEXBUS0_CLK/DSM_AUD_RN_M0/FLEXBUS1_CSN_M4/SAI2_MCLK_M1/GPIO1_C1_d	GPIO1_C1		FLEXBUS0_CLK	DSM_AUD_RN_M0	FLEXBUS1_CSN_M4	SAI2_MCLK_M1				IO	I	down	Level2	✓		
106	FLEXBUS0_D9/DSM_AUD_RP_M0/FLEXBUS0_CSN_M5/SAI2_SDI_M1/RM_IO27/GPIO1_C2_d	GPIO1_C2		FLEXBUS0_D9	DSM_AUD_RP_M0	FLEXBUS0_CSN_M5	SAI2_SDI_M1	RM_IO27			IO	I	down	Level2	✓		
107	FLEXBUS0_D8/FLEXBUS1_CSN_M5/SAI2_SDO_M1/RM_IO28/GPIO1_C3_d	GPIO1_C3		FLEXBUS0_D8		FLEXBUS1_CSN_M5	SAI2_SDO_M1	RM_IO28			IO	I	down	Level2	✓		
108	FLEXBUS0_D7/GPIO1_C4_d	GPIO1_C4		FLEXBUS0_D7							IO	I	down	Level2	✓		
109	FLEXBUS0_D6/GPIO1_C5_d	GPIO1_C5		FLEXBUS0_D6							IO	I	down	Level2	✓		
113	FLEXBUS0_D5/GPIO1_C6_d	GPIO1_C6		FLEXBUS0_D5							IO	I	down	Level2	✓		
114	FLEXBUS0_D4/GPIO1_C7_d	GPIO1_C7		FLEXBUS0_D4							IO	I	down	Level2	✓		
115	FLEXBUS0_D3/DSM_AUD_LN_M0/GPIO1_D0_d	GPIO1_D0		FLEXBUS0_D3	DSM_AUD_LN_M0						IO	I	down	Level2	✓		
116	FLEXBUS0_D2/DSM_AUD_LP_M0/UART5_RTSN_M1/RM_IO29/GPIO1_D1_d	GPIO1_D1		FLEXBUS0_D2	DSM_AUD_LP_M0		UART5_RTSN_M1	RM_IO29			IO	I	down	Level2	✓		
117	FLEXBUS0_D1/UART5_TX_M1/RM_IO30/GPIO1_D2_d	GPIO1_D2		FLEXBUS0_D1			UART5_TX_M1	RM_IO30			IO	I	down	Level2	✓		
118	FLEXBUS0_D0/UART5_RX_M1/RM_IO31/GPIO1_D3_d	GPIO1_D3		FLEXBUS0_D0			UART5_RX_M1	RM_IO31			IO	I	down	Level2	✓		
59	FSPI_CSN/GPIO2_A0_u	GPIO2_A0	FSPI_CSN								IO	I	up	Level2	✓		VCCIO2_VCC
54	FSPI_CLK/GPIO2_A1_d	GPIO2_A1	FSPI_CLK								IO	I	down	Level3	✓		
55	FSPI_D0/GPIO2_A2_u	GPIO2_A2	FSPI_D0								IO	I	up	Level2	✓		
58	FSPI_D1/GPIO2_A3_u	GPIO2_A3	FSPI_D1								IO	I	up	Level2	✓		
57	FSPI_D2/GPIO2_A4_u	GPIO2_A4	FSPI_D2								IO	I	up	Level2	✓		
53	FSPI_D3/GPIO2_A5_u	GPIO2_A5	FSPI_D3								IO	I	up	Level2	✓	VCCIO3_VCC	
50	SPI2_CLK/GPIO2_B0_d	GPIO2_B0	SPI2_CLK								IO	I	down	Level2	✓		
49	SPI2_CSN/GPIO2_B1_d	GPIO2_B1	SPI2_CSN								IO	I	down	Level2	✓		
48	SPI2_MOSI/GPIO2_B2_d	GPIO2_B2	SPI2_MOSI								IO	I	down	Level2	✓		
47	SPI2_MISO/GPIO2_B3_d	GPIO2_B3	SPI2_MISO								IO	I	down	Level2	✓		
46	DSM_AUD_RN_M1/SAI3_SCLK/GPIO2_B4_d	GPIO2_B4	DSM_AUD_RN_M1	SAI3_SCLK							IO	I	down	Level2	✓		
45	DSM_AUD_RP_M1/SAI3_LRCK/GPIO2_B5_d	GPIO2_B5	DSM_AUD_RP_M1	SAI3_LRCK							IO	I	down	Level2	✓		
44	DSM_AUD_LN_M1/SAI3_SDI/GPIO2_B6_d	GPIO2_B6	DSM_AUD_LN_M1	SAI3_SDI							IO	I	down	Level2	✓		
43	DSM_AUD_LP_M1/SAI3_SDO/GPIO2_B7_d	GPIO2_B7	DSM_AUD_LP_M1	SAI3_SDO							IO	I	down	Level2	✓		
42	SAI3_MCLK/GPIO2_C0_d	GPIO2_C0		SAI3_MCLK							IO	I	down	Level2	✓		
37	SDMMC_CLK/GPIO3_A0_d	GPIO3_A0	SDMMC_CLK								IO	I	down	Level3	✓	VCCIO4_VCC	
38	SDMMC_CMD/GPIO3_A1_d	GPIO3_A1	SDMMC_CMD								IO	I	down	Level2	✓		
36	SDMMC_D0/GPIO3_A2_d	GPIO3_A2	SDMMC_D0								IO	I	down	Level2	✓		
35	SDMMC_D1/TEST_CLK_OUT/GPIO3_A3_d	GPIO3_A3	SDMMC_D1	TEST_CLK_OUT							IO	I	down	Level2	✓		
41	SDMMC_D2/JTAG_TCK_M0/GPIO3_A4_d	GPIO3_A4	SDMMC_D2	JTAG_TCK_M0							IO	I	down	Level2	✓		
40	SDMMC_D3/JTAG_TMS_M0/GPIO3_A5_d	GPIO3_A5	SDMMC_D3	JTAG_TMS_M0							IO	I	down	Level2	✓		
34	SAI2_SDI_M0/GPIO3_A6_d	GPIO3_A6	SAI2_SDI_M0								IO	I	down	Level2	✓		
33	SAI2_SCLK_M0/GPIO3_A7_d	GPIO3_A7	SAI2_SCLK_M0								IO	I	down	Level2	✓		
32	SAI2_SDO_M0/GPIO3_B0_d	GPIO3_B0	SAI2_SDO_M0								IO	I	down	Level2	✓		
31	SAI2_LRCK_M0/GPIO3_B1_d	GPIO3_B1	SAI2_LRCK_M0								IO	I	down	Level2	✓		
30	UART5_CTSN_M0/GPIO3_B2_d	GPIO3_B2	UART5_CTSN_M0								IO	I	down	Level2	✓		
29	UART5_RX_M0/GPIO3_B3_d	GPIO3_B3	UART5_RX_M0								IO	I	down	Level2	✓		
28	UART5_TX_M0/GPIO3_B4_d	GPIO3_B4	UART5_TX_M0								IO	I	down	Level2	✓		

Pin	Pin Name	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Pad Type ^①	Def ^③	Pull	Drive Strength ^②	INT	Power Domain
27	UART5_RTSN_M0/GPIO3_B5_d	GPIO3_B5	UART5_RTSN_M0								IO	I	down	Level2	✓	
26	SAI2_MCLK_M0/GPIO3_B6_d	GPIO3_B6	SAI2_MCLK_M0								IO	I	down	Level2	✓	
81	GPO4_A0_z	GPO4_A0									O	O	Z			
82	GPO4_A1_z	GPO4_A1									O	O	Z			
79	GPO4_A2_z	GPO4_A2									O	O	Z			
80	GPO4_A3_z	GPO4_A3									O	O	Z			
77	GPO4_A4_z	GPO4_A4									O	O	Z			
78	GPO4_A5_z	GPO4_A5									O	O	Z			
63	SARADC_IN0/GPIO4_B0_z	GPIO4_B0	SARADC_IN0								IO	I	z	Level1	✓	SARADC
62	SARADC_IN1/GPIO4_B1_z	GPIO4_B1	SARADC_IN1								IO	I	z	Level1	✓	
61	SARADC_IN2/GPIO4_B2_z	GPIO4_B2	SARADC_IN2								IO	I	z	Level1	✓	
60	SARADC_IN3/GPIO4_B3_z	GPIO4_B3	SARADC_IN3								IO	I	z	Level1	✓	
72	USB20_OTG0_DP	USB20_OTG0_DP									A					USB
71	USB20_OTG0_DM	USB20_OTG0_DM									A					
74	USB20_OTG1_DP	USB20_OTG1_DP									A					
73	USB20_OTG1_DM	USB20_OTG1_DM									A					
68	ACODEC_ADC_INP	ACODEC_ADC_INP									A					ACODEC ADC
67	ACODEC_ADC_INN	ACODEC_ADC_INN									A					
66	ACODEC_ADC_VCM	ACODEC_ADC_VCM									A					
65	ACODEC_ADC_AVDD1V6	ACODEC_ADC_AVDD1V6									A					

Notes:

- : Pad types: I = input, O = output, I/O = input/output (bidirectional)
 AP = Analog Power, AG = Analog Ground
 DP = Digital Power, DG = Digital Ground
 A = Analog
- : Output Drive Unit is mA, only Digital IO has drive value;
- : Reset state: I = input, O = output;

2.9 IO Pin Name Description

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 2-4 IO function description list

Interface	Pin Name	Direction	Description
Misc	OSC_XIN	I	Clock input of crystal XO
	OSC_XOUT	O	Clock output of crystal XO
	NPOR	I	Chip hardware reset input
	OSC_CLK_OUT	O	OSC Clock Output for external function module
	REF_CLK0_OUT	O	REF Clock Output for external function module
	REF_CLK1_OUT	O	REF Clock Output for external function module
	AUPLL_CLK_IN	I	REF Clock Input for internal PLL
	TEST_CLK_OUT	O	Chip internal clock output for measurement
	PMU_SLEEP	O	Chip low power mode output indication signal
	CORE_POWER_OFF	O	Chip low power mode output indication signal
	TSADC_CTRL	O	Chip high temperature output indication signal
	CLK_32K	I/O	32K clock If configured as input, clock is provided from external circuit; If configured as output, clock is provided from internal circuit of chip;

Interface	Pin Name	Direction	Description
SWJ-DP	JTAG_TCK_Mi (i=0~1)	I	SWD interface clock input for CPU
	JTAG_TMS_Mi (i=0~1)	I/O	SWD interface data input/output for CPU

Interface	Pin Name	Direction	Description
SD/MMC Host Controller	SDMMC_CLK	O	sdmmc card clock
	SDMMC_CMD	I/O	sdmmc card command output and response input
	SDMMC_D[i] (i=0~3)	I/O	sdmmc card data input and output

Interface	Pin Name	Direction	Description
FSPI Controller	FSPI_CLK	O	fspi serial clock
	FSPI_CSN	O	fspi chip select signal, low active
	FSPI_Di(i=0~3)	I/O	fspi serial data input/output signal

Interface	Pin Name	Direction	Description
SAI0	SAI0_MCLK	I/O	I2S/PCM/TDM master clock
	SAI0_SCLK	I/O	I2S/PCM/TDM serial clock
	SAI0_LRCK	I/O	I2S/PCM/TDM channel indication signal
	SAI0_SDO	O	I2S/PCM/TDM serial data output
	SAI0_SDI0	I	I2S/PCM/TDM serial data input
	SAI0_SDI1	I	I2S/PCM/TDM serial data input
	SAI0_SDI2	I	I2S/PCM/TDM serial data input
	SAI0_SDI3	I	I2S/PCM/TDM serial data input

Interface	Pin Name	Direction	Description
SAI1	SAI1_MCLK	I/O	I2S/PCM/TDM master clock
	SAI1_SCLK	I/O	I2S/PCM/TDM serial clock
	SAI1_LRCK	I/O	I2S/PCM/TDM channel indication signal
	SAI1_SDO0	O	I2S/PCM/TDM serial data output
	SAI1_SDO1	O	I2S/PCM/TDM serial data output
	SAI1_SDO2	O	I2S/PCM/TDM serial data output
	SAI1_SDO3	O	I2S/PCM/TDM serial data output
	SAI1_SDI	I	I2S/PCM/TDM serial data input

Interface	Pin Name	Direction	Description
SAI2	SAI2_MCLK_Mi(i=0~1)	I/O	I2S/PCM/TDM master clock
	SAI2_SCLK_Mi(i=0~1)	I/O	I2S/PCM/TDM serial clock
	SAI2_LRCK_Mi(i=0~1)	I/O	I2S/PCM/TDM channel indication signal
	SAI2_SDO_Mi(i=0~1)	O	I2S/PCM/TDM serial data output
	SAI2_SDI_Mi(i=0~1)	I	I2S/PCM/TDM serial data input

Interface	Pin Name	Direction	Description
SAI3	SAI3_MCLK	I/O	I2S/PCM/TDM master clock
	SAI3_SCLK	I/O	I2S/PCM/TDM serial clock
	SAI3_LRCK	I/O	I2S/PCM/TDM channel indication signal
	SAI3_SDO	O	I2S/PCM/TDM serial data output
	SAI3_SDI	I	I2S/PCM/TDM serial data input

Interface	Pin Name	Direction	Description
PDM	PDM_CLK0	O	PDM sampling clock
	PDM_CLK1	O	PDM sampling clock
	PDM_SDIj(i=0~3)	I	PDM data

Interface	Pin Name	Direction	Description
Audio DSM	DSM_AUD_RP_Mi(i=0~1)	O	Audio DSM Right Channel positive differential data output
	DSM_AUD_RN_Mi(i=0~1)	O	Audio DSM Right Channel negative differential data output

Interface	Pin Name	Direction	Description
	DSM_AUD_LP_Mi(i=0~1)	O	Audio DSM Left Channel positive differential data output
	DSM_AUD_LN_Mi(i=0~1)	O	Audio DSM Left Channel negative differential data output

Interface	Pin Name	Direction	Description
SPI0/SPI1	SPIi_CLK(i=0~1)	I/O	SPI serial clock
	SPIi_CSN0(i=0~1)	I/O	SPI chip select signal, low active
	SPIi_CSN1(i=0~1)	O	SPI chip select signal, low active
	SPIi_MISO(i=0~1)	I/O	SPI serial data input/output
	SPIi_MOSI(i=1~2)	I/O	SPI serial data input/output

Interface	Pin Name	Direction	Description
SPI2	SPI2_CLK	I	SPI serial clock
	SPI2_CSN)	I	SPI chip select signal, low active
	SPI2_MOSI	I	SPI serial data input
	SPI2_MISO	O	SPI serial data output

Interface	Pin Name	Direction	Description
PWM	PWM0_CHi(i=0~3)	I/O	Pulse Width Modulation input and output
	PWM1_CHi(i=0~7)	I/O	Pulse Width Modulation input and output
	PWM1_BIP_CNTR_Ai(i=0~5)	I	Phase A input for AB phase counter
	PWM1_BIP_CNTR_Bi(i=0~5)	I	Phase B input for AB phase counter

Interface	Pin Name	Direction	Description
I2C	I2Ci_SDA(i=0,1,2)	I/O	I2C data
	I2Ci_SCL(i=0,1,2)	I/O	I2C clock

Interface	Pin Name	Direction	Description
UART	UART0_RX	I	UART serial data input
	UART0_TX	O	UART serial data output
	UARTi_RX(i=1,2,3,4)	I	UART serial data input
	UARTi_TX(i=1,2,3,4)	O	UART serial data output
	UARTi_CTSN(i=1,2,3,4)	I	UART clear to send modem status input

Interface	Pin Name	Direction	Description
	UART _i _RTSN (<i>i</i> =1,2,3,4)	O	UART modem control request to send output
	UART5_RX_Mi(<i>i</i> =0~1)	I	UART serial data input
	UART5_TX_Mi(<i>i</i> =0~1)	O	UART serial data output
	UART5_CTSN_Mi(<i>i</i> =0~1)	I	UART clear to send modem status input
	UART5_RTSN_Mi(<i>i</i> =0~1)	O	UART modem control request to send output

Interface	Pin Name	Direction	Description
Touch Key	TOUCH_KEY_INi(<i>i</i> =0~7)	I	Touch Key data input
	TOUCH_KEY_DRIVE	O	Touch Key drive clock output

Interface	Pin Name	Direction	Description
FLEXBUS	FLEXBUS0_CLK	O	FLEXBUS0 clock output
	FLEXBUS0_Di(<i>i</i> =0~15)	I/O	FLEXBUS0 data input/output
	FLEXBUS1_CLK	I/O	FLEXBUS1 clock input/output DVP mode, acted as VICAP_CLK input
	FLEXBUS1_Di(<i>i</i> =0~15)	I	FLEXBUS0 data input DVP mode, FLEXBUS1_D6 and FLEXBUS1_D7 acted as VICAP_VSYNC and VICAP_HREF input signal separately. FLEXBUS1_D8~FLEXBUS1_D16 acted as VICAP_DATA0~VICAP_DATA7 input signal.
	FLEXBUS0_CSN_Mi(<i>i</i> =0~5)	O	FLEXBUS0 chip selection output
	FLEXBUS1_CSN_Mi(<i>i</i> =0~5)	O	FLEXBUS1 chip selection output

Interface	Pin Name	Direction	Description
Rockchip matrix IO	RM_IOi(<i>i</i> =0~31)	I/O	IO matrix

Interface	Pin Name	Direction	Description
SARADC	SARADC_INi(<i>i</i> =0~3)	I/O	SARADC input signal for 4 channel

Interface	Pin Name	Direction	Description
USB 2.0	USB20_OTG0_DP	I/O	USB 2.0 Port0 Data signal DP
	USB20_OTG0_DM	I/O	USB 2.0 Port0 Data signal DM
	USB20_OTG1_DP	I/O	USB 2.0 Port1 Data signal DP

	USB20_OTG1_DM	I/O	USB 2.0 Port1 Data signal DM
	USB20_OTG0_VBUS DET	I	Port0 insert detect when act as USB device
	USB20_OTG0_ID	I	Port0 USB Mini-Receptacle Identifier

Interface	Pin Name	Direction	Description
ACODEC ADC	ACODEC_ADC_INP	I	ADC input signal
	ACODEC_ADC_INN	I	ADC input signal
	ACODEC_ADC_VCM	O	Internal voltage output
	ACODEC_ADC_AVDD 1V6	O	Internal voltage output

Interface	Pin Name	Direction	Description
DDR Interface	DDR_CLKP	O	Active-high clock signal to the memory device.
	DDR_CLKN	O	Active-low clock signal to the memory device.
	DDR_CKE	O	Active-high clock enable signal to the memory device
	DDR_CSN	O	Active-low chip select signal to the memory device.
	DDR2_RASN/DDR3_A 10	O	DDR2: Active-low row address strobe to the memory device. DDR3: Address signal to the memory device.
	DDR2_CASN/DDR3_B A1	O	DDR2: Active-low column address strobe to the memory device. DDR3: Bank address signal to the memory device.
	DDR2_WEN/DDR3_R ASN	O	DDR2: Active-low write enable strobe to the memory device. DDR3: Active-low row address strobe to the memory device.
	DDR2_BA0/DDR3_CA SN	O	DDR2: Bank address signal to the memory device. DDR3: Active-low column address strobe to the memory device.
	DDR2_BA1/DDR3_W EN	O	DDR2: Bank address signal to the memory device. DDR3: Active-low write enable strobe to the memory device.
	DDR2_BA2/DDR3_BA 2	O	DDR2: Bank address signal to the memory device. DDR3: Bank address signal to the memory device.
	DDR2_A0/DDR3_A12	O	DDR2: Address signal to the memory device. DDR3: Address signal to the memory device.
	DDR2_A1/DDR3_A3	O	DDR2: Address signal to the memory device.

Interface	Pin Name	Direction	Description
			DDR3: Address signal to the memory device.
	DDR2_A2/DDR3_A4	O	DDR2: Address signal to the memory device. DDR3: Address signal to the memory device.
	DDR2_A3/DDR3_A0	O	DDR2: Address signal to the memory device. DDR3: Address signal to the memory device.
	DDR2_A4/DDR3_A1	O	DDR2: Address signal to the memory device. DDR3: Address signal to the memory device.
	DDR2_A5/DDR3_A5	O	DDR2: Address signal to the memory device. DDR3: Address signal to the memory device.
	DDR2_A6/DDR3_A6	O	DDR2: Address signal to the memory device. DDR3: Address signal to the memory device.
	DDR2_A7/DDR3_A2	O	DDR2: Address signal to the memory device. DDR3: Address signal to the memory device.
	DDR2_A8/DDR3_A8	O	DDR2: Address signal to the memory device. DDR3: Address signal to the memory device.
	DDR2_A9/DDR3_A7	O	DDR2: Address signal to the memory device. DDR3: Address signal to the memory device.
	DDR2_A10/DDR3_BA0	O	DDR2: Address signal to the memory device. DDR3: Bank address signal to the memory device.
	DDR2_A11/DDR3_A11	O	DDR2: Address signal to the memory device. DDR3: Address signal to the memory device.
	DDR2_A12/DDR3_A9	O	DDR2: Address signal to the memory device. DDR3: Address signal to the memory device.
	DDR2_A13/DDR3_A13	O	DDR2: Address signal to the memory device. DDR3: Address signal to the memory device.
	DDR2_A14/DDR3_A14	O	DDR2: Address signal to the memory device. DDR3: Address signal to the memory device.
	DDR2_A15/DDR3_A15	O	DDR2: Address signal to the memory device. DDR3: Address signal to the memory device.
	DDR_DQ i ($i=0\sim 15$)	I/O	Bidirectional data line to the memory device.
	DDR_DQS i P($i=0\sim 1$)	I/O	Active-high bidirectional data strobes to the memory device.
	DDR_DQS i N($i=0\sim 1$)	I/O	Active-low bidirectional data strobes to the memory device.
	DDR_DM i ($i=0\sim 1$)	O	Data mask signal to the memory device.
	DDR_ODT	O	On-Die Termination output signal.
	DDR3_RESET	O	Reset signal to the memory device.
	DDR_VREF_CA	O	CA VREF for DDR
	DDR_VREF_DQ	O	DQ VREF for DDR
	DDR_RZQ	O	RZQ for DDR
	DDR_OPEN0	O	Debug IO
	DDR_OPEN1	O	Debug IO

2.10 Rockchip Matrix IO Function List

RK3502G2 supports one Rockchip Matrix IO (RM_IO) which are designed to let numerous functional signals share limited pin interfaces. Within the same matrix, any function signal can be mapped to any pin interface by software configurable. RM_IO support 98 function signals map to 32 pin interfaces (GPIO0_A0~GPIO0_C7, GPIO1_B1~GPIO1_B3, GPIO1_C2~GPIO1_C3, GPIO1_D1~GPIO1_D3)

Table 2-5 Matrix IO function list

Function Index	RM_IO	Function Index	RM_IO
1	UART1_TX	46	SAI0_MCLK
2	UART1_RX	47	SAI0_SCLK
3	UART2_TX	48	SAI0_LRCK
4	UART2_RX	49	SAI0_SDI0
5	UART3_TX	50	SAI0_SDI1
6	UART3_RX	51	SAI0_SDI2
7	UART3_CTSN	52	SAI0_SDI3
8	UART3_RTSN	53	SAI0_SDO
9	UART4_TX	54	SAI1_MCLK
10	UART4_RX	55	SAI1_SCLK
11	UART4_CTSN	56	SAI1_LRCK
12	UART4_RTSN	57	SAI1_SDI
13	CLK_32K	58	SAI1_SDO0
14	I2C0_SCL	59	SAI1_SDO1
15	I2C0_SDA	60	SAI1_SDO2
16	I2C1_SCL	61	SAI1_SDO3
17	I2C1_SDA	62	SPI0_CLK
18	I2C2_SCL	63	SPI0_MOSI
19	I2C2_SDA	64	SPI0_MISO
20	PDM_CLK0	65	SPI0_CSN0
21	PDM_SDI0	66	SPI0_CSN1
22	PDM_SDI1	67	SPI1_CLK
23	PDM_SDI2	68	SPI1_MOSI
24	PDM_SDI3	69	SPI1_MISO
25	PWM0_CH0	70	SPI1_CSN0
26	PWM0_CH1	71	SPI1_CSN1
27	PWM0_CH2	72	TSADC_CTRL
28	PWM0_CH3	73	PMU_SLEEP
29	PWM1_CH0	74	CORE_POWER_OFF
30	PWM1_CH1	75	

Function Index	RM_IO	Function Index	RM_IO
31	PWM1_CH2	76	
32	PWM1_CH3	77	PWM1_BIP_CNTR_A0
33	PWM1_CH4	78	PWM1_BIP_CNTR_A1
34	PWM1_CH5	79	PWM1_BIP_CNTR_A2
35	PWM1_CH6	80	PWM1_BIP_CNTR_A3
36	PWM1_CH7	81	PWM1_BIP_CNTR_A4
37	TOUCH_KEY_DRIVE	82	PWM1_BIP_CNTR_A5
38	TOUCH_KEY_IN0	83	PWM1_BIP_CNTR_B0
39	TOUCH_KEY_IN1	84	PWM1_BIP_CNTR_B1
40	TOUCH_KEY_IN2	85	PWM1_BIP_CNTR_B2
41	TOUCH_KEY_IN3	86	PWM1_BIP_CNTR_B3
42	TOUCH_KEY_IN4	87	PWM1_BIP_CNTR_B4
43	TOUCH_KEY_IN5	88	PWM1_BIP_CNTR_B5
44	TOUCH_KEY_IN6	89	PDM_CLK1
45	TOUCH_KEY_IN7		

2.11 FLEXBUS Interface Typical Application Example

RK3502G2 FLEXBUS can be adapted to certain timing interface through software programming. In this section, we will list the pin mapping relationship for some typical application interfaces, such as ADC, DAC, DVP panel.

Table 2-6 Pin Mapping between FLEXBUS and ADC

FLEXBUS Interface	Direction	ADC Application Interface
FLEXBUS1_D0	Input	ADC_D0
FLEXBUS1_D1	Input	ADC_D1
FLEXBUS1_D2	Input	ADC_D2
FLEXBUS1_D3	Input	ADC_D3
FLEXBUS1_D4	Input	ADC_D4
FLEXBUS1_D5	Input	ADC_D5
FLEXBUS1_D6	Input	ADC_D6
FLEXBUS1_D7	Input	ADC_D7
FLEXBUS1_D8	Input	ADC_D8
FLEXBUS1_D9	Input	ADC_D9
FLEXBUS1_D10	Input	ADC_D10
FLEXBUS1_D11	Input	ADC_D11
FLEXBUS1_D12	Input	ADC_D12
FLEXBUS1_D13	Input	ADC_D13
FLEXBUS1_D14	Input	ADC_D14

FLEXBUS1_D15	Input	ADC_D15
FLEXBUS1_CLK	Input Output	ADC_CLK_IN(from ADC) ADC_CLK_OUT(To ADC)

Table 2-7 Pin Mapping between FLEXBUS and DAC

FLEXBUS Interface	Direction	DAC Application Interface
FLEXBUS0_D0	Output	DAC_D0
FLEXBUS0_D1	Output	DAC_D1
FLEXBUS0_D2	Output	DAC_D2
FLEXBUS0_D3	Output	DAC_D3
FLEXBUS0_D4	Output	DAC_D4
FLEXBUS0_D5	Output	DAC_D5
FLEXBUS0_D6	Output	DAC_D6
FLEXBUS0_D7	Output	DAC_D7
FLEXBUS0_D8	Output	DAC_D8
FLEXBUS0_D9	Output	DAC_D9
FLEXBUS0_D10	Output	DAC_D10
FLEXBUS0_D11	Output	DAC_D11
FLEXBUS0_D12	Output	DAC_D12
FLEXBUS0_D13	Output	DAC_D13
FLEXBUS0_D14	Output	DAC_D14
FLEXBUS0_D15	Output	DAC_D15
FLEXBUS0_CLK	Output	DAC_CLK
FLEXBUS0_CSN	Output	DAC_CS

Table 2-8 Pin Mapping between FLEXBUS and DVP Camera

FLEXBUS Interface	Direction	DVP Application Interface
FLEXBUS1_D6	Input	VI_CIF_VSYNC
FLEXBUS1_D7	Input	VI_CIF_HREF
FLEXBUS1_D8	Input	VI_CIF_D0
FLEXBUS1_D9	Input	VI_CIF_D1
FLEXBUS1_D10	Input	VI_CIF_D2
FLEXBUS1_D11	Input	VI_CIF_D3
FLEXBUS1_D12	Input	VI_CIF_D4
FLEXBUS1_D13	Input	VI_CIF_D5
FLEXBUS1_D14	Input	VI_CIF_D6
FLEXBUS1_D15	Input	VI_CIF_D7
FLEXBUS1_CLK	Input	VI_CIF_CLK

Chapter 3 Electrical Specification

3.1 Absolute Ratings

The below table provides the absolute ratings.

Absolute maximum or minimum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

Table 3-1 Absolute ratings

Parameters	Related Power Group	Min	Max	Unit
Supply voltage for CPU	CPU_DVDD	-0.30	TBD	V
Supply voltage for LOGIC	LOGIC_DVDD	-0.30	1.05	V
Supply voltage for PMU	PMU_LOGIC_DVDD0V9	-0.30	1.05	V
0.9V supply voltage	AVDD_0V9 USB20_OTG_DVDD0V9	-0.30	1.05	V
1.8V supply voltage	SYS_PLL_AVDD1V8 AVDD_1V8 AVCC_1V8 ACODEC_ADC_AVDD1V8 SARADC_AVDD1V8 TSADC_VCC1V8 USB20_OTG_AVDD1V8	-0.30	2.10	V
3.3V supply voltage	PMUIO_VCC3V3 USB20_OTG_AVDD3V3	-0.30	3.80	V
1.8V/3.3V supply voltage	VCCIO1_VCC VCCIO2_VCC VCCIO3_VCC VCCIO4_VCC	-0.30	3.80	V
Supply voltage for DDR IO	DDR_VDDQ	-0.30	2.00	V
Storage Temperature	Tstg	-40	125	°C
Max Conjunction Temperature	Tj		125	°C

3.2 Recommended Operating Condition

The following table describes the recommended operating condition.

Table 3-2 Recommended operating condition

Parameters	Symbol	Min	Typ	Max	Unit
Voltage for CPU	CPU_DVDD	0.81	0.90	TBD	V
Voltage for LOGIC	LOGIC_DVDD	0.81	0.90	0.99	V
Voltage for PMU	PMU_LOGIC_DVDD0V9	0.81	0.90	0.99	V
Voltage for PLL Analog (1.8V)	SYS_PLL_AVDD1V8	1.62	1.80	1.98	V
Voltage for GPIO (3.3V only)	PMUIO_VCC3V3	3.00	3.30	3.63	V
Voltage for GPIO (1.8V/3.3V)	VCCIO1_VCC VCCIO2_VCC VCCIO3_VCC VCCIO4_VCC	1.62 3.00	1.80 3.30	1.98 3.63	V
Voltage for USB Analog(0.9V)	AVDD_0V9	0.81	0.90	0.99	V

Parameters	Symbol	Min	Typ	Max	Unit
Voltage for USB/TSADC Analog (1.8V)	AVDD_1V8	1.62	1.80	1.98	V
Voltage for ACODEC ADC/SARADC/OTP Analog (1.8V)	AVCC_1V8	1.62	1.80	1.98	V
Voltage for ACODEC ADC Analog (1.8V)	ACODEC_ADC_AVDD1V8	1.62	1.80	1.98	V
Voltage for SARADC/OTP Analog (1.8V)	SARADC_AVDD1V8	1.62	1.80	1.98	V
Voltage for TSADC Analog (1.8V)	TSADC_VCC1V8	1.62	1.80	1.98	V
Voltage for USB Analog (0.9V)	USB20_OTG_DVDD0V9	0.81	0.90	0.99	V
Voltage for USB Analog (1.8V)	USB20_OTG_AVDD1V8	1.62	1.8	1.98	V
Voltage for USB Analog (3.3V)	USB20_OTG_AVDD3V3	3.00	3.30	3.63	V
DDR2 IO power	DDR_VDDQ	1.71	1.80	1.89	V
DDR3 IO power	DDR_VDDQ	1.425	1.50	1.575	V
DDR3L IO Power	DDR_VDDQ	1.283	1.35	1.418	V
OSC input clock frequency	F _{osc}	N/A	24	N/A	MHz
Ambient Operating Temperature	T _A	-20	25	80	°C

Notes: Please refer to "Power/Ground IO Description" section for relationship between power symbol and chip model

3.3 DC Characteristics

Table 3-3 DC Characteristics

Parameters	Symbol	Min	Typ	Max	Unit	
Digital GPIO @3.3V	Input Low Voltage	V _{il}	-0.3	NA	0.8	V
	Input High Voltage	V _{ih}	2.0	NA	VDDO+0.3	V
	Output Low Voltage	V _{ol}	-0.3	NA	0.4	V
	Output High Voltage	V _{oh}	2.4	NA	VDDO+0.3	V
	Pullup Resistor	R _{pu}	16	30	43	Kohm
	Pulldown Resistor	R _{pd}	16	30	43	Kohm
Digital GPIO @1.8V	Input Low Voltage	V _{il}	-0.3	NA	0.35*VDDO	V
	Input High Voltage	V _{ih}	0.65*VDDO	NA	VDDO+0.3	V
	Output Low Voltage	V _{ol}	-0.3	NA	0.4	V
	Output High Voltage	V _{oh}	1.4	NA	VDDO+0.3	V
	Pullup Resistor	R _{pu}	16	30	43	Kohm
	Pulldown Resistor	R _{pd}	16	30	43	Kohm

Parameters	Symbol	Min	Typ	Max	Unit	
DDR IO @ DDR2 mode	Input High Voltage	V _{ih_dds}	VREF + 0.13	NA	DDR_VDDQ	V
	Input Low Voltage	V _{il_dds}	VSS	NA	VREF - 0.13	V
	Output High Voltage	V _{oh_dds}	VREF + 0.13	NA	DDR_VDDQ	V
	Output Low Voltage	V _{ol_dds}	VSS	NA	VREF-0.13	V
DDR IO @ DDR3 mode	Input High Voltage	V _{ih_dds}	VREF + 0.10	NA	DDR_VDDQ	V
	Input Low Voltage	V _{il_dds}	VSS	NA	VREF - 0.10	V
	Output High Voltage	V _{oh_dds}	VREF + 0.10	NA	DDR_VDDQ	V
	Output Low Voltage	V _{ol_dds}	VSS	NA	VREF - 0.10	V
	Input High Voltage	V _{ih_dds}	VREF + 0.09	NA	DDR_VDDQ	V

Parameters		Symbol	Min	Typ	Max	Unit
DDR IO @ @DDR3L mode	Input Low Voltage	Vil_dds	VSS	NA	VREF - 0.09	V
	Output High Voltage	Voh_dds	VREF + 0.09	NA	DDR_VDDQ	V
	Output Low Voltage	Vol_dds	VSS	NA	VREF - 0.09	V

3.4 Electrical Characteristics for General IO

Table 3-4 Electrical Characteristics for Digital General IO

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
Digital GPIO @3.3V	Input leakage current	Ii	Vin = 3.3V or 0V	NA	NA	15	uA
	Tri-state output leakage current	Ioz	Vout = 3.3V or 0V	NA	NA	15	uA
	High level input current	Iih	Vin = 3.3V, pulldown disabled	NA	NA	15	uA
			Vin = 3.3V, pulldown enabled	NA	NA	250	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	NA	NA	15	uA
			Vin = 0V, pullup enabled	NA	NA	250	uA
Digital GPIO @1.8V	Input leakage current	Ii	Vin = 1.8V or 0V	NA	NA	15	uA
	Tri-state output leakage current	Ioz	Vout = 1.8V or 0V	NA	NA	15	uA
	High level input current	Iih	Vin = 1.8V, pulldown disabled	NA	NA	15	uA
			Vin = 1.8V, pulldown enabled	NA	NA	150	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	NA	NA	15	uA
			Vin = 0V, pullup enabled	NA	NA	150	uA

3.5 Electrical Characteristics for PLL

Table 3-5 Electrical Characteristics for FRAC PLL

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
	Input clock frequency(Frac)	F _{in}	Fin = FREF	10	NA	1200	MHz
	VCO operating range	F _{vco}	Fvco = FREF * FBDIV	950	NA	3800	MHz
	Output clock frequency	F _{out}	Fout = Fvco/POSTDIV	19	NA	3800	MHz
	Lock time	T _{lt}	FREF=24M,REFDIV=1	NA	250	500	Input clock cycles

Notes:

① REFDIV is the input divider value;

② FBDIV is the feedback divider value;

③ POSTDIV is the output divider value.

3.6 Electrical Characteristics for USB2.0 Interface

Table 3-6 Electrical Characteristics for USB2.0 Interface

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Transmitter						
Output Resistance	ROUT	Classic mode (Vout = 0 or 3.3V)	40.5	45	49.5	ohms
		HS mode (Vout = 0 to 800mV)	40.5	45	49.5	ohms
Output Capacitance	COUT	seen from D+ or D-			3	pF
Output Common Mode Voltage	VM	Classic (LS/FS) mode	1.45	1.65	1.85	V
		HS mode	0.175	0.2	0.225	V
Differential output signal high	VOH	Classic (LS/FS); Io=0mA	2.97	3.3	3.63	V
		Classic (LS/FS); Io=6mA	2.2	2.7	NA	V
		HS mode; Io=0mA	360	400	440	mV
Differential output signal low	VOL	Classic (LS/FS); Io=0mA	-0.33	0	0.33	V
		Classic (LS/FS); Io=6mA	NA	0.3	0.8	V
		HS mode; Io=0mA	-40	0	40	mV
Receiver						
Receiver sensitivity	RSENS	Classic mode	NA	+ -250	NA	mV
		HS mode	NA	+ -25	NA	mV
Receiver common mode	RCM	Classic mode	0.8	1.65	2.5	V
		HS mode (differential and squelch comparator)	0.1	0.2	0.3	V
		HS mode (disconnect comparator)	0.5	0.6	0.7	V
Input capacitance (seen at D+ or D-)			NA	NA	3	pF
Squelch threshold			100	NA	150	mV
Disconnect threshold			570	600	664	mV

3.7 Electrical Characteristics for SARADC

Table 3-7 Electrical Characteristics for SARADC

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Resolution			NA	10	NA	bit
Effective Number of Bit	ENOB		NA	9	NA	bit
Differential Non-Linearity	DNL		-1	NA	+1	LSB
Integral Non-Linearity	INL		-2	NA	+2	LSB
Reference voltage	VREFP		NA	1.8	NA	V
Input Capacitance	C _{IN}		NA	8	NA	pF
Sampling Rate	f _S		NA	NA	1	MS/s
Spurious Free Dynamic Range	SFDR	f _S =1MS/s f _{OUT} =1.17KHz	NA	61	NA	dB

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Signal to Noise and Harmonic Ratio	SNDR		NA	56	NA	dB

3.8 Electrical Characteristics for TSADC

Table 3-8 Electrical Characteristics for TSADC

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Accuracy from -40°C to 125°C	T _{JACC}		NA	NA	±5	°C
Sensing Temperature Range	T _{RANGE}		-40	NA	125	°C
Resolution	T _{LSB}		NA	0.6	NA	°C

3.9 Electrical Characteristics for CODEC ADC

Table 3-9 Electrical Characteristics for CODEC ADC

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Resolution				24		°C
Full Scale Input Range		0dB Gain in PGA state		+/- 1.0		V _{rms}
Input Resistance	R _{IN}			20		Kohm
Input Capacitance	C _{IN}			10		pF
Negative Gain Range	G(negative)		-9		0	dB
Negative Gain Step				3		dB/Step
Positive Gain Range	G(positive)		0		48	dB
Positive Gain Step				12		dB/Step
Signal to Noise Ratio	SNR	f _s =48kHz -60dBFS, A-weighted		94		dB
Total Harmonic Distortion	THD	f _s =48kHz -3dBFS, A-weighted		98		dB
Power Supply Rejection	PSRR			90		dB

Chapter 4 Thermal Management

4.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature has to be below 125°C.

4.2 Package Thermal Characteristics

Table 4-1 provides the thermal resistance characteristics for the package used on the SoC. The resulting simulation data for reference only, please prevail in kind test.

Table 4-1 Thermal Resistance Characteristics

Parameter	Symbol	Value	Unit	Note
Junction-to-ambient thermal resistance	θ_{JA}	TBD	(°C/W)	(1)
Junction-to-board thermal resistance	θ_{JB}	TBD	(°C/W)	(2)
Junction-to-case thermal resistance	θ_{JC}	TBD	(°C/W)	(3)
Thermal characterization parameter	ψ_{JT}	TBD	(°C/W)	(4)

Note (1): The package-board system is placed in the natural convection (JEDEC JESD51-2 standard), and the 2S2P test-board is designed in accordance with JESD 51-7/JESD 51-9. The actual system design and environment may be different. (The PCB is 4 layers, 114.3 mm*76.2 mm)

Note (2): θ_{JB} is measured in the special environment (JEDEC JESD51-8 standard), and the printed circuit board used to mount the devices is specified in JESD51-7.

Note (3): The thermal resistance θ_{JC} is provided in compliance with the JEDEC JESD51-14.

Note (4): ψ_{JT} - The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package, ψ_{JT} is measured in the test environment of θ_{JA} (JEDEC JESD51-2 standard).