Rockchip RK3506G2 Datasheet

Revision 1.5
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Revision History

Date	Revision	Description
2026-04-13	1.5	1. Add RMII 10/100 Ethernet Controller feature in 1.2.9 2. Add DDR rate in 1.2.10 Package Type 3. Correct flexbus interface name in Table 2-14 4. Update maximum absolute supply voltage for CPU in Table 3-1 5. Update minimum and maximum recommended operating supply voltage for CPU and Logic in Table 3-2
2025-09-30	1.4	Update the description of CAN
2025-07-22	1.3	Update package dimension
2025-04-30	1.2	Update the bit clock information of audio interface
2025-04-11	1.1	Update the DDR frequency and thermal resistance parameters; Update the POD thickness
2024-08-16	1.0	Initial release

Table of Content

Figure Index

Table Index

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Chapter 1 Introduction

1.1 Overview

RK3506G2 is a high-performance triple core Cortex-A7 application processor designed for intelligent voice interaction, audio input/output processing, image output processing and other digital multimedia applications.
Embedded 2D hardware engine and display output engine for minimizing CPU overhead to meet image display requirements.
Embedded rich peripheral interfaces, such as SAI, PDM, SPDIF, Audio DSM, Audio ADC, USB2 OTG, RMII, CAN and so on, can meet different application development, reduce hardware development complexity and development cost.
RK3506G2 has high-performance external memory interface capable of sustaining demanding memory bandwidths. Integrated 128MB DDR3 is available for customer.

1.2 Features

1.2.1 Microprocessor

- Triple-core ARM Cortex-A7 CPU
- ARM architecture v7-A instruction set
- ARM Neon Advanced SIMD (single instruction, multiple data) support for accelerated media and signal processing computation
- Include VFPv4-D32 hardware to support single and double-precision operations
- Integrated 16KB L1 instruction cache, 16KB L1 data cache
- 128KB unified system L2 cache
- TrustZone technology support
- One isolated voltage domain to support DVFS

1.2.2 Memory Organization

- Internal on-chip memory
  - BootROM
  - System SRAM

- External off-chip memory
  - SPI Nor/Nand Flash
  - SDMMC(eMMC/SD Card)

1.2.3 Internal Memory

- Internal BootRom
  - Support system boot from the following device:
    - SPI Flash interface
    - SDMMC(eMMC/SD Card) interface
  - Support system code download by the following interface:
    - USB OTG interface (Device mode)
    - SPI interface(Slave mode)

- Internal SRAM
  - 48KB System SRAM

- Integrated 128MB DDR is available. RK3506G2 supports up to DDR3L-1500.

1.2.4 External Memory or Storage device

- Serial Flash Interface
  - Support transfer data from/to SPI flash device
  - Support x1,x2,x4 data bits mode
  - Support up to 1 chip select

- SD/MMC Interface

- Compatible with standard iNAND interface
- Compatible with eMMC specification 4.51
- Compatible with SD3.0, MMC ver4.51
- Compatible with SDIO3.0 protocol
- Data bus width is 4bits

1.2.5 System Component

- Cortex-M0
  - The ARMv6-M Thumb instruction set
  - Thumb-2 technology
  - Nested Vectored Interrupt Controller (NVIC)
  - Serial wire debug port (SW-DP) debug access

- CRU (clock & reset unit)
  - One oscillator with external 24MHz crystal input
  - One internal low frequency RC clock
  - One internal power on reset circuit
  - Support single-end 32.768KHz clock input/output from/to GPIO
  - Support PLL control and generate various clock frequency for chip
  - Support clock gating control for individual components
  - Support global soft-reset control for whole chip, also individual soft-reset for each component

- PMU(power management unit)
  - Three separate voltage domains(CPU_DVDD/LOGIC_DVDD/PMU_DVDD)
  - Multiple configurable work sleep modes to save power consumption by different frequency or automatic clock gating control or external power on/off control

- Timer
  - Twelve 64-bit timers with interrupt-based operation
  - One 64-bit timer with interrupt-based operation for low power mode application
  - Support two operation modes: free-running and user-defined count
  - Support timer work state checkable

- PWM0
  - 4-channel PWM with interrupt-based operation
  - Support capture mode
  - Provides reference mode and output various duty-cycle waveform
  - Support continuous mode or one-shot mode
  - Support one channel IR RX application
  - Support four channel waveform generation through lookup table

- PWM1
  - 8-channels PWM with interrupt-based operation
  - Support capture mode
  - Provides reference mode and output various duty-cycle waveform
  - Support continuous mode or one-shot mode
  - Support one channel IR TX application
  - Support one clock frequency calculation engine and one clock free running counter
  - Support six channel biphasic counter

- Watchdog
  - Support two 32-bit watchdog counter
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - Generate a system reset

        - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
    - Programmable reset pulse length
    - Totally 16 defined ranges of main timeout period

- Mailbox
    - One Mailbox to service Cortex-A7 and Cortex-M0 communication
    - Support four mailbox elements, each element includes one data word, one command word register and one flag bit that can represent one interrupt

- Spinlock
    - Support spinlock registers for software to realize resource management

- DMA
    - Support two embedded DMA controllers
    - Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory
    - Support TrustZone technology and programmable secure state for each DMA channel
    - DMAC0 support 6 channels in total
    - DMAC1 support 8 channels in total

- Secure System
    - Cipher engine
        - Support SHA-1, SHA-256/224, MD5 with hardware padding
        - Support HMAC of SHA-1, SHA-256, MD5 with hardware padding
        - Support AES-128, AES-192, AES-256 encrypt & decrypt cipher
        - Support AES ECB/CBC/OFB/CFB/CTR/CTS/XTS/CCM/GCM/CBC-MAC/CMAC mode
        - Support up to 4096 bits PKA mathematical operations for RSA
    - Support two 256 bits RNG output
    - Support secure boot
    - Support secure debug
    - Support secure OTP
    - Support secure OS
    - Support bus firewall

1.2.6 Graphics Engine

- 2D Graphics Engine
    - SRC0 Input data format:
        - ARGB8888/RGBA8888/RGBA4444/RGBA5551
        - RGB888P/RGB565
        - YUV422-P/YUV422-SP-8bit/10bit(clip to 8bit after input)
        - YUV420-P/YUV420-SP-8bit/10bit(clip to 8bit after input)
        - YVYU422-8bit
        - YUV400-8bit
        - BPP1/2/4/8
    - SRC1 Input data format:
        - ARGB8888/RGBA8888/RGBA4444/RGBA5551/A8
        - RGB888P/RGB565
    - Output data format(all YUV format is 8bit):
        - ARGB8888/RGBA8888/ARGB4444/RGBA4444/ARGB5551/RGBA5551
        - RGB888/RGB565
        - YUV420/YUV422 P/SP
        - YUV400
    - Pixel Format conversion, BT.601/BT.709
    - Dither operation

- Max resolution: 1280x1280 source, 1280x1280 destination
- Scaling
  - Down-scaling: Average filter
  - Up-scaling: Bi-cubic filter(Horizontal, Vertical), Bi-linear filter(Vertical)
  - Arbitrary non-integer scaling ratio, from 1/16 to 16
- Rotation
  - 0, 90, 180, 270 degree rotation
  - x-mirror, y-mirror operation
  - Mirroring and rotation co-operation
- BitBLT
  - Block transfer
  - Color palette/Color fill, support with alpha
  - Transparency mode (color keying/stencil test, specified value/value range)
  - Two source BitBLT
  - A+B=B only BitBLT, A support rotate & scale when B fixed
  - A+B=C second source (B) has same attribute with (C) plus rotation function
- Alpha Blending
  - Comprehensive per-pixel alpha(color/alpha channel separately)
  - Fading
  - Support SRC1(R2Y)+SRC0(YUV) -> DST(YUV)
  - Support DST Full CSC convert for YUV2YUV
- Others
  - Supports Gaussian filters with a window size of 3 * 3

1.2.7 Video Output Processor

- Display Interface
  - Support parallel MCU/RGB LCD interface: 24-bit(RGB888), 18-bit(RGB666), 16-bit(RGB565)
  - Support serial MCU/RGB LCD interface: 3x8-bit(RGB888), 3x6-bit(RGB666), 2x8-bit(RGB565)
  - Support BT.656/BT.1120 interface
  - Support 2lane MIPI interface, 1.5Gbps/lane
  - Max output resolution is 1280x1280@60fps
- Display process
  - Background layer
    - programmable 24-bit color
  - Win1 layer
    - RGB888, ARGB888, RGB565
    - Support virtual display
    - 256 level alpha blending (pre-multiplied alpha support)
    - Transparency color key
    - RGB2YUV(BT601/BT709)
- Others
  - Support RGB or YUV domain overlay
  - BCSH (Brightness, Contrast, Saturation, Hue adjustment)
  - BCSH: RGB2YUV(BT601/BT709)
  - Support dither down allegro RGB888to666 RGB888to565 and dither down FRC(Frame Rate Control) (configurable) RGB888to666
  - Blank and black display
  - Standby mode

1.2.8 Audio Interface

- SAI
  - Support five SAI components
  - Support audio protocol: I2S, PCM, TDM
  - Support up to 128 slots available with configurable size
  - Support slot length 8 to 32 bits configurable

- Support master and slave mode, software configurable
- Support serial bit clock up to 50MHz
- Support slot valid data length 8 to 32 bits configurable
- SAI0 support up to one lane transmitter and four lane parallel receivers
- SAI1 support up to four lane parallel transmitters and one lane receiver
- SAI2 support up to one lane transmitter and one lane receiver
- SAI0/1/2 connected to chip GPIO
- SAI3 support up to one lane transmitter and one lane receiver
- SAI4 support up to one lane receiver
- SAI3 connected to internal Audio DSM modulator and chip GPIO optional, and SAI4 connected to internal Audio ADC

- PDM
  - Support PDM master receive mode
  - Support 5 wire PDM interface with one is clock and 4 data line
  - Support up to 8 mono microphones
  - Support 16~24 bits sample resolution

- SPDIF
  - Support SPDIF TX x 1
  - Support SPDIF RX x 1
  - Support 16bits/20bits/24bits resolution
  - Support linear PCM mode (IEC-60958)
  - Support non-linear PCM transfer (IEC-61937)

- ASRC
  - Support two ASRC components
  - Support fixed length conversion mode and real time conversion mode
  - Support asynchronous sample rate clock for real time conversion mode
  - Support 4 channel sample rate converter for each ASRC
  - Support combine two ASRC component to meet 8 channel sample rate converter

- Audio DSM
  - Support 2-channel digital DAC
  - Support I2S/PCM master and slave mode
  - Support 16 bit sample resolution
  - Support volume control

- Audio ADC
  - One channel 24 bit ADC microphone input
  - Support one differential microphone input
  - Support I2S as the digital signal interface
  - Support both master and slave mode
  - Support 16bits/24bits resolution
  - Support I2S normal, left and right justified mode

1.2.9 Connectivity

- RMII 10/100 Ethernet Controller
  - Support two Ethernet Controllers
  - Supports 10/100-Mbps data transfer rates with the RMII interfaces
  - Supports both full-duplex and half-duplex operation
  - Support IEEE 1588-2002 (version 1) and IEEE 1588-2008 (version 2) Timestamp
  - Support Flexible Pulse-Per-Second (PPS) Output

- USB 2.0 OTG
  - Support two USB 2.0 OTG ports
  - Compatible with USB 2.0 specification

- Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode

- DSMC master interface
  - Support master role
  - Support transfer data from/to Xccela pSRAM device
  - Support transfer data from/to Hyperbus pSRAM device
  - Support act as local bus to transfer data from/to another device with DSMC slave interface
  - Support x8,x16 data bits mode
  - Support DDR mode

- DSMC slave interface
  - Support slave role
  - Support act as local bus to transfer data from/to another device with DSMC master interface
  - Support x8 data bits mode
  - Support DDR mode

- FLEXBUS interface
  - Support transfer data from internal memory to GPIO by DMA
  - Support transfer data from GPIO to internal memory by DMA
  - Support multiple operating modes
    - Multiplexing TX clock and RX clock, Multiplexing TX data and RX data
      - Support TX only mode, RX only mode, TX then RX mode
    - Multiplexing TX clock and RX clock, Separating TX data and RX data
      - Support TX only mode, RX only mode, TX and RX mode, TX then RX mode
    - Separating TX clock and RX clock, Separating TX data and RX data
      - Support TX only mode, RX only mode, TX and RX mode
  - Support clock free running mode and following data mode
  - Support TX data width 1, 2, 4, 8, 16 bit configurable
  - Support RX data width 1, 2, 4, 8, 16 bit configurable
  - Support continue transmission mode and fix length transmission mode
  - Support one chip selection function for multiplexing TX clock and RX clock mode
  - Support two chip selection function for separating TX clock and RX clock mode, one for TX direction, the other for RX direction
  - Support TX clock auto gating
  - Support DVP (RGB888, RGB565, YUV422) interface for camera sensor

- SPI interface
  - Support three SPI Controllers
  - SPI0/SPI1 support serial-master and serial-slave mode, software-configurable
  - Support 2 chip-selects output in serial-master mode
  - SPI2 support serial-slave mode

- I2C interface
  - Support three I2C interface
  - Support 7bits and 10bits address mode
  - Software programmable clock frequency
  - Data on the I2C-bus can be transferred at rates of up to 100 Kbit/s in the Standard-mode, up to 400 Kbit/s in the Fast-mode or up to 1 Mbit/s in Fast-mode Plus

- UART Controller
  - Support six UART interface
  - Embedded two 64-byte FIFO for TX and RX operation respectively
  - Support 5bit, 6bit, 7bit, 8bit serial data transmit or receive
  - Standard asynchronous communication bits such as start, stop and parity

- Support different input clock for UART operation to get up to 4Mbps baud rate
- Support auto flow control mode

- CAN Controller
  - Support two CAN interface
  - Compatible with ISO 11898-1-2003 specification
  - Support transmit or receive standard frame
  - Support transmit or receive extended frame

- Touch Key Controller
  - Support muti-channel CapSense monitor
  - Support trigger interrupt waterline configurable
  - Support LPF and DC elimination

1.2.10 Others

- Multiple groups of GPIO
  - All of GPIOs can be used to generate interrupt
  - Support level trigger and edge trigger interrupt
  - Support configurable polarity of level trigger interrupt
  - Support configurable rising edge, falling edge and both edge trigger interrupt
  - Support configurable pull direction (pullup or pulldown)
  - Support configurable drive strength
  - Support configurable slew rate

- Temperature Sensor (TS-ADC)
  - Up to 50KS/s sampling rate
  - Support one temperature sensor
  - -40~125℃ temperature range and +/-5℃ temperature accuracy

- Successive Approximation ADC (SARADC)
  - 10-bit resolution
  - Up to 1MS/s sampling rate
  - 4 single-ended input channels
  - GPIO multiplexed

- OTP
  - Support 8K bits Size, 7K bit for secure application
  - Support Program/Read/Idle mode

- Package Type
  - RK3506G2: QFN128L(body: 12.3mm x 12.3mm; lead pitch: 0.35mm)
    - Embedded with 128MB DDR3L (1500)

1.3 Block Diagram

The following figure shows the basic block diagram.

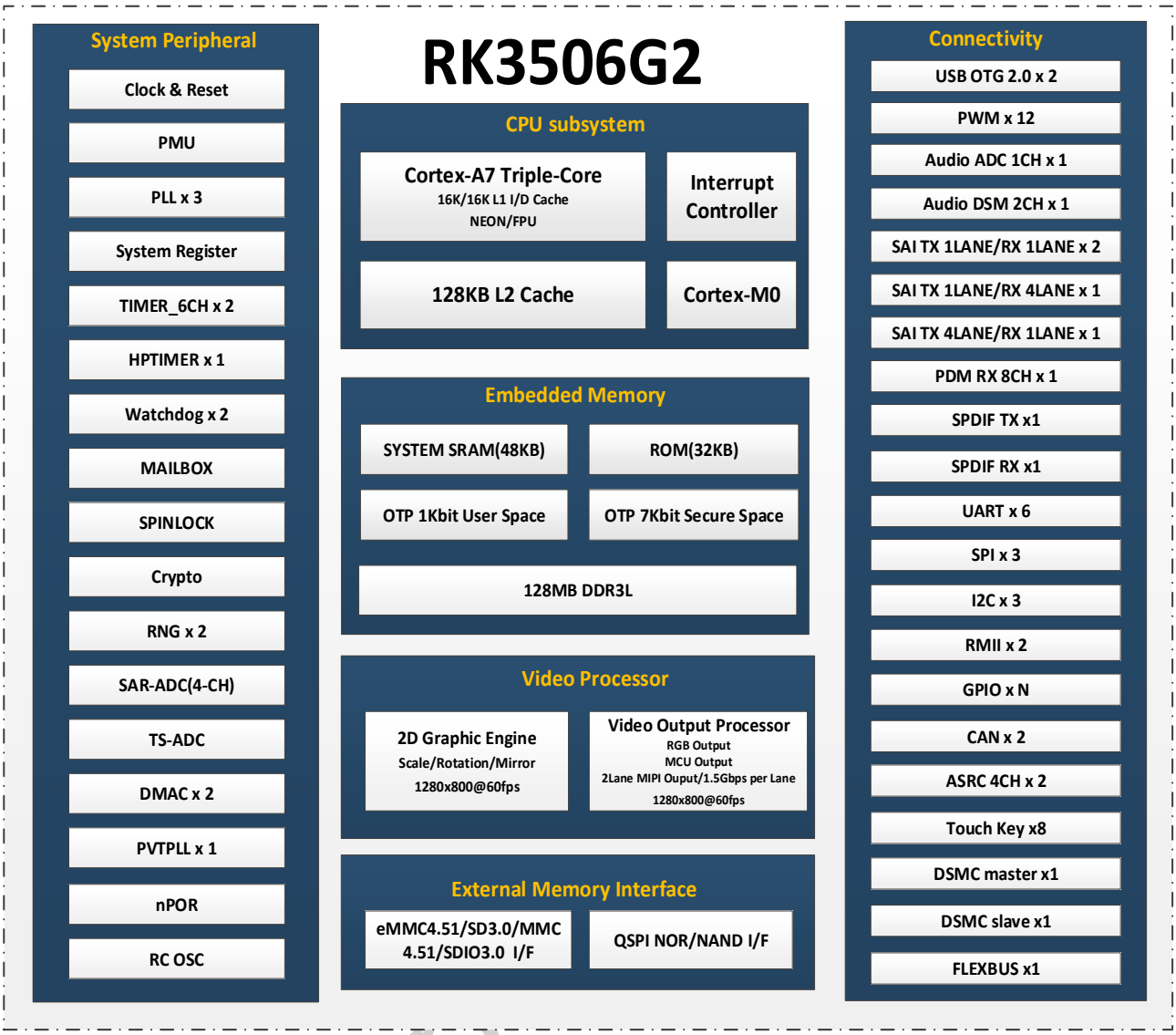

Fig.1-1 RK3506G2 Block Diagram

Chapter 2 Package Information

2.1 Order Information

Orderable Device	RoHS status	Package	Package Qty	Device Feature
RK3506G2	RoHS	QFN128L	1520 pcs	Audio Application Processor

2.2 Top Marking

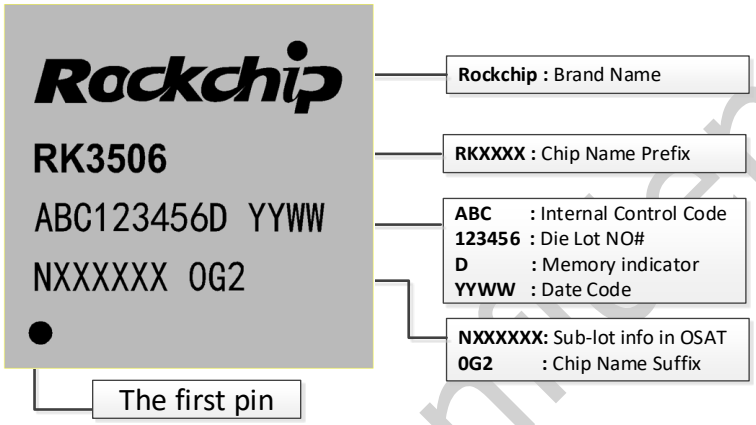

Fig.2-1 RK3506G2 Package Definition

2.3 Package Dimension

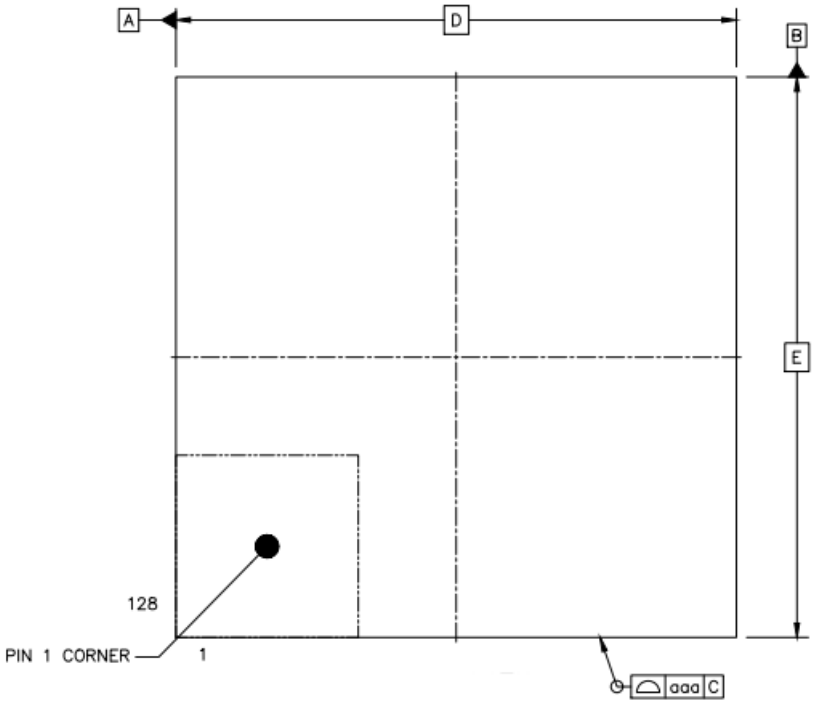

Fig.2-2 Package Top View

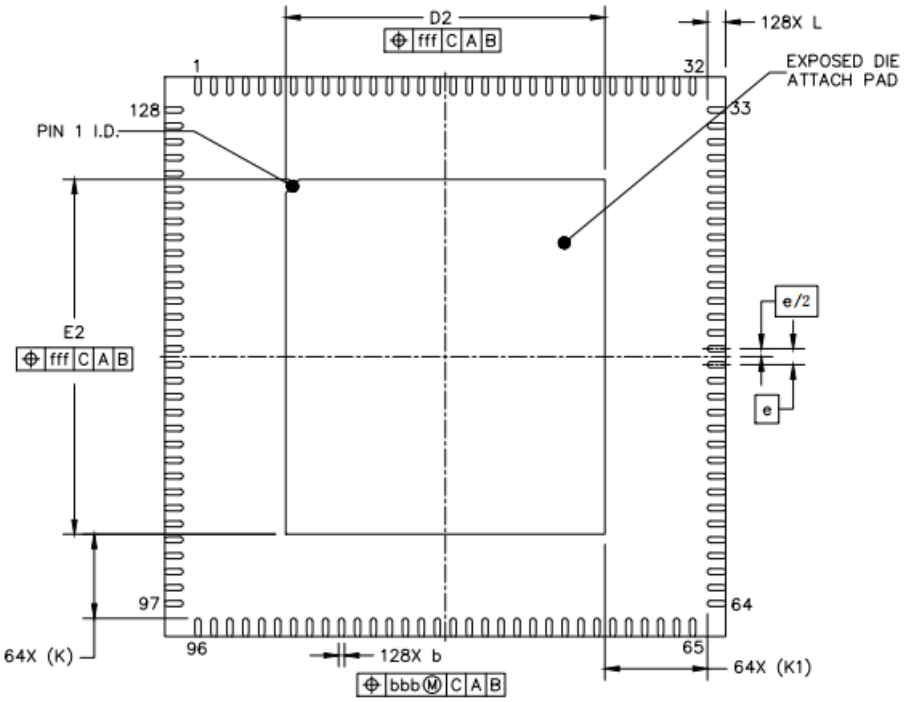

Fig.2-3 Package Bottom View

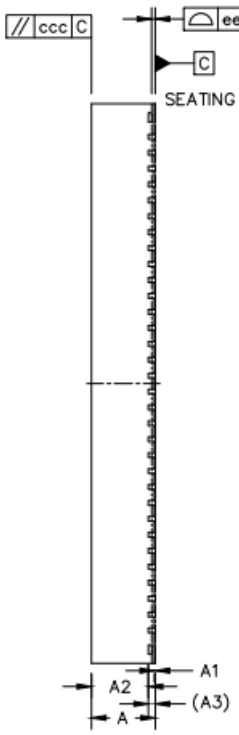

Fig.2-4 Package Side View

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	1.35	1.4	1.45
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	1.25	---
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b	0.08	0.13	0.18
BODY SIZE	X	D		12.3 BSC	
	Y	E		12.3 BSC	
LEAD PITCH		e		0.35 BSC	
EP SIZE	X	D2	6.9	7	7.1
	Y	E2	7.7	7.8	7.9
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		1.85 REF	
		K1		2.25 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
EXPOSED PAD OFFSET		fff		0.1	

Fig.2-5 Package Dimension

2.4 MSL Information

Moisture sensitivity Level: 3

2.5 Lead Finish/Ball material Information

Lead Finish/Ball material: Sn

2.6 Pin Number List

Table 2-1 Pin Number Order Information

Pin	Pin Name	Abbreviated Pin Name
1	SPI0_MOSI/RM_IO17/GPIO0_C1_d	GPIO0_C1
2	SPI0_CLK/RM_IO16/GPIO0_C0_d	GPIO0_C0
3	SAI1_SDO3/SPI0_CSN1/RM_IO15/GPIO0_B7_d	GPIO0_B7
4	SAI1_SDO2/SPI1_CSN0/RM_IO14/GPIO0_B6_d	GPIO0_B6
5	SAI1_SDO1/RM_IO13/GPIO0_B5_d	GPIO0_B5
6	SAI1_SDO0/RM_IO12/GPIO0_B4_d	GPIO0_B4
7	SAI1_SDI/RM_IO11/GPIO0_B3_d	GPIO0_B3
8	SAI1_LRCK/SPI1_MISO/RM_IO10/GPIO0_B2_d	GPIO0_B2
9	PMUIO_VCC3V3	PMUIO_VCC3V3
10	NPOR	NPOR
11	PMU_LOGIC_DVDD0V9	PMU_LOGIC_DVDD0V9
12	SAI1_SCLK/SPI1_MOSI/RM_IO9/GPIO0_B1_d	GPIO0_B1
13	SAI1_MCLK/SPI1_CLK/RM_IO8/GPIO0_B0_d	GPIO0_B0
14	SAI0_SDI3/SPI1_CSN1/RM_IO7/GPIO0_A7_d	GPIO0_A7
15	SAI0_SDI2/RM_IO6/GPIO0_A6_d	GPIO0_A6
16	SAI0_SDI1/RM_IO5/GPIO0_A5_d	GPIO0_A5
17	SAI0_SDI0/RM_IO4/GPIO0_A4_d	GPIO0_A4
18	SAI0_SDO/RM_IO3/GPIO0_A3_d	GPIO0_A3
19	SAI0_MCLK/RM_IO2/GPIO0_A2_u	GPIO0_A2
20	SAI0_SCLK/RM_IO1/GPIO0_A1_d	GPIO0_A1

Pin	Pin Name	Abbreviated Pin Name
21	SAI0_LRCK/RM_IO0/GPIO0_A0_u	GPIO0_A0
22	DDR_VDDQ	DDR_VDDQ
23	DDR_VDDQ	DDR_VDDQ
24	VSS	VSS
25	DDR_VDDQ	DDR_VDDQ
26	SAI2_MCLK_M0/ETH_RMII1_RXDVCRS/GPIO3_B6_d	GPIO3_B6
27	UART5_RTSN_M0/ETH_RMII1_MDIO/GPIO3_B5_d	GPIO3_B5
28	UART5_TX_M0/ETH_RMII1_MDC/GPIO3_B4_d	GPIO3_B4
29	UART5_RX_M0/ETH_RMII1_TXEN/GPIO3_B3_d	GPIO3_B3
30	UART5_CTSN_M0/ETH_RMII1_TXD1/GPIO3_B2_d	GPIO3_B2
31	SAI2_LRCK_M0/ETH_RMII1_TXD0/GPIO3_B1_d	GPIO3_B1
32	SAI2_SDO_M0/ETH_RMII1_CLK/GPIO3_B0_d	GPIO3_B0
33	SAI2_SCLK_M0/ETH_RMII1_RXD1/GPIO3_A7_d	GPIO3_A7
34	SAI2_SDI_M0/ETH_RMII1_RXD0/GPIO3_A6_d	GPIO3_A6
35	SDMMC_D1/TEST_CLK_OUT/GPIO3_A3_d	GPIO3_A3
36	SDMMC_D0/GPIO3_A2_d	GPIO3_A2
37	SDMMC_CLK/GPIO3_A0_d	GPIO3_A0
38	SDMMC_CMD/GPIO3_A1_d	GPIO3_A1
39	VCCIO4_VCC	VCCIO4_VCC
40	SDMMC_D3/JTAG_TMS_M0/GPIO3_A5_d	GPIO3_A5
41	SDMMC_D2/JTAG_TCK_M0/GPIO3_A4_d	GPIO3_A4
42	ETH_RMII0_RXDVCRS/SAI3_MCLK/GPIO2_C0_d	GPIO2_C0
43	ETH_RMII0_MDIO/DSM_AUD_LP_M1/SAI3_SDO/GPIO2_B7_d	GPIO2_B7
44	ETH_RMII0_MDC/DSM_AUD_LN_M1/SAI3_SDI/GPIO2_B6_d	GPIO2_B6
45	ETH_RMII0_TXEN/DSM_AUD_RP_M1/SAI3_LRCK/GPIO2_B5_d	GPIO2_B5
46	ETH_RMII0_TXD1/DSM_AUD_RN_M1/SAI3_SCLK/GPIO2_B4_d	GPIO2_B4
47	ETH_RMII0_TXD0/SPI2_MISO/GPIO2_B3_d	GPIO2_B3
48	ETH_RMII0_CLK/SPI2_MOSI/GPIO2_B2_d	GPIO2_B2
49	ETH_RMII0_RXD1/SPI2_CSN/GPIO2_B1_d	GPIO2_B1
50	ETH_RMII0_RXD0/SPI2_CLK/GPIO2_B0_d	GPIO2_B0
51	LOGIC_DVDD	LOGIC_DVDD
52	VCCIO3_VCC	VCCIO3_VCC
53	FSPI_D3/GPIO2_A5_u	GPIO2_A5
54	FSPI_CLK/GPIO2_A1_d	GPIO2_A1
55	FSPI_D0/GPIO2_A2_u	GPIO2_A2
56	VCCIO2_VCC	VCCIO2_VCC
57	FSPI_D2/GPIO2_A4_u	GPIO2_A4
58	FSPI_D1/GPIO2_A3_u	GPIO2_A3
59	FSPI_CSN/GPIO2_A0_u	GPIO2_A0
60	SARADC_IN3/GPIO4_B3_z	SARADC_IN3/GPIO4_B3_z
61	SARADC_IN2/GPIO4_B2_z	SARADC_IN2/GPIO4_B2_z
62	SARADC_IN1/GPIO4_B1_z	SARADC_IN1/GPIO4_B1_z
63	SARADC_IN0/GPIO4_B0_z	SARADC_IN0/GPIO4_B0_z
64	AVCC_1V8	AVCC_1V8
65	ACODEC_ADC_AVDD1V6	ACODEC_ADC_AVDD1V6
66	ACODEC_ADC_VCM	ACODEC_ADC_VCM
67	ACODEC_ADC_INN	ACODEC_ADC_INN
68	ACODEC_ADC_INP	ACODEC_ADC_INP
69	ACODEC_ADC_AVSS	ACODEC_ADC_AVSS

Pin	Pin Name	Abbreviated Pin Name
70	USB20_OTG_AVDD3V3	USB20_OTG_AVDD3V3
71	USB20_OTG0_DM	USB20_OTG0_DM
72	USB20_OTG0_DP	USB20_OTG0_DP
73	USB20_OTG1_DM	USB20_OTG1_DM
74	USB20_OTG1_DP	USB20_OTG1_DP
75	AVDD_0V9	AVDD_0V9
76	AVDD_1V8	AVDD_1V8
77	MIPI_DPHY_DSI_TX_CLKN/GPO4_A4_z	MIPI_DPHY_DSI_TX_CLKN/GPO4_A4_z
78	MIPI_DPHY_DSI_TX_CLKP/GPO4_A5_z	MIPI_DPHY_DSI_TX_CLKP/GPO4_A5_z
79	MIPI_DPHY_DSI_TX_D1N/GPO4_A2_z	MIPI_DPHY_DSI_TX_D1N/GPO4_A2_z
80	MIPI_DPHY_DSI_TX_D1P/GPO4_A3_z	MIPI_DPHY_DSI_TX_D1P/GPO4_A3_z
81	MIPI_DPHY_DSI_TX_D0N/GPO4_A0_z	MIPI_DPHY_DSI_TX_D0N/GPO4_A0_z
82	MIPI_DPHY_DSI_TX_D0P/GPO4_A1_z	MIPI_DPHY_DSI_TX_D0P/GPO4_A1_z
83	VO_LCDC_DEN/DSMC_CLKP/FLEXBUS1_D0/GPIO1_A0_d	GPIO1_A0
84	VO_LCDC_VSYNC/DSMC_CLKN/FLEXBUS1_D1/DSMC_INT0/DSMC_SLV_INT/GPIO1_A1_d	GPIO1_A1
85	CPU_DVDD	CPU_DVDD
86	VSS	VSS
87	LOGIC_DVDD	LOGIC_DVDD
88	VO_LCDC_HSYNC/DSMC_DQS0/FLEXBUS1_D2/GPIO1_A2_d	GPIO1_A2
89	VO_LCDC_CLK/DSMC_D0/FLEXBUS1_D3/GPIO1_A3_d	GPIO1_A3
90	VO_LCDC_D23/DSMC_D1/FLEXBUS1_D4/GPIO1_A4_d	GPIO1_A4
91	VO_LCDC_D22/DSMC_D2/FLEXBUS1_D5/GPIO1_A5_d	GPIO1_A5
92	VCCIO1_VCC	VCCIO1_VCC
93	VO_LCDC_D21/DSMC_D3/FLEXBUS1_D6/GPIO1_A6_d	GPIO1_A6
94	VO_LCDC_D20/DSMC_D4/FLEXBUS1_D7/GPIO1_A7_d	GPIO1_A7
95	VO_LCDC_D19/DSMC_D5/FLEXBUS1_D8/FLEXBUS0_CSN_M0/GPIO1_B0_d	GPIO1_B0
96	VO_LCDC_D18/DSMC_CSN1/FLEXBUS1_D9/FLEXBUS1_CSN_M0/UART5_CTSN_M1/RM_IO24/GPIO1_B1_d	GPIO1_B1
97	VO_LCDC_D17/DSMC_INT2/FLEXBUS1_D10/FLEXBUS0_D15/FLEXBUS0_CSN_M1/SAI2_SCLK_M1/RM_IO25/GPIO1_B2_d	GPIO1_B2
98	VO_LCDC_D16/DSMC_INT3/FLEXBUS1_D11/FLEXBUS0_D14/FLEXBUS1_CSN_M1/SAI2_LRCK_M1/RM_IO26/GPIO1_B3_d	GPIO1_B3
99	VO_LCDC_D15/DSMC_D6/FLEXBUS1_D12/FLEXBUS0_D13/FLEXBUS0_CSN_M2/GPIO1_B4_d	GPIO1_B4
100	VO_LCDC_D14/DSMC_D7/FLEXBUS1_D13/FLEXBUS0_D12/FLEXBUS1_CSN_M2/GPIO1_B5_d	GPIO1_B5
101	VO_LCDC_D13/DSMC_CSN0/FLEXBUS1_D14/FLEXBUS0_D11/FLEXBUS0_CSN_M3/GPIO1_B6_d	GPIO1_B6
102	VO_LCDC_D12/DSMC_RDYN/FLEXBUS1_D15/FLEXBUS0_D10/FLEXBUS1_CSN_M3/GPIO1_B7_d	GPIO1_B7
103	VCCIO1_VCC	VCCIO1_VCC
104	VO_LCDC_D11/DSMC_RESETN/FLEXBUS1_CLK/DSMC_INT1/FLEXBUS0_CSN_M4/DSMC_SLV_CLK/GPIO1_C0_d	GPIO1_C0
105	VO_LCDC_D10/DSMC_D8/FLEXBUS0_CLK/DSM_AUD_RN_M0/FLEXBUS1_CSN_M4/SAI2_MCLK_M1/DSMC_SLV_DQS0/GPIO1_C1_d	GPIO1_C1
106	VO_LCDC_D9/DSMC_D9/FLEXBUS0_D9/DSM_AUD_RP_M0/FLEXBUS0_CSN_M5/SAI2_SDI_M1/RM_IO27/DSMC_SLV_D0/GPIO1_C2_d	GPIO1_C2
107	VO_LCDC_D8/DSMC_D10/FLEXBUS0_D8/FLEXBUS1_CSN_M5/SAI2_SDO_M1/RM_IO28/DSMC_SLV_D1/GPIO1_C3_d	GPIO1_C3
108	VO_LCDC_D7/DSMC_D11/FLEXBUS0_D7/DSMC_SLV_D2/GPIO1_C4_d	GPIO1_C4
109	VO_LCDC_D6/DSMC_D12/FLEXBUS0_D6/DSMC_SLV_D3/GPIO1_C5_d	GPIO1_C5
110	LOGIC_DVDD	LOGIC_DVDD
111	VSS	VSS
112	CPU_DVDD	CPU_DVDD
113	VO_LCDC_D5/DSMC_D13/FLEXBUS0_D5/DSMC_SLV_D4/GPIO1_C6_d	GPIO1_C6
114	VO_LCDC_D4/DSMC_D14/FLEXBUS0_D4/DSMC_SLV_D5/GPIO1_C7_d	GPIO1_C7

Pin	Pin Name	Abbreviated Pin Name
115	VO_LCDC_D3/DSMC_D15/FLEXBUS0_D3/DSM_AUD_LN_M0/DSMC_SLV_D6/GPIO1_D0_d	GPIO1_D0
116	VO_LCDC_D2/DSMC_DQS1/FLEXBUS0_D2/DSM_AUD_LP_M0/UART5_RTSN_M1/RM_IO29/DSMC_SLV_D7/GPIO1_D1_d	GPIO1_D1
117	VO_LCDC_D1/DSMC_CSN2/FLEXBUS0_D1/UART5_TX_M1/RM_IO30/DSMC_SLV_CSN0/GPIO1_D2_d	GPIO1_D2
118	VO_LCDC_D0/DSMC_CSN3/FLEXBUS0_D0/UART5_RX_M1/RM_IO31/DSMC_SLV_RDYN/GPIO1_D3_d	GPIO1_D3
119	OSC_CLK_OUT/REF_CLK0_OUT/GPIO0_D0_d	GPIO0_D0
120	SYS_PLL_AVDD1V8	SYS_PLL_AVDD1V8
121	OSC_XIN	OSC_XIN
122	OSC_XOUT	OSC_XOUT
123	UART0_RX/JTAG_TMS_M1/RM_IO23/GPIO0_C7_u	GPIO0_C7
124	UART0_TX/JTAG_TCK_M1/RM_IO22/GPIO0_C6_u	GPIO0_C6
125	CPU_AVS/RM_IO21/GPIO0_C5_z	GPIO0_C5
126	ETH_CLK0_25M_OUT/AUPLL_CLK_IN/RM_IO20/GPIO0_C4_d	GPIO0_C4
127	ETH_CLK1_25M_OUT/SPI0_CSN0/RM_IO19/GPIO0_C3_d	GPIO0_C3
128	REF_CLK1_OUT/SPI0_MISO/RM_IO18/GPIO0_C2_d	GPIO0_C2
EPAD	VSS	VSS

2.7 Power/Ground IO Description

Table 2-2 Power/Ground IO information

Group	Pin#	Descriptions
VSS	24, 86, 111, EPAD	Digital Ground
ACODEC_ADC_AVSS	69	ACODEC ADC Analog Ground
CPU_DVDD	85, 112	Logic Power
LOGIC_DVDD	51, 87, 110	DSP0 Power
PMU_LOGIC_DVDD0V9	11	PMU Power
PMUIO_VCC3V3	9	PMU IO Power
VCCIO1_VCC	92, 103	VCCIO1 IO Power
VCCIO2_VCC	56	VCCIO2 IO Power
VCCIO3_VCC	52	VCCIO3 IO Power
VCCIO4_VCC	39	VCCIO4 IO Power
SYS_PLL_AVDD1V8	120	PLL Power
USB20_OTG_AVDD3V3	70	USB OTG2.0 Power
AVDD_0V9	75	USB OTG2.0/MIPI DPHY Analog Power
AVDD_1V8	76	USB OTG2.0/MIPI DPHY/TSADC Analog Power

Group	Pin#	Descriptions
AVCC_1V8	64	ACODEC ADC/SARADC/OTP Analog Power
DDR_VDDQ	22, 23, 25	DDR Power

2.8 Function IO Description

Table 2-3 Function IO description

Pin	Pin Name	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Pad Type①	Def③	Pull	Drive Strength②	INT	Power Domain
121	OSC_XIN	OSC_XIN									I	I	N/A	N/A		PLL
122	OSC_XOUT	OSC_XOUT									O	O	N/A	N/A		
119	OSC_CLK_OUT/REF_CLK0_OUT/GPIO0_D0_d	GPIO0_D0	OSC_CLK_OUT	REF_CLK0_OUT							IO	I	down	Level1	√	
10	NPOR	NPOR									I	I	N/A	N/A		PMUIO_VCC3V3
21	SAI0_LRCK/RM_IO0/GPIO0_A0_u	GPIO0_A0	SAI0_LRCK						RM_IO0		IO	I	up	Level2	√	
20	SAI0_SCLK/RM_IO1/GPIO0_A1_d	GPIO0_A1	SAI0_SCLK						RM_IO1		IO	I	down	Level2	√	
19	SAI0_MCLK/RM_IO2/GPIO0_A2_u	GPIO0_A2	SAI0_MCLK						RM_IO2		IO	I	up	Level2	√	
18	SAI0_SDO/RM_IO3/GPIO0_A3_d	GPIO0_A3	SAI0_SDO						RM_IO3		IO	I	down	Level2	√	
17	SAI0_SDI0/RM_IO4/GPIO0_A4_d	GPIO0_A4	SAI0_SDI0						RM_IO4		IO	I	down	Level2	√	
16	SAI0_SDI1/RM_IO5/GPIO0_A5_d	GPIO0_A5	SAI0_SDI1						RM_IO5		IO	I	down	Level2	√	
15	SAI0_SDI2/RM_IO6/GPIO0_A6_d	GPIO0_A6	SAI0_SDI2						RM_IO6		IO	I	down	Level2	√	
14	SAI0_SDI3/SPI1_CSN1/RM_IO7/GPIO0_A7_d	GPIO0_A7	SAI0_SDI3	SPI1_CSN1					RM_IO7		IO	I	down	Level2	√	
13	SAI1_MCLK/SPI1_CLK/RM_IO8/GPIO0_B0_d	GPIO0_B0	SAI1_MCLK	SPI1_CLK					RM_IO8		IO	I	down	Level2	√	
12	SAI1_SCLK/SPI1_MOSI/RM_IO9/GPIO0_B1_d	GPIO0_B1	SAI1_SCLK	SPI1_MOSI					RM_IO9		IO	I	down	Level2	√	
8	SAI1_LRCK/SPI1_MISO/RM_IO10/GPIO0_B2_d	GPIO0_B2	SAI1_LRCK	SPI1_MISO					RM_IO10		IO	I	down	Level2	√	
7	SAI1_SDI/RM_IO11/GPIO0_B3_d	GPIO0_B3	SAI1_SDI						RM_IO11		IO	I	down	Level2	√	
6	SAI1_SDO0/RM_IO12/GPIO0_B4_d	GPIO0_B4	SAI1_SDO0						RM_IO12		IO	I	down	Level2	√	
5	SAI1_SDO1/RM_IO13/GPIO0_B5_d	GPIO0_B5	SAI1_SDO1						RM_IO13		IO	I	down	Level2	√	
4	SAI1_SDO2/SPI1_CSN0/RM_IO14/GPIO0_B6_d	GPIO0_B6	SAI1_SDO2	SPI1_CSN0					RM_IO14		IO	I	down	Level2	√	
3	SAI1_SDO3/SPI0_CSN1/RM_IO15/GPIO0_B7_d	GPIO0_B7	SAI1_SDO3	SPI0_CSN1					RM_IO15		IO	I	down	Level2	√	
2	SPI0_CLK/RM_IO16/GPIO0_C0_d	GPIO0_C0		SPI0_CLK					RM_IO16		IO	I	down	Level2	√	
1	SPI0_MOSI/RM_IO17/GPIO0_C1_d	GPIO0_C1		SPI0_MOSI					RM_IO17		IO	I	down	Level2	√	
128	REF_CLK1_OUT/SPI0_MISO/RM_IO18/GPIO0_C2_d	GPIO0_C2	REF_CLK1_OUT	SPI0_MISO					RM_IO18		IO	I	down	Level2	√	
127	ETH_CLK1_25M_OUT/SPI0_CSN0/RM_IO19/GPIO0_C3_d	GPIO0_C3	ETH_CLK1_25M_OUT	SPI0_CSN0					RM_IO19		IO	I	down	Level2	√	
126	ETH_CLK0_25M_OUT/AUPLL_CLK_IN/RM_IO20/GPIO0_C4_d	GPIO0_C4	ETH_CLK0_25M_OUT	AUPLL_CLK_IN					RM_IO20		IO	I	down	Level2	√	
125	CPU_AVS/RM_IO21/GPIO0_C5_z	GPIO0_C5	CPU_AVS						RM_IO21		IO	I	z	Level2	√	
124	UART0_TX/JTAG_TCK_M1/RM_IO22/GPIO0_C6_u	GPIO0_C6	UART0_TX	JTAG_TCK_M1					RM_IO22		IO	I	up	Level2	√	
123	UART0_RX/JTAG_TMS_M1/RM_IO23/GPIO0_C7_u	GPIO0_C7	UART0_RX	JTAG_TMS_M1					RM_IO23		IO	I	up	Level2	√	
83	VO_LCDC_DEN/DSMC_CLKP/FLEXBUS1_D0/GPIO1_A0_d	GPIO1_A0	VO_LCDC_DEN	DSMC_CLKP	FLEXBUS1_D0						IO	I	down	Level2	√	VCCIO1_VCC
84	VO_LCDC_VSYNC/DSMC_CLKN/FLEXBUS1_D1/DSMC_INT0/DSMC_SLV_INT/GPIO1_A1_d	GPIO1_A1	VO_LCDC_VSYNC	DSMC_CLKN	FLEXBUS1_D1	DSMC_INT0				DSMC_SLV_INT	IO	I	down	Level2	√	
88	VO_LCDC_HSYNC/DSMC_DQS0/FLEXBUS1_D2/GPIO1_A2_d	GPIO1_A2	VO_LCDC_HSYNC	DSMC_DQS0	FLEXBUS1_D2						IO	I	down	Level2	√	
89	VO_LCDC_CLK/DSMC_D0/FLEXBUS1_D3/GPIO1_A3_d	GPIO1_A3	VO_LCDC_CLK	DSMC_D0	FLEXBUS1_D3						IO	I	down	Level2	√	
90	VO_LCDC_D23/DSMC_D1/FLEXBUS1_D4/GPIO1_A4_d	GPIO1_A4	VO_LCDC_D23	DSMC_D1	FLEXBUS1_D4						IO	I	down	Level2	√	
91	VO_LCDC_D22/DSMC_D2/FLEXBUS1_D5/GPIO1_A5_d	GPIO1_A5	VO_LCDC_D22	DSMC_D2	FLEXBUS1_D5						IO	I	down	Level2	√	
93	VO_LCDC_D21/DSMC_D3/FLEXBUS1_D6/GPIO1_A6_d	GPIO1_A6	VO_LCDC_D21	DSMC_D3	FLEXBUS1_D6						IO	I	down	Level2	√	
94	VO_LCDC_D20/DSMC_D4/FLEXBUS1_D7/GPIO1_A7_d	GPIO1_A7	VO_LCDC_D20	DSMC_D4	FLEXBUS1_D7						IO	I	down	Level2	√	
95	VO_LCDC_D19/DSMC_D5/FLEXBUS1_D8/FLEXBUS0_CSN_M0/GPIO1_B0_d	GPIO1_B0	VO_LCDC_D19	DSMC_D5	FLEXBUS1_D8		FLEXBUS0_CSN_M0				IO	I	down	Level2	√	
96	VO_LCDC_D18/DSMC_CSN1/FLEXBUS1_D9/FLEXBUS1_CSN_M0/UART5_CTSN_M1/RM_IO24/GPIO1_B1_d	GPIO1_B1	VO_LCDC_D18	DSMC_CSN1	FLEXBUS1_D9		FLEXBUS1_CSN_M0	UART5_CTSN_M1	RM_IO24		IO	I	down	Level2	√	
97	VO_LCDC_D17/DSMC_INT2/FLEXBUS1_D10/FLEXBUS0_D15/FLEXBUS0_CSN_M1/SAI2_SCLK_M1/RM_IO25/GPIO1_B2_d	GPIO1_B2	VO_LCDC_D17	DSMC_INT2	FLEXBUS1_D10	FLEXBUS0_D15	FLEXBUS0_CSN_M1	SAI2_SCLK_M1	RM_IO25		IO	I	down	Level2	√	

Pin	Pin Name	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Pad Type①	Def③	Pull	Drive Strength②	INT	Power Domain
98	VO_LCDC_D16/DSMC_INT3/FLEXBUS1_D11/FLEXBUS0_D14/FLEXBUS1_CSN_M1/SAI2_LRCK_M1/RM_IO26/GPIO1_B3_d	GPIO1_B3	VO_LCDC_D16	DSMC_INT3	FLEXBUS1_D11	FLEXBUS0_D14	FLEXBUS1_CSN_M1	SAI2_LRCK_M1	RM_IO26		IO	I	down	Level2	√	
99	VO_LCDC_D15/DSMC_D6/FLEXBUS1_D12/FLEXBUS0_D13/FLEXBUS0_CSN_M2/GPIO1_B4_d	GPIO1_B4	VO_LCDC_D15	DSMC_D6	FLEXBUS1_D12	FLEXBUS0_D13	FLEXBUS0_CSN_M2				IO	I	down	Level2	√	
100	VO_LCDC_D14/DSMC_D7/FLEXBUS1_D13/FLEXBUS0_D12/FLEXBUS1_CSN_M2/GPIO1_B5_d	GPIO1_B5	VO_LCDC_D14	DSMC_D7	FLEXBUS1_D13	FLEXBUS0_D12	FLEXBUS1_CSN_M2				IO	I	down	Level2	√	
101	VO_LCDC_D13/DSMC_CSN0/FLEXBUS1_D14/FLEXBUS0_D11/FLEXBUS0_CSN_M3/GPIO1_B6_d	GPIO1_B6	VO_LCDC_D13	DSMC_CSN0	FLEXBUS1_D14	FLEXBUS0_D11	FLEXBUS0_CSN_M3				IO	I	down	Level2	√	
102	VO_LCDC_D12/DSMC_RDYN/FLEXBUS1_D15/FLEXBUS0_D10/FLEXBUS1_CSN_M3/GPIO1_B7_d	GPIO1_B7	VO_LCDC_D12	DSMC_RDYN	FLEXBUS1_D15	FLEXBUS0_D10	FLEXBUS1_CSN_M3				IO	I	down	Level2	√	
104	VO_LCDC_D11/DSMC_RESETN/FLEXBUS1_CLK/DSMC_INT1/FLEXBUS0_CSN_M4/DSMC_SLV_CLK/GPIO1_C0_d	GPIO1_C0	VO_LCDC_D11	DSMC_RESETN	FLEXBUS1_CLK	DSMC_INT1	FLEXBUS0_CSN_M4			DSMC_SLV_CLK	IO	I	down	Level2	√	
105	VO_LCDC_D10/DSMC_D8/FLEXBUS0_CLK/DSM_AUD_RN_M0/FLEXBUS1_CSN_M4/SAI2_MCLK_M1/DSMC_SLV_DQS0/GPIO1_C1_d	GPIO1_C1	VO_LCDC_D10	DSMC_D8	FLEXBUS0_CLK	DSM_AUD_RN_M0	FLEXBUS1_CSN_M4	SAI2_MCLK_M1		DSMC_SLV_DQS0	IO	I	down	Level2	√	
106	VO_LCDC_D9/DSMC_D9/FLEXBUS0_D9/DSM_AUD_RP_M0/FLEXBUS0_CSN_M5/SAI2_SDI_M1/RM_IO27/DSMC_SLV_D0/GPIO1_C2_d	GPIO1_C2	VO_LCDC_D9	DSMC_D9	FLEXBUS0_D9	DSM_AUD_RP_M0	FLEXBUS0_CSN_M5	SAI2_SDI_M1	RM_IO27	DSMC_SLV_D0	IO	I	down	Level2	√	
107	VO_LCDC_D8/DSMC_D10/FLEXBUS0_D8/FLEXBUS1_CSN_M5/SAI2_SDO_M1/RM_IO28/DSMC_SLV_D1/GPIO1_C3_d	GPIO1_C3	VO_LCDC_D8	DSMC_D10	FLEXBUS0_D8		FLEXBUS1_CSN_M5	SAI2_SDO_M1	RM_IO28	DSMC_SLV_D1	IO	I	down	Level2	√	
108	VO_LCDC_D7/DSMC_D11/FLEXBUS0_D7/DSMC_SLV_D2/GPIO1_C4_d	GPIO1_C4	VO_LCDC_D7	DSMC_D11	FLEXBUS0_D7					DSMC_SLV_D2	IO	I	down	Level2	√	
109	VO_LCDC_D6/DSMC_D12/FLEXBUS0_D6/DSMC_SLV_D3/GPIO1_C5_d	GPIO1_C5	VO_LCDC_D6	DSMC_D12	FLEXBUS0_D6					DSMC_SLV_D3	IO	I	down	Level2	√	
113	VO_LCDC_D5/DSMC_D13/FLEXBUS0_D5/DSMC_SLV_D4/GPIO1_C6_d	GPIO1_C6	VO_LCDC_D5	DSMC_D13	FLEXBUS0_D5					DSMC_SLV_D4	IO	I	down	Level2	√	
114	VO_LCDC_D4/DSMC_D14/FLEXBUS0_D4/DSMC_SLV_D5/GPIO1_C7_d	GPIO1_C7	VO_LCDC_D4	DSMC_D14	FLEXBUS0_D4					DSMC_SLV_D5	IO	I	down	Level2	√	
115	VO_LCDC_D3/DSMC_D15/FLEXBUS0_D3/DSM_AUD_LN_M0/DSMC_SLV_D6/GPIO1_D0_d	GPIO1_D0	VO_LCDC_D3	DSMC_D15	FLEXBUS0_D3	DSM_AUD_LN_M0				DSMC_SLV_D6	IO	I	down	Level2	√	
116	VO_LCDC_D2/DSMC_DQS1/FLEXBUS0_D2/DSM_AUD_LP_M0/UART5_RTSN_M1/RM_IO29/DSMC_SLV_D7/GPIO1_D1_d	GPIO1_D1	VO_LCDC_D2	DSMC_DQS1	FLEXBUS0_D2	DSM_AUD_LP_M0		UART5_RTSN_M1	RM_IO29	DSMC_SLV_D7	IO	I	down	Level2	√	
117	VO_LCDC_D1/DSMC_CSN2/FLEXBUS0_D1/UART5_TX_M1/RM_IO30/DSMC_SLV_CSN0/GPIO1_D2_d	GPIO1_D2	VO_LCDC_D1	DSMC_CSN2	FLEXBUS0_D1			UART5_TX_M1	RM_IO30	DSMC_SLV_CSN0	IO	I	down	Level2	√	
118	VO_LCDC_D0/DSMC_CSN3/FLEXBUS0_D0/UART5_RX_M1/RM_IO31/DSMC_SLV_RDYN/GPIO1_D3_d	GPIO1_D3	VO_LCDC_D0	DSMC_CSN3	FLEXBUS0_D0			UART5_RX_M1	RM_IO31	DSMC_SLV_RDYN	IO	I	down	Level2	√	
59	FSPI_CSN/GPIO2_A0_u	GPIO2_A0	FSPI_CSN								IO	I	up	Level2	√	
54	FSPI_CLK/GPIO2_A1_d	GPIO2_A1	FSPI_CLK								IO	I	down	Level3	√	
55	FSPI_D0/GPIO2_A2_u	GPIO2_A2	FSPI_D0								IO	I	up	Level2	√	
58	FSPI_D1/GPIO2_A3_u	GPIO2_A3	FSPI_D1								IO	I	up	Level2	√	VCCIO2_VCC
57	FSPI_D2/GPIO2_A4_u	GPIO2_A4	FSPI_D2								IO	I	up	Level2	√	
53	FSPI_D3/GPIO2_A5_u	GPIO2_A5	FSPI_D3								IO	I	up	Level2	√	
50	ETH_RMII0_RXD0/SPI2_CLK/GPIO2_B0_d	GPIO2_B0	ETH_RMII0_RXD0	SPI2_CLK							IO	I	down	Level2	√	
49	ETH_RMII0_RXD1/SPI2_CSN/GPIO2_B1_d	GPIO2_B1	ETH_RMII0_RXD1	SPI2_CSN							IO	I	down	Level2	√	
48	ETH_RMII0_CLK/SPI2_MOSI/GPIO2_B2_d	GPIO2_B2	ETH_RMII0_CLK	SPI2_MOSI							IO	I	down	Level2	√	
47	ETH_RMII0_TXD0/SPI2_MISO/GPIO2_B3_d	GPIO2_B3	ETH_RMII0_TXD0	SPI2_MISO							IO	I	down	Level2	√	
46	ETH_RMII0_TXD1/DSM_AUD_RN_M1/SAI3_SCLK/GPIO2_B4_d	GPIO2_B4	ETH_RMII0_TXD1	DSM_AUD_RN_M1	SAI3_SCLK						IO	I	down	Level2	√	VCCIO3_VCC
45	ETH_RMII0_TXEN/DSM_AUD_RP_M1/SAI3_LRCK/GPIO2_B5_d	GPIO2_B5	ETH_RMII0_TXEN	DSM_AUD_RP_M1	SAI3_LRCK						IO	I	down	Level2	√	
44	ETH_RMII0_MDC/DSM_AUD_LN_M1/SAI3_SDI/GPIO2_B6_d	GPIO2_B6	ETH_RMII0_MDC	DSM_AUD_LN_M1	SAI3_SDI						IO	I	down	Level2	√	
43	ETH_RMII0_MDIO/DSM_AUD_LP_M1/SAI3_SDO/GPIO2_B7_d	GPIO2_B7	ETH_RMII0_MDIO	DSM_AUD_LP_M1	SAI3_SDO						IO	I	down	Level2	√	
42	ETH_RMII0_RXDVCRS/SAI3_MCLK/GPIO2_C0_d	GPIO2_C0	ETH_RMII0_RXDVCRS		SAI3_MCLK						IO	I	down	Level2	√	
37	SDMMC_CLK/GPIO3_A0_d	GPIO3_A0	SDMMC_CLK								IO	I	down	Level3	√	
38	SDMMC_CMD/GPIO3_A1_d	GPIO3_A1	SDMMC_CMD								IO	I	down	Level2	√	
36	SDMMC_D0/GPIO3_A2_d	GPIO3_A2	SDMMC_D0								IO	I	down	Level2	√	VCCIO4_VCC
35	SDMMC_D1/TEST_CLK_OUT/GPIO3_A3_d	GPIO3_A3	SDMMC_D1	TEST_CLK_OUT							IO	I	down	Level2	√	
41	SDMMC_D2/JTAG_TCK_M0/GPIO3_A4_d	GPIO3_A4	SDMMC_D2	JTAG_TCK_M0							IO	I	down	Level2	√	

Pin	Pin Name	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Pad Type①	Def③	Pull	Drive Strength②	INT	Power Domain
40	SDMMC_D3/JTAG_TMS_M0/GPIO3_A5_d	GPIO3_A5	SDMMC_D3	JTAG_TMS_M0							IO	I	down	Level2	√	
34	SAI2_SDI_M0/ETH_RMII1_RXD0/GPIO3_A6_d	GPIO3_A6	SAI2_SDI_M0	ETH_RMII1_RXD0							IO	I	down	Level2	√	
33	SAI2_SCLK_M0/ETH_RMII1_RXD1/GPIO3_A7_d	GPIO3_A7	SAI2_SCLK_M0	ETH_RMII1_RXD1							IO	I	down	Level2	√	
32	SAI2_SDO_M0/ETH_RMII1_CLK/GPIO3_B0_d	GPIO3_B0	SAI2_SDO_M0	ETH_RMII1_CLK							IO	I	down	Level2	√	
31	SAI2_LRCK_M0/ETH_RMII1_TXD0/GPIO3_B1_d	GPIO3_B1	SAI2_LRCK_M0	ETH_RMII1_TXD0							IO	I	down	Level2	√	
30	UART5_CTSN_M0/ETH_RMII1_TXD1/GPIO3_B2_d	GPIO3_B2	UART5_CTSN_M0	ETH_RMII1_TXD1							IO	I	down	Level2	√	
29	UART5_RX_M0/ETH_RMII1_TXEN/GPIO3_B3_d	GPIO3_B3	UART5_RX_M0	ETH_RMII1_TXEN							IO	I	down	Level2	√	
28	UART5_TX_M0/ETH_RMII1_MDC/GPIO3_B4_d	GPIO3_B4	UART5_TX_M0	ETH_RMII1_MDC							IO	I	down	Level2	√	
27	UART5_RTSN_M0/ETH_RMII1_MDIO/GPIO3_B5_d	GPIO3_B5	UART5_RTSN_M0	ETH_RMII1_MDIO							IO	I	down	Level2	√	
26	SAI2_MCLK_M0/ETH_RMII1_RXDVCRS/GPIO3_B6_d	GPIO3_B6	SAI2_MCLK_M0	ETH_RMII1_RXDVCRS							IO	I	down	Level2	√	
81	MIPI_DPHY_DSI_TX_D0N/GPO4_A0_z	GPO4_A0	MIPI_DPHY_DSI_TX_D0N								O	O	Z			MIPI
82	MIPI_DPHY_DSI_TX_D0P/GPO4_A1_z	GPO4_A1	MIPI_DPHY_DSI_TX_D0P								O	O	Z			
79	MIPI_DPHY_DSI_TX_D1N/GPO4_A2_z	GPO4_A2	MIPI_DPHY_DSI_TX_D1N								O	O	Z			
80	MIPI_DPHY_DSI_TX_D1P/GPO4_A3_z	GPO4_A3	MIPI_DPHY_DSI_TX_D1P								O	O	Z			
77	MIPI_DPHY_DSI_TX_CLKN/GPO4_A4_z	GPO4_A4	MIPI_DPHY_DSI_TX_CLKN								O	O	Z			
78	MIPI_DPHY_DSI_TX_CLKP/GPO4_A5_z	GPO4_A5	MIPI_DPHY_DSI_TX_CLKP								O	O	Z			
63	SARADC_IN0/GPIO4_B0_z	GPIO4_B0	SARADC_IN0								IO	I	z	Level1	√	SARADC
62	SARADC_IN1/GPIO4_B1_z	GPIO4_B1	SARADC_IN1								IO	I	z	Level1	√	
61	SARADC_IN2/GPIO4_B2_z	GPIO4_B2	SARADC_IN2								IO	I	z	Level1	√	
60	SARADC_IN3/GPIO4_B3_z	GPIO4_B3	SARADC_IN3								IO	I	z	Level1	√	
72	USB20_OTG0_DP	USB20_OTG0_DP									A					USB
71	USB20_OTG0_DM	USB20_OTG0_DM									A					
74	USB20_OTG1_DP	USB20_OTG1_DP									A					
73	USB20_OTG1_DM	USB20_OTG1_DM									A					
68	ACODEC_ADC_INP	ACODEC_ADC_INP									A					ACODEC ADC
67	ACODEC_ADC_INN	ACODEC_ADC_INN									A					
66	ACODEC_ADC_VCM	ACODEC_ADC_VCM									A					
65	ACODEC_ADC_AVDD1V6	ACODEC_ADC_AVDD1V6									A					

Notes:

□: Pad types: I = input, O = output, I/O = input/output (bidirectional)
AP = Analog Power, AG = Analog Ground
DP = Digital Power, DG = Digital Ground
A = Analog

□: Output Drive Unit is mA, only Digital IO has drive value;

□: Reset state: I = input, O = output;

2.9 IO Pin Name Description

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 2-4 IO function description list

Interface	Pin Name	Direction	Description
Misc	OSC_XIN	I	Clock input of crystal XO
	OSC_XOUT	O	Clock output of crystal XO
	NPOR	I	Chip hardware reset input
	OSC_CLK_OUT	O	OSC Clock Output for external function module
	REF_CLK0_OUT	O	REF Clock Output for external function module
	REF_CLK1_OUT	O	REF Clock Output for external function module
	ETH_CLK0_25M_OUT	O	REF Clock Output for external function module
	ETH_CLK1_25M_OUT	O	REF Clock Output for external function module
	AUPLL_CLK_IN	I	REF Clock Input for internal PLL
	TEST_CLK_OUT	O	Chip internal clock output for measurement
	PMU_SLEEP	O	Chip low power mode output indication signal
	CORE_POWER_OFF	O	Chip low power mode output indication signal
	TSADC_CTRL	O	Chip high temperature output indication signal
	CLK_32K	I/O	32K clock If configured as input，clock is provided from external circuit； If configured as output，clock is provided from internal circuit of chip；

Interface	Pin Name	Direction	Description
SWJ-DP	JTAG_TCK_M*i* (*i*=0~1)	I	SWD interface clock input for CPU
	JTAG_TMS_M*i* (*i*=0~1)	I/O	SWD interface data input/output for CPU

Interface	Pin Name	Direction	Description
SD/MMC Host Controller	SDMMC_CLK	O	sdmmc card clock
	SDMMC_CMD	I/O	sdmmc card command output and response input
	SDMMC_D[*i*] (*i*=0~3)	I/O	sdmmc card data input and output

Interface	Pin Name	Direction	Description

FSPI Controller	FSPI_CLK	O	fspi serial clock
	FSPI_CSN	O	fspi chip select signal, low active
	FSPI_D*i*(*i*=0~3)	I/O	fspi serial data input/output signal

Interface	Pin Name	Direction	Description
Display Interface	VO_LCDC_DEN	O	LCDC RGB interface data enable, MCU interface REN signal
	VO_LCDC_VSYNC	O	LCDC RGB interface vertical sync pulse, MCU interface CSN signal
	VO_LCDC_HSYNC	O	LCDC RGB interface horizontal sync pulse, MCU interface WEN signal
	VO_LCDC_CLK	O	LCDC RGB interface display clock out, MCU interface RS signal
	VO_LCDC_D*i*(*i*=0~23)	I/O	LCDC RGB interface data output, MCU interface data input/output

Interface	Pin Name	Direction	Description
SAI0	SAI0_MCLK	I/O	I2S/PCM/TDM master clock
	SAI0_SCLK	I/O	I2S/PCM/TDM serial clock
	SAI0_LRCK	I/O	I2S/PCM/TDM channel indication signal
	SAI0_SDO	O	I2S/PCM/TDM serial data output
	SAI0_SDI0	I	I2S/PCM/TDM serial data input
	SAI0_SDI1	I	I2S/PCM/TDM serial data input
	SAI0_SDI2	I	I2S/PCM/TDM serial data input
	SAI0_SDI3	I	I2S/PCM/TDM serial data input

Interface	Pin Name	Direction	Description
SAI1	SAI1_MCLK	I/O	I2S/PCM/TDM master clock
	SAI1_SCLK	I/O	I2S/PCM/TDM serial clock
	SAI1_LRCK	I/O	I2S/PCM/TDM channel indication signal
	SAI1_SDO0	O	I2S/PCM/TDM serial data output
	SAI1_SDO1	O	I2S/PCM/TDM serial data output
	SAI1_SDO2	O	I2S/PCM/TDM serial data output
	SAI1_SDO3	O	I2S/PCM/TDM serial data output
	SAI1_SDI	I	I2S/PCM/TDM serial data input

Interface	Pin Name	Direction	Description
SAI2	SAI2_MCLK_M*i*(*i*=0~1)	I/O	I2S/PCM/TDM master clock
	SAI2_SCLK_M*i*(*i*=0~1)	I/O	I2S/PCM/TDM serial clock
	SAI2_LRCK_M*i*(*i*=0~1)	I/O	I2S/PCM/TDM channel indication signal
	SAI2_SDO_M*i*(*i*=0~1	O	I2S/PCM/TDM serial data output

Interface	Pin Name	Direction	Description
	)		
	SAI2_SDI_M*i*(*i*=0~1)	I	I2S/PCM/TDM serial data input

Interface	Pin Name	Direction	Description
SAI3	SAI3_MCLK	I/O	I2S/PCM/TDM master clock
	SAI3_SCLK	I/O	I2S/PCM/TDM serial clock
	SAI3_LRCK	I/O	I2S/PCM/TDM channel indication signal
	SAI3_SDO	O	I2S/PCM/TDM serial data output
	SAI3_SDI	I	I2S/PCM/TDM serial data input

Interface	Pin Name	Direction	Description
PDM	PDM_CLK0	O	PDM sampling clock
	PDM_CLK1	O	PDM sampling clock
	PDM_SDI*i*(*i*=0~3)	I	PDM data

Interface	Pin Name	Direction	Description
Audio DSM	DSM_AUD_RP_M*i*(*i*=0~1)	O	Audio DSM Right Channel positive differential data output
	DSM_AUD_RN_M*i*(*i*=0~1)	O	Audio DSM Right Channel negative differential data output
	DSM_AUD_LP_M*i*(*i*=0~1)	O	Audio DSM Left Channel positive differential data output
	DSM_AUD_LN_M*i*(*i*=0~1)	O	Audio DSM Left Channel negative differential data output

Interface	Pin Name	Direction	Description
SPDIF	SPDIF_TX	O	SPDIF output data
	SPDIF_RX	I	SPDIF input data

Interface	Pin Name	Direction	Description
SPI0/SPI1	SPI*i*_CLK(*i*=0~1)	I/O	SPI serial clock
	SPI*i*_CSN0(*i*=0~1)	I/O	SPI chip select signal, low active
	SPI*i*_CSN1(*i*=0~1)	O	SPI chip select signal, low active
	SPI*i*_MISO(*i*=0~1)	I/O	SPI serial data input/output
	SPI*i*_MOSI(*i*=1~2)	I/O	SPI serial data input/output

Interface	Pin Name	Direction	Description

SPI2	SPI2_CLK	I	SPI serial clock
	SPI2_CSN)	I	SPI chip select signal, low active
	SPI2_MOSI	I	SPI serial data input
	SPI2_MISO	O	SPI serial data output

Interface	Pin Name	Direction	Description
PWM	PWM0_CH*i*(*i*=0~3)	I/O	Pulse Width Modulation input and output
	PWM1_CH*i*(*i*=0~7)	I/O	Pulse Width Modulation input and output
	PWM1_BIP_CNTR_A*i*(*i*=0~5)	I	Phase A input for AB phase counter
	PWM1_BIP_CNTR_B*i*(*i*=0~5)	I	Phase B input for AB phase counter

Interface	Pin Name	Direction	Description
I2C	I2C*i*_SDA (*i*=0,1,2)	I/O	I2C data
	I2C*i*_SCL (*i*=0,1,2)	I/O	I2C clock

Interface	Pin Name	Direction	Description
UART	UART0_RX	I	UART serial data input
	UART0_TX	O	UART serial data output
	UART*i*_RX (*i*=1,2,3,4)	I	UART serial data input
	UART*i*_TX (*i*=1,2,3,4)	O	UART serial data output
	UART*i*_CTSN (*i*=1,2,3,4)	I	UART clear to send modem status input
	UART*i*_RTSN (*i*=1,2,3,4)	O	UART modem control request to send output
	UART5_RX_M*i*(*i*=0~1)	I	UART serial data input
	UART5_TX_M*i*(*i*=0~1)	O	UART serial data output
	UART5_CTSN_M*i*(*i*=0~1)	I	UART clear to send modem status input
	UART5_RTSN_M*i*(*i*=0~1)	O	UART modem control request to send output

Interface	Pin Name	Direction	Description
Touch Key	TOUCH_KEY_IN*i*(*i*=0~7)	I	Touch Key data input

Interface	Pin Name	Direction	Description
	TOUCH_KEY_DRIVE	O	Touch Key drive clock output

Interface	Pin Name	Direction	Description
RMII	ETH_RMII*i*_CLK(*i*=0~1)	I/O	RMII REC_CLK output or external clock input
	ETH_RMII*i*_MDC(*i*=0~1)	O	RMII management interface clock
	ETH_RMII*i*_MDIO(*i*=0~1)	I/O	RMII management interface data
	ETH_RMII*i*_TXD0(*i*=0~1)	O	RMII TX data
	ETH_RMII*i*_TXD1(*i*=0~1)	O	RMII TX data
	ETH_RMII*i*_RXD0(*i*=0~1)	I	RMII RX data
	ETH_RMII*i*_RXD1(*i*=0~1)	I	RMII RX data
	ETH_RMII*i*_TXEN(*i*=0~1)	O	RMII TX data enable
	ETH_RMII*i*_RXDVCRS(*i*=0~1)	I	RMII RX indication signal

Interface	Pin Name	Direction	Description
FLEXBUS	FLEXBUS0_CLK	O	FLEXBUS0 clock output
	FLEXBUS0_D*i*(*i*=0~15)	I/O	FLEXBUS0 data input/output
	FLEXBUS1_CLK	I/O	FLEXBUS1 clock input/output DVP mode, acted as VICAP_CLK input
	FLEXBUS1_D*i*(*i*=0~15)	I	FLEXBUS0 data input DVP mode, FLEXBUS1_D6 and FLEXBUS1_D7 acted as VICAP_VSYNC and VICAP_HREF input signal separately. FLEXBUS1_D8~ FLEXBUS1_D16 acted as VICAP_DATA0~ VICAP_DATA7 input signal.
	FLEXBUS0_CSN_M*i*(*i*=0~5)	O	FLEXBUS0 chip selection output
	FLEXBUS1_CSN_M*i*(*i*=0~5)	O	FLEXBUS1 chip selection output

Interface	Pin Name	Direction	Description
Master DSMC	DSMC_CLKP	O	Master DSMC positive differential clock output
	DSMC_CLKN	O	Master DSMC negative differential clock output

Interface	Pin Name	Direction	Description
	DSMC_D*i*(*i*=0~15)	I/O	Master DSMC data input/output
	DSMC_DQS*i*(*i*=0~1)	I/O	Master DSMC data write mask output and data strobe input
	DSMC_CSN*i*(*i*=0~3)	O	Master DSMC chip selection output
	DSMC_RESETN	O	Master DSMC reset signal output
	DSMC_RDYN	I	Master DSMC ready indication signal input
	DSMC_INT*i*(*i*=0~3)	I	Master DSMC interrupt indication signal input

Interface	Pin Name	Direction	Description
Slave DSMC	DSMC_SLV_CLK	I	Slave DSMC clock input
	DSMC_SLV_D*i*(*i*=0~7)	I/O	Slave DSMC data input/output
	DSMC_SLV_DQS0	I/O	Slave DSMC data write mask input and data strobe output
	DSMC_SLV_CSN0	I	Slave DSMC chip selection input
	DSMC_SLV_RDYN	O	Slave DSMC ready indication signal output
	DSMC_SLV_INT	O	Slave DSMC interrupt indication signal output

Interface	Pin Name	Direction	Description
Rockchip matrix IO	RM_IO*i*(*i*=0~31)	I/O	IO matrix

Interface	Pin Name	Direction	Description
SARADC	SARADC_IN*i*(*i*=0~3)	I/O	SARADC input signal for 4 channel

Interface	Pin Name	Direction	Description
MIPI DSI	MIPI_DPHY_DSI_TX_D*i*P(*i*=0~1)	I/O	MIPI DSI positive differential data line transceiver output
	MIPI_DPHY_DSI_TX_D*i*N(*i*=0~1)	I/O	MIPI DSI negative differential data line transceiver output
	MIPI_DPHY_DSI_TX_CLKP	I/O	MIPI DSI positive differential clock line transceiver output
	MIPI_DPHY_DSI_TX_CLKN	I/O	MIPI DSI negative differential clock line transceiver output

Interface	Pin Name	Direction	Description
USB 2.0	USB20_OTG0_DP	I/O	USB 2.0 Port0 Data signal DP
	USB20_OTG0_DM	I/O	USB 2.0 Port0 Data signal DM
	USB20_OTG1_DP	I/O	USB 2.0 Port1 Data signal DP
	USB20_OTG1_DM	I/O	USB 2.0 Port1 Data signal DM

	USB20_OTG0_VBUS DET	I	Port0 insert detect when act as USB device
	USB20_OTG0_ID	I	Port0 USB Mini-Receptacle Identifier

Interface	Pin Name	Direction	Description
ACODEC ADC	ACODEC_ADC_INP	I	ADC input signal
	ACODEC_ADC_INN	I	ADC input signal
	ACODEC_ADC_VCM	O	Internal voltage output
	ACODEC_ADC_AVDD 1V6	O	Internal voltage output

Interface	Pin Name	Direction	Description
DDR Interface	DDR_CLKP	O	Active-high clock signal to the memory device.
	DDR_CLKN	O	Active-low clock signal to the memory device.
	DDR_CKE	O	Active-high clock enable signal to the memory device
	DDR_CSN	O	Active-low chip select signal to the memory device.
	DDR2_RASN/DDR3_A 10	O	DDR2: Active-low row address strobe to the memory device. DDR3: Address signal to the memory device.
	DDR2_CASN/DDR3_B A1	O	DDR2: Active-low column address strobe to the memory device. DDR3: Bank address signal to the memory device.
	DDR2_WEN/DDR3_R ASN	O	DDR2: Active-low write enable strobe to the memory device. DDR3: Active-low row address strobe to the memory device.
	DDR2_BA0/DDR3_CA SN	O	DDR2: Bank address signal to the memory device. DDR3: Active-low column address strobe to the memory device.
	DDR2_BA1/DDR3_W EN	O	DDR2: Bank address signal to the memory device. DDR3: Active-low write enable strobe to the memory device.
	DDR2_BA2/DDR3_BA 2	O	DDR2: Bank address signal to the memory device. DDR3: Bank address signal to the memory device.
	DDR2_A0/DDR3_A12	O	DDR2: Address signal to the memory device.

Interface	Pin Name	Direction	Description
			DDR3: Address signal to the memory device.
	DDR2_A1/DDR3_A3	O	DDR2: Address signal to the memory device. DDR3: Address signal to the memory device.
	DDR2_A2/DDR3_A4	O	DDR2: Address signal to the memory device. DDR3: Address signal to the memory device.
	DDR2_A3/DDR3_A0	O	DDR2: Address signal to the memory device. DDR3: Address signal to the memory device.
	DDR2_A4/DDR3_A1	O	DDR2: Address signal to the memory device. DDR3: Address signal to the memory device.
	DDR2_A5/DDR3_A5	O	DDR2: Address signal to the memory device. DDR3: Address signal to the memory device.
	DDR2_A6/DDR3_A6	O	DDR2: Address signal to the memory device. DDR3: Address signal to the memory device.
	DDR2_A7/DDR3_A2	O	DDR2: Address signal to the memory device. DDR3: Address signal to the memory device.
	DDR2_A8/DDR3_A8	O	DDR2: Address signal to the memory device. DDR3: Address signal to the memory device.
	DDR2_A9/DDR3_A7	O	DDR2: Address signal to the memory device. DDR3: Address signal to the memory device.
	DDR2_A10/DDR3_BA0	O	DDR2: Address signal to the memory device. DDR3: Bank address signal to the memory device.
	DDR2_A11/DDR3_A11	O	DDR2: Address signal to the memory device. DDR3: Address signal to the memory device.
	DDR2_A12/DDR3_A9	O	DDR2: Address signal to the memory device. DDR3: Address signal to the memory device.
	DDR2_A13/DDR3_A13	O	DDR2: Address signal to the memory device. DDR3: Address signal to the memory device.
	DDR2_A14/DDR3_A14	O	DDR2: Address signal to the memory device. DDR3: Address signal to the memory device.
	DDR2_A15/DDR3_A15	O	DDR2: Address signal to the memory device. DDR3: Address signal to the memory device.
	DDR_DQ*i*(*i*=0~15)	I/O	Bidirectional data line to the memory device.
	DDR_DQS*i*P(i=0~1)	I/O	Active-high bidirectional data strobes to the memory device.
	DDR_DQS*i*N(*i*=0~1)	I/O	Active-low bidirectional data strobes to the memory device.
	DDR_DM*i*(1=0~1)	O	Data mask signal to the memory device.
	DDR_ODT	O	On-Die Termination output signal.
	DDR3_RESET	O	Reset signal to the memory device.
	DDR_VREF_CA	O	CA VREF for DDR

Interface	Pin Name	Direction	Description
	DDR_VREF_DQ	O	DQ VREF for DDR
	DDR_RZQ	O	RZQ for DDR
	DDR_OPEN0	O	Debug IO
	DDR_OPEN1	O	Debug IO

2.10 Rockchip Matrix IO Function List

RK3506G2 supports one Rockchip Matrix IO (RM_IO) which are designed to let numerous functional signals share limited pin interfaces. Within the same matrix, any function signal can be mapped to any pin interface by software configurable. RM_IO support 98 function signals map to 32 pin interfaces (GPIO0_A0~GPIO0_C7, GPIO1_B1~GPIO1_B3, GPIO1_C2~GPIO1_C3, GPIO1_D1~GPIO1_D3)

Table 2-5 Matrix IO function list

Function Index	RM_IO	Function Index	RM_IO
1	UART1_TX	50	TOUCH_KEY_IN7
2	UART1_RX	51	SAI0_MCLK
3	UART2_TX	52	SAI0_SCLK
4	UART2_RX	53	SAI0_LRCK
5	UART3_TX	54	SAI0_SDI0
6	UART3_RX	55	SAI0_SDI1
7	UART3_CTSN	56	SAI0_SDI2
8	UART3_RTSN	57	SAI0_SDI3
9	UART4_TX	58	SAI0_SDO
10	UART4_RX	59	SAI1_MCLK
11	UART4_CTSN	60	SAI1_SCLK
12	UART4_RTSN	61	SAI1_LRCK
13	MIPI_DPHY_DSI_TX_TE	62	SAI1_SDI
14	CLK_32K	63	SAI1_SDO0
15	I2C0_SCL	64	SAI1_SDO1
16	I2C0_SDA	65	SAI1_SDO2
17	I2C1_SCL	66	SAI1_SDO3
18	I2C1_SDA	67	SPI0_CLK
19	I2C2_SCL	68	SPI0_MOSI
20	I2C2_SDA	69	SPI0_MISO
21	PDM_CLK0	70	SPI0_CSN0
22	PDM_SDI0	71	SPI0_CSN1
23	PDM_SDI1	72	SPI1_CLK

Function Index	RM_IO	Function Index	RM_IO
24	PDM_SDI2	73	SPI1_MOSI
25	PDM_SDI3	74	SPI1_MISO
26	CAN1_TX	75	SPI1_CSN0
27	CAN1_RX	76	SPI1_CSN1
28	CAN0_TX	77	TSADC_CTRL
29	CAN0_RX	78	PMU_SLEEP
30	PWM0_CH0	79	CORE_POWER_OFF
31	PWM0_CH1	80	SPDIF_TX
32	PWM0_CH2	81	SPDIF_RX
33	PWM0_CH3	82	PWM1_BIP_CNTR_A0
34	PWM1_CH0	83	PWM1_BIP_CNTR_A1
35	PWM1_CH1	84	PWM1_BIP_CNTR_A2
36	PWM1_CH2	85	PWM1_BIP_CNTR_A3
37	PWM1_CH3	86	PWM1_BIP_CNTR_A4
38	PWM1_CH4	87	PWM1_BIP_CNTR_A5
39	PWM1_CH5	88	PWM1_BIP_CNTR_B0
40	PWM1_CH6	89	PWM1_BIP_CNTR_B1
41	PWM1_CH7	90	PWM1_BIP_CNTR_B2
42	TOUCH_KEY_DRIVE	91	PWM1_BIP_CNTR_B3
43	TOUCH_KEY_IN0	92	PWM1_BIP_CNTR_B4
44	TOUCH_KEY_IN1	93	PWM1_BIP_CNTR_B5
45	TOUCH_KEY_IN2	94	PDM_CLK1
46	TOUCH_KEY_IN3	95	ETH_RMII0_PPSCLK
47	TOUCH_KEY_IN4	96	ETH_RMII0_PPSTRIG
48	TOUCH_KEY_IN5	97	ETH_RMII1_PPSCLK
49	TOUCH_KEY_IN6	98	ETH_RMII1_PPSTRIG

2.11 FLEXBUS Interface Typical Application Example

RK3506G2 FLEXBUS can be adapted to certain timing interface through software programming. In this section, we will list the pin mapping relationship for some typical application interfaces, such as ADC, DAC, DVP, QSPI LCD panel.

Table 2-6 Pin Mapping between FLEXBUS and ADC

FLEXBUS Interface	Direction	ADC Application Interface
FLEXBUS1_D0	Input	ADC_D0

FLEXBUS1_D1	Input	ADC_D1
FLEXBUS1_D2	Input	ADC_D2
FLEXBUS1_D3	Input	ADC_D3
FLEXBUS1_D4	Input	ADC_D4
FLEXBUS1_D5	Input	ADC_D5
FLEXBUS1_D6	Input	ADC_D6
FLEXBUS1_D7	Input	ADC_D7
FLEXBUS1_D8	Input	ADC_D8
FLEXBUS1_D9	Input	ADC_D9
FLEXBUS1_D10	Input	ADC_D10
FLEXBUS1_D11	Input	ADC_D11
FLEXBUS1_D12	Input	ADC_D12
FLEXBUS1_D13	Input	ADC_D13
FLEXBUS1_D14	Input	ADC_D14
FLEXBUS1_D15	Input	ADC_D15
FLEXBUS1_CLK	Input Output	ADC_CLK_IN(from ADC) ADC_CLK_OUT(To ADC)

Table 2-7 Pin Mapping between FLEXBUS and DAC

FLEXBUS Interface	Direction	DAC Application Interface
FLEXBUS0_D0	Output	DAC_D0
FLEXBUS0_D1	Output	DAC_D1
FLEXBUS0_D2	Output	DAC_D2
FLEXBUS0_D3	Output	DAC_D3
FLEXBUS0_D4	Output	DAC_D4
FLEXBUS0_D5	Output	DAC_D5
FLEXBUS0_D6	Output	DAC_D6
FLEXBUS0_D7	Output	DAC_D7
FLEXBUS0_D8	Output	DAC_D8
FLEXBUS0_D9	Output	DAC_D9
FLEXBUS0_D10	Output	DAC_D10
FLEXBUS0_D11	Output	DAC_D11
FLEXBUS0_D12	Output	DAC_D12
FLEXBUS0_D13	Output	DAC_D13
FLEXBUS0_D14	Output	DAC_D14
FLEXBUS0_D15	Output	DAC_D15

FLEXBUS0_CLK	Output	DAC_CLK
FLEXBUS0_CSN	Output	DAC_CS

Table 2-8 Pin Mapping between FLEXBUS and DVP Camera

FLEXBUS Interface	Direction	DVP Application Interface
FLEXBUS1_D1	Input	VI_CIF_VSYNC
FLEXBUS1_D2	Input	VI_CIF_HREF
FLEXBUS1_D3	Input	VI_CIF_D0
FLEXBUS1_D4	Input	VI_CIF_D1
FLEXBUS1_D5	Input	VI_CIF_D2
FLEXBUS1_D6	Input	VI_CIF_D3
FLEXBUS1_D7	Input	VI_CIF_D4
FLEXBUS1_D8	Input	VI_CIF_D5
FLEXBUS1_D12	Input	VI_CIF_D6
FLEXBUS1_D13	Input	VI_CIF_D7
FLEXBUS1_CLK	Input	VI_CIF_CLK

Table 2-9 Pin Mapping between FLEXBUS and QSPI LCD Panel

FLEXBUS Interface	Direction	QSPI LCD Application Interface
FLEXBUS0_D0	Inout	QSPI_D0
FLEXBUS0_D1	Inout	QSPI_D1
FLEXBUS0_D2	Inout	QSPI_D2
FLEXBUS0_D3	Inout	QSPI_D3
FLEXBUS0_CLK	Output	QSPI_CLK
FLEXBUS0_CS	Output	QSPI_CS

Chapter 3 Electrical Specification

3.1 Absolute Ratings

The below table provides the absolute ratings.
Absolute maximum or minimum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

Table 3-1 Absolute ratings

Parameters	Related Power Group	Min	Max	Unit
Supply voltage for CPU	CPU_DVDD	-0.30	1.225	V
Supply voltage for LOGIC	LOGIC_DVDD	-0.30	1.05	V
Supply voltage for PMU	PMU_LOGIC_DVDD0V9	-0.30	1.05	V
0.9V supply voltage	AVDD_0V9 MIPI_DPHY_AVDD0V9 USB20_OTG_DVDD0V9	-0.30	1.05	V
1.8V supply voltage	SYS_PLL_AVDD1V8 AVDD_1V8 AVCC_1V8 ACODEC_ADC_AVDD1V8 SARADC_AVDD1V8 TSADC_VCC1V8 MIPI_DPHY_AVDD1V8 USB20_OTG_AVDD1V8	-0.30	2.10	V
3.3V supply voltage	PMUIO_VCC3V3 USB20_OTG_AVDD3V3	-0.30	3.80	V
1.8V/3.3V supply voltage	VCCIO1_VCC VCCIO2_VCC VCCIO3_VCC VCCIO4_VCC	-0.30	3.80	V
Supply voltage for DDR IO	DDR_VDDQ	-0.30	2.00	V
Storage Temperature	Tstg	-40	125	℃
Max Conjunction Temperature	Tj		125	℃

3.2 Recommended Operating Condition

The following table describes the recommended operating condition.

Table 3-2 Recommended operating condition

Parameters	Symbol	Min	Typ	Max	Unit
Voltage for CPU	CPU_DVDD	0.807	0.95	1.155	V
Voltage for LOGIC	LOGIC_DVDD	0.855	0.90	0.998	V
Voltage for PMU	PMU_LOGIC_DVDD0V9	0.81	0.90	0.99	V
Voltage for PLL Analog (1.8V)	SYS_PLL_AVDD1V8	1.62	1.80	1.98	V
Voltage for GPIO (3.3V only)	PMUIO_VCC3V3	3.00	3.30	3.63	V

Parameters	Symbol	Min	Typ	Max	Unit
Voltage for GPIO (1.8V/3.3V)	VCCIO1_VCC VCCIO2_VCC VCCIO3_VCC VCCIO4_VCC	1.62 3.00	1.80 3.30	1.98 3.63	V
Voltage for USB/MIPI Analog(0.9V)	AVDD_0V9	0.81	0.90	0.99	V
Voltage for USB/MIPI/TSADC Analog (1.8V)	AVDD_1V8	1.62	1.80	1.98	V
Voltage for ACODEC ADC/SARADC/OTP Analog (1.8V)	AVCC_1V8	1.62	1.80	1.98	V
Voltage for ACODEC ADC Analog (1.8V)	ACODEC_ADC_AVDD1V8	1.62	1.80	1.98	V
Voltage for SARADC/OTP Analog (1.8V)	SARADC_AVDD1V8	1.62	1.80	1.98	V
Voltage for TSADC Analog (1.8V)	TSADC_VCC1V8	1.62	1.80	1.98	V
Voltage for MIPI Analog(0.9V)	MIPI_DPHY_AVDD0V9	0.81	0.90	0.99	V
Voltage for MIPI Analog (1.8V)	MIPI_DPHY_AVDD1V8	1.62	1.80	1.98	V
Voltage for USB Analog (0.9V)	USB20_OTG_DVDD0V9	0.81	0.90	0.99	V
Voltage for USB Analog (1.8V)	USB20_OTG_AVDD1V8	1.62	1.8	1.98	V
Voltage for USB Analog (3.3V)	USB20_OTG_AVDD3V3	3.00	3.30	3.63	V
DDR2 IO power	DDR_VDDQ	1.71	1.80	1.89	V
DDR3 IO power	DDR_VDDQ	1.425	1.50	1.575	V
DDR3L IO Power	DDR_VDDQ	1.283	1.35	1.418	V
OSC input clock frequency	F_{osc}	N/A	24	N/A	MHz
Ambient Operating Temperature	T_A	-20	25	80	℃

Notes: Please refer to "Power/Ground IO Description" section for relationship between power symbol and chip model

3.3 DC Characteristics

Table 3-3 DC Characteristics

Parameters		Symbol	Min	Typ	Max	Unit
Digital GPIO @3.3V	Input Low Voltage	Vil	-0.3	NA	0.8	V
	Input High Voltage	Vih	2.0	NA	VDDO+0.3	V
	Output Low Voltage	Vol	-0.3	NA	0.4	V
	Output High Voltage	Voh	2.4	NA	VDDO+0.3	V
	Pullup Resistor	Rpu	16	30	43	Kohm
	Pulldown Resistor	Rpd	16	30	43	Kohm
Digital GPIO @1.8V	Input Low Voltage	Vil	-0.3	NA	0.35*VDDO	V
	Input High Voltage	Vih	0.65*VDDO	NA	VDDO+0.3	V
	Output Low Voltage	Vol	-0.3	NA	0.4	V
	Output High Voltage	Voh	1.4	NA	VDDO+0.3	V
	Pullup Resistor	Rpu	16	30	43	Kohm
	Pulldown Resistor	Rpd	16	30	43	Kohm

Parameters		Symbol	Min	Typ	Max	Unit
DDR IO @ DDR2 mode	Input High Voltage	Vih_ddr	VREF + 0.13	NA	DDR_VDDQ	V
	Input Low Voltage	Vil_ddr	VSS	NA	VREF - 0.13	V
	Output High Voltage	Voh_ddr	VREF + 0.13	NA	DDR_VDDQ	V
	Output Low Voltage	Vol_ddr	VSS	NA	VREF-0.13	V
DDR IO @ @DDR3 mode	Input High Voltage	Vih_ddr	VREF + 0.10	NA	DDR_VDDQ	V
	Input Low Voltage	Vil_ddr	VSS	NA	VREF - 0.10	V
	Output High Voltage	Voh_ddr	VREF + 0.10	NA	DDR_VDDQ	V
	Output Low Voltage	Vol_ddr	VSS	NA	VREF - 0.10	V
DDR IO @ @DDR3L mode	Input High Voltage	Vih_ddr	VREF + 0.09	NA	DDR_VDDQ	V
	Input Low Voltage	Vil_ddr	VSS	NA	VREF - 0.09	V
	Output High Voltage	Voh_ddr	VREF + 0.09	NA	DDR_VDDQ	V
	Output Low Voltage	Vol_ddr	VSS	NA	VREF - 0.09	V

3.4 Electrical Characteristics for General IO

Table 3-4 Electrical Characteristics for Digital General IO

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
Digital GPIO @3.3V	Input leakage current	Ii	Vin = 3.3V or 0V	NA	NA	15	uA
	Tri-state output leakage current	Ioz	Vout = 3.3V or 0V	NA	NA	15	uA
	High level input current	Iih	Vin = 3.3V, pulldown disabled	NA	NA	15	uA
			Vin = 3.3V, pulldown enabled	NA	NA	250	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	NA	NA	15	uA
			Vin = 0V, pullup enabled	NA	NA	250	uA
Digital GPIO @1.8V	Input leakage current	Ii	Vin = 1.8V or 0V	NA	NA	15	uA
	Tri-state output leakage current	Ioz	Vout = 1.8V or 0V	NA	NA	15	uA
	High level input current	Iih	Vin = 1.8V, pulldown disabled	NA	NA	15	uA
			Vin = 1.8V, pulldown enabled	NA	NA	150	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	NA	NA	15	uA
			Vin = 0V, pullup enabled	NA	NA	150	uA

3.5 Electrical Characteristics for PLL

Table 3-5 Electrical Characteristics for FRAC PLL

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
	Input clock frequency(Frac)	F_{in}	Fin = FREF	10	NA	1200	MHz
	VCO operating range	F_{vco}	Fvco = FREF * FBDIV	950	NA	3800	MHz
	Output clock frequency	F_{out}	Fout = Fvco/POSTDIV	19	NA	3800	MHz
	Lock time	T_{lt}	FREF=24M,REFDIV=1	NA	250	500	Input clock cycles

Notes:
① REFDIV is the input divider value;
② FBDIV is the feedback divider value;
③ POSTDIV is the output divider value.

3.6 Electrical Characteristics for USB2.0 Interface

Table 3-6 Electrical Characteristics for USB2.0 Interface

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Transmitter						
Output Resistance	ROUT	Classic mode (Vout = 0 or 3.3V)	40.5	45	49.5	ohms
		HS mode (Vout = 0 to 800mV)	40.5	45	49.5	ohms
Output Capacitance	COUT	seen from D+ or D-			3	pF
Output Common Mode Voltage	VM	Classic (LS/FS) mode	1.45	1.65	1.85	V
		HS mode	0.175	0.2	0.225	V
Differential output signal high	VOH	Classic (LS/FS); Io=0mA	2.97	3.3	3.63	V
		Classic (LS/FS); Io=6mA	2.2	2.7	NA	V
		HS mode; Io=0mA	360	400	440	mV
Differential output signal low	VOL	Classic (LS/FS); Io=0mA	-0.33	0	0.33	V
		Classic (LS/FS); Io=6mA	NA	0.3	0.8	V
		HS mode; Io=0mA	-40	0	40	mV
Receiver						
Receiver sensitivity	RSENS	Classic mode	NA	+-250	NA	mV
		HS mode	NA	+-25	NA	mV
Receiver common mode	RCM	Classic mode	0.8	1.65	2.5	V
		HS mode (differential and squelch comparator)	0.1	0.2	0.3	V
		HS mode (disconnect comparator)	0.5	0.6	0.7	V

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Input capacitance (seen at D+ or D-)			NA	NA	3	pF
Squelch threshold			100	NA	150	mV
Disconnect threshold			570	600	664	mV

3.7 Electrical Characteristics for SARADC

Table 3-7 Electrical Characteristics for SARADC

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Resolution			NA	10	NA	bit
Effective Number of Bit	ENOB		NA	9	NA	bit
Differential Non-Linearity	DNL		-1	NA	+1	LSB
Integral Non-Linearity	INL		-2	NA	+2	LSB
Reference voltage	VREFP		NA	1.8	NA	V
Input Capacitance	C_{IN}		NA	8	NA	pF
Sampling Rate	f_S		NA	NA	1	MS/s
Spurious Free Dynamic Range	SFDR	f_S=1MS/s f_{OUT}=1.17KHz	NA	61	NA	dB
Signal to Noise and Harmonic Ratio	SNDR		NA	56	NA	dB

3.8 Electrical Characteristics for TSADC

Table 3-8 Electrical Characteristics for TSADC

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Accuracy from -40℃ to 125℃	T_{JACC}		NA	NA	±5	℃
Sensing Temperature Range	T_{RANGE}		-40	NA	125	℃
Resolution	T_{LSB}		NA	0.6	NA	℃

3.9 Electrical Characteristics for CODEC ADC

Table 3-9 Electrical Characteristics for CODEC ADC

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Resolution				24		℃
Full Scale Input Range		0dB Gain in PGA state		+/- 1.0		Vrms
Input Resistance	RIN			20		Kohm
Input Capacitance	CIN			10		pF
Negative Gain Range	G(negative)		-9		0	dB
Negative Gain Step				3		dB/Step
Positive Gain Range	G(positive)		0		48	dB
Positive Gain Step				12		dB/Step
Signal to Noise Ratio	SNR	fs=48kHz -60dBFS, A-weighted		94		dB
Total Harmonic Distortion	THD	fs=48kHz -3dBFS, A-weighted		98		dB

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Power Supply Rejection	PSRR			90		dB

3.10 Electrical Characteristics for MIPI DSI

Table 3-10 Electrical Characteristics for MIPI DSI

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
HS TX static Common-mode voltage	Vcmtx		150	200	250	mV
HS transmit differential voltage	|VOD|		140	200	270	mV
HS Single ended output impedance	ZOS		40	50	62.5	ohm
HS TX 20%-80% rise time and fall time	Tr and Tf	HS bit rates<=1Gbps			0.3	UI
		1Gbps < HS bit rates <= 1.5Gbps			0.35	UI

Chapter 4 Thermal Management

4.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature has to be below 125℃.

4.2 Package Thermal Characteristics

Table 4-1 provides the thermal resistance characteristics for the package used on the SoC. The resulting simulation data for reference only, please prevail in kind test.

Table 4-1 Thermal Resistance Characteristics

Parameter	Symbol	Value	Unit	Note
Junction-to-ambient thermal resistance	θ_{JA}	17.87	(℃/W)	(1)
Junction-to-board thermal resistance	θ_{JB}	8.18	(℃/W)	(2)
Junction-to-case thermal resistance	θ_{JC}	14.83	(℃/W)	(3)
Thermal characterization parameter	ψ_{JT}	1.8	(℃/W)	(4)

Note (1): The package-board system is placed in the natural convection (JEDEC JESD51-2 standard), and the 2S2P test-board is designed in accordance with JESD 51-7/JESD 51-9. The actual system design and environment may be different. (The PCB is 4 layers, 114.3 mm*76.2 mm)
Note (2): θ_{JB} is measured in the special environment (JEDEC JESD51-8 standard), and the printed circuit board used to mount the devices is specified in JESD51-7.
Note (3): The thermal resistance θ_{JC} is provided in compliance with the JEDEC JESD51-14.
Note (4): ψ_{JT} - The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package, $\psi_{JT}$is measured in the test environment of θ_{JA} (JEDEC JESD51-2 standard).

