

**Rockchip  
RK3538  
Datasheet**

### Revision History

Date	Revision	Description
2026-02-02	1.0	Initial Release

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## Chapter 1 Introduction

### 1.1 Overview

RK3538 is a high performance quad-core application processor designed for smart IPTV/OTT and high-end multimedia application. It is a high integration and cost efficient SOC for 1080P video application.

Quad-core Cortex-A55 is integrated with separate Neon and FPU co-processor, each core has a 32KB L1 Cache and a 64KB L2 cache, also with shared 512KB L3 Cache to enhance system performance.

ARM Mali-G310 GPU supports high-resolution display and game. It handles graphics programs like OpenCL 3.0, OpenGL ES1.1/2.0/3.2, Vulkan 1.2.

Dedicated ARM TrustZone based secure system to handle safety management for video and display applications. It includes CRYPTO engine, RNG, firewall engine to guarantee the whole system's security.

32-bit DRAM interface providing high bandwidth DDR3(L)/LPDDR3/DDR4/LPDDR4(4X) support.

The advanced video decoder supports 60fps playback of 1080P full-high-definition video with up to 10-bit pixels. It supports AV1, H.265, H.264, VP9, etc. video standards.

Display controller supports flexible surface and output stream. Outputs include two outputs switchable between HDMI 2.1 transmitter with HDR, CEC, HDCP2.3 support and CVBS through VDAC.

In addition to these major elements, RK3538 processors have a broad range of peripheral interfaces like sdio, usb2, mac, i2s, etc. to enable communication with wireless base-band, other communications peripherals, audio codec, power management, and mass storage.

### 1.2 Features

#### 1.2.1 Application Processor

- Quad-core ARM Cortex-A55 CPU
- ARM Neon Advanced SIMD (single instruction, multiple data) support for accelerated media and signal processing computation
- Include VFP hardware to support single and double-precision operations
- ARMv8 Cryptography Extensions
- Integrated 32KB L1 instruction cache, 32KB L1 data cache and 64KB L2 data cache
- 512KB unified system L3 cache
- TrustZone technology support
- Separate power domains for CPU core system to support internal power switch and externally turn on/off based on different application scenario
- One isolated voltage domain

#### 1.2.2 Graphic Processor

- ARM Mali-G310 GPU
- API feature set with support for shader-based and fixed-function graphics APIs
- Anti-aliasing capabilities
- Effective core for General Purpose computing on GPU applications
- High memory bandwidth and low power consumption for 3D graphics content
- 8-bit, 10-bit, and 16-bit YUV input and output formats
- OpenCL 3.0, OpenGL ES1.1/2.0/3.2, Vulkan 1.2 Supported

### 1.2.3 Memory Organization

- Internal on-chip memory
  - BootRom
    - ◆ Support system boot from the following device:
      - SPI interface
      - eMMC interface
      - SD/MMC interface
      - NANDC interface
    - ◆ Support system code download by the following interface:
      - USB interface
  - 128KB Share Memory
  - 8KB PMU SRAM
- External off-chip memory
  - eMMC Interface
    - ◆ Fully compliant with JEDEC eMMC5.1 specification
    - ◆ Support HS400, support CMD Queue
    - ◆ Support three data bus width: 1bit, 4bits or 8bits
  - SD/MMC Interface
    - ◆ Compatible with SD3.0, MMC ver4.51
    - ◆ Data bus width is 4bits
  - Flexible Serial Flash Interface (FSPI)
    - ◆ Support transfer data from/to serial flash device
    - ◆ Support 1bit, 2bits, 4bits or 8bits data bus width
  - NANDC Flash Interface
    - ◆ Support Asynchronous Flash Interface with 8bits data width ("Asyn8x" for short)
    - ◆ Support 2NAND Flash devices(2 chip select)
    - ◆ Support SLC Flash
    - ◆ 16bit/1KB BCH/ECC: support 16bitBCH/ECC, which can detect and correct up to 16 error bits in every 1K bytes data and 4 bytes meta-data
- Dynamic Memory Interface : DDR3(L)/LPDDR3/DDR4/LPDDR4(4X)
  - Compatible with JEDEC standard DDR3/DDR3L/LPDDR3/DDR4/LPDDR4/LPDDR4X SDRAM
  - Supports 32 Bits data width, approximately 2GB addressing space

### 1.2.4 System Component

- MCU
  - RISC-V MCU in PMU domain with dedicated mailbox and watchdog.
  - Integrated Debug Controller with JTAG interface
- CRU (clock & reset unit)
  - Support total 4 PLLs(3 fracPLLs and 1 intPLL) to generate all clocks
  - One oscillator with 24MHz clock input
  - Support clock gating control for individual components
  - Support global soft-reset control for whole chip, also individual soft-reset for each component
- PMU (power management unit)
  - Multiple configurable work modes to save power by different frequency or automatic clock gating control or power domain on/off control
  - Lots of wake-up sources in different mode
  - Support 3 separate voltage domains, VDD\_ARM,VDD\_LOGIC,VDD\_PMU.
- Timer
  - Support 2 secure timers with 64bits counter and interrupt-based operation
  - Support 6 non-secure timers with 64bits counter and interrupt-based operation
  - Support 1 high precision timer which support auto synchronous function after

- exited from low power.
  - Support two operation modes: free-running and user-defined count for each timer
  - Support timer work state check-able
- PWM
  - Support 8 on-chip PWMs (PWM0~PWM7) with interrupt-based operation
  - For PWM0 to PWM3, following feature are supported
    - ◆ Support power key capture mode
    - ◆ Support generates waveform through lookup table
    - ◆ Support clock frequency meter
    - ◆ Support clock counter
    - ◆ Support IR transmission
  - For PWM4 to PWM7, following feature are supported
    - ◆ Support LEDC function
    - ◆ Support IR transmission
- Watchdog
  - 32-bit watchdog counter
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - ◆ Generate a system reset
    - ◆ First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
  - One Watchdog for non-secure application
  - One Watchdog for secure application
  - One Watchdog for MCU
- Interrupt Controller
  - Support 256 SPI interrupt sources input from different components inside RK3538
  - Support 16 software-triggered interrupts
  - Input interrupt level is fixed, high-level sensitive or rising edge sensitive
  - Support different interrupt priority for each interrupt source, and they are always software-programmable
- DMAC
  - Support 4 physical channels
  - Support 29 groups of peripheral request interfaces
  - Support 36 logic channels, each logic channel support the following feature
    - ◆ Support the data transfer of memory-to-memory, memory-to-peripherals, peripherals-to-memory
    - ◆ Support Linked list DMA function to complete scatter-gather transfer
    - ◆ Support three kinds of multi-block transfer: contiguous address, auto reload, link list
- Secure System
  - Support one crypto engine
    - ◆ system feature
      - Support DMA controller to transfer data between CE(Crypto Engine) and memory
      - Support 3 AHB slave interfaces KLCE(CE for keylad), SCE(CE for secure world) and NSCE(CE for non-secure world) each
      - SCE and NSCE has 2 channels for software request, KLCE has 1 channels for software request
      - Support 3 interrupt for KLCE, SCE and NSCE each
      - Symmetric, HASH ctrl logics are separate, which can handle task simultaneously
      - Supports task chain mode for each request. Task or task chain are executed

- at request order
  - 8 scatter group(sg) are supported for both input and output data in each TD
  - KLCE, SCE and NSCE issues task request through its own interface, do not know the existence of each other
- ◆ Symmetrical algorithms
  - Support lockstep error monitoring
  - Support anti side channel attack
  - Supports AES, DES, 3DES, SM4
  - Support AES-128, AES-192, AES-256
  - Support ECB/CBC/OFB/CFB/CTR/CTS/XTS/CCM/GCM/CBC-MAC/CMAC mode for AES and SM4
  - Support ECB/CBC/OFB/CFB mode for DES/TDES
- ◆ Hash algorithm
  - Support lockstep error monitoring
  - Support anti side channel attack
  - Support SHA-1, SHA-256/224, SHA-512/384, SHA-512, MD5, SM3 with hardware padding
  - Support HMAC of SHA-1, SHA-256, SHA-512, MD5, SM3 with hardware padding
- ◆ Asymmetrical algorithms
  - Support RSA, ECC, SM2
  - RSA512/1024/2048/3072/4096-bit
  - ECC192/224/256/384-bit
- ◆ support key-ladder(KL)
  - Supports obtaining the root key from OTP or RKRNG
  - Support writing out root key or derived key to some specific modules by using apb master
  - Number of stages can be configured
- Supports data scrambling for all DDR types
- Support security TRNG and non security TRNG
- Support random number attack detection
- Support secure OTP
- Support secure debug
- Support secure OS
- Except CPU/RKCE/RGA/RKVDEC/GPU, the other masters in the SoC can also support security and non-security mode by software-programmable
- Some slave components in SoC can only be addressed by security master and the other slave components can be addressed by security master or non-security master by software-programmable
- System SRAM space can be divided into 2 parts, each part can be software-programmable to be enabled by each master
- External DDR space can be divided into 32 parts, each part can be software-programmable to be enabled by each master
- Mailbox
  - One Mailbox in SoC to service CPU and MCU communication
  - Support four mailbox elements, each element includes one data word, one command word register and one flag bit that can represent one interrupt
  - Provide 32 lock registers for software to use to indicate whether mailbox is occupied

### 1.2.5 Video CODEC

- Video Decoder
  - MMU embedded with MMU interrupt support
  - Simultaneously decode two channel H.265 HEVC/MVC Main/Main still/Main10/Main10 still/RExt/MV-HEVC Profile yuv400/yuv420/yuv422/yuv444@L4.1 each up to 1920x1080@60fps

- Simultaneously decode two channel H.264 AVC/MVC baseline/Main/Main10/High/High10/High4:2:2/High4:4:4 Profile yuv400/yuv420/yuv422/yuv444@L4.2 each up to 1920x1080@60fps
- Simultaneously decode two channel VP9 Profile2 yuv420 each up to 1920x1080@60fps
- Simultaneously decode two channel AV1 Main/Main10 Profile yuv420@L4.1 up each to 1920x1080@60fps
- VP8 version2, up to 1920x1088@60fps
- VC1 Simple Profile@low, medium, high levels, Main Profile@low, medium, high levels, Advanced Profile@level0~3, up to 1920x1088@60fps
- MPEG-4 Simple Profile@L0~6, Advanced Simple Profile@L0~5, up to 1920x1088@60fps
- MPEG-2 Main Profile, low, medium and high levels, up to 1920x1088@60fps
- MPEG-1 Main Profile, low, medium and high levels, up to 1920x1088@60fps
- H.263 Profile0, levels 10-70, up to 720x576@60fps
- JPEG Baseline interleaved, up to 8176x8176@76 milion pixels per second

### 1.2.6 JPEG CODEC

- JPEG decoder
  - Supports Baseline (DCT sequential)
  - Supports JPEG file interchange format (JFIF) 1.02
  - Supports image size is from 48x48 to 65520x65520
  - Supports YUV400/YUV420/YUV422/YUV440/YUV411/YUV444
  - Supports low delay input and low delay output
  - Supports Tile/YUYV/RGB output
  - Supports Ultra-fast decoder
  - Supports enhance link mode

### 1.2.7 Image Enhancement (VDPP module)

- DEI(De-interlace)
  - **Image format**
    - ◆ Input data: YUV420/YUV422; Semi-planar/planar; UV swap
    - ◆ Output data: YUV420/YUV422; Semi-planar; UV swap;
    - ◆ Max resolution for dynamic image up to 1920x1080
  - **De-interlace mode**
    - ◆ **I5O2**: Input 5 Fields Output 2 frames mode
    - ◆ **I5O1T/I5O1B**: Input 5 Fields Output 1 Top/1 Bottom frame mode
    - ◆ **I2O2**: Input 2 Fields Output 2 frames mode
    - ◆ **I1O1T/I1O1B**: Input 1 Field Output 1 Top/1 Bottom frame mode
    - ◆ **PULLDOWN\_REC**: Pull-down Recovery mode
    - ◆ **DETECT\_ONLY**: Detect Only mode
  - **De-interlace function**
    - ◆ **FF/FO/PD DETECT**: Frame Field/Field Order/Pull Down Detection
    - ◆ **MV HIST**: Motion Vector Histogram
    - ◆ **MD/ME/MC**: Motion Detection/Estimate/Compensation
    - ◆ **EEDI**: Enhanced Edge based Interpolation
    - ◆ **OSD DETECT**: On-Screen Display Detection
    - ◆ **CC**: Combining Check
- VEP(Video Enhance Processor)
  - **Image format**
    - ◆ Input data: YUV420; Semi-planar; UV swap
    - ◆ Output data: YUV420/YUV444; Semi-planar; UV swap;
    - ◆ YUV support up sampling conversion from 420 to 444 by ZME module
    - ◆ Input and output max resolution for dynamic image up to 1920x1080
    - ◆ Y and UV component independent resolution output
  - **DMSR**
    - ◆ De-Mosquito noise, De-Ringing effect and De-Shooting effect
    - ◆ Only process the Y 8bit component

- **ES (Edge Smoothing)**
  - ◆ Only process the Y 8bit component
  - ◆ The maximum supported image width: 1280;
- **ZME (Zoom Manage Engine)**
  - ◆ Video resize based Multi-phase Algorithm
  - ◆ Horizontal arbitrary non-integer scaling ratio, from 1/7 to 8
  - ◆ Vertical arbitrary non-integer scaling ratio, from 1/6 to 6
  - ◆ Dering
- **SHARP**
  - ◆ Support maximum width: 1920
  - ◆ Input and output image data format: YUV 10bit
- **PYRAMID**
  - ◆ Downsampling processing yields small-sized images
  - ◆ Only process the Y 8bit component
- **BLCK**
  - ◆ Image black border detection
  - ◆ The maximum supported image size: 3840\*2160;

### 1.2.8 2D Graphics Engine(RGA)

2D Graphics Engine:

- **Data format**
  - SRC0 Input data format:
    - ◆ ARGB8888/RGBA8888/RGBA4444/RGBA5551
    - ◆ RGB888P/RGB565
    - ◆ YUV422-P/YUV422-SP-8bit/10bit
    - ◆ YUV420-P/YUV420-SP-8bit/10bit
    - ◆ YUV444I/YUV444SP-8bit
    - ◆ YVYU422-8bit
    - ◆ YUV400-8bit
    - ◆ AFBC32X8-8bit(split mode only) ARGB8888/RGB888P/YUV420/YUV422
    - ◆ AFBC32X8-10bit(split mode only) YUV422/YUV420
    - ◆ BPP1/2/4/8
  - SRC1 Input data format:
    - ◆ ARGB8888/RGBA8888/RGBA4444/RGBA5551/A8
    - ◆ RGB888P/RGB565
  - Output data format(all YUV format is 8bit):
    - ◆ ARGB8888/RGBA8888/ARGB4444/RGBA4444/ARGB5551/RGBA5551
    - ◆ RGB888/RGB565
    - ◆ YUV420/YUV422 P/SP
    - ◆ YUV400/Y4
    - ◆ YUV444SP/444I
    - ◆ AFBC32X8-8bit(split mode only) ARGB8888/RGB888P/YUV422/YUV420
    - ◆ AFBC32X8-10bit(split mode only) YUV422/YUV420/YUV444/RGBA1010102
  - Pixel Format conversion, BT.601/BT.709
  - Dither operation
  - Max resolution: 8192x8192 source, 4096x4096 destination
- **Scaling**
  - Down-scaling: Average/Bilinear filter
  - Up-scaling: Bi-cubic filter(source>1992 would use Bi-linear)
  - Arbitrary non-integer scaling ratio, from 1/16 to 16
- **Rotation**
  - 0, 90, 180, 270 degree rotation
  - x-mirror, y-mirror operation
  - Mirroring and rotation co-operation
- **BitBLT**
  - Block transfer
  - Color palette/Color fill, support with alpha

- Transparency mode (color keying/stencil test, specified value/value range)
- Two source BitBLT
- A+B=B only BitBLT, A support rotate & scale when B fixed
- A+B=C second source (B) has same attribute with (C) plus rotation function
- **Alpha Blending**
  - Comprehensive per-pixel alpha(color/alpha channel separately)
  - Fading
  - Support SRC1(R2Y)+SRC0(YUV) -> DST(YUV)
  - Support DST Full CSC convert for YUV2YUV
- **OSD Automatic Inversion**
  - Supports OSD sources in ARGB8888/ARGB1555/ARGB444/ARGB2BPP format
  - Support SRC0 and OSD overlay
- **Others**
  - Support MMU and MMU table pre-fetch

### 1.2.9 Video Output Processor

- Cluster 0
  - Resolution
    - ◆ Max resolution: 1920x1080
  - Data format
    - ◆ AFBCD: RGBA8888/RGB888/RGBA1010102/YUV422\_8bit (10bit) /YUV444\_8bit (10bit)
    - ◆ RFBCD: RGBA8888/RGB888/RGBA1010102/YUV422\_8bit (10bit) /YUV444\_8bit (10bit)
    - ◆ Raster: RGBA8888/RGB888/RGB565/RGB1010102/YUV444\_8bit (10bit) / YUV422\_8bit (10bit) /YUV400\_8bit (10bit)
  - Image
    - ◆ Support virtual width
    - ◆ Support active offset
    - ◆ Support display offset
    - ◆ Support Y/X mirror
      - AFBC/RFBC support X mirror and Y mirror
      - Raster and tile only support Y mirror
    - ◆ Swap: alpha/RB/UV/RG swap
    - ◆ Support YUV clip
  - Scale
    - ◆ Scale down
      - Support scale rate 1/4~1
      - Support Pre-scale: Avg2/4, Gt2/4
      - Scale mode: Best-neigh/Bilinear/Multi-phase filter
    - ◆ Scale up
      - Support scale rate 1~8
      - Y scale mode: Best-neigh/Bilinear/Multi-phase filter
      - X scale mode: Best-neigh/Bilinear/Multi-phase filter
  - CSC matrix
  - DCI
    - ◆ Only CLUSTER0\_WIN0 support
- ESMART 0/1/2
  - Horizontal scale up:
    - ◆ Output max resolution: 1920x1080
  - Horizontal scale down:
    - ◆ Input max resolution: 1920x1080
  - Data format
    - ◆ RGB: ARGB8888/RGB888/RGB565/RGBA1010102/RGBA5551
    - ◆ YUV: YUV422/YUV444/YUV400 8bit/10bit
    - ◆ YUYV: YUYV422/UYVY422
  - Image
    - ◆ Support virtual width

- ◆ Support active offset
- ◆ Support display offset
- ◆ Support Y-mirror
- ◆ Swap: alpha/RB/RG/UV swap
- ◆ Support YUV clip
- Multi-region
  - ◆ Only one region at one line
  - ◆ All regions are RGB or YUV format
  - ◆ Up to 4 regions
- CURSOR
  - Max resolution:256x256
  - Data format
    - ◆ RGB: ARGB8888/RGB888/RGB565/RGBA1010102/RGBA5551
  - Image
    - ◆ Support virtual width
    - ◆ Support active offset
    - ◆ Support display offset
    - ◆ Support Y-mirror
    - ◆ Swap: alpha/RB/RG/UV swap
  - CSC matrix

### 1.2.10 Display Interface

- Display Interface
  - Support HDMI 2.1 output up to 1080P 10bit @60Hz
  - TV interface: TV encoder 10bit out for DAC
  - Display output interface:
    - ◆ HDMI Interface
      - ❖ Max resolution support 1920x1080@yuv444-60Hz
      - ❖ Support RGB/YUV444/YUV422 (up to 10bit) format
    - ◆ CVBS : NTSC/PAL
- HDMI 2.1 Compliance
  - Support for 1080P@60 Hz video modes
  - Extended Metadata Packets such as HDR10+
  - SCDC I2C DDC access
  - TMDS Scrambler to enable support for 1080p@60fps with RGB/YCbCr 4:4:4/YCbCr 4:2:2
  - Character Error Detection
  - Multi-stream Audio Support (Multi-stream Audio Sample)
- HDCP 1.4 Compliance
  - According to HDMI 2.1 Specification, support for this HDCP encryption/decryption method is not available when operating in Fixed Rate Link mode
  - For HDMI 2.0 and lower version specifications, HDCP 1.4 content protection engine is available
- HDCP 2.3 Compliance
  - External HDCP 2 interface is provided, which allows connecting HDCP 2 Embedded Security Module IP that can be licensed separately

### 1.2.11 Audio Interface

- SAI(Serial Audio Interface):
  - SAI0/SAI2 with 2 channel
    - ◆ Up to 2 channels for TX and 2 channels RX path
    - ◆ Audio resolution from 16bits to 32bits
    - ◆ Sample rate up to 192KHz
    - ◆ Provides master and slave work mode, software configurable
    - ◆ Support 3 I2S formats (normal, left-justified, right-justified)
    - ◆ Support 4 PCM formats (early, late1, late2, late3)
    - ◆ SAI and PCM cannot be used at the same time
    - ◆ SAI0 connect to GPIO

- ◆ SAI2 connect to Audio CODEC, RX path not supported
- SAI1 with 8 channel
  - ◆ Up to 8 channels TX and 8 channels RX path
  - ◆ Audio resolution from 16bits to 32bits
  - ◆ Sample rate up to 192KHz
  - ◆ Provides master and slave work mode, software configurable
  - ◆ Support 3 I2S formats (normal, left-justified, right-justified)
  - ◆ SAI1 connect to GPIO
  - ◆ SAI3 connect to HDMI, RX path not supported
- PDM
  - Up to 8 channels
  - Audio resolution from 16bits to 24bits
  - Sample rate up to 192KHz
  - Support PDM master receive mode
- SPDIF
  - SPDIF\_TX connect to GPIO
- Audio CODEC
  - 24bit DAC
  - Support Line-out
  - Support Mono, Stereo channel performance
  - Integrated digital interpolation and decimation filter.
  - Sampling rate of 8kHz/12kHz/16kHz/24KHz/32kHz/44.1KHz/48KHz/96KHz

### 1.2.12 Connectivity

- SDIO interface
  - Compatible with SDIO 3.0 protocol
  - 4bits data bus widths
- SPI Controller
  - Support serial-master and serial-slave mode, software-configurable
  - DMA-based or interrupt-based operation
  - Embedded two 32x16bits FIFO for TX and RX operation respectively
  - Support 2 chip-selects output in serial-master mode
  - 2 on-chip SPI controller
- UART Controller
  - 6 on-chip UART controller
  - DMA-based or interrupt-based operation
  - UART0/1/2Embedded two 64Bytes FIFO for TX and RX operation respectively
  - Support 5bit,6bit,7bit,8bit serial data transmit or receive
  - Standard asynchronous communication bits such as start, stop and parity
  - Support different input clock for UART operation to get up to 4Mbps or another special baud rate
  - Support non-integer clock divides for baud clock generation
  - Support auto flow control mode
- I2C controller
  - 6 on-chip I2C controller
  - Multi-master I2C operation
  - Support 7bits and 10bits address mode
  - Software programmable clock frequency and transfer rate up to 400Kbit/s in the fast mode
  - Serial 8bits oriented and bidirectional data transfers can be made at up to 100Kbit/s in the standard mode

- MAC 10/100 Ethernet Controller
  - Support 10/100 Mbps data transfer rates with the RMI interfaces
  - Support both full-duplex and half-duplex operation
  - Supports IEEE 802.1Q VLAN tag detection for reception frames
  - Support detection of LAN wake-up frames and AMD Magic Packet frames
  - Support checking IPv4 header checksum and TCP, UDP, or ICMP checksum encapsulated in IPv4 or IPv6 datagram
  - Support for TCP Segmentation Offload (TSO) and UDP Fragmentation Offload (UFO)
- MAC 10/100M Ethernet controller and MAC PHY
  - Support one Ethernet controllers
  - Support 10/100-Mbps data transfer rates with the RMI interfaces
  - Support both full-duplex and half-duplex operation
- USB 2.0 DRD interface
  - Compatible Specification
    - ◆ Universal Serial Bus Specification, Revision 2.0
    - ◆ Extensible Host Controller Interface for Universal Serial Bus (xHCI), Revision 1.1
  - Support Control/Bulk/Interrupt/Isochronous Transfer
- USB 2.0 Host interface
  - Support one USB2.0 Host
  - Compatible with USB 2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Support Enhanced Host Controller Interface Specification (EHCI), Revision 1.0
  - Support Open Host Controller Interface Specification (OHCI), Revision 1.0a

### 1.2.13 Others

- Multiple group of GPIO
  - All of GPIOs can be used to generate interrupt to CPU
  - Support level trigger and edge trigger interrupt
  - Support configurable polarity of level trigger interrupt
  - Support configurable rising edge, falling edge and both edge trigger interrupt
- HDMI Special IO
  - 3.3V power supply, 5V voltage tolerance for HPD/IIC IOs
  - Special electronic characteristics for HDMI CEC/HPD/DDC IOs
- Temperature Sensor (TS-ADC)
  - Support User-Defined Mode and Automatic Mode
  - In User-Defined Mode, start\_of\_conversion can be controlled completely by software, and also can be generated by hardware.
  - In Automatic Mode, the temperature of alarm (high/low temperature) interrupt can be configurable
  - In Automatic Mode, the temperature of system reset can be configurable
  - Support 2 channel TS-ADC (used for CPU and NPU respectively)
  - -40~125°C temperature range and +/-5°C temperature accuracy
- Successive approximation ADC (SARADC)
  - 13-bit resolution
  - Up to 2MS/s sampling rate
  - Total 24 single-ended input channels
  - Support single mode and series conversion mode
- OTP
  - Support 8K bits size, 7K bits for secure application

- Support Program/Read/Idle mode
- Package Type
  - FBGA434L (body:13.3mm x 13.5mm ;ball size: 0.3mm ;ball pitch: 0.65/0.6mm)

Notes :

① DDR3/DDR3L/DDR4/LPDDR3/LPDDR4/LPDDR4X are not used simultaneously

② Support 1x USB2 Host+1x USB2 DRD

### 1.3 Block Diagram

The following diagram shows the basic block diagram.

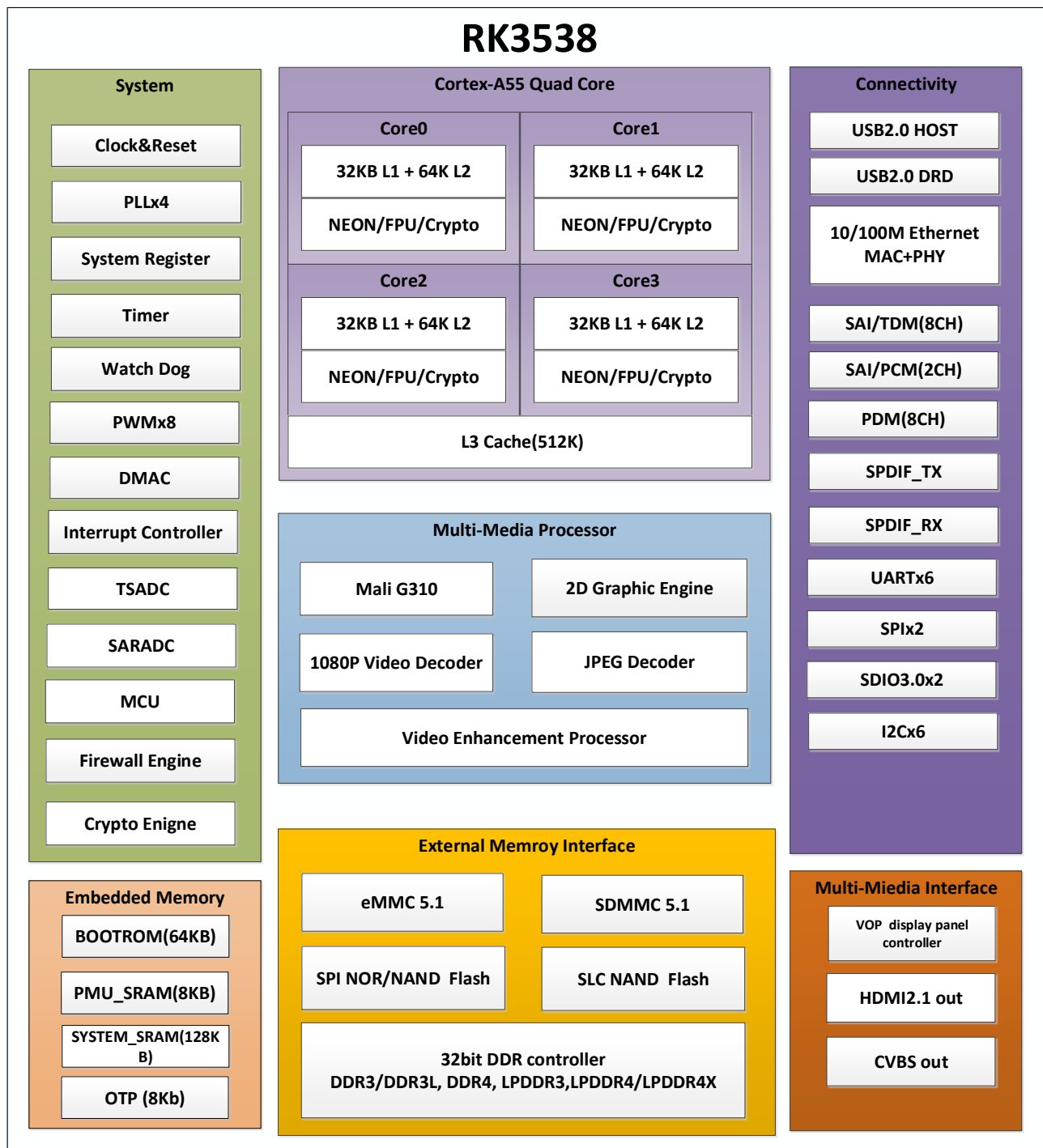


Fig.1-1 Block Diagram

## Chapter 2 Package Information

### 2.1 Order Information

Orderable Device	RoHS status	Package	Package Q'ty	Device Feature
RK3538	RoHS	WB(TFBGA)	119/ tray 1190/ inner box 7140/ box	Quad-core Application Processor

### 2.2 Top Marking

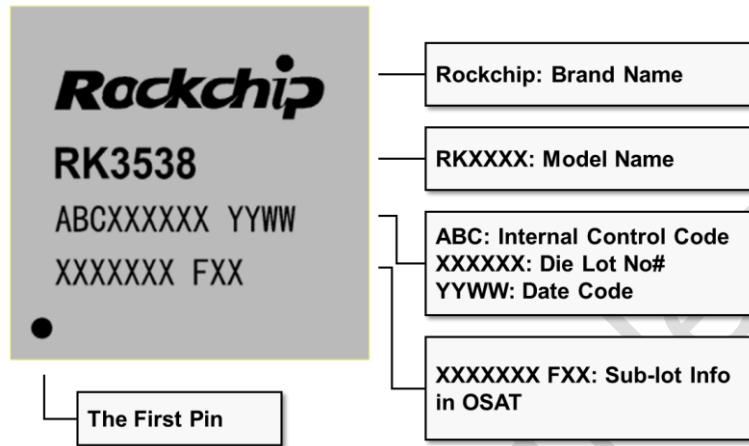


Fig.2-1 Package Definition

### 2.3 Package Dimension

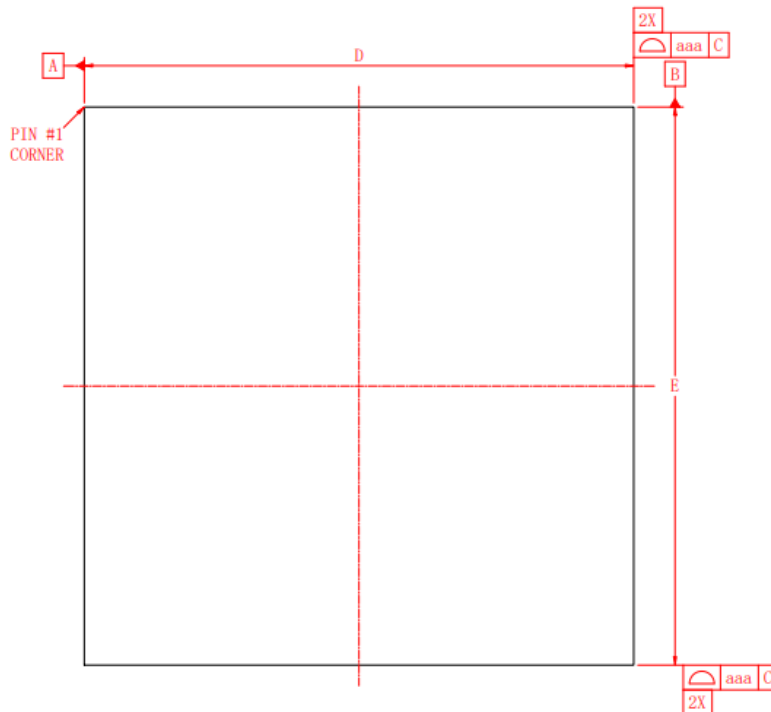


Fig.2-2 Package Top View

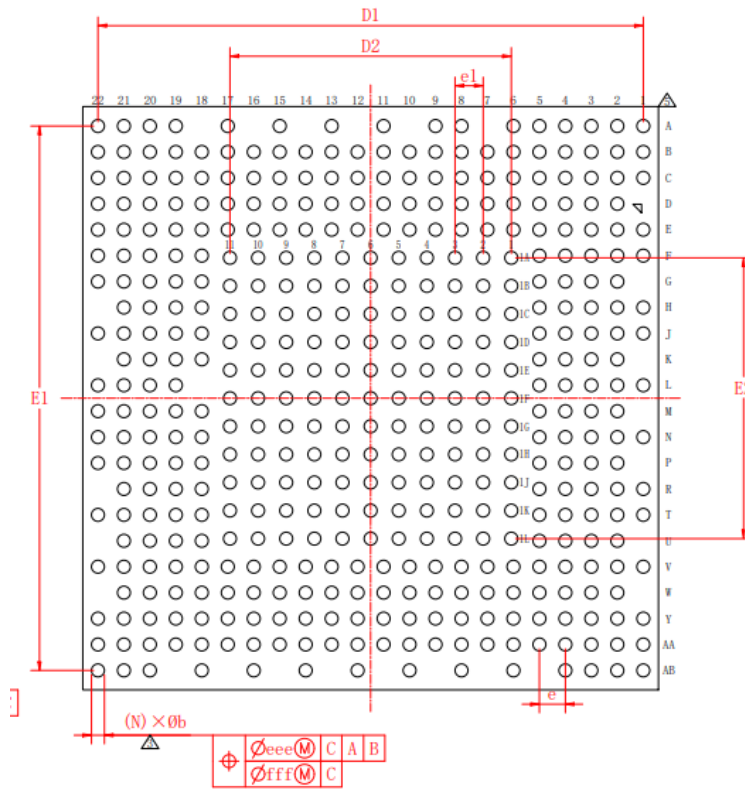


Fig.2-3 Package Bottom View

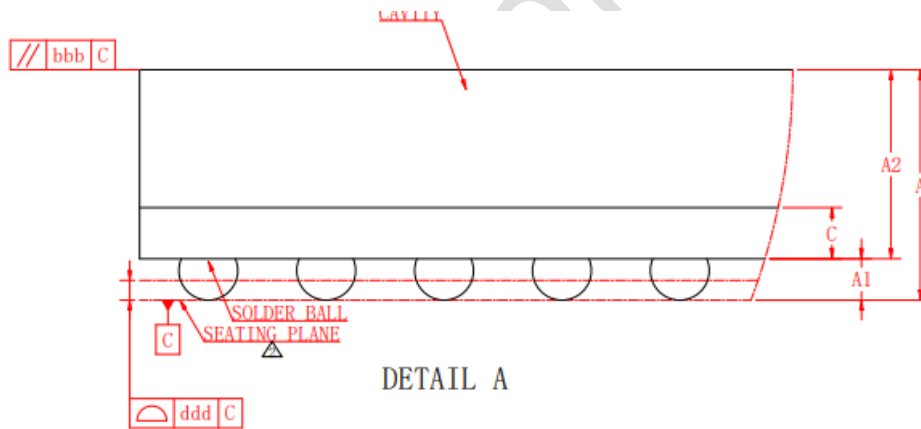


Fig.2-4 Package Side View

symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.090	1.170	1.250	0.043	0.046	0.049
A1	0.160	0.210	0.260	0.006	0.008	0.010
A2	0.910	0.960	1.010	0.036	0.038	0.040
c	0.230	0.260	0.290	0.009	0.010	0.011
D	13.200	13.300	13.400	0.520	0.524	0.528
E	13.400	13.500	13.600	0.528	0.531	0.535
D1	---	12.600	---	---	0.496	---
E1	---	12.600	---	---	0.496	---
D2	---	6.500	---	---	0.256	---
E2	---	6.500	---	---	0.256	---
e	---	0.600	---	---	0.024	---
e1	---	0.650	---	---	0.026	---
b	0.250	0.300	0.350	0.010	0.012	0.014
aaa	0.100			0.004		
bbb	0.100			0.004		
ddd	0.080			0.003		
eee	0.150			0.006		
fff	0.050			0.002		
Ball Diam	0.300			0.012		
N	434			434		
MD/ME	22/22			22/22		

Fig.2-5 Package Dimension

## 2.4 MSL Information

Moisture sensitivity Level : MSL3

## 2.5 Lead Finish/Ball material Information

Lead Finish/Ball material : SnAgCu

## 2.6 Pin Number List

Table 2-1 Pin Number Order Information

Pin name	Pin#	Pin name	Pin#
DDR_PLL_AVDD1V8	1A1	DDRPHY_A_DM1/DDR4_DMU_A/LPDDR4_DM1_A/DDR3_DM1/LPDDR3_DM2	D2
VSS	1A2	VSS	D3
DDR_VDDQ	1A3	DDRPHY_A_DQ11/DDR4_DQU2_A/LPDDR4_DQ11_A/DDR3_D9/LPDDR3_D17	D4

Pin name	Pin#	Pin name	Pin#
DDR_VDDQ	1A4	DDRPHY_A_DQ10/DDR4_DQU0_A/LPDDR4_DQ10_A/DDR3_D15/LPDDR3_D21	D5
DDR_VDDQ	1A5	DDRPHY_A_DQ14/DDR4_DQU4_A/LPDDR4_DQ14_A/DDR3_D13/LPDDR3_D22	D6
VSS	1A6	VSS	D7
VSS	1A7	DDRPHY_A_DQ4/DDR4_DQL4_A/LPDDR4_DQ4_A/DDR3_D6/LPDDR3_D4	D8
VCCIO1_VCC	1A8	DDRPHY_A_DQ7/DDR4_DQL3_A/LPDDR4_DQ7_A/DDR3_D3/LPDDR3_D7	D9
VCCIO2_VCC	1A9	DDRPHY_B_DQ0/DDR4_DQU4_B/LPDDR4_DQ0_B/DDR3_D29/LPDDR3_D14	D10
VSS	1A10	DDRPHY_B_DQ7/DDR4_DQU2_B/LPDDR4_DQ7_B/DDR3_D25/LPDDR3_D11	D11
VSS	1A11	DDRPHY_B_DM1/DDR4_DML_B/LPDDR4_DM1_B/DDR3_DM2/LPDDR3_DM3	D12
VSS	1B1	DDRPHY_B_DQ15/DDR4_DQL5_B/LPDDR4_DQ15_B/DDR3_D23/LPDDR3_D29	D13
DDR_VDDQ	1B2	DDRPHY_B_DQ9/DDR4_DQL3_B/LPDDR4_DQ9_B/DDR3_D19/LPDDR3_D26	D14
DDR_VDDQL	1B3	EMMC_STRB/FLASH_CLE/FSPI_RSTN/GPIO1_B2_D	D15
DDR_VDDQL	1B4	VSS	D16
DDR_VDDQL	1B5	EMMC_CLK/FSPI_DQS/I2C5_SCL_M1/GPIO1_B1_D	D17
DDR_VDDQL	1B6	FLASH_CSN0/FSPI_CSN0/GPIO1_B7_U	D18
VSS	1B7	FLASH_RDN/FSPI_D1/GPIO1_B6_U	D19
VSS	1B8	VSS	D20
USB20_DVDD0V9	1B9	USB0_DRD_DP	D21
USB20_AVDD3V3	1B10	USB0_DRD_DM	D22
USB20_AVDD1V8	1B11	DDRPHY_A_DQ12/DDR4_DQU7_A/LPDDR4_DQ12_A/DDR3_D10/LPDDR3_D20	E1
DDR_VDDQ	1C1	DDRPHY_A_DQ9/DDR4_DQU5_A/LPDDR4_DQ9_A/DDR3_D14/LPDDR3_D16	E2
DDR_VDDQL	1C2	DDRPHY_A_DQ8/DDR4_DQU1_A/LPDDR4_DQ8_A/DDR3_D12/LPDDR3_D19	E3
VSS	1C3	VSS	E4
VSS	1C4	DDR_RZQ	E5

Pin name	Pin#	Pin name	Pin#
VSS	1C5	VSS	E6
VSS	1C6	VSS	E7
VSS	1C7	DDRPHY_A_DQ5/DDR4_DQL5_A/LPDDR4_DQ5_A/DDR3_D7/LPDDR3_D5	E8
VSS	1C8	VSS	E9
FEPHY_AVDD0V9	1C9	VSS	E10
FEPHY_AVDD3V3	1C10	VSS	E11
FEPHY_AVDD1V8	1C11	VSS	E12
DDR_VDDQ	1D1	DDRPHY_B_DQ14/DDR4_DQL7_B/LPDDR4_DQ14_B/DDR3_D21/LPDDR3_D25	E13
DDR_VDDQL	1D2	VSS	E14
VSS	1D3	EMMC_CMD/FLASH_WRN/FSPI_CS1/GPIO1_B0_U	E15
LOGIC_DVDD	1D4	VSS	E16
VSS	1D5	EMMC_RSTN/FLASH_WPN/FSPI_D0/GPIO1_B3_D	E17
LOGIC_DVDD	1D6	FLASH_CS1/FSPI_D3/I2C5_SDA_M1/GPIO1_C0_U	E18
VSS	1D7	VSS	E19
FEPHY_REXT	1D8	SDMMC0_CLK/TEST_CLK_OUT_M1/FEPHY_LED_SPD_M1/GPIO2_A5_D	E20
VSSA	1D9	FEPHY_RXP	E21
VSSA	1D10	FEPHY_RXN	E22
VSSA	1D11	DDRPHY_ODT1/DDR4_ODT1/LPDDR4_ODT0_A/DDR3_ODT1/LPDDR3_ODT1	F1
DDR_VDDQ	1E1	DDRPHY_A5/DDR4_A5/LPDDR4_A1_A/DDR3_A4	F2
DDR_VDDQL	1E2	DDRPHY_A7/DDR4_A7/LPDDR4_A4_A/DDR3_A6	F3
VSS	1E3	DDRPHY_A16/DDR4_RASN/A16/LPDDR4_A0_A/DDR3_CKE0	F4
LOGIC_DVDD	1E4	VSS	F5
VSS	1E5	VSS	F18
VSS	1E6	SDMMC0_DET_N/GPIO2_A6_U	F19
LOGIC_DVDD	1E7	VSSA	F20
RFU3	1E8	FEPHY_TXP	F21
HDMI_REXT	1E9	FEPHY_TXN	F22
HDMI_TX_DVDD0V9	1E10	DDRPHY_A15/DDR4_CASN/A15/LPDDR4_A3_A/DDR3_BA1/LPDDR3_A0	G2

Pin name	Pin#	Pin name	Pin#
HDMI_TX_AVDD1V8	1E1 1	VSS	G3
VSS	1F1	DDRRPHY_CSN1/DDR4_CSN1/L PDDR4_CSN0_A/DDR3_CSN1/ LPDDR3_CSN0	G4
DDRRPHY_VREFOUT	1F2	DDRRPHY_BG1/DDR4_BG1/DDR 3_A15	G5
VSS	1F3	VSS	G18
LOGIC_DVDD	1F4	USB0_DRD_VBUSDET	G19
LOGIC_DVDD	1F5	VSSA	G20
VSS	1F6	HDMI_TX_D2P	G21
LOGIC_DVDD	1F7	VSSA	G22
VSS	1F8	DDRRPHY_A9/DDR4_A9/LPDDR 4_CLKP_A/DDR3_A11/LPDDR3 _A2	H1
ACODEC_VSSA	1F9	DDRRPHY_A13/DDR4_A13/LPD DR4_CLKN_A/DDR3_A8/LPDD R3_A3	H2
OTP_VCC1V8	1F1 0	VSS	H3
ACODEC_AVDD1V8	1F1 1	DDRRPHY_A12/DDR4_A12/LPD DR4_A2_A/DDR3_A10/LPDDR 3_A4	H4
VSS	1G1	VSS	H5
VCCIO6_VCC	1G2	VSSA	H18
CPU_DVDD	1G3	USB0_DRD_ID	H19
VSS	1G4	VSSA	H20
VSS	1G5	HDMI_TX_D2N	H21
VSS	1G6	DDRRPHY_CLKP/DDR4_CLKP/LP DDR4_CLKP_B/DDR3_CLKP/LP DDR3_CLKP	J1
VSS	1G7	DDRRPHY_CLKN/DDR4_CLKN/L PDDR4_CLKN_B/DDR3_CLKN/ LPDDR3_CLKN	J2
VSS	1G8	DDRRPHY_BA1/DDR4_BA1/LPD DR4_A5_A/DDR3_A12/LPDDR 3_A1	J3
VDAC_IREF	1G9	DDRRPHY_CSN0/DDR4_CSN0/L PDDR4_CSN1_A/DDR3_CASN/ LPDDR3_CSN1	J4
VDAC_AVDD1V8	1G1 0	VSS	J5
VDAC_VSSA	1G1 1	VSSA	J18
VSS	1H1	VSSA	J19
VSS	1H2	VSSA	J20
CPU_DVDD	1H3	HDMI_TX_D1P	J21

Pin name	Pin#	Pin name	Pin#
VSS	1H4	HDMI_TX_D1N	J22
VSS	1H5	DDRPHY_A2/DDR4_A2/LPDDR4_ODT0_B/DDR3_A13/LPDDR3_ODT3	K2
LOGIC_DVDD	1H6	VSS	K3
VSS	1H7	DDRPHY_A0/DDR4_A0/LPDDR4_ODT1_B/DDR3_A9/LPDDR3_ODT2	K4
VSS	1H8	VSS	K5
PLL_VSSA	1H9	VSSA	K18
PLL_AVDD1V8	1H10	RFU1	K19
VSS	1H11	RFU2	K20
CPU_DVDD	1J1	HDMI_TX_D0P	K21
CPU_DVDD	1J2	DDRPHY_A1/DDR4_A1/LPDDR4_CKE1_A/DDR3_A14	L1
CPU_DVDD	1J3	DDRPHY_A3/DDR4_A3/LPDDR4_CKE0_A/DDR3_A1	L2
VSS	1J4	DDRPHY_ODT0/DDR4_ODT0/LPDDR4_ODT1_A/DDR3_WEN/LPDDR3_ODT0	L3
LOGIC_DVDD	1J5	DDRPHY_A6/DDR4_A6/LPDDR4_CSN1_B/DDR3_A3/LPDDR3_CSN2	L4
VSS	1J6	VSS	L5
LOGIC_DVDD	1J7	VSSA	L19
VSS	1J8	VSSA	L20
PLL_AVDD0V9	1J9	HDMI_TX_D0N	L21
PMUIO0_VCC3V3	1J10	VSSA	L22
VSS	1J11	DDRPHY_A10/DDR4_A10/LPDDR4_A1_B/DDR3_A0	M2
CPU_DVDD	1K1	DDRPHY_BA0/DDR4_BA0/LPDDR4_CKE0_B/DDR3_BA2/LPDDR3_CKE0	M3
CPU_DVDD	1K2	DDRPHY_A11/DDR4_A11/LPDDR4_A5_B/DDR3_A7/LPDDR3_A7	M4
CPU_DVDD	1K3	VSS	M5
CPU_DVDD	1K4	ACODEC_VCM	M18
LOGIC_DVDD	1K5	ACODEC_VSSA	M19
VSS	1K6	VSSA	M20
VSS	1K7	HDMI_TX_CLKP	M21
LOGIC_DVDD	1K8	HDMI_TX_CLKN	M22
VSS	1K9	DDRPHY_A4/DDR4_A4/LPDDR4_A0_B/DDR3_A2/LPDDR3_A5	N1
VSS	1K10	DDRPHY_CKE/DDR4_CKE/LPDDR4_CKE1_B/DDR3_RASN	N2

Pin name	Pin#	Pin name	Pin#
VSS	1K1 1	VSS	N3
VSS	1L1	DDRPHY_A14/DDR4_WEN/A14 /LPDDR4_CSN0_B/DDR3_ODT 0/LPDDR3_CSN3	N4
VCCIO3_VCC	1L2	VSS	N5
VSS	1L3	VDAC_VSSA	N18
VSS	1L4	VDAC_VSSA	N19
VSS	1L5	VSS	N20
VCCIO4_VCC	1L6	VSSA	N21
VSS	1L7	ACODEC_LINEOUT_L	N22
SARADC_AVDD1V8	1L8	DDRPHY_A8/DDR4_A8/LPDDR 4_A4_B/DDR3_A5/LPDDR3_A6	P2
VSS	1L9	DDRPHY_BG0/DDR4_BG0/LPD DR4_A3_B/DDR3_BA0/LPDDR 3_A8	P3
PMUIO1_VCC	1L1 0	VSS	P4
PMU_LOGIC_DVDD	1L1 1	VSS	P5
VSS	A1	HDMI_TX_SDA_5V/I2C2_SDA_ M1/GPIO0_B1_Z	P18
DDRPHY_A_DM0/DDR4_DML_A/LPDDR 4_DM0_A/DDR3_DM0/LPDDR3_DM0	A2	HDMI_TX_SCL_5V/I2C2_SCL_ M1/GPIO0_B0_Z	P19
DDRPHY_A_DQ1/DDR4_DQL2_A/LPDDR 4_DQ1_A/DDR3_D0/LPDDR3_D1	A3	VSS	P20
DDRPHY_A_DQS0P/DDR4_DQSL_P_A/L PDDR4_DQS0P_A/DDR3_DQS0P/LPDDR 3_DQS0P	A4	VDAC_IOUTN	P21
VSS	A5	ACODEC_LINEOUT_R	P22
DDRPHY_A_DQ6/DDR4_DQL7_A/LPDDR 4_DQ6_A/DDR3_D5/LPDDR3_D6	A6	DDRPHY_RESETN/DDR4_RESE TN/LPDDR4_RESETN/DDR3_R ESETN	R1
VSS	A8	DDRPHY_ACTN/DDR4_ACTN/L PDDR4_A2_B/DDR3_CSN0/LP DDR3_A9	R2
DDRPHY_B_DQS0N/DDR4_DQSU_N_B/ LPDDR4_DQS0N_B/DDR3_DQS3N/LPD DR3_DQS1N	A9	VSS	R3
DDRPHY_B_DQ6/DDR4_DQU6_B/LPDD R4_DQ6_B/DDR3_D27/LPDDR3_D10	A11	I2C2_SDA_M2/GPIO6_C3_D	R4
DDRPHY_B_DQS1N/DDR4_DQSL_N_B/L PDDR4_DQS1N_B/DDR3_DQS2N/LPDD R3_DQS3N	A13	VSS	R5
DDRPHY_B_DQ11/DDR4_DQL6_B/LPDD R4_DQ11_B/DDR3_D22/LPDDR3_D31	A15	PMU_LDO_3V3_IN	R18
EMMC_D1/FLASH_D3/UART4_CTSN_M1 /GPIO1_A1_U	A17	HDMI_TX_CEC_3V3/GPIO0_A7 _U	R19
FLASH_ALE/FSPI_CLK/GPIO1_B4_D	A19	VSS	R20
SDMMC0_D2/JTAG_CPU_TCK_M0/UART 4_RTSN_M0/JTAG_MCU_TCK_M0/JTAG _GPU_TCK_M0/GPIO2_A2_D	A20	VDAC_IOUTP	R21

Pin name	Pin#	Pin name	Pin#
SDMMC0_CMD/FEPHY_LED_LINK_M1/GPIO2_A4_D	A21	SPDIF_TX_M0/UART1_CTSN_M1/GPIO6_A0_D	T1
VSS	A22	VSS	T2
PWM1_CH0_M1/PDM_SDI2_M0/GPIO6_A6_D	AA1	I2C1_SDA_M0/FEPHY_LED_SPD_M0/GPIO6_B1_D	T3
PWM1_CH1_M1/PDM_CLK0_M0/GPIO6_A5_D	AA2	SAI1_MCLK_M0/PWM1_CH0_M0/SPI0_CSN1_M0/GPIO6_C1_D	T4
ETH1_PPSCCLK/PWM1_CH2_M1/PDM_SDI1_M0/GPIO6_A4_D	AA3	VSS	T5
SAI0_LRCK_M0/GPIO3_B5_D	AA4	HDMI_TX_HPD_5V/GPIO0_A6_Z	T18
UART2_CTSN_M0/GPIO3_B2_D	AA5	I2C0_SDA_M0/PWM0_CH3_M0/GPIO0_B6_D	T19
SDIO_PWREN/I2C3_SDA_M0/GPIO3_C3_D	AA6	VSS	T20
SDIO_D1/GPIO3_A1_D	AA7	OSC_SOC_XOUT	T21
SDIO_D3/GPIO3_A3_D	AA8	OSC_SOC_XIN	T22
SDIO_CMD/GPIO3_A4_D	AA9	SAI1_SDI2_M0/I2C1_SCL_M0/FEPHY_LED_LINK_M0/GPIO6_B2_D	U2
SAI0_LRCK_M1/PDM_SDI2_M1/GPIO5_C1_D	AA10	SDMMC0_PWREN/UART1_RTSN_M1/PDM_SDI0_M0/GPIO6_A1_D	U3
UART2_RTSN_M1/SAI1_SDO0_M1/GPIO5_B1_D	AA11	VSS	U4
SAI0_SDO_M1/PDM_CLK1_M1/UART3_TX_M1/I2C1_SCL_M1/GPIO5_B7_D	AA12	SAI1_SCLK_M0/GPIO6_B7_D	U5
UART2_TX_M1/SAI1_LRCK_M1/GPIO5_B0_D	AA13	VSS	U18
SPI0_MISO_M1/SAI2_LRCK_M1/GPIO5_A2_D	AA14	I2C0_SCL_M0/PWM0_CH2_M0/ARM_AVS/GPIO0_B5_D	U19
SAI1_SDO1_M1/SAI1_SDI3_M1/GPIO5_B5_D	AA15	TSADC_SHUT/TSADC_SHUTORG/GPIO0_A0_Z	U20
SDMMC1_D1/SAI2_SCLK_M0/SPI1_CLK_M0/GPIO4_A1_D	AA16	NPOR_DET	U21
SDMMC1_CMD/SAI2_SDO_M0/SPI1_CS_N1_M0/GPIO4_A4_D	AA17	SAI1_SDO2_M0/PWM1_CH3_M0/SPI0_MOSI_M0/GPIO6_C4_D	V1
SARADC_IN0	AA18	I2C2_SCL_M2/GPIO6_C2_D	V2
SARADC_IN2	AA19	SAI1_SDO3_M0/PWM1_CH2_M0/GPIO6_C6_D	V3
UART3_RX_M2/I2C5_SDA_M2/GPIO0_D1_D	AA20	SAI1_LRCK_M0/GPIO6_C0_D	V4
GPIO0_D5_D	AA21	VSS	V5
CLK_32K_OUT_M2/CLK_32K_IN/GPIO0_D4_D	AA22	VSS	V6
VSS	AB1	SPDIF_TX_M1/CLK_32K_OUT_M0/I2C3_SCL_M0/GPIO3_C2_D	V7

Pin name	Pin#	Pin name	Pin#
ETH1_PTP_REFCLK/PWM1_CH3_M1/PDM_SDI3_M0/I2C3_SCL_M2/GPIO6_B0_D	AB2	I2C4_SCL_M0/GPIO3_C0_D	V8
SAI0_MCLK_M0/I2C2_SCL_M0/GPIO3_B3_D	AB3	VSS	V9
SAI0_SDO_M0/GPIO3_B7_D	AB4	VCCIO5_VCC	V10
UART2_RX_M0/GPIO3_A7_D	AB6	VSS	V11
SDIO_D2/GPIO3_A2_D	AB8	VSS	V12
REF_CLK_OUT_M1/SPDIF_TX_M2/SPI1_MISO_M1/CLK_32K_OUT_M1/UART5_RX_M1/I2C3_SDA_M1/UART1_CTSN_M2/GPIO5_C2_D	AB10	SAI1_SDO2_M1/SAI1_SDI2_M1/PDM_SDI3_M1/UART1_RX_M2/GPIO5_B4_D	V13
SAI2_MCLK_M1/UART5_TX_M0/GPIO5_A0_D	AB12	VSS	V14
SPI0_CSN0_M1/GPIO5_A3_D	AB14	SAI0_SCLK_M1/SPI1_MOSI_M1/PDM_SDI0_M1/UART5_TX_M1/I2C3_SCL_M1/UART1_RTSN_M2/GPIO5_C0_D	V15
SDMMC1_DET_N/I2C1_SDA_M2/GPIO4_A6_U	AB16	VSS	V16
SDMMC1_D2/SAI2_LRCK_M0/GPIO4_A2_D	AB18	VSS	V17
I2C0_SDA_M1/UART3_RTSN/GPIO0_D3_D	AB20	PWM0_CH2_M1/GPIO0_B3_D	V18
UART3_TX_M2/I2C5_SCL_M2/GPIO0_D0_D	AB21	REF_CLK_OUT_M0/TEST_CLK_OUT_M0/AUPLL_CLK_IN/GPIO0_A1_D	V19
VSS	AB22	PWR_CTRL1/PWM0_CH0_M1/GPIO0_A3_U	V20
VSS	B1	PWM0_CH1_M1/GPIO0_B2_D	V21
DDRPHY_A_DQ15/DDR4_DQU6_A/LPDDR4_DQ15_A/DDR3_D11/LPDDR3_D18	B2	PWR_CTRL0/PWM0_CH0_M0/GPIO0_A2_D	V22
DDRPHY_A_DQ0/DDR4_DQL6_A/LPDDR4_DQ0_A/DDR3_D4/LPDDR3_D0	B3	SAI1_SDI3_M0/PWM1_CH1_M0/SPI0_MISO_M0/GPIO6_C5_D	W2
DDRPHY_A_DQS0N/DDR4_DQSL_N_A/LPDDR4_DQS0N_A/DDR3_DQS0N/LPDDR3_DQS0N	B4	SAI1_SDO0_M0/UART1_CTSN_M0/UART3_RX_M0/GPIO6_B3_D	W3
DDRPHY_A_DQ3/DDR4_DQL1_A/LPDDR4_DQ3_A/DDR3_D1/LPDDR3_D3	B5	UART1_RX_M1/SPI0_CLK_M0/GPIO6_A3_D	W4
VSS	B6	PDM_CLK1_M0/I2C3_SDA_M2/GPIO6_A7_D	W5
DDRPHY_B_DQ4/DDR4_DQU7_B/LPDDR4_DQ4_B/DDR3_D26/LPDDR3_D9	B7	UART2_RTSN_M0/GPIO3_B1_D	W6
DDRPHY_B_DQ2/DDR4_DQU1_B/LPDDR4_DQ2_B/DDR3_D28/LPDDR3_D13	B8	SAI0_SCLK_M0/GPIO3_B4_D	W7
DDRPHY_B_DQS0P/DDR4_DQSU_P_B/LPDDR4_DQS0P_B/DDR3_DQS3P/LPDDR3_DQS1P	B9	I2C4_SDA_M0/GPIO3_C1_D	W8
DDRPHY_B_DQ1/DDR4_DQU0_B/LPDDR4_DQ1_B/DDR3_D31/LPDDR3_D12	B10	SDIO_DET_N/I2C2_SDA_M0/GPIO3_A6_D	W9

Pin name	Pin#	Pin name	Pin#
VSS	B11	SPI1_CSN0_M1/SAI1_MCLK_M1/PDM_CLK0_M1/UART5_CTS_N/UART1_TX_M2/GPIO5_A6_D	W10
DDRRPHY_B_DQ13/DDR4_DQL2_B/LPDDR4_DQ13_B/DDR3_D20/LPDDR3_D24	B12	SAI1_SDO3_M1/SAI1_SDI1_M1/GPIO5_B3_D	W11
DDRRPHY_B_DQS1P/DDR4_DQSL_P_B/LPDDR4_DQS1P_B/DDR3_DQS2P/LPDDR3_DQS3P	B13	SPI0_CLK_M1/SAI2_SDO_M1/I2C5_SCL_M0/GPIO5_A4_D	W12
DDRRPHY_B_DQ8/DDR4_DQL1_B/LPDDR4_DQ8_B/DDR3_D17/LPDDR3_D27	B14	SPI0_MOSI_M1/I2C5_SDA_M0/GPIO5_A5_D	W13
DDRRPHY_B_DQ10/DDR4_DQL4_B/LPDDR4_DQ10_B/DDR3_D18/LPDDR3_D30	B15	VSS	W14
EMMC_D6/FLASH_D0/FSPI_D7/GPIO1_A6_U	B16	SAI0_MCLK_M1/SPI1_CLK_M1/PDM_SDI1_M1/UART5_RTSN/SDMMC1_PWREN/GPIO5_C3_D	W15
EMMC_D2/FLASH_D2/UART4_RX_M1/GPIO1_A2_U	B17	SDMMC1_CLK/I2C1_SCL_M2/GPIO4_A5_D	W16
EMMC_D4/FLASH_D5/FSPI_D5/I2C4_SCL_M2/GPIO1_A4_U	B18	SDMMC1_D3/SPI1_MISO_M0/GPIO4_A3_D	W17
EMMC_D5/FLASH_D7/FSPI_D4/I2C4_SDA_M2/GPIO1_A5_U	B19	PWM0_CH1_M0/GPIO0_A5_D	W18
SDMMC0_D3/JTAG_CPU_TMS_M0/UART4_CTSN_M0/JTAG_MCU_TMS_M0/JTAG_GPU_TMS_M0/GPIO2_A3_D	B20	VSS	W19
SDMMC0_D1/UART0_TX_M1/UART4_TX_M0/I2C4_SCL_M1/GPIO2_A1_D	B21	PWR_CTRL2_5V/GPIO0_A4_Z	W20
VSS	B22	PWM0_CH3_M1/GPU_AVS/GPIO0_B4_D	W21
DDRRPHY_A_DQS1P/DDR4_DQSU_P_A/LPDDR4_DQS1P_A/DDR3_DQS1P/LPDDR3_DQS2P	C1	SAI1_SDI0_M0/UART1_RX_M0/GPIO6_B6_D	Y1
DDRRPHY_A_DQS1N/DDR4_DQSU_N_A/LPDDR4_DQS1N_A/DDR3_DQS1N/LPDDR3_DQS2N	C2	SAI1_SDO1_M0/UART1_TX_M0/GPIO6_B5_D	Y2
DDRRPHY_A_DQ13/DDR4_DQU3_A/LPDDR4_DQ13_A/DDR3_D8/LPDDR3_D23	C3	SAI1_SDI1_M0/UART1_RTSN_M0/UART3_TX_M0/GPIO6_B4_D	Y3
VSS	C4	ETH1_PPSTRIG/UART1_TX_M1/SPI0_CSN0_M0/GPIO6_A2_D	Y4
VSS	C5	SAI0_SDI_M0/GPIO3_B6_D	Y5
DDRRPHY_A_DQ2/DDR4_DQL0_A/LPDDR4_DQ2_A/DDR3_D2/LPDDR3_D2	C6	UART2_TX_M0/GPIO3_B0_D	Y6
VSS	C7	VSS	Y7
DDRRPHY_B_DQ3/DDR4_DQU5_B/LPDDR4_DQ3_B/DDR3_D30/LPDDR3_D8	C8	SDIO_D0/GPIO3_A0_D	Y8
VSS	C9	SDIO_CLK/GPIO3_A5_D	Y9
VSS	C10	VSS	Y10
DDRRPHY_B_DM0/DDR4_DMU_B/LPDDR4_DM0_B/DDR3_DM3/LPDDR3_DM1	C11	UART2_CTSN_M1/SAI1_SDI0_M1/GPIO5_B2_D	Y11
DDRRPHY_B_DQ5/DDR4_DQU3_B/LPDDR4_DQ5_B/DDR3_D24/LPDDR3_D15	C12	SPI0_CSN1_M1/SAI2_SCLK_M1/UART5_RX_M0/GPIO5_A1_D	Y12
VSS	C13	VSS	Y13

Pin name	Pin#	Pin name	Pin#
DDRPHY_B_DQ12/DDR4_DQLO_B/LPDDR4_DQ12_B/DDR3_D16/LPDDR3_D28	C14	UART2_RX_M1/SAI1_SCLK_M1/SPI1_CSN1_M1/GPIO5_A7_D	Y14
VSS	C15	SAI0_SDI_M1/UART3_RX_M1/I2C1_SDA_M1/GPIO5_B6_D	Y15
EMMC_D7/FLASH_D1/FSPI_D6/GPIO1_A7_U	C16	VSS	Y16
EMMC_D0/FLASH_D4/UART4_RTSN_M1/GPIO1_A0_U	C17	SDMMC1_D0/SAI2_MCLK_M0/SPI1_CSN0_M0/GPIO4_A0_D	Y17
EMMC_D3/FLASH_D6/UART4_TX_M1/GPIO1_A3_U	C18	SARADC_IN1	Y18
FLASH_RDY/FSPI_D2/GPIO1_B5_U	C19	SARADC_IN3	Y19
SDMMC0_D0/UART0_RX_M1/UART4_RX_M0/I2C4_SDA_M1/GPIO2_A0_D	C20	I2C0_SCL_M1/UART3_CTSN/GPIO0_D2_D	Y20
USB1_HOST_DP	C21	UART0_TX_M0/JTAG_CPU_TCK_M1/JTAG_MCU_TCK_M1/JTAG_GPU_TCK_M1/GPIO0_C0_U	Y21
USB1_HOST_DM	C22	UART0_RX_M0/JTAG_CPU_TMS_M1/JTAG_MCU_TMS_M1/JTAG_GPU_TMS_M1/GPIO0_B7_U	Y22

## 2.7 IO Pin Name Description

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 2-2 IO Function Description List

Interface	Pin Name	Direction	Description
Misc	OSC_XIN	I	Clock input of 24M crystal XO
	OSC_XOUT	O	Clock output of 24M crystal XO
	REF_CLK0_OUT	O	24M Clock out
	CLK_32K_OUT_Mi (i=0~3)	O	32K Reference Clock Output
	CLK_32K_IN	I	32K clock in
	FEPHY_LEDLINK_Mi (i=0,1)	O	FEPHY link status indication
	FEPHY_LEDSPD_Mi (i=0,1)	O	FEPHY speed indication
	ETH1_PPSCCLK	O	Ethernet1 PPS clock signal
	ETH1_PTP_REFCLK	I	Ethernet0 PTP reference clock

Interface	Pin Name	Direction	Description
SW-DP	JTAG_CPU_TCK_Mi (i=0~1)	I	SWD interface clock input
	JTAG_CPU_TMS_Mi (i=0~1)	I/O	SWD interface data input/output

Interface	Pin Name	Direction	Description
eMMC Interface	EMMC_CLK	O	eMMC card clock
	EMMC_CMD	I/O	eMMC card command output and response input
	EMMC_D[i]	I/O	eMMC card data input and output

Interface	Pin Name	Direction	Description
	(i=0~7)		
	EMMC_STRB	I	eMMC strobe
	EMMC_RSTN	O	eMMC reset signal, active low

Interface	Pin Name	Direction	Description
SPI	SPIj_CLK_Mi (i=0~1) (j=0,1)	I	SPI serial clock
	SPIj_CSN0_Mi (i=0~1) (j=0,1)	I/O	SPI chip select signal, low active
	SPIj_CSN1_Mi (i=0~1) (j=0,1)	O	SPI chip select signal, low active
	SPIj_MOSI_Mi (i=0~1) (j=0,1)	I	SPI serial data input
	SPIj_MISO_Mi (i=0~1) (j=0,1)	O	SPI serial data output

Interface	Pin Name	Direction	Description
FSPI Controller	FSPI_CLK	O	FSPI serial clock
	FSPI_CSN0	O	FSPI chip select0 signal, low active
	FSPI_CSN1	O	FSPI chip select1 signal, low active
	FSPI_Di(i=0~7)	I/O	FSPI serial data input/output signal
	FSPI_RSTN	O	FSPI reset signal, active low
	FSPI_DQS	I/O	FSPI data strobe

Interface	Pin Name	Direction	Description
NAND	FLASH_ALE	O	Flash address latch enable signal
	FLASH_CLE	O	Flash command latch enable signal
	FLASH_WRN	O	Flash write enable and clock signal
	FLASH_RDN	O	Flash read enable and write/read signal
	FLASH_RDY	I	Flash ready/busy signal
	FLASH_CSi(i=0,1)	O	Flash chip enable signal for chip
	FLASH_WP	O	Flash write-protected signal
	FLASH_DATAi(i=0~7)	I/O	Flash data inputs/outputs signal

Interface	Pin Name	Direction	Description
SD/MMC/ SDIO Host Controller	SDMMCi_CLK(i=0,1)	O	SDMMC card clock
	SDMMCi_CMD(i=0,1)	I/O	SDMMC card command output and response input
	SDMMCi_D[j] (i=0~1)(j=0~3)	I/O	SDMMC card data input and output

Interface	Pin Name	Direction	Description
SAIO Controller	SAIO_MCLK_Mj (j=0~1)	I/O	I2S/PCM/TDM reference clock

Interface	Pin Name	Direction	Description
	SAI0_SCLK_Mj (j=0~1)	I/O	I2S/PCM/TDM serial clock
	SAI0_LRCK_Mj (j=0~1)	I/O	I2S/PCM/TDM channel indication signal
	SAI0_SDO_Mj (j=0~1)	O	I2S/PCM/TDM serial data output
	SAI0_SDI_Mj (j=0~1)	I	I2S/PCM/TDM serial data input

Interface	Pin Name	Direction	Description
SAI1 Controller	SAI1_MCLK_Mj (j=0~2)	I/O	I2S/PCM/TDM reference clock
	SAI1_SCLK_Mj (j=0~2)	I/O	I2S/PCM/TDM serial clock
	SAI1_LRCK_Mj (j=0~2)	I/O	I2S/PCM/TDM channel indication signal
	SAI1_SDOi_Mj (i=0~3)(j=0~2)	O	I2S/PCM/TDM serial data output
	SAI1_SDIi_Mj (i=0~3)(j=0~2)	I	I2S/PCM/TDM serial data input

Interface	Pin Name	Direction	Description
SAI2 Controller	SAI2_MCLK_Mj (j=0~1)	I/O	I2S/PCM/TDM reference clock
	SAI2_SCLK_Mj (j=0~1)	I/O	I2S/PCM/TDM serial clock
	SAI2_LRCK_Mj (j=0~1)	I/O	I2S/PCM/TDM channel indication signal
	SAI2_SDO_Mj (j=0~1)	O	I2S/PCM/TDM serial data output
	SAI2_SDI_Mj (j=0~1)	I	I2S/PCM/TDM serial data input

Interface	Pin Name	Direction	Description
PWM	PWM0_CHi_Mj(i=0~3)(j=0,1)	I/O	Pulse Width Modulation input and output
	PWM1_CHi_Mj(i=0~3)(j=0,1)	I/O	Pulse Width Modulation input and output

Interface	Pin Name	Direction	Description
I2C	I2C0_SDA_Mj (j=0,1)	I/O	I2C0 data
	I2C0_SCL_Mj (j=0,1)	I/O	I2C0 clock
	I2Ci_SDA_Mj (i=1~5)(j=0~2)	I/O	I2C data
	I2Ci_SCL_Mj (i=1~5)(j=0~2)	I/O	I2C clock

Interface	Pin Name	Direction	Description
UART0	UART0_RX_Mj (j=0,1)	I	UART0 serial data input
	UART0_TX_Mj (j=0,1)	O	UART0 serial data output

Interface	Pin Name	Direction	Description
UART1	UART1_RX_Mj (j=0,1,2)	I	UART1 serial data input
	UART1_TX_Mj (j=0,1,2)	O	UART1 serial data output
	UART1_CTSN_Mj (j=0,1,2)	I	UART1 clear to send modem status input
	UART1_RTSN_Mj	O	UART1 modem control request to send

Interface	Pin Name	Direction	Description
	(j=0,1,2)		output

Interface	Pin Name	Direction	Description
UART2	UART2_RX_Mj (j=0,1)	I	UART2 serial data input
	UART2_TX_Mj (j=0,1)	O	UART2 serial data output
	UART2_CTSN_Mj (j=0,1)	I	UART2 clear to send modem status input
	UART2_RTSN_Mj (j=0,1)	O	UART2 modem control request to send output

Interface	Pin Name	Direction	Description
UART3	UART3_RX_Mj (j=0,1,2)	I	UART3 serial data input
	UART3_TX_Mj (j=0,1,2)	O	UART3 serial data output
	UART3_CTSN	I	UART3 clear to send modem status input
	UART3_RTSN	O	UART3 modem control request to send output

Interface	Pin Name	Direction	Description
UART4	UART4_RX_Mj (j=0,1)	I	UART4 serial data input
	UART4_TX_Mj (j=0,1)	O	UART4 serial data output
	UART4_CTSN_Mj (j=0,1)	I	UART4 clear to send modem status input
	UART4_RTSN_Mj (j=0,1)	O	UART4 modem control request to send output

Interface	Pin Name	Direction	Description
UART5	UART5_RX_Mj (j=0,1)	I	UART5 serial data input
	UART5_TX_Mj (j=0,1)	O	UART5 serial data output
	UART5_CTSN	I	UART5 clear to send modem status input
	UART5_RTSN	O	UART5 modem control request to send output

Interface	Pin Name	Direction	Description
FEPHY	FEPHY_REXT	O	External 6K-Ohm resistor to ground
	FEPHY_RXN	I/O	FEPHY transceiver negative output/input
	FEPHY_RXP	I/O	FEPHY transceiver positive output/input
	FEPHY_TXN	I/O	FEPHY transceiver negative output/input
	FEPHY_TXP	I/O	FEPHY transceiver positive output/input

Interface	Pin Name	Direction	Description
ACODEC	ACODEC_LINEOUT_R	O	ACODEC right channel output
	ACODEC_LINEOUT_L	O	ACODEC left channel output
	ACODEC_VCM	O	Reference voltage output

Interface	Pin Name	Direction	Description
USB 2.0	USB2_HOST_DP	I/O	USB 2.0 Data signal DP
	USB2_HOST_DM	I/O	USB 2.0 Data signal DM
	USB2_DRD_DP	I/O	USB 2.0 Data signal DP
	USB2_DRD_DM	I/O	USB 2.0 Data signal DM

Interface	Pin Name	Direction	Description
VDAC	VDAC_IREF	I	Connect external resistor to generate current reference
	VDAC_IOUTP	O	Data signal positive output
	VDAC_IOUTN	O	Data signal negative output

Interface	Pin Name	Direction	Description
SARSDC ADC	SARADC_INi(i=0~3)	I	Analog input

Interface	Pin Name	Direction	Description
HDMI	HDMI_TX_D0N	O	TMDS channel 0 negative data line
	HDMI_TX_D0P	O	TMDS channel 0 positive data line
	HDMI_TX_D1N	O	TMDS channel 1 negative data line
	HDMI_TX_D1P	O	TMDS channel 1 positive data line
	HDMI_TX_D2N	O	TMDS channel 2 negative data line
	HDMI_TX_D2P	O	TMDS channel 2 positive data line
	HDMI_REXT	O	Connect 2.0Kohm resistor to ground to generate reference current
	HDMI_TX_HPD_5V	I	HDMI 5V hot plug detect signal
	HDMI_TX_CEC_3V3	I/O	HDMI 3.3V CEC signal
	HDMI_TX_SCL_5V	I/O	HDMI 5V I2C SCL signal
	HDMI_TX_SDA_5V	I/O	HDMI 5V I2C SDA signal

Interface	Pin Name	Direction	Description
DDR Interface	CLKP	O	Active-high clock signal to the memory device.
	CLKN	O	Active-low clock signal to the memory device.
	CKE	O	Active-high clock enable signal to the memory device
	CSN[i] (i=0~3)	O	Active-low chip select signal to the memory device. AThere are two chip select.
	RASn	O	Active-low row address strobe to the memory device.
	CASn	O	Active-low column address strobe to the memory device.
	WEn	O	Active-low write enable strobe to the memory device.
	BA[i] (i=0,1)	O	Bank address signal to the memory device.
	BG[i] (i=0,1)	O	Bank group signal to the memory device.
	A[i] (i=0~17)	O	Address signal to the memory device.
	DQ[i] (i=0~31)	I/O	BiDir.al data line to the memory device.
	DQS[i]_P (i=0~3)	I/O	Active-high biDir.al data strobes to the memory device.
	DQS[i]_N (i=0~3)	I/O	Active-low biDir.al data strobes to the memory device.

Interface	Pin Name	Direction	Description
	DM[ <i>i</i> ] ( <i>i</i> =0~3)	O	Active-low data mask signal to the memory device.
	ODT[ <i>i</i> ] ( <i>i</i> =0,1)	O	On-Die Termination output signal for two chip select.
	RESETn	O	DDR3/DDR4 reset signal to the memory device
	ACTN	O	Activation command input

## Chapter 3 Electrical Specification

### 3.1 Absolute Ratings

The below table provides the absolute ratings.

Absolute maximum or minimum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

Table 3-1 Absolute ratings

Parameters	Related Power Group	Min	Max	Unit
Supply voltage for CPU	CPU_DVDD	0	1.1	V
Supply voltage for Logic	LOGIC_DVDD	0	1.1	V
0.9V supply voltage	HDMI_TX_DVDD0V9 FEPHY_AVDD0V9 USB20_DVDD0V9 PLL_AVDD0V9	0	1.1	V
Supply voltage for PMUIO1	PMUIO1_VCC	0	3.8	V
Supply voltage for VCCIO1	VCCIO1_VCC	0	3.8	V
Supply voltage for VCCIO2	VCCIO2_VCC	0	3.8	V
Supply voltage for VCCIO3	VCCIO3_VCC	0	3.8	V
Supply voltage for VCCIO4	VCCIO4_VCC	0	3.8	V
Supply voltage for VCCIO5	VCCIO5_VCC	0	3.8	V
Supply voltage for VCCIO6	VCCIO6_VCC	0	3.8	V
1.8V supply voltage	ACODEC_AVDD1V8 PLL_AVDD1V8 DDR_PLL_AVDD1V8 HDMI_TX_AVDD1V8 OTP_VCC1V8 FEPHY_AVDD1V8 SARADC_AVDD1V8 USB20_AVDD1V8 VDAC_AVDD1V8	0	2.0	V
3.3V supply voltage	PMU_LDO_3V3_IN PMUIO0_VCC3V3 FEPHY_AVDD3V3 USB20_AVDD3V3	0	3.8	V
Supply voltage for DDR IO	DDR_VDDQ DDR_VDDQL	0	TBD	V
Storage Temperature	Tstg	-40	125	°C
Max Conjunction Temperature	Tj	NA	125	°C

### 3.2 Recommended Operating Condition

Following table describes the recommended operating condition.

Table 3-2 Recommended operating condition

Parameters	Symbol	Min	Typ	Max	Unit
Voltage for CPU	CPU_DVDD	0.81	0.90	TBD	V
Voltage for LOGIC	LOGIC_DVDD	0.81	0.90	0.99	V
Supply voltage for PMUIO0	PMUIO0_VCC3V3 PMUIO0_LDO3V3	2.97	3.3	3.63	V
Supply voltage for PMUIO1	PMUIO1_VCC	1.62 2.97	1.8 3.3	1.98 3.63	V
Supply voltage for VCCIO1	VCCIO1_VCC	1.62 2.97	1.8 3.3	1.98 3.63	V
Supply voltage for VCCIO2	VCCIO2_VCC	1.62 2.97	1.8 3.3	1.98 3.63	V
Supply voltage for VCCIO3	VCCIO3_VCC	1.62 2.97	1.8 3.3	1.98 3.63	V
Supply voltage for VCCIO4	VCCIO4_VCC	1.62 2.97	1.8 3.3	1.98 3.63	V
Supply voltage for VCCIO5	VCCIO5_VCC	1.62 2.97	1.8 3.3	1.98 3.63	V
Supply voltage for VCCIO6	VCCIO6_VCC	1.62 2.97	1.8 3.3	1.98 3.63	V

Parameters	Symbol	Min	Typ	Max	Unit
Voltage for PLL Analog (1.8V)	PLL_AVDD1V8 DDR_PLL_AVDD1V8	1.62	1.8	1.98	V
Voltage for HDMI Analog (1.8V)	HDMI_TX_AVDD1V8	1.62	1.8	1.98	V
Voltage for USB Analog (1.8V)	USB20_AVDD1V8	1.62	1.8	1.98	V
Voltage for USB Analog (3.3V)	USB20_AVDD3V3	3.0	3.3	3.6	V
Voltage for FEPHY Analog (1.8V)	FEPHY_AVDD1V8	1.62	1.8	1.98	V
Voltage for FEPHY Analog (3.3V)	FEPHY_AVDD3V3	2.97	3.3	3.63	V
Voltage for OTP Analog(1.8V)	OTP_VCC1V8	1.62	1.8	1.98	V
Voltage for VDAC Analog(1.8V)	VDAC_AVDD1V8	1.62	1.8	1.98	V
Voltage for ACODEC Analog(1.8V)	ACODEC_AVDD1V8	1.62	1.8	1.98	V
Voltage for SARADC Analog(1.8V)	SARADC_AVDD1V8	1.62	1.8	1.98	V
DDR3 IO VDDQ Voltage	DDR_VDDQ	1.425	1.5	1.575	V
DDR3L IO VDDQ Voltage	DDR_VDDQ	1.283	1.35	1.417	V
LPDDR3 IO VDDQ Voltage	DDR_VDDQ	1.14	1.2	1.3	V
DDR4 IO VDDQ Voltage	DDR_VDDQ	1.14	1.2	1.3	V
LPDDR4 IO VDDQ Voltage	DDR_VDDQ	1.06	1.1	1.17	V
LPDDR4X IO VDDQ Voltage	DDR_VDDQL	0.54	0.6	0.66	V
Ambient Operating Temperature	T <sub>A</sub>	0	NA	80	°C

### 3.3 DC Characteristics

Table 3-3 DC Characteristics

Parameters		Symbol	Min	Typ	Max	Unit
Digital GPIO @3.3V	Input Low Voltage	Vil	-0.3	NA	0.8	V
	Input High Voltage	Vih	2.0	NA	VDDO+0.3	V
	Output Low Voltage	Vol	-0.3	NA	0.4	V
	Output High Voltage	Voh	2.4	NA	VDDO+0.3	V
	Pullup Resistor	Rpu	16	26	43	Kohm
	Pulldown Resistor	Rpd	16	26	43	Kohm
Digital GPIO @1.8V	Input Low Voltage	Vil	-0.3	NA	0.35*VDDO	V
	Input High Voltage	Vih	0.65*VDDO	NA	VDDO+0.3	V
	Output Low Voltage	Vol	-0.3	NA	0.4	V
	Output High Voltage	Voh	1.4	NA	VDDO+0.3	V
	Pullup Resistor	Rpu	16	26	43	Kohm
	Pulldown Resistor	Rpd	16	26	43	Kohm
HDMI IIC IO@5V	Input Low Voltage	Vil	-0.3	NA	0.3*VDDO	V
	Input High Voltage	Vih	0.7*VDDO	NA	VDDO+0.3	V
	Output Low Voltage	Vol	-0.3	NA	0.4	V
	Output High Voltage	Voh	0.9*VDDO	NA	VDDO+0.3	V
	Positive Going Threshold Voltage	Vt+	0.5*VDDO	NA	0.7*VDDO	V
	Negative Going Threshold Voltage	Vt-	0.3*VDDO	NA	0.5*VDDO	V
	Input Hysteresis	Vhys	0.1*VDDO	NA	0.2*VDDO	V
HDMI HPD IO@5V	Input Low Voltage	Vil	-0.3	NA	0.3*VDDO	V
	Input High Voltage	Vih	2.0	NA	VDDO+0.3	V
	Output Low Voltage	Vol	-0.3	NA	0.4	V
	Output High Voltage	Voh	0.9*VDDO	NA	VDDO+0.3	V
	Positive Going Threshold Voltage	Vt+	2.0	NA	2.4	V
	Negative Going Threshold Voltage	Vt-	1.4	NA	1.6	V
	Input Hysteresis	Vhys	0.3	NA	0.6	V
HDMI CEC IO@3.3V	Input Low Voltage	Vil	-0.3	NA	0.3*VDDO	V
	Input High Voltage	Vih	2.0	NA	VDDO	V
	Output Low Voltage	Vol	-0.3	NA	0.4	V

Parameters	Symbol	Min	Typ	Max	Unit
Output High Voltage	Voh	0.9*VDDO	NA	VDDO+0.3	V
Positive Going Threshold Voltage	Vt+	0.5*VDDO	NA	0.7*VDDO	V
Negative Going Threshold Voltage	Vt-	0.3*VDDO	NA	0.5*VDDO	V
Input Hysteresis	Vhys	0.1*VDDO	NA	0.2*VDDO	V
Pmos driving current(PAD=0.8VDDO) SEL:DS1/DS0	IOH		00 4mA 01 6mA 10 8mA 11 12mA		mA
Nmos driving current(PAD=0.4) SEL:DS1/DS0	IOL		00 4mA 01 6mA 10 8mA 11 12mA		mA
Pullup high resistance	Rpu	22.95K	27K	31.05K	Ohm

VDDO is the 5V/3.3V supply voltage connected to external pull-up resistor

Parameters	Symbol	Min	Typ	Max	Unit	
DDR IO @DDR3 mode	Input High Voltage	Vih_dds	Vref+0.1	NA	DDR_VDDQ	V
	Input Low Voltage	Vil_dds	VSS	NA	Vref-0.1	V
	output impedance	Rtt	20	NA	60	Ohm
DDR IO @DDR3L mode	Input High Voltage	Vih_dds	Vref+0.1	NA	DDR_VDDQ	V
	Input Low Voltage	Vil_dds	VSS	NA	Vref-0.1	V
	output impedance	Rtt	20	NA	60	Ohm
DDR IO @DDR4 mode	Input High Voltage	Vih_dds	Vref+0.1	NA	DDR_VDDQ	V
	Input Low Voltage	Vil_dds	VSS	NA	Vref-0.1	V
	output impedance	Rtt	20	NA	60	Ohm
DDR IO @LPDDR3 mode	Input High Voltage	Vih_dds	Vref+0.1	NA	DDR_VDDQ	V
	Input Low Voltage	Vil_dds	VSS	NA	Vref-0.1	V
	output impedance	Rtt	20	NA	60	Ohm
DDR IO @LPDDR4 mode	Input High Voltage	Vih_dds	Vref+0.1	NA	DDR_VDDQ	V
	Input Low Voltage	Vil_dds	VSS	NA	Vref-0.1	V
	output impedance	Rtt	20	NA	60	Ohm
DDR IO @LPDDR4X mode	Input High Voltage	Vih_dds	Vref+0.1	NA	DDR_VDDQL	V
	Input Low Voltage	Vil_dds	VSS	NA	Vref-0.1	V
	output impedance	Rtt	20	NA	60	Ohm

### 3.4 Electrical Characteristics for General IO

Table 3-4 Electrical Characteristics for Digital General IO

Parameters	Symbol	Test condition	Min	Typ	Max	Unit	
Digital GPIO @3.3V	Input leakage current	Ii	Vin = 3.3V or 0V	NA	NA	10	uA
	Tri-state output leakage current	Ioz	Vout = 3.3V or 0V	NA	NA	10	uA
	High level input current	Iih	Vin = 3.3V, pulldown disabled	NA	NA	10	uA
			Vin = 3.3V, pulldown enabled	NA	NA	10	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	NA	NA	10	uA
			Vin = 0V, pullup enabled	NA	NA	10	uA
Input leakage current	Ii	Vin = 1.8V or 0V	NA	NA	10	uA	

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
Digital GPIO @1.8V	Tri-state output leakage current	I <sub>oz</sub>	V <sub>out</sub> = 1.8V or 0V	NA	NA	10	uA
	High level input current	I <sub>ih</sub>	V <sub>in</sub> = 1.8V, pulldown disabled	NA	NA	10	uA
			V <sub>in</sub> = 1.8V, pulldown enabled	NA	NA	10	uA
	Low level input current	I <sub>il</sub>	V <sub>in</sub> = 0V, pullup disabled	NA	NA	10	uA
V <sub>in</sub> = 0V, pullup enabled			NA	NA	10	uA	

Note: VDDO and DVDD are both IO power Supply

### 3.5 Electrical Characteristics for PLL

Table 3-5 Electrical Characteristics for INT PLL

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
	Input clock frequency(Frac)	F <sub>in</sub>	F <sub>in</sub> = FREF @1.8V/0.99V	10	NA	800	MHz
	VCO operating range	F <sub>vco</sub>	F <sub>vco</sub> = Fref * FBDIV @3.3V/0.99V	475	NA	1900	MHz
	Output clock frequency	F <sub>out</sub>	F <sub>out</sub> = Fvco/POSTDIV @3.3V/0.99V	9	NA	1900	MHz
	Lock time	T <sub>lit</sub>	@ 3.3V/0.99V, FREF=24M,REFDIV=1	NA	1000	1500	Input clock cycles

Table 3-6 Electrical Characteristics for FRAC PLL

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
	Input clock frequency(Frac)	F <sub>in</sub>	F <sub>in</sub> = FREF @1.8V/0.99V	1	NA	1200	MHz
	VCO operating range	F <sub>vco</sub>	F <sub>vco</sub> = Fref * FBDIV @3.3V/0.99V	950	NA	3800	MHz
	Output clock frequency	F <sub>out</sub>	F <sub>out</sub> = Fvco/POSTDIV @3.3V/0.99V	19	NA	3800	MHz
	Lock time	T <sub>lit</sub>	@ 3.3V/0.99V, FREF=24M,REFDIV=1	NA	250	500	Input clock cycles

Notes:

- ① REF<sub>DIV</sub> is the input divider value;
- ② F<sub>B</sub><sub>DIV</sub> is the feedback divider value;
- ③ POST<sub>DIV</sub> is the output divider value

### 3.6 Electrical Characteristics for USB2.0 Interface

Table 3-7 Electrical Characteristics for USB2.0 Interface

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Transmitter						
Output resistance	ROUT	Classic mode (V <sub>out</sub> = 0 or 3.3V)	40.5	45	49.5	ohms
		HS mode (V <sub>out</sub> = 0 to 800mV)	40.5	45	49.5	ohms
Output Capacitance	COUT	seen from D+ or D-			3	pF
Output Common Mode Voltage	VM	Classic (LS/FS) mode	1.45	1.65	1.85	V
		HS mode	0.175	0.2	0.225	V
Differential output signal high	VOH	Classic (LS/FS); I <sub>o</sub> =0mA	2.97	3.3	3.63	V
		Classic (LS/FS); I <sub>o</sub> =6mA	2.2	2.7	NA	V
		HS mode; I <sub>o</sub> =0mA	360	400	440	mV
Differential output signal low	VOL	Classic (LS/FS); I <sub>o</sub> =0mA	-0.33	0	0.33	V
		Classic (LS/FS); I <sub>o</sub> =6mA	NA	0.3	0.8	V
		HS mode; I <sub>o</sub> =0mA	-40	0	40	mV
Receiver						
Receiver sensitivity	RSENS	Classic mode		±250		mV
		HS mode		±25		mV

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Receiver common mode	RCM	Classic mode	0.8	1.65	2.5	V
		HS mode (differential and squelch comparator)	0.1	0.2	0.3	V
		HS mode (disconnect comparator)	0.5	0.6	0.7	V
Input capacitance (seen at D+ or D-)			NA	NA	3	pF
Squelch threshold			100	NA	150	mV
Disconnect threshold			570	600	664	mV

### 3.7 Electrical Characteristics for HDMI

Table 3-8 Electrical Characteristics for HDMI

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Differential output signal rise time	tR	20~80% RL=50Ω	75	NA	NA	ps
	tR_DATA	20~80% RL=50Ω	42.5	NA	NA	ps
	tR_CLOCK	20~80% RL=50Ω	75	NA	NA	ps
Differential output signal fall time	tF	20~80% RL=50Ω	75	NA	NA	ps
	tF_DATA	20~80% RL=50Ω	42.5	NA	NA	ps
	tF_CLOCK	20~80% RL=50Ω	75	NA	NA	ps

### 3.8 Electrical Characteristics for Audio CODEC interface

Table 3-9 Electrical Characteristics for Audio CODEC

Test conditions: AVDD = 1.8V, DVDD = 0.8V, TA = 25°C, 1KHz Sine Input, Fs = 48KHz

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Operating Condition						
Analog Supply	AVDD		1.62	1.8	1.98	V
DAC Line Output						
Programmable Gain	GDRV		-39	NA	6	dB
Gain Step Size			NA	1.5	NA	dB
Signal to Noise Ratio	SNR	A-weighted	NA	93	NA	dB
Total Harmonic Distortion	THD	-3dBFS output 600Ω load	NA	-84	NA	dB
Power Supply Rejection	PSRR	1KHz	NA	55	NA	dB
Power Consumption						
Standby			NA	0.05	NA	mA
Stereo Playback		Quiescent output	NA	5	NA	mA

### 3.9 Electrical Characteristics for SARADC

Table 3-10 Electrical Characteristics for SARADC

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Resolution			NA	13	NA	bit
Effective Number of Bit	ENOB		NA	9	NA	bit
Differential Non-Linearity	DNL		-1	NA	+1	LSB
Integral Non-Linearity	INL		-2	NA	+2	LSB
Reference voltage	VREFP		NA	1.8	NA	V
Input Capacitance	C <sub>IN</sub>		NA	8	NA	pF
Sampling Rate	f <sub>S</sub>		NA	NA	1	MS/s
Spurious Free Dynamic Range	SFDR	f <sub>S</sub> =1MS/s f <sub>OUT</sub> =1.17KHz	NA	61	NA	dB

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Signal to Noise and Harmonic Ratio	SNDR		NA	56	NA	dB

### 3.10 Electrical Characteristics for TSADC

Table 3-11 Electrical Characteristics for TSADC

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Accuracy from -40°C to 125°C	T <sub>JACC</sub>		NA	NA	±5	°C
Sensing Temperature Range	T <sub>RANGE</sub>		-40	NA	125	°C
Resolution	T <sub>LSB</sub>		NA	0.6	NA	°C

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## Chapter 4 Thermal Management

### 4.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature has to be below 125°C.

### 4.2 Package Thermal Characteristics

Table 4-1 provides the thermal resistance characteristics for the package used on the SoC. The resulting simulation data for reference only, please prevail in kind test.

Table 4-1 Thermal Resistance Characteristics

Symbol	Description	Value	Unit	Note
$\theta_{JA}$	Junction-to-ambient thermal resistance	21.92	(°C/W)	(1)
$\theta_{JB}$	Junction-to-board thermal resistance	12.46	(°C/W)	(2)
$\theta_{JC}$	Junction-to-case thermal resistance	7.29	(°C/W)	(3)
$\psi_{JT}$	Thermal characterization parameter	0.2	(°C/W)	(4)

Note (1): The package-board system is placed in the natural convection (JEDEC JESD51-2 standard), and the 2S2P test-board is designed in accordance with JESD 51-7/JESD 51-9. The actual system design and environment may be different.(The PCB is 4 layers, 114.3 mm\*101.6 mm)

Note (2):  $\theta_{JB}$  is measured in the special environment (JEDEC JESD51-8 standard), and the printed circuit board used to mount the devices is specified in JESD51-7.

Note (3): The thermal resistance  $\theta_{JC}$  is provided in compliance with the JEDEC JESD51-14.

Note (4):  $\psi_{JT}$  - The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package,  $\psi_{JT}$  is measured in the test environment of  $\theta_{JA}$  (JEDEC JESD51-2 standard).