# *Rockchip RK3588 Datasheet*



## Revision History

| Date | Revision | Description |
|---|---|---|
| 2022-05-24 | 1.4 | Update Package dimension and Block Diagram |
| 2022-03-28 | 1.3 | Update Package information and operating condition |
| 2022-03-14 | 1.2 | Update recommended operating condition |
| 2022-01-24 | 1.1 | Update the description |
| 2021-12-20 | 1.0 | Initial Release for special reference |

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# Chapter 1 Introduction

## 1.1 Overview

RK3588 is a low power, high performance processor for ARM-based PC and Edge Computing device, personal mobile internet device and other digital multimedia applications, and integrates quad-core Cortex-A76 and quad-core Cortex-A55 with separately NEON coprocessor.

Many embedded powerful hardware engines provide optimized performance for high-end application. RK3588 supports H.265 and VP9 decoder by 8K@60fps, H.264 decoder by 8K@30fps, and AV1 decoder by 4K@60fps, also support H.264 and H.265 encoder by 8K@30fps, high-quality JPEG encoder/decoder, specialized image preprocessor and postprocessor.

Embedded 3D GPU makes RK3588 completely compatible with OpenGLES 1.1, 2.0, and 3.2, OpenCL up to 2.2 and Vulkan1.2. Special 2D hardware engine with MMU will maximize display performance and provide very smoothly operation.

RK3588 introduces a new generation totally hardware-based maximum 48-Megapixel ISP (image signal processor). It implements a lot of algorithm accelerators, such as HDR, 3A, LSC, 3DNR, 2DNR, sharpening, dehaze, fisheye correction, gamma correction and so on.

The build-in NPU supports INT4/INT8/INT16/FP16 hybrid operation and computing power is up to 6TOPs. In addition, with its strong compatibility, network models based on a series of frameworks such as TensorFlow/MXNet/PyTorch/Caffe can be easily converted.

RK3588 has high-performance quad channel external memory interface (LPDDR4/LPDDR4X/LPDDR5) capable of sustaining demanding memory bandwidths, also provides a complete set of peripheral interface to support very flexible applications.

## 1.2 Features

The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

### 1.2.1 Microprocessor

- Quad-core ARM Cortex-A76 MPCore processor and quad-core ARM Cortex-A55 MPCore processor, both are high-performance, low-power and cached application processor
- DSU (DynamIQ Shared Unit) comprises the L3 memory system, control logic, and external interfaces to support a DynamIQ cluster
- Full implementation of the ARM architecture v8-A instruction set, ARM Neon Advanced SIMD (single instruction, multiple data) support for accelerating media and signal processing
- ARMv8 Cryptography Extensions
- Trustzone technology support
- Integrated 64KB L1 instruction cache, 64KB L1 data cache and 512KB L2 cache for each Cortex-A76
- Integrated 32KB L1 instruction cache, 32KB L1 data cache and 128KB L2 cache for each Cortex-A55
- Quad-core Cortex-A76 and Quad-core Cortex-A55 share 3MB L3 cache
- Eight separate power domains for CPU core system to support internal power switch and externally turn on/off based on different application scenario
  - PD_CPU_0: 1st Cortex-A55 + Neon + FPU + L1/L2 I/D Cache
  - PD_CPU_1: 2nd Cortex-A55 + Neon + FPU + L1/L2 I/D Cache
  - PD_CPU_2: 3rd Cortex-A55 + Neon + FPU + L1/L2 I/D Cache
  - PD_CPU_3: 4th Cortex-A55 + Neon + FPU + L1/L2 I/D Cache
  - PD_CPU_4: 1st Cortex-A76 + Neon + FPU + L1/L2 I/D Cache
  - PD_CPU_5: 2nd Cortex-A76 + Neon + FPU + L1/L2 I/D Cache
  - PD_CPU_6: 3rd Cortex-A76 + Neon + FPU + L1/L2 I/D Cache
  - PD_CPU_7: 4th Cortex-A76 + Neon + FPU + L1/L2 I/D Cache

- Three isolated voltage domains to support DVFS, one for A76_0 and A76_1, one for A76_2 and A76_3, the other for DSU and Cortex-A55.

### 1.2.2 Memory Organization

- Internal on-chip memory
  - BootRom
    - Support system boot from the following device:
      - SPI interface
      - eMMC interface
      - SD/MMC interface
    - Support system code download by the following interface:
      - USB OTG interface
  - Share Memory in the voltage domain of VD_LOGIC
  - PMU SRAM in VD_PMU for low power application
- External off-chip memory
  - Dynamic Memory Interface
    - Compatible with JEDEC standards LPDDR4/LPDDR4X/LPDDR5
    - Support four channels, each channel 16bits data widths
    - Support up to 2 ranks (chip selects) for each channel
    - Totally up to 32GB address space
    - Low power modes, such as power-down and self-refresh for SDRAM
  - eMMC Interface
    - Fully compliant with JEDEC eMMC 5.1 and eMMC 5.0 specification
    - Backward compliant with eMMC 4.51 and earlier versions specification.
    - Support HS400, HS200, DDR50 and legacy operating modes
    - Support three data bus width: 1bit, 4bits or 8bits
  - SD/MMC Interface
    - Compatible with SD3.0, MMC ver4.51
    - Data bus width is 4bits
  - Flexible Serial Flash Interface(FSPI)
    - Support transfer data from/to serial flash device
    - Support 1bit, 2bits or 4bits data bus width
    - Support 2 chips select

### 1.2.3 System Component

- MCU
  - Three Cortex-M0 MCUs inside RK3588
  - MCU in VD_PMU integrate 16KB Cache and 16KB TCM
  - MCU in VD_NPU integrate 16KB Cache and 64KB TCM
  - MCU in PD_CENTER integrate 32KB TCM
  - Integrated Programmable Interrupt Controller, all IRQ lines connected to GIC for CPU also connect to MCU in VD_PMU(PMU_M0) and PD_CENTER(DDR_M0)
  - Integrated Debug Controller with JTAG interface
- CRU (clock & reset unit)
  - Support total 18 PLLs to generate all clocks
  - One oscillator with 24MHz clock input
  - Support clock gating control for individual components
  - Support global soft-reset control for whole chip, also individual soft-reset for each component
- PMU(power management unit)
  - Multiple configurable work modes to save power by different frequency or automatic clock gating control or power domain on/off control
  - Lots of wakeup sources in different mode
  - Support 10 separate voltage domains
  - Support 45 separate power domains, which can be power up/down by software based on different application scenes
- Timer
  - Support 12 secure timers with 64bits counter and interrupt-based operation
  - Support 18 non-secure timers with 64bits counter and interrupt-based operation
  - Support two operation modes: free-running and user-defined count for each timer

- Support timer work state checkable
- PWM
  - Support 16 on-chip PWMs(PWM0~PWM15) with interrupt-based operation
  - Programmable pre-scaled operation to bus clock and then further scaled
  - Embedded 32-bit timer/counter facility
  - Support capture mode
  - Support continuous mode or one-shot mode
  - Provides reference mode and output various duty-cycle waveform
  - Optimized for IR application for PWM3, PWM7, PWM11, PWM15
- Watchdog
  - 32-bit watchdog counter
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - Generate a system reset
    - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
  - Totally five Watchdog for CPU and MCU
- Interrupt Controller
  - Support 12 PPI interrupt source and 480 SPI interrupt sources input from different components inside RK3588
  - Support 16 software-triggered interrupts
  - Input interrupt level is fixed, high-level sensitive for SPI and low-level sensitive for PPI
  - Support different interrupt priority for each interrupt source, and they are always software-programmable
- DMAC
  - Micro-code programming based DMA
  - Linked list DMA function is supported to complete scatter-gather transfer
  - Support data transfer types including memory-to-memory, memory-to-peripherals, peripherals-to-memory
  - Totally three embedded DMA controllers for peripheral system
  - Each DMAC features:
    - Support 8 channels
    - 32 hardware request from peripherals
    - 2 interrupt output
    - Support TrustZone technology and programmable secure state for each DMA channel
- Secure System
  - Embedded two cipher engine
    - Support Link List Item (LLI) DMA transfer
    - Support SHA-1, SHA-256/224, SHA-512/384, MD5, SM3 with hardware padding
    - Support HMAC of SHA-1, SHA-256, SHA-512, MD5, SM3 with hardware padding
    - Support AES-128, AES-192, AES-256 encrypt & decrypt cipher
    - Support AES ECB/CBC/OFB/CFB/CTR/CTS/XTS/CCM/GCM/CBC-MAC/CMAC mode
    - Support SM4 ECB/CBC/OFB/CFB/CTR/CTS/XTS/CCM/GCM/CBC-MAC/CMAC mode
    - Support DES & TDES cipher, with ECB/CBC/OFB/CFB mode
    - Support up to 4096 bits PKA mathematical operations for RSA/ECC/SM2
    - Support generating random numbers
  - Support keyladder to guarantee key secure
  - Support data scrambling for all DDR types
  - Support secure OTP
  - Support secure debug
  - Support secure DFT test
  - Support secure OS
  - Except CPU, the other masters in the SoC can also support security and non-

security mode by software-programmable
  - Some slave components in SoC can only be addressed by security master and the other slave components can be addressed by security master or non-security master by software-programmable
  - System SRAM(share memory), part of space is addressed only in security mode
  - External DDR space can be divided into 16 parts, each part can be software-programmable to be enabled by each master
- Mailbox
  - Three Mailbox in SoC to service CPU and MCU communication
  - Support four mailbox elements per mailbox, each element includes one data word, one command word register and one flag bit that can represent one interrupt
  - Provide 32 lock registers for software to use to indicate whether mailbox is occupied
- Decompression
  - Support for decompressing GZIP files
  - Support for decompressing LZ4 files, including the General Structure of LZ4 Frame format and the Legacy Frame format.
  - Support for decompressing data in DEFLATE format
  - Support for decompressing data in ZLIB format
  - Support Hash32 check in LZ4 decompression process
  - Support the limit size function of the decompressed data to prevent the memory from being maliciously destroyed during the decompression process

### 1.2.4 Video CODEC

- Video Decoder
  - Real-time video decoder of MPEG-1, MPEG-2, MPEG-4, H.263, H.264, H.265, VC-1, VP9, VP8, MVC, AV1
  - MMU Embedded
  - Multi-channel decoder in parallel for less resolution
  - H.264 AVC/MVC Main10 L6.0 : 8K@30fps (7680x4320)[2]
  - VP9 Profile0/2 L6.1 : 8K@60fps (7680x4320)
  - H.265 HEVC/MVC Main10 L6.1 : 8K@60fps (7680x4320)
  - AVS2 Profile0/2 L10.2.6 : 8K@60fps (7680x4320)
  - AV1 Main Profile 8/10bit L5.3 : 4K@60fps (3840x2160)
  - MPEG-2 up to MP : 1080p@60fps (1920x1088)
  - MPEG-1 up to MP : 1080p@60fps (1920x1088)
  - VC-1 up to AP level 3 : 1080p@60fps (1920x1088)
  - VP8 version2 : 1080p@60fps (1920x1088)
- Video Encoder
  - Real-time H.265/H.264 video encoding
  - Support up to 8K@30fps
  - Multi-channel encoder in parallel for less resolution

### 1.2.5 JPEG CODEC

- JPEG Encoder
  - Baseline (DCT sequential)
  - Encoder size is from 96x96 to 8192x8192(67Mpixels)
  - Up to 90 million pixels per second
  - Embedded four encoder units
- JPEG Decoder
  - Decoder size is from 48x48 to 65536x65536
  - Support YUV400/YUV411/YUV420/YUV422/YUV440/YUV444
  - Support up to 1080P@280fps, and 560 million pixels per second
  - Support MJPEG
  - Embedded four encoder units

### 1.2.6 Neural Process Unit

- Neural network acceleration engine with processing performance up to 6 TOPS
- Include triple NPU core, and support triple core co-work, dual core co-work, and work independently
- Support integer 4, integer 8, integer 16, float 16, Bfloat 16 and tf32 operation

- Embedded 384KBx3 internal buffer
- Multi-task, multi-scenario in parallel
- Support deep learning frameworks: TensorFlow, Caffe, Tflite, Pytorch, Onnx NN, Android NN, etc.
- One isolated voltage domain to support DVFS

### 1.2.7 Graphics Engine

- 3D Graphics Engine
  - ARM Mali-G610 MP4
  - High performance OpenGLES 1.1, 2.0 and 3.2, OpenCL 2.2, Vulkan1.2 etc.
  - Embedded 4 shader cores with shared hierarchical tiler
  - Provide MMU and L2 Cache with 4x 256KB size
  - The latest Valhall architecture
  - ARM Frame Buffer Compression(AFBC) 1.3
  - Support Serial Wire debug for embedded MCU
  - One isolated voltage domain to support DVFS
- 2D Graphics Engine
  - Source format: ARGB/RGB888/RGB565/YUV420/YUV422/BPP
  - Destination formats: ARGB/RGB888/RGB565/YUV420/YUV422
  - Max resolution: 8192x8192 source, 4096x4096 destination
  - Block transfer and Transparency mode
  - Color fill with gradient fill, and pattern fill
  - Alpha blending modes including global alpha, per pixel alpha (color/alpha channel separately) and fading
  - Arbitrary non-integer scaling ratio, from 1/8 to 8
  - 0, 90, 180, 270 degree rotation, x-mirror, y-mirror & rotation operation
  - ROP2, ROP3, ROP4
  - Support 4k/64k page size MMU
- Image Enhancement Processor
  - Image format
    - Input data: YUV420/YUV422, semi-planar/planar, UV swap
    - Output data: YUV420/YUV422, semi-planar, UV swap, Tile mode
    - YUV down sampling conversion from 422 to 420
    - Max resolution for dynamic image up to 1920x1080
  - De-interlace

### 1.2.8 Video Input Interface

- MIPI interface
  - Two MIPI DC(DPHY/CPHY) combo PHY
    - Support to use DPHY or CPHY
    - Each MIPI DPHY V2.0, 4lanes, 4.5Gbps per lane
    - Each MIPI CPHY V1.1, 3lanes, 2.5Gsps per lane
  - Four MIPI CSI DPHY
    - Each MIPI DPHY V1.2, 2lanes, 2.5Gbps per lane
    - Support to combine 2 DPHY together to one 4lanes
  - Support camera input combination:
    - 2 MIPI DCPHY + 4 MIPI CSI DPHY(2 lanes), totally support 6 cameras input
    - 2 MIPI DCPHY + 1 MIPI CSI DPHY(4 lanes) + 2 MIPI CSI DPHY(2 lanes), totally support 5 cameras input
    - 2 MIPI DCPHY + 2 MIPI CSI DPHY(4 lanes), totally support 4 cameras input
- DVP interface
  - One 8/10/12/16-bit standard DVP interface, up to 150MHz input data
  - Support BT.601/BT.656 and BT.1120 VI interface
  - Support the polarity of pixel_clk, hsync, vsync configurable
- HDMI RX interface
  - Single-port HDMI 2.0 RX PHY, 4 lanes, no sideband channels
  - Data rate support in HDMI 2.0 mode
    - 6Gbps down to 3.4Gbps
  - Data rate support in HDMI 1.4 mode
    - 3.4Gbps down to 250Mbps

- HDMI 2.0 video formats
  - TMDS Scrambler to enable support for 2160p@60 Hz with RGB/YCbCr4:4:4 or YCbCr4:2:2
  - Supports YCbCr 4:2:0 to enable 2160p@60Hz at lower HDMI link speeds
- HDMI 1.4b video formats
  - All CEA-861-E video formats up to 1080p@120Hz
  - HDMI 1.4b 4K x 2K video formats(3840x2160p@24Hz/25Hz/30Hz and 4096x2160p@24Hz)
  - HDMI 1.4b 3D video modes with up to 340 MHz(TMDS clock)
- Support HDCP2.3 and HDCP1.4

### 1.2.9 Image Signal Processor

- Video Capture(VICAP)
  - Support BT601, BT656, BT1120
  - Support receiving six interfaces of MIPI CSI/DSI, up to four IDs for each interface
  - Support five CSI data formats: RAW8/10/12/14, YUV422
  - Support three modes of HDR: virtual channel mode, identification code mode, line counter mode
  - Support RAW data through to ISP0/1
- Maximum input
  - 48M：8064x6048@15 dual ISP
  - 32M：6528x4898@30 dual ISP
  - 16M：4672x3504@30 single ISP
- 3A: include AE/Histogram, AF, AWB statistics output
- FPN: Fixed Pattern Noise removal
- BLC: Black Level Correction
- DPCC: Static/Dynamic defect pixel cluster correction
- PDAF: Phase Detection Auto Focus
- LSC: Lens shading correction
- Bayer-2DNR: Spatial Bayer-raw De-noising
- Bayer-3DNR: Temporal Bayer-raw De-noising
- CAC: Chromatic Aberration Correction
- HDR: 3-Frame Merge into High-Dynamic Range
- DRC: HDR Dynamic Range Compression, Tone mapping
- GIC: Green Imbalance Correction
- Debayer: Advanced Adaptive Demosaic with Chromatic Aberration Correction
- CCM/CSM: Color correction matrix; RGB2YUV etc
- Gamma: Gamma out correction
- Dehaze/Enhance: Automatic Dehaze and Effect enhancement
- 3DLUT: 3D-Lut Color Palette for Customer
- LDCH: Lens-distortion only in the horizontal direction
- YUV-2DNR: Spatial YUV De-noising
- Sharp: Image Sharpening and boundary filtering
- CMSK: privacy mask
- GAIN: image local gain
- Support multi-sensor reuse ISP
- FishEye Correction(FEC)
  - Input mode and data format
    - Support RASTER: YUV422SP, YUV422I, YUV420SP
  - Output mode and data format
    - RASTER: YUV422SP, YUV422I, YUV420SP
    - FBCE: YUV422SP, YUV420SP
  - Support 16x8, 32x16 two density
  - Support up to 4 times reduction factor
  - Resolution 128x128~4095x4095
  - Y Interpolation: Bicubic; C Interpolation: Biliner

### 1.2.10 Display interface

- HDMI/eDP TX interface
  - Support two HDMI/eDP TX combo interface, but HDMI and eDP can not work at the

same time for each interface
  - Support x1, x2 and x4 configuration for each interface
  - Support all the data rates for HDMI FRL: 3, 6, 8, 10 and 12Gbps
  - Support 1.62Gbps, 2.7Gbps and 5.4Gbps for eDP
  - Support up to 7680x4320@60Hz for HDMI TX, and 4K@60Hz for eDP
  - Support RGB/YUV(up to 10bit) format for HDMI TX
  - Support RGB, YCbCr 4:4:4, YCbCr 4:2:2 and 8/10 bit per component video format for eDP
  - Support DSC 1.2a for HDMI TX
  - Support HDCP2.3 for HDMI TX, and HDCP1.3 for eDP
- DP TX interface
  - Support 2 DP TX 1.4a interface which combo with USB3.1 Gen1
  - Support 1/2/4lanes for each interface
  - Support 1.62Gbps, 2.7Gbps, 5.4Gbps and 8.1Gbps Serializer
  - Support up to 7680x4320@30Hz
  - Support RGB/YUV(up to 10bit) format
  - Support Single Stream Transport(SST)
  - Support DP Alt mode on USB Type-C
  - Support HDCP2.3, HDCP 1.3
- MIPI DSI interface
  - Support 2 MIPI DPHY 2.0 or CPHY 1.1 interface
  - Support 4 data lanes and 4.5Gbps maximum data rate per lane for DPHY
  - Support 3 data trios and 2.0Gsps maximum data rate per trio for CPHY
  - Support max resolution 4K@60Hz
  - Support dual MIPI display: left-right mode
  - Support RGB(up to 10bit) format
  - Support DSC 1.1/1.2a
- BT.1120 video output interface
  - Support up to 1920x1080@60Hz
  - Support RGB(up to 8bit) format
  - Up to 150MHz data rate

### 1.2.11 Video Output Processor

- Video ports
  - Video Port0, max output resolution: 7680x4320@60Hz
  - Video Port1, max output resolution: 4096x4320@60Hz
  - Video Port2, max output resolution: 4096x4320@60Hz
  - Video Port3, max output resolution: 2048x1080@60Hz
- Cluster 0/1/2/3
  - Max input and output resolution 4096x4320
  - Support AFBCD
  - Support RGB/YUV/YUYV format
  - Support scale up/down ratio 4~1/4
  - Support rotation
- ESMART 0/1/2/3
  - Max input and output resolution 4096x4320
  - Support RGB/YUV/YUYV format
  - Support scale up/down ratio 8~1/8
  - Support 4 region
- Overlay
  - Support up to 8 layers overlay: 4 cluster/4 esmart
  - Support RGB/YUV domain overlay
- Post process
  - HDR
    - HDR10/HDR HLG
    - HDR2SDR/SDR2HDR
  - 3D-LUT/P2I/CSC/BCSH/DITHER/CABC/GAMMA/COLORBAR
- Write back
  - Format: ARGB8888/RGB888/RGB565/YUV420

- Max resolution: 1920x1080

### 1.2.12 Audio Interface

- I2S0/I2S1 with 8 channels
  - Up to 8 channels TX and 8 channels RX path
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal, left-justified, right-justified)
  - Support 4 PCM formats (early, late1, late2, late3)
  - Support TDM normal, 1/2 cycle left shift, 1 cycle left shift, 2 cycle left shift, right shift mode serial audio data transfer
  - I2S, PCM and TDM mode cannot be used at the same time
- I2S2/I2S3 with 2 channels
  - Up to 2 channels for TX and 2 channels RX path
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal, left-justified, right-justified)
  - Support 4 PCM formats (early, late1, late2, late3)
  - I2S and PCM cannot be used at the same time
- SPDIF0/SPDIF1
  - Support two 16-bit audio data store together in one 32-bit wide location
  - Support biphase format stereo audio data output
  - Support 16 to 31 bit audio data left or right justified in 32-bit wide sample data buffer
  - Support 16, 20, 24 bits audio data transfer in linear PCM mode
  - Support non-linear PCM transfer
- PDM0/PDM1
  - Up to 8 channels
  - Audio resolution from 16bits to 24bits
  - Sample rate up to 192KHz
  - Support PDM master receive mode
- Digital Audio Codec
  - Support 2 channels digital DAC
  - Support I2S/PCM interface, master and slave mode
  - Support 16 bit sample resolution
  - Support three modes of mixing for every digital DAC channel
  - Support volume control
- VAD(Voice Activity Detection)
  - Support read voice data from I2S/PDM
  - Support voice amplitude detection
  - Support Multi-Mic array data storing
  - Support a level combined interrupt

### 1.2.13 Connectivity

- SDIO interface
  - Compatible with SDIO3.0 protocol
  - 4-bit data bus widths
- GMAC 10/100/1000M Ethernet controller
  - Support two Ethernet controllers
  - Support 10/100/1000-Mbps data transfer rates with the RGMII interfaces
  - Support 10/100-Mbps data transfer rates with the RMII interfaces
  - Support both full-duplex and half-duplex operation
- USB3.1 Gen1
  - Support USB3.1 Gen1,equal to USB3.2 Gen1 and USB3.0,up to 5Gbps datarate
  - Embedded 2 USB3.1 OTG interfaces which combo with DP TX (USB3OTG_0 and USB3OTG_1)
  - Embedded 1 USB3.1 Host interface which combo with Combo PIPE PHY2 (USB3OTG_2)

- Compatible Specification
  - Universal Serial Bus 3.0 Specification, Revision 1.0
  - Universal Serial Bus Specification, Revision 2.0 (exclude USB3OTG_2)
  - eXtensible Host Controller Interface for Universal Serial Bus (xHCI), Revision 1.1
- Support Control/Bulk (including stream)/Interrupt/Isochronous Transfer
- Simultaneous IN and OUT transfer for USB3.1 Gen1
- Descriptor caching and data pre-fetching used to improve system performance in high-latency systems
- LPM protocol in USB 2.0 (exclude USB3OTG_2) and U0, U1, U2, and U3 states for USB3.1 Gen1
- USB3.1 Gen1 Device Features
  - Up to 10 IN endpoints, including control endpoint 0
  - Up to 6 OUT endpoints, including control endpoint 0
  - Up to 16 endpoint transfer resources, each one for each endpoint
  - Flexible endpoint configuration for multiple applications/USB set-configuration modes
  - Hardware handles ERDY and burst
  - Stream-based bulk endpoints with controller automatically initiating data movement
  - Isochronous endpoints with isochronous data in data buffers
  - Flexible Descriptor with rich set of features to support buffer interrupt moderation, multiple transfers, isochronous, control, and scattered buffering support
- USB3.1 Gen1 xHCI Host Features
  - Support up to 64 devices
  - Support 1 interrupter
  - Support 1 USB2.0 port (exclude USB3OTG_2) and 1 Super-Speed port
  - Support standard or open-source xHCI and class driver
- USB3.1 Gen1 Dual-Role Device (DRD) Features
  - Static Device Operation
  - Static Host Operation
  - USB3.1/USB2.0 OTG A device and B device basing on ID, USB3OTG_2 only support USB3.1 Gen1
  - Not Support USB3.1/USB2.0 OTG session request protocol (SRP), host negotiation protocol (HNP) and Role Swap Protocol (RSP)
- Miscellaneous Features
  - USB2.0 PHY support Battery Charge detection
  - USB3OTG_0 and USB3OTG_1 support USB Type-C and DP Alt Mode
  - USB3OTG_2 PHY combos with PCIE and SATA

- USB 2.0 Host
  - Compatible with USB 2.0 specification
  - Support two USB 2.0 Host
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Support Enhanced Host Controller Interface Specification (EHCI), Revision 1.0
  - Support Open Host Controller Interface Specification (OHCI), Revision 1.0a
- Combo PIPE PHY Interface
  - Support three Combo PIPE PHYs with PCIe2.1/SATA3.0/USB3.1 controller
  - Combo PIPE PHY0 support one of the following interfaces
    - SATA
    - PCIe2.1
  - Combo PIPE PHY1 support one of the following interfaces
    - SATA
    - PCIe2.1
  - Combo PIPE PHY2 support one of the following interfaces
    - SATA
    - PCIe2.1
    - USB3.1 Gen1

  - PCIe2.1 Interface
    - Compatible with PCI Express Base Specification Revision 2.1
    - Support 1 lane for each PCIe2.1 interface
    - Support Root Complex(RC) only
    - Support 5Gbps data rate
  - SATA Interface
    - Compatible with Serial ATA 3.1 and AHCI revision 1.3.1
    - Support eSATA
    - Support 1 port for each SATA interface
    - Support 6Gbps data rate
- PCIe3.0 Interface
  - Compatible with PCI Express Base Specification Revision 3.0
  - Support dual operation mode: Root Complex(RC) and End Point(EP)
  - Support data rates: 2.5Gbps(PCIe1.1), 5Gbps(PCIe2.1), 8Gps(PCIe3.0)
  - Support aggregation and bifurcation with 1x 4lanes, 2x 2lanes, 4x 1lanes and 1x 2lanes + 2x 1lanes
- SPI interface
  - Support 5 SPI Controllers(SPI0-SPI4)
  - Support two chip-select output
  - Support serial-master and serial-slave mode, software-configurable
- I2C Master controller
  - Support 9 I2C Master(I2C0-I2C8)
  - Support 7bits and 10bits address mode
  - Software programmable clock frequency
  - Data on the I2C-bus can be transferred at rates of up to 100k bits/s in the Standard-mode, up to 400k bits/s in the Fast-mode
- UART interface
  - Support 10 UART interfaces(UART0-UART9)
  - Embedded two 64-byte FIFO for TX and RX operation respectively
  - Support 5bit, 6bit, 7bit, 8bit serial data transmit or receive
  - Standard asynchronous communication bits such as start, stop and parity
  - Support different input clock for UART operation to get up to 4Mbps baud rate
  - Support auto flow control mode for all UART
- CAN Bus
  - Support 3 CAN buses
  - Support CAN 2.0B protocol
  - Support transmit or receive CAN standard frame
  - Support transmit or receive CAN extended frame
  - Support transmit or receive data frame, remote frame, overload frame, error frame and frame interval

### 1.2.14 Others

- Multiple group of GPIO
  - All of GPIOs can be used to generate interrupt
  - Support level trigger and edge trigger interrupt
  - Support configurable polarity of level trigger interrupt
  - Support configurable rising edge, falling edge and both edge trigger interrupt
  - Support configurable pull direction(a weak pull-up and a weak pull-down)
  - Support configurable drive strength
- Temperature Sensor (TS-ADC)
  - Support User-Defined Mode and Automatic Mode
  - In User-Defined Mode, start_of_conversion can be controlled completely by software, and also can be generated by hardware.
  - In Automatic Mode, the temperature of alarm(high/low temperature) interrupt can be configurable
  - In Automatic Mode, the temperature of system reset can be configurable
  - Support to 7 channel TS-ADC, the temperature criteria of each channel can be configurable
  - -40~125°C temperature range and 1°C temperature resolution

- Successive approximation ADC (SARADC)
  - 12-bit resolution
  - Up to 1MS/s sampling rate
  - 8 single-ended input channels
- OTP
  - Support 32Kbit space and higher 4k address space is non-secure part.
  - Support read and program word mask in secure model
  - Support maximum 32 bit OTP program operation
  - Support maximum 16 word OTP read operation
  - Program and Read state can be read
  - Program fail address record
- Package Type
  - FCBGA1088L (body: 23mm x 23mm; ball size: 0.36mm; ball pitch: 0.65mm)

## 1.3 Block Diagram

The following diagram shows the basic block diagram.

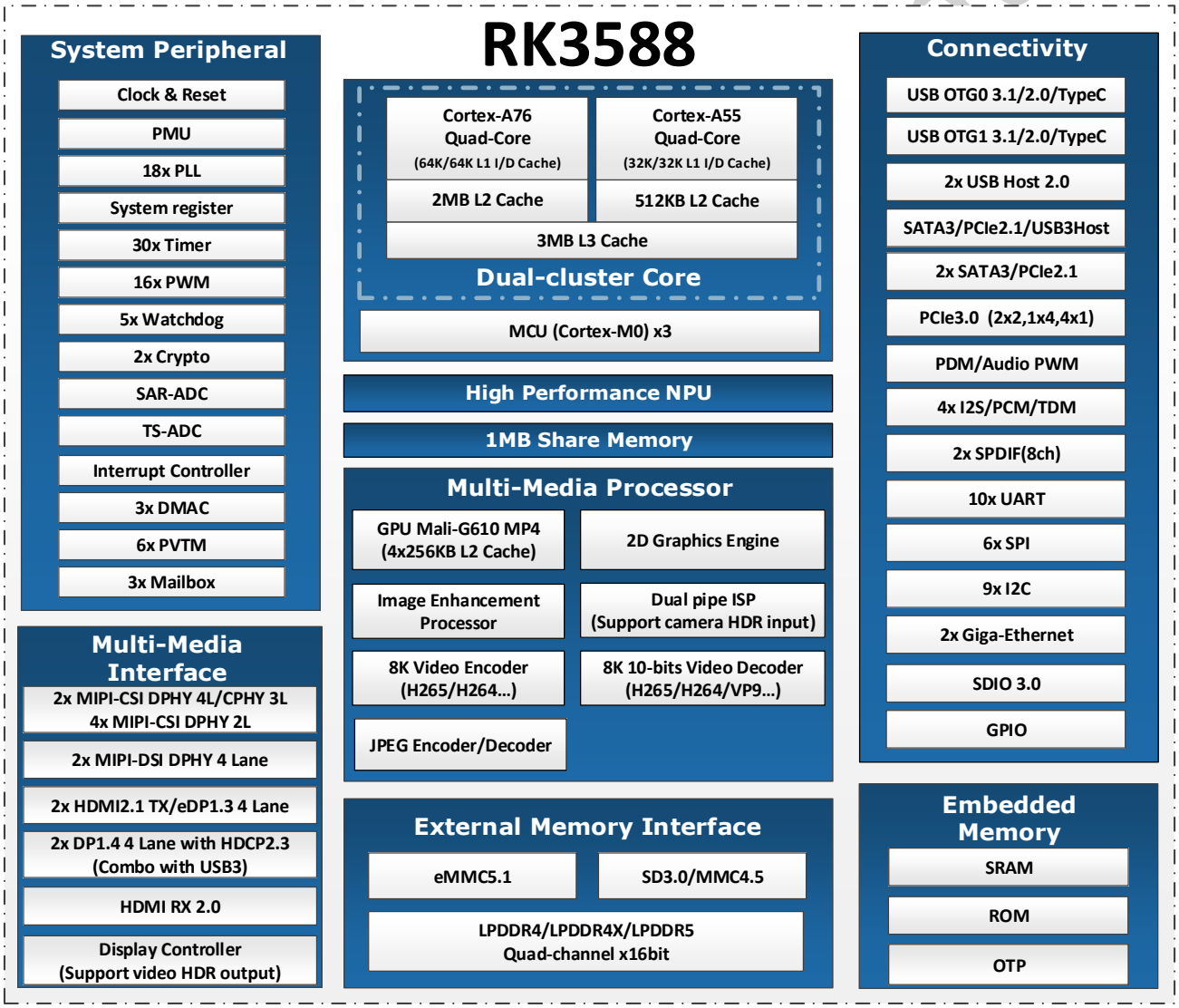


Fig. 1-1 Block Diagram

# Chapter 2 Package Information

## 2.1 Order Information

| Orderable Device | RoHS status | Package | Package QTY | Device Feature |
|---|---|---|---|---|
| RK3588 | RoHS | FCBGA1088L | 600PCS by tray | Application processor |

## 2.2 Top Marking

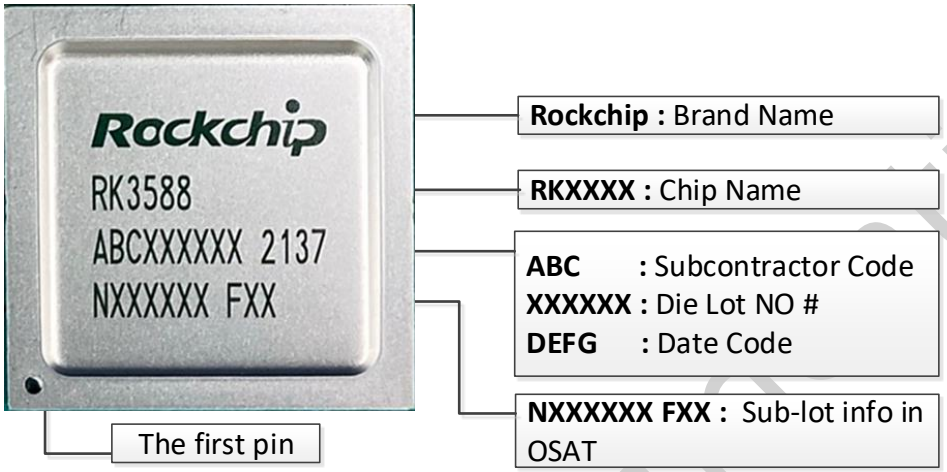


Fig. 2-1 Package definition

## 2.3 Package Dimension

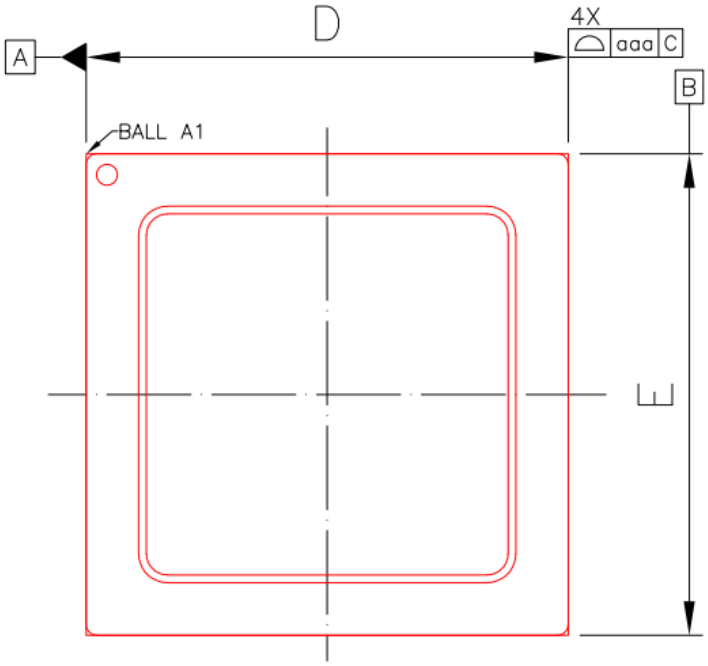


Fig. 2-2 Package Top View

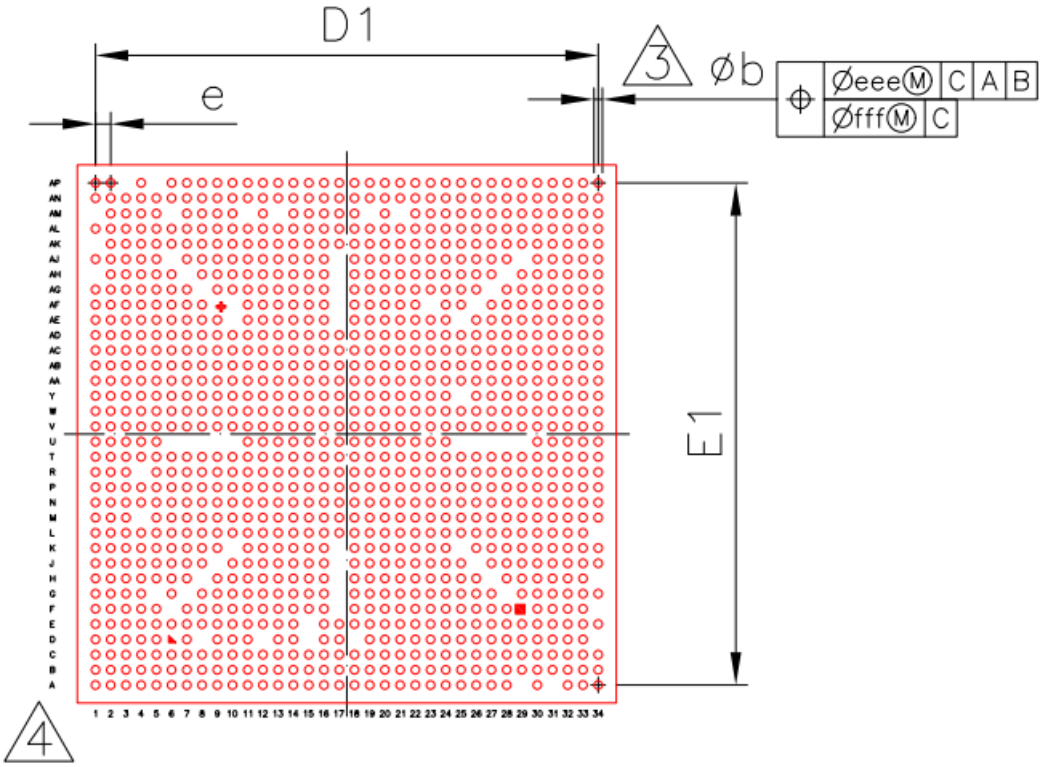


Fig. 2-3 Package Bottom View

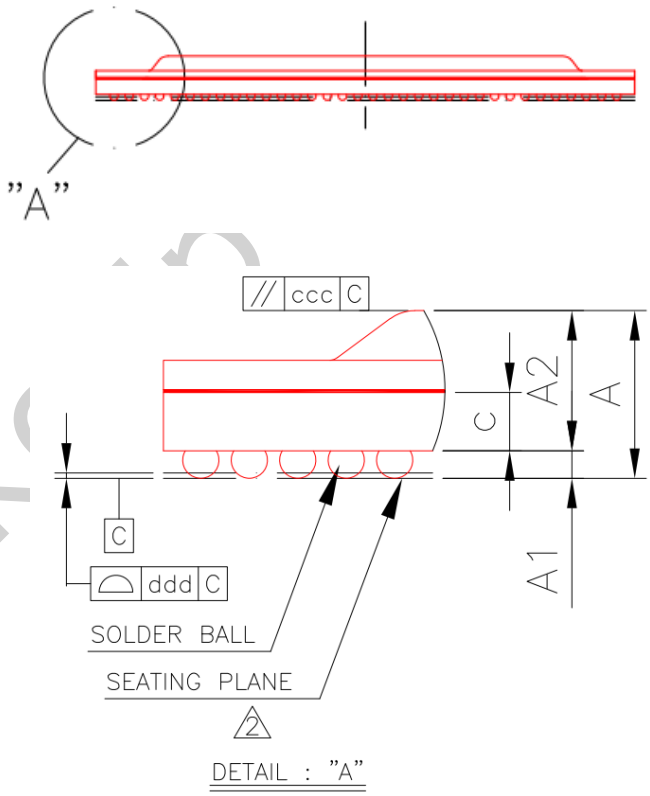


Fig. 2-4 Package Side View

| Symbol | Dimension in mm | | | Dimension in inch | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 1.727 | 1.885 | 2.043 | 0.068 | 0.074 | 0.080 |
| A1 | 0.20 | 0.25 | 0.30 | 0.008 | 0.010 | 0.012 |
| A2 | 1.485 | 1.635 | 1.785 | 0.058 | 0.064 | 0.070 |
| c | 0.56 | 0.66 | 0.76 | 0.022 | 0.026 | 0.030 |
| D | 22.90 | 23.00 | 23.15 | 0.902 | 0.906 | 0.911 |
| E | 22.90 | 23.00 | 23.15 | 0.902 | 0.906 | 0.911 |
| D1 | --- | 21.45 | --- | --- | 0.844 | --- |
| E1 | --- | 21.45 | --- | --- | 0.844 | --- |
| e | --- | 0.65 | --- | --- | 0.026 | --- |
| b | 0.31 | 0.36 | 0.41 | 0.012 | 0.014 | 0.016 |
| aaa | 0.20 | | | 0.008 | | |
| ccc | 0.35 | | | 0.014 | | |
| ddd | 0.15 | | | 0.006 | | |
| eee | 0.20 | | | 0.008 | | |
| fff | 0.08 | | | 0.003 | | |
| MD/ME | 34/34 | | | | | |

Fig. 2-5 Package Dimension

## 2.4 MSL Information

Moisture sensitivity Level ： MSL3

## 2.5 Lead Finish/Ball material Information

Lead Finish/Ball material ： SnAgCu

## 2.6 Pin Number List

Table 2-1 Pin Number Order Information

| Pin Name | Pin | Pin Name | Pin |
|---|---|---|---|
| VSS_1 | A1 | VSS_12 | C5 |
| DDR_CH1_DQ10_C | A2 | VSS_13 | C6 |
| DDR_CH1_DQ8_C | A3 | VSS_14 | C7 |
| DDR_CH1_DQ14_C | A4 | VSS_15 | C8 |
| DDR_CH1_DQ12_C | A5 | VSS_16 | C9 |
| DDR_CH1_DQ4_C | A6 | DDR_CH0_DQ15_B | D1 |
| DDR_CH1_DQ6_C | A7 | DDR_CH0_DQ8_B | D2 |
| DDR_CH1_DQ0_C | A8 | VSS_34 | D3 |
| DDR_CH1_DQ2_C | A9 | DDR_CH1_DM1_C | D4 |
| DDR_CH1_A4_C | A10 | DDR_CH1_DQS1N_C | D5 |
| VSS_2 | A11 | DDR_CH1_WCK1P_C | D7 |
| DDR_CH1_CKB_C | A12 | DDR_CH1_DQS0N_C | D9 |
| DDR_CH1_CKB_D | A13 | DDR_CH1_A6_C | D10 |
| VSS_3 | A14 | DDR_CH1_LP4/4X_CKE0/LP5_CS0_C | D11 |
| DDR_CH1_A4_D | A15 | DDR_CH1_A3_C | D13 |
| DDR_CH1_DQ2_D | A16 | DDR_CH1_A6_D | D14 |
| DDR_CH1_DQ0_D | A17 | DDR_CH1_LP4/4X_CKE0/LP5_CS0_D | D16 |
| DDR_CH1_DQ6_D | A18 | DDR_CH1_WCK0N_D | D17 |
| DDR_CH1_DQ4_D | A19 | DDR_CH1_LP4/4X_CS1_D | D19 |
| DDR_CH1_DQ12_D | A20 | DDR_CH1_DM0_D | D20 |
| DDR_CH1_DQ14_D | A21 | DDR_CH1_DQS1P_D | D21 |
| DDR_CH1_DQ8_D | A22 | DDR_CH1_DM1_D | D22 |
| DDR_CH1_DQ10_D | A23 | VSS_35 | D23 |
| PCIE30X1_1_CLKREQN_M2/DP0_HPDIN_M2/I2C2_SDA_M4/UART6_RX_M1/SPI4_MISO_M2/GPIO1_A0_d | A24 | VSS_36 | D24 |
| PCIE30X1_1_WAKEN_M2/DP1_HPDIN_M2/SATA1_ACT_LED_M1/I2C2_SCL_M4/UART6_TX_M1/SPI4_MOSI_M2/GPIO1_A1_d | A25 | PDM1_SDI2_M1/PCIE30X4_WAKEN_M3/SPI0_MISO_M2/GPIO1_B1_d | D25 |
| VOP_POST_EMPTY/I2C4_SDA_M3/UART6_RTSN_M1/PWM0_M2/SPI4_CLK_M2/GPIO1_A2_d | A26 | PDM1_SDI3_M1/PCIE30X4_PERSTN_M3/UART4_RX_M2/SPI0_MOSI_M2/GPIO1_B2_d | D26 |
| HDMI_TX1_SDA_M2/I2C4_SCL_M3/UART6_CTSN_M1/PWM1_M2/SPI4_CS0_M2/GPIO1_A3_d | A27 | PDM1_CLK1_M1/PCIE30X1_0_WAKEN_M2/SATA0_ACT_LED_M1/UART4_TX_M2/SPI0_CLK_M2/GPIO1_B3_d | D27 |
| PCIE30_PORT1_REF_CLKP | A28 | I2S0_SDI0/GPIO1_D4_d | D28 |
| PCIE30_PORT1_TX0N | A30 | PDM0_CLK0_M0/I2C4_SDA_M4/PWM15_IR_M2/GPIO1_C6_d | D29 |
| PCIE30_PORT1_RX0N | A32 | I2S0_LRCK/I2C2_SCL_M3/UART4_RTSN/GPIO1_C5_d | D30 |
| PCIE30_PORT1_RESREF | A33 | VSS_37 | D31 |
| VSS_4 | A34 | PCIE30_PORT0_TX0P | D32 |
| DDR_CH0_DQ14_A | AA1 | PCIE30_PORT0_TX0N | D33 |
| DDR_CH0_DQ15_A | AA2 | DDR_CH0_DQ13_B | E1 |

| Pin Name | Pin | Pin Name | Pin |
|---|---|---|---|
| VSS_248 | AA3 | DDR_CH0_DQ14_B | E2 |
| DDR_CH0_DQS1N_A | AA4 | VSS_38 | E3 |
| DDR_CH0_DQS1P_A | AA5 | DDR_CH0_DM1_B | E4 |
| VSS_249 | AA6 | DDR_CH1_DQS1P_C | E5 |
| VCCIO2_1V8 | AA7 | VSS_39 | E6 |
| AVSS_15 | AA8 | DDR_CH1_WCK1N_C | E7 |
| HDMI/eDP_TX0_VDD_0V75 | AA9 | VSS_40 | E8 |
| AVSS_16 | AA10 | DDR_CH1_DQS0P_C | E9 |
| VSS_250 | AA11 | DDR_CH1_RESET_C | E10 |
| VDD_GPU_MEM_0 | AA12 | DDR_CH1_LP4/4X_CKE1/LP5_CS1_C | E11 |
| VDD_GPU_0 | AA13 | VSS_41 | E12 |
| VDD_GPU_7 | AA14 | DDR_CH1_A2_C | E13 |
| VDD_GPU_11 | AA15 | DDR_CH1_A3_D | E14 |
| VSS_251 | AA16 | DDR_CH1_LP4/4X_CKE1/LP5_CS1_D | E16 |
| VSS_252 | AA17 | DDR_CH1_WCK0P_D | E17 |
| VSS_253 | AA18 | VSS_42 | E18 |
| VSS_254 | AA19 | DDR_CH1_LP4/4X_CS0_D | E19 |
| VSS_255 | AA20 | VSS_43 | E20 |
| VSS_256 | AA21 | DDR_CH1_DQS1N_D | E21 |
| VSS_257 | AA22 | VSS_44 | E22 |
| VSS_258 | AA23 | VSS_45 | E23 |
| VSS_259 | AA24 | PDM1_CLK0_M1/PCIE30X1_0_PERSTN_M2/UART7_RX_M2/SPI0_CS0_M2/GPIO1_B4_u | E24 |
| MIPI_CSI1_AVCC0V75 | AA25 | PCIE30X1_0_CLKREQN_M2/UART7_TX_M2/SPI0_CS1_M2/GPIO1_B5_u | E25 |
| MIPI_CSI1_AVCC1V8 | AA26 | MIPI_CAMERA1_CLK_M0/SPDIF0_TX_M0/PCIE30X2_WAKEN_M3/HDMI_RX_HPDIN_M2/I2C5_SCL_M3/UART1_TX_M1/GPIO1_B6_d | E26 |
| HDMI_TX0_HPD_M1/PCIE30X2_PERSTN_M2/HDMI_RX_HPDIN_M1/MCU_JTAG_TCK_M1/UART9_RX_M2/SPI0_CS0_M3/GPIO3_D4_d | AA27 | MIPI_CAMERA2_CLK_M0/SPDIF1_TX_M0/PCIE30X2_PERSTN_M3/HDMI_RX_CEC_M2/SATA2_ACT_LED_M1/I2C5_SDA_M3/UART1_RX_M1/PWM13_M2/GPIO1_B7_u | E27 |
| GMAC1_PTP_REF_CLK/HDMI_TX1_HPD_M1/I2C3_SCL_M1/SPI1_MOSI_M1/GPIO3_B7_d | AA28 | I2S0_SDI1/PDM0_SDI3_M0/I2C1_SDA_M4/UART4_RX_M0/PWM1_M1/SPI1_CS0_M2/GPIO1_D3_d | E28 |
| GMAC1_TXD2/SDIO_D0_M1/I2S3_MCLK/FSPI_D0_M2/I2C6_SDA_M4/PWM10_M0/SPI4_MISO_M1/GPIO3_A0_u | AA29 | I2S0_SDO0/I2C4_SCL_M4/UART4_CTSN/GPIO1_C7_d | E29 |
| GMAC1_TXD3/SDIO_D1_M1/I2S3_SCLK/AUDDSM_LN/FSPI_D1_M2/I2C6_SCL_M4/PWM11_IR_M0/SPI4_MOSI_M1/GPIO3_A1_u | AA30 | PDM0_CLK1_M0/I2C2_SDA_M3/PWM11_IR_M2/SPI4_CS1_M0/GPIO1_C4_d | E30 |
| VSS_260 | AA31 | I2S0_SCLK/I2C6_SCL_M1/UART3_CTSN/PWM7_IR_M2/SPI4_CS0_M0/GPIO1_C3_d | E31 |
| EMMC_D5/I2C1_SDA_M3/UART5_TX_M2/GPIO2_D5_u | AA32 | VSS_46 | E32 |
| EMMC_D3/FSPI_D3_M0/GPIO2_D3_u | AA33 | PCIE30_PORT0_REF_CLKP | E33 |
| EMMC_RSTN/I2C2_SCL_M2/UART5_RTSN_M1/GPIO2_A3_d | AA34 | PCIE30_PORT0_REF_CLKN | E34 |
| DDR_CH0_DQ9_A | AB1 | DDR_CH0_DQ4_B | F1 |
| DDR_CH0_DQ8_A | AB2 | DDR_CH0_DQ12_B | F2 |
| VSS_261 | AB3 | VSS_47 | F3 |
| DDR_CH0_DM1_A | AB4 | DDR_CH0_DQS1N_B | F4 |
| VSS_262 | AB5 | DDR_CH0_DQS1P_B | F5 |
| AVSS_17 | AB6 | VSS_48 | F7 |
| AVSS_18 | AB7 | DDR_CH1_DM0_C | F8 |
| AVSS_19 | AB8 | VSS_49 | F9 |
| HDMI/eDP_TX0_AVDD_0V75 | AB9 | VSS_50 | F10 |
| AVSS_20 | AB10 | VSS_51 | F11 |
| VSS_263 | AB11 | DDR_CH1_A1_C | F12 |
| VDD_GPU_MEM_1 | AB12 | VSS_52 | F13 |
| VDD_GPU_1 | AB13 | VSS_53 | F14 |
| VDD_GPU_6 | AB14 | VSS_54 | F15 |
| VDD_GPU_10 | AB15 | VSS_55 | F16 |
| VSS_264 | AB16 | DDR_CH1_ZQ_D | F18 |
| VSS_265 | AB17 | VSS_56 | F19 |
| VSS_266 | AB18 | VSS_57 | F20 |
| VSS_267 | AB19 | VSS_58 | F21 |
| VSS_268 | AB20 | VSS_59 | F22 |
| VDD_NPU_6 | AB21 | VSS_60 | F23 |
| VDD_NPU_5 | AB22 | MIPI_CAMERA3_CLK_M0/HDMI_RX_SCL_M2/I2C8_SCL_M2/UART1_RTSN_M1/PWM14_M2/GPIO1_D6_u | F24 |
| VDD_NPU_2 | AB23 | MIPI_CAMERA4_CLK_M0/PCIE30X2_CLKREQN_M3/HDMI_RX_SDA_M2/I2C8_SDA_M2/UART1_CTSN_M1/PWM15_IR_M3/GPIO1_D7_u | F25 |
| VSS_269 | AB24 | I2S0_SDO1/I2C7_SCL_M0/UART6_TX_M2/SPI1_MISO_M2/GPIO1_D0_d | F26 |
| MIPI_CSI0_AVCC0V75 | AB25 | I2S0_SDO2/I2S0_SDI3/PDM0_SDI1_M0/I2C7_SDA_M0/UART6_RX_M2/SPI1_MOSI_M2/GPIO1_D1_d | F27 |
| MIPI_CSI0_AVCC1V8 | AB26 | I2S0_SDO3/I2S0_SDI2/PDM0_SDI2_M0/I2C1_SCL_M4/UART4_TX_M0/PWM0_M1/SPI1_CLK_M2/GPIO1_D2_d | F28 |
| VSS_270 | AB27 | I2S0_MCLK/I2C6_SDA_M1/UART3_RTSN/PWM3_IR_M2/SPI4_CLK_M0/GPIO1_C2__d | F30 |
| PCIE30X4_BUTTON_RSTN/DP1_HPDIN_M0/MCU_JTAG_TMS_M1/UART9_TX_M2/PWM11_IR_M3/SPI0_CS1_M3/GPIO3_D5_d | AB28 | VSS_61 | F31 |
| VSS_271 | AB29 | PCIE30_PORT0_RX1P | F32 |
| GMAC0_PPSTRING/FSPI_CS1N_M1/HDMI_TX1_SCL_M0/I2C4_SCL_M1/UART7_TX_M0/GPIO2_B5_u | AB30 | PCIE30_PORT0_RX1N | F33 |
| GMAC0_PTP_REFCLK/FSPI_CS0N_M1/HDMI_TX1_SDA_M0/I2C4_SDA_M1/UART7_RX_M0/GPIO2_B4_u | AB31 | DDR_CH0_DQ6_B | G1 |
| VSS_272 | AB32 | DDR_CH0_DQ5_B | G2 |
| GMAC0_MDIO/I2C0_SCL_M1/UART9_CTSN_M0/PWM6_M2/SPI3_MOSI_M0/GPIO4_C5_d | AB33 | VSS_62 | G3 |
| GMAC0_MDC/I2C7_SDA_M1/UART9_RTSN_M0/PWM5_M2/SPI3_MISO_M0/GPIO4_C4_d | AB34 | DDR_CH0_DM0_B | G4 |

| Pin Name | Pin | Pin Name | Pin |
|---|---|---|---|
| DDR_CH0_DQ10_A | AC1 | VSS_63 | G6 |
| DDR_CH0_DQ11_A | AC2 | DDR_CH1_ZQ_C | G8 |
| VSS_273 | AC3 | DDR_CH1_WCK0P_C | G9 |
| VSS_274 | AC4 | VSS_64 | G10 |
| AVSS_21 | AC5 | DDR_CH1_LP4/4X_CS0_C | G11 |
| HDMI/eDP_TX0_VDD_CMN_1V8 | AC6 | DDR_CH1_A0_C | G12 |
| HDMI/eDP_TX0_VDD_IO_1V8 | AC7 | DDR_CH1_A2_D | G13 |
| AVSS_22 | AC8 | DDR_CH1_A1_D | G14 |
| HDMI/eDP_TX1_AVDD_0V75 | AC9 | VSS_65 | G15 |
| AVSS_23 | AC10 | DDR_CH1_DQS0N_D | G16 |
| VSS_275 | AC11 | DDR_CH1_WCK1N_D | G18 |
| VSS_276 | AC12 | VSS_66 | G19 |
| VDD_GPU_2 | AC13 | VCCIO1_1V8 | G20 |
| VDD_GPU_5 | AC14 | VSS_67 | G21 |
| VDD_GPU_9 | AC15 | VSS_68 | G22 |
| VSS_277 | AC16 | PCIE30_PORT0_AVDD1V8 | G23 |
| VDD_LOGIC_5 | AC17 | PCIE30_PORT0_AVDD0V75 | G24 |
| VDD_LOGIC_4 | AC18 | VSS_69 | G25 |
| VDD_LOGIC_3 | AC19 | PDM0_SDI0_M0/SPI1_CS1_M2/GPIO1_D5_d | G26 |
| VSS_278 | AC20 | I2C3_SCL_M0/UART3_TX_M0/SPI4_MOSI_M0/GPIO1_C1_z | G27 |
| VSS_279 | AC21 | I2C3_SDA_M0/UART3_RX_M0/SPI4_MISO_M0/GPIO1_C0_z | G29 |
| VDD_NPU_4 | AC22 | PCIE20_2_REFCLKN | G30 |
| VDD_NPU_1 | AC23 | PCIE20_2_REFCLKP | G31 |
| VSS_280 | AC24 | VSS_70 | G32 |
| VCCIO6_1V8 | AC25 | PCIE30_PORT0_RX0P | G33 |
| VCCIO6 | AC26 | PCIE30_PORT0_RX0N | G34 |
| VSS_281 | AC27 | DDR_CH0_DQ0_B | H1 |
| GMAC1_TXD0/I2S2_SDO_M1/UART2_RTSN/GPIO3_B3_u | AC28 | DDR_CH0_DQ7_B | H2 |
| GMAC1_TXD1/I2S2_MCLK_M1/UART2_CTSN/GPIO3_B4_u | AC29 | VSS_71 | H3 |
| GMAC0_PPSCLK/TEST_CLKOUT_M1/HDMI_TX1_CEC_M0/UART9_RX_M0/SPI1_CS1_M0/GPIO2_C4_d | AC30 | DDR_CH0_WCK1P_B | H4 |
| GMAC0_RXD3/SDIO_D1_M0/FSPI_D1_M1/UART6_TX_M0/GPIO2_A7_u | AC31 | DDR_CH0_WCK1N_B | H5 |
| GMAC0_RXD2/SDIO_D0_M0/FSPI_D0_M1/UART6_RX_M0/GPIO2_A6_u | AC32 | VSS_72 | H6 |
| GMAC0_TXD2/SDIO_D3_M0/FSPI_D3_M1/I2C8_SDA_M1/UART6_CTSN_M0/GPIO2_B1_u | AC33 | DDR_CH0_ZQ_B | H7 |
| GMAC0_TXD3/SDIO_CMD_M0/I2C3_SCL_M3/GPIO2_B2_u | AC34 | DDR_CH1_WCK0N_C | H9 |
| SDMMC_D1/PDM1_SDI2_M0/JTAG_TMS_M1/I2C3_SDA_M4/UART2_RX_M1/PWM9_M1/GPIO4_D1_u | AD1 | VSS_73 | H10 |
| SDMMC_D0/PDM1_SDI3_M0/JTAG_TCK_M1/I2C3_SCL_M4/UART2_TX_M1/PWM8_M1/GPIO4_D0_u | AD2 | DDR_CH1_LP4/4X_CS1_C | H11 |
| OTP_VDDOTP_0V75 | AD3 | VSS_74 | H12 |
| NC | AD4 | DDR_CH1_VDDQ_CKE | H13 |
| AVSS_24 | AD5 | VSS_75 | H14 |
| HDMI/eDP_TX1_VDD_CMN_1V8 | AD6 | DDR_CH1_A0_D | H15 |
| HDMI/eDP_TX1_VDD_IO_1V8 | AD7 | DDR_CH1_DQS0P_D | H16 |
| AVSS_25 | AD8 | DDR_CH1_WCK1P_D | H18 |
| HDMI/eDP_TX1_VDD_0V75 | AD9 | VSS_76 | H19 |
| AVSS_26 | AD10 | VCCIO4_1V8 | H20 |
| VSS_282 | AD11 | VCCIO4 | H21 |
| VSS_283 | AD12 | VSS_77 | H22 |
| VDD_GPU_3 | AD13 | PCIE30_PORT1_AVDD1V8 | H23 |
| VDD_GPU_4 | AD14 | PCIE30_PORT1_AVDD0V75 | H24 |
| VDD_GPU_8 | AD15 | VSS_78 | H25 |
| VSS_284 | AD16 | VSS_79 | H26 |
| VDD_LOGIC_0 | AD17 | AVSS_1 | H28 |
| VDD_LOGIC_1 | AD18 | PCIE20_2_TXN/SATA30_2_TXN/USB30_SSTXN | H29 |
| VDD_LOGIC_2 | AD19 | PCIE20_2_TXP/SATA30_2_TXP/USB30_SSTXP | H30 |
| VSS_285 | AD20 | AVSS_2 | H31 |
| VSS_286 | AD21 | PCIE20_1_REFCLKP | H32 |
| VDD_NPU_3 | AD22 | PCIE20_1_REFCLKN | H33 |
| VDD_NPU_0 | AD23 | DDR_CH0_DQ2_B | J1 |
| VSS_287 | AD24 | DDR_CH0_DQ1_B | J2 |
| VSS_288 | AD25 | VSS_80 | J3 |
| VSS_289 | AD26 | VSS_81 | J4 |
| GMAC1_RXD2/SDIO_D2_M1/I2S3_LRCK/AUDDSM_LP/FSPI_D2_M2/UART8_TX_M1/SPI4_CLK_M1/GPIO3_A2_u | AD27 | VSS_82 | J5 |
| GMAC1_TXCLK/SDIO_CMD_M1/I2S3_SDI/AUDDSM_RP/UART8_RTSN_M1/SPI4_CS1_M1/GPIO3_A4_d | AD28 | VSS_83 | J6 |
| GMAC1_TXEN/I2S2_SCLK_M1/CAN1_RX_M0/UART3_TX_M1/PWM12_M0/GPIO3_B5_u | AD29 | DDR_CH0_DQS0N_B | J7 |
| ETH0_REFCLKO_25M/I2S2_SDI_M0/I2C6_SCL_M2/SPI1_CS0_M0/GPIO2_C3_d | AD30 | DDR_CH0_DQS0P_B | J8 |
| GMAC0_RXD1/I2C6_SDA_M2/UART9_TX_M0/SPI1_MOSI_M0/GPIO2_C2_d | AD31 | VSS_84 | J10 |
| GMAC0_RXD0/I2C2_SCL_M1/UART1_CTSN_M0/SPI1_MISO_M0/GPIO2_C1_d | AD32 | VSS_85 | J11 |
| GMAC0_TXD0/I2S2_MCLK_M0/I2C5_SCL_M4/UART1_RX_M0/GPIO2_B6_d | AD33 | VSS_86 | J12 |
| GMAC0_TXD1/I2S2_SCLK_M0/I2C5_SDA_M4/UART1_TX_M0/GPIO2_B7_d | AD34 | VSS_87 | J13 |
| SDMMC_CLK/PDM1_CLK0_M0/TEST_CLKOUT_M0/MCU_JTAG_TMS_M0/CAN0_RX_M1/UART5_TX_M0/GPIO4_D5_d | AE1 | VSS_88 | J14 |
| SDMMC_CMD/PDM1_CLK1_M0/MCU_JTAG_TCK_M0/CAN0_TX_M1/UART5_RX_M0/PWM7_IR_M1/GPIO4_D4_u | AE2 | VSS_89 | J15 |

| Pin Name | Pin | Pin Name | Pin |
|---|---|---|---|
| VSS_290 | AE3 | VSS_90 | J16 |
| HDMI_RX_VPH3V3 | AE4 | VSS_91 | J18 |
| HDMI_RX_DVDD3V3 | AE5 | VSS_92 | J19 |
| AVSS_27 | AE6 | VSS_93 | J20 |
| AVSS_28 | AE7 | VSS_94 | J21 |
| HDMI_RX_AVDD0V75 | AE8 | VSS_95 | J22 |
| AVSS_29 | AE9 | VSS_96 | J23 |
| VSS_291 | AE11 | VSS_97 | J24 |
| VSS_292 | AE12 | VSS_98 | J25 |
| VSS_293 | AE13 | AVSS_3 | J27 |
| VSS_294 | AE14 | AVSS_4 | J28 |
| VSS_295 | AE15 | AVSS_5 | J29 |
| VSS_296 | AE16 | PCIE20_2_RXN/SATA30_2_RXN/USB30_SSRXN | J30 |
| VSS_297 | AE18 | PCIE20_2_RXP/SATA30_2_RXP/USB30_SSRXP | J31 |
| VSS_298 | AE19 | AVSS_6 | J32 |
| VSS_299 | AE20 | PCIE20_1_RXP/SATA30_1_RXP | J33 |
| VSS_300 | AE21 | PCIE20_1_RXN/SATA30_1_RXN | J34 |
| VDD_NPU_MEM_0 | AE22 | DDR_CH0_A4_B | K1 |
| VDD_NPU_MEM_1 | AE23 | DDR_CH0_DQ3_B | K2 |
| VSS_301 | AE24 | VSS_99 | K3 |
| VSS_302 | AE26 | DDR_CH0_WCK0N_B | K4 |
| GMAC1_RXD3/SDIO_D3_M1/I2S3_SDO/AUDDSM_RN/FSPI_D3_M2/UART8_RX_M1/SPI4_CS0_M1/GPIO3_A3_u | AE27 | DDR_CH0_WCK0P_B | K5 |
| GMAC1_TXER/I2S2_SDI_M1/UART2_RX_M2/PWM3_IR_M1/GPIO3_B2_d | AE28 | VSS_100 | K6 |
| GMAC1_MCLKINOUT/I2S2_LRCK_M1/CAN1_TX_M0/UART3_RX_M1/PWM13_M0/GPIO3_B6_d | AE29 | DDR_CH0_RESET_B | K7 |
| CLK32K_OUT1/GPIO2_C5_d | AE30 | VSS_101 | K8 |
| GMAC0_RXDV_CRS/UART7_RTSN_M0/PWM2_M2/SPI3_CS0_M0/GPIO4_C2_d | AE31 | VSS_102 | K9 |
| GMAC0_RXCLK/SDIO_D2_M0/FSPI_D2_M1/I2C8_SCL_M1/UART6_RTSN_M0/GPIO2_B0_u | AE32 | DDR_CH1_VDDQ_0 | K11 |
| GMAC0_TXCLK/SDIO_CLK_M0/FSPI_CLK_M1/I2C3_SDA_M3/GPIO2_B3_d | AE33 | DDR_CH1_VDDQ_1 | K12 |
| GMAC0_TXEN/I2S2_LRCK_M0/I2C2_SDA_M1/UART1_RTSN_M0/SPI1_CLK_M0/GPIO2_C0_d | AE34 | DDR_CH1_VDDQ_2 | K13 |
| SDMMC_D3/PDM1_SDI0_M0/JTAG_TMS_M0/I2C8_SDA_M0/UART5_RTSN_M0/PWM10_M1/GPIO4_D3_u | AF1 | DDR_CH1_VDDQ_3 | K14 |
| SDMMC_D2/PDM1_SDI1_M0/JTAG_TCK_M0/I2C8_SCL_M0/UART5_CTSN_M0/GPIO4_D2_u | AF2 | DDR_CH1_VDDQ_4 | K15 |
| HDMI_RX_REXT | AF3 | DDR_CH1_PLL_AVDD1V8 | K16 |
| AVSS_30 | AF4 | VSS_103 | K18 |
| HDMI_RX_CLKN | AF5 | VDD_LOGIC_8 | K19 |
| HDMI_RX_CLKP | AF6 | VDD_LOGIC_9 | K20 |
| AVSS_31 | AF7 | VSS_104 | K21 |
| AVSS_32 | AF8 | VSS_105 | K22 |
| AVSS_33 | AF11 | VDD_CPU_BIG1_9 | K23 |
| AVSS_34 | AF12 | VDD_CPU_BIG1_0 | K24 |
| AVSS_35 | AF13 | AVSS_7 | K26 |
| AVSS_36 | AF14 | PCIE20_SATA30_USB30_2_AVDD_1V8 | K27 |
| AVSS_37 | AF15 | PCIE20_SATA30_USB30_2_AVDD_0V85 | K28 |
| AVSS_38 | AF16 | CLK32K_IN/CLK32K_OUT0/GPIO0_B2_u | K29 |
| TSADC_TEST_OUT_TS | AF18 | SPI2_CS0_M2/I2C1_SDA_M1/PWM5_M0/UART0_TX_M1/GPIO0_B1_z | K30 |
| MIPI_D/C_PHY1_VREG | AF19 | AVSS_8 | K31 |
| MIPI_D/C_PHY0_VREG | AF20 | AVSS_9 | K32 |
| AVSS_39 | AF21 | PCIE20_1_TXP/SATA30_1_TXP | K33 |
| VSS_303 | AF22 | PCIE20_1_TXN/SATA30_1_TXN | K34 |
| VSS_304 | AF24 | VSS_106 | L1 |
| VSS_305 | AF25 | DDR_CH0_A5_B | L2 |
| VSS_306 | AF27 | VSS_107 | L3 |
| VSS_307 | AF28 | DDR_CH0_LP4/4X_CKE1/LP5_CS1_B | L4 |
| VSS_308 | AF29 | DDR_CH0_LP4/4X_CKE0/LP5_CS0_B | L5 |
| VSS_309 | AF30 | VSS_108 | L6 |
| VSS_310 | AF31 | DDR_CH0_LP4/4X_CS0_B | L7 |
| VSS_311 | AF32 | DDR_CH0_LP4/4X_CS1_B | L8 |
| GMAC0_TXER/I2C0_SDA_M1/UART7_CTSN_M0/PWM7_IR_M3/SPI3_CLK_M0/GPIO4_C6_d | AF33 | VSS_109 | L9 |
| GMAC0_MCLKINOUT/I2S2_SDO_M0/I2C7_SCL_M1/PWM4_M1/SPI3_CS1_M0/GPIO4_C3_d | AF34 | DDR_CH0_VDDQ_CK | L10 |
| HDMI_TX0_SBDN/eDP_TX0_AUXN | AG1 | DDR_CH1_VDD_0 | L11 |
| HDMI_TX0_SBDP/eDP_TX0_AUXP | AG2 | DDR_CH1_VDD_1 | L12 |
| AVSS_40 | AG3 | DDR_CH1_VDD_2 | L13 |
| HDMI_RX_D0N | AG4 | DDR_CH1_VDD_3 | L14 |
| HDMI_RX_D0P | AG5 | DDR_CH1_PLL_DVDD | L15 |
| AVSS_41 | AG6 | DDR_CH1_PLL_AVSS | L16 |
| AVSS_42 | AG7 | DDR_CH1_VDD_MIF_0 | L17 |
| USB20_HOST0_REXT | AG9 | DDR_CH1_VDD_MIF_1 | L18 |
| AVSS_43 | AG10 | VSS_110 | L19 |
| USB20_AVDD_1V8 | AG11 | VSS_111 | L20 |
| AVSS_44 | AG12 | VSS_112 | L21 |
| TYPEC1_DP1_VDDH_1V8 | AG13 | VSS_113 | L22 |
| TYPEC0_DP0_VDDH_1V8 | AG14 | VDD_CPU_BIG1_8 | L23 |
| AVSS_45 | AG15 | VDD_CPU_BIG1_1 | L24 |
| TYPEC1_DP1_REXT | AG16 | VSS_114 | L25 |
| AVSS_46 | AG18 | AVSS_10 | L26 |
| MIPI_D/C_PHY1_VDD | AG19 | PCIE20_SATA30_1_AVDD_1V8 | L27 |
| MIPI_D/C_PHY0_VDD | AG20 | PCIE20_SATA30_1_AVDD_0V85 | L28 |

| Pin Name | Pin | Pin Name | Pin |
|---|---|---|---|
| AVSS_47 | AG21 | SPI2_MISO_M2/I2C0_SCL_M0/GPIO0_B3_z | L29 |
| AVSS_48 | AG22 | SPI2_CS1_M2/I2C1_SCL_M1/UART0_RX_M1/GPIO0_B0_z | L30 |
| CIF_D13/PCIE20X1_2_PERSTN_M0/HDMI_RX_CEC_M1/UART4_TX_M1/PWM9_M2/SPI0_MISO_M3/GPIO3_D1_d | AG23 | AVSS_11 | L31 |
| CIF_D15/PCIE30X2_WAKEN_M2/HDMI_RX_SDA_M1/I2C7_SDA_M2/UART9_CTSN_M2/PWM10_M2/SPI0_CLK_M3/GPIO3_D3_d | AG24 | PCIE20_0_REFCLKP | L32 |
| CIF_D14/PCIE30X2_CLKREQN_M2/HDMI_RX_SCL_M1/I2C7_SCL_M2/UART9_RTSN_M2/SPI0_MOSI_M3/GPIO3_D2_d | AG25 | PCIE20_0_REFCLKN | L33 |
| CIF_D10/PCIE30X4_PERSTN_M2/HDMI_TX1_SCL_M1/SPI3_MISO_M3/GPIO3_C6_u | AG26 | DDR_CH0_CKB_B | M1 |
| GMAC1_RXD1/MIPI_CAMERA3_CLK_M1/PWM9_M0/GPIO3_B0_u | AG28 | DDR_CH0_CK_B | M2 |
| GMAC1_RXD0/MIPI_CAMERA2_CLK_M1/PWM8_M0/GPIO3_A7_u | AG29 | VSS_115 | M3 |
| VSS_312 | AG30 | DDR_CH0_A1_B | M5 |
| MIPI_CSI1_D0P | AG31 | VSS_116 | M6 |
| MIPI_CSI1_D0N | AG32 | DDR_CH0_A6_B | M7 |
| MIPI_CSI0_D0P | AG33 | DDR_CH0_A0_B | M8 |
| MIPI_CSI0_D0N | AG34 | VSS_117 | M9 |
| HDMI_TX0_D3N/eDP_TX0_D3N | AH2 | DDR_CH0_VDDQ_0 | M10 |
| HDMI_TX0_D3P/eDP_TX0_D3P | AH3 | DDR_CH0_PLL_AVSS | M11 |
| AVSS_49 | AH4 | DDR_CH0_PLL_AVDD1V8 | M12 |
| HDMI_RX_D1N | AH5 | DDR_CH1_VDDQ_CK | M13 |
| HDMI_RX_D1P | AH6 | VSS_118 | M14 |
| AVSS_50 | AH8 | VSS_119 | M15 |
| USB20_HOST1_REXT | AH9 | VDD_CPU_BIG0_0 | M16 |
| USB20_DVDD_0V75 | AH10 | VDD_CPU_BIG0_9 | M17 |
| AVSS_51 | AH11 | VSS_120 | M18 |
| AVSS_52 | AH12 | VDD_CPU_BIG0_MEM_0 | M19 |
| TYPEC1_DP1_VDD_0V85 | AH13 | VSS_121 | M20 |
| TYPEC0_DP0_VDDA_0V85 | AH14 | VDD_CPU_BIG1_MEM_0 | M21 |
| AVSS_53 | AH15 | VSS_122 | M22 |
| TYPEC0_DP0_REXT | AH16 | VDD_CPU_BIG1_7 | M23 |
| SARADC_AVDD_1V8 | AH18 | VDD_CPU_BIG1_2 | M24 |
| MIPI_D/C_PHY1_VDD_1V2 | AH19 | VSS_123 | M25 |
| MIPI_D/C_PHY0_VDD_1V2 | AH20 | AVSS_12 | M26 |
| AVSS_54 | AH21 | PCIE20_SATA30_0_AVDD_1V8 | M27 |
| AVSS_55 | AH22 | PCIE20_SATA30_0_AVDD_0V85 | M28 |
| AVSS_56 | AH23 | TVSS_d | M29 |
| CIF_D12/PCIE20X1_2_WAKEN_M0/HDMI_TX0_SDA_M2/I2C5_SDA_M0/UART4_RX_M1/PWM8_M2/SPI3_CLK_M3/GPIO3_D0_u | AH24 | PMIC_INT_L/GPIO0_A7_u | M30 |
| CIF_D9/FSPI_CS1N_M2/PCIE30X4_WAKEN_M2/HDMI_TX1_SDA_M1/CAN2_TX_M0/UART5_RX_M1/SPI3_CS1_M3/GPIO3_C5_u | AH25 | NPOR_u | M31 |
| CIF_D8/FSPI_CS0N_M2/PCIE30X4_CLKREQN_M2/HDMI_TX1_CEC_M2/CAN2_RX_M0/UART5_TX_M1/SPI3_CS0_M3/GPIO3_C4_u | AH26 | AVSS_13 | M32 |
| ETH1_REFCLKO_25M/MIPI_CAMERA1_CLK_M1/I2C4_SCL_M0/GPIO3_A6_d | AH27 | PCIE20_0_TXN/SATA30_0_TXN | M33 |
| GMAC1_RXDV_CRS/MIPI_CAMERA4_CLK_M1/UART2_TX_M2/PWM2_M1/GPIO3_B1_d | AH29 | PCIE20_0_TXP/SATA30_0_TXP | M34 |
| GMAC1_RXCLK/SDIO_CLK_M1/MIPI_CAMERA0_CLK_M1/FSPI_CLK_M2/I2C4_SDA_M0/UART8_CTSN_M1/GPIO3_A5_d | AH30 | DDR_CH0_CKB_A | N1 |
| MIPI_CSI1_D1P | AH31 | DDR_CH0_CK_A | N2 |
| MIPI_CSI1_D1N | AH32 | VSS_124 | N3 |
| MIPI_CSI0_D1P | AH33 | DDR_CH0_A3_B | N4 |
| MIPI_CSI0_D1N | AH34 | DDR_CH0_A2_B | N5 |
| HDMI_TX0_D0N/eDP_TX0_D0N | AJ1 | VSS_125 | N6 |
| HDMI_TX0_D0P/eDP_TX0_D0P | AJ2 | DDR_CH0_LP4/4X_CKE1/LP5_CS1_A | N7 |
| AVSS_57 | AJ3 | DDR_CH0_VDDQ_CKE | N8 |
| HDMI_RX_D2N | AJ4 | VSS_126 | N9 |
| HDMI_RX_D2P | AJ5 | DDR_CH0_VDDQ_1 | N10 |
| AVSS_58 | AJ7 | VSS_127 | N11 |
| AVSS_59 | AJ8 | DDR_CH0_PLL_DVDD | N12 |
| AVSS_60 | AJ9 | DDR_CH0_VDD_MIF_0 | N13 |
| USB20_AVDD_3V3 | AJ10 | VSS_128 | N14 |
| AVSS_61 | AJ11 | VSS_129 | N15 |
| AVSS_62 | AJ12 | VDD_CPU_BIG0_1 | N16 |
| TYPEC1_DP1_VDDA_0V85 | AJ13 | VDD_CPU_BIG0_8 | N17 |
| TYPEC0_DP0_VDD_0V85 | AJ14 | VSS_130 | N18 |
| AVSS_63 | AJ15 | VDD_CPU_BIG0_MEM_1 | N19 |
| AVSS_64 | AJ16 | VSS_131 | N20 |
| AVSS_65 | AJ18 | VDD_CPU_BIG1_MEM_1 | N21 |
| MIPI_D/C_PHY1_VDD_1V8 | AJ19 | VSS_132 | N22 |
| MIPI_D/C_PHY0_VDD_1V8 | AJ20 | VDD_CPU_BIG1_6 | N23 |
| AVSS_66 | AJ21 | VDD_CPU_BIG1_3 | N24 |
| AVSS_67 | AJ22 | VSS_133 | N25 |
| AVSS_68 | AJ23 | VSS_134 | N26 |
| CIF_D11/PCIE20X1_2_CLKREQN_M0/HDMI_TX0_SCL_M2/I2C5_SCL_M0/SPI3_MOSI_M3/GPIO3_C7_u | AJ24 | OSC_1V8 | N27 |
| BT1120_D14/PCIE20X1_2_WAKEN_M1/HDMI_TX0_SDA_M0/I2C8_SCL_M3/SPI3_CS0_M1/GPIO4_C0_u | AJ25 | PMUIO1_1V8 | N28 |
| BT1120_D11/PCIE30X4_WAKEN_M1/HDMI_RX_CEC_M0/SATA1_ACT_LED_M0/UART9_RX_M1/PWM12_M1/SPI3_MISO_M1/GPIO4_B5_d | AJ26 | VSS_135 | N29 |
| BT1120_D12/PCIE30X4_PERSTN_M1/HDMI_RX_HPDIN_M0/SA | AJ27 | SPI2_MOSI_M2/I2C0_SDA_M0/GPIO0_A6_z | N30 |

| Pin Name | Pin | Pin Name | Pin |
|---|---|---|---|
| TA0_ACT_LED_M0/I2C5_SCL_M1/PWM13_M1/SPI3_MOSI_M1/GPIO4_B6_d | | | |
| BT1120_D13/PCIE20X1_2_CLKREQN_M1/HDMI_TX0_SCL_M0/I2C5_SDA_M1/SPI3_CLK_M1/GPIO4_B7_u | AJ28 | SPI2_CLK_M2/SDMMC_PWREN/PMU_DEBUG/GPIO0_A5_d | N31 |
| VSS_313 | AJ30 | AVSS_14 | N32 |
| MIPI_CSI1_CLK0P | AJ31 | PCIE20_0_RXP/SATA30_0_RXP | N33 |
| MIPI_CSI1_CLK0N | AJ32 | PCIE20_0_RXN/SATA30_0_RXN | N34 |
| MIPI_CSI0_CLK0P | AJ33 | VSS_136 | P1 |
| MIPI_CSI0_CLK0N | AJ34 | DDR_CH0_A5_A | P2 |
| HDMI_TX0_D1N/eDP_TX0_D1N | AK2 | VSS_137 | P3 |
| HDMI_TX0_D1P/eDP_TX0_D1P | AK3 | DDR_CH0_A2_A | P4 |
| AVSS_69 | AK4 | DDR_CH0_A3_A | P5 |
| AVSS_70 | AK5 | VSS_138 | P6 |
| USB20_HOST0_DP | AK6 | DDR_CH0_LP4/4X_CKE0/LP5_CS0_A | P7 |
| AVSS_71 | AK7 | VSS_139 | P8 |
| TYPEC1_USB20_OTG_ID | AK8 | VSS_140 | P9 |
| TYPEC1_USB20_OTG_DP | AK9 | DDR_CH0_VDDQ_2 | P10 |
| AVSS_72 | AK10 | VSS_141 | P11 |
| AVSS_73 | AK11 | DDR_CH0_VDD_3 | P12 |
| AVSS_74 | AK12 | DDR_CH0_VDD_MIF_1 | P13 |
| AVSS_75 | AK13 | VSS_142 | P14 |
| AVSS_76 | AK14 | VSS_143 | P15 |
| SARADC_IN5 | AK15 | VDD_CPU_BIG0_2 | P16 |
| SARADC_IN2 | AK16 | VDD_CPU_BIG0_7 | P17 |
| SARADC_IN7 | AK17 | VSS_144 | P18 |
| MIPI_DPHY1_RX_D0P/MIPI_CPHY1_RX_TRIO0_B | AK18 | VSS_145 | P19 |
| MIPI_DPHY1_RX_D1P/MIPI_CPHY1_RX_TRIO1_A | AK19 | VSS_146 | P20 |
| MIPI_DPHY1_RX_CLKP/MIPI_CPHY1_RX_TRIO1_C | AK20 | VSS_147 | P21 |
| MIPI_DPHY1_RX_D2P/MIPI_CPHY1_RX_TRIO2_B | AK21 | VSS_148 | P22 |
| MIPI_DPHY1_RX_D3P/NO_USE | AK22 | VDD_CPU_BIG1_5 | P23 |
| AVSS_77 | AK23 | VDD_CPU_BIG1_4 | P24 |
| BT1120_D15/SPDIF1_TX_M2/PCIE20X1_2_PERSTN_M1/HDMI_TX0_CEC_M0/I2C8_SDA_M3/PWM6_M1/SPI3_CS1_M1/GPIO4_C1_d | AK24 | VSS_149 | P25 |
| CIF_HREF/BT1120_D8/I2S1_SDO1_M0/PCIE30X1_1_BUTTON_RSTN/I2C7_SCL_M3/UART8_RTSN_M0/PWM14_M1/SPI0_CS0_M1/CAN1_RX_M1/GPIO4_B2_u | AK25 | VSS_150 | P26 |
| CIF_CLKIN/BT1120_CLKOUT/I2S1_SDI3_M0/PCIE30X2_PERSTN_M1/I2C6_SDA_M3/UART8_TX_M0/SPI2_CS1_M1/GPIO4_B0_d | AK26 | PMU_0V75 | P27 |
| CIF_D5/BT1120_D5/I2S1_SDI0_M0/PCIE30X1_0_PERSTN_M1/I2C3_SDA_M2/UART3_TX_M2/SPI2_MOSI_M1/GPIO4_A5_d | AK27 | PMUIO2 | P28 |
| VSS_314 | AK28 | I2S1_MCLK_M1/JTAG_TCK_M2/I2C1_SCL_M0/UART2_TX_M0/PCIE30X1_1_CLKREQN_M0/GPIO0_B5_d | P29 |
| VSS_315 | AK29 | I2S1_SDI0_M1/GPU_AVS/UART0_TX_M0/I2C4_SCL_M2/DP1_HPDIN_M1/PWM4_M0/PCIE30X1_0_PERSTN_M0/GPIO0_C5_u | P30 |
| CIF_D0/BT1120_D0/I2S1_MCLK_M0/PCIE30X1_1_CLKREQN_M1/UART9_RTSN_M1/SPI0_MISO_M1/GPIO4_A0_d | AK30 | SDMMC_DET/GPIO0_A4_u | P31 |
| MIPI_CSI1_D2P | AK31 | TSADC_SHUT_ORG/TSADC_SHUT/GPIO0_A1_z | P32 |
| MIPI_CSI1_D2N | AK32 | REFCLK_OUT/GPIO0_A0_d | P33 |
| MIPI_CSI0_D2P | AK33 | VSS_151 | P34 |
| MIPI_CSI0_D2N | AK34 | DDR_CH0_A4_A | R1 |
| HDMI_TX0_D2N/eDP_TX0_D2N | AL1 | DDR_CH0_DQ3_A | R2 |
| HDMI_TX0_D2P/eDP_TX0_D2P | AL2 | VSS_152 | R3 |
| AVSS_78 | AL3 | VSS_153 | R5 |
| AVSS_79 | AL4 | DDR_CH0_LP4/4X_CS0_A | R6 |
| AVSS_80 | AL5 | DDR_CH0_LP4/4X_CS1_A | R7 |
| USB20_HOST0_DM | AL6 | VSS_154 | R8 |
| USB20_HOST1_DP | AL7 | VSS_155 | R9 |
| TYPEC1_USB20_VBUSDET | AL8 | DDR_CH0_VDDQ_3 | R10 |
| TYPEC1_USB20_OTG_DM | AL9 | VSS_156 | R11 |
| TYPEC1_SBU1/DP1_AUXP | AL10 | DDR_CH0_VDD_2 | R12 |
| AVSS_81 | AL11 | VSS_157 | R13 |
| TYPEC0_USB20_OTG_DP | AL12 | VDD_VDENC_0 | R14 |
| AVSS_82 | AL13 | VSS_158 | R15 |
| TYPEC0_USB20_OTG_ID | AL14 | VDD_CPU_BIG0_3 | R16 |
| TYPEC0_SBU1/DP0_AUXP | AL15 | VDD_CPU_BIG0_6 | R17 |
| SARADC_IN1 | AL16 | VSS_159 | R18 |
| SARADC_IN6 | AL17 | VSS_160 | R19 |
| MIPI_DPHY1_RX_D0N/MIPI_CPHY1_RX_TRIO0_A | AL18 | VSS_161 | R20 |
| MIPI_DPHY1_RX_D1N/MIPI_CPHY1_RX_TRIO0_C | AL19 | VSS_162 | R21 |
| MIPI_DPHY1_RX_CLKN/MIPI_CPHY1_RX_TRIO1_B | AL20 | VSS_163 | R22 |
| MIPI_DPHY1_RX_D2N/MIPI_CPHY1_RX_TRIO2_A | AL21 | VSS_164 | R23 |
| MIPI_DPHY1_RX_D3N/MIPI_CPHY1_RX_TRIO2_C | AL22 | VSS_165 | R24 |
| AVSS_83 | AL23 | VSS_166 | R25 |
| MIPI_CAMERA0_CLK_M0/SPDIF1_TX_M1/I2S1_SDO0_M0/PCIE30X1_0_BUTTON_RSTN/SATA2_ACT_LED_M0/I2C6_SCL_M3/UART8_RX_M0/SPI0_CS1_M1/GPIO4_B1_u | AL24 | VSS_167 | R26 |
| VSS_316 | AL25 | PMUIO2_1V8 | R27 |
| CIF_CLKOUT/BT1120_D10/I2S1_SDO3_M0/PCIE30X4_CLKREQN_M1/DP0_HPDIN_M0/SPDIF0_TX_M1/UART9_TX_M1/PWM11_IR_M1/GPIO4_B4_u | AL26 | VSS_168 | R28 |
| CIF_D6/BT1120_D6/I2S1_SDI1_M0/PCIE30X2_CLKREQN_M1/I2C5_SCL_M2/UART3_RX_M2/SPI2_CLK_M1/GPIO4_A6_d | AL27 | I2S1_SCLK_M1/JTAG_TMS_M2/I2C1_SDA_M0/UART2_RX_M0/PCIE30X1_1_WAKEN_M0/GPIO0_B6_d | R29 |
| CIF_D4/BT1120_D4/PCIE30X1_0_WAKEN_M1/I2C3_SCL_M2/UART0_RX_M2/SPI2_MISO_M1/GPIO4_A4_d | AL28 | PDM0_CLK1_M1/PWM2_M0/UART0_RX_M0/I2C4_SDA_M2/DP0_HPDIN_M1/PCIE30X1_0_WAKEN_M0/GPIO0_C4_d | R30 |
| CIF_D3/BT1120_D3/PCIE30X1_0_CLKREQN_M1/UART0_TX_M | AL29 | PMIC_SLEEP2/GPIO0_A3_d | R31 |

| Pin Name | Pin | Pin Name | Pin |
|---|---|---|---|
| 2/GPIO4_A3_d | | | |
| CIF_D1/BT1120_D1/I2S1_SCLK_M0/PCIE30X1_1_WAKEN_M1/UART9_CTSN_M1/SPI0_MOSI_M1/GPIO4_A1_d | AL30 | PMIC_SLEEP1/GPIO0_A2_d | R32 |
| MIPI_CSI1_D3P | AL31 | VSS_169 | R33 |
| MIPI_CSI1_D3N | AL32 | XIN_24M | R34 |
| MIPI_CSI0_D3P | AL33 | DDR_CH0_DQ2_A | T1 |
| MIPI_CSI0_D3N | AL34 | DDR_CH0_DQ1_A | T2 |
| HDMI/eDP_TX0_REXT | AM2 | VSS_170 | T3 |
| HDMI_TX1_D3P/eDP_TX1_D3P | AM3 | DDR_CH0_RESET_A | T4 |
| AVSS_84 | AM4 | DDR_CH0_A6_A | T5 |
| HDMI_TX1_D1P/eDP_TX1_D1P | AM5 | VSS_171 | T6 |
| USB20_HOST1_DM | AM7 | DDR_CH0_A0_A | T7 |
| AVSS_85 | AM8 | DDR_CH0_A1_A | T8 |
| AVSS_86 | AM9 | VSS_172 | T9 |
| TYPEC1_SBU2/DP1_AUXN | AM10 | DDR_CH0_VDDQ_4 | T10 |
| TYPEC0_USB20_OTG_DM | AM12 | VSS_173 | T11 |
| TYPEC0_USB20_VBUSDET | AM14 | DDR_CH0_VDD_1 | T12 |
| TYPEC0_SBU2/DP0_AUXN | AM15 | VSS_174 | T13 |
| SARADC_IN0_BOOT | AM16 | VDD_VDENC_1 | T14 |
| SARADC_IN4 | AM17 | VSS_175 | T15 |
| AVSS_87 | AM18 | VDD_CPU_BIG0_4 | T16 |
| AVSS_88 | AM20 | VDD_CPU_BIG0_5 | T17 |
| AVSS_89 | AM22 | VSS_176 | T18 |
| AVSS_90 | AM23 | VSS_177 | T19 |
| AVSS_91 | AM24 | VSS_178 | T20 |
| CIF_VSYNC/BT1120_D9/I2S1_SDO2_M0/PCIE20X1_2_BUTTON_RSTN/I2C7_SDA_M3/UART8_CTSN_M0/PWM15_IR_M1/CAN1_TX_M1/GPIO4_B3_u | AM25 | VDD_CPU_LIT_MEM_1 | T21 |
| AVSS_92 | AM26 | VDD_CPU_LIT_MEM_0 | T22 |
| CIF_D7/BT1120_D7/I2S1_SDI2_M0/PCIE30X2_WAKEN_M1/I2C5_SDA_M2/SPI2_CS0_M1/GPIO4_A7_d | AM27 | VSS_179 | T23 |
| AVSS_93 | AM28 | VSS_180 | T24 |
| CIF_D2/BT1120_D2/I2S1_LRCK_M0/PCIE30X1_1_PERSTN_M1/SPI0_CLK_M1/GPIO4_A2_d | AM29 | VSS_181 | T25 |
| VSS_317 | AM30 | VSS_182 | T26 |
| MIPI_CSI1_CLK1P | AM31 | VSS_183 | T27 |
| MIPI_CSI1_CLK1N | AM32 | I2S1_LRCK_M1/PWM0_M0/I2C2_SCL_M0/CAN0_TX_M0/SPI0_CS1_M0/PCIE30X1_1_PERSTN_M0/GPIO0_B7_d | T28 |
| MIPI_CSI0_CLK1P | AM33 | I2S1_SDI1_M1/NPU_AVS/UART0_RTSN/PWM5_M1/SPI0_CLK_M0/PCIE30X4_CLKREQN_M0/SATA_CP_POD/GPIO0_C6_u | T29 |
| MIPI_CSI0_CLK1N | AM34 | PMIC_SLEEP5/GPIO0_C3_d | T30 |
| HDMI/eDP_TX1_REXT | AN1 | PDM0_CLK0_M1/PWM1_M0/I2C2_SDA_M0/CAN0_RX_M0/SPI0_MOSI_M0/PCIE30X1_0_CLKREQN_M0/GPIO0_C0_d | T31 |
| HDMI_TX1_SBDP/eDP_TX1_AUXP | AN2 | PMIC_SLEEP4/GPIO0_C2_d | T32 |
| HDMI_TX1_D0P/eDP_TX1_D0P | AN4 | VSS_184 | T33 |
| HDMI_TX1_D1N/eDP_TX1_D1N | AN5 | XOUT_24M | T34 |
| HDMI_TX1_D2P/eDP_TX1_D2P | AN6 | DDR_CH0_DQ0_A | U1 |
| AVSS_94 | AN7 | DDR_CH0_DQ7_A | U2 |
| TYPEC1_SSRX1P/DP1_TX0P | AN8 | VSS_185 | U3 |
| TYPEC1_SSTX1N/DP1_TX1N | AN9 | DDR_CH0_DQS0N_A | U4 |
| TYPEC1_SSRX2P/DP1_TX2P | AN10 | DDR_CH0_DQS0P_A | U5 |
| TYPEC1_SSTX2N/DP1_TX3N | AN11 | DDR_CH0_VDD_0 | U11 |
| AVSS_95 | AN12 | VSS_186 | U12 |
| TYPEC0_SSRX1P/DP0_TX0P | AN13 | VSS_187 | U13 |
| TYPEC0_SSTX1N/DP0_TX1N | AN14 | VDD_VDENC_2 | U14 |
| TYPEC0_SSRX2P/DP0_TX2P | AN15 | VSS_188 | U15 |
| TYPEC0_SSTX2N/DP0_TX3N | AN16 | VSS_189 | U16 |
| SARADC_IN3 | AN17 | VSS_190 | U17 |
| MIPI_DPHY1_TX_D0P/MIPI_CPHY1_TX_TRIO0_B | AN18 | PLL_AVDD1V8 | U18 |
| MIPI_DPHY1_TX_D1P/MIPI_CPHY1_TX_TRIO1_A | AN19 | PLL_AVSS | U19 |
| MIPI_DPHY1_TX_CLKP/MIPI_CPHY1_TX_TRIO1_C | AN20 | VSS_191 | U20 |
| MIPI_DPHY1_TX_D2P/MIPI_CPHY1_TX_TRIO2_B | AN21 | VDD_CPU_LIT_7 | U21 |
| MIPI_DPHY1_TX_D3P/NO_USE | AN22 | VDD_CPU_LIT_0 | U22 |
| AVSS_96 | AN23 | VSS_192 | U23 |
| MIPI_DPHY0_TX_D0P/MIPI_CPHY0_TX_TRIO0_B | AN24 | VSS_193 | U24 |
| MIPI_DPHY0_TX_D1P/MIPI_CPHY0_TX_TRIO1_A | AN25 | VSS_194 | U30 |
| MIPI_DPHY0_TX_CLKP/MIPI_CPHY0_TX_TRIO1_C | AN26 | VSS_195 | U31 |
| MIPI_DPHY0_TX_D2P/MIPI_CPHY0_TX_TRIO2_B | AN27 | PMIC_SLEEP3/GPIO0_C1_d | U32 |
| MIPI_DPHY0_TX_D3P/NO_USE | AN28 | LITCPU_AVS/SPI3_CLK_M2/GPIO0_D3_u | U33 |
| MIPI_DPHY0_RX_D0P/MIPI_CPHY0_RX_TRIO0_B | AN29 | VSS_196 | U34 |
| HDMI_TX1_D3N/eDP_TX1_D3N | AN3 | DDR_CH0_DQ6_A | V1 |
| MIPI_DPHY0_RX_D1P/MIPI_CPHY0_RX_TRIO1_A | AN30 | DDR_CH0_DQ5_A | V2 |
| AVSS_97 | AN31 | VSS_197 | V3 |
| MIPI_DPHY0_RX_CLKP/MIPI_CPHY0_RX_TRIO1_C | AN32 | VSS_198 | V4 |
| MIPI_DPHY0_RX_D2P/MIPI_CPHY0_RX_TRIO2_B | AN33 | VSS_199 | V5 |
| MIPI_DPHY0_RX_D3P/NO_USE | AN34 | DDR_CH0_WCK0N_A | V6 |
| AVSS_98 | AP1 | DDR_CH0_WCK0P_A | V7 |
| HDMI_TX1_D0N/eDP_TX1_D0N | AP4 | VSS_200 | V8 |
| HDMI_TX1_D2N/eDP_TX1_D2N | AP6 | VSS_201 | V9 |
| TYPEC1_USB20_OTG1_REXT | AP7 | VSS_202 | V10 |
| TYPEC1_SSRX1N/DP1_TX0N | AP8 | VSS_203 | V11 |
| TYPEC1_SSTX1P/DP1_TX1P | AP9 | VDD_VDENC_MEM_0 | V12 |
| TYPEC1_SSRX2N/DP1_TX2N | AP10 | VDD_VDENC_MEM_1 | V13 |
| TYPEC1_SSTX2P/DP1_TX3P | AP11 | VDD_VDENC_3 | V14 |
| TYPEC0_USB20_OTG0_REXT | AP12 | VSS_204 | V15 |
| TYPEC0_SSRX1N/DP0_TX0N | AP13 | VDD_LOGIC_6 | V16 |

| Pin Name | Pin | Pin Name | Pin |
|---|---|---|---|
| TYPEC0_SSTX1P/DP0_TX1P | AP14 | VDD_LOGIC_7 | V17 |
| TYPEC0_SSRX2N/DP0_TX2N | AP15 | VSS_205 | V18 |
| TYPEC0_SSTX2P/DP0_TX3P | AP16 | VSS_206 | V19 |
| AVSS_99 | AP17 | PLL_DVDD0V75 | V20 |
| MIPI_DPHY1_TX_D0N/MIPI_CPHY1_TX_TRIO0_A | AP18 | VDD_CPU_LIT_6 | V21 |
| MIPI_DPHY1_TX_D1N/MIPI_CPHY1_TX_TRIO0_C | AP19 | VDD_CPU_LIT_1 | V22 |
| HDMI_TX1_SBDN/eDP_TX1_AUXN | AP2 | VSS_207 | V23 |
| MIPI_DPHY1_TX_CLKN/MIPI_CPHY1_TX_TRIO1_B | AP20 | VSS_208 | V24 |
| MIPI_DPHY1_TX_D2N/MIPI_CPHY1_TX_TRIO2_A | AP21 | VSS_209 | V25 |
| MIPI_DPHY1_TX_D3N/MIPI_CPHY1_TX_TRIO2_C | AP22 | EMMCIO_1V8 | V26 |
| AVSS_100 | AP23 | VSS_210 | V27 |
| MIPI_DPHY0_TX_D0N/MIPI_CPHY0_TX_TRIO0_A | AP24 | I2S1_SDO3_M1/CPU_BIG1_AVS/I2C1_SDA_M2/CAN2_TX_M1/HDMI_TX0_SCL_M1/SPI3_CS1_M2/SATA_MP_SWITCH/GPIO0_D5_u | V28 |
| MIPI_DPHY0_TX_D1N/MIPI_CPHY0_TX_TRIO0_C | AP25 | I2S1_SDO2_M1/PDM0_SDI2_M1/PWM3_IR_M0/I2C1_SCL_M2/CAN2_RX_M1/HDMI_TX0_SDA_M1/SPI3_CS0_M2/PCIE30X2_PERSTN_M0/SATA_CPDET/GPIO0_D4_u | V29 |
| MIPI_DPHY0_TX_CLKN/MIPI_CPHY0_TX_TRIO1_B | AP26 | VSS_211 | V30 |
| MIPI_DPHY0_TX_D2N/MIPI_CPHY0_TX_TRIO2_A | AP27 | I2S1_SDI2_M1/PDM0_SDI0_M1/I2C6_SDA_M0/UART1_RTSN_M2/PWM6_M0/SPI0_MISO_M0/PCIE30X4_WAKEN_M0/GPIO0_C7_d | V31 |
| MIPI_DPHY0_TX_D3N/MIPI_CPHY0_TX_TRIO2_C | AP28 | EMMC_D2/FSPI_D2_M0/GPIO2_D2_u | V32 |
| MIPI_DPHY0_RX_D0N/MIPI_CPHY0_RX_TRIO0_A | AP29 | EMMC_D7/FSPI_CS1N_M0/GPIO2_D7_u | V33 |
| MIPI_DPHY0_RX_D1N/MIPI_CPHY0_RX_TRIO0_C | AP30 | EMMC_CLKOUT/GPIO2_A1_d | V34 |
| MIPI_DPHY0_RX_CLKN/MIPI_CPHY0_RX_TRIO1_B | AP31 | DDR_CH0_DQ4_A | W1 |
| MIPI_DPHY0_RX_D2N/MIPI_CPHY0_RX_TRIO2_A | AP32 | VSS_212 | W2 |
| MIPI_DPHY0_RX_D3N/MIPI_CPHY0_RX_TRIO2_C | AP33 | VSS_213 | W3 |
| AVSS_101 | AP34 | DDR_CH0_WCK1P_A | W4 |
| DDR_CH0_DQ11_B | B1 | DDR_CH0_WCK1N_A | W5 |
| DDR_CH1_DQ11_C | B2 | VSS_214 | W6 |
| DDR_CH1_DQ9_C | B3 | VSS_215 | W7 |
| DDR_CH1_DQ15_C | B4 | DDR_CH0_ZQ_A | W8 |
| DDR_CH1_DQ13_C | B5 | VSS_216 | W9 |
| VSS_5 | B6 | VSS_217 | W10 |
| DDR_CH1_DQ5_C | B7 | VSS_218 | W11 |
| DDR_CH1_DQ7_C | B8 | VSS_219 | W12 |
| DDR_CH1_DQ1_C | B9 | VDD_VDENC_5 | W13 |
| DDR_CH1_DQ3_C | B10 | VDD_VDENC_4 | W14 |
| DDR_CH1_A5_C | B11 | VSS_220 | W15 |
| DDR_CH1_CK_C | B12 | VSS_221 | W16 |
| DDR_CH1_CK_D | B13 | VSS_222 | W17 |
| DDR_CH1_A5_D | B14 | VSS_223 | W18 |
| DDR_CH1_DQ3_D | B15 | VSS_224 | W19 |
| DDR_CH1_DQ1_D | B16 | VSS_225 | W20 |
| DDR_CH1_DQ7_D | B17 | VDD_CPU_LIT_5 | W21 |
| DDR_CH1_DQ5_D | B18 | VDD_CPU_LIT_2 | W22 |
| VSS_6 | B19 | VSS_226 | W23 |
| DDR_CH1_DQ13_D | B20 | VSS_227 | W24 |
| DDR_CH1_DQ15_D | B21 | VCCIO5_1V8 | W25 |
| DDR_CH1_DQ9_D | B22 | VCCIO5 | W26 |
| DDR_CH1_DQ11_D | B23 | VSS_228 | W27 |
| VSS_7 | B24 | PMIC_SLEEP6/PDM0_SDI3_M1/GPIO0_D6_d | W28 |
| HDMI_TX1_SCL_M2/SPI2_MISO_M0/GPIO1_A4_d | B25 | I2S1_SDO1_M1/I2C0_SDA_M2/UART1_RX_M2/HDMI_RX_SCL_M0/SPI3_MOSI_M2/PCIE30X2_WAKEN_M0/HDMI_TX1_CEC_M1/GPIO0_D2_u | W29 |
| HDMI_TX0_HPD_M0/SPI2_MOSI_M0/GPIO1_A5_d | B26 | I2S1_SDO0_M1/CPU_BIG0_AVS/I2C0_SCL_M2/UART0_CTSN/UART1_TX_M2/HDMI_RX_SDA_M0/SPI0_CS0_M0/PCIE30X2_CLKREQN_M0/HDMI_TX0_CEC_M1/GPIO0_D1_u | W30 |
| VSS_8 | B27 | I2S1_SDI3_M1/PDM0_SDI1_M1/I2C6_SCL_M0/UART1_CTSN_M2/PWM7_IR_M0/SPI3_MISO_M2/PCIE30X4_PERSTN_M0/GPIO0_D0_d | W31 |
| PCIE30_PORT1_REF_CLKN | B28 | EMMC_D6/FSPI_CS0N_M0/GPIO2_D6_u | W32 |
| PCIE30_PORT1_TX1N | B29 | EMMC_D1/FSPI_D1_M0/GPIO2_D1_u | W33 |
| PCIE30_PORT1_TX0P | B30 | EMMC_CMD/FSPI_CLK_M0/GPIO2_A0_u | W34 |
| PCIE30_PORT1_RX1N | B31 | DDR_CH0_DQ12_A | Y1 |
| PCIE30_PORT1_RX0P | B32 | DDR_CH0_DQ13_A | Y2 |
| VSS_9 | B33 | VSS_229 | Y3 |
| PCIE30_PORT0_RESREF | B34 | DDR_CH0_DM0_A | Y4 |
| DDR_CH0_DQ9_B | C1 | VSS_230 | Y5 |
| DDR_CH0_DQ10_B | C2 | VSS_231 | Y6 |
| VSS_10 | C3 | VCCIO2 | Y7 |
| VSS_11 | C4 | VSS_232 | Y8 |
| VSS_17 | C10 | VSS_233 | Y9 |
| VSS_18 | C11 | VSS_234 | Y10 |
| VSS_19 | C12 | VSS_235 | Y11 |
| VSS_20 | C13 | VSS_236 | Y12 |
| VSS_21 | C14 | VSS_237 | Y13 |
| VSS_22 | C15 | VSS_238 | Y14 |
| VSS_23 | C16 | VSS_239 | Y15 |
| VSS_24 | C17 | VSS_240 | Y16 |
| VSS_25 | C18 | VSS_241 | Y17 |
| DDR_CH1_RESET_D | C19 | VSS_242 | Y18 |
| VSS_26 | C20 | VSS_243 | Y19 |
| VSS_27 | C21 | VSS_244 | Y20 |
| VSS_28 | C22 | VDD_CPU_LIT_4 | Y21 |
| VSS_29 | C23 | VDD_CPU_LIT_3 | Y22 |
| HDMI_TX1_HPD_M0/SPI2_CLK_M0/GPIO1_A6_d | C24 | VSS_245 | Y23 |

| Pin Name | Pin | Pin Name | Pin |
|---|---|---|---|
| PDM1_SDI0_M1/PCIE30X1_1_PERSTN_M2/PWM3_IR_M3/SPI2_CS0_M0/GPIO1_A7_u | C25 | VSS_246 | Y24 |
| VSS_30 | C26 | VCCIO3_1V8 | Y26 |
| PDM1_SDI1_M1/PCIE30X4_CLKREQN_M3/SPI2_CS1_M0/GPIO1_B0_u | C27 | GMAC1_PPSCLK/PCIE30X2_BUTTON_RSTN/UART7_RX_M1/SPI1_CLK_M1/GPIO3_C1_d | Y27 |
| VSS_31 | C28 | VSS_247 | Y28 |
| PCIE30_PORT1_TX1P | C29 | GMAC1_PPSTRIG/I2C3_SDA_M1/UART7_TX_M1/SPI1_MISO_M1/GPIO3_C0_d | Y29 |
| VSS_32 | C30 | GMAC1_MDIO/MIPI_TE1/I2C8_SDA_M4/UART7_CTSN_M1/PWM15_IR_M0/SPI1_CS1_M1/GPIO3_C3_d | Y30 |
| PCIE30_PORT1_RX1P | C31 | GMAC1_MDC/MIPI_TE0/I2C8_SCL_M4/UART7_RTSN_M1/PWM14_M0/SPI1_CS0_M1/GPIO3_C2_d | Y31 |
| VSS_33 | C32 | EMMC_D4/I2C1_SCL_M3/UART5_RX_M2/GPIO2_D4_u | Y32 |
| PCIE30_PORT0_TX1P | C33 | EMMC_D0/FSPI_D0_M0/GPIO2_D0_u | Y33 |
| PCIE30_PORT0_TX1N | C34 | EMMC_DATA_STROBE/I2C2_SDA_M2/UART5_CTSN_M1/GPIO2_A2_d | Y34 |

# Chapter 3 Electrical Specification

## 3.1 Absolute Ratings

The below table provides the absolute ratings.

Absolute maximum or minimum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

Table 3-1 Absolute ratings

| Parameters | Related Power Group | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage for CPU | VDD_CPU_BIG0<br>VDD_CPU_BIG1<br>VDD_CPU_LIT | -0.3 | 1.1 | V |
| Supply voltage for CPU memory | VDD_CPU_BIG0_MEM<br>VDD_CPU_BIG1_MEM<br>VDD_CPU_LIT_MEM | -0.3 | 1.1 | V |
| Supply voltage for GPU | VDD_GPU | -0.3 | 1.1 | V |
| Supply voltage for GPU memory | VDD_GPU_MEM | -0.3 | 1.1 | V |
| Supply voltage for NPU | VDD_NPU | -0.3 | 1.1 | V |
| Supply voltage for NPU memory | VDD_NPU_MEM | -0.3 | 1.1 | V |
| Supply voltage for VCODEC | VDD_VDENC | -0.3 | 0.95 | V |
| Supply voltage for VCODEC memory | VDD_VDENC_MEM | -0.3 | 0.95 | V |
| Supply voltage for core logic | VDD_LOGIC | -0.3 | 0.95 | V |
| 0.75V supply voltage | PMU_0V75<br>PLL_DVDD0V75<br>USB20_DVDD_0V75<br>HDMI/eDP_TX0_VDD_0V75<br>HDMI/eDP_TX0_AVDD_0V75<br>HDMI/eDP_TX1_VDD_0V75<br>HDMI/eDP_TX1_AVDD_0V75<br>HDMI_RX_AVDD0V75<br>MIPI_CSI0_AVCC0V75<br>MIPI_CSI1_AVCC0V75<br>PCIE30_PORT0_AVDD0V75<br>PCIE30_PORT1_AVDD0V75<br>OTP_VDDOTP_0V75 | -0.3 | 0.95 | V |
| 0.85V supply voltage | DDR_CH0_VDD<br>DDR_CH0_VDD_MIF<br>DDR_CH0_PLL_DVDD<br>DDR_CH1_VDD<br>DDR_CH1_VDD_MIF<br>DDR_CH1_PLL_DVDD<br>TYPEC0_DP0_VDD_0V85<br>TYPEC0_DP0_VDDA_0V85<br>TYPEC1_DP1_VDD_0V85<br>TYPEC1_DP1_VDDA_0V85<br>MIPI_D/C_PHY0_VDD<br>MIPI_D/C_PHY1_VDD<br>PCIE20_SATA30_0_AVDD_0V85<br>PCIE20_SATA30_1_AVDD_0V85<br>PCIE20_SATA30_USB30_2_AVDD_0V85 | -0.3 | 1.00 | V |
| 1.2V supply voltage | MIPI_D/C_PHY0_VDD_1V2<br>MIPI_D/C_PHY1_VDD_1V2 | -0.3 | 1.35 | V |
| 1.8V supply voltage | DDR_CH0_PLL_AVDD1V8<br>DDR_CH1_PLL_AVDD1V8<br>PLL_AVDD1V8<br>USB20_AVDD_1V8<br>TYPEC0_DP0_VDDH_1V8<br>TYPEC1_DP1_VDDH_1V8<br>HDMI/eDP_TX0_VDD_CMN_1V8<br>HDMI/eDP_TX0_VDD_IO_1V8<br>HDMI/eDP_TX1_VDD_CMN_1V8<br>HDMI/eDP_TX1_VDD_IO_1V8<br>MIPI_CSI0_AVCC1V8<br>MIPI_CSI1_AVCC1V8<br>MIPI_D/C_PHY0_VDD_1V8<br>MIPI_D/C_PHY1_VDD_1V8<br>PCIE20_SATA30_0_AVDD_1V8<br>PCIE20_SATA30_1_AVDD_1V8 | -0.5 | 1.98 | V |

| Parameters | Related Power Group | Min | Max | Unit |
|---|---|---|---|---|
| | PCIE20_SATA30_USB30_2_AVDD_1V8<br>PCIE30_PORT0_AVDD1V8<br>PCIE30_PORT1_AVDD1V8<br>SARADC_AVDD_1V8<br>OSC_1V8 | | | |
| 3.3V supply voltage | USB20_AVDD_3V3<br>HDMI_RX_DVDD3V3<br>HDMI_RX_VPH3V3 | -0.5 | 3.63 | V |
| 1.8V only GPIO supply voltage | PMUIO1_1V8<br>EMMCIO_1V8<br>VCCIO1_1V8<br>VCCIO3_1V8 | -0.5 | 1.98 | V |
| 1.8V/3.3V GPIO supply voltage | PMUIO2_1V8<br>VCCIO2_1V8<br>VCCIO4_1V8<br>VCCIO5_1V8<br>VCCIO6_1V8 | -0.5 | 3.63 | V |
| Supply voltage for DDR IO (LPDDR4/4X 0.6V; LPDDR5 0.5V) | DDR_CH0_VDDQ<br>DDR_CH0_VDDQ_CK<br>DDR_CH1_VDDQ<br>DDR_CH1_VDDQ_CK | -0.3 | 0.7 | V |
| Supply voltage for DDR IO (LPDDR4/4X 1.1V; LPDDR5 1.05V) | DDR_CH0_VDDQ_CKE<br>DDR_CH1_VDDQ_CKE | -0.3 | 1.25 | V |
| Storage Temperature | Tstg | -40 | 125 | ℃ |
| Max Conjunction Temperature | Tj | NA | 125 | ℃ |

## 3.2 Recommended Operating Condition

Following table describes the recommended operating condition.

Table 3-2 Recommended operating condition

| Parameters | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Voltage for CPU BigCore 0 | VDD_CPU_BIG0 | 0.55 | 0.75 | 1.05 | V |
| Voltage for CPU BigCore 0 Memory | VDD_CPU_BIG0_MEM | 0.675 | 0.75 | 1.05 | V |
| Voltage for CPU BigCore 1 | VDD_CPU_BIG1 | 0.55 | 0.75 | 1.05 | V |
| Voltage for CPU BigCore 1 Memory | VDD_CPU_BIG1_MEM | 0.675 | 0.75 | 1.05 | V |
| Voltage for CPU LitCore and DSU | VDD_CPU_LIT | 0.55 | 0.75 | 0.95 | V |
| Voltage for CPU LitCore and DSU Memory | VDD_CPU_LIT_MEM | 0.675 | 0.75 | 0.95 | V |
| Voltage for GPU | VDD_GPU | 0.55 | 0.75 | 0.95 | V |
| Voltage for GPU Memory | VDD_GPU_MEM | 0.675 | 0.75 | 0.95 | V |
| Voltage for NPU | VDD_NPU | 0.55 | 0.75 | 0.95 | V |
| Voltage for NPU Memory | VDD_NPU_MEM | 0.675 | 0.75 | 0.95 | V |
| Voltage for VCODEC | VDD_VDENC | 0.675 | 0.75 | 0.825 | V |
| Voltage for VCODEC Memory | VDD_VDENC_MEM | 0.675 | 0.75 | 0.825 | V |
| Voltage for Logic | VDD_LOGIC | 0.675 | 0.75 | 0.825 | V |
| Voltage for PMU | PMU_0V75 | 0.675 | 0.75 | 0.825 | V |
| Digital GPIO Power (1.8V only) | PMUIO1_1V8, VCCIO1_1V8, VCCIO3_1V8 | 1.65 | 1.8 | 1.95 | V |
| Digital GPIO Power (3.3V/1.8V) | PMUIO2_1V8, VCCIO2_1V8, VCCIO4_1V8, VCCIO5_1V8, VCCIO6_1V8 | 2.7<br>1.65 | 3.3<br>1.8 | 3.6<br>1.95 | V |
| eMMC IO Power (1.8V) | EMMCIO_1V8 | 1.65 | 1.8 | 1.95 | V |
| DDR CH0 Logic power(0.85V) | DDR_CH0_VDD, DDR_CH0_VDD_MIF, DDR_CH1_VDD, DDR_CH1_VDD_MIF, | 0.675 | 0.85 | 0.935 | V |
| DDR CH0_PLL power(0.85V) | DDR_CH0_PLL_DVDD, DDR_CH1_PLL_DVDD | 0.675 | 0.85 | 0.8925 | V |
| DDR CH0_PLL power(1.8V) | DDR_CH0_PLL_AVDD1V8, DDR_CH1_PLL_AVDD1V8 | 1.62 | 1.8 | 1.98 | V |

| Parameters | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| LPDDR4 IO VDDQ power | DDR_CH0_VDDQ, DDR_CH0_VDDQ_CK, DDR_CH1_VDDQ, DDR_CH1_VDDQ_CK | 0.57 | 0.6 | 0.63 | V |
| LPDDR4 Retention IO VDDQ Power | DDR_CH0_VDDQ_CKE, DDR_CH1_VDDQ_CKE | 1.045 | 1.1 | 1.155 | V |
| LPDDR5 IO VDDQ power | DDR_CH0_VDDQ, DDR_CH0_VDDQ_CK, DDR_CH1_VDDQ, DDR_CH1_VDDQ_CK | 0.475 | 0.5 | 0.525 | V |
| LPDDR5 Retention IO VDDQ Power | DDR_CH0_VDDQ_CKE, DDR_CH1_VDDQ_CKE | 1.0 | 1.05 | 1.1 | V |
| PLL Analog Power(0.75V) | PLL_DVDD0V75 | 0.675 | 0.75 | 0.8925 | V |
| PLL Analog Power(1.8V) | PLL_AVDD1V8 | 1.62 | 1.8 | 1.98 | V |
| USB 2.0 Analog Power (0.75V) | USB20_DVDD_0V75 | 0.6975 | 0.75 | 0.825 | V |
| USB 2.0 Analog Power (1.8V) | USB20_AVDD_1V8 | 1.674 | 1.8 | 1.98 | V |
| USB 2.0 Analog Power (3.3V) | USB20_AVDD_3V3 | 3.069 | 3.3 | 3.63 | V |
| USB & DP Analog Power (0.85V) | TYPEC0_DP0_VDD_0V85, TYPEC0_DP0_VDDA_0V85, TYPEC1_DP1_VDD_0V85, TYPEC1_DP1_VDDA_0V85 | 0.8075 | 0.85 | 0.8925 | V |
| USB & DP Analog Power (1.8V) | TYPEC0_DP0_VDDH_1V8, TYPEC1_DP1_VDDH_1V8 | 1.71 | 1.8 | 1.89 | V |
| Combo PIPE PHY Analog Power(0.85V) | PCIE20_SATA30_0_AVDD_0V85, PCIE20_SATA30_1_AVDD_0V85, PCIE20_SATA30_USB30_2_AVDD_0V85 | 0.8 | 0.85 | 0.935 | V |
| Combo PIPE PHY Analog Power(1.8V) | PCIE20_SATA30_0_AVDD_1V8, PCIE20_SATA30_1_AVDD_1V8, PCIE20_SATA30_USB30_2_AVDD_1V8 | 1.62 | 1.8 | 1.98 | V |
| PCIe30 Analog Power(0.75V) | PCIE30_PORT0_AVDD0V75, PCIE30_PORT1_AVDD0V75 | 0.7125 | 0.75 | 0.8925 | V |
| PCIe30 Analog Power(1.8V) | PCIE30_PORT0_AVDD1V8, PCIE30_PORT1_AVDD1V8 | 1.71 | 1.8 | 1.89 | V |
| MIPI CSI DPHY Analog Power(0.75V) | MIPI_CSI0_AVCC0V75, MIPI_CSI1_AVCC0V75 | 0.675 | 0.75 | 0.825 | V |
| MIPI CSI DPHY Analog Power(1.8V) | MIPI_CSI0_AVCC1V8, MIPI_CSI1_AVCC1V8 | 1.62 | 1.8 | 1.98 | V |
| MIPI DCPHY Analog Power (0.85V) | MIPI_D/C_PHY0_VDD, MIPI_D/C_PHY1_VDD | 0.7125 | 0.85 | 0.8925 | V |
| MIPI DCPHY Analog Power (1.2V) | MIPI_D/C_PHY0_VDD_1V2, MIPI_D/C_PHY1_VDD_1V2 | 1.14 | 1.2 | 1.26 | V |
| MIPI DCPHY Analog Power (1.8V) | MIPI_D/C_PHY0_VDD_1V8, MIPI_D/C_PHY1_VDD_1V8 | 1.71 | 1.8 | 1.89 | V |
| HDMI RX Analog Power(0.75V) | HDMI_RX_AVDD0V75 | 0.675 | 0.75 | 0.825 | V |
| HDMI RX Analog Power(3.3V) | HDMI_RX_DVDD3V3 | 3.135 | 3.3 | 3.465 | V |
| HDMI RX Analog Power(3.3V) | HDMI_RX_VPH3V3 | 3.135 | 3.3 | 3.465 | V |
| HDMI/eDP TX Digital Power (0.75V) | HDMI/eDP_TX0_VDD_0V75, HDMI/eDP_TX1_VDD_0V75 | 0.675 | 0.75 | 0.825 | V |
| HDMI/eDP TX Analog Power (0.75V) | HDMI/eDP_TX0_AVDD_0V75, HDMI/eDP_TX1_AVDD_0V75 | 0.675 | 0.75 | 0.825 | V |
| HDMI/eDP TX Analog Power (1.8V) | HDMI/eDP_TX0_VDD_CMN_1V8, HDMI/eDP_TX1_VDD_CMN_1V8 | 1.62 | 1.8 | 1.98 | V |
| HDMI/eDP TX Analog Power (1.8V) | HDMI/eDP_TX0_VDD_IO_1V8, HDMI/eDP_TX1_VDD_IO_1V8 | 1.62 | 1.8 | 1.98 | V |
| SARADC Analog Power(1.8V) | SARADC_AVDD_1V8 | 1.62 | 1.8 | 1.98 | V |
| OTP Analog Power(0.75V) | OTP_VDDOTP_0V75 | 0.675 | 0.75 | 0.825 | V |
| OSC Analog Power(1.8V) | OSC_1V8 | 1.65 | 1.8 | 1.95 | V |
| OSC input clock frequency | | NA | 24 | NA | MHz |
| Max CPU frequency | | NA | NA | 2.2-2.4 | GHz |
| Max GPU frequency | | NA | NA | 1000 | MHz |
| Max NPU frequency | | NA | NA | 1000 | MHz |
| Ambient Operating Temperature | $T_A$ | 0 | NA | 80 | ℃ |

# 3.3 DC Characteristics

Table 3-3 DC Characteristics

| Parameters | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Digital 3.3V/1.8V GPIO @3.3V | Input Low Voltage | $V_{IL}$ | VSS | NA | 0.3*VDDO | V |
| | Input High Voltage | $V_{IH}$ | 0.7*VDDO | NA | VDDO | V |
| | Output Low Voltage | $V_{OL}$ | VSS | NA | 0.25*DVDD | V |
| | Output High Voltage | $V_{OH}$ | 0.75*DVDD | NA | DVDD | V |
| | Pullup Resistor | $R_{RPU}$ | 10 | NA | 100 | Kohm |
| | Pulldown Resistor | $R_{RPD}$ | 10 | NA | 100 | Kohm |
| Digital 3.3V/1.8V GPIO @1.8V | Input Low Voltage | $V_{IL}$ | VSS | NA | 0.3*VDDO | V |
| | Input High Voltage | $V_{IH}$ | 0.7*VDDO | NA | VDDO | V |
| | Output Low Voltage | $V_{OL}$ | VSS | NA | 0.25*DVDD | V |
| | Output High Voltage | $V_{OH}$ | 0.75*DVDD | NA | DVDD | V |
| | Pullup Resistor | $R_{RPU}$ | 10 | NA | 50 | Kohm |
| | Pulldown Resistor | $R_{RPD}$ | 10 | NA | 50 | Kohm |
| Digital 1.8V only GPIO @1.8V | Input Low Voltage | $V_{IL}$ | VSS | NA | 0.3*VDDO | V |
| | Input High Voltage | $V_{IH}$ | 0.7*VDDO | NA | VDDO | V |
| | Output Low Voltage | $V_{OL}$ | VSS | NA | 0.25*DVDD | V |
| | Output High Voltage | $V_{OH}$ | 0.75*DVDD | NA | DVDD | V |
| | Pullup Resistor | $R_{RPU}$ | 10 | NA | 50 | Kohm |
| | Pulldown Resistor | $R_{RPD}$ | 10 | NA | 50 | Kohm |
| eMMC IO @1.8V | Input Low Voltage | $V_{IL}$ | VSS | NA | 0.35*DVDD | V |
| | Input High Voltage | $V_{IH}$ | 0.65*DVDD | NA | DVDD | V |
| | Output Low Voltage | $V_{OL}$ | VSS | NA | 0.45 | V |
| | Output High Voltage | $V_{OH}$ | DVDD-0.45 | NA | DVDD | V |
| | Pullup Resistor | $R_{RPU}$ | 10 | NA | 50 | Kohm |
| | Pulldown Resistor | $R_{RPD}$ | 10 | NA | 50 | Kohm |
| DDR IO | Input Low Voltage | $V_{IL}$ | NA | NA | Vref-0.14 | V |
| | Input High Voltage | $V_{IH}$ | Vref+0.14 | NA | NA | V |
| | Output Log Voltage | $V_{OL}$ | NA | NA | 0.2 | V |
| | Output High Voltage | $V_{OH}$ | 0.25 | NA | NA | V |
| | Input Low Current | $I_{IL}$ | -100/-500 | NA | 100/500 | Room/Hot uA |
| | Input High Current | $I_{IH}$ | -100/-500 | NA | 100/500 | Room/Hot uA |

*Note: VDDO and DVDD are both IO power Supply*

# 3.4 Electrical Characteristics for General IO

Table 3-4 Electrical Characteristics for Digital General IO

| Parameters | | Symbol | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Digital 3.3V/1.8V GPIO @3.3V | Input leakage current | $I_{PAD}$ | DVDD=Max, $V_{PAD}$=0V or DVDD | -10 | NA | 10 | uA |
| | Input Hysteresis for Schmitt Trigger Operation | $V_H$ | | 0.08* VDDO | NA | NA | V |
| | Input pullup resistor current | $I_{RPU}$ | $V_{PAD}$ = 0V | -20 | NA | -180 | uA |
| | Input pulldown resistor current | $I_{RPD}$ | $V_{PAD}$ = VDDO | 20 | NA | 180 | uA |
| Digital 3.3V/1.8V GPIO @1.8V | Input leakage current | $I_{PAD}$ | DVDD=Max, $V_{PAD}$=0V or DVDD | -10 | NA | 10 | uA |
| | Input Hysteresis for Schmitt Trigger Operation | $V_H$ | | 0.1* VDDO | NA | NA | V |
| | Input pullup resistor current | $I_{RPU}$ | $V_{PAD}$ = 0V | -20 | NA | -180 | uA |
| | Input pulldown resistor current | $I_{RPD}$ | $V_{PAD}$ = VDDO | 20 | NA | 180 | uA |
| | Input leakage current | $I_{PAD}$ | DVDD=Max, $V_{PAD}$=0V or DVDD | -10 | NA | 10 | uA |

| Parameters | | Symbol | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Digital 1.8V only GPIO @1.8V | Input Hysteresis for Schmitt Trigger Operation | $V_H$ | | 0.1* VDDO | NA | NA | V |
| | Input pullup resistor current | $I_{RPU}$ | $V_{PAD}$ = 0V | -20 | NA | -170 | uA |
| | Input pulldown resistor current | $I_{RPD}$ | $V_{PAD}$ = VDDO | 20 | NA | 170 | uA |
| eMMC IO @1.8V | Input leakage current | $I_{PAD}$ | DVDD=Max, $V_{PAD}$=0V or DVDD | -10 | NA | 10 | uA |
| | Input Hysteresis for Schmitt Trigger Operation | $V_H$ | | 0.1* DVDD | NA | NA | V |
| | Input pullup resistor current | $I_{RPU}$ | $V_{PAD}$ = 0V | -20 | NA | -170 | uA |
| | Input pulldown resistor current | $I_{RPD}$ | $V_{PAD}$ = VDDO | 20 | NA | 170 | uA |

*Note: VDDO and DVDD are both IO power Supply*

# 3.5 Electrical Characteristics for PLL

Table 3-5 Electrical Characteristics for INT PLL

| Parameters | Symbol | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input clock frequency | $F_{FIN}$ | | 4.5 | - | 300 | MHz |
| Reference frequency($F_{FIN}$/p) | $F_{FREE}$ | | 4.5 | 7 | 12 | MHz |
| Frequency of PLL's output | $F_{FOUT}$ | | 35.2 | - | 4500 | MHz |
| Frequency of VCO's output | $F_{FVCO}$ | | 2250 | - | 4500 | MHz |
| Lock time | $T_{LT}$ | Measured at all $F_{FIN}$ and $F_{FOUT}$ range. RESETB=High | - | - | 150 | Cycles |

Table 3-6 Electrical Characteristics for FRAC PLL

| Parameters | Symbol | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input clock frequency | $F_{FIN}$ | | 6 | - | 300 | MHz |
| Reference frequency($F_{FIN}$/p) | $F_{FREE}$ | | 6 | 20 | 30 | MHz |
| Frequency of PLL's output | $F_{FOUT}$ | | 35.2 | - | 4500 | MHz |
| Frequency of VCO's output | $F_{FVCO}$ | | 2250 | - | 4500 | MHz |
| Lock time | $T_{LT}$ | Measured at all $F_{FIN}$ and $F_{FOUT}$ range. RESETB=High | - | - | 500 | Cycles |

Table 3-7 Electrical Characteristics for DDR PLL

| Parameters | Symbol | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input clock frequency | $F_{FIN}$ | | 6 | - | 300 | MHz |
| Reference frequency($F_{FIN}$/p) | $F_{FREE}$ | | 6 | 20 | 30 | MHz |
| Frequency of PLL's output | $F_{FOUT}$ | | 51.6 | - | 6600 | MHz |
| Frequency of VCO's output | $F_{FVCO}$ | | 3300 | - | 6600 | MHz |
| Lock time | $T_{LT}$ | Measured at all $F_{FIN}$ and $F_{FOUT}$ range. RESETB=High | - | - | 500 | Cycles |

*Notes:*

① *p is the input divider value*

# 3.6 Electrical Characteristics for PCIe2/SATA Interface

Table 3-8 Electrical Characteristics for PCIe2/SATA Interface

| Parameters | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Transmitter | | | | | |
| Differential Peak-Peak TX Output Voltage Swing | $V_{TX\_DIFF\_PP}$ | 800 | 1000 | 1200 | mV |
| Differential Peak-Peak Low Power TX Output Voltage Swing | $V_{TX\_DIFF\_PP\_LOW}$ | 400 | NA | 1200 | mV |
| The output impedance | $R_{TX\_DIFF\_DC}$ | 80 | 100 | 120 | ohm |
| Single Ended Output Resistance Matching | $R_{TX\_DC\_OFFSET}$ | NA | NA | 5 | % |
| Transmitter output common mode voltage | $V_{TX\_DC\_CM}$ | 400 | NA | 800 | mV |
| Maximum mismatch between TXP and TXM for both time and amp | $V_{TX\_CM\_AC\_PP\_ACTIVE}$ | NA | NA | 50 | mV |
| The amount of voltage change allowed during Receiver Detection | $V_{TX\_RCV\_DETECT}$ | NA | NA | 600 | mV |
| TX de-emphasis | $V_{TX\_DE\_RATIO}$ | 3.0 | 3.5 | 4.0 | dB |
| AC Coupling Capacitor(USB3.1/PCIe) | $C_{AC\_COUPLING}$ | 75 | NA | 200 | nF |

| Parameters | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| AC Coupling Capacitor(SATA) | | 6 | NA | 12 | nF |
| Output rising time for 20% to 80% | $T_r$ | 25 | NA | NA | ps |
| Output falling time for 20% to 80% | $T_f$ | 25 | NA | NA | ps |
| Transmitter short circuit limit | $I_{TX\_SHORT}$ | NA | NA | 20 | mA |
| Output differential skew | $T_{SKEW\_DIFF}$ | -15 | NA | 15 | ps |
| Receiver | | | | | |
| Input Voltage Swing | $V_{RXDPP\_C}$ | 250 | NA | 1200 | mVpp |
| The input differential impedance | $R_{RXD\_C}$ | 80 | 100 | 120 | Ohm |
| Single Ended input Resistance Matching | $R_{RXD\_C\_MS}$ | NA | NA | 5 | % |

## 3.7 Electrical Characteristics for MIPI CDPHY interface

Table 3-9 Electrical Characteristics for MIPI CDPHY interface

| Parameters | Symbol | Description | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| LP-RX | $V_{IH}$ | Logic1 input voltage | All conditions | 880 | NA | NA | mV |
| | $V_{IL}$ | Logic0 input voltage, not in ULPS state | All conditions | NA | NA | 550 | mV |
| Skew Calibration | $T_{skewcal}$ (initial) | Duration for which the transmitter drives the skew-calibration pattern in the initial skew calibration mode | >1.5Gbps | NA | NA | 100 | us |
| | | | | 2^15 | NA | NA | UI |
| | $T_{skewcal}$ (periodic) | Duration for which the transmitter drives the skew-calibration pattern in the periodic skew calibration mode | >1.5Gbps (optional) | NA | NA | 10 | us |
| | | | | 2^13 | NA | NA | UI |

## 3.8 Electrical Characteristics for MIPI CSI DPHY interface

Table 3-10 Electrical Characteristics for MIPI CSI DPHY interface

| Parameters | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Common-mode interference beyond 450 MHz | ΔVCMRX(HF) | NA | NA | 100 | mV |
| | | NA | NA | 50 | mV |
| Common-mode interference 50MHz-450MHz | ΔVCMRX(LF) | -50 | NA | 50 | mV |
| | | -25 | NA | 25 | mV |
| Common-mode termination | CCM | NA | NA | 60 | pF |
| Input pulse rejection | eSPIKE | NA | NA | 300 | V.ps |
| Minimum pulse width response | TMIN-RX | 20 | NA | NA | ns |
| Peak interference amplitude | VINT | NA | NA | 200 | mV |
| Interference frequency | fINT | 450 | NA | NA | MHz |

## 3.9 Electrical Characteristics for SARADC

Table 3-10 Electrical Characteristics for SARADC

| Parameters | Symbol | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Resolution | | | NA | 12 | NA | Bit |
| Anglog Input Range | AIN | | AVSS18 | NA | AVDD18 | V |
| Differential Non-Linearity | DNL | PD = Low<br>$F_s$ = 1MS/s<br>$F_{CLK}$ = 20MHz<br>$F_{SOC}$ = 1MHz<br>$F_{AIN}$ = 10kHz ramp wave | NA | ±1.0 | ±3.0 | LSB |
| Integral Non-Linearity | INL | | NA | ±2.0 | ±6.0 | LSB |
| Top Offset Voltage Error | $E_{OT}$ | | NA | ±10 | ±20 | LSB |
| Bottom Offset Voltage Error | $E_{OB}$ | | NA | ±10 | ±20 | LSB |

## 3.10 Electrical Characteristics for TSADC

Table 3-11 Electrical Characteristics for TSADC

| Parameters | Symbol | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Accuracy from -40℃ to 125℃ | $T_{JACC}$ | Temp: -40 ~ 125℃<br>Supply: 1.62V ~ 1.98V | NA | ±3 | ±5 | ℃ |
| Sensing Temperature Range | $T_{RANGE}$ | | -40 | NA | 125 | ℃ |
| Resolution | $T_{LSB}$ | | NA | 1 | NA | ℃ |

# Chapter 4 Thermal Management

## 4.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature has to be below 125℃.

## 4.2 Package Thermal Characteristics

Table 4-1 provides the thermal resistance characteristics for the package used on the SoC. The resulting simulation data for reference only, please prevail in kind test.

Table 4-1 Thermal Resistance Characteristics

| Parameter | Symbol | Typical | Unit |
|---|---|---|---|
| Junction-to-ambient thermal resistance | $\boldsymbol{\theta_{JA}}$ | 8.7 | (℃/$\boldsymbol{W}$) |
| Junction-to-board thermal resistance | $\boldsymbol{\theta_{JB}}$ | 3.5 | (℃/$\boldsymbol{W}$) |
| Junction-to-case thermal resistance | $\boldsymbol{\theta_{JC}}$ | 0.12 | (℃/$\boldsymbol{W}$) |

*Note: The testing PCB is 10 layers,* 114*mmx*101*mm, Ambient temperature is 25℃.*