Rockchip RK3588C Datasheet

Revision History

Date	Revision	Description
2025-12-26	1.4	Modify block diagram, adding FSPI as external memory interface and changing the number of SPI controllers. Modify the full name of FSPI in 1.2.2
2024-12-12	1.3	Update digital GPIO power parameters in 3.1
2024-08-21	1.2	Update digital GPIO power parameters; Add the timing requirement of display interface and VOP
2023-02-10	1.1	Update the block diagram, delete CAN information
2022-07-28	1.0	Initial Release for special reference

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Chapter 1 Introduction

1.1 Overview

RK3588C is a low power, high performance processor for NVR and Edge Computing device, and integrates quad-core Cortex-A76 and quad-core Cortex-A55 with separately NEON coprocessor.

Many embedded powerful hardware engines provide optimized performance for high-end application. RK3588C supports H.265 and VP9 decoder by 8K@60fps, H.264 decoder by 8K@30fps, and AV1 decoder by 4K@60fps, also support H.264 and H.265 encoder by 8K@30fps, high-quality JPEG encoder/decoder, specialized image preprocessor and postprocessor.

Embedded 3D GPU makes RK3588C completely compatible with OpenGLES 1.1, 2.0, and 3.2, OpenCL up to 2.2 and Vulkan1.2. Special 2D hardware engine with MMU will maximize display performance and provide very smoothly operation.

The build-in NPU supports INT4/INT8/INT16/FP16 hybrid operation and computing power is up to 6TOPs. In addition, with its strong compatibility, network models based on a series of frameworks such as TensorFlow/MXNet/PyTorch/Caffe can be easily converted.

RK3588C has high-performance quad channel external memory interface (LPDDR4/LPDDR4X) capable of sustaining demanding memory bandwidths, also provides a complete set of peripheral interface to support very flexible applications.

1.2 Features

1.2.1 Microprocessor

- Quad-core ARM Cortex-A76 MPCore processor and quad-core ARM Cortex-A55 MPCore processor, both are high-performance, low-power and cached application processor
- DSU (DynamIQ Shared Unit) comprises the L3 memory system, control logic, and external interfaces to support a DynamIQ cluster
- Full implementation of the ARM architecture v8-A instruction set, ARM Neon Advanced SIMD (single instruction, multiple data) support for accelerating media and signal processing
- ARMv8 Cryptography Extensions
- Trustzone technology support
- Integrated 64KB L1 instruction cache, 64KB L1 data cache and 512KB L2 cache for each Cortex-A76
- Integrated 32KB L1 instruction cache, 32KB L1 data cache and 128KB L2 cache for each Cortex-A55
- Quad-core Cortex-A76 and Quad-core Cortex-A55 share 3MB L3 cache
- Eight separate power domains for CPU core system to support internal power switch and externally turn on/off based on different application scenario
  - PD_CPU_0: 1st Cortex-A55 + Neon + FPU + L1/L2 I/D Cache
  - PD_CPU_1: 2nd Cortex-A55 + Neon + FPU + L1/L2 I/D Cache
  - PD_CPU_2: 3rd Cortex-A55 + Neon + FPU + L1/L2 I/D Cache
  - PD_CPU_3: 4th Cortex-A55 + Neon + FPU + L1/L2 I/D Cache
  - PD_CPU_4: 1st Cortex-A76 + Neon + FPU + L1/L2 I/D Cache
  - PD_CPU_5: 2nd Cortex-A76 + Neon + FPU + L1/L2 I/D Cache
  - PD_CPU_6: 3rd Cortex-A76 + Neon + FPU + L1/L2 I/D Cache
  - PD_CPU_7: 4th Cortex-A76 + Neon + FPU + L1/L2 I/D Cache
- Three isolated voltage domains to support DVFS, one for A76_0 and A76_1, one for A76_2 and A76_3, the other for DSU and Cortex-A55.

1.2.2 Memory Organization

- Internal on-chip memory
  - BootRom
    - Support system boot from the following device:
      - SPI interface

        - eMMC interface
        - SD/MMC interface
      - Support system code download by the following interface:
        - USB OTG interface
  - Share Memory in the voltage domain of VD_LOGIC
  - PMU SRAM in VD_PMU for low power application
- External off-chip memory
  - Dynamic Memory Interface
    - Compatible with JEDEC standards LPDDR4/LPDDR4X
    - Support four channels, each channel 16bits data widths
    - Support up to 2 ranks (chip selects) for each channel
    - Totally up to 32GB address space
    - Low power modes, such as power-down and self-refresh for SDRAM
  - eMMC Interface
    - Fully compliant with JEDEC eMMC 5.1 and eMMC 5.0 specification
    - Backward compliant with eMMC 4.51 and earlier versions specification.
    - Support HS400, HS200, DDR50 and legacy operating modes
    - Support three data bus width: 1bit, 4bits or 8bits
  - SD/MMC Interface
    - Compatible with SD3.0, MMC ver4.51
    - Data bus width is 4bits
  - Flexible Serial Peripheral Interface(FSPI)
    - Support transfer data from/to serial flash device
    - Support 1bit, 2bits or 4bits data bus width
    - Support 2 chips select

1.2.3 System Component

- MCU
  - Three Cortex-M0 MCUs inside RK3588C
  - MCU in VD_PMU integrate 16KB Cache and 16KB TCM
  - MCU in VD_NPU integrate 16KB Cache and 64KB TCM
  - MCU in PD_CENTER integrate 32KB TCM
  - Integrated Programmable Interrupt Controller, all IRQ lines connected to GIC for CPU also connect to MCU in VD_PMU(PMU_M0) and PD_CENTER(DDR_M0)
  - Integrated Debug Controller with JTAG interface
- CRU (clock & reset unit)
  - Support total 18 PLLs to generate all clocks
  - One oscillator with 24MHz clock input
  - Support clock gating control for individual components
  - Support global soft-reset control for whole chip, also individual soft-reset for each component
- PMU(power management unit)
  - Multiple configurable work modes to save power by different frequency or automatic clock gating control or power domain on/off control
  - Lots of wakeup sources in different mode
  - Support 10 separate voltage domains
  - Support 45 separate power domains, which can be power up/down by software based on different application scenes
- Timer
  - Support 12 secure timers with 64bits counter and interrupt-based operation
  - Support 18 non-secure timers with 64bits counter and interrupt-based operation
  - Support two operation modes: free-running and user-defined count for each timer
  - Support timer work state checkable
- PWM
  - Support 16 on-chip PWMs(PWM0~PWM15) with interrupt-based operation
  - Programmable pre-scaled operation to bus clock and then further scaled
  - Embedded 32-bit timer/counter facility
  - Support capture mode
  - Support continuous mode or one-shot mode

- Provides reference mode and output various duty-cycle waveform
- Optimized for IR application for PWM3, PWM7, PWM11, PWM15

- Watchdog
  - 32-bit watchdog counter
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - Generate a system reset
    - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
  - Totally five Watchdog for CPU and MCU
- Interrupt Controller
  - Support 12 PPI interrupt source and 480 SPI interrupt sources input from different components inside RK3588C
  - Support 16 software-triggered interrupts
  - Input interrupt level is fixed, high-level sensitive for SPI and low-level sensitive for PPI
  - Support different interrupt priority for each interrupt source, and they are always software-programmable
- DMAC
  - Micro-code programming based DMA
  - Linked list DMA function is supported to complete scatter-gather transfer
  - Support data transfer types including memory-to-memory, memory-to-peripherals, peripherals-to-memory
  - Totally three embedded DMA controllers for peripheral system
  - Each DMAC features:
    - Support 8 channels
    - 32 hardware request from peripherals
    - 2 interrupt output
    - Support TrustZone technology and programmable secure state for each DMA channel
- Secure System
  - Embedded two cipher engine
    - Support Link List Item (LLI) DMA transfer
    - Support SHA-1, SHA-256/224, SHA-512/384, MD5, SM3 with hardware padding
    - Support HMAC of SHA-1, SHA-256, SHA-512, MD5, SM3 with hardware padding
    - Support AES-128, AES-192, AES-256 encrypt & decrypt cipher
    - Support AES ECB/CBC/OFB/CFB/CTR/CTS/XTS/CCM/GCM/CBC-MAC/CMAC mode
    - Support SM4 ECB/CBC/OFB/CFB/CTR/CTS/XTS/CCM/GCM/CBC-MAC/CMAC mode
    - Support DES & TDES cipher, with ECB/CBC/OFB/CFB mode
    - Support up to 4096 bits PKA mathematical operations for RSA/ECC/SM2
    - Support generating random numbers
  - Support keyladder to guarantee key secure
  - Support data scrambling for all DDR types
  - Support secure OTP
  - Support secure debug
  - Support secure DFT test
  - Support secure OS
  - Except CPU, the other masters in the SoC can also support security and non-security mode by software-programmable
  - Some slave components in SoC can only be addressed by security master and the other slave components can be addressed by security master or non-security master by software-programmable
  - System SRAM(share memory), part of space is addressed only in security mode
  - External DDR space can be divided into 16 parts, each part can be software-programmable to be enabled by each master

- Mailbox
  - Three Mailbox in SoC to service CPU and MCU communication
  - Support four mailbox elements per mailbox, each element includes one data word, one command word register and one flag bit that can represent one interrupt
  - Provide 32 lock registers for software to use to indicate whether mailbox is occupied
- Decompression
  - Support for decompressing GZIP files
  - Support for decompressing LZ4 files, including the General Structure of LZ4 Frame format and the Legacy Frame format.
  - Support for decompressing data in DEFLATE format
  - Support for decompressing data in ZLIB format
  - Support Hash32 check in LZ4 decompression process
  - Support the limit size function of the decompressed data to prevent the memory from being maliciously destroyed during the decompression process

1.2.4 Video CODEC

- Video Decoder
  - Real-time video decoder of MPEG-1, MPEG-2, MPEG-4, H.263, H.264, H.265, VC-1, VP9, VP8, MVC, AV1
  - MMU Embedded
  - Multi-channel decoder in parallel for less resolution
  - H.264 AVC/MVC Main10 L6.0 : 8K@30fps (7680x4320)②
  - VP9 Profile0/2 L6.1 : 8K@60fps (7680x4320)
  - H.265 HEVC/MVC Main10 L6.1 : 8K@60fps (7680x4320)
  - AVS2 Profile0/2 L10.2.6 : 8K@60fps (7680x4320)
  - AV1 Main Profile 8/10bit L5.3 : 4K@60fps (3840x2160)
  - MPEG-2 up to MP : 1080p@60fps (1920x1088)
  - MPEG-1 up to MP : 1080p@60fps (1920x1088)
  - VC-1 up to AP level 3 : 1080p@60fps (1920x1088)
  - VP8 version2 : 1080p@60fps (1920x1088)
- Video Encoder
  - Real-time H.265/H.264 video encoding
  - Support up to 8K@30fps
  - Multi-channel encoder in parallel for less resolution

1.2.5 JPEG CODEC

- JPEG Encoder
  - Baseline (DCT sequential)
  - Encoder size is from 96x96 to 8192x8192(67Mpixels)
  - Up to 90 million pixels per second
  - Embedded four encoder units
- JPEG Decoder
  - Decoder size is from 48x48 to 65536x65536
  - Support YUV400/YUV411/YUV420/YUV422/YUV440/YUV444
  - Support up to 1080P@280fps, and 560 million pixels per second
  - Support MJPEG
  - Embedded four encoder units

1.2.6 Neural Process Unit

- Neural network acceleration engine with processing performance up to 6 TOPS
- Include triple NPU core, and support triple core co-work, dual core co-work, and work independently
- Support integer 4, integer 8, integer 16, float 16, Bfloat 16 and tf32 operation
- Embedded 384KBx3 internal buffer
- Multi-task, multi-scenario in parallel
- Support deep learning frameworks: TensorFlow, Caffe, Tflite, Pytorch, Onnx NN, Android NN, etc.
- One isolated voltage domain to support DVFS

1.2.7 Graphics Engine

- 3D Graphics Engine
  - ARM Mali-G610 MP4
  - High performance OpenGLES 1.1, 2.0 and 3.2, OpenCL 2.2, Vulkan1.2 etc.
  - Embedded 4 shader cores with shared hierarchical tiler
  - Provide MMU and L2 Cache with 4x 256KB size
  - The latest Valhall architecture
  - ARM Frame Buffer Compression(AFBC) 1.3
  - Support Serial Wire debug for embedded MCU
  - One isolated voltage domain to support DVFS
- 2D Graphics Engine
  - Source format: ARGB/RGB888/RGB565/YUV420/YUV422/BPP
  - Destination formats: ARGB/RGB888/RGB565/YUV420/YUV422
  - Max resolution: 8192x8192 source, 4096x4096 destination
  - Block transfer and Transparency mode
  - Color fill with gradient fill, and pattern fill
  - Alpha blending modes including global alpha, per pixel alpha (color/alpha channel separately) and fading
  - Arbitrary non-integer scaling ratio, from 1/8 to 8
  - 0, 90, 180, 270 degree rotation, x-mirror, y-mirror & rotation operation
  - ROP2, ROP3, ROP4
  - Support 4k/64k page size MMU
- Image Enhancement Processor
  - Image format
    - Input data: YUV420/YUV422, semi-planar/planar, UV swap
    - Output data: YUV420/YUV422, semi-planar, UV swap, Tile mode
    - YUV down sampling conversion from 422 to 420
    - Max resolution for dynamic image up to 1920x1080
  - De-interlace

1.2.8 Video Input Interface

- DVP interface
  - One 8/10/12/16-bit standard DVP interface, up to 150MHz input data
  - Support BT.601/BT.656 and BT.1120 VI interface
  - Support the polarity of pixel_clk, hsync, vsync configurable

1.2.9 Display interface

- HDMI2.1 TX interface
  - Support one HDMI2.1 TX interface
  - Support x3 and x4 configuration for HDMI2.1 FRL mode
  - Backward compliant with HDMI2.1 TMDS and earlier versions specification
  - Support all the data rates for HDMI FRL: 3, 6, 8, 10 and 12Gbps
  - Support up to 7680x4320@60Hz for HDMI TX
  - Support RGB/YUV(up to 10bit) format for HDMI TX
  - Support DSC 1.2a for HDMI TX
  - Support HDCP2.3 for HDMI TX
- HDMI2.0/eDP1.4 TX interface
  - Support 1 HDMI2.0/eDP1.4 TX combo interface, but HDMI and eDP can not work at the same time for each interface
  - Support x1, x2 and x4 configuration for eDP
  - Support 1.62Gbps, 2.7Gbps and 5.4Gbps for eDP
  - Support up to 4096x2160@60Hz for HDMI TX, and 4K@60Hz for eDP
  - Support RGB/YUV(up to 10bit) format for HDMI TX
  - Support RGB, YCbCr 4:4:4, YCbCr 4:2:2 and 8/10 bit per component video format for eDP
  - Support DSC 1.2a for HDMI TX
  - Support HDCP2.3 for HDMI TX, and HDCP1.3 for eDP
  - Requirement of HDMI TX interface video timing
    - Suggest following CTA-861 standard
    - When the video timing is not standard, HSYNC/HBP/HFP is suggested 4 pixel

aligned
- DP TX interface
  - Support 1 DP TX 1.4a interface which combo with USB3.1 Gen1
  - Support 1/2/4lanes for each interface
  - Support 1.62Gbps, 2.7Gbps, 5.4Gbps and 8.1Gbps Serializer
  - Support up to 7680x4320@30Hz
  - Support RGB/YUV(up to 10bit) format
  - Support Single Stream Transport(SST)
  - Support DP Alt mode on USB Type-C
  - Support HDCP2.3, HDCP 1.3
  - Requirement of interface video timing
    - Suggest following the CTA-861 standard
    - When the video timing is not standard, the Min value of HSYNC/HBP/HFP is 16 pixel
- BT.1120 video output interface
  - Support up to 1920x1080@60Hz
  - Up to 150MHz data rate

1.2.10 Video Output Processor

- Video ports
  - Video Port0, max output resolution: 7680x4320@60Hz
  - Video Port1, max output resolution: 4096x4320@60Hz
  - Video Port2, max output resolution: 4096x4320@60Hz
  - Video Port3, max output resolution: 2048x1080@60Hz
- Cluster 0/1/2/3
  - Max input and output resolution 4096x4320
  - Support AFBCD
  - Support RGB/YUV/YUYV format
  - Support scale up/down ratio 4~1/4
  - Support rotation
- ESMART 0/1/2/3
  - Max input and output resolution 4096x4320
  - Support RGB/YUV/YUYV format
  - Support scale up/down ratio 8~1/8
  - Support 4 region
- Overlay
  - Support up to 8 layers overlay: 4 cluster/4 esmart
  - Support RGB/YUV domain overlay
- Post process
  - HDR
    - HDR10/HDR HLG
    - HDR2SDR/SDR2HDR
  - 3D-LUT/P2I/CSC/BCSH/DITHER/CABC/GAMMA/COLORBAR
- Write back
  - Format: ARGB8888/RGB888/RGB565/YUV420
  - Max resolution: 1920x1080
- Requirement of VOP interface video timing
  - HACTIVE must be 4 pixel aligned
  - When enabling split mode or MIPI dual channel mode or yuv420 format, the POST HSYNC/HBP/HFP must be 2 pixel aligned
  - When enabling MIPI DSC video mode, the min value of POST HSYNC/HBP/HFP is 16 pixel, the Min value of DSC_SYS_CTRL HSYNC/HBP/HFP is 8 pixel

1.2.11 Audio Interface

- I2S1 with 8 channels
  - Up to 8 channels TX and 8 channels RX path
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal, left-justified, right-justified)

  - Support 4 PCM formats (early, late1, late2, late3)
  - Support TDM normal, 1/2 cycle left shift, 1 cycle left shift, 2 cycle left shift, right shift mode serial audio data transfer
  - I2S, PCM and TDM mode cannot be used at the same time
- I2S0 with 4 channels
  - Up to 4 channels TX or 4 channels RX path
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal, left-justified, right-justified)
  - Support 4 PCM formats (early, late1, late2, late3)
  - Support TDM normal, 1/2 cycle left shift, 1 cycle left shift, 2 cycle left shift, right shift mode serial audio data transfer
  - I2S, PCM and TDM mode cannot be used at the same time
- I2S2/I2S3 with 2 channels
  - Up to 2 channels for TX and 2 channels RX path
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal, left-justified, right-justified)
  - Support 4 PCM formats (early, late1, late2, late3)
  - I2S and PCM cannot be used at the same time
- SPDIF0/SPDIF1
  - Support two 16-bit audio data store together in one 32-bit wide location
  - Support biphase format stereo audio data output
  - Support 16 to 31 bit audio data left or right justified in 32-bit wide sample data buffer
  - Support 16, 20, 24 bits audio data transfer in linear PCM mode
  - Support non-linear PCM transfer
- PDM0/PDM1
  - Up to 8 channels
  - Audio resolution from 16bits to 24bits
  - Sample rate up to 192KHz
  - Support PDM master receive mode
- Digital Audio Codec
  - Support 2 channels digital DAC
  - Support I2S/PCM interface, master and slave mode
  - Support 16 bit sample resolution
  - Support three modes of mixing for every digital DAC channel
  - Support volume control
- VAD(Voice Activity Detection)
  - Support read voice data from I2S/PDM
  - Support voice amplitude detection
  - Support Multi-Mic array data storing
  - Support a level combined interrupt

1.2.12 Connectivity

- SDIO interface
  - Compatible with SDIO3.0 protocol
  - 4-bit data bus widths
- GMAC 10/100/1000M Ethernet controller
  - Support two Ethernet controllers
  - Support 10/100/1000-Mbps data transfer rates with the RGMII interfaces
  - Support 10/100-Mbps data transfer rates with the RMII interfaces
  - Support both full-duplex and half-duplex operation
- USB3.1 Gen1
  - Support USB3.1 Gen1, equal to USB3.2 Gen1 and USB3.0, up to 5Gbps datarate
  - Embedded 1 USB3.1 OTG interfaces which combo with DP TX (USB3OTG_0)
  - Embedded 1 USB3.1 Host interface which combo with Combo PIPE PHY2

(USB3OTG_2)
- Compatible Specification
  - Universal Serial Bus 3.0 Specification, Revision 1.0
  - Universal Serial Bus Specification, Revision 2.0 (exclude USB3OTG_2)
  - eXtensible Host Controller Interface for Universal Serial Bus (xHCI), Revision 1.1
- Support Control/Bulk (including stream)/Interrupt/Isochronous Transfer
- Simultaneous IN and OUT transfer for USB3.1 Gen1
- Descriptor caching and data pre-fetching used to improve system performance in high-latency systems
- LPM protocol in USB 2.0 (exclude USB3OTG_2) and U0, U1, U2, and U3 states for USB3.1 Gen1
- USB3.1 Gen1 Device Features
  - Up to 10 IN endpoints, including control endpoint 0
  - Up to 6 OUT endpoints, including control endpoint 0
  - Up to 16 endpoint transfer resources, each one for each endpoint
  - Flexible endpoint configuration for multiple applications/USB set-configuration modes
  - Hardware handles ERDY and burst
  - Stream-based bulk endpoints with controller automatically initiating data movement
  - Isochronous endpoints with isochronous data in data buffers
  - Flexible Descriptor with rich set of features to support buffer interrupt moderation, multiple transfers, isochronous, control, and scattered buffering support
- USB3.1 Gen1 xHCI Host Features
  - Support up to 64 devices
  - Support 1 interrupter
  - Support 1 USB2.0 port (exclude USB3OTG_2) and 1 Super-Speed port
  - Support standard or open-source xHCI and class driver
- USB3.1 Gen1 Dual-Role Device (DRD) Features
  - Static Device Operation
  - Static Host Operation
  - USB3.1/USB2.0 OTG A device and B device basing on ID, USB3OTG_2 only support USB3.1 Gen1
  - Not Support USB3.1/USB2.0 OTG session request protocol (SRP), host negotiation protocol (HNP) and Role Swap Protocol (RSP)
- Miscellaneous Features
  - USB2.0 PHY support Battery Charge detection
  - USB3OTG_0 support USB Type-C and DP Alt Mode
  - USB3OTG_2 PHY combos with PCIE and SATA

- USB20 OTG
  - Compatible Specification
    - Universal Serial Bus Specification, Revision 2.0 (exclude USB3OTG_2)
    - eXtensible Host Controller Interface for Universal Serial Bus (xHCI), Revision 1.1
  - Support Control/Bulk (including stream)/Interrupt/Isochronous Transfer
  - Descriptor caching and data pre-fetching used to improve system performance in high-latency systems
  - Miscellaneous Features
    - USB2.0 PHY support Battery Charge detection
  - Dual-Role Device (DRD) Features
    - Static Device Operation
    - Static Host Operation
    - USB2.0 OTG A device and B device basing on ID
    - Not Support USB2.0 OTG session request protocol (SRP), host negotiation protocol (HNP) and Role Swap Protocol (RSP)

- USB2.0 Device Features
  - Up to 10 IN endpoints, including control endpoint 0
  - Up to 6 OUT endpoints, including control endpoint 0
  - Up to 16 endpoint transfer resources, each one for each endpoint
  - Flexible endpoint configuration for multiple applications/USB set-configuration modes
- USB2.0 xHCI Host Features
  - Support up to 64 devices
  - Support 1 interrupter

  Support 1 USB2.0 port

- USB 2.0 Host
  - Compatible with USB 2.0 specification
  - Support two USB 2.0 Host
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Support Enhanced Host Controller Interface Specification (EHCI), Revision 1.0
  - Support Open Host Controller Interface Specification (OHCI), Revision 1.0a
  -
- Combo PIPE PHY Interface
  - Support three Combo PIPE PHYs with PCIe2.1/SATA3.0/USB3.1 controller
  - Combo PIPE PHY0 support one of the following interfaces
    - SATA
    - PCIe2.1
  - Combo PIPE PHY1 support one of the following interfaces
    - SATA
    - PCIe2.1
  - Combo PIPE PHY2 support one of the following interfaces
    - SATA
    - PCIe2.1
    - USB3.1 Gen1
  - PCIe2.1 Interface
    - Compatible with PCI Express Base Specification Revision 2.1
    - Support 1 lane for each PCIe2.1 interface
    - Support Root Complex(RC) only
    - Support 5Gbps data rate
  - SATA Interface
    - Compatible with Serial ATA 3.1 and AHCI revision 1.3.1
    - Support eSATA
    - Support 1 port for each SATA interface
    - Support 6Gbps data rate
- PCIe3.0 Interface
  - Compatible with PCI Express Base Specification Revision 3.0
  - Support dual operation mode: Root Complex(RC) and End Point(EP)
  - Support data rates: 2.5Gbps(PCIe1.1), 5Gbps(PCIe2.1), 8Gps(PCIe3.0)
  - Support aggregation and bifurcation with 1x 2lanes, 2x 1lanes
- SPI interface
  - Support 5 SPI Controllers(SPI0-SPI4)
  - Support two chip-select output
  - Support serial-master and serial-slave mode, software-configurable
- I2C Master controller
  - Support 9 I2C Master(I2C0-I2C8)
  - Support 7bits and 10bits address mode
  - Software programmable clock frequency
  - Data on the I2C-bus can be transferred at rates of up to 100k bits/s in the Standard-mode, up to 400k bits/s in the Fast-mode
- UART interface
  - Support 10 UART interfaces(UART0-UART9)
  - Embedded two 64-byte FIFO for TX and RX operation respectively

- Support 5bit, 6bit, 7bit, 8bit serial data transmit or receive
- Standard asynchronous communication bits such as start, stop and parity
- Support different input clock for UART operation to get up to 4Mbps baud rate
- Support auto flow control mode for all UART

1.2.13 Others

- Multiple group of GPIO
  - All of GPIOs can be used to generate interrupt
  - Support level trigger and edge trigger interrupt
  - Support configurable polarity of level trigger interrupt
  - Support configurable rising edge, falling edge and both edge trigger interrupt
  - Support configurable pull direction(a weak pull-up and a weak pull-down)
  - Support configurable drive strength
- Temperature Sensor (TS-ADC)
  - Support User-Defined Mode and Automatic Mode
  - In User-Defined Mode, start_of_conversion can be controlled completely by software, and also can be generated by hardware.
  - In Automatic Mode, the temperature of alarm(high/low temperature) interrupt can be configurable
  - In Automatic Mode, the temperature of system reset can be configurable
  - Support to 7 channel TS-ADC, the temperature criteria of each channel can be configurable
  - -40~125°C temperature range and 1°C temperature resolution
- Successive approximation ADC (SARADC)
  - 12-bit resolution
  - Up to 1MS/s sampling rate
  - 4 single-ended input channels
- OTP
  - Support 32Kbit space and higher 4k address space is non-secure part.
  - Support read and program word mask in secure model
  - Support maximum 32 bit OTP program operation
  - Support maximum 16 word OTP read operation
  - Program and Read state can be read
  - Program fail address record
- Package Type
  - FCCSP766L (body: 17mm x 19mm; ball size: 0.3mm; ball pitch: 0.6mm&0.65mm)

1.3 Block Diagram

The following figure shows the basic block diagram.

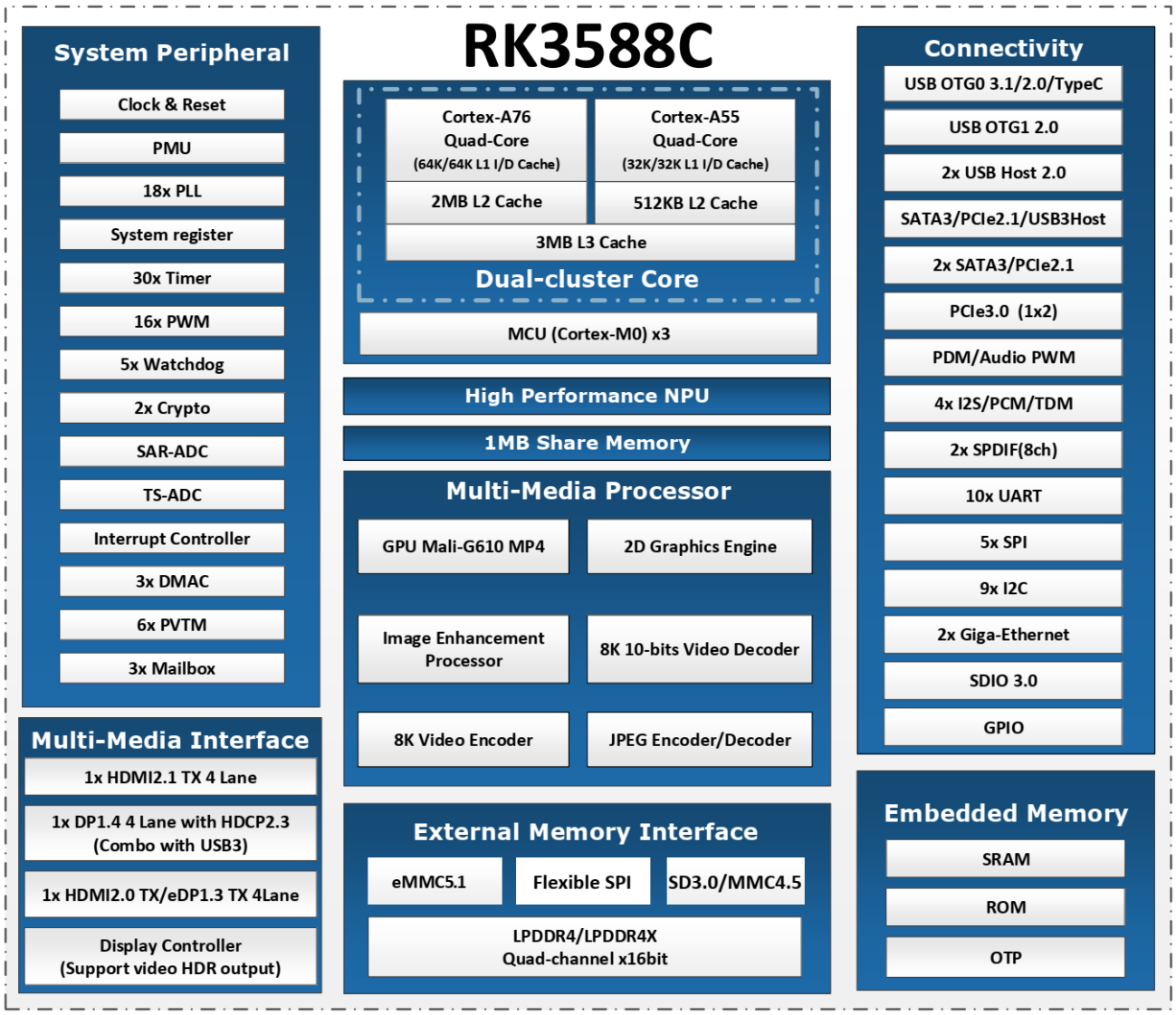

Fig. 1-1 Block Diagram

Chapter 2 Package Information

2.1 Order Information

Orderable Device	RoHS status	Package	Package QTY	Device Feature
RK3588C	RoHS	ED-FCCSP 17x19 766L	840PCS by tray	Application processor

2.2 Top Marking

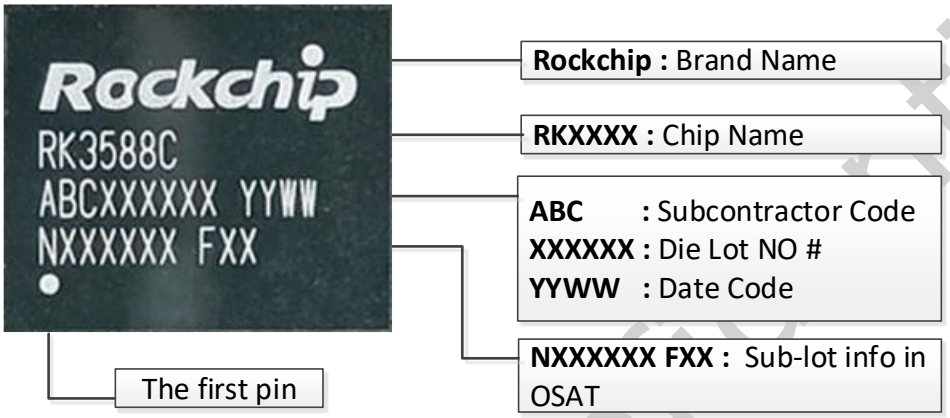

Fig. 2-1 Package definition

2.3 Package Dimension

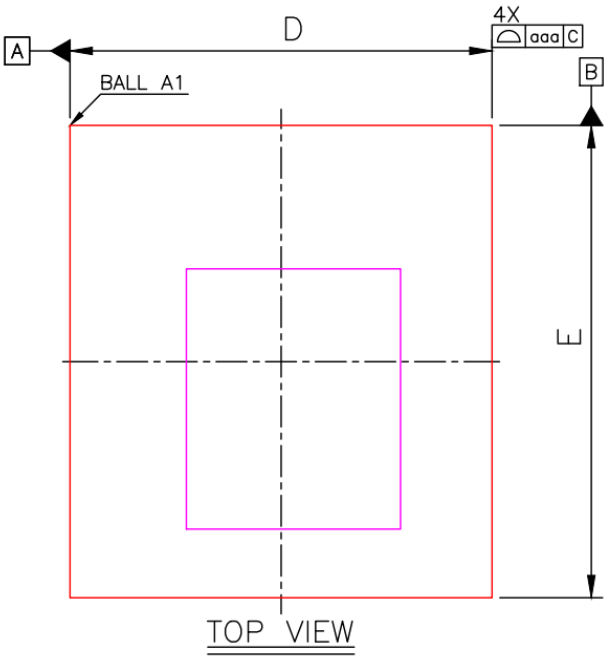

Fig. 2-2 Package Top View

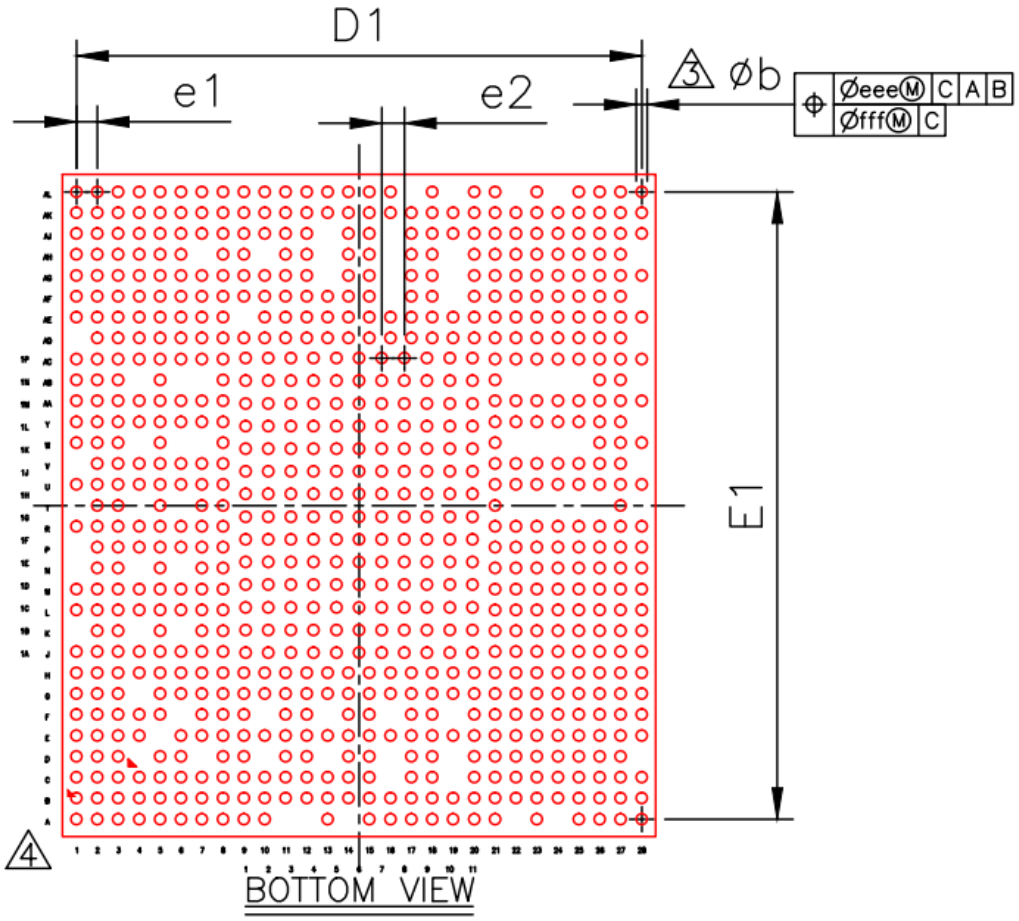

Fig. 2-3 Package Bottom View

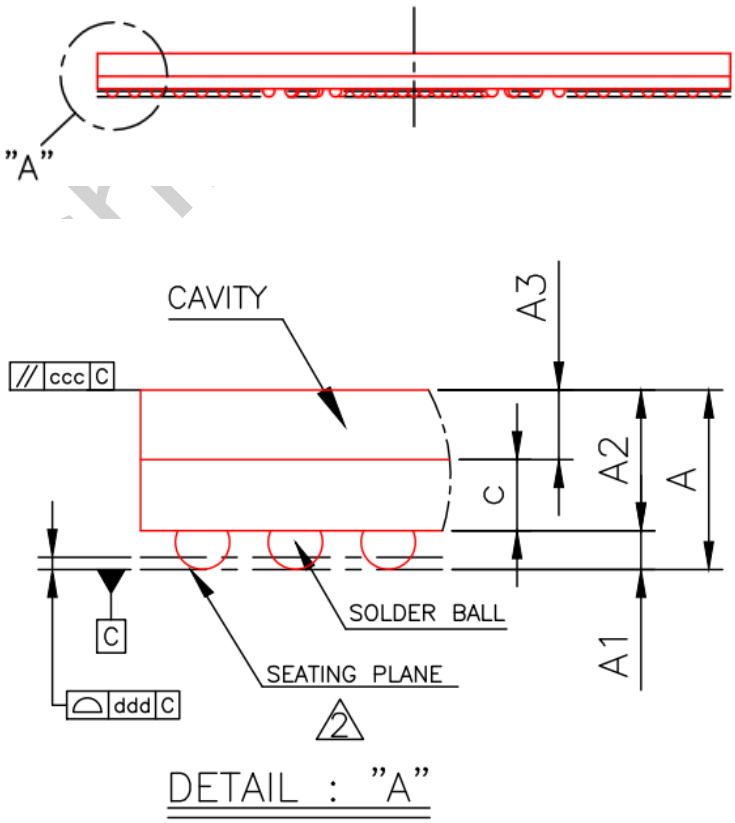

Fig. 2-4 Package Side View

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.04	1.150	1.221	0.041	0.045	0.048
A1	0.160	0.210	0.260	0.006	0.008	0.010
A2	0.860	0.940	0.990	0.034	0.037	0.039
A3	0.570	0.600	0.630	0.022	0.024	0.025
c	0.300	0.340	0.380	0.012	0.013	0.015
D	16.900	17.000	17.100	0.665	0.669	0.673
E	18.900	19.000	19.100	0.744	0.748	0.752
D1	---	16.200	---	---	0.638	---
E1	---	18.000	---	---	0.709	---
e1	---	0.600	---	---	0.024	---
e2	---	0.650	---	---	0.026	---
b	0.260	0.310	0.360	0.010	0.012	0.014
aaa	0.150			0.006		
ccc	0.200			0.008		
ddd	0.150			0.006		
eee	0.150			0.006		
fff	0.080			0.003		

Fig. 2-5 Package Dimension

2.4 MSL Information

Moisture sensitivity level ： MSL3

2.5 Lead Finish/Ball Material Information

Lead finish/Ball material ： SnAgCu

2.6 Pin Number List

Table 2-1 Pin Number Order Information

Pin Name	Pin	Pin Name	Pin
VSS_1	A1	RFU3	F22
DDR_CH1_DQ10_C	A2	I2S0_SDO2/I2S0_SDI3/PDM0_SDI1_M0/GPIO1_D1	F23
DDR_CH1_DQ8_C	A3	PDM1_CLK1_M1/PCIE30X1_0_WAKEN_M2/SATA0_ACT_LED _M1/UART4_TX_M2/SPI0_CLK_M2/GPIO1_B3	F24
DDR_CH1_DQ14_C	A4	VOP_POST_EMPTY/I2C4_SDA_M3/UART6_RTSN_M1/PWM0_ M2/SPI4_CLK_M2/GPIO1_A2	F25
DDR_CH1_DQ12_C	A5	VSS_40	F26
DDR_CH1_DM0_C	A6	PCIE30_PORT0_TX0N	F27
DDR_CH1_DQ5_C	A7	PCIE30_PORT0_TX0P	F28
DDR_CH1_DQ0_C	A8	VSS_39	F21
DDR_CH1_DQ2_C	A9	DDR_CH0_DQ13_B	G1
VSS_2	A10	DDR_CH0_DQ14_B	G2
DDR_CH1_A2_D	A13	VSS_41	G3
DDR_CH1_DQ2_D	A15	DDR_CH0_DQS1N_B	G5
DDR_CH1_DQ0_D	A16	VSS_42	G6
DDR_CH1_DQ12_D	A17	VSS_43	G7
DDR_CH1_DQ14_D	A18	DDR_CH1_A2_C	G8
DDR_CH1_DQ8_D	A19	VSS_44	G9
DDR_CH1_DQ10_D	A20	VSS_45	G10
DDR_CH1_DM0_D	A21	DDR_CH1_A5_C	G11
PDM1_SDI0_M1/PCIE30X1_1_PERSTN_M2/PWM3_IR_M3/SP I2_CS0_M0/GPIO1_A7	A23	VSS_46	G12
I2C8_SDA_M2/UART1_CTSN_M1/PWM15_IR_M3/GPIO1_D7	A25	VSS_47	G13

I2C8_SCL_M2/UART1_RTSN_M1/PWM14_M2/GPIO1_D6	A26	DDR_CH1_A1_D	G14
SPDIF0_TX_M0/I2C5_SCL_M3/UART1_TX_M1/GPIO1_B6	A27	VSS_48	G15
VSS_3	A28	VSS_49	G16
DDR_CH0_DQ9_A	AA1	DDR_CH1_LP4/4X_CS0_D	G17
DDR_CH0_DQ8_A	AA2	VSS_50	G18
VSS_117	AA3	VSS_51	G19
VSS_118	AA4	DDR_CH1_DQ6_D	G20
DDR_CH0_DQ13_A	AA5	RFU1	G21
DDR_CH0_DQ12_A	AA6	RFU4	G22
VSS_119	AA7	VSS_52	G23
VSS_120	AA8	VSS_53	G24
VSS_121	AA21	VSS_54	G25
VCCIO5_1V8	AA22	VSS_55	G26
GMAC1_MDC/I2C8_SCL_M4/UART7_RTSN_M1/PWM14_M0/SPI1_CS0_M1/GPIO3_C2	AA23	PCIE30_PORT0_RX1N	G27
EMMC_RSTN/I2C2_SCL_M2/UART5_RTSN_M1/GPIO2_A3	AA24	PCIE30_PORT0_RX1P	G28
EMMC_CLKOUT/GPIO2_A1	AA25	DDR_CH0_DQ7_B	H1
GMAC1_RXD3/SDIO_D3_M1/I2S3_SDO/AUDDSM_RN/FSPI_D3_M2/UART8_RX_M1/SPI4_CS0_M1/GPIO3_A3	AA26	DDR_CH0_DQ12_B	H2
EMMC_D7/FSPI_CS1N_M0/GPIO2_D7	AA27	VSS_56	H3
I2S1_MCLK_M1/JTAG_TCK_M2/I2C1_SCL_M0/UART2_TX_M0/PCIE30X1_1_CLKREQN_M0/GPIO0_B5	AA28	DDR_CH0_DQS0P_B	H4
DDR_CH0_DM1_A	AB1	DDR_CH0_DQS0N_B	H5
DDR_CH0_DQ11_A	AB2	VSS_57	H6
VSS_122	AB3	VSS_58	H7
VSS_123	AB5	DDR_CH1_ZQ_C	H8
AVSS_2	AB8	VSS_59	H9
VCCIO3_1V8	AB21	VSS_60	H10
EMMC_D6/FSPI_CS0N_M0/GPIO2_D6	AB26	VSS_61	H11
EMMC_D2/FSPI_D2_M0/GPIO2_D2	AB27	VSS_62	H12
DDR_CH0_DQ10_A	AC1	VSS_63	H13
VSS_124	AC2	VSS_64	H14
VSS_125	AC3	VSS_65	H15
DDR_CH0_DQS1N_A	AC4	VSS_66	H16
DDR_CH0_DQS1P_A	AC5	VSS_67	H17
VSS_126	AC6	VSS_68	H18
AVSS_3	AC7	DDR_CH1_ZQ_D	H19
HDMI_TX0_VDD_0V75	AC8	VSS_69	H20
VCCIO6_1V8	AC21	VSS_70	H21
ETH0_REFCLKO_25M/I2S2_SDI_M0/I2C6_SCL_M2/SPI1_CS0_M0/GPIO2_C3	AC22	VSS_71	H22
EMMC_CMD/FSPI_CLK_M0/GPIO2_A0	AC23	VSS_72	H23
VSS_127	AC24	PCIE30_PORT0_REF_CLKP	H24
EMMC_DATA_STROBE/I2C2_SDA_M2/UART5_CTSN_M1/GPIO2_A2	AC25	PCIE30_PORT0_REF_CLKN	H25
EMMC_D1/FSPI_D1_M0/GPIO2_D1	AC26	VSS_73	H26
EMMC_D4/I2C1_SCL_M3/UART5_RX_M2/GPIO2_D4	AC27	PCIE30_PORT0_RX0N	H27
EMMC_D0/FSPI_D0_M0/GPIO2_D0	AC28	PCIE30_PORT0_RX0P	H28
SDMMC_D0/PDM1_SDI3_M0/JTAG_TCK_M1/I2C3_SCL_M4/UART2_TX_M1/PWM8_M1/GPIO4_D0	AD2	DDR_CH0_DQ1_B	J1
SDMMC_D1/PDM1_SDI2_M0/JTAG_TMS_M1/I2C3_SDA_M4/UART2_RX_M1/PWM9_M1/GPIO4_D1	AD3	DDR_CH0_DQ0_B	J2
SDMMC_CMD/PDM1_CLK1_M0/MCU_JTAG_TCK_M0/UART5_RX_M0/PWM7_IR_M1/GPIO4_D4	AD4	DDR_CH0_DQ2_B	J3
VSS_128	AD5	VSS_74	J4
VSS_129	AD6	DDR_CH0_LP4/4X_CS0_B	J5
AVSS_4	AD7	VSS_75	J6
HDMI_TX0_VDD_IO_1V8	AD8	DDR_CH0_ZQ_B	J7
HDMI/eDP_TX1_VDD_0V75	AD9	VSS_76	J8
HDMI/eDP_TX1_AVDD_0V75	AD10	VSS_77	J21
VSS_130	AD11	PCIE30_PORT0_RESREF	J22
VSS_131	AD12	AVSS1_1	J23
VDD_GPU_9	AD13	PCIE20_2_REFCLKP	J24
VDD_GPU_10	AD14	PCIE20_2_REFCLKN	J25
VSS_132	AD15	AVSS1_2	J26
VSS_133	AD16	PCIE20_2_TXP/SATA30_2_TXP/USB30_SSTXP	J27
VSS_134	AD17	PCIE20_2_TXN/SATA30_2_TXN/USB30_SSTXN	J28

VSS_135	AD18	DDR_CH0_DQ3_B	K2
VSS_136	AD19	VSS_78	K3
VSS_137	AD20	VSS_79	K5
VSS_138	AD21	VSS_80	K7
VSS_139	AD22	DDR_CH01_VDDQ_CKE	K8
VSS_140	AD23	VSS_81	K21
RFU8	AD24	PCIE30_PORT0_AVDD0V75	K22
GMAC0_TXD2/SDIO_D3_M0/I2C8_SDA_M1/UART6_CTSN_M0/GPIO2_B1	AD25	AVSS1_3	K23
EMMC_D3/FSPI_D3_M0/GPIO2_D3	AD26	AVSS1_4	K24
EMMC_D5/I2C1_SDA_M3/UART5_TX_M2/GPIO2_D5	AD27	AVSS1_5	K25
HDMI_TX0_D3N	AE1	AVSS1_6	K26
AVSS_5	AE2	PCIE20_2_RXN/SATA30_2_RXN/USB30_SSRXN	K27
SDMMC_CLK/PDM1_CLK0_M0/TEST_CLKOUT_M0/MCU_JTAG_TMS_M0/UART5_TX_M0/GPIO4_D5	AE3	PCIE20_2_RXP/SATA30_2_RXP/USB30_SSRXP	K28
SDMMC_D3/PDM1_SDI0_M0/JTAG_TMS_M0/I2C8_SDA_M0/UART5_RTSN_M0/PWM10_M1/GPIO4_D3	AE4	DDR_CH0_CKB_B	L1
SDMMC_D2/PDM1_SDI1_M0/JTAG_TCK_M0/I2C8_SCL_M0/UART5_CTSN_M0/GPIO4_D2	AE5	DDR_CH0_CK_B	L2
AVSS_6	AE6	VSS_82	L3
AVSS_7	AE7	DDR_CH0_A3_B	L4
HDMI/eDP_TX1_VDD_IO_1V8	AE8	DDR_CH0_A2_B	L5
HDMI_TX0_VDD_CMN_1V8	AE10	VSS_83	L6
VSS_141	AE11	DDR_CH0_LP4/4X_CS1_B	L7
VSS_142	AE12	VSS_84	L8
VSS_143	AE13	PCIE30_PORT0_AVDD1V8	L21
VSS_144	AE14	PCIE20_SATA30_USB30_2_AVDD_0V85	L22
VSS_145	AE15	AVSS1_7	L23
VSS_146	AE16	PCIE20_1_REFCLKP	L24
VDD_LOGIC_10	AE17	PCIE20_1_REFCLKN	L25
VDD_LOGIC_11	AE18	AVSS1_8	L26
VDD_LOGIC_12	AE19	PCIE20_1_RXP/SATA30_1_RXP	L27
VDD_LOGIC_13	AE20	PCIE20_1_RXN/SATA30_1_RXN	L28
VSS_147	AE21	DDR_CH0_CKB_A	M1
VSS_148	AE22	DDR_CH0_CK_A	M2
RFU7	AE23	VSS_85	M3
GMAC0_RXD2/SDIO_D0_M0/UART6_RX_M0/GPIO2_A6	AE24	VSS_86	M4
GMAC0_TXD3/SDIO_CMD_M0/I2C3_SCL_M3/GPIO2_B2	AE25	DDR_CH0_A1_B	M5
LITCPU_AVS/SPI3_CLK_M2/GPIO0_D3	AE26	DDR_CH0_A0_B	M6
I2S1_SDO2_M1/PDM0_SDI2_M1/PWM3_IR_M0/I2C1_SCL_M2/HDMI_TX0_SDA_M1/SPI3_CS0_M2/SATA_CPDET/GPIO0_D4	AE27	VSS_87	M7
I2S1_LRCK0_M1/PWM0_M0/I2C2_SCL_M0/SPI0_CS1_M0/PCIE30X1_1_PERSTN_M0/GPIO0_B7	AE28	VSS_88	M8
AVSS_8	AF1	PCIE20_SATA30_1_AVDD_1V8	M21
HDMI_TX0_D3P	AF2	PCIE20_SATA30_1_AVDD_0V85	M22
AVSS_9	AF3	AVSS1_9	M23
AVSS_10	AF4	PCIE20_0_REFCLKP	M24
AVSS_11	AF5	PCIE20_0_REFCLKN	M25
AVSS_12	AF6	AVSS1_10	M26
AVSS_13	AF7	PCIE20_1_TXN/SATA30_1_TXN	M27
AVSS_14	AF8	PCIE20_1_TXP/SATA30_1_TXP	M28
AVSS_15	AF9	DDR_CH0_A4_A	N2
HDMI/eDP_TX1_VDD_CMN_1V8	AF10	DDR_CH0_A5_A	N3
USB20_AVDD_3V3	AF11	VSS_89	N5
AVSS_16	AF12	VSS_90	N7
AVSS_17	AF13	VSS_91	N8
AVSS_18	AF14	PCIE20_SATA30_0_AVDD_1V8	N21
TYPEC0_DP0_VDDH_1V8	AF15	PCIE20_SATA30_0_AVDD_0V85	N22
SARADC_AVDD_1V8	AF17	TVSS	N23
VSS_149	AF18	AVSS1_11	N24
CIF_VSYNC/BT1120_D9/I2S1_SDO2_M0/PCIE20X1_2_BUTTON_RSTN/I2C7_SDA_M3/UART8_CTSN_M0/PWM15_IR_M1/GPIO4_B3	AF20	AVSS1_12	N25
VCCIO6	AF21	AVSS1_13	N26
GMAC0_PPSCLK/TEST_CLKOUT_M1/HDMI_TX1_CEC_M0/UART9_RX_M0/SPI1_CS1_M0/GPIO2_C4	AF22	PCIE20_0_TXP/SATA30_0_TXP	N27

SPDIF1_TX_M1/I2S1_SDO0_M0/PCIE30X1_0_BUTTON_RSTN/SATA2_ACT_LED_M0/I2C6_SCL_M3/UART8_RX_M0/SPI0_CS1_M1/GPIO4_B1	AF23	PCIE20_0_TXN/SATA30_0_TXN	N28
GMAC0_RXCLK/SDIO_D2_M0/I2C8_SCL_M1/UART6_RTSN_M0/GPIO2_B0	AF24	VSS_92	P2
CIF_D15/I2C7_SDA_M2/UART9_CTSN_M2/PWM10_M2/SPI0_CLK_M3/GPIO3_D3	AF25	DDR_CH0_DQ3_A	P3
I2S1_SDI2_M1/PDM0_SDI0_M1/I2C6_SDA_M0/UART1_RTSN_M2/PWM6_M0/SPI0_MISO_M0/PCIE30X4_WAKEN_M0/GPIO0_C7	AF26	DDR_CH0_A4_B	P4
I2S1_LRCK1_M1/PDM0_CLK1_M1/PWM2_M0/UART0_RX_M0/I2C4_SDA_M2/DP0_HPDIN_M1/PCIE30X1_0_WAKEN_M0/GPIO0_C4	AF27	DDR_CH0_A5_B	P5
HDMI_TX0_D0P	AG1	VSS_93	P6
HDMI_TX0_D0N	AG2	DDR_CH0_LP4/4X_CKE0_B	P7
AVSS_19	AG3	VSS_94	P8
HDMI_TX0_REXT	AG4	OSC_1V8	P21
HDMI_TX1_SBDN/EDP_TX1_AUXN	AG5	VSS_95	P22
USB20_HOST0_REXT	AG6	TSADC_SHUT_ORG/TSADC_SHUT/GPIO0_A1	P23
AVSS_20	AG7	PMIC_SLEEP1/GPIO0_A2	P24
USB20_HOST0_DP	AG8	SPI2_MOSI_M2/I2C0_SDA_M0/GPIO0_A6	P25
USB20_AVDD_1V8	AG9	AVSS1_14	P26
USB20_DVDD_0V75	AG10	PCIE20_0_RXN/SATA30_0_RXN	P27
TYPEC0_USB20_VBUSDET	AG11	PCIE20_0_RXP/SATA30_0_RXP	P28
TYPEC0_USB20_OTG_ID	AG12	DDR_CH0_DQ2_A	R1
TYPEC0_DP0_VDD_0V85	AG14	DDR_CH0_DQ1_A	R2
TYPEC0_DP0_VDDA_0V85	AG15	DDR_CH0_DQ5_A	R3
AVSS_21	AG17	VSS_96	R4
BT1120_D11/PCIE30X4_WAKEN_M1/SATA1_ACT_LED_M0/UART9_RX_M1/PWM12_M1/SPI3_MISO_M1/GPIO4_B5	AG18	DDR_CH0_LP4/4X_CKE1_A	R5
CIF_CLKIN/BT1120_CLKOUT/I2S1_SDI3_M0/I2C6_SDA_M3/UART8_TX_M0/SPI2_CS1_M1/GPIO4_B0	AG20	DDR_CH0_LP4/4X_CKE1_B	R6
BT1120_D12/PCIE30X4_PERSTN_M1/SATA0_ACT_LED_M0/I2C5_SCL_M1/PWM13_M1/SPI3_MOSI_M1/GPIO4_B6	AG21	VSS_97	R7
RFU6	AG22	VSS_98	R8
CIF_HREF/BT1120_D8/I2S1_SDO1_M0/PCIE30X1_1_BUTTON_RSTN/I2C7_SCL_M3/UART8_RTSN_M0/PWM14_M1/SPI0_CS0_M1/ GPIO4_B2	AG23	PMU_0V75	R21
GMAC0_TXCLK/SDIO_CLK_M0/I2C3_SDA_M3/GPIO2_B3	AG24	PMUIO2	R22
RFU5	AG25	PMIC_INT_L/GPIO0_A7	R23
CIF_D12/PCIE20X1_2_WAKEN_M0/HDMI_TX0_SDA_M2/I2C5_SDA_M0/UART4_RX_M1/PWM8_M2/SPI3_CLK_M3/GPIO3_D0	AG26	SPI2_MISO_M2/I2C0_SCL_M0/GPIO0_B3	R24
I2S1_SCLK0_M1/JTAG_TMS_M2/I2C1_SDA_M0/UART2_RX_M0/PCIE30X1_1_WAKEN_M0/GPIO0_B6	AG27	SDMMC_DET/GPIO0_A4	R25
I2S1_SCLK1_M1/PDM0_CLK0_M1/PWM1_M0/I2C2_SDA_M0/SPI0_MOSI_M0/PCIE30X1_0_CLKREQN_M0/GPIO0_C0	AG28	VSS_99	R26
HDMI_TX0_D1P	AH1	XOUT_24M	R27
HDMI_TX0_D1N	AH2	XIN_24M	R28
AVSS_22	AH3	DDR_CH0_DQ4_A	T2
HDMI/eDP_TX1_REXT	AH4	VSS_100	T3
HDMI_TX1_SBDP/EDP_TX1_AUXP	AH5	VSS_101	T5
USB20_HOST1_REXT	AH6	VSS_102	T7
USB20_HOST0_DM	AH8	VSS_103	T8
USB20_OTG1_REXT	AH9	PMUIO1_1V8	T21
TYPEC0_USB20_OTG0_REXT	AH11	REFCLK_OUT/GPIO0_A0	T27
TYPEC0_DP0_REXT	AH12	DDR_CH0_DQS0N_A	U1
SARADC_IN1	AH14	DDR_CH0_DQS0P_A	U2
SARADC_IN3	AH15	VSS_104	U3
SARADC_IN2	AH17	DDR_CH0_LP4/4X_CKE0_A	U4
CIF_CLKOUT/BT1120_D10/I2S1_SDO3_M0/PCIE30X4_CLKREQN_M1/DP0_HPDIN_M0/SPDIF0_TX_M1/UART9_TX_M1/PWM11_IR_M1/GPIO4_B4	AH18	DDR_CH0_A3_A	U5
BT1120_D14/PCIE20X1_2_WAKEN_M1/HDMI_TX0_SDA_M0/I2C8_SCL_M3/SPI3_CS0_M1/GPIO4_C0	AH20	VSS_105	U6
BT1120_D15/SPDIF1_TX_M2/PCIE20X1_2_PERSTN_M1/HDMI_TX0_CEC_M0/I2C8_SDA_M3/PWM6_M1/SPI3_CS1_M1/GPIO4_C1	AH21	DDR_CH0_A1_A	U7
VSS_150	AH22	VSS_106	U8
GMAC0_TXEN/I2S2_LRCK_M0/I2C2_SDA_M1/UART1_RTSN_M0/SPI1_CLK_M0/GPIO2_C0	AH23	PMUIO2_1V8	U21
GMAC0_RXD0/I2C2_SCL_M1/UART1_CTSN_M0/SPI1_MISO_M0/GPIO2_C1	AH24	VSS_107	U22
CIF_D14/I2C7_SCL_M2/UART9_RTSN_M2/SPI0_MOSI_M3/GPIO3_D2	AH25	I2S1_SDO1_M1/I2C0_SDA_M2/UART1_RX_M2/SPI3_MOSI_M2/HDMI_TX1_CEC_M1/GPIO0_D2	U23

GMAC1_TXD1/I2S2_MCLK_M1/UART2_CTSN/GPIO3_B4	AH26	I2S1_SDI3_M1/PDM0_SDI1_M1/I2C6_SCL_M0/UART1_CTSN_M2/PWM7_IR_M0/SPI3_MISO_M2/PCIE30X4_PERSTN_M0/GPIO0_D0	U24
PMIC_SLEEP_3/GPIO0_C1	AH27	PMIC_SLEEP_5/GPIO0_C3	U25
HDMI_TX0_D2P	AJ1	SPI2_CS0_M2/I2C1_SDA_M1/PWM5_M0/UART0_TX_M1/GPIO0_B1	U26
HDMI_TX0_D2N	AJ2	SPI2_CS1_M2/I2C1_SCL_M1/UART0_RX_M1/GPIO0_B0	U27
AVSS_23	AJ3	SPI2_CLK_M2/SDMMC_PWREN/PMU_DEBUG/GPIO0_A5	U28
AVSS_24	AJ4	DDR_CH0_DQ0_A	V2
AVSS_25	AJ5	DDR_CH0_DM0_A	V3
AVSS_26	AJ6	VSS_108	V4
AVSS_27	AJ7	DDR_CH0_LP4/4X_CS1_A	V5
AVSS_28	AJ8	DDR_CH0_LP4/4X_CS0_A	V6
AVSS_29	AJ9	DDR_CH0_RESET_A	V7
AVSS_30	AJ10	VSS_109	V8
AVSS_31	AJ11	VSS_110	V21
AVSS_32	AJ12	EMMCIO_1V8	V22
AVSS_33	AJ14	GMAC1_TXD2/SDIO_D0_M1/I2S3_MCLK/FSPI_D0_M2/I2C6_SDA_M4/PWM10_M0/SPI4_MISO_M1/GPIO3_A0	V23
SARADC_IN0_BOOT	AJ15	I2S1_SDI1_M1/NPU_AVS/UART0_RTSN/PWM5_M1/SPI0_CLK_M0/PCIE30X4_CLKREQN_M0/SATA_CP_POD/GPIO0_C6	V24
VSS_151	AJ17	PMIC_SLEEP6/PDM0_SDI3_M1/GPIO0_D6	V25
BT1120_D13/PCIE20X1_2_CLKREQN_M1/HDMI_TX0_SCL_M0/I2C5_SDA_M1/SPI3_CLK_M1/GPIO4_B7	AJ18	I2S1_SDI0_M1/GPU_AVS/UART0_TX_M0/I2C4_SCL_M2/DP1_HPDIN_M1/PWM4_M0/PCIE30X1_0_PERSTN_M0/GPIO0_C5	V26
CIF_D6/BT1120_D6/I2S1_SDI1_M0/I2C5_SCL_M2/UART3_RX_M2/SPI2_CLK_M1/GPIO4_A6	AJ19	CLK32K_IN/CLK32K_OUT0/GPIO0_B2	V27
CIF_D2/BT1120_D2/I2S1_LRCK_M0/PCIE30X1_1_PERSTN_M1/SPI0_CLK_M1/GPIO4_A2	AJ20	DDR_CH0_DQ7_A	W1
CIF_D1/BT1120_D1/I2S1_SCLK_M0/PCIE30X1_1_WAKEN_M1/UART9_CTSN_M1/SPI0_MOSI_M1/GPIO4_A1	AJ21	DDR_CH0_DQ6_A	W2
GMAC0_RXD3/SDIO_D1_M0/UART6_TX_M0/GPIO2_A7	AJ22	VSS_111	W3
GMAC0_RXD1/I2C6_SDA_M2/UART9_TX_M0/SPI1_MOSI_M0/GPIO2_C2	AJ23	VSS_112	W5
CIF_D11/PCIE20X1_2_CLKREQN_M0/HDMI_TX0_SCL_M2/I2C5_SCL_M0/SPI3_MOSI_M3/GPIO3_C7	AJ24	DDR_CH0_ZQ_A	W8
GMAC1_PPSCLK/UART7_RX_M1/SPI1_CLK_M1/GPIO3_C1	AJ25	VSS_113	W21
GMAC1_PTP_REF_CLK/HDMI_TX1_HPD_M1/I2C3_SCL_M1/SPI1_MOSI_M1/GPIO3_B7	AJ26	I2S1_SDO3_M1/CPU_BIG1_AVS/I2C1_SDA_M2/HDMI_TX0_SCL_M1/SPI3_CS1_M2/SATA_MP_SWITCH/GPIO0_D5	W26
GMAC1_RXD2/SDIO_D2_M1/I2S3_LRCK/AUDDSM_LP/FSPI_D2_M2/UART8_TX_M1/SPI4_CLK_M1/GPIO3_A2	AJ27	PMIC_SLEEP2/GPIO0_A3	W27
GMAC1_TXD3/SDIO_D1_M1/I2S3_SCLK/AUDDSM_LN/FSPI_D1_M2/I2C6_SCL_M4/PWM11_IR_M0/SPI4_MOSI_M1/GPIO3_A1	AJ28	NPOR	W28
HDMI_TX1_D3N/EDP_TX1_D3N	AK1	DDR_CH0_DQ14_A	Y1
HDMI_TX1_D3P/EDP_TX1_D3P	AK2	DDR_CH0_DQ15_A	Y2
HDMI_TX1_D0P/EDP_TX1_D0P	AK3	VSS_114	Y3
HDMI_TX1_D1P/EDP_TX1_D1P	AK4	DDR_CH0_A2_A	Y4
HDMI_TX1_D2P/EDP_TX1_D2P	AK5	DDR_CH0_A0_A	Y5
USB20_HOST1_DM	AK6	VSS_115	Y6
USB20_OTG1_DM	AK7	VSS_116	Y7
TYPEC0_USB20_OTG_DM	AK8	VCCIO2_1V8	Y8
TYPEC0_SSRX1N/DP0_TX0N	AK9	VCCIO5	Y21
TYPEC0_SSTX1P/DP0_TX1P	AK10	CIF_D8/FSPI_CS0N_M2/PCIE30X4_CLKREQN_M2/HDMI_TX1_CEC_M2/ UART5_TX_M1/SPI3_CS0_M3/GPIO3_C4	Y22
TYPEC0_SBU1/DP0_AUXP	AK11	GMAC1_MCLKINOUT/I2S2_LRCK_M1/UART3_RX_M1/PWM13_M0/GPIO3_B6	Y23
TYPEC0_SSRX2N/DP0_TX2N	AK12	GMAC1_TXD0/I2S2_SDO_M1/UART2_RTSN/GPIO3_B3	Y24
TYPEC0_SSTX2P/DP0_TX3P	AK13	ETH1_REFCLKO_25M/I2C4_SCL_M0/GPIO3_A6	Y25
CIF_D5/BT1120_D5/I2S1_SDI0_M0/PCIE30X1_0_PERSTN_M1/I2C3_SDA_M2/UART3_TX_M2/SPI2_MOSI_M1/GPIO4_A5	AK14	PMIC_SLEEP_4/GPIO0_C2	Y26
CIF_D4/BT1120_D4/PCIE30X1_0_WAKEN_M1/I2C3_SCL_M2/UART0_RX_M2/SPI2_MISO_M1/GPIO4_A4	AK15	I2S1_SDO0_M1/CPU_BIG0_AVS/I2C0_SCL_M2/UART0_CTSN/UART1_TX_M2/SPI0_CS0_M0/HDMI_TX0_CEC_M1/GPIO0_D1	Y27
CIF_D3/BT1120_D3/PCIE30X1_0_CLKREQN_M1/UART0_TX_M2/GPIO4_A3	AK16	DDR_CH0_VDDQ_0	1E1
CIF_D7/BT1120_D7/I2S1_SDI2_M0/I2C5_SDA_M2/SPI2_CS0_M1/GPIO4_A7	AK17	DDR_CH01_PLL_AVDD1V8	1E2
GMAC0_RXDV_CRS/PWM2_M2/GPIO4_C2	AK18	VSS_175	1E3
GMAC0_MCLKINOUT/I2S2_SDO_M0/I2C7_SCL_M1/PWM4_M1/GPIO4_C3	AK19	DDR_CH1_VDD_5	1E4
GMAC0_TXD1/I2S2_SCLK_M0/I2C5_SDA_M4/UART1_TX_M0/GPIO2_B7	AK20	VDD_LOGIC_0	1E5
PCIE30X4_BUTTON_RSTN/DP1_HPDIN_M0/MCU_JTAG_TMS_M1/UART9_TX_M2/PWM11_IR_M3/SPI0_CS1_M3/GPIO3_D5	AK21	VSS_176	1E6
CIF_D13/PCIE20X1_2_PERSTN_M0/UART4_TX_M1/PWM9_M2/SPI0_MISO_M3/GPIO3_D1	AK22	VDD_CPU_BIG_3	1E7
CIF_D9/FSPI_CS1N_M2/PCIE30X4_WAKEN_M2/HDMI_TX1_SDA_M1/ UART5_RX_M1/SPI3_CS1_M3/GPIO3_C5	AK23	VDD_CPU_BIG_4	1E8

CIF_D10/PCIE30X4_PERSTN_M2/HDMI_TX1_SCL_M1/SPI3_MISO_M3/GPIO3_C6	AK24	VDD_CPU_BIG_5	1E9
GMAC1_PPSTRIG/I2C3_SDA_M1/UART7_TX_M1/SPI1_MISO_M1/GPIO3_C0	AK25	VDD_CPU_BIG_6	1E10
GMAC1_RXD1/PWM9_M0/GPIO3_B0	AK26	PLL_AVDD1V8	1E11
GMAC1_RXCLK/SDIO_CLK_M1/FSPI_CLK_M2/I2C4_SDA_M0/UART8_CTSN_M1/GPIO3_A5	AK27	VSS_153	1A1
GMAC1_TXCLK/SDIO_CMD_M1/I2S3_SDI/AUDDSM_RP/UART8_RTSN_M1/SPI4_CS1_M1/GPIO3_A4	AK28	VSS_154	1A2
AVSS_34	AL1	VSS_155	1A3
HDMI_TX1_D0N/EDP_TX1_D0N	AL2	VSS_156	1A4
HDMI_TX1_D1N/EDP_TX1_D1N	AL3	VSS_157	1A5
HDMI_TX1_D2N/EDP_TX1_D2N	AL4	VSS_158	1A6
AVSS_35	AL5	VSS_159	1A7
USB20_HOST1_DP	AL6	VSS_160	1A8
USB20_OTG1_DP	AL7	VSS_161	1A9
TYPEC0_USB20_OTG_DP	AL8	VSS_162	1A10
TYPEC0_SSRX1P/DP0_TX0P	AL9	VSS_163	1A11
TYPEC0_SSTX1N/DP0_TX1N	AL10	VSS_164	1B1
TYPEC0_SBU2/DP0_AUXN	AL11	DDR_CH1_VDDQ_0	1B2
TYPEC0_SSRX2P/DP0_TX2P	AL12	DDR_CH1_VDDQ_1	1B3
TYPEC0_SSTX2N/DP0_TX3N	AL13	DDR_CH1_VDDQ_2	1B4
CIF_D0/BT1120_D0/I2S1_MCLK_M0/PCIE30X1_1_CLKREQN_M1/UART9_RTSN_M1/SPI0_MISO_M1/GPIO4_A0	AL14	DDR_CH1_VDDQ_3	1B5
GMAC0_TXD0/I2S2_MCLK_M0/I2C5_SCL_M4/UART1_RX_M0/GPIO2_B6	AL15	DDR_CH1_VDDQ_4	1B6
GMAC0_MDIO/UART9_CTSN_M0/PWM6_M2/GPIO4_C5	AL16	DDR_CH01_PLL_AVSS_2	1B7
GMAC0_MDC/I2C7_SDA_M1/UART9_RTSN_M0/PWM5_M2/GPIO4_C4	AL18	VSS_165	1B8
HDMI_TX0_HPD_M1/MCU_JTAG_TCK_M1/UART9_RX_M2/SPI0_CS0_M3/GPIO3_D4	AL20	VCCIO4	1B9
GMAC1_MDIO/I2C8_SDA_M4/UART7_CTSN_M1/PWM15_IR_M0/SPI1_CS1_M1/GPIO3_C3	AL21	VCCIO4_1V8	1B10
GMAC1_TXEN/I2S2_SCLK_M1/UART3_TX_M1/PWM12_M0/GPIO3_B5	AL23	VCCIO1_1V8	1B11
GMAC1_RXDV_CRS/UART2_TX_M2/PWM2_M1/GPIO3_B1	AL25	VSS_166	1C1
GMAC1_RXD0/PWM8_M0/GPIO3_A7	AL26	DDR_CH01_PLL_DVDD	1C2
GMAC1_TXER/I2S2_SDI_M1/UART2_RX_M2/PWM3_IR_M1/GPIO3_B2	AL27	DDR_CH1_VDD_0	1C3
VSS_152	AL28	DDR_CH1_VDD_1	1C4
DDR_CH0_DM0_B	B1	DDR_CH1_VDD_2	1C5
DDR_CH1_DQ11_C	B2	DDR_CH1_VDD_3	1C6
DDR_CH1_DQ9_C	B3	DDR_CH1_VDDQ_CK	1C7
DDR_CH1_DQ15_C	B4	VSS_167	1C8
DDR_CH1_DQ13_C	B5	VSS_168	1C9
DDR_CH1_DQ7_C	B6	VSS_169	1C10
DDR_CH1_DQ6_C	B7	VSS_170	1C11
DDR_CH1_DQ4_C	B8	DDR_CH0_VDDQ_CK	1D1
DDR_CH1_DQ3_C	B9	DDR_CH01_PLL_AVSS_1	1D2
DDR_CH1_CK_C	B10	VSS_171	1D3
VSS_4	B11	DDR_CH1_VDD_4	1D4
DDR_CH1_CK_D	B12	VSS_172	1D5
DDR_CH1_A3_D	B13	VSS_173	1D6
DDR_CH1_A4_D	B14	VSS_174	1D7
DDR_CH1_DQ3_D	B15	VDD_CPU_BIG_0	1D8
DDR_CH1_DQ1_D	B16	VDD_CPU_BIG_1	1D9
DDR_CH1_DQ7_D	B17	VDD_CPU_BIG_2	1D10
DDR_CH1_DQ13_D	B18	PCIE20_SATA30_USB30_2_AVDD_1V8	1D11
DDR_CH1_DQ15_D	B19	DDR_CH0_VDDQ_1	1F1
DDR_CH1_DQ9_D	B20	DDR_CH0_VDD_0	1F2
DDR_CH1_DQ11_D	B21	DDR_CH0_VDD_1	1F3
VSS_5	B22	VSS_177	1F4
HDMI_TX1_SCL_M2/SPI2_MISO_M0/GPIO1_A4	B23	VDD_LOGIC_1	1F5
PDM1_CLK0_M1/PCIE30X1_0_PERSTN_M2/UART7_RX_M2/SPI0_CS0_M2/GPIO1_B4	B24	VSS_178	1F6
SPDIF1_TX_M0/SATA2_ACT_LED_M1/I2C5_SDA_M3/UART1_RX_M1/PWM13_M2/GPIO1_B7	B25	VDD_CPU_BIG_7	1F7
HDMI_TX1_HPD_M0/SPI2_CLK_M0/GPIO1_A6	B26	VDD_CPU_BIG_8	1F8
PDM1_SDI3_M1/PCIE30X4_PERSTN_M3/UART4_RX_M2/SPI0_MOSI_M2/GPIO1_B2	B27	VDD_CPU_BIG_9	1F9
PDM1_SDI2_M1/PCIE30X4_WAKEN_M3/SPI0_MISO_M2/GPIO1_B1	B28	VDD_CPU_BIG_10	1F10

DDR_CH0_DQ5_B	C1	PLL_AVSS	1F11
DDR_CH0_DQ6_B	C2	DDR_CH0_VDDQ_2	1G1
VSS_6	C3	DDR_CH0_VDD_2	1G2
VSS_7	C4	DDR_CH0_VDD_3	1G3
VSS_8	C5	VSS_179	1G4
VSS_9	C6	VDD_LOGIC_2	1G5
VSS_10	C7	VSS_180	1G6
VSS_11	C8	VSS_181	1G7
DDR_CH1_DQ1_C	C9	VSS_182	1G8
DDR_CH1_CKB_C	C10	VSS_183	1G9
VSS_12	C11	VSS_184	1G10
DDR_CH1_CKB_D	C12	PLL_DVDD0V75	1G11
DDR_CH1_A5_D	C13	DDR_CH0_VDDQ_3	1H1
VSS_13	C14	DDR_CH0_VDD_4	1H2
VSS_14	C15	VSS_185	1H3
VSS_15	C17	VSS_186	1H4
VSS_16	C18	VDD_LOGIC_3	1H5
VSS_17	C20	VSS_187	1H6
DDR_CH1_DM1_D	C21	VSS_188	1H7
PCIE30X1_0_CLKREQN_M2/UART7_TX_M2/SPI0_CS1_M2/GPIO1_B5	C22	VDD_CPU_LIT_0	1H8
PDM1_SDI1_M1/PCIE30X4_CLKREQN_M3/SPI2_CS1_M0/GPIO1_B0	C23	VDD_CPU_LIT_1	1H9
PCIE30X1_1_CLKREQN_M2/DP0_HPDIN_M2/I2C2_SDA_M4/UART6_RX_M1/SPI4_MISO_M2/GPIO1_A0	C24	VSS_189	1H10
HDMI_TX0_HPD_M0/SPI2_MOSI_M0/GPIO1_A5	C25	VSS_190	1H11
HDMI_TX1_SDA_M2/I2C4_SCL_M3/UART6_CTSN_M1/PWM1_M2/SPI4_CS0_M2/GPIO1_A3	C26	DDR_CH0_VDDQ_4	1J1
I2S0_SDO0/I2C4_SCL_M4/UART4_CTSN/GPIO1_C7	C27	DDR_CH0_VDD_5	1J2
PDM0_CLK0_M0/I2C4_SDA_M4/PWM15_IR_M2/GPIO1_C6	C28	VSS_191	1J3
DDR_CH0_DQ11_B	D1	VDD_LOGIC_4	1J4
DDR_CH0_DQ4_B	D2	VDD_LOGIC_5	1J5
VSS_18	D3	VSS_192	1J6
DDR_CH1_DM1_C	D5	VDD_CPU_LIT_2	1J7
DDR_CH1_DQS1N_C	D6	VDD_CPU_LIT_3	1J8
DDR_CH1_DQS0N_C	D8	VDD_CPU_LIT_4	1J9
VSS_19	D9	VDD_CPU_LIT_5	1J10
DDR_CH1_LP4/4X_CS1_C	D11	VSS_193	1J11
VSS_20	D12	VSS_194	1K1
DDR_CH1_LP4/4X_CKE0_C	D14	VSS_195	1K2
VSS_21	D15	VSS_196	1K3
DDR_CH1_A0_D	D17	VDD_LOGIC_6	1K4
VSS_22	D18	VDD_LOGIC_7	1K5
DDR_CH1_DQS0N_D	D20	VDD_LOGIC_8	1K6
DDR_CH1_DQS1N_D	D21	VSS_197	1K7
RFU0	D22	VSS_198	1K8
PCIE30X1_1_WAKEN_M2/DP1_HPDIN_M2/SATA1_ACT_LED_M1/I2C2_SCL_M4/UART6_TX_M1/SPI4_MOSI_M2/GPIO1_A1	D23	VSS_199	1K9
I2S0_LRCK/UART4_RTSN/GPIO1_C5	D24	VSS_200	1K10
I2C3_SDA_M0/UART3_RX_M0/SPI4_MISO_M0/GPIO1_C0	D25	VSS_201	1K11
I2S0_SCLK/I2C6_SCL_M1/UART3_CTSN/PWM7_IR_M2/SPI4_CS0_M0/GPIO1_C3	D26	VCCIO2	1L1
VSS_23	D27	VSS_202	1L2
DDR_CH0_DQ9_B	E1	VSS_203	1L3
DDR_CH0_DQ10_B	E2	VSS_204	1L4
VSS_24	E3	VSS_205	1L5
DDR_CH0_DM1_B	E4	VDD_LOGIC_9	1L6
DDR_CH1_DQS1P_C	E6	VSS_206	1L7
VSS_25	E7	VSS_207	1L8
DDR_CH1_DQS0P_C	E8	VDD_NPU_0	1L9
DDR_CH1_A3_C	E9	VDD_NPU_1	1L10
VSS_26	E10	VSS_208	1L11
DDR_CH1_LP4/4X_CS0_C	E11	OTP_VDDOTP_0V75	1M1
DDR_CH1_A1_C	E12	VSS_209	1M2
VSS_27	E13	VDD_GPU_0	1M3
DDR_CH1_LP4/4X_CKE1_C	E14	VDD_GPU_1	1M4

DDR_CH1_LP4/4X_CKE0_D	E15	VDD_GPU_2	1M5
VSS_28	E16	VSS_210	1M6
DDR_CH1_LP4/4X_CS1_D	E17	VSS_211	1M7
DDR_CH1_DQ5_D	E18	VSS_212	1M8
VSS_29	E19	VDD_NPU_2	1M9
DDR_CH1_DQS0P_D	E20	VDD_NPU_3	1M10
DDR_CH1_DQS1P_D	E21	VSS_213	1M11
RFU2	E22	VSS_214	1N1
I2S0_SDI0/GPIO1_D4	E23	VSS_215	1N2
I2C3_SCL_M0/UART3_TX_M0/SPI4_MOSI_M0/GPIO1_C1	E24	VSS_216	1N3
I2S0_MCLK/I2C6_SDA_M1/UART3_RTSN/PWM3_IR_M2/SPI4_CLK_M0/GPIO1_C2	E25	VDD_GPU_3	1N4
VSS_30	E26	VDD_GPU_4	1N5
PCIE30_PORT0_TX1N	E27	VDD_GPU_5	1N6
PCIE30_PORT0_TX1P	E28	VSS_217	1N7
DDR_CH0_DQ15_B	F1	VSS_218	1N8
DDR_CH0_DQ8_B	F2	VDD_NPU_4	1N9
VSS_31	F3	VDD_NPU_5	1N10
VSS_32	F4	VSS_219	1N11
DDR_CH0_DQS1P_B	F5	HDMI_TX0_AVDD_0V75	1P1
VSS_33	F7	AVSS_1	1P2
VSS_34	F8	VSS_220	1P3
DDR_CH1_A4_C	F9	VDD_GPU_6	1P4
VSS_35	F11	VDD_GPU_7	1P5
DDR_CH1_A0_C	F12	VDD_GPU_8	1P6
VSS_36	F14	VSS_221	1P7
DDR_CH1_LP4/4X_CKE1_D	F15	VSS_222	1P8
VSS_37	F17	VSS_223	1P9
DDR_CH1_DQ4_D	F18	VSS_224	1P10
VSS_38	F20	VSS_225	1P11

Chapter 3 Electrical Specification

3.1 Absolute Ratings

The below table provides the absolute ratings.

Absolute maximum or minimum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

Table 3-1 Absolute ratings

Parameters	Related Power Group	Min	Max	Unit
Supply voltage for CPU	VDD_CPU_BIG VDD_CPU_LIT	-0.3	1.1	V
Supply voltage for CPU memory	VDD_CPU_BIG VDD_CPU_LIT	-0.3	1.1	V
Supply voltage for GPU	VDD_GPU	-0.3	1.1	V
Supply voltage for GPU memory	VDD_GPU	-0.3	1.1	V
Supply voltage for NPU	VDD_NPU	-0.3	1.1	V
Supply voltage for NPU memory	VDD_NPU	-0.3	1.1	V
Supply voltage for core logic, VCODEC and VCODEC Memory	VDD_LOGIC	-0.3	0.95	V
0.75V supply voltage	PMU_0V75 PLL_DVDD0V75 USB20_DVDD_0V75 HDMI_TX0_VDD_0V75 HDMI_TX0_AVDD_0V75 HDMI/eDP_TX1_VDD_0V75 HDMI/eDP_TX1_AVDD_0V75 PCIE30_PORT0_AVDD0V75 OTP_VDDOTP_0V75	-0.3	0.95	V
0.85V supply voltage	DDR_CH0_VDD DDR_CH1_VDD DDR_CH01_PLL_DVDD TYPEC0_DP0_VDD_0V85 TYPEC0_DP0_VDDA_0V85 PCIE20_SATA30_0_AVDD_0V85 PCIE20_SATA30_1_AVDD_0V85 PCIE20_SATA30_USB30_2_AVDD_0V85	-0.3	1.00	V
1.8V supply voltage	DDR_CH01_PLL_AVDD1V8 PLL_AVDD1V8 USB20_AVDD_1V8 TYPEC0_DP0_VDDH_1V8 HDMI_TX0_VDD_CMN_1V8 HDMI_TX0_VDD_IO_1V8 HDMI/eDP_TX1_VDD_CMN_1V8 HDMI/eDP_TX1_VDD_IO_1V8 PCIE20_SATA30_0_AVDD_1V8 PCIE20_SATA30_1_AVDD_1V8 PCIE20_SATA30_USB30_2_AVDD_1V8 PCIE30_PORT0_AVDD1V8 SARADC_AVDD_1V8 OSC_1V8	-0.5	1.98	V
3.3V supply voltage	USB20_AVDD_3V3	-0.5	3.63	V
1.8V only GPIO supply voltage	PMUIO1_1V8 EMMCIO_1V8 VCCIO1_1V8 VCCIO3_1V8	-0.5	1.98	V
1.8V/3.3V GPIO supply voltage	PMUIO2 VCCIO2 VCCIO4 VCCIO5 VCCIO6	-0.5	3.63	V
Supply voltage for DDR IO (LPDDR4/4X 0.6V)	DDR_CH0_VDDQ DDR_CH0_VDDQ_CK DDR_CH1_VDDQ DDR_CH1_VDDQ_CK	-0.3	0.7	V
Supply voltage for DDR IO (LPDDR4/4X 1.1V)	DDR_CH01_VDDQ_CKE	-0.3	1.25	V
Storage Temperature	Tstg	-40	125	℃
Max Conjunction Temperature	Tj	NA	125	℃

3.2 Recommended Operating Conditions

The following table describes the recommended operating conditions.

Table 3-2 Recommended operating conditions

Parameters	Symbol	Min	Typ	Max	Unit
Voltage for CPU BigCore 0/1 and Memory	VDD_CPU_BIG	0.75	0.75	0.95	V
Voltage for CPU LitCore, DSU and their Memory	VDD_CPU_LIT	0.75	0.75	0.95	V
Voltage for GPU and Memory	VDD_GPU	0.75	0.75	0.85	V
Voltage for NPU and Memory	VDD_NPU	0.75	0.75	0.85	V
Voltage for Logic, VCODEC and VCODEC Memory	VDD_LOGIC	0.675	0.75	0.825	V
Voltage for PMU	PMU_0V75	0.675	0.75	0.825	V
Digital GPIO Power (1.8V only)	PMUIO1_1V8, VCCIO1_1V8, VCCIO3_1V8	1.65	1.8	1.95	V
Digital GPIO Power (3.3V/1.8V)	PMUIO2, VCCIO2, VCCIO4, VCCIO5, VCCIO6	2.7 1.65	3.3 1.8	3.6 1.95	V
eMMC IO Power (1.8V)	EMMCIO_1V8	1.65	1.8	1.95	V
DDR CH0 Logic power(0.85V)	DDR_CH0_VDD, DDR_CH1_VDD,	0.675	0.85	0.935	V
DDR CH01_PLL power(0.85V)	DDR_CH01_PLL_DVDD	0.675	0.85	0.8925	V
DDR CH01_PLL power(1.8V)	DDR_CH01_PLL_AVDD1V8	1.62	1.8	1.98	V
LPDDR4 IO VDDQ power	DDR_CH0_VDDQ, DDR_CH0_VDDQ_CK, DDR_CH1_VDDQ, DDR_CH1_VDDQ_CK	0.57	0.6	0.63	V
LPDDR4 Retention IO VDDQ Power	DDR_CH01_VDDQ_CKE	1.045	1.1	1.155	V
PLL Analog Power(0.75V)	PLL_DVDD0V75	0.675	0.75	0.8925	V
PLL Analog Power(1.8V)	PLL_AVDD1V8	1.62	1.8	1.98	V
USB 2.0 Analog Power (0.75V)	USB20_DVDD_0V75	0.6975	0.75	0.825	V
USB 2.0 Analog Power (1.8V)	USB20_AVDD_1V8	1.674	1.8	1.98	V
USB 2.0 Analog Power (3.3V)	USB20_AVDD_3V3	3.069	3.3	3.63	V
USB & DP Analog Power (0.85V)	TYPEC0_DP0_VDD_0V85, TYPEC0_DP0_VDDA_0V85	0.8075	0.85	0.8925	V
USB & DP Analog Power (1.8V)	TYPEC0_DP0_VDDH_1V8	1.71	1.8	1.89	V
Combo PIPE PHY Analog Power(0.85V)	PCIE20_SATA30_0_AVDD_0V85, PCIE20_SATA30_1_AVDD_0V85, PCIE20_SATA30_USB30_2_AVDD_0V85	0.8	0.85	0.935	V
Combo PIPE PHY Analog Power(1.8V)	PCIE20_SATA30_0_AVDD_1V8, PCIE20_SATA30_1_AVDD_1V8, PCIE20_SATA30_USB30_2_AVDD_1V8	1.62	1.8	1.98	V
PCIe30 Analog Power(0.75V)	PCIE30_PORT0_AVDD0V75	0.7125	0.75	0.8925	V
PCIe30 Analog Power(1.8V)	PCIE30_PORT0_AVDD1V8	1.71	1.8	1.89	V
HDMI/eDP TX Digital Power (0.75V)	HDMI_TX0_VDD_0V75, HDMI/eDP_TX1_VDD_0V75	0.675	0.75	0.85	V
HDMI/eDP TX Analog Power (0.75V)	HDMI_TX0_AVDD_0V75, HDMI/eDP_TX1_AVDD_0V75	0.675	0.75	0.85	V
HDMI/eDP TX Analog Power (1.8V)	HDMI_TX0_VDD_CMN_1V8, HDMI/eDP_TX1_VDD_CMN_1V8	1.62	1.8	1.98	V
HDMI/eDP TX Analog Power (1.8V)	HDMI_TX0_VDD_IO_1V8, HDMI/eDP_TX1_VDD_IO_1V8	1.62	1.8	1.98	V
SARADC Analog Power(1.8V)	SARADC_AVDD_1V8	1.62	1.8	1.98	V
OTP Analog Power(0.75V)	OTP_VDDOTP_0V75	0.675	0.75	0.825	V

Parameters	Symbol	Min	Typ	Max	Unit
OSC Analog Power(1.8V)	OSC_1V8	1.65	1.8	1.95	V
OSC input clock frequency		NA	24	NA	MHz
Max CPU frequency		NA	NA	2.2-2.4	GHz
Max GPU frequency		NA	NA	1000	MHz
Max NPU frequency		NA	NA	1000	MHz
Ambient Operating Temperature	T_A	0	NA	80	℃

3.3 DC Characteristics

Table 3-3 DC Characteristics

Parameters		Symbol	Min	Typ	Max	Unit
Digital 3.3V/1.8V GPIO @3.3V	Input Low Voltage	V_{IL}	VSS	NA	0.3*VDDO	V
	Input High Voltage	V_{IH}	0.7*VDDO	NA	VDDO	V
	Output Low Voltage	V_{OL}	VSS	NA	0.25*DVDD	V
	Output High Voltage	V_{OH}	0.75*DVDD	NA	DVDD	V
	Pullup Resistor	R_{RPU}	10	NA	100	Kohm
	Pulldown Resistor	R_{RPD}	10	NA	100	Kohm
Digital 3.3V/1.8V GPIO @1.8V	Input Low Voltage	V_{IL}	VSS	NA	0.3*VDDO	V
	Input High Voltage	V_{IH}	0.7*VDDO	NA	VDDO	V
	Output Low Voltage	V_{OL}	VSS	NA	0.25*DVDD	V
	Output High Voltage	V_{OH}	0.75*DVDD	NA	DVDD	V
	Pullup Resistor	R_{RPU}	10	NA	50	Kohm
	Pulldown Resistor	R_{RPD}	10	NA	50	Kohm
Digital 1.8V only GPIO @1.8V	Input Low Voltage	V_{IL}	VSS	NA	0.3*VDDO	V
	Input High Voltage	V_{IH}	0.7*VDDO	NA	VDDO	V
	Output Low Voltage	V_{OL}	VSS	NA	0.25*DVDD	V
	Output High Voltage	V_{OH}	0.75*DVDD	NA	DVDD	V
	Pullup Resistor	R_{RPU}	10	NA	50	Kohm
	Pulldown Resistor	R_{RPD}	10	NA	50	Kohm
eMMC IO @1.8V	Input Low Voltage	V_{IL}	VSS	NA	0.35*DVDD	V
	Input High Voltage	V_{IH}	0.65*DVDD	NA	DVDD	V
	Output Low Voltage	V_{OL}	VSS	NA	0.45	V
	Output High Voltage	V_{OH}	DVDD-0.45	NA	DVDD	V
	Pullup Resistor	R_{RPU}	10	NA	50	Kohm
	Pulldown Resistor	R_{RPD}	10	NA	50	Kohm
DDR IO	Input Low Voltage	V_{IL}	NA	NA	Vref-0.14	V
	Input High Voltage	V_{IH}	Vref+0.14	NA	NA	V
	Output Log Voltage	V_{OL}	NA	NA	0.2	V
	Output High Voltage	V_{OH}	0.25	NA	NA	V
	Input Low Current	I_{IL}	-100/-500	NA	100/500	Room/Hot uA
	Input High Current	I_{IH}	-100/-500	NA	100/500	Room/Hot uA

Note: VDDO and DVDD are both IO power Supply

3.4 Electrical Characteristics for General IO

Table 3-4 Electrical Characteristics for Digital General IO

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
Digital 3.3V/1.8V GPIO @3.3V	Input leakage current	I_{PAD}	DVDD=Max, V_{PAD}=0V or DVDD	-10	NA	10	uA
	Input Hysteresis for Schmitt Trigger Operation	V_H		0.08* VDDO	NA	NA	V

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
	Input pullup resistor current	I_{RPU}	V_{PAD} = 0V	-20	NA	-180	uA
	Input pulldown resistor current	I_{RPD}	V_{PAD} = VDDO	20	NA	180	uA
Digital 3.3V/1.8V GPIO @1.8V	Input leakage current	I_{PAD}	DVDD=Max, V_{PAD}=0V or DVDD	-10	NA	10	uA
	Input Hysteresis for Schmitt Trigger Operation	V_H		0.1* VDDO	NA	NA	V
	Input pullup resistor current	I_{RPU}	V_{PAD} = 0V	-20	NA	-180	uA
	Input pulldown resistor current	I_{RPD}	V_{PAD} = VDDO	20	NA	180	uA
Digital 1.8V only GPIO @1.8V	Input leakage current	I_{PAD}	DVDD=Max, V_{PAD}=0V or DVDD	-10	NA	10	uA
	Input Hysteresis for Schmitt Trigger Operation	V_H		0.1* VDDO	NA	NA	V
	Input pullup resistor current	I_{RPU}	V_{PAD} = 0V	-20	NA	-170	uA
	Input pulldown resistor current	I_{RPD}	V_{PAD} = VDDO	20	NA	170	uA
eMMC IO @1.8V	Input leakage current	I_{PAD}	DVDD=Max, V_{PAD}=0V or DVDD	-10	NA	10	uA
	Input Hysteresis for Schmitt Trigger Operation	V_H		0.1* DVDD	NA	NA	V
	Input pullup resistor current	I_{RPU}	V_{PAD} = 0V	-20	NA	-170	uA
	Input pulldown resistor current	I_{RPD}	V_{PAD} = VDDO	20	NA	170	uA

Note: VDDO and DVDD are both IO power Supply

3.5 Electrical Characteristics for PLL

Table 3-5 Electrical Characteristics for INT PLL

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Input clock frequency	F_{FIN}		4.5	-	300	MHz
Reference frequency(F_{FIN}/p)	F_{FREE}		4.5	7	12	MHz
Frequency of PLL's output	F_{FOUT}		35.2	-	4500	MHz
Frequency of VCO's output	F_{FVCO}		2250	-	4500	MHz
Lock time	T_{LT}	Measured at all F_{FIN} and F_{FOUT} range. RESETB=High	-	-	150	Cycles

Table 3-6 Electrical Characteristics for FRAC PLL

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Input clock frequency	F_{FIN}		6	-	300	MHz
Reference frequency(F_{FIN}/p)	F_{FREE}		6	20	30	MHz
Frequency of PLL's output	F_{FOUT}		35.2	-	4500	MHz
Frequency of VCO's output	F_{FVCO}		2250	-	4500	MHz
Lock time	T_{LT}	Measured at all F_{FIN} and F_{FOUT} range. RESETB=High	-	-	500	Cycles

Table 3-7 Electrical Characteristics for DDR PLL

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Input clock frequency	F_{FIN}		6	-	300	MHz
Reference frequency(F_{FIN}/p)	F_{FREE}		6	20	30	MHz
Frequency of PLL's output	F_{FOUT}		51.6	-	6600	MHz
Frequency of VCO's output	F_{FVCO}		3300	-	6600	MHz
Lock time	T_{LT}	Measured at all F_{FIN} and F_{FOUT} range. RESETB=High	-	-	500	Cycles

Notes:

① p is the input divider value

3.6 Electrical Characteristics for PCIe2/SATA Interface

Table 3-8 Electrical Characteristics for PCIe2/SATA Interface

Parameters	Symbol	Min	Typ	Max	Unit
Transmitter					

Parameters	Symbol	Min	Typ	Max	Unit
Differential Peak-Peak TX Output Voltage Swing	$V_{TX\_DIFF\_PP}$	800	1000	1200	mV
Differential Peak-Peak Low Power TX Output Voltage Swing	$V_{TX\_DIFF\_PP\_LOW}$	400	NA	1200	mV
The output impedance	$R_{TX\_DIFF\_DC}$	80	100	120	ohm
Single Ended Output Resistance Matching	$R_{TX\_DC\_OFFSET}$	NA	NA	5	%
Transmitter output common mode voltage	$V_{TX\_DC\_CM}$	400	NA	800	mV
Maximum mismatch between TXP and TXM for both time and amp	$V_{TX\_CM\_AC\_PP\_ACTIVE}$	NA	NA	50	mV
The amount of voltage change allowed during Receiver Detection	$V_{TX\_RCV\_DETECT}$	NA	NA	600	mV
TX de-emphasis	$V_{TX\_DE\_RATIO}$	3.0	3.5	4.0	dB
AC Coupling Capacitor(USB3.1/PCIe)	$C_{AC\_COUPLING}$	75	NA	200	nF
AC Coupling Capacitor(SATA)		6	NA	12	nF
Output rising time for 20% to 80%	T_r	25	NA	NA	ps
Output falling time for 20% to 80%	T_f	25	NA	NA	ps
Transmitter short circuit limit	I_{TX_SHORT}	NA	NA	20	mA
Output differential skew	T_{SKEW_DIFF}	-15	NA	15	ps
Receiver					
Input Voltage Swing	V_{RXDPP_C}	250	NA	1200	mVpp
The input differential impedance	R_{RXD_C}	80	100	120	Ohm
Single Ended input Resistance Matching	$R_{RXD\_C\_MS}$	NA	NA	5	%

3.7 Electrical Characteristics for SARADC

Table 3-9 Electrical Characteristics for SARADC

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Resolution			NA	12	NA	Bit
Anglog Input Range	AIN		AVSS18	NA	AVDD18	V
Differential Non-Linearity	DNL	PD = Low F_s = 1MS/s F_{CLK} = 20MHz F_{SOC} = 1MHz F_{AIN} = 10kHz ramp wave	NA	±1.0	±3.0	LSB
Integral Non-Linearity	INL		NA	±2.0	±6.0	LSB
Top Offset Voltage Error	E_{OT}		NA	±10	±20	LSB
Bottom Offset Voltage Error	E_{OB}		NA	±10	±20	LSB

3.8 Electrical Characteristics for TSADC

Table 3-10 Electrical Characteristics for TSADC

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Accuracy from -40℃ to 125℃	T_{JACC}	Temp: -40 ~ 125℃ Supply: 1.62V ~ 1.98V	NA	±3	±5	℃
Sensing Temperature Range	T_{RANGE}		-40	NA	125	℃
Resolution	T_{LSB}		NA	1	NA	℃

Chapter 4 Thermal Management

4.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature has to be below 125℃.

4.2 Package Thermal Characteristics

Table 4-1 provides the thermal resistance characteristics for the package used on the SoC. The resulting simulation data for reference only, please prevail in kind test.

Table 4-1 Thermal Resistance Characteristics

Parameter	Symbol	Typical	Unit
Junction-to-ambient thermal resistance	$\boldsymbol{\theta_{JA}}$	15.6	(℃/$\boldsymbol{W}$)
Junction-to-board thermal resistance	$\boldsymbol{\theta_{JB}}$	4.6	(℃/$\boldsymbol{W}$)
Junction-to-case thermal resistance	$\boldsymbol{\theta_{JC}}$	0.03	(℃/$\boldsymbol{W}$)

Note: The testing PCB is JEDEC 2S2P 114.3*mmx*76.2*mmx1.6mm, Ambient temperature is 25℃.*