Rockchip RK621 Datasheet

Revision 1.0
Nov. 2024

Revision History

Date	Revision	Description
2024-11-26	1.0	Initial release

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Chapter 1 Introduction

RK621 is a high-integration interface chip, which can support HDMI as input and MIPI as output with featured scaler inside. The key application scenario is extension of display output port for original application processor such as RK3288 /RK3399/RK3588, or HDMI in interface providing.

1.1 Features

1.1.1 Video input interface

- HDMI RX interface
  - Compliant with HDMI 1.4/HDMI 2.0
  - Supports HDCP 1.4
  - Supports 8/10bit per component video format
  - Supports rgb888/yuv444/yuv422/yuv420
  - Supports Max resolution 3840x2160@60fps
  - Supports data rates up to 600Mhz, with PHY bit rate 6Gbps per lane
  - Supports DDC Bus I2C master interface at 3.3/5V
  - Supports EDID and CEC function
  - Supports DVI

1.1.2 Video output interface

- MIPI TX interface
  - DSI
    - Compliant with MIPI DPHY V1.2
    - Support the DPI interface color coding mappings into 24-bit Interface
    - Up to 4 D-PHY Data Lanes
    - Supports data rate up to 1.3Gbps
  - CSI
    - Compliant with MIPI DPHY V1.2
    - Support format: YUV422
    - Up to 4 D-PHY Data Lanes
    - Supports data rate up to 1.3Gbps
- LVDS TX interface
  - Compliant with the Standard TIA/EIA-644-A LVDS standard
  - Supports data rate up to 1Gbps
  - Support 8bit format-1, format-2, format-3 display mode, Support 6bit display mode.

Table 1-1 RK621 video output interface

Interface	Resolution	Data rate	Bit rate per lane
MIPI DSI	1080p@60fps	NA	1.3Gbps
MIPI CSI	3840x2160@30fps	NA	1.3Gbps
LVDS	720p@60fps	NA	1 Gbps

1.1.3 RX adapter

- Support RX HDCP1.4 inside-key memory. It is readable and writable
- Support on-chip EDID memory. It is readable and writable

1.1.4 Post process

- CSC
  - RGB2YUV
  - YUV2RGB
  - YUV2VYU
  - CSC matrix
- Display interface
  - Asynchronous output pixel clock (PLL required)
  - Flexible display timing setting
  - Configurable border black area
- Scaling down

- Max input resolution: 3840x2160
- Arbitrary non-integer scaling ratio
- Support two mode: bilinear and average
- Max 1/4 scaling ratio for bilinear scaling down
- Max 1/4 scaling ratio for average scaling down

- Scaling up
  - Max output resolution: 1920x1080
  - Arbitrary non-integer scaling ratio
  - Support four scaling up mode for different effect
  - Max 4 scaling ratio

1.1.5 Others

- Audio
  - Support HDMI RX I2S interface, up to 192kHz sample rate, 2 channel
  - Support I/O I2S interface
- Package Type
  - QFN56 (body:6mm x 6mm, pitch0.35)

1.2 Block Diagram

The following diagram shows the basic block diagram for RK621.

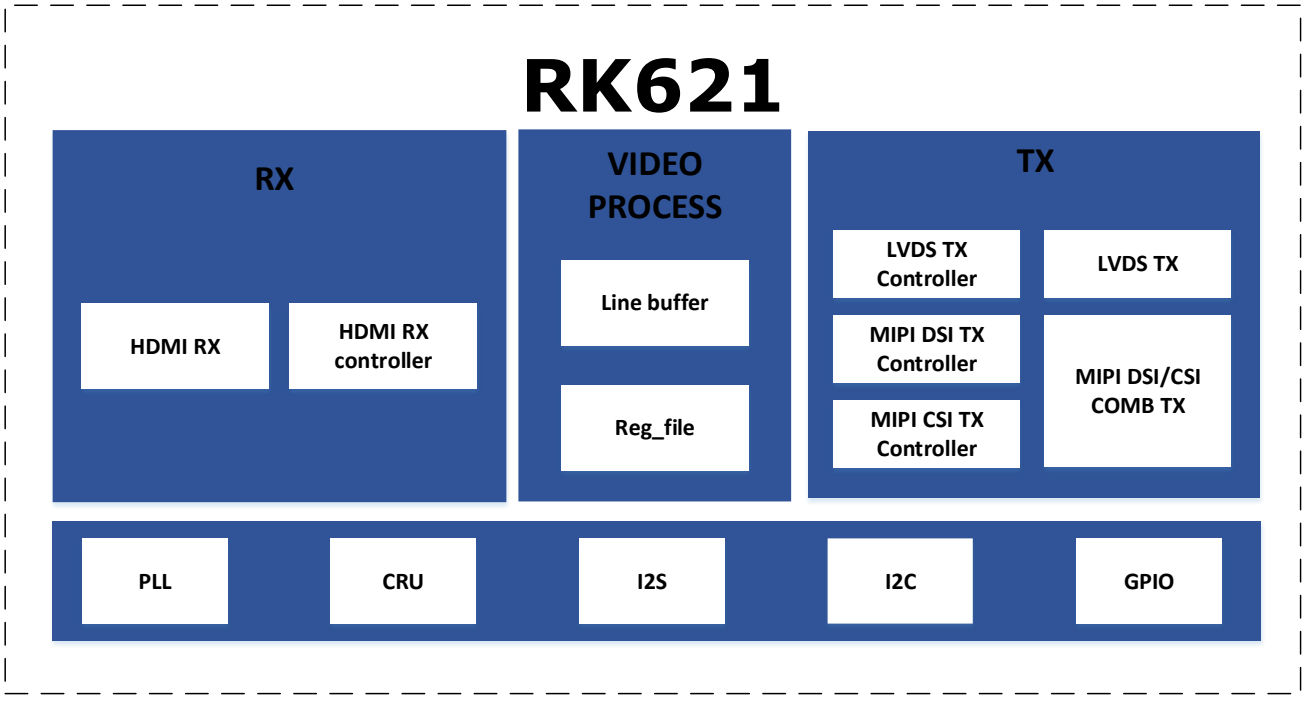

Fig. 1-1 RK621 Block Diagram

Chapter 2 Package Information

2.1 Order Information

Orderable Device	RoHS status	Package	Package Qty	Device Feature
RK621	RoHS	QFN6x6	4900PCS	High speed interface bridge chip

2.2 Top Marking

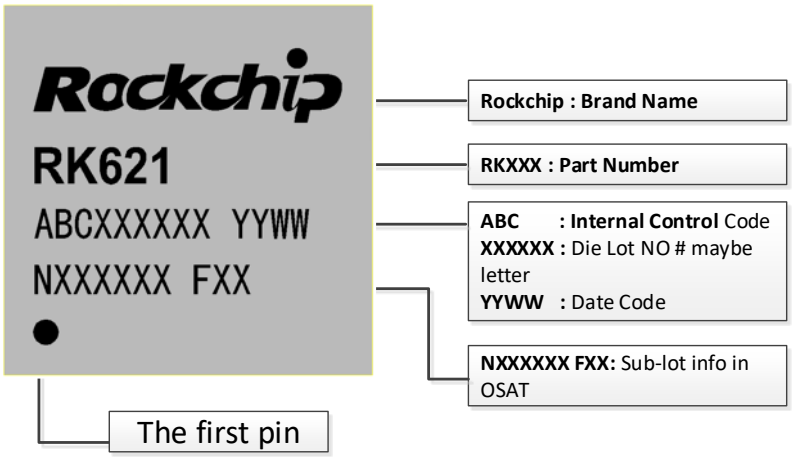

Fig. 2-1 RK621 Package definition

2.3 Package Dimension

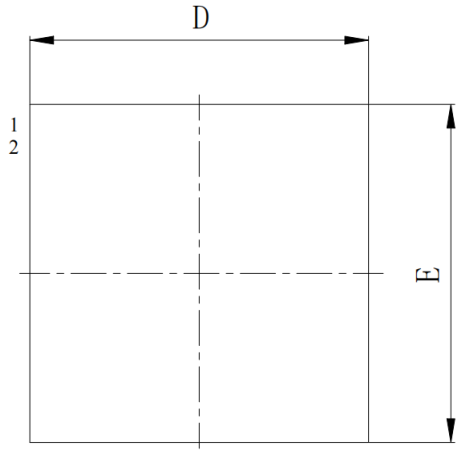

Fig. 2-2 RK621 Package Top View

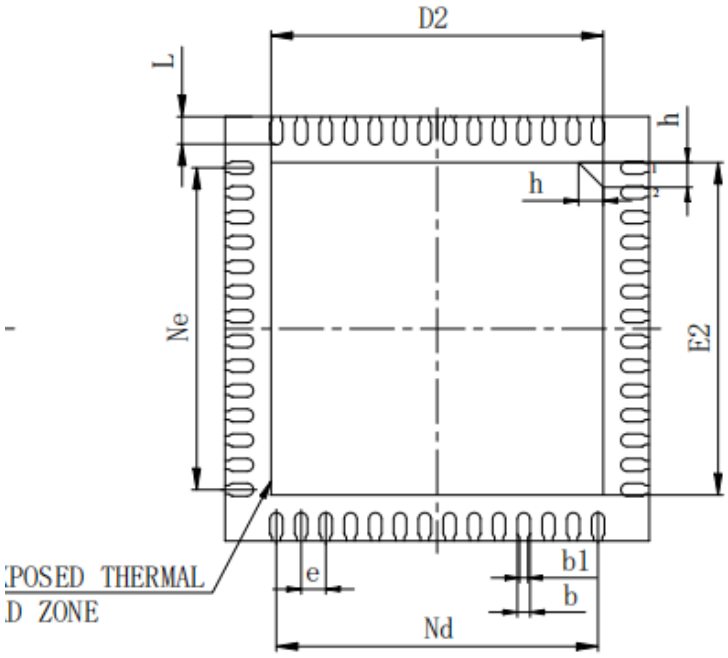

Fig. 2-3 RK621 Package Bottom View

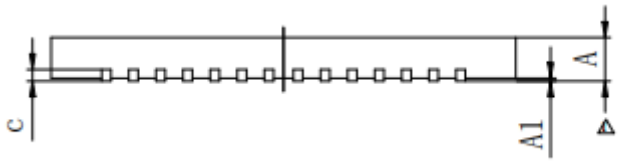

Fig. 2-4 RK621 Package side View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.13	0.18	0.23
b1	0.12REF		
c	0.18	0.20	0.25
D	5.90	6.00	6.10
D2	4.60	4.70	4.80
e	0.35BSC		
Ne	4.55BSC		
Nd	4.55BSC		
E	5.90	6.00	6.10
E2	4.60	4.70	4.80
L	0.35	0.40	0.45
h	0.30	0.35	0.40

Fig. 2-5 RK621 Package Dimension

2.4 MSL Information

Moisture sensitivity Level ： MSL3

2.5 Lead Finish/Ball material Information

Lead Finish/Ball material ： Sn

2.6 Pin Number Order

Table 2-1 RK621 QFN56 Pin Number Order Information

Pin Number	Pin Name	Pin Number	Pin Name
1	LVDS/MIPI_AVDD_1V1_1	29	HDMIRX_REXT
2	LVDS/MIPI_TX_CLKP	30	HDMIRX_CLKN
3	LVDS/MIPI_TX_CLKN	31	HDMIRX_CLKP
4	LVDS/MIPI_AVDD_3V3_1	32	HDMIRX_AVDD_3V3_1
5	LVDS/MIPI_TX1P	33	HDMIRX_DVDD_1V1_1
6	LVDS/MIPI_TX1N	34	HDMIRX_D0N
7	LVDS/MIPI_AVDD_1V1_2	35	HDMIRX_D0P
8	LVDS/MIPI_TX0P	36	HDMIRX_AVDD_2V5
9	LVDS/MIPI_TX0N	37	HDMIRX_D1N
10	DVDD_1	38	HDMIRX_D1P
11	VCCIO1_1	39	HDMIRX_AVDD_3V3_2
12	GPIO0_A3/I2S_LRCK_M0	40	HDMIRX_DVDD_1V1_2
13	GPIO0_A2/I2S_SCK_M0	41	HDMIRX_D2N
14	GPIO0_A4/I2S_D0_M0	42	HDMIRX_D2P
15	VSS1	43	DVDD_3
16	PLL_AVDD_3V3	44	GPIO3_B4/INT
17	OSC_XIN	45	RESETN
18	OSC_XOUT	46	TVSS
19	PLL_AVDD_1V1	47	I2C_ADDR/GPIO3_B3
20	GPIO1_B4/I2C_SCL	48	VCCIO1_3
21	GPIO1_B5/I2C_SDA	49	LVDS/MIPI_AVDD_3V3_2
22	GPIO1_B2/HDMIRX_SCL_M0	50	LVDS/MIPI_PLL_AVDD_3V3
23	GPIO1_B0/HDMIRX_HPD_M0	51	LVDS/MIPI_REXT
24	GPIO1_B1/HDMIRX_SDA_M0	52	LVDS/MIPI_AVDD_1V1_3
25	GPIO1_B3/HDMIRX_CEC_M0	53	LVDS/MIPI_TX3P
26	DVDD_2	54	LVDS/MIPI_TX3N
27	GPIO1_A0/TEST_CLKO/I2S_MCLK	55	LVDS/MIPI_TX2P
28	VCCIO1_2	56	LVDS/MIPI_TX2N

Chapter 3 Electrical Specification

3.1 Absolute Maximum Ratings

Table 3-1 RK621 Absolute Maximum Ratings

Parameters	Related Power Group	Max	Unit
DC supply voltage for internal digital logic@1.1v	DVDD_x	1.32	V
DC supply voltage for digital GPIO@3.3V mode	VCCIO1_x	3.99 3.99 3.99	V
DC supply voltage for HDMI RX	HDMIRX_AVDD_3V3_x HDMIRX_DVDD_1V1_x	3.99 1.32	V
DC supply voltage for LVDS/MIPI TX	LVDS/MIPI_PLL_AVDD_3V3 LVDS/MIPI_AVDD_3V3_x LVDS/MIPI_AVDD_1V1_x	3.99 3.99 1.32	V
DC supply voltage for PLL	PLL_AVDD_3V3 PLL_AVDD_1V1	3.99 1.32	V
Storage Temperature	Tstg	125	℃
Max Conjunction Temperature	Tj	125	℃

Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

3.2 Recommended Operating Condition

Following table describes the recommended operating condition.

Table 3-2 RK621 Recommended Operating Condition

Parameters	Symbol	Min	Typ	Max	Unit
DC supply voltage for internal digital logic@1.1v	DVDD_x	0.99	1.1	1.21	V
DC supply voltage for digital GPIO@3.3V mode	VCCIO1_x	3.135 3.135 3.135	3.3 3.3 3.3	3.465 3.465 3.465	V
DC supply voltage for HDMI RX	HDMIRX_AVDD_3V3_x HDMIRX_DVDD_1V1_x	3.135 0.99	3.3 1.1	3.465 1.21	V
DC supply voltage for LVDS/MIPI TX	LVDS/MIPI_PLL_AVDD_3V3 LVDS/MIPI_AVDD_3V3_x LVDS/MIPI_AVDD_1V1_x	3.135 3.135 0.99	3.3 3.3 1.1	3.465 3.465 1.21	V
DC supply voltage for PLL	PLL_AVDD_3V3 PLL_AVDD_1V1	3.135 0.99	3.3 1.1	3.465 1.21	V
PLL input clock frequency		N/A	24	N/A	MHz
Operating Temperature		-20	25	80	℃

3.3 DC Characteristics

Table 3-3 RK621 DC Characteristics

Parameters		Symbol	Min	Typ	Max	Units
Digital GPIO @3.3V for GPIO0/1/3	Input Low Voltage	Vil	-0.3	0	0.8	V
	Input High Voltage	Vih	2.0	3.3	3.465	V
	Output Low Voltage	Vol	NA	0	0.4	V
	Output High Voltage	Voh	2.4	3.3	NA	V
	Threshold Point	Vtr+	1	1.16	1.34	V
		Vtr-	1.02	1.19	1.39	V
	Pullup Resistor	Rpu	26	46	71	Kohm
	Pulldown Resistor	Rpd	27	48	102	Kohm

3.4 Recommended Operating Frequency

Table 3-4 RK621 Recommended Operating Frequency

Parameter	Condition	Symbol	Min	Typ	Max	Unit
CPLL	1.1V , 25 ℃	cpll	270	1188	1600	MHz
	1.21V , -40 ℃		270	1188	1600	
	0.99V , 125 ℃		270	1188	1600	
GPLL	1.1V , 25 ℃	gpll	270	984	1600	MHz
	1.21V , -40 ℃		270	984	1600	
	0.99V , 125 ℃		270	984	1600	
APLL	1.1V , 25 ℃	apll	270	984	1600	MHz
	1.21V , -40 ℃		270	984	1600	
	0.99V , 125 ℃		270	984	1600	
HDMI RX CTRL	1.1V , 25 ℃	dclk_rx	13.5	594	600	MHz
	1.21V , -40 ℃		13.5	594	600	
	0.99V , 125 ℃		13.5	594	600	
Process	1.1V , 25 ℃	Sclk	13.5	594	600	MHz
	1.21V , -40 ℃		13.5	594	600	
	0.99V , 125 ℃		13.5	594	600	

Chapter 4 Thermal Management

4.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature has to be below 125℃.

4.2 Package Thermal Characteristics

Table 4-1 provides the thermal resistance characteristics for the package used on the SoC. The resulting simulation data for reference only, please prevail in kind test.

Table 4-1 Thermal Resistance Characteristics

Symbol	Description	Value	Unit	Note
θ_{JA}	Junction-to-ambient thermal resistance	21.53	(℃/W)	(1)
θ_{JB}	Junction-to-board thermal resistance	8.18	(℃/W)	(2)
θ_{JC}	Junction-to-case thermal resistance	24.4	(℃/W)	(3)
ψ_{JT}	Thermal characterization parameter	0.37	(℃/W)	(4)

Note (1): The package-board system is placed in the natural convection (JEDEC JESD51-2 standard), and the 2S2P test-board is designed in accordance with JESD 51-7/JESD 51-9. The actual system design and environment may be different.

Note (2): θ_{JB} is measured in the special environment (JEDEC JESD51-8 standard), and the printed circuit board used to mount the devices is specified in JESD51-7.

Note (3): The thermal resistance θ_{JC} is provided in compliance with the JEDEC JESD51-14.

Note (4): ψ_{JT} - The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package, ψ_{JT} is measured in the test environment of θ_{JA} (JEDEC JESD51-2 standard).

