Rockchip RK625 Datasheet

Revision 1.0
Dec. 2020

Revision History

Date	Revision	Description
2020-12-29	1.0	Initial Release

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Chapter 1 Introduction

1.1 Overview

RK625 is a dedicated USB camera driver with integrated ISP and JPEG encoder. Supports 2 channel MIPI-CSI RX and USB2.0 HS with UVC1.1, which greatly enable its application to various low-power and low-cost camera products.

1.2 Features

The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

1.2.1 MCU Microprocessor

- ARM Cortex M0, 32-bit RISC processor
- Integrated interrupt controller
- 16KB I/D Cache
- 2-way set associative
- 256 bits Cache line

1.2.2 Memory Organization

- Internal on-chip memory
  - BootROM
  - Internal SRAM

- Memory device by Multiple Chip Package(MCP)
  - MCP with Serial Nor Flash by Flexible Serial Peripheral Interface(FSPI)
    - Support transfer data from/to serial flash device
    - Support x1, x2, x4 data bits mode
    - Support XIP(eXecute In Place)
    - Support 1 chip select
    - Support 2MB optional capacity

1.2.3 Internal Memory

- Internal BootROM
  - Support system boot from FSPI Nor Flash interface
  - Support system code download by USB2.0 interface (Device mode)

- Internal SRAM
  - Three banks system memory
    - Bank0: 64KB
    - Bank1: 160KB
    - Bank2: 160KB
  - High 32KB of Bank0 can be software configurable as Bank1 space or Bank2 space
  - 64KB TCM of MCU

1.2.4 System Component

- CRU (clock & reset unit)
  - One oscillator with 24MHz clock input
  - Support one PLL to generate all clocks
  - Support clock gating control for individual components
  - Support global soft-reset control for whole chip, also individual soft-reset for each component
  - Support auto clock gating with MCU WFI indication signal

- Timer
  - Total Six 64bits timers with interrupt-based operation
  - Support two operation modes: free-running and user-defined count
  - Support timer work state checkable

- Watchdog
  - 32 bits watchdog counter
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - Generate a system reset
    - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
  - Programmable reset pulse length
  - Total 16 defined-ranges of main timeout period

- DMAC
  - Support for memory-to-memory, memory-to-peripheral and peripheral-to-memory DMA transfers
  - Up to 3 channels, programmable channel priority
  - 6 hardware request from peripherals, programmable hardware request priority
  - Multi-block transfers achieved through
    - Linked Lists (block chaining)
    - Auto-reloading of channel registers
    - Contiguous address between blocks
  - Support Scatter/Gather

- JS HASH accelerator
  - JS Hash operation module to speed up the operation
  - Initial hash value configurable
  - 1M byte data length operation

- Buffer Manage
  - Support data interaction management between ISP/VICAP and JPEG Encoder
  - Support data interaction management between ISP/VICAP/JPEG Encoder and USB Controller

1.2.5 Video Input Interface

- MIPI RX D-PHY interface
  - Two MIPI RX D-PHY interfaces, connected with VICAP and ISP respectively
  - Compliant with the MIPI D-PHY interface specification, revision 1.1
  - Lane operation ranging from 80Mbps to 1.5Gbps in forward direction
  - Aggregate throughput up to 3Gbps with two data lanes of each D-PHY

- Video Capture(VICAP)
  - Support MIPI DPHY input interface
  - Support BT601/BT656 YCbCr 422 and RAW8/10/12 input
  - Support window cropping
  - Support virtual stride when write to internal memory
  - Support different stored address for Y and UV
  - Support 422/420/400 output

- Image Signal Processing(ISP)
  - Support MIPI DPHY input interface
  - Support raw8/raw10/raw12, YUV422 input
  - Luminance/chrominance and chrominance blue/red swapping for YUV input signals
  - Color processing (contrast, saturation, brightness, hue, offset, range)

- Black level compensation
- Four channel Lens shade correction (Vignetting)
- Auto focus measurement
- White balancing and black level measurement
- Auto exposure support by brightness measurement in 5x5 sub windows
- Defect pixel cluster correction unit (DPCC) supports on the fly and table based pixel correction
- De-noising pre filter (DPF)
- Enhanced color interpolation (RGB Bayer demosaicing)
- Chromatic aberration correction
- Combined edge sensitive Sharpening / Blurring filter (Noise filter)
- Color correction matrix (cross talk matrix)
- Flexible Histogram calculation
- Digital image effects (Emboss, Sketch, Sepia, B/W (Grayscale), Color Selection, Negative image, sharpening)
- Solarize effect through gamma correction
- Maximum input resolution of 2592x1944 pixels
- Main scaler with pixel-accurate up-scaling and down-scaling to any resolution between 2592x1944 and 32x16 pixel in processing mode
- Support image cropping

- JPEG Encoder
  - Two JPEG encoders, connected with VICAP and ISP respectively
  - Support YUV420 input formats
  - Support Non-progressive JPEG output data formats
  - Support image size up to 8192x8192
  - Maximum data rate up to 90 million pixels per second

1.2.6 Connectivity

- USB 2.0 Device Interface
  - Compatible with USB 2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Supports UVC1.1, transfer speed up to 32MBps

- SPI interface
  - Support two SPI Controllers
  - Support one chip-select for each SPI Controller
  - Support serial-master and serial-slave mode, software-configurable

- I2C interface
  - Support two I2C interfaces
  - Support 7bits and 10bits address mode
  - Software programmable clock frequency
  - Data on the I2C-bus can be transferred at rates of up to 100 kbit/s in the Standard-mode, up to 400 kbit/s in the Fast-mode or up to 1 Mbit/s in Fast-mode Plus

- UART Controller
  - Support three UART interfaces (UART0/UART1/UART2)
  - Embedded two 64-byte FIFO for TX and RX operation respectively
  - Support 5 bits, 6 bits, 7 bits, 8 bits serial data transmit or receive
  - Standard asynchronous communication bits such as start, stop and parity
  - Support different input clock for UART operation to get up to 4Mbps baud rate
  - Support auto flow control mode

- PWM
  - One on-chip PWM controllers with interrupt-based operation
  - Programmable pre-scaled operation to bus clock and then further scaled

- Embedded 32 bits timer/counter facility
- Support capture mode
- Provides reference mode and output various duty-cycle waveform
- Support continuous mode or one-shot mode

- Multiple group of GPIO
  - All of GPIOs can be used to generate interrupt
  - Support level trigger and edge trigger interrupt
  - Support configurable polarity of level trigger interrupt
  - Support configurable rising edge, falling edge and both edge trigger interrupt
  - Support configurable pull direction(pull-up or pull-down)

- Successive Approximation ADC (SARADC)
  - 10 bits resolution
  - Up to 1MS/s sampling rate
  - 3 single-ended input channels

1.3 Block Diagram

The following diagram shows the basic block diagram.

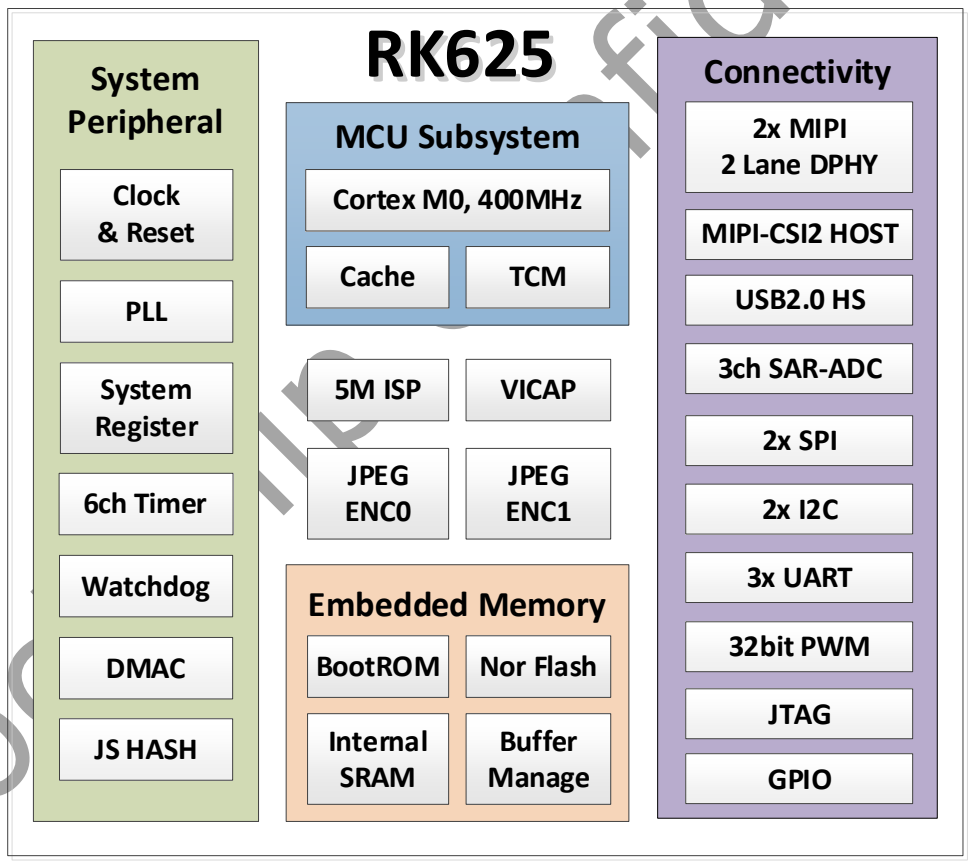


Fig.1-1 RK625 Block Diagram

Chapter 2 Package Information

2.1 Order Information

Orderable Device	RoHS status	Package	Package Qty	Device Feature
RK625	RoHS	QFN68L	2000pcs by reel	USB Camera MCU

2.2 Top Marking

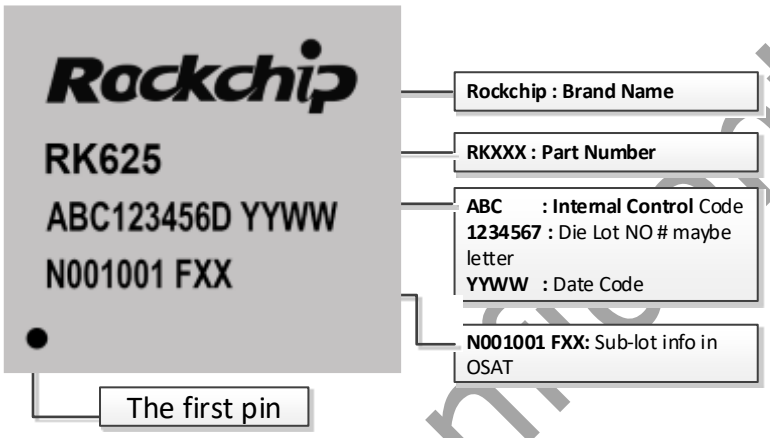


Fig.2-1 Package definition

2.3 QFN68L Dimension

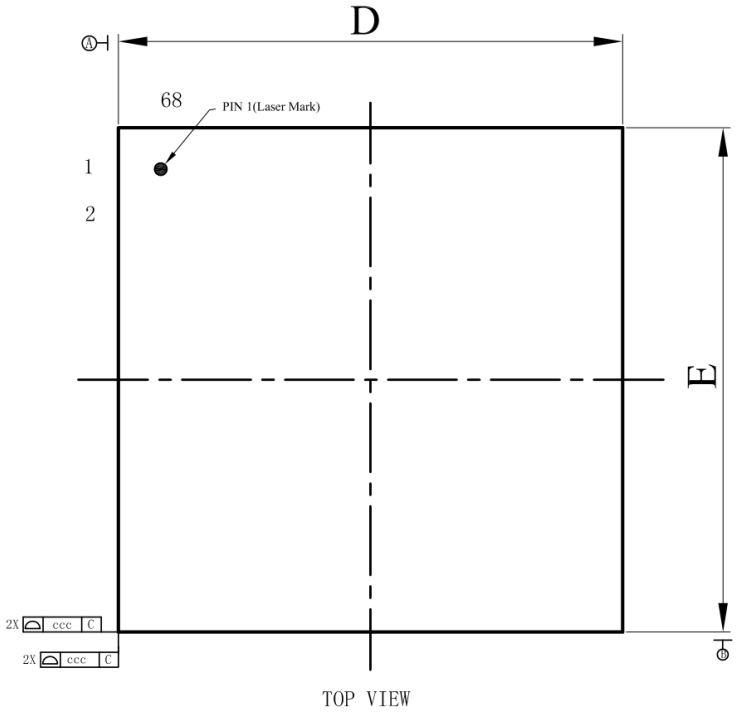


Fig.2-2 Package Top View

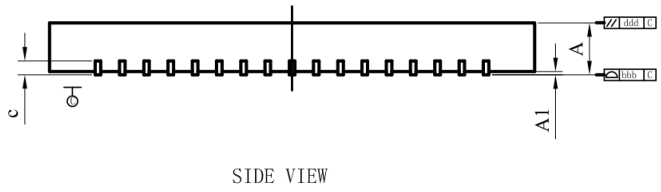


Fig.2-3 Package Side View

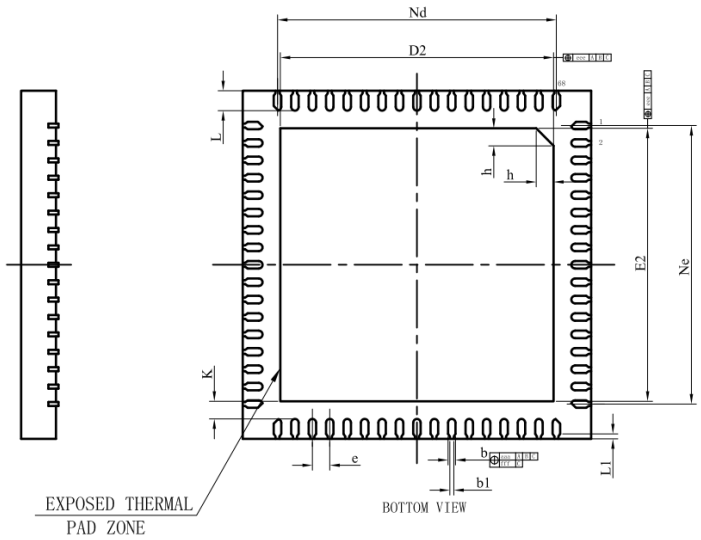


Fig.2-4 Package Bottom View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.10	0.15	0.20
b1	0.08REF		
c	0.18	0.20	0.25
D	6.90	7.00	7.10
D2	5.39	5.49	5.59
e	0.35BSC		
Nd	5.60BSC		
E	6.90	7.00	7.10
E2	5.39	5.49	5.59
Ne	5.60BSC		
L	0.35	0.40	0.45
L1	0.10REF		
K	0.20	--	--
h	0.30	0.35	0.40
aaa	0.07		
bbb	0.08		
ccc	0.10		
ddd	0.10		
eee	0.10		
fff	0.05		

Fig.2-5 Package dimension

2.4 Pin Map

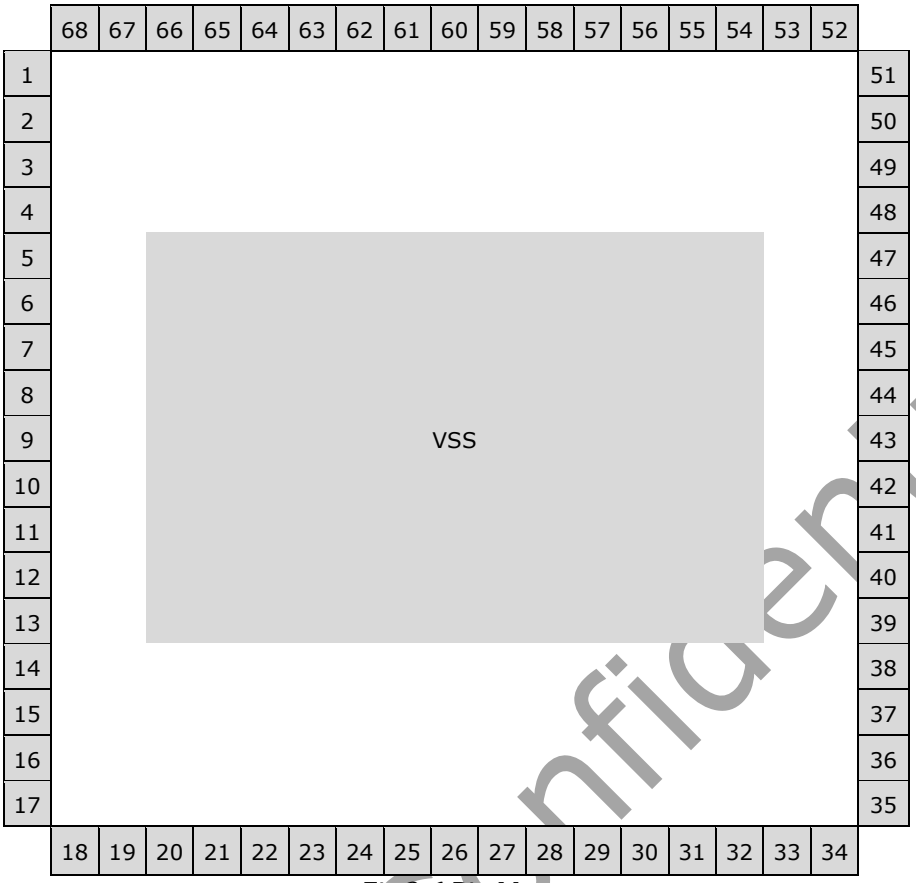


Fig.2-6 Pin Map

2.5 Pin Number List

Table 2-1 Pin Number List Information

No.	Pin Name	No.	Pin Name
1	I2C1_SDA/GPIO1_A1_u	36	SPI0_MOSI/GPIO0_A1_u
2	I2C1_SCL/GPIO1_A2_u	37	SPI0_CSN/GPIO0_A2_u
3	GPIO1_A3_u	38	SPI0_CLK/GPIO0_A3_d
4	VCCIO1_3V3_1	39	VCCIO0_1V8_1
5	GPIO1_B0_u	40	REF_CLKOUT/GPIO0_A4_u
6	GPIO1_B1_u	41	GPIO0_B3_d
7	GPIO1_B2_d	42	GPIO0_B0_d
8	NPOR_u	43	VCCIO2_1V8/3V3
9	TEST_d	44	VCC_PLL_1V8
10	VDD	45	VCC_PLL_1V1
11	SARADC_AIN[2]	46	XIN24_IN
12	SARADC_AIN[1]	47	XIN24_OUT
13	SARADC_AIN[0]	48	VDD
14	USB0_DN	49	PWM0/GPIO0_C0_d
15	USB0_DP	50	GPIO0_B6_z
16	USBRBIAS	51	GPIO0_A5_d
17	USB_1V1	52	I2C0_SCL/GPIO0_B5_u
18	VCCIO1_3V3_2	53	I2C0_SDA/GPIO0_B4_u
19	UART_RX/JTAG_TCK/GPIO1_B3_u	54	GPIO0_A6_u
20	UART_TX/JTAG_TMS/GPIO1_B4_u	55	GPIO0_B2_d
21	SPI1_CLK/GPIO1_A7_d	56	VCCIO0_1V8_2
22	SPI1_CSN/GPIO1_A6_u	57	MIPI_CLKOUT/GPIO0_B1_u
23	SPI1_MOSI/GPIO1_A5_u	58	GPIO0_A7_u
24	SPI1_MISO/GPIO1_A4_u	59	MIPI1_REXT
25	VDD	60	MIPI1_AVDD
26	MIPI0_REXT	61	MIPI1_D1P
27	MIPI0_AVDD	62	MIPI1_D1N

No.	Pin Name	No.	Pin Name
28	MIPI0_D1P	63	MIPI1_CLKN
29	MIPI0_D1N	64	MIPI1_CLKP
30	MIPI0_CLKN	65	MIPI1_AVDD
31	MIPI0_CLKP	66	MIPI1_D0P
32	MIPI0_AVDD	67	MIPI1_D0N
33	MIPI0_D0P	68	GPIO1_A0_d
34	MIPI0_D0N	EPAD	VSS
35	SPI0_MISO/GPIO0_A0_u		

2.6 Power/Ground IO Description

Table 2-2 Power/Ground IO information

Group	Pin#	Descriptions
VSS	EPAD	Digital Ground
VDD	10,25,48	Digital Power
VCCIO0_1V8_1	39	VCCIO0 Power Domain Power
VCCIO0_1V8_2	56	VCCIO0 Power Domain Power
VCCIO1_3V3_1	4	VCCIO1 Power Domain Power
VCCIO1_3V3_2	18	VCCIO1 Power Domain Power
VCCIO2_1V8/3V3	43	VCCIO2 Power Domain Power
USB_1V1	17	USB PHY Power
MIPI0_AVDD	27,32	MIPI0 DPHY Power
MIPI1_AVDD	60,65	MIPI1 DPHY Power
VCC_PLL_1V1	45	PLL Analog Power
VCC_PLL_1V8	44	PLL Analog Power

2.7 Function IO Description

Table 2-3 Function IO description

Pin	Pin Name	Func1	Func2	Func3	Pad Type①	Def②	Pull	Power Domain
1	I2C1_SDA/GPIO1_A1_u	I2C1_SDA	GPIO1_A1		I/O	I	up	VCCIO1
2	I2C1_SCL/GPIO1_A2_u	I2C1_SCL	GPIO1_A2		I/O	I	up	VCCIO1
3	GPIO1_A3_u	GPIO1_A3			I/O	I	up	VCCIO1
5	GPIO1_B0_u	GPIO1_B0			I/O	I	up	VCCIO1
6	GPIO1_B1_u	GPIO1_B1			I/O	I	up	VCCIO1
7	GPIO1_B2_d	GPIO1_B2			I/O	I	down	VCCIO1
8	NPOR_u	NPOR			I	I	up	VCCIO1
9	TEST_d	TEST			I	I	down	VCCIO1
11	SARADC_AIN[2]	SARADC_AIN[2]			A			VCCIO1
12	SARADC_AIN[1]	SARADC_AIN[1]			A			VCCIO1
13	SARADC_AIN[0]	SARADC_AIN[0]			A			VCCIO1
14	USB0_DP	USB0_DP			A			VCCIO1
15	USB0_DN	USB0_DN			A			VCCIO1
16	USBRBIAS	USBRBIAS			A			VCCIO1
19	UART_RX/jtagTCK/GPIO1_B3_u	UART_RX	JTAG_TCK	GPIO1_B3	I/O	I	up	VCCIO1
20	UART_TX/jtag_TMS/GPIO1_B4_u	UART_TX	JTAG_TMS	GPIO1_B4	I/O	I	up	VCCIO1
21	SPI1_CLK/GPIO1_A7_d	SPI1_CLK	GPIO1_A7		I/O	I	down	VCCIO1
22	SPI1_CSN/GPIO1_A6_u	SPI1_CSN	GPIO1_A6		I/O	I	up	VCCIO1
23	SPI1_MOSI/GPIO1_A5_u	SPI1_MOSI	GPIO1_A5		I/O	I	up	VCCIO1
24	SPI1_MISO/GPIO1_A4_u	SPI1_MISO	GPIO1_A4		I/O	I	up	VCCIO1
26	MIPI0_REXT	MIPI0_REXT			A			MIPI0
28	MIPI0_D1P	MIPI0_D1P			A			MIPI0
29	MIPI0_D1N	MIPI0_D1N			A			MIPI0
30	MIPI0_CLKN	MIPI0_CLKN			A			MIPI0
31	MIPI0_CLKP	MIPI0_CLKP			A			MIPI0
33	MIPI0_D0P	MIPI0_D0P			A			MIPI0
34	MIPI0_D0N	MIPI0_D0N			A			MIPI0
35	SPI0_MISO/GPIO0_A0_u	SPI0_MISO	GPIO0_A0		I/O	I	up	VCCIO0
36	SPI0_MOSI/GPIO0_A1_u	SPI0_MOSI	GPIO0_A1		I/O	I	up	VCCIO0
37	SPI0_CSN/GPIO0_A2_u	SPI0_CSN	GPIO0_A2		I/O	I	up	VCCIO0
38	SPI0_CLK/GPIO0_A3_d	SPI0_CLK	GPIO0_A3		I/O	I	down	VCCIO0
40	REF_CLKOUT/GPIO0_A4_u	REF_CLKOUT	GPIO0_A4		I/O	I	up	VCCIO0

Pin	Pin Name	Func1	Func2	Func3	Pad Type①	Def②	Pull	Power Domain
41	GPIO0_B3_d	GPIO0_B3			I/O	I	down	VCCIO0
42	GPIO0_B0_d	GPIO0_B0			I/O	I	down	VCCIO0
46	XIN24_IN	XIN24_IN			A			VCCIO0
47	XIN24_OUT	XIN24_OUT			A			VCCIO0
49	PWM0/GPIO0_C0_d	PWM0	GPIO0_C0		I/O	I	down	VCCIO0
50	GPIO0_B6_z	GPIO0_B6			I/O	I	high-z	VCCIO0
51	GPIO0_A5_d	GPIO0_A5			I/O	I	down	VCCIO0
52	I2C0_SCL/GPIO0_B5_u	I2C0_SCL	GPIO0_B5		I/O	I	up	VCCIO0
53	I2C0_SDA/GPIO0_B4_u	I2C0_SDA	GPIO0_B4		I/O	I	up	VCCIO0
54	GPIO0_A6_u	GPIO0_A6			I/O	I	up	VCCIO0
55	GPIO0_B2_d	GPIO0_B2			I/O	I	down	VCCIO0
57	MIPI_CLKOUT/GPIO0_B1_u	MIPI_CLKOUT	GPIO0_B1		I/O	I	up	VCCIO0
58	GPIO0_A7_u	GPIO0_A7			I/O	I	up	VCCIO0
59	MIPI1_REXT	MIPI1_REXT			A			MIPI1
61	MIPI1_D1P	MIPI1_D1P			A			MIPI1
62	MIPI1_D1N	MIPI1_D1N			A			MIPI1
63	MIPI1_CLKN	MIPI1_CLKN			A			MIPI1
64	MIPI1_CLKP	MIPI1_CLKP			A			MIPI1
66	MIPI1_D0P	MIPI1_D0P			A			MIPI1
67	MIPI1_D0N	MIPI1_D0N			A			MIPI1
68	GPIO1_A0_d	GPIO1_A0			I/O	I	down	VCCIO1

Notes:

①: Pad types: I = input, O = output, I/O = input/output (bidirectional)

AP = Analog Power, AG = Analog Ground
DP = Digital Power, DG = Digital Ground
A = Analog

②: Reset state: I = input, O = output;

2.8 IO Pin Name Description

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 2-4 IO function description list

Interface	Pin Name	Direction	Description
Misc	XIN24_IN	I	Clock input of 24MHz crystal
	XIN24_OUT	O	Clock output of 24MHz crystal
	NPOR	I	Chip hardware reset
	TEST	I	Chip test mode enable
	REF_CLKOUT	O	Clock output for external device
	MIPI_CLKOUT	O	Clock output for external device

Interface	Pin Name	Direction	Description
DEBUG	JTAG_TCK	I	tck signal for MCU
	JTAG_TMS	I/O	tms signal for MCU

Interface	Pin Name	Direction	Description
SPI	SPI*i*_CLK(*i*=0,1)	I/O	SPI serial clock
	SPI*i*_CSN(*i*=0,1)	I/O	SPI chip select signal, low active
	SPI*i*_MISO(*i*=0,1)	I/O	SPI serial data input/output
	SPI*i*_MOSI(*i*=0,1)	I/O	SPI serial data input/output

Interface	Pin Name	Direction	Description
PWM	PWM0	I/O	Pulse Width Modulation input and output

Interface	Pin Name	Direction	Description
I2C	I2C*i*_SDA(*i*=0,1)	I/O	I2C data
	I2C*i*_SCL(*i*=0,1)	I/O	I2C clock

Interface	Pin Name	Direction	Description
UART	UART_RX	I	UART serial data input
	UART_TX	O	UART serial data output

Interface	Pin Name	Direction	Description
USB 2.0	USB0_DP	I/O	USB 2.0 Data signal DP
	USB0_DN	I/O	USB 2.0 Data signal DN
	USBRBIAS	I/O	Connect 133ohm resistor to ground to generate reference current

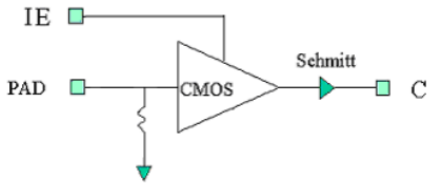
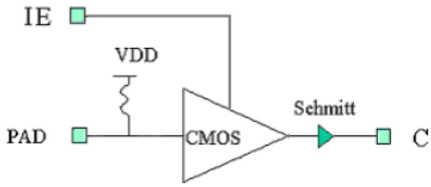
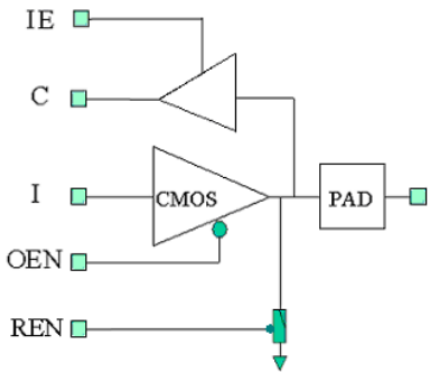
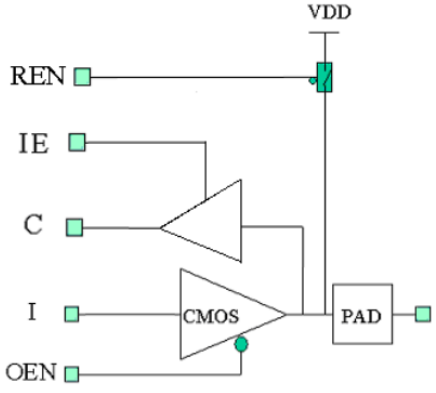
Interface	Pin Name	Direction	Description
MIPI0	MIPI0_D0P	I/O	Positive D-PHY Differential Data Line0 Receiver
	MIPI0_D0N	I/O	Negative D-PHY Differential Data Line0 Receiver
	MIPI0_D1P	I/O	Positive D-PHY Differential Data Line1 Receiver
	MIPI0_D1N	I/O	Negative D-PHY Differential Data Line1 Receiver
	MIPI0_CLKP	I/O	Positive D-PHY Differential Clock Line Receiver
	MIPI0_CLKN	I/O	Negative D-PHY Differential Clock Line Receiver
	MIPI0_REXT	I/O	External 4.02 KΩ Resistor Connection

Interface	Pin Name	Direction	Description
MIPI1	MIPI1_D0P	I/O	Positive D-PHY Differential Data Line0 Receiver
	MIPI1_D0N	I/O	Negative D-PHY Differential Data Line0 Receiver
	MIPI1_D1P	I/O	Positive D-PHY Differential Data Line1 Receiver
	MIPI1_D1N	I/O	Negative D-PHY Differential Data Line1 Receiver
	MIPI1_CLKP	I/O	Positive D-PHY Differential Clock Line Receiver
	MIPI1_CLKN	I/O	Negative D-PHY Differential Clock Line Receiver
	MIPI1_REXT	I/O	External 4.02 KΩ Resistor Connection

2.9 IO Type

The following list shows Digital IO type.

Table 2-5 IO Type List

Type	Diagram	Description	Pin Name
A		Enable controlled Schmitt trigger input pad with pull-down	Pad of digital GPIO
B		Enable controlled Schmitt trigger input pad with pull-up	Pad of digital GPIO
C		3-state output pad with enable controlled input and enable controlled pull-down	Pad of digital GPIO
D		3-state output pad with enable controlled input and enable controlled pull-up	Pad of digital GPIO

Chapter 3 Electrical Specification

3.1 Absolute Ratings

The below table provides the absolute ratings. Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

Table 3-1 Absolute ratings

Parameters	Related Power Group	Min	Max	Unit
Supply voltage for Digital	VDD	0	1.21	V
Supply voltage for VCCIO0_1V8_1	VCCIO0_1V8_1	0	1.98	V
Supply voltage for VCCIO0_1V8_2	VCCIO0_1V8_2	0	1.98	V
Supply voltage for VCCIO1_3V3_1	VCCIO1_3V3_1	0	3.63	V
Supply voltage for VCCIO1_3V3_1	VCCIO1_3V3_2	0	3.63	V
Supply voltage for VCCIO2_1V8/3V3	VCCIO2_1V8/3V3	0	3.63	V
Supply voltage for USB	USB_1V1	0	1.21	V
Supply voltage for MIPI0_AVDD	MIPI0_AVDD	0	2.75	V
Supply voltage for MIPI1_AVDD	MIPI1_AVDD	0	2.75	V
Supply voltage for VCC_PLL_1V1	VCC_PLL_1V1	0	1.21	V
Supply voltage for VCC_PLL_1V8	VCC_PLL_1V8	0	1.98	V
Storage Temperature	Tstg			℃
Max Conjunction Temperature	Tj	-40	125	℃

3.2 Recommended Operating Condition

Following table describes the recommended operating condition.

Table 3-2 Recommended operating condition

Parameters	Symbol	Min	Typ	Max	Unit
Supply voltage for Digital	VDD	0.99	1.10	1.21	V
Supply voltage for VCCIO0_1V8_1	VCCIO0_1V8_1	1.62	1.80	1.98	V
Supply voltage for VCCIO0_1V8_2	VCCIO0_1V8_2	1.62	1.80	1.98	V
Supply voltage for VCCIO1_3V3_1	VCCIO1_3V3_1	2.97	3.30	3.63	V
Supply voltage for VCCIO1_3V3_1	VCCIO1_3V3_2	2.97	3.30	3.63	V
Supply voltage for VCCIO2_1V8/3V3	VCCIO2_1V8/3V3	2.97 1.62	3.30 1.80	3.63 1.98	V
Supply voltage for USB	USB_1V1	0.99	1.10	1.21	V
Supply voltage for MIPI0_AVDD	MIPI0_AVDD	2.25	2.50	2.75	V
Supply voltage for MIPI1_AVDD	MIPI1_AVDD	2.25	2.50	2.75	V
Supply voltage for VCC_PLL_1V1	VCC_PLL_1V1	0.99	1.10	1.21	V
Supply voltage for VCC_PLL_1V8	VCC_PLL_1V8	1.62	1.80	1.98	V
OSC input clock frequency		N/A	24	N/A	MHz
Ambient Operating Temperature	T_A	TBD	25	TBD	℃

Notes:

② Symbol name is same as the pin name in the io descriptions

3.3 DC Characteristics

Table 3-3 DC Characteristics

Parameters		Symbol	Min	Typ	Max	Unit
Digital GPIO @3.3V mode	Input Low Voltage	Vil	-0.3	NA	0.8	V
	Input High Voltage	Vih	2.0	NA	3.6	V
	Output Low Voltage	Vol	NA	NA	0.4	V
	Output High Voltage	Voh	2.4	NA	NA	V
	Pullup Resistor	Rpu	27	40	64	Kohm
	Pulldown Resistor	Rpd	30	46	80	Kohm
Digital GPIO @1.8V mode	Input Low Voltage	Vil	-0.3	NA	0.63	V
	Input High Voltage	Vih	1.17	NA	2.1	V
	Output Low Voltage	Vol	NA	NA	0.45	V
	Output High Voltage	Voh	1.35	NA	NA	V
	Pullup Resistor	Rpu	53	89	165	Kohm
	Pulldown Resistor	Rpd	53	96	194	Kohm

3.4 Electrical Characteristics for General IO

Table 3-4 Electrical Characteristics for Digital General IO

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
Digital GPIO @3.3V mode	Input leakage current	Ii	Vin = 3.3V or 0V	NA	NA	10	uA
	Tri-state output leakage current	Ioz	Vout = 3.3V or 0V	NA	NA	10	uA
Digital GPIO @1.8V mode	Input leakage current	Ii	Vin = 1.8V or 0V	NA	NA	10	uA
	Tri-state output leakage current	Ioz	Vout = 1.8V or 0V	NA	NA	10	uA

3.5 Electrical Characteristics for PLL

Table 3-5 Electrical Characteristics for PLL

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
PLL	Input clock frequency(Int)	F_{in}	Fin = FREF @1.8V/1.1V	1		800	MHz
	Input clock frequency(Frac)	F_{in}	Fin = FREF @1.8V/1.1V	10		800	MHz
	VCO operating range	F_{vco}	Fvco = Fref * FBDIV @1.8V/1.1V	600		2400	MHz
	Lock time	T_{lt}	FREF=25M, REFDIV=1 @1.8V/1.1V		1000	1500	Input clock cycles
	VDDHV current consumption		Fvco = 1000MHz, @1.8V Current scale as $(Fvco/1GHz)^{1.5}$		1	1.2	mA
	DVDD Current consumption		DVDD =1.1V		1.3	1.56	uA/MHz
	Power consumption (power-down mode)		PD=HIGH, @27 ℃		0.01@1.8v 10@1.1v		uA

Notes:

① REFDIV is the input divider value;

② FBDIV is the feedback divider value;

③ VDDHV is supplied by VCC_PLL_1V8, DVDD is supplied by VCC_PLL_1V1

3.6 Electrical Characteristics for USB 2.0 Interface

Table 3-6 Electrical Characteristics for USB 2.0 Interface

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Output resistance	Rout	Classic mode HS mode	40.5	45	49.5	ohm
Output Capacitance	Cout				3	pF
Differential output signal high	Voh	Classic(LS/FS),Io=0mA	2.97	3.3	3.63	V
		Classic(LS/FS),Io=6mA	2.2	2.7		V
		HS mode,Io=0mA	360	400	440	mV
Differential output signal low	Vol	Classic(LS/FS),Io=0mA	-0.33	0	0.33	V
		Classic(LS/FS),Io=6mA		0.3	0.8	V
		HS mode,Io=0mA	-40	0	40	mV
Output Common Mode Voltage	VM	Classic(LS/FS) mode	1.45	1.65	1.85	V
		HS mode	0.175	0.2	0.225	V
Rise and fall time	Tr/Tf	LS mode	75	87.5	300	ns
		FS mode	4	12	20	ns
		HS mode	0.8	1.0	1.2	ns
Receiver sensitivity	Rsens	Classic(LS/FS) mode		±250		mV
		HS mode		±25		mV
Receiver common mode	RCM	Classic(LS/FS) mode	0.8	1.65	2.5	V
		HS mode(differential and squelch comparator)	0.1	0.2	0.3	V
		HS mode(disconnect comparator)	0.5	0.6	0.7	V
Input capacitance	Cin	Seen at D+ or D-			3	pF
Pulldown Resistor on DP/DM	Rpu		14.5	15	16	Kohm
Pullup Resistor on DP/DM	Rpd		2.35	2.4	2.5	Kohm
UID Pullup resistor			160	200	240	Kohm

3.7 Electrical Characteristics for MIPI DPHY

Table 3-7 Electrical Characteristics for MIPI DPHY

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Input signal voltage range	V_I		-50		1350	mV
Ground shift	V_{GNDSH}		-50		50	mV
Maximum transient output voltage level	$V_{OH(absmax)}$		-0.15		1.45	V
Maximum transient time above $V_{OH(absmax)}$	$t_{vOH(absmax)}$				20	ns
Differential input high voltage threshold	V_{IDTH}				70	mV
Differential input low voltage threshold	V_{IDTL}		-70			mV
Single ended input high voltage	V_{IHHS}				460	mV
Single ended input low voltage	V_{ILHS}		-40			mV
Input common mode voltage	V_{CMRXDC}		70		330	mV
Differential input impedance	Z_{ID}		80		125	ohm

3.8 Electrical Characteristics for SARADC

Table 3-8 Electrical Characteristics for SARADC

Parameters	Symbol	Test condition	Min	Typ	Max	Units
ADC resolution				10		Bits
Conversion speed	Fs				1	MSPS
Differential Non Linearity	DNL				+/-0.16	LSB
Integral Non Linearity	INL				+/-0.15	LSB
Input Capacitance	CIN			1		pF
Sampling Clock	SOC				1	MHz
Main Clock Frequency	CLK				11	MHz
Data Latency				10		Clock Cycle
SNR plus Distortion (Up to 5th harmonic)	SINAD	Fin=1.05K Fin=463K		58.4 58.9		dB
Spurious-Free Dynamic Range	SFDR	Fin=1.05K Fin=463K		82.4 66.0		dB
Second-Harmonic Distortion	2HD	Fin=1.05K Fin=463K		-90.7 -75.0		dB
Third-Harmonic Distortion	3HD	Fin=1.05K Fin=463K		-91.1 -66.0		dB
Total Harmonic Distortion (First 5 Harmonics)	THD	Fin=1.05K Fin=463K		-78.7 -64.6		
Effective Number of Bits	ENOB	Fin=1.05K Fin=463K		9.42 9.50		Bits
Analog Supply Current				590		uA
Digital Supply Current				22		uA
Power Down Current				0.5		uA

Chapter 4 Thermal Management

4.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature has to be below 125℃.

4.2 Package Thermal Characteristics

Table 4-1 provides the RK625 thermal resistance characteristics for the package used on the MCU. The resulting simulation data for reference only, please prevail in kind test.

Table 4-1 Thermal Resistance Characteristics

Parameter	Symbol	Typical	Unit
Junction-to-ambient thermal resistance	$\boldsymbol{\theta_{JA}}$	29.0	(℃/$\boldsymbol{W}$)
Junction-to-board thermal resistance	$\boldsymbol{\theta_{JB}}$	6.6	(℃/$\boldsymbol{W}$)
Junction-to-case thermal resistance	$\boldsymbol{\theta_{JC}}$	8.7	(℃/$\boldsymbol{W}$)

Note: The testing PCB is 4 layers, 114.3 mm × 101.5 mm, 1.6 mm thickness, Ambient temperature is 25℃.