

# Rockchip RK628E Datasheet

## Revision History

Date	Revision	Description
2024-07-02	1.4	Update the parameters in 3.1 Absolute Maximum Ratings and 3.2 Recommended Operating Condition
2022-01-05	1.3	Update the description
2021-08-01	1.2	Update the description
2020-06-01	1.1	Update the description
2020-04-13	1.0	Initial released

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## Chapter 1 Introduction

RK628E is a high-integration interface chip, which can support HDMI /parallel RGB /BT.1120 as input and dual MIPI/dual LVDS/GVI(general video interface)/parallel RGB/ BT.1120 as output with featured scaler inside. The key application scenario is extension of display output port for original application processor such as RK3288 /RK3399, or HDMI in interface providing.

### 1.1 Features

#### 1.1.1 Video input interface

- HDMI RX interface
  - Compliant with HDMI 1.4/HDMI 2.0
  - Supports HDCP 1.4
  - Supports 8/10bit per component video format
  - Supports rgb888/yuv444/yuv422/yuv420
  - Supports Max resolution 4096x2304@60fps
  - Supports data rates up to 300MHZ,with phy bit rate 3Gbps per lane
  - Supports DDC Bus I2C master interface at 3.3/5V
  - Supports EDID and CEC function
- Parallel IN interface
  - Supports Max resolution 1080p@60fps
  - Supports 16bits BT.1120 in
  - Supports 24bits parallel RGB in

Table 1-1 RK628E video input interface

Interface	Resolution	Data rate	Bit rate per lane
HDMI	4096x2304@60	NA	3Gbps
BT.1120	1080p@60fps	148.5M	NA
RGB	1080p@60fps	148.5M	NA

#### 1.1.2 Video output interface

- HDMI TX interface
  - Supports all DTV resolutions including 720p /1080p
  - Supports data rate from 25MHz, 1.65bps up to 3.4Gbps over a Single channel HDMI Internal SRAM
  - TMDS Tx Drivers with programmable output swing, resister values and pre-emphasis
  - DDC Bus I2C master interface at 3.3/5V
  - The EDID and CEC function are also supported by HDMI Transmitter Controller
- MIPI TX interface
  - DSI
    - ◆ Compliant with MIPI DPHY V1.2
    - ◆ Support the DPI interface color coding mappings into 24-bit Interface
    - ◆ Up to 4 D-PHY Data Lanes per channel
    - ◆ Supports data rate up to 1.2Gbps
    - ◆ Supports dual channel DSI
  - CSI
    - ◆ Compliant with MIPI DPHY V1.2
    - ◆ Support format: YUV422
    - ◆ Up to 4 D-PHY Data Lanes
    - ◆ Supports data rate up to 1.2Gbps
    - ◆ Supports single channel
- GVI TX interface
  - Supports RGB666/RGB888/RGB101010/YUV422-8bit/YUV422-10bit format
  - Supports Max resolution 4096x2304@60fps
  - Supports up to 3.75Gbps data rate(effective data rate 3Gbps)
  - Supports 1/2/4/8 lanes

- Supports output lanes flexible mapping
- Supports 1/2 section mode
- LVDS TX interface
  - Compliant with the Standard TIA/EIA-644-A LVDS standard
  - Supports data rate up to 1Gbps
  - Support 8bit format-1, format-2, format-3 display mode, Support 6bit display mode.
  - Supports dual channel LVDS
- Parallel OUT interface
  - Supports Max resolution 1080p@60fps
  - Supports 16bits BT.1120 out
  - Supports 24bits parallel RGB out

Table 1-2 RK628E video output interface

Interface	Resolution	Data rate	Bit rate per lane
GVI	4096x2304@60fps	NA	3.75Gbps
Dual MIPI DSI	2560x1600@60fps	NA	1.2Gbps
MIPI DSI	1080p@60fps	NA	1.2Gbps
MIPI CSI	3840x2160@30fps	NA	1.2Gbps
Dual LVDS	1080p@60fps	NA	1 Gbps
LVDS	720p@60fps	NA	1.Gbps
BT.1120	1080p@60fps	148.5M	NA
RGB	1080p@60fps	148.5M	NA
HDMI	1080p@60fps	148.5M	NA

### 1.1.3 TX/RX adapter

- Interaction of HDP signal between HDMI TX and HDMI RX
- Support HDMI TX CEC function
- Support RX HDCP1.4 inside-key memory. It is readable and writable
- Support HDMI RX/TX
- Support on-chip EDID memory. It is readable and writable

### 1.1.4 Post process

- CSC
  - RGB2YUV
  - YUV2RGB
  - YUV2VYU
- Display interface
  - Parallel display Interface: 30-bit(RGB/YUV)
  - Asynchronous output pixel clock (PLL required)
  - Flexible display timing setting
  - Configurable border black area
- Scaling down
  - Max input resolution: 4096x2304
  - Arbitrary non-integer scaling ratio
  - Support two mode: bilinear and average
  - Max 1/4 scaling ratio for bilinear scaling down
  - Max 1/6 scaling ratio for average scaling down
- Scaling up
  - Max output resolution: 4096x2304
  - Arbitrary non-integer scaling ratio
  - Support four scaling up mode for different effect
  - Max 6 scaling ratio
- Split
  - Left-right mode
  - Odd-even mode

### 1.1.5 Others

- Audio
  - Support HDMI RX I2S interface, up to 192kHz sample rate, 8 channel

- Support I/O I2S interface, 8 channel
- Support HDMI TX I2S interface, 8 channel
- Support the connection of RX and TX's I2S
- EFUSE
  - One-time programmable nonvolatile EFUSE storage cells organized as 64x8 bits
  - 1.1V typical core voltage
  - AVDD is NOT allowed to exceed 2.75V
  - Burning requirements:
    - ◆ 2.5V typical burning voltage (AVDD), AVDD must be high during PGM mode. AVDD must be low or floating during READ mode and inactive mode
    - ◆ 2us burning pulse width
    - ◆ Ambient temperature range of 10~40°C
    - ◆ Burning at wafer, package, or field level
- Package Type
  - BGA144

## 1.2 Block Diagram

The following figure shows the basic block diagram for RK628E.

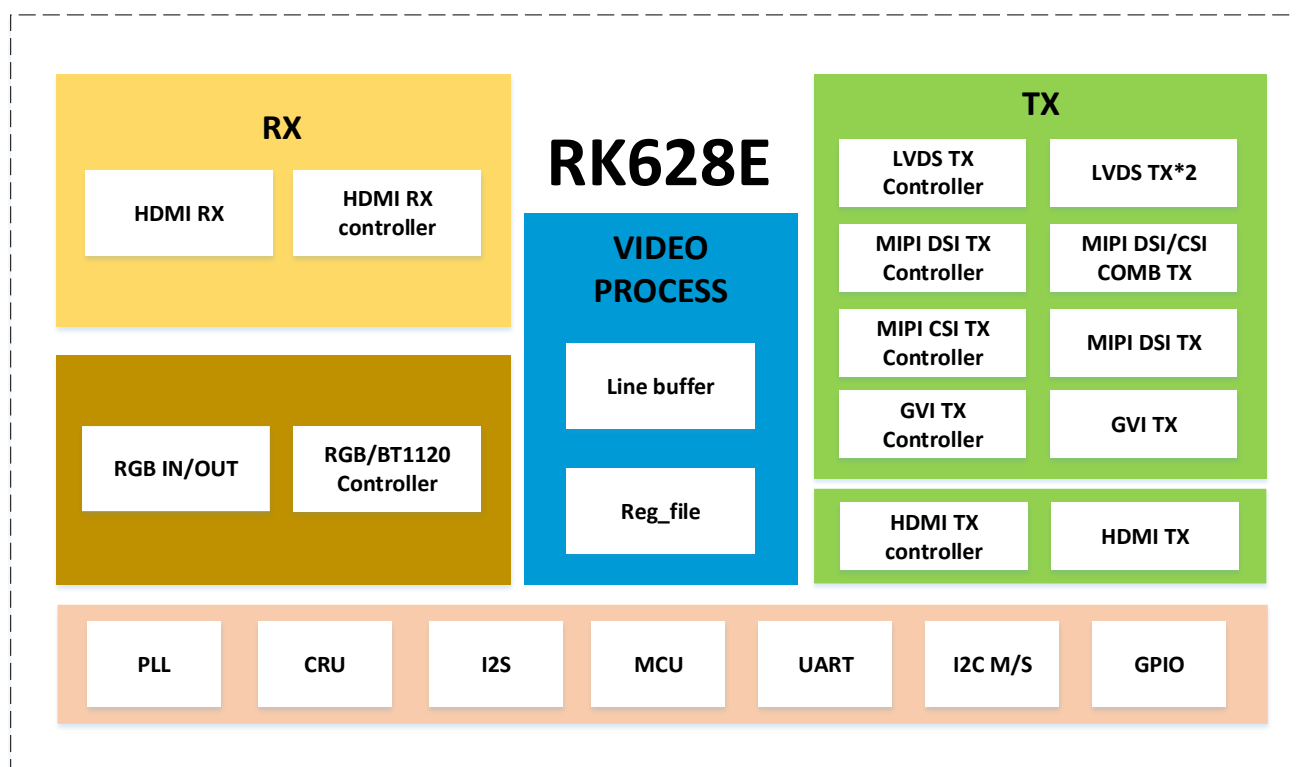


Fig. 1-1 RK628E Block Diagram

## Chapter 2 Package Information

### 2.1 Order Information

Orderable Device	RoHS status	Package	Package Qty	Device Feature
RK628E	RoHS	TFBGA144	3480pcs	High speed interface bridge chip

### 2.2 Top Marking

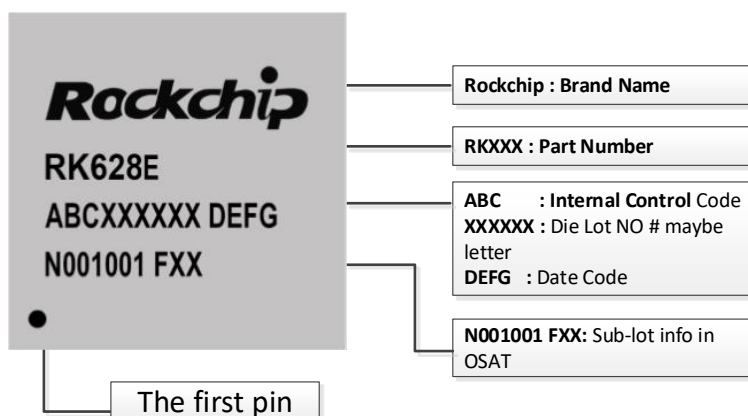


Fig. 2-1 RK628E Package definition

### 2.3 Package Information

BGA144(body: 8mmx8mm; ball size: 0.3mm; ball pitch: 0.65mm)

### 2.4 TFBGA144 Dimension

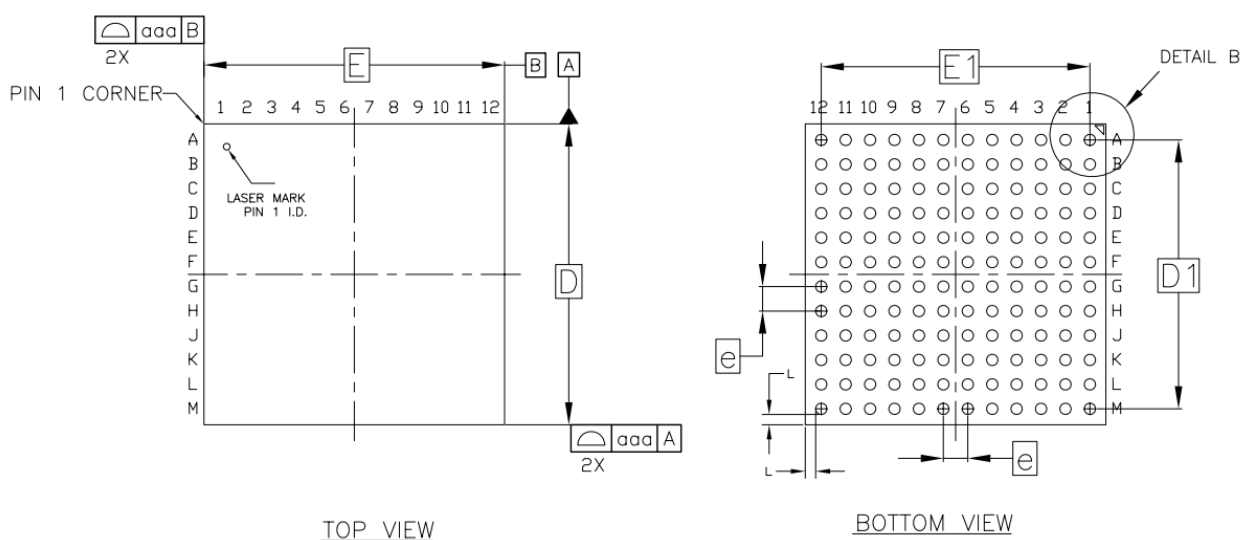


Fig. 2-2 RK628E TFBGA144 Package Top View and bottom View

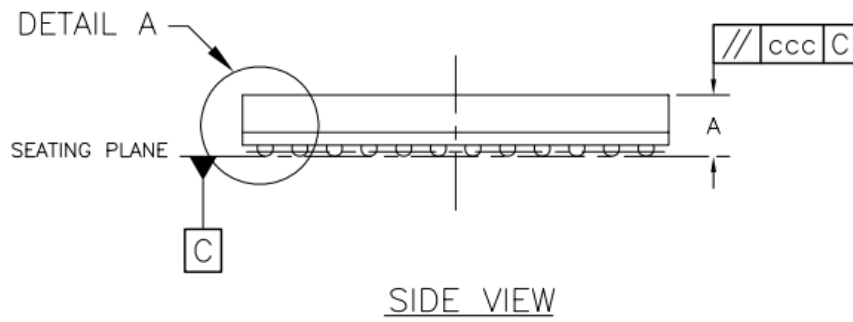


Fig. 2-3 RK628E TFBGA144 Package side View

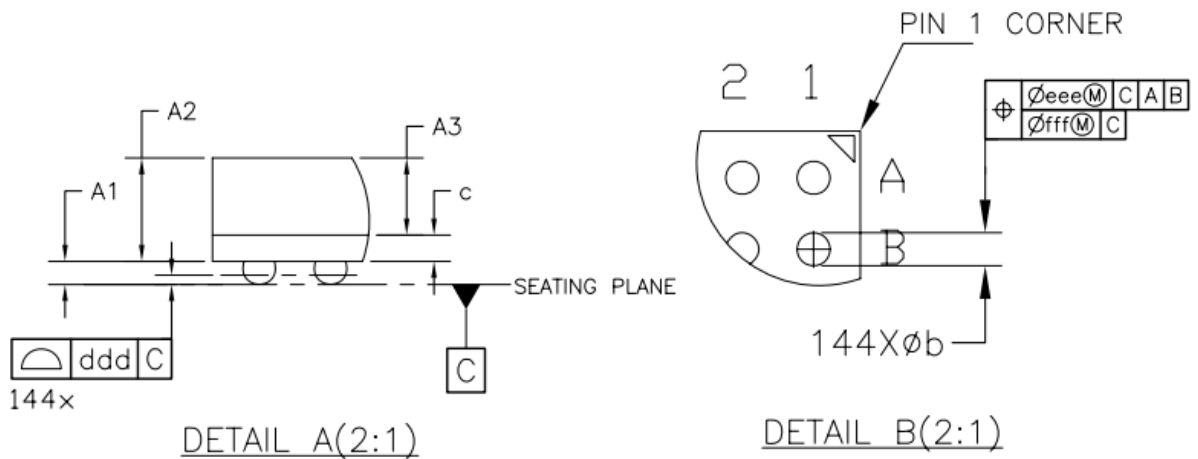


Fig. 2-4 RK628E TFBGA144 Package side View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	1.15	1.23
A1	0.16	0.21	0.26
A2	0.89	0.94	0.99
A3	0.70 BASIC		
c	0.20	0.24	0.28
D	7.90	8.00	8.10
D1	7.15 BASIC		
E	7.90	8.00	8.10
E1	7.15 BASIC		
e	0.65 BASIC		
b	0.25	0.30	0.35
L	0.275 REF		
aaa	0.15		
ccc	0.15		
ddd	0.10		
eee	0.15		
fff	0.08		

Fig. 2-5 RK628E TFBGA144 Package Dimension

Note:

1. CONTROLLING DIMENSION: MILLIMETER.

2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION *b* IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. SPECIAL CHARACTERISTICS C CLASS: A, *ddd*.
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
6. THE TILT OF HEAT SINK SHOULD BE WITHIN 10MIL(0.254mm) (VERTICAL POSITION).

## 2.5 TFBGA144 Pin Number Order

Table 2-1 RK628E TFBGA144 Pin Number Order Information

Pin Number	Pin Name	Pin Number	Pin Name
A1	VSS_1	G1	GVI/LVDS/MIPI_TX0N
A2	GVI/LVDS/MIPI_TX5P	G2	GVI/LVDS/MIPI_TX0P
A3	GVI/LVDS/MIPI_TX6P	G3	VSS_25
A4	GVI/LVDS/MIPI_TX7P	G4	VSS_19
A5	GVI/LVDS/MIPI_TX8P	G5	VSS_9
A6	GVI/LVDS/MIPI_TX9P	G6	VSS_13
A7	GPIO3_B1/GVI_HPD	G7	VSS_16
A8	GPIO3_A1/VOP_HSYNC	G8	VSS_20
A9	VOP_DCLK	G9	HDMIRX_EXTR
A10	GPIO2_C4/VOP_D20/JTAGTDI	G10	GPIO2_A0/VOP_D0
A11	GPIO2_C1/VOP_D17/XIPSFCMISO	G11	GPIO2_A1/VOP_D1
A12	VSS_2	G12	GPIO2_A2/VOP_D2
B1	GVI/LVDS/MIPI_REXT	H1	GPIO0_A7/I2S_D3_M0/UARTTRTSN
B2	GVI/LVDS/MIPI_TX5N	H2	GPIO0_A6/I2S_D2_M0/UARTCTSN
B3	GVI/LVDS/MIPI_TX6N	H3	GPIO0_A5/I2S_D1_M0/UARTRX
B4	GVI/LVDS/MIPI_TX7N	H4	RESETN
B5	GVI/LVDS/MIPI_TX8N	H5	VCCIO1
B6	GVI/LVDS/MIPI_TX9N	H6	VSS_29
B7	GPIO3_B2/GVI_LOCK	H7	GPIO1_A0/TEST_CLKO
B8	GPIO3_A3/VOP_VSYNC	H8	GPIO1_A1/SFC_CSLK
B9	GPIO3_A0/VOP_DEN	H9	HDMIRX_DVDD_1V1_1
B10	GPIO2_C3/VOP_D19/JTAGTDO	H10	VSS_18
B11	GPIO2_C0/VOP_D16/XIPSFCCSN	H11	HDMIRX_D2N
B12	GPIO2_B7/VOP_D15	H12	HDMIRX_D2P
C1	GVI/LVDS/MIPI_TX4N	J1	GPIO0_A3/I2S_LRCK_M0
C2	GVI/LVDS/MIPI_TX4P	J2	GPIO0_A2/I2S_SCK_M0
C3	GVI/LVDS/MIPI_PLL_AVDD_3V3	J3	INT/SPIBOOT
C4	VSS_26	J4	HDMITX_DVDD_1V1_2
C5	GVI/LVDS/MIPI_AVDD_1V1_3	J5	HDMITX_DVDD_1V1_3
C6	VSS_27	J6	HDMITX_DVDD_1V1_1
C7	I2C_ADDR	J7	PLL_AVDD_1V1
C8	GPIO2_C7/VOP_D23/JTAGTRSN	J8	EFUSE_VDD_2V5
C9	GPIO2_C6/VOP_D22/JTAGTCK	J9	HDMIRX_DVDD_1V1_2
C10	GPIO2_C2/VOP_D18/XIPSFCMOSI	J10	HDMIRX_AVDD_3V3_1
C11	GPIO2_B4/VOP_D12	J11	HDMIRX_D1N
C12	GPIO2_B6/VOP_D14	J12	HDMIRX_D1P
D1	GVI/LVDS/MIPI_TX3N	K1	GPIO0_B1/HDMITX_SDA
D2	GVI/LVDS/MIPI_TX3P	K2	GPIO0_A4/I2S_D0_M0/UARTTX
D3	VSS_5	K3	I2C_SDA
D4	GVI/LVDS/MIPI_AVDD_1V1_1	K4	HDMITX_AVDD_3V3
D5	GVI/LVDS/MIPI_AVDD_3V3_1	K5	VSS_7
D6	VSS_24	K6	VSS_22
D7	TEST	K7	VSS_10
D8	DVDD_2	K8	GPIO1_B0/HDMIRX_HPD_M0

Pin Number	Pin Name	Pin Number	Pin Name
D9	GPIO2_C5/VOP_D21/JTAGTMS	K9	GPIO1_B3/HDMIRX_CEC_M0
D10	GPIO2_B2/VOP_D10	K10	VSS_23
D11	GPIO2_B3/VOP_D11	K11	HDMIRX_D0N
D12	GPIO2_B5/VOP_D13	K12	HDMIRX_D0P
E1	GVI/LVDS/MIPI_TX2N	L1	GPIO0_B2/HDMITX_SCL
E2	GVI/LVDS/MIPI_TX2P	L2	GPIO0_B0/HDMITX_HPD
E3	GVI/LVDS/MIPI_AVDD_1V1_2	L3	I2C_SCL
E4	GVI/LVDS/MIPI_AVDD_3V3_2	L4	HDMITX_CLKN
E5	VSS_11	L5	HDMITX_D0N
E6	VSS_14	L6	HDMITX_D1N
E7	VSS_28	L7	HDMITX_D2N
E8	VCCIO2_1	L8	GPIO1_B2/HDMIRX_SCL_M0
E9	DVDD_1	L9	OSC_OUT
E10	GPIO2_A7/VOP_D7	L10	VSS_28
E11	GPIO2_B1/VOP_D9	L11	HDMIRX_CLKN
E12	GPIO2_B0/VOP_D8	L12	HDMIRX_CLKP
F1	GVI/LVDS/MIPI_TX1N	M1	VSS_4
F2	GVI/LVDS/MIPI_TX1P	M2	GPIO0_B3/HDMITX_CEC
F3	GVI/LVDS/MIPI_AVDD_1V1_4	M3	HDMITX_EXTR
F4	VSS_6	M4	HDMITX_CLKP
F5	VSS_8	M5	HDMITX_D0P
F6	VSS_12	M6	HDMITX_D1P
F7	VSS_15	M7	HDMITX_D2P
F8	VCCIO2_2	M8	GPIO1_B1/HDMIRX_SDA_M0
F9	GPIO2_A3/VOP_D3	M9	OSC_IN
F10	GPIO2_A6/VOP_D6	M10	PLL_AVDD
F11	GPIO2_A5/VOP_D5	M11	VSS_29
F12	GPIO2_A4/VOP_D4	M12	VSS_3

## 2.6 TFBGA144 Ball Map

144	1	2	3	4	5	6	7	8	9	10	11	12
A	VSS_1	GVILVDSMIPL_TX 5P	GVILVDSMIPL_TX 6P	GVILVDSMIPL_TX 7P	GVILVDSMIPL_TX 8P	GVILVDSMIPL_TX 9P	GPIO3_B1/GVL_H PD	GPIO3_A1/VOP_H SYNC	VOP_DCLK	GPIO2_C4/VOP_D 20/UART_RX_M0/ TAG_TDI	GPIO2_C1/VOP_D 17/XIPSPFC_MISO	VSS_2
B	GVILVDSMIPL_RE XT	GVILVDSMIPL_TX 5N	GVILVDSMIPL_TX 6N	GVILVDSMIPL_TX 7N	GVILVDSMIPL_TX 8N	GVILVDSMIPL_TX 9N	GPIO3_B2/GVL_LO CK	GPIO3_A3/VOP_V SYNC	GPIO3_A0/VOP_D EN	GPIO2_C3/VOP_D 19/UART_TX_M0/ TAG_TDO	GPIO2_C0/VOP_D 16/XIPSPFC_CSN	GPIO2_B7/VOP_D 15
C	GVILVDSMIPL_TX 4N	GVILVDSMIPL_TX 4P	GVILVDSMIPL_PL L_AVDD_3V3	VSS_26	GVILVDSMIPL_AV DD_1V1_3	VSS_27	I2C_ADDR	GPIO2_C7/VOP_D 23/UART_TRSTN	GPIO2_C6/VOP_D 22/UART_RTSN_ M0/UART_TCK	GPIO2_C2/VOP_D 18/XIPSPFC_MOSI	GPIO2_B4/VOP_D 12	GPIO2_B6/VOP_D 14
D	GVILVDSMIPL_TX 3N	GVILVDSMIPL_TX 3P	VSS_5	GVILVDSMIPL_AV DD_1V1_1	GVILVDSMIPL_AV DD_3V3_1	VSS_24	TEST	DVDD_2	GPIO2_C5/VOP_D 21/UART_CTSN_ M0/UART_TMS	GPIO2_B2/VOP_D 10	GPIO2_B3/VOP_D 11	GPIO2_B5/VOP_D 13
E	GVILVDSMIPL_TX 2N	GVILVDSMIPL_TX 2P	GVILVDSMIPL_AV DD_1V1_2	GVILVDSMIPL_AV DD_3V3_2	VSS_11	VSS_14	VSS_21	VCCIO2_1	DVDD_1	GPIO2_A7/VOP_D 7	GPIO2_B1/VOP_D 9	GPIO2_B0/VOP_D 8
F	GVILVDSMIPL_TX 1N	GVILVDSMIPL_TX 1P	GVILVDSMIPL_AV DD_1V1_4	VSS_6	VSS_8	VSS_12	VSS_15	VCCIO2_2	GPIO2_A3/VOP_D 3	GPIO2_A6/VOP_D 6	GPIO2_A5/VOP_D 5	GPIO2_A4/VOP_D 4
G	GVILVDSMIPL_TX 0N	GVILVDSMIPL_TX 0P	VSS_25	VSS_19	VSS_9	VSS_13	VSS_16	VSS_20	HDMIRX_EXTR	GPIO2_A0/VOP_D 0	GPIO2_A1/VOP_D 1	GPIO2_A2/VOP_D 2
H	GPIO0_A7/I2S_D3 _M0/UART_RTSN_ _M1	GPIO0_A6/I2S_D2 _M0/UART_CTSN_ _M1	GPIO0_A5/I2S_D1 _M0/UART_RX_M 1	RSETN	VCCIO1	VSS_17	GPIO1_A0/TEST_ CLKO	GPIO1_A1/XIPSPFC_ CSLK	HDMIRX_DVDD_1 V1_1	VSS_18	HDMIRX_D2N	HDMIRX_D2P
J	GPIO0_A3/I2S_LR CK_M0	GPIO0_A2/I2S_SC K_M0	GPIO0_B4/INT/SP I_BOOT	HDMITX_DVDD_1 V1_2	HDMITX_DVDD_1 V1_3	HDMITX_DVDD_1 V1_1	PLL_AVDD_1V1	EFUSE_VDD_2V5	HDMIRX_DVDD_1 V1_2	HDMIRX_AVDD_3 V3_1	HDMIRX_D1N	HDMIRX_D1P
K	GPIO0_B1/HDMIT X_SDA	GPIO0_A4/I2S_D0 _M0/UART_TX_M1	GPIO1_B5/I2CS_S _DAI2CM_SDA	HDMITX_AVDD_3 V3	VSS_7	VSS_22	VSS_10	GPIO1_B0/HDMIR X_HPD_M0	GPIO1_B3/HDMIR X_CEC_M0	VSS_23	HDMIRX_D0N	HDMIRX_D0P
L	GPIO0_B2/HDMIT X_SCL	GPIO0_B0/HDMIT X_HPD	GPIO1_B4/I2CS_S _CL/I2CM_SCL	HDMITX_CLKN	HDMITX_D0N	HDMITX_D1N	HDMITX_D2N	GPIO1_B2/HDMIR X_SCL_M0	OSC_OUT	VSS_28	HDMIRX_CLKN	HDMIRX_CLKP
M	VSS_4	GPIO0_B3/HDMIT X_CEC	HDMITX_EXTR	HDMITX_CLKP	HDMITX_D0P	HDMITX_D1P	HDMITX_D2P	GPIO1_B1/HDMIR X_SDA_M0	OSC_IN	PLL_AVDD	VSS_29	VSS_3

Fig. 2-6 RK628E BGA144 Ball Map

## 2.7 Pin Description

In this chapter, the pin description will be divided into two parts, one is all power/ground descriptions in Table 2-2 for BGA144, include analog power/ground; another is all the function signals descriptions in Table 2-2, also include analog function signals.

## 2.8 RK628E Power/Ground IO Description

Table 2-2 RK628E Power/Ground IO Information for BGA628

Group	Ball#	Descriptions
VSS	A1,A12, C4,C6,D3,D6, E5,E6,E7, F4,F5,F6,F7, G3,G4,G5,G6,G7,G8 H6, H10, K5,K6,K7,K10, M1,M12	Ground
DVDD	D8,E9	Digital 1.1v power
VCCIO1	H5	IO1 3.3v power
VCCIO2	E8,F8	IO2 3.3v power

Group	Ball#	Descriptions
PLL_AVDD	M10	PLL analog 3.3v power
PLL_AVDD_1V1	J7	PLL analog 1.1v power
EFUSE_VDD_2V5	J8	EFUSE 2.5v power
GVI/LVDS/MIPI_PLL_AVDD_3V3	C3	TX PHY PLL Power
GVI/LVDS/MIPI_AVDD_3V3	D5,E4	TX PHY 3.3v Power
GVI/LVDS/MIPI_AVDD_1V1	C5,D4,E3,F3	TX PHY 1.1v Power
HDMITX_DVDD_1V1	J4,J5,J6	HDMI TX digital 1.1v power
HDMITX_AVDD_3V3	K4	HDMI TX analog 3.3v power
HDMIRX_DVDD_1V1	H9,J9	HDMI RX PHY 1.1v power
HDMIRX_AVDD_3V3	J10	HDMI RX PHY 3.3v power

## 2.9 RK628E Function IO Description

Table 2-3 RK628E Function IO Description

Pad#	Ball#	func1	func2	func3	Pad Type <sup>o</sup>	Drive Strength <sup>o</sup>	Pull	Reset State <sup>o</sup>	Power Supply
OSC_IN	M9				H	2	NA	I	
OSC_OUT	L9				H	2	NA	O	
RESETN	H4				B	2	Up	I	
TEST	D7				B	2	down	I	
I2C_ADDR	C7				B	4	down	I	
I2C_SCL	L3				G	4	up	I	
I2C_SDA	K3				G	4	up	I	
INT	J3				B	2	down	I	
GPIO0_A2/I2S_SCK_M0	J2	I2S_SCK_M0			D	12	down	I	
GPIO0_A3/I2S_LRCK_M0	J1	I2S_LRCK_M0			B	12	down	I	
GPIO0_A4/I2S_D0_M0/UA_RTTX	K2	I2S_D0_M0			B	12	down	I	
GPIO0_A5/I2S_D1_M0/UA_RTRX	H3	I2S_D1_M0			B	12	down	I	
GPIO0_A6/I2S_D2_M0/UA_RTCTSN	H2	I2S_D2_M0			B	12	down	I	
GPIO0_A7/I2S_D3_M0/UA_RTRTSN	H1	I2S_D3_M0			B	12	down	I	
GPIO0_B0/HDMITX_HPD	L2	HDMITX_HPD			E	4	down	I	
GPIO0_B1/HDMITX_SDA	K1	HDMITX_SDA			G	4	up	I	
GPIO0_B2/HDMITX_SCL	L1	HDMITX_SCL			G	4	up	I	
GPIO0_B3/HDMITX_CEC	M2	HDMITX_CEC			G	4	up	I	
GPIO1_A0/TEST_CLKO	H7	TEST_CLKO			B	4	down	I	
GPIO1_A1/SFC_CLK	H8	SFC_CLK			B	4	down	I	
GPIO1_B0/HDMIRX_HPD_M0	K8	HDMIRX_HPD_M0			F	4	up	I	
GPIO1_B1/HDMIRX_SDA_M0	M8	HDMIRX_SDA_M0			G	4	up	I	
GPIO1_B2/HDMIRX_SCL_M0	L8	HDMIRX_SCL_M0			G	4	up	I	
GPIO1_B3/HDMIRX_CEC_M0	K9	HDMIRX_CEC_M0			G	4	up	I	
GPIO2_A0/VOP_D0	G10	VOP_D0			I	12	down	I	GPIO
GPIO2_A1/VOP_D1	G11	VOP_D1			I	12	down	I	
GPIO2_A2/VOP_D2	G12	VOP_D2			I	12	down	I	
GPIO2_A3/VOP_D3	F9	VOP_D3			I	12	down	I	
GPIO2_A4/VOP_D4	F12	VOP_D4			I	12	down	I	
GPIO2_A5/VOP_D5	F11	VOP_D5			I	12	down	I	
GPIO2_A6/VOP_D6	F10	VOP_D6			I	12	down	I	
GPIO2_A7/VOP_D7	E10	VOP_D7			I	12	down	I	
GPIO2_B0/VOP_D8	E12	VOP_D8			I	12	down	I	
GPIO2_B1/VOP_D9	E11	VOP_D9			I	12	down	I	
GPIO2_B2/VOP_D10	D10	VOP_D10			I	12	down	I	

Pad#	Ball#	func1	func2	func3	Pad Type <sup>o</sup>	Drive Strength <sup>o</sup>	Pull	Reset State <sup>o</sup>	Power Supply
GPIO2_B3/VOP_D11	D11	VOP_D11			I	12	down	I	Power Supply
GPIO2_B4/VOP_D12	C11	VOP_D12			I	12	down	I	
GPIO2_B5/VOP_D13	D12	VOP_D13			I	12	down	I	
GPIO2_B6/VOP_D14	C12	VOP_D14			I	12	down	I	
GPIO2_B7/VOP_D15	B12	VOP_D15			I	12	down	I	
GPIO2_C0/VOP_D16/XIPS FCCSN	B11	VOP_D16			I	12	down	I	
GPIO2_C1/VOP_D17/XIPS FCMISO	A11	VOP_D17			I	12	down	I	
GPIO2_C2/VOP_D18/XIPS FCMOSI	C10	VOP_D18			I	12	down	I	
GPIO2_C3/VOP_D19/RISC VJTAGTDO	B10	VOP_D19			I	12	down	I	
GPIO2_C4/VOP_D20/RISC VJTAGTDI	A10	VOP_D20			I	12	down	I	
GPIO2_C5/VOP_D21/RISC VJTAGCTMS	D9	VOP_D21			I	12	down	I	
GPIO2_C6/VOP_D22/RISC VJTAGTCK	C9	VOP_D22			I	12	down	I	
GPIO2_C7/VOP_D23/RISC VJTAGRSTN	C8	VOP_D23			I	12	down	I	
VOP_DCLK	A9	VOP_DCLK			I	16	down	I	
GPIO3_A0/VOP_DEN	B9	VOP_DEN			I	12	down	I	
GPIO3_A1/VOP_HSYNC	A8	VOP_HSYNC			I	12	down	I	
GPIO3_A3/VOP_VSYNC	B8	VOP_VSYNC			I	12	down	I	
GPIO3_B1/GVI_HPD	A7	GVI_HPD			C	4	up	I	
GPIO3_B2/GVI_LOCK	B7	GVI_LOCK			C	4	up	I	
HDMIRX_EXTR	G9				A	NA	NA	NA	HDMI
HDMIRX_CLKN	L11				A	NA	NA	NA	
HDMIRX_CLKP	L12				A	NA	NA	NA	
HDMIRX_D0N	K11				A	NA	NA	NA	
HDMIRX_D0P	K12				A	NA	NA	NA	
HDMIRX_D1N	J11				A	NA	NA	NA	
HDMIRX_D1P	J12				A	NA	NA	NA	
HDMIRX_D2N	H11				A	NA	NA	NA	
HDMIRX_D2P	H12				A	NA	NA	NA	
HDMITX_CLKN	L4				A	NA	NA	NA	HDMITX
HDMITX_CLKP	M4				A	NA	NA	NA	
HDMITX_D0N	L5				A	NA	NA	NA	
HDMITX_D0P	M5				A	NA	NA	NA	
HDMITX_D1N	L6				A	NA	NA	NA	
HDMITX_D1P	M6				A	NA	NA	NA	
HDMITX_D2N	L7				A	NA	NA	NA	
HDMITX_D2P	M7				A	NA	NA	NA	
HDMITX_EXTR	M3				A	NA	NA	NA	
GVI/LVDS/MIPI_REXT	B1				A	NA	NA	NA	GVI/LVDS/MIPI_TX
GVI/LVDS/MIPI_TX0N	G1				A	NA	NA	NA	
GVI/LVDS/MIPI_TX0P	G2				A	NA	NA	NA	
GVI/LVDS/MIPI_TX1N	F1				A	NA	NA	NA	
GVI/LVDS/MIPI_TX1P	F2				A	NA	NA	NA	
GVI/LVDS/MIPI_TX2N	E1				A	NA	NA	NA	
GVI/LVDS/MIPI_TX2P	E2				A	NA	NA	NA	
GVI/LVDS/MIPI_TX3N	D1				A	NA	NA	NA	
GVI/LVDS/MIPI_TX3P	D2				A	NA	NA	NA	
GVI/LVDS/MIPI_TX4N	C1				A	NA	NA	NA	
GVI/LVDS/MIPI_TX4P	C2				A	NA	NA	NA	
GVI/LVDS/MIPI_TX5N	B2				A	NA	NA	NA	
GVI/LVDS/MIPI_TX5P	A2				A	NA	NA	NA	
GVI/LVDS/MIPI_TX6N	B3				A	NA	NA	NA	
GVI/LVDS/MIPI_TX6P	A3				A	NA	NA	NA	
GVI/LVDS/MIPI_TX7N	B4				A	NA	NA	NA	

Pad#	Ball#	func1	func2	func3	Pad Type <sup>①</sup>	Drive Strength <sup>②</sup>	Pull	Reset State <sup>③</sup>	Power Supply
GVI/LVDS/MIPI_TX7P	A4				A	NA	NA	NA	
GVI/LVDS/MIPI_TX8N	B5				A	NA	NA	NA	
GVI/LVDS/MIPI_TX8P	A5				A	NA	NA	NA	
GVI/LVDS/MIPI_TX9N	B6				A	NA	NA	NA	
GVI/LVDS/MIPI_TX9P	A6				A	NA	NA	NA	

Notes:

①: Pad types: I = input, O = output, I/O = input/output (bidirectional)

AP = Analog Power, AG = Analog Ground

DP = Digital Power, DG = Digital Ground

A = Analog

②: Output Drive Unit is mA, only Digital IO has drive value;

③: Reset state: I = input without any pull resistor, O = output without any pull resistor;

## 2.10 IO Pin Name Description

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 2-4 RK628E IO Function Description List

Interface	Pin Name	Direction	Description
MISC	XIN_OSC	I	Clock input of 24/27MHz crystal
	XOUT_OSC	O	Clock output of 24/27MHz crystal
	NPOR	I	Chip hardware reset

Interface	Pin Name	Direction	Description
GVI/LVDS/MIPI_TX	GVI/LVDS/MIPI_REXT	I	
	GVI/LVDS/MIPI_TXiN(i=0~9)	O	GVI/LVDS/MIPI Tx negative differential line driver data output
	GVI/LVDS/MIPI_TXiP(i=0~9)	O	GVI/LVDS/MIPI Tx positive differential line driver data output

Interface	Pin Name	Direction	Description
HDMI_RX	HDMIRX_EXTR	I	USIC DATA signal
	HDMIRX_CLKN	I	HDMI clk lane N
	HDMIRX_CLKP	I	HDMI clk lane P
	HDMIRX_D0N	I	HDMI data lane 0
	HDMIRX_D0P	I	HDMI data lane 0
	HDMIRX_D1N	I	HDMI data lane 1
	HDMIRX_D1P	I	HDMI data lane 1
	HDMIRX_D2N	I	HDMI data lane 2
	HDMIRX_D2P	I	HDMI data lane 2

Interface	Pin Name	Direction	Description
HDMI_TX	HDMITX_CLKN	O	HDMI negative TMDS differential line driver clock output.
	HDMITX_CLKP	O	HDMI positive TMDS differential line driver clock output.
	HDMITX_DiN(i=0~2)	O	HDMI negative TMDS differential line driver data output.

Interface	Pin Name	Direction	Description
	HDMITX_DiP(i=0~2)	O	HDMI positive TMDS differential line driver data output.
	HDMITX_EXTR	I	HDMI reference resistor

Interface	Pin Name	Direction	Description
VOP	VOP_DCLK	O	Parallel interface clock
	GPIO3_A0/VOP_DEN	O	Parallel interface data enable
	GPIO3_A1/VOP_HSYNC	O	Parallel interface HSYNC signal
	GPIO3_A3/VOP_VSYNC	O	Parallel interface VSYNC signal
	GPIO2_A0/VOP_D0 ~ GPIO2_B7/VOP_D15	O	Parallel interface data0~data15
	GPIO2_C0/VOP_D16/XIPSFCCSN ~ GPIO2_C7/VOP_D23/RISCVJTAGRTSN	O	Parallel interface data16~data23

Interface	Pin Name	Direction	Description
JTAG	GPIO2_C3/VOP_D19/RISCVJTAGTDO	O	JTAG TDO signal
	GPIO2_C4/VOP_D20/RISCVJTAGTDI	I	JTAG TDI signal
	GPIO2_C5/VOP_D21/RISCVJTAGTMS	I	JTAG TMS signal
	GPIO2_C6/VOP_D22/RISCVJTAGTCK	I	JTAG TCK signal
	GPIO2_C7/VOP_D23/RISCVJTAGRTSN	I	JTAG RTSN signal

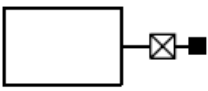
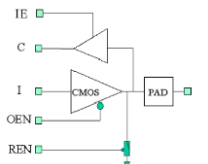
Interface	Pin Name	Direction	Description
SFC	GPIO1_A1/SFC_CSLK	O	SFC clock
	GPIO2_C0/VOP_D16/XIPSFCCSN	O	SFC chip select
	GPIO2_C1/VOP_D17/XIPSFCMISO	I/O	SFC data master in slave out
	GPIO2_C2/VOP_D18/XIPSFCMOSI	I/O	SFC data master out slave in

Interface	Pin Name	Direction	Description
UART	GPIO0_A4/I2S_D0_M0/UARTRX	O	UART tx signal
	GPIO0_A5/I2S_D1_M0/UARTRX	I	UART rx signal
	GPIO0_A6/I2S_D2_M0/UARTCTSN	I	UART cstn signal
	GPIO0_A7/I2S_D3_M0/UARTTRTSN	O	UART rtsn signal

## 2.11 RK628E IO Type

The following list shows IO type except Analog IO and all of Power/Ground IO.

Table 2-5 RK628E IO Type List

Type	Diagram	Description	Pin Name
A		Analog IO Cell with IO Voltage	EFUSE
B		3-state output pad with enable controlled input and enable controlled pull-down	GPIO0_A3/I2S_LRCK_M0

Type	Diagram	Description	Pin Name
C		3-state output pad with enable controlled Schmitt trigger input and pull-down	GPIO0_A2/I2S_SCK_M0
D		3-state output pad with enable controlled input and enable controlled pull-up	GPIO3_B1/GVI_HPD
E		3-state bi-direction I/O pads with controlled driving strength of low level, slew rate and uncontrolled pull-down resistor	GPIO0_B0/HDMITX_HPD
F		3-state bi-direction I/O pads with controlled driving strength of low level, slew rate and uncontrolled pull-up resistor	GPIO0_B1/HDMITX_SDA
G		3-state bi-direction I/O pads with controlled driving strength of low level, slew rate and uncontrolled Schmitt trigger, pull-up resistor	GPIO1_B0/HDMIRX_HPD_M0
H		CRYSTAL OSCILLATOR WITH INTERNAL RESISTOR	OSC_IN OSC_OUT
I		3-state bi-direction I/O pads with programmable drive-strength, controlled input enable, Schmitt trigger and pull-up / pull-down resistor	GPIO2_A0/VOP_D0

## Chapter 3 Electrical Specification

### 3.1 Absolute Maximum Ratings

Table 3-1 RK628E Absolute Maximum Ratings

Parameters	Related Power Group	Max	Unit
DC supply voltage for internal digital logic@1.1v	DVDD_1,DVDD_2	1.32	V
DC supply voltage for digital GPIO@1.8V mode	VCCIO2_1 VCCIO2_2	1.98 1.98	V
DC supply voltage for digital GPIO@3.3V mode	VCCIO1 VCCIO2_1 VCCIO2_2	3.63 3.63 3.63	V
DC supply voltage for HDMI RX	HDMIRX_AVDD_3V3 HDMIRX_DVDD_1V1	3.63 1.32	V
DC supply voltage for GVI/LVDS/MIPI TX	GVI/LVDS/MIPI_PLL_AVDD_3V3 GVI/LVDS/MIPI_AVDD_3V3 GVI/LVDS/MIPI_AVDD_1V1	3.63 3.63 1.32	V
DC supply voltage for HDMI TX	HDMITX_DVDD_1V1 HDMITX_AVDD_3V3	1.32 3.63	V
DC supply voltage for PLL	PLL_AVDD_1V1 PLL_AVDD_3V3	1.32 3.63	V
Storage Temperature	Tstg	125	°C
Max Conjunction Temperature	Tj	125	°C

Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

### 3.2 Recommended Operating Condition

The following table describes the recommended operating condition.

Table 3-2 RK628E Recommended Operating Condition

Parameters	Symbol	Min	Typ	Max	Unit
DC supply voltage for internal digital logic@1.1v	DVDD_1,DVDD_2	0.99	1.1	1.21	V
DC supply voltage for digital GPIO@1.8V mode	VCCIO2_1 VCCIO2_2	1.71 1.71	1.8 1.8	1.89 1.89	V
DC supply voltage for digital GPIO@3.3V mode	VCCIO1 VCCIO2_1 VCCIO2_2	3.135 3.135 3.135	3.3 3.3 3.3	3.465 3.465 3.465	V
DC supply voltage for HDMI RX	HDMIRX_AVDD_3V3 HDMIRX_DVDD_1V1	3.135 0.99	3.3 1.1	3.465 1.21	V
DC supply voltage for GVI/LVDS/MIPI TX	GVI/LVDS/MIPI_PLL_AVDD_3V3 GVI/LVDS/MIPI_AVDD_3V3 GVI/LVDS/MIPI_AVDD_1V1	3.135 3.135 0.99	3.3 3.3 1.1	3.465 3.465 1.21	V
DC supply voltage for HDMI TX	HDMITX_AVDD_3V3 HDMITX_DVDD_1V1	3.135 0.99	3.3 1.1	3.465 1.21	V
DC supply voltage for PLL	PLL_AVDD_3V3 PLL_AVDD_1V1	3.135 0.99	3.3 1.1	3.465 1.21	V
PLL input clock frequency		N/A	24	N/A	MHz
Operating Temperature		-20	25	80	°C

### 3.3 DC Characteristics

Table 3-3 RK628E DC Characteristics

Parameters	Symbol	Min	Typ	Max	Units	
Digital GPIO @3.3V for GPIO0/1/2/3	Input Low Voltage	Vil	-0.3	NA	0.8	V
	Input High Voltage	Vih	2.0	NA	3.465	V
	Output Low Voltage	Vol	NA	NA	0.4	V
	Output High Voltage	Voh	2.4	NA	NA	V
	Threshold Point	Vtr+	1	1.16	1.34	V

Parameters		Symbol	Min	Typ	Max	Units
		Vtr-	1.02	1.19	1.39	V
	Pullup Resistor	Rpu	26	46	71	Kohm
	Pulldown Resistor	Rpd	27	48	102	Kohm
Digital GPIO @1.8V for GPIO0/1/2/3	Input Low Voltage	Vil	-0.3	NA	0.58	V
	Input High Voltage	Vih	1.27	NA	3.15	V
	Output Low Voltage	Vol	NA	NA	0.45	V
	Output High Voltage	Voh	1.40	NA	NA	V
	Threshold Point	Vtr+	0.9	0.95	1.01	V
		Vtr-	0.91	0.97	1.03	V
	Pullup Resistor	Rpu	33	58	88	Kohm
Pulldown Resistor	Rpd	34	60	93	Kohm	

### 3.4 Recommended Operating Frequency

Table 3-4 RK628E Recommended Operating Frequency

Parameter	Condition	Symbol	Min	Typ	Max	Unit
CPLL	0.9V , 25 °C	cppll				MHz
	0.99V , -40 °C					
	0.81V , 125 °C				1600	
GPLL	0.9V , 25 °C	gppll				MHz
	0.99V , -40 °C					
	0.81V , 125 °C				1600	
HDMI RX CTRL	0.9V , 25 °C	dclk_rx				MHz
	0.99V , -40 °C					
	0.81V , 125 °C				375	
Process	0.9V , 25 °C	Sclk				MHz
	0.99V , -40 °C					
	0.81V , 125 °C				600	