Rockchip RK630 Datasheet

Revision History

Date	Revision	Description
2022-03-10	1.1	Update order information
2021-10-15	1.0	Initial released

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Chapter 1 Introduction

1.1 Overview

RK630 is a low cost affinity chip which is integrated a lot of analog IPs. It can work together with an AP which does not have following interfaces but want to use them:

- CVBS out
- ACODEC
- EPHY(MAC PHY)
- 5V IO
- RTC

RK630 can be configured by I2C slave interface or SPI slave interface, which is selected by an input IO. It also provides a 1.1v voltage output by a LDO inside the chip. Several 5V compatible IOs are integrated which can support HDMI 5V function and provide 3.3V IO interface with AP.

1.2 Features

The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

1.2.1 CVBS Encoder

- BT656 decoder
  - Support for interlace output
- TV interface
  - TV encoder 10bit out for DAC
  - Up sample to 108M
- Resolution
  - PAL/NTSC

1.2.2 Audio CODEC

- 24 bit DAC with 95dB SNR
- Support DC-coupled capless headphone output
- Support 16Ω to 32Ω headphone output and speaker output
- 24 bit ADC with 92dB SNR
- Support single-ended and differential microphone input and line input
- Automatic Level Control (ALC) for smooth audio recording
- Support Mono, Stereo, 5.1 and 7.1 HiFi channel performance
- Programmable input and output analog gains
- Digital interpolation and decimation filter integrated
- Sampling rate of 8/12/16/24/ 32/44.1/48/96kHz
- 3.3V supply for analog and 1.1V supply for digital
- Optional fractional PLL available that support 6MHz to 20MHz clock input to any clock

1.2.3 EPHY(MAC PHY)

- Fully IEEE 802.3 10/100 Base-TX compliant and supports EEE
- Capable to support length up to 120m in 100Base-TX for UTP CAT 5 cables
- Integrated MDI termination resistors
- Auto negotiation and parallel detection capability for automatic speed and duplex selection
- Supports MII and RMII interfaces
- Auto polarity correction in 10Base-T
- Design for Testability with extensive testability feature and 95% fault coverage
- Supports Auto-MDIX function for Plug-n-Play
- Programmable loopback mode for diagnostic
- Supports programmable LED output for different applications and power on LED Self-Test
- Supports 24M/25M/27M REFCLK clock sources
- Supports WOL (Wake-On-Lan) functionality

1.2.4 Video DAC

- 10-bit resolution

- Single channel
- Up to 300Msps throughput rate
- Programmable current output: 14.7mA~34.8mA with 64 adjustable steps
- Current consumption: 1mA @Iout = 14.7mA, 39mA @Iout = 34.8mA
- 57dBc SFDR @Iout = 14.7, fclk = 300MHz and fout = 5MHz;45dBc SFDR @Iout = 34.8, fclk = 300MHz and fout = 5MHz;
- Clock frequency: 27MHz to 300MHz
- Cable connection detection
- Build-in bandgap reference
- 1.8V supply for analog and 1.0V supply for digital

1.2.5 LDO

- Support 1.1V output and 3.3V input

1.2.6 5V IO

- Support 5V compliant IO, which use 3.3V power
- 5V Pull-up outside the chip

1.2.7 EFUSE

- One-time programmable nonvolatile EFUSE storage cells organized as 64x8 bit
- 1-bit can be programmed each time in program mode
- 8-bit can be read at on time in read mode

1.2.8 RTC

- Support 32.768kHz clock output
- Provides year, month, day, weekday, hours, minutes and seconds based on a 32.768kHz crystal oscillator
- Support 12 hour mode and 24 hour mode
- BCD coding of time, calendar, and alarm
- Support battery voltage detect
- Supper low power
- Support masked interrupt such as alarm interrupt, periodic interrupt, chip power-off interrupt, and battery power low interrupt

1.2.9 Others

- Package Type: QFN (body:6mm x 6mm ; 56pin)

1.3 Block Diagram

The following diagram shows the basic block diagram for RK630

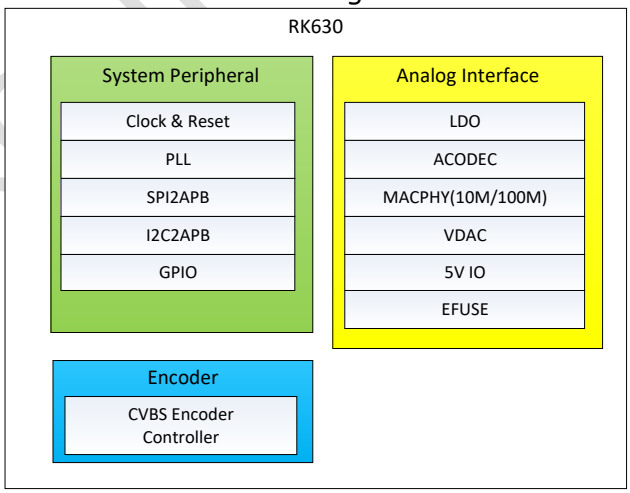


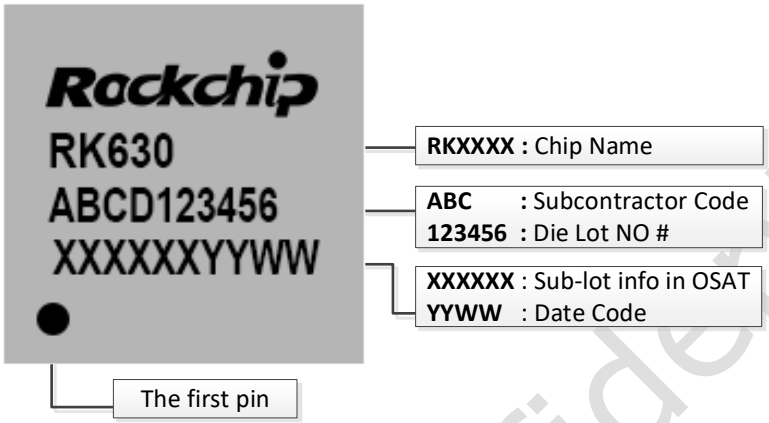
Fig. 1-1 RK630 Block Diagram

Chapter 2 Package Information

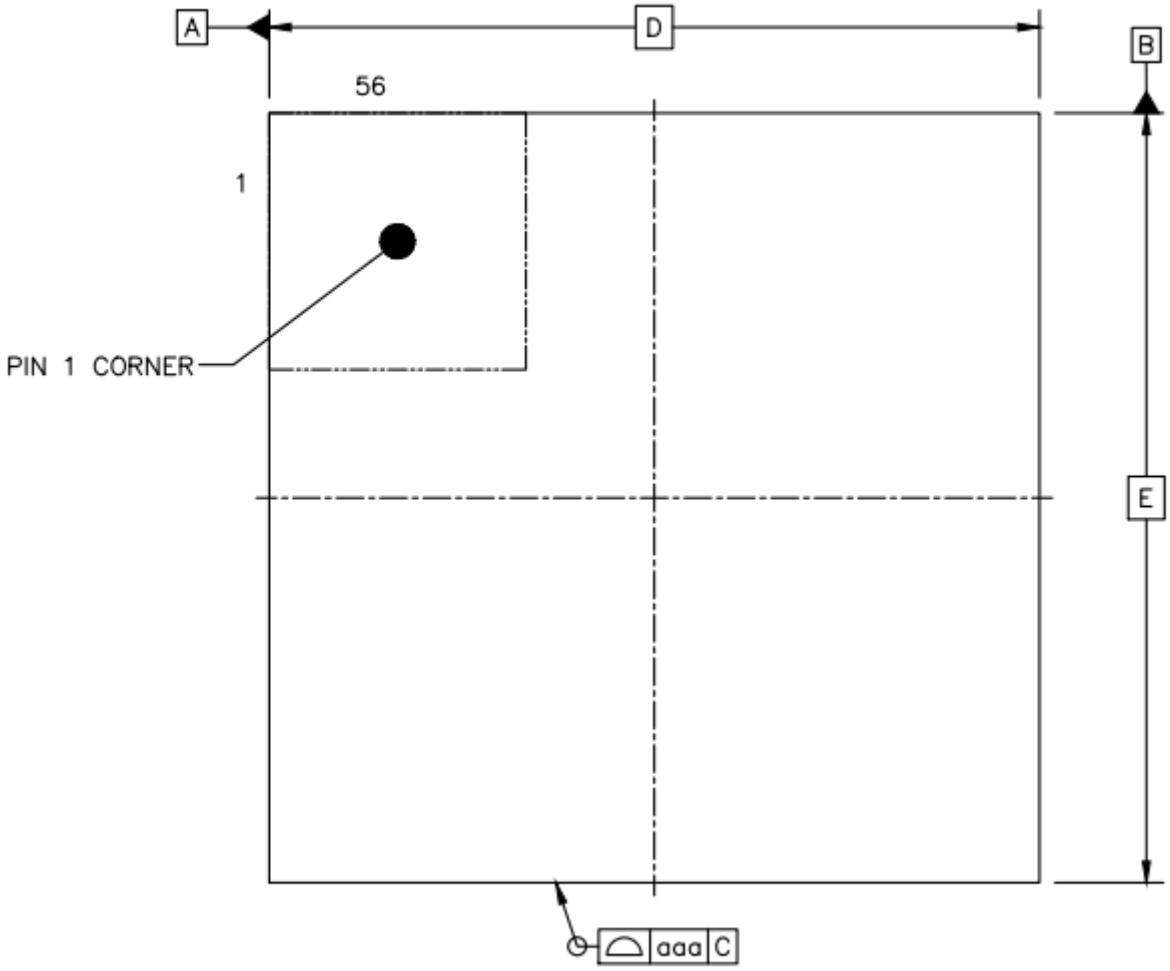
2.1 Order Information

Orderable Device	RoHS status	Package	Package Qty	Device Feature
RK630	RoHS	QFN6X6	3000 by reel	Digital Analog Mix IC with Audio and EPHY

2.2 Top Marking



2.3 Package Dimension



TOP VIEW

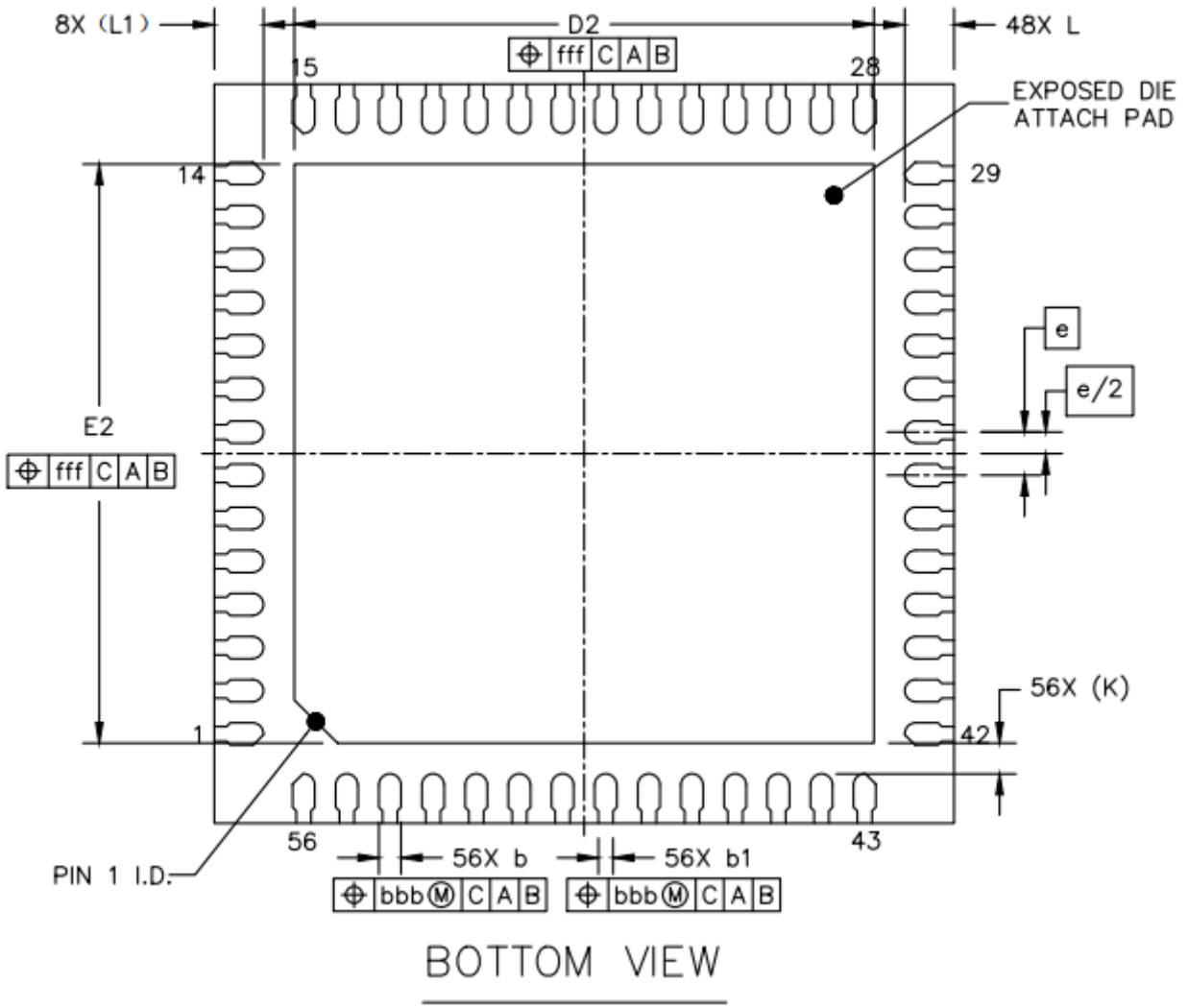


Fig. 2-1 RK630 Package Top View and bottom view

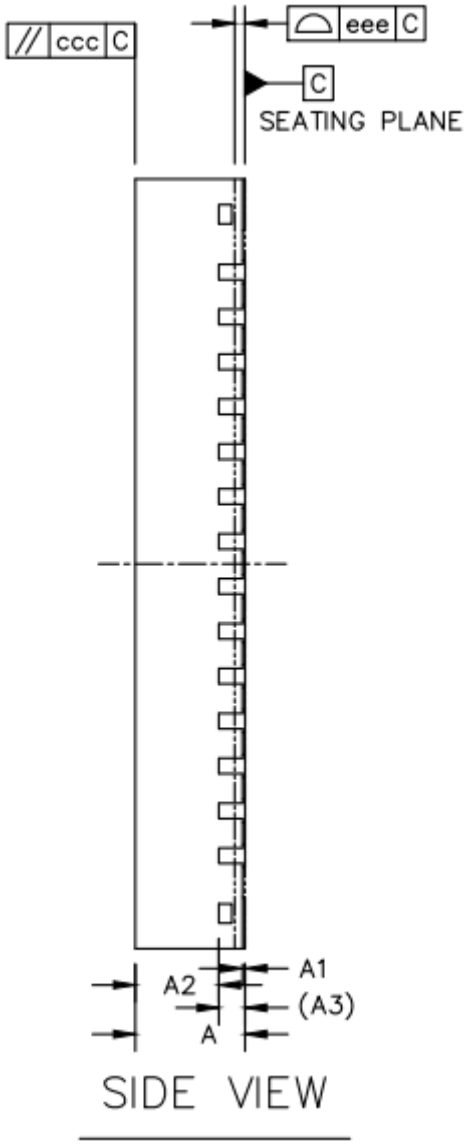


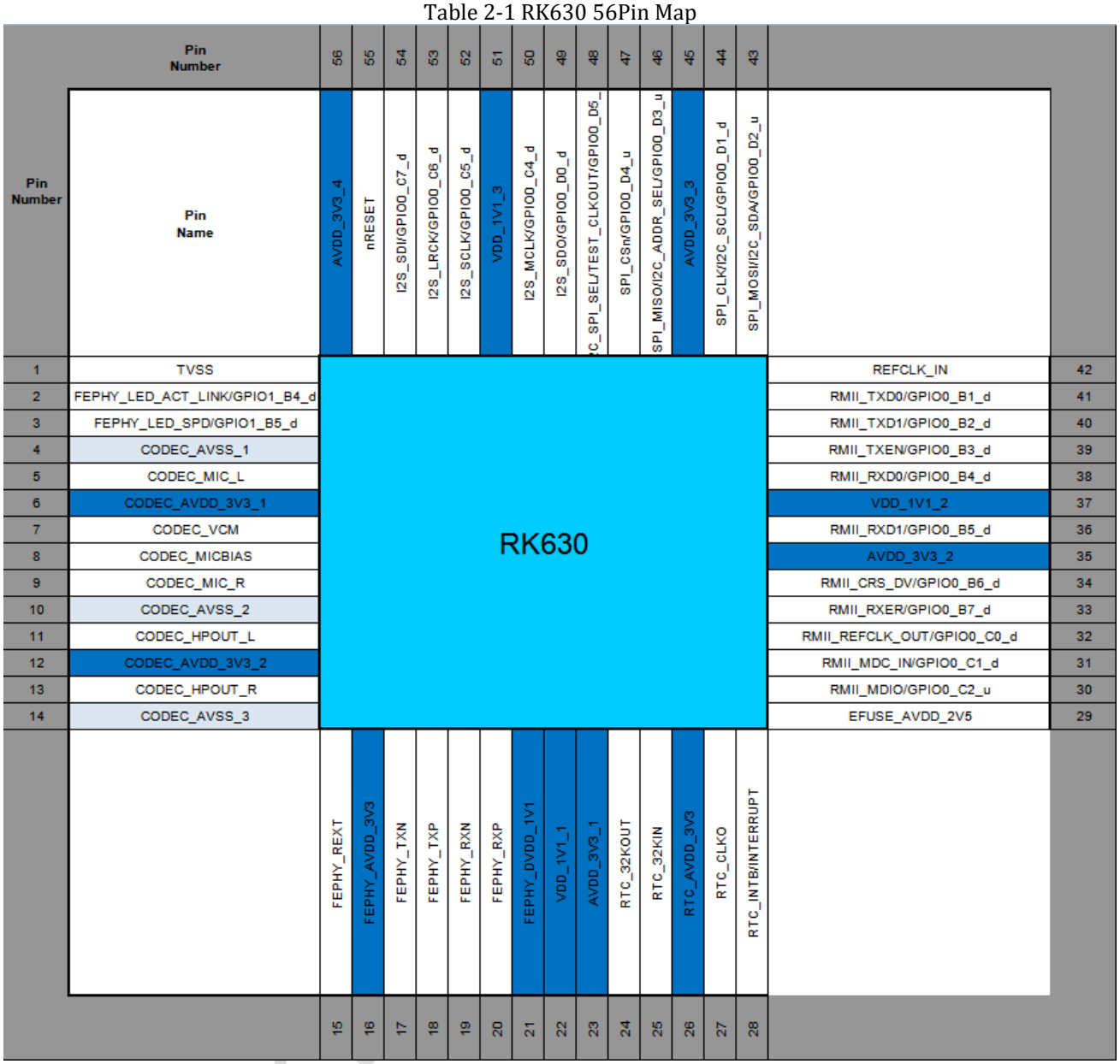
Fig. 2-2 RK630 Package Side View

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.13	0.18	0.23
		b1	0.07	0.12	0.17
BODY SIZE	X	D		6 BSC	
	Y	E		6 BSC	
LEAD PITCH		e		0.35 BSC	
EP SIZE	X	D2	4.65	4.7	4.75
	Y	E2	4.65	4.7	4.75
LEAD LENGTH		L	0.35	0.4	0.45
		L1		0.4 REF	
LEAD TIP TO EXPOSED PAD EDGE		K		0.25 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
EXPOSED PAD OFFSET		fff		0.1	

Fig. 2-3 RK630 Package Dimension

2.4 RK630 BALL MAP

Table 2-1 RK630 56Pin Map



2.5 Pin Number List

Table 2-2 RK630 Pin Number Order Information

Pin Name	Pin#
TVSS	1
FEPHY_LED_ACT_LINK/GPIO1_B4_D	2
FEPHY_LED_SPD/GPIO1_B5_D	3
CODEC_AVSS_1	4
CODEC_MIC_L	5
CODEC_AVDD_3V3_1	6
CODEC_VCM	7
CODEC_MICBIAS	8
CODEC_MIC_R	9
CODEC_AVSS_2	10
CODEC_HPOUT_L	11
CODEC_AVDD_3V3_2	12

Pin Name	Pin#
CODEC_HPOUT_R	13
CODEC_AVSS_3	14
FEPHY_REXT	15
FEPHY_AVDD_3V3	16
FEPHY_TXN	17
FEPHY_TXP	18
FEPHY_RXP	20
FEPHY_DVDD_1V1	21
VDD_1V1_1	22
AVDD_3V3_1	23
RTC_32KOUT	24
RTC_32KIN	25
RTC_AVDD_3V3	26
RTC_CLKO	27
RTC_INTB/INTERRUPT	28
EFUSE_AVDD_2V5	29
RMII_MDIO/GPIO0_C2_U	30
RMII_MDC_IN/GPIO0_C1_D	31
RMII_REFCLK_OUT/GPIO0_C0_D	32
RMII_RXER/GPIO0_B7_D	33
RMII_CRS_DV/GPIO0_B6_D	34
AVDD_3V3_2	35
RMII_RXD1/GPIO0_B5_D	36
VDD_1V1_2	37
RMII_RXD0/GPIO0_B4_D	38
RMII_TXEN/GPIO0_B3_D	39
RMII_TXD1/GPIO0_B2_D	40
RMII_TXD0/GPIO0_B1_D	41
REFCLK_IN	42
SPI_MOSI/I2C_SDA/GPIO0_D2_U	43
SPI_CLK/I2C_SCL/GPIO0_D1_D	44
AVDD_3V3_3	45
SPI_MISO/I2C_ADDR_SEL/GPIO0_D3_U	46
SPI_CSN/GPIO0_D4_U	47
I2C_SPI_SEL/TEST_CLKOUT/GPIO0_D5_D	48
I2S_SDO/GPIO0_D0_D	49
I2S_MCLK/GPIO0_C4_D	50
VDD_1V1_3	51
I2S_SCLK/GPIO0_C5_D	52
I2S_LRCK/GPIO0_C6_D	53
I2S_SDI/GPIO0_C7_D	54
nRESET	55
AVDD_3V3_4	56

2.6 RK630 Power/Ground IO Description

Table 2-3 RK630 Power/Ground IO information

Group	Ball#	Descriptions
VSS	E-PAD	Internal Core Ground Digital IO Ground
ACODEC_VDD_3V3	6,12	Codec Analog Power
ACODEC_VSS	4,10,14	Codec Analog Ground
MACPHY_VDD_3V3	16	MACPHY 3.3V Analog Power
MACPHY_VDD_1V1	21	MACPHY 1.1V Analog Power
LDO_VDD_3V3	23	LDO 3.3V Analog Power
VCCIO1_VDD_3V3	35	VCCIO1 Post VDD
VCCIO2_VDD_3V3	45,56	VCCIO2 Post VDD
VCCIO1_VDD_1V1	37	VCCIO1 Pre VDD
VCCIO2_VDD_1V1	51	VCCIO2 Pre VDD
EFUSE_AVDD_2V5	29	EFUSE 2.5V Analog Power
RTC_AVDD	26	RTC Analog Power(1.6V-5V)

2.7 RK630 Function IO Description

Table 2-4 RK630 Function IO description

Pin	Pin Name	Func1	Func2	Func3	Func4	Pad Type①	Def ③	Pull	Drive Strength ②	INT ④	DIE Power domain
41	GPIO0_B1/RMII_TXD0	GPIO0_B1	RMII_TXD0			I/O	I	down	4	√	VCCIO1
40	GPIO0_B2/RMII_TXD1	GPIO0_B2	RMII_TXD1			I/O	I	down	4	√	
39	GPIO0_B3/RMII_TXEN	GPIO0_B3	RMII_TXEN			I/O	I	down	4	√	
38	GPIO0_B4/RMII_RXD0	GPIO0_B4	RMII_RXD0			I/O	O	down	4	√	
36	GPIO0_B5/RMII_RXD1	GPIO0_B5	RMII_RXD1			I/O	O	down	4	√	
34	GPIO0_B6/RMII_CRSDV	GPIO0_B6	RMII_CRSDV			I/O	O	down	4	√	
33	GPIO0_B7/RMII_RXER	GPIO0_B7	RMII_RXER			I/O	O	down	4	√	
32	GPIO0_C0/RMII_REFCLKOUT	GPIO0_C0	RMII_REFCLKOUT			I/O	O	down	8	√	
31	GPIO0_C1/RMII_MDCIN	GPIO0_C1	RMII_MDCIN			I/O	I	up	4	√	
30	GPIO0_C2/RMII_MDIO	GPIO0_C2	RMII_MDIO			I/O	O	up	4	√	
42	REFCLK_IN	REFCLK_IN				I/O	I	down	4	√	
50	GPIO0_C4/I2S_MCLK	GPIO0_C4	I2S_MCLK			I/O	I	down	4	√	VCCIO2
52	GPIO0_C5/I2S_SCLK	GPIO0_C5	I2S_SCLK			I/O	I/O	down	4	√	
53	GPIO0_C6/I2S_LRCK	GPIO0_C6	I2S_LRCK			I/O	I/O	down	4	√	
54	GPIO0_C7/I2S_SDI	GPIO0_C7	I2S_SDI			I/O	I	down	4	√	
49	GPIO0_D0/I2S_SDO	GPIO0_D0	I2S_SDO			I/O	O	down	4	√	
44	GPIO0_D1/SPI_CLK/I2C_SCL	GPIO0_D1	SPI_CLK	I2C_SCL		I/O	I	up	4	√	
43	GPIO0_D2/SPI_MOSI/I2C_SDA	GPIO0_D2	SPI_MOSI	SPI_MOSI		I/O	I	up	4	√	
46	GPIO0_D3/SPI_MISO/I2C_ADDRSEL	GPIO0_D3	SPI_MISO	I2C_ADDRSEL		I/O	O	up	4	√	
47	GPIO0_D4/SPI_CSN	GPIO0_D4	SPI_CSN			I/O	I	up	4	√	
48	GPIO0_D5/TEST_CLKOUT/I2C_SPISEL	GPIO0_D5	TEST_CLKOUT	I2C_SPISEL	INTERRUPT_O	I/O	I/O	up	4	√	
55	NPOR	NPOR				I/O	I	up	2	√	
1	TEST	TEST				I/O	O	down	2	√	
25	RTC_32KIN					I		NA		√	RTC
24	RTC_32KOUT					O		NA		√	
28	RTC_INTB					O		up		√	
27	RTC_CLKO					O		NA		√	
5	CODEC_MICL					A		NA		√	CODEC
7	CODEC_VCM					A		NA		√	
8	CODEC_MICBIAS					A		NA		√	
9	CODEC_MICR					A		NA		√	
11	CODEC_VOUTL					A		NA		√	
13	CODEC_VOUTR					A		NA		√	
15	EPHY_RXN					A		NA		√	
16	EPHY_RXP					A		NA		√	
13	EPHY_TXN					A		NA		√	
14	EPHY_TXP					A		NA		√	
11	EPHY_RTX					A		NA		√	
17	LDO_VDD11					A		NA		√	LDO

Notes:
①:Type: I = input, O = output, I/O = input/output (bidirectional)
AP = Analog Power, AG = Analog Ground
DP = Digital Power, DG = Digital Ground
A = Analog
②:Output Drive Unit is mA, only Digital IO has drive value;
③:Def: I = input without any pull resistor, O = output without any pull resistor;
④:INT: interrupt

2.8 IO Pin Name Description

In this chapter, the pin description will be divided into two parts, one is all power/ground descriptions in Table 1-1, include analog power/ground; another is all the function signals descriptions in Table 1-2, also include analog power/ground.

2.8.1 IO Pin Name Description

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 2-5 RK630 IO function description list

Interface	Pin Name	Direction	Description
MISC	REFCLKIN	I	Reference clock input
	TEST	I	Test enable
	NPOR	I	Chip hardware reset

Interface	Pin Name	Direction	Description
BT656	BT656_Di(i=0~3)	I	BT656 data in
	BT656_CLKIN	I	BT656 clock

Interface	Pin Name	Direction	Description
I2C	I2C_SCL	I	I2C clock
	I2C_SDA	I	I2C data
	I2C_ADDRSEL	I	I2C Address select

Interface	Pin Name	Direction	Description
I2S Controller	I2S_SCLK	I/O	I2S serial clock
	I2S_MCLK	I	I2S clock source
	I2S_LRCK	I/O	I2S left & right channel signal for transmitting serial data, synchronous left & right channel in I2S mode
	I2S_SDO	O	I2S serial data output
	I2S_SDI	I	I2S serial data input

Interface	Pin Name	Direction	Description
SPI Controller	SPI_CLK	I/O	SPI serial clock
	SPI_CSN	I/O	SPI chip select signal ,low active
	SPI_MISO	O	SPI serial data input
	SPI_MOSI	I	SPI serial data output

Interface	Pin Name	Direction	Description
HDMI5V	HDMI_SDA3V3	I/O	SDA 3.3v
	HDMI_SDA5V	I/O	SDA 5v
	HDMI_SCL3V3	I/O	SCL 3.3v
	HDMI_SCL5V	I/O	SCL 5v
	HDMI_CEC3V3	I/O	CEC 3.3v

Interface	Pin Name	Direction	Description
	HDMI_CEC5V	I/O	CEC 5v
	HDMI_HPD3V3	O	HPD 3.3v
	HDMI_HPD5V	I	HPD 5v

Interface	Pin Name	Direction	Description
GMAC	GMAC_TXDi(i=0~1)	I	GMAC TX data
	GMAC_RXDi(i=0~1)	O	GMAC RX data
	GMAC_TXEN	I	GMAC TX data enable
	GMAC_RXDV	O	Collision and Data Valid
	GMAC_RXER	O	GMAC RX error signal
	GMAC_MDIO	I/O	GMAC management interface data
	GMAC_MDC	I	GMAC management interface clock
	GMAC_REFCLKOUT	O	RMII REC_CLK output or GMAC external clock input

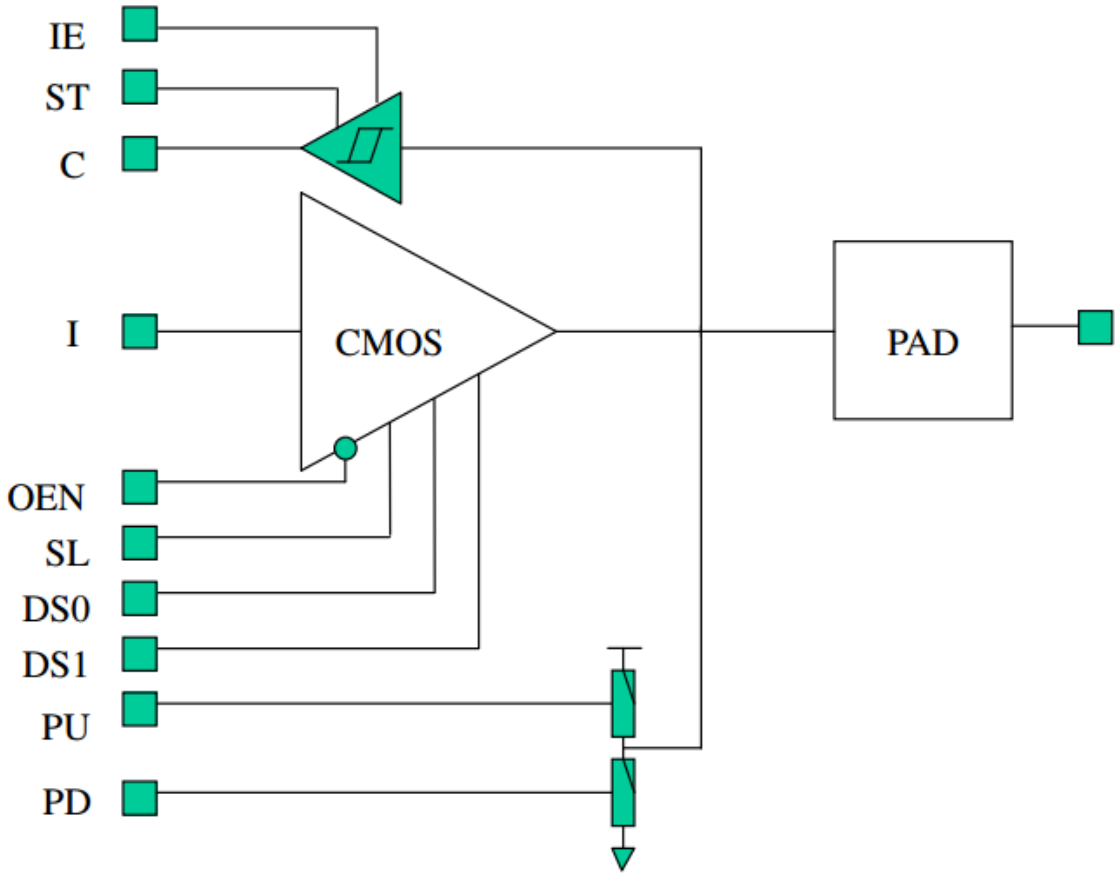
Interface	Pin Name	Direction	Description
EPHY	EPHY_ATBUSB	I/O	EPHY test point B
	EPHY_ATBUSA	I/O	EPHY test point A
	EPHY_RXN	I/O	Transceiver negative output/input
	EPHY_RXP	I/O	Transceiver positive output/input
	EPHY_TXN	I/O	Transceiver negative output/input
	EPHY_TXP	I/O	Transceiver positive output/input
	EPHY_RTX	I/O	External 6K-Ohm 1 resistor to ground

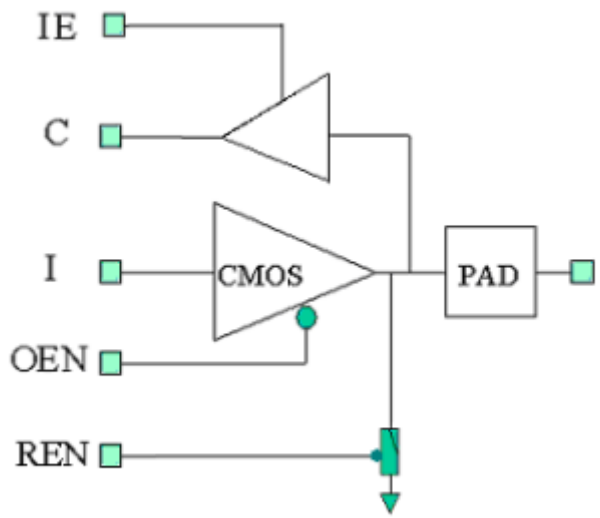
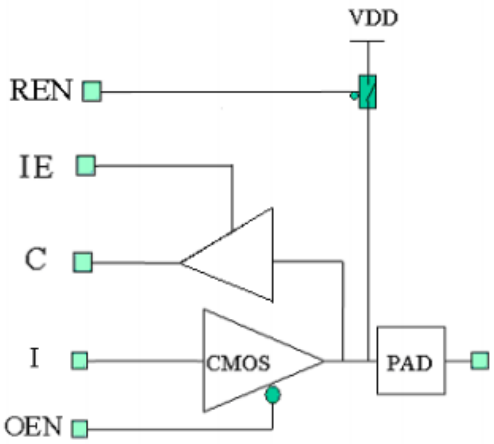
Interface	Pin Name	Direction	Description
CODEC	CODEC_MICL	I	Left channel Microphone input
	CODEC_MICR	I	Right channel Microphone input
	CODEC_LINEL	I	Left channel line input
	CODEC_LINER	I	Right channel line input
	CODEC_VCM	O	Reference voltage output
	CODEC_MICBIAS	O	Microphone bias output
	CODEC_VOUTL	O	Left channel headphone output
	CODEC_AOMS	I	Headphone virtual ground feedback
	CODEC_AOM	O	Headphone virtual ground output
	CODEC_VOUTR	O	Right channel headphone output
	CODEC_HPDET	I	Headphone jack detection input

2.8.2 IO Type

The following list shows IO type except DDR IO and all of Power/Ground IO.

Table 2-6 RK630 IO Type List

Type	Diagram	Description	Pin Name
A		Pad for 5V tolerance	hdmi_scl5v hdmi_sda5v hdmi_hpd5v hdmi_cec5v

Type	Diagram	Description	Pin Name
B		Tri-state output pad with input, which is always pull-down	Pad of digital GPIO
C		Tri-state output pad with input, which is always pull-up	Pad of digital GPIO

Chapter 3 Electrical Specification

3.1 Absolute Ratings

Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

Table 3-1 RK630 Absolute maximum ratings

Parameters	Related Power Group	Max	Unit
DC supply voltage for Internal digital logic	LOGIC_VDD	1.21	V
DC supply voltage for Digital GPIO	VCCIO0_VDD VCCIO1_VDD VCCIO2_VDD	3.63	V
DC supply voltage for Analog part of EFUSE	EFUSE	2.75	V
DC supply voltage for Analog part of RTC	RTC_AVDD	5.00	V
DC supply voltage for Analog part of VDAC	VDAC_AVDD_3V3	3.6	V
DC supply voltage for digital part of ACODEC	ACODEC_AVDD_1V1	1.21	V
DC supply voltage for Analog part of ACODEC	ACODEC_AVDD_3V3	3.63	V
DC supply voltage for digital part of EPHY	EPHY_AVDD_1V1	1.21	V
DC supply voltage for Analog part of EPHY	EPHY_AVDD_3V3	3.63	V
DC supply voltage for Analog part of LDO	LDO_AVDD_3V3	3.63	V
Storage Temperature		85	℃

3.2 Recommended Operating Condition

Following table describes the recommended operating condition.

Table 3-2 RK630 Recommended operating condition

Parameters	Symbol	Min	Typ	Max	Units
Internal digital logic Power	LOGIC_VDD	0.99	1.1	1.21	V
Digital GPIO Power(3.3V/2.5V/1.8V)	VCCIO0_VDD VCCIO1_VDD VCCIO23_VDD VCCIO4_VDD	3 2.25 1.62	3.3 2.5 1.8	3.6 2.75 1.98	V
EFUSE 2.5V Analog Power	EFUSE_AVDD_2V5	1.21	2.5	2.75	V
RTC Analog Power	RTC_AVDD	1.6	-	5.0	V
VDAC 3.3V Analog Power	VDAC_AVDD_3V3	3	3.3	3.63	V
ACODEC 1.1V Analog Power	ACODEC_AVDD_1V1	0.99	1.1	1.21	V
ACODEC 3.3V Analog Power	ACODEC_AVDD_3V3	3	3.3	3.63	V
EPHY Analog Power	EPHY_AVDD_1V1	0.99	1.1	1.21	V
Operating Temperature		-40	25	85	℃

3.3 DC Characteristics

Table 3-3 RK630 DC Characteristics

Parameters		Symbol	Min	Typ	Max	Units
Digital GPIO @3.3V	Input Low Voltage	Vil	-0.3	0	3.3x0.3	V
	Input High Voltage	Vih	3.3x0.7	3.3	3.3+0.3	V
	Output Low Voltage	Vol	-0.3	NA	NA	V
	Output High Voltage	Voh	NA	NA	3.6	V
	Pullup Resistor	Rpu	33.7	58	101.5	Kohm
	Pulldown Resistor	Rpd	34.2	60.1	109.3	Kohm
Digital GPIO @1.8V	Input Low Voltage	Vil	-0.3	0	1.8x0.3	V
	Input High Voltage	Vih	1.8x0.7	1.8	1.8 + 0.3	V
	Output Low Voltage	Vol	-0.3	NA	NA	V
	Output High Voltage	Voh	NA	NA	1.8+0.3	V
	Pullup Resistor	Rpu	35	62.9	120	Kohm
	Pulldown Resistor	Rpd	35.1	61	113.9	Kohm

Parameters		Symbol	Min	Typ	Max	Units
CODEC	Microphone Bias	Vmicb	0.5 * AVDD		0.85 * AVDD	V
		Imicb			3	mA
	Microphone Gain Boost PGA	Gbst	0		20	dB
		Cin		10		pF
	ALC PGA	Galc	-18		28.5	dB
	ADC	SNR		92		dB
		THD		-81		dB
	DAC	SNR		95		dB
		THD		-84		dB
	Output Driver	Gdrv	-39		6	dB
		Rout		1		Ω
		Cout		20		0pF
		PSRR		70		dB
	Line Output	SNR		93		1dB
		THD		-84		dB
	Headphone Output	SNR		92		D12B
		THD		-70		dB

3.4 Electrical Characteristics for General IO

Table 3-4 RK630 Electrical Characteristics for Digital General IO

Parameters		Symbol	Test condition	Min	Typ	Max	Units
Digital GPIO @3.3V	Input leakage current	Ii	Vin = 3.3V or 0V	NA	NA	10	uA
	Tri-state output leakage current	Ioz	Vout = 3.3V or 0V	NA	NA	10	uA
	High level input current	Iih	Vin = 3.3V, pulldown disabled	NA	NA	10	uA
			Vin = 3.3V, pulldown enabled	NA	NA	106.4	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	NA	NA	10	uA
			Vin = 0V, pullup enabled	NA	NA	107.8	uA
Digital GPIO @1.8V	Input leakage current	Ii	Vin = 1.8V or 0V	NA	NA	10	uA
	Tri-state output leakage current	Ioz	Vout = 1.8V or 0V	NA	NA	10	uA
	High level input current	Iih	Vin = 1.8V, pulldown disabled	NA	NA	10	uA
			Vin = 1.8V, pulldown enabled	NA	NA	61.3	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	NA	NA	10	uA
			Vin = 0V, pullup enabled	NA	NA	61.4	uA

3.5 Electrical Characteristics for EFUSE

Table 3-5 RK630 Electrical Characteristics for EFUSE

Parameters		Symbol	Test condition	Min	Typ	Max	Units
EFUSE	Read operating junction temperature	Tread		-40	25	125	℃
	Burn operating ambient temperature	Tburn		10	24	40	℃
	Standby current	Istandby			1		uA
	Peak burning current	Iprog			15		mA
	Current during normal reading	Iactive	10MHz		4		mA

3.6 Electrical Characteristics for ACODEC

Table 3-6 RK630 Electrical Characteristics for ACODEC

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Analog Supply	AVDD		1.62	1.8	1.98	V
Digital Supply	DVDD		0.9	1.0	1.1	V
Junction Temperature	Tj		-40		125	℃
Bias Voltage	VMICB		0.5 * AVDD		0.85 * AVDD	V
Bias Voltage	IMICB				3	mA
Programmable Gain	GBST		0		20	dB
Input Resistance	RIN	GBST=0dB		110		KΩ
		GBST=20dB		20		KΩ
Input Capacitance	CIN			10		pF
Programmable Gain	GALC		-18		28.5	dB
Signal to Noise Ratio	SNR	A-weighted		92		dB
Total Harmonic Distortion	THD	-3dBFS input		-81		dB
Programmable Gain	GDRV		-39		6	dB
Output Resistance	ROUT			1		Ω
Output Capacitance	COUT			20		pF
Power Supply Rejection	PSRR	1KHz		70		dB
Signal to Noise Ration	SNR	A-weighted		93		dB
Total Harmonic Distortion	THD	-3dBFS output 600Ω load		-80		dB

3.7 Electrical Characteristics for EPHY

Table 3-7 RK630 Electrical Characteristics for EPHY

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Analog 3.3V power supply	VDD33		3.0	3.3	3.6	V
Analog 1.1V power supply	VDD11		1.0	1.1	1.2	V
Operating Temperature	TOP		-40	25	125	℃
System clock frequency	Fsys			24/25/27		Mhz
System clock duty-cycle	Dsys		45		55	%
System clock TIE peak-to-peak jitter	Tsys_jit				0.15	ns
REFCLK clock period	T50		20-50	20	20+50	ppm
REFCLK clock high time	T50_high		7	10	13	ns
REFCLK clock jitter	T50_jit			0.15		
MII TX/RX clock perid	Tmiiclk			40/400		ns
TXEN and TXD setup to TXCLK falling edge	Ttxsu		10			ns
TXEN and TXD hold to TXCLK falling edge	Ttxhold		10			ns
RXCLK to RXDV and RXD[3:0] output delay	Trxdly		14	24	34	ns

3.8 Electrical Characteristics for VDAC

Table 3-8 RK630 Electrical Characteristics for VDAC

Parameters	Symbol	Test condition	Min	Typ	Max	Units
High Voltage Analog Supply	avddhv6.0		3.0	3.3	3.6	V
Digital Supply Voltage	dvdd		0.99	1.1	1.21	V

Parameters	Symbol	Test condition	Min	Typ	Max	Units
High Voltage Analog Current		Ifs=34mA		51		mA
Digital Current		Fs=300Mhz		0.7		mA
Junction Temperature			-40	50	125	℃
Bandgap Voltage	Vbg			1.21		V
Reference Resistor				1130		Ohm
Reference Current				1.07		mA
Resolution				10		bit
Output Full Scale Range					34	mA
Output Compliance Range				1.3		V
Full Scale Output Swing			0.56		1.3	V
Resistive Load				37.5		Ohm
Offset Error				±1		%FS
Gain Error				±2		%FS
Absolute Gain Error				±4		%FS
DNL		Ifs=34mA		±0.5		LSB
INL		Ifs=34mA		±1		LSB
Update Rate			1		300	MHz
Clock duty cycle			45		55	%
Setup Time	Tst		-0.4	0	1.6	ns
Hold Time	Th		0.9	1.1	1.6	ns
Propagation Delay	Tpd		0.7	1.1	1.8	ns
Startup Time				3	4	us
Cable sensing Cycle time				4.5		clk cycles

