Rockchip RK730 Datasheet

Revision 1.2
August 2025

Revision History

Date	Revision	Description
2024-11-18	1.0	Initial release
2025-8-4	1.1	1. remove AVDD/DVDD pin 2. Change the associated descriptions of Power Pin.
2025-8-8	1.2	Correct the description in SPLL-03 register

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Chapter 1 Introduction

1.1 Overview

The RK730 is a high performance, low-power audio CODEC. It consists of 2-channel ADC and 2-channel DAC, and microphone boost, microphone-bias, and headphone driver circuit to support normal CODEC functions. The headphone drivers can support maximum 100mW with 16ohm loading. Additionally, chip also support differential output mode. In this mode, the maximum HP drive output amplitude can reach 4.8Vpp in 3.3V power supply.

A wind reduction filter is built in on recording path. The filter can remove the wind noise and keep the recording quality.

I2C mode is support for signal connection. In this mode, the address of chip can be selected between 0X16/0X17 by tie low/high the CE Pin of chip.

1.2 Feature

ADC

- 24bit, 8KHz to 192KHz sampling frequency
- 100dB dynamic range, 100dB signal to noise ratio, -95dB THD+N Typical
- Two stereo or mono microphone interface with microphone amplifier. The maximum gain of microphone reaches +54dB.
- Various gain and analog input differential/pseudo-differential mode.

DAC

- 24bit, 8KHz to 192KHz sampling frequency.
- 100dB dynamic range, 98dB signal to noise ratio, -85dB THD+N
- 50mW headphone amplifier for 32ohm loading and 100mW for 16ohm loading , pop noise free.
- Support HP differential output mode. In this mode, the maxim output amplitude of HP can reach 4.8Vpp in 3.3V power supply.

Digital

- With HPF in analog-input and digital-input path.
- Support I2C interface, and the input signal modes include I2S/PCM.
- Internal PLL can receive wide range input clk.
- Zero detection and soft volume for pop noise suppression

1.3 Block Diagram

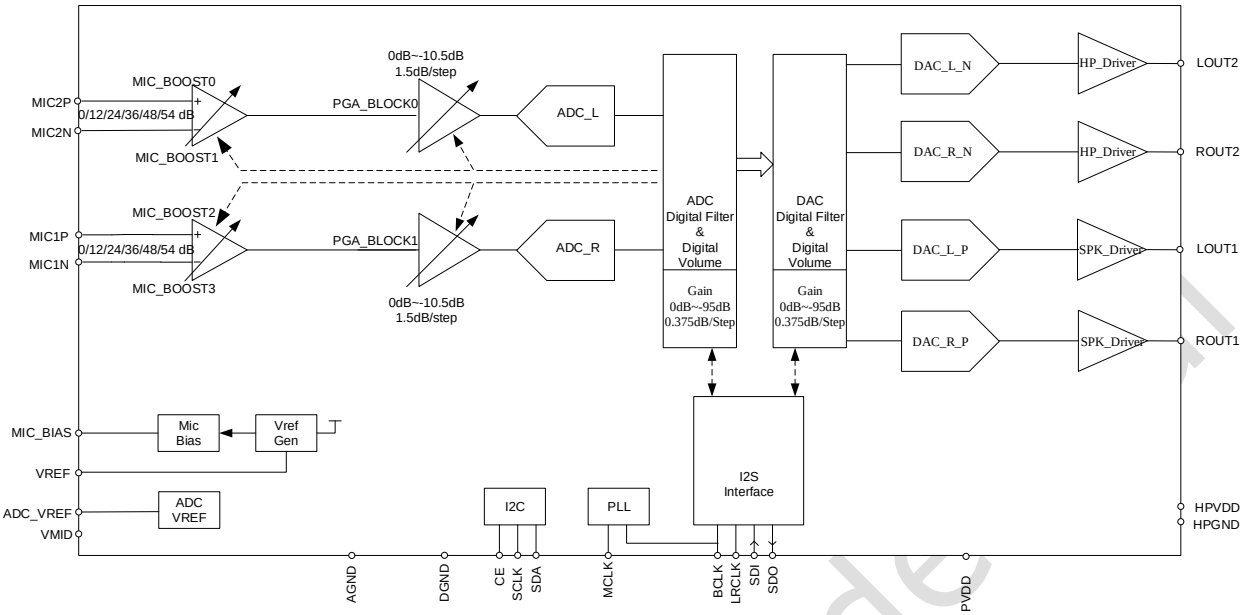


Fig. 1-1 RK730 Functional Block Diagram

1.4 Typical Application Diagrams

HP/SPK Normal mode application diagram

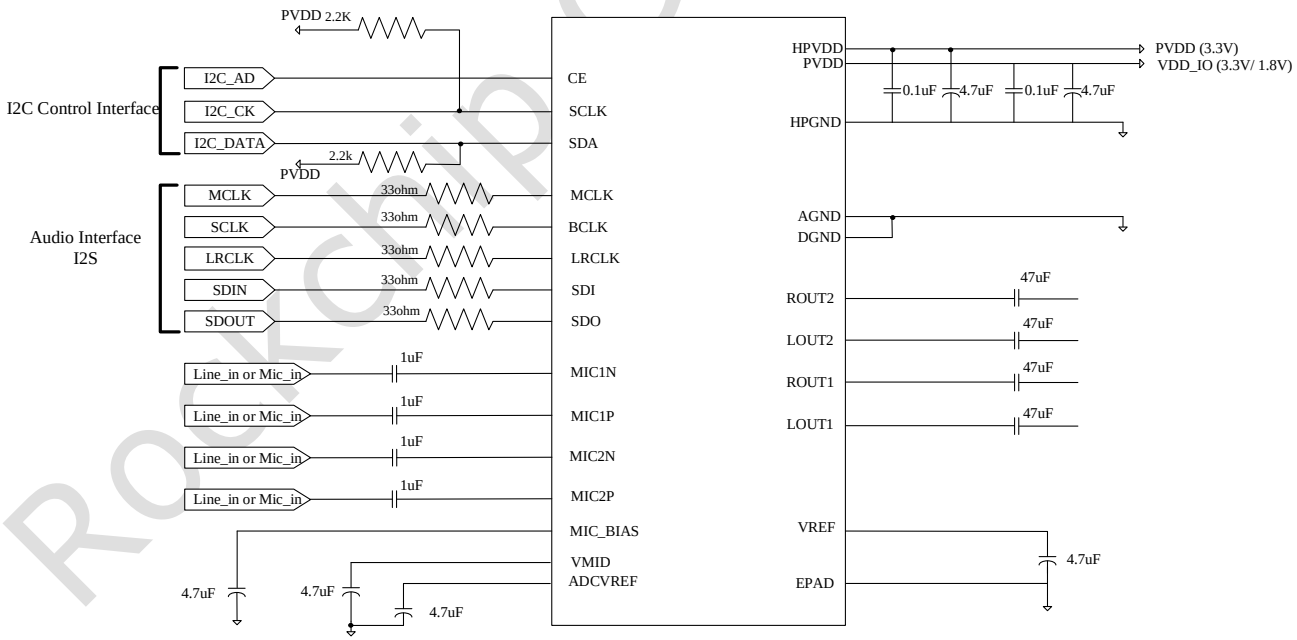


Fig. 1-2 RK730 Typical Application Diagram

HP/SPK Differential mode application diagram

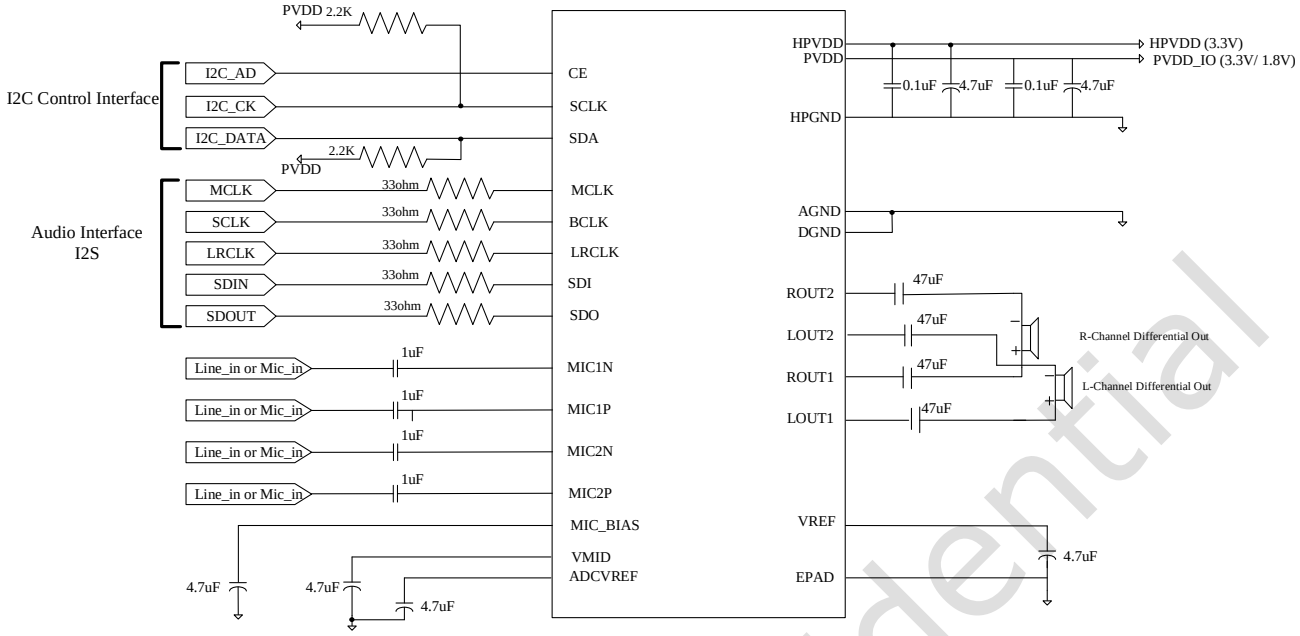


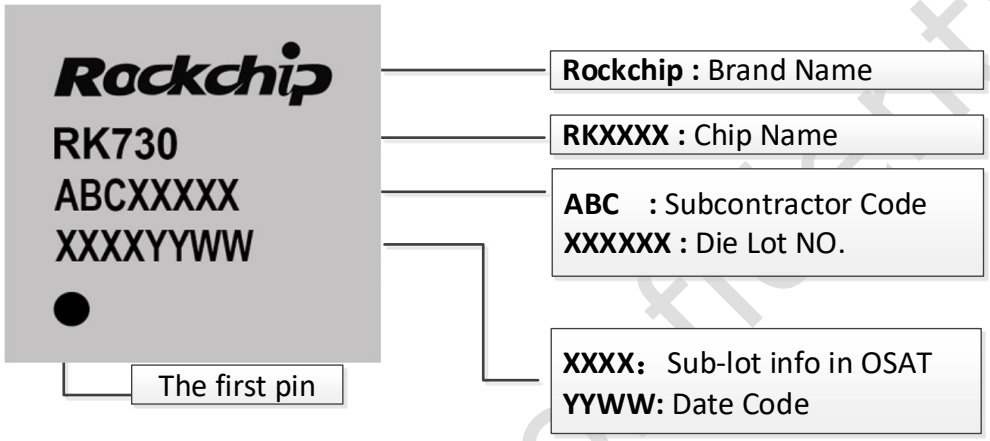
Fig. 1-3 RK730 DAC differential Mode Application Diagram

Chapter 2 Package information

2.1 Ordering information

Orderable Device	RoHS status	Package	Package Detail
RK730	RoHS	QFN28 (4X4) 0.45 Pitch	5000 pcs/ tape, 5 tapes/box, by reel

2.2 Top Marking



2.3 Dimension

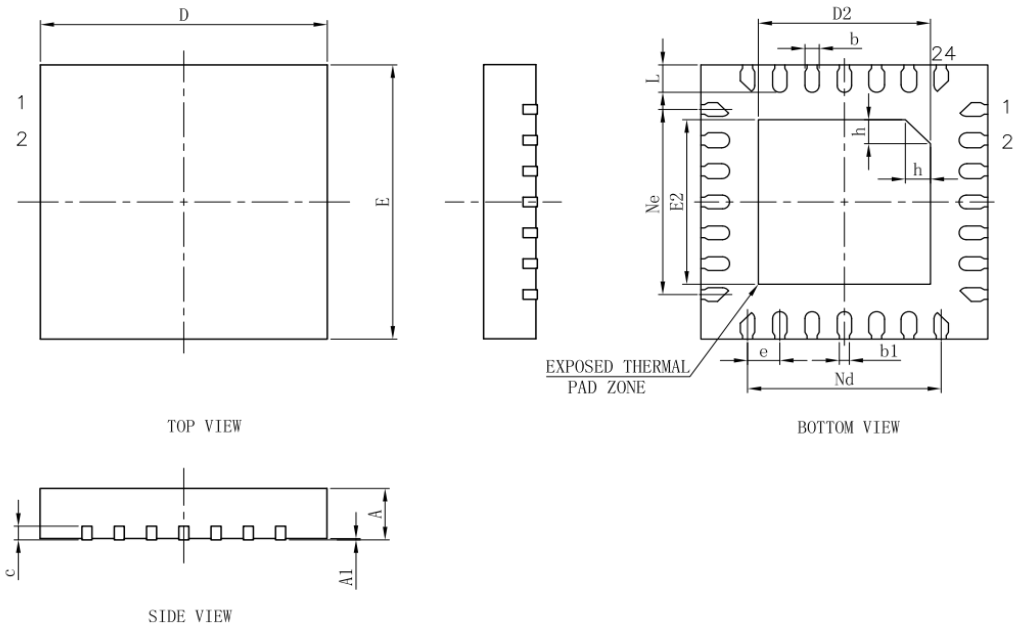


Fig. 2-1 QFN28 4mmX4mm Diagram

DESCRIPTION	SYMBOL	MILLIMETER		
		MIN	NOM	MAX
TOTAL THICKNESS	A	0.70	0.75	0.80
STAND OFF	A1	0	0.02	0.05
LEAD WIDTH	b	0.15	0.20	0.25
	b1		0.14REF	
MATERIAL THICKNESS	c	0.18	0.20	0.25
PACKAGE SIZE	D	3.90	4.00	4.10
EP SIZE	D2	2.30	2.40	2.50
LEAD PITCH	e		0.45BSC	
	Ne		2.70BSC	
	Nd		2.70BSC	
PACKAGE SIZE	E	3.90	4.00	4.10
EP SIZE	E2	2.30	2.40	2.50
LEAD LENGTH	L	0.35	0.40	0.45
LEAD WIDTH	h	0.30	0.35	0.40
	L/F loader size		114X114	

2.4 Pin Assignment

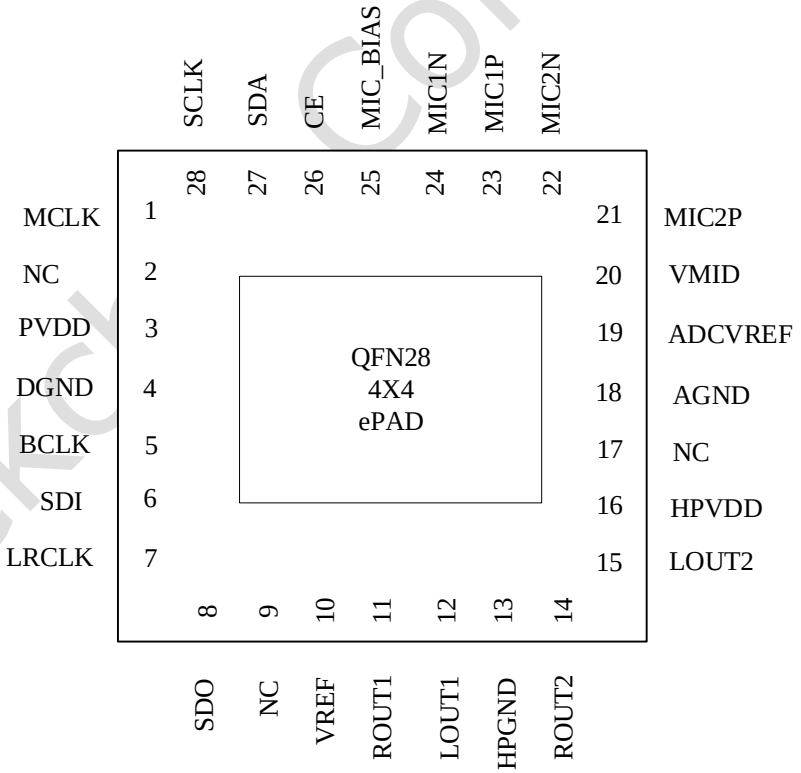


Fig. 2-2 Pin Assignment

2.5 Pinout Number Order

PIN NO	PIN NAME	I/O	PIN DESCRIPTION
1	MCLK	I	Master clock pin
2	NC		Do not connect, left floating
3	PVDD	Supply	Digital IO power supply pin
4	DGND	Supply	Digital Ground
5	BCLK	I/O	I2S interface Bit clock Pin
6	SDI	I	I2S interface input pin
7	LRCLK	I/O	I2S interface Synchronous clock Pin
8	SDO	O	I2S interface output pin
9	NC		Do not connect, left floating
10	VREF	O	Decoupling Cap Pin
11	ROUT1	O	Speaker right channel output Pin (include Lineout/HP)
12	LOUT1	O	Speaker left channel output Pin (include Lineout/HP)
13	HPGND	Supply	Headphone Ground
14	ROUT2	O	HP right channel output Pin (include Lineout/HP)
15	LOUT2	O	HP left channel output Pin (include Lineout/HP)
16	HPVDD	Supply	Headphone power supply
17	NC		Do not connect, left floating
18	AGND	Supply	Analog Ground
19	ADCVREF	O	ADC reference voltage pin
20	VMID	O	Analog reference voltage pin
21	MIC2P	I	MIC second positive input Pin
22	MIC2N	I	MIC second negative input pin
23	MIC1P	I	MIC first positive input Pin
24	MIC1N	I	MIC first negative input pin
25	MIC_BIAS	O	MIC reference voltage pin
26	CE	I	I2C device address selection
27	SDA	I/O	I2C Data Pin
28	SCL	O	I2C clock Pin
EPAD	EPAD	Supply	Ground

Chapter 3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Parameter	Min	Max	Units
Analog Supply Voltage	-0.3	3.6	V
Digital Supply Voltage	-0.3	3.6	V
Input Voltage range	-0.3	3.6	V
Operating Temperature Range	-40	+85	℃
Storage Temperature Range	-65	+150	℃

Note：

Exposure to the conditions exceeded absolute maximum ratings may cause the permanent damages and affect the reliability and safety of both device and systems using the device. The functional operations cannot be guaranteed beyond specified values in the recommended conditions.

3.2 Recommended Operating Conditions

Parameter	Min	TYP	Max	Units
Power Supply				V
PVDD	1.62	1.8/3.3	3.6	V
HPVDD	3.0	3.3	3.6	V

3.3 Analog Specifications

3.3.1 ADC Performance

Parameter	Min	TYP	Max	Units
Full scale input level		1.0		Vrms
Dynamic range (wi A-wt filter)		101		dB
THD+N	-98	-95		dB
Cross Talk(1KHz)	-100	-98		dB
Signal to Noise Ratio (wi A-wt filter)		100		dB
Interchannel Gain Mismatch		0.1		dB
Input resistor		20		Kohm

3.3.2 ADC Digital Filter

Parameter	Min	TYP	Max	Units
Passband		0.4917		Fs
Stopband		0.5479		Fs
Passband Ripple		0.05		dB
Stopband Attenuation		100		dB

3.3.3 DAC to HP performance

Parameter	Min	TYP	Max	Units
Full scale output level		1		Vrms
Signal to Noise Ratio (wi A-wt filter)		98		dB
Dynamic range (wi A-wt filter)		100		dB
THD+N		-85		dB

3.3.4 DAC to HP differential mode performance

Parameter	Min	TYP	Max	Units
Full scale output level		2		Vrms
Signal to Noise Ratio (wi A-wt filter)		98		dB
Dynamic range (wi A-wt filter)		103		dB
THD+N		-88		dB

Chapter 4 Function Description

4.1 Power Supply

In RK730, different power supply voltage is used to make chip work correctly. PVDD is for digital I/O power and create the digital core power. HPVDD is for analog output headphone power and create the analog core power. The default value of this power supply is list on below.

Table 4-1 Power supply of chip

Power	PVDD	HPVDD
setting	3.3V/1.8V	3.3V

4.2 PLL

The system clock of audio core come from internal PLL block. The reference clock of PLL come from the MCLK pin of chip. With the different input frequency clock, the PLL can provide the main clock single for 48K serial sample rate (include 12K/24K/48K/96K/192K Hz), 44.1K serial sample rate (include 11.025K/22.05K/44.1K/88.2K/176.4KHz) and 32K serial sample rate (include 8K/16K/32K/64K/128K). If no MCLK is provided by system, the PLL also can used the BCLK as the signal resource. The detail information is list on below.

Table 4-2 The PLL input clock and output clock serial

PLL working channel select (4bit control)	Reference clock frequency (MHz)	PLL output clock serial	Signal resource
0000	12.288	48K serial	MCLK
0001		44.1K serial	
0010		32K serial	
0011	12	48K serial	MCLK
0100		44.1K serial	
0101		32K serial	
0110	3.072	48K sample	BCLK
0111	2.822	44.1K sample	
1000	2.048	32K sample	
1001	24	48K serial	MCLK
1010		44.1K serial	
1011		32K serial	
1100	6.144	48K serial	MCLK
1101	11.2896	44.1K serial	
1110	8.192	32K serial	
1111	No select	No select	

4.3 ADC Signal Replication

If the ADC input signal is mono, the chip can copy the data to another channel and realize the Stereo output. The detail function is list below:

Table 4-3 ADC output signal selection

Data function	Register	Output type
I2S output	00	Left data = left ADC, right data = right ADC
	01	Left data = left ADC, right data = left ADC
	10	Left data = right ADC, right data = right ADC
	11	Left data = right ADC, right data = left ADC

4.4 DAC signal mixer function

In the signal path, the side tone function is used to feeding a properly gained microphone signal into the DAC stream. The side tone put the ADC output from the microphone input with the digital gain, and adds it to the output signal of the DAC interface.

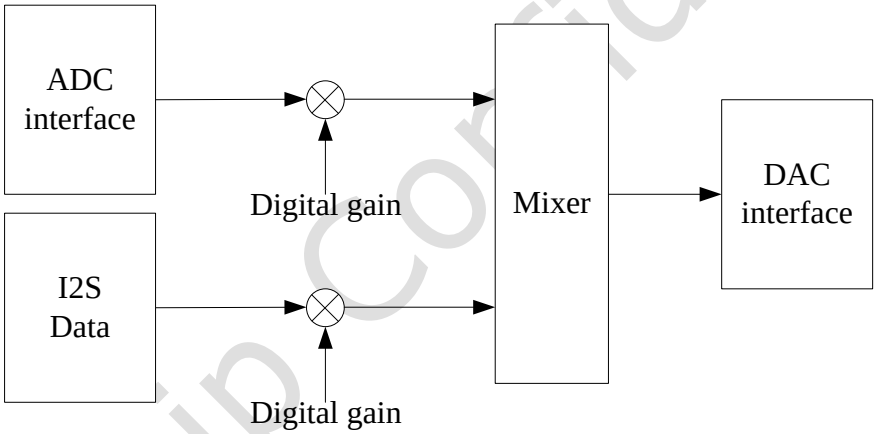


Fig. 4-1 Side Tone function signal flower

The detail side tone function is listed in the following table.

Table 4-4 The Side Tone function description

Side Tone Register	ADC(%)	I2S (%)	Output (%)
0000	100	0	100
0001	87.5	12.5	100
0010	75	25	100
0011	62.5	37.5	100
0100	50	50	100
0101	37.5	62.5	100
0110	25	75	100
0111	12.5	87.5	100
1XXX (except 1111)	0	100	100
1111	(I2S_L+I2S_R)/2	(I2S_L+I2S_R)/2	

4.5 I2C Interface

I2C interface is a bi-directional serial bus which use SDA and SCLK for data transfer. The PIN CE is used as address select Pin, which support 0X17 (tie high) or 0X16 (tie low). The detail timing information can be found in Figure 4-3. Each bit in a byte is sampled during SCLK high with MSB bit being transmitted first. The transfer rate of this interface can be up to 400KHz.

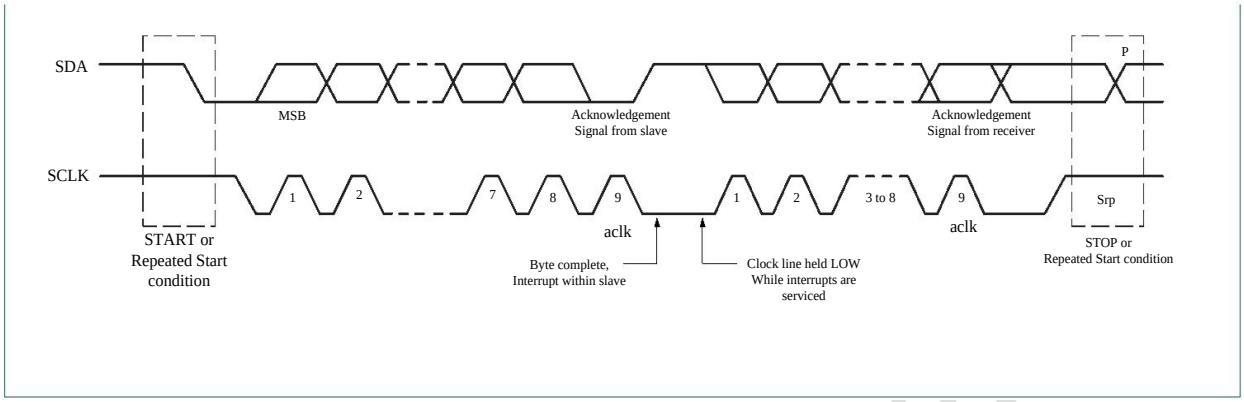


Fig. 4-2 Data transmission timing information for I2C Bus

A Data transmission start with a "start" signal, which is defined as a high-to-low transition at SDA while SCLK is high. The first byte transferred is the address, it is a seven-bit register address followed by a RW bit. Once an acknowledge bit is received, the data transfer starts to proceed on a byte-by-byte data base on the direction specified by the RW bit. The master can terminate the communication by generating a "stop" signal, which is defined as a low-to-high transition at SDA while SCLK is high.

4.6 SPI Interface

RK730 has a SPI (Serial Peripheral Interface) compliant synchronous serial slave controller inside the chip. It provides the ability to allow the external master SPI controller to access the internal registers, and thus control the operations of chip. All lines on the SPI bus are unidirectional: The SPI_CLK is generated by the master controller and is primarily used to synchronize data transfer, the SPI_DIN line carries data from the master to the slave; SPI_CSn is generated by the master to select RK730. The timing diagram of this interface is given in Fig 4-4. The high to low transition at SPI_CSn pin indicates the SPI interface selected. Each write procedure contains 3 words, i.e. Chip Address plus R/W bit, internal register address and internal register data. Every word length is fixed at 8 bits. The input SPI_DIN data are sampled at the rising edge of SPI_CLK clock.

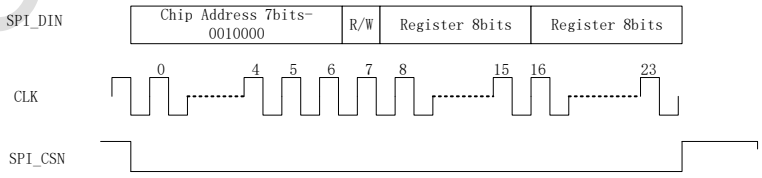


Fig 4-4 SPI Configuration Interface Timing Diagram

4.7 Digital Audio Interface

The device provides four formats of serial audio data interface to the input of the DAC or output from the ADC through LRCK, SCLK and SDIN/SDOUT pins. The four formats are I2S, left justified, right justified and DSP/PCM mode. The relationship of SDATA (SDIN/SDOUT), SCLK and LRCK with the three formats is shown through Figure 4-5 to Figure 4-9

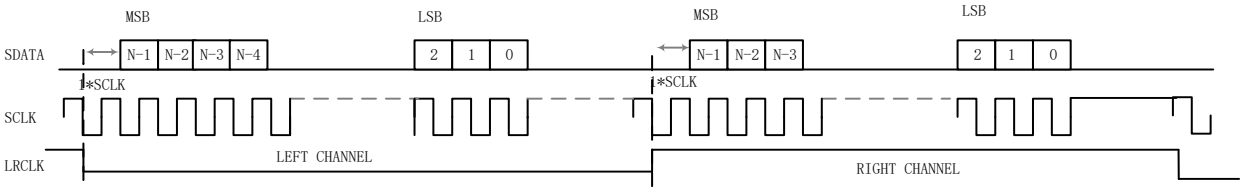


Fig 4-5 I2S Serial Audio Data Format

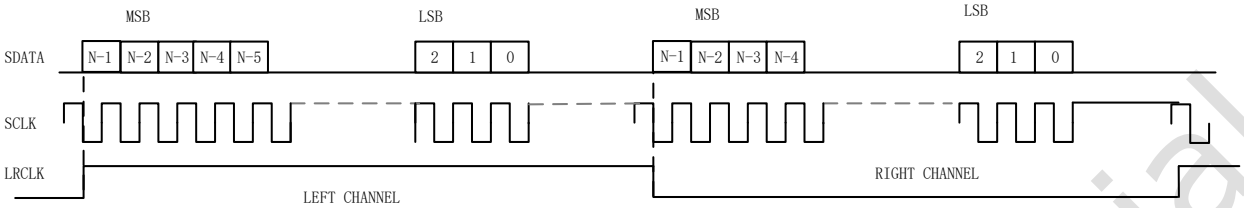


Fig 4-6 Left Justified Serial Audio Data Format

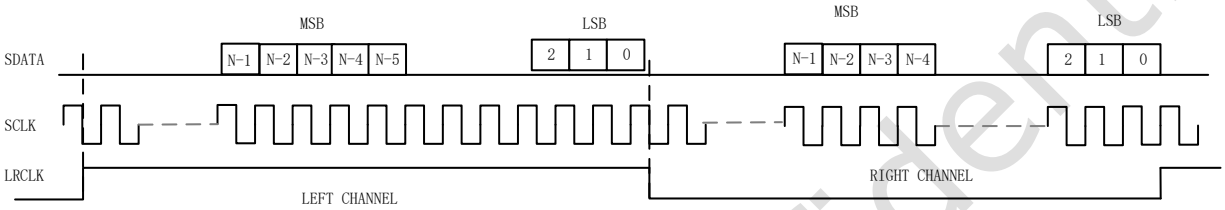


Fig 4-7 Right Justified Serial Audio Data Format

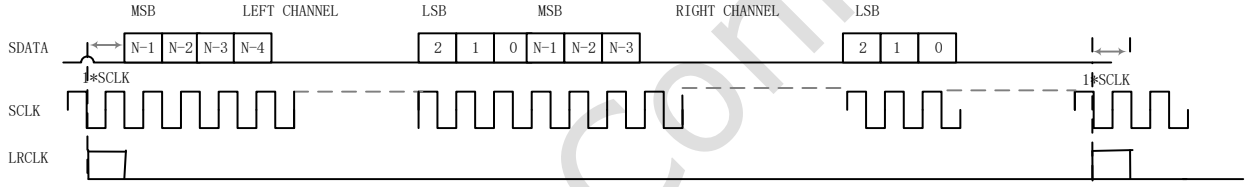


Fig 4-8 DSP/PCM Mode A

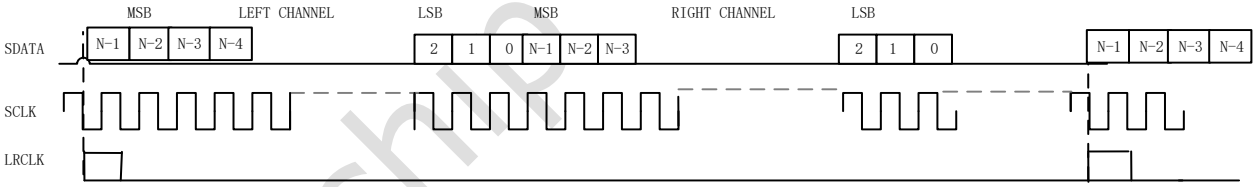


Fig 4-9 DSP/PCM Mode B

Chapter 5 Register Description

5.1 Register Summary

Name	Offset	Size	Reset Value	Description
CODEC_HK_TOP_0	0x0000	B	0x08	
CODEC_HK_TOP_1	0x0001	B	0xC0	
CODEC_HK_TOP_2	0x0002	B	0x20	
CODEC_HK_TRIM	0x0003	B	0x00	
CODEC_ADC_0	0x0004	B	0x03	
CODEC_ADC_1	0x0005	B	0x42	
CODEC_ADC_2	0x0006	B	0x02	
CODEC_ADC_3	0x0007	B	0x05	
CODEC_DAC_0	0x0008	B	0x07	
CODEC_DAC_1	0x0009	B	0x70	
CODEC_MIC_BOOST_0	0x000a	B	0x01	
CODEC_MIC_BOOST_1	0x000b	B	0x01	
CODEC_MIC_BOOST_2	0x000c	B	0x01	
CODEC_MIC_BOOST_3	0x000d	B	0x01	
CODEC_ADC_PGA_BLOCK_0	0x000e	B	0x01	
CODEC_ADC_PGA_BLOCK_1	0x000f	B	0x01	
CODEC_SYSPLL_0	0x0010	B	0xff	
CODEC_SYSPLL_3	0x0013	B	0x04	
CODEC_LDO	0x001f	B	0x11	
CODEC_MIC_BIAS	0x0020	B	0x09	
CODEC_HP_0	0x0021	B	0xAC	
CODEC_HP_1	0x0022	B	0x80	
CODEC_HP_2	0x0023	B	0x00	
CODEC_SPK_0	0x0024	B	0xAC	
CODEC_SPK_1	0x0025	B	0x80	
CODEC_DTOP_DIGEN_CLKE	0x0040	B	0x00	
CODEC_DTOP_SRT	0x0041	B	0x00	
CODEC_DADC_SEL	0x0042	B	0x00	
CODEC_DDAC_SEL	0x0043	B	0x88	
CODEC_DTOP_VUCTL	0x0044	B	0x03	
CODEC_DTOP_VUCTIME	0x0045	B	0xFF	
CODEC_DADC_VOLL	0x0046	B	0x00	
CODEC_DADC_VOLR	0x0047	B	0x00	
CODEC_DDAC_VOLL	0x0048	B	0x00	
CODEC_DDAC_VOLR	0x0049	B	0x00	
CODEC_DADC_RVOLL	0x004a	B	0xFF	
CODEC_DADC_RVOLR	0x004b	B	0xFF	
CODEC_DDAC_RVOLL	0x004c	B	0xFF	
CODEC_DDAC_RVOLR	0x004d	B	0xFF	
CODEC_DADC_FILTER	0x004e	B	0x1E	

CODEC_DDAC_FILTER	0x004f	B	0xF4	
CODEC_DDAC_PREL	0x0050	B	0x00	
CODEC_DDAC_PRER	0x0051	B	0x00	
CODEC_DDAC_POSTL	0x0052	B	0x1F	
CODEC_DDAC_POSTR	0x0053	B	0x1F	
CODEC_DDAC_DRC0	0x005e	B	0x9A	
CODEC_DDAC_DRC1	0x005f	B	0xCC	
CODEC_DDAC_DRC2	0x0060	B	0x1F	
CODEC_DDAC_DRC3	0x0061	B	0xCC	
CODEC_DDAC_DRC4	0x0062	B	0x0E	
CODEC_DDAC_DRC5	0x0063	B	0x08	
CODEC_DDAC_DRC6	0x0064	B	0x06	
CODEC_DDAC_DRC7	0x0065	B	0x02	
CODEC_DDAC_DRC8	0x0066	B	0x05	
CODEC_DDAC_DRC9	0x0067	B	0x01	
CODEC_READ1	0x0068	B	0x00	
CODEC_DI2S_CKM	0x0069	B	0x01	
CODEC_DI2S_OFFSET	0x006a	B	0x00	
CODEC_DI2S_RSD	0x006b	B	0x00	
CODEC_DI2S_RXCR1	0x006c	B	0x00	
CODEC_DI2S_RXCR2	0x006d	B	0x17	
CODEC_DI2S_RXCMD_TSD	0x006e	B	0x00	
CODEC_DI2S_TXCR1	0x006f	B	0x00	
CODEC_DI2S_TXCR2	0x0070	B	0x17	
CODEC_DI2S_TXCR3_TXCMD	0x0071	B	0x00	

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

5.2 Register Description

CODEC_HK_TOP_0
Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
7	RW	0x00	HK_VREF_TEST enable control 0: unable 1: enable
6	RW	0x00	HK_OSC_TEST enable control 0: unable 1: enable
5:4	RW	0x00	HK_VAG_1P6V_SEL: The control signal of VAG_1P6V 0x0: 1.6V 0x1: 1.52V 0x2: 1.7V 0x3: 1.8V
3	RW	0x01	HK_OSC_EN enable control 0: unable 1: enable

Bit	Attr	Reset Value	Description
2	RW	0x00	HK_HALF_VAG_BUF1: The control signal of whether bias current of vag_buf reduces by half 0: not decrease 1: decrease half
1:0	RW	0x00	HK_DAC_CHOP_SEL: The chop clock frequency selection of DAC 0x0: no chop 0x1: 200KHz 0x2: 400KHz 0x3: 800KHz

CODEC_HK_TOP_1
Address: Operational Base + offset (0x0001)

Bit	Attr	Reset Value	Description
7	RW	0x01	HK_PWD_VAG_BUF: VAG_BUF in HK model power down 0: power on 1: power down
6	RW	0x01	HK_PWD_DAC_BUF: DAC_BUF in HK model power down 0: power on 1: power down
5:4	RW	0x00	HK_IBIAS_STD_SEL: The Selection signal of initial current of bias current 0x0: 20uA 0x1: 16.5uA 0x2: 23.5uA 0x3: 27.5uA
3:0	RW	0x00	HK_IBIAS_GAIN_BIT: The gain selection of output current 0x0: 100% 0x1: 71.5% 0x2: 62.5% 0x3: 50% 0x4: 50% 0x6: 38.2% 0x7: 32% 0x8: 200% 0x9: 143% 0xA: 120%

CODEC_HK_TOP_2
Address: Operational Base + offset (0x0002)

Bit	Attr	Reset Value	Description
7:4	RW	0x02	CHIP VERSION
3:1	RW	0x00	HK_VREF_TRIM: The regulation signal of reference voltage 0x0: 896mV ~ 904mV 0x1: 888mV ~ 896mV 0x2: 880mV ~ 888mV 0x3: 872mV ~ 880mV 0x4: 904mV ~ 912mV 0x5: 912mV ~ 920mV 0x6: 920mV ~ 928mV 0x7: 928mV ~ 936mV
0	RW	0x00	Reserved

CODEC_HK_TRIM
Address: Operational Base + offset (0x0003)

Bit	Attr	Reset Value	Description
7	RW	0x00	Reserved
6:4	RW	0x00	HK_TRIM_CAP: The calibration signal of 1.6MHz clock capacity
3:0	RW	0x00	HK_TRIM_RES: The calibration signal of 1.6MHz clock resistance

CODEC_ADC_0
Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
7:6	RW	0x00	adc_delay_clksel: ADC L/R sampling clock delaying control signal 0x0: delay 100% 0x1: delay 75% 0x2: delay 50% 0x3: delay 25%
5:4	RW	0x00	adc_delay_sarsel: ADCL/R SAR quantizer delaying control signal 0x0: delay 100% 0x1: delay 75% 0x2: delay 50% 0x3: delay 25%
3	RW	0x00	adc_sar_eld_off: ADC sar eld compensation function off signal 0: ELD enable 1: ELD disable
2	RW	0x00	adc_zero: ADCL/R integrator reset signal 0: normal 1: reset

Bit	Attr	Reset Value	Description
1	RW	0x01	adc_r_pwd: ADCR power down control signal 0: power on 1: power down
0	RW	0x01	adc_l_pwd: ADCL power down control signal 0: power on 1: power down

CODEC_ADC_1
Address: Operational Base + offset (0x0005)

Bit	Attr	Reset Value	Description
7:5	RW	0x02	adc_ibctrl: ADC L/R overall bias current control 0x0: 133% 0x1: 114% 0x2: 100% 0x3: 89% 0x4: 80% 0x5: 73% 0x6: 67% 0x7: 62%
4	RW	0x00	adc_ibref_inc: ADC ref current control 0: 100% 1: 150%
3	RW	0x00	adc_ibop3_inc: ADC L/R amplifier3 current control 0: 100% 1: 150%
2	RW	0x00	adc_ibop2_inc: ADC L/R amplifier2 current control 0: 100% 1: 200%
1:0	RW	0x02	adc_ibop1_ctrl: ADC L/R amplifier1 current control 0x0: 50% 0x1: 75% 0x2: 100% 0x3: 125%

CODEC_ADC_2
Address: Operational Base + offset (0x0006)

Bit	Attr	Reset Value	Description
7	RW	0x00	adc_chop_ref_sel: 0: fchop_ref=fs, 1: fchop_ref=fs/2
6	RW	0x00	adc_chop_ref_en: 0: refbuf chop disable, 1: refbuf chop enable
5	RW	0x00	adc_chop_sel: 0: fchop_integ=fs/2, 1: fchop_integ=fs/16
4	RW	0x00	adc_chop_en: 0: integ chop disable, 1: integ chop enable
3	RW	0x00	adc_dith_en: 0: dither disable（default）, 1: dither enable

Bit	Attr	Reset Value	Description
2:0	RW	0x02	adc_captrim: ADCL/R integral capacity trim the circuit 0x0: C*0.8 0x1: C*0.9 0x2: C*1.0（default：fs=6.144M） 0x3: C*1.1（fs=5.6448M） 0x4: C*1.2 0x5: C*1.3 0x6: C*1.4 0x7: C*1.5（fs=4.096M）

CODEC_ADC_3
Address: Operational Base + offset (0x0007)

Bit	Attr	Reset Value	Description
7	RW	0x00	Reserved
6	RW	0x00	adc_stop_rtz: ADC L/R RTZ function disable 0: rtz enable, 1: rtz disable
5:4	RW	0x00	adc_dem_ctrl: ADCL/R dem algorithm control signal 00：Temp（default） 01：DWA 10：Bi-DWA1 11：Bi-DWA2
3:2	RW	0x01	adc_sarref_sel<1:0>: 00：1.691V 01：1.8V（default） 10：1.904V 11：1.995V
1:0	RW	0x01	adc_refsel<1:0>: 00：1.2V 01：1.4V（default） 10：1.62V 11：1.7V

CODEC_DAC_0
Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
7：3	RW	0x00	Reserved
2	RW	0x01	pwd_dac_hp_ibias: DAC_HP_ibias power down control 0: enable, 1: disable default
1	RW	0x01	pwd_dac_hp_r: DAC_HP_R power down control 0: enable, 1: disable default

Bit	Attr	Reset Value	Description
0	RW	0x01	pwd_dac_hp_l: DAC_HP_L power down control 0: enable, 1: disable default

CODEC_DAC_1
Address: Operational Base + offset (0x0009)

Bit	Attr	Reset Value	Description
7	RW	0x00	Reserved
6	RW	0x01	pwd_dac_spk_ibias: DAC_spk_ibias power down control 1: power down the spk ibias 0: power on the spk ibias
5	RW	0x01	pwd_dac_spk_r: DAC_spk_R power down control 1: power down the R channel of dac_spk 0: power on the R channel of dac_spk
4	RW	0x01	pwd_dac_spk_l: DAC_spk_L power down control 1: power down the L channel of dac_spk 0: power on the L channel of dac_spk
3:2	RW	0x00	DAC_opbias_sel<1:0>: select the bias current of total dac block 00: 2uA 01: 3uA 10: 4uA 11: 1uA
1:0	RW	0x00	DAC_amp_chg<1:0>: change the dac output amplitude 00: 0dB 01: -1dB 10: 1dB 11: -1.4dB

CODEC_MIC_BOOST_0
Address: Operational Base + offset (0x000a)

Bit	Attr	Reset Value	Description
7:6	RW	0x00	Reserved
5:4	RW	0x00	mic_r2_dec: mic_r2 negative gain selection 0x0: -0dB 0x1: -3dB 0x2: -6dB 0x3: -9dB

Bit	Attr	Reset Value	Description
3:1	RW	0x00	mic_r2_boost: mic_r2 positive gain selection 0x0: 0dB gain 0x1: 6dB gain 0x2: 12dB gain 0x3: 24dB gain 0x4: 36dB gain 0x5: 42dB gain 0x6: 48dB gain 0x7: 54dB gain
0	RW	0x01	mic_r2_pwd: the mic block in Rin2 path power down control 0: power on 1: power down

CODEC_MIC_BOOST_1
Address: Operational Base + offset (0x000b)

Bit	Attr	Reset Value	Description
7:6	RW	0x00	Reserved
5:4	RW	0x00	mic_l2_dec: mic_l2 negative gain selection 0x0: -0dB 0x1: -3dB 0x2: -6dB 0x3: -9dB
3:1	RW	0x00	mic_l2_boost: mic_l2 positive gain selection 0x0: 0dB gain 0x1: 6dB gain 0x2: 12dB gain 0x3: 24dB gain 0x4: 36dB gain 0x5: 42dB gain 0x6: 48dB gain 0x7: 54dB gain
0	RW	0x01	mic_l2_pwd: the mic block in Lin2 path power down control 1: power down 0: power on

CODEC_MIC_BOOST_2
Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
7	RW	0x00	mic_input_toggle : make The MIC Rin1 and MIC Lin2 input exchangeable 0: not exchangeable 1: exchangeable
6	RW	0x00	Reserved

Bit	Attr	Reset Value	Description
5:4	RW	0x00	mic_r1_dec: mic_r1 negative gain selection 0x0: -0dB 0x1: -3dB 0x2: -6dB 0x3: -9dB
3:1	RW	0x00	mic_r1_boost: mic_r1 positive gain selection 0x0: 0dB gain 0x1: 6dB gain 0x2: 12dB gain 0x3: 24dB gain 0x4: 36dB gain 0x5: 42dB gain 0x6: 48dB gain 0x7: 54dB gain
0	RW	0x01	mic_r1_pwd: the mic block in Rin1 path power down control 0: power on 1: power down

CODEC_MIC_BOOST_3
Address: Operational Base + offset (0x000d)

Bit	Attr	Reset Value	Description
7:6	RW	0x00	mic_chop_sel:mic chop clock frequency selection 0x0: no chop signal 0x1: 200KHz 0x2: 400KHz 0x3: 800KHz
5:4	RW	0x00	mic_l1_dec: mic_l1 negative gain selection 0x0: -0dB 0x1: -3dB 0x2: -6dB 0x3: -9dB
3:1	RW	0x00	mic_l1_boost: mic_l1 positive gain selection 0x0: 0dB gain 0x1: 6dB gain 0x2: 12dB gain 0x3: 24dB gain 0x4: 36dB gain 0x5: 42dB gain 0x6: 48dB gain 0x7: 54dB gain
0	RW	0x01	mic_l1_pwd: the mic block in Lin1 path power down control 0: power on 1: power down

CODEC_ADC_PGA_BLOCK_0
Address: Operational Base + offset (0x000e)

Bit	Attr	Reset Value	Description
7:6	RW	0x00	Reserved
5:4	RW	0x0	adc_pga_l_path_sel: adc_pga_l path mode selection 0x0: differential input mode 0x1: vinr2 input path mode 0x2: vinl2 input path mode 0x3: no signal
3:1	RW	0x0	adc_pga_l_gain: adc_pga_l gain selection: 0x0: 0dB gain 0x1: -1.5dB gain 0x2: -3dB gain 0x3: -4.5dB gain 0x4: -6dB gain 0x5: -7.5dB gain 0x6: -9dB gain 0x7: -10.5dB gain
0	RW	0x1	adc_pga_l_pwd :adc_pga_l block power down control 0: power on 1: power down

CODEC_ADC_PGA_BLOCK_1
Address: Operational Base + offset (0x000f)

Bit	Attr	Reset Value	Description
7:6	RW	0x00	pga_chop_sel: pga chop clock frequency selection 0x0: no chop signal 0x1: 200KHz 0x2: 400KHz 0x3: 800KHz
5:4	RW	0x00	adc_pga_r_path_sel: adc_pga_r path mode selection 0x0: differential input mode 0x1: vinr1 input path mode 0x2: vinl1 input path mode 0x3: no signal

Bit	Attr	Reset Value	Description
3:1	RW	0x00	adc_pga_r_gain: adc_pga_r gain selection: 0x0: 0dB gain 0x1: -1.5dB gain 0x2: -3dB gain 0x3: -4.5dB gain 0x4: -6dB gain 0x5: -7.5dB gain 0x6: -9dB gain 0x7: -10.5dB gain
0	RW	0x01	adc_pga_r_pwd :adc_pga_r block power down control 0: power on 1: power down

CODEC_SYSPLL_0
Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
7	RW	0x01	syspll_pdtop :syspll total power down control 0: power on 1: power down
6	RW	0x01	syspll_pdvtune: syspll RVCO tuning voltage power down control 0: power on, RVCO open-loop 1: power down
5	RW	0x01	syspll_pdd_rvco: syspll RVCO bypass control 0: None bypass switch 1: bypass switch and quickly Pre-charge;
4	RW	0x01	syspll_pd_rvco: syspll RVCO power down control 0: power on 1: power down
3	RW	0x01	syspll_pd_pstdiv: syspll Pst-divider power down control 0: power on 1: power down
2	RW	0x01	syspll_pd_prediv: syspll Pre-divider power down control 0: power on 1: power down
1	RW	0x01	syspll_pd_chgp: syspll charge pump power down control 0: power on 1: power down
0	RW	0x01	syspll_pd_buf: syspll RVCO buffer power down control 0: power on 1: power down

CODEC_SYSPLL_3
Address: Operational Base + offset (0x0013)

Bit	Attr	Reset Value	Description
7:4	RW	0x00	syspll_channel: SYSPLL work frequency selection 0x0: input 12.288MHz, output 61.44MHz/12.288MHz 0x1: input 12.288MHz, output 56.448MHz/11.2896MHz 0x2: input 12.288MHz, output 40.96MHz/8.192MHz 0x3: input 12MHz, output 61.44MHz/12.288MHz 0x4: input 12MHz, output 56.448MHz/11.2896MHz 0x5: input 12MHz, output 40.96MHz/8.192MHz 0x6: input 3.072MHz (from BCLK), output 61.44MHz/12.288MHz 0x7: input 2.822MHz (from BCLK), output 56.448MHz/11.2896MHz 0x8: input 2.048MHz (from BCLK), output 40.96MHz/8.192MHz 0x9: input 24MHz, output 61.44MHz/12.288MHz 0xA: input 24MHz, output 56.448MHz/11.2896MHz 0xB: input 24MHz, output 40.96MHz/8.192MHz 0xC: input 6.144MHz, output 61.44MHz/12.288MHz 0xD: input 11.2896MHz, output 56.448MHz/11.2896MHz 0xE: input 8.192MHz, output 40.96MHz/8.192MHz
3:2	RW	0x01	syspll_fsclk_channel: SYSPLL FSCLK selection 0x1: divide by 6 0x3: divide by 9
1:0	RW	0x00	syspll_refclk_channel: SYSPLL MCLK selection 0x0: select 12.288MHz / 12MHz 0x1: select 24.576MHz / 24MHz

CODEC_LDO
Address: Operational Base + offset (0x001f)

Bit	Attr	Reset Value	Description
7	RW	0x00	ANA_LDO_EN: ADC_LDO enabling signal 0: disable 1: enable
6	RW	0x00	ANA_LDO_BYPASS: ANA_LDO bypass signal 0: normal 1: bypass
5:4	RW	0x01	ANA_LDO_VSEL: ANA_LDO output voltage value selection 0x0: 1.691V 0x1: 1.800V 0x2: 1.904V 0x3: 1.995V
3	RW	0x00	Reserved
2	RW	0x00	DIG_LDO_BYPASS: DIG_LDO bypass signal 0: normal 1: bypass
1:0	RW	0x01	DIG_LDO_VSEL: DIG_LDO output voltage value selection 0x0: 1.404V 0x1: 1.500V 0x2: 1.600V 0x3: 1.711V

CODEC_MIC_BIAS
Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
7:4	RW	0x00	Reserved
3:2	RW	0x02	mic_bias_sel: MIC_BIAS output voltage selection 0x0: 2.0V 0x1: 2.2V 0x2: 2.5V 0x3: 2.8V
1	RW	0x00	mic_bias_lp: MIC_BIAS low power mode enabling signal 0: disable 1: enable
0	RW	0x01	mic_bias_pwd: MIC_BIAS clock power down control 0: power on 1: power down

CODEC_ HP_0
Address: Operational Base + offset (0x0021)

Bit	Attr	Reset Value	Description
7	RW	0x01	hp_pwd_antipop: HP antipop process power down control 0: power on 1: power down
6	RW	0x00	hp_dec_en: HP decrease the gain control 1: enable the function gain decrease 0: disable the function gain decrease
5	RW	0x01	hp_pwd_ibias: HP_IBIAS power down control 0: power on 1: power down
4	RW	0x00	hp_twotage_en: HP operation amplifier function enabling control 0:disable 1: enable
3	RW	0x01	hp_ostg_pwd: HP output stage power down control 0: power on 1: power down
2	RW	0x01	hp_pwd: HP block power down control 0: power on 1: power down
1:0	RW	0x00	hp_bias_sel: HP bias current selection 0x0: 2uA 0x1: 3uA 0x2: 4uA 0x3: 1uA

CODEC_HP_1
Address: Operational Base + offset (0x0022)

Bit	Attr	Reset Value	Description
7:6	RW	0x02	hp_antipop_sel: select antipop time 0x0: 0.5s 0x1: 0.75s 0x2: 1.5s 0x3: 2s

Bit	Attr	Reset Value	Description
5:4	RW	0x00	hp_inc_amp: HP increase amplitude gain selection 0x0: +1dB 0x1: +3dB 0x2: +6dB 0x3: +9dB
3:0	RW	0x01	hp_dec_bit: HP decrease gain selection 0x0: 0dB 0x1: -1dB 0x2: -2dB 0x3: -3dB 0x4: -4dB 0x5: -5dB 0x6: -6dB 0x7: -7dB 0x8: -8dB 0x9: -9dB 0xa: -10dB 0xb: -11dB 0xc: -12dB 0xd: -13dB 0xe: -14dB 0xf: -15dB

CODEC_HP_2
Address: Operational Base + offset (0x0023)

Bit	Attr	Reset Value	Description
7:2	RW	0x00	Reserved
1:0	RW	0x00	hp_spk_chop_sel: HP/SPK chop clock frequency selection 0x0: disable chop function 0x1: 200KHz 0x2: 400KHz 0x3: 800KHz

CODEC_ SPK_0
Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
7	RW	0x01	spk_pwd_antipop: SPK antipop process power down control 0: power on 1: power down
6	RW	0x00	spk_dec_en: SPK decrease the gain control 0: disable the function gain decrease 1: enable the function gain decrease
5	RW	0x01	spk_pwd_ibias: SPK_IBIAS power down control 0: power on 1: power down
4	RW	0x00	spk_twotage_en: SPK operation amplifier function enabling control 0:disable 1: enable
3	RW	0x01	spk_ostage_pwd: SPK output stage power down control 0: power on 1: power down

Bit	Attr	Reset Value	Description
2	RW	0x01	spk_pwd: SPK block power down control 0: power on 1: power down
1:0	RW	0x00	spk_bias_sel: SPK bias current selection 0x0: 2uA 0x1: 3uA 0x2: 4uA 0x3: 1uA

CODEC_SPK_1

Address: Operational Base + offset (0x0025)

Bit	Attr	Reset Value	Description
7:6	RW	0x02	spk_antipop_sel: select antipop time 0x0: 0.5s 0x1: 0.75s 0x2: 1.5s 0x3: 2s
5:4	RW	0x00	spk_inc_amp: SPK increase amplitude gain selection 0x0: +1dB 0x1: +3dB 0x2: +6dB 0x3: +9dB
3:0	RW	0x00	spk_dec_bit: SPK decrease gain selection 0x0: 0dB 0x1: -1dB 0x2: -2dB 0x3: -3dB 0x4: -4dB 0x5: -5dB 0x6: -6dB 0x7: -7dB 0x8: -8dB 0x9: -9dB 0xa: -10dB 0xb: -11dB 0xc: -12dB 0xd: -13dB 0xe: -14dB 0xf: -15dB

CODEC_DTOP_DIGEN_CLKE

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
7	RW	0x00	ADC_CKE: ADC clock enable
6	RW	0x00	I2STX_CKE: I2S Tx channel clock enable
5	RW	0x00	ADC_EN: digital adc left channel enable
4	RW	0x00	I2STX_EN: I2S Tx channel enable
3	RW	0x00	DAC_CKE: DAC clock enable
2	RW	0x00	I2SRX_CKE: I2S Rx channel clock enable
1	RW	0x00	DAC_EN: digital dac left channel enable
0	RW	0x00	I2SRX_EN: I2S Rx channel enable

CODEC_DTOP_SRT

Address: Operational Base + offset (0x0041)

Bit	Attr	Reset Value	Description
7	RW	0x00	SRST: soft reset control 0: not reset 1: reset
6:4	RW	0x00	DACSRT: DAC sample rate = 8k/11.025k/12k * power(2,DACSRT) 0x0: 8k/11.025k/12k 0x1: 16k/22.05k/24k 0x2: 32k/44.1k/48k 0x3: 64k/88.2k/96k 0x4: 128k/176.4k/192k
3	RW	0x00	Reserved
2:0	RW	0x00	ADCSRT: ADC sample rate = 8k/11.025k/12k * power(2,ADCSRT) 0x0: 8k/11.025k/12k 0x1: 16k/22.05k/24k 0x2: 32k/44.1k/48k 0x3: 64k/88.2k/96k 0x4: 128k/176.4k/192k

CODEC_DADC_SEL
Address: Operational Base + offset (0x0042)

Bit	Attr	Reset Value	Description
7:5	RW	0x00	Reserved
4	RW	0x00	DACMT: DAC mute function control 0:unmute 1:mute
3	RW	0x00	ADC_MUTE_R: ADC path R-channel mute 0:unmute 1:mute
2	RW	0x00	ADC_MUTE_L: ADC path L-channel mute 0:unmute 1:mute
1:0	RW	0x00	ADC_DATSEL: ADC path signal copy select 0x0: left data = left ADC, right data = right ADC 0x1: left data = left ADC, right data = left ADC 0x2: left data = right ADC, right data = right ADC 0x3: left data = right ADC, right data = left ADC

CODEC_DDAC_SEL
Address: Operational Base + offset (0x0043)

Bit	Attr	Reset Value	Description
7:4	RW	0x8	DAC_MIXER_R: function same as DAC_MIXER_L except for R channel
3:0	RW	0x8	DAC_MIXER_L: DAC path SideTone select 0x0: DAC input = 100%ADC+0%I2SRX 0x1: DAC input = 87.5%ADC+12.5%I2SRX 0x2: DAC input = 75%ADC+25%I2SRX 0x3: DAC input = 62.5%ADC+37.5%I2SRX 0x4: DAC input = 50%ADC+50%I2SRX 0x5: DAC input = 37.5%ADC+62.5%I2SRX 0x6: DAC input = 25%ADC+75%I2SRX 0x7: DAC input = 12.5%ADC+87.5%I2SRX

Bit	Attr	Reset Value	Description
			0x8-0xE: DAC input = 0%ADC+100%I2SRX 0xF: DAC input = 50%I2SRX_L+50%I2SRX_R

CODEC_DTOP_VUCTL
Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
7	RW	0x00	ADC_BYPS: ADC volume control bypass 0: enable 1: bypass
6	RW	0x00	DAC_BYPS: DAC volume control bypass 0: enable 1: bypass
5	RW	0x00	Reserved
4	RW	0x00	DACFade: DAC fade control 0: update to new volume immediately 1: fade enable
3	RW	0x00	DAC_LV_POL: DAC path L channel digital volume gain polarity 0: negative gain 1: positive gain
2	RW	0x00	DAC_RV_POL: DAC path R channel digital volume gain polarity 0: negative gain 1: positive gain
1	RW	0x01	Reserved
0	RW	0x01	DACZDT 0: update every sample 1: update when zero-cross point

CODEC_DTOP_VUCTIME
Address: Operational Base + offset (0x0045)

Bit	Attr	Reset Value	Description
7:0	RW	0xff	VUCT: Time limit = VUCT *(1/sample rate)

CODEC_DADC_VOLL
Address: Operational Base + offset (0x0046)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	ADCLV: ADC path L-channel Digital Volume Register 0db~-95db,0.375db/step

CODEC_DADC_VOLR
Address: Operational Base + offset (0x0047)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	ADCRV: ADC path R-channel Digital Volume Register 0db~-95db,0.375db/step

CODEC_DDAC_VOLL
Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	DACLV: DAC path L-channel Digital Volume Register 0db~-95db,0.375db/step

CODEC_DDAC_VOLR
Address: Operational Base + offset (0x0049)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	DACRV: DAC path R-channel Digital Volume Register 0db~-95db,0.375db/step

CODEC_DADC_RVOLL
Address: Operational Base + offset (0x004a)

Bit	Attr	Reset Value	Description
7:0	RO	0xff	ADCRLV: ADC internal gain of left channel

CODEC_DADC_RVOLR
Address: Operational Base + offset (0x004b)

Bit	Attr	Reset Value	Description
7:0	RO	0xff	ADCRRV: ADC internal gain of right channel

CODEC_DDAC_RVOLL
Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
7:0	RO	0xff	DACRLV: DAC internal gain of left channel

CODEC_DDAC_RVOLR
Address: Operational Base + offset (0x004d)

Bit	Attr	Reset Value	Description
7:0	RO	0xff	DACRRV: DAC internal gain of right channel

CODEC_DADC_FILTER
Address: Operational Base + offset (0x004e)

Bit	Attr	Reset Value	Description
7	RW	0x00	HPFL: ADC path L channel HPF enable 0:disable 1:enable
6	RW	0x00	HPFR: ADC path R channel HPF enable 0:disable 1:enable
5:4	RW	0x01	HPF_CF: ADC path HPF center frequency 0x0: 3.79HZ 0x1: 60HZ 0x2: 243HZ 0x3: 493HZ
3	RW	0x01	CICCOMP_ENA32: cic comp filter enable when sample rate is 48K
2	RW	0x01	CICCOMP_ENA64: cic comp filter enable when sample rate is 24K

Bit	Attr	Reset Value	Description
1:0	RW	0x02	CICCOMP_CF: CIC compensation filter output scale coefficient 0x0: 3/8 0x1: 6/8 0x2: 1

CODEC_DDAC_FILTER
Address: Operational Base + offset (0x004f)

Bit	Attr	Reset Value	Description
7:6	RW	0x3	DAC_MODATCF: attenuation coeffcient for DAC modulator input 0x0: 0.9 (11'h399) 0x1: 0.85 (11'h366) 0x2: 0.75 (11'h300) 0x3: 1 (11'h400)
5:4	RW	0x3	DAC_HB1ATCF: attenuation coeffcient for DAC HB1 filter input 0x0: 0.9 (11'h399) 0x1: 0.85 (11'h366) 0x2: 0.75 (11'h300) 0x3: 1 (11'h400)
3:2	RW	0x1	DAC_D_HPF_CF: DAC path HPF center frequency 0x0:80HZ 0x1:100HZ 0x2:120HZ 0x3:140HZ
1	RW	0x0	Reserved
0	RW	0x0	DAC_D_HPF: DAC path HPF enable 0:disable 1:enable

CODEC_DDAC_PREL
Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
7:5	RW	0x0	Reserved
4:0	RW	0x00	DAC_PRE_GAIN_L: pre-drc gain for DAC channel L, 0~28.5dB, 1.5dB/step 0x00: 0dB, … 0x0F: 22.5dB 0x10: 24dB … 0x13: 28.5dB

CODEC_DDAC_PRER
Address: Operational Base + offset (0x0051)

Bit	Attr	Reset Value	Description
7:5	RW	0x0	Reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x00	DAC_PRE_GAIN_R: pre-drc gain for DAC channel R, 0~28.5dB, 1.5dB/step 0x00: 0dB … 0x0F: 22.5dB 0x10: 24dB … 0x13: 28.5dB

CODEC_DDAC_POSTL
Address: Operational Base + offset (0x0052)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	Reserved
5:0	RW	0x1f	DAC_POST_GAIN_L: post-drc gain for DAC channel L, -11.625~12dB, 0.375dB/step 0x0: -11.625dB … 0xF: -6dB 0x10: -5.625dB … 0x1F: 0dB 0x20: 0.375dB … 6'h3F: 12dB

CODEC_DDAC_POSTR
Address: Operational Base + offset (0x0053)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	Reserved
5:0	RW	0x1f	DAC_POST_GAIN_R: post-drc gain for DAC channel R, -11.625~12dB, 0.375dB/step 0x0: -11.625dB … 0xF: -6dB 0x10: -5.625dB … 0x1F: 0dB 0x20: 0.375dB … 6'h3F: 12dB

CODEC_DDAC_DRC0
Address: Operational Base + offset (0x005e)

Bit	Attr	Reset Value	Description
7:4	RW	0x09	DRC_NGRED: reducing noise level: 0~45dB, 3dB/step
3	RW	0x01	DRC_PRREC_EN: recovery enable 0: disable 1: enable

Bit	Attr	Reset Value	Description
2	RW	0x00	DRC_ZCR_EN: disable zero crossing 0: enable 1: disable
1	RW	0x01	DRC_NG_EN: Noise gate enable control 0: disable 1: enable
0	RW	0x00	DRC_EN: DRC enable control 0: disable 1: enable

CODEC_DDAC_DRC1
Address: Operational Base + offset (0x005f)

Bit	Attr	Reset Value	Description
7:0	RW	0xcc	DRC_PROFFSET[7:0]: DAC threshold scale coefficient in PRMODE S9.8 default:9'h0CC-->0.8

CODEC_DDAC_DRC2
Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
7	RW	0x00	DRC_PROFFSET[8]: DAC threshold scale coefficient in PRMODE S9.8 default:9'h0CC-->0.8
6:5	RW	0x0	Reserved
4:0	RW	0x1f	DRC_PRTHD: DAC limiter threshold: 0~-46.5dB, 1.5dB/step

CODEC_DDAC_DRC3
Address: Operational Base + offset (0x0061)

Bit	Attr	Reset Value	Description
7:0	RW	0xcc	DRC_NGOFFSET[7:0]: DAC threshold scale coefficient in NGMODE S9.8 default:9'h0CC-->0.8

CODEC_DDAC_DRC4
Address: Operational Base + offset (0x0062)

Bit	Attr	Reset Value	Description
7	RW	0x00	DRC_NGOFFSET[8]: DAC threshold scale coefficient in NGMODE S9.8 default:9'h0CC-->0.8
6:5	RW	0x0	Reserved
4:0	RW	0x0e	DRC_NGTHD: DAC noise gate threshold: -36~-82.5dB, 1.5dB/step

CODEC_ DDAC_DRC5
Address: Operational Base + offset (0x0063)

Bit	Attr	Reset Value	Description
7:5	RW	0x0	Reserved
4:0	RW	0x08	DRC_LEN: DAC power detect length: 2^DRC_DRC_LEN

CODEC_ DDAC_DRC6
Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
7:5	RW	0x0	Reserved
4:0	RW	0x06	DRC_PRARATE:DAC limiter attack rate: 4×2^DRC_PRARATE

CODEC_ DDAC_DRC7
Address: Operational Base + offset (0x0065)

Bit	Attr	Reset Value	Description
7:5	RW	0x0	Reserved
4:0	RW	0x02	DRC_PRRRATE: DAC limiter recovery rate: 4×2^DRC_PRRRATE

CODEC_ DDAC_DRC8
Address: Operational Base + offset (0x0066)

Bit	Attr	Reset Value	Description
7:5	RW	0x0	Reserved
4:0	RW	0x05	DRC_NGARATE: DAC noise gate attack rate: 4×2^DRC_NGARATE

CODEC_ DDAC_DRC9
Address: Operational Base + offset (0x0067)

Bit	Attr	Reset Value	Description
7:5	RW	0x0	Reserved
4:0	RW	0x01	DRC_NGRRATE: DAC noise gate recovery rate: 4×2^DRC_NGRRATE

CODEC_ READ1
Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
7:3	RW	0x0	Reserved
2	RO	0x00	DAC_MTST: DAC mute status 0: not in mute status; 1: now in mute status
1	RO	0x00	DAC_NGVALID: DAC NG status 0: not in NG status; 1: now in NG status
0	RO	0x00	ADC_NGVALID: ADC NG status 0: not in NG status; 1: now in NG status

CODEC_DI2S_CKM
Address: Operational Base + offset (0x0069)

Bit	Attr	Reset Value	Description
7:4	RW	0x00	SCK_DIV: F(mclk2x)/F(sclk) - 1
3	RW	0x00	SCK_EN: i2s sclk clock enable, active in master mode. 0: disable 1: enable
2	RW	0x00	SCK_P: sclk polarity 0: normal 1: reversed

Bit	Attr	Reset Value	Description
1	RW	0x00	I2S_RX_MST: I2S Rx master mode enable 0: slave mode 1: master mode
0	RW	0x01	I2S_MST: I2S Tx master mode enable 0: slave mode 1: master mode

CODEC_DI2S_OFFSET
Address: Operational Base + offset (0x006a)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	CH_OFFSET_1: the changing edge of the lrclk starts data transfer after a delay of ch_offset_1. 0x00: offset = 0 BCLKs 0x01: offset = 1 BCLKs …… 0xFE: offset = 254 BCLKs 0xFF: offset = 255 BCLKs

CODEC_DI2S_RSD
Address: Operational Base + offset (0x006b)

Bit	Attr	Reset Value	Description
7:3	RW	0x0	Reserved
2:1	RW	0x00	SCKD_RX: sclk divider for Rx lrck generator 0x0:64 0x1:128, valid only if lrclk <= 96k 0x2:256, valid only if lrclk <= 48k
0	RW	0x00	RXRL_P: I2S Rx lrck polarity 0: normal 1: reversed

CODEC_DI2S_RXCR1
Address: Operational Base + offset (0x006c)

Bit	Attr	Reset Value	Description
7	RW	0x0	Reserved
6	RW	0x00	TFS_RX: Rx transfer mode seletor 0: I2S, 1: PCM
5:4	RW	0x00	PBM_RX: Rx PCM bus mode 0x0: no delay 0x1: delay1 0x2: delay2 0x3: delay3
3:2	RW	0x00	IBM_RX: Rx I2S bus mode 0x0: normal 0x1: left 0x2: right
1	RW	0x00	EXRL_RX: Rx exchange right/left
0	RW	0x00	LSB_RX: 0x0: MSB 0x1: LSB

CODEC_DI2S_RXCR2
Address: Operational Base + offset (0x006d)

Bit	Attr	Reset Value	Description
7:5	RW	0x0	Reserved
4:0	RW	0x17	VDW_RX: valid date width 0x17: 24 bits data width 0x0F: 16 bits data width others: reserved

CODEC_DI2S_RXCMD_TSD
Address: Operational Base + offset (0x006e)

Bit	Attr	Reset Value	Description
7	RW	0x00	RXS: Rx transfer start
6	RW	0x00	RXC: Rx transfer clear
5:3	RW	0x0	Reserved
2:1	RW	0x00	SCKD_TX: sclk divider for Tx lrck generator 0x0:64 0x1:128, valid only if lrclk <= 96k 0x2:256, valid only if lrclk <= 48k
0	RW	0x00	TXRL_P: I2S Tx lrck polarity

CODEC_DI2S_TXCR1
Address: Operational Base + offset (0x006f)

Bit	Attr	Reset Value	Description
7	RW	0x0	Reserved
6	RW	0x00	TFS_TX: Tx transfer mode seletor 0: I2S, 1: PCM
5:4	RW	0x00	PBM_TX: Tx PCM bus mode 0x0: no delay 0x1: delay1 0x2: delay2 0x3: delay3
3:2	RW	0x00	IBM_TX: Tx I2S bus mode 0x0: normal 0x1: left 0x2: right
1	RW	0x00	EXRL_TX: Tx exchange right/left
0	RW	0x00	LSB_TX: 0x0: MSB 0x1: LSB

CODEC_DI2S_TXCR2
Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
7:5	RW	0x00	SDO_SEL_TX: sdo output data select 0x0、0x7: (ADC L/ADC R) 0x1: (ADC L, ADC R/DAC L, DAC R) 0x2: (ADC L/DAC L) 0x3: (ADC L/DAC R) 0x4: (ADC R/DAC L) 0x5: (ADC R/DAC R) 0x6: (DAC L/DAC R)

Bit	Attr	Reset Value	Description
4:0	RW	0x17	VDW_TX: valid date width 0x17: 24 bits data width 0x0F: 16 bits data width others: reserved

CODEC_DI2S_TXCR3_TXCMD
Address: Operational Base + offset (0x0071)

Bit	Attr	Reset Value	Description
7	RW	0x00	TXS: Tx transfer start
6	RW	0x00	TXC: Tx transfer clear
5:0	RW	0x00	RCNT_TX: right justified counter for I2S right justified slave mode only

Chapter 6 USER GUIDE

This chapter will give some reference register configurations about how to power up/off CODEC, make the codec in the stand by state and how to control the DAC, ADC to integrate the CODEC with you environment.

6.1 Power UP

This section will give the suggest configuration steps to power up the CODEC.

STEP	DESCRIPTION
0	Supply the power of the digital part and analog part
1	Configure the register **CODEC_LDO** reg0x1F[7] to 1'b1, enable the analog LDO VMID
2	Configure the register **CODEC_SYSPLL_0** reg0x10[7:0] to 8'b00000000, to power on syspll

6.2 Power OFF

This section will give the suggest configuration steps to power off the CODEC.

STEP	DESCRIPTION
0	Keep the power on and disable the DAC and ADC path.
1	Configure the register **CODEC_SYSPLL_0** reg0x10[7:0] to 8'b11111111, to power down syspll.
2	Configure the register **CODEC_LDO** reg0x1F[7] to 1'b0, disable the analog LDO VMID.
3	Power off the analog and digital power supply

6.3 ENABLE ADC

This section will give the suggest configuration steps to enable the ADC.

STEP	DESCRIPTION
0	Power up the CODEC according to the section 6.1.
1	Configure the register **CODEC_HK_TOP_1** reg0x01[7] to 1'b0, to power on VAG buffer.
2	Configure the register **CODEC_MIC_BOOST_0** reg0x0A[0] to 1'b0, to power on mic_r2.
3	Configure the register **CODEC_MIC_BOOST_1** reg0x0B[0] to 1'b0, to power on mic_l2.
4	Configure the register **CODEC_MIC_BOOST_2** reg0x0C[0] to 1'b0, to power on mic_r1.
5	Configure the register **CODEC_MIC_BOOST_3** reg0x0D[0] to 1'b0, to power on mic_l1. Configure the register **CODEC_MIC_BOOST_3** reg0x0D[7:6] to 2'b01, set mic chop clock frequency.
6	Configure the register **CODEC_ADC_PGA_BLOCK_0** reg0x0E[0] to 1'b0, to power on adc_pga_l.
7	Configure the register **CODEC_ADC_PGA_BLOCK_1** reg0x0F[0] to 1'b0, to power on adc_pga_r. Configure the register **CODEC_ADC_PGA_BLOCK_1** reg0x0F[7:6] to 2'b01, to set pga chop clock frequency.
8	Configure the register **CODEC_ADC_0** reg0x04[1:0] to 2'b00, to power on adc_r & adc_l.
9	Configure the register **CODEC_ADC_2** reg0x06[4] to 1'b1, to enable adc_chop.

	Configure the register **CODEC_ADC_2** reg0x06[3] to 1'b1, to enable adc_dither.
10	Configure the register **CODEC_ADC_3** reg0x07[5:4] to 2'b01, to set adc_dem_ctrl as DWA.
11	Configure the register **CODEC_DTOP_SRT** reg0x41[2:0] to 3'b010, to set ADC sample rate.
12	Configure the register **CODEC_DTOP_VUCTL** reg0x44[7] to 1'b1, to enable ADC_BYPS.
13	Configure the register **CODEC_DI2S_CKM** reg0x69[0] to 1'b0, to set I2S slave mode.
14	Configure the register **CODEC_DI2S_TXCR1** reg0x6F[6] to 1'b0, to set I2S mode.
15	Configure the register **CODEC_DI2S_TXCR3_TXCMD** reg0x71[7:0] to 8'b10001000, to set tx transfer start.
16	Configure the register **CODEC_DTOP_DIGEN_CLKE** reg0x40[7:6] to 2'b11, to enable ADC_CKE & I2STX_CKE.
17	Configure the register **CODEC_DTOP_DIGEN_CLKE** reg0x40[5:4] to 2'b11, to enable digital ADC & I2STX channel.
18	Begin recording.

6.4 DISABLE ADC

This section will give the suggest configuration steps to disable the ADC.

STEP	DESCRIPTION
0	Keep ADC channel work and stop recording.
1	Configure the register **CODEC_DTOP_DIGEN_CLKE** reg0x40[5:4] to 2'b00, to disable digital ADC & I2STX channel.
2	Configure the register **CODEC_DTOP_DIGEN_CLKE** reg0x40[7:6] to 2'b00, to disable ADC_CKE & I2STX_CKE.
3	Configure the register **CODEC_DI2S_TXCR3_TXCMD** reg0x71[7:0] to 8'b00000000, to set tx transfer stop.
8	Configure the register **CODEC_ADC_0** reg0x04[1:0] to 2'b11, to power down adc_r & adc_l.
7	Configure the register **CODEC_ADC_PGA_BLOCK_1** reg0x0F[0] to 1'b1, to power down adc_pga_r.
	Configure the register **CODEC_ADC_PGA_BLOCK_0** reg0x0E[0] to 1'b1, to power down adc_pga_l.
6	Configure the register **CODEC_MIC_BOOST_3** reg0x0D[0] to 1'b1, to power down mic_l1.
4	Configure the register **CODEC_MIC_BOOST_2** reg0x0C[0] to 1'b1, to power down mic_r1.
3	Configure the register **CODEC_MIC_BOOST_1** reg0x0B[0] to 1'b1, to power down mic_l2.
2	Configure the register **CODEC_MIC_BOOST_0** reg0x0A[0] to 1'b1, to power down mic_r2.
1	Configure the register **CODEC_HK_TOP_1** reg0x01[7] to 1'b1, to power down VAG buffer.

6.5 ENABLE DAC

This section will give the suggest configuration steps to enable the DAC.

STEP	DESCRIPTION
0	Power up the CODEC according to the section 6.1.
1	Configure the register **CODEC_HK_TOP_1** reg0x01[7:6] to 2'b00, to power on VAG buffer and DAC buffer.

2	Configure the register **CODEC_DTOP_SRT** reg0x41[6:4] to 3'b010, to set DAC sample rate.
3	Configure the register **CODEC_DTOP_VUCTL** reg0x44[6] to 1'b1, to enable DAC_BYPS.
4	Configure the register **CODEC_DI2S_CKM** reg0x69[7:0] to 8'b00111010.
5	Configure the register **CODEC_DTOP_DIGEN_CLKE** reg0x40[7:4] to 4'b0101, to enable I2STX_EN & I2STX_CKE.
6	Configure the register **CODEC_DTOP_DIGEN_CLKE** reg0x40[7:4] to 4'b0000, to disable I2STX_EN & I2STX_CKE.
7	Configure the register **CODEC_DI2S_CKM** reg0x69[7:0] to 8'b00000000, to enable I2S slave mode.
8	Configure the register **CODEC_DI2S_RXCMD_TSD** reg0x6E[7] to 1'b1, to enable rx transfer start.
9	Configure the register **CODEC_DTOP_DIGEN_CLKE** reg0x40[3:0] to 4'b0101, to enable I2SRX_EN & I2SRX_CKE.
10	Configure the register **CODEC_DTOP_DIGEN_CLKE** reg0x40[3:0] to 4'b1111, to enable DAC_EN & DAC_CKE.
11	Configure the register **CODEC_DDAC_FILTER** reg0x4F[7:4] to 4'b0000, to set DAC_MODATCF & DAC_HB1ATCF.
12	Configure the register **CODEC_DAC_0** reg0x08[2:0] to 3'b000, to power on dac_hp_bias, dac_hp_r and dac_hp_l.
13	Configure the register **CODEC_DAC_1** reg0x09[6:4] to 3'b000, to power on dac_spk_bias, dac_spk_r and dac_spk_l.
14	Configure the register **CODEC_HP_0** reg0x21[7:0] to 8'b10000000, to enable the function hp_gain increase, power on hp_ostg & hp
15	Configure the register **CODEC_SPK_0** reg0x24[7:0] to 8'b10000000, to enable the function spk_gain increase, power on spk_ostg & hp
16	Play the music.

6.6 DISABLE DAC

This section will give the suggest configuration steps to disable the DAC.

STEP	DESCRIPTION
0	Keep the DAC channel work and input the mute signal.
1	Configure the register **CODEC_SPK_0** reg0x24[3:2] to 2'b11, to power down spk_ostg & hp
2	Configure the register **CODEC_HP_0** reg0x21[3:2] to 2'b11, to power down hp_ostg & hp
3	Configure the register **CODEC_DAC_1** reg0x09[6:4] to 3'b111, to power down dac_spk_bias, dac_spk_r and dac_spk_l.
4	Configure the register **CODEC_DAC_0** reg0x08[2:0] to 3'b111, to power down dac_hp_bias, dac_hp_r and dac_hp_l.
5	Configure the register **CODEC_DTOP_DIGEN_CLKE** reg0x40[3:0] to 4'b0101, to disable DAC_EN & DAC_CKE.
6	Configure the register **CODEC_DTOP_DIGEN_CLKE** reg0x40[3:0] to 4'b0000, to disable I2SRX_EN & I2SRX_CKE.
7	Configure the register **CODEC_DI2S_RXCMD_TSD** reg0x6E[7] to 1'b0, to enable rx transfer stop.
8	Configure the register **CODEC_HK_TOP_1** reg0x01[7:6] to 2'b11, to power down VAG buffer and DAC buffer.