Rockchip RK801 Datasheet

Revision 1.1
Mar.2025

Revision History

Date	Revision	Description
2025-03-31	1.1	1. Update Register Description of XX_EN_MASK and SYS_CFG1 2. Update description of the Device Sleep Enable Conditions 3. Modify the description of the Power Sequence for RK801-2 4. Update rated output current of the Buck4
2024-11-25	1.0	Initial release

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Chapter 1 Introduction

1.1 Overview

The RK801 is a complex power-management integrated circuit (PMIC). The RK801 can provide a complete power management solution with very few external components.
The RK801 contains 2 LDO regulators, Power-up/power-down controller is configurable and can support any customized power-up/power-down sequences (OTP based).
The RK801 integrates 4 channels step-down DC-DC converters (2 channels HV buck and 2 channels LV buck). All of them adopt ripple base control to achieve very fast load transient response. Meanwhile, all of them can dynamically adjust the output voltage, as required by the processor based on the processor's operation status so as to maximize the system efficiency. The output voltages of most channels can be configured through the I2C interface. The inputs of all channels have soft start function, which greatly reduces the inrush current at the startup. 2MHz switching frequency for LV buck and good control method decrease the external inductance and capacitance.
The RK801 is available in a QFN28 4.0 mm x 4.0 mm package, with a 0.4-mm pin pitch.

1.2 Feature

- Input voltage range of VCCH1/2: 4.5V – 14.2V
- Low standby current of 100uA
- 2MHz Switching Frequency for low voltage buck3,4 and 0.75MHz Switching Frequency for high voltage buck1,2
- Internal compensation and soft start
- I^2C Programmable output levels
- High efficiency architecture
- Integrated Vout Discharge Circuit for BUCK and LDO
- Power:
  - CH1: Synchronous HV-Buck regulator, 3A max
  - CH2: Synchronous HV-Buck regulator, 3A max
  - CH3: Synchronous LV-Buck regulator, 1.5A max
  - CH4: Synchronous LV-Buck regulator, 2.5A max
  - CH5, CH6: Linear regulators LDO1/2, 800mA max
  - CH7: SWITCH: 2A max
- Auxiliary: Flexible Power Sequence control
- Package: 4mmx4mm QFN28 (pitch 0.4mm)

1.3 Block Diagram

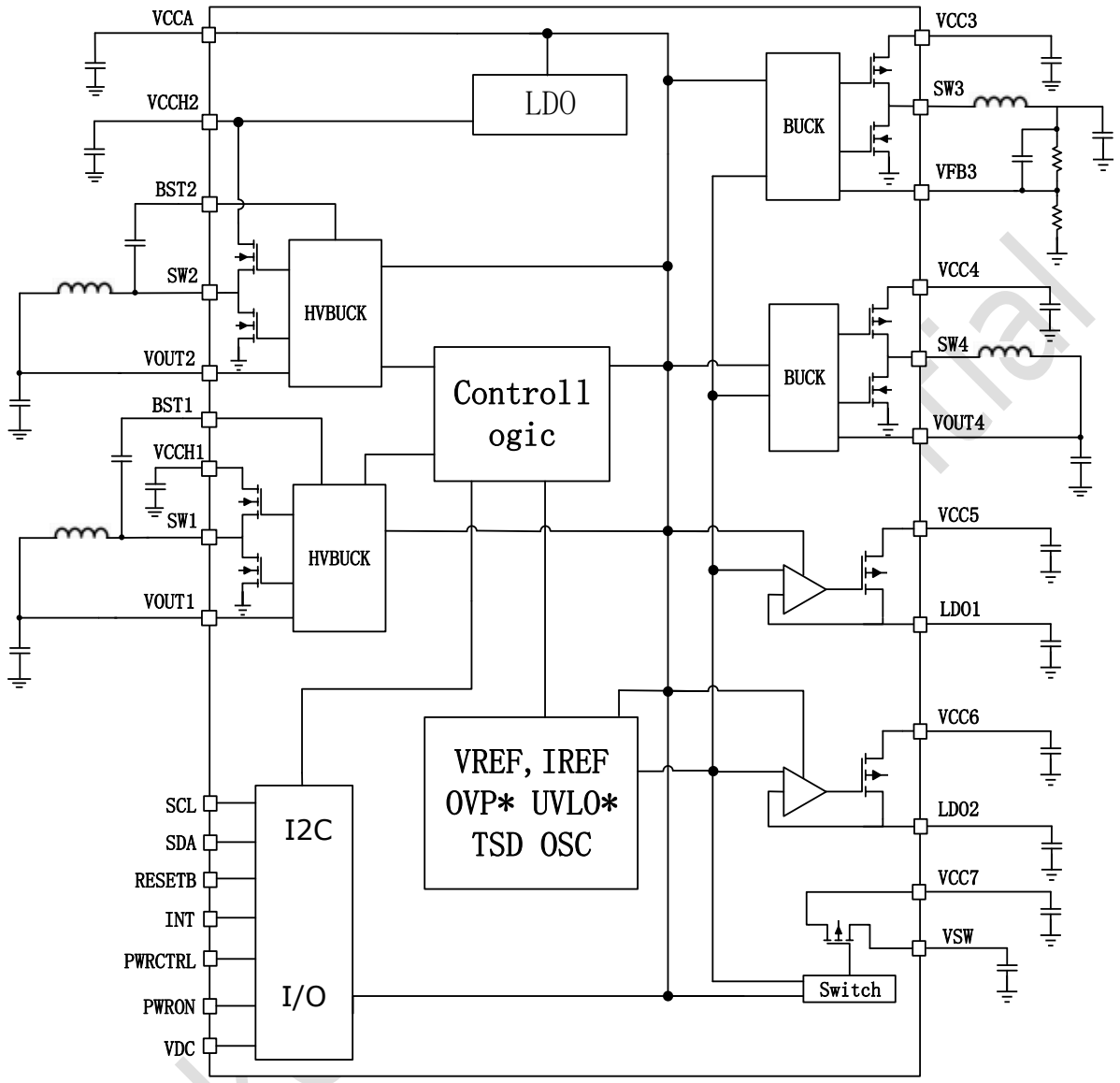


Fig.1-1 RK801 Block diagram

1.4 Typical Application Diagram

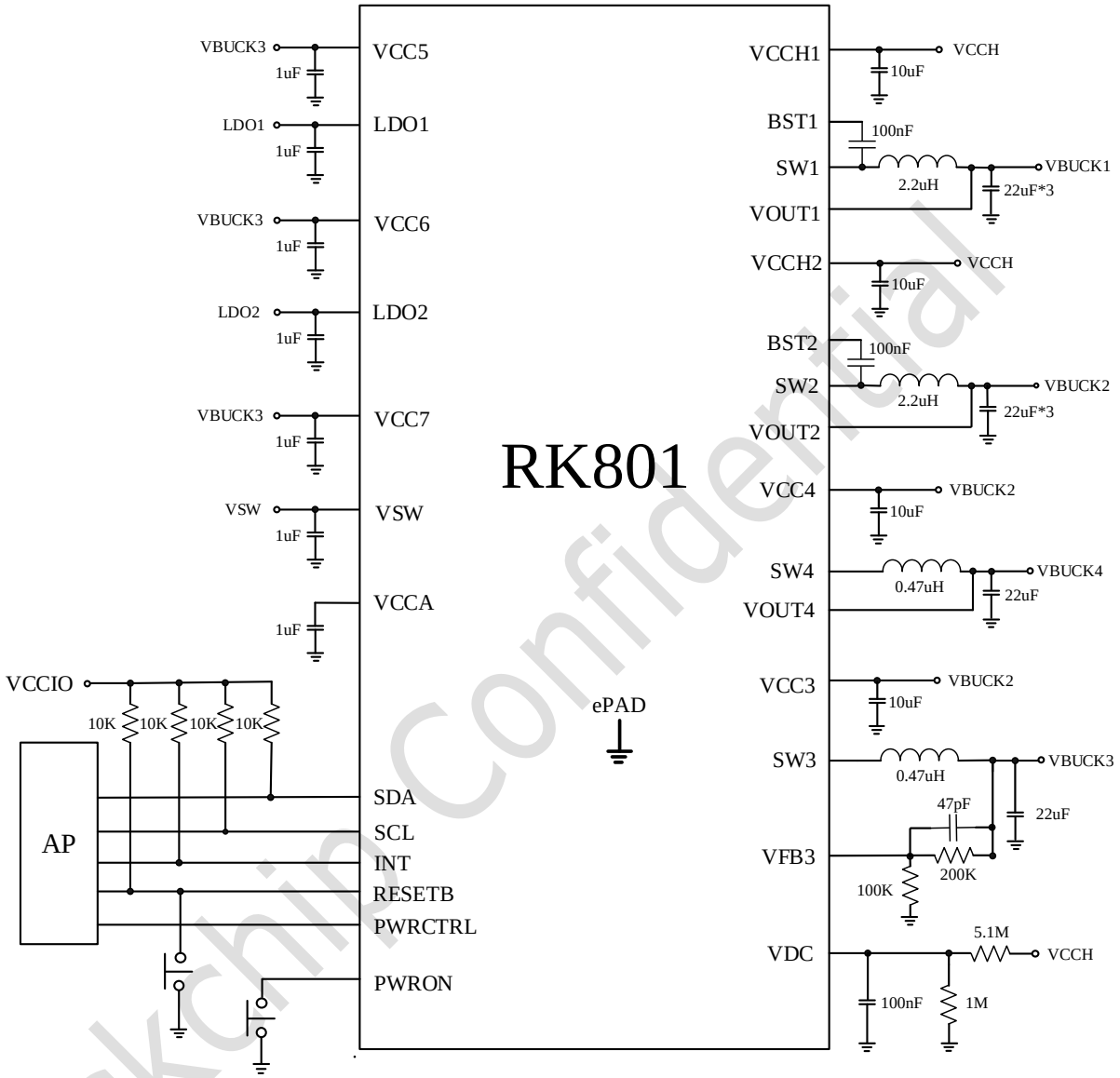


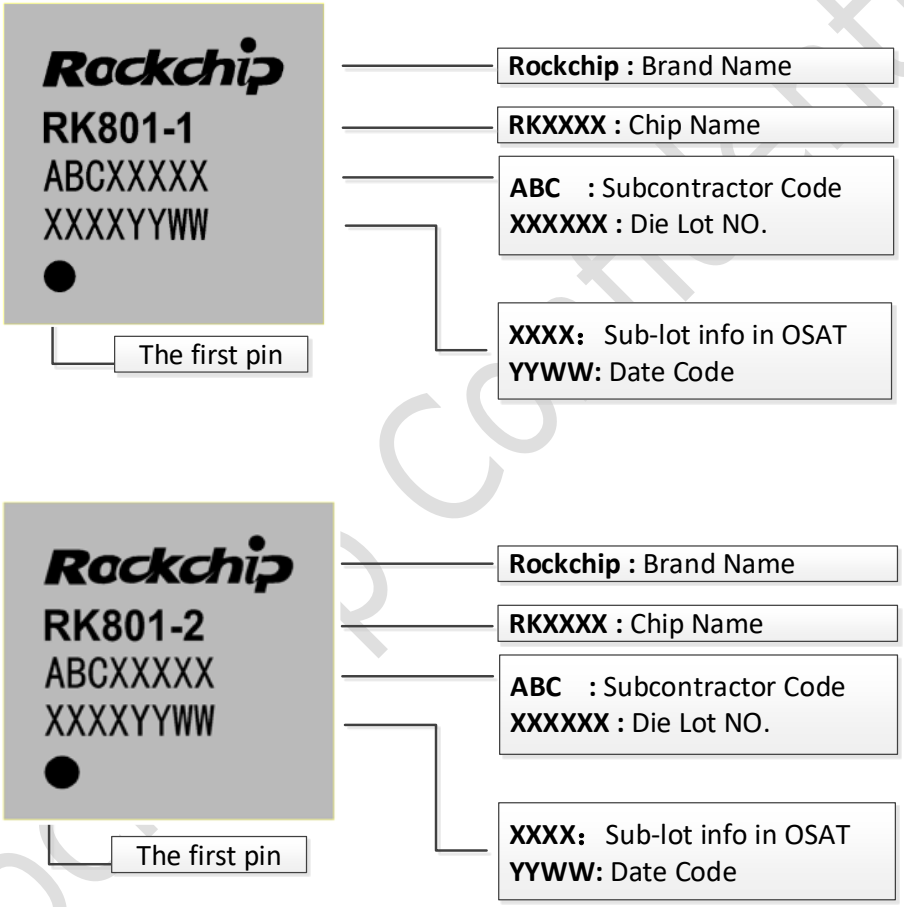
Fig. 1-2 RK801 Application

Chapter 2 Package information

2.1 Ordering information

Orderable Device	RoHS status	Package	Package type	One Reel IC Qty	Master carton reel Qty
RK801-1	RoHS	QFN (4X4)	Reel	2000	5
RK801-2	RoHS	QFN (4X4)	Reel	2000	5

2.2 Top Marking



2.3 MSL Information

Moisture sensitivity Level ： MSL3

2.4 Lead Finish/Pin Material Information

Lead Finish/Pin Material ： Sn

2.5 Dimension

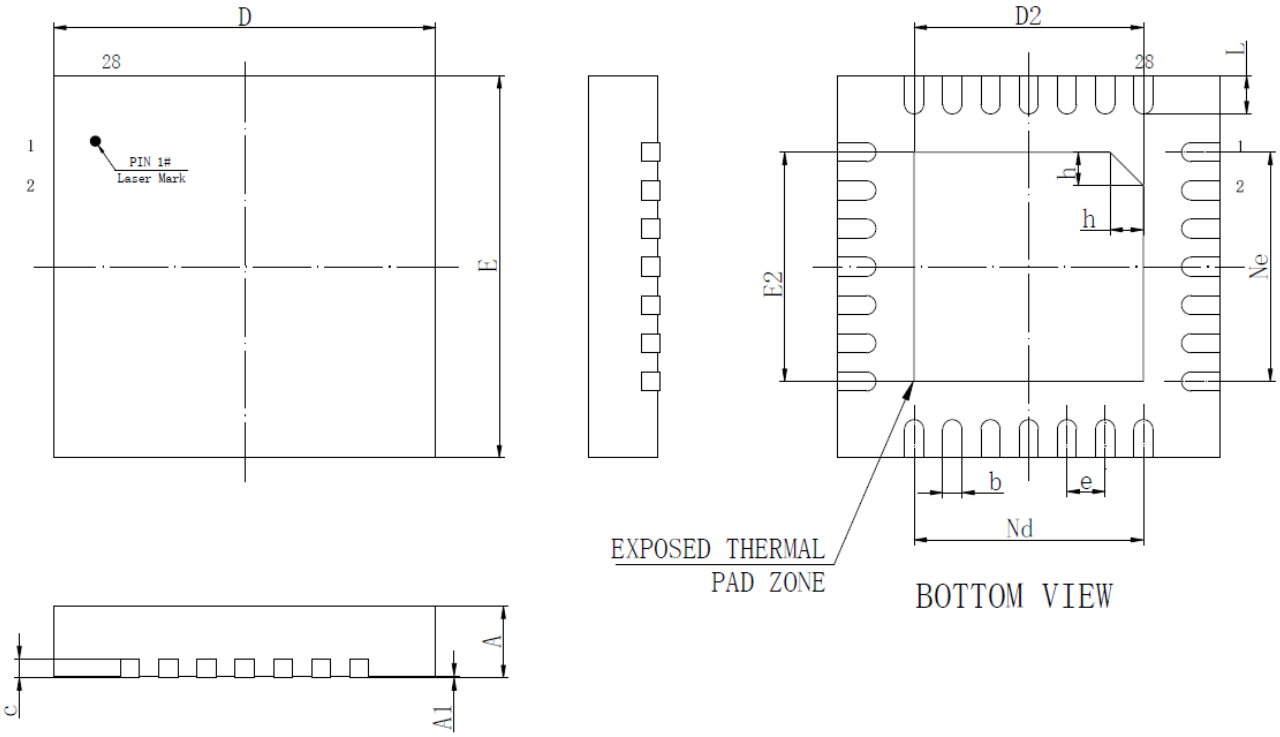


Fig. 2-1 QFN28 4mm X 4mm（Pitch is 0.4mm）

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0. 70	0.75	0. 80
A1	0	0. 02	0. 05
b	0. 15	0.20	0. 25
c	0.18	0.20	0.25
D	3. 90	4. 00	4. 10
D2	2. 30	2. 40	2. 50
e	0. 40BSC		
Nd	2. 40BSC		
E	3. 90	4. 00	4. 10
E2	2. 30	2. 40	2. 50
Ne	2. 40BSC		
L	0. 35	0. 40	0. 45
h	0. 30	0. 35	0. 40

Note:

- *Coplanarity applies to leads, corner leads and die attach pad.*
- *Dimension b applies to metalized terminal and is measured between 0.15mm and 0.25mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measure in that radius area.*
- *0.2mm of dimension b is recommended in PCB layout.*

2.6 Pin Assignment

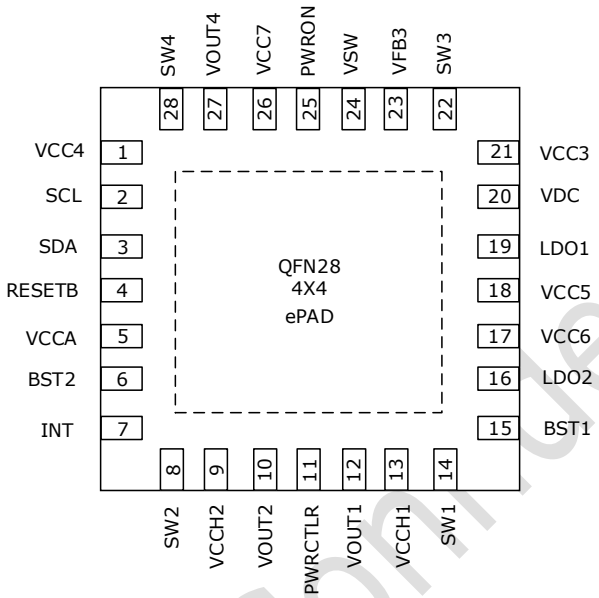


Fig. 2-2 Pin Assignment

2.7 Pinout Number Order

PIN NO	PIN NAME	PIN DESCRIPTION
1	VCC4	Power supply of BUCK4
2	SCL	I2C clock input(Open drain output)
3	SDA	I2C data input and output(Open drain output)
4	RESETB	Reset pin after power on, active low;
5	VCCA	Power supply of inner circuit;
6	BST2	Boostrap capacitor of High voltage BUCK2
7	INT	Interrupt request pin(Open drain output)
8	SW2	Switching node of High voltage BUCK2
9	VCCH2	Power supply of High voltage BUCK2
10	VOUT2	Output feedback voltage of high voltage of BUCK2
11	PWRCTLR	PWRCTLR control input.
12	VOUT1	Output feedback voltage of high voltage of BUCK1
13	VCCH1	Power supply of High voltage BUCK1
14	SW1	Switching node of High voltage BUCK1
15	BST1	Boostrap capacitor of High voltage BUCK1
16	LDO2	LDO2 output
17	VCC6	Power supply of LDO2
18	VCC5	Power supply of LDO1
19	LDO1	LDO1 output

PIN NO	PIN NAME	PIN DESCRIPTION
20	VDC	VDC input;
21	VCC3	Power supply of BUCK3
22	SW3	Switching node of BUCK3
23	VFB3	Output feedback voltage of BUCK3
24	VSW	Output of SWITCH
25	PWRON	Power on key input, active low, internal 22k resistor pull high to VCCA
26	VCC7	Power supply of SWITCH
27	VOUT4	Output feedback voltage of BUCK4
28	SW4	Switching node of BUCK4
Exposed pad	Exposed ground	Ground

Chapter 3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Parameter	Min	Max	Units
Voltage range on pins BSTx	-0.3	25	
Voltage range on pins VCCHx	-0.3	20	V
Voltage range on pins SW1/2	-0.3（-2V for <20ns and -3.5V for <10ns）	20(22V for <20ns)	V
Voltage range on pins SW3/4	-0.3（-2V for <20ns and -3.5V for <10ns）	6.5(7V for <20ns)	V
Voltage range on pins all other PINx	-0.3	6.5	V
Storage temperature range, TS	-40	150	℃
Junction temperature		150	℃
Continuous Power Dissipation(T_A=+25° C）		3.88	W
Maximum Soldering Temperature,T_{SOLDER}		300	℃

Note 1. Exposure to the conditions exceeded absolute maximum ratings may cause the permanent damages and affect the reliability and safety of both device and systems using the device. The functional operations cannot be guaranteed beyond specified values in the recommended conditions.

3.2 Recommended Operating Conditions

Parameter	Min	TYP	Max	Units
Voltage range between pin BST1 and SW1 Voltage range between pin BST2 and SW2	3		5.5	V
Voltage range on pins VCCH1/2/SW1/SW2	4.5		14.4	V
Voltage range on pins VCC3/4	3.0	5	5.5	V
Voltage range on pins VCC5/6	2.2	5	5.5	V
Voltage range on pins VCC7	1.8	5	5.5	V
Voltage range on other pins			5.5	V
Operating temperature range, TJ	-40		125	℃

3.3 DC Characteristics

T_J=25C; V_{VCCH}=12V,V_{VCCA}=VCCx=5V, unless otherwise specified.

Parameter	Symbol	Note	Min.	Typ.	Max.	Unit
VCCH Input (VCCH is the power supply of high voltage BUCK)						
VCCH Operating Range	V_{VCCH}		4.5	12	14.2	V
VCCH over voltage protect	V_{VCCH_ov}			14.4		V
VCCH under voltage protect	V_{VCCH_uv}			4.2		V
VCCA under voltage protect	V_{VCCA_uv}			3.6		V
Shut down current	I_{VCCH_off}	VCCH=12V		8	14	uA
Power on current 2: buck2, buck3,LDO1/LDO2 power on, Null load	I_{VCCH_on}	VCCH=12V		0.2		mA
Power on and sleep current: buck2, buck3,LDO1/ldo2 power on, low power mode, sleep mode, Null load	Isleep	VCCH=12V		0.1		mA
VCC3,4 Input (VCC3,4 is the power supply of low voltage buck)						

Parameter	Symbol	Note	Min.	Typ.	Max.	Unit
VCC3/4 Operating Range	V_{VCC3}		3	5	5.5	V
VCC3/4 under voltage protect	V_{VCC3_uv}			2.8		V
VCC5,6 Input (VCC5,6 is the power supply of LDO)						
VCC5/6 Operating Range	V_{VCC5}		2.2		5.5	V
CH1：Buck 1						
Input supply voltage range	V_{CCH1}		4.5		14.2	V
Output Voltage Accuracy @ all load @ all input voltage range	V_{OUT1}	0. 5V~1.5V by I2C programmed. (Step=12.5mV)/1.8V/2. 2V/3.3V/5.0V/5.25V	0.891	0.9	0.918	V
Rated output current	I_{MAX1}		3			A
Switching Frequency when FPWM mode at Null load	Fsw1	V_{CCH1}=12V,V_{OUT1}=Default Voltage(Refer to Figure 4-5)	0.675	0.75	0.825	MHz
set register 0x33H=55 and 0x21H=18,when the input voltage is lower than 6V, which is used to reduce the output ripple.						
CH2：Buck 2						
Input supply voltage range	V_{CCH2}		4.5		14.2	V
Output Voltage Accuracy @ all load @ all input voltage range	V_{OUT2}	0.8V/0.85V/0.9V/1.8V/2. 2V/3.3V/5.0V/5.25V	4.875	5	5.125	V
Rated output current	I_{MAX2}		3			A
Switching Frequency when FPWM mode at Null load	Fsw2	V_{CCH2}=12V,V_{OUT2}=Default Voltage(Refer to Figure 4-5)	0.675	0.75	0.825	MHz
set register 0x33H=55 and 0x21H=18,when the input voltage is lower than 6V, which is used to reduce the output ripple.						
CH3：Buck 3						
Input supply voltage range	V_{CC3}		3		5.5	V
Output Voltage Accuracy @ all load @ all input voltage range	V_{FB3}	Selection of external resistor divider	0.364	0.375	0.386	V
Rated output current	I_{MAX3}		1.5			A
Switching Frequency when FPWM mode at Null load	Fsw3	V_{CCH3}=12V,V_{OUT3}=1.2V	1.8	2.0	2.2	MHz
VBUCK3= V_{FB3} * (1+Rfbup/Rfbdn)； please refer to the typical application						
CH4：Buck 4						
Input supply voltage range	V_{CC4}		3		5.5	V
Feedback Voltage, Default	V_{out4}	0. 5V~1.5V by I2C programmed. (Step=12.5mV)/1.8V /2.2V/2.5V/2.8V/3.0 V/3.3V/	3.234	3.3	3.366	V
Rated output current	I_{MAX4}		2.5			A
Switching Frequency when FPWM mode at Null load	Fsw4	V_{CCH4}=12V,V_{OUT4}=Default Voltage(Refer to Figure 4-5)	1.8	2.0	2.2	MHz
CH5 ： LDO1						
Input supply voltage range	V_{CC5}		2.2		5.5	V
Output Voltage Accuracy @ all load @ all input voltage range	V_{LDO1}	0.5V~3.4V programmed by I2C. Step=50mV	0.882	0.9	0.918	V
Rated output current	I_{MAX5}	V_{CC5}-V_{LDO1}≥1. 7V V_{CC5}-V_{LDO1}≥0. 4V	800 300			mA
Power supply reject ratio (f=1kHz)	PSRR1	V_{CC5}=3.3V, V_{LDO1}=0.9V		60		dB
When VCC5-VLDO1≤50mV,set 0x06<6>=1, used to reduce light load leakage of LDO.(Under normal working conditions, set 0x06<6>=1,the current is increased by about 4uA).						
CH6 ： LDO2						
Input supply voltage range	V_{CC6}		2.2		5.5	V
Output Voltage Accuracy @ all	V_{LDO2}	0.5V~3.4V programmed by I2C.	1.764	1.8	1.836	V

Parameter	Symbol	Note	Min.	Typ.	Max.	Unit
load @ all input voltage range		Step=50mV				
Rated output current	I_{MAX6}	V_{CC6}-V_{LDO2}≥1.7V V_{CC6}-V_{LDO2}≥0.4V	800 300			mA
Power supply reject ratio (f=1kHz)	PSRR2	V_{CC6}=3.3V, V_{LDO2}=1.8V		60		dB
When VCC6-VLDO2≤50mV,set 0x06<6>=1, used to reduce light load leakage of LDO.(Under normal working conditions, set 0x06<6>=1,the current is increased by about 4uA).						
CH7 ： SWITCH						
Input supply voltage range	V_{CC7}		1.8		5.5	V
On resistance (@VCC7≥ 3.3V)	Ron(@VCC7≥ 3.3)				200	mΩ
	Ron(@VCC7≥ 1.8)				300	mΩ
Rated output current	I_{MAX7}		2			A
Short current limited				400		mA
I2C Interface(7 bits I2C slave address: 27H,28H)						
SCL clock frequency	f_{SCL}				1	MHz
Logic input						
Input LOW-Level Voltage	V_{IL}		-0.3		0.4	V
Input HIGH-Level Voltage: SCLK，PWRCTRL，SDA	V_{IH}		1.2		VCCA +0.3	V
VDC threshold voltage			1.15	1.2	1.25	V
VDC hysteresis voltage				100		mV
OPEN DRAIN OUTPUT PIN						
RESETB,INT,SDA,SCL						
INTERNAL RC CLOCK						
The frequency of RC oscillator is 32.768 kHz			-20%		+20%	
Note:The influence of this parameter should be taken into account, such as power sequence and Power on-off delay.						

Chapter 4 Function Description

4.1 State Machine Description

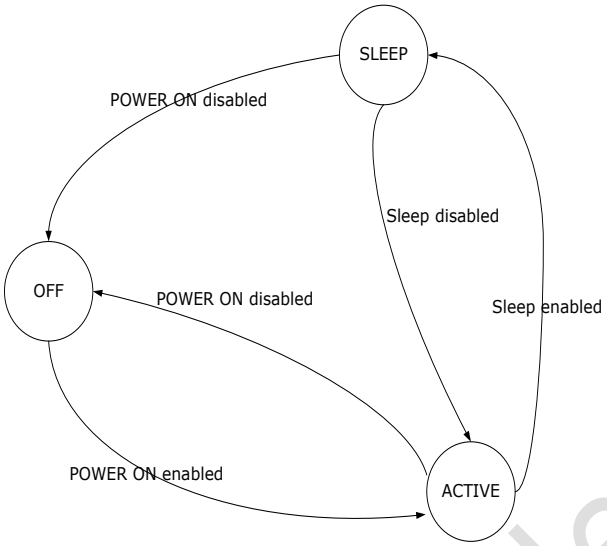


Fig. 4-1 State Machine

The RK801 state machine shown as above. The state shift by "power on", "power down", "reset", "active to sleep" and "sleep to active"

4.2 Device Power on Enable Conditions

- If none of the device power-on disable conditions is met, the following conditions are available to turn on the device:
  - VDC signal is high level.
  - PWRON signal keep low level at lease 500/20mS(+power on time add) while the device is off.

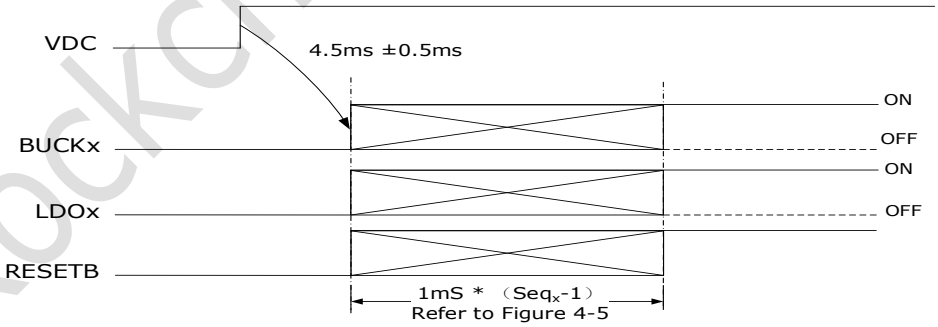


Fig. 4-2 VDC high level to turn on the PMIC

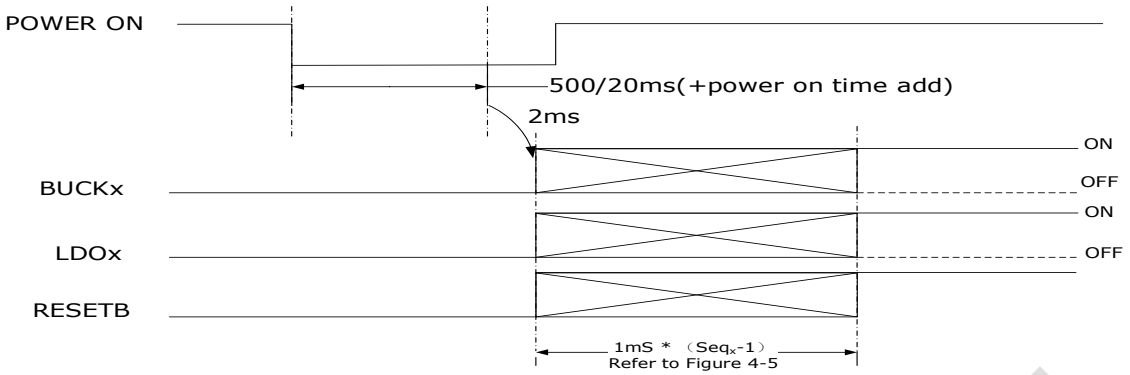
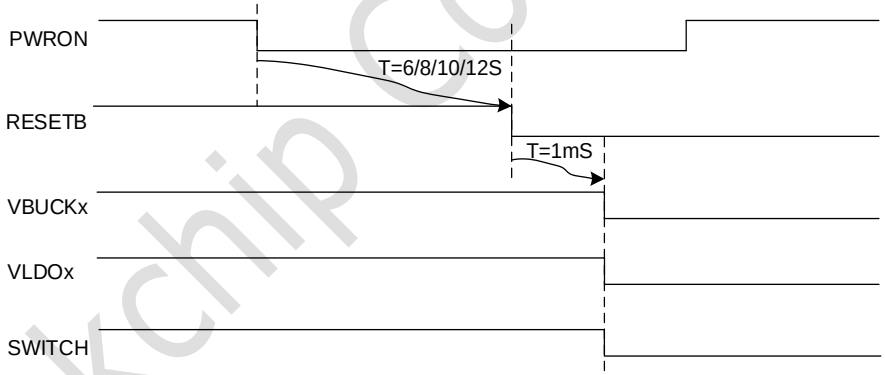


Fig. 4-3 POWER ON to turn on the PMIC

4.3 Device Power on Disable Conditions

- PWRON signal low level during more than the long-press delay: pwron_lp_off_time (POWERON_LP_ACT=0).
- Die temperature has reached the thermal shutdown threshold.
- VCCA down below VCCA_UV threshold.
- VCCH down below VCCH_UV threshold.
- VCCH higher than VCCH_OV threshold.
- PWRCTRL signal active, and Reg1A<1:0>=10
- DEV_OFF control bit set to 1.



Note:This label indicates the shutdown sequence in Default state. If the shutdown sequence is modified, the actual shutdown sequence is used

Fig. 4-4 Long press "PWRON" key to turn off the PMIC

4.4 Device Sleep Enable Conditions

- PWRCTRL signal high level and Reg20<1>=1, and Reg1A<1:0>=01.
- PWRCTRL signal low level and Reg50<1>=0, and Reg1A<1:0>=01.

4.5 Power Sequence

Power sequence			RK801-1	
	Output voltage range	Max output current	Default(V)	SEQ(*1mS)
BUCK1	0. 5V-1.5V （step 12.5mV)	3A	3.3	3

	/1.8V/2.2V/3.3V /5V/5.25V			
BUCK2	0.8V/0.85V/0.9V /1.8V/2.2V/2.3V	3A	5.25	1
BUCK3	setting by external resistors	1.5A	X	5
BUCK4	0. 5V-1.5V （step 12.5mV) /1.8V/2.2V/2.8V /3V/3.3V	2.5A	0.95	4
LDO1	0.5V-3.4V (step=50mV)	800mA	0.9	2
LDO2	0.5V-3.4V (step=50mV)	800mA	1.8	5
SWITCH		2A		6
RESETB				16

Fig. 4-5 RK801-1 power Start Up Sequence

X: The buck3 voltage is decided by external resistors. The RESETB is open drain output.

Power sequence			RK801-2	
	Output voltage range	Max output current	Default(V)	SEQ(*1mS)
BUCK1	0. 5V-1.5V （step 12.5mV) /1.8V/2.2V/3.3V /5V/5.25V	3A	0.95	2
BUCK2	0.8V/0.85V/0.9V /1.8V/2.2V/2.3V	3A	3.3	1
BUCK3	setting by external resistors	1.5A	X	3
BUCK4	0. 5V-1.5V （step 12.5mV) /1.8V/2.2V/2.8V /3V/3.3V	2.5A	0.90	2
LDO1	0.5V-3.4V (step=50mV)	800mA	0.9	2
LDO2	0.5V-3.4V (step=50mV)	800mA	1.8	3
SWITCH		2A		4
RESETB				16

Fig. 4-6 RK801-2 power Start Up Sequence

X: The buck3 voltage is decided by external resistors. The RESETB is open drain output.

4.6 Power Channels

4.6.1 Buck Description

The RK801 provides 2 channels HV synchronous buck converters and 2 channels LV synchronous buck converters, which deliver up to 3A, 1.5A and 2A respectively. An enhanced COT architecture is used, which improves the transient response significantly. 0.75MHz/2MHz switching frequency and good control method decrease the external inductance and capacitance. All output voltages can be adjusted dynamically during operation through DVS

(Dynamic Voltage Scaling), which guarantees a linear and gradual voltage ramping up and down. A complete set of protection functions, such as short circuit protection, is implemented in the buck converters too.

Meanwhile, bucks converters have good efficiency characteristics at AUTO mode. The test data is shown as below. All channels of buck output voltage set to default.

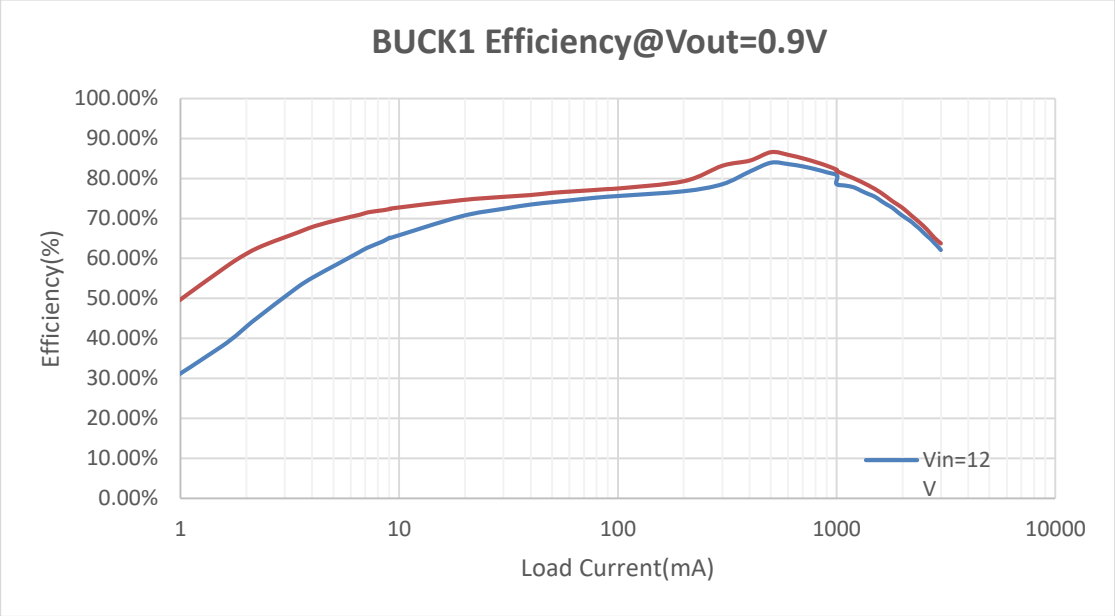


Fig. 4-7 BUCK1 for 0.9V output efficiency curve when different input voltage

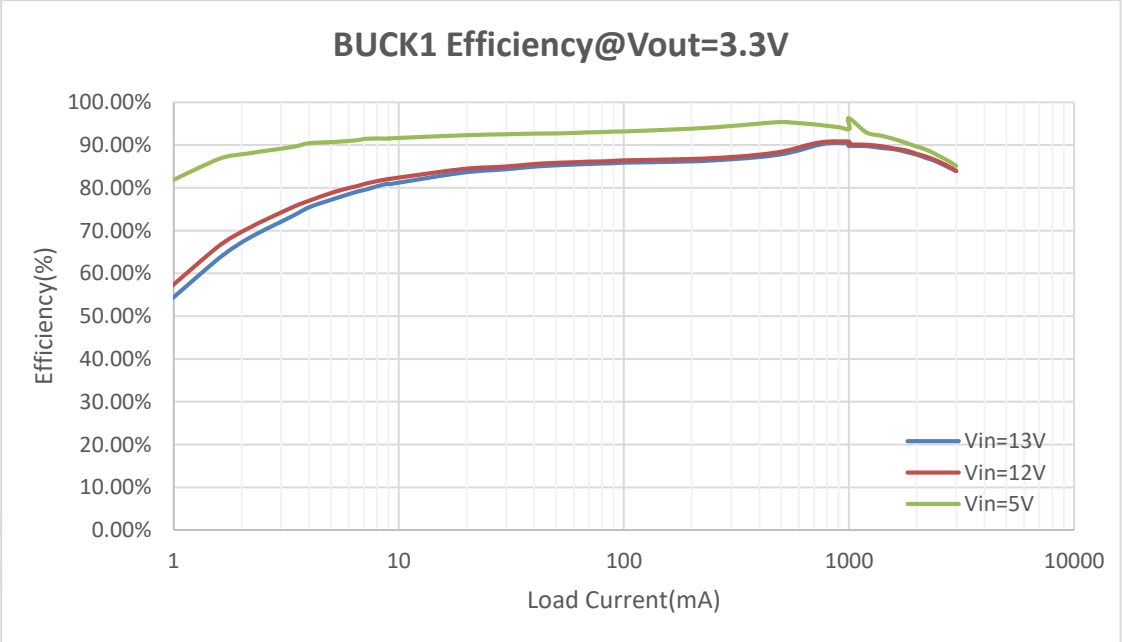


Fig. 4-8 BUCK1 for 3.3V output efficiency curve when different input voltage

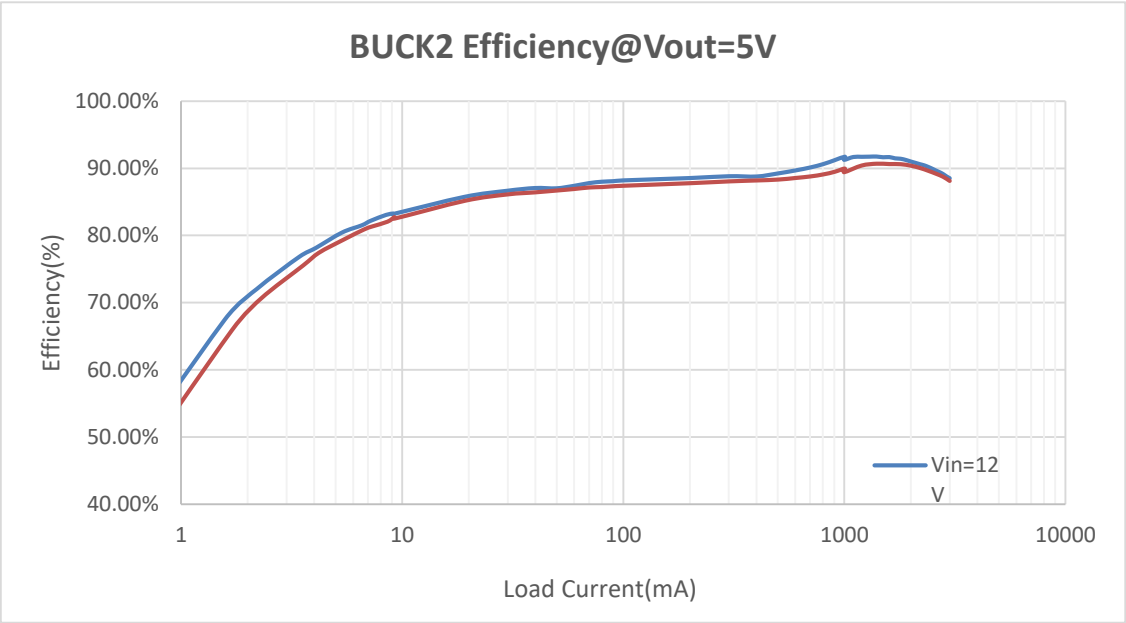


Fig. 4-9 BUCK2 for 5.0V output efficiency curve when different input voltage

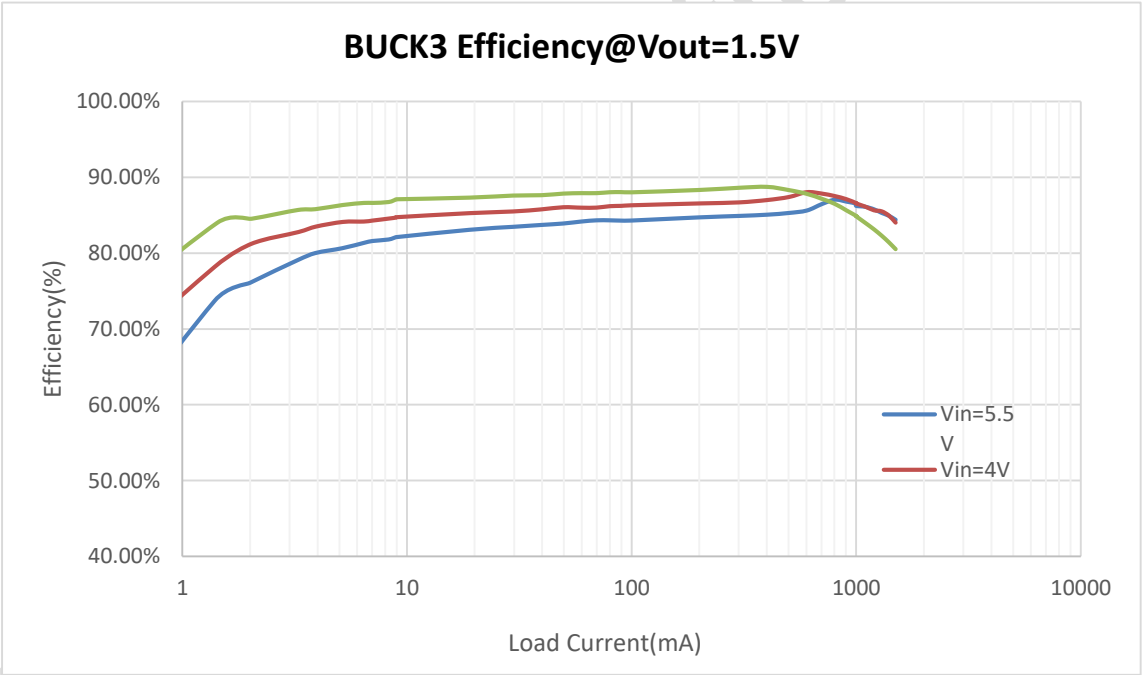


Fig. 4-10 BUCK3 for 1.5V output efficiency curve when different input voltage

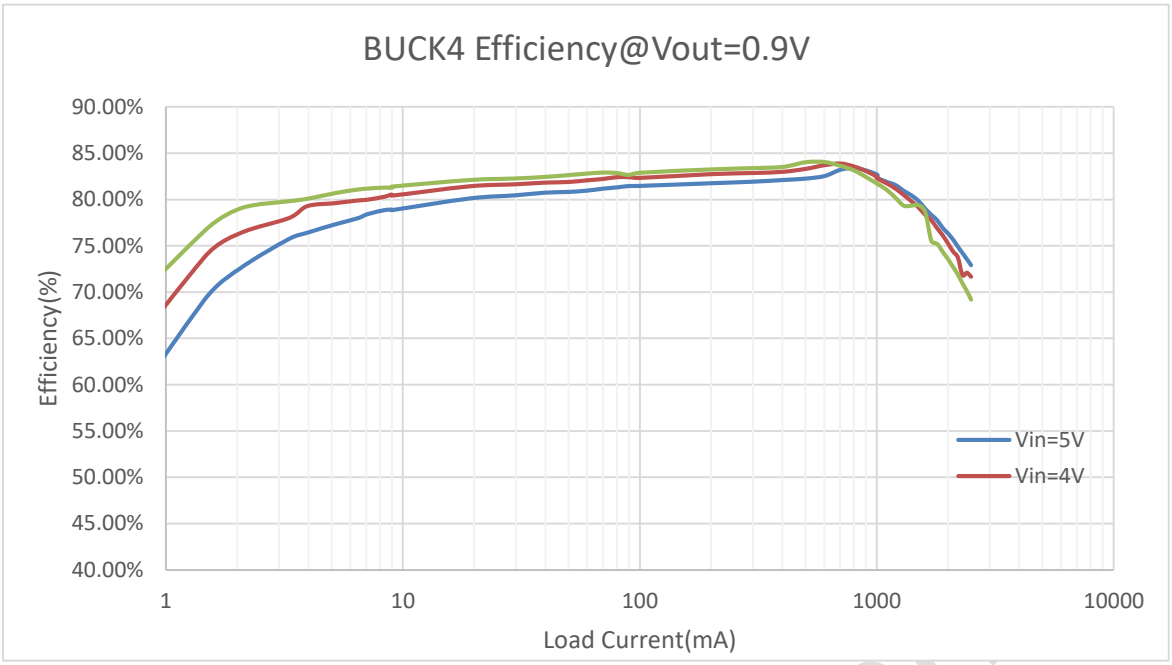


Fig. 4-11 BUCK4 for 0.9V output efficiency curve when different input voltage

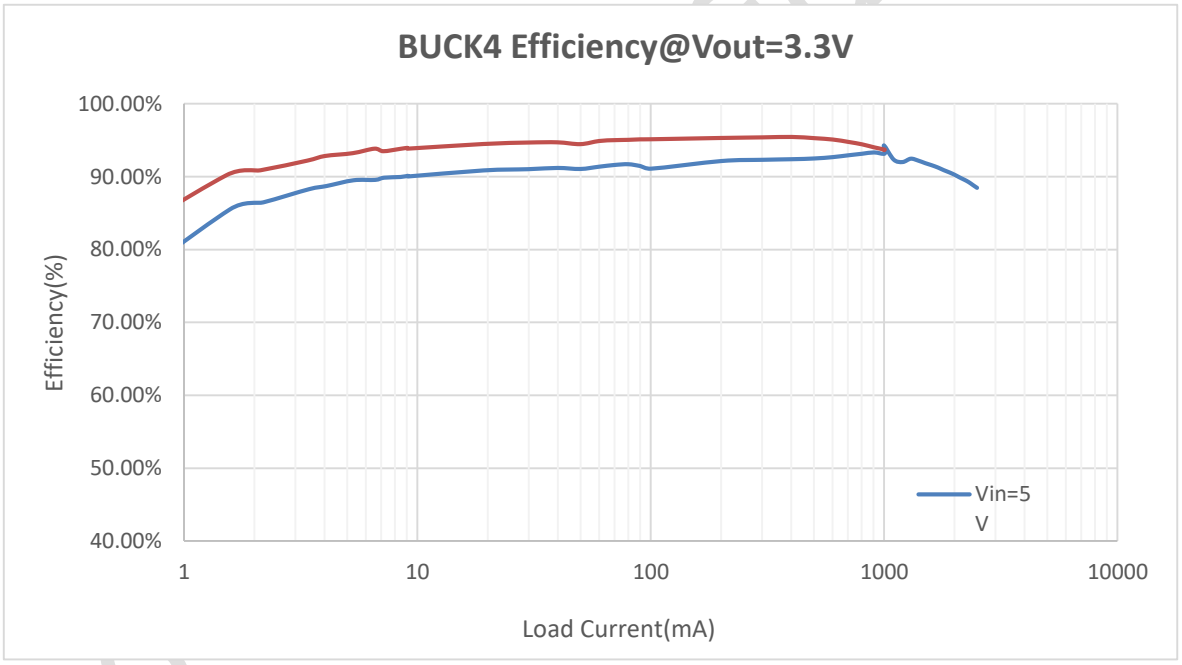


Fig. 4-12 BUCK4 for 3.3V output efficiency curve when different input voltage

4.6.2 LDO Description

The RK801 also integrates two LDO, that capable of providing up to 800mA . All channels of LDO output capacitance could be 1.0uF that decreases the system cost. The parameters such as output voltage in the different operating modes can be adjusted through the I^2C .

Chapter 5 Register Description

5.1 Register Summary

Name	Offset	Reset Value	Description
CHIP_NAME	0x00		
CHIP_VER	0x01		
OTP_VER	0x02	OTP	
POWER_EN0	0x03	OTP	Shutdown Reset
POWER_EN1	0x04	OTP	Shutdown Reset
POWER_SLP_EN	0x05	OTP	Shutdown Reset
POWER_FPWM_EN	0x06	OTP	Shutdown Reset:Bit3~Bit0 Por Reset:Bit6~Bit4
SLP_LP_CONFIG	0x07	OTP	Shutdown Reset:Bit3,Bit1 Por Reset:Bit7~Bit4
BUCK _CONFIG	0x08	OTP	Por Reset
BUCK1_ON_VSEL	0x09	0x20	Shutdown Reset
BUCK2_ON_VSEL	0x0a	0x06	Shutdown Reset
BUCK4_ON_VSEL	0x0b	0x56	Shutdown Reset
LDO1_ON_VSEL	0x0c	0x08	Shutdown Reset
LDO2_ON_VSEL	0x0d	0x1A	Shutdown Reset
BUCK1_SLP_VSEL	0x0e	0x20	Shutdown Reset
BUCK2_ SLP _VSEL	0x0F	0x06	Shutdown Reset
BUCK4_ SLP _VSEL	0x10	0x56	Shutdown Reset
LDO1_ SLP _VSEL	0x11	0x08	Shutdown Reset
LDO2_ SLP _VSEL	0x12	0x1A	Shutdown Reset
LDO_ SW _IMAX	0x13	0x00	Shutdown Reset
SYS_STS	0x14	0x00	Por Reset
SYS_CFG0	0x15	0x00	Por Reset
SYS_CFG1	0x16	0x00	Por Reset
SYS_CFG2	0x17	0x00	Shutdown Reset
SYS_CFG3	0x18	0x00	Por Reset
SYS_CFG4	0x19	0x00	Por Reset
SLEEP_CFG	0x1A	0x00	Shutdown Reset
ON_SOURCE	0x1B	0x00	
OFF_SOURCE	0x1C	0x00	
PWRON_KEY	0x1D	0x00	Por Reset
INT_STS0	0x1E	0x00	Por Reset
INT_MASK0	0x1F	0x00	Por Reset
INT_CONFIG	0x20	0x00	Shutdown Reset
CON_BACK1	0x21	0x00	Por Reset
CON_BACK2	0x22	0x00	Shutdown Reset
DATA_CON0	0x23	0x00	Por Reset
DATA_CON1	0x24	0x00	Por Reset
DATA_CON2	0x25	0x00	Por Reset
DATA_CON3	0x26	0x00	Por Reset
POWER_EXIT_SLP_SEQ0	0x27	0x00	Shutdown Reset
POWER_EXIT_SLP_SEQ1	0x28	0x00	Shutdown Reset
POWER_EXIT_SLP_SEQ2	0x29	0x00	Shutdown Reset
POWER_EXIT_SLP_SEQ3	0x2A	0x00	Shutdown Reset

Name	Offset	Reset Value	Description
POWER_ENTER_SLEEP_OR_SHOUTDOWN_SEQ0	0x2B	0x00	Por Reset
POWER_ENTER_SLEEP_OR_SHOUTDOWN_SEQ1	0x2C	0x00	Por Reset
POWER_ENTER_SLEEP_OR_SHOUTDOWN_SEQ2	0x2D	0x00	Por Reset
POWER_ENTER_SLEEP_OR_SHOUTDOWN_SEQ3	0x2E	0x00	Por Reset
BUCK_DEBUG6	0x34	0x00	Por Reset

Note: Por Reset indicates power-on reset or undervoltage reset.

5.2 Register Description

CHIP_NAME
Address: (0x00)

Bit	Attr	Reset Value	Description
7:0	RO	0x80	CHIP_NAME CHIP_NAME[11:4]: RK801

CHIP_VER
Address: (0x01)

Bit	Attr	Reset Value	Description
7:4	RO	0x01	CHIP_NAME CHIP_NAME[3:0]: RK801
3:0	RO	0x0	CHIP_VER CHIP_VER: CHIP version

OTP_VER
Address: (0x02)

Bit	Attr	Reset Value	Description
7:4	NA	0x0	RESV RESV: Reserve
3:0	RO	0x0	OTP_VER CHIP_VER: OTP version

POWER_EN0
Address: (0x03)

Bit	Attr	Reset Value	Description
7	W1C	0x0	BUCK3_EN_MASK BUCK3_EN_MASK: MUST write them to "1" if want to change corresponding BUCK3_EN bit，and BUCK3_EN_MASK bits auto clear after Written.

Bit	Attr	Reset Value	Description
6	W1C	0x0	BUCK4_EN_MASK BUCK4_EN_MASK: MUST write them to "1" if want to change corresponding BUCK4_EN bit，and BUCK4_EN_MASK bits auto clear after Written.
5	W1C	0x0	BUCK2_EN_MASK BUCK2_EN_MASK: MUST write them to "1" if want to change corresponding BUCK2_EN bit，and BUCK2_EN_MASK bits auto clear after Written.
4	W1C	0x0	BUCK1_EN_MASK BUCK1_EN_MASK: MUST write them to "1" if want to change corresponding BUCK1_EN bit，and BUCK1_EN_MASK bits auto clear after Written.
3	RW	OTP	BUCK3_EN BUCK3_EN: BUCK3 enable in active mode 1, Enable 0, Disable the default value is set by OTP
2	RW	OTP	BUCK4_EN BUCK4_EN: BUCK4 enable in active mode 1, Enable 0, Disable the default value is set by OTP
1	RW	OTP	BUCK2_EN BUCK2_EN: BUCK2 enable in active mode 1, Enable 0, Disable the default value is set by OTP
0	RW	OTP	BUCK1_EN BUCK1_EN: BUCK1 enable in active mode 1, Enable 0, Disable the default value is set by OTP

POWER_EN1
Address: (0x04)

Bit	Attr	Reset Value	Description
7	NA	0x0	RESV RESV: Reserve
6	W1C	0x0	SW_EN_MASK SW_EN_MASK: MUST write them to "1" if want to change corresponding SW_EN bit，and SW_EN_MASK bits auto clear after Written.
5	W1C	0x0	LDO2_EN_MASK LDO2_EN_MASK: MUST write them to "1" if want to change corresponding LDO2_EN bit，and LDO2_EN_MASK bits auto clear after Written.
4	W1C	0x0	LDO1_EN_MASK LDO1_EN_MASK: MUST write them to "1" if want to change corresponding LDO1_EN bit，and LDO1_EN_MASK bits auto clear after Written.
3	RW	0x0	RESV RESV: Reserve
2	RW	OTP	SW_EN SW_EN: SW enable in active mode 1, Enable 0, Disable the default value is set by OTP
1	RW	OTP	LDO2_EN LDO2_EN: LDO2 enable in active mode 1, Enable 0, Disable the default value is set by OTP
0	RW	OTP	LDO1_EN LDO1_EN: LDO1 enable in active mode 1, Enable 0, Disable the default value is set by OTP

POWER_SLEEP_EN
Address: (0x05)

Bit	Attr	Reset Value	Description
7	RW	OTP	RESV RESV: Reserve
6	RW	OTP	SW_SLP_EN SW_SLP_EN: SW enable in SLEEP mode 1, Enable 0, Disable

Bit	Attr	Reset Value	Description
5	RW	OTP	LDO2_SLP_EN LDO2_SLP_EN: LDO2 enable in SLEEP mode 1, Enable 0, Disable
4	RW	OTP	LDO1_SLP_EN LDO1_SLP_EN: LDO1 enable in SLEEP mode 1, Enable 0, Disable
3	RW	OTP	BUCK3_SLP_EN BUCK3_SLP_EN: BUCK3 enable in SLEEP mode 1, Enable 0, Disable
2	RW	OTP	BUCK4_SLP_EN BUCK4_SLP_EN: BUCK4 enable in SLEEP mode 1, Enable 0, Disable
1	RW	OTP	BUCK2_SLP_EN BUCK2_SLP_EN: BUCK2 enable in SLEEP mode 1, Enable 0, Disable
0	RW	OTP	BUCK1_SLP_EN BUCK1_SLP_EN: BUCK1 enable in SLEEP mode 1, Enable 0, Disable

POWER_FPWM_EN
Address: (0x06)

Bit	Attr	Reset Value	Description
7	NA	0x0	RESV RESV: Reserve
6	RW	0x0	LDO_HRDEC_EN LDO_HRDEC_EN:Low voltage difference application under light no-load condition, when the input and output low voltage difference, control the standby current enable 0: disable 1:enable
5:4	RW	0x0	LDO_RLOAD_SEL[1:0] LDO_RLOAD_SEL[1:0]:False load channel of LDO selection 00:0uA 01：20uA 10:200uA 11:1.6mA Note：The output Voltage of LDO is 0.5V

Bit	Attr	Reset Value	Description
3	RW	0x0	BUCK3_FPWM BUCK3_FPWM: BUCK3 Forced PWM mode selection 1, Forced PWM mode in active mode; 0, PWM/PFM auto change mode
2	RW	0x0	BUCK4_FPWM BUCK4_FPWM: BUCK4 Forced PWM mode selection 1, Forced PWM mode in active mode; 0, PWM/PFM auto change mode
1	RW	0x0	BUCK2_FPWM BUCK2_FPWM: BUCK2 Forced PWM mode selection 1, Forced PWM mode in active mode; 0, PWM/PFM auto change mode
0	RW	0x0	BUCK1_FPWM BUCK1_FPWM: BUCK1 Forced PWM mode selection 1, Forced PWM mode in active mode; 0, PWM/PFM auto change mode

SLP_LP_CONFIG
Address: (0x07)

Bit	Attr	Reset Value	Description
7	RW	0x0	BUCK3_CMIN_MAXON BUCK3_CMIN_MAXON: When BUCK3 cmin is triggered, The PMOS is forced to turn on time. 0 : 2.5uS 1: 5uS
6	RW	0x0	BUCK4_CMIN_MAXON BUCK4_CMIN_MAXON: When BUCK4 cmin is triggered, The PMOS is forced to turn on time. 0 : 2.5uS 1: 5uS
5:4	RW	0x0	RESV RESV: Reserve
3	RW	0x0	BUCK_SLP_LP_EN BUCK_SLP_LP_EN: Low power function enable bit of BUCK. (SLEEP mode) 0: disable 1:enable
2	NA	0x0	RESV RESV: Reserve
1	RW	0x0	LDO_SLP_LP_EN LDO_SLP_LP_EN: Low power function enable bit of LDO. (SLEEP mode) 0: disable 1:enable

Bit	Attr	Reset Value	Description
0	NA	0x0	RESV RESV: Reserve

BUCK_CONFIG
Address: (0x08)

Bit	Attr	Reset Value	Description
7:6	RW	0x01	BUCK3_ILVL[1:0] BUCK3_ILVL ： BUCK3 inductive current limit select 00:1.4A 01:1.8A 10:2.3A 11:2.7A
5:4	RW	0x01	BUCK4_ILVL[1:0] BUCK4_ILVL ： BUCK4 inductive current limit select 00:2.3A 01:2.8A 10:3.2A 11:3.7A
3:2	RW	0x01	BUCK2_ILVL[1:0] BUCK2_ILVL ： BUCK2 inductive current limit select 00:2.4A 01:3.2A 10:3.6A 11:4A
1:0	RW	0x01	BUCK1_ILVL[1:0] BUCK1_ILVL ： BUCK1 inductive current limit select 00:2.4A 01:3.2A 10:3.6A 11:4A

BUCK1_ON_VSEL
Address: (0x09)

Bit	Attr	Reset Value	Description
7	RW	0x0	RESV RESV: Reserve
6:0	RW	OTP	BUCK1_ON_VSEL[6:0] BUCK1_ON_VSEL: BUCK1 active mode voltage select, 0.5V~1.5V(step=12.5mV)/1.8V/2.2V/3.3V/5.0V/5.25V, the detail bits decode shown in the sheet called "Decode" the default value is set by boot

BUCK2_ON_VSEL
Address: (0x0A)

Bit	Attr	Reset Value	Description
7	RW	0x0	RESV RESV: Reserve

Bit	Attr	Reset Value	Description
6:0	RW	OTP	BUCK2_ON_VSEL[6:0] BUCK2_ON_VSEL: BUCK2 active mode voltage select, 0.8V/0.85V/0.9V/1.8V/2.2V/3.3V/5.0V/5.25V the detail bits decode shown in the sheet called "Decode" the default value is set by boot

BUCK4_ON_VSEL
Address: (0x0B)

Bit	Attr	Reset Value	Description
7	NA	0x0	RESV RESV: Reserve
6:0	RW	OTP	BUCK4_ON_VSEL[6:0] BUCK4_ON_VSEL: BUCK4 active mode voltage select, 0.5V~1.5V(step=12.5mV)/1.8V/2.2V/2.5V/2.8V/3V/3.3V, the detail bits decode shown in the sheet called "Decode" the default value is set by boot

LDO1_ON_VSEL
Address: (0x0C)

Bit	Attr	Reset Value	Description
7:6	NA	0x0	RESV RESV: Reserve
5:0	RW	OTP	LDO1_ON_VSEL[6:0] LDO1_ON_VSEL: LDO1 active mode voltage select, 0.5V~3.4V(step=50mV) the detail bits decode shown in the sheet called "Decode" the default value is set by boot

LDO2_ON_VSEL
Address: (0x0D)

Bit	Attr	Reset Value	Description
7:6	NA	0x0	RESV RESV: Reserve
5:0	RW	OTP	LDO2_ON_VSEL[6:0] LDO2_ON_VSEL: LDO2 active mode voltage select, 0.5V~3.4V(step=50mV) the detail bits decode shown in the sheet called "Decode" the default value is set by boot

BUCK1_SLP_VSEL
Address: (0x0E)

Bit	Attr	Reset Value	Description
7	RW	0x0	RESV RESV: Reserve
6:0	RW	OTP	BUCK1_SLP_VSEL[6:0] BUCK1_SLP_VSEL: BUCK1 sleep mode voltage select, 0.5V~1.5V(step=12.5mV)/1.8V/2.2V/3.3V/5.0V/5.25V, the detail bits decode shown in the sheet called "Decode" the default value is set by boot

BUCK2_SLP_VSEL
Address: (0x0A)

Bit	Attr	Reset Value	Description
7	NA	0x0	RESV RESV: Reserve
6:0	RW	OTP	BUCK2_SLP_VSEL[6:0] BUCK2_SLP_VSEL: BUCK2 sleep mode voltage select, 0.8V/0.85V/0.9V/1.8V/2.2V/3.3V/5.0V/5.25V the detail bits decode shown in the sheet called "Decode" the default value is set by boot

BUCK4_SLP_VSEL
Address: (0x010)

Bit	Attr	Reset Value	Description
7	NA	0x0	RESV RESV: Reserve
6:0	RW	OTP	BUCK4_SLP_VSEL[6:0] BUCK4_SLP_VSEL: BUCK4 sleep mode voltage select, 0.5V~1.5V(step=12.5mV)/1.8V/2.2V/2.5V/2.8V/3V/3.3V, the detail bits decode shown in the sheet called "Decode" the default value is set by boot

LDO1_SLP_VSEL
Address: (0x11)

Bit	Attr	Reset Value	Description
7:6	NA	0x0	RESV RESV: Reserve
5:0	RW	OTP	LDO1_SLP_VSEL[6:0] LDO1_SLP_VSEL: LDO1 sleep mode voltage select, 0.5V~3.4V(step=50mV) the detail bits decode shown in the sheet called "Decode" the default value is set by boot

LDO2_SLP_VSEL
Address: (0x12)

Bit	Attr	Reset Value	Description
7:6	NA	0x0	RESV RESV: Reserve
5:0	RW	OTP	LDO2_SLP_VSEL[6:0] LDO2_SLP_VSEL: LDO2 sleep mode voltage select, 0.5V~3.4V(step=50mV) the detail bits decode shown in the sheet called "Decode" the default value is set by boot

LDO_SW_IMAX
Address: (0x13)

Bit	Attr	Reset Value	Description
7:3	NA	0x0	RESV RESV: Reserve
2	RW	0x0	SW_IMAX SW_IMAX: SW current limit setting 0: normal, 1: 130% of normal value
1	RW	0x0	LDO2_IMAX LDO2_IMAX&SW_IMAX: LDO2 current limit setting 0: normal, 1: 130% of normal value
0	RW	0x0	LDO1_IMAX LDO1_IMAX&SW_IMAX: LDO1 current limit setting 0: normal, 1: 130% of normal value

SYS_STS
Address: (0x14)

Bit	Attr	Reset Value	Description
7:5	RW	0x0	RESV RESV: Reserve

Bit	Attr	Reset Value	Description
4	RO	0x0	VLV_BUCK_UV VLV_BUCK_UV：Low buck input under voltage status bit
3	RO	0x0	TSD_STS TSD_STS：Thermal shut down
2	RO	0x0	HOTDIE_STS HOTDIE_STS：Hot-die warning
1	RO	0x0	VDC_STS VDC_STS： 0:low level; 1:high level
0	RO	0x0	POWERON_STS POWERON_STS：PWRON key status 0: PWRON not press 1:PWRON button pressed

SYS_CFG0
Address: (0x15)

Bit	Attr	Reset Value	Description
7	RW	0x0	VCCHV_OV_SEL VCCHV_OV_SEL: system shut down voltage select 0: 14.4v(default)；1: 13.5v
6	RW	0x0	VCCHV_UV_DLY VCCHV_UV_DLY: system shut down delay 0: :3.0us(default)；1: 10us
5	RW	0x0	VCCA_UV_SEL VCCA_UV_SEL: system shut down voltage select 0: :3.6V(default) 1:3.3V
4	RW	0x0	VCCA_UV_DLY VCCA_UV_DLY: system shut down delay 0: :3.0us(default)；1: 10us
3	RW	0x0	VCCLV_UV_SEL VCCLV_UV_SEL: BUCK3/BUCK4 shut down voltage select 0：2.6v(default)；1：2,8v
2	RW	0x0	VCCLV_UV_DLY VCCLV_UV_DLY: system shut down delay 0: :3.0us(default)；1: 10us
1	RW	0x0	RESV RESV: Reserve

Bit	Attr	Reset Value	Description
0	RW	0x0	HVLDO_DISABLE HVLDO_DISABLE: HVLDO EN 0: Enable 1: Disable (When the input VSYS is 5V, the VCCA should connected to the external 5V power supply and the internal high voltage LDO is turned off)

SYS_CFG1
Address: (0x16)

Bit	Attr	Reset Value	Description
7	RW	0x0	VCCHV_OV_DLY VCCHV_OV_DLY: VCCHV_OV comparator delay time selection 0：3.5us 1：10us
6:3	RW	0x0	RESV RESV: Reserve
2	RW	0x1	TSD_TEMP TSD_TEMP: Thermal shutdown temperature threshold 0: 140℃; 1: 160℃
1:0	RW	0x10	HOT_DIE_TEMP_SEL[1:0] HOT_DIE_TEMP_SEL: Hot-die temperature threshold 00:85℃ 01:95℃ 10:105℃ 11:115℃

SYS_CFG2
Address: (0x17)

Bit	Attr	Reset Value	Description
7	RW	0x0	BUCK _SST BUCK _SST: BUCKn soft start time for 0V to 1V BUCK1/2 0:620uS 1:310uS BUCK3/4 0:480uS 1:240uS
6	RW	0x0	RESV RESV: Reserve

Bit	Attr	Reset Value	Description
5:4	RW	0x0	RST_FUN RST_FUN: 00：restart PMU 01: Reset all the power off reset registers, forcing th e state to switch to ACTIVE mode 1X： Reset all the power off reset registers, forcing th e state to switch to ACTIVE mode, and simultan eously pull down the RESETB PIN for 5mS befor e releasing
3	RW	0x0	DEV_RST DEV_RST: Write 1 will Reset PMIC，the reset mode is determined by RST_FUN (RST_FUN: two ways to trigger reset mode ： 1）DEV_RST write 1；2）PWRCTRL PIN effect and PWRCTRL_FUNC=11; 3)RESETB low
2	RW	0x0	RESV RESV: Reserve
1	RW	0x1	SLP_POL SLP_POL: sleep pin polarity 0: active low 1: active high
0	RW	0x0	DEV_OFF DEV_OFF: Write 1 will start an ACTIVE to OFF or SLEEP to OFF device state transition (switch-off event). This bit is cleared in OFF state.

SYS_CFG3
Address: (0x18)

Bit	Attr	Reset Value	Description
7	RW	0x0	RESV RESV: Reserve
6	RW	0x0	BK_LDO_3V_EN BK_LDO_3V_EN: Low power function enable bit of 3VLDO 0: disable 1:enable
5	RW	0x0	VCCHV_UV_SEL VCCHV_UV_SEL:VCCH low voltage threshold 0:4.2V 1:6V
4	RW	0x0	RESV RESV: Reserve

Bit	Attr	Reset Value	Description
3	RW	OTP	POWERON_TIME POWERON_TIME:time to push power botton th en system on 0:500ms 1:20ms
2	RW	0x0	RESV RESV: Reserve
1	RW	0x0	OSC_1M_BUCK4 OSC_1M_BUCK4: The operating frequency of BUCK4 is down to 1M 0: disable 1:enable
0	RW	0x0	OSC_1M_BUCK3 OSC_1M_BUCK3: The operating frequency of BUCK3 is down to 1M 0: disable 1:enable

SYS_CFG4
Address: (0x19)

Bit	Attr	Reset Value	Description
7:3	NA	0x0	RESV RESV: Reserve
2:0	RW	0x0	POWERON_TIME_ADD POWERON_TIME_ADD : POWERON_TIME Time of OTP setting plus the time of this register setting 000:0mS(default)；001：20ms；010:100ms，011:500ms；100:1000ms；101:1500ms，110:2000ms；111：3000ms；

SLEEP_CFG
Address: (0x1A)

Bit	Attr	Reset Value	Description
7:2	RW	0x0	RESV RESV: Reserve
1:0	RW	0x0	PWRCTRL_FUNC: PWRCTRL PIN function selection 00: not effect; 01: sleep function; 10: shutdown function; 11: restart PMU function.

ON_SOURCE
Address: (0x1B)

Bit	Attr	Reset Value	Description
7	NA	0x0	RESV RESV: Reserve
6	RO	0x0	PWRON ON_PWRON:PRESS PWRON to turn on PMU
5	RO	0x0	ON_VDC ON_VDC:VDC set high to turn on PMU
4	NA	0x0	RESV RESV: Reserve
3	RO	0x0	RESTART_RESETB RESTART_RESETB:PULL LOW the RESETB to restart the PMU
2	RO	0x0	RESTART_PWRON_LP RESTART_PWRON_LP: Long press PWRON to restart the PMU
1	RO	0x0	RESTART_SLP RESTART_SLP:PWRCTRL PIN ACTIVE to restart the PMU
0	RO	0x0	RESTART_DEV_RST RESTART_DEV_RST:DEV_RST Set 1 and RST_FUN=00 to restart the PMU

OFF_SOURCE
Address: (0x1C)

Bit	Attr	Reset Value	Description
7	RO	0x0	OFF_SLP OFF_SLP: PWRCTRL PIN ACTIVE to turn off PMU
6	RO	0x0	OFF_TSD OFF_TSD:TSD to turn off PMU
5	RO	0x0	DEV_OFF OFF_DEV_OFF:I2C write DEV_OFF to turn off PMU
4	RO	0x0	PWRON_LP OFF_PWRON_LP: long press PWRON to turn off PMU
3	RO	0x0	OFF_OV OFF_OV:VCCH OV to turn off PMU
2	RO	0x0	VCCHV_UV VCCHV_UV: VCCHV_UV to turn off PMU
1	RO	0x0	VCCA_UV VCCA_UV: VCCHV_UV to turn off PMU
0	RO	0x0	RESV RESV: Reserve

PWRON_KEY

Address: (0x1D)

Bit	Attr	Reset Value	Description
7	NA	0x0	RESV RESV: Reserve
6	RW	0x0	POWERON_LP_ACT PWRON_LP_ACT: PWRON long press act 0: turn off 1: turn off and then restart
5:4	RW	0x0	PWRON_LP_OFF_TIME PWRON_LP_OFF_TIME: PWRON long press time 00: 6s, 01: 8s, 10: 10s, 11: 12s
3:2	RW	0x01	PWRON_LP_TM_SEL PWRON_LP_TM_SEL<1:0>:PWRON long press interrupt time selection 00: 0.5S 01:1S 10:1.5S 11:2S
1:0	RW	0x10	POWERON_DB_SEL PWRON_DB_SEL<1:0>:PWRON FALL interrupt debounce time selection 00: 32uS 01:10mS 10:20mS 11:40mS

INT_STS0
Address: (0x1E)

Bit	Attr	Reset Value	Description
7	NA	0x0	RESV RESV: Reserve
6	W1C	0x0	VDC_FALL_INT VDC_FALL_INT:VDC falling event interrupt
5	W1C	0x0	VDC_RISE_INT VDC_RISE_INT: VDC rising event interrupt
4	W1C	0x0	HOTDIE_INT HOTDIE_INT: Hot die event interrupt status
3	W1C	0x0	POWERON_LP_INT POWERON_LP_INT:POWERON PIN long press event interrupt status
2	W1C	0x0	POWERON_INT POWERON_INT: PWRON event interrupt status when Press the POWERON key in the shutdown state.
1	W1C	0x0	POWERON_RISE_INT POWERON_RISE_INT: POWERON rising event interrupt
0	W1C	0x0	POWERON_FALL_INT POWERON_FALL_INT: POWERON falling event interrupt

INT_MASK0
Address: (0x1F)

Bit	Attr	Reset Value	Description
7	NA	0x0	RESV RESV: Reserve
6	RW	0x0	VDC_FALL_INT_MASK 0:Do not mask interrupt 1: mask VDC falling event interrupt
5	RW	0x0	VDC_RISE_INT_MASK 0:Do not mask interrupt 1: mask VDC rising event interrupt
4	RW	0x0	HOTDIE_INT_MASK 0:Do not mask interrupt 1: mask Hot die event interrupt
3	RW	0x0	POWERON_LP_INT_MASK 0:Do not mask interrupt 1: mask PWRON PIN long press event interrupt
2	RW	0x0	POWERON_INT_MASK 0:Do not mask interrupt 1: mask PWRON event interrupt
1	RW	0x0	POWERON_RISE_INT_MASK 0:Do not mask interrupt 1: mask PWRON rising event interrupt
0	RW	0x0	POWERON_FALL_INT_MASK 0:Do not mask interrupt 1: mask PWRON falling event interrupt0:Do not mask interrupt 1: mask PWRON PIN long press event interrupt

INT_CONFIG
Address: (0x20)

Bit	Attr	Reset Value	Description
7:2	NA	0x0	RESV RESV: Reserve
1	RW	0x1	INT_POL INT_POL: INT pin polarity 0: active low 1: active high
0	RW	0x0	INT_FUNCTION INT_FUNCTION: interrupt watchdog function select 0: exit interrupt 1: exit interrupt and exit sleep mode

POWER_EXIT_SLP_SEQ0
Address: (0x27)

Bit	Attr	Reset Value	Description
7:6	NA	0x0	RESV RESV: Reserve
5：3	RW	0x0	BUCK2_EXIT_SLP_SEQ BUCK2_EXIT_SLP_SEQ：BUCK2 exit SLEEP mode sequence,1MS/2MS/4MS by OTP programmed for 1 step
2：0	RW	0x0	BUCK1_EXIT_SLP_SEQ BUCK1_EXIT_SLP_SEQ：BUCK1 exit SLEEP mode sequence,1MS/2MS/4MS by OTP programmed for 1 step

POWER_EXIT_SLP_SEQ1
Address: (0x28)

Bit	Attr	Reset Value	Description
7:6	NA	0x0	RESV RESV: Reserve
5：3	RW	0x0	BUCK3_EXIT_SLP_SEQ BUCK3_EXIT_SLP_SEQ：BUCK3 exit SLEEP mode sequence,1MS/2MS/4MS by OTP programmed for 1 step
2：0	RW	0x0	BUCK4_EXIT_SLP_SEQ BUCK4_EXIT_SLP_SEQ：BUCK4 exit SLEEP mode sequence,1MS/2MS/4MS by OTP programmed for 1 step

POWER_EXIT_SLP_SEQ2
Address: (0x29)

Bit	Attr	Reset Value	Description
7:6	NA	0x0	RESV RESV: Reserve
5：3	RW	0x0	LDO2_EXIT_SLP_SEQ LDO2_EXIT_SLP_SEQ：LDO2 exit SLEEP mode sequence,1MS/2MS/4MS by OTP programmed for 1 step
2：0	RW	0x0	LDO1_EXIT_SLP_SEQ LDO1_EXIT_SLP_SEQ：LDO1 exit SLEEP mode sequence,1MS/2MS/4MS by OTP programmed for 1 step

POWER_EXIT_SLP_SEQ3
Address: (0x2A)

Bit	Attr	Reset Value	Description
7:3	NA	0x0	RESV RESV: Reserve
2：0	RW	0x0	SW_EXIT_SLP_SEQ SW_EXIT_SLP_SEQ：SW exit SLEEP mode sequence,1MS/2MS/4MS by OTP programmed for 1 step

POWER_ENTER_SLP_OR_SHUTDOWN_SEQ0
Address: (0x2B)

Bit	Attr	Reset Value	Description
7:6	NA	0x0	RESV RESV: Reserve
5：3	RW	0x0	BUCK2_SLP_SHUTDOWN_SEQ BUCK2_SLP_SHUTDOWN_SEQ：BUCK2 enter SLEEP mode and shutdown sequence, 1MS/2MS/4MS by OTP programmed for 1 step
2：0	RW	0x0	BUCK1_SLP_SHUTDOWN _SEQ BUCK1_SLP_SHUTDOWN _SEQ：BUCK1 enter SLEEP mode and shutdown sequence, 1MS/2MS/4MS by OTP programmed for 1 step

POWER_ENTER_SLP_OR_SHUTDOWN_SEQ1
Address: (0x2C)

Bit	Attr	Reset Value	Description
7:6	NA	0x0	RESV RESV: Reserve
5：3	RW	0x0	BUCK3_SLP_SHUTDOWN_SEQ BUCK3_SLP_SHUTDOWN_SEQ：BUCK3 enter SLEEP mode and shutdown sequence, 1MS/2MS/4MS by OTP programmed for 1 step
2：0	RW	0x0	BUCK4_SLP_SHUTDOWN _SEQ BUCK4_SLP_SHUTDOWN _SEQ：BUCK4 enter SLEEP mode and shutdown sequence, 1MS/2MS/4MS by OTP programmed for 1 step

POWER_ENTER_SLP_OR_SHUTDOWN_SEQ2
Address: (0x2D)

Bit	Attr	Reset Value	Description
7:6	NA	0x0	RESV RESV: Reserve
5：3	RW	0x0	LDO2_SLP_SHUTDOWN_SEQ LDO2_SLP_SHUTDOWN_SEQ：LDO2 enter SLEEP mode and shutdown sequence, 1MS/2MS/4MS by OTP programmed for 1 step

Bit	Attr	Reset Value	Description
2：0	RW	0x0	LDO1_SLP_SHUTDOWN _SEQ LDO1_SLP_SHUTDOWN _SEQ：LDO1 enter SLEEP mode and shutdown sequence, 1MS/2MS/4MS by OTP programmed for 1 step

POWER_ENTER_SLP_OR_SHUTDOWN_SEQ3
Address: (0x2E)

Bit	Attr	Reset Value	Description
7:3	NA	0x0	RESV RESV: Reserve
2：0	RW	0x0	SW_SLP_SHUTDOWN _SEQ SW_SLP_SHUTDOWN _SEQ：SW enter SLEEP mode and shutdown sequence, 1MS/2MS/4MS by OTP programmed for 1 step

BUCK_DEBUG6
Address: (0x34)

Bit	Attr	Reset Value	Description
7:6	NA	0x0	RESV RESV: Reserve
5	RW	0x0	BUCK3_CMIN_ENB BUCK3_CMIN_ENB:BUCK3 min Current limit enable 0: Enable 1:Disable
4:3	RW	0x01	BUCK3_CMIN_SEL BUCK3_CMIN_SEL:BUCK3 min Current limit select 00:250mA 01:375mA 10:480mA 11:620mA
2	RW	0x0	BUCK4_CMIN_ENB BUCK4_CMIN_ENB:BUCK4 min Current limit enable 0: Enable 1:Disable
1:0	RW	0x01	BUCK4_CMIN_SEL BUCK4_CMIN_SEL:BUCK4 min Current limit select 00:250mA 01:375mA 10:480mA 11:620mA

Chapter 6 Thermal Management

6.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature of RK801 has to be below 125℃.

Depending on the thermal mechanical design (Smartphone, Tablet, Personal Navigation Device, etc), the system thermal management software and the worst case thermal applications, the junction temperature might be exposed to higher values than those specified above.

Therefore, it is recommended to perform thermal simulations at device level (Smartphone, Tablet, Personal Navigation Device, etc) with the measured power of the worst case UC of the device.

6.2 Layout Example

Reasonable PCB wiring directly affects the performance of the chip. So we need to pay special attention to the following points in PCB Layout.

- The capacitor of the CIN must be placed close enough to the pins. To minimize input interference as much as possible.
- The PCB copper area associated with SW pin must be minimized to reduce SW noise.
- Node on the PCB layout to minimize the noise coupling to VOUT pin,Minimize FB routing and return loop area.
- The capacitor of the BST must be placed close enough to the SW Pin.
- To ensure adequate heat dissipation and interference shielding, we must maximize the copper area of the PCB connected to GND .It is recommended to set reasonable and plenty of through via underneath the ground pad to improve the performance of the circuit loop.

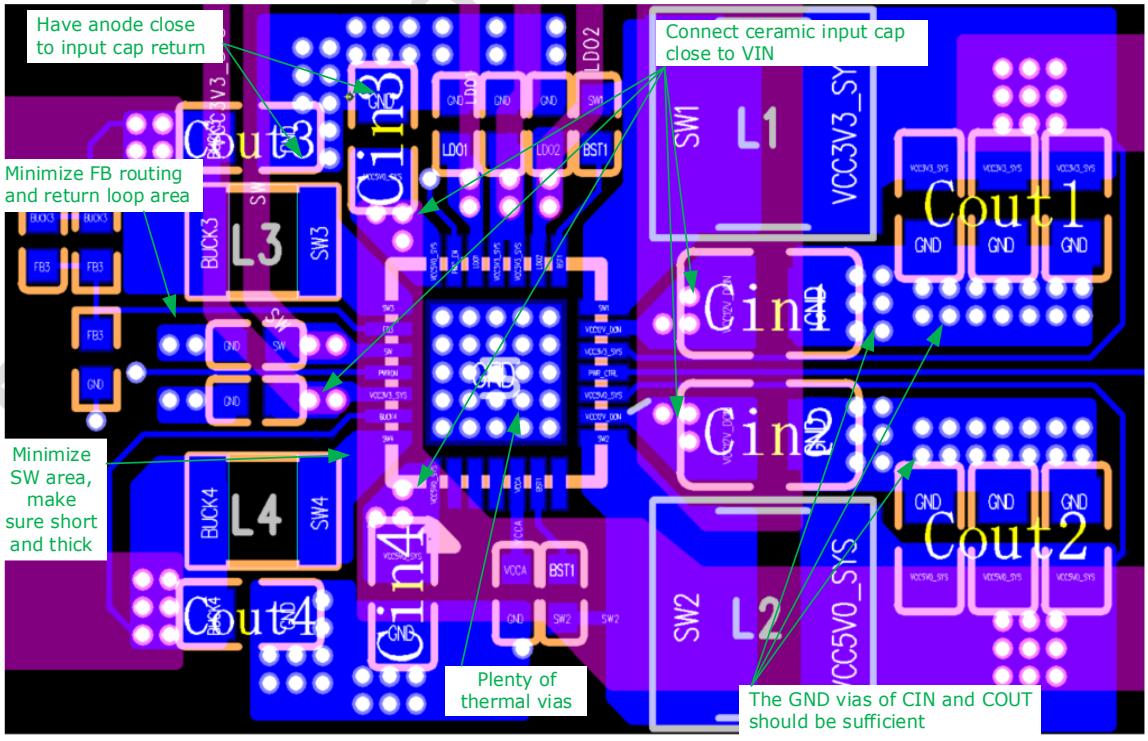


Fig. 6-1 PCB Layout Suggestion

6.3 Package Thermal Characteristics

Table 6-1 provides the thermal resistance characteristics for the package used on this device.

Table 6-1 Thermal Resistance Characteristics

PACKAGE (4mmx4mm QFN28)	θ_{JA}(℃/W)	θ_{JB}(℃/W)	θ_{JC}(℃/W)
RK801	32.17	24.46	52.79

Note: The testing PCB is based on 4 layers, 114mm x 76 mm, 1.6mm thickness, Ambient temperature is 85°C.

Table 6-2 SnPb Eutectic Process-Classification Temperatures (TC)

Package Thickness	Volume mms <350	Volume mms ≥350
<2.5 mm	235 ℃	220℃
≥2.5 mm	220 ℃	220℃

Table 6-3 Pb-Free Process-Classification Temperatures (TC)

Package Thickness	Volume mmcess-C	Volume mmcess-Class	Volume mmcess-Cl
<1.6 mm	260 ℃	260 ℃	260℃
1.6 mm-2.5 mm	260℃	250 ℃	245℃
>2.5 mm	250 ℃	245 ℃	245℃

Note 1:At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (TP) can exceed the values specified in Tables 6-2or 6-3. The use of a higher Tp does not change the classification temperature (Tc).

Note 2: Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or nonintegral heat sinks.

Note 3: The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

Note 4: Moisture sensitivity levels of components intended for use in a Pb-free assembly process shall be evaluated using the Pb-free classification temperatures and profiles defined in Tables 4.2 and 6-4, whether or not Pb-free.

Note 5: SMD packages classified to a give moisture sensitivity level by using Procedures or Criteria defined within any previous version of J-STD-020, JESD22-A112(rescinded),IPC-SM-786 (rescinded) do not need to be reclassified to the current revision unless a change in classification level or a higher peak classification temperature is desired.

Table 6-4 Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T smin) Temperature max(Tsmax) Time (Tsmin to Tsmax)(ts)	 100℃ 150℃ 60-120 seconds	 150℃ 200℃ 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3 ℃ /second max.	3 ℃ /second max.
Liquidous temperature (TL) Time at liquidous (tL)	183 ℃60-150 seconds	217 ℃ 60-150 seconds
Peak package body temperature (Tp)*	See classification temp in Table 6-2	See classification temp in Table 6-3
Time(tp)* * within 5℃ of the specified classification temperature (Tc)	20** seconds	30** seconds
Average ramp-down rate (Tp to Tsmax)	6℃ /second max.	6 ℃ /second max.
Time 25 ℃ to peak temperature	6 minutes max.	8 minutes max.
*Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.		

Note 1: All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow(e.g.,ive-bug). If

parts are reflowed in other than the normal ive-bug assembly reflow orientation (i.e.,dead-bug), Tp shall be within ±2℃ of the live-bug Tp and still meet the Tc requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures refer to JEP140 for recommended thermocouple use.

Note 2: Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly

profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table 6-4.

For example, if Tc is 260 ℃and time Tp is 30 seconds, this means the following for the supplier and the user.

For a supplier. The peak temperature must be at least 260 ℃.The time above 255 C must be at least 30 seconds.

For a user: The peak temperature must not exceed 260 ℃. The time above 255 ℃C must not exceed 30 seconds.

Note 3: All components in the test load shall meet the classification profile requirements.

Note 4: SMD packages classified to a given moisture sensitivity level by using Procedures or Criteria defined within any previous version of ,J-STD-020

JESD22-A112 (rescinded), IPC-SM-786(rescinded) do not need to be reclassified to the current revision unless a change in classification level or a higher peak classification temperature is desired.

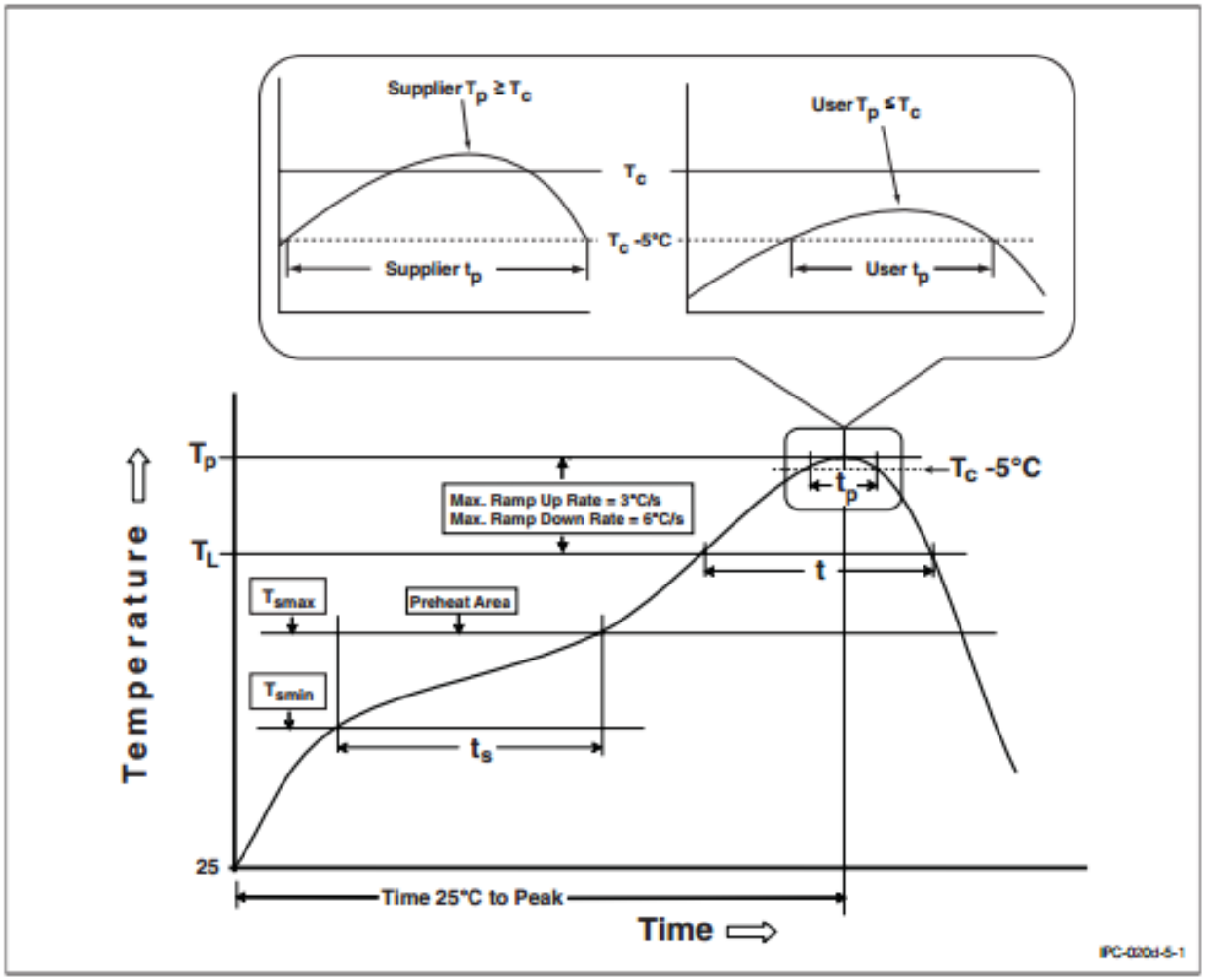


Figure 5-1 Classification Profile

