Rockchip RK805B Datasheet

Revision 1.0
Jan. 2026

Revision History

Date	Revision	Description
2026-01-12	1.0	Initial Release

Table of Content

Figure Index

Table Index

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Chapter 1 Introduction

1.1 Overview

The RK805B is a complete power supply solution for portable systems. The highly integrated device includes four buck DC-DC converters, three high performance LDOs, two general purpose push-pull outputs,I^2C interface, programmable power sequencing and an RTC.
The RK805B improves performance, reduces component count and size, and therefore provides lower cost solution compared to conventional portable designs. The ultra-fast 2MHz COT ripple-based control DC/DC architecture optimizes the transient performance and is compatible with tiny low-cost ceramic inductors and capacitors. All DC/DC channels include integrated MOSFETS. Internal soft-start and compensation circuits minimize external components count. Most outputs can be programmed through the I^2C interface.

The RK805B integrates internal RC oscillator for low-cost application without RTC function.

1.2 Feature

- Input voltage range: 2.7V to 5.5V
- 2MHz Switching Frequency for bucks
- COT ripple-based control architecture for best transient performance
- Internal compensation and soft start
- I^2C Programmable output levels and power sequencing
- High efficiency architecture
- Integrated Vout Discharge Circuit for BUCK and LDO
- Power:
  - BUCK1: Synchronous Buck regulator, 4A max
  - BUCK2: Synchronous Buck regulator, 4A max
  - BUCK3: Synchronous Buck regulator, 2A max
  - BUCK4: Synchronous Buck regulator, 2A max
  - LDO1/LDO2/LDO3: Linear regulators, 300mA max
  - OUT1/OUT2:General digital output,COMS level output,high level is VOUT4
- Auxiliary: Flexible Power Sequence control
- Package: 4mmx4mm QFN32 (pitch 0.4mm)

1.3 Typical Application Diagrams

1.3.1 RK805B_CM_MODE=1

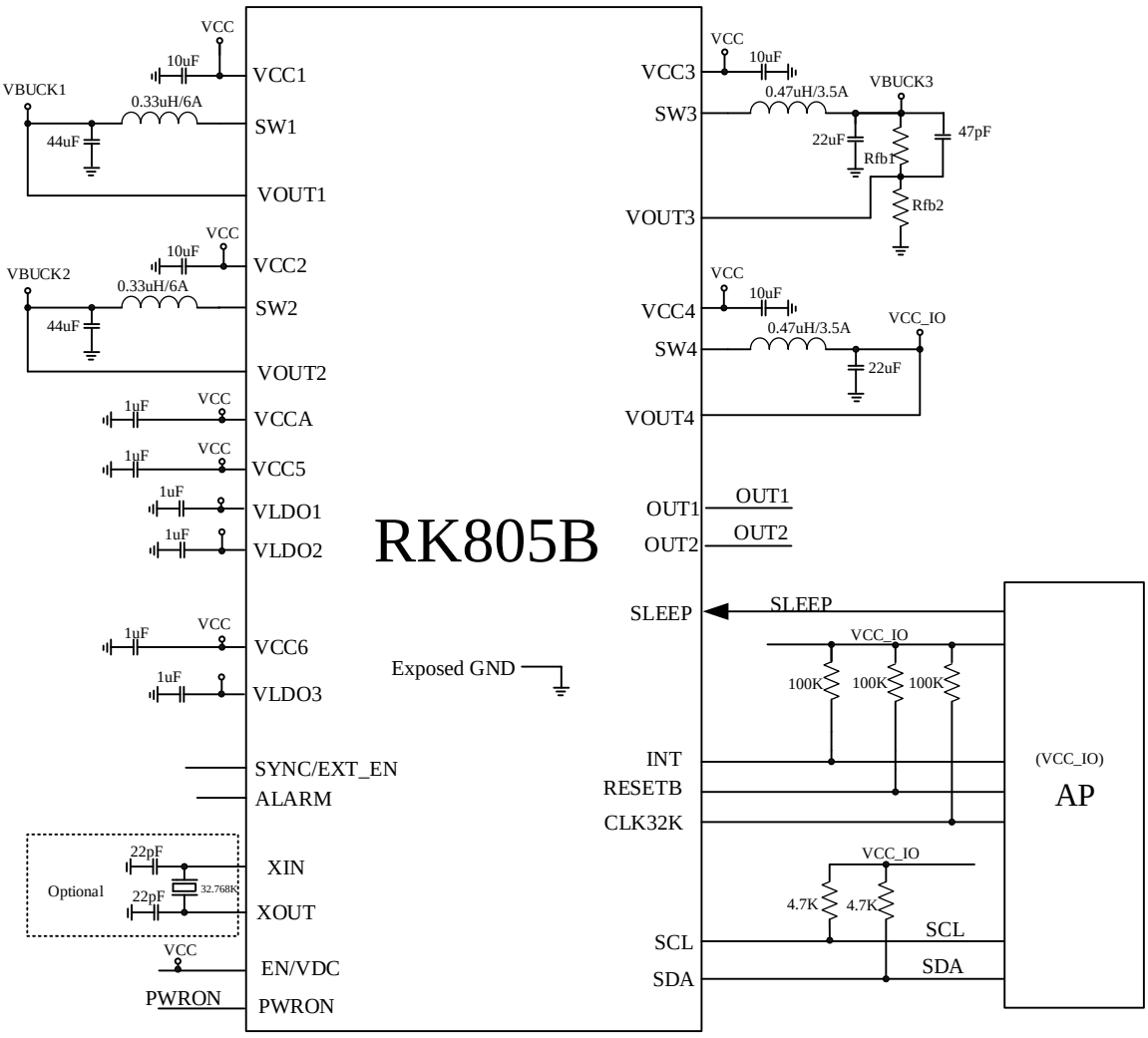
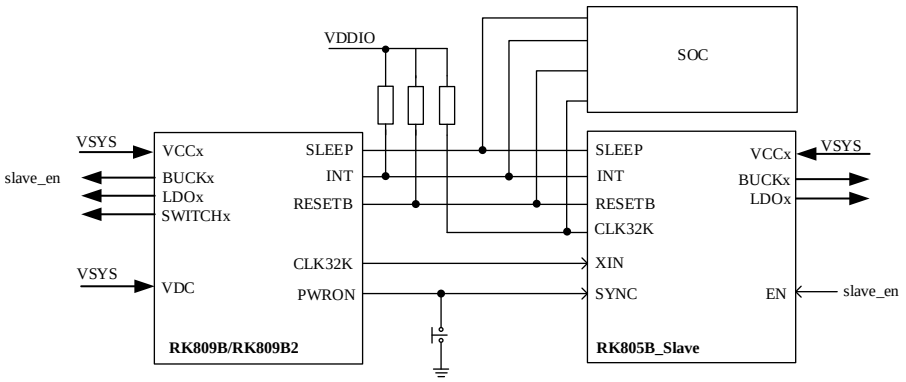
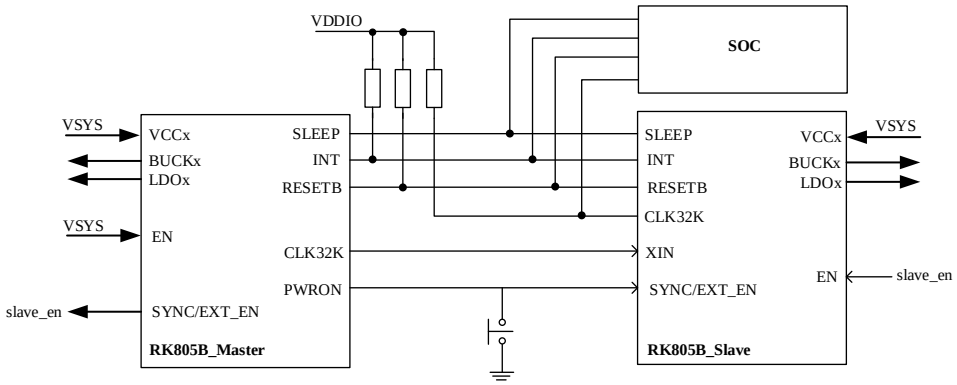


Fig. 1-1 RK805B One Battery Cell Application



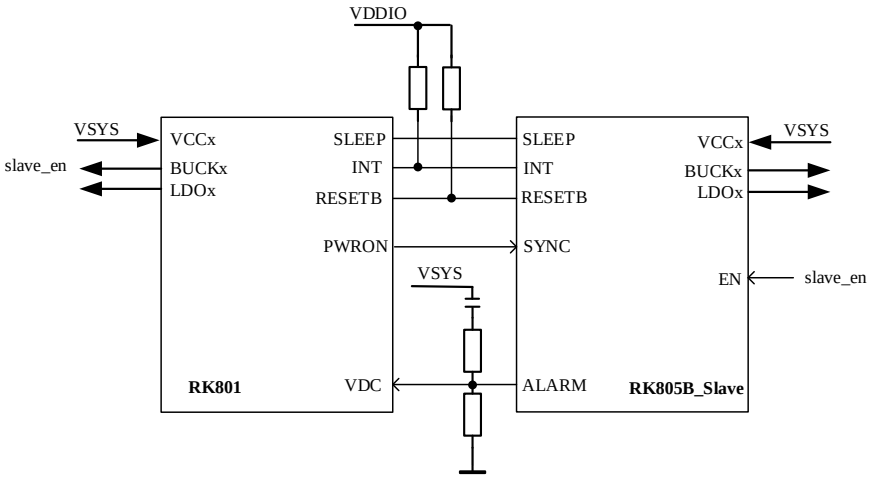
Notes：In this case ,the function of VB_LO_ACT for RK809B/RK809B2 should be set to shut down system. The CLK32K clock of RK809B/RK809B2 cannot be turned off when the device is shut down. And the PWRON of RK809B/RK809B2 cannot be connected elsewhere because it will be pulled low for 1ms when the device is shut down.

Fig. 1-2 RK805B with RK809B/RK809B2 Combined Application



In this case ,the function of VB_LO_ACT for RK805B Master should be set to shut down system. And the PWRON of RK805B Master cannot be connected elsewhere because it will be pulled low for 1ms when the device is shut down.

Fig. 1-3 RK805B with RK805B Combined Application



Notes: In this case ,the PWRON of RK801 cannot be connected elsewhere because it will be pulled low for 1ms when the device is shut down.

Fig. 1-4 RK805B with RK801 Combined Application

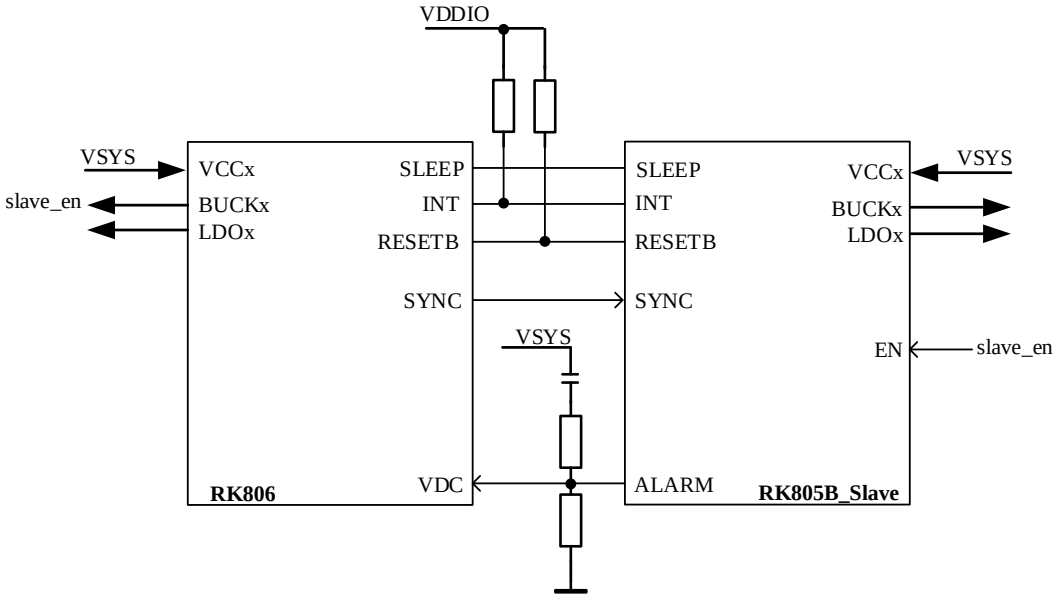


Fig. 1-5 RK805B with RK806 Combined Application

1.3.2 RK805B_CM_MODE=0，the application fully compatible replacement with RK805 .

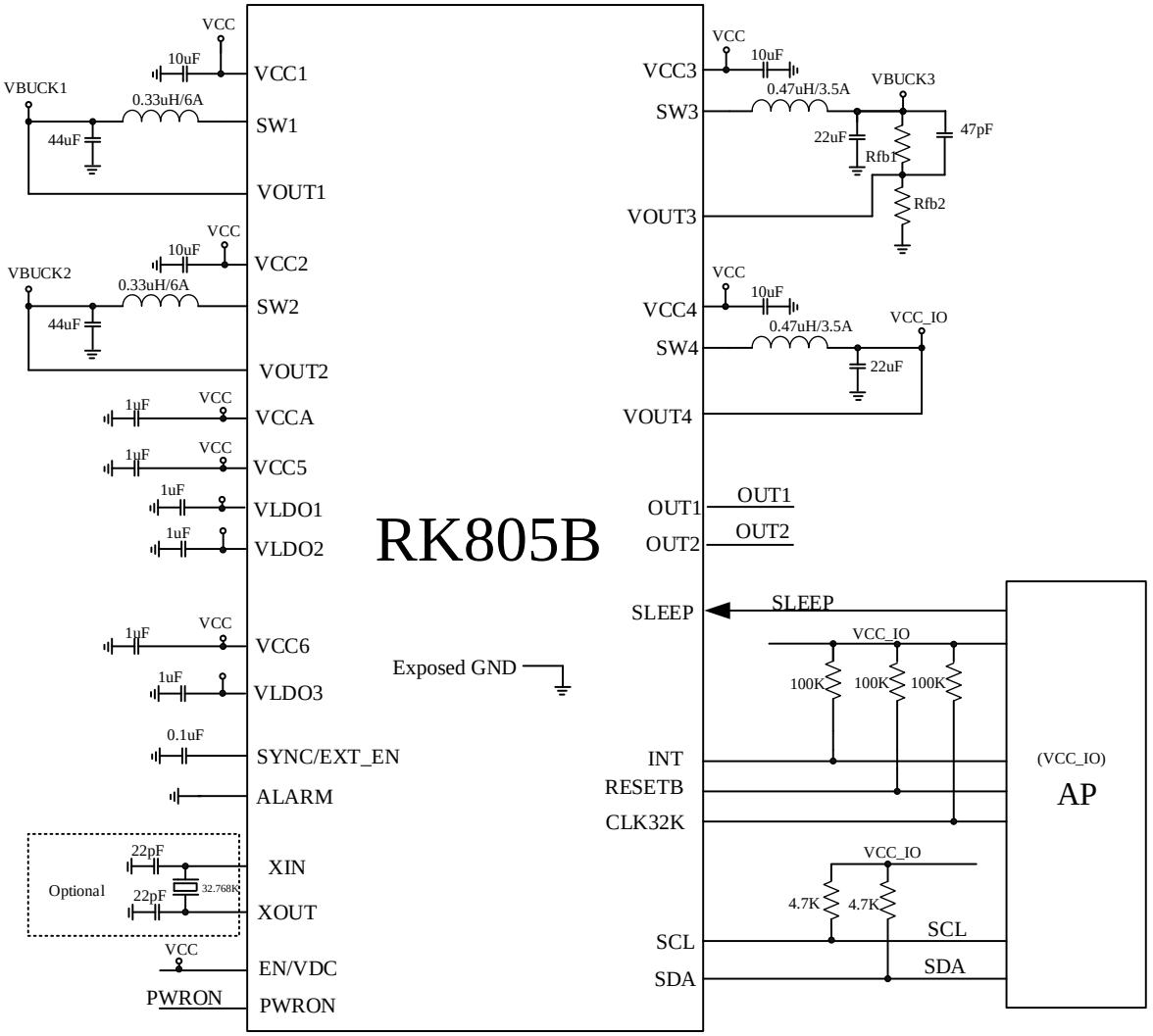


Fig. 1-6 RK805B One Battery Cell Application

Note: Within this mode,there are still some differences between RK805B and RK805 that need to be noted.

(a)SYNC/EXT_EN can be connected to ground through Via a capacitor,in the same way as the REFGND pin of the RK805 ,or it can be floating.

SYNC: Used for synchronily starting up with the Master when in Slave mode.

EXT_EN:In Master mode,the EXT_EN function is used to control the enable signal of the external DCDC converter. After a 4mS delay from the rising edag of EXT_EN ,the DCDC channels of the RK805B to be start up following the predefined power-up sequence.

(b)RTC_ALARM can connected to ground through a capactor just like the Pin of VREF for RK805 ,it also can be floating.

RTC_ALARM:When used with RK806/RK801,it can act as a timed startup function,which adresses the RK806/RK801 lack of this feature.

(c)The XIN Pin of RK805B does not require a pull-up resistor connected to VCCA.

(d)The maximum currents of BUCK1~BUCK4 and LDO3 are different,for details,please refer to the relevant documents.

(e)The maximum load capacity of BUCK1/2 of the RK805B is 4A,While that of BUCK3/4 is

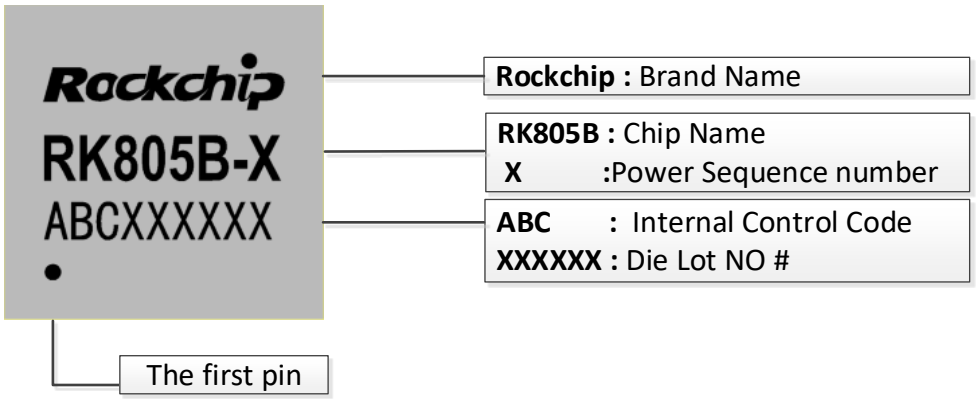
2A.When theRK805B is used as a replacement for the RK805 without modifying the application schme,please select inductors of 0.47uH/3A(for BUCK1/2) and 0.47uH/2A(for BUCK3/4) respectively.

Chapter 2 Package information

2.1 Ordering information

Orderable Device	RoHS status	Package	Package Qty
RK805B-1	RoHS pass	QFN32(4X4)	4900ea/inner box* 6 inner boxes/outer box
RK805B-2	RoHS pass	QFN32(4X4)	4900ea/inner box* 6 inner boxes/outer box
RK805B-3	RoHS pass	QFN32(4X4)	4900ea/inner box* 6 inner boxes/outer box
RK805B-4	RoHS pass	QFN32(4X4)	4900ea/inner box* 6 inner boxes/outer box
RK805B-6	RoHS pass	QFN32(4X4)	4900ea/inner box* 6 inner boxes/outer box
RK805B-8	RoHS pass	QFN32(4X4)	4900ea/inner box* 6 inner boxes/outer box

2.2 Top Marking



2.3 Dimension

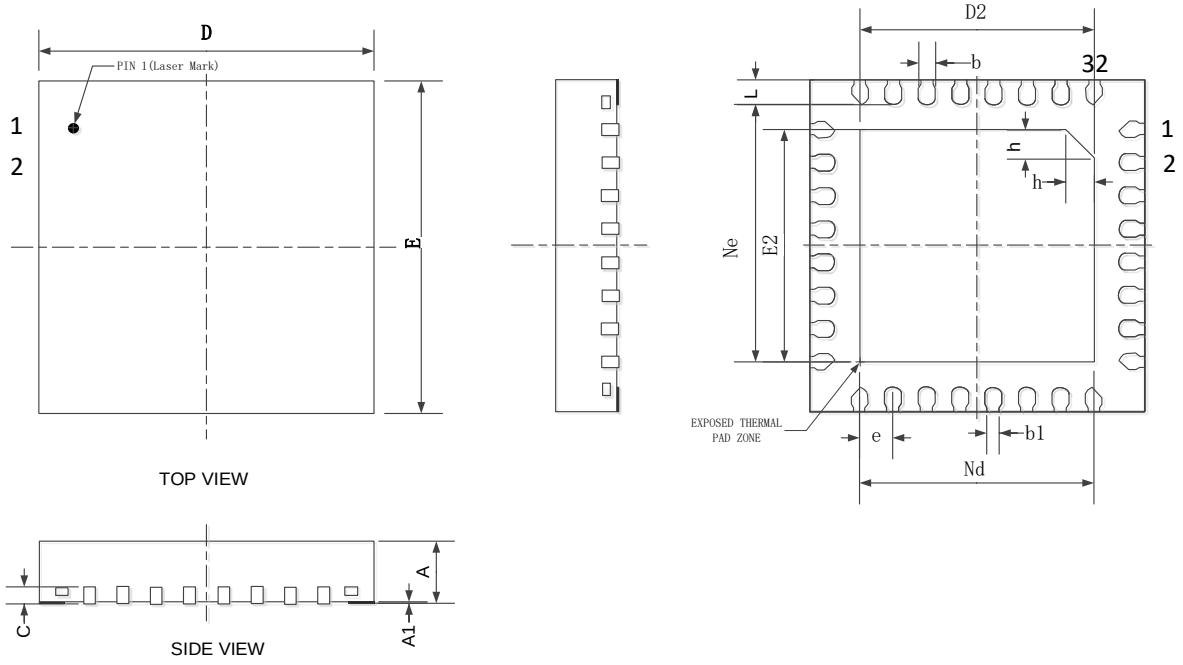


Fig. 2-1 QFN32 4mm X 4mm（Pitch is 0.4mm）

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1		0.14REF	
c	0.18	0.2	0.25
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
e		0.40BSC	
Ne		2.80BSC	
Nd		2.80BSC	
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
L	0.25	0.30	0.35
h	0.30	0.35	0.40

Note:

- *Coplanarity applies to leads, corner leads and die attach pad.*
- *Dimension b applies to metalized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measure in that radius area.*
- *0.15mm of dimension b is recommended in PCB layout.*

2.4 Pin Assignment

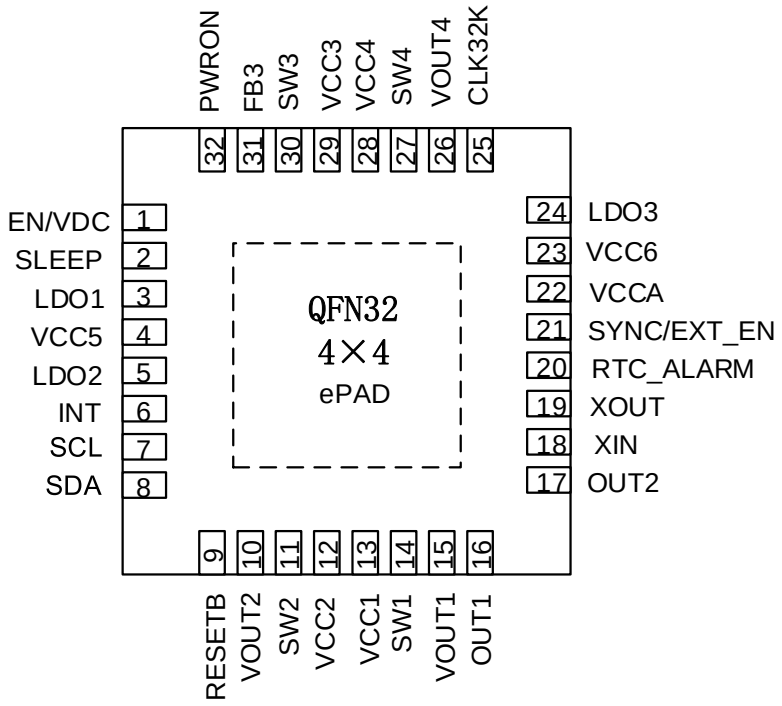


Fig. 2-2 Pin Assignment

2.5 Pinout Number Order

PIN NO	PIN NAME	PIN DESCRIPTION
1	EN/VDC	Power on or power off enable pin, active high, internal 800k resistor pull low to ground. (slave mode) VDC function for master mode.
2	SLEEP	Sleep mode control input
3	LDO1	LDO1 output
4	VCC5	Power supply of LDO1/2
5	LDO2	LDO2 output
6	INT	Interrupt request pin, open drain
7	SCL	I2C clock input
8	SDA	I2C data input and output
9	RESETB	Reset pin after power on, active low
10	VOUT2	Output feedback voltage of buck2
11	SW2	Switching node of buck2
12	VCC2	Power supply of buck2
13	VCC1	Power supply of buck1
14	SW1	Switching node of buck1
15	VOUT1	Output feedback voltage of buck1
16	OUT1	General digital output pin 1, CMOS level output, high level is VOUT4
17	OUT2	General digital output pin 2, CMOS level output, high level is VOUT4

PIN NO	PIN NAME	PIN DESCRIPTION
18	XIN	32.768KHz crystal oscillator input
19	XOUT	32.768KHz crystal oscillator output
20	RTC_ALARM	When RTC alarm occurs, this pin is pulled high to VCCA, clear the reg11<6> to pull low this pin. Internal reference voltage.(RK805B_CM_MODE=0)
21	SYNC/EXT_EN	slave mode ： Sync power down function when combined with RK809B application. Master mode ： EXT_EN function to control external DCDC enable. When EXT_EN rising edge comes, the voltage of VCCx must be higher than 2.7V threshold within 4mS. Reference ground.(RK805B_CM_MODE=0)
22	VCCA	Power supply of controller
23	VCC6	Power supply of LDO3
24	LDO3	LDO3 output
25	CLK32K	slave mode ： 32.768KHz clock output, open drain Master mode ： coms output,the high level is same as VCCA,and connect to XIN of the RK805B slave
26	VOUT4	Output feedback voltage of buck4
27	SW4	Switching node of buck4
28	VCC4	Power supply of buck4
29	VCC3	Power supply of buck3
30	SW3	Switching node of buck3
31	FB3	Output feedback voltage of buck3
32	PWRON	Power on key input, active low, internal 17k resistor pull high to VCCA
Exposed pad	Exposed ground	Ground

Chapter 3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Parameter	Min	Max	Units
Voltage range on pins VCCx，FB3,VOUTx	-0.3	6.5	V
Voltage range on pins LDOx	-0.3	6.5	V
Voltage range on pin CLK32K, SLEEP	-0.3	6.5	V
Voltage range on pins XIN,XOUT, EN，PWRON,SYNC,RTC_ALARM	-0.3	VCCx+0.3	V
Voltage range on pins RESETB, INT, SDA, SCL,OUT1,OUT2	-0.3	VCCA+0.3V	V
Voltage range on pins SW1/2/3/4	-0.3（-2V for <10ns and -3.5V for <5ns）	6(8.5V for <10ns)	V
Storage temperature range, TS	-40	150	℃
Operating temperature range, TJ		150	℃
Maximum Soldering Temperature,T_{SOLDER}		300	℃

Note 1. Exposure to the conditions exceeded absolute maximum ratings may cause permanent damages and affect reliability and safety of both device and systems using the device. The functional operations cannot be guaranteed beyond specified values in the recommended conditions.

3.2 Recommended Operating Conditions

Parameter	Min	TYP	Max	Units
Voltage range on pins VCC1/2/3/4	2.7	5	5.5	V
Voltage range on pins VCC5/6/7	2	5	5.5	V
Voltage range on other pins			5.5	V
Power Dissipation			2.7	W
Operating temperature range, TJ	-40		125	℃

3.3 DC Characteristics

T_J=25C; V_{VCCA}=VCCx=5V, unless otherwise specified.

Parameter	Symbol	Note	Min.	Typ.	Max.	Unit
Power dissipation						
VCCA Operating Range	V_{VCCA}		2.7	5	5.5	V
VCCA over voltage protect	V_{VCCA_ov}			6		V
VCCA under voltage protect	V_{VCCA_uv}	Step=0.1V, from 2.7V to 3.4V programmable		2.7		V
VCCA low voltage alarm	V_{VCCA_lv}	Step=0.1V, from 2.8V to 3.5V programmable		3.3		V
VCCA OK voltage threshold	V_{VCCA_OK}	2.8V/3.0V/3.4V/3.6V OTP programmable		3.0		V
TSD threshold, when the temperature is higher than it, The PMIC would be shutdown.	Tsd	140/160℃ by I2C programmed. Typical is 140℃.	135	140	145	℃
T warning threshold, when the temperature is higher than it, interrupt happen.	Twa	85~115℃ by I2C programmed. Typical is 85℃.	80	85	90	℃
Long press PWRON key time	Tlp	6s~12s by I2C programmed. Typical is 6s.		6		s
Short press PWRON key time	Tst	500ms/100ms/20mS/ 40mS by OTP programed. Typical is 500ms.		500		ms
Sequence gap	Seq_gap	1ms/2ms/4mS by OTP programed. Typical is 2ms.		2		ms
CH1：Buck 1						
Input supply voltage range	V_{CC1}		2.7		5.5	V
VCC1 under voltage protect	V_{VCC1_uv}			2.7		V
Output Voltage Accuracy @ all load @ all input voltage range	V_{out1}	0.5V~1.45V by I2C programmed. Typical is 1.0V. (Step=12.5mV)/1.8V/ 2.0V/2.2V/2.3V RK805B_CM_MODE=1	0.99	1.0	1.01	V
Output Voltage Accuracy @ all load @ all input voltage range	V_{out1}	0.7125V~1.45V by I2C programmed. Typical is 1.0V. (Step=12.5mV)/1.8V/ 2.0V/2.2V/2.3V RK805B_CM_MODE=0	0.99	1.0	1.01	V
Rated output current	I_{MAX1}			4		A
Switching Frequency when CCM mode	Fsw1	Vin-Vout>1.5V	1.75	2.0	2.25	MHz
Efficiency	Eff1	VCC1=5V, Vout=1V,Iout=0.4A		85		%

Parameter	Symbol	Note	Min.	Typ.	Max.	Unit
	Eff2	VCC1=5V, Vout=1V,Iout=4A		67		%
CH1：Buck 2						
Input supply voltage range	V_{CC2}		2.7		5.5	V
Output Voltage Accuracy @ all load @ all input voltage range	V_{out2}	0.5V~1.45V by I2C programmed. Typical is 1.0V. (Step=12.5mV)/1.8V/ 2.0V/2.2V/2.3V RK805B_CM_MODE=1	0.99	1.0	1.01	V
Output Voltage Accuracy @ all load @ all input voltage range	V_{out2}	0.7125V~1.45V by I2C programmed. Typical is 1.0V. (Step=12.5mV)/1.8V/ 2.0V/2.2V/2.3V RK805B_CM_MODE=0	0.99	1.0	1.01	V
Rated output current	I_{MAX2}			4		A
Switching Frequency when CCM mode	Fsw2	Vin-Vout>1.5V	1.75	2.0	2.25	MHz
Efficiency	Eff1	VCC2=5V, Vout=1V,Iout=0.4A		85		%
	Eff2	VCC2=5V, Vout=1V,Iout=4A		67		%
CH1：Buck 3						
Input supply voltage range	V_{CC3}		2.7		5.5	V
Feedback Voltage, Default	V_{FB3}	Typ Vref=0.4V(RK805B_CM_MODE=1）, Optional 0.8V(RK805B_CM_MODE=0）	0.396	0.400	0.404	V
Rated output current	I_{MAX3}			2		A
Switching Frequency when CCM mode	Fsw3	Vin-Vout>1.5V	1.75	2.0	2.25	MHz
Efficiency	Eff1	VCC3=5V, Vout=1.5V,Iout=0.4A		86		%
	Eff2	VCC3=5V, Vout=1.5V,Iout=2A		75		%
VBUCK3OUT= V_{FB3} * (1+Rfbup/Rfbdn)； please refer to the typical application						
CH1：Buck 4						
Input supply voltage range	V_{CC4}		2.7		5.5	V
Output Voltage Accuracy @ all load @ all input voltage range	V_{out4}	0.5V~3.4V by I2C programmed. Typical is 3.3V. Step=50mV RK805B_CM_MODE=1	3.267	3.3	3.333	V
Output Voltage Accuracy @ all load @ all input voltage range	V_{out4}	0.8V~3.4V by I2C programmed. Typical is 3.3V. Step=50mV RK805B_CM_MODE=0	3.267	3.3	3.333	V
Rated output current	I_{MAX4}			2		A
Switching Frequency when CCM mode	Fsw4	Vin-Vout>1.5V	1.75	2.0	2.25	MHz
Efficiency	Eff1	VCC4=5V, Vout=3.3V, Iout=0.4A		90		%
	Eff2	VCC4=5V, Vout=3.3V,Iout=2A		88		%
CH5 ： LDO1						
Input supply voltage range	V_{CC5}		2.2		5.5	V
	V_{LDO1}	0.5V~3.4V by I2C	0.98	1.0	1.02	V

Parameter	Symbol	Note	Min.	Typ.	Max.	Unit
Output Voltage Accuracy @ all load @ all input voltage range		programmed. Typical is 1V. Step=50mV RK805B_CM_MODE=1				
Output Voltage Accuracy @ all load @ all input voltage range	V_{LDO1}	0.8V~3.4V by I2C programmed. Typical is 1V. Step=100mV RK805B_CM_MODE=0	0.98	1.0	1.02	V
Rated output current	I_{MAX1}	Vcc5- Vldo1≥0.4V, Vldo1≤2.5V		300		mA
		Vcc5- Vldo1≥0.2V, Vldo1>2.5V				
Power supply reject ratio (f=1kHz)	PSRR1	V_{CC5}=5V,V_{LDO1}=1V		50		dB
CH6 ： LDO2						
Input supply voltage range	V_{CC5}		2.2		5.5	V
Output Voltage Accuracy @ all load @ all input voltage range	V_{LDO2}	0.5V~3.4V by I2C programmed. Typical is 1V. Step=50mV RK805B_CM_MODE=1	1.764	1.8	1.836	V
Output Voltage Accuracy @ all load @ all input voltage range	V_{LDO2}	0.8V~3.4V by I2C programmed. Typical is 1V. Step=50mV RK805B_CM_MODE=0	1.764	1.8	1.836	V
Rated output current	I_{MAX2}	Vcc6- Vldo2≥0.4V, Vldo2≤2.5V		300		mA
		Vcc6- Vldo2≥0.2V, Vldo2>2.5V				
Power supply reject ratio (f=1kHz)	PSRR2	V_{CC5}=5V,V_{LDO2}=1.8V		50		dB
CH7 ： LDO3						
Input supply voltage range	V_{CC6}		2.2		5.5	V
Output Voltage Accuracy @ all load @ all input voltage range	V_{LDO3}	0.5V~3.4V by I2C programmed. Typical is 1V. Step=50mV RK805B_CM_MODE=1	0.98	1.0	1.02	V
Output Voltage Accuracy @ all load @ all input voltage range	V_{LDO2}	0.8V~3.4V by I2C programmed. Typical is 1V. Step=50mV RK805B_CM_MODE=0	0.98	1.0	1.02	V
Rated output current	I_{MAX3}	Vcc7- Vldo3≥0.4V, Vldo3≤2.5V		300		mA
		Vcc7- Vldo3≥0.2V, Vldo3>2.5V				
Power supply reject ratio (f=1kHz)	PSRR3	V_{CCA}=5V, V_{LDO3}=1.0V		50		dB
I2C Interface(7 bits I2C slave address:0011000/7 bits I2C master address :0101000)						
SCL clock frequency	f_{SCL}				1	MHz
RTC						
RTC operation voltage			2		5.5	V
CLK32K Jitter					100	nS
CLK32K duty			40		60	%
junction capacitance of XIN					8	pF
junction capacitance of XOUT					10	pF
IO Interface						
EN pin input high level	V_{IH1}	RK805B_CM_MODE=1	0.5		0.69	V

Parameter	Symbol	Note	Min.	Typ.	Max.	Unit
threshold						
EN pin input low level threshold	V_{IL1}	RK805B_CM_MODE=1	0.40	0.44	0.48	V
EN pin input high level threshold	V_{IH2}	RK805B_CM_MODE=0	0.6		1.0	V
EN pin input low level threshold	V_{IL2}	RK805B_CM_MODE=0	0.40	0.44	0.48	V
PWRON/SYNC pins pull high to VCCA resistance		RK805B_CM_MODE=0 or master=1: SYNC 17K open		17		K
PWRON/SYNC pins input high level threshold	VIH		0.7* VCCA			V
PWRON/SYNC pins input low level threshold	V_{IL2}				0.3*VCCA	V
SLEEP/RESETB/SCL/SDA pins input high level threshold	V_{IH2}		1.05			V
PWRON/SYNC/SLEEP/RESETB/SCL/SDA pins input low level threshold	V_{IL2}				0.45	V
CLK32K/OUT1/OUT2/RESETB/SDA/INT/EXT_EN open drain output pins low level voltage	V_{OL1}	3.0 mA sink current			0.4	V
RTC_ALARM output pin high level voltage	V_{OL1}	source current	VCCA-0.4			V
Power consumption						
Shutdown current, only RTC work	I_{SD}	EN=0, VCCA current.			10	uA
Shutdown current	I_{SD}	EN=1,shut down pmu, VCCA current.			35	uA
Sleep mode current	I_{SD}	Power on buck1/2, ldo1/2, VCCA and VCCx current, null load.			100	uA
Active mode current		Power on all channel, VCCA and VCCx current, null load.			300	uA

Chapter 4 Function Description

4.1 State Machine Description

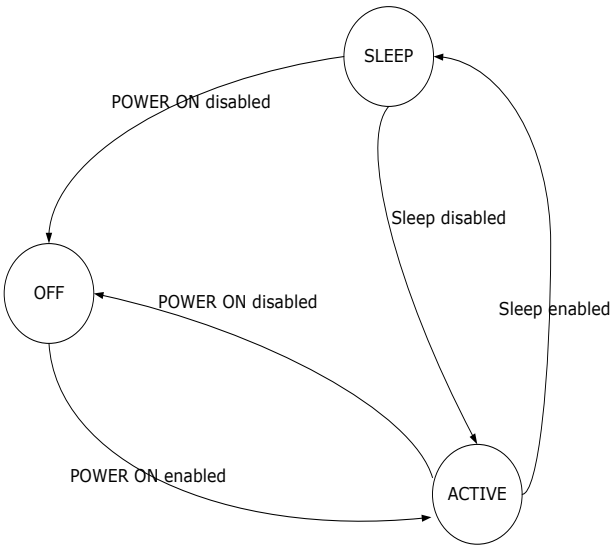


Fig. 4-1 State Machine

4.2 Device Power on Enable Conditions

- If none of the device power-on disable conditions is met, the following conditions are available to turn on the device:
  - EN signal rising edge (slave mode), EN signal high level (master mode).

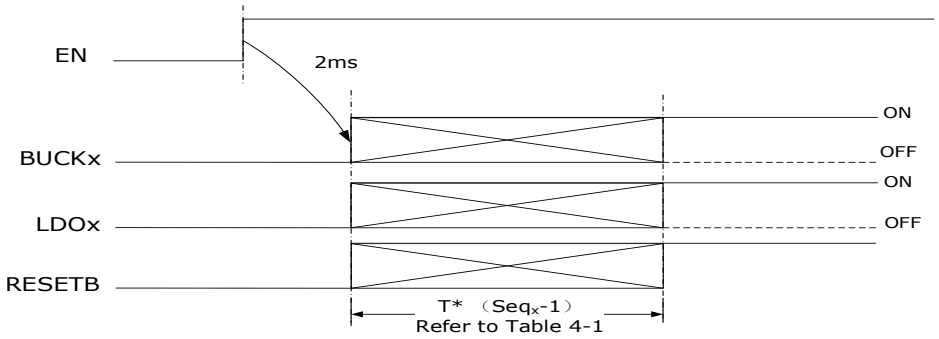


Fig. 4-2 EN rising edge to turn on the PMIC (slave mode)

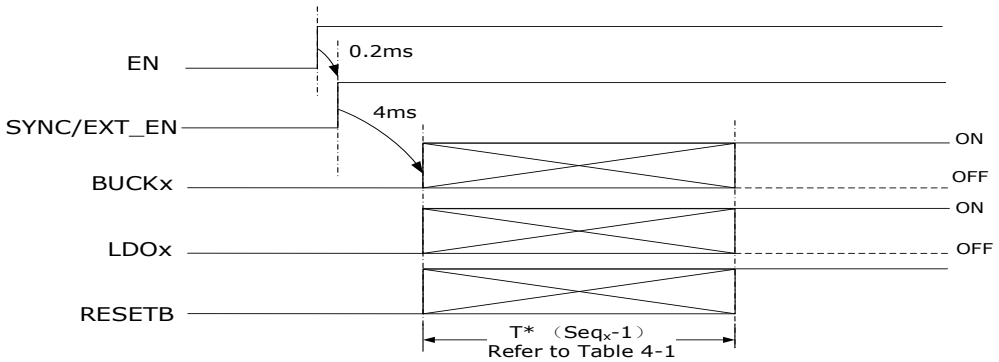
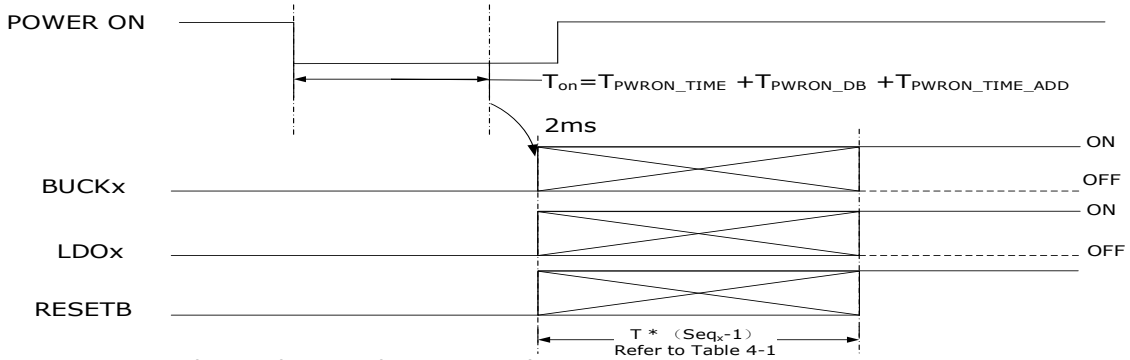


Fig. 4-3 EN high level to turn on the PMIC (Master mode)

- PWRON signal keep low level at least 500mS while the device is off.



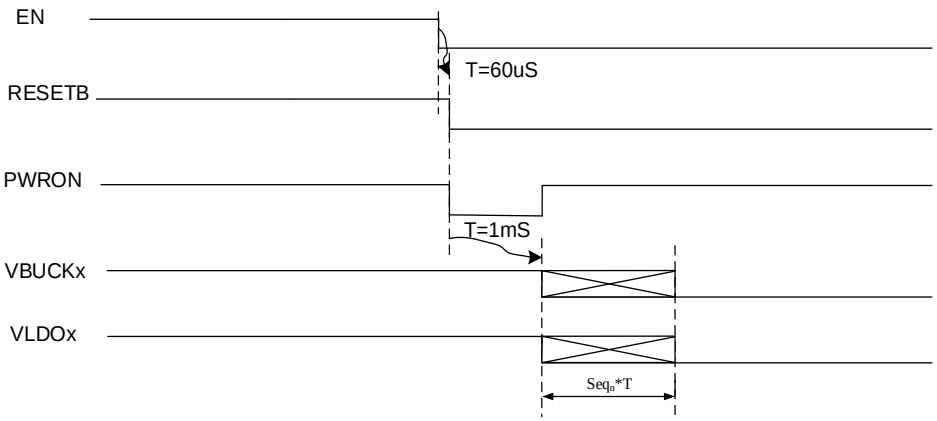
T_{PWRON_TIME}:20mS/40mS/100mS/500mS set by OTP
T_{PWRON_DB} can be set by Register 0x48<6：5>
$T_{PWRON\_ST\_TIME\_ADD}$ can be set by Register 0xB0<2:0>

Fig. 4-4 POWER ON to turn on the PMIC

- RTC alarm interrupt flag active while the device is off.

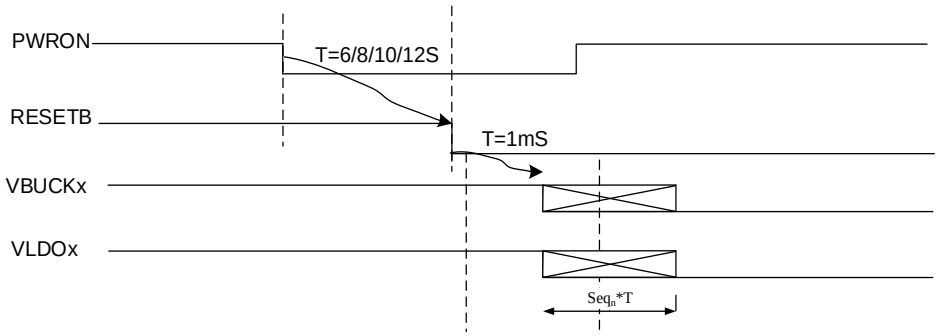
4.3 Device Power on Disable Conditions

- EN signal keep low level. (slave mode)
- PWRON signal low level during more than the long-press delay: pwron_lp_off_time (POWERON_LP_ACT=0).
- Die temperature has reached the thermal shutdown threshold.
- VCCA down below UVLO threshold.
- VCCA down below VBLO threshold, and Reg21<4>=0.
- VCCA higher than OVP threshold.
- VCC1 down below 2.7V.
- SLEEP signal active, and Reg50<3:2>=10
- DEV_OFF control bit set to 1.
- RESETB signal falling edge and SYNC signal is low level.



Note: Seq_n is the number of shutdown sequence (0xB6~0xB9),T Refer to table 4-1 sequence gap.

Fig. 4-5 EN signal keep low level to turn off the PMIC (slave mode)



Note: Seq_n is the number of shutdown sequence (0xB6~0xB9),T Refer to table 4-1 sequence gap.

Fig. 4-6 Long press "PWRON" key to turn off the PMIC

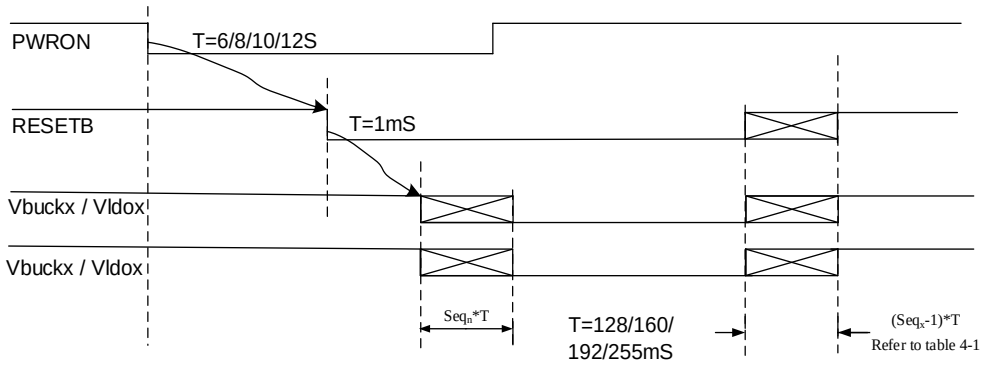
RK805B_CM_MODE=1,if one of the device power-on disable conditions is met, PWRON will be pull down for 1mS after RESETB signal turn to low level.

4.4 Device Power Restart Conditions

- PWRON signal low level duration longer than the long-press delay
- RST occurs and RegB1<7:6>=00.

RST occurs including:

- DEV_RST control bit set to 1.
- RESETB signal falling edge and SYNC signal is high level.
- SLEEP signal active, and Reg50<3:2>=11



Note: Seq_n is the number of shutdown sequence (0xB6~0xB9), T Refer to table 4-1 sequence gap.

Fig. 4-7 Long press "PWRON" key to restart the PMIC

4.5 Device Sleep Enable Conditions

- SLEEP signal high level and Reg50<1>=1, and Reg50<3:2>=01.
- SLEEP signal low level and Reg50<1>=0, and Reg50<3:2>=01.
- Reg50<3:2>=01 and Reg4b<1>=1.

4.6 Power Sequence

Power sequence			RK805B-1		RK805B-2		RK805B-3		RK805B-4		RK805B-6		RK805B-8	
RK805B_CM_MODE			0		0		0		1		0		1	
Short press PWRON key time			500mS		500mS		500mS		500mS		500mS		500mS	
VCCA_OK voltage threshold			3.0V		3.0V		3.0V		3.0V		3.0V		3.0V	
Sequence gap（T）			2mS		2mS		2mS		2mS		2mS		2mS	
	Output voltage range	Max output current	Volt(V)	Seq	Volt(V)	Seq	Volt(V)	Seq	Volt(V)	Seq	Volt(V)	Seq	Volt(V)	Seq
BUCK1	0.5V-1.45V	4A	1.1	2	1.0	3	1.1	2	0.9	1	0.9	2	0.75	1
BUCK2	0.5V-1.45V	4A	1.1	2	2.2	1	1.1	1	0.9	1	0.9	2	0.85	1
BUCK3	setting by external resistors	2A	X	3	X	4	X	3	X	3	X	3	X	5
BUCK4	0.5V-3.4V	2A	3.3	5	3.3	6	3.3	1	0.95	4	3.3	5	0.85	1
LDO1	0.5V-3.4V	300mA	1.8	4	1.0	2	3.3	4	0.9	1	1.8	4	3.3	4
LDO2	0.5V-3.4V	300mA	1.8	4	1.8	5	0.6	OFF	1.8	2	1.8	4	3.3	4
LDO3	0.5V-3.4V	300mA	1.0	1	1.0	2	1.1	1	3.3	4	0.9	1	0.6	OFF
RESETB				10		10	-	10	-	10	X	10	-	10

Table 4-1 Power Start Up Sequence

X: The buck3 voltage is decided by external resistors. The RESETB is open drain output.

4.7 Power Channels

4.7.1 Buck Description

The RK805B provides four high current synchronous buck converters, which deliver up to 4A, 3A and 2A respectively. An enhanced COT architecture is used, which improves the transient response significantly. 2MHz switching frequency and good control method reduce the external inductance and capacitance required. A complete set of protection functions, such as short circuit protection, is implemented in the buck converters too.

For example, the BUCK1: Vout=1.0V, Vin=5V, L=0.33uH, Cout=44uF. Load Current transient from 0.04A to 4A. The output voltage drop at load current rising edge is about **32mV**, which is very good characteristics. The other bucks have the same architecture as BUCK1, so they have the same load transient response characteristics.

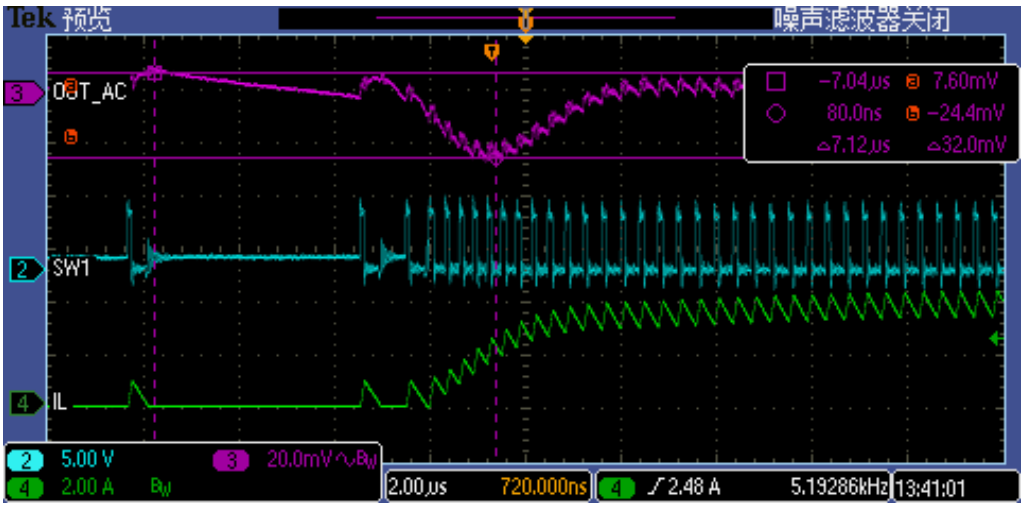


Fig. 4-8 BUCK1 load transient rising edge

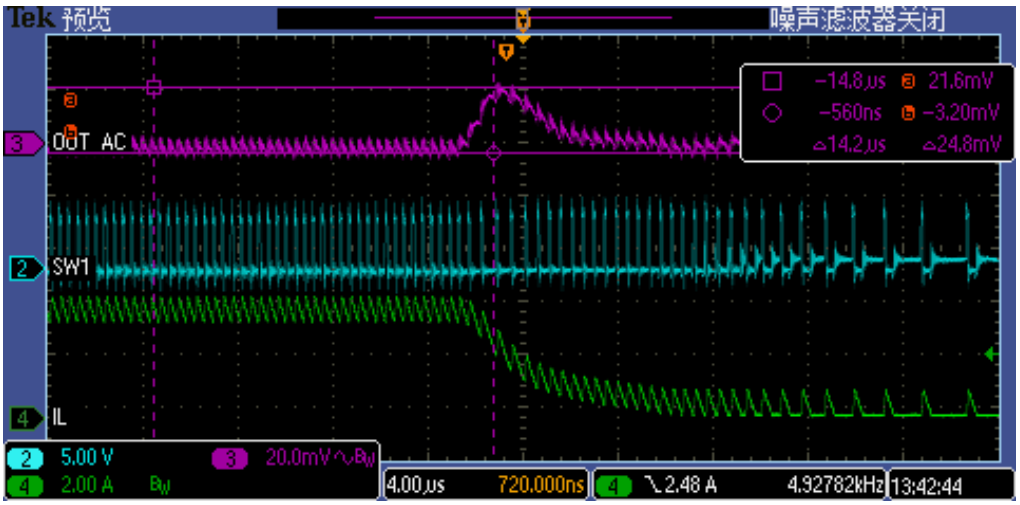


Fig. 4-9 BUCK1 load transient rising edge

Meanwhile, buck converters have good efficiency characteristics at AUTO mode. The test data is shown as below. BUCK output voltages of all channels are set to default.

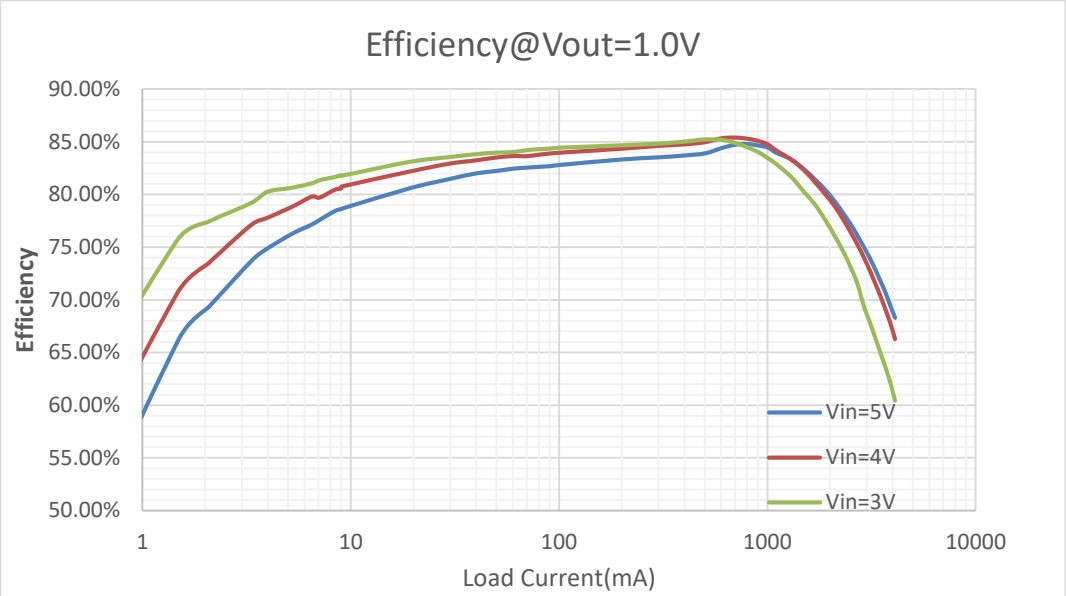


Fig. 4-10 BUCK1 efficiency curve with different input voltage

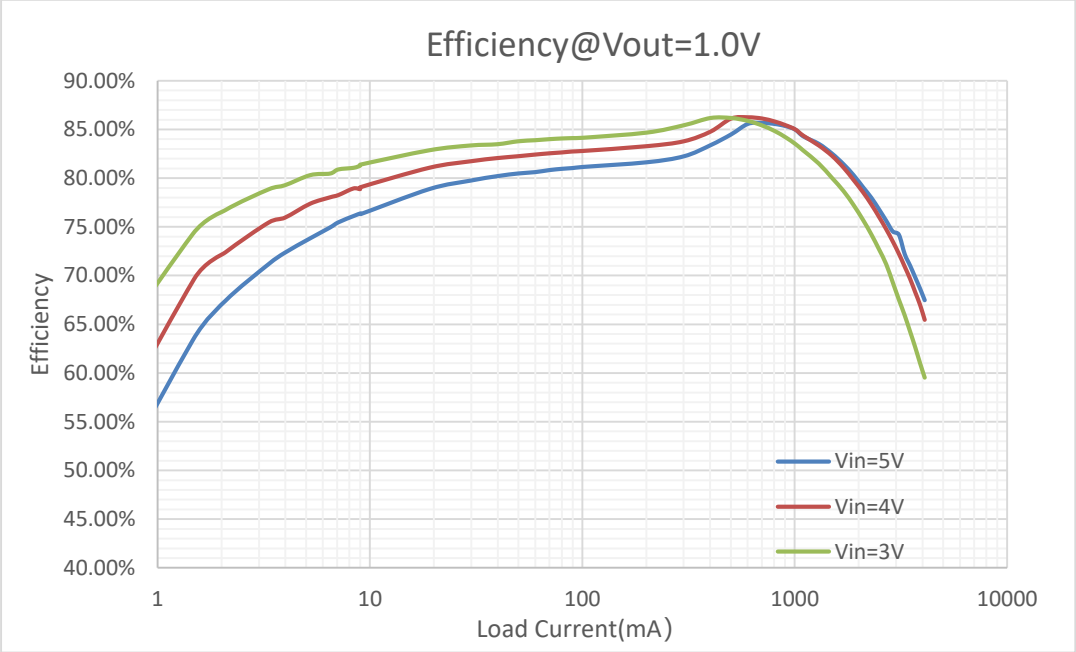


Fig. 4-11 BUCK2 efficiency curve with different input voltage

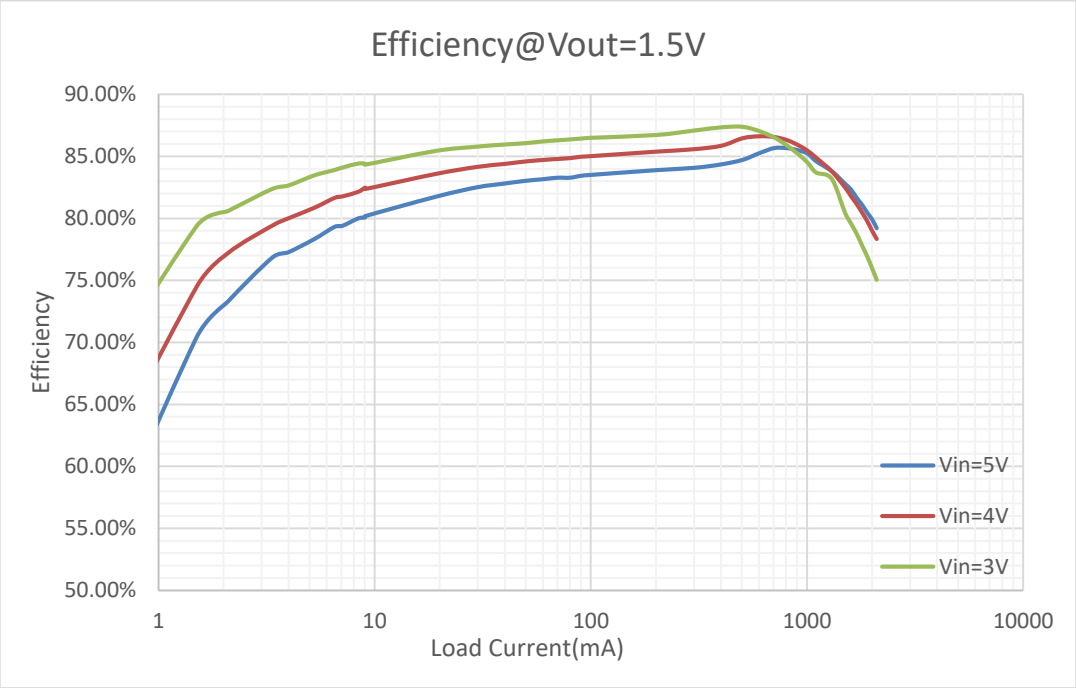


Fig. 4-12 BUCK3 efficiency curve with different input voltage

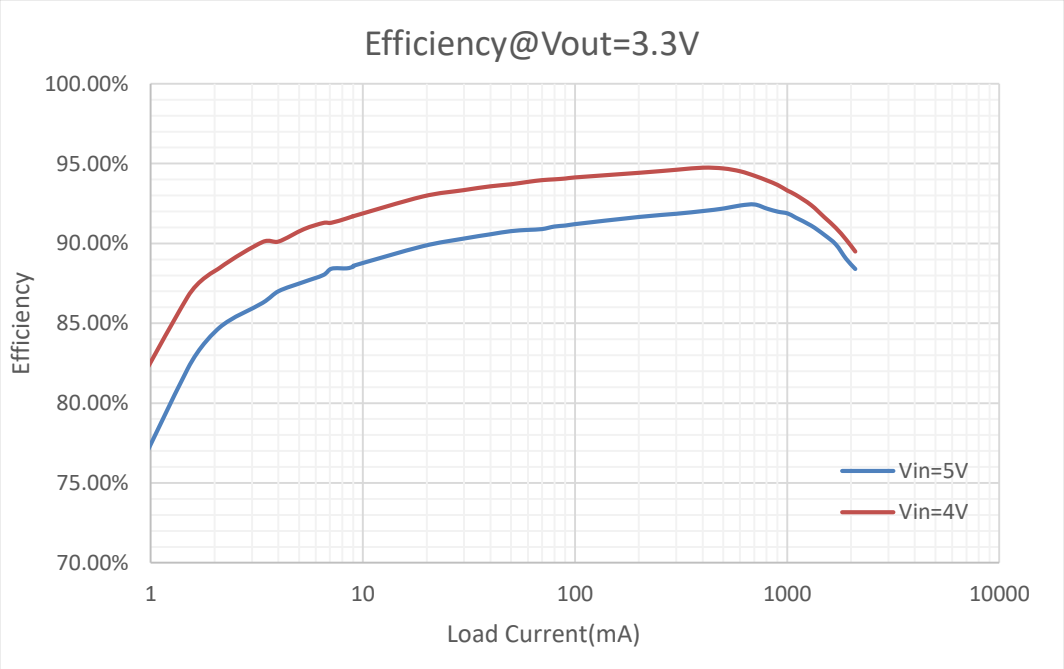


Fig. 4-13 BUCK4 efficiency curve with different input voltage

4.7.2 LDO Description

The RK805B also integrates three LDOs, each capable of providing up to 300mA. Output capacitance for each LDO can be as low as 1.0uF to reduce system cost. The parameters such as output voltage in the different operating modes can be adjusted through the I^2C .

Chapter 5 Register Description

5.1 Register Summary

Name	Offset	Size	Reset Value	Description
SECONDS	0x00	8	0x00	Por Reset
MINUTES	0x01	8	0x50	Por Reset
HOURS	0x02	8	0x08	Por Reset
DAYS	0x03	8	0x21	Por Reset
MONTHS	0x04	8	0x01	Por Reset
YEARS	0x05	8	0x16	Por Reset
WEEKS	0x06	8	0x04	Por Reset
ALARM_SECONDS	0x08	8	0x00	Por Reset
ALARM_MINUTES	0x09	8	0x00	Por Reset
ALARM_HOURS	0x0A	8	0x00	Por Reset
ALARM_DAYS	0x0B	8	0x01	Por Reset
ALARM_MONTHS	0x0C	8	0x01	Por Reset
ALARM_YEARS	0x0D	8	0x00	Por Reset
RTC_CTRL	0x10	8	0x00	Por Reset
RTC_STATUS	0x11	8	0x82	Por Reset
RTC_INT	0x12	8	0x00	Por Reset
RTC_COMP_LSB	0x13	8	0x00	Por Reset
RTC_COMP_MSB	0x14	8	0x00	Por Reset
CHIP_NAME	0x17	8	0x80	Por Reset
CHIP_VER	0x18	8	0x53	Por Reset
OTP_VER	0x19	8	0x00	Por Reset
CLK32KOUT	0x20	8	0x01	Por Reset
VB_MON	0x21	8	0x14	Shutdown Reset:Bit4,Bit0~Bit2 Por Reset:Bit7~Bit5，Bit3
THERMAL	0x22	8	0x00	Shutdown Reset:Bit7~Bit2 Por Reset:Bit1~Bit0
DCDC_EN_REG1	0x23	8	0x00	Shutdown Reset
SLEEP_EN_REG1	0x25	8	0x00	Shutdown Reset
SLEEP_EN_REG2	0x26	8	0x00	Shutdown Reset
LDO_EN_REG1	0x27	8	0x00	Shutdown Reset
SLP_LP_EN	0x2A	8	0x00	Shutdown Reset
BUCK1_CONFIG	0x2E	8	0x7A	Shutdown Reset:Bit7~Bit6 Por Reset:Bit5
BUCK1_ON_VSEL	0x2F	8	0x00	Shutdown Reset
BUCK1_SLP_VSEL	0x30	8	0x00	Shutdown Reset
BUCK2_CONFIG	0x32	8	0x7A	Shutdown Reset:Bit7~Bit6 Por Reset:Bit5
BUCK2_ON_VSEL	0x33	8	0x00	Shutdown Reset
BUCK2_SLP_VSEL	0x34	8	0x00	Shutdown Reset

Name	Offset	Size	Reset Value	Description
BUCK3_CONFIG	0x36	8	0x2A	Shutdown Reset:Bit7~Bit6, Bit4~Bit0 Por Reset:Bit5
BUCK4_CONFIG	0x37	8	0x2A	Shutdown Reset:Bit4~Bit0 Por Reset:Bit5
BUCK4_ON_VSEL	0x38	8	0x00	Shutdown Reset
BUCK4_SLP_VSEL	0x39	8	0x00	Shutdown Reset
LDO1_ON_VSEL	0x3B	8	0xA0	Shutdown Reset:Bit6~Bit0 Por Reset:Bit7
LDO1_SLP_VSEL	0x3C	8	0x00	Shutdown Reset
LDO2_ON_VSEL	0x3D	8	0xA0	Shutdown Reset:Bit6~Bit0 Por Reset:Bit7
LDO2_SLP_VSEL	0x3E	8	0x00	Shutdown Reset
LDO3_ON_VSEL	0x3F	8	0xA0	Shutdown Reset:Bit6~Bit0 Por Reset:Bit7
LDO3_SLP_VSEL	0x40	8	0x00	Shutdown Reset
PWRON_LP_SEL	0x47	8	0x20	Por Reset
PWRON_DB_SEL	0x48	8	0x40	Por Reset
DEVCTRL	0x4B	8	0x00	Shutdown Reset:Bit7,Bit3~Bit0 Por Reset:Bit6~Bit5
INT_STS	0x4C	8	0x00	Shutdown Reset
INT_STS_MSK	0x4D	8	0x00	Shutdown Reset:Bit7~Bit3, Bit1~Bit0 Por Reset:Bit2
IO_POL	0x50	8	0x02	Shutdown Reset
RESERVE_REG1	0x52	8	0x00	Shutdown Reset
RESERVE_REG2	0x53	8	0x00	Por Reset
OFF_SOURCE2	0xAD	8	0x00	Por Reset
ON_SOURCE	0xAE	8	0x00	Por Reset
OFF_SOURCE	0xAF	8	0x00	Por Reset
SYS_CFG1	0xB0	8	0x00	Por Reset
SYS_CFG2	0xB1	8	0x00	Shutdown Reset
EXIT_SLP_SEQ1	0xB2	8	0x00	Shutdown Reset
EXIT_SLP_SEQ2	0xB3	8	0x00	Shutdown Reset
EXIT_SLP_SEQ3	0xB4	8	0x00	Shutdown Reset
EXIT_SLP_SEQ4	0xB5	8	0x00	Shutdown Reset
ENTER_SLP_SEQ1	0xB6	8	0x00	Por Reset
ENTER_SLP_SEQ2	0xB7	8	0x00	Por Reset
ENTER_SLP_SEQ3	0xB8	8	0x00	Por Reset
ENTER_SLP_SEQ4	0xB9	8	0x00	Por Reset
LP_CFG	0xBE	8	0x00	Por Reset
SYS_CFG3	0xBF	8	0x00	Por Reset

5.2 Register Description

SECONDS
Address: (0x00)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7	RW	na	1'h0	Reserved
6:4	RW	sec1[2:0]	3'h0	BCD coding from 00 - 59
3:0	RW	sec0[3:0]	4'h0	BCD coding from 00 - 59

MINUTES
Address: (0x01)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7	RW	na	1'h0	Reserved
6:4	RW	min1[2:0]	3'h5	BCD coding from 00 - 59
3:0	RW	min0[3:0]	4'h0	BCD coding from 00 - 59

HOURS
Address: (0x02)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7	RW	ampm	1'h0	PM_AM: only used in PM-AM mode, 1, PM. 0,AM.
6	RW	na	1'h0	Reserved
5:4	RW	hour1[1:0]	2'h0	HOUR1/0 BCD coding form 0-11/23
3:0	RW	hour0[3:0]	4'h8	HOUR1/0 BCD coding form 0-11/23

DAYS
Address: (0x03)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:6	RW	na[1:0]	2'h0	Reserved
5:4	RW	day1[1:0]	2'h2	BCD coding from 01 - 28/29/30/31
3:0	RW	day0[3:0]	4'h1	BCD coding from 01 - 28/29/30/31

MONTHS
Address: (0x04)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:5	RW	na[2:0]	3'h0	Reserved
4	RW	month1	1'h0	BCD coding form 01 - 12
3:0	RW	month0[3:0]	4'h1	BCD coding form 01 - 12

YEARS
Address: (0x05)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:4	RW	year1[3:0]	4'h1	BCD coding form 00- 99
3:0	RW	year0[3:0]	4'h6	BCD coding form 00- 99

WEEKS
Address: (0x06)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:3	RW	na[4:0]	5'h0	Reserved
2:0	RW	week[2:0]	3'h4	BCD coding from 1-7

ALARM_SECONDS
Address: (0x08)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7	RW	na	1'h0	Reserved
6:4	RW	alarm_sec1[2:0]	3'h0	BCD coding from 00 - 59
3:0	RW	alarm_sec0[3:0]	4'h0	BCD coding from 00 - 59

ALARM_MINUTES
Address: (0x09)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7	RW	na	1'h0	Reserved
6:4	RW	alarm_min1[2:0]	3'h0	BCD coding from 00 - 59
3:0	RW	alarm_min1[3:0]	4'h0	BCD coding from 00 - 59

ALARM_HOURS
Address: (0x0A)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7	RW	alarm_am_pm	1'h0	PM_AM: only used in PM-AM mode, 1, PM. 0,AM.
6	RW	na	1'h0	Reserved
5:4	RW	alarm_hour1[1:0]	2'h0	HOUR1/0 BCD coding form 0-11/23
3:0	RW	alarm_hour0[3:0]	4'h0	HOUR1/0 BCD coding form 0-11/23

ALARM_DAYS
Address: (0x0B)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:6	RW	na[1:0]	2'h0	Reserved
5:4	RW	alarm_day1[1:0]	2'h0	BCD coding from 01 - 28/29/30/31
3:0	RW	alarm_day0[3:0]	4'h1	BCD coding from 01 - 28/29/30/31

ALARM_MONTHS
Address: (0x0C)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:5	RW	na[2:0]	3'h0	Reserved
4	RW	alarm_month1	1'h0	BCD coding form 01 - 12
3:0	RW	alarm_month0[3:0]	4'h1	BCD coding form 01 - 12

ALARM_YEARS
Address: (0x0D)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:4	RW	alarm_year1[3:0]	4'h0	BCD coding form 00- 99
3:0	RW	alarm_year0[3:0]	4'h0	BCD coding form 00- 99

RTC_CTRL
Address: (0x10)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7	RW	rtc_readsel	1'h0	RTC_READ_SEL: 0: Read Attr directly to dynamic registers 1, Read Attr to static shadowed registers
6	RW	get_time	1'h0	GET_TIME: rising transition of this register transferred dynamic registers into static shadowed registers.
5	RW	set_32_counter	1'h0	SET_32_COUNTER: 1: set the 32-kHz counter with COMP_REG value. It must only be used when the RTC is frozen.
4	RW	na	1'h0	
3	RW	ampm_mode	1'h0	AMPM_MODE: 0: 24 hours mode. 1,12 hours mode (PM-AM mode)
2	RW	auto_comp	1'h0	AUTO_COMP: 0, No auto compensation RW 0. 1, Auto compensation enabled
1	RW	round_30s (auto clr)	1'h0	ROUND_30S: 1: When 1 is written, the time is rounded to the closest minute in next second. self cleared after rounding
0	RW	stop_rtc	1'h0	STOP_RTC: 1: RTC is frozen 0: RTC is running. RTC_time can only be changed during RTC frozen

RTC_STATUS
Address: (0x11)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7	W1C	power_up	1'h1	POWER_UP: POWER_UP is set by a reset, is cleared by writing one in this bit.
6	W1C	alarm	1'h0	ALARM: Indicates that an alarm interrupt has been generated (bit clear by writing 1) The alarm interrupt keeps its low level, until the micro-controller write 1 in the ALARM bit of. Write this bit to clr d2a_rtc_alarm_out.
5	W1C	event_1d	1'h0	EVENT_1D: One day has occurred
4	W1C	event_1h	1'h0	EVENT_1H: One hour has occurred
3	W1C	event_1m	1'h0	EVENT_1M: One minute has occurred
2	W1C	event_1s	1'h0	EVENT_1S :One secondr has occurred
1	RO	run	1'h1	RUN:

				0, RTC is frozen. 1, RTC is running. This bit shows the real state of the RTC
0	RO	na	1'h0	Reserved

RTC_INT
Address: (0x12)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:5	RW	na[2:0]	3'h0	Reserved
4	RW	int_sleep_mask_en	1'h0	INT_SLEEP_MASK_EN: 1: Mask periodic interrupt while the device is in SLEEP mode 0: Normal mode, no interrupt masked.
3	RW	alarm_en	1'h0	Enable alarm. 1: Enable 0: Disable
2	RW	timer_en	1'h0	Enable periodic interrupt 1: Enable 0: Disable
1:0	RW	every[1:0]	2'h0	EVERY: 00: every second 01: every minute 10: every hour 11: every day

RTC_COMP_LSB
Address: (0x13)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:0	RW	rtc_comp_lsb[7:0]	8'h0	This register contains the number of 32-kHz periods to be added into the 32KHz counter every hour [LSB]

RTC_COMP_MSB
Address: (0x14)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:0	RW	rtc_comp_msb[7:0]	8'h0	This register contains the number of 32-kHz periods to be added into the 32KHz counter every hour [MSB]

CHIP_NAME
Address: (0x17)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:0	RO	chip_name[11:4]	8'h80	chip name: RK805

CHIP_VER
Address: (0x18)

Bits	Attr	Field	DEFAULT/ Reset Value	Description

7:4	RO	chip_name[3:0]	4'h5	chip name:from 1 max to 15
3:0	RO	chip_ver[3:0]	4'h3	chip version:from 1 max to 15

OTP_VER
Address: (0x19)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:4	RO	na[3:0]		Reserved
3:0	RO	otp_ver[3:0]	otp	OTP version: OTP revize version the default value is set by efuse.

CLK32KOUT
Address: (0x20)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:1	RW	resev	5'h0	Reserved
0	RW	clk32kout_en	1'h1	clk32kout_en: 1. CLK32KOUT output is enabled 0. CLK32KOUT output is disabled

VB_MON
Address: (0x21)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7	RO	pwron_sts	1'h0	PWRON key status 1: PWRON not press 0:PWRON button pressed
6	RW	na	1'h0	Reserved
5	RO	vcca_uv_sts	1'h0	VCCA under voltage lockout status(shut down system if the bit=1)
4	RW	vb_lo_act	1'h1	VCCA low voltage action 0: shut down system 1: insert interrupt
3	RO	vb_lo_sts	1'h0	VCCA low voltage status 0: VCCA VB_LO_SEL 1: VCCA VB_LO_SEL
2:0	RW	vb_lo_vsel[2:0]	3'h4	VCCA low voltage threshold 000~111: 2.8V~ 3.5V, step=100mV

THERMAL
Address: (0x22)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:5	RW	vb_uv_sel[2:0]	3'h0	VCCA low voltage selection to shut down system 000~111:2.7v~3.4v
4	RW	tsd_temp	1'h0	TSD_TEMP: Thermal shutdown temperture threshold 0: 140□; 1: 160□
3:2	RW	hotdie_temp[1:0]	2'h0	HOTDIE_TEMP: Hot-die temperature threshold 00:85□ 01:95□ 10:105□ 11:115□
1	RO	hotdie_sts	1'h0	HOTDIE_STS: Hot-die warning

0	RO	tsd_sts	1'h0	TSD_STS: Thermal shut down

DCDC_EN_REG1
Address: (0x23)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7	RW	buck4_en_mask	1'h0	MUST write them to "1" if want to change corresponding BUCK4_EN bit, the BUCK4_EN_MASK bits should be clear when BUCK4_EN bits have been written.
6	RW	buck3_en_mask	1'h0	MUST write them to "1" if want to change corresponding BUCK3_EN bit,the BUCK3_EN_MASK bits should be clear when BUCK3_EN bits have been written.
5	RW	buck2_en_mask	1'h0	MUST write them to "1" if want to change corresponding BUCK2_EN bit,the BUCK2_EN_MASK bits should be clear when BUCK2_EN bits have been written.
4	RW	buck1_en_mask	1'h0	MUST write them to "1" if want to change corresponding BUCK1_EN bit,the BUCK1_EN_MASK bits should be clear when BUCK1_EN bits have been written.
3	RW	buck4_en	otp	BUCK4 enable in active mode 1, Enable 0, Disable the default value is set by efuse.
2	RW	buck3_en	otp	BUCK3 enable in active mode 1, Enable 0, Disable the default value is set by efuse.
1	RW	buck2_en	otp	BUCK2 enable in active mode 1, Enable 0, Disable the default value is set by efuse.
0	RW	buck1_en	otp	BUCK1 enable in active mode 1, Enable 0, Disable the default value is set by efuse.

SLEEP_EN_REG1
Address: (0x25)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:4	RW	na[3:0]	4'h0	Reserved
3	RW	buck4_en_slp	otp	1, this channel is enable in sleep mode 0,this channel is disable in sleep mode
2	RW	buck3_en_slp	otp	1, this channel is enable in sleep mode 0,this channel is disable in sleep mode
1	RW	buck2_en_slp	otp	1, this channel is enable in sleep mode 0,this channel is disable in sleep mode
0	RW	buck1_en_slp	otp	1, this channel is enable in sleep mode 0,this channel is disable in sleep mode

SLEEP_EN_REG2
Address: (0x26)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:3	RW	na[3:0]	5'h0	Reserved
2	RW	ldo3_en_slp	otp	1, LDO is enable in sleep mode 0,this channel is disable in sleep mode
1	RW	ldo2_en_slp	otp	1, LDO is enable in sleep mode 0,this channel is disable in sleep mode
0	RW	ldo1_en_slp	otp	1, LDO is enable in sleep mode 0,this channel is disable in sleep mode

LDO_EN_REG1
Address: (0x27)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7	RW	na	1'h0	
6	RW	ldo3_en_mask	1'h0	LDO3_EN_MASK: MUST write them to "1" if want to change corresponding LDO3_EN bit,the LDO3_EN_MASK bits should be clear when LDO3_EN bits have been written.
5	RW	ldo2_en_mask	1'h0	LDO2_EN_MASK: MUST write them to "1" if want to change corresponding LDO2_EN bit,the LDO2_EN_MASK bits should be clear when LDO2_EN bits have been written.
4	RW	ldo1_en_mask	1'h0	LDO1_EN_MASK: MUST write them to "1" if want to change corresponding LDO1_EN bit,,the LDO1_EN_MASK bits should be clear when LDO1_EN bits have been written.
3	RW	na	1'h0	
2	RW	ldo3_en	otp	LDO3 enable in active mode 1, Enable 0, Disable the default value is set by efuse.
1	RW	ldo2_en	otp	LDO2 enable in active mode 1, Enable 0, Disable the default value is set by efuse.
0	RW	ldo1_en	otp	LDO1 enable in active mode 1, Enable 0, Disable the default value is set by efuse.

SLP_LP_EN
Address: (0x2A)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:2	RW	resev1	1'h0	Reserved
1	RW	buck_slp_lp_en	1'h0	Low power function enable bit of BUCK in sleep mode(active mode: d2a_buck_slp_lp_en=0) 0: disable 1:enable
0	RW	ldo_slp_lp_en	1'h0	Low power function enable bit of LDO in

				sleep mode(active mode: d2a_buck_slp_lp_en=0) 0: disable 1:enable

BUCK1_CONFIG
Address: (0x2E)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:6	RW	buck1_ilmax[1:0]	2'h1	BUCK1_ILMAX: 00:2.5A, 01:3A; 10:3.5A; 11:4A
5	RW	buck1_dischg_en	1'h1	BUCK1 discharge enable when the channle is off 0: Disable 1:enable
4:0	RW	resv[5:0]	5'h1A	Reserved

BUCK1_ON_VSEL
Address: (0x2F)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7	RW	buck1_fpwm_on	1'h0	1, Forced PWM mode in active mode. 0, PWM/PFM auto change mode.(default)
6:0	RW	buck1_on_vsel[6:0]	otp	when RK805B_CM_MODE=1: buck1 voltage select is 7bits. 0x00:0.5V, 0x01:0.5125V, 0x02:0.525V, … 0x4c:1.45V; 0x4d:1.8V, 0x4e:2V, 0x4f:2.2V, 0x50 and above: 2.3V; when RK805B_CM_MODE=0: buck1 voltage select is 6bits. 0x00:0.7125V, 0x01:0.725V, 0x02:0.7375V, … 0x3b:1.45V; 0x3c:1.8V, 0x3d:2V, 0x3e:2.2V, 0x3f: 2.3V;

BUCK1_SLP_VSEL
Address: (0x30)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7	RW	buck1_fpwm_slp	1'h0	1, Forced PWM mode in sleep mode. 0, PWM/PFM auto change mode.(default)
6:0	RW	buck1_slp_vsel[6:0]	otp	when RK805B_CM_MODE=1: buck1 voltage select is 7bits. 0x00:0.5V, 0x01:0.5125V, 0x02:0.525V, … 0x4c:1.45V; 0x4d:1.8V, 0x4e:2V, 0x4f:2.2V, 0x50 and above: 2.3V; when RK805B_CM_MODE=0: buck1 voltage select is 6bits. 0x00:0.7125V, 0x01:0.725V, 0x02:0.7375V, … 0x3b:1.45V; 0x3c:1.8V, 0x3d:2V, 0x3e:2.2V, 0x3f:

				2.3V;

BUCK2_CONFIG
Address: (0x32)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:6	RW	buck2_ilmax[1:0]	2'h1	BUCK2_ILMAX: 00:2.5A, 01:3A; 10:3.5A; 11:4A
5	RW	buck2_dischg_en	1'h1	BUCK1 discharge enable when the channle is off 0: Disable 1:enable
4:0	RW	resv[5:0]	5'h1A	Reserved

BUCK2_ON_VSEL
Address: (0x33)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7	RW	buck2_fpwm_on	1'h0	1, Forced PWM mode in active mode. 0, PWM/PFM auto change mode.(default)
6:0	RW	buck2_on_vsel[6:0]	otp	when RK805B_CM_MODE=1: buck2 voltage select is 7bits. 0x00:0.5V, 0x01:0.5125V, 0x02:0.525V, … 0x4c:1.45V; 0x4d:1.8V, 0x4e:2V, 0x4f:2.2V, 0x50 and above: 2.3V; when RK805B_CM_MODE=0: buck2 voltage select is 6bits. 0x00:0.7125V, 0x01:0.725V, 0x02:0.7375V, … 0x3b:1.45V; 0x3c:1.8V, 0x3d:2V, 0x3e:2.2V, 0x3f: 2.3V;

BUCK2_SLP_VSEL
Address: (0x34)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7	RW	buck2_fpwm_slp	1'h0	1, Forced PWM mode in sleep mode. 0, PWM/PFM auto change mode.(default)
6:0	RW	buck2_slp_vsel[6:0]	otp	when RK805B_CM_MODE=1: buck2 voltage select is 7bits. 0x00:0.5V, 0x01:0.5125V, 0x02:0.525V, … 0x4c:1.45V; 0x4d:1.8V, 0x4e:2V, 0x4f:2.2V, 0x50 and above: 2.3V; when RK805B_CM_MODE=0: buck2 voltage select is 6bits. 0x00:0.7125V, 0x01:0.725V, 0x02:0.7375V, … 0x3b:1.45V; 0x3c:1.8V, 0x3d:2V, 0x3e:2.2V, 0x3f: 2.3V;

BUCK3_CONFIG
Address: (0x36)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7	RW	buck3_fpwm_on	1'h0	1, Forced PWM mode in active mode. 0, PWM/PFM auto change mode.(default)
6	RW	resv1	1'h0	Reserved
5	RW	buck3_dischg_en	1'h1	BUCK3 discharge enable when the channle is off 0: Disable 1:enable
4:3	RW	buck3_ilmax[1:0]	2'h1	BUCK3_ILMAX: 00: 1.5A, 01: 2A; 10:2.5A; 11:3A
2:0	RW	resv[2:0]	3'h0	Reserved

BUCK4_CONFIG
Address: (0x37)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:6	RW	na	1'h0	Reserved
5	RW	buck4_dischg_en	1'h1	BUCK4 discharge enable when the channle is off 0: Disable 1:enable
4:3	RW	buck4_ilmax[1:0]	2'h1	BUCK4_ILMAX: 00: 2A, 01: 2.5A; 10:3A; 11:3.5A
2:0	RW	resv[2:0]	3'h0	Reserved

BUCK4_ON_VSEL
Address: (0x38)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7	RW	buck4_fpwm_on	1'h0	1, Forced PWM mode in active mode. 0, PWM/PFM auto change mode.(default)
6	RW	na	1'h0	Reserved
5:0	RW	buck4_slp_vsel[5:0]	otp	when RK805B_CM_MODE=1: buck4 voltage select is 6bits. 0x00:0.5V, 0x01:0.55V, 0x02:0.6V, … 0x3a and above: 3.4V; when RK805B_CM_MODE=0: buck4 voltage select is 5bits. 0x00:0.8V, 0x01:0.9V, 0x02:1V, … 0x1a and above: 3.4V;

BUCK4_SLP_VSEL
Address: (0x39)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7	RW	buck4_fpwm_slp	1'h0	1, Forced PWM mode in sleep mode. 0, PWM/PFM auto change mode.(default)
6	RW	na	1'h0	

5:0	RW	buck4_slp_vsel[5:0]	otp	when RK805B_CM_MODE=1: buck4 voltage select is 6bits. 0x00:0.5V, 0x01:0.55V, 0x02:0.6V, … 0x3a and above: 3.4V; when RK805B_CM_MODE=0: buck4 voltage select is 5bits. 0x00:0.8V, 0x01:0.9V, 0x02:1V, … 0x1a and above: 3.4V;

LDO1_ON_VSEL
Address: (0x3B)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7	RW	ldo1_dischg_en_ver1	1'h1	this bit is ldo1_dischg_en function.
6	RW	ldo1_imax	1'h0	LDO1 current limit setting 0: normal, 1: 130% of norminal value
5:0	RW	ldo1_dischg_en_ver0_ldo1_on_vsel[5:0]	1'h1/otp	when RK805B_CM_MODE=0: this bit is ldo1_dischg_en function. And ldo1 voltage select is 5bits. 0x00:0.8V, 0x01:0.9V, 0x02:1V, … 0x1a and above: 3.4V; when RK805B_CM_MODE=1: ldo1 voltage select is 6bits, and this bit is ldo1_on_vsel[5]. 0x00:0.5V, 0x01:0.55V, 0x02:0.6V, … 0x3a and above: 3.4V;

LDO1_SLP_VSEL
Address: (0x3C)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:6	RW	na[1:0]	2'h0	Reserved
5:0	RW	ldo1_slp_vsel[5:0]	otp	when RK805B_CM_MODE=0: ldo1 voltage select is 5bits. 0x00:0.8V, 0x01:0.9V, 0x02:1V, … 0x1a and above: 3.4V; when RK805B_CM_MODE=1: ldo1 voltage select is 6bits, and this bit is ldo1_slp_vsel[5]. 0x00:0.5V, 0x01:0.55V, 0x02:0.6V, … 0x3a and above: 3.4V;

LDO2_ON_VSEL
Address: (0x3D)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7	RW	ldo2_dischg_en_ver1	1'h1	this bit is ldo2_dischg_en function.
6	RW	ldo2_imax	1'h0	LDO2 current limit setting 0: normal, 1: 130% of norminal value

5:0	RW	ldo2_dischg_en_ver0_ldo2_on_vsel[5:0]	1'h1/otp	when RK805B_CM_MODE=0: this bit is ldo2_dischg_en function. And ldo2 voltage select is 5bits. 0x00:0.8V, 0x01:0.9V, 0x02:1V, … 0x1a and above: 3.4V; when RK805B_CM_MODE=1: ldo2 voltage select is 6bits, and this bit is ldo2_on_vsel[5]. 0x00:0.5V, 0x01:0.55V, 0x02:0.6V, … 0x3a and above: 3.4V;

LDO2_SLP_VSEL
Address: (0x3E)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:6	RW	na[1:0]	2'h0	Reserved
5:0	RW	ldo2_slp_vsel[5:0]	otp	when RK805B_CM_MODE=0: ldo2 voltage select is 5bits. 0x00:0.8V, 0x01:0.9V, 0x02:1V, … 0x1a and above: 3.4V; when RK805B_CM_MODE=1: ldo2 voltage select is 6bits, and this bit is ldo2_slp_vsel[5]. 0x00:0.5V, 0x01:0.55V, 0x02:0.6V, … 0x3a and above: 3.4V;

LDO3_ON_VSEL
Address: (0x3F)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7	RW	ldo3_dischg_en_ver1	1'h1	this bit is ldo3_dischg_en function.
6	RW	ldo3_imax	1'h0	LDO3 current limit setting 0: normal, 1: 130% of norminal value
5:0	RW	ldo3_dischg_en_ver0_ldo3_on_vsel[5:0]	1'h1/otp	when RK805B_CM_MODE=0: this bit is ldo3_dischg_en function. And ldo3 voltage select is 5bits. 0x00:0.8V, 0x01:0.9V, 0x02:1V, … 0x1a and above: 3.4V; when RK805B_CM_MODE=1: ldo3 voltage select is 6bits, and this bit is ldo3_on_vsel[5]. 0x00:0.5V, 0x01:0.55V, 0x02:0.6V, … 0x3a and above: 3.4V;

LDO3_SLP_VSEL
Address: (0x40)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:6	RW	na[1:0]	2'h0	

5:0	RW	ldo2_slp_vsel[5:0]	otp	when RK805B_CM_MODE=0: ldo3 voltage select is 5bits. 0x00:0.8V, 0x01:0.9V, 0x02:1V, … 0x1a and above: 3.4V; when RK805B_CM_MODE=1: ldo3 voltage select is 6bits, and this bit is ldo3_slp_vsel[5]. 0x00:0.5V, 0x01:0.55V, 0x02:0.6V, … 0x3a and above: 3.4V;

PWRON_LP_SEL
Address: (0x47)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7	RW	na	1'h0	
6:5	RW	pwron_lp_int_time l[1:0]	2'h1	PWRON_LP_TM_SEL[1:0]:PWRON long press interupt time selection: Relevant to Reg4C[3]. 00: 0.5S 01:1S 10:1.5S 11:2S
4:0	RW	na[4:0]	5'h0	Reserved

PWRON_DB_SEL
Address: (0x48)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7	RW	na	1'h0	Reserved
6:5	RW	pwron_db_sel[1:0]	2'h2	PWRON_DB_SEL[1:0]:PWRON interrupt debounce time selection: Relevant to Reg21[7]. 00: 230uS 01:10mS 10:20mS 11:40mS
4:0	RW	na[4:0]	5'h0	Reserved

DEVCTRL
Address: (0x4B)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7	RW	int_fc_en	1'h0	interrupt watchdog function enable 0:disable. Normal interrupt mode, when interrupt occurred, the INT pin would be active until be cleared. 1:enable, it means when interrupt occurred, the INT pin would be a rectangular wave,the frequency is 2S, non-active time is 10ms.
6	RW	pwron_lp_act	1'h0	PWRON_LP_ACT: PWRON long press act. 0: turn off (But if USB effective,then it will be start again) 1: turn off and then restart
5:4	RW	pwron_lp_off_time [1:0]	2'h0	PWRON_LP_OFF_TIME: PWRON long press time:

				00: 6s, 01: 8s, 10: 10s, 11: 12s
3	RW	dev_rst	1'h0	Write 1 will trigger a RST action.
2	RW	na	1'h0	
1	RW	dev_slp	1'h0	either this bit = 1 or SLEEP pin active edge trigger, enter sleep mode; both this bit =0 or SLEEP pin non-active active edge trigger, exit sleep mode;
0	RW	dev_off	1'h0	Write 1 will start an ACTIVE to OFF or SLEEP to OFF device state transition.

INT_STS
Address: (0x4C)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7	W1C	pwron_fall_int	1'h0	PWRON falling event interrupt 1, Interrupt asserted, write "1" to clear 0, No interrupt
6	W1C	rtc_period_int	1'h0	RTC period event interrupt. 1, Interrupt asserted, write "1" to clear 0, No interrupt
5	W1C	rtc_alarm_int	1'h0	RTC alarm event interrupt. 1, Interrupt asserted, write "1" to clear 0, No interrupt
4	W1C	hotdie_int	1'h0	Hot die event interrupt status. 1, Interrupt asserted, write "1" to clear 0, No interrupt
3	W1C	pwron_lp_int	1'h0	PWRON PIN long press event interrupt status. 1, Interrupt asserted, write "1" to clear 0, No interrupt
2	W1C	pwron_int	1'h0	PWRON start up event interrupt status. 1, Interrupt asserted, write "1" to clear 0, No interrupt
1	W1C	vb_lo_int	1'h0	VCCA under voltage alarm event interrupt status. 1, Interrupt asserted, write "1" to clear 0, No interrupt
0	W1C	pwron_rise_int	1'h0	PWRON rising event interrupt 1, Interrupt asserted, write "1" to clear 0, No interrupt

INT_STS_MSK
Address: (0x4D)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7	RW	pwron_fall_int_im	1'h0	1, Mask specified interrupt 0, Do not mask specified interrupt
6	RW	rtc_period_im	1'h0	1, Mask specified interrupt 0, Do not mask specified interrupt
5	RW	rtc_alarm_im	1'h0	1, Mask specified interrupt 0, Do not mask specified interrupt
4	RW	hotdie_im	1'h0	1, Mask specified interrupt

				0, Do not mask specified interrupt
3	RW	pwron_lp_im	1'h0	1, Mask specified interrupt 0, Do not mask specified interrupt
2	RW	pwron_im	1'h0	1, Mask specified interrupt 0, Do not mask specified interrupt
1	RW	vb_lo_im	1'h0	1, Mask specified interrupt 0, Do not mask specified interrupt
0	RW	pwron_rise_int_im	1'h0	1, Mask specified interrupt 0, Do not mask specified interrupt

IO_POL
Address: (0x50)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:4	RW	na[3:0]	4'h0	Reserved
3:2	RW	slp_fun[1:0]	2'h0	SLEEP PIN function selection: 00: not effect; 01: sleep function; 10:shutdown function; 11:trigger a RST action
1	RW	slp_pol	1'h1	SLEEP pin polarity 0: active low 1:active high
0	RW	int_pol	1'h0	INT pin polarity 0: active low 1: active high

RESERVE_REG1
Address: (0x52)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:2	RW	reserved[5:0]	6'h0	Reserved
1	RW	out2	1'h0	output 2 to pin
0	RW	out1	1'h0	output 1 to pin

RESERVE_REG2
Address: (0x53)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:1	RW	reserved_por[7:1]	8'h0	Reserved
0	RW	clk32kout_en_blk	1'h0	1, Mask clk32kout_en 0, Do not mask clk32kout_en Note:Only used for Master mode

OFF_SOURCE2
Address: (0xAD)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:2	RO	na	6'h0	Reserved
1	RO	off_vcc1_uv	1'h0	VCC1 UV to turn off PMU
0	RO	off_resetb_sync	1'h0	PULL low the RESETB PIN to shutdown the PMU when SYNC at low level

ON_SOURCE

Address: (0xAE)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7	RO	on_pwron	1'h0	PRESS PWRON to turn on PMU
6	RO	on_en	1'h0	Pull high EN PIN to turn on PMU
5	RO	on_rtc	1'h0	RTC timer to turn on PMU
4	RO	restart_resetb	1'h0	PULL low the RESETB PIN to restart the PMU
3	RO	restart_pwron_lp	1'h0	Long press PWRON to restart the PMU
2	RO	restart_sleep	1'h0	SLEEP pin to restart the PMU
1	RO	restart_dev_rst	1'h0	write dev_rst register to restart the PMU
0	RO	na	1'h0	Reserved

OFF_SOURCE
Address: (0xAF)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7	RO	off_en	1'h0	Pull low EN PIN to turn off PMU
6	RO	off_vcca_ov	1'h0	VCCA OV to turn off PMU
5	RO	off_tsd	1'h0	TSD to turn off PMU
4	RO	off_vcca_uv	1'h0	VCCA UV to turn off PMU
3	RO	off_dev_off	1'h0	I2C write DEV_OFF to turn off PMU
2	RO	off_pwron_lp	1'h0	long press PWRON to turn off PMU
1	RO	off_sleep	1'h0	SLEEP PIN ACTIVE to turn off PMU
0	RO	off_vcca_lo	1'h0	VCCA Low (if Reg21[4]vb_lo_act=0)to turn off PMU

SYS_CFG1
Address: (0xB0)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7	RW	rtc_alarm_int_st_en	1'h0	1: rtc_alarm_int will trigger pmu start up; 0:rtc_alarm_int will NOT trigger pmu start up;
6	RW	vb_lo_dbt	1'h0	1:2ms; 0:30uS;
5	RW	vb_lo_opt	1'h0	1:vb_lo threhold=4.3V; 0:vb_lo threhold set by reg21[3]
4:3	RW	pwron_st_time_base[1:0]	2'h0	00:500mS 01:100mS ; 10:20mS;11:40mS;
2:0	RW	pwron_st_time_add[2:0]	3'h0	the PWRON pin start up debounce time=pwron_st_time_add[2:0]+pwron_st_time_base[1:0]. pwron_st_time_add[2:0]: 000:0mS; 001: 20ms; 010:100ms, 011:500ms; 100:1000ms; 101:1500ms, 110:2000ms; 111: 3000ms; default: 000

SYS_CFG2
Address: (0xB1)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:6	RW	rst_fun[1:0]	1'h0	rst_fun[1:0]:this is define the action by RST. 00:restart pmu; 01:reset all register that Reset source=RST, and force exit SLEEP mode; 1x:reset all register that Reset source=RST, and force exit SLEEP mode, and ties low RESETB pin for 5ms. Notice: Write reg4B[3]=1, or pull low RESETB pin, or SLEEP pin active && slp_fun=11, will trigger one time RST action.
5	RW	slp_function_work	1'h0	0: noraml mode; 1: after exit sleep mode, the reg50[3:2](slp_fun) will be reset to 0.
4	RW	int_function	1'h0	0:when interrupt occurred, only effect the INT pin and INT reg; 1:when interrupt occurred, not only effect the INT pin and INT reg, but also exit sleep mode.
3:2	RW	exit_slp_dly	2'h0	when enter sleep mode: firstly, the ENTER_SLP_SEQ goes, and delay this time. Even if exiting sleep condtion occurs, it must be exited after this delay time. ENTER_SLP_SEQ->delay->EXIT_SLP_SEQ 00: 0ms; 01:10ms; 10:20ms; 11:50ms
1	RW	exit_slp_int	1'h0	1: when INT to trigger exit sleep: trigger INT after exit_slp_dly. 0: when INT to trigger exit sleep: trigger INT immediately.
0	RW	na	1'h0	Reserved

EXIT_SLP_SEQ1
Address: (0xB2)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:4	RW	exit_slp_buck1_seq[3:0]	4'h0	exit sleep mode, sequence contro reg.
3:0	RW	exit_slp_buck2_seq[3:0]	4'h0	exit sleep mode, sequence contro reg.

EXIT_SLP_SEQ2
Address: (0xB3)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:4	RW	exit_slp_buck3_seq[3:0]	4'h0	exit sleep mode, sequence contro reg.
3:0	RW	exit_slp_buck4_seq[3:0]	4'h0	exit sleep mode, sequence contro reg.

EXIT_SLP_SEQ3
Address: (0xB4)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:4	RW	exit_slp_ldo1_seq[3:0]	4'h0	exit sleep mode, sequence contro reg.
3:0	RW	exit_slp_ldo2_seq[3:0]	4'h0	exit sleep mode, sequence contro reg.

EXIT_SLP_SEQ4
Address: (0xB5)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:4	RW	exit_slp_ldo3_seq[3:0]	4'h0	exit sleep mode, sequence contro reg.
3:0	RW	na[3:0]	4'h0	Reserved

ENTER_SLP_SEQ1
Address: (0xB6)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:4	RW	enter_slp_buck1_seq[3:0]	4'h0	enter sleep mode or shutdown, sequence contro reg.
3:0	RW	enter_slp_buck2_seq[3:0]	4'h0	enter sleep mode or shutdown, sequence contro reg.

ENTER_SLP_SEQ2
Address: (0xB7)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:4	RW	enter_slp_buck3_seq[3:0]	4'h0	enter sleep mode or shutdown, sequence contro reg.
3:0	RW	enter_slp_buck4_seq[3:0]	4'h0	enter sleep mode or shutdown, sequence contro reg.

ENTER_SLP_SEQ3
Address: (0xB8)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:4	RW	enter_slp_ldo1_seq[3:0]	4'h0	enter sleep mode or shutdown, sequence contro reg.
3:0	RW	enter_slp_ldo2_seq[3:0]	4'h0	enter sleep mode or shutdown, sequence contro reg.

ENTER_SLP_SEQ4
Address: (0xB9)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:4	RW	enter_slp_ldo3_seq[3:0]	4'h0	enter sleep mode or shutdown, sequence contro reg.

3:0	RW	na[3:0]	4'h0	Reserved

DATA1
Address: (0xBA)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:0	RW	data[7:0]	8'h0	for soft ware use.

DATA2
Address: (0xBB)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:0	RW	data[7:0]	8'h0	for soft ware use.

DATA3
Address: (0xBC)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:0	RW	data[7:0]	8'h0	for soft ware use.

DATA4
Address: (0xBD)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:0	RW	data[7:0]	8'h0	for soft ware use.

LP_CFG
Address: (0xBE)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7:5	RW	na[3:0]	1'h0	Reserved
4	RW	rtc_en_mask	1'h0	rtc_en_mask: MUST write them to "1" if want to change corresponding RTC_EN bit
3	RW	na	1'h0	
2	RW	en_pd_res_open	1'h0	1:open the EN pin pull down resistor ; 0: EN pin 800k pull down
1	RW	na	1'h0	
0	RW	rtc_en	1'h1	1:rtc block clk input enable; 0:rtc block clk input disable; the RTC will do NOT work.

SYS_CFG3
Address: (0xBF)

Bits	Attr	Field	DEFAULT/ Reset Value	Description
7	RO	vcca_ov	1'h0	VCCA ov status
6	RO	vcc1_uv	1'h0	VCC1 uv status
5	RW	uvdly_opt	1'h0	vb uv analog delay option.
4	RW	buck1_dischrg_opt	1'h0	1:discharge resistance=50R; 0:250R
3	RW	buck2_dischrg_opt	1'h0	1:discharge resistance=50R; 0:250R

2	RW	na	1'h0	Reserved
1:0	RW	off_time_sel[1:0]	1'h0	power down wait time selection. 00:128ms; 01:160ms 10:192ms; 11:255ms;

Chapter 6 Thermal Management

6.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature of RK805B has to be below 125° C.

Depending on the thermal mechanical design (Smartphone, Tablet, Personal Navigation Device, etc), the system thermal management software and worst case thermal applications, the junction temperature might be exposed to higher values than those specified above.

Therefore, it is recommended to perform thermal simulations at device level (Smartphone, Tablet, Personal Navigation Device, etc) with the measured power of the worst case UC of the device.

6.2 Package Thermal Characteristics

Table 6-1 provides the thermal resistance characteristics for the package used on this device.

Table 6-1 Thermal Resistance Characteristics

Symbol	Description	Value	Unit	Note
θ_{JA}	Junction-to-ambient thermal resistance	26.13	(□/W)	(1)
θ_{JB}	Junction-to-board thermal resistance	9.04	(□/W)	(2)
θ_{JC}	Junction-to-case thermal resistance	42.54	(□/W)	(3)
ψ_{JT}	Thermal characterization parameter	1.05	(□/W)	(4)

Note (1): The package-board system is placed in the natural convection (JEDEC JESD51-2 standard), and the high effective thermal conductivity test board(2S2P) is designed in accordance with JESD 51-7 & JESD 51-5. The actual system design and environment may be different.（The PCB is 4 layers, 114.5 mm*72.6 mm）

Note (2): θJB is measured in the special environment (JEDEC JESD51-8 standard), and the printed circuit board used to mount the devices is specified in JESD51-7.

Note (3): The thermal resistance θJC is provided in compliance with the JEDEC JESD51-14.

Note (4): ψJT - The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package, ψJT is measured in the test environment of θJA (JEDEC JESD51-2 standard).