Rockchip RK809B2 Datasheet

Revision 1.0
Jan. 2026

Revision History

Date	Revision	Description
2026-01-13	1.0	Initial Release

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Chapter 1 Introduction

1.1 Overview

The RK809B2 is a complex power-management integrated circuit (PMIC) integrated CODEC for multi-core system applications powered by an external power supply. The RK809B2 can provide a complete power management solution with very few external components.

The RK809B2 provides five fast load transient synchronous step-down converters. The device also contains 7 LDO regulators, two switches and a battery fuel gauge. Power-up/power-down controller is configurable and can support any customized power-up/power-down sequences (OTP based). A real-time clock (RTC) is also integrated to provide a 32.768-kHz output buffer, and real time function. The RK809B2 supports 32.768-kHz clock generation based on a crystal oscillator. It also includes PD interface, Audio CODEC , real ground Head phone driver and ClassD driver.

The RK809B2 integrates four channels step-down DC-DC converters. All of them adopt ripple base control to achieve very fast load transient response. Meanwhile, all of them can dynamically adjust the output voltage, as required by the processor based on the processor's operation status so as to maximize the system efficiency. The output voltages of most channels can be configured through the I2C interface. The inputs of all channels have soft start function, which greatly reduces the inrush current at the startup. 2.5MHz switching frequency and good control method decrease the external inductance and capacitance. The RK809B2 also integrate a peak current mode control high efficiency buck converter, maximum current up to 2.5A, it's usually used to power LDOs.

The RK809B2 integrates seven channels LDO regulators. The inputs of all LDO regulators could be decrease to 2V for high convert efficiency. The output voltages of all LDO regulators can be configured through the I2C interface.

A "battery fuel gauge" is integrated in the RK809B2. Using the proprietary algorithms and the sensed battery current and voltage, the gauge can accurately calculate the battery capacity based on the charging/discharging characteristics of the battery preloaded in the system. The gauge then sends the battery capacity information to the processor through the I2C interface.

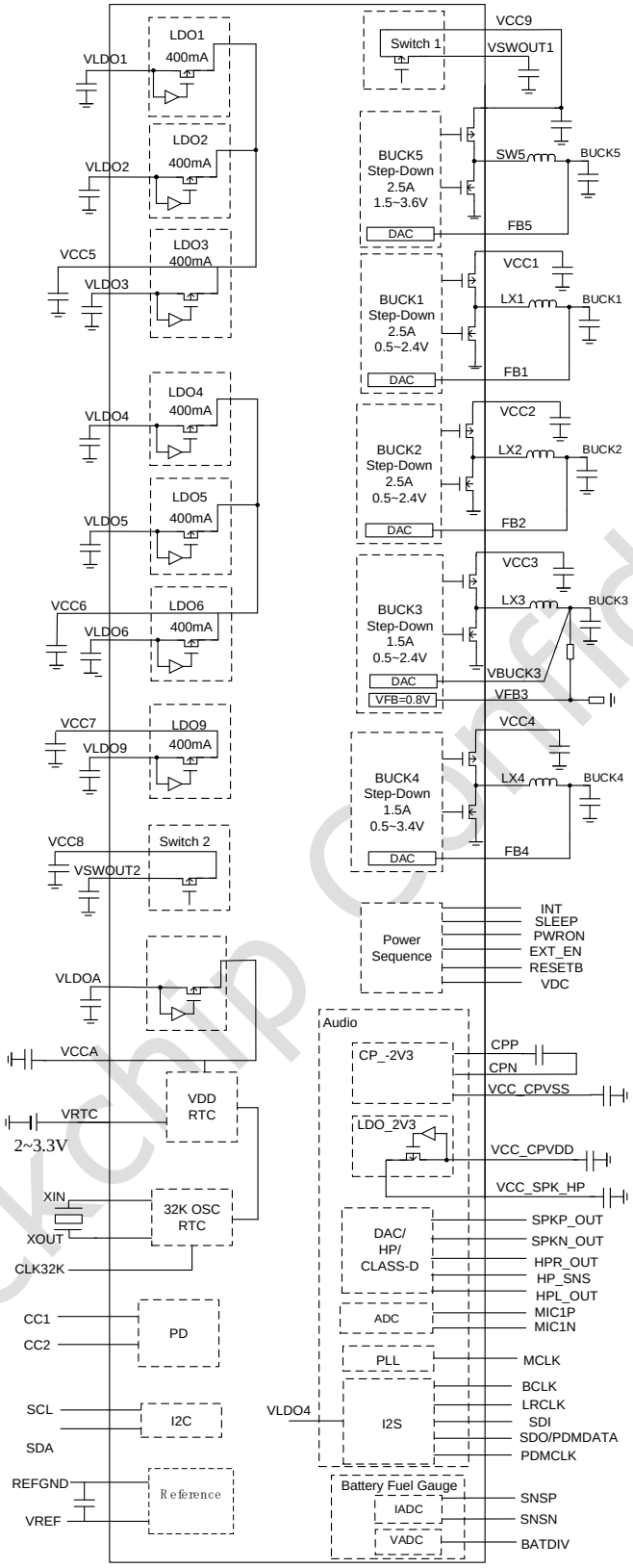
The RK809B2 also integrates complete audio system. The single end or differential mode Micro-phone can be connected to RK809B2 through two AC-couple capacitors. 24-bits ADC and gain adjustable PGA would convert the micro-phone signal to digital signal. The sound recording path has very low THD (-75dB @1KHz@580mV source). 24 bits DAC would convert digital signal to analog signal, and Class-AB driver adopt real-ground structure for Head-phone application, has very low THD (-90dB @1KHz@-3dBFS source). Meanwhile, Class-D driver integrated for speaker application. The speaker and head-phone can be used at the same time. I2S interface is integrated to communicate with processor.

The RK809B2 is available in a QFN68 7.0 mm x 7.0 mm package, with a 0.35-mm pin pitch.

1.2 Feature

- Input range: 2.7V - 5.5V
- Low standby current of 18 uA
- Power channels:
  - BUCK1: 0.5V~2.4V, 2.5A max, very fast transient response
  - BUCK2: 0.5V~2.4V, 2.5A max, very fast transient response
  - BUCK3: 0.5V~2.4V (or resistor divider), 1.5A max, very fast transient response
  - BUCK4: 0.5V~3.4V, 1.5A max, very fast transient response
  - BUCK5: 1.5V~3.6V, 2.5 A max, fast transient response
  - LDO1~LDO6,LDO9: 0.6V~3.4V, 400mA max
  - Switch1: 2.1 A max, Rdson=90mΩ
  - Switch2: 2.1 A max, Rdson=100mΩ
  - OTP Programmable power up/down sequences and voltage
- Accurate battery fuel gauge with two separate battery voltage and current ADC
  - 16 bits ADC for battery voltage
  - 16 bits ADC for battery current sense
  - OCV algorithm combine with Coulom-counter algorithm
- Real time clock（RTC）
- PD interface
- Audio System
  - Audio codec: 24bits for both ADC and DAC
  - Support single end or differential mode Micro-phone input
  - Support real ground class-AB PA to drive Head-phone, 32Ohm Load
  - Support class-D PA to drive speaker, 1.3W
  - Support I2S as the digital signal interface for both DAC and ADC
  - Support programmable digital and analog gains
  - Sample rate: 48KHz~192KHz
  - Integrates internal PLL
  - Support PDM mode(external input PCLK)
- Package:7mmx7mm QFN68

1.3 Block Diagram



Note: 1. The detail audio block diagram is shown at chapter "4.4 Audio System".
2. The I2S interface is internal pull high to VLDO4.

Fig. 1-1 RK809B2 Functional Block Diagram

1.4 Typical Application Diagrams

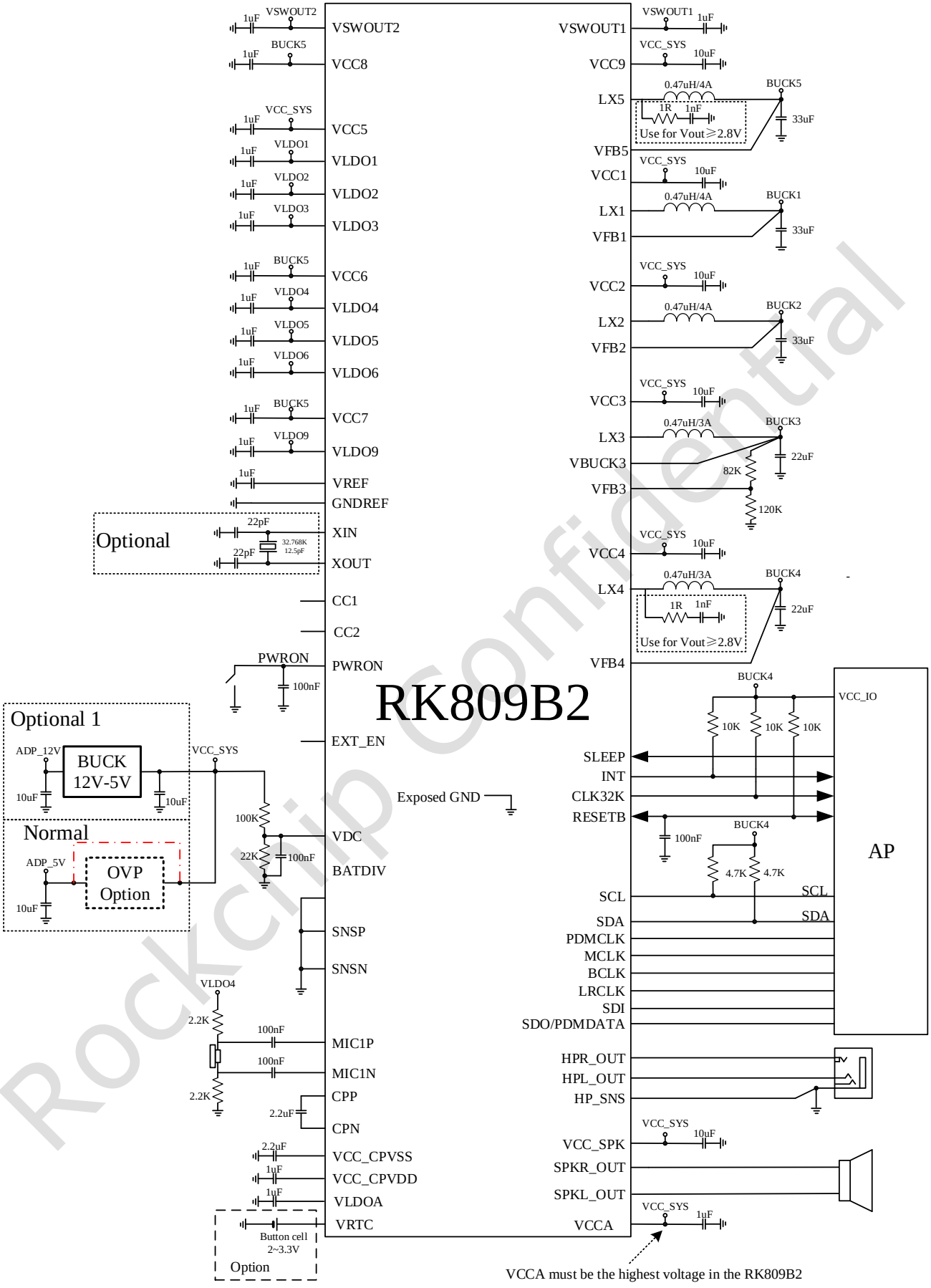


Fig. 1-2 RK809B2 Typical Application Diagram for no battery

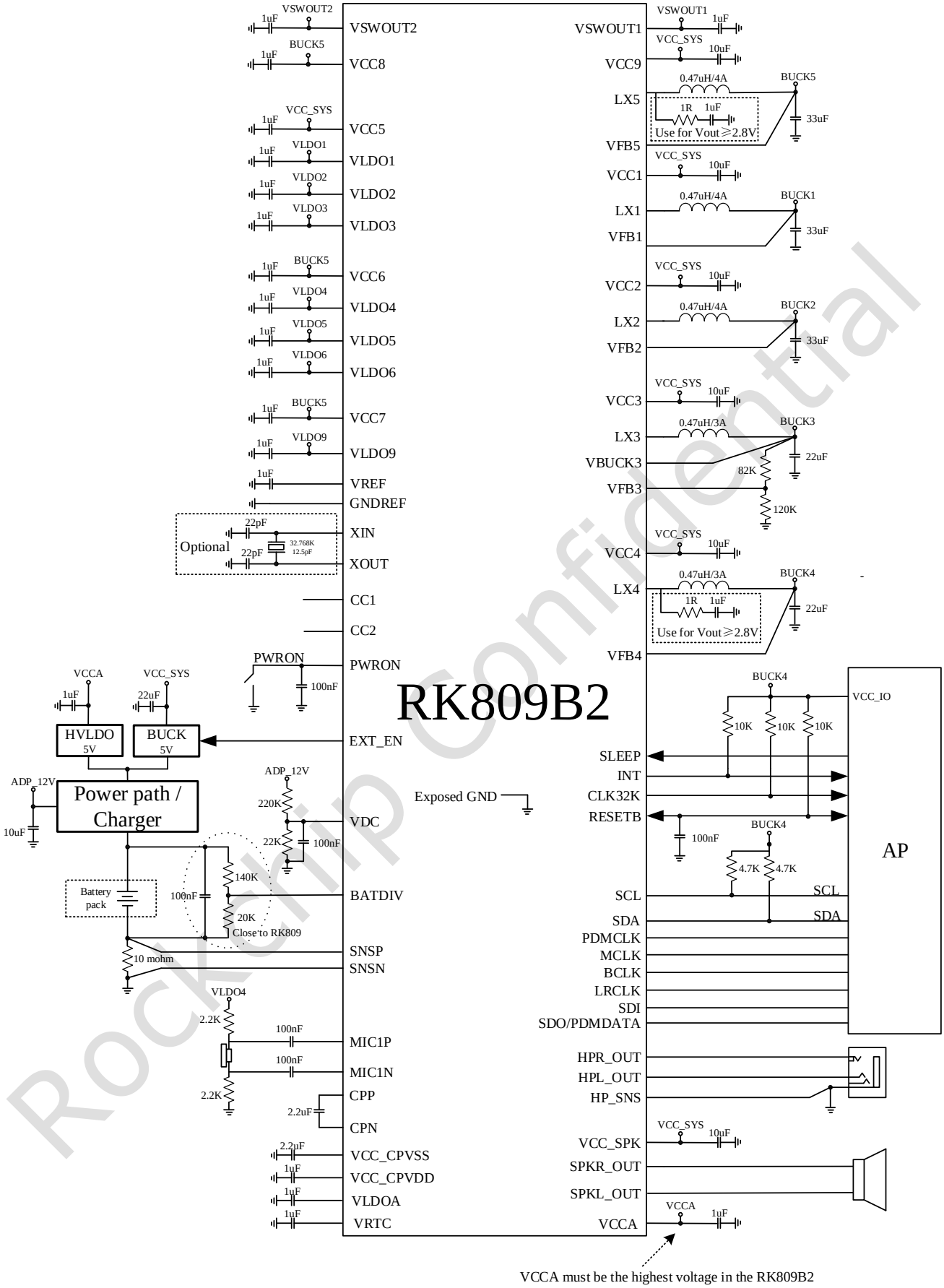


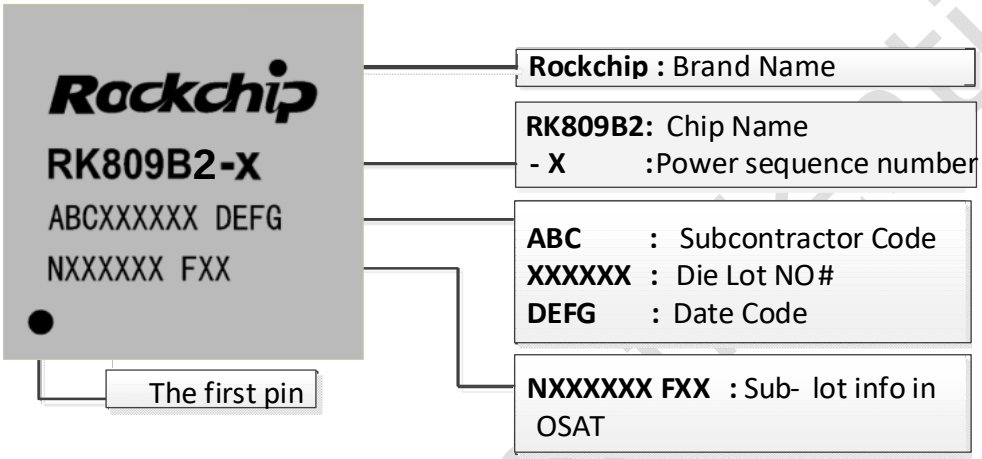
Fig. 1-3 RK809B2 Typical Application Diagram for two battery

Chapter 2 Package information

2.1 Ordering information

Orderable Device	RoHS status	Package	Package Detail
RK809B2-X	RoHS	QFN68 (7X7)	2000 pcs/ tape, 5 tapes/box, by reel

2.2 Top Marking



2.3 MSL Information

Moisture sensitivity Level ： MSL3

2.4 Lead Finish/Pin Material Information

Lead Finish/Pin Material ： Sn

2.5 Dimension

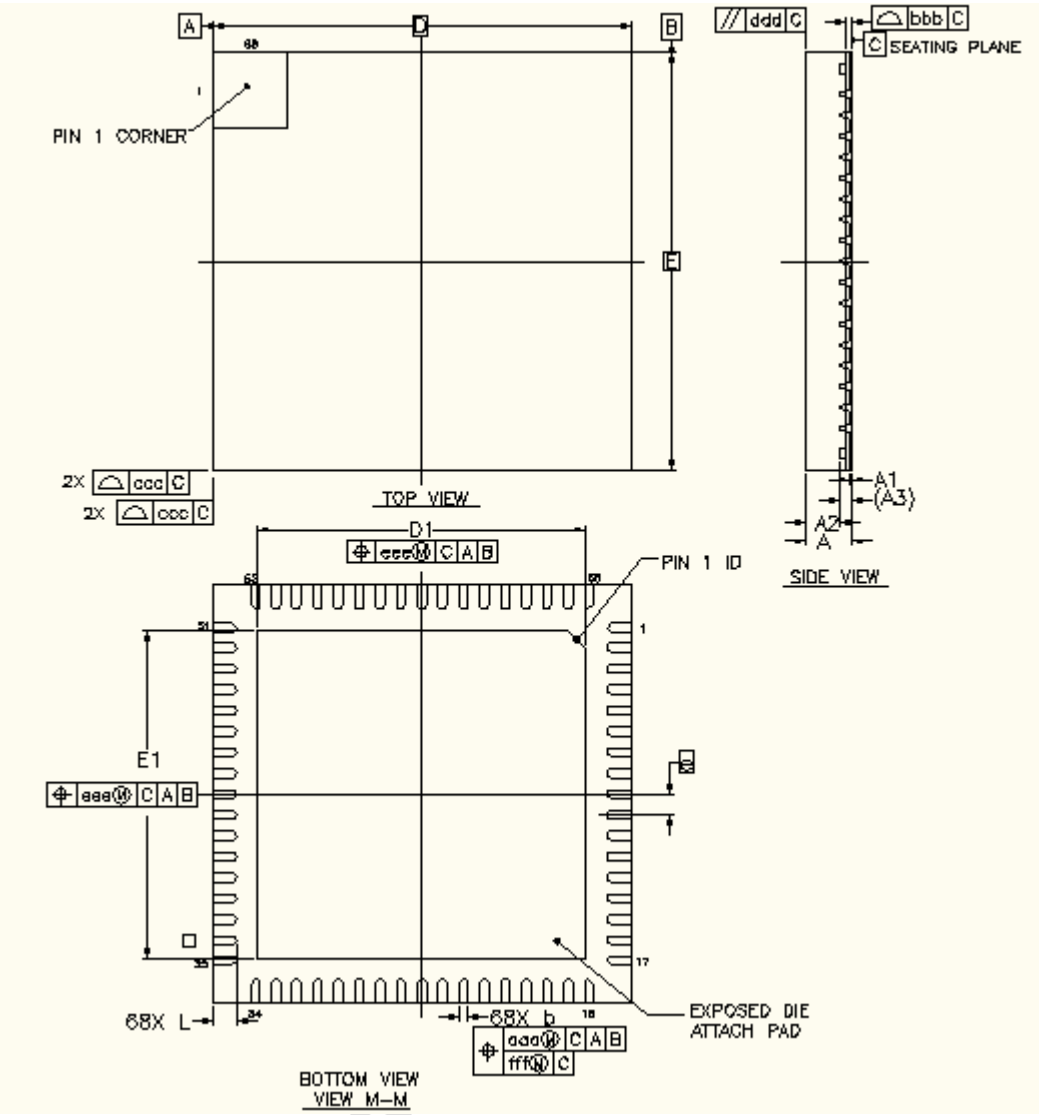


Fig. 2-1 QFN687mm X 7mm

DESCRIPTION	SYMBOL	MILLIMETER		
		MIN	NOM	MAX
TOTAL THICKNESS	A	0.70	0.75	0.80
STAND OFF	A1	0	0.035	0.05
MOLD THICKNESS	A2	-	0.55	0.57
MATERIAL THICKNESS	A3	-	0.203_{REF}	-
PACKAGE SIZE	D	-	7_{BSC}	-
	E	-	7_{BSC}	-
EP SIZE	D1	5.39	5.49	5.59
	E1	5.39	5.49	5.59
LEAD LENGTH	L	0.30	0.4	0.50
LEAD PITCH	e		0.35_{BSC}	
LEAD WIDTH	b	0.1	0.15	0.2
LEAD OSITION OFFSET	aaa		0.07	
LEAD COPLANARITY	bbb		0.08	
PACKAGE EDGE PROFILE	ccc		0.10	
MOLD FLATNESS	ddd		0.10	
EP POSITION OFFSET	eee		0.10	
	fff		0.05	

Note:

1. *Coplanarity applies to leads, corner leads and die attach pad.*
2. *Dimension b applies to metalized terminal and is measured between 0.15mm and 0.30mm from the*

terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measure in that radius area.

2.6 Pin Assignment

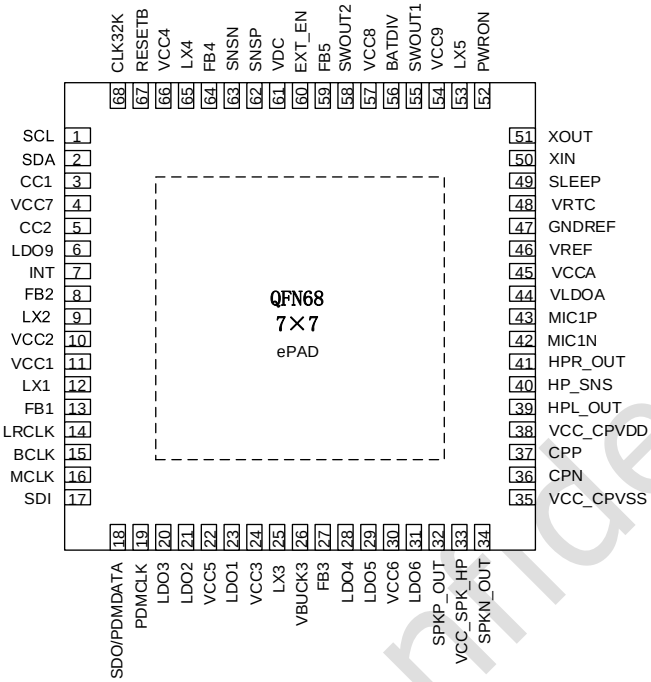


Fig. 2-2 Pin Assignment QFN7x7-68(Pitch=0.35mm)

2.7 Pinout Number Order

PIN NO	PIN NAME	PIN DESCRIPTION
1	SCL	I2C clock input
2	SDA	I2C data input and output
3	CC1	CC1 output for PD
4	VCC7	Power supply of LDO9
5	CC2	CC2 output for PD
6	LDO9	LDO9 output
7	INT	Interrupt request pin, open drain
8	FB2	Output feedback voltage of buck2
9	LX2	Switching node of buck2
10	VCC2	Power supply of buck2
11	VCC1	Power supply of buck1
12	LX1	Switching node of buck1
13	FB1	Output feedback voltage of buck1
14	LRCLK	The I2S framing clock
15	BCLK	The I2S bit clock
16	MCLK	The I2S main clock input pin
17	SDI	The I2S DAC input data
18	SDO/PDMDATA	The I2S ADC output data/PDM Data for the DSADC
19	PDMCLK	PDM CLK for the DSADC OUTPUT
20	LDO3	LDO3 output
21	LDO2	LDO2 output
22	VCC5	Power supply of LDO1/2/3
23	LDO1	LDO1 output

PIN NO	PIN NAME	PIN DESCRIPTION
24	VCC3	Power supply of buck3
25	LX3	Switching node of buck3
26	VBUCK3	Output voltage of buck3
27	FB3	Output feedback voltage of buck3
28	LDO4	LDO4 output
29	LDO5	LDO5 output
30	VCC6	Power supply of LDO4/5/6
31	LDO6	LDO6 output
32	SPKP_OUT	Positive speaker driver output
33	VCC_SPK_HP	Power supply for speaker and charger pump
34	SPKN_OUT	Negative speaker driver output.
35	VCC_CPVSS	Negative power supply for the headphone
36	CPN	Negative switching node of the charger pump
37	CPP	Positive switching node of the charger pump.
38	VCC_CPVDD	Positive power supply for the headphone
39	HPL_OUT	Left channel output of the headphone
40	HP_SNS	Reference ground for the headphone
41	HPR_OUT	Right channel output of the headphone
42	MICIN	Negative input of the Microphone
43	MICIP	Positive input of the Microphone
44	VLDOA	Power supply for internal 1.8V analog circuit
45	VCCA	Power supply filter
46	VREF	Internal reference voltage
47	GNDREF	Reference ground
48	VRTC	Button battery input
49	SLEEP	Sleep mode control input
50	XIN	32.768KHz crystal oscillator input
51	XOUT	32.768KHz crystal oscillator output
52	PWRON	Power on key input, active low, internal 35k(±15%) resistor pull high to VCCA
53	LX5	Switching node of BUCK5
54	VCC9	Power supply of buck5 and SWOUT1
55	SWOUT1	Power switch out 1
56	BATDIV	Divided voltage of positive battery
57	VCC8	Power supply of SWOUT2
58	SWOUT2	Power switch out 2
59	FB5	Output feedback voltage of buck5
60	EXT_EN	Enable Signal for external high voltage BUCK
61	VDC	If it exceeds 0.55V for the first time, it will start the PMIC(rising edge triggering start).And it is connected to the divider of external power supply generally.
62	SNSP	Bat charging and discharging sense current positive pin
63	SNSN	Bat charging and discharging sense current negative pin
64	FB4	Output feedback voltage of buck4
65	LX4	Switching node of buck4
66	VCC4	Power supply of buck4
67	RESETB	Reset pin after power on, active low
68	CLK32K	32.768KHz clock output, it can be configure for open drain or CMOS output(the high level is same as VCCA).
Exposed	Exposed	Ground

PIN NO	PIN NAME	PIN DESCRIPTION
pad	ground	

Chapter 3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Parameter	Min	Max	Units
Voltage range on pins SWOUTx, VCC1~9,VCCA,VCC_SPK_HP,LDOx, FBx,VBUCK3,SPKP_OUT,SPKN_OUT,VLDOA	-0.3	6.5	V
Voltage range on pins LXx	-0.3（-2V for <20ns and -3.5V for <10ns）	6.5(7V for <20ns)	V
Voltage range on pin CLK32K,RESETB, SLEEP,SCL,SDA,INT,PWRON,XIN,XOUT, VDC,EXT_EN	-0.3	6.5V	V
Voltage range on pins LRCLK,BCLK,MCLK,SDI,SDO/PDMCLK	-0.3	6.5V	V
Voltage range on pins SNSP,SNSN,VREF,VRTC,MIC1N,MIC1P, BATDIV	-0.3	3.6	V
Voltage range on pins HP_SNS,HPR_OUT,HPL_OUT	-3	3	V
Voltage range on pins VCC_CPVDD,CPP	-0.3	3	V
Voltage range on pins VCC_CPVSS,CPN	-3	0.3	V
Storage temperature range, T_S	-40	150	℃
Operating temperature range, T_J	-40	125	℃
Maximum Soldering Temperature, T_{SOLDER}		300	℃

Note：

Exposure to the conditions exceeded absolute maximum ratings may cause the permanent damages and affect the reliability and safety of both device and systems using the device. The functional operations cannot be guaranteed beyond specified values in the recommended conditions.

3.2 Recommended Operating Conditions

Parameter	Min	Max	Units
Voltage range on pins SWOUTx, VCC1~9,VCCA,VCC_SPK_HP,LDOx, BATDIV, FBx,VBUCK3,SPKP_OUT,SPKN_OUT,VRTC,VLDOA	-0.3	5.5	V
Voltage range on pin CLK32K,RESETB, SLEEP,SCL,SDA,INT,PWRON,XIN,XOUT, VDC,EXT_EN	-0.3	VLDOA+0.3	V
Voltage range on pins LRCLK,BCLK,MCLK,SDI,SDO/PDMCLK	-0.3	VLDO4+0.3	V
Voltage range on pins SNSP,SNSN,VREF,MIC1N,MIC1P	-0.3	2.85	V
Voltage range on pins HP_SNS,HPR_OUT,HPL_OUT	-2.8	2.8	V
Voltage range on pins VCC_CPVDD,CPP	-0.3	2.8	V
Voltage range on pins VCC_CPVSS,CPN	-2.8	0.3	V
Power Dissipation		2	W

3.3 DC Characteristics

Test conditions: VCC9=5.0V,TA=25°C for typical values, unless otherwise noted.

PARAMETERS	SYMBOL	Note	MIN	TYP	MAX	UNIT
Power dissipation						
Shut down Current	Isd			18	20	uA

PARAMETERS	SYMBOL	Note		MIN	TYP	MAX	UNIT
Power on current 1: All bucks, LDOs, ADC power on, Null load	Iq1				1.9		mA
Power on current 2: buck1/buck4, LDO1/ldo2 power on, Null load	Iq2				0.65		mA
Power on and sleep current: buck1/buck4, LDO1/ldo2 power on, low power mode, sleep mode, Null load	Isleep				0.19		mA
System Characteristics							
VB_OK threshold, the VCC9 voltage should be higher than it to power on the PMIC.	Vok	2.8V~3.6V by OTP programmed.	VB_OK_SEL[1:0]=0b01	2.744	2.8	2.856	V
			VB_OK_SEL[1:0]=0b00	2.94	3.0	3.06	V
			VB_OK_SEL[1:0]=0b10	3.332	3.4	3.468	V
			VB_OK_SEL[1:0]=0b11	3.546	3.6	3.654	V
VB_UV threshold, when the VCC9 voltage is lower than it, The PMIC would be shutdown.	Vuv	2.7V~3.4V by I2C programmed. Typical is 2.7V.	VB_UV_SEL[2:0]=0b000	2.646	2.7	2.754	V
			VB_UV_SEL[2:0]=0b011	2.94	3.0	3.06	V
			VB_UV_SEL[2:0]=0b111	3.332	3.4	3.468	V
VB_LO threshold, when the VCC9 voltage is lower than it, The PMIC would be shut down or interrupt happen.	Vlo	2.8V~3.5V by I2C programmed. Typical is 3.2V.	VB_LO_SEL[2:0] = 0b000	2.744	2.8	2.856	V
			VB_LO_SEL[2:0] = 0b100	3.136	3.2	3.264	V
			VB_LO_SEL[2:0] = 0b111	3.43	3.5	3.57	V
VB_OV threshold, when the VCC9 voltage is higher than it, The PMIC would be shutdown.	Vov			5.8	6	6.2	V
TSD threshold, when the temperature is higher than it, The PMIC would be shutdown.	Tsd	140/160℃ by I2C programmed. Typical is 160℃.	TSD_TEMP=0b0	135	140	145	℃
			TSD_TEMP=0b1	155	160	165	℃
T warning threshold, when the temperature is higher than it, interrupt happen.	Twa	85~115℃ by I2C programmed. Typical is 115℃.	HOTDIE_TEMP[1:0]=0b00	80	85	90	℃
			HOTDIE_TEMP[1:0]=0b01	90	95	100	℃
			HOTDIE_TEMP[1:0]= 0b10	100	105	110	℃
			HOTDIE_TEMP[1:0]= 0b11	110	115	120	℃
Long press PWRON key time	Tlp	6s~12s by I2C programmed. Typical is 6s.	PWRON_LP_OFF_TIME[1:0]=0b00		6		s
			PWRON_LP_OFF_TIME[1:0]=0b01		8		s
			PWRON_LP_OFF_TIME[1:0]=0b10		10		s
			PWRON_LP_OFF_TIME[1:0]=0b1		12		s

PARAMETERS	SYMBOL	Note		MIN	TYP	MAX	UNIT
			1				
Short press PWRON key time	Tst	20.32mS~3.5S by I2C programmed Typical is 520mS	PWRON_ON_TIME=0b0 PWRON_ON_TIME_H=0b0 POWERON_TIME_ADD=0b000 PWRON_DB_SEL=0b10		520		ms
Sequence gap	Seq_gap	1ms/2ms/4mS by OTP programed. Typical is 2ms.			2		ms

Test conditions: VCCx=5.0V,TA=25°C for typical values, unless otherwise noted.

PARAMETERS	SYMBOL	Note	MIN	TYP	MAX	UNIT
BUCK1: Fast load transient response step-down converter						
Input supply voltage range	Vcc1		2.7		5.5	V
Output Voltage Accuracy @ all load @ all input voltage range	Vfb1	0.5V~2.4V by I2C programmed. Typical is 1.0V. Step=12.5mV(0.5V~1.5V) Step=100mV(1.5V~2.4V)	0.98	1.0	1.02	V
Load Transient Response L=0.47uH, Cout=32uF.	Vdrop1	0.25A to 2.5A, 0.5A/uS, Vout=1V		20		mV
Rated output current	Imax1		2.5			A
Switching Frequency when CCM mode	Fsw1	Vin-Vout>1.5V	1.75	2.0	2.25	MHz
Conversion Efficiency (Vin=4.2V,Vout=1V)		Iout=2A Iout=1A Iout=0.3A		75 82 85		%
BUCK2: Fast load transient response step-down converter						
Input supply voltage range	Vcc2		2.7		5.5	V
Output Voltage Accuracy @ all load @ all input voltage range	Vfb2	0.5V~2.4V by I2C programmed. Typical is 1.0V. Step=12.5mV(0.5V~1.5V) Step=100mV(1.5V~2.4V)	0.98	1.0	1.02	V
Load Transient Response L=0.47uH, Cout=32uF.	Vdrop2	0.25A to 2.5A, 0.5A/uS, Vout=1V		20		mV
Rated output current	Imax2		2.5			A
Switching Frequency when CCM mode	Fsw2	Vin-Vout>1.5V	1.75	2.0	2.25	MHz
Conversion Efficiency (Vin=4.2V,Vout=1V)		Iout=2A Iout=1A Iout=0.3A		75 82 85		%
BUCK3: Fast load transient response step-down converter						
Input supply voltage range	Vcc3		2.7		5.5	V
Feedback Voltage, Default	Vfb3	Selection of external resistor divider	0.784	0.8	0.816	V
Output Voltage Accuracy @ all load @ all input voltage range	Vbuck3	If internal divide mode selected: 0.5V~2.4V by I2C programmed. Typical is 1.25V. Step=12.5mV (0.5V~1.5V) Step=100mV (1.5V~2.4V)	1.225	1.25	1.275	V
Load Transient Response L=0.47uH, Cout=22uF.	Vdrop3	0.15A to 1.5A, 0.5A/uS, Vout=1.25V		17		mV
Rated output current	Imax3		1.5			A
Switching Frequency when CCM mode	Fsw3	Vin-Vout>1.5V	1.75	2.0	2.25	MHz

PARAMETERS	SYMBOL	Note	MIN	TYP	MAX	UNIT
Conversion Efficiency (Vin=4.2V,Vout=1.25V)		Iout=1A Iout=0.3A		82 83		%
BUCK4: Fast load transient response step-down converter						
Input supply voltage range	Vcc4		2.7		5.5	V
Output Voltage Accuracy @ all load @ all input voltage range	Vfb4	0.5V~3.4V by I2C programmed. Typical is 3V. Step=12.5mV (0.5V~1.5V) Step=100mV (1.5V~3.4V)	2.94	3	3.06	V
Load Transient Response L=0.47uH, Cout=22uF.	Vdrop4	0.15A to 1.5A, 0.5A/uS, Vout=3V		22		mV
Rated output current	Imax4		1.5			A
Switching Frequency when CCM mode	Fsw4	Vin-Vout>1.5V	1.75	2.0	2.25	MHz
Conversion Efficiency, (Vin=4.2V,Vout=3V)		Iout=1A Iout=0.3A		92 93		%
LDO1						
Input supply voltage range	Vcc5		2		5.5	V
Output Voltage Accuracy @ all load @ all input voltage range	Vldo1	0.6V~3.4V by I2C programmed. Typical is 1V. Step=25mV	0.98	1	1.02	V
Rated output current	Imaxl1	Vcc5- Vldo1>0.4V	400			mA
		Vcc5- Vldo1>0.2V	200			mA
PSRR@ 1KHz		Vin rms=200mV		65		dB
PSRR@ 10KHz		Vin rms=200mV		60		dB
LDO2						
Input supply voltage range	Vcc5		2		5.5	V
Output Voltage Accuracy @ all load @ all input voltage range	Vldo2	0.6V~3.4V by I2C programmed. Typical is 1.8V. Step=25mV	1.764	1.8	1.836	V
Rated output current	Imaxl2	Vcc5- Vldo2>0.4V	400			mA
		Vcc5- Vldo2>0.2V	200			mA
PSRR@ 1KHz		Vin rms=200mV		65		dB
PSRR@ 10KHz		Vin rms=200mV		60		dB
LDO3:						
Input supply voltage range	Vcc5		2		5.5	V
Output Voltage Accuracy @ all load @ all input voltage range	Vldo3	0.6V~3.4V by I2C programmed. Typical is 1V. Step=25mV	0.98	1	1.02	V
Rated output current	Imaxl3	Vcc5- Vldo3>0.4V	400			mA
		Vcc5- Vldo3>0.2V	200			mA
PSRR@ 1KHz		Vin rms=200mV		65		dB
PSRR@ 10KHz		Vin rms=200mV		60		dB
LDO4						
Input supply voltage range	Vcc6		2		5.5	V
Output Voltage Accuracy @ all load @ all input voltage range	Vldo4	0.6V~3.4V by I2C programmed. Typical is 3V. Step=25mV	2.94	3	3.06	V
Rated output current	Imaxl4	Vcc6- Vldo4>0.4V	400			mA
		Vcc6- Vldo4>0.2V	200			mA
PSRR@ 1KHz		Vin rms=200mV		65		dB
PSRR@ 10KHz		Vin rms=200mV		60		dB
LDO5						
Input supply voltage range	Vcc6		2		5.5	V
Output Voltage Accuracy @	Vldo5	0.6V~3.4V by I2C programmed.	2.94	3	3.06	V

PARAMETERS	SYMBOL	Note		MIN	TYP	MAX	UNIT
all load @ all input voltage range		Typical is 3V. Step=25mV					
Rated output current	Imaxl5	Vcc6- Vldo5>0.4V		400			mA
		Vcc6- Vldo5>0.2V		200			mA
PSRR@ 1KHz		Vin rms=200mV			65		dB
PSRR@ 10KHz		Vin rms=200mV			60		dB
LDO6							
Input supply voltage range	Vcc6			2		5.5	V
Output Voltage Accuracy @ all load @ all input voltage range	Vldo6	0.6V~3.4V by I2C programmed. Typical is 3V. Step=25mV		2.94	3	3.06	V
Rated output current	Imaxl6	Vcc6- Vldo6>0.4V		400			mA
		Vcc6- Vldo6>0.2V		200			mA
PSRR@ 1KHz		Vin rms=200mV			65		dB
PSRR@ 10KHz		Vin rms=200mV			60		dB
LDO9							
Input supply voltage range	Vcc7			2		5.5	V
Output Voltage Accuracy @ all load @ all input voltage range	Vldo9	0.6V~3.4V by I2C programmed. Typical is 1.5V. Step=25mV		1.47	1.5	1.53	V
Rated output current	Imaxl9	Vcc7- Vldo9>0.4V		400			mA
		Vcc7- Vldo9>0.2V		200			mA
PSRR@ 1KHz		Vin rms=200mV			65		dB
PSRR@ 10KHz		Vin rms=200mV			60		dB
BUCK5: High efficiency step-down converter							
Input supply voltage range	Vcc9			2.7		5.5	V
Output Voltage Accuracy @ all load @ all input voltage range	Vfb5	1.5V~3.6V by I2C programmed. Typical is 3.3V.		3.234	3.3	3.366	V
Load Transient Response L=0.47uH, Cout=44uF.	Vdrop5	0.25A to 2.5A, 0.5A/uS, Vout=3V				40	mV
Rated output current	Imax5			2.5			A
Switching Frequency when CCM mode	Fsw5	Vin-Vout>1.5V		1.75	2.0	2.25	MHz
Conversion Efficiency, (Vin=4.2V,Vout=3.3V)		Iout=2A Iout=0.3A			90 92		% %
SWOUT1							
Input supply voltage range	Vcc9			2.7		5.5	V
Rdson					90		mΩ
Rated output current	Imax6	1A~2.1A by I2C programmed. Typical is 2.1A.	SW1_ILIM[1:0]= 0b00	1			A
			SW1_ILIM[1:0]= 0b01	1.5			A
			SW1_ILIM[1:0]= 0b10	1.8			A
			SW1_ILIM[1:0]= 0b11	2.1			A
SWOUT2							
Input supply voltage range of Boost	Vcc8			2.7		5.5	V
Rdson					100	120	mΩ
Rated output current	Imax7	1A~2.1A by I2C programmed. Typical is 2.1A.	SW2_ILIM[1:0]= 0b00	1			A
			SW2_ILIM[1:0]= 0b01	1.5			A
			SW2_ILIM[1:0]= 0b10	1.8			A
			SW2_ILIM[1:0]= 0b11	2.1			A

Test conditions: VCC9=5V, BAT_DIV=1.0V, TA=25°C for typical values, unless otherwise noted.

PARAMETERS	SYMBOL	Note	MIN	TYP	MAX	UNIT
A/D CONVERTER						
Voltage measuring ADC resolution				16		bits
Voltage measuring ADC accuracy			-0.5%		+0.5%	%
Range of SWOUT1 voltage measurement			1		6	V
Range of BAT_DIV voltage measurement			0		1.2	V
Range of SWOUT2 voltage measurement			1		6	V
Range of TS voltage measurement			0		1.2	V
Current measuring ADC resolution		MSB is sign bit		16		bits
Current measuring ADC accuracy		ABS(Ibat)>0.2A	-0.5%		+0.5%	%
Range of Current ADC measurement		SNSP/SNSN sense resistor=10mOhm	-5.625		5.625	A
Coulom-counter range				32		bits
Coulom-counter accuracy		ABS(Ibat)>0.2A	-1		+1	%

Test conditions: VCC_SPK=5V, VCC9=5.0V, TA=25°C for typical values, unless otherwise noted.

PARAMETERS	SYMBOL	Note	MIN	TYP	MAX	UNIT
ClassD Audio PA						
Input supply voltage range	Vccspk	VCC_SPK_HP	2.7		5.5	V
THD+N		1KHz, Po=0.4Wrms, VCC_SPK_HP =3.8V		-75		dB
RMS Power		8 ohm load, VCC_SPK_HP =3.8V, THD+N=1%		700		mW
		8 ohm load, VCC_SPK_HP =5V, THD+N=1%		1100		mW
		8 ohm load, VCC_SPK_HP =5V, THD+N=10%		1300		mW
PSRR		217Hz, VCC_SPK_HP =200mVpk-pk+3.8V,		65		dB
Output Offset Voltage		VCC_SPK_HP =3.8V	- 15		+ 15	mV
Noise Level		VCC_SPK_HP =3.8V 0dB Gain, 8ohm, A-weighted		100		uV
Efficiency		VCC_SPK_HP =3.8V,0.4W,8ohm with 68uH, 1KHz		88		%
Quiescent current		No load,		4		mA

PARAMETERS	SYMBOL	Note	MIN	TYP	MAX	UNIT
		VCC_SPK_HP =3.8				
DAC to Head phone outputs						
Full scale output level		RL=32ohm		0.5		Vrms
		RL=300ohm		0.8		Vrms
Signal to Noise Ratio	SNR	A-weighted RL=32ohm，-60dBFS，Fs=48KHz		97		dB
Total Harmonic Distortion + Noise	THD+N	A-weighted RL=32ohm -3dBFS Fs=48KHz		-86		dB
Micro-phone to ADC stereo input						
Full sale input voltage				0.8		Vrms
Input common voltage	V_{COMN}			0.9		V
SNR		A-weighted，-60dBFS,Fs=48KHz		88		dB
THD+N		A-weighted 997Hz -3dBFS Differential input signal, Fs=48KHz		-86		dB

Test conditions: BAT=4.0V, TA=25°C for typical values, unless otherwise noted.

PARAMETERS	SYMBOL	Note	MIN	TYP	MAX	UNIT
I2C interface :7bits I2C address is 0x20/0x22 (If no special note, the default option is 0x20 in this Datasheet)						
SCL clock frequency	f_{SCL}				400	KHz
LOGIC INPUT						
Input LOW-Level Voltage	V_{IL}				0.4	V
Input HIGH-Level Voltage: LRCLK,BCLK,MCLK,SDI,PDMCLK	V_{IH1}		VLDO4* 0.7		VCCA	V
Input HIGH-Level Voltage: SCL,SDA,SLEEP,TS/GPIO,GATE/GPIO,RESETB	V_{IH2}		1.05		VCCA	V
LOGIC OUTPUT						
LOW-Level Output Voltage, 3.0 mA sink current	V_{OL}				0.4	V
HIGH-Level Output Voltage, 3.0 mA source current: LRCLK,BCLK,SDO/PDMDATA	V_{OH1}		VLDO4-0.4		VLDO4	V
HIGH-Level Output Voltage, 3.0 mA source current: TS/GPIO,GATE/GPIO	V_{OH2}		VCCA-0.4		VCCA	V
INTERNAL RC CLOCK						
The frequency of RC oscillator is 32.768 kHz			-20%		+20%	
START UP SEQUE						
1/2/4mS intervals between the channels to start up can by I2C programmed ,typcial is 2mS			-20%		+20%	

PARAMETERS	SYMBOL	Note	MIN	TYP	MAX	UNIT
OPEN DRAIN OUTPUT PIN						
CLK32K,RESETB,INT,SDA						

Chapter 4 Function Description

4.1 Top State Machine

4.1.1 State Machine Description

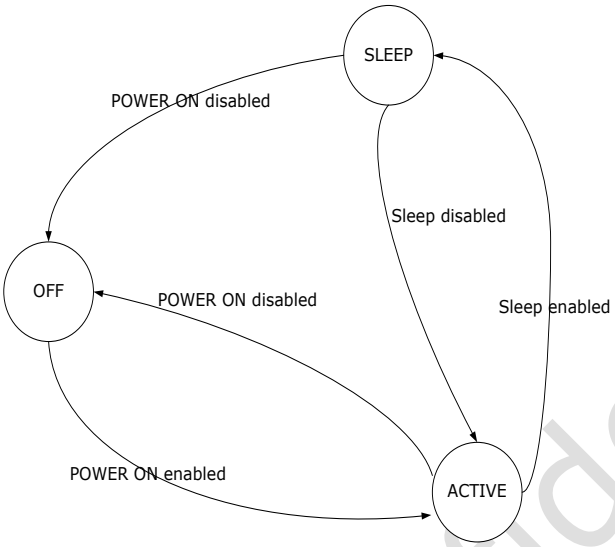


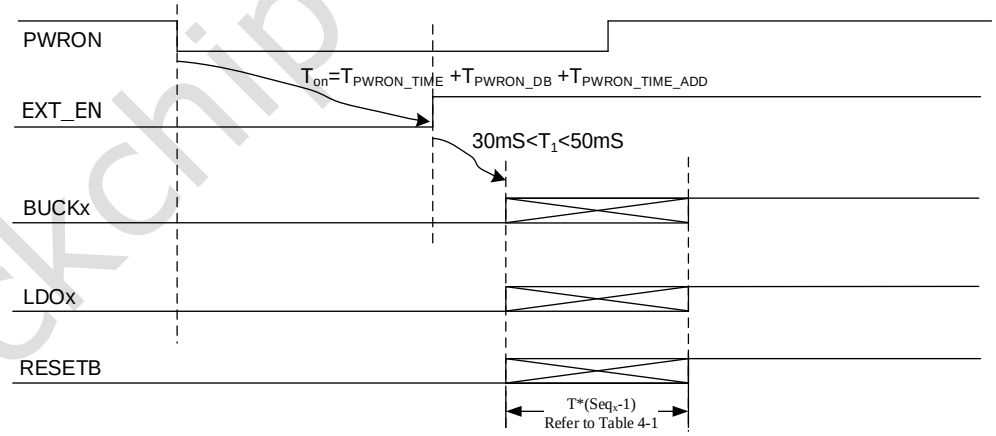
Fig. 4-1 State Machine

The RK809B2 state machine shown as above. The state shift by "power on", "power down", "reset", "active to sleep" and "sleep to active".

4.1.2 Power on Description

There are three kinds of method to power on the PMIC.

1. Press "PWRON" key



T_{PWRON_TIME}:20mS/40mS/100mS/500mS set by OTP
T_{PWRON_DB} can be set by Register 0xF7<1:0>
$T_{PWRON\_TIME\_ADD}$ can be set by Register 0x69<2:0>

Fig. 4-2 Press "PWRON" key to turn on the PMIC

When the PMIC powered by VCC9 which voltage is higher than "VB_OK" threshold, keeping low level at "PWRON" pin for T_{on} would turn on the PMIC. The "PWRON" pin de-bounce time can be adjusted by I2C.

All the power channels start up at the default output voltages with a preset power up sequence, which has Seq_gap（1mS/2mS/4mS) intervals between the channels. When the power up process is done, the RESETB turns to high logic level to inform the processor that all the power rails are up and stable.

2. RTC Alarm

When the PMIC powered by VCC9 which voltage is higher than "VB_OK" threshold (typical 3.4V), Setting RTC alarm would turn on the PMIC. The power on sequence is the same with the first one.

For example, set RTC alarm registers: 0x07, 0x08, 0x09, 0x0A, 0x0B, 0x0C. And then set register 0x0F=2FH.

3. VDC voltage Rising-edge or high level

When the PMIC powered by VCC9/VCCA, and then VDC plug in,the PMIC would be turn on. VDC aslo can be set level-triggered by writing register bit 0x66<0>="1",The power on sequence shown as below.

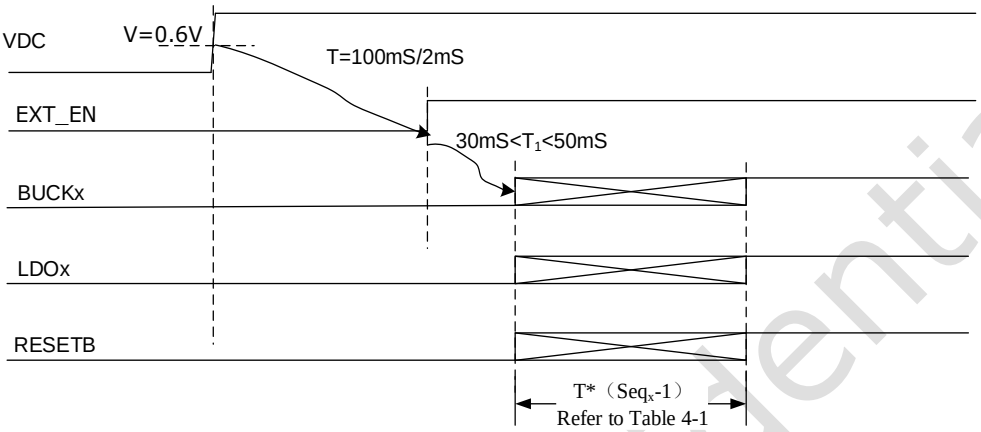


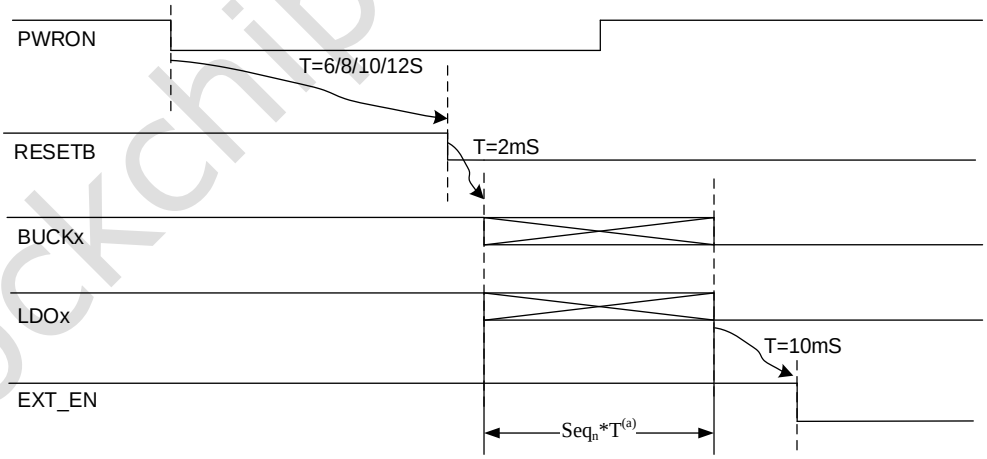
Fig. 4-3 VDC voltage Rising-edge or high level to turn on the PMIC

4.1.3 Power down Description

There are 10 kinds of method to power down the PMIC.

Power down sequence can be set by Register 0x68~0x6F(the 7bits I2C address of the I2C interface is 0x22)

1. Long press "PWRON" key



(a):Seqn is the number of shutdown sequence refer to Register 0x68~0x6F(7 bits I2C address is 0x22), T refer to Table 4-1 Sequence gap

Fig. 4-4 Long press "PWRON" key to turn off the PMIC

When the PMIC work in the "ON" state or "SLEEP" state, Writing register bit 0xF7<6>="0", and then keeping low level at "PWRON" pin for 6/8/10/12S would turn off the PMIC. The "PWRON" pin de-bounce time (6/8/10/12S) can be adjusted by I2C.

When power down enable, The RESETB pin would be pulled low to reset the processor. And then 2ms later, the power channels start to be turned off with the shutdown Sequence.

2. Write shutdown Register

When the PMIC work in the "ON" state or "SLEEP" state, writing register bit 0xF4<0>="1" ,PWRON signal will be pull down for 1mS,At the same time RESETB will be pull down ,And then 2mS later ,the power channels start to be turned off with the shutdown Sequence.

3.SLEEP pin active

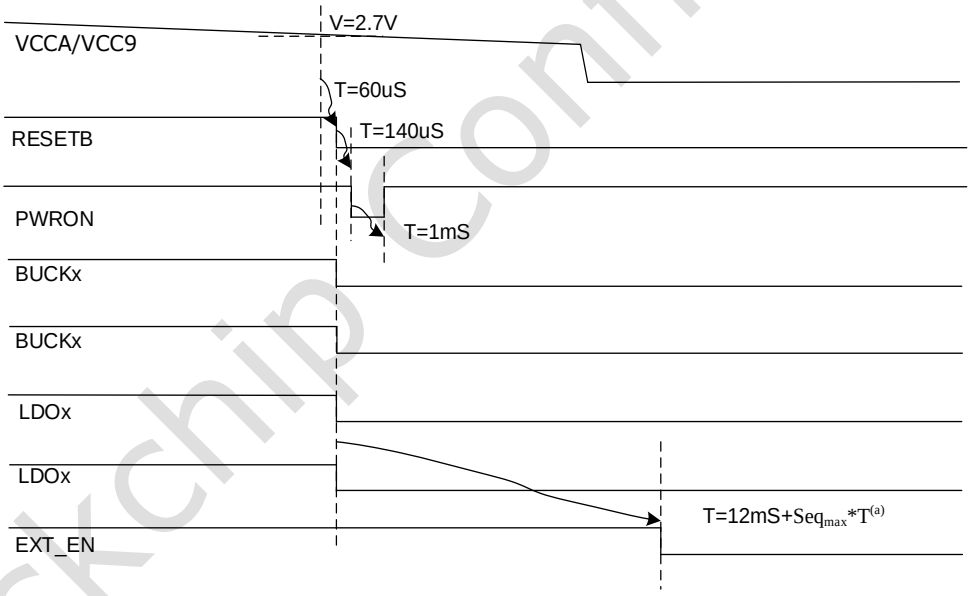
When the PMIC work in the "ON" state or "SLEEP" state, if Register bit 0XF4<4:3>="10", and "SLEEP" pin active (the polarity can be programmed by Register bit 0XF4<5>), PWRON signal will be pull down for 1mS,At the same time RESETB will be pull down ,And then 2mS later ,the power channels start to be turned off with the shutdown Sequence.

4.WDT active

When the PMIC work in the "ON" state or "SLEEP" state, if Register bit 0x65<5>="0" ,and writing the Register bit 0x65<4>="1" and then wait the time of WDT_SEL(typcial is 50mS),PWRON signal will be pull down for 1mS,At the same time RESETB will be pull down ,And then 2mS later ,the power channels start to be turned off with the shutdown Sequence.

5. SYS under-voltage

When the PMIC work in the "ON" state or "SLEEP" state, if VCCA/VCC9 lower than VB_UV threshold (typical 2.7V) for 60uS, PWRON signal will be pull down for 1mS,At the same time RESETB will be pull down ,the PMIC would be turn off. For safe attention, the buck converter would be shut down immediately when detect VB_UV. Then 2mS later，LDO Channels start to be turned off with the shutdown Sequence.



(a):Seq$_{max}$ is maximum number of the shutdown sequence refer to Register 0x68~0x6E(7 bits I2C address is 0x22), T refer to Table 4-1 Sequence gap.

Fig. 4-5 VCC under-voltage to turn off the PMIC

This would lead to processor system halted. So, Writing register bit 0xC6<5>="1" can fix this issue. The detail sequence will be found in "reset Description" chapter.

6. SYS over-voltage

When the PMIC work in the "ON" state or "SLEEP" state, if VCCA /VCC9 higher than 6V, the PMIC would be turn off. PWRON signal will be pull down for 1mS,At the same time RESETB will be pull down ,the PMIC would be turn off. For safe attention, the buck converter would be shut down immediately . Then 2mS later，LDO Channels start to be turned off with the shutdown Sequence.

7. SYS low-voltage

When the PMIC work in the "ON" state or "SLEEP" state, if VCCA /VCC9 lower than

VB_LO threshold (typical 3.2V) for 2mS and Register bit 0XF1<3>="0", the PMIC would be turn off. PWRON signal will be pull down for 1mS,At the same time RESETB will be pull down ,the PMIC would be turn off. For safe attention, the buck converter would be shut down immediately . Then 2mS later，LDO Channels start to be turned off with the shutdown Sequence.

8. TSD protection

When the PMIC work in the "ON" state or "SLEEP" state, if the temperature is higher than TSD threshold (typical 160 degree), the PMIC would be turn off. PWRON signal will be pull down for 1mS,At the same time RESETB will be pull down ,the PMIC would be turn off. For safe attention, the buck converter would be shut down immediately . Then 2mS later，LDO Channels start to be turned off with the shutdown Sequence.

9.VCCA under_voltage

When the PMIC work in the "ON" state or "SLEEP" state, if the voltage of VCCA lower than VB_UV threshold(typcial 2.7V), the PMIC would be turn off. PWRON signal will be pull down for 1mS,At the same time RESETB will be pull down ,the PMIC would be turn off. For safe attention, the buck converter would be shut down immediately . Then 2mS later，LDO Channels start to be turned off with the shutdown Sequence.

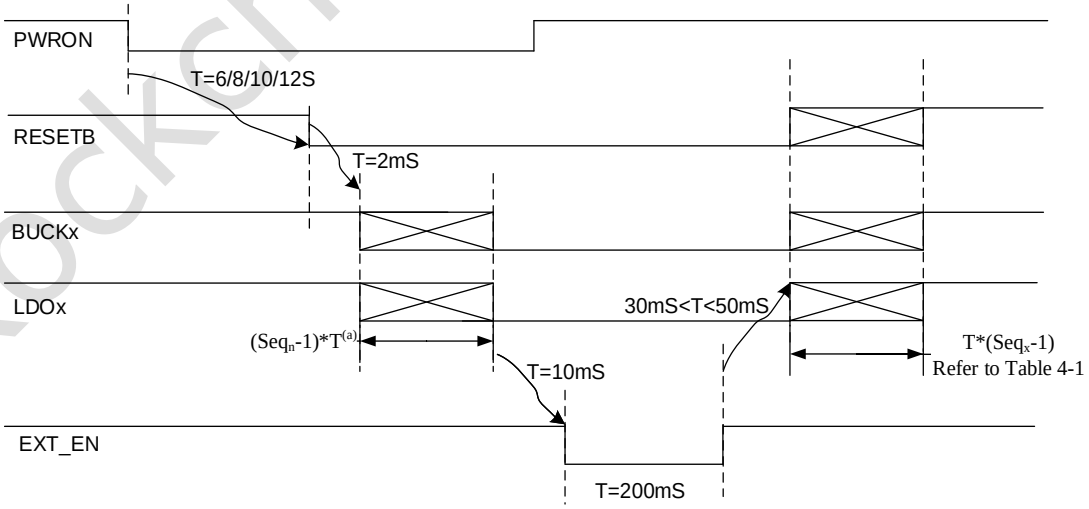
10. VLDOA under_voltage

When the PMIC work in the "ON" state or "SLEEP" state,if the voltage of VLDOA lower than 2.5V, the PMIC would be turn off. PWRON signal will be pull down for 1mS,At the same time RESETB will be pull down ,the PMIC would be turn off. For safe attention, the buck converter would be shut down immediately . Then 2mS later，LDO Channels start to be turned off with the shutdown Sequence.

4.1.4 Reset Description

There are 5 kinds of method to reset the PMIC. If register bits 0xF4<7:6>="00", reset function means restart PMIC. If register bits 0xF4<7:6>="01", reset function means reset registers, all channels of power would be reset to default state.

1. Long press "PWRON" key



(a):Seq_n is the number of shutdown sequence refer to Register 0x6A~0x6E(7 bits I2C address is 0x22), T refer to Table 4-1 Sequence gap.

Fig. 4-6 Long press "PWRON" key to restart the PMIC

When the PMIC work in the "ON" state or "SLEEP" state, Writing register bit 0xF7<6>="1", and then keeping low level at "PWRON" pin for 6/8/10/12S would restart the PMIC. The "PWRON" pin de-bounce time (6/8/10/12S) can be adjusted by I2C.

Note: If the VCC9 voltage is lower than VB_OK threshold, the PMIC would be shut down but restart.

2. SLEEP pin active

When the PMIC work in the "ON" state or "SLEEP" state, if Register bit 0XF4<4:3>="11", and "SLEEP" pin active (the polarity can be programmed by Register bit 0XF4<5>), the PMIC would restart. The restart sequence is the same with the first one.

Note: If the VCCA/VCC9 voltage is lower than VB_OK threshold, the PMIC would be shut down but restart.

Note: It should delay about 66uS after changing the "SLEEP" pin active each time.

3. RESETB pin pull low

When the PMIC work in the "ON" state or "SLEEP" state, if "RESETB" pin is pull down, the PMIC would restart immediately. The restart sequence is the same with the first one.

Note: If the VCC9 voltage is lower than VB_OK threshold, the PMIC would be shut down but restart.

4. Write DEV_RST Register

When the PMIC work in the "ON" state or "SLEEP" state, if the register bit 0xF4<7:6>="00",and writing register bit 0xF4<2>="1",then the PMIC would be sgut down but restart.

5. WDT active

When the PMIC work in the "ON" state or "SLEEP" state, if the register bit 0x65<5>="1", and writing register bit 0x65<4>="1",and then after the time of WDT_SEL programmed by I2C(typcial is 50mS),the PMIC would be shut down but restart.

4.1.5 Power Sequence Description

Power sequence			RK809B2-8	
Short press PWRON key time			500mS	
VDC debounce time			2mS	
32.768KHz clock output mode			CMOS	
VB_OK voltage threshold			3.0V	
Sequence gap（T）			2mS	
	Range of output	Imax	Volt(V)	Seq
BUCK1	0.5V-2.4V	2.5A	0.85	1
BUCK2	0.5V-2.4V	2.5A	0.85	1
BUCK3	X(external divided resistor) Or 0.5V-2.4v(internal divided resistor)	1.5A	X	1
BUCK4	0.5V-3.4V	1.5A	1.8	4
BUCK5	1.5V-3.6V	2.5A	3.3	5
LDO1	0.6V-3.4V	400mA	0.85	1
LDO2	0.6V-3.4V	400mA	0.75	1
LDO3	0.6V-3.4V	400mA	0.75	1
LDO4	0.6V-3.4V	400mA	0.6	OFF
LDO5	0.6V-3.4V	400mA	1.8	4
LDO6	0.6V-3.4V	400mA	1.8	4
LDO9	0.6V-3.4V	400mA	1.2	3
SWOUT1				5
SWOUT2				5
VB_OK	2.8V-3.6V		3.0	
RESETB				11

Table 4-1 RK809B2 Power up sequence

(x:BUCK3 voltage determined by external divided resistor)

4.1.6 Sleep Description

The RK809B2 could be set to SLEEP mode by two kinds of way.

1. Register bits 0xF4<4:3>="01", and then Register bit 0xF4<1>="1".

2. Register bits 0xF4<4:3>="01", and then "SLEEP" pin active (the polarity can be programmed by Register bit 0XF4<5>)

When sleep mode, the power dissipation of RK809B2 would be decreased. Writing register bits 0xB9<4:0>="11111", 0xB9<7>="1", 0xF3<3>="1", 0xE3<7>="1" would be decrease quiescent current further.

Enter SLEEP sequence can be set by Register 0x68~0x6F(the 7bits I2C address of the I2C interface is 0x22)

Exit SLEEP sequence can be set by Register 0x60~0x67(the 7bits I2C address of the I2C interface is 0x22)

4.2 Power Channels

4.2.1 Buck Description

The RK809B2 provides four high current synchronous buck converters, which deliver up to 3A, 3A, 1.5A and 1.5A, respectively. An enhanced COT architecture is used, which improves the transient response significantly. 2.5MHz switching frequency and good control method decrease the external inductance and capacitance. All output voltages can be adjusted dynamically during operation through DVS (Dynamic Voltage Scaling), which guarantees a linear and gradual voltage ramping up and down. A complete set of protection functions, such as short circuit protection, is implemented in the buck converters too.

For example, the BUCK1: Vout=1V, Vin=4V, L=0.47uH, Cout=32uF. Load Current transient from 0.01A to 3A, the current slew rate is 3A/uS (using MOSFET transition). The output voltage drop when load current rising edge is about **38mV**, that is very good characteristics. The other bucks has the same architecture with BUCK1, so they have the same load transient response characteristics.

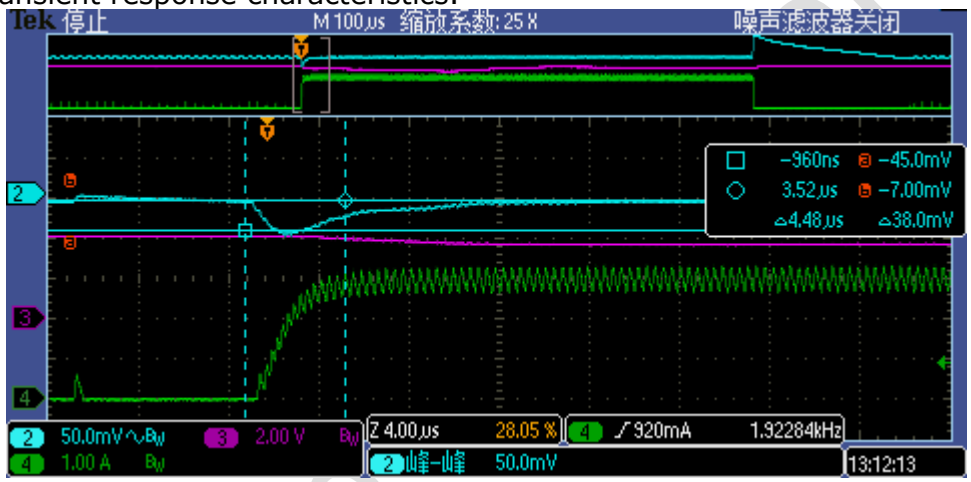


Fig. 4-7 BUCK1 load transient rising edge

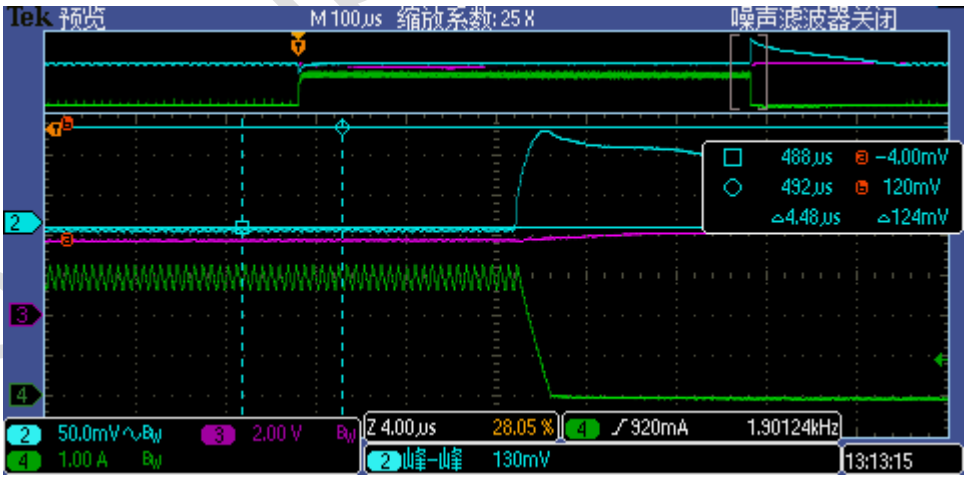


Fig. 4-8 BUCK1 load transient falling edge

If decreasing inductance to 0.33uH and increasing output capacitance to 44uF, the load transient response characteristics would be better.

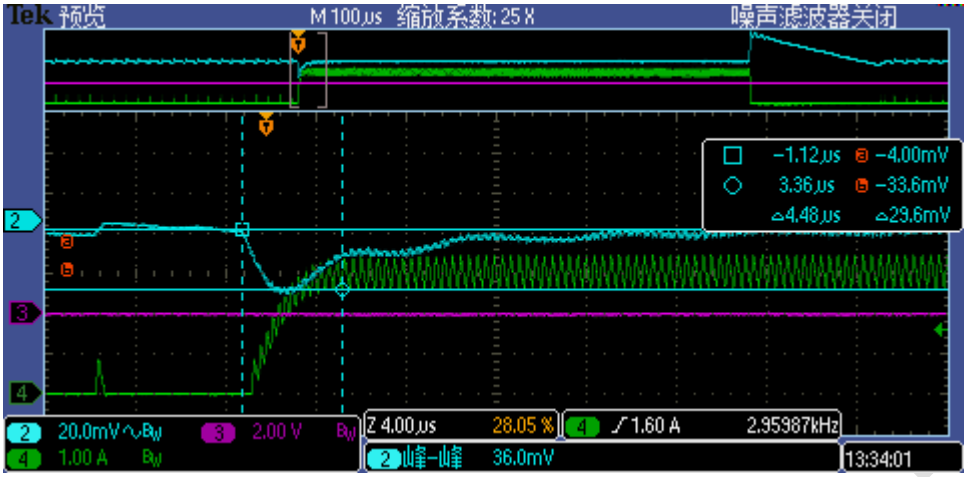


Fig. 4-9 BUCK1 load transient rising edge 2

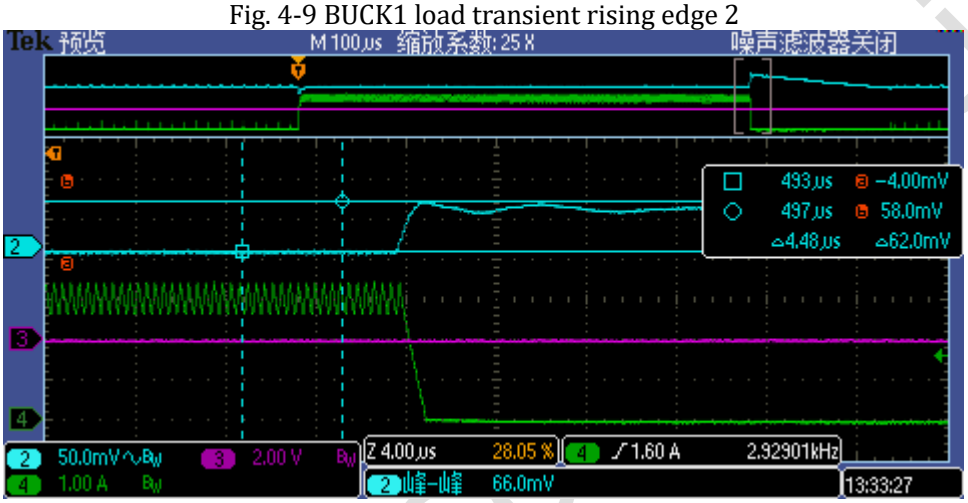


Fig. 4-10 BUCK1 load transient falling edge 2

Meanwhile, bucks converters have good efficiency characteristics. The test data shown as below. All channels of buck output voltage set to default.

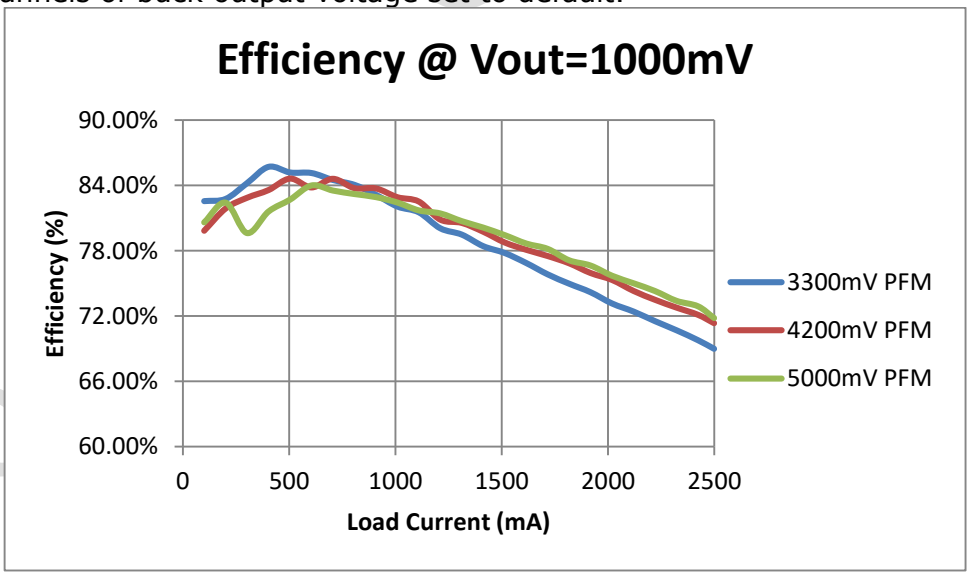


Fig. 4-11 BUCK1 efficiency curve when different input voltage

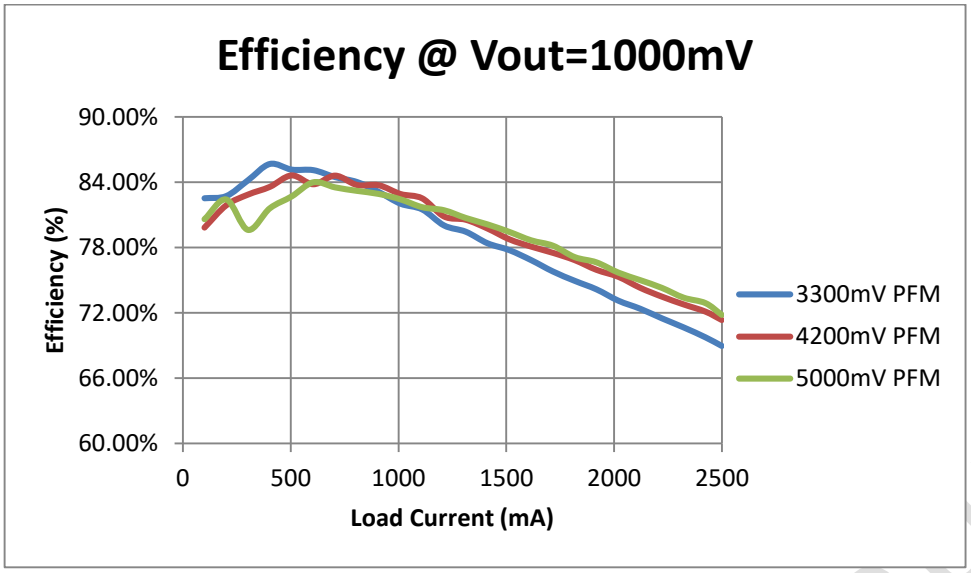


Fig. 4-12 BUCK2 efficiency curve when different input voltage

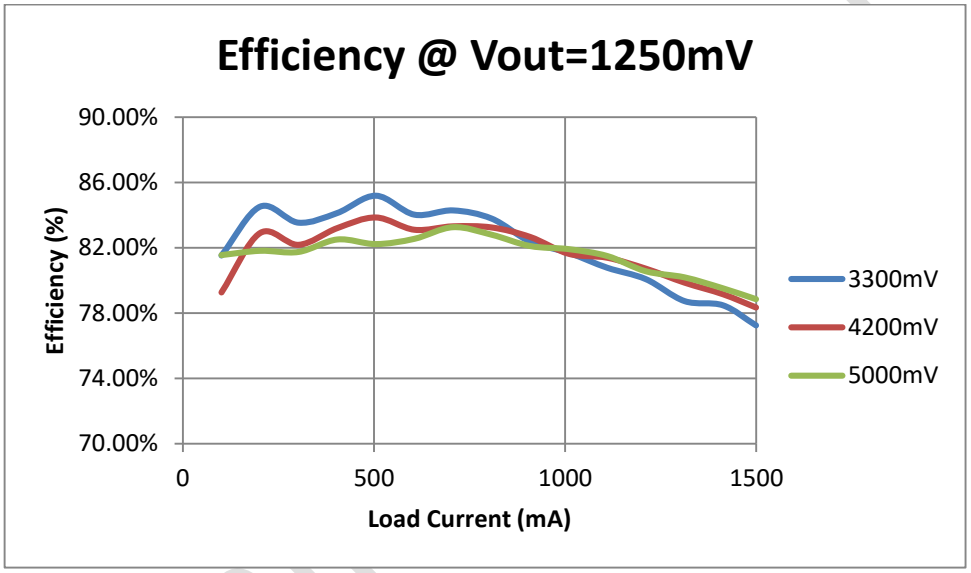


Fig. 4-13 BUCK3 efficiency curve when different input voltage

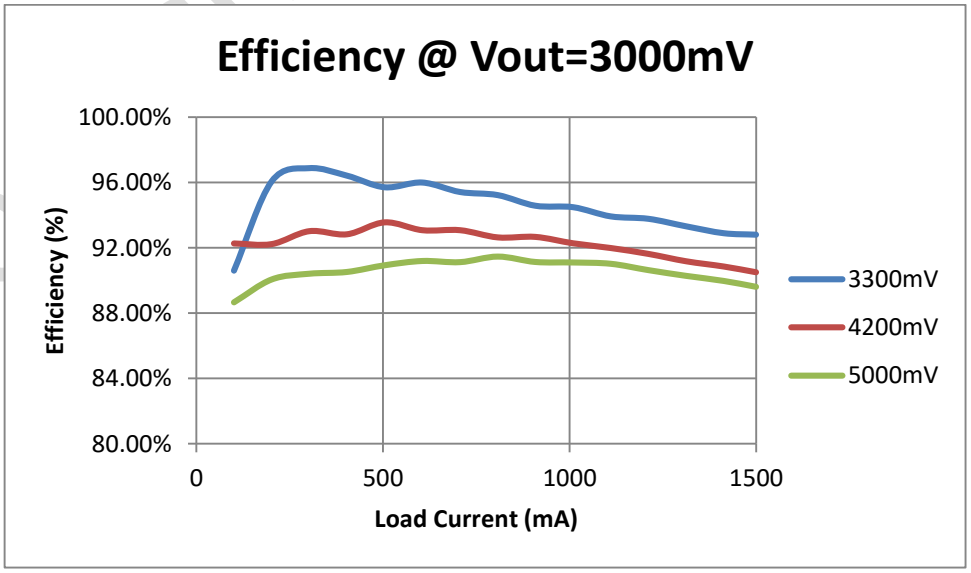


Fig. 4-14 BUCK4 efficiency curve when different input voltage

The RK809B2 also integrates a buck5, adopt peak current mode control, which has good performance in load transient response and efficiency.

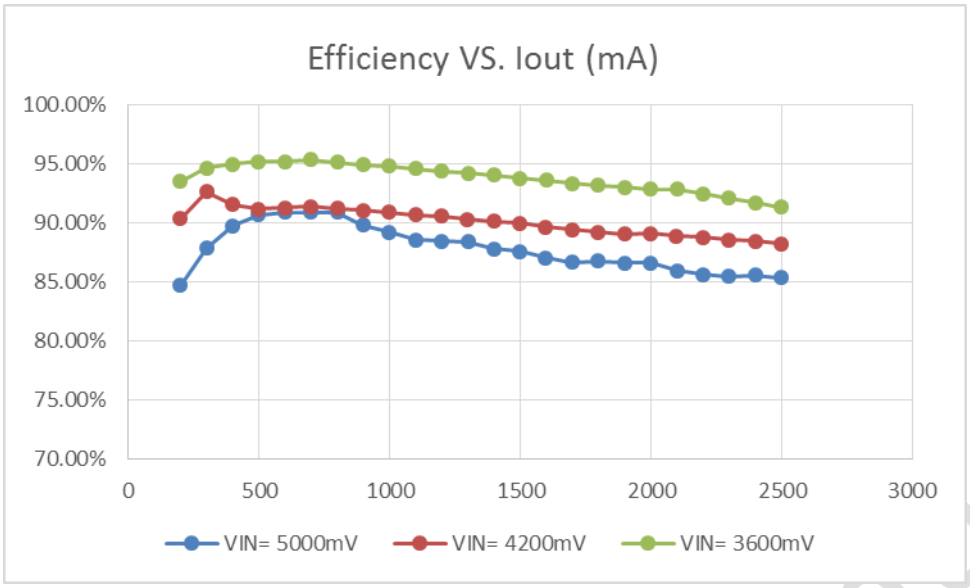


Fig. 4-15 BUCK5 efficiency curve when different input voltage,Vout=3.3V

4.2.2 LDO Description

The RK809B2 also integrates seven LDOs, with 6 LDOs (LDO~LDO6,LDO9) capable of providing up to 400mA.All channels of LDO output capacitance could be 1.0uF that decreases the system cost. The parameters such as output voltage in the different operating modes can be adjusted through the I²C interface.

4.3 Battery Gas Gauge

The RK809B2 provides an accurate battery fuel gauge. A 16-bits battery voltage ADC and a 16-bits battery current ADC are integrated in the RK809B2 to collect the information on the battery, such as battery voltage, etc. Using the proprietary algorithms and the information collected by the ADC, the battery fuel gauge can accurately calculate the battery capacity based on the charging/discharging characteristics of the battery preloaded in the system. The gauge then sends the battery capacity information to the processor through the I²C interface.

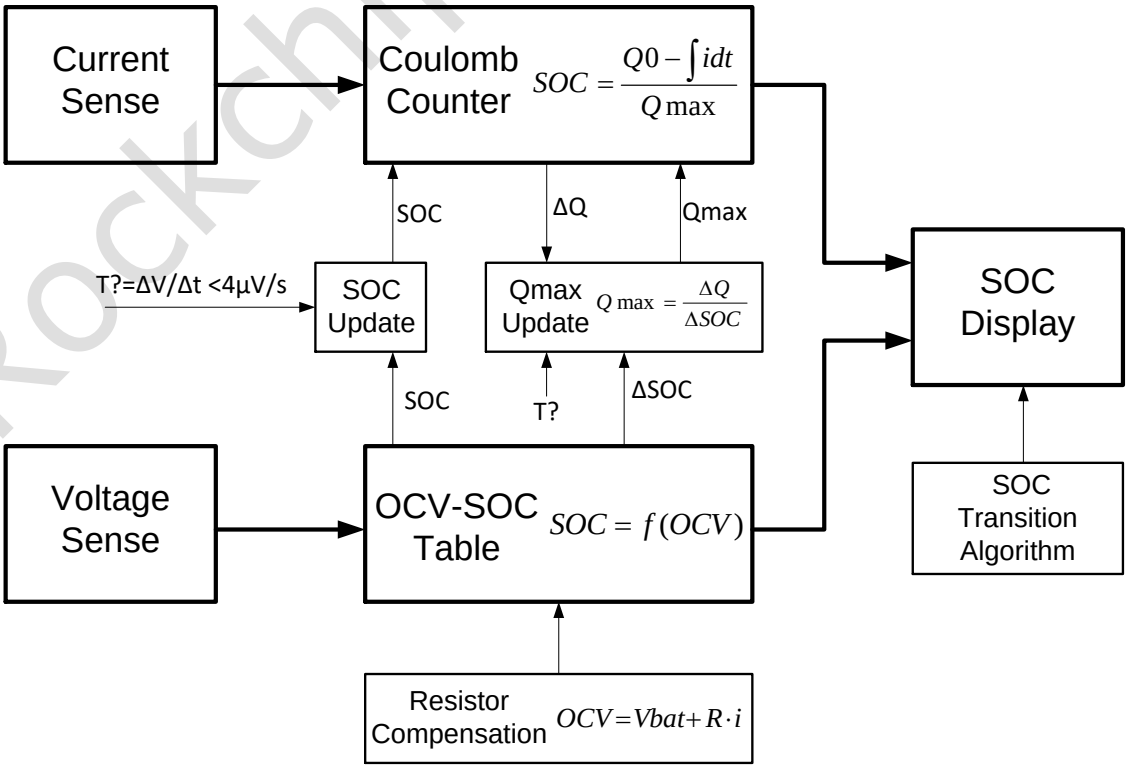


Fig. 4-16 Gas gauge architecture

The gas gauge accuracy determined by ADC accuracy, the ADC accuracy test data shown as below:

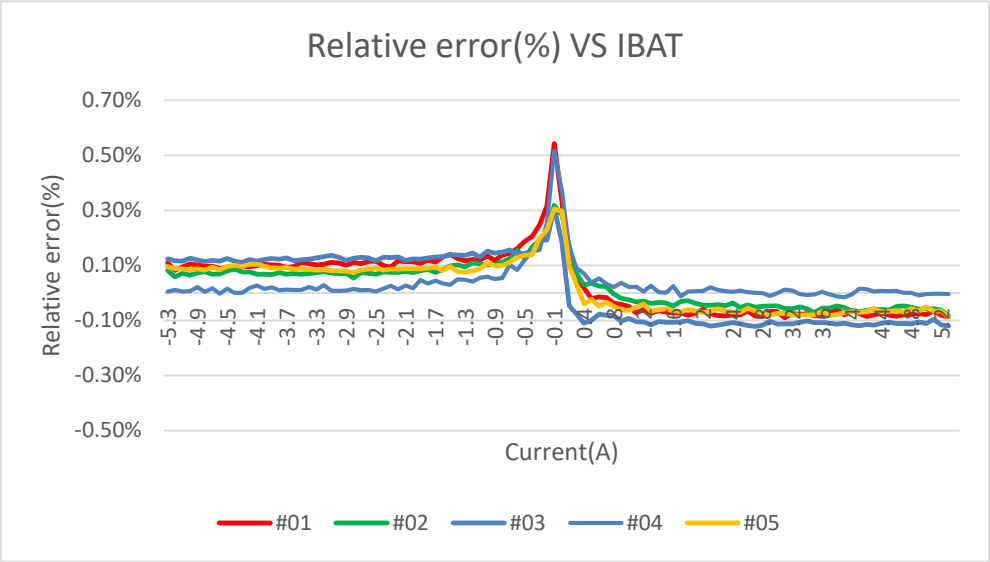


Fig. 4-17 Current ADC Relative Error Curve

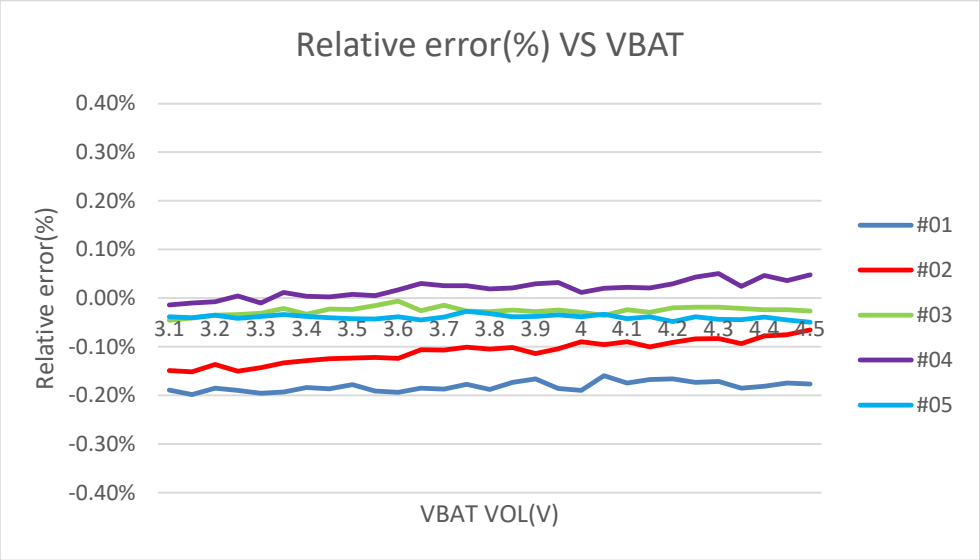


Fig. 4-18 Voltage ADC Relative Error Curve

4.4 Audio System

4.4.1 General Description

The RK809B2 integrates a high performance 24 bits ADC and a high performance 24 bits DAC. The audio recording path is composed of MIC_PGA and audio ADC. DAC would convert digital signal to analog signal, and Class-AB driver adopt real-ground structure for Head-phone application, has very low THD (-90dB @1KHz@-3dBFS source). Meanwhile, Class-D driver integrated for speaker application. The speaker and head-phone can be used at the same time. I2S interface is integrated to communicate with processor.

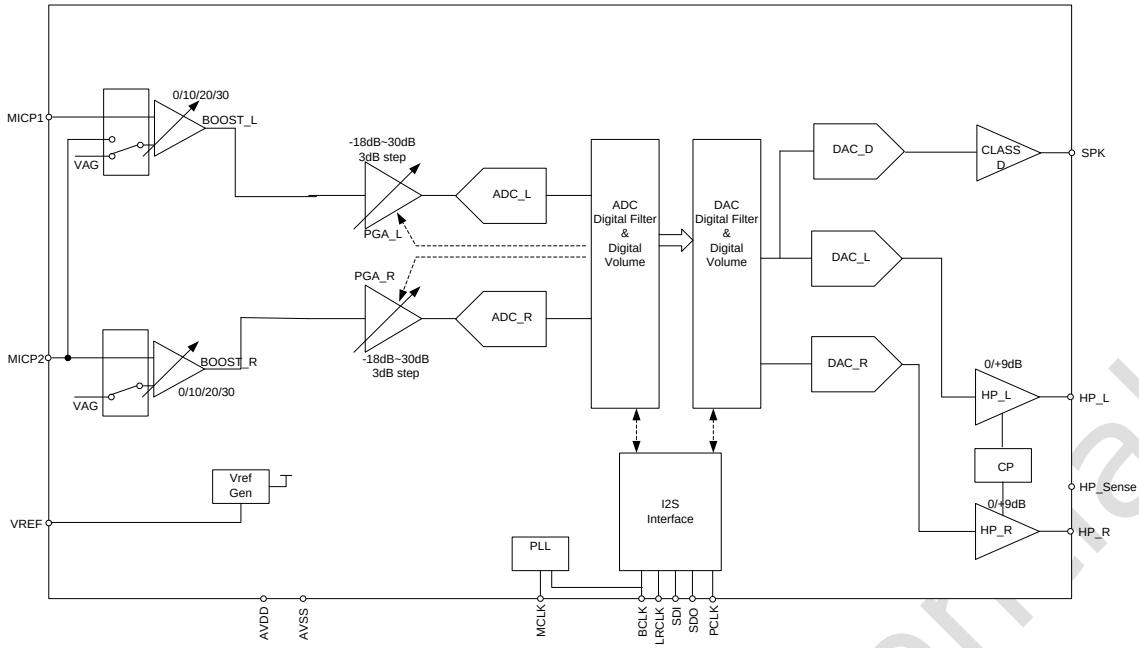


Fig. 4-19 Audio system architecture

4.4.2 Audio Recording Path Description

The RK809B2 integrate complete audio recording path solution. Users should set registers as below toure config audio recording path. For example, sample rate is 48K, MCLK=12.288MHz.

1. Enable I2S: 0x30=00H, 0x15=FFH.
2. Enable reference: 0x17=40H.
3. Setup PLL: 0x42=04H, 0x43=58H, 0x44=2DH, 0x45=0C, 0x46=A5H, 0x47=00H.
4. Setup sample rate: 0x1E=02H.
5. Setup I2S: 0x48=00H, 0x4D=00H, 0x4E=17H, 0x4F=80H.
6. Enable ADC: 0x15=F0H, 0x18=08H.
7. Enable Micro-phone: 0x27=70H (for differential mode MIC); Or 0x27=00H (for single end mode MIC).

The audio recording path THD+N ratio test data shown as below: typical case is -86dB.

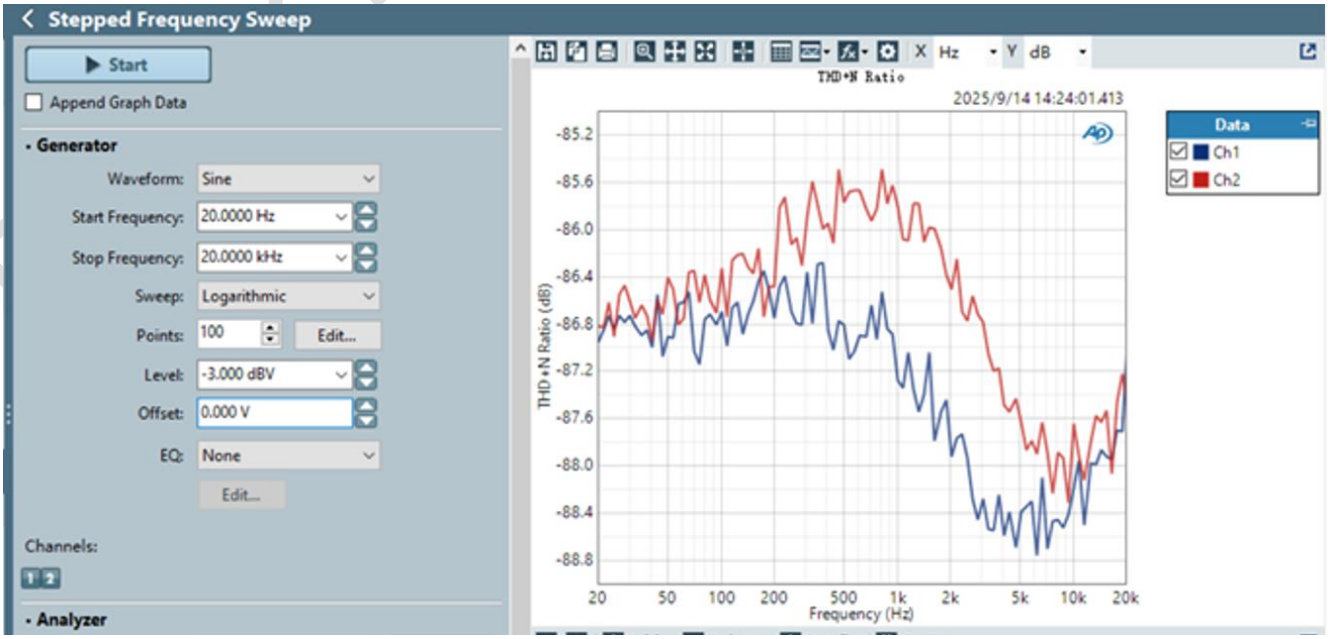


Fig. 4-20 Audio recording path THD+N ratio at differential mode

4.4.3 Head-Phone Path Description

The RK809B2 integrates a stereo output and with cap-free type headphone amplifier. It doesn't need to connect external capacitance, and can connect to earphone device directly.

Users should set registers as below to configure Head-phone path. For example, sample rate is 48K, MCLK=12.288MHz.

1. Enable I2S: 0x30=00H, 0x15=FFH.
2. Enable reference: 0x17=40H.
3. Setup PLL: 0x42=04H, 0x43=58H, 0x44=2DH, 0x45=0C, 0x46=A5H, 0x47=00H.
4. Setup sample rate: 0x35=02H.
5. Setup I2S: 0x48=00H, 0x49=00H, 0x4A=00H, 0x4B=17H, 0x4C=20H.
6. Enable DAC: 0x15=0FH, 0x2F=04H.
7. Enable Head-phone: 0x3F=11H, 0x3D=80H.

The Head-phone path THD+N ratio test data shown as below: typical case is -86dB.

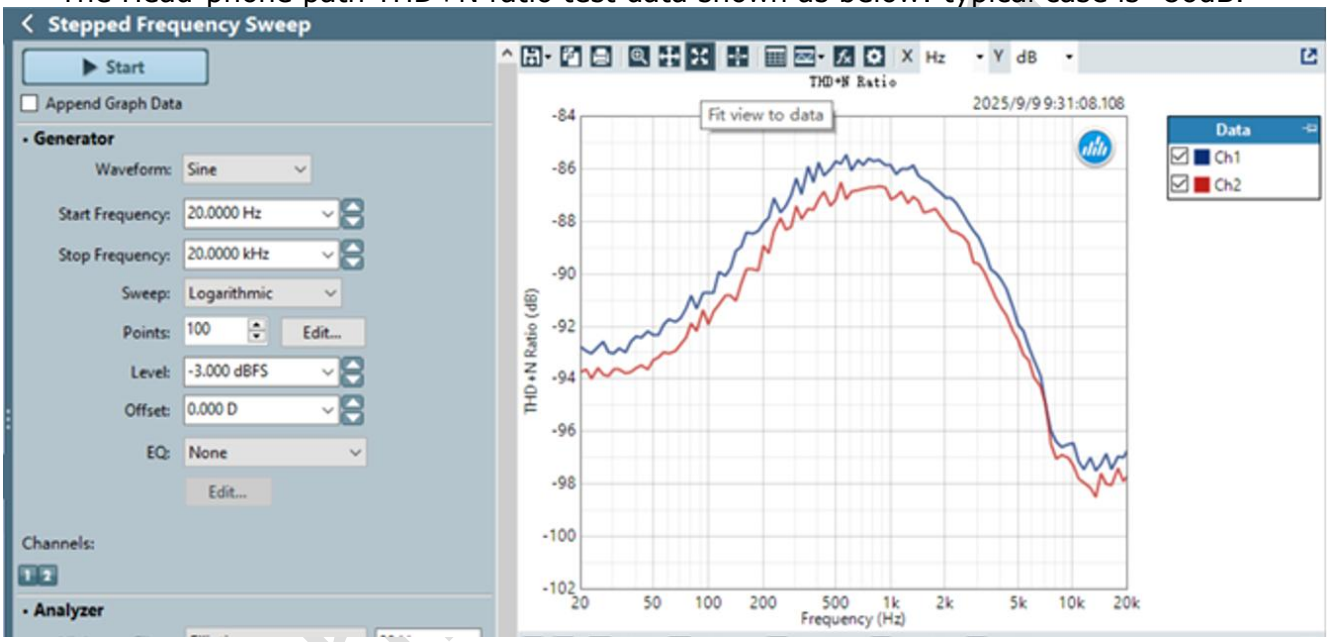


Fig. 4-21 Head-phone path THD+N ratio

4.4.4 Speaker Path Description

The RK809B2 integrates a high efficiency stereo Class-D type amplifier capable of delivering 1.3W of power on an 8ohm BTL load from a 5V power supply. It integrates over-current protection.

Users should set registers as below to configure Speaker path. For example, sample rate is 48K, MCLK=12.288MHz.

1. Enable I2S: 0x30=10H, 0x15=FFH.
2. Enable reference: 0x17=40H.
3. Setup PLL: 0x42=04H, 0x43=58H, 0x44=2DH, 0x45=0C, 0x46=A5H, 0x47=00H.
4. Setup sample rate: 0x35=02H.
5. Setup I2S: 0x48=00H, 0x49=00H, 0x4A=00H, 0x4B=17H, 0x4C=20H.
6. Enable DAC: 0x15=0FH, 0x2F=03H.
7. Enable Class D: 0x38=10H, 0x40=A5H.

The Speaker path THD+N ratio test data shown as below: typical case is -75dB.

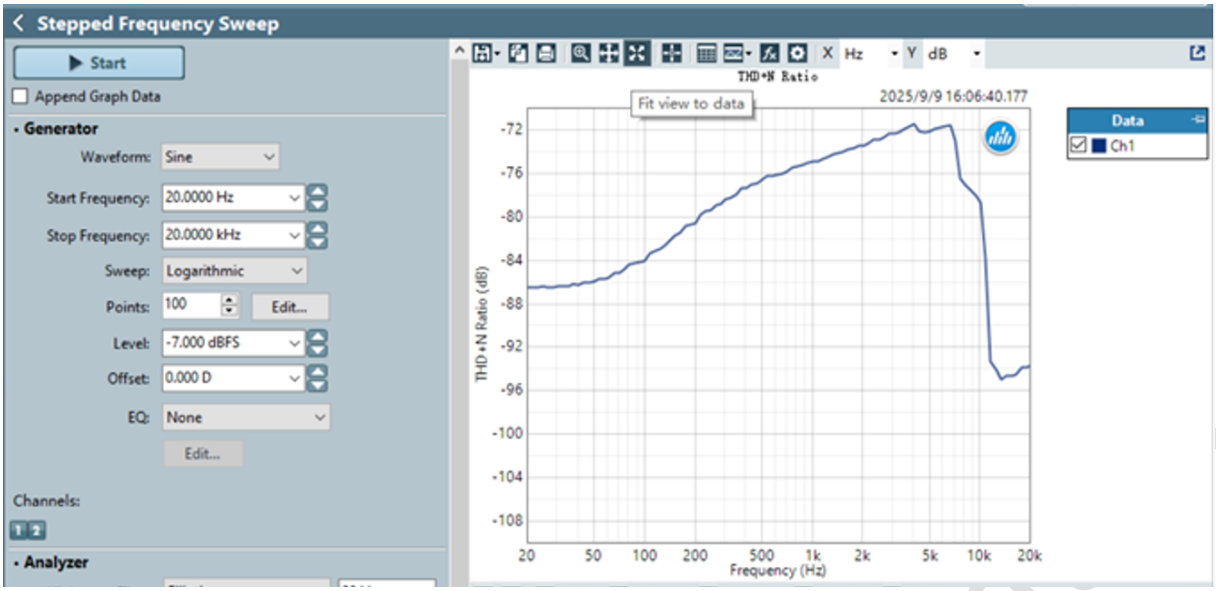


Fig. 4-22 Speaker path THD+N ratio

4.4.5 I2S Description

The RK809B2 supports I2S for the digital audio data interface. The I2S/PCM audio digital interface is used to input data to a stereo DAC or output data from a stereo ADC. The I2S/PCM audio interface can be configured to Master mode or Slave mode. In Master Mode, BCLK and LRCLK are configured as output, but MCLK is fixed as input. In Slave Mode, BCLK and LRCLK are configured as input, and the MCLK is still as input.

4.4.6 RC Oscillator Description

The RK809B2 integrates an RC oscillator. If the external crystal oscillator is not connected, the chip will be driven by the internal RC oscillator. Without external crystal oscillator, the system costs can be saved, but the RTC and the fuel gauge will be inaccurate.

4.4.7 PD Interface

The RK809B2 integrates a PD controller that complies with the PD3.0 standards. USB Type-C CC control and sensing and USB PD Message delivery. RK809B2 has programmable Rp and Rd settings for each CC line. It does the USB type-C detection including attach and orientation. RK809B2 integrates a complete BMC encoding including a receiver and transmitter. The PD block enables full support for alternative interfaces of the Type-C specification.

4.5 Others

4.5.1 Real Time Clock (RTC) Description

The RK809B2 integrates a crystal oscillator buffer and a real time clock (RTC). The buffer works with an external 32.768 kHz crystal oscillator. With the RTC function, the PMIC provides second/minute/hour/day/month/year information, alarm wake up as well as time calibration. The RK809B2 provides one channel of 32.768 kHz clocks with open drain outputs, where it is default on and is controlled through I^2C interface.

Chapter 5 Register Description

5.1 Register Summary

Name	Offset	Size	Reset Value	Description	I2C address 7Bits
RTC_SECONDS	0x00	8	0x00	Por Reset	0x20
RTC_MINUTES	0x01	8	0x00	Por Reset	0x20
RTC_HOURS	0x02	8	0x09	Por Reset	0x20
RTC_DAYS	0x03	8	0x04	Por Reset	0x20
RTC_MONTHS	0x04	8	0x08	Por Reset	0x20
RTC_YEARS	0x05	8	0x17	Por Reset	0x20
RTC_WEEKS	0x06	8	0x05	Por Reset	0x20
RTC_ALARM_SECONDS	0x07	8	0x00	Por Reset	0x20
RTC_ALARM_MINUTES	0x08	8	0x00	Por Reset	0x20
RTC_ALARM_HOURS	0x09	8	0x00	Por Reset	0x20
RTC_ALARM_DAYS	0x0a	8	0x01	Por Reset	0x20
RTC_ALARM_MONTHS	0x0b	8	0x01	Por Reset	0x20
RTC_ALARM_YEARS	0x0c	8	0x00	Por Reset	0x20
RTC_RTC_CTRL	0x0d	8	0x00	Por Reset	0x20
RTC_RTC_STATUS	0x0e	8	0x82	Por Reset	0x20
RTC_RTC_INT	0x0f	8	0x00	Por Reset	0x20
RTC_RTC_COMP_LSB	0x10	8	0x00	Por Reset	0x20
RTC_RTC_COMP_MSB	0x11	8	0x00	Por Reset	0x20
CODEC_DTOP_VUCTL	0x12	8	0x03	Por Reset	0x20
CODEC_DTOP_VUCTIME	0x13	8	0x00	Por Reset	0x20
CODEC_DTOP_LPT_SRST	0x14	8	0x00	Por Reset	0x20
CODEC_DTOP_DIGEN_CLKE	0x15	8	0x00	Por Reset	0x20
CODEC_AREF_RTCFG1	0x17	8	0x06	Por Reset	0x20
CODEC_AADC_CFG0	0x18	8	0xc8	Por Reset	0x20
CODEC_DADC_VOLL	0x1a	8	0x00	Por Reset	0x20
CODEC_DADC_VOLR	0x1b	8	0x00	Por Reset	0x20
CODEC_DADC_SR_ACL0	0x1e	8	0x00	Por Reset	0x20
CODEC_DADC_HPF	0x22	8	0x00	Por Reset	0x20
CODEC_DADC_RVOLL	0x23	8	0xff	Por Reset	0x20
CODEC_DADC_RVOLR	0x24	8	0xff	Por Reset	0x20
CODEC_AMIC_CFG0	0x27	8	0x70	Por Reset	0x20
CODEC_AMIC_CFG1	0x28	8	0x00	Por Reset	0x20
CODEC_DMIC_PGA_GAIN	0x29	8	0x66	Por Reset	0x20
CODEC_ADAC_CFG1	0x2f	8	0x07	Por Reset	0x20
CODEC_DDAC_POPD_DACST	0x30	8	0x82	Por Reset	0x20
CODEC_DDAC_VOLL	0x31	8	0x00	Por Reset	0x20
CODEC_DDAC_VOLR	0x32	8	0x00	Por Reset	0x20
CODEC_DDAC_SR_LMT0	0x35	8	0x00	Por Reset	0x20
CODEC_DDAC_MUTE_MIXCTL	0x38	8	0xa0	Por Reset	0x20

Name	Offset	Size	Reset Value	Description	I2C address 7Bits
CODEC_DDAC_RVOLL	0x39	8	0xff	Por Reset	0x20
CODEC_DDAC_RVOLR	0x3a	8	0xff	Por Reset	0x20
CODEC_AHP_ANTI0	0x3b	8	0x00	Por Reset	0x20
CODEC_AHP_ANTI1	0x3c	8	0x00	Por Reset	0x20
CODEC_AHP_CFG0	0x3d	8	0xe0	Por Reset	0x20
CODEC_AHP_CFG1	0x3e	8	0x1f	Por Reset	0x20
CODEC_AHP_CP	0x3f	8	0x09	Por Reset	0x20
CODEC_ACLASSD_CFG1	0x40	8	0x69	Por Reset	0x20
CODEC_ACLASSD_CFG2	0x41	8	0x44	Por Reset	0x20
CODEC_APLL_CFG0	0x42	8	0x04	Por Reset	0x20
CODEC_APLL_CFG4	0x46	8	0x65	Por Reset	0x20
CODEC_APLL_CFG5	0x47	8	0x01	Por Reset	0x20
CODEC_DI2S_CKM	0x48	8	0x01	Por Reset	0x20
CODEC_DI2S_RSD	0x49	8	0x00	Por Reset	0x20
CODEC_DI2S_RXCR1	0x4a	8	0x00	Por Reset	0x20
CODEC_DI2S_RXCR2	0x4b	8	0x17	Por Reset	0x20
CODEC_DI2S_RXCMD_TSD	0x4c	8	0x00	Por Reset	0x20
CODEC_DI2S_TXCR1	0x4d	8	0x00	Por Reset	0x20
CODEC_DI2S_TXCR2	0x4e	8	0x17	Por Reset	0x20
CODEC_DI2S_TXCR3_TXCMD	0x4f	8	0x00	Por Reset	0x20
gas_gauge_ADC_CONFIG0	0x50	8	0x8c	Por Reset	0x20
gas_gauge_ADC_CONFIG1	0x55	8	0x30	Por Reset	0x20
gas_gauge_GG_CON	0x56	8	0x44	Por Reset	0x20
gas_gauge_GG_STS	0x57	8	0x00	Por Reset	0x20
gas_gauge_RELAX_THRE_H	0x58	8	0x00	Por Reset	0x20
gas_gauge_RELAX_THRE_L	0x59	8	0x60	Por Reset	0x20
gas_gauge_RELAX_VOL1_H	0x5a	8	0x00	Por Reset	0x20
gas_gauge_RELAX_VOL1_L	0x5b	8	0x00	Por Reset	0x20
gas_gauge_RELAX_VOL2_H	0x5c	8	0x00	Por Reset	0x20
gas_gauge_RELAX_VOL2_L	0x5d	8	0x00	Por Reset	0x20
gas_gauge_RELAX_CUR1_H	0x5e	8	0x00	Por Reset	0x20
gas_gauge_RELAX_CUR1_L	0x5f	8	0x00	Por Reset	0x20
gas_gauge_RELAX_CUR2_H	0x60	8	0x00	Por Reset	0x20
gas_gauge_RELAX_CUR2_L	0x61	8	0x00	Por Reset	0x20
gas_gauge_OCV_THRE_VOL	0x62	8	0x00	Por Reset	0x20
gas_gauge_OCV_VOL_H	0x63	8	0x00	Por Reset	0x20
gas_gauge_OCV_VOL_L	0x64	8	0x00	Por Reset	0x20
gas_gauge_OCV_VOL0_H	0x65	8	0x00	Por Reset	0x20
gas_gauge_PWRON_VOL_H	0x6b	8	0x00	Por Reset	0x20
gas_gauge_PWRON_VOL_L	0x6c	8	0x00	Por Reset	0x20
gas_gauge_PWRON_CUR_H	0x6d	8	0x00	Por Reset	0x20
gas_gauge_PWRON_CUR_L	0x6e	8	0x00	Por Reset	0x20
gas_gauge_OFF_CNT	0x6f	8	0x00	Por Reset	0x20

Name	Offset	Size	Reset Value	Description	I2C address 7Bits
gas_gauge_Q_INIT_H3	0x70	8	0x00	Por Reset	0x20
gas_gauge_Q_INIT_H2	0x71	8	0x00	Por Reset	0x20
gas_gauge_Q_INIT_L1	0x72	8	0x00	Por Reset	0x20
gas_gauge_Q_INIT_L0	0x73	8	0x00	Por Reset	0x20
gas_gauge_Q_PRES_H3	0x74	8	0x00	Por Reset	0x20
gas_gauge_Q_PRES_H2	0x75	8	0x00	Por Reset	0x20
gas_gauge_Q_PRES_L1	0x76	8	0x00	Por Reset	0x20
gas_gauge_Q_PRES_L0	0x77	8	0x00	Por Reset	0x20
gas_gauge_BAT_VOL_H	0x78	8	0x00	Por Reset	0x20
gas_gauge_BAT_VOL_L	0x79	8	0x00	Por Reset	0x20
gas_gauge_BAT_CUR_H	0x7a	8	0x00	Por Reset	0x20
gas_gauge_BAT_CUR	0x7b	8	0x00	Por Reset	0x20
gas_gauge_BAT_TS_H	0x7c	8	0x00	Por Reset	0x20
gas_gauge_BAT_TS_L	0x7d	8	0x00	Por Reset	0x20
gas_gauge_USB_VOL_H	0x7e	8	0x00	Por Reset	0x20
gas_gauge_USB_VOL_L	0x7f	8	0x00	Por Reset	0x20
gas_gauge_SYS_VOL_H	0x80	8	0x00	Por Reset	0x20
gas_gauge_SYS_VOL_L	0x81	8	0x00	Por Reset	0x20
gas_gauge_Q_MAX_H3	0x82	8	0x00	Por Reset	0x20
gas_gauge_Q_MAX_H2	0x83	8	0x00	Por Reset	0x20
gas_gauge_Q_MAX_L1	0x84	8	0x00	Por Reset	0x20
gas_gauge_Q_MAX_L0	0x85	8	0x00	Por Reset	0x20
gas_gauge_Q_TERM_H3	0x86	8	0x00	Por Reset	0x20
gas_gauge_Q_TERM_H2	0x87	8	0x00	Por Reset	0x20
gas_gauge_Q_TERM_L1	0x88	8	0x00	Por Reset	0x20
gas_gauge_Q_TERM_L0	0x89	8	0x00	Por Reset	0x20
gas_gauge_Q_OCV_H3	0x8a	8	0x00	Por Reset	0x20
gas_gauge_Q_OCV_H2	0x8b	8	0x00	Por Reset	0x20
gas_gauge_Q_OCV_L1	0x8c	8	0x00	Por Reset	0x20
CUR_ADC_K<15:8>	0x8d	8	OTP	Por Reset	0x20
CUR_ADC_K<7:0>	0x8e	8	OTP	Por Reset	0x20
gas_gauge_SLEEP_CON_SAMP_CUR_H	0x8f	8	0x00	Por Reset	0x20
gas_gauge_SLEEP_CON_SAMP_CUR	0x90	8	0x60	Por Reset	0x20
gas_gauge_CAL_OFFSET_H	0x91	8	0x7f	Por Reset	0x20
gas_gauge_CAL_OFFSET_L	0x92	8	0xff	Por Reset	0x20
gas_gauge_VCALIB0_H	0x93	8	0x00	Por Reset	0x20
gas_gauge_VCALIB0_L	0x94	8	0x00	Por Reset	0x20
gas_gauge_VCALIB1_H	0x95	8	0x00	Por Reset	0x20
gas_gauge_VCALIB1_L	0x96	8	0x00	Por Reset	0x20
gas_gauge_IOFFSET_H	0x97	8	0x00	Por Reset	0x20
gas_gauge_IOFFSET_L	0x98	8	0x00	Por Reset	0x20

Name	Offset	Size	Reset Value	Description	I2C address 7Bits
gas_gauge_BAT_R0	0x99	8	0x00	Por Reset	0x20
gas_gauge_BAT_R1	0x9a	8	0x00	Por Reset	0x20
gas_gauge_BAT_R2	0x9b	8	0x00	Por Reset	0x20
gas_gauge_BAT_R3	0x9c	8	0x00	Por Reset	0x20
gas_gauge_DATA0	0x9d	8	0x00	Por Reset	0x20
gas_gauge_DATA1	0x9e	8	0x00	Por Reset	0x20
gas_gauge_DATA2	0x9f	8	0x00	Por Reset	0x20
gas_gauge_DATA3	0xa0	8	0x00	Por Reset	0x20
gas_gauge_DATA4	0xa1	8	0x00	Por Reset	0x20
gas_gauge_DATA5	0xa2	8	0x00	Por Reset	0x20
gas_gauge_DATA6	0xa3	8	0x00	Por Reset	0x20
gas_gauge_DATA7	0xa4	8	0x00	Por Reset	0x20
gas_gauge_DATA8	0xa5	8	0x00	Por Reset	0x20
gas_gauge_DATA9	0xa6	8	0x00	Por Reset	0x20
gas_gauge_DATA10	0xa7	8	0x00	Por Reset	0x20
gas_gauge_DATA11	0xa8	8	0x00	Por Reset	0x20
VBAT_ADC_B<15:8>	0xa9	8	OTP	Por Reset	0x20
VBAT_ADC_B<7:0>	0xaa	8	OTP	Por Reset	0x20
VBAT_ADC_K<15:8>	0xab	8	OTP	Por Reset	0x20
VBAT_ADC_K<7:0>	0xac	8	OTP	Por Reset	0x20
TS_ADC_K<15:8>	0xad	8	OTP	Por Reset	0x20
TS_ADC_K<7:0>	0xae	8	OTP	Por Reset	0x20
TS_ADC_B<15:8>	0xaf	8	OTP	Por Reset	0x20
TS_ADC_B<7:0>	0xb0	8	OTP	Por Reset	0x20
PMIC_POWER_EN0	0xb1	8	OTP	Shutdown Reset	0x20
PMIC_POWER_EN1	0xb2	8	OTP	Shutdown Reset	0x20
PMIC_POWER_EN2	0xb3	8	OTP	Shutdown Reset	0x20
PMIC_POWER_EN3	0xb4	8	OTP	Shutdown Reset	0x20
PMIC_POWER_SLP_EN0	0xb5	8	OTP	Shutdown Reset	0x20
PMIC_POWER_SLP_EN1	0xb6	8	OTP	Shutdown Reset	0x20
PMIC_POWER_DISCHRG_EN0	0xb7	8	0xff	Por Reset	0x20
PMIC_POWER_DISCHRG_EN1	0xb8	8	0xff	Por Reset	0x20
PMIC_POWER_CONFIG	0xb9	8	0x00	Por Reset	0x20
PMIC_BUCK1_CONFIG	0xba	8	0x64	Shutdown Reset	0x20
PMIC_BUCK1_ON_VSEL	0xbb	8	OTP	Shutdown Reset	0x20
PMIC_BUCK1_SLP_VSEL	0xbc	8	OTP	Shutdown Reset	0x20
PMIC_BUCK2_CONFIG	0xbd	8	0x64	Shutdown Reset	0x20
PMIC_BUCK2_ON_VSEL	0xbe	8	OTP	Shutdown Reset	0x20
PMIC_BUCK2_SLP_VSEL	0xbf	8	OTP	Shutdown Reset	0x20
PMIC_BUCK3_CONFIG	0xc0	8	0x64	Shutdown Reset	0x20
PMIC_BUCK3_ON_VSEL	0xc1	8	OTP	Shutdown Reset	0x20
PMIC_BUCK3_SLP_VSEL	0xc2	8	OTP	Shutdown Reset	0x20
PMIC_BUCK4_CONFIG	0xc3	8	0x64	Shutdown Reset	0x20

Name	Offset	Size	Reset Value	Description	I2C address 7Bits
PMIC_BUCK4_ON_VSEL	0xc4	8	OTP	Shutdown Reset	0x20
PMIC_BUCK4_SLP_VSEL	0xc5	8	OTP	Shutdown Reset	0x20
PMIC_BUCK4_CMIN	0xc6	8	0x04	Por Reset	0x20
PMIC_LDO1_ON_VSEL	0xcc	8	OTP	Shutdown Reset	0x20
PMIC_LDO1_SLP_VSEL	0xcd	8	OTP	Shutdown Reset	0x20
PMIC_LDO2_ON_VSEL	0xce	8	OTP	Shutdown Reset	0x20
PMIC_LDO2_SLP_VSEL	0xcf	8	OTP	Shutdown Reset	0x20
PMIC_LDO3_ON_VSEL	0xd0	8	OTP	Shutdown Reset	0x20
PMIC_LDO3_SLP_VSEL	0xd1	8	OTP	Shutdown Reset	0x20
PMIC_LDO4_ON_VSEL	0xd2	8	OTP	Shutdown Reset	0x20
PMIC_LDO4_SLP_VSEL	0xd3	8	OTP	Shutdown Reset	0x20
PMIC_LDO5_ON_VSEL	0xd4	8	OTP	Shutdown Reset	0x20
PMIC_LDO5_SLP_VSEL	0xd5	8	OTP	Shutdown Reset	0x20
PMIC_LDO6_ON_VSEL	0xd6	8	OTP	Shutdown Reset	0x20
PMIC_LDO6_SLP_VSEL	0xd7	8	OTP	Shutdown Reset	0x20
PMIC_LDO9_ON_VSEL	0xdc	8	OTP	Shutdown Reset	0x20
PMIC_LDO9_SLP_VSEL	0xdd	8	OTP	Shutdown Reset	0x20
PMIC_BOOST_OTG_CONFIG0	0xde	8	0x0b	Shutdown Reset	0x20
PMIC_BOOST_CONFIG1	0xdf	8	0x33	Shutdown Reset	0x20
PMIC_CHRG_OUT	0xe4	8	0xa2	Por Reset	0x20
PMIC_CHRG_IN	0xe5	8	0xc8	Por Reset	0x20
PMIC_CHRG_TERM	0xe6	8	0xc1	Por Reset:Bit7,Bit5~Bit0 Shutdown Reset:Bit6	0x20
PMIC_CHRG_TERM_DIG	0xe7	8	0x00	Por Reset	0x20
PMIC_BAT_HTS_TS	0xe8	8	0x00	Por Reset	0x20
PMIC_BAT_LTS_TS	0xe9	8	0xff	Por Reset	0x20
PMIC_CHRG_TO	0xea	8	0x22	Por Reset	0x20
PMIC_CHRG_STS	0xeb	8	0x00	Por Reset	0x20
PMIC_BAT_DISCHRG	0xec	8	0x0a	Por Reset	0x20
PMIC_CHIP_NAME	0xed	8	0x81	Por Reset	0x20
PMIC_CHIP_VER	0xee	8	0x72	Por Reset	0x20
PMIC_OTP_VER	0xef	8	OTP	Por Reset	0x20
PMIC_SYS_STS	0xf0	8	0x00	Por Reset:Bit6~Bit0 Shutdown Reset:Bit7	0x20
PMIC_SYS_CFG0	0xf1	8	0x84	Shutdown Reset	0x20

Name	Offset	Size	Reset Value	Description	I2C address 7Bits
PMIC_SYS_CFG1	0xf2	8	0x80	Por Reset:Bit6~Bit0 Shutdown Reset:Bit7	0x20
PMIC_SYS_CFG2	0xf3	8	0x00	Por Reset	0x20
PMIC_SYS_CFG3	0xf4	8	0x20	Shutdown Reset	0x20
PMIC_ON_SOURCE	0xf5	8	0x00	Por Reset:Bit7~Bit6	0x20
PMIC_OFF_SOURCE	0xf6	8	0x00		0x20
PMIC_PWRON_KEY	0xf7	8	0x06	Por Reset	0x20
PMIC_INT_STS0	0xf8	8	0x00	Por Reset	0x20
PMIC_INT_MSK0	0xf9	8	0x00	Por Reset	0x20
PMIC_INT_STS1	0xfa	8	0x00	Por Reset	0x20
PMIC_INT_MSK1	0xfb	8	0x00	Por Reset	0x20
PMIC_INT_STS2	0xfc	8	0x00	Por Reset	0x20
PMIC_INT_MSK2	0xfd	8	0x00	Por Reset	0x20
PMIC_GPIO_INT_CONFIG	0xfe	8	0x22	Por Reset	0x20
POWER_CONFIG2	0x67	8	0x00	Por Reset	0x20
CODEC_CONFIG	0x8C	8	0x00	Por Reset	0x20
APLL_CFG6	0x8B	8	0x0D	Por Reset	0x20
POWER_CONFIG2	0x67	8	0x00	Por Reset	0x20
CODEC_CONFIG	0x8C	8	0x00	Por Reset	0x20
PLDO_HRDEC_EN	0x8A	8	0x00	Por Reset	0x20
SYS_CFG4	0x66	8	0x00	Por Reset:Bit0 Shutdown Reset:Bit7~Bit1	0x20
SYS_CFG5	0x68	8	0x00	Por Reset	0x20
SYS_CFG6	0x69	8	0x00	Por Reset	0x20
SYS_CFG7_OFF_SOURCE2	0x6A	8	0x00	Por Reset:Bit7~Bit3 Shutdown Reset:Bit2~Bit0	0x20
INT_STS3	0x64	8	0x00	Por Reset	0x20
INT_MASK3	0x65	8	0x00	Por Reset	0x20
POWER_EXIT_SLP_SEQ0	0x60	8	0x00	Shutdown	0x22
POWER_EXIT_SLP_SEQ1	0x61	8	0x00	Shutdown	0x22
POWER_EXIT_SLP_SEQ2	0x62	8	0x00	Shutdown	0x22
POWER_EXIT_SLP_SEQ3	0x63	8	0x00	Shutdown	0x22
POWER_EXIT_SLP_SEQ4	0x64	8	0x00	Shutdown	0x22
POWER_EXIT_SLP_SEQ6	0x66	8	0x00	Shutdown	0x22
POWER_EXIT_SLP_SEQ7	0x67	8	0x00	Shutdown	0x22
POWER_ENTER_SLP_SD_SEQ0	0x68	8	0x00	Shutdown	0x22
POWER_ENTER_SLP_SD_SEQ1	0x69	8	0x00	Shutdown	0x22
POWER_ENTER_SLP_SD_SEQ2	0x6A	8	0x00	Shutdown	0x22

Name	Offset	Size	Reset Value	Description	I2C address 7Bits
POWER_ENTER_SLP_SD_SEQ3	0x6B	8	0x00	Shutdown	0x22
POWER_ENTER_SLP_SD_SEQ4	0x6C	8	0x00	Shutdown	0x22
POWER_ENTER_SLP_SD_SEQ6	0x6E	8	0x00	Shutdown	0x22
POWER_ENTER_SLP_SD_SEQ7	0x6F	8	0x00	Shutdown	0x22
device_id	0x00	8	OTP	Por Reset	0x22
int_sts	0x01	8	0x00	Shutdown	0x22
int_mask	0x02	8	0x3d	Shutdown	0x22
typec_ctrl	0x03	8	0x00	Shutdown	0x22
typec_ctrl1	0x04	8	0x00	Shutdown	0x22
typec_ctrl2	0x05	8	0x05	Shutdown	0x22
typec_ctrl3	0x06	8	0x03	Shutdown	0x22
typec_sts	0x07	8	0x00	Shutdown	0x22
typec_sts1	0x08	8	0x00	Shutdown	0x22
typec_rx_detect	0x09	8	0x00	Shutdown	0x22
typec_rx_detect1	0x0a	8	0x00	Shutdown	0x22
typec_rx_info	0x0b	8	0x00	Shutdown	0x22
typec_rx_ctrl	0x0c	8	0x00	Shutdown	0x22
typec_tx_cfg	0x0d	8	0x00	Shutdown	0x22
pd_tx_cfg1	0x0e	8	0x00	Shutdown	0x22
pd_tx_cfg2	0x0f	8	0x00	Shutdown	0x22
pd_tx_ctrl	0x10	8	0x00	Shutdown	0x22
typec_bmc_sts	0x11	8	0x00	Shutdown	0x22
Pd_reset	0x12	8	0x00	Shutdown	0x22
rx_cnt	0x13	8	0x00	Shutdown	0x22
reg_back	0x14	8	0x00	Shutdown	0x22
pd_data_header_l	0x15	8	0x00	Shutdown	0x22
pd_data_header_h	0x16	8	0x00	Shutdown	0x22
pd_data_buffer	0x17~ 0x32	8	0x00	Shutdown	0x22

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

5.2 Register Description

RTC_SECONDS
Address: (0x00)

Bit	Attr	Reset Value	Description
7	RW	0x0	RESV Reserved
6:4	RW	0x0	SEC1 Set the second digit of the RTC seconds (0-5)

Bit	Attr	Reset Value	Description
3:0	RW	0x0	SEC0 Set the first digit of the RTC seconds (0-9)

RTC_MINUTES
Address: (0x01)

Bit	Attr	Reset Value	Description
7	RW	0x0	RESV Reserved
6:4	RW	0x0	MIN1 Set the second digit of the RTC minutes (0-5)
3:0	RW	0x0	MIN0 Set the first digit of the RTC minutes (0-9)

RTC_HOURS
Address: (0x02)

Bit	Attr	Reset Value	Description
7	RW	0x0	AMPM Only used in PM-AM mode, 1: PM. 0:AM
6	RW	0x0	RESV Reserved
5:4	RW	0x0	HOUR1 Set the second digit of the RTC hours
3:0	RW	0x9	HOUR0 Set the first digit of the RTC hours

RTC_DAYS
Address: (0x03)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	RESV Reserved
5:4	RW	0x0	DAY1 Set the second digit of the RTC days
3:0	RW	0x4	DAY0 Set the first digit of the RTC days

RTC_MONTHS
Address: (0x04)

Bit	Attr	Reset Value	Description
7:5	RW	0x0	RESV Reserved

Bit	Attr	Reset Value	Description
4	RW	0x0	MONTH1 Set the second digit of the RTC months
3:0	RW	0x8	MONTH0 Set the first digit of the RTC months

RTC_YEARS
Address: (0x05)

Bit	Attr	Reset Value	Description
7:4	RW	0x1	YEAR1 Set the second digit of the RTC years
3:0	RW	0x7	YEAR0 Set the first digit of the RTC years

RTC_WEEKS
Address: (0x06)

Bit	Attr	Reset Value	Description
7:3	RW	0x00	RESV Reserved
2:0	RW	0x5	WEEK Set the second digit of the RTC weeks

RTC_ALARM_SECONDS
Address: (0x07)

Bit	Attr	Reset Value	Description
7	RW	0x0	RESV Reserved
6:4	RW	0x0	ALARM_SEC1 Set the second digit of the RTC alarm seconds
3:0	RW	0x0	ALARM_SEC0 Set the first digit of the RTC alarm seconds

RTC_ALARM_MINUTES
Address: (0x08)

Bit	Attr	Reset Value	Description
7	RW	0x0	RESV Reserved
6:4	RW	0x0	ALARM_MIN1 Set the second digit of the RTC alarm minutes

Bit	Attr	Reset Value	Description
3:0	RW	0x0	ALARM_MIN0 Set the first digit of the RTC alarm minutes

RTC_ALARM_HOURS
Address: (0x09)

Bit	Attr	Reset Value	Description
7	RW	0x0	ALARM_PM_AM Set alarm PM or AM: only used in PM-AM mode, 1: PM. 0:AM
6	RW	0x0	RESV Reserved
5:4	RW	0x0	ALARM_HOUR1 Set the second digit of the RTC alarm hours
3:0	RW	0x0	ALARM_HOUR0 Set the first digit of the RTC alarm hours

RTC_ALARM_DAYS
Address: (0x0a)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	RESV Reserved
5:4	RW	0x0	ALARM_DAY1 Set the second digit of the RTC alarm days
3:0	RW	0x1	ALARM_DAY0 Set the first digit of the RTC alarm days

RTC_ALARM_MONTHS
Address: (0x0b)

Bit	Attr	Reset Value	Description
7:5	RW	0x0	RESV Reserved
4	RW	0x0	ALARM_MONTH1 Set the second digit of the RTC alarm months
3:0	RW	0x1	ALARM_MONTH0 Set the first digit of the RTC alarm months

RTC_ALARM_YEARS
Address: (0x0c)

Bit	Attr	Reset Value	Description
7:4	RW	0x0	ALARM_YEAR1 Set the second digit of the RTC alarm years
3:0	RW	0x0	ALARM_YEAR0 Set the first digit of the RTC alarm years

RTC_RTC_CTRL
Address: (0x0d)

Bit	Attr	Reset Value	Description
7	RW	0x0	RTC_READ_SEL 0: Read access directly to dynamic registers 1: Read access to static shadowed registers
6	RW	0x0	GET_TIME Rising transition of this register transferred dynamic registers into static shadowed registers.
5	RW	0x0	SET_32_COUNTER 1: set the 32-kHz counter with COMP_REG value. Note: It must only be used when the RTC is frozen.
4	RW	0x0	RESV Reserved
3	RW	0x0	AMPM_MODE 0: 24 hours mode. 1: 12 hours mode (PM-AM mode)
2	RW	0x0	AUTO_COMP 0: No auto compensation. 1: Auto compensation enabled
1	RW	0x0	ROUND_30S When "1" is written, the time is rounded to the closest minute in next second. Note: self cleared after rounding (Auto Clr)
0	RW	0x0	STOP_RTC 1: RTC is frozen 0: RTC is running. Note: RTC_time can only be changed during RTC frozen.

RTC_RTC_STATUS
Address: (0x0e)

Bit	Attr	Reset Value	Description
7	W1C	0x1	POWER_UP POWER_UP is set by a reset, is cleared by writing "1" in this bit.

Bit	Attr	Reset Value	Description
6	W1C	0x0	ALARM Indicates that an alarm interrupt has been generated. Note: The alarm interrupt keeps its low level, until the micro-controller write "1" in the ALARM bit
5	W1C	0x0	EVENT_1D One day has occurred
4	W1C	0x0	EVENT_1H One hour has occurred
3	W1C	0x0	EVENT_1M One minute has occurred
2	W1C	0x0	EVENT_1S One second has occurred
1	RO	0x1	RUN 0: RTC is frozen. 1: RTC is running. Note: This bit shows the real state of the RTC.
0	RW	0x0	RESV Reserved

RTC_RTC_INT
Address: (0x0f)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	RESV Reserved
5	RW	0x0	RESV Reserved
4	RW	0x0	INT_SLEEP_MASK_EN 1: Mask periodic interrupt while the device is in SLEEP mode 0: Normal mode, no interrupt masked.
3	RW	0x0	INT_ALARM_EN Enable one interrupt when the alarm value is reached 1: Enable 0: Disable
2	RW	0x0	INT_TIMER_EN 1: Enable periodic interrupt; 0: disable periodic interrupt
1:0	RW	0x0	EVERY 00: every second; 01: every minute; 10: every hour; 11: every day

RTC_RTC_COMP_LSB
Address: (0x10)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	RTC_COMP_LSB This register contains the number of 32-kHz periods to be added into the 32KHz counter every hour [LSB]

RTC_RTC_COMP_MSB
Address: (0x11)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	RTC_COMP_MSB This register contains the number of 32-kHz periods to be added into the 32KHz counter every hour [MSB]

CODEC_DTOP_VUCTL
Address: (0x12)

Bit	Attr	Reset Value	Description
7	RW	0x0	ADC_BYPS ADC volume control bypass 0:ADC volume control enable 1: ADC volume control bypass
6	RW	0x0	DAC_BYPS 0:DAC volume control enable 1:DAC volume control bypass
5	RW	0x0	ADCFade ADC Fade: ADC volume adjust mode 0:update to new volume immediately; 1:update volume as ADCZDT field describes;
4	RW	0x0	DACFade DAC Fade: DAC volume adjust mode 0:update to new volume immediately; 1:update volume as DACZDT field describes;
3:2	RW	0x0	RESV Reserved
1	RW	0x1	ADCZDT ADC cross zero detect enable. It works when ADC_BYPS is 0 and ADC_FADE is 1. 0:volume adjusts every sample 1:volume adjusts only when audio waveform crosses zero or volume-control time-limit condition meets; Note: All codec register reset by 'RST'or power down.

Bit	Attr	Reset Value	Description
0	RW	0x1	DACZDT DAC cross zero detect enable. It works when DAC_BYPS is 0 and DAC_FADE is 1. 0:volume adjusts every sample 1:volume adjusts only when audio waveform crosses zero or volume-control time-limit condition meets; Note: All codec register reset by 'RST'or power down.

CODEC_DTOP_VUCTIME
Address: (0x13)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	VUCT VUCT: volume control time limit, valid only in fade cross zero mode Time limit = VUCT *(1/sample rate) Unit: LRCLK

CODEC_DTOP_LPT_SRST
Address: (0x14)

Bit	Attr	Reset Value	Description
7	RW	0x0	RESV Reserved
6	RW	0x0	SRST SRST:soft reset, write 1 to reset read 1: resetting 0: not resetting
5	RW	0x0	LP_DET LP_DET: low power detected, valid when DAC automatically power-on and power-down enabled 0:not detected; 1:low power detected;
4:0	RW	0x00	LPT LPT: low power detect threshold:power(2,LPT)

CODEC_DTOP_DIGEN_CLKE
Address: (0x15)

Bit	Attr	Reset Value	Description
7	RW	0x0	ADC_CKE ADC clock enable 1:enable; 0:disable;
6	RW	0x0	I2STX_CKE I2S Tx channel clock enable 1:enable; 0:disable;
5	RW	0x0	ADC_EN Digital adc channel enable 1:enable; 0:disable;

Bit	Attr	Reset Value	Description
4	RW	0x0	I2STX_EN I2S Tx channel enable 1:enable; 0:disable;
3	RW	0x0	DAC_CKE DAC clock enable 1:enable; 0:disable;
2	RW	0x0	I2SRX_CKE I2S Rx channel clock enable 1:enable; 0:disable;
1	RW	0x0	DAC_EN Digital dac channel enable 1:enable; 0:disable;
0	RW	0x0	I2SRX_EN I2S Rx channel enable 1:enable; 0:disable;

CODEC_AREF_RTCFG1
Address: (0x17)

Bit	Attr	Reset Value	Description
7	RW	0x0	Internal used, don't over write.
6	RW	0x0	RESV Reserved
5	RW	0x0	REF_ADC_SEL Select the ADC reference voltage 0: 1.2V 1: 1.5V
4:3	RW	0x0	VAG_SEL Select the VAG voltage 00:0.9V 01:0.72V 10:1.08V 11:1.26V
2	RW	0x1	PWD_IBIAS Power down the ibias block in REF_TOP 0:IBIAS block power on 1:IBIAS block power down
1	RW	0x1	PWD_VAG_BUF Power down the Vag buffer in REF_TOP 0:Vag buffer block power on 1:Vag buffer block power down
0	RW	0x0	RESV Reserved

CODEC_AADC_CFG0
Address: (0x18)

Bit	Attr	Reset Value	Description
7	RW	0x1	ADC_L_PWD Power down ADC left channel 0: ADC left channel power on 1: ADC left channel power down
6	RW	0x1	ADC_R_PWD Power down ADC right channel 0: ADC right channel power on 1: ADC right channel power down

Bit	Attr	Reset Value	Description
5	RW	0x0	ADC_CLK_EDGE_SEL Select the ADC output data and clock edge relationship 0: using the ADC falling edge to send the ADC data 1: using the ADC rising edge to send the ADC data
4	RW	0x0	RESV Reserved
3	RW	0x1	ADC_DITH_OFF Disable the dither function of ADC 0: enable the ADC dither 1:disable the ADC dither
2:0	RW	0x0	ADC_DITH_SEL Select the dither frequency of ADC 000: 1/50 of ADC clock 001: 1/33 of ADC clock 010: 1/20 of ADC clock 011: 1/15 of ADC clock 100: 1/10 of ADC clock 101: 1/8 of ADC clock 110: 1/6 of ADC clock 111: 1/4 of ADC clock

CODEC_DADC_VOLL
Address: (0x1a)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	ADCLV ADC path L-channel Digital Volume Register 0db~-95db, 0.375db/step 8'h0: 0db 8'h1:-0.375db 8'h2:-0.75db 8'h3:-1.125db … 8'hff:-95db

CODEC_DADC_VOLR
Address: (0x1b)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	ADCRV ADC path R-channel Digital Volume Register 0db~-95db, 0.375db/step 8'h0: 0db 8'h1:-0.375db 8'h2:-0.75db 8'h3:-1.125db … 8'hff:-95db

CODEC_DADC_SR_ACL0
Address: (0x1e)

Bit	Attr	Reset Value	Description
7	RW	0x0	RESV Reserved
6	RW	0x0	RESV Reserved
5	RW	0x0	ADC_LV_POL ADC path L-channel Digital Volume polarity 0:negative gain; 1:postive gain
4	RW	0x0	ADC_RV_POL ADC path R-channel Digital Volume polarity 0:negative gain; 1:postive gain
3	RW	0x0	RESV Reserved
2:0	RW	0x0	ADCSRT ADC sample rate times: sample rate = 8k/11.025k/12k * power(2,ADCSRT) note that sample rate base(8K/11.025K/12K) is decided by PLL configuration.

CODEC_DADC_HPF
Address: (0x22)

Bit	Attr	Reset Value	Description
7	RW	0x0	HPFL: high pass filter enable for left channel 0:high pass filter for left channel is disabled 1: high pass filter for left channel is enabled
6	RW	0x0	HPFR: high pass filter enable for right channel 0:high pass filter for right channel is disabled 1: high pass filter for right channel is enabled
5:4	RW	0x0	HPF_CF: high pass filter configure register 00:3.79Hz; 01:60Hz; 02:243Hz; 03:493Hz
3:0	RW	0x0	RESV Reserved

CODEC_DADC_RVOLL
Address: (0x23)

Bit	Attr	Reset Value	Description
7:0	RO	0xff	ADCRLV ADC internal gain of left ch

CODEC_DADC_RVOLR
Address: (0x24)

Bit	Attr	Reset Value	Description
7:0	RO	0xff	ADCRRV ADC internal gain of right ch

CODEC_AMIC_CFG0
Address: (0x27)

Bit	Attr	Reset Value	Description
7	RW	0x0	MIC_DIFF_EN Enable differential mic mode 0:disable 1:enable
6	RW	0x1	PWD_MIC MIC Power Down 0: MIC block power on 1: MIC block power down
5	RW	0x1	PWD_PGA_L PGA_L Power Down 0:PGA_L block power on 1:PGA_L block power down
4	RW	0x1	RESV Reserved
3:2	RW	0x0	MIC_L_BOOST Select the gain of left mic input signal 00:0dB, 01:10dB 10:20dB 11:30dB
1:0	RW	0x0	MIC_R_BOOST Select the gain of right mic input signal 00:0dB, 01:10dB 10:20dB 11:30dB

CODEC_AMIC_CFG1
Address: (0x28)

Bit	Attr	Reset Value	Description
7	RW	0x0	PGA_L_IN_SEL PGA L-channel input select 0: Positive end of Mic amplifier output 1:internal reference voltage
6	RW	0x0	PGA_R_IN_SEL PGA R-channel input select 0: Negative end of Mic amplifier output 1:internal reference voltage
5	RW	0x0	MIC_CHOP_EN Enable the chopping function of MIC 0:disable 1:enable
4	RW	0x0	PGA_CHOP_EN Enable the chopping function of PGA 0:disable 1:enable
3:2	RW	0x0	MIC_CHOP_SEL 00:200k, 01:400k, 10:800k, 11:Reserved
1:0	RW	0x0	PGA_CHOP_SEL 00:200k, 01:400k, 10:800k, 11:Reserved

CODEC_DMIC_PGA_GAIN
Address: (0x29)

Bit	Attr	Reset Value	Description
7:4	RW	0x6	PGA_L_GAIN Change the gain of PGA block, the value changed from -18dB to 27dB. 0000:-18db; 1111:27db, 3db/step
3:0	RW	0x6	PGA_R_GAIN Change the gain of PGA block, the value changed from -18dB to 27dB. 0000: -18db; 1111:27db, 3db/step

CODEC_ADAC_CFG1
Address: (0x2f)

Bit	Attr	Reset Value	Description
7	RW	0x0	DOUBLE_DACIBIAS double DAC internal current resource
6	RW	0x0	INC_DAC_SWITCH increase the DAC internal switch signal control time
5	RW	0x0	STOP_DAC_RSTB stop the RSTB clock
4	RW	0x0	STOP_DAC_SWITCH stop the switch clock in DAC
3	RW	0x0	PWD_DACIBIAS power down the DAC internal current resource 0: DACIBIAS powerup 1: DACIBIAS powerdown
2	RW	0x1	PWD_DACD Class D DAC power down 0: Class D DAC power up 1: Class D DAC power down
1	RW	0x1	PWD_DACL L channel DAC power down 0: L channel DAC power up 1: L channel DAC power down
0	RW	0x1	PWD_DACR R channel DAC power down 0: R channel DAC power up 1: R channel DAC power down

CODEC_DDAC_POPD_DACST
Address: (0x30)

Bit	Attr	Reset Value	Description
7:2	RW	0x0	RESV Reserved
1	RO	0x1	DAC_MTST DAC mute status 0:DAC is not in mute status 1:DAC is in mute status
0	RO	0x0	RESV Reserved

CODEC_DDAC_VOLL
Address: (0x31)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	DACLV DAC path L-channel Digital Volume Register -1.125db~-95db,0.375db/step 0~2 are not allowed to use, and only use 3~255

CODEC_DDAC_VOLR
Address: (0x32)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	DACRV DAC path R-channel Digital Volume Register -1.125db~-95db,0.375db/step 0~2 are not allowed to use, and only use 3~255

CODEC_DDAC_SR_LMT0
Address: (0x35)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	RESV Reserved
5	RW	0x0	DAC_LV_POL 0：negative gain; 1:postive gain
4	RW	0x0	DAC_RV_POL 0：negative gain; 1:postive gain
3	RW	0x0	RESV Reserved
2:0	RW	0x0	DACSRT DAC sample rate times sample rate = 8k/11.025k/12k * power(2,DACSRT)

CODEC_DDAC_MUTE_MIXCTL
Address: (0x38)

Bit	Attr	Reset Value	Description
7	RW	0x1	DAC_D_HPF 0:disable HPF;1:enable HPF;
6:5	RW	0x1	DAC_D_HPF_CF 00:80HZ; 01:100HZ; 02:120HZ; 03:140HZ
4	RW	0x0	CLASS_D_MODE 1:CLASS D mode, 0:L/R mode
3	RW	0x0	CLASSD_MODE_L_SEL 0：MIX L and R; 1：L
2	RW	0x0	RESV Reserved
1	RW	0x0	MIX_ON 0:mixer disable;1: Reserved;

Bit	Attr	Reset Value	Description
0	RW	0x0	DACMT DAC mute enable 0:DAC mute is disabled 1:DAC mute is enable

CODEC_DDAC_RVOLL
Address: (0x39)

Bit	Attr	Reset Value	Description
7:0	RO	0xff	DACRLV DAC internal gain of left ch

CODEC_DDAC_RVOLR
Address: (0x3a)

Bit	Attr	Reset Value	Description
7:0	RO	0xff	DACRRV DAC internal gain of right ch

CODEC_AHP_CFG0
Address: (0x3d)

Bit	Attr	Reset Value	Description
7	RW	0x1	PWD_SOSTAGE power down the HP SOSTAGE 0:power up 1:power down
6	RW	0x1	PWD_HP_OSTAGE power down the HP OSTAGE 0:power up 1:power down
5	RW	0x1	PWD_HP_BUF power down the HP pre amp stage 0:power up 1:power down
4:3	RW	0x0	INC_HP_AMP increase the HP amplitude from 3dB to 9dB, 00:0db 01:3db 10:6db 11: 9db
2	RW	0x0	HP_2STAGE_EN Power down the HP two stage opamp 0:disable 1:enable
1:0	RW	0x0	HP_IBIAS_SEL HP BIAS current select 00:100% 01:150% 10:200% 11:50%

CODEC_AHP_CFG1
Address: (0x3e)

Bit	Attr	Reset Value	Description
7:5	RW	0x0	RESV Reserved

Bit	Attr	Reset Value	Description
4	RW	0x1	HP_ANTIPOP_EN enable the HP antipop function 0:disable 1:enable
3:0	RW	0xf	HP_ANTIPOP_BIT control the HP antipop gain from -15dB to 0dB 0000: 0dB 0001:-1dB 0010:-2dB … 1111:-15dB

CODEC_AHP_CP
Address: (0x3f)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	RESV Reserved
5	RW	0x0	HP_CP_CLK_SEL 0：CLK select for head phone charge pump 1MHz□:500KHz
4	RW	0x0	HP_CP_EN HP charge pump enable. 0:disable 1:enable
3	RW	0x1	HP_CP_ENDIS_LDO HP charge pump discharge ldo enable 0:disable 1:enable
2	RW	0x0	HP_CP_HIMAXB HP charge pump max current: 0:500mA,1:750mA
1:0	RW	0x1	HP_CP_VSEL HP charge pump voltage select: 00:2.1V,01:2.3V⇫:2.5V,11:2.7V

CODEC_ACLASSD_CFG1
Address: (0x40)

Bit	Attr	Reset Value	Description
7	RW	0x0	CLASSD_EN CLASS D enable 0:disable 1:enable
6	RW	0x1	CLASSD_MUTE_EN CLASS D mute_ramp function enable 0:disable 1:enable
5	RW	0x1	CLASSD_SSC_EN CLASS D Spread-Spectrum enable 0:disable 1:enable
4	RW	0x0	CLASSD_SSC_SEL CLASS D Spread-Spectrum steps select 0: 8 steps 1:16 step
3:2	RW	0x2	CLASSD_MUTE_RATE 00:0ms;01:16ms;10:32ms;11:64ms

Bit	Attr	Reset Value	Description
1:0	RW	0x1	CLASSD_SW_RATE 00:2.5ns;01:5ns;10:7.5ns;11:10ns

CODEC_ACLASSD_CFG2
Address: (0x41)

Bit	Attr	Reset Value	Description
7	RO	0x0	CLASSD_OCP_STS IF this bit is high, it need to restart CLASS D.
6:4	RW	0x4	CLASSD_OCPP CLASS D PFET OCP Select 000: 0.5A 001: 0.625A 010: 0.75A 011: 0.875A 100:1A（Default） 101: 1.125A 110: 1.25A 111: 1.375A
3	RO	0x0	CLASSD_MUTE_DONE When class d mute finished, this bit will be set high.
2:0	RW	0x4	RESV Reserved

CODEC_APLL_CFG0
Address: (0x42)

Bit	Attr	Reset Value	Description
7:5	RW	0x0	RESV Reserved
4	RW	0x0	PLL_CLKIN_SEL the PLL input clock select, 0->main clk 1->main clk/2
3:0	RW	0x0	RESV Reserved

CODEC_APLL_CFG4
Address: (0x46)

Bit	Attr	Reset Value	Description
7:4	RW	0x6	PLL_OUTDIV PLL VCO output clock divide value select outdiv<3:2>: 00-> divide 5 01-> divide 10 10-> divide 3 11-> divide 6 outdiv<1:0>: 00-> divide 3 01-> divide 1 10-> divide 2 11-> divide 1"
3:0	RW	0x5	RESV Reserved

CODEC_APLL_CFG5
Address: (0x47)

Bit	Attr	Reset Value	Description
7:3	RW	0x00	RESV Reserved

Bit	Attr	Reset Value	Description
2	RW	0x0	PLL_RESET reset the total PLL register 0:release reset 1:set reset
1	RW	0x0	PLL_TEST check the PLL internal VCO control voltage 0:disable 1:enable
0	RW	0x1	PLL_PWD pll power down 0: PLL power up 1:PLL power down

CODEC_DI2S_CKM
Address: (0x48)

Bit	Attr	Reset Value	Description
7:4	RW	0x0	SCK_DIV F(mclk2x)/F(sclk) - 1
3	RW	0x0	PDM_EN I2S SDO output delta-sigma ADC 1bit data. 0:disable; 1:enable.
2	RW	0x0	SCK_EN i2ssclk clock enable, active in master mode. 0:disable 1:enable
1	RW	0x0	SCK_P sclk polarity 0: normal 1:inverted
0	RW	0x1	I2S_TX_MST I2S TX module as 0: slave mode 1: master mode

CODEC_DI2S_RSD
Address: (0x49)

Bit	Attr	Reset Value	Description
7:4	RW	0x0	RESV Reserved
3	RW	0x0	PDM_LR_SEL 0：L; 1：R
2:1	RW	0x0	SCKD_RX sclk divider for rxlrck generator 00:64 01:128 10:256(01 valid only if lrclk<= 96k, 10 valid only if lrclk<= 48k)
0	RW	0x0	RXRL_P I2S Rx lrck polarity 0: normal 1:inverted

CODEC_DI2S_RXCR1
Address: (0x4a)

Bit	Attr	Reset Value	Description
7	RW	0x0	RESV Reserved
6	RW	0x0	TFS_RX Rx transfer mode selector: 0: I2S 1:PCM
5:4	RW	0x0	PBM_RX Rx PCM bus mode: 00: delay0 01:delay1 10: delay2 11:delay3
3:2	RW	0x0	IBM_RX Rx I2S bus mode: 00: normal 01:left 10:right
1	RW	0x0	EXRL_RX Rx exchange right/left channel for rx 0: normal 1:exchange right and left channel
0	RW	0x0	LSB_RX 0: LSB 1:MSB

CODEC_DI2S_RXCR2
Address: (0x4b)

Bit	Attr	Reset Value	Description
7:5	RW	0x0	RESV Reserved
4:0	RW	0x17	VDW_RX valid date width 0x17: 24 bits data width; 0x0F: 16 bits data width; others: reserved

CODEC_DI2S_RXCMD_TSD
Address: (0x4c)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	RESV Reserved
5	RW	0x0	RXS rx transfer start 0: rx stop 1:rx start
4	RW	0x0	RXC rx transfer clear, high active
3	RW	0x0	RESV Reserved
2:1	RW	0x0	SCKD_TX sclk divider for txlrck generator 00:64 01:128 10:256(01 valid only if lrclk<= 96k, 10 valid only if lrclk<= 48k)
0	RW	0x0	TXRL_P I2S Txlrck polarity 0:normal 1:inverted

CODEC_DI2S_TXCR1
Address: (0x4d)

Bit	Attr	Reset Value	Description
7	RW	0x0	RESV Reserved
6	RW	0x0	TFS_TX Tx transfer mode selector: 0: I2S 1:PCM
5:4	RW	0x0	PBM_TX Tx PCM bus mode: 00: delay0 01: delay1 10: delay2
3:2	RW	0x0	IBM_TX Tx I2S bus mode: 00: normal 01:left 10:right
1	RW	0x0	EXRL_TX Tx exchange right/left channel for TX 0: normal 1:exchange right and left channel
0	RW	0x0	LSB_TX 0: LSB 1:MSB

CODEC_DI2S_TXCR2
Address: (0x4e)

Bit	Attr	Reset Value	Description
7:5	RW	0x0	RESV Reserved
4:0	RW	0x17	VDW_TX valid date width 0x17: 24 bits data width; 0x0F: 16 bits data width; others: reserved

CODEC_DI2S_TXCR3_TXCMD
Address: (0x4f)

Bit	Attr	Reset Value	Description
7	RW	0x0	TXS tx transfer start 0: tx stop 1:tx start
6	RW	0x0	TXC tx transfer clear, high active
5:0	RW	0x00	RCNT_TX right justified counter for I2S right justified slave mode only

gas_gauge_ADC_CONFIG0
Address: (0x50)

Bit	Attr	Reset Value	Description
7	RW	0x1	GG_EN GG_EN: Gasgauge module enable bit 0:disable 1: enable

Bit	Attr	Reset Value	Description
6	RW	0x0	SW1_VOL_ADC_EN SW1_VOL_ADC_EN: if GG_EN=0, then the ADC of SWOUT1 voltage controlled by the bit 0:disable 1:enable
5	RW	0x0	RESV RESV: Reserve
4	RW	0x0	SW2_VOL_ADC_EN SW2_VOL_ADC_EN: if GG_EN=0, the ADC of SWOUT2 voltage by the bit 0:disable 1:enable
3	RW	0x1	BAT_VOL_ADC_EN BAT_VOL_ADC_EN: if GG_EN=0, then the ADC of BATDIV voltage controlled by the bit 0:disable 1:enable
2	RW	0x1	BAT_CUR_ADC_EN BAT_CUR_ADC_EN: if GG_EN=0, then the ADC of BAT current controlled by the bit 0:disable 1:enable
1	RW	0x0	RESV RESV: Reserve
0	RW	0x0	ADC_SLP_RATE ADC_SLP_RATE: the ADC sample rate: 0:512; 1:1024

gas_gauge_ADC_CONFIG1
Address: (0x55)

Bit	Attr	Reset Value	Description
7	RC	0x0	VOL_CUR_CALIB_UPD VOL_CUR_CALIB_UPD: The voltage ADC and current ADC calibration finished status 0:not finished 1:finished (Write "1" to clear)
6	RW	0x0	RESV RESV: Reserve
5:4	RW	0x3	RESV RESV: Reserve
3	RW	0x0	RESV RESV: Reserve
2	RW	0x0	RESV RESV: Reserve
1:0	RW	0x0	RLX_CUR_FILTER RLX_CUR_FILTER：Relax mode enter threshold filter. 00:4S; 01:1S; 10:2S; 11:8S;

gas_gauge_GG_CON
Address: (0x56)

Bit	Attr	Reset Value	Description
7:6	RW	0x1	RLX_SPT RLX_SPT: relax mode voltage sampling interval time T_RELAX: Relax mode enter and quit time 00:8min 01:16min 10:32min 11:48min
5:4	RW	0x0	ADC_OFF_CAL_INTERV ADC_OFF_CAL_INTERV<1:0>: ADC offset calibration interval time 00:8min 01:16min 10:32min 11:48min
3:2	RW	0x1	FRAME_SMP_INTERV FRAME_SMP_INTERV<1:0>:Data frame sample interval in the sleep state(Unit:S) 00:0S 01:1S 10:2S 11:3S
1	RW	0x0	VOL_OUT_MOD VOL_OUT_MOD: Voltage output mode 0:Average Voltage 1:Instant Voltage
0	RW	0x0	CUR_OUT_MOD CUR_OUT_MOD: Current output mode 0:Average Current 1:Instant Current

gas_gauge_GG_STS
Address: (0x57)

Bit	Attr	Reset Value	Description
7	RO	0x0	RESV Reserved
6	RO	0x0	TERM_UPD TERM_UPD: Flag bit for Q_TERM update 0：NOT 1:YES
5	RW	0x0	QMAX_UPD_SOFT QMAX_UPD_SOFT: software Flag bit for QMAX update 0：NOT 1:YES
4	RO	0x0	BAT_CON BAT_CON: battery first connection, edge trigger 0:NOT 1:YES
3	RO	0x0	RELAX_VOL1_UPD RELAX_VOL1_UPD: battery voltage1 updated in relax status 0:NOT 1:YES
2	RO	0x0	RELAX_VOL2_UPD RELAX_VOL2_UPD: battery voltage2 updated in relax status 0:NOT 1:YES
1	RO	0x0	RELAX_STS RELAX_STS: battery coming into relax status 0:NOT 1:YES
0	RO	0x0	RESV Reserved

gas_gauge_RELAX_THRE_H
Address: (0x58)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	RELAX_THRE_CUR RELAX_THRE_CUR: relax mode threshold current set.<15:8>

gas_gauge_RELAX_THRE_L
Address: (0x59)

Bit	Attr	Reset Value	Description
7:0	RW	0x60	RELAX_THRE_CUR RELAX_THRE_CUR: relax mode threshold current set. <7:0>

gas_gauge_RELAX_VOL1_H
Address: (0x5a)

Bit	Attr	Reset Value	Description
7:0	RO	0x00	RELAX_VOL1_H RELAX_VOL1_H<15:8>: relax 1st mode voltage

gas_gauge_RELAX_VOL1_L
Address: (0x5b)

Bit	Attr	Reset Value	Description
7:0	RO	0x00	RELAX_VOL1_L RELAX_VOL1_L<7:0>: relax 1st mode voltage

gas_gauge_RELAX_VOL2_H
Address: (0x5c)

Bit	Attr	Reset Value	Description
7:0	RO	0x00	RELAX_VOL2 RELAX_VOL2<15:8>: relax 2nd mode voltage

gas_gauge_RELAX_VOL2_L
Address: (0x5d)

Bit	Attr	Reset Value	Description
7:0	RO	0x00	RELAX_VOL2 RELAX_VOL2<7:0>: relax 2nd mode voltage

gas_gauge_RELAX_CUR1_H
Address: (0x5e)

Bit	Attr	Reset Value	Description
7:0	RO	0x00	RELAX_CUR1 RELAX_CUR1<15:8>:relax 1st mode current

gas_gauge_RELAX_CUR1_L
Address: (0x5f)

Bit	Attr	Reset Value	Description
7:0	RO	0x00	RELAX_CUR1 RELAX_CUR1<7:0>: relax 1st mode current

gas_gauge_RELAX_CUR2_H
Address: (0x60)

Bit	Attr	Reset Value	Description
7:0	RO	0x00	RELAX_CUR2 RELAX_CUR2<15:8>: relax 2nd mode current

gas_gauge_RELAX_CUR2_L
Address: (0x61)

Bit	Attr	Reset Value	Description
7:0	RO	0x00	RELAX_CUR2 RELAX_CUR2<7:0>: relax 2nd mode current

gas_gauge_OCV_THRE_VOL
Address: (0x62)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	OCV_THRE_VOL OCV_THRE_VOL:OCV mode threshold. 00:0.5mV; 01:1mV; 02:1.5mV…..FF:127.5mV

gas_gauge_OCV_VOL_H
Address: (0x63)

Bit	Attr	Reset Value	Description
7:0	RO	0x00	OCV_VOL_REG OCV_VOL_REG<15:8>: OCV voltage

gas_gauge_PWRON_VOL_H
Address: (0x6b)

Bit	Attr	Reset Value	Description
7:0	RO	0x00	PWRON_VOL_REG PWRON_VOL_REG<15:8>: power on bat voltage

gas_gauge_PWRON_VOL_L
Address: (0x6c)

Bit	Attr	Reset Value	Description
7:0	RO	0x00	PWRON_VOL_REG PWRON_VOL_REG<7:0>: power on bat voltage

gas_gauge_PWRON_CUR_H
Address: (0x6d)

Bit	Attr	Reset Value	Description
7:0	RO	0x00	PWRON_CUR_REG PWRON_CUR_REG<15:8>: power on bat current

gas_gauge_PWRON_CUR_L
Address: (0x6e)

Bit	Attr	Reset Value	Description
7:0	RO	0x00	PWRON_CUR_REG PWRON_CUR_REG<7:0>: power on bat current

gas_gauge_OFF_CNT
Address: (0x6f)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	OFF_CNT OFF_CNT<7:0>: power off time; 10MIN COUNTER ADD 1

gas_gauge_Q_INIT_H3
Address: (0x70)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	Q_INIT Q_INIT<31:24>:Initial value of coulomb

gas_gauge_Q_INIT_H2
Address: (0x71)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	Q_INIT Q_INIT<23:16>:Initial value of coulomb

gas_gauge_Q_INIT_L1
Address: (0x72)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	Q_INIT Q_INIT<15:8>:Initial value of coulomb

gas_gauge_Q_INIT_L0
Address: (0x73)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	Q_INIT Q_INIT<7:0>:Initial value of coulomb

gas_gauge_Q_PRES_H3
Address: (0x74)

Bit	Attr	Reset Value	Description
7:0	RO	0x00	Q_PRES Q_PRES<31:24>:Coulomb value

gas_gauge_Q_PRES_H2
Address: (0x75)

Bit	Attr	Reset Value	Description
7:0	RO	0x00	Q_PRES Q_PRES<23:16>:Coulomb value

gas_gauge_Q_PRES_L1
Address: (0x76)

Bit	Attr	Reset Value	Description
7:0	RO	0x00	Q_PRES Q_PRES<15:8>:Coulomb value

gas_gauge_Q_PRES_L0
Address: (0x77)

Bit	Attr	Reset Value	Description
7:0	RO	0x00	Q_PRES Q_PRES<7:0>:Coulomb value

gas_gauge_BAT_VOL_H
Address: (0x78)

Bit	Attr	Reset Value	Description
7:0	RO	0x00	BAT_VOL BAT_VOL<15:8>: batdiv voltage

gas_gauge_BAT_VOL_L
Address: (0x79)

Bit	Attr	Reset Value	Description
7:0	RO	0x00	BAT_VOL BAT_VOL<7:0>:batdiv voltage

gas_gauge_BAT_CUR_H
Address: (0x7a)

Bit	Attr	Reset Value	Description
7:0	RO	0x00	BAT_CUR BAT_CUR<15:8>:battery current

gas_gauge_BAT_CUR
Address: (0x7b)

Bit	Attr	Reset Value	Description
7:0	RO	0x00	BAT_CUR BAT_CUR<7:0>:BAT_CUR: battery current

gas_gauge_SW2_VOL_H
Address: (0x7e)

Bit	Attr	Reset Value	Description
7:0	RO	0x00	SWOUT2_VOL SWOUT2_VOL<15:8>：SWOUT2 voltage value

gas_gauge_SW2_VOL_L
Address: (0x7f)

Bit	Attr	Reset Value	Description
7:0	RO	0x00	SWOUT2_VOL SWOUT2_VOL<7:0>：SWOUT2 voltage value

gas_gauge_SW1_VOL_H
Address: (0x80)

Bit	Attr	Reset Value	Description
7:0	RO	0x00	SWOUT1_VOL SWOUT1_VOL<15:8>: SWOUT1 voltage value

gas_gauge_SW1_VOL_L
Address: (0x81)

Bit	Attr	Reset Value	Description
7:0	RO	0x00	SWOUT1_VOL SWOUT1_VOL<7:0>：SWOUT1 voltage value

gas_gauge_Q_MAX_H3

Address: (0x82)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	Q_MAX Q_MAX<31:24>：Qmax value

gas_gauge_Q_MAX_H2
Address: (0x83)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	Q_MAX Q_MAX<23:16>：Qmax value

gas_gauge_Q_MAX_L1
Address: (0x84)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	Q_MAX Q_MAX<15:8>：Qmax value

gas_gauge_Q_MAX_L0
Address: (0x85)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	Q_MAX Q_MAX<7:0>：Qmax value

gas_gauge_Q_TERM_H3
Address: (0x86)

Bit	Attr	Reset Value	Description
7:0	RO	0x00	Q_TERM Q_TERM<31:24>：charge terminal Coulomp value

gas_gauge_Q_TERM_H2
Address: (0x87)

Bit	Attr	Reset Value	Description
7:0	RO	0x00	Q_TERM Q_TERM<23:16>：charge terminal Coulomp value

gas_gauge_Q_TERM_L1
Address: (0x88)

Bit	Attr	Reset Value	Description
7:0	RO	0x00	Q_TERM Q_TERM<15:8>：charge terminal Coulomp value

gas_gauge_Q_TERM_L0
Address: (0x89)

Bit	Attr	Reset Value	Description
7:0	RO	0x00	Q_TERM Q_TERM<7:0>：charge terminal Coulomp value

CUR_ADC_K<15:8>
Address: (0x8d)

Bit	Attr	Reset Value	Description
7:0	RO	0x00	CUR_ADC_K<15:8> CUR_ADC_K<15:8>:The high 8 bits of the external calibration K value for the current ADC

CUR_ADC_K<7:0>
Address: (0x8e)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	CUR_ADC_K<7:0> CUR_ADC_K<7:0>: The low 8 bits of the external calibration K value for the current ADC

gas_gauge_SLEEP_CON_SAMP_CUR_H
Address: (0x8f)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	SLEEP_CON_SAMP_CUR SLEEP_CON_SAMP_CUR<15:8>:SLEEP mode，When the current is greater than the set value, it is sampled once again, until it is less than the set value, and the value is updated to the RELAX register

gas_gauge_SLEEP_CON_SAMP_CUR
Address: (0x90)

Bit	Attr	Reset Value	Description
7:0	RW	0x60	SLEEP_CON_SAMP_CUR SLEEP_CON_SAMP_CUR<7:0>: SLEEP mode，When the current is greater than the set value, it is sampled once again, until it is less than the set value, and the value is updated to the RELAX register

gas_gauge_CAL_OFFSET_H
Address: (0x91)

Bit	Attr	Reset Value	Description
7:0	RW	0x7f	CAL_OFFSET_REG CAL_OFFSET_REG<15:8>: PCB current offset value high bit

gas_gauge_CAL_OFFSET_L
Address: (0x92)

Bit	Attr	Reset Value	Description
7:0	RW	0xff	CAL_OFFSET_REG CAL_OFFSET_REG<7:0>: PCB current offset value low bit

gas_gauge_VCALIB0_H
Address: (0x93)

Bit	Attr	Reset Value	Description
7:0	RO	0x00	VCALIB0 VCALIB0<15:8>:Voltage0 offset value for AP to calculate offset error and gain error

gas_gauge_VCALIB0_L
Address: (0x94)

Bit	Attr	Reset Value	Description
7:0	RO	0x00	VCALIB0 VCALIB0<7:0>:Voltage0 offset value for AP to calculate offset error and gain error

gas_gauge_VCALIB1_H
Address: (0x95)

Bit	Attr	Reset Value	Description
7:0	RO	0x00	VCALIB1 VCALIB1<15:8>:Voltage1 offset value for AP to calculate offset error and gain error

gas_gauge_VCALIB1_L
Address: (0x96)

Bit	Attr	Reset Value	Description
7:0	RO	0x00	VCALIB1 VCALIB1<7:0>:Voltage1 offset value for AP to calculate offset error and gain error

gas_gauge_IOFFSET_H
Address: (0x97)

Bit	Attr	Reset Value	Description
7:0	RO	0x00	IOFFSET IOFFSET<15:8>:Current offset value calculated

gas_gauge_IOFFSET_L
Address: (0x98)

Bit	Attr	Reset Value	Description
7:0	RO	0x00	IOFFSET IOFFSET<7:0>:Current offset value calculated

gas_gauge_BAT_R0
Address: (0x99)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	BAT_R0 BAT_R0<7:0>:BAT resistance

gas_gauge_BAT_R1
Address: (0x9a)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	BAT_R1 BAT_R1<7:0>:BAT resistance

gas_gauge_BAT_R2
Address: (0x9b)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	BAT_R2 BAT_R2<7:0>:BAT resistance

gas_gauge_BAT_R3
Address: (0x9c)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	BAT_R3 BAT_R3<7:0>:BAT resistance

gas_gauge_DATA0
Address: (0x9d)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	DATA DATA<7:0>:data for AP

gas_gauge_DATA1

Address: (0x9e)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	DATA DATA<7:0>:data for AP

gas_gauge_DATA2
Address: (0x9f)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	DATA DATA<7:0>:data for AP

gas_gauge_DATA3
Address: (0xa0)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	DATA DATA<7:0>:data for AP

gas_gauge_DATA4
Address: (0xa1)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	DATA DATA<7:0>:data for AP

gas_gauge_DATA5
Address: (0xa2)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	DATA DATA<7:0>:data for AP

gas_gauge_DATA6
Address: (0xa3)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	DATA DATA<7:0>:data for AP

gas_gauge_DATA7
Address: (0xa4)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	DATA DATA<7:0>:data for AP

gas_gauge_DATA8

Address: (0xa5)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	DATA DATA<7:0>:data for AP

gas_gauge_DATA9
Address: (0xa6)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	DATA DATA<7:0>:data for AP

gas_gauge_DATA10
Address: (0xa7)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	DATA DATA<7:0>:data for AP

gas_gauge_DATA11
Address: (0xa8)

Bit	Attr	Reset Value	Description
7:0	RW	0x00	DATA DATA<7:0>:data for AP

VBAT_ADC_B<15:8>
Address:(0xa9)

Bit	Attr	Reset Value	Description
7:0	RO	OTP	VBAT_ADC_B<15:8> default:OTP

VBAT_ADC_B<7:0>
Address:(0xaa)

Bit	Attr	Reset Value	Description
7:0	RO	OTP	VBAT_ADC_B<7:0> default: OTP

VBAT_ADC_K<15:8>
Address:(0xab)

Bit	Attr	Reset Value	Description
7:0	RO	OTP	VBAT_ADC_K<15:8> default: OTP

VBAT_ADC_K<7:0>

Address:(0xac)

Bit	Attr	Reset Value	Description
7:0	RO	OTP	VBAT_ADC_K<7:0> default: OTP

TS_ADC_K<15:8>
Address:(0xad)

Bit	Attr	Reset Value	Description
7:0	RO	OTP	TS_ADC_K<15:8> default: OTP

TS_ADC_K<7:0>
Address:(0x00ae)

Bit	Attr	Reset Value	Description
7:0	RO	OTP	TS_ADC_K<7:0> default: OTP

TS_ADC_B<15:8>
Address:(0xaf)

Bit	Attr	Reset Value	Description
7:0	RO	OTP	TS_ADC_B<15:8> default: OTP

TS_ADC_B<7:0>
Address:(0xb0)

Bit	Attr	Reset Value	Description
7:0	RO	OTP	TS_ADC_B<7:0> default: OTP

PMIC_POWER_EN0
Address: (0xb1)

Bit	Attr	Reset Value	Description
7	RW	0x0	BUCK4_EN_MASK BUCK4_EN_MASK: MUST write them to "1" if want to change corresponding BUCK4_EN bit，The BUCK4_EN_MASK bits should be clear when BUCK4_EN bits have been written.

Bit	Attr	Reset Value	Description
6	RW	0x0	BUCK3_EN_MASK BUCK3_EN_MASK: MUST write them to "1" if want to change corresponding BUCK3_EN bit，The BUCK3_EN_MASK bits should be clear when BUCK3_EN bits have been written.
5	RW	0x0	BUCK2_EN_MASK BUCK2_EN_MASK: MUST write them to "1" if want to change corresponding BUCK2_EN bit，The BUCK2_EN_MASK bits should be clear when BUCK2_EN bits have been written.
4	RW	0x0	BUCK1_EN_MASK BUCK1_EN_MASK: MUST write them to "1" if want to change corresponding BUCK1_EN bit，The BUCK1_EN_MASK bits should be clear when BUCK1_EN bits have been written.
3	RW	OTP	BUCK4_EN BUCK4_EN: BUCK4 enable in active mode 1, Enable 0, Disable the default value is set by otp reset by power down or RST.
2	RW	OTP	BUCK3_EN BUCK3_EN: BUCK3 enable in active mode 1, Enable 0, Disable the default value is set by otp reset by power down or RST.
1	RW	OTP	BUCK2_EN BUCK2_EN: BUCK2 enable in active mode 1, Enable 0, Disable the default value is set by otp reset by power down or RST.
0	RW	OTP	BUCK1_EN BUCK1_EN: BUCK1 enable in active mode 1, Enable 0, Disable the default value is set by otp reset by power down or RST.

PMIC_POWER_EN1
Address: (0xb2)

Bit	Attr	Reset Value	Description
7	RW	0x0	LDO4_EN_MASK LDO4_EN_MASK: MUST write them to "1" if want to change corresponding LDO4_EN bit，The LDO4_EN_MASK bits should be clear when LDO4_EN bits have been written.
6	RW	0x0	LDO3_EN_MASK LDO3_EN_MASK: MUST write them to "1" if want to change corresponding LDO3_EN bit，The LDO3_EN_MASK bits should be clear when LDO3_EN bits have been written.
5	RW	0x0	LDO2_EN_MASK LDO2_EN_MASK: MUST write them to "1" if want to change corresponding LDO2_EN bit，The LDO2_EN_MASK bits should be clear when LDO2_EN bits have been written.
4	RW	0x0	LDO1_EN_MASK LDO1_EN_MASK: MUST write them to "1" if want to change corresponding LDO1_EN bit，The LDO1_EN_MASK bits should be clear when LDO1_EN bits have been written.
3	RW	OTP	LDO4_EN LDO4_EN: LDO4 enable in active mode 1, Enable 0, Disable the default value is set by otp reset by power down or RST.
2	RW	OTP	LDO3_EN LDO3_EN: LDO3 enable in active mode 1, Enable 0, Disable the default value is set by otp reset by power down or RST.
1	RW	OTP	LDO2_EN LDO2_EN: LDO2 enable in active mode 1, Enable 0, Disable the default value is set by otp reset by power down or RST.
0	RW	OTP	LDO1_EN LDO1_EN: LDO1 enable in active mode 1, Enable 0, Disable the default value is set by otp reset by power down or RST.

PMIC_POWER_EN2
Address: (0xb3)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	RESV RESV:Reserve
5	RW	0x0	LDO6_EN_MASK LDO6_EN_MASK: MUST write them to "1" if want to change corresponding LDO6_EN bit，The LDO6_EN_MASK bits should be clear when LDO6_EN bits have been written.
4	RW	0x0	LDO5_EN_MASK LDO5_EN_MASK: MUST write them to "1" if want to change corresponding LDO5_EN bit，The LDO5_EN_MASK bits should be clear when LDO5_EN bits have been written.
3:2	RW	OTP	RESV RESV:Reserve
1	RW	OTP	LDO6_EN LDO6_EN: LDO6 enable in active mode 1, Enable 0, Disable the default value is set by otp reset by power down or RST.
0	RW	OTP	LDO5_EN LDO5_EN: LDO5 enable in active mode 1, Enable 0, Disable the default value is set by otp reset by power down or RST.

PMIC_POWER_EN3
Address: (0xb4)

Bit	Attr	Reset Value	Description
7	RW	0x0	SW2_EN_MASK SW2_EN _MASK : MUST write them to "1" if want to change corresponding SW2_EN bit，The SW2_EN_MASK bits should be clear when SW2_EN bits have been written.
6	RW	0x0	SW1_EN_MASK SW1_EN _MASK : MUST write them to "1" if want to change corresponding SW1_EN bit，The SW1_EN_MASK bits should be clear when SW1_EN bits have been written.

Bit	Attr	Reset Value	Description
5	RW	0x0	BUCK5_EN_MASK BUCK5_EN _MASK: MUST write them to "1" if want to change corresponding BUCK5_EN bit，The BUCK5_EN_MASK bits should be clear when BUCK5_EN bits have been written.
4	RW	0x0	LDO9_EN_MASK LDO9_EN_MASK: MUST write them to "1" if want to change corresponding LDO9_EN bit，The LDO9_EN_MASK bits should be clear when LDO9_EN bits have been written.
3	RW	OTP	SW2_EN SW2_EN : SWOUT2 enable in active mode 1, Enable 0, Disable the default value is set by otp. reset by power down or RST.
2	RW	OTP	SW1_EN SW1_EN : SWOUT1 enable in active mode 1, Enable 0, Disable the default value is set by otp. reset by power down or RST.
1	RW	OTP	BUCK5_EN BUCK5_EN : BUCK5 enable in active mode 1, Enable 0, Disable the default value is set by otp. reset by power down or RST.
0	RW	OTP	LDO9_EN LDO9_EN: LDO9 enable in active mode 1, Enable 0, Disable the default value is set by otp. reset by power down or RST.

PMIC_POWER_SLP_EN0
Address: (0xb5)

Bit	Attr	Reset Value	Description
7	RW	OTP	SW2_SLP_EN SW2_SLP_EN : SWOUT2 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp. reset by power down or RST.
6	RW	OTP	SW1_SLP_EN SW1_SLP_EN : SWOUT1 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp. reset by power down or RST.
5	RW	OTP	BUCK5_SLP_EN BUCK5_SLP_EN : BUCK5 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp. reset by power down or RST.
4	RW	OTP	LDO9_SLP_EN LDO9_SLP_EN: LDO9 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp. reset by power down or RST.
3	RW	OTP	BUCK4_SLP_EN Field0000 Abstract BUCK4_SLP_EN: BUCK4 enable in SLEEP mode 1, Enable 0, Disable the default value is set by OTP. reset by power down or RST.
2	RW	OTP	BUCK3_SLP_EN BUCK3_SLP_EN: BUCK3 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp. reset by power down or RST.

Bit	Attr	Reset Value	Description
1	RW	OTP	BUCK2_SLP_EN BUCK2_SLP_EN: BUCK2 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp. reset by power down or RST.
0	RW	OTP	BUCK1_SLP_EN BUCK1_SLP_EN: BUCK1 enable in SLEEP mode 1, Enable 0, Disable the default value is set by OTP. reset by power down or RST.

PMIC_POWER_SLP_EN1
Address: (0xb6)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	RESV RESV:Reserve
5	RW	OTP	LDO6_SLP_EN LDO6_SLP_EN: LDO6 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp reset by power down or RST.
4	RW	OTP	LDO5_SLP_EN LDO5_SLP_EN: LDO5 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp reset by power down or RST.
3	RW	OTP	LDO4_SLP_EN LDO4_SLP_EN: LDO4 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp reset by power down or RST.
2	RW	OTP	LDO3_SLP_EN LDO3_SLP_EN: LDO3 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp reset by power down or RST.

Bit	Attr	Reset Value	Description
1	RW	OTP	LDO2_SLP_EN LDO2_SLP_EN: LDO2 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp reset by power down or RST.
0	RW	OTP	LDO1_SLP_EN LDO1_SLP_EN: LDO1 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp reset by power down or RST.

PMIC_POWER_DISCHRG_EN0
Address: (0xb7)

Bit	Attr	Reset Value	Description
7	RW	0x1	SW2_DISCHG_EN SW2_DISCHG_EN: SWOUT2 discharge enable when the channel is off 0: Disable 1:enable
6	RW	0x1	SW1_DISCHG_EN SW1_DISCHG_EN: SWOUT1 discharge enable when the channel is off 0: Disable 1:enable
5	RW	0x1	BUCK5_DISCHG_EN BUCK5_DISCHG_EN: BUCK5 discharge enable when the channel is off 0: Disable 1:enable
4	RW	0x1	LDO9_DISCHG_EN LDO9_DISCHG_EN: LDO9 discharge enable when the channel is off 0: Disable 1:enable
3	RW	0x1	BUCK4_DISCHG_EN BUCK4_DISCHG_EN: BUCK4 discharge enable when the channel is off 0: Disable 1:enable
2	RW	0x1	BUCK3_DISCHG_EN BUCK3_DISCHG_EN: BUCK3 discharge enable when the channel is off 0: Disable 1:enable
1	RW	0x1	BUCK2_DISCHG_EN BUCK2_DISCHG_EN: BUCK2 discharge enable when the channel is off 0: Disable 1:enable

Bit	Attr	Reset Value	Description
0	RW	0x1	BUCK1_DISCHG_EN BUCK1_DISCHG_EN: BUCK1 discharge enable when the channel is off 0: Disable 1:enable

PMIC_POWER_DISCHRG_EN1
Address: (0xb8)

Bit	Attr	Reset Value	Description
7:6	RW	0x3	RESV RESV:Reserve
5	RW	0x1	LDO6_DISCHG_EN LDO6_DISCHG_EN: LDO6 discharge enable when the channel is off 0: Disable 1:enable:
4	RW	0x1	LDO5_DISCHG_EN LDO5_DISCHG_EN: LDO5 discharge enable when the channel is off 0: Disable 1:enable:
3	RW	0x1	LDO4_DISCHG_EN LDO4_DISCHG_EN: LDO4 discharge enable when the channel is off 0: Disable 1:enable:
2	RW	0x1	LDO3_DISCHG_EN LDO3_DISCHG_EN: LDO3 discharge enable when the channel is off 0: Disable 1:enable:
1	RW	0x1	LDO2_DISCHG_EN LDO2_DISCHG_EN: LDO2 discharge enable when the channel is off 0: Disable 1:enable:
0	RW	0x1	LDO1_DISCHG_EN LDO1_DISCHG_EN: LDO1 discharge enable when the channel is off 0: Disable 1:enable

PMIC_POWER_CONFIG
Address: (0xb9)

Bit	Attr	Reset Value	Description
7	RW	0x0	LDO_SLP_LP_EN LDO_SLP_LP_EN: Low power function enable bit of LDO 0: disable 1:enable

Bit	Attr	Reset Value	Description
6	RW	OTP	BUCK3_FB_RES BUKC3_FB_RES: BUCK3 feedback select 0: select external feedback resistor; 1: select internal feedback resistor
1	RW	0x0	RESE reseve
0	RW	0x0	BUCK_LP_EN BUCK_LP_EN: Low power function enable bit of BUCK 0: disable 1:enable

PMIC_BUCK1_CONFIG
Address: (0xba)

Bit	Attr	Reset Value	Description
7:6	RW	0x1	BUCK1_RATE BUCK1_RATE<1:0>: BUCK1 voltage change rate after DVS 00: 3mV/uS; 01: 6.3mV/uS; 10:12.5mV/uS; 11: 25mV/uS reset by power down or RST.
5:3	RW	0x4	BUCK1_ILPK BUCK1_ILPK<2:0>: BUCK1 peak current limit select, MUST linkage adjustment with the BUCK1_ ILPK <2:0>(write the same code) 000:2A 010:2.25A 010:2.5A 011:2.75A 100:3A 110:3.25A 110:3.5A 111:3.75A reset by power down or RST.
2:0	RW	0x4	BUCK1_ILVL BUCK1_ILVL<2:0>: BUCK1 valley current limit select, linkage adjustment with the BUCK1_ ILVL <2:0>(write the same code) 000:2A 010:2.25A 010:2.5A 011:2.75A 100:3A 101:3.25A 110:3.5A 111:3.75A reset by power down or RST.

PMIC_BUCK1_ON_VSEL
Address: (0xbb)

Bit	Attr	Reset Value	Description
7	RW	0x0	BUCK1_ON_FPWM BUCK1_ON_FPWM: BUCK1 Forced PWM mode selection 1, Forced PWM mode in active mode; 0, PWM/PFM auto change mode reset by power down or RST.

Bit	Attr	Reset Value	Description
6:0	RW	OTP	BUCK1_ON_VSEL BUCK1_ON_VSEL<6:0>: BUCK1 active mode voltage select 0000000:0.5V 0000001:0.5125V 0000010:0.525V ... 1010000:1.5V 1010001:1.6V 1010010:1.7V ... 1011000:2.3V 1011001~1111111:2.4V the default value is set by otp reset by power down or RST.

PMIC_BUCK1_SLP_VSEL
Address: (0xbc)

Bit	Attr	Reset Value	Description
7	RW	0x0	BUCK1_SLP_FPWM BUCK1_SLP_FPWM: 1, Forced PWM mode in sleep mode. 0, PWM/PFM auto change mode. reset by power down or RST.
6:0	RW	OTP	BUCK1_SLP_VSEL BUCK1_SLP_VSEL<6:0>: BUCK1 SLEEP mode voltage select 0000000:0.5V 0000001:0.5125V 0000010:0.525V ... 1010000:1.5V 1010001:1.6V 1010010:1.7V ... 1011000:2.3V 1011001~1111111:2.4V the default value is set byotp reset by power down or RST.

PMIC_BUCK2_CONFIG
Address: (0xbd)

Bit	Attr	Reset Value	Description
7:6	RW	0x1	BUCK2_RATE BUCK2_RATE<1:0>: BUCK2 voltage change rate after DVS 00: 3mV/uS; 01: 6.3mV/uS; 10:12.5mV/uS; 11: 25mV/uS reset by power down or RST.

Bit	Attr	Reset Value	Description
5:3	RW	0x4	BUCK2_ILPK BUCK2_ILPK<2:0>: BUCK2 peak current limit select, MUST linkage adjustment with the BUCK2_ ILPK <2:0>(write the same code) 000:2A 010:2.25A 010:2.5A 011:2.75A 100:3A 101:3.25A 110:3.5A 111:3.75A reset by power down or RST.
2:0	RW	0x4	BUCK2_ILVL BUCK2_ILVL<2:0>: BUCK2 valley current limit select, linkage adjustment with the BUCK2_ ILVL <2:0>(write the same code) 000:2A 010:2.25A 010:2.5A 011:2.75A 100:3A 101:3.25A 110:3.5A 111:3.75A reset by power down or RST.

PMIC_BUCK2_ON_VSEL
Address: (0xbe)

Bit	Attr	Reset Value	Description
7	RW	0x0	BUCK2_ON_FPWM BUCK2_ON_FPWM: BUCK2 Forced PWM mode selection 1, Forced PWM mode in active mode; 0, PWM/PFM auto change mode reset by power down or RST.
6:0	RW	OTP	BUCK2_ON_VSEL BUCK2_ON_VSEL<6:0>: BUCK2 active mode voltage select 0000000:0.5V 0000001:0.5125V 0000010:0.525V ... 1010000:1.5V 1010001:1.6V 1010010:1.7V ... 1011000:2.3V 1011001~1111111:2.4V the default value is set by otp reset by power down or RST.

PMIC_BUCK2_SLP_VSEL
Address: (0xbf)

Bit	Attr	Reset Value	Description
7	RW	0x0	BUCK2_SLP_FPWM BUCK2_SLP_FPWM: 1, Forced PWM mode in sleep mode. 0, PWM/PFM auto change mode. reset by power down or RST.

Bit	Attr	Reset Value	Description
6:0	RW	OTP	BUCK2_SLP_VSEL BUCK2_SLP_VSEL<6:0>: BUCK2 SLEEP mode voltage select 0000000:0.5V 0000001:0.5125V 0000010:0.525V ... 1010000:1.5V 1010001:1.6V 1010010:1.7V ... 1011000:2.3V 1011001~1111111:2.4V the default value is set by otp reset by power down or RST.

PMIC_BUCK3_CONFIG
Address: (0xc0)

Bit	Attr	Reset Value	Description
7:6	RW	0x1	BUCK3_RATE BUCK3_RATE<1:0>: BUCK3 voltage change rate after DVS 00: 3mV/uS; 01: 6.3mV/uS; 10:12.5mV/uS; 11: 25mV/uS reset by power down or RST.
5:3	RW	0x4	BUCK3_ILPK BUCK3_ILPK<2:0>: BUCK3 peak current limit select, MUST linkage adjustment with the BUCK3_ ILPK <2:0>(write the same code) 000:1A 010:1.25A 010:1.5A 011:1.75A 100:2A 101:2.25A 110:2.5A 111:2.75A reset by power down or RST.
2:0	RW	0x4	BUCK3_ILVL BUCK3_ILVL<2:0>: BUCK3 valley current limit select, linkage adjustment with the BUCK3_ ILVL <2:0>(write the same code) 000:1A 010:1.25A 010:1.5A 011:1.75A 100:2A 110:2.25A 110:2.5A 111:2.75A reset by power down or RST.

PMIC_BUCK3_ON_VSEL
Address: (0xc1)

Bit	Attr	Reset Value	Description
7	RW	0x0	BUCK3_ON_FPWM BUCK3_ON_FPWM: BUCK3 Forced PWM mode selection 1, Forced PWM mode in active mode; 0, PWM/PFM auto change mode reset by power down or RST.

Bit	Attr	Reset Value	Description
6:0	RW	OTP	BUCK3_ON_VSEL BUCK3_ON_VSEL<6:0>: BUCK3 active mode voltage select 0000000:0.5V 0000001:0.5125V 0000010:0.525V ... 1010000:1.5V 1010001:1.6V 1010010:1.7V ... 1011000:2.3V 1011001~1111111:2.4V the default value is set by otp reset by power down or RST.

PMIC_BUCK3_SLP_VSEL
Address: (0xc2)

Bit	Attr	Reset Value	Description
7	RW	0x0	BUCK3_SLP_FPWM BUCK3_SLP_FPWM: 1, Forced PWM mode in sleep mode. 0, PWM/PFM auto change mode. reset by power down or RST.
6:0	RW	OTP	BUCK3_SLP_VSEL BUCK3_SLP_VSEL<6:0>: BUCK3 SLEEP mode voltage select 0000000:0.5V 0000001:0.5125V 0000010:0.525V ... 1010000:1.5V 1010001:1.6V 1010010:1.7V ... 1011000:2.3V 1011001~1111111:2.4V the default value is set by otp reset by power down or RST.

PMIC_BUCK4_CONFIG
Address: (0xc3)

Bit	Attr	Reset Value	Description
7:6	RW	0x1	BUCK4_RATE BUCK4_RATE<1:0>: BUCK4 voltage change rate after DVS 00: 3mV/uS; 01: 6.3mV/uS; 10:12.5mV/uS; 11: 25mV/uS reset by power down or RST.

Bit	Attr	Reset Value	Description
5:3	RW	0x4	BUCK4_ILPK BUCK4_ILPK<2:0>: BUCK4 peak current limit select, MUST linkage adjustment with the BUCK4_ ILPK <2:0>(write the same code) 000:1A 010:1.25A 010:1.5A 011:1.75A 100:2A 101:2.25A 110:2.5A 111:2.75A reset by power down or RST.
2:0	RW	0x4	BUCK4_ILVL BUCK4_ILVL<2:0>: BUCK4 valley current limit select, linkage adjustment with the BUCK4_ ILVL <2:0>(write the same code) 000:1A 010:1.25A 010:1.5A 011:1.75A 100:2A 101:2.25A 110:2.5A 111:2.75A reset by power down or RST.

PMIC_BUCK4_ON_VSEL
Address: (0xc4)

Bit	Attr	Reset Value	Description
7	RW	0x0	BUCK4_ON_FPWM BUCK4_ON_FPWM: BUCK4 Forced PWM mode selection 1, Forced PWM mode in active mode; 0, PWM/PFM auto change mode reset by power down or RST.
6:0	RW	OTP	BUCK4_ON_VSEL BUCK4_ON_VSEL<6:0>: BUCK4 active mode voltage select 0000000:0.5V 0000001:0.5125V 0000010:0.525V ... 1010000:1.5V 1010001:1.6V 1010010:1.7V ... 1100011~1111111:3.4V the default value is set by otp reset by power down or RST.

PMIC_BUCK4_SLP_VSEL
Address: (0xc5)

Bit	Attr	Reset Value	Description
7	RW	0x0	BUCK4_SLP_FPWM BUCK4_SLP_FPWM: 1, Forced PWM mode in sleep mode. 0, PWM/PFM auto change mode. reset by power down or RST.

Bit	Attr	Reset Value	Description
6:0	RW	OTP	BUCK4_SLP_VSEL BUCK4_SLP_VSEL<6:0>: BUCK4 SLEEP mode voltage select 0000000:0.5V 0000001:0.5125V 0000010:0.525V ... 1010000:1.5V 1010001:1.6V 1010010:1.7V ... 1100011~1111111:3.4V the default value is set by otp reset by power down or RST.

PMIC_BUCK4_CMIN
Address: (0xc6)

Bit	Attr	Reset Value	Description
7	RW	0x0	SYSUV_DLY_SEL SYSUV_DLY_SEL: Sys under voltage delay time selection 0: 5uS 1:50uS
6	RW	0x0	LDO3_UVSD_EN LDO3_UVSD_EN: SYSUV to shutdown the LDO3 function 0:Disable 1:enable
5	RW	0x0	SYSUV_TRIG_RESETB_EN SYSUV_TRIG_RESETB_EN:SYSUV to trigger restart the PMIC function 0:Disable 1:enable
4	RW	0x0	I2S_RX_MST I2S_RX_MST:I2S RX module 1: master mode 0: slave mode reset by power down or RST.
3	RW	0x0	BUCK4_CMIN_EN BUCK4_CMIN_EN:BUCK4 min Current limit enable 1, Enable 0, Disable reset by power down or RST.
2:1	RW	0x2	BUCK4_CMIN_SEL BUCK4_CMIN_SEL<2:1>：BUCK4 min Current limit select reset by power down or RST. 00:200mA 01:300mA 10:400mA 11:500mA
0	RW	0x0	TON_MAX 0: Typical 7us 1: Typical 3us

PMIC_LDO1_ON_VSEL
Address: (0xcc)

Bit	Attr	Reset Value	Description
7	RW	0x0	LDO1_IMAX LDO1_IMAX:LDO1 current limit setting 0: normal, 1: 130% of nominal value reset by power down or RST.
6:0	RW	OTP	LDO1_ON_VSEL LDO1_ON_VSEL: LDO1 active mode voltage select, 0.6V~3.4V(step=25mV) 0000000:0.6V 0000001:0.625V 0000010:0.65V ... 1110000~1111111:3.4V the default value is set by otp reset by power down or RST.

PMIC_LDO1_SLP_VSEL
Address: (0xcd)

Bit	Attr	Reset Value	Description
7	RW	0x0	RESV RESV:Reserve
6:0	RW	OTP	LDO1_SLP_VSEL LDO1_SLP_VSEL:LDO1 SLEEP mode voltage select, 0.6V~3.4V(step=25mV) 0000000:0.6V 0000001:0.625V 0000010:0.65V ... 1110000~1111111:3.4V the default value is set by otp reset by power down or RST.

PMIC_LDO2_ON_VSEL
Address: (0xce)

Bit	Attr	Reset Value	Description
7	RW	0x0	LDO2_IMAX LDO2_IMAX:LDO2 current limit setting 0: normal, 1: 130% of nominal value reset by power down or RST.
6:0	RW	OTP	LDO2_ON_VSEL LDO2_ON_VSEL: LDO2 active mode voltage select, 0.6V~3.4V(step=25mV) 0000000:0.6V 0000001:0.625V 0000010:0.65V ... 1110000~1111111:3.4V the default value is set by otp reset by power down or RST.

PMIC_LDO2_SLP_VSEL
Address: (0xcf)

Bit	Attr	Reset Value	Description
7	RW	0x0	RESV RESV:Reserve
6:0	RW	OTP	LDO2_SLP_VSEL LDO2_SLP_VSEL:LDO2 SLEEP mode voltage select, 0.6V~3.4V(step=25mV) 0000000:0.6V 0000001:0.625V 0000010:0.65V ... 1110000~1111111:3.4V the default value is set by otp reset by power down or RST.

PMIC_LDO3_ON_VSEL
Address: (0xd0)

Bit	Attr	Reset Value	Description
7	RW	0x0	LDO3_IMAX LDO3_IMAX:LDO3 current limit setting 0: normal, 1: 130% of nominal value reset by power down or RST.
6:0	RW	OTP	LDO3_ON_VSEL LDO3_ON_VSEL: LDO3 active mode voltage select, 0.6V~3.4V(step=25mV) 0000000:0.6V 0000001:0.625V 0000010:0.65V ... 1110000~1111111:3.4V the default value is set by otp reset by power down or RST.

PMIC_LDO3_SLP_VSEL
Address: (0xd1)

Bit	Attr	Reset Value	Description
7	RW	0x0	RESV RESV:Reserve
6:0	RW	OTP	LDO3_SLP_VSEL LDO3_SLP_VSEL:LDO3 SLEEP mode voltage select, 0.6V~3.4V(step=25mV) 0000000:0.6V 0000001:0.625V 0000010:0.65V ... 1110000~1111111:3.4V the default value is set by otp reset by power down or RST.

PMIC_LDO4_ON_VSEL
Address: (0xd2)

Bit	Attr	Reset Value	Description
7	RW	0x0	LDO4_IMAX LDO4_IMAX:LDO4 current limit setting 0: normal, 1: 130% of nominal value reset by power down or RST.
6:0	RW	OTP	LDO4_ON_VSEL LDO4_ON_VSEL: LDO4 active mode voltage select, 0.6V~3.4V(step=25mV) 0000000:0.6V 0000001:0.625V 0000010:0.65V ... 1110000~1111111:3.4V the default value is set by otp reset by power down or RST.

PMIC_LDO4_SLP_VSEL
Address: (0xd3)

Bit	Attr	Reset Value	Description
7	RW	0x0	RESV RESV:Reserve
6:0	RW	OTP	LDO4_SLP_VSEL LDO4_SLP_VSEL:LDO4 SLEEP mode voltage select, 0.6V~3.4V(step=25mV) 0000000:0.6V 0000001:0.625V 0000010:0.65V ... 1110000~1111111:3.4V the default value is set by otp reset by power down or RST.

PMIC_LDO5_ON_VSEL
Address: (0xd4)

Bit	Attr	Reset Value	Description
7	RW	0x0	LDO5_IMAX LDO5_IMAX:LDO5current limit setting 0: normal, 1: 130% of nominal value reset by power down or RST.

Bit	Attr	Reset Value	Description
6:0	RW	OTP	LDO5_ON_VSEL LDO5_ON_VSEL: LDO5 active mode voltage select, 0.6V~3.4V(step=25mV) 0000000:0.6V 0000001:0.625V 0000010:0.65V ... 1110000~1111111:3.4V the default value is set by otp reset by power down or RST.

PMIC_LDO5_SLP_VSEL
Address: (0xd5)

Bit	Attr	Reset Value	Description
7	RW	0x0	RESV RESV:Reserve
6:0	RW	OTP	LDO5_SLP_VSEL LDO5_SLP_VSEL:LDO5 SLEEP mode voltage select, 0.6V~3.4V(step=25mV) 0000000:0.6V 0000001:0.625V 0000010:0.65V ... 1110000~1111111:3.4V the default value is set by otp reset by power down or RST.

PMIC_LDO6_ON_VSEL
Address: (0xd6)

Bit	Attr	Reset Value	Description
7	RW	0x0	LDO6_IMAX LDO6_IMAX:LDO6 current limit setting 0: normal, 1: 130% of nominal value reset by power down or RST.
6:0	RW	OTP	LDO6_ON_VSEL LDO6_ON_VSEL: LDO6 active mode voltage select, 0.6V~3.4V(step=25mV) 0000000:0.6V 0000001:0.625V 0000010:0.65V ... 1110000~1111111:3.4V the default value is set by otp reset by power down or RST.

PMIC_LDO6_SLP_VSEL
Address: (0xd7)

Bit	Attr	Reset Value	Description
7	RW	0x0	RESV RESV:Reserve
6:0	RW	OTP	LDO6_SLP_VSEL LDO6_SLP_VSEL:LDO6 SLEEP mode voltage select, 0.6V~3.4V(step=25mV) 0000000:0.6V 0000001:0.625V 0000010:0.65V ... 1110000~1111111:3.4V the default value is set by otp reset by power down or RST.

PMIC_LDO9_ON_VSEL
Address: (0xdc)

Bit	Attr	Reset Value	Description
7	RW	0x0	LDO9_IMAX LDO9_IMAX:LDO9 current limit setting 0: normal, 1: 130% of nominal value reset by power down or RST.
6:0	RW	OTP	LDO9_ON_VSEL LDO9_ON_VSEL: LDO9 active mode voltage select, 0.6V~3.4V(step=25mV) 0000000:0.6V 0000001:0.625V 0000010:0.65V ... 1110000~1111111:3.4V the default value is set by otp reset by power down or RST.

PMIC_LDO9_SLP_VSEL
Address: (0xdd)

Bit	Attr	Reset Value	Description
7	RW	0x0	RESV RESV:Reserve

Bit	Attr	Reset Value	Description
6:0	RW	OTP	LDO9_SLP_VSEL LDO9_SLP_VSEL:LDO9 SLEEP mode voltage select, 0.6V~3.4V(step=25mV) 0000000:0.6V 0000001:0.625V 0000010:0.65V ... 1110000~1111111:3.4V the default value is set by otp reset by power down or RST.

PMIC_BUCK5_SW1_CONFIG0
Address: (0xde)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	SW1_ILIM SW1_ILIM: SWOUT1 current limit selection 00: 1A 01:1.5A 10:1.8A 11: 2.1A reset by power down or RST.
5	RW	0x0	RESV Reserved
4:3	RW	0x1	BUCK5_ILMAX BUCK5_ILMAX:BUCK5 inductor peak current setting 00:2.5A 01:3A 10:4A 11:4.5A reset by power down or RST.
2:0	RW	OTP	BUCK5_ON_VSEL BUCK5_ON_VSEL:BUCK5 active mode voltage select. 000: 1.5V; 001: 1.8V; 010: 2.0V; 011: 2.2V 100: 2.8V; 101: 3.0V; 110: 3.3V; 111: 3.6V the default value is set by otp reset by power down or RST.

PMIC_BUCK5_CONFIG1
Address: (0xdf)

Bit	Attr	Reset Value	Description
7:6	RW	0x1	RESV Reserved
5:3	RW	0x2	SW2_ILIM SW2_ILIM<2:0>: SWOUT2 current limit select 000: 1A 001:1.5A 010:1.8A 011: 2.1A 1xx: 2.1A

Bit	Attr	Reset Value	Description
2:0	RW	OTP	BUCK5_SLP_VSEL BUCK5_SLP_VSEL:BUCK5 SLEEP mode voltage select. 000: 1.5V; 001: 1.8V; 010: 2.0V; 011: 2.2V 100: 2.8V; 101: 3.0V; 110: 3.3V; 111: 3.6V the default value is set by otp reset by power down or RST.

PMIC_CHIP_NAME
Address: (0xed)

Bit	Attr	Reset Value	Description
7:0	RO	0x80	CHIP_NAME CHIP_NAME:CHIP name code<11:4>.default 80

PMIC_CHIP_VER
Address: (0xee)

Bit	Attr	Reset Value	Description
7:4	RO	0x9	CHIP_NAME CHIP_NAME:CHIP name code<3:0>.default 9
3:0	RO	0x2	RESV RESV: Reserve

PMIC_OTP_VER
Address: (0xef)

Bit	Attr	Reset Value	Description
7:4	RW	0x0	RESV RESV: Reserve
3:0	RO	OTP	OTP_VER OTP_VER: OTP revize version. default OTP.

PMIC_SYS_STS
Address: (0xf0)

Bit	Attr	Reset Value	Description
7	RO	0x0	PWRON_STS PWRON_STS: PWRON key status 1: PWRON not press 0:PWRON button pressed reset by power down or RST

Bit	Attr	Reset Value	Description
6	RO	0x0	PLUG_IN_STS PLUG_IN_STS: USB plug-in event occurs(VDC>0.55V) 0: no USB plug in 1: USB plugged in
5	RO	0x0	VCC9_UV_STS VCC9_UV_STS: VCC9 under voltage lockout status
4	RO	0x0	VCC9_LO_STS VCC9_LO_STS: VCC9 low voltage status 0: VCC9>VB_LO_SEL 1: VCC9<VB_LO_SEL
3	RO	0x0	HOTDIE_STS HOTDIE_STS: Hot-die warning
2	RO	0x0	TSD_STS TSD_STS: Thermal shut down
1	RO	0x0	RESV RESV: Reserve
0	RO	0x0	VCC9_OV_STS VCC9_OV_STS: VCC9 over voltage status bit

PMIC_SYS_CFG0
Address: (0xf1)

Bit	Attr	Reset Value	Description
7	RW	0x1	RESV RESV: Reserve
6:4	RW	0x0	VCC9_UV_SEL VCC9_UV_SEL:VCC9 shut down voltage select, 2.7V~3.4V, step=100mV 000:2.7V; 001:2.8V; 010:2.9V; 011:3.0V 100:3.1V; 101:3.2V; 110:3.3V; 111:3.4V reset by power down or RST
3	RW	0x1	VCC9_LO_ACT VCC9_LO_ACT: VCC9 low voltage action 0: shut down system 1: insert interrupt reset by power down or RST
2:0	RW	0x4	VCC9_LO_SEL VCC9_LO_SEL: VCC9 low voltage threshold,2.8V~3.5V, step=100mV 000:2.8V; 001:2.9V; 010:3.0V; 011:3.1V 100:3.2V; 101:3.3V; 110:3.4V; 111:3.5V reset by power down or RST

PMIC_SYS_CFG1
Address: (0xf2)

Bit	Attr	Reset Value	Description
7	RW	0x1	CLK32KOUT_EN CLK32KOUT_EN: CLK32K output is enable 1. enable 0. disable reset by power down or RST
6	RW	0x0	TSD_TEMP TSD_TEMP: Thermal shutdown temperature threshold 0: 140℃; 1: 160℃ reset by power down or RST
5:4	RW	0x0	HOTDIE_TEMP HOTDIE_TEMP: Hot-die temperature threshold 00:85℃ 01:95℃ 10:105℃ 11:115℃ reset by power down or RST
3	RW	0x0	VCC9_OV_SD_EN VCC9_OV_SD_EN: Shut down the BUCK1~5 mosfet if the VCC9 OV happens 0:Disable 1:Enable
2	RW	0x0	VCC9_OV_SD_TIME VCC9_OV_SD_TIME: VCC9 OV comparator delay time selection 0: 8uS 1:30uS
1	RW	0x0	RESV RESV: Reserve
0	RW	0x0	RESV RESV: Reserve

PMIC_SYS_CFG2
Address: (0xf3)

Bit	Attr	Reset Value	Description
7	RW	0x0	ADC_PHASE ADC_PHASE: ADC phase select 0: normal 1: reverse
6	RW	0x1	BUCK5_CLK_SEL BUCK5_CLK_SEL: BUCK5 clock select 0:1Meg 1:2Meg
5:2	RW	0x0	RESV RESV: Reserve
1	RW	0x0	VCC9_UV_PRE_DLY VCC9_UV_PRE_DLY: VCC9 under voltage delay time select 0:1.5uS 1:5uS
0	RW	0x0	RESV RESV: Reserve

PMIC_SYS_CFG3
Address: (0xf4)

Note: Do not operate the F4 register consecutively, two operations on the F4 register must include at least one register read between operations, and delay 2ms.

Bit	Attr	Reset Value	Description
7:6	RW	0x0	RST_FUN: reset function selection: 00: Restart the PMU. 01: reset DCDC and LDO. (Do not use this mode when SLEEP.) 1x: Do not use.
5	RW	0x1	SLP_POL SLP_POL: SLEEP pin polarity 0:active low 1:active high reset by power down or RST
4:3	RW	0x0	SLP_FUN SLP_FUN: SLEEP PIN function selection: 00: not effect; 01: sleep function; 10:shutdown function; 11:restart pmu function. reset by power down or RST
2	RW	0x0	DEV_RST DEV_RST: Write 1 will 'RST' the device. Note: 'RST' is not only a reset source, but a special function defined by 'RST_FUN' reset by power down or RST
1	RW	0x0	DEV_SLP DEV_SLP: Write 1 will go to SLEEP state. reset by power down or RST
0	RW	0x0	DEV_OFF DEV_OFF: Write 1 will shutdown the device. reset by power down or RST

PMIC_ON_SOURCE
Address: (0xf5)

Bit	Attr	Reset Value	Description
7	RO	0x0	ON_PWRON ON_PWRON: PRESS PWRON to turn on PMU reset by power down or RST, and load this bit after reset.
6	RO	0x0	ON_PLUG_IN ON_PLUG_IN:USB PLUG IN to turn on PMU
5	RO	0x0	ON_RTC ON_RTC:RTC timer to turn on PMU
4	RO	0x0	RESTART_RESETB RESTART_RESETB:PULL LOW the RESETB PIN to restart the PMU
3	RO	0x0	RESTART_PWRON_LP RESTART_PWRON_LP:Long press PWRON to restart the PMU
2	RO	0x0	RESTART_SLP RESTART_SLP:SLEEP PIN ACTIVE to restart the PMU reset by power down or RST

Bit	Attr	Reset Value	Description
1	RW	0x0	RESTART_DEV_RST RESTART_DEV_RST: I2C write DEV_RST to restart PMU
0	RO	0x0	WDT_CLR WDT_CLR:To reset the watchdog timer resets and starts counting again

PMIC_OFF_SOURCE
Address: (0xf6)

Bit	Attr	Reset Value	Description
7	RO	0x0	OFF_SLP OFF_SLP: SLEEP PIN ACTIVE to turn off PMU reset by power down or RST, and load this bit after reset.
6	RO	0x0	OFF_VCC9_OV OFF_VCC9_OV:VCC9 OV to turn off PMU reset by power down or RST, and load this bit after reset.
5	RO	0x0	OFF_TSD OFF_TSD:TSD to turn off PMU reset by power down or RST, and load this bit after reset.
4	RO	0x0	OFF_VCC9_UV OFF_VCC9_UV: VCC9 UV to turn off PMU reset by power down or RST, and load this bit after reset.
3	RO	0x0	OFF_DEV_OFF OFF_DEV_OFF:I2C write DEV_OFF to turn off PMU reset by power down or RST, and load this bit after reset.
2	RO	0x0	OFF_PWRON_LP OFF_PWRON_LP: long press PWRON to turn off PMU reset by power down or RST, and load this bit after reset.
1	RO	0x0	OFF_WDT OFF_WDT: Watch dog to turn off PMU reset by power down or RST, and load this bit after reset.
0	RO	0x0	OFF_VCC9_LO OFF_VCC9_LO:VCC9 Low (if VCC9_LO_ACT=0)to turn off PMU reset by power down or RST, and load this bit after reset.

PMIC_PWRON_KEY
Address: (0xf7)

Bit	Attr	Reset Value	Description
7	RW	OTP	PWRON_ON_TIME PWRON_ON_TIME:0:500mS; 1:100mS default OTP.
6	RW	0x0	PWRON_LP_ACT PWRON_LP_ACT: PWRON long press act 0: turn off 1: turn off and then restart
5:4	RW	0x0	PWRON_LP_OFF_TIME PWRON_LP_OFF_TIME: PWRON long press time: 00: 6s, 01: 8s, 10: 10s, 11: 12s
3:2	RW	0x1	PWRON_LP_TM PWRON_LP_TM_SEL<1:0>:PWRON long press interrupt time selection: 00: 0.5S 01:1S 10:1.5S 11:2S
1:0	RW	0x2	PWRON_DB_SEL PWRON_DB_SEL<1:0>:PWRON interrupt debounce time selection: 00: 32uS 01:10mS 10:20mS 11:40mS

PMIC_INT_STS0
Address: (0xf8)

Bit	Attr	Reset Value	Description
7	W1C	0x0	VCC9_LO_INT VCC9_LO_INT: VCC9 under voltage alarm event interrupt status. reset by power down or RST.
6	W1C	0x0	RTC_PERIOD_INT RTC_PERIOD_INT: RTC period event interrupt. reset by power down or RST.
5	W1C	0x0	RTC_ALARM_INT RTC_ALARM_INT: RTC alarm event interrupt. reset by power down or RST.
4	W1C	0x0	HOTDIE_INT HOTDIE_INT: Hot die event interrupt status. reset by power down or RST.
3	W1C	0x0	PWRON_LP_INT PWRON_LP_INT: PWRON PIN long press event interrupt status. reset by power down or RST.
2	W1C	0x0	PWRON_INT PWRON_INT: PWRON event interrupt status. reset by power down or RST.
1	W1C	0x0	PWRON_RISE_INT PWRON_RISE_INT:PWRON rising event interrupt reset by power down or RST.
0	W1C	0x0	PWRON_FALL_INT PWRON_FALL_INT:PWRON falling event interrupt reset by power down or RST.

PMIC_INT_MSK0
Address: (0xf9)

Bit	Attr	Reset Value	Description
7	RW	0x0	VB_LO_IM VB_LO_IM: Battery under voltage alarm event interrupt mask reset by power down or RST.
6	RW	0x0	RTC_PERIOD_IM RTC_PERIOD_IM: RTC period event interrupt mask reset by power down or RST.
5	RW	0x0	RTC_ALARM_IM RTC_ALARM_IM: RTC alarm event interrupt mask reset by power down or RST.
4	RW	0x0	HOTDIE_IM HOTDIE_IM: Hot die event interrupt mask reset by power down or RST.
3	RW	0x0	PWRON_LP_IM PWRON_LP_IM: PWRON PIN long press event interrupt mask reset by power down or RST.
2	RW	0x0	PWRON_IM PWRON_IM:PWRON event interrupt mask reset by power down or RST.
1	RW	0x0	PWRON_RISE_INT_IM PWRON_RISE_INT_IM:PWRON rising event interrupt mask reset by power down or RST.
0	RW	0x0	PWRON_FALL_INT_IM PWRON_FALL_INT_IM:PWRON falling event interrupt mask reset by power down or RST.

PMIC_INT_STS1
Address: (0xfa)

Bit	Attr	Reset Value	Description
7:2	W1C	0x0	RESV RESV: Reserve
1	W1C	0x0	PLUG_OUT_INT PLUG_OUT_INT: USB plug out event interrupt reset by power down or RST.
0	W1C	0x0	PLUG_IN_INT PLUG_IN_INT: USB plug in event interrupt reset by power down or RST.

PMIC_INT_MSK1
Address: (0xfb)

Bit	Attr	Reset Value	Description
7:2	RW	0x0	RESV RESV: Reserve
1	RW	0x0	PLUG_OUT_INT_IM PLUG_OUT_INT_IM: USB plug out event interrupt mask reset by power down or RST.
0	RW	0x0	PLUG_IN_INT_IM PLUG_IN_INT_IM: USB plug in event interrupt mask reset by power down or RST.

PMIC_INT_STS2
Address: (0xfc)

Bit	Attr	Reset Value	Description
7:6	RC	0x0	RESV RESV: Reserve
5	W1C	0x0	CLASSD_OCP_INT CLASSD_OCP_INT:CLASS D OCP interrupt. reset by power down or RST.
4	W1C	0x0	CLASSD_MUTE_DONE CLASSD_MUTE_DONE_INT:CLASSD_MUTE_DONE interrupt. reset by power down or RST.
3:0	W1C	0x0	RESV RESV: Reserve

PMIC_INT_MSK2
Address: (0xfd)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	RESV RESV: Reserve
5	RW	0x0	CLASSD_OCP_INT_IM CLASSD_OCP_INT_IM:CLASS D OCP interrupt mask. reset by power down or RST.
4	RW	0x0	CLASSD_MUTE_DONE_IM CLASSD_MUTE_DONE_IM:CLASSD_MUTE_DONE interrupt mask. reset by power down or RST.
3:0	RW	0x0	RESV RESV: Reserve

PMIC_GPIO_INT_CONFIG
Address: (0xfe)

Bit	Attr	Reset Value	Description
7:2	RW	0x0	RESV RESV: Reserve

Bit	Attr	Reset Value	Description
1	RW	0x1	INT_POL INT_POL: INT pin polarity 0: active low 1: active high reset by power down or RST.
0	RW	0x0	INT_FC_EN INT_FC_EN: interrupt watchdog function enable 0:disable 1:enable reset by power down or RST.

POWER_CONFIG2
Address:(0x67)

Bit	Attr	Reset Value	Description
7	RW	0x0	CICCOMP_CF CICCOMP_CF:Gain reduction 0:1 1:6/8
6	RW	0x0	ADCL_PHASE_INV_CTRL ADCL_PHASE_INV_CTRL:Perform an inverse phase processing on the data
5	RW	0x0	MIC_GAIN_SEL MIC_GAIN_SEL: attenuate 2.5 dB for the MIC, and increase the digital filter by 2.5 dB.
4	RW	0x0	CHOP_VGA_EN CHOP_VGA_EN:vag buffer of mic and pga chop enable 0:disable 1；enable
3	RW	0x0	BOOST_MIC_PGA BOOST_MIC_PGA:mic and pga current increase to 150% 0:100%(default) 1:150%
2	RW	0x0	HPCP_RLOADCTRL_EN HPCP_RLOADCTRL_EN: 0:0uA 1:30uA
1	RW	0x0	RESV RESV: Reserve
0	RW	OTP	CIC_COMP_ENA CIC_COMP_ENA:CIC compensation filter 0:disable 1:enable

CODEC_CONFIG
Address:(0x8C)

Bit	Attr	Reset Value	Description
7	RW	0x0	DAC_MODATCF DAC_MODATCF:Control the attenuation coefficient of the modulator input 0:1 1:0.9
6	RW	0x0	DAC_HB1ATCF DAC_HB1ATCF:Control the attenuation coefficient of the HB1 0:1 1:0.9
5:4	RW	0x0	HP_CHOP_SEL[1:0] HP_CHOP_SEL[1:0]:
3	RW	0x0	DAC_HP_HPF DAC_HP_HPF:The Qualcomm filter enable control bit in the headphone mode (valid when CLASS_D_MODE = 0) 0：disable HPF for ClassD 1：enable HPF for ClassD
2：1	RW	0x0	DAC_BSTLDO_SEL DAC_BSTLDO_SEL: 00：2.1V(default) 01：1.92V 10：1.76V 11：1.6V
0	RW	0x0	FW_SEL FW_SEL: 0：AP selects the old version of the software configuration 1：AP selects the new version of the software configuration

PLDO_HRDEC_EN
Address:(0x8A)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	RESV RESV:Reserve
5	RW	0x0	LDO6_HRDEC_EN LDO6_HRDEC_EN:reduce the light load of LDO6 when VCC6-LDO6≤50mV and the voltage of LDO6≥2.2V 0:enable 1:disable
4	RW	0x0	LDO5_HRDEC_EN LDO5_HRDEC_EN:reduce the light load of LDO5 when VCC6-LDO5≤50mV and the voltage of LDO5≥2.2V 0:enable 1:disable

Bit	Attr	Reset Value	Description
3	RW	0x0	LDO4_HRDEC_EN LDO4_HRDEC_EN:reduce the light load of LDO4 when VCC6-LDO4≤50mV and the voltage of LDO4≥2.2V 0:enable 1:disable
2	RW	0x0	LDO3_HRDEC_EN LDO3_HRDEC_EN:reduce the light load of LDO3 when VCC5-LDO3≤50mV and the voltage of LDO3≥2.2V 0:enable 1:disable
1	RW	0x0	LDO2_HRDEC_EN LDO2_HRDEC_EN:reduce the light load of LDO2 when VCC5-LDO2≤50mV and the voltage of LDO2≥2.2V 0:enable 1:disable
0	RW	0x0	LDO1_HRDEC_EN LDO1_HRDEC_EN:reduce the light load of LDO1 when VCC5-LDO1≤50mV and the voltage of LDO1≥2.2V 0:enable 1:disable

CHRG_CONFIG0
Address:(0xCB)

Bit	Attr	Reset Value	Description
7:5	RW	0x0	RESV RESV: Reserve
4	RW	0x0	LDO9_HRDEC_EN LDO9_HRDEC_EN:reduce the light load of LDO9 when VCC7-LDO9≤50mV and the voltage of LDO9≥2.2V 0:enable 1:disable
3:0	RW	0x0	RESV RESV: Reserve

SYS_CFG4
Address:(0x66)

Bit	Attr	Reset Value	Description
7	RW	0x0	RESV RESV: Reserve
6	RW	0x0	DEEP_SLP_CTRL DEEP_SLP_CTRL:ultra-low-power 0:enable 1:disable
5	RW	OTP	CLK_32K_ENB CLK_32K_ENB:CLK_32K 0:enable 1:disable
4	RW	0x0	INT_FUNCTION INT_FUNCTION: 0:Interrupt only 1:Interrupt and exit SLEEP mode
3	RW	0x0	SLP_FUN_WORK SLP_FUN_WORK: The SLP_FUN reture default after exit SLEEP
2	RW	0x0	EXIT_SLP_INT EXIT_SLP_INT:Interrupt after the sequence of enter/exit and EXIT_SLP_DELAY delay is completed
1	RW	0x0	RESV RESV: Reserve
0	RW	OTP	VDC_POWERON VDC_POWERON : VDC turn on PMU 0:edge-triggered 1:level triggered

SYS_CFG5
Address:(0x68)

Bit	Attr	Reset Value	Description
7	RW	0x0	RESV RESV: Reserve
6	RW	0x0	VLDO_3P3_SEL VLDO_3P3_SEL :0:3.3V 1:3.5V
5	RW	0x0	CPCLK_SEL CPCLK_SEL : cp clk_frequency selection 0:500k 1:1M
4:3	RW	0x0	RESV RESV: Reserve
2	RW	0x0	VLDO_SEL VLDO_SEL : internal LDO voltage option 00:2.85V(default) 01:2.8V 10:3V 11:2.95V

Bit	Attr	Reset Value	Description
1	RW	0x0	SYS_OVP_SEL SYS_OVP_SEL : system ovp threshold value 0:6V 1:5.5V

SYS_CFG6
Address:(0x69)

Bit	Attr	Reset Value	Description
7	RW	0x0	RESV RESV: Reserve
6	RW	0x0	SYSOV_LOCKENB SYSOV_LOCKENB:SYS OV latch 0:enable 1:disable
5	RW	0x0	LDOA_LOCK_ENB LDOA_LOCK_ENB:LDOA UV latch 0:enable 1:disable
4	RW	0x0	CMIN_FUN_SEL CMIN_FUN_SEL: CMIN function for BUCK4 0：MAXON control 1：LCCMP control
3	RW	0x0	RESV RESV: Reserve
2:0	RW	0x0	POWERON_TIME_ADD POWERON_TIME_ADD： 000:0S；001：20ms；010:100ms， 011:500ms；100:1000ms；101:1500ms， 110:2000ms；111：3000ms

SYS_CFG7_OFF_SOURCE2
Address:(0x6A)

Bit	Attr	Reset Value	Description
7	RW	OTP	PWRON_ON_TIME_H PWRON_ON_TIME_H:if this bit was set 1,then Reg0xF7<7> :PWRON_ON_TIME 0:20mS 1:40mS
6	RW	0x0	VBLO_DB VBLO_DB：0：2mS 1: 2 32k clocks
5	RW	0x0	VBLO_OPT VBLO_OPT:The vaule of VBLO is 4.5V,if this bit is set 1
4:3	RW	0x0	EXIT_SLP_DELAY EXIT_SLP_DELAY:The delay time after completing the SLEEP sequence 00 0ms 01 10ms 10:20ms 11:50ms
2	RO	0x0	RESTART_WDT RESTART_WDT: Watchdog event to restart PMU

Bit	Attr	Reset Value	Description
1	RO	0x0	OFF_VLDOA_UV OFF_VLDOA_UV: VLDOA UV to turn off PMU
0	RO	0x0	OFF_VCCA_UV OFF_VCCA_UV:VCCA UV to turn off PMU

INT_STS3
Address:(0x64)

Bit	Attr	Reset Value	Description
7:2	RW	0x0	
1	R0	0x0	RST_STS RST_STS: RST_FUN=01/10 and restart event occurred,reset by power down
0	RW	0x0	RESV RESV: Reserve

INT_MASK3
Address:(0x65)

Bit	Attr	Reset Value	Description
7	RW	0x0	RESV RESV: Reserve
6	RW	0x0	USBOV_5P6V_OPT USBOV_5P6V_OPT: USB ovp threshold value 0:6.0V 1:5.3V
5	RW	0x0	WDT_ACT WDT_ACT: Watchdog function settings 0:shut down system 1: reset system
4	RW	0x0	WDT_EN WDT_EN: Watchdog function 0:disable 1:enable
3	RW	0x0	WDT_SET WDT_SET:Watchdog timer settings 000：50ms；001：100ms；010：500ms； 011：1S；100：2S；101：10s；110：1min； 111：10min；
0	RW	0x1	RESV RESV: Reserve

Note: 7bits I2C address is 0x22 all of follow registers
POWER_EXIT_SLP_SEQ0
Address: (0X60)

Bit	Attr	Reset Value	Description
7:4	RW	0x0	BUCK2_EXIT_SLP_SEQ BUCK2_EXIT_SLP_SEQ:BUCK2 exit SLEEP sequence ,2mS/step default，1mS/step and 4mS/step option by efuse
3:0	RW	0x0	BUCK1_EXIT_SLP_SEQ BUCK1_EXIT_SLP_SEQ:BUCK1 exit SLEEP sequence ,2mS/step default，1mS/step and 4mS/step option by efuse

POWER_EXIT_SLP_SEQ1
Address: (0X61)

Bit	Attr	Reset Value	Description
7:4	RW	0x0	BUCK4_EXIT_SLP_SEQ BUCK4_EXIT_SLP_SEQ:BUCK4 exit SLEEP sequence ,2mS/step default，1mS/step and 4mS/step option by efuse
3:0	RW	0x0	BUCK3_EXIT_SLP_SEQ BUCK3_EXIT_SLP_SEQ:BUCK3 exit SLEEP sequence ,2mS/step default，1mS/step and 4mS/step option by efuse

POWER_EXIT_SLP_SEQ2
Address: (0X62)

Bit	Attr	Reset Value	Description
7:4	RW	0x0	LDO2_EXIT_SLP_SEQ LDO2_EXIT_SLP_SEQ:LDO2 exit SLEEP sequence ,2mS/step default，1mS/step and 4mS/step option by efuse
3:0	RW	0x0	LDO1_EXIT_SLP_SEQ LDO1_EXIT_SLP_SEQ:LDO1 exit SLEEP sequence ,2mS/step default，1mS/step and 4mS/step option by efuse

POWER_EXIT_SLP_SEQ3
Address: (0X63)

Bit	Attr	Reset Value	Description
7:4	RW	0x0	LDO4_EXIT_SLP_SEQ LDO4_EXIT_SLP_SEQ:LDO4 exit SLEEP sequence ,2mS/step default，1mS/step and 4mS/step option by efuse
3:0	RW	0x0	LDO3_EXIT_SLP_SEQ LDO3_EXIT_SLP_SEQ:LDO3 exit SLEEP sequence ,2mS/step default，1mS/step and 4mS/step option by efuse

POWER_EXIT_SLP_SEQ4
Address: (0X64)

Bit	Attr	Reset Value	Description
7:4	RW	0x0	LDO6_EXIT_SLP_SEQ LDO6_EXIT_SLP_SEQ:LDO6 exit SLEEP sequence ,2mS/step default，1mS/step and 4mS/step option by efuse
3:0	RW	0x0	LDO5_EXIT_SLP_SEQ LDO5_EXIT_SLP_SEQ:LDO5 exit SLEEP sequence ,2mS/step default，1mS/step and 4mS/step option by efuse

POWER_EXIT_SLP_SEQ6
Address: (0X66)

Bit	Attr	Reset Value	Description
7:4	RW	0x0	SW1_EXIT_SLP_SEQ SW1_EXIT_SLP_SEQ:SW1 exit SLEEP sequence ,2mS/step default，1mS/step and 4mS/step option by efuse
3:0	RW	0x0	LDO9_EXIT_SLP_SEQ LDO9_EXIT_SLP_SEQ:LDO9 exit SLEEP sequence ,2mS/step default，1mS/step and 4mS/step option by efuse

POWER_EXIT_SLP_SEQ7
Address: (0X67)

Bit	Attr	Reset Value	Description
7:4	RW	0x0	BUCK5_EXIT_SLP_SEQ BUCK5_EXIT_SLP_SEQ:BUCK5 exit SLEEP sequence ,2mS/step default，1mS/step and 4mS/step option by efuse
3:0	RW	0x0	SW2_EXIT_SLP_SEQ SW2_EXIT_SLP_SEQ:SW2 exit SLEEP sequence ,2mS/step default，1mS/step and 4mS/step option by efuse

POWER_ENTER_SLP_SD_SEQ0
Address: (0X68)

Bit	Attr	Reset Value	Description
7:4	RW	0x0	BUCK2_SLP_SD_SEQ BUCK2_SLP_SD_SEQ:BUCK2 enter SLEEP or set down sequence ,2mS/step default，1mS/step and 4mS/step option by efuse
3:0	RW	0x0	BUCK1_SLP_SD_SEQ BUCK1_SLP_SD_SEQ:BUCK1 enter SLEEP or set down sequence ,2mS/step default，1mS/step and 4mS/step option by efuse

POWER_ENTER_SLP_SD_SEQ1
Address: (0X69)

Bit	Attr	Reset Value	Description
7:4	RW	0x0	BUCK4_SLP_SD_SEQ BUCK4_SLP_SD_SEQ:BUCK4 enter SLEEP or set down sequence ,2mS/step default，1mS/step and 4mS/step option by efuse
3:0	RW	0x0	BUCK3_SLP_SD_SEQ BUCK3_SLP_SD_SEQ:BUCK3 enter SLEEP or set down sequence ,2mS/step default，1mS/step and 4mS/step option by efuse

POWER_ENTER_SLP_SD_SEQ2
Address: (0X6A)

Bit	Attr	Reset Value	Description
7:4	RW	0x0	BUCK2_SLP_SD_SEQ BUCK2_SLP_SD_SEQ:BUCK2 enter SLEEP or set down sequence ,2mS/step default，1mS/step and 4mS/step option by efuse
3:0	RW	0x0	BUCK1_SLP_SD_SEQ BUCK1_SLP_SD_SEQ:BUCK1 enter SLEEP or set down sequence ,2mS/step default，1mS/step and 4mS/step option by efuse

POWER_ENTER_SLP_SD_SEQ3
Address: (0X6B)

Bit	Attr	Reset Value	Description
7:4	RW	0x0	LDO2_SLP_SD_SEQ LDO2_SLP_SD_SEQ:LDO2 enter SLEEP or set down sequence ,2mS/step default, 1mS/step and 4mS/step option by efuse
3:0	RW	0x0	LDO1_SLP_SD_SEQ LDO1_SLP_SD_SEQ:LDO1 enter SLEEP or set down sequence ,2mS/step default，1mS/step and 4mS/step option by efuse

POWER_ENTER_SLP_SD_SEQ4
Address: (0X6C)

Bit	Attr	Reset Value	Description
7:4	RW	0x0	LDO4_SLP_SD_SEQ LDO4_SLP_SD_SEQ:LDO4 enter SLEEP or set down sequence ,2mS/step default, 1mS/step and 4mS/step option by efuse
3:0	RW	0x0	LDO3_SLP_SD_SEQ LDO3_SLP_SD_SEQ:LDO3 enter SLEEP or set down sequence ,2mS/step default，1mS/step and 4mS/step option by efuse

POWER_ENTER_SLP_SD_SEQ5
Address: (0X6D)

Bit	Attr	Reset Value	Description
7:4	RW	0x0	LDO6_SLP_SD_SEQ LDO6_SLP_SD_SEQ:LDO6 enter SLEEP or set down sequence ,2mS/step default, 1mS/step and 4mS/step option by efuse
3:0	RW	0x0	LDO5_SLP_SD_SEQ LDO5_SLP_SD_SEQ:LDO5 enter SLEEP or set down sequence ,2mS/step default，1mS/step and 4mS/step option by efuse

POWER_ENTER_SLP_SD_SEQ7
Address: (0X6F)

Bit	Attr	Reset Value	Description
7:4	RW	0x0	BUCK5_SLP_SD_SEQ BUCK5_SLP_SD_SEQ:BUCK5 enter SLEEP or set down sequence ,2mS/step default，1mS/step and 4mS/step option by efuse
3:0	RW	0x0	SW2_SLP_SD_SEQ SW2_SLP_SD_SEQ:SW2 enter SLEEP or set down sequence ,2mS/step default，1mS/step and 4mS/step option by efuse

DEVICE_ID
Address: (0x00)

Bit	Attr	Reset Value	Description
7:4	RW	OTP	VERSION_ID VERSION_ID:Version ID
3:0	RW	OTP	REVERSION_ID REVERSION_ID: PD ID

INT_STS
Address: (0x01)

Bit	Attr	Reset Value	Description
7	RW	0x0	VSAFE0V_INT VSAFE0V_INT:USB Voltage under 0.8V event interrupt.
6	RW	0x0	CC_OV_STS_INT CC_OV_STS_INT: CC OV event interrupt.
5	RW	0x0	TX_SOP_SUC_INT TX_SOP_SUC_INT:The data packet was sent successfully and "goodcrc " was received event interrupt.
4	RW	0x0	TX_SOP_FAIL_INT TX_SOP_FAIL_INT: send SOP Fail event interrupt.
3	RW	0x0	RX_HARD_RST_INT RX_HARD_RST_INT: receive hardrst signal event interrupt.
2	RW	0x0	RX_SUC_INT RX_SUC_INT: Correctly receive the data and reply"goodcrc" event interrupt
1	RW	0x0	PLUG_INT PLUG_INT: USB plug in event interrupt
0	RW	0x0	TYPEC_INT TYPEC_INT:CC status 0:cc_status not change 1:cc_status changed

INT_MASK
Address: (0x02)

Bit	Attr	Reset Value	Description
7	RW	0x0	VSAFE0V_INT_EN VSAFE0V_INT_EN:USB Voltage under 0.8V event interrupt enable 0:disable 1:enable
6	RW	0x0	CC_OV_STS_INT_EN CC_OV_STS_INT_EN:CC OV event interrupt enable 0:disable 1:enable
5	RW	0x1	TX_SOP_SUC_INT_EN TX_SOP_SUC_INT_EN:The data packet was sent successfully and "goodcrc " was received event interrupt enable 0:disable 1:enable
4	RW	0x1	TX_SOP_FAIL_INT_EN TX_SOP_FAIL_INT_EN:send SOP Fail event interrupt enable 0:disable 1:enable
3	RW	0x1	RX_HARD_RST_INT_EN RX_HARD_RST_INT_EN:receive hardrst signal event interrupt enable 0:disable 1:enable
2	RW	0x1	RX_SUC_INT_EN RX_SUC_INT_EN:Correctly receive the data and reply"goodcrc" event interrupt enable 0:disable 1:enable
1	RW	0x0	PLUG_INT_EN PLUG_INT_EN:USB plug in event interrupt enable 0:disable 1:enable
0	RW	0x1	TYPEC_INT TYPEC_INT:CC status event interrupt enable 0:disable 1:enable

TYPEC_CTRL
Address: (0x03)

Bit	Attr	Reset Value	Description
7:1	RW	0X0	RESV RESV:Reserve
0	RW	0x0	CC_PLUG_ORIENT: The communication channel select 0:CC1 1:CC2

TYPEC_CTRL1
Address: (0x04)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	RESV RESV:Reserve
1	RW	0x0	CLK_16M_EN CLK_16M_EN :write "1" to force enable 16M clk
0	RW	0x0	PD_PWD PD_PWD:write "1" to disable 16M clk

TYPEC_CTRL2
Address: (0x05)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	RESV RESV:Reserve
3	RW	0x0	TOGGLE TOGGLE: 0: disable drp toggle 1:enable drp toggle
2	RW	0x1	CC_RD_EN CC_RD_EN : 0: enable RP 1:enable RD
1:0	RW	0x1	RP_VALUE RP_VALUE: 00:rp off 01:30.5K pull-up 10:1.5A 11:3A

TYPEC_CTRL3
Address: (0x06)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	T_DRP T_DRP: 00:60ms 01:70ms 10:80ms 11：90ms
5:4	RW	0x0	DRP_TOGGLE DRP_TOGGLE: 00:30%src+70%snk 01:40%src+60%snk 10：50% src+50%snk 11:60%src+40%snk
3	RW	0x0	TYPEC_EN TYPEC_EN:Typec enable 0:disable 1:enable RP and CC detect
2	RW	0x0	VSAFE0V_DETECT_EN VSAFE0V_DETECT_EN:USB Voltage under 0.8V detect enable 0:disable 1:enable
1	RW	0x1	LP_MODE_WORK_EN LP_MODE_WORK_EN: Typec low-power work enable 0:disable 1:enable
0	RW	0x1	LP_MODE LP_MODE:Typec enter low-power mode 0:disable 1:enable

TYPEC_STS
Address: (0x07)

Bit	Attr	Reset Value	Description
7	RW	0x0	RESV RESV:Reserve
6	RO	0x0	PD_CC_OV_STS PD_CC_OV_STS: CC OV status
5	RO	0x0	PD_CONN_STS PD_CONN_STS:PD status 0: toggle finish 1:toggle continue
4	RO	0x0	CONN_RESULT CONN_RESULT:CC status 0:RP 1:RD
3:2	RO	0x0	CC2_STS CC2_STS: SRC:00:OPEN 01:RA 10:RD 11:RESERVE SNK:00:OPEN 01:80uA pull-up 10:180uA pull-up 11:330ua
1:0	RO	0x0	CC1_STS CC1_STS: SRC:00:OPEN 01:RA 10:RD 11:RESERVE SNK: 00:OPEN 01:80uA pull-up 10:180uA pull-up 11:330uA pull-up

TYPEC_STS1
Address: (0x08)

Bit	Attr	Reset Value	Description
7:2	RW	0x0	RESV RESV:Reserve
1	RO	0x0	PLUG_STS PLUG_STS: 0:unplug 1: plug in
0	RO	0x0	VSAFE0V_STS VSAFE0V_STS: the voltage of USB status 0:below 0.8V 1:above 0.8V

TYPEC_RX_DETECT
Address: (0x09)

Bit	Attr	Reset Value	Description
7:5	RW	0x0	RESV RESV:Reserve
4	RW	0x0	CABLE_PLUG CABLE_PLUG: 0: Message originated from Source, Sink, or DRP 1: Message originated from a Cable Plug
3	RW	0x0	DATA_ROLE DATA_ROLE: 0:ufp 1:dfp
2:1	RW	0x0	PD_SPEC_REV PD_SPEC_REV: 00:rev1.0 01:rev2.0 10:rev3.0 11:reserve
0	RW	0x0	PWR_ROLE PWR_ROLE: 0: sink 1:source

TYPEC_RX_DETECT1
Address: (0x0A)

Bit	Attr	Reset Value	Description
7:5	RW	0X0	HARD_RST_EN HARD_RST_EN:enable receive the signal of hard reset 0:disable 1:enable
6	RW	0x0	CABLE_RST_EN CABLE_RST_EN:enable receive the signal of cable reset 0:disable 1:enable
5:4	RW	0x0	RESV RESV:RESERVE
3	RW	0x0	SOP11_EN SOP11_EN: 0: TCPC does not detect SOP" message 1: TCPC detects SOP" message
2:1	RW	0x0	SOP1_EN SOP1_EN: 0: TCPC does not detect SOP' message 1: TCPC detects SOP' message
0	RW	0x0	SOP_EN SOP_EN: 0: TCPC does not detect SOP message 1: TCPC detects SOP message

TYPEC_RX_INFO
Address: (0x0B)

Bit	Attr	Reset Value	Description
7:3	RW	0x0	RESV RESV:Reserve
2:0	RW	0x0	SOP_MSG_TYPE SOP_MSG_TYPE: 000: Received SOP 001: Received SOP’ 010: Received SOP'' 011: Received SOP_DBG' 100: Received SOP_DBG'' 110: Received Cable Reset

TYPEC_RX_CTRL
Address: (0x0C)

Bit	Attr	Reset Value	Description
7:1	RW	0x0	RESV RESV:Reserve
0	RW	0x0	RX_FUN_EN RX_FUN_EN:RX function enable 0:disable 1:enable

TYPEC_TX_CFG
Address: (0x0C)

Bit	Attr	Reset Value	Description
7:5	RW	0x0	RESV RESV:Reserve
4:3	RW	0x0	RETRY_CNT RETRY_CNT: 00: No message retry is required 01: Automatically retry message transmission once 10: Automatically retry message transmission twice 11: Automatically retry message transmission three times
2:0	RW	0x0	TX_SOP_MSG TX_SOP_MSG: 000: Transmit SOP 001: Transmit SOP' 010: Transmit SOP'' 011: reserved 100: reserved 101: Transmit Hard Reset 110: Transmit Cable Reset 111: Transmit BIST Carrier Mode 2 (TCPC shall exit the BIST mode no later than tBISTContMode max)

TYPEC_TX_CFG1
Address: (0x0E)

Bit	Attr	Reset Value	Description
7	RW	0x0	PD_RP_AUTO_OFF_EN PD_RP_AUTO_OFF_EN: when TX is turn on the RP auto off enable 0:disable 1:enable
6	RW	0x0	FIFO_READ_SEL FIFO_READ_SEL: 0:the fifo value read by I2C is TX data 1:the fifo value read by I2C is TX data
5	RW	0x0	GOODCRC_CHECK_DISABLE GOODCRC_CHECK_DISABLE: 0: normal operation 1:GOODCRC checking disable.will not wait for GoodCRC
4:3	RW	0x0	RESV RESV:Reserve
2	RW	0x0	BIST_TEST_MODE BIST_TEST_MODE:enter bist mode
1	RW	0x0	TX_CARRIER_MODE TX_CARRIER_MODE: 0:TX BIST Carrier Mode2 only for BIST Cont Mode 1:TX BIST Carrier Mode2 continuously
0	RW	0x0	TX_FUN_EN TX_FUN_EN: TX function enable 0:disable 1:enable

TYPEC_TX_CFG2
Address: (0x0F)

Bit	Attr	Reset Value	Description
7:1	RW	0x0	RESV RESV:Reserve
0	WC	0x0	TX_BMC_EN: Enable the sending of bmc The TX_BMC_EN bits should be clear after TX_BMC_EN bits have been written.

PD_TX_CTRL
Address: (0x10)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	RESV RESV:Reserve
5:0	RW	0x0	TX_BYTE_CNT:The number of bytes the TCPM will write This is the number of bytes in the TX_BUFFER_DATA_OBJECTS plus two (for the TX_BUF_HEADER)

TYPEC_BMC_STS
Address: (0x11)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	RESV RESV:Reserve
5	RW	0x0	CC_BUSY_STS CC_BUSY_STS: CC status 0:There is no data transmission on the CC. 1:There is data transmission on the CC.
4	RW	0x0	RX_FUN_STS RX_FUN_STS:RX receiving status 0: no data 1:received data
3	RW	0x0	RX_PREAMBLE_STS RX_PREAMBLE_STS: Status for RX preamble 0: preamble not received 1: preamble received
2	RW	0x0	RESV RESV:RESERVE
1	RW	0x0	RX_EOP_STS RX_EOP_STS:Status for RX EOP 0: EOP is not received 1: EOP is received
0	RW	0x0	RX_SOP_STS RX_SOP_STS:Status for RX SOP 0:SOP received with no error 1:SOP received with error

RESET
Address: (0x12)

Bit	Attr	Reset Value	Description
7:3	RW	0x0	RESV RESV:Reserve
2	RW	0x0	TX_SRST TX_SRST:Reset related register of the TX 0:release reset 1:set reset
1	RW	0x0	RX_SRST RX_SRST:Reset related register of the RX 0:release reset 1:set reset
0	RW	0x0	PD_RESET PD_RESET:PD reset ,reset of the TX and RX status 0:release reset 1:set reset

RX_CNT

Address: (0x13)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	RESV RESV:Reserve
5:0	RW	0x0	RX_CNT RX_CNT:The length of the received data for RX,not include header data.

RX_CNT
Address: (0x14)

Bit	Attr	Reset Value	Description
7:3	RW	0x0	RESV RESV:Reserve
2:0	RW	0x0	REG_BACK REG_BACK:data

PD_DATA_HEADER_L
Address: (0x15)

Bit	Attr	Reset Value	Description
7:0	RW	0x0	PD_DATA_HEADER_L PD_DATA_HEADER_L:The lower eight bits of the header for PD data

PD_DATA_HEADER_H
Address: (0x16)

Bit	Attr	Reset Value	Description
7:0	RW	0x0	PD_DATA_HEADER_H PD_DATA_HEADER_H:The high eight bits of the header for PD data

PD_DATA_BUFFER
Address: (0x17~0x32)

Bit	Attr	Reset Value	Description
7:0	RW	0x0	PD_DATA_BUFFER PD_DATA_BUFFER:PD data buffer

Chapter 6 Thermal Management

6.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature of RK809B2 has to be below 125℃.

Depending on the thermal mechanical design (Smartphone, Tablet, Personal Navigation Device, etc), the system thermal management software and worst case thermal applications, the junction temperature might be exposed to higher values than those specified above.

Therefore, it is recommended to perform thermal simulations at device level (Smartphone, Tablet, Personal Navigation Device, etc) with the measured power of the worst case UC of the device.

6.2 Package Thermal Characteristics

Table 6-1 provides the thermal resistance characteristics for the package used on this device.

Table 6-1 Thermal Resistance Characteristics

PACKAGE (QFN7X7-68)	**POWER(W)**	$\boldsymbol{\theta_{JA}}$(℃/$\boldsymbol{W}$)	$\boldsymbol{\theta_{JB}}$(℃/$\boldsymbol{W}$)	$\boldsymbol{\theta_{JC}}$(℃/$\boldsymbol{W}$)
RK809B2	2	21.99	12	6.58

Note: The testing PCB is based on 4 layers, 114mm x 76 mm, 1.6mm thickness, Ambient temperature is 85°C.