Rockchip RK960 Datasheet

Revision 1.0
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Revision History

Date	Revision	Description
2024-09-11	1.0	Initial Release

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Chapter 1 Introduction

1.1 Overview

RK960 integrates 802.11b/g/n WLAN and Bluetooth 5.3 dual mode function in single chip. It mainly includes 1x1 WLAN protocol accelerator, WLAN DSSS/CCK/OFDM PHY, BR/EDR/BLE link layer controller, BT GFSK/DQPSK/8-DPSK modem, and 2.4G ISM band WLAN and BT combination radio frequency module. RK960 is a complete high throughput performance, high cost-effective and low power WLAN and Bluetooth combination solution, which is designed for productions covering Internet of Things (IoT), Wearable equipment, Home automation, Cloud Connectivity and so on.

RK960 provides a compact ultra-small form factor solution with minimal external components to drive the costs for mass volumes and allows for flexibility in size, form, and function. Taking advanced design techniques and process technology to deliver the lowest active and idle power, RK960 extends the system battery life while maintaining consistent connectivity and still provides a rich set of features.

RK960 is a very highly integrated design with internal PA, TR switch, Balun, LNA for low BOM cost. The chip is embedded with low power and low cost processor to talk with host device. With the internal processor, RK960 firmware can be flexibly developed for meeting different customer production application requirement.

RK960 provides the automatic hardware calibration solution to tune the RF characteristic to achieve best RF performance, which can avoid RF performance penalty causing by the hardware board differentiation.

1.2 Features

The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

1.2.1 MCU Microprocessor

- Integrated MCU processor
- Integrated interrupt controller
- Serial wire debug port
- Independent MCU in WLAN subsystem and BT subsystem

1.2.2 Memory Organization

- Internal on-chip memory
  - BootROM
  - Internal SRAM
  - Internal ROM
  - eFuse

1.2.3 Internal Memory

- Internal BootROM
  - Independent BootROM in WLAN subsystem and BT subsystem
  - Support system code download by SDIO or SPI in WLAN subsystem
  - Support system code download by UART in BT subsystem

- Internal SRAM
  - One bank system sram in WLAN subsystem
  - One bank system sram in BT subsystem

- Internal ROM
  - One bank system rom in WLAN subsystem
  - One bank system rom in BT subsystem

- eFuse
  - Support 512 bit Size
  - Support Program/Read/Idle mode

1.2.4 System Component

- CRU (clock & reset unit)
  - One oscillator with 24MHz clock input
  - One RC oscillator clock with trim function
  - Support low power clock input directly at 32.768KHz
  - Support one PLL to generate all clocks
  - Support clock gating control for individual components
  - Support global soft-reset control for whole chip, also individual soft-reset for each component
  - Support independent CRU in WLAN subsystem and BT subsystem, also a shared CRU for WLAN/BT common component clock and reset control

- PMU(power management unit)
  - Support only one 3.3v VIN power supply input and one VDDIO power supply input
  - Integrate three LDOs, to supply whole chip power rails
  - Support two separate power domains, which can be power up/down by software based on different application scenes
  - Support multiple configurable work modes to save power by different frequency or automatic clock gating control or power domain on/off control
  - Support independent PMU for WLAN subsystem and BT subsystem

- Timer
  - Total two 64bits timers with interrupt-based operation
  - Support two operation modes: free-running and user-defined count
  - Support timer work state checkable

- Watchdog
  - Total two 32-bit watchdog counters
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - Generate a system reset
    - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
  - Programmable reset pulse length
  - Total 16 defined-ranges of main timeout period

- MailBox
  - One MailBox to service WLAN MCU and BT MCU communication
  - Support four mailbox elements per mailbox, each element includes one data word, one command word register and one flag bit that can represent one interrupt
  - Provide muti-lock registers for software to use to indicate whether mailbox is occupied

- DMAC
  - Support memory-to-memory, memory-to-peripheral and peripheral-to-memory DMA transfers
  - Up to three channels, programmable channel priority
  - Four hardware request from peripherals, programmable hardware request priority

- Multi-block transfers achieved through
  - Linked Lists (block chaining)
  - Auto-reloading of channel registers
  - Contiguous address between blocks
- Support Scatter/Gather

1.2.5 WLAN Subsystem

- IEEE 802.11b/g/n compatible WLAN
- Pass WiFi Alliance Certification Test
- WLAN Baseband Part
  - Support HT20 single-band
  - HW/SW partition optimized to minimize power consumption
  - Frame aggregation for increased MAC efficiency(A-MSDU,A-MPDU) and Low latency immediate High-Throughput Block Acknowledgement
  - Support MAC enhancements including 802.11d/e/h/i/k/r/w
  - Support for WEP, WPA (RSNA using TKIP and MIC), WPA2 (RSNA using CCMP), WPA3(RSNA using CCMP-128)
  - Support both Group Owner (GO) and Group Client (GC) Wi-Fi Direct modes
  - Support concurrent Wi-Fi and Wi-Fi Direct operation
  - Intelligent power control, including 802.11 power save mode
  - Support WLAN/Bluetooth coexistence mechanism
  - Support 96KB data buffer
- WLAN Modem Part
  - Support 6 Mbps to 65 Mbps OFDM(72.2Mbps in SGI mode), 11 Mbps and 5.5 Mbps CCK and legacy 2 Mbps and 1 Mbps DSSS data rates
  - OFDM
    - Modulations: BPSK, QPSK, 16QAM, and 64QAM
    - Code rates: 1/2, 2/3, 3/4 and 5/6
    - Preambles: legacy, greenfield, and mixed mode preambles
    - Single convolutional encoder
    - RIFS of 2 μs (802.11n only)
  - DSSS/CCK
    - Modulations: DBPSK, DQPSK, and CCK
    - Preambles: long and short

1.2.6 BT Subsystem

- Compliance with Bluetooth specification version 5.3 dual mode
- Pass BQB Bluetooth Certification Test
- Bluetooth Controller Part
  - Simultaneous BR/EDR + BLE dual-mode support, and BR/EDR and BLE use the same radio in TDMA mode
  - Low power modes supporting 32.0kHz or 32.768kHz low-power clock frequencies
  - Support 48KB data buffer
  - BR/EDR controller
    - All ACL, CSB, SCO and eSCO packet types (1, 3 and 5 slots packets), including EDR Packets
    - Encryption / Decryption (E0 and/or AES-CCM)
    - Bit stream processing (HEC, CRC, Whitening, FEC 1/3, FEC 2/3)
    - Hopping frequency calculation (1600 and 3200 hops/s)
    - Adaptive Frequency Hopping
    - Bluetooth clock and offsets
    - TDMA / TDD frames formatting and synchronization
    - Audio Path including CVSD, a/μ-Law, PCM codecs, and VoHCI support
  - BLE controller
    - All packet types (Broadcasting / Advertising / Data / Control)
    - Advertising Extension
    - Isochronous channel / Audio over BLE operations support

  - Encryption / Decryption (AES-CCM)
  - Bit stream processing (CRC, Whitening)
  - Frequency Hopping calculation
  - FDMA / TDMA / events formatting and synchronization
  - All device roles support (Broadcaster, Central, Observer, Peripheral)
- Bluetooth Modem Part
  - Supports Bluetooth basic rate (BR, 1Mbps), enhanced data rate (EDR, 2/3Mbps) and low energy (BLE, 1Mbps/2Mbps/500Kbps/125Kbps)
  - Contains digital modem for all supported modulation formats, include GFSK/ π /4-DQPSK/8-DPSK
  - Support 1Msym/s and 2Msym/s
  - Support Long Range

1.2.7 WLAN/Bluetooth Combination Transceiver

- Full Compliance with IEEE 802.11b/g/n and Dual-Mode Bluetooth specification version 5.3
- Pass FCC, CE Certification Test
- Support 2.4G ISM low band RF front-ends
- Receiver integrate Balun, LNA, Mixer, filter and high speed A/D converters
- Support Receiver AGC control, DC tracking and control, quadrature imbalance tracking and control
- Transmitter integrate high speed D/A converters, filter, modulator, PA and Balun
- Support Transmitter I/Q calibration and LO leakage correction
- RF LC oscillator PLL provides the quadrature LO signals to the low band up and down converters. Fractional synthesizer design is employed to accommodate different reference frequencies
- Integrate transmitter and receiver switch to support one RFIO port
- RF receiver's Noise Figure (NF) <5 dB, and has flat filter frequency response, small flick noise and good enough linearity
- Zero-IF for WLAN and Low-IF for BT
- Support external PA/LNA to achieve stronger TX/RX performance

1.2.8 I2S/PCM Interface

- Up to 2 channels TX and 2 channels RX path
- Support master mode and slave mode
- Support I2S normal, left and right justified mode serial audio data transfer
- Support PCM early, late1, late2, late3 mode serial audio data transfer
- Support resolution from 16bits to 32bits

1.2.9 Connectivity

- UART Controller
  - Support three UART interface
  - Embedded two 64-byte FIFO for TX and RX operation respectively
  - Support 5bit,6bit,7bit,8bit serial data transmit or receive
  - Standard asynchronous communication bits such as start, stop and parity
  - Support different input clock for UART operation to get up to 4Mbps baud rate
  - Support auto flow control mode

- SDIO Slave interface
  - Compliant with SDIO Specification Version 3.00
  - Support 4bit data bus width
  - Support 2 Functions
  - Support DMA operation for high speed data transfer
  - Support Dual-Buffer mode to optimize throughput

- SPI Slave interface
  - Support slave mode SPI protocol

- Support serial-slave mode only
- Embedded a APB master interface

- I2C interface
  - Support one I2C interface
  - Support 7bits and 10bits address mode
  - Software programmable clock frequency
  - Data on the I2C-bus can be transferred at rates of up to 100 kbit/s in the Standard-mode, up to 400 kbit/s in the Fast-mode or up to 1 Mbit/s in Fast-mode Plus

- Multiple group of GPIO
  - All of GPIOs can be used to generate interrupt
  - Support level trigger and edge trigger interrupt
  - Support configurable polarity of level trigger interrupt
  - Support configurable rising edge, falling edge and both edge trigger interrupt
  - Support configurable pull direction(pull-up or pull-down)

- Temperature Sensor
  - Support one temperature sensor

- ADC
  - 10-bit resolution
  - One single-ended input channels
  - Input range: 0~1 (V)

1.3 Block Diagram

The following diagram shows the basic block diagram.

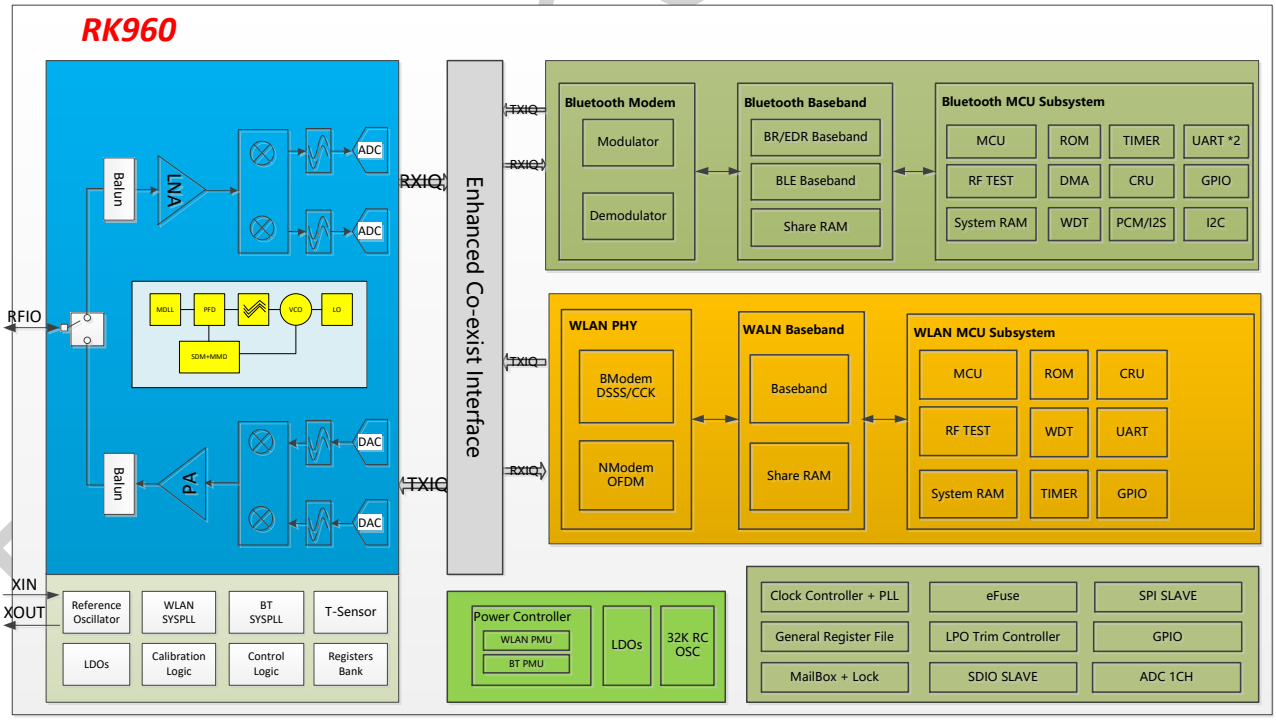


Fig.1-1 RK960 Block Diagram

Chapter 2 Package Information

2.1 Order Information

Orderable Device	RoHS status	Package	Package Qty	Device Feature
RK960	RoHS	QFN48L	3000pcs	WLAN&BT Combination Connectivity Chip

2.2 Top Marking

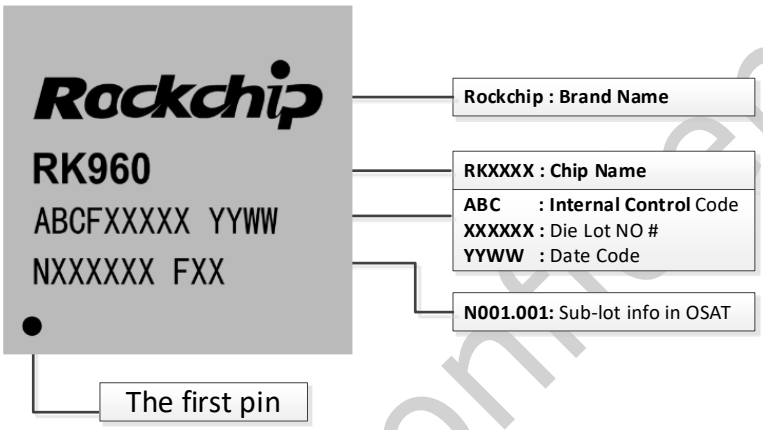


Fig.2-1 Package definition

2.3 QFN48L Dimension

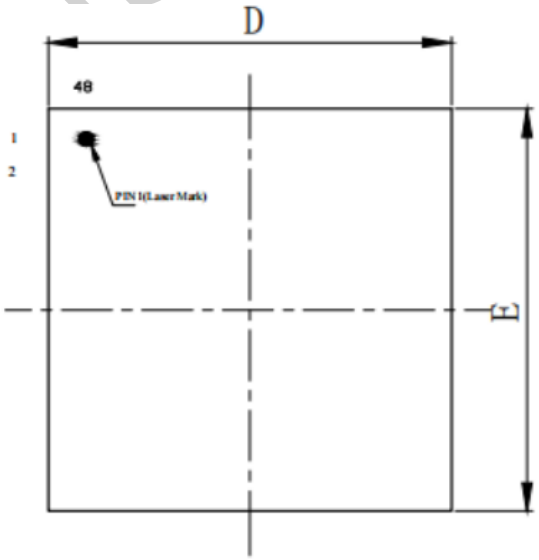


Fig.2-2 Package Top View

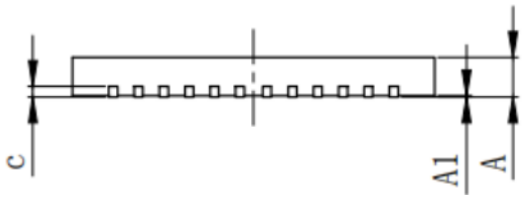


Fig.2-3 Package Side View

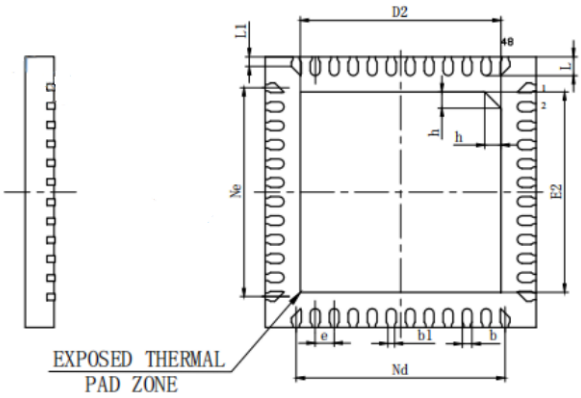


Fig.2-4 Package Bottom View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.50	0.55	0.60
	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.13	0.18	0.23
b1	0.12REF		
c	0.10	0.15	0.20
D	4.90	5.00	5.10
D2	3.60	3.70	3.80
e	0.35BSC		
Ne	3.85BSC		
Nd	3.85BSC		
E	4.90	5.00	5.10
E2	3.60	3.70	3.80
L	0.30	0.35	0.40
L1	0.13	0.18	0.23
h	0.25	0.30	0.35
载体尺寸 (mil)	154X154		

Fig.2-5 Package dimension

2.4 Ball Map

		48 RTC_OUT_VCC1V1	47 LDO_IN_VCC3V3	46 LDO_OUT_VCC1V3	45 LDO_OUT_VCC1V1	44 RF_AVDD3V3	43 RF_RBIAS	42 OSC_XIN	41 OSC__XOUT	40 RF_AVDD1V3_3	39 RF_TEST2	38 RF_TEST1	37 RF_AVDD1V3_2		
BT_EN	1	QFN48L												36	RF_AVDD1V3_1
WLAN_EN	2													35	AVSS
TVSS	3													34	ANT_RF
VCCIO_0	4													33	PA_AVDD3V3
WL_WAKE_HOST	5													32	RF_AVDD1V3_0
SDIO_CLK	6													31	RF_DVDD1V1
SDIO_CMD	7													30	VDD1V1_1
SDIO_D0	8													29	GPIO_1
SDIO_D1	9													28	VCCIO_2
SDIO_D2	10													27	UART2_RX
SDIO_D3	11													26	UART2_TX
GPIO_0	12													25	UART2_CTSN
		13 VDD1V1_0	14 EFUSE_AVDD2V5	15 LPO_CLK_IN	16 TEST_CLK_OUT	17 BT_WAKE_HSOT	18 HOST_WAKE_BT	19 PCM_CLK	20 PCM_IN	21 VCCIO_1	22 PCM_OUT	23 PCM_SYNC	24 UART2_RTSN		

Fig.2-6 Ball Map

2.5 Pin Number List

Table 2-1 Pin Number List Information

PIN NO.	Pin Name	Type	Description
1	BT_EN	I	BT ENABLE
2	WLAN_EN	I	WLAN ENABLE
3	TVSS	I/0	NO Connect
4	VCCIO_0	I	VCCIO power supply
5	WL_WAKE_HOST	I/0	WLAN wake up indication signal from RK960 to HOST
6	SDIO_CLK	I/0	SDIO clock input
7	SDIO_CMD	I/0	SDIO command line
8	SDIO_D0	I/0	SDIO data line 0
9	SDIO_D1	I/0	SDIO data line 1
10	SDIO_D2	I/0	SDIO data line 2
11	SDIO_D3	I/0	SDIO data line 3
12	GPIO_0	I/0	Programmable GPIO pins
13	VDD1V1_0	I	VDD1V1 power supply
14	EFUSE_AVDD2V5	I	EFUSE AVDD2V5 power supply
15	LPO_CLK_IN	I/0	External sleep clock input 32.768 kHz
16	TEST_CLK_OUT	I/0	Test clock output signal
17	BT_WAKE_HOST	I/0	BT wake up indication signal from RK960 to HOST
18	HOST_WAKE_BT	I/0	BT wake up indication signal from HOST to RK960

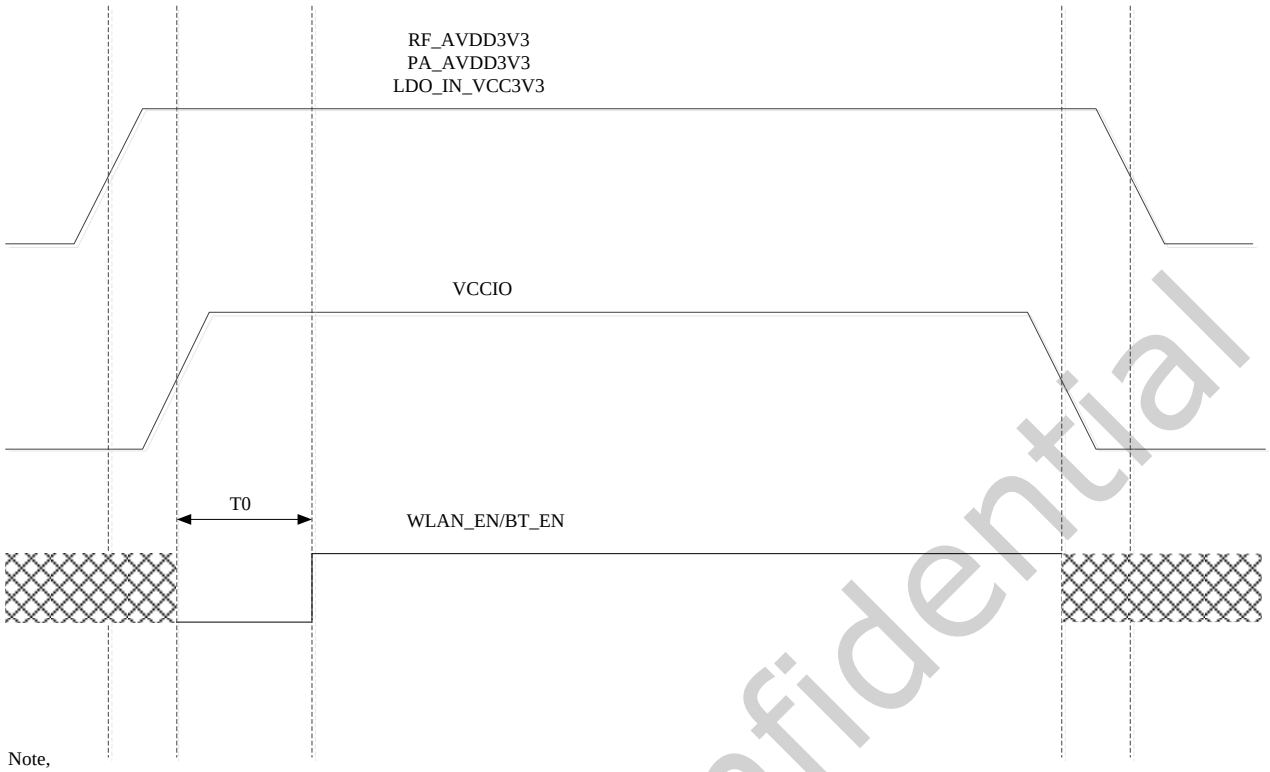
PIN NO.	Pin Name	Type	Description
19	PCM_CLK	I/0	BT PCM clock
20	PCM_IN	I/0	BT PCM data input
21	VCCIO_1	I	VCCIO power supply
22	PCM_OUT	I/0	BT PCM data output
23	PCM_SYNC	I/0	BT PCM SYNC
24	UART2_RTSN	I/0	UART request-to-send
25	UART2_CTSN	I/0	UART clear-to-send
26	UART2_TX	I/0	UART serial output
27	UART2_RX	I/0	UART serial input
28	VCCIO_2	I	VCCIO power supply
29	GPIO_1	I/0	Programmable GPIO pins
30	VDD1V1_1	I	VDD1V1_1 Power supply
31	RF_DVDD1V1	I	RF_DVDD1V1 Power supply
32	RF_AVDD1V3_0	I	RF_AVDD1V3 Power supply
33	PA_AVDD3V3	I	PA_AVDD3V3 Power supply
34	ANT_RF	I/0	BT and WLAN RF output port
35	AVSS	I	Gound
36	RF_AVDD1V3_1	I	RF AVDD1V3 power supply
37	RF_AVDD1V3_2	I	RF AVDD1V3 power supply
38	RF_TEST1	I	RF_TEST1
39	RF_TEST2	I	RF_TEST2
40	RF_AVDD1V3_3	I	RF AVDD1V3 power supply
41	OSC_XOUT	O	XTAL oscillator output
42	OSC_XIN	I	XTAL oscillator input
43	RF_RBIAS	I	RF_RBIAS 14.3K to ground
44	RF_AVDD3V3	I	RF AVDD3V3 power supply
45	LDO_OUT_VCC1V1	O	Output of LDO VCC1V1
46	LDO_OUT_VCC1V3	O	Output of LDO VCC1V3
47	LDO_IN_VCC3V3	I	LDO input power supply
48	RTC_OUT_VCC1V1	O	Output of RTC LDO VCC1V1
EPAD	EPAD	I	EPAD

2.6 Power/Ground IO Description

Table 2-2 Power/Ground IO information

Group	Ball#	Descriptions
VSS	EPAD	EPAD Ground
AVSS	35	Analog Ground
VDD1V1	13,30	Digital Power
RF_DVDD1V1	31	RF Digital Power
VCCIO	4,21,28	VCCIO Power
EFUSE_AVDD2V5	14	eFuse Analog Power
LDO_IN_VCC3V3	47	LDO Analog Power
RF_AVDD3V3	44	RF Analog Power
PA_AVDD3V3	33	RF Analog Power
RF_AVDD1V3	32,36,37,40	RF Analog Power

2.7 Power Sequence



Note,
1) There is no special power up timing requirement between RF_AVDD3V3/PA_AVDD3V3/LDO_IN_VCC3V3/VCCIO
2) T0 need to>=1ms, means after all power supplies are stable, WLAN_EN or BT_EN need to be low greater than 1ms, then can be raised to high
3) There is no special power down timing requirement

Fig.2-7 Power Sequence Requirement

Chapter 3 Electrical Specification

3.1 Absolute Ratings

The below table provides the absolute ratings. Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

Table 3-1 Absolute ratings

Parameters	Related Power Group	Min	Max	Unit
Supply voltage for Digital	VDD1V1	0	1.21	V
Supply voltage for RF Digital	RF_DVDD1V1	0	1.21	V
Supply voltage for VCCIO	VCCIO	0	3.63	V
Supply voltage for RF	RF_AVDD1V3	0	1.43	V
Supply voltage for RF	RF_AVDD3V3	0	3.63	V
Supply voltage for RF	PA_AVDD3V3	0	3.63	V
Supply voltage for LDO	LDO_IN_VCC3V3	0	3.63	V
Supply voltage for eFuse	EFUSE_AVDD2V5	0	2.75	V
Storage Temperature	Tstg	-40	125	℃
Max Conjunction Temperature	Tj	-40	125	℃

3.2 Recommended Operating Condition

Following table describes the recommended operating condition.

Table 3-2 Recommended operating condition

Parameters	Symbol	Min	Typ	Max	Unit
Supply voltage for Digital	VDD1V1	0.99	1.10	1.21	V
Supply voltage for RF Digital	RF_DVDD1V1	0.99	1.10	1.21	V
Supply voltage for VCCIO	VCCIO	2.97 1.62	3.30 1.80	3.63 1.98	V
Supply voltage for RF	RF_AVDD1V3	1.17	1.30	1.43	V
Supply voltage for RF	RF_AVDD3V3	2.97	3.30	3.63	V
Supply voltage for RF	PA_AVDD3V3	2.97	3.30	3.63	V
Supply voltage for LDO	LDO_IN_VCC3V3	2.97	3.30	3.63	V
Supply voltage for eFuse	EFUSE_AVDD2V5	2.25	2.50	2.75	V
OSC input clock frequency		N/A	24	N/A	MHz
Ambient Operating Temperature	T_A	TBD	25	TBD	℃