

# **Rockchip RK962 Datasheet**

**Revision 1.2  
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## Revision History

Date	Revision	Description
2024-02-07	1.0	Initial Release
2025-07-14	1.1	Update the size of the internal storage
2025-07-23	1.2	Add SPI flash description, modify the power supply info

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## Table of Content

Table of Content .....	3
Figure Index .....	4
Table Index.....	4
<a href="#">Warranty Disclaimer</a> .....	6
Chapter 1 Introduction .....	7
1.1 Overview .....	7
1.2 Features .....	7
1.3 Block Diagram .....	11
Chapter 2 Package Information.....	12
2.1 Order Information .....	12
2.2 Top Marking .....	12
2.3 QFN48L Dimension .....	12
2.4 Ball Map .....	14
2.5 Pin Number List .....	14
2.6 Power/Ground IO Description .....	15
2.7 Function IO Description.....	16
2.8 IO Pin Name Description .....	17
Chapter 3 Electrical Specification .....	19
3.1 Absolute Ratings .....	19
3.2 Recommended Operating Condition .....	19

**Figure Index**

Fig.1-1 RK962 Block Diagram ..... 11  
Fig.2-1 Package definition ..... 12  
Fig.2-2 Package Top View..... 12  
Fig.2-3 Package Side View ..... 12  
Fig.2-4 Package Bottom View ..... 13  
Fig.2-5 Package dimension..... 13  
Fig.2-6 Ball Map ..... 14

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## **Table Index**

Table 2-1	Pin Number List Information .....	14
Table 2-2	Power/Ground IO information .....	15
Table 2-3	Function IO description .....	16
Table 2-4	IO function description list.....	17
Table 3-1	Absolute ratings.....	19
Table 3-2	Recommended operating condition .....	19

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## Chapter 1 Introduction

### 1.1 Overview

RK962 integrates 802.11b/g/n WLAN and Bluetooth 5.3 dual mode function in single chip. It mainly includes 1x1 WLAN protocol accelerator, WLAN DSSS/CCK/OFDM PHY, BR/EDR/BLE link layer controller, BT GFSK/DQPSK/8-DPSK modem, and 2.4G ISM band WLAN and BT combination radio frequency module. RK962 is a complete high throughput performance, high cost-effective and low power WLAN and Bluetooth combination solution, which is designed for productions covering Internet of Things (IoT), Wearable equipment, Home automation, Cloud Connectivity and so on.

RK962 provides a compact ultra-small form factor solution with minimal external components to drive the costs for mass volumes and allows for flexibility in size, form, and function. Taking advanced design techniques and process technology to deliver the lowest active and idle power, RK962 extends the system battery life while maintaining consistent connectivity and still provides a rich set of features.

RK962 is a very highly integrated design with internal PA, TR switch, Balun, LNA for low BOM cost. The chip is embedded with low power and low cost processor to talk with host device. With the internal processor, RK962 firmware can be flexibly developed for meeting different customer production application requirement.

RK962 provides the automatic hardware calibration solution to tune the RF characteristic to achieve best RF performance, which can avoid RF performance penalty causing by the hardware board differentiation.

### 1.2 Features

The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

#### 1.2.1 MCU Microprocessor

- Integrated MCU processor
- Integrated interrupt controller
- Serial wire debug port
- Independent MCU in WLAN subsystem and BT subsystem

#### 1.2.2 Memory Organization

- Internal on-chip memory
  - BootROM
  - Internal SRAM 320k Byte
  - Internal ROM 688k Byte
  - eFuse
- External SPI flash
  - Support system self-boot by automatically loading code from SPI flash
  - Support flash programming via BT UART through a serial host software

#### 1.2.3 Internal Memory

- Internal BootROM
  - Independent BootROM in WLAN subsystem and BT subsystem
  - Support system code download by SDIO or SPI in WLAN subsystem
  - Support system code download by UART in BT subsystem
- Internal SRAM
  - One bank system sram in WLAN subsystem

- One bank system sram in BT subsystem
- Internal ROM
  - One bank system rom in WLAN subsystem
  - One bank system rom in BT subsystem
- eFuse
  - Support 512 bit Size
  - Support Program/Read/Idle mode

#### 1.2.4 System Component

- CRU (clock & reset unit)
  - One oscillator with 24MHz clock input
  - One RC oscillator clock with trim function
  - Support low power clock input directly at 32.768KHz
  - Support one PLL to generate all clocks
  - Support clock gating control for individual components
  - Support global soft-reset control for whole chip, also individual soft-reset for each component
  - Support independent CRU in WLAN subsystem and BT subsystem, also a shared CRU for WLAN/BT common component clock and reset control
- PMU(power management unit)
  - Support one 3.3v VIN power supply input, one 1.3v VIN power supply input and one VDDIO power supply input
  - Integrate LDO for 1.1v power supply, to achieve better power consumption performance, this power supply can optionally use an external DC-DC/LDO with a higher energy efficiency ratio
  - Support two separate power domains, which can be power up/down by software based on different application scenes
  - Support multiple configurable work modes to save power by different frequency or automatic clock gating control or power domain on/off control
  - Support independent PMU for WLAN subsystem and BT subsystem
- Timer
  - Total two 64bits timers with interrupt-based operation
  - Support two operation modes: free-running and user-defined count
  - Support timer work state check-able
- Watchdog
  - Total two 32-bit watchdog counters
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - ◆ Generate a system reset
    - ◆ First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
  - Programmable reset pulse length
  - Total 16 defined-ranges of main timeout period
- MailBox
  - One MailBox to service WLAN MCU and BT MCU communication
  - Support four mailbox elements per mailbox, each element includes one data word, one command word register and one flag bit that can represent one interrupt
  - Provide muti-lock registers for software to use to indicate whether mailbox is occupied
- DMAC
  - Support memory-to-memory, memory-to-peripheral and peripheral-to-memory DMA

transfers

- Up to three channels, programmable channel priority
- Four hardware request from peripherals, programmable hardware request priority
- Multi-block transfers achieved through
  - ◆ Linked Lists (block chaining)
  - ◆ Auto-reloading of channel registers
  - ◆ Contiguous address between blocks
- Support Scatter/Gather

### 1.2.5 WLAN Subsystem

- IEEE 802.11b/g/n compatible WLAN
- Pass WiFi Alliance Certification Test
- WLAN Baseband Part
  - Support HT20 single-band
  - HW/SW partition optimized to minimize power consumption
  - Frame aggregation for increased MAC efficiency(A-MSDU,A-MPDU) and Low latency immediate High-Throughput Block Acknowledgement
  - Support MAC enhancements including 802.11d/e/h/i/k/r/w
  - Support for WEP, WPA (RSNA using TKIP and MIC), WPA2 (RSNA using CCMP), WPA3(RSNA using CCMP-128)
  - Support both Group Owner (GO) and Group Client (GC) Wi-Fi Direct modes
  - Support concurrent Wi-Fi and Wi-Fi Direct operation
  - Intelligent power control, including 802.11 power save mode
  - Support WLAN/Bluetooth coexistence mechanism
  - Support 96KB data buffer
- WLAN Modem Part
  - Support 6 Mbps to 65 Mbps OFDM(72.2Mbps in SGI mode), 11 Mbps and 5.5 Mbps CCK and legacy 2 Mbps and 1 Mbps DSSS data rates
  - OFDM
    - ◆ Modulations: BPSK, QPSK, 16QAM, and 64QAM
    - ◆ Code rates: 1/2, 2/3, 3/4 and 5/6
    - ◆ Preambles: legacy, greenfield, and mixed mode preambles
    - ◆ Single convolutional encoder
    - ◆ RIFS of 2  $\mu$ s (802.11n only)
  - DSSS/CCK
    - ◆ Modulations: DBPSK, DQPSK, and CCK
    - ◆ Preambles: long and short

### 1.2.6 BT Subsystem

- Compliance with Bluetooth specification version 5.3 dual mode
- Pass BQB Bluetooth Certification Test
- Bluetooth Controller Part
  - Simultaneous BR/EDR + BLE dual-mode support, and BR/EDR and BLE use the same radio in TDMA mode
  - Low power modes supporting 32.0kHz or 32.768kHz low-power clock frequencies
  - Support 48KB data buffer
  - BR/EDR controller
    - ◆ All ACL, CSB, SCO and eSCO packet types (1, 3 and 5 slots packets), including EDR Packets
    - ◆ Encryption / Decryption (E0 and/or AES-CCM)
    - ◆ Bit stream processing (HEC, CRC, Whitening, FEC 1/3, FEC 2/3)
    - ◆ Hopping frequency calculation (1600 and 3200 hops/s)
    - ◆ Adaptive Frequency Hopping
    - ◆ Bluetooth clock and offsets
    - ◆ TDMA / TDD frames formatting and synchronization
    - ◆ Audio Path including CVSD, a/ $\mu$ -Law, PCM codecs, and VoHCI support
  - BLE controller

- ◆ All packet types (Broadcasting / Advertising / Data / Control)
- ◆ Advertising Extension
- ◆ Isochronous channel / Audio over BLE operations support
- ◆ Encryption / Decryption (AES-CCM )
- ◆ Bit stream processing (CRC, Whitening)
- ◆ Frequency Hopping calculation
- ◆ FDMA / TDMA / events formatting and synchronization
- ◆ All device roles support (Broadcaster, Central, Observer, Peripheral)
- Bluetooth Modem Part
  - Supports Bluetooth basic rate (BR, 1Mbps), enhanced data rate (EDR, 2/3Mbps) and low energy (BLE, 1Mbps/2Mbps/500Kbps/125Kbps)
  - Contains digital modem for all supported modulation formats, include GFSK/ $\pi$ /4-DQPSK/8-DPSK
  - Support 1Msym/s and 2Msym/s
  - Support Long Range

### 1.2.7 WLAN/Bluetooth Combination Transceiver

- Full Compliance with IEEE 802.11b/g/n and Dual-Mode Bluetooth specification version 5.3
- Pass FCC, CE Certification Test
- Support 2.4G ISM low band RF front-ends
- Receiver integrate Balun, LNA, Mixer, filter and high speed A/D converters
- Support Receiver AGC control, DC tracking and control, quadrature imbalance tracking and control
- Transmitter integrate high speed D/A converters, filter, modulator, PA and Balun
- Support Transmitter I/Q calibration and LO leakage correction
- RF LC oscillator PLL provides the quadrature LO signals to the low band up and down converters. Fractional synthesizer design is employed to accommodate different reference frequencies
- Integrate transmitter and receiver switch to support one RFIO port
- RF receiver's Noise Figure (NF) <5 dB, and has flat filter frequency response, small flick noise and good enough linearity
- Zero-IF for WLAN and Low-IF for BT
- Support external PA/LNA to achieve stronger TX/RX performance

### 1.2.8 I2S/PCM Interface

- Up to 2 channels TX and 2 channels RX path
- Support master mode and slave mode
- Support I2S normal, left and right justified mode serial audio data transfer
- Support PCM early, late1, late2, late3 mode serial audio data transfer
- Support resolution from 16bits to 32bits

### 1.2.9 Connectivity

- UART Controller
  - Support three UART interface
  - Embedded two 64-byte FIFO for TX and RX operation respectively
  - Support 5bit,6bit,7bit,8bit serial data transmit or receive
  - Standard asynchronous communication bits such as start, stop and parity
  - Support different input clock for UART operation to get up to 4Mbps baud rate
  - Support auto flow control mode
- SDIO Slave interface
  - Compliant with SDIO Specification Version 3.00
  - Support 4bit data bus width
  - Support 2 Functions
  - Support DMA operation for high speed data transfer
  - Support Dual-Buffer mode to optimize throughput

- SPI Slave interface
  - Support slave mode SPI protocol
  - Support serial-slave mode only
  - Embedded a APB master interface
- I2C interface
  - Support one I2C interface
  - Support 7bits and 10bits address mode
  - Software programmable clock frequency
  - Data on the I2C-bus can be transferred at rates of up to 100 kbit/s in the Standard-mode, up to 400 kbit/s in the Fast-mode or up to 1 Mbit/s in Fast-mode Plus
- Multiple group of GPIO
  - All of GPIOs can be used to generate interrupt
  - Support level trigger and edge trigger interrupt
  - Support configurable polarity of level trigger interrupt
  - Support configurable rising edge, falling edge and both edge trigger interrupt
  - Support configurable pull direction(pull-up or pull-down)
- Temperature Sensor
  - Support one temperature sensor
- ADC
  - 10-bit resolution
  - One single-ended input channels
  - Input range: 0~1 (V)

### 1.3 Block Diagram

The following diagram shows the basic block diagram.

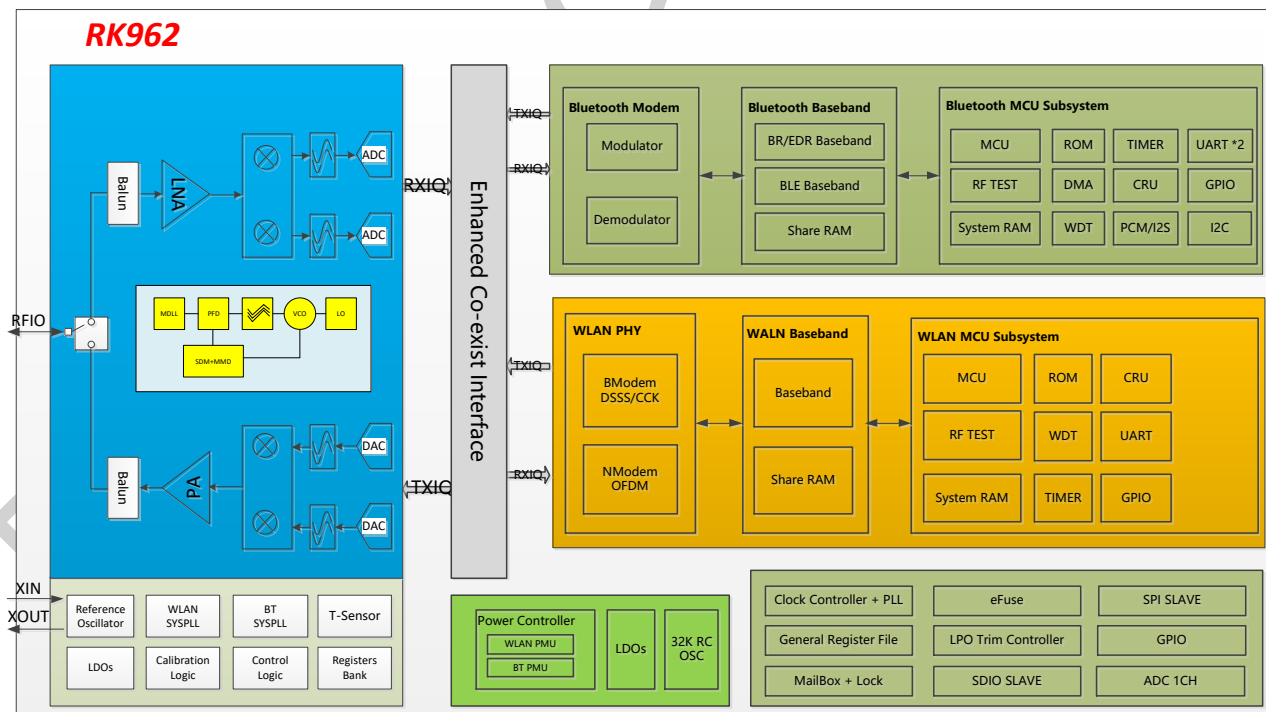


Fig.1-1 RK962 Block Diagram

## Chapter 2 Package Information

### 2.1 Order Information

Orderable Device	RoHS status	Package	Package Qty	Device Feature
RK962	RoHS	QFN48L		WLAN&BT Combination Connectivity Chip

### 2.2 Top Marking

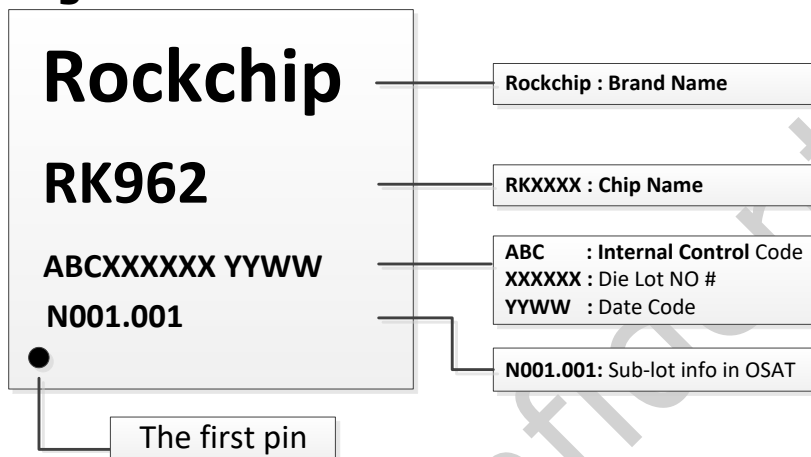


Fig.2-1 Package definition

### 2.3 QFN48L Dimension

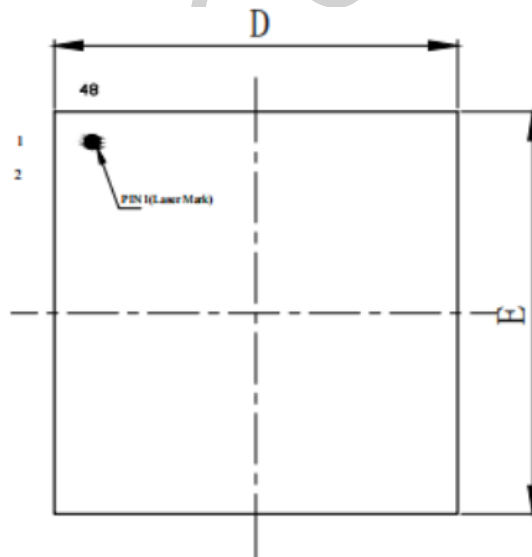


Fig.2-2 Package Top View

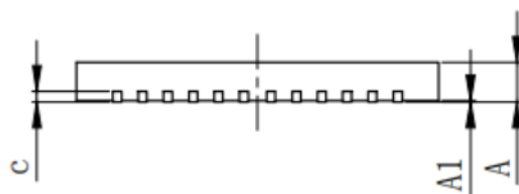


Fig.2-3 Package Side View

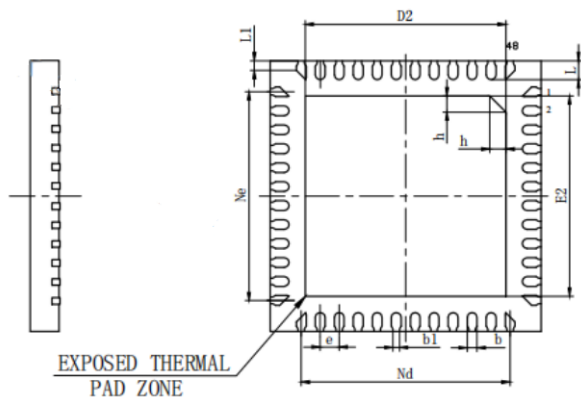


Fig.2-4 Package Bottom View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.50	0.55	0.60
	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.13	0.18	0.23
b1	0.12REF		
c	0.10	0.15	0.20
D	4.90	5.00	5.10
D2	3.60	3.70	3.80
e	0.35BSC		
Ne	3.85BSC		
Nd	3.85BSC		
E	4.90	5.00	5.10
E2	3.60	3.70	3.80
L	0.30	0.35	0.40
L1	0.13	0.18	0.23
h	0.25	0.30	0.35
载体尺寸 (mil)	154X154		

Fig.2-5 Package dimension

## 2.4 Ball Map

		RTC_OUT_VCC1V1	LDO_IN_VCC3V3	LDO_IN_VCC1V3	LDO_OUT_VCC1V1	RF_AVDD3V3	RF_RBIA5	OSC_XIN	OSC_XOUT	RF_AVDD1V3_3	AVSS_1	ADC_IN	RF_AVDD1V3_2	
		48	47	46	45	44	43	42	41	40	39	38	37	
BT_EN	1	QFN48L											36	RF_AVDD1V3_1
WLAN_EN	2												35	AVSS_0
GPO	3												34	ANT_RF
VCCIO_0	4												33	PA_AVDD3V3
WL_WAKE_HOST/GPIO2_A0	5												32	RF_AVDD1V3_0
SDIO_CLK/SPI_CLK/GPIO2_A1	6												31	RF_DVDD1V1
SDIO_CMD/SPI_MOSI/GPIO2_A2	7												30	VDD1V1_1
SDIO_D0/SPI_MISO/GPIO2_A3	8												29	UART0_RX/UART1_TX_M0/GPIO2_C4
SDIO_D1/SPI_CSN/GPIO2_A4	9												28	VCCIO_2
SDIO_D2/UART1_TX_M1/GPIO2_A5	10												27	UART2_RX/GPIO2_C3
SDIO_D3/UART0_TX_M1/GPIO2_A6	11												26	UART2_TX/GPIO2_C2
UART1_RX/UART0_TX_M0/GPIO2_A7	12												25	UART2_CTSN/GPIO2_C1
		VDD1V1_0	EFUSE_AVDD2V5	CLK_32K_IN/GPIO2_B0	PWR_CTRL/GPIO2_B1	BT_WAKE_HOST/GPIO2_B2	HOST_WAKE_BT/GPIO2_B3	PCM_CLK/I2S_SCLK/GPIO2_B4	PCM_IN/I2S_SD/I2C_SCI/GPIO2_B5	VCCIO_1	PCM_OUT/I2S_SDO/I2C_SDA/GPIO2_B6	PCM_SYNC/I2S_LRCK/GPIO2_B7	UART2_RTSN/GPIO2_C0	

Fig.2-6 Ball Map

## 2.5 Pin Number List

Table 2-1 Pin Number List Information

PIN NO.	Pin Name
1	BT_EN
2	WLAN_EN
3	GPO
4	VCCIO_0
5	WL_WAKE_HOST/GPIO2_A0
6	SDIO_CLK/SPI_CLK/GPIO2_A1
7	SDIO_CMD/SPI_MOSI/GPIO2_A2
8	SDIO_D0/SPI_MISO/GPIO2_A3
9	SDIO_D1/SPI_CSN/GPIO2_A4
10	SDIO_D2/UART1_TX_M1/GPIO2_A5
11	SDIO_D3/UART0_TX_M1/GPIO2_A6
12	UART1_RX/UART0_TX_M0/GPIO2_A7
13	VDD1V1_0
14	EFUSE_AVDD2V5
15	CLK_32K_IN/GPIO2_B0
16	PWR_CTRL/GPIO2_B1
17	BT_WAKE_HOST/GPIO2_B2
18	HOST_WAKE_BT/GPIO2_B3

19	PCM_CLK/I2S_SCLK/GPIO2_B4
20	PCM_IN/I2S_SDI/I2C_SCL/GPIO2_B5
21	VCCIO_1
22	PCM_OUT/I2S_SDO/I2C_SDA/GPIO2_B6
23	PCM_SYNC/I2S_LRCK/GPIO2_B7
24	UART2_RTSN/GPIO2_C0
25	UART2_CTSN/GPIO2_C1
26	UART2_TX/GPIO2_C2
27	UART2_RX/GPIO2_C3
28	VCCIO_2
29	UART0_RX/UART1_TX_M0/GPIO2_C4
30	VDD1V1_1
31	RF_DVDD1V1
32	RF_AVDD1V3_0
33	PA_AVDD3V3
34	ANT_RF
35	AVSS_0
36	RF_AVDD1V3_1
37	RF_AVDD1V3_2
38	ADC_IN
39	AVSS_1
40	RF_AVDD1V3_3
41	OSC_XOUT
42	OSC_XIN
43	RF_RBIAS
44	RF_AVDD3V3
45	LDO_OUT_VCC1V1
46	LDO_IN_VCC1V3
47	LDO_IN_VCC3V3
48	RTC_OUT_VCC1V1
EPAD	EPAD

## 2.6 Power/Ground IO Description

Table 2-2 Power/Ground IO information

Group	Ball#	Descriptions
VSS	EPAD	EPAD Ground
AVSS	35,39	Analog Ground
VDD1V1	13,30	Digital Power
RF_DVDD1V1	31	RF Digital Power
VCCIO	4,21,28	VCCIO Power
EFUSE_AVDD2V5	14	eFuse Analog Power
LDO_IN_VCC1V3	46	LDO Analog Power
LDO_IN_VCC3V3	47	LDO Analog Power
RF_AVDD3V3	44	RF Analog Power
PA_AVDD3V3	33	RF Analog Power
RF_AVDD1V3	32,36,37,40	RF Analog Power

## 2.7 Function IO Description

Table 2-3 Function IO description

Pin	Pin Name	Func1	Func2	Func3	Func4	Pad Type	Def	Pull
1	BT_EN	BT_EN				I	I	high-z
2	WLAN_EN	WLAN_EN				I	I	high-z
3	GPO	GPO				O	O	down
5	WL_WAKE_HOST/GPIO2_A0	GPIO2_A0	WL_WAKE_HOST			I/O	I	down
6	SDIO_CLK/SPI_CLK/GPIO2_A1	GPIO2_A1	SDIO_CLK	SPI_CLK		I/O	I	high-z
7	SDIO_CMD/SPI_MOSI/GPIO2_A2	GPIO2_A2	SDIO_CMD	SPI_MOSI		I/O	I	up
8	SDIO_D0/SPI_MISO/GPIO2_A3	GPIO2_A3	SDIO_D0	SPI_MISO		I/O	I	up
9	SDIO_D1/SPI_CSN/GPIO2_A4	GPIO2_A4	SDIO_D1	SPI_CSN		I/O	I	up
10	SDIO_D2/UART1_TX_M1/GPIO2_A5	GPIO2_A5	SDIO_D2	UART1_TX_M1		I/O	I	high-z
11	SDIO_D3/UART0_TX_M1/GPIO2_A6	GPIO2_A6	SDIO_D3	UART0_TX_M1		I/O	I	up
12	UART1_RX/UART0_TX_M0/GPIO2_A7	GPIO2_A7	UART1_RX	UART0_TX_M0		I/O	I	up
15	CLK_32K_IN/GPIO2_B0	GPIO2_B0	CLK_32K_IN			I/O	I	high-z
16	PWR_CTRL/GPIO2_B1	GPIO2_B1	PWR_CTRL			I/O	O	down
17	BT_WAKE_HOST/GPIO2_B2	GPIO2_B2	BT_WAKE_HOST			I/O	I	down
18	HOST_WAKE_BT/GPIO2_B3	GPIO2_B3	HOST_WAKE_BT			I/O	I	down
19	PCM_CLK/I2S_SCLK/GPIO2_B4	GPIO2_B4	PCM_CLK	I2S_SCLK		I/O	I	high-z
20	PCM_IN/I2S_SDI/I2C_SCL/GPIO2_B5	GPIO2_B5	PCM_IN	I2S_SDI	I2C_SCL	I/O	I	up
22	PCM_OUT/I2S_SDO/I2C_SDA/GPIO2_B6	GPIO2_B6	PCM_OUT	I2S_SDO	I2C_SDA	I/O	I	up
23	PCM_SYNC/I2S_LRCK/GPIO2_B7	GPIO2_B7	PCM_SYNC	I2S_LRCK		I/O	I	down
24	UART2_RTSN/GPIO2_C0	GPIO2_C0	UART2_RTSN			I/O	I	high-z
25	UART2_CTSN/GPIO2_C1	GPIO2_C1	UART2_CTSN			I/O	I	up
26	UART2_TX/GPIO2_C2	GPIO2_C2	UART2_TX			I/O	I	up
27	UART2_RX/GPIO2_C3	GPIO2_C3	UART2_RX			I/O	I	up
29	UART0_RX/UART1_TX_M0/GPIO2_C4	GPIO2_C4	UART0_RX	UART1_TX_M0		I/O	I	up
34	ANT_RF	ANT_RF				A		
38	ADC_IN	ADC_IN				A		
41	OSC_XOUT	OSC_XOUT				A		
42	OSC_XIN	OSC_XIN				A		
43	RF_RBIA	RF_RBIA				A		

**Notes:**

- Pad types: I = input, O = output, I/O = input/output (bidirectional)  
 AP = Analog Power, AG = Analog Ground  
 DP = Digital Power, DG = Digital Ground  
 A = Analog
- Reset state: I = input, O = output;

## 2.8 IO Pin Name Description

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 2-4 IO function description list

Interface	Pin Name	Direction	Description
Misc	OSC_XIN	I	Clock input of crystal XO
	OSC_XOUT	O	Clock output of crystal XO
	BT_EN	I	BT subsystem enable signal, active high
	WLAN_EN	I	WLAN subsystem enable signal, active high
	WL_WAKE_HOST	O	Output signal to wake up host processor by WLAN subsystem, active high
	BT_WAKE_HOST	O	Output signal to wake up host processor by BT subsystem, active high
	HOST_WAKE_BT	I	Input signal to wake up BT subsystem by host processor, active high
	PWR_CTRL	O	Output signal to control host processor power up or power down. High means power up, and low means power down
	CLK_32K_IN	I	32K clock input

Interface	Pin Name	Direction	Description
SDIO Slave Controller	SDIO_CLK	I	SDIO clock input
	SDIO_CMD	I/O	SDIO command input and response output
	SDIO_D[i] (i=0~3)	I/O	SDIO data input and output

Interface	Pin Name	Direction	Description
SPI	SPI_CLK	I	SPI serial clock
	SPI_CSN	I	SPI chip select signal, low active
	SPI_MOSI	I	SPI serial data input
	SPI_MISO	O	SPI serial data output

Interface	Pin Name	Direction	Description
PCM Controller	PCM_CLK	I/O	PCM serial clock
	PCM_SYNC	I/O	PCM channel indication signal
	PCM_OUT	O	PCM serial data output
	PCM_IN	I	PCM serial data input

Interface	Pin Name	Direction	Description
I2S Controller	I2S_SCLK	I/O	I2S serial clock
	I2S_LRCK	I/O	I2S channel indication signal
	I2S_SDO	O	I2S serial data output

Interface	Pin Name	Direction	Description
	I2S_SDI	I	I2S serial data input

Interface	Pin Name	Direction	Description
I2C	I2C_SDA	I/O	I2C data
	I2C_SCL	I/O	I2C clock

Interface	Pin Name	Direction	Description
UART	UART0_RX	I	UART serial data input
	UART0_TX_M <i>(i=0,1)</i>	O	UART serial data output
	UART1_RX	I	UART serial data input
	UART1_TX_M <i>(i=0,1)</i>	O	UART serial data output
	UART2_RX	I	UART serial data input
	UART2_TX	O	UART serial data output
	UART2_CTSN	I	UART clear to send modem status input
	UART2_RTSN	O	UART modem control request to send output

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## Chapter 3 Electrical Specification

### 3.1 Absolute Ratings

The below table provides the absolute ratings. Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

Table 3-1 Absolute ratings

Parameters	Related Power Group	Min	Max	Unit
Supply voltage for Digital	VDD1V1	0	1.21	V
Supply voltage for RF Digital	RF_DVDD1V1	0	1.21	V
Supply voltage for VCCIO	VCCIO	0	3.63	V
Supply voltage for RF	RF_AVDD1V3	0	1.43	V
Supply voltage for RF	RF_AVDD3V3	0	3.63	V
Supply voltage for RF	PA_AVDD3V3	0	3.63	V
Supply voltage for LDO	LDO_IN_VCC3V3	0	3.63	V
Supply voltage for LDO	LDO_IN_VCC1V3		1.365	V
Supply voltage for eFuse	EFUSE_AVDD2V5	0	2.75	V
Storage Temperature	Tstg	-40	125	°C
Max Conjunction Temperature	Tj	-40	125	°C

### 3.2 Recommended Operating Condition

Following table describes the recommended operating condition.

Table 3-2 Recommended operating condition

Parameters	Symbol	Min	Typ	Max	Unit
Supply voltage for Digital	VDD1V1	0.99	1.10	1.21	V
Supply voltage for RF Digital	RF_DVDD1V1	0.99	1.10	1.21	V
Supply voltage for VCCIO	VCCIO	2.97 1.62	3.30 1.80	3.63 1.98	V
Supply voltage for RF	RF_AVDD1V3	1.17	1.30	1.43	V
Supply voltage for RF	RF_AVDD3V3	2.97	3.30	3.63	V
Supply voltage for RF	PA_AVDD3V3	2.97	3.30	3.63	V
Supply voltage for LDO	LDO_IN_VCC3V3	2.97	3.30	3.63	V
Supply voltage for LDO	LDO_IN_VCC1V3	1.235	1.30	1.365	V
Supply voltage for eFuse	EFUSE_AVDD2V5	2.25	2.50	2.75	V
OSC input clock frequency		N/A	24	N/A	MHz
Ambient Operating Temperature	T <sub>A</sub>	TBD	25	TBD	°C