Rockchip RKNanoD Datasheet

Revision 1.8
Jan. 2022

Revision History

Date	Revision	Description
2022-1-18	1.8	Update the package QTY
2017-5-11	1.7	Update the package QTY of -G
2017-2-14	1.6	Update
2016-6-20	1.5	Update
2016-3-18	1.4	Update
2016-1-20	1.3	Update
2015-8-27	1.2	Update
2015-6-26	1.1	Add LQFP128 related information
2015-5-19	1.0	Update
2015-4-28	0.2	Add WDT feature, update block diagram
2015-1-26	0.1	First release

Table of Content

Figure Index

Table Index

Warranty Disclaimer

Rockchip Electronics Co.,Ltd makes no warranty, representation or guarantee (expressed, implied, statutory, or otherwise) by or with respect to anything in this document, and shall not be liable for any implied warranties of non-infringement, merchantability or fitness for a particular purpose or for any indirect, special or consequential damages.

Information furnished is believed to be accurate and reliable. However, Rockchip Electronics Co.,Ltd assumes no responsibility for the consequences of use of such information or for any infringement of patents or other rights of third parties that may result from its use.

Rockchip Electronics Co.,Ltd's products are not designed, intended, or authorized for using as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Rockchip Electronics Co.,Ltd's product could create a situation where personal injury or death may occur, should buyer purchase or use Rockchip Electronics Co.,Ltd's products for any such unintended or unauthorized application, buyers shall indemnify and hold Rockchip Electronics Co.,Ltd and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, expenses, and reasonable attorney fees arising out of, either directly or indirectly, any claim of personal injury or death that may be associated with such unintended or unauthorized use, even if such claim alleges that Rockchip Electronics Co.,Ltd was negligent regarding the design or manufacture of the part.

Copyright and Patent Right

Information in this document is provided solely to enable system and software implementers to use Rockchip Electronics Co.,Ltd 's products. There are no expressed or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Rockchip Electronics Co.,Ltd does not convey any license under its patent rights nor the rights of others.
All copyright and patent rights referenced in this document belong to their respective owners and shall be subject to corresponding copyright and patent licensing requirements.

Trademarks

Rockchip and Rockchip™ logo and the name of Rockchip Electronics Co.,Ltd's products are trademarks of Rockchip Electronics Co.,Ltd. and are exclusively owned by Rockchip Electronics Co.,Ltd. References to other companies and their products use trademarks owned by the respective companies and are for reference purpose only.

Confidentiality

The information contained herein (including any attachments) is confidential. The recipient hereby acknowledges the confidentiality of this document, and except for the specific purpose, this document shall not be disclosed to any third party.

Reverse engineering or disassembly is prohibited.

ROCKCHIP ELECTRONICS CO.,LTD. RESERVES THE RIGHT TO MAKE CHANGES IN ITS PRODUCTS OR PRODUCT SPECIFICATIONS WITH THE INTENT TO IMPROVE FUNCTION OR DESIGN AT ANY TIME AND WITHOUT NOTICE AND IS NOT REQUIRED TO UNDATE THIS DOCUMENTATION TO REFLECT SUCH CHANGES.

Chapter 1 Introduction

1.1 Overview

RKnanoD is a ARM Cortex-M3 based microcontroller for Wireless Audio, MP3 player and IOT applications.

RKnanoD includes two M3 cores , up to 1M Bytes Ram, internal power management unit, high quality audio codec, dedicated hardware MP3 decode accelerator, hardware lossless audio decode accelerator and rich peripheral interface. RKnanoD can support Wi-Fi and Bluetooth protocol without external memory, support 24 bits 192k Hz sample rate lossless audio decoding with low power consumption, and support three power modes.

1.2 Features

The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

1.2.1 Boot Option

- Boot from eMMC flash
- Boot from SPI Nand/Nor flash
- Boot from USB

1.2.2 Memory Organization

- 16KB boot ROM
- 64KB PMU SRAM for low power sleep mode
- 320KB SYSRAM0 and 256KB SYSRAM1
- 128KB HIGHRAM0 and 256KB HIGHRAM1
- 64KB/bank clock-gate control for reduce power consumption

1.2.3 Processor

- Dual ARM Cortex-M3 core
  - A Thumb instruction set subset
  - Banked Stack Pointer (SP) only
  - Hardware divide instructions, SDIV and UDIV (Thumb 32-bit instructions)
  - Handler and Thread modes
  - Thumb and Debug states
  - Interruptible-continued LDM/STM, PUSH/POP for low interrupt latency
  - Automatic processor state saving and restoration for low latency Interrupt Service Routine (ISR) entry and exit
  - Support for ARMv6 unaligned accesses
- Nested Vectored Interrupt Controller (NVIC)
  - 32-level priority of interrupt
  - Dynamic reprioritization of interrupts
  - Priority grouping. This enables selection of pre-empting interrupt levelsand non pre-empting interrupt levels
  - Support for tail-chaining and late arrival of interrupts. This enablesback-to-back interrupt processing without the overhead of state saving andrestoration between interrupts
  - Processor state automatically saved on interrupt entry, and restored oninterrupt exit, with no instruction overhead.
- Mail box
  - Support dual-core system: system core and calculation core
  - Support APB interface
  - Support four mailbox elements, each element includes one data word, one command word register and one flag bit that can represent one interrupt

- Four interrupts to system core
- Four interrupts to calculation core

1.2.4 Power Management Unit

- Multiple configurable work modes to save power by different frequency or automatically clock gating control or power domain on/off control
- 2 voltage domains and 3 separate power domains, which can be power up/down by software based on different application scenes

1.2.5 CRU (clock & reset unit)

- Support clock gating control for individual components
- One oscillator with 24MHz clock input and 1 embedded general purpose PLL
- Support global soft-reset control for whole SOC, also individual soft-reset for every components

1.2.6 Hardware Accelerator for MP3 decode

- MP3 imdct36 calculation module
- MP3 sub-band synthesize module

1.2.7 Watch Dog

- 32 bits WDT counter width
- Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
- WDT can perform two types of operations when timeout occurs:
  - Generate a system reset
  - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
- Programmable reset pulse length
- Total 16 defined-ranges of main timeout period

1.2.8 Memory Interface

- SD/MMC controller
  - SD/MMC SPI mode/1bit mode/4bit mode
  - Support Multi Media Card Specification Version 4.41
  - Support SD Memory Card Specification Version 2.0
  - Cards Clock Rate up to PCLK, Re-scaling the SD/MMC clock (PCLK) with the 8-bits pre-scale register in SCU block
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection

- eMMC Interface
  - Support MMC4.41 protocol
  - Provide eMMC boot sequence to receive boot data from external eMMC device
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection
  - 8bits data bus width

- SFCInterface
  - Support transfer data from/to SPI flash device
  - Support x1,x2,x4 data bits mode
  - Support interrupt output, interrupt maskable
  - Support Spansion, MXIC,Gigadevice…vendor's nor flash memory

1.2.9 DISPLAY interface

- Support source data format: RGB565, YUV420
- Support UV swap
- Support YUV2RGB
- Support BT601 limited range
- Support BT709 limited range
- Support BT601 full range
- Support allegro dither down for RGB888 to RGB565
- Support RGB565 display data format
- Support display data swap
- Support max output resolution 400x400
- Built-in i8080 MCU interface
- Support EPD

1.2.10 DMA Controller

- Two DMA Controllers in chip
  - DMAC1 Support 6 DMA channels
  - DMAC2 Support 2 DMA channels
  - Support incremental and fixed addressing mode
  - Support hardware and software trigger DMA transfer mode
  - Support error interrupt, transport-complete interrupt
  - When transport data is not align with source burst, the last data will be transported in single burst mode
  - Support LLP mode and auto-reload

1.2.11 USB interface

- USB 2.0 OTG controller and PHY
- Operates in High-Speed and Full-Speed mode
- Support Session Request Protocol(SRP) and Host Negotiation Protocol(HNP)
- Support 6 endpoints, one control endpoint,two IN/OUT endpoints,one IN endpoint
- Support 4 channels at Host mode,support bulk transfer

1.2.12 Low speed Peripheral interface

- I2C controller
  - Support 3 I2C controllers
  - Supports master modes of I2C bus
  - Software programmable clock frequency and transfer rate up to 100Kbit/s in standard mode or up to 400Kbit/s in Fast mode
  - Supports 7 bits and 10 bits addressing modes
- I2S

- Support 2 I2S controllers
- Support mono/stereo audio file
- Support16 ~ 32 bits audio data transfer
- Support audio sample rate up to 192 KHz
- Support I2S, Left-Justified and Right-Justified digital serial data format

- PWM
  - 5 on-chip PWMs with interrupt-based operation
  - Programmable counter and duty cycle
  - Chained timer for long period purpose
  - Support single counter mode and reload mode
  - Configurable polarity
  - Support interrupt output
- SPI master
  - 2 on-chip SPIs
  - Serial-master operation – Enables serial communication with serial-slave peripheral devices
  - DMA Controller Interface – Enables interface to a DMA controller using a handshaking interface for transfer requests
  - Support interrupt interface to interrupt controller, and independently masking of interrupts
  - One hardware slave-select lines
  - Dynamic control of the serial bit rate of the data transfer
- GPIO
  - 3 groups of GPIO (GPIO0~GPIO2) , 32 GPIOs per group
  - All of GPIOs can be used to generate interrupt to CPU
  - All of pull-up GPIOs are software-programmable for pull-up resistor or not
  - All of pull-down GPIOs are software-programmable for pull-down resistor or not
  - All of GPIOs are always in input direction in default after power-on-reset
- Timer
  - 2 on-chip 64bits Timers in SoC with interrupt-based operation
  - Provide two operation modes: free-running and user-defined count
  - Support timer work state checkable
- UART
  - 6 on-chip UARTs
  - AMBA APB interface
  - DMA Controller Interface – Enables interface to a DMA controller over the AMBA bus using a handshaking interface for transfer requests.
  - Support interrupt interface to interrupt controller.

1.2.13 Analog IP interface

- AUDIO-CODEC
  - High Digital to Analog Convert SNR.
  - High Analog to Digital Convert SNR.
  - Differential analog input microphone input with boost pre-amplify and low-noise microphone bias.

- Stereo line input.
- Stereo line output.
- PLL internal.
- Stereo virtual-ground headphone amplifier with ultra low power.
- One 24bit/8k~192K I2S/PCM interface for stereo DAC and ADC.
- ALC (Automatic Level Control) in ADC path and DRC (Dynamic Range control) in DAC path.
- The high-pass filter in ADC path.
- Soft pop noise suppression.

- SAR-ADC(Successive Approximation Register)
  - 8-channel single-ended 10-bit SAR analog-to-digital converter
  - Sample rate Fs is 200KHz
  - SAR-ADC clock must be large than 11*Fs, recommend is 11*Fs
  - DNL less than1 LSB , INL less than 2.0 LSB
  - Power supply is 3.3V (±10%) for analog interface, power dissipation is less than 900uW

1.3 Block Diagram

The following diagram shows the basic block diagram.

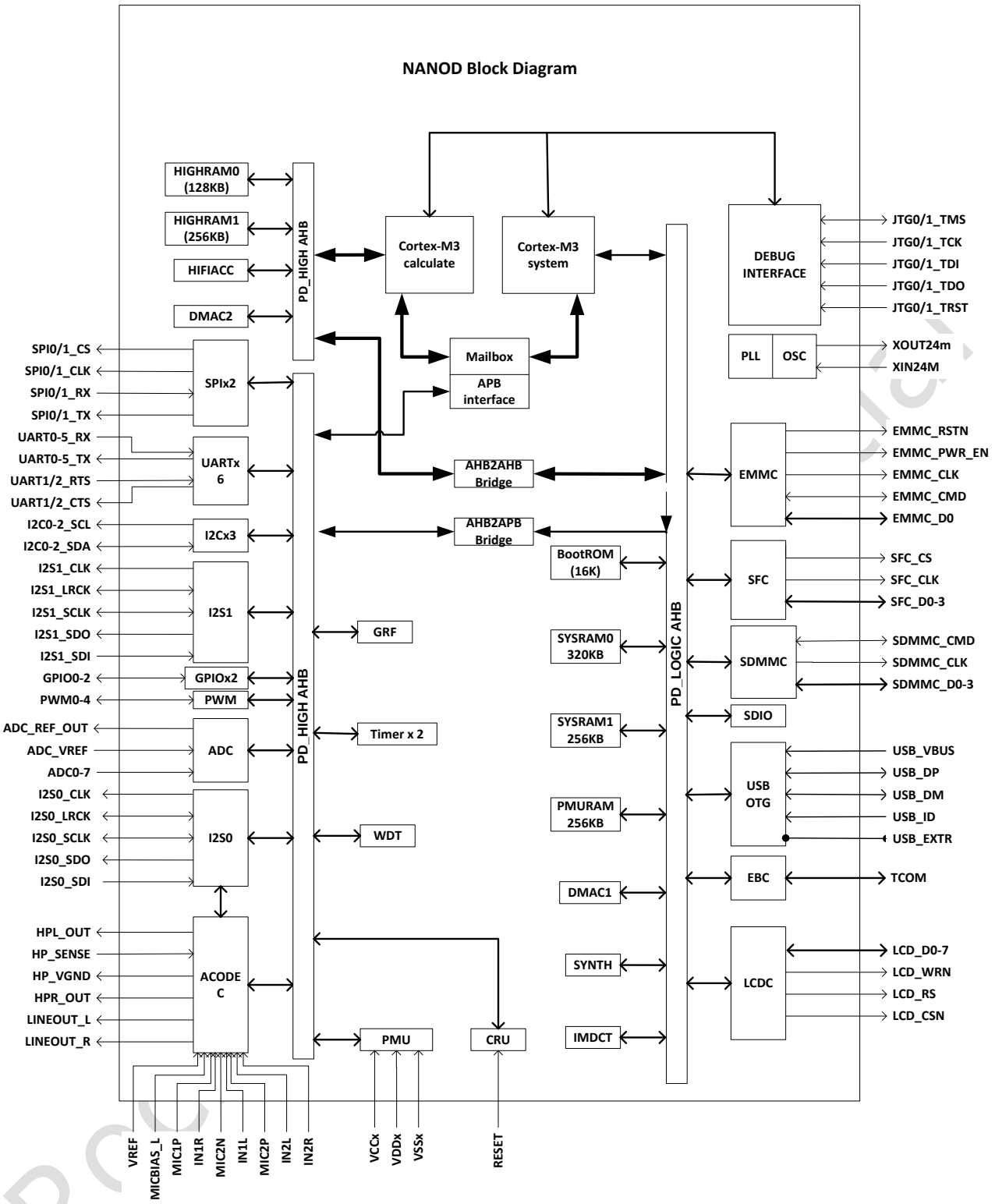


Fig.1-1Block Diagram

Chapter 2 Package information

2.1 Ordering information

Orderable Device	RoHS status	Package	Package Qty	Device special feature
RKNanoD-N	RoHS	QFN68	2000pcs by reel	Dual Cortex-M3 embed controller
RKNanoD-G	RoHS	LFBGA121	2000pcs by reel	Dual Cortex-M3 embed controller
RKNanoD-L	RoHS	LQFP128	900pcs by tray	Dual Cortex-M3 embed controller

2.2 Top Marking

Rockchip: Brand Name

RKXXXX: Chip Name
G:BGA

ABC: Subcontractor Code
XXXXXX: Die Lot NO#
DEFG: Date Code
● The first pin

Rockchip: Brand Name

RKXXXX: Chip Name
N:QFN

ABC: Subcontractor Code
XXXXXX: Die Lot NO#
DEFG: Date Code
● The first pin

Rockchip: Brand Name

RKXXXX: Chip Name
L:LQFP

ABC: Subcontractor Code
XXXXXX: Die Lot NO#
DEFG: Date Code
● The first pin

2.3 Dimension

2.3.1 QFN68 Package

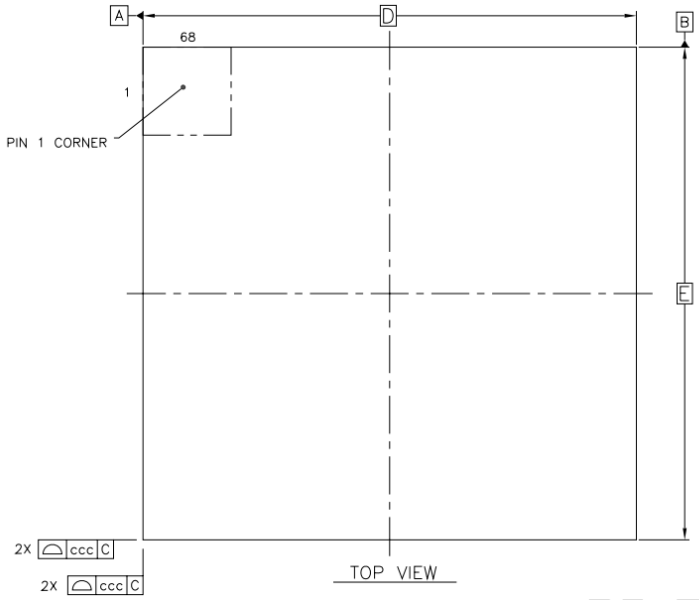


Fig.2-1 RKNanoD-NQFN68 Package Top View

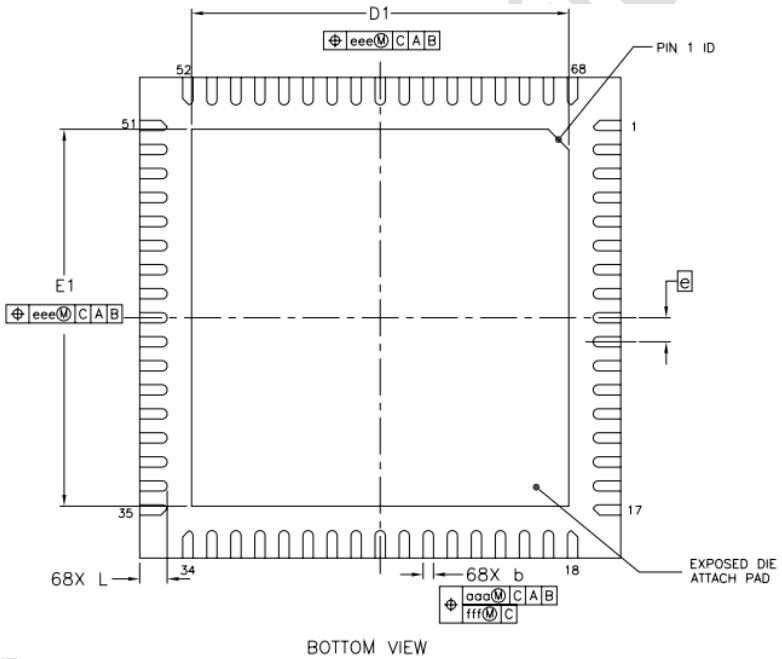


Fig.2-2 RKNanoD-NQFN68 Package Bottom View

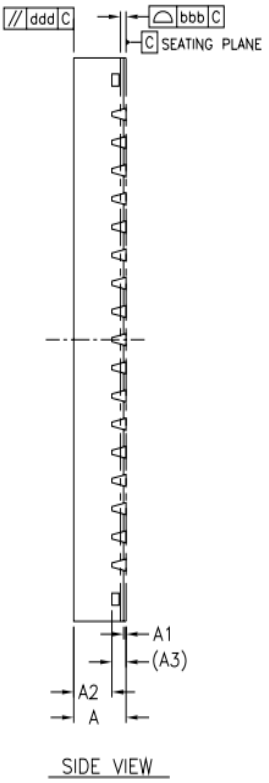


Fig.2-3 RKNanoD-NQFN68 Package Side View

FOR CUSTOMER ONLY				
PACKAGE TYPE	QFN			
PIN COUNT	68			
DESCRIPTION	SYMBOL	MILLIMETER		
		MIN	NOM	MAX
TOTAL THICKNESS	A	0.70	0.75	0.80
STAND OFF	A1	0	0.035	0.05
MOLD THICKNESS	A2	–	0.55	0.57
MATERIAL THICKNESS	A3	–	0.203 REF	–
PACKAGE SIZE	D	–	7 BSC	–
	E	–	7 BSC	–
EP SIZE	D1	5.39	5.49	5.59
	E1	5.39	5.49	5.59
LEAD LENGTH	L	0.30	0.40	0.50
LEAD PITCH	e	0.35 BSC		
LEAD WIDTH	b	0.10	0.15	0.20
LEAD POSITION OFFSET	aaa	0.07		
LEAD COPLANARITY	bbb	0.08		
PACKAGE EDGE PROFILE	ccc	0.10		
MOLD FLATNESS	ddd	0.10		
EP POSITION OFFSET	eee	0.10		
	fff	0.05		

Fig.2-4 RKNanoD-NQFN68 Package Dimension

2.3.2 LFBGA121 Package

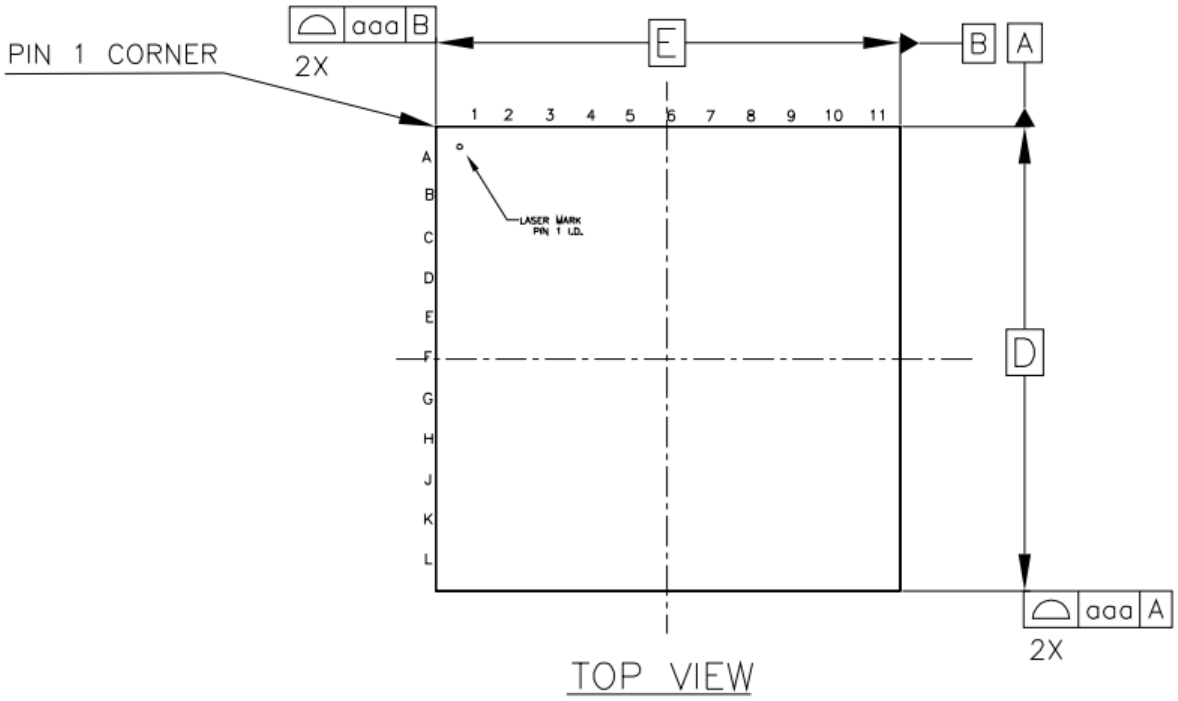


Fig. 2-5 RKNanoD-GLFBGA121 Package Top View

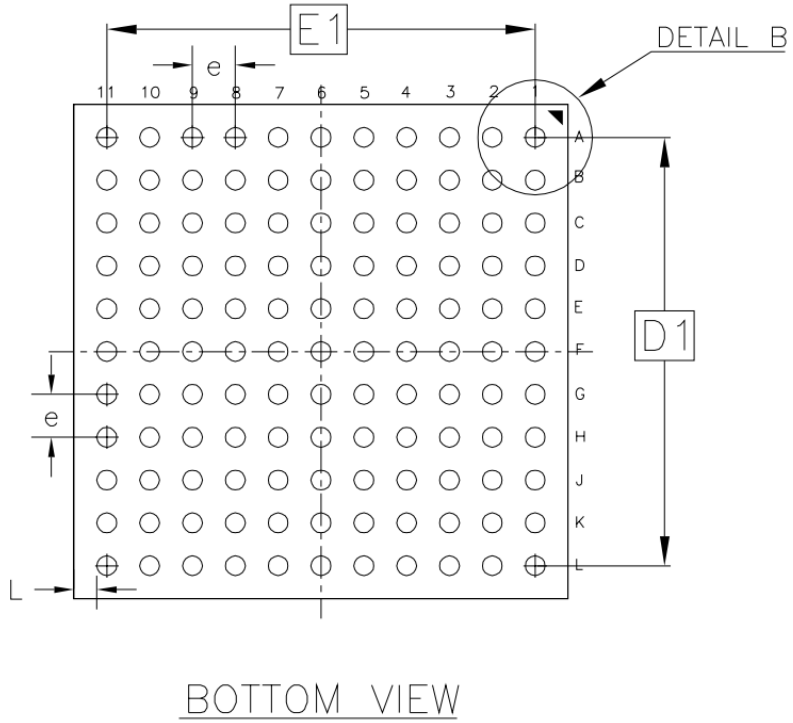


Fig. 2-6 RKNanoD-GLFBGA121 Package BOTTOM View

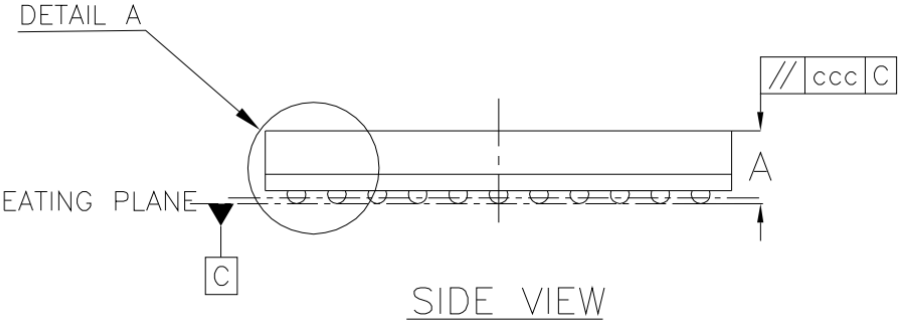


Fig. 2-7 RKNanoD-GLFBGA121 Package SIDE View

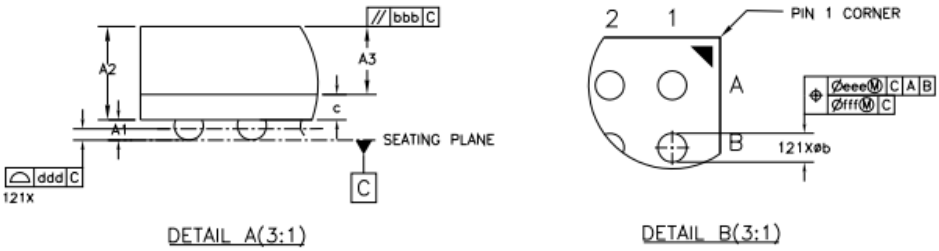


Fig. 2-8 RKNanoD-GLFBGA121 Packag eDETAIL A & B

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.25
A1	0.16	0.21	0.26
A2	0.91	0.96	1.01
A3	0.70 BASIC		
c	0.21	0.26	0.31
D	7.40	7.50	7.60
D1	6.50 BASIC		
E	7.40	7.50	7.60
E1	6.50 BASIC		
e	0.65 BASIC		
L	0.35 REF		
b	0.25	0.30	0.35
aaa	0.10		
bbb	0.10		
ccc	0.20		
ddd	0.08		
eee	0.15		
fff	0.08		

Fig. 2-9 RKNanoD-GLFBGA121 Package Dimension

2.3.3 LQFP128 Package

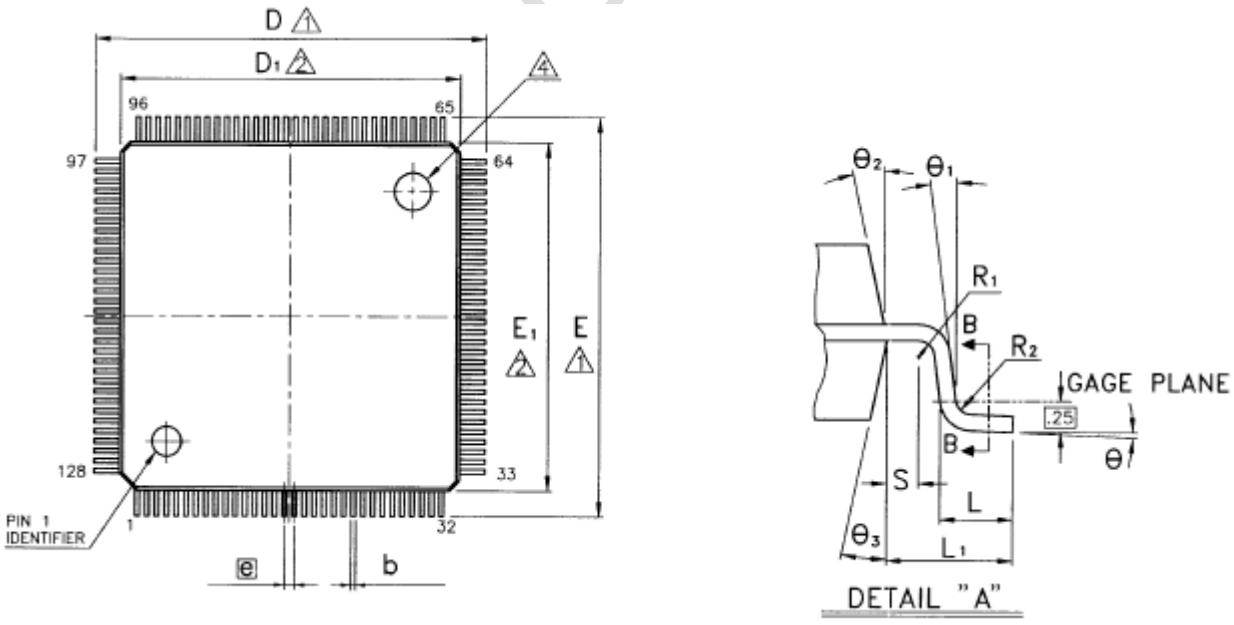


Fig. 2-10 RKNanoD-LQFP128 Package Top View

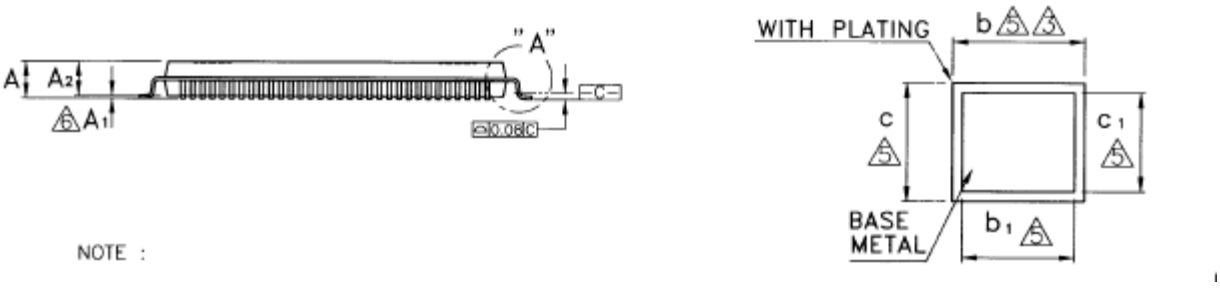


Fig. 2-11 RKNanoD-LQFP128 Package Side View

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	—	0.002	—	—
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.16	0.004	—	0.006
D	15.85	16.00	16.15	0.624	0.630	0.636
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.85	16.00	16.15	0.624	0.630	0.636
E1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	12°TYP			12°TYP		
θ3	12°TYP			12°TYP		

Fig. 2-12 RKNanoD-LQFP128 Package Dimension

2.4 RKNanoD PIN Description

2.4.1 RKNanoD-N PIN Description

Table 2-1 RKNanoD-N Pin Information

PIN	PIN_Name	Fountion0	Fountion1	Fountion2	Fountion3	Pull ②	Pin types ③	Power Domain ④
1	I2C2C_SDA/JTG0_TRST/POWERHOLD/GPIOP2_A6	GPIOP2_A6	I2C2C_SDA	JTG0_TRST	POWERHOLD	down	I/O	IO
2	UART1A_RX/I2C0B_SCL/SPI1B_TX/GPIOP2_C1	GPIOP2_C1	UART1A_RX	I2C0B_SCL	SPI1B_TX	up	I/O	IO
3	UART1A_TX/I2C0B_SDA/SPI1B_CLK/GPIOP2_C0	GPIOP2_C0	UART1A_TX	I2C0B_SDA	SPI1B_CLK	up	I/O	IO
4	VDD	VDD					DP	
5	XOUT24M	XOUT24M					O	IO
6	XIN24M	XIN24M					I	IO
7	VDD_PLL	VDD_PLL					AP	PLL
8	VCC_PLL	VCC_PLL					AP	PLL
9	VCC	VCC					DP	IO
10	SDMMC_CMD/SPI1A_CS/UART3_TX/GPIO1_A5	GPIO1_A5	SDMMC_CMD	SPI1A_CS	UART3_TX	up	I/O	IO
11	SDMMC_CLK/SPI1A_CLK/UART3_RX/GPIO1_A6	GPIO1_A6	SDMMC_CLK	SPI1A_CLK	UART3_RX	up	I/O	IO
12	SDMMC_D0/SPI1A_RX/UART4_TX/GPIO1_A7	GPIO1_A7	SDMMC_D0	SPI1A_RX	UART4_TX	up	I/O	IO

13	SDMMC_D1/SPI1A_TX/UART4_RX/GPIO1_B0	GPIO1_B0	SDMMC_D1	SPI1A_TX	UART4_RX	up	I/O	IO
PIN	**PIN_Name**	**Fountion0**	**Fountion1**	**Fountion2**	**Fountion3**	**Pull ②**	**Pin types ①**	**Power Domain ④**
14	SDMMC_D2/I2C1B_SCL/UART5_TX/GPIO1_B1	GPIO1_B1	SDMMC_D2	I2C1B_SCL	UART5_TX	up	I/O	IO
15	SDMMC_D3/I2C1B_SDA/UART5_RX/GPIO1_B2	GPIO1_B2	SDMMC_D3	I2C1B_SDA	UART5_RX	up	I/O	IO
16	VDD	VDD					DP	
17	USB_DM	USB_DM	UART0B_RX				A	USB
18	USB_DP	USB_DP	UART0B_TX				A	USB
19	VBUS	VBUS					I	USB
20	USB_VDD12	USB_VDD12					DP	USB
21	USB_EXTR	USB_EXTR					I	USB
22	AVDD_IO/USB_VCC33	AVDD_IO	USB_VCC33				AP	USB
23	AVSS_IO	AVSS_IO					AG	USB
24	HPL_OUT	HPL_OUT					A	ACODEC
25	HP_SENSE	HP_SENSE					A	ACODEC
26	HP_VGND	HP_VGND					A	ACODEC
27	HPR_OUT	HPR_OUT					A	ACODEC
28	VREF	VREF					A	ACODEC
29	MICBIAS_L	MICBIAS_L					A	ACODEC
30	MIC1N	MIC1N					A	ACODEC
31	MIC1P	MIC1P					A	ACODEC
32	IN1R	IN1R	MIC2N				A	ACODEC
33	IN1L	IN1L	MIC2P				A	ACODEC
34	AVSS	AVSS					AG	ACODEC
35	AVDD	AVDD					AP	ACODEC
36	ADC0	ADC0					A	IO
37	ADC1	ADC1					A	IO
38	VCC/ADC_VCC33	VCC	ADC_VCC33				DP	IO
39	EMMC_PWREN/I2S1B_CLK/GPIO0_A0	GPIO0_A0	EMMC_PWREN	I2S1B_CLK		down	I/O	IO
40	EMMC_CLK/I2S1B_LRCK/UART2C_TX/GPIO0A1	GPIO0A1	EMMC_CLK	I2S1B_LRCK	UART2C_TX	down	I/O	IO
41	EMMC_CMD/I2S1B_SCLK/UART2C_RX/GPIO0_A2	GPIO0_A2	EMMC_CMD	I2S1B_SCLK	UART2C_RX	up	I/O	IO
42	EMMC_D0/I2S1B_SDO/UART2C_CTS/GPIO0_A3	GPIO0_A3	EMMC_D0	I2S1B_SDO	UART2C_CTS	up	I/O	IO
43	EMMC_D1/I2S1B_SDI/UART2C_RTS/GPIO0_A4	GPIO0_A4	EMMC_D1	I2S1B_SDI	UART2C_RTS	up	I/O	IO
44	EMMC_D2/SFC_D3/I2C0C_SDA/GPIO0_A5	GPIO0_A5	EMMC_D2	SFC_D3	I2C0C_SDA	up	I/O	IO
45	EMMC_D3/SFC_D2/I2C0C_SCL/GPIO0_A6	GPIO0_A6	EMMC_D3	SFC_D2	I2C0C_SCL	up	I/O	IO
46	EMMC_D4/SFC_D1/GPIO0_A7	GPIO0_A7	EMMC_D4	SFC_D1		up	I/O	IO
47	EMMC_D5/SFC_D0/JTG1_TDI/GPIO0_B0	GPIO0_B0	EMMC_D5	SFC_D0	JTG1_TDI	up	I/O	IO
48	EMMC_D6/SFC_CLK/JTG1_TDO/GPIO0_B1	GPIO0_B1	EMMC_D6	SFC_CLK	JTG1_TDO	up	I/O	IO
49	EMMC_D7/SFC_CS/JTG1_TRST/GPIO0_B2	GPIO0_B2	EMMC_D7	SFC_CS	JTG1_TRST	up	I/O	IO
50	VDD	VDD					DP	
51	LCD_D0/SPI0A_TX/GPIO0_C0	GPIO0_C0	LCD_D0	SPI0A_TX		up	I/O	IO
52	LCD_D1/SPI0A_RX/GPIO0_C1	GPIO0_C1	LCD_D1	SPI0A_RX		up	I/O	IO
53	LCD_D2/SPI0A_CLK/GPIO0_C2	GPIO0_C2	LCD_D2	SPI0A_CLK		up	I/O	IO
54	LCD_D3/SPI0A_CS/GPIO0_C3	GPIO0_C3	LCD_D3	SPI0A_CS		up	I/O	IO
55	LCD_D4/UART2B_RX/GPIO0_C4	GPIO0_C4	LCD_D4	UART2B_RX		up	I/O	IO
56	LCD_D5/UART2B_TX/GPIO0_C5	GPIO0_C5	LCD_D5	UART2B_TX		up	I/O	IO
57	LCD_D6/UART2B_RTS/GPIO0_C6	GPIO0_C6	LCD_D6	UART2B_RTS		up	I/O	IO
58	LCD_D7/UART2B_CTS/GPIO0_C7	GPIO0_C7	LCD_D7	UART2B_CTS		up	I/O	IO
59	LCD_WRN/I2C2B_SCL/GPIO0_D0	GPIO0_D0	LCD_WRN	I2C2B_SCL		up	I/O	IO
60	LCD_RS/I2C2B_SDA/GPIO0_D1	GPIO0_D1	LCD_RS	I2C2B_SDA		up	I/O	IO
61	VDD	VDD					DP	
62	VCC	VCC					DP	IO

63	UART1A_RTS/JTG0_TMS/SPI1B_CS/GPIOP2_B6	GPIOP2_B6	UART1A_RTS	JTG0_TMS	SPI1B_CS	up	I/O	IO
64	UART1A_CTS/JTG0_TCK/SPI1B_RX/GPIOP2_B7	GPIOP2_B7	UART1A_CTS	JTG0_TCK	SPI1B_RX	up	I/O	IO
PIN	**PIN_Name**	**Fountion0**	**Fountion1**	**Fountion2**	**Fountion3**	**Pull ②**	**Pin types ①**	**Power Domain④**
65	RESET	RESET					I	IO
66	PWM1/CLK_OBS/EBC_GDPWR1/GPIOP2_A3	GPIOP2_A3	PWM1	CLK_OBS		up	I/O	IO
67	PWM0/JTG0_TDI/PMU_ST2/GPIOP2_A4	GPIOP2_A4	PWM0	JTG0_TDI	PMU_ST2	down	I/O	IO
68	I2C2C_SCL/JTG0_TDO/PMU_ST1/GPIOP2_A5	GPIOP2_A5	I2C2C_SCL	JTG0_TDO	PLAYON	down	I/O	IO
69	GND						DG	

Note:

①:Pintypes: I = input, O = output, I/O = input/output (bidirectional),

AP = Analog Power, AG = Analog Ground
DP = Digital Power, DG = Digital Ground
A = Analog

②: The pull up/pull down can be disabled.

③:POWERHOLD and PLAYON are defined by software.

④: Power domain

IO: power supply for system and logic
PLL: power supply for PLL
USB: power supply for USB and ACODEC IO
ACODEC: power supply for ACODEC core

2.4.2 RKNanoD-G ball Description

Table 2-2 RKNanoD-G ball information

Ball	Ball_Name	Fountion0	Fountion1	Fountion2	Fountion3	Pull②	Pintypes①	Power Domain③
A1	I2C2C_SDA/JTG0_TRST/POWERHOLD/GPIOP2_A6	GPIOP2_A6	I2C2C_SDA	JTG0_TRST	POWERHOLD	down	I/O	PMU
A2	I2C2C_SCL/JTG0_TDO/PLAYON/GPIOP2_A5	GPIOP2_A5	I2C2C_SCL	JTG0_TDO	PLAYON	down	I/O	PMU
A3	PWM0/JTG0_TDI/PMU_ST2/GPIOP2_A4	GPIOP2_A4	PWM0	JTG0_TDI	PMU_ST2	down	I/O	PMU
A4	UART1A_CTS/JTG0_TCK/SPI1B_RX/GPIOP2_B7	GPIOP2_B7	UART1A_CTS	JTG0_TCK	SPI1B_RX	up	I/O	PMU
A5	PWM3/I2C2A_SCL/EBC_SDCE0/GPIOP2_A1	GPIOP2_A1	PWM3	I2C2A_SCL	EBC_SDCE0	up	I/O	PMU
A6	I2C1A_SDA/SPI0B_CS/EBC_SDCE3/GPIOP2_B0	GPIOP2_B0	I2C1A_SDA	SPI0B_CS	EBC_SDCE3	up	I/O	PMU
A7	UART2A_TX/I2S0_LRCK/EBC_GDSP/GPIO0_B6	GPIO0_B6	UART2A_TX	I2S0_LRCK	EBC_GDSP	up	I/O	IO1
A8	LCD_D7/UART2B_CTS/EBC_SDDO7/GPIO0_C7	GPIO0_C7	LCD_D7	UART2B_CTS	EBC_SDDO7	up	I/O	IO1
A9	LCD_D4/UART2B_RX/EBC_SDDO4/GPIO0_C4	GPIO0_C4	LCD_D4	UART2B_RX	EBC_SDDO4	up	I/O	IO1
A10	LCD_D1/SPI0A_RX/EBC_SDDO1/GPIO0_C1	GPIO0_C1	LCD_D1	SPI0A_RX	EBC_SDDO1	up	I/O	IO1
A11	LCD_D0/SPI0A_TX/EBC_SDDO0/GPIO0_C0	GPIO0_C0	LCD_D0	SPI0A_TX	EBC_SDDO0	up	I/O	IO1
B1	PWM1/CLK_OBS/EBC_GDPWR1/GPIOP2_A3	GPIOP2_A3	PWM1	CLK_OBS	EBC_GDPWR1	up	I/O	PMU
B2	RESET	RESET				down	I	PMU
B3	UART1A_RTS/JTG0_TMS/SPI1B_CS/GPIOP2_B6	GPIOP2_B6	UART1A_RTS	JTG0_TMS	SPI1B_CS	up	I/O	PMU
B4	PWM2EBC_GDPWR2/PMU_ST3/GPIOP2_A2	GPIOP2_A2	PWM2	EBC_GDPWR2	PMU_ST3	down	I/O	PMU
B5	PWM4/I2C2A_SDA/EBC_GDPWR0/GPIOP2_A0	GPIOP2_A0	PWM4	I2C2A_SDA	EBC_GDPWR0	up	I/O	PMU
B6	UART2A_RTS/I2S0_SDI/EBC_VCOM/GPIO0_B3	GPIO0_B3	UART2A_RTS	I2S0_SDI	EBC_VCOM	up	I/O	IO1
B7	UART2A_RX/I2S0_SCLK/EBC_GDCLK/GPIO0_B5	GPIO0_B5	UART2A_RX	I2S0_SCLK	EBC_GDCLK	up	I/O	IO1
B8	LCD_CSN/I2S0_CLK/EBC_GDOE/GPIO0_B7	GPIO0_B7	LCD_CSN	I2S0_CLK	EBC_GDOE	up	I/O	IO1
B9	LCD_WRN/I2C2B_SCL/EBC_SDLE/GPIO0_D0	GPIO0_D0	LCD_WRN	I2C2B_SCL	EBC_SDLE	up	I/O	IO1
B10	LCD_D5/UART2B_TX/EBC_SDDO5/GPIO0_C5	GPIO0_C5	LCD_D5	UART2B_TX	EBC_SDDO5	up	I/O	IO1
B11	LCD_D2/SPI0A_CLK/EBC_SDDO2/GPIO0_C2	GPIO0_C2	LCD_D2	SPI0A_CLK	EBC_SDDO2	up	I/O	IO1
C1	UART0A_TX/JTG1_TCK/I2C1C_SCL/GPIOP2_B5	GPIOP2_B5	UART0A_TX	JTG1_TCK	I2C1C_SCL	up	I/O	PMU
C2	UART0A_RX/JTG1_TMS/I2C1C_SDA/GPIOP2_B4	GPIOP2_B4	UART0A_RX	JTG1_TMS	I2C1C_SDA	up	I/O	PMU
C3	PMU_IDLE/GPIOP2_A7	GPIOP2_A7	PMU_IDLE			down	I/O	PMU
C4	VCC_PMU	VCC_PMU					DP	PMU

Ball	Ball_Name	Fountion0	Fountion1	Fountion2	Fountion3	Pull②	Pintypes①	Power Domain③
C5	I2C1A_SCL/SPI0B_CLK/EBC_BORDER1/GPIOP2_B1	GPIOP2_B1	I2C1A_SCL	SPI0B_CLK	EBC_BORDER1	up	I/O	PMU
C6	UART2A_CTS/I2S0_SDO/EBC_SDCLK/GPIO0_B4	GPIO0_B4	UART2A_CTS	I2S0_SDO	EBC_SDCLK	up	I/O	IO1
C7	VDD	VDD					DP	
C8	LCD_RS/I2C2B_SDA/EBC_SDOE/GPIO0_D1	GPIO0_D1	LCD_RS	I2C2B_SDA	EBC_SDOE	up	I/O	IO1
C9	LCD_D6/UART2B_RTS/EBC_SDDO6/GPIO0_C6	GPIO0_C6	LCD_D6	UART2B_RTS	EBC_SDDO6	up	I/O	IO1
C10	EMMC_D4/SFC_D1/GPIO0_A7	GPIO0_A7	EMMC_D4	SFC_D1		up	I/O	IO0
C11	LCD_D3/SPI0A_CS/EBC_SDDO3/GPIO0_C3	GPIO0_C3	LCD_D3	SPI0A_CS	EBC_SDDO3	up	I/O	IO1
D1	XIN24M	XIN24M					I	PMU
D2	UART1A_TX/I2C0B_SDA/SPI1B_CLK/GPIOP2_C0	GPIOP2_C0	UART1A_TX	I2C0B_SDA	SPI1B_CLK	up	I/O	PMU
D3	UART1A_RX/I2C0B_SCL/SPI1B_TX/GPIOP2_C1	GPIOP2_C1	UART1A_RX	I2C0B_SCL	SPI1B_TX	up	I/O	PMU
D4	VDD_PMU	VDD_PMU					DP	PMU
D5	I2C0A_SCL/SPI0B_TX/EBC_SDCE5/GPIOP2_B2	GPIOP2_B2	I2C0A_SCL	SPI0B_TX	EBC_SDCE5	up	I/O	PMU
D6	VSS	VSS					DG	PMU
D7	VCC_1	VCC_1					DP	IO1
D8	VSS	VSS					DG	
D9	EMMC_D2/SFC_D3/I2C0C_SDA/GPIO0_A5	GPIO0_A5	EMMC_D2	SFC_D3	I2C0C_SDA	up	I/O	IO0
D10	EMMC_D5/SFC_D0/JTG1_TDI/GPIO0_B0	GPIO0_B0	EMMC_D5	SFC_D0	JTG1_TDI	up	I/O	IO0
D11	EMMC_D6/SFC_CLK/JTG1_TDO/GPIO0_B1	GPIO0_B1	EMMC_D6	SFC_CLK	JTG1_TDO	up	I/O	IO0
E1	VDD_PLL	VDD_PLL					AP	PLL
E2	XOUT24M	XOUT24M					I	PMU
E3	PMU_TEST	PMU_TEST					I	PMU
E4	SDMMC_CMD/SPI1A_CS/UART3_TX/GPIO1_A5	GPIO1_A5	SDMMC_CMD	SPI1A_CS	UART3_TX	up	I/O	IO2
E5	I2C0A_SDA/SPI0B_RX/EBC_BORDER0/GPIOP2_B3	GPIOP2_B3	I2C0A_SDA	SPI0B_RX	EBC_BORDER0	up	I/O	PMU
E6	VSS	VSS					DG	
E7	VSS	VSS					DG	
E8	VSS	VSS					DG	
E9	VCC_0	VCC_0					DP	IO0
E10	EMMC_D3/SFC_D2/I2C0C_SCL/GPIO0_A6	GPIO0_A6	EMMC_D3	SFC_D2	I2C0C_SCL	up	I/O	IO0
E11	EMMC_D7/SFC_CS/JTG1_TRST/GPIO0_B2	GPIO0_B2	EMMC_D7	SFC_CS	JTG1_TRST	up	I/O	IO0
F1	VCC_PLL	VCC_PLL					DP	PLL
F2	SDMMC_D1/SPI1A_TX/UART4_RX/GPIO1_B0	GPIO1_B0	SDMMC_D1	SPI1A_TX	UART4_RX	up	I/O	IO2
F3	SDMMC_D2/I2C1B_SCL/UART5_TX/GPIO1_B1	GPIO1_B1	SDMMC_D2	I2C1B_SCL	UART5_TX	up	I/O	IO2
F4	SDMMC_CLK/SPI1A_CLK/UART3_RX/GPIO1_A6	GPIO1_A6	SDMMC_CLK	SPI1A_CLK	UART3_RX	up	I/O	IO2
F5	ADC5	ADC5					A	ADC
F6	ADC4	ADC4					A	ADC
F7	VSS	VSS					DG	
F8	VDD	VDD					DP	
F9	VCC_0	VCC_0					DP	IO0
F10	EMMC_D0/I2S1B_SDO/UART2C_CTS/GPIO0_A3	GPIO0_A3	EMMC_D0	I2S1B_SDO	UART2C_CTS	up	I/O	IO0
F11	EMMC_D1/I2S1B_SDI/UART2C_RTS/GPIO0_A4	GPIO0_A4	EMMC_D1	I2S1B_SDI	UART2C_RTS	up	I/O	IO0
G1	I2S1A_CLK/EBC_GDRL/GPIO1_A0	GPIO1_A0	I2S1A_CLK	EBC_GDRL		down	I/O	IO2
G2	SDMMC_D3/I2C1B_SDA/UART5_RX/GPIO1_B2	GPIO1_B2	SDMMC_D3	I2C1B_SDA	UART5_RX	up	I/O	IO2
G3	SDMMC_D0/SPI1A_RX/UART4_TX/GPIO1_A7	GPIO1_A7	SDMMC_D0	SPI1A_RX	UART4_TX	up	I/O	IO2
G4	VCC_2	VCC_2					DP	IO2
G5	ADC3	ADC3					A	ADC
G6	ADC6	ADC6					A	ADC
G7	ADC7	ADC7					A	ADC
G8	ADC_VSS	ADC_VSS					AG	ADC

Ball	Ball_Name	Fountion0	Fountion1	Fountion2	Fountion3	Pull②	Pintypes①	Power Domain③
G9	ADC_REF_OUT	ADC_REF_OUT					A	ADC
G10	EMMC_CMD/I2S1B_SCLK/UART2C_RX/GPIO0_A2	GPIO0_A2	EMMC_CMD	I2S1B_SCLK	UART2C_RX	up	I/O	IO0
G11	EMMC_CLK/I2S1B_LRCK/UART2C_TX/GPIO0_A1	GPIO0_A1	EMMC_CLK	I2S1B_LRCK	UART2C_TX	down	I/O	IO0
H1	I2S1A_SCLK/UART1B_TX/EBC_SDCE2/GPIO1_A2	GPIO1_A2	I2S1A_SCLK	UART1B_TX	EBC_SDCE2	down	I/O	IO2
H2	IO_TEST	IO_TEST					I	IO2
H3	VDD	VDD					DG	
H4	VCC_2	VCC_2					DP	IO2
H5	ADC1	ADC1					A	ADC
H6	ADC0	ADC0					A	ADC
H7	ADC2	ADC2					A	ADC
H8	ADC_VCC33	ADC_VCC33					AP	ADC
H9	ADC_VREF	ADC_VREF					A	ADC
H10	EMMC_PWREN/I2S1B_CLK/GPIO0_A0	GPIO0_A0	EMMC_PWREN	I2S1B_CLK		down	I/O	IO0
H11	EMMC_RSTN/GPIO1_B3	GPIO1_B3	EMMC_RSTN			down	I/O	IO0
J1	I2S1A_SDI/UART1B_RTS/EBC_SDCE4/GPIO1_A4	GPIO1_A4	I2S1A_SDI	UART1B_RTS	EBC_SDCE4	down	I/O	IO2
J2	I2S1A_SDO/UART1B_CTS/EBC_SDCE1/GPIO1_A3	GPIO1_A3	I2S1A_SDO	UART1B_CTS	EBC_SDCE1	down	I/O	IO2
J3	I2S1A_LRCK/UART1B_RX/EBC_SDSHR/GPIO1_A1	GPIO1_A1	I2S1A_LRCK	UART1B_RX	EBC_SDSHR	down	I/O	IO2
J4	VSS	VSS					DG	
J5	USB_VSSA	USB_VSSA					AG	USB
J6	MICBIAS_R	MICBIAS_R					A	ACODEC
J7	MICBIAS_L	MICBIAS_L					A	ACODEC
J8	AVSS	AVSS					AG	ACODEC
J9	AVDD	AVDD					AP	ACODEC
J10	IN2L	IN2L					A	ACODEC
J11	IN1R	IN1R					A	ACODEC
K1	USB_EXTR	USB_EXTR					A	USB
K2	AVSS_IO	AVSS_IO					AG	USB
K3	VDD	VDD					DP	IO
K4	VBUS	VBUS					I	USB
K5	AVDD_IO/USB_VCC33	AVDD_IO	USB_VCC33				AP	USB
K6	HPR_OUT	HPR_OUT					A	ACODEC
K7	HP_SENSE	HP_SENSE					A	ACODEC
K8	MIC1P	MIC1P					A	ACODEC
K9	MIC2P	MIC2P					A	ACODEC
K10	IN2R	IN2R					A	ACODEC
K11	IN1L	IN1L					A	ACODEC
L1	USB_DM	USB_DM	UART0B_RX				A	USB
L2	USB_DP	USB_DP	UART0B_TX				A	USB
L3	USB_VDD12	USB_VDD12					AP	USB
L4	USB_ID	USB_ID					I	USB
L5	HPL_OUT	HPL_OUT					A	ACODEC
L6	HP_VGND	HP_VGND					A	ACODEC
L7	MIC1N	MIC1N					A	ACODEC
L8	MIC2N	MIC2N					A	ACODEC
L9	LINEOUT_R	LINEOUT_R					A	ACODEC
L10	LINEOUT_L	LINEOUT_L					A	ACODEC
L11	VREF	VREF					A	

Note:

①:Pintypes: I = input, O = output, I/O = input/output (bidirectional),
AP = Analog Power, AG = Analog Ground
DP = Digital Power, DG = Digital Ground
A = Analog
②: The pull up/pull down can be disabled.
③:Power domain
PMU: power supply for PMU(always on logic), the GPIOs of this power domain can wake up system
from sleep mode
PLL: power supply for PLL
USB: power supply for USB and ACODEC IO
ACODEC: power supply for ACODEC core
ADC: power supply for ADC
IO0: power supply from VCC_0
IO1: power supply from VCC_1
IO2: power supply from VCC_2

Table 2-3 RKNanoD-G ball map

	1	2	3	4	5	6	7	8	9	10	11
A	POWERHOLD	PLAYON	PWM0	UART1A_CTS	PWM3	I2C1A_SDA	UART2A_TX	LCD_D7	LCD_D4	LCD_D1	LCD_D0
B	PWM1	RESET	UART1A_RTS	PWM2	PWM4	UART2A_RTS	UART2A_RX	LCD_CSN	LCD_WRN	LCD_D5	LCD_D2
C	UART0A_TX	UART0A_RX	PMU_IDLE	VCC_PMU0	I2C1A_SCL	UART2A_CTS	VDD	LCD_RS	LCD_D6	EMMC_D4	LCD_D3
D	XIN24M	UART1A_TX	UART1A_RX	VDD_PMU	I2C0A_SCL	VSS	VCC_1	VSS	EMMC_D2	EMMC_D5	EMMC_D6
E	VDD_PLL	XOUT24M	PMUTEST	SDMMC_CMD	I2C0A_SDA	VSS	VSS	VSS	VCC_0	EMMC_D3	EMMC_D7
F	VCC_PLL	SDMMC_D1	SDMMC_D2	SDMMC_CLK	ADC5	ADC4	VSS	VDD	VCC_0	EMMC_D0	EMMC_D1
G	I2S1A_CLK	SDMMC_D3	SDMMC_D0	VCC_2	ADC3	ADC6	ADC7	ADC_VSS	ADC_REF_OUT	EMMC_CMD	EMMC_CLK
H	I2S1A_SCLK	TEST_PAD	VDD	VCC_2	ADC1	ADC0	ADC2	ADC_VCC33	ADC_VREF	EMMC_PWR_EN	EMMC_RSTN
J	I2S1A_SDI	I2S1A_SDO	I2S1A_LRCK	VSS	USB_VSSA	MICBIAS_R	MICBIAS_L	AVSS	AVDD	IN2L	IN1R
K	USB_EXTR	AVSS_IO	VDD	VBUS	AVDD_IO/USB_VCC33	HPR_OUT	HP_SENSE	MIC1P	MIC2P	IN2R	IN1L
L	USB_DM	USB_DP	USB_VDD12	USB_ID	HPL_OUT	HP_VGND	MIC1N	MIC2N	LINEOUT_R	LINEOUT_L	VREF

2.4.3 RKNanoD-L pin Description

Pin	PIN_Name	Fountion0	Fountion 1	Fountion2	Fountion 3	Pull	Pin_types	Power
1	I2C2C_SDA/JTG0_TRST/POWERHOLD/GPIOP2_A6	GPIOP2_A6	I2C2C_SDA	JTG0_TRST	POWERHOLD	down	I/O	PMU
2	UART0A_TX/JTG1_TCK/I2C1C_SCL/GPIOP2_B5	GPIOP2_B5	UART0A_TX	JTG1_TCK	I2C1C_SCL	up	I/O	PMU
3	UART0A_RX/JTG1_TMS/I2C1C_SDA/GPIOP2_B4	GPIOP2_B4	UART0A_RX	JTG1_TMS	I2C1C_SDA	up	I/O	PMU
4	UART1A_RX/I2C0B_SCL/SPI1B_TX/GPIOP2_C1	GPIOP2_C1	UART1A_RX	I2C0B_SCL	SPI1B_TX	up	I/O	PMU
5	UART1A_TX/I2C0B_SDA/SPI1B_CLK/GPIOP2_C0	GPIOP2_C0	UART1A_TX	I2C0B_SDA	SPI1B_CLK	up	I/O	PMU
6	VDD_PMU	VDD_PMU					DP	PMU
7	VSS	VSS					DG	
8	XOUT24M	XOUT24M					I	PMU
9	XIN24M	XIN24M					I	PMU
10	VDD_PLL	VDD_PLL					AP	PLL
11	VSS	VSS					DG	
12	VCC_PLL	VCC_PLL					DP	PLL
13	VSS	VSS					DG	
14	VCC_2	VCC_2					DP	IO2
15	VDD	VDD					DP	
16	VSS	VSS					DG	
17	SDMMC_CMD/SPI1A_CS/UART3_TX/GPIO1_A5	GPIO1_A5	SDMMC_CMD	SPI1A_CS	UART3_TX	up	I/O	IO2
18	SDMMC_CLK/SPI1A_CLK/UART3_RX/GPIO1_A6	GPIO1_A6	SDMMC_CLK	SPI1A_CLK	UART3_RX	up	I/O	IO2
19	VSS	VSS					DG	
20	VDD	VDD					DP	
21	SDMMC_D0/SPI1A_RX/UART4_TX/GPIO1_A7	GPIO1_A7	SDMMC_D0	SPI1A_RX	UART4_TX	up	I/O	IO2
22	SDMMC_D1/SPI1A_TX/UART4_RX/GPIO1_B0	GPIO1_B0	SDMMC_D1	SPI1A_TX	UART4_RX	up	I/O	IO2
23	VSS	VSS					DG	
24	VCC_2	VCC_2					DP	IO2
25	SDMMC_D2/I2C1B_SCL/UART5_TX/GPIO1_B1	GPIO1_B1	SDMMC_D2	I2C1B_SCL	UART5_TX	up	I/O	IO2
26	SDMMC_D3/I2C1B_SDA/UART5_RX/GPIO1_B2	GPIO1_B2	SDMMC_D3	I2C1B_SDA	UART5_RX	up	I/O	IO2
27	I2S1A_CLK/EBC_GDRL/GPIO1_A0	GPIO1_A0	I2S1A_CLK	EBC_GDRL		down	I/O	IO2
28	IO_TEST	IO_TEST					I	IO2
29	I2S1A_LRCK/UART1B_RX/EBC_SDSHR/GPIO1_A1	GPIO1_A1	I2S1A_LRCK	UART1B_RX	EBC_SDSHR	down	I/O	IO2
30	I2S1A_SCLK/UART1B_TX/EBC_SDCE2/GPIO1_A2	GPIO1_A2	I2S1A_SCLK	UART1B_TX	EBC_SDCE2	down	I/O	IO2
31	I2S1A_SDO/UART1B_CTS/EBC_SDCE1/GPIO1_A3	GPIO1_A3	I2S1A_SDO	UART1B_CTS	EBC_SDCE1	down	I/O	IO2
32	I2S1A_SDI/UART1B_RTS/EBC_SDCE4/GPIO1_A4	GPIO1_A4	I2S1A_SDI	UART1B_RTS	EBC_SDCE4	down	I/O	IO2
33	VDD	VDD					DP	
34	VSS	VSS					DG	
35	VCC_2	VCC_2					DP	IO2
36	USB_DM	USB_DM	UART0B_RX				A	USB
37	USB_DP	USB_DP	UART0B_TX				A	USB
38	USB_ID	USB_ID					I	USB
39	VBUS	VBUS					I	USB
40	AVDD_IO/USB_VCC33	AVDD_IO	USB_VCC33				AP	USB
41	USB_VSSA	USB_VSSA					AG	USB
42	USB_VDD12	USB_VDD12					AP	USB

Pin	PIN_Name	Fountion0	Fountion 1	Fountio n2	Fountion 3	Pull	Pin_ types	Power
43	USB_EXTR	USB_EXTR					A	USB
44	AVDD_IO/USB_VCC33	AVDD_IO	USB_VCC 33				AP	USB
45	AVSS_IO	AVSS_IO					AG	USB
46	HPL_OUT	HPL_OUT					A	ACODEC
47	HP_SENSE	HP_SENSE					A	ACODEC
48	HP_VGND	HP_VGND					A	ACODEC
49	HPR_OUT	HPR_OUT					A	ACODEC
50	LINEOUT_L	LINEOUT_L					A	ACODEC
51	LINEOUT_R	LINEOUT_R					A	ACODEC
52	VREF	VREF					A	ACODEC
53	MICBIAS_L	MICBIAS_L					A	ACODEC
54	MIC1N	MIC1N					A	ACODEC
55	MIC1P	MIC1P					A	ACODEC
56	IN1R	IN1R					A	ACODEC
57	MIC2N	MIC2N					A	ACODEC
58	MIC2P	MIC2P					A	ACODEC
59	IN1L	IN1L					A	ACODEC
60	IN2R	IN2R					A	ACODEC
61	IN2L	IN2L					A	ACODEC
62	AVSS	AVSS					AG	ACODEC
63	AVDD	AVDD					AP	ACODEC
64	ADC_REF_OUT	ADC_REF_O UT					A	ADC
65	ADC_VREF	ADC_VREF					A	ADC
66	ADC0	ADC0					A	ADC
67	ADC1	ADC1					A	ADC
68	ADC2	ADC2					A	ADC
69	ADC3	ADC3					A	ADC
70	ADC4	ADC4					A	ADC
71	ADC5	ADC5					A	ADC
72	ADC_VSS	ADC_VSS					AG	ADC
73	ADC_VCC33	ADC_VCC33					AP	ADC
74	VSS	VSS					DG	
75	VDD	VDD					DP	
76	VSS	VSS					DG	
77	VCC_0	VCC_0					DP	IO0
78	EMMC_PWREN/I2S1B_CLK/GPIO0_A0	GPIO0_A0	EMMC_PW REN	I2S1B_CL K		dow n	I/O	IO0
79	EMMC_CLK/I2S1B_LRCK/UART2C_TX/GPIO0_A1	GPIO0_A1	EMMC_CL K	I2S1B_LR CK	UART2C_T X	dow n	I/O	IO0
80	EMMC_CMD/I2S1B_SCLK/UART2C_RX/GPIO0_A2	GPIO0_A2	EMMC_CM D	I2S1B_SC LK	UART2C_R X	up	I/O	IO0
81	EMMC_D0/I2S1B_SDO/UART2C_CTS/GPIO0_A3	GPIO0_A3	EMMC_D0	I2S1B_SD O	UART2C_C TS	up	I/O	IO0
82	EMMC_D1/I2S1B_SDI/UART2C_RTS/GPIO0_A4	GPIO0_A4	EMMC_D1	I2S1B_SD I	UART2C_R TS	up	I/O	IO0
83	VSS	VSS					DG	
84	VDD	VDD					DP	
85	EMMC_D2/SFC_D3/I2C0C_SDA/GPIO0_A5	GPIO0_A5	EMMC_D2	SFC_D3	I2C0C_SD A	up	I/O	IO0
86	EMMC_D3/SFC_D2/I2C0C_SCL/GPIO0_A6	GPIO0_A6	EMMC_D3	SFC_D2	I2C0C_SC L	up	I/O	IO0
87	VSS	VSS					DG	
88	VCC_0	VCC_0					DP	IO0
89	EMMC_D4/SFC_D1/GPIO0_A7	GPIO0_A7	EMMC_D4	SFC_D1		up	I/O	IO0

Pin	PIN_Name	Fountion0	Fountion 1	Fountio n2	Fountion 3	Pull	Pin_ types	Power
90	EMMC_D5/SFC_D0/JTG1_TDI/GPIO 0_B0	GPIO0_B0	EMMC_D5	SFC_D0	JTG1_TDI	up	I/O	IO0
91	EMMC_D6/SFC_CLK/JTG1_TDO/GP IO0_B1	GPIO0_B1	EMMC_D6	SFC_CLK	JTG1_TDO	up	I/O	IO0
92	EMMC_D7/SFC_CS/JTG1_TRST/GPI O0_B2	GPIO0_B2	EMMC_D7	SFC_CS	JTG1_TRS T	up	I/O	IO0
93	VDD	VDD					DP	
94	VSS	VSS					DG	
95	VDD	VDD					DP	
96	VCC_1	VCC_1					DP	IO1
97	LCD_D0/SPI0A_TX/EBC_SDDO0/G PIO0_C0	GPIO0_C0	LCD_D0	SPI0A_TX	EBC_SDD O0	up	I/O	IO1
98	LCD_D1/SPI0A_RX/EBC_SDDO1/G PIO0_C1	GPIO0_C1	LCD_D1	SPI0A_RX	EBC_SDD O1	up	I/O	IO1
99	LCD_D2/SPI0A_CLK/EBC_SDDO2/ GPIO0_C2	GPIO0_C2	LCD_D2	SPI0A_CL K	EBC_SDD O2	up	I/O	IO1
100	LCD_D3/SPI0A_CS/EBC_SDDO3/G PIO0_C3	GPIO0_C3	LCD_D3	SPI0A_CS	EBC_SDD O3	up	I/O	IO1
101	LCD_D4/UART2B_RX/EBC_SDDO4/ GPIO0_C4	GPIO0_C4	LCD_D4	UART2B_ RX	EBC_SDD O4	up	I/O	IO1
102	LCD_D5/UART2B_TX/EBC_SDDO5/ GPIO0_C5	GPIO0_C5	LCD_D5	UART2B_ TX	EBC_SDD O5	up	I/O	IO1
103	LCD_D6/UART2B_RTS/EBC_SDDO 6/GPIO0_C6	GPIO0_C6	LCD_D6	UART2B_ RTS	EBC_SDD O6	up	I/O	IO1
104	LCD_D7/UART2B_CTS/EBC_SDDO 7/GPIO0_C7	GPIO0_C7	LCD_D7	UART2B_ CTS	EBC_SDD O7	up	I/O	IO1
105	LCD_WRN/I2C2B_SCL/EBC_SDLE/ GPIO0_D0	GPIO0_D0	LCD_WRN	I2C2B_SC L	EBC_SDLE	up	I/O	IO1
106	LCD_RS/I2C2B_SDA/EBC_SDOE/G PIO0_D1	GPIO0_D1	LCD_RS	I2C2B_SD A	EBC_SDOE	up	I/O	IO1
107	VDD	VDD					DP	
108	LCD_CSN/I2S0_CLK/EBC_GDOE/G PIO0_B7	GPIO0_B7	LCD_CSN	I2S0_CLK	EBC_GDO E	up	I/O	IO1
109	UART2A_TX/I2S0_LRCK/EBC_GDS P/GPIO0_B6	GPIO0_B6	UART2A_T X	I2S0_LRC K	EBC_GDSP	up	I/O	IO1
110	UART2A_RX/I2S0_SCLK/EBC_GDC LK/GPIO0_B5	GPIO0_B5	UART2A_R X	I2S0_SCL K	EBC_GDCL K	up	I/O	IO1
111	UART2A_CTS/I2S0_SDO/EBC_SDC LK/GPIO0_B4	GPIO0_B4	UART2A_C TS	I2S0_SDO	EBC_SDCL K	up	I/O	IO1
112	UART2A_RTS/I2S0_SDI/EBC_VCO M/GPIO0_B3	GPIO0_B3	UART2A_R TS	I2S0_SDI	EBC_VCO M	up	I/O	IO1
113	VCC_1	VCC_1					DP	IO1
114	I2C1A_SDA/SPI0B_CS/EBC_SDCE3 /GPIOP2_B0	GPIOP2_B0	I2C1A_SD A	SPI0B_CS	EBC_SDCE 3	up	I/O	PMU
115	I2C1A_SCL/SPI0B_CLK/EBC_BORD ER1/GPIOP2_B1	GPIOP2_B1	I2C1A_SC L	SPI0B_CL K	EBC_BORD ER1	up	I/O	PMU
116	I2C0A_SCL/SPI0B_TX/EBC_SDCE5 /GPIOP2_B2	GPIOP2_B2	I2C0A_SC L	SPI0B_TX	EBC_SDCE 5	up	I/O	PMU
117	I2C0A_SDA/SPI0B_RX/EBC_BORD ER0/GPIOP2_B3	GPIOP2_B3	I2C0A_SD A	SPI0B_RX	EBC_BORD ER0	up	I/O	PMU
118	PWM4/I2C2A_SDA/EBC_GDPWR0/ GPIOP2_A0	GPIOP2_A0	PWM4	I2C2A_SD A	EBC_GDP WR0	up	I/O	PMU
119	PWM3/I2C2A_SCL/EBC_SDCE0/GP IOP2_A1	GPIOP2_A1	PWM3	I2C2A_SC L	EBC_SDCE 0	up	I/O	PMU
120	PWM2/EBC_GDPWR2/PMU_ST3/GP IOP2_A2	GPIOP2_A2	PWM2	EBC_GDP WR2	PMU_ST3	dow n	I/O	PMU
121	PMU_IDLE/GPIOP2_A7	GPIOP2_A7	PMU_IDLE			dow n	I/O	PMU
122	VCC_PMU	VCC_PMU					DP	PMU
123	UART1A_RTS/JTG0_TMS/SPI1B_CS /GPIOP2_B6	GPIOP2_B6	UART1A_R TS	JTG0_TMS	SPI1B_CS	up	I/O	PMU
124	UART1A_CTS/JTG0_TCK/SPI1B_RX /GPIOP2_B7	GPIOP2_B7	UART1A_C TS	JTG0_TCK	SPI1B_RX	up	I/O	PMU
125	RESET	RESET				dow n	I	PMU
126	PWM1/CLK_OBS/EBC_GDPWR1/GP IOP2_A3	GPIOP2_A3	PWM1	CLK_OBS	EBC_GDP WR1	up	I/O	PMU
127	PWM0/JTG0_TDI/PMU_ST2/GPIOP2 _A4	GPIOP2_A4	PWM0	JTG0_TDI	PMU_ST2	dow n	I/O	PMU
128	I2C2C_SCL/JTG0_TDO/PLAYON/GP IOP2_A5	GPIOP2_A5	I2C2C_SC L	JTG0_TD O	PLAYON	dow n	I/O	PMU

Note:

①:Pintypes: I = input, O = output, I/O = input/output (bidirectional),
AP = Analog Power, AG = Analog Ground
DP = Digital Power, DG = Digital Ground
A = Analog

②: The pull up/pull down can be disabled.

***③:** POWERHOLD and PLAYON are defined by software.*

④: Power domain
IO: power supply for system and logic
PLL: power supply for PLL
USB: power supply for USB and ACODEC IO
ACODEC: power supply for ACODEC core

2.5 RKNanoD Power/ground IO descriptions

Table 2-4 RKNanoD-N Power/Ground IO information

Pin Name	Pin Number	Descriptions
VDD	4,16,50,61	Internal core Power
VCC	9,38,62	Digital IO Power Supply
VDD_PLL	7	PLL Analog Power Supply
VCC_PLL	8	PLL Analog Power Supply
USB_VDD12	20	USB Analog Power Supply
AVDD_IO/USB_VCC33	22	Codec and USB Analog Power Supply
AVSS_IO	23	Codec and USB Analog Ground
AVDD	35	Codec Analog Power Supply
AVSS	34	Codec and USB Analog Ground
GND	69	Digital Ground

Table 2-5 RKNanoD-L Power/Ground IO information

Pin Name	Pin Number	Descriptions
VDD	6,15,20,33,75,84,93,95,107	Internal core Power
VCC	14,24,35,73,96,113	Digital IO Power Supply
VDD_PLL	10	PLL Analog Power Supply
VCC_PLL	12	PLL Analog Power Supply
USB_VDD12	42	USB Analog Power Supply
AVDD_IO/USB_VCC33	44	Codec and USB Analog Power Supply
AVSS_IO	45	Codec and USB Analog Ground
AVDD	63	Codec Analog Power Supply
AVSS	62	Codec and USB Analog Ground
GND	7,13,16,19,23,34,74,76,83,87,94	Digital Ground

Table 2-6 RKNanoD-G Power/Ground IO information

Ball Name	Ball Number	Descriptions
VDD	C7,F8,H3,K3	Internal core Power
VCC_0	E9,F9	Digital IO Power Supply
VCC_1	D7	Digital IO Power Supply
VCC_2	G4,H4	Digital IO Power Supply
VDD_PMU	D4	PMU Domain Logic Power Supply

VCC_PMU	C4	PMU Domain IO Power Supply
VDD_PLL	E1	PLL Analog Power Supply
VCC_PLL	F1	PLL Analog Power Supply
ADC_VCC33	H8	SARADC Analog Power Supply
ADC_VSS	G8	SARADC Analog Power Ground
Ball Name	**Ball Number**	**Descriptions**
AVDD	J9	Codec Analog Power Supply
AVSS	J8	Codec Analog Power Ground
USB_VDD12	L3	USB Analog Power Supply
USB_VSSA	J5	USB Analog Ground
AVDD_IO/USB_VCC33	K5	Codec and USB Analog Power Supply
AVSS_IO	K2	Codec and USB Analog Power Ground
VSS	D6,D8,E6,E7,E8,F7,J4	Digital Power Ground

2.6 IO pin name descriptions

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 2-7 RKNanoD IO function description list

Interface	Pin Name	Direction	Description
Misc	XIN24M	I	Clock input of 24MHz crystal
	XOUT24M	O	Clock output of 24MHz crystal
	RESET	I	Chip hardware reset
	CLK_OBS	O	Clock select output
	PMU_IDLE	O	PMU idle signal output
	PMU_TEST	I	Test pin
	IO_TEST	I	Test pin

Interface	Pin Name	Direction	Description
JTAG0	JTG0_TRST	I	JTAG0 interface reset input
	JTG0_TCK	I	JTAG0 interface clock input/SWD interface clock input
	JTG0_TDI	I	JTAG0 interface TDI input
	JTG0_TMS	I/O	JTAG0 interface TMS input/SWD interface data out
	JTG0_TDO	O	JTAG0 interface TDO output

Interface	Pin Name	Direction	Description
JTAG1	JTG1_TRST	I	JTAG1 interface reset input
	JTG1_TCK	I	JTAG1 interface clock input/SWD interface clock input
	JTG1_TDI	I	JTAG1 interface TDI input
	JTG1_TMS	I/O	JTAG1 interface TMS input/SWD interface data out
	JTG1_TDO	O	JTAG1 interface TDO output

Interface	Pin Name	Direction	Description
eMMC Interface	EMMC_CLK	O	emmcflash clock.
	EMMC_CMD	I/O	emmcflash command output and response input.
	EMMC_Di (i=0~7)	I/O	emmcflash data input and output.
	EMMC_PWREN	O	emmcflash power-enable control signal
	EMMC_RSTN	O	emmcflash reset signal

Interface	Pin Name	Direction	Description
SDMMC Host Controller	SDMMC_CLK	O	sdmmc card clock.
	SDMMC_CMD	I/O	sdmmc card command output and responseinput.
	SDMMC_Di (i=0~3)	I/O	sdmmc card data input and output.

Interface	Pin Name	Direction	Description
SFC Host Controller	SFC_CS	O	Serial flash chip select
	SFC_CLK	O	Serial flash clock output
	SFC_Di (i=0~3)	I/O	Serial flash data input/output

Interface	Pin Name	Direction	Description
LCDC	LCD_Di (i=0~7)	O	LCDC i8080 interface data output
	LCD_WRN	O	LCDC i8080 interface write enable
	LCD_RS	O	LCDC i8080 interface command/data signal
	LCD_CSN	O	LCDC i8080 interface chip select

Interface	Pin Name	Direction	Description
EBC	EBC_SDCLK	O	EPD source clock
	EBC_SDLE	O	EPD latch pulse
	EBC_SDOE	O	EPD source data output enable
	EBC_SDECi (i=0~5)	O	EPD source data shift enable
	EBC_SDDOi (i=0~7)	O	EPD source data
	EBC_SDSHR	O	EPD source scan direction
	EBC_GDCLK	O	EPD gate clock
	EBC_GDOE	O	EPD gate output mode
	EBC_GDSP	O	EPD gate start pulse
	EBC_GDRL	O	EPD gate scan direction
	EBC_VCOM	O	EPD com voltage enable
	EBC_BORDERi (i=0,1)	O	EPD border output signal
	EBC_GDPWRi (i=0~2)	O	EPD power control signal

Interface	Pin Name	Direction	Description
SPI Interface	SPI0A_CLK	I/O	Spi0 port A serial clock
	SPI0A_CS	I/O	spi0 port A chip select signal,low active
	SPI0A_TX	O	spi0 port A serial data output
	SPI0A_RX	I	spi0 port A serial data input
	SPI0B_CLK	I/O	Spi0 port B serial clock
	SPI0B_CS	I/O	spi0 port B chip select signal,low active
	SPI0B_TX	O	spi0 port B serial data output
	SPI0B_RX	I	spi0 port B serial data input
	SPI1A_CLK	I/O	Spi1 port A serial clock
	SPI1A_CS	I/O	Spi1 port A chip select signal,low active
	SPI1A_TX	O	Spi1 port A serial data output
	SPI1A_RX	I	Spi1 port A serial data input
	SPI1B_CLK	I/O	Spi1 port B serial clock
	SPI1B_CS	I/O	Spi1 port B chip select signal, low active
	SPI1B_TX	O	Spi1 port B serial data output
	SPI1B_RX	I	Spi1 port B serial data input

Interface	Pin Name	Direction	Description
I2C master	I2C0A_SDA	I/O	I2C0 port A_ data
	I2C0A_SCL	O	I2C0 portAclock
	I2C0B_SDA	I/O	I2C0 port B_ data
	I2C0B_SCL	O	I2C0 portBclock
	I2C0C_SDA	I/O	I2C0 port C_ data
	I2C0C_SCL	O	I2C0 portCclock
	I2C1A_SDA	I/O	I2C1 port A_ data
	I2C1A_SCL	O	I2C1 portAclock
	I2C1B_SDA	I/O	I2C1 port B_ data
	I2C1B_SCL	O	I2C1 portBclock
	I2C1C_SDA	I/O	I2C1 port C_ data
	I2C1C_SCL	O	I2C1 portCclock
	I2C2A_SDA	I/O	I2C2 port A_ data
	I2C2A_SCL	O	I2C2portA clock
	I2C2B_SDA	I/O	I2C2 port B_ data
	I2C2B_SCL	O	I2C2 portBclock
	I2C2C_SDA	I/O	I2C2 port C_ data
	I2C2C_SCL	O	I2C2 portCclock

Interface	Pin Name	Direction	Description
UART	UART0A_RX	I	UART0 port Aserial data input

Interface	Pin Name	Direction	Description
	UART0A_TX	O	UART0 port A serial data output
	UART0B_RX	I	UART0 port Bserial data input
	UART0B_TX	O	UART0 port B serial data output
	UART1A_RX	I	UART1 port Aserial data input
	UART1A_TX	O	UART1 port A serial data output
	UART1A_CTS	O	UART1 port A clear to send
	UART1A_RTS	I	UART1 port A request to send
	UART1B_RX	I	UART1 port Bserial data input
	UART1B_TX	O	UART1 port B serial data output
	UART1B_CTS	O	UART1 port B clear to send
	UART1B_RTS	I	UART1 port B request to send
	UART2A_RX	I	UART2 port Aserial data input
	UART2A_TX	O	UART2 port A serial data output
	UART2A_CTS	O	UART2 port A clear to send
	UART2A_RTS	I	UART2 port A request to send
	UART2B_RX	I	UART2 port Bserial data input
	UART2B_TX	O	UART2 port B serial data output
	UART2B_CTS	O	UART2 port C clear to send
	UART2B_RTS	I	UART2 port C request to send
	UART2C_RX	I	UART2 port Cserial data input
	UART2C_TX	O	UART2 port C serial data output
	UART2C_CTS	O	UART2 port C clear to send
	UART2C_RTS	I	UART2 port C request to send
	UART3_RX	I	UART3serial data input
	UART3_TX	O	UART3 serial data output
	UART4_RX	I	UART4serial data input
	UART4_TX	O	UART4 serial data output
	UART5_RX	I	UART5serial data input
	UART5_TX	O	UART5 serial data output

Interface	Pin Name	Direction	Description
I2S Controller	I2S0_CLK	O	I2S0 clock source
	I2S0_SCLK	I/O	I2S0 serial clock
	I2S0_LRCK	I/O	I2S0 left & right channel signal for serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	I2S0_SDI	I	I2S0 serial data input
	I2S0_SDO	O	I2S0 serial data output
	I2S1A_CLK	O	I2S1port A clock source
	I2S1A_SCLK	I/O	I2S1port A serial clock
	I2S1A_LRCK	I/O	I2S1port A left & right channel signal for serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	I2S1A_SDI	I	I2S1port A serial data input

Interface	Pin Name	Direction	Description
	I2S1A_SDO	O	I2S1port A serial data output
	I2S1B_CLK	O	I2S1port B clock source
	I2S1B_SCLK	I/O	I2S1port B serial clock
	I2S1B_LRCK	I/O	I2S1port B left & right channel signal for serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	I2S1B_SDI	I	I2S1port B serial data input
	I2S1B_SDO	O	I2S1port B serial data output

Interface	Pin Name	Direction	Description
PWM	PWM4	O	Pulse Width Modulation output
	PWM3	O	Pulse Width Modulation output
	PWM2	O	Pulse Width Modulation output
	PWM1	O	Pulse Width Modulation output
	PWM0	O	Pulse Width Modulation output

Interface	Pin Name	Direction	Description
SAR-ADC	ADC_REF_OUT	O	SAR-ADC reference voltage output
	ADC_VREF	I	SAR-ADC reference voltage input
	SARADC_AIN[i] (i=0~7)	I	SAR-ADC input signal for 8channel

Interface	Pin Name	Direction	Description
ACODEC	HP_SENSE	I	The HP ground signal sense pin
	HPL_OUT	O	The HP left channel output pin
	HP_VGND	O	The HP virtual ground pin
	HPR_OUT	O	The HP right channel output pin
	LINEOUT_L	O	The Lineout Left channel output pin
	LINEOUT_R	O	The Lineout Right channel output pin
	VREF	O	The Codec IP reference voltage pin, should connect 1uf cap for stable
	MICBIAS_L	O	The Mic-phone left channel bias voltage pin
	MICBIAS_R	O	The Mic-phone right channel bias voltage pin
	MIC1P	I	The Mic-phone 1 differential input plus pin
	MIC1N	I	The Mic-phone 1 differential input minus pin
	IN1L	I	The Line-in 1 left channel input pin
	IN2L	I	The Line-in 2 left channel input pin

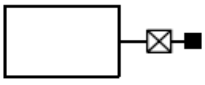
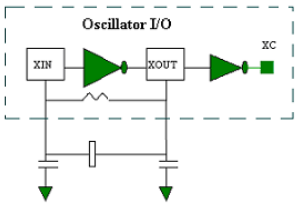
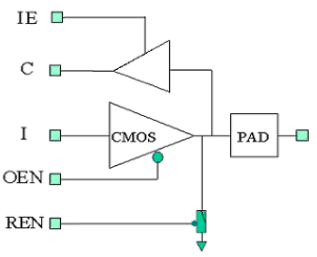
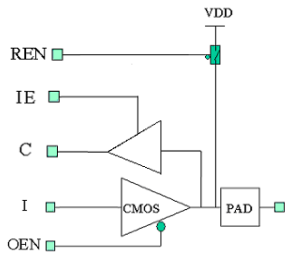
	MIC2N	I	The Mic-phone 2 differential input minus pin
	MIC2P	I	The Mic-phone 2 differential input plus pin
	IN1R	I	The Line-in 1 right channel input pin
	IN2R	I	The Line-in 2 right channel input pin

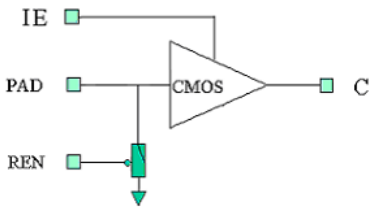
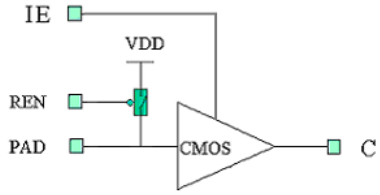
Interface	Pin Name	Direction	Description
USB OTG 2.0	USB_DM	I/O	USB OTG 2.0 Data signal DM
	USB_EXTR	N/A	Reference external resistance
	USB_DP	I/O	USB OTG 2.0 Data signal DP
	VBUS	N/A	USB OTG 2.0 5V power supply pin
	USB_ID	I	USB OTG 2.0 ID indicator

2.7 IO Type

The following list shows IO type except Power/Ground IO.

Table 2-8 RKNanoD IO Type List

Type	Diagram	Description	Pin Name
A		Dedicated Power supply to Internal Macro with IO voltage	SARADC_AIN[2:0]
B		Crystal Oscillator with internal register	XIN24M/XOUT24M
C		CMOS 3-state output pad with controllable input and controllable pull-down	Part of digital GPIO (PBCDxRN)
D		CMOS 3-state output pad with controllable input and controllable pull-up	Part of digital GPIO (PBCUxRN)

Type	Diagram	Description	Pin Name
E		controllable input pad with controllable pull-down	Part of digital GPIO (PICDRN)
F		controllable input pad with controllable pull-up	Part of digital GPIO (PICURN)

Chapter 3 Electrical Specification

3.1 Absolute Maximum Ratings

Table 3-1 RKNanoD absolute maximum ratings

Parameters	Max①	Unit
DC supply voltage for Internal digital logic	1.32	V
DC supply voltage for Digital GPIO(except for SAR-ADC, PLL, USB)	3.6	V
DC supply voltage for Analog part of SAR-ADC	3.6	V
DC supply voltage for Analog part of PLL	3.63	V
DC supply voltage for Analog part of USB OTG	3.63	V
Analog Input voltage for SAR-ADC	2.75	V
Analog Input voltage for DP/DM/VBUS of USB OTG	5	V
Digital input voltage for input buffer of GPIO	3.6	V
Digital output voltage for output buffer of GPIO	3.6	V
Storage Temperature	125	℃
Max Conjunction Temperature	125	℃

Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

3.2 Recommended Operating Conditions

Table 3-2 RKNanoD recommended operating conditions①

Parameters	Min	Typ	Max	Units
Internal digital logic Power	1.08	1.2	1.32	V
Digital GPIO Power(3.3V)	2.97	3.3	3.6	V
Digital GPIO Power(1.8V)	1.62	1.8	1.98	V
PLL Analog Power	1.35	3.3	3.63	V
PLL Analog Power	1.08	1.2	1.32	V
SAR-ADC Analog Power	2.97	3.3	3.63	V
SAR-ADC external reference Power	0.2* SAR_AVDD33		0.9* SAR_AVDD33	
USB OTG Analog Power(3.3V)	2.97	3.3	3.63	V
USB OTG external resistor	40.5	45	49.5	Ohm
Acodec Analog Power	2.97	3.3	3.63	V
PLL input clock frequency	N/A	24	N/A	MHz
Ambient Operating Temperature ②	-10	25	85	℃

Note:

① Recommended operating conditions update with real test after chip arrived.
② with the reference software setup, the reference software will limit the chipset temperature about 85℃

3.3 DC Characteristics

Table 3-3 RKNanoD DC Characteristics

Parameters		Symbol	Min	Typ	Max	Units
	Input Low Voltage	Vil	-0.3	0	0.8	V

Parameters		Symbol	Min	Typ	Max	Units
Digital GPIO @3.3V	Input High Voltage	Vih	2	3.3	3.6	V
	Output Low Voltage	Vol	N/A	0	0.4	V
	Output High Voltage	Voh	2.4	3.3	N/A	V
	Threshold Point	Vt	1.21	1.42	1.64	V
	Schmitt trig Low to High threshold point	Vt+	1.36	1.6	1.86	V
	Schmitt trig High to Low threshold point	Vt-	0.93	1.09	1.3	V
	Pull-up Resistor	Rpu	33	41	62	Kohm
	Pull-down Resistor	Rpd	33	42	68	Kohm
Digital GPIO @1.8V	Input Low Voltage	Vil	-0.3	0	0.63	V
	Input High Voltage	Vih	1.17	1.8	2.1	V
	Output Low Voltage	Vol	N/A	0	0.45	V
	Output High Voltage	Voh	1.35	1.8	N/A	V
	Threshold Point	Vt	0.72	0.83	0.95	V
	Schmitt trig Low to High threshold point	Vt+	0.74	0.88	1.03	V
	Schmitt trig High to Low threshold point	Vt-	0.52	0.61	0.73	V
	Pull-up Resistor	Rpu	67	93	152	Kohm
	Pull-down Resistor	Rpd	64	92	170	Kohm
PLL	Input High Voltage	Vih_pll	0.8*DVDD_iPLL (i=A,D,CG)	DVDD_iPLL (i=A,D,CG)	DVDD_iPLL (i=A,D,CG)	V
	Input Low Voltage	Vil_pll	0	0	0.2*DVDD_iPLL (i=A,D,CG)	V

3.4 Electrical Characteristics for General IO

Table 3-4 RKNanoD Electrical Characteristics for Digital General IO

Parameters		Symbol	Test condition	Min	Typ	Max	Units
	Input leakage current	Il	Vin = 3.3V or 0V	-10	N/A	10	uA

Parameters		Symbol	Test condition	Min	Typ	Max	Units
Digital GPIO @3.3V	Tri-state output leakage current	Ioz	Vout = 3.3V or 0V	-10	N/A	10	uA
Digital GPIO @1.8V	Input leakage current	Ii	Vin = 1.8V or 0V	-10	N/A	10	uA
	Tri-state output leakage current	Ioz	Vout = 1.8V or 0V	-10	N/A	10	uA

3.5 Electrical Characteristics for PLL

Table 3-5 RKNanoD Electrical Characteristics for PLL

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Input clock frequency	Fin	Fin = FREF @3.3V/1.2V①	1/10	24	800	MHz
Comparison frequency	Fref	FREF = Fin/REFDIV @3.3V/1.2V	1	N/A	40	MHz
VCO operating range	Fvco	Fvco = Fref * FBDIV① @3.3V/1.2V	400	N/A	1600	MHz
Output clock frequency	Fout	Fout = Fvco/POSTDIV① @3.3V/1.2V	1	N/A	1600	MHz
Lock time②	Tlt	@ 3.3V/1.2V, FREF=24M,REFDIV=1	N/A	41.7	62.5	us
VDDHV Power consumption ③ (normal mode)	N/A	Fvco = 1000MHz, @3.3V, 25 ℃	N/A	1	1.2	mA
VDD Power consumption (normal mode)	N/A	@3.3V/1.2V, 25 ℃	N/A	3	4	uW/MHz
Power consumption (power-down mode)	N/A	PD=HIGH, @27 ℃	N/A	10	N/A	uA

Notes :

① REFDIV is the input divider value; FBDIV is the feedback div POSTDIV is the output divider value ider value;

② Lock Time is 1000cycles of input clocks in typ, and 1500cycles of input clocks in max.

③ Current scale as (Fvco/1GHz)1.5

3.6 Electrical Characteristics for SAR-ADC

Table 3-6 RKNanoD Electrical Characteristics for SAR-ADC

Parameters	Symbol	Test condition	Min	Typ	Max	Units
ADC resolution			N/A	10	N/A	bits
Input Range	CH[2:0]	3-channel single-ended input	0.01*SAR_AVDD33	N/A	0.99*SAR_AVDD33	V
Input Capacitance	CIN		N/A	1	N/A	pF
Sampling Clock			N/A	N/A	200	KHz
Main Clock Frequency	CLK		N/A	N/A	2.2	MHz
Data Latency			N/A	10	N/A	Clock Cycle
SNR plus Distortion(Up to 5th harmonic)	SINAD	Fin=10K Fin=99K	N/A	61.49 60.58	N/A	dB

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Spurious-Free Dynamic Range	SFDR	Fin=10K Fin=99K	N/A	66.29 67.14	N/A	dB
Second-Harmonic Distortion	2HD	Fin=10K Fin=99K	N/A	-72.64 -69.94	N/A	dB
Third-Harmonic Distortion	3HD	Fin=10K Fin=99K	N/A	-74.79 -68.85	N/A	dB
Effective Number of Bits	ENOB	Fin=10K Fin=99K	N/A	9.92 9.77	N/A	Bits
Positive Reference	VREF		0.5*SARADC_AVDD33		0.99*SARADC_AVDD33	V
Analog Supply Current(SARADC_VDDA)			N/A	278	N/A	uA
Digital Supply Current			N/A	10	N/A	uA
Reference Supply Current			N/A	55	N/A	uA

3.7 Electrical Characteristics for USB Interface

Table 3-7 RKNanoD Electrical Characteristics for USB Interface

Parameters		Test condition	Min	Typ	Max	Units
HS transmit,(quiescent supply current; Vin=0 or 1)	Current From USB_AVDD33	USB_AVDD33 = 3.3V USB_DVDD12 = 1.2V	N/A	N/A	0.1	mA
	Current From USB_DVDD12		N/A	N/A	20	mA
Classic mode active(quiescent supply current; Vin=0 or 1)	Current From USB_AVDD33		N/A	N/A	0.5	mA
	Current From USB_DVDD12		N/A	N/A	0.5	mA
HS mode(CL=10pF) Active supply current	Current From USB_AVDD33		N/A	0.1	N/A	mA
	Current From USB_DVDD12		N/A	2.22	N/A	mA
FS transmit,(CL=50pF) Active supply current	Current From USB_AVDD33		N/A	10	30	mA
	Current From USB_DVDD12		N/A	5	10	mA
LS transmit(CL=50 to 350pF) Active supply current	Current From USB_AVDD33		N/A	2	25	mA
	Current From USB_DVDD12		N/A	2	5	mA
Suspend mode	Current From USB_AVDD33		N/A	N/A	50	uA
	Current From USB_DVDD12		N/A	N/A	5	uA

3.8 Electrical Characteristics for Audio Codec Interface

Table 3-8 RKNanoD Electrical Characteristics for Audio Codec Interface

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Full Scale Input Voltage Line Input	N/A		1N/A	1	N/A	Vpeak
Full Scale Input Voltage Mic Input (signal)	N/A		N/A	1	N/A	Vpeak
Full Scale Input Voltage Mic Input (differential)	N/A		N/A	1	N/A	Vpeak
Full Scale Output Voltage HP (for 32ohm Loading)	N/A		N/A	1	N/A	Vpeak
Full Scale Output Voltage HP (for 16ohm Loading)	N/A		N/A	1	N/A	Vpeak

Parameters	Symbol	Test condition	Min	Typ	Max	Units
S/N Ratio Stereo DAC to HP with 10k/32/16 ohm loading	N/A	With A-weight Filter	N/A	100	N/A	dB
S/N Ratio Stereo DAC to Line Out with 10k ohm loading	N/A	With A-weight Filter	N/A	100	N/A	dB
S/N Ratio Line in to Stereo ADC	N/A	With A-weight Filter	N/A	90	N/A	dB
S/N Ratio Mic in to Stereo ADC with 0db gain (single end)	N/A	With A-weight Filter	N/A	90	N/A	dB
S/N Ratio Mic in to Stereo ADC with 0db signal (differential end)	N/A	With A-weight Filter	N/A	90	N/A	dB
Total Harmonic Distortion + Noise Stereo DAC to HP（32ohm loading）	N/A		N/A	67	N/A	dB
Total Harmonic Distortion + Noise Stereo DAC to Line Out	N/A		N/A	83	N/A	dB
Total Harmonic Distortion + Noise Line in to Stereo ADC	N/A		N/A	72	N/A	dB
Total Harmonic Distortion + Noise Mic to Stereo ADC with 0db gain (differential or single end)	N/A		N/A	72	N/A	dB
MicBias Output Voltage	N/A		1.5	N/A	AVDD	V
MicBias Drive Current	N/A		N/A	3	N/A	mA

