Rockchip
RK1808!
Technical Reference Manual

!2/3!
B /31 2: !

! !

! !

!	!	!

Table of Content

7/5! !

21/4! !

29/5! !

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31/7!B !

32/5! !

33/5! !

35/5! !

38/6! !

38/7!B !

Figure Index!

Fig. 23-10 UART clock generation

Fig. 28-2 WDT Operation Flow

! !

NOTICE

! !312:-! ! ! ! /H /B ! ! /

!2 ! !!

2/2B ! !

!	! B !	!	!	! B !	!

!	! B !	!	!	! B !	!

Table 1-1 RK1808 Address Mapping

Notes:
PMU_SRAM only has 8KB memory size
Service_xxx are interconnect register. Refer to chapter interconnect for more details.

Table 1-2 RK1808 remap function

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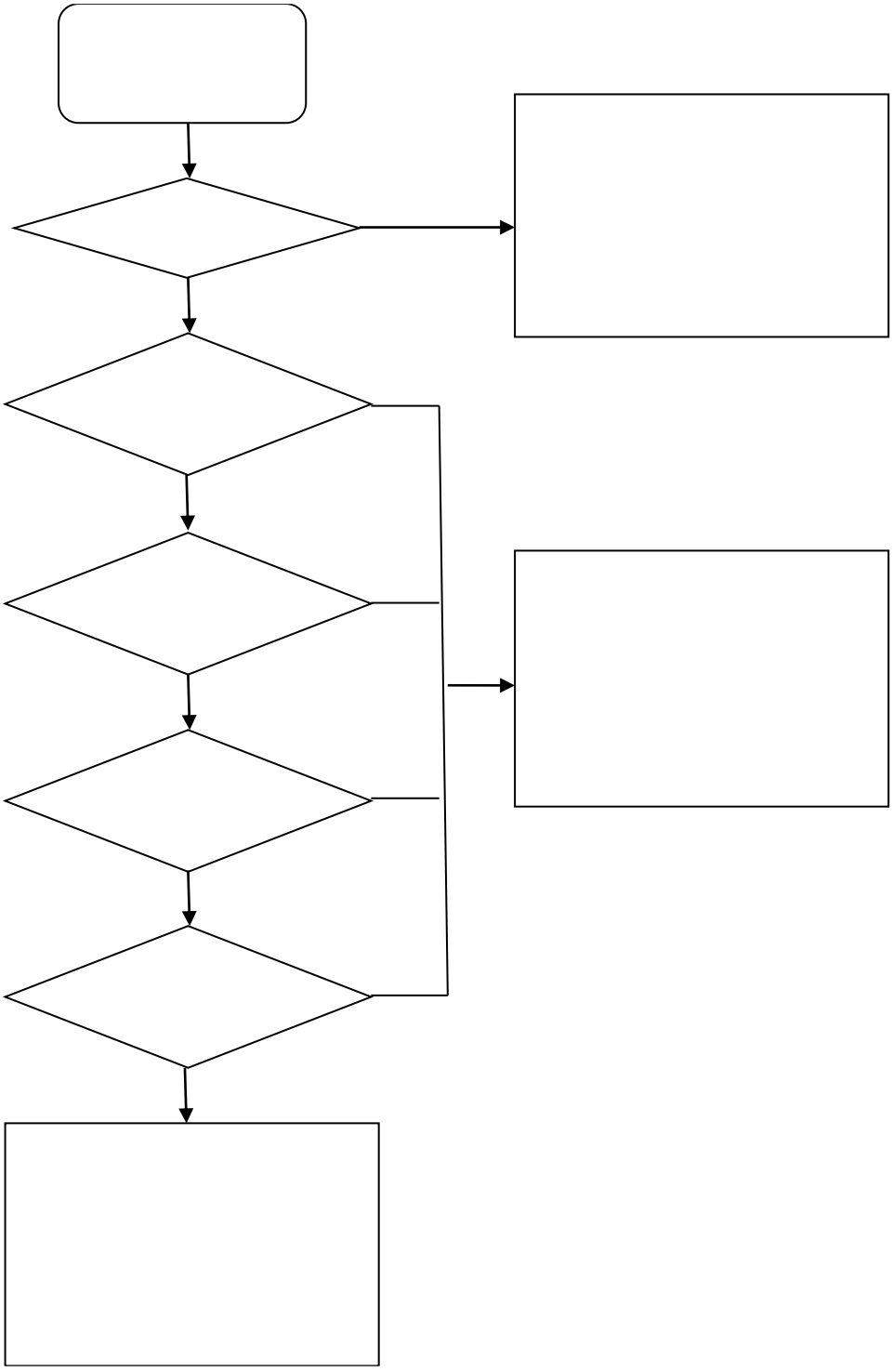

Fig. 1-1 RK1808 boot procedure flow

2.4 ! ! !

Table 1-3 RK1808 Interrupt connection list

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2/5 ! B! ! ! !

Table 1-4 RK1808 DMAC Hardware request connection list

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3/6 ! !

3/6/2 !

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3.6.3 ! !

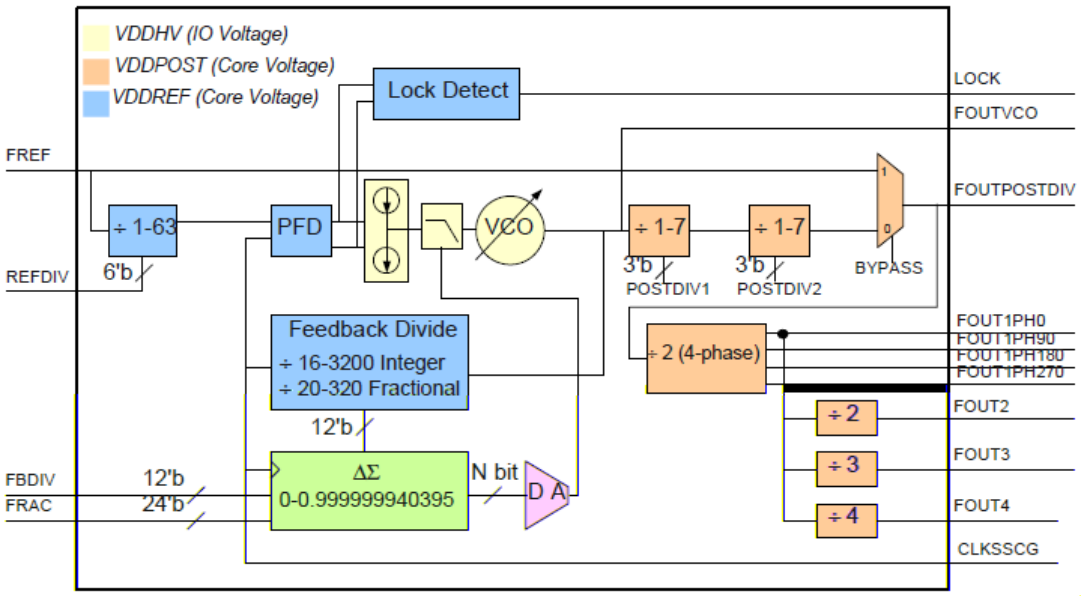

Fig. 2-3 PLL Block Diagram

3.7 ! !

3.7.2 !B ! !

3.7.3 ! !

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*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

3/7/4 ! ! !

B 1!

!	B !	! !	!

B 2!

!	B !	! !	!

!	B !	! !	!

B 3!

!	B !	! !	!

B 4!

!	B !	! !	!

B 5!

!	B !	! !	!

1!

!	B !	! !	!

2!

!	B !	! !	!

!	B !	! !	!

3!

!	B !	! !	!

4!

!	B !	! !	!

5!

!	B !	! !	!

1!

!	B !	! !	!

2!

!	B !	! !	!

!	B !	! !	!

3!

!	B !	! !	!

4!

!	B !	! !	!

!	B !	! !	!

5!

!	B !	! !	!

1!

!	B !	! !	!

!	B !	! !	!

2!

!	B !	! !	!

!	B !	! !	!

3!

!	B !	! !	!

4!

!	B !	! !	!

!	B !	! !	!

5!

!	B !	! !	!

1!

!	B !	! !	!

!	B !	! !	!

2!

!	B !	! !	!

3!

!	B !	! !	!

!	B !	! !	!

4!

!	B !	! !	!

!	B !	! !	!

5!

!	B !	! !	!

!

!	B !	! !	!

!	B !	! !	!

_____!

!	B !	! !	!

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!	B !	! !	!

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!	B !	! !	!

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!	B !	! !	!

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!	B !	! !	!

1!

!	B !	! !	!

!	B !	! !	!

2!

!	B !	! !	!

3!

!	B !	! !	!

!	B !	! !	!

4!

!	B !	! !	!

5!

!	B !	! !	!

6!

!	B !	! !	!

7!

!	B !	! !	!

8!

!	B !	! !	!

!	B !	! !	!

9!

!	B !	! !	!

: !

!	B !	! !	!

21!

!	B !	! !	!

!	B !	! !	!

22!

!	B !	! !	!

23!

!	B !	! !	!

!	B !	! !	!

24!

!	B !	! !	!

25!

!	B !	! !	!

26!

!	B !	! !	!

27!

!	B !	! !	!

28!

!	B !	! !	!

!	B !	! !	!

29!

!	B !	! !	!

2: !

!	B !	! !	!

!	B !	! !	!

31!

!	B !	! !	!

32!

!	B !	! !	!

33!

!	B !	! !	!

!	B !	! !	!

34!

!	B !	! !	!

35!

!	B !	! !	!

36!

!	B !	! !	!

37!

!	B !	! !	!

38!

!	B !	! !	!

!	B !	! !	!

39!

!	B !	! !	!

3: !

!	B !	! !	!

!	B !	! !	!

41!

!	B !	! !	!

42!

!	B !	! !	!

43!

!	B !	!	!	4 48 2: 2/1: 5/63884: 1/351/83! 4 48 !1/63!8: 1/

!	B !	! !	!

46!

!	B !	! !	!

47!

!	B !	! !	!

!	B !	! !	!

48!

!	B !	! !	!

49!

!	B !	! !	!

4: !

!	B !	! !	!

54!

!	B !	! !	!

55!

!	B !	! !	!

56!

!	B !	! !	!

57!

!	B !	! !	!

58!

!	B !	! !	!

59!

!	B !	! !	!

5: !

!	B !	! !	!

61!

!	B !	! !	!

!	B !	! !	!

63!

!	B !	! !	!

64!

!	B !	! !	!

65!

!	B !	! !	!

66!

!	B !	! !	!

67!

!	B !	! !	!

68!

!	B !	! !	!

!	B !	! !	!

69!

!	B !	! !	!

6: !

!	B !	! !	!

71!

!	B !	! !	!

!	B !	! !	!

72!

!	B !	! !	!

73!

!	B !	! !	!

74!

!	B !	! !	!

!	B !	! !	!

75!

!	B !	! !	!

76!

!	B !	! !	!

77!

!	B !	! !	!

78!

!	B !	! !	!

79!

!	B !	! !	!

7: !

!	B !	! !	!

81!

!	B !	! !	!

82!

!	B !	! !	!

!	B !	! !	!

83!

!	B !	! !	!

!	B !	! !	!

B 1!

!	B !	! !	!

!	B !	! !	!

B 2!

!	B !	! !	!

!	B !	! !	!

B 3!

!	B !	! !	!

!	B !	! !	!

B 4!

!	B !	! !	!

!	B !	! !	!

B 5!

!	B !	! !	!

!	B !	! !	!

B 6!

!	B !	! !	!

B 7!

!	B !	! !	!

!	B !	! !	!

B 8!

!	B !	! !	!

!	B !	! !	!

B 9!

!	B !	! !	!

!	B !	! !	!

B :!

!	B !	! !	!

B 21!

!	B !	! !	!

B 22!

!	B !	! !	!

B 23!

!	B !	! !	!

!	B !	! !	!

B 24!

!	B !	! !	!

!	B !	! !	!

B 25!

!	B !	! !	!

!	B !	!	!	!

!	B !	! !	!

B 27!

!	B !	! !	!

!	B !	! !	!

B 28!

!	B !	! !	!

!	B !	! !	!

B 29!

!	B !	! !	!

B 2: !

!	B !	! !	!

1 4!

!	B !	! !	!

5 8!

!	B !	! !	!

9_22!

!	B !	! !	!

23_26!

!	B !	! !	!

27_2: !

!	B !	! !	!

31_34!

!	B !	! !	!

35_38!

!	B !	! !	!

39 42!

!	B !	! !	!

43 46!

!	B !	! !	!

47 4: !

!	B !	! !	!

51 54!

!	B !	! !	!

55 58!

!	B !	! !	!

59 62!

!	B !	! !	!

63 66!

!	B !	! !	!

!

67 6: !

!	B !	! !	!

71 74!

!	B !	! !	!

75 78!

!	B !	! !	!

79 82!

!	B !	! !	!

83 86!

!	B !	! !	!

87 8: !

!	B !	! !	!

91 94!

!	B !	! !	!

95 98!

!	B !	! !	!

99 : 2!

!	B !	! !	!

: 3 : 6!

!	B !	! !	!

: 7 : : !

!	B !	! !	!

211 214!

!	B !	! !	!

215 218!

!	B !	! !	!

219 222!

!	B !	! !	!

223 226!

!	B !	! !	!

227 22: !

!	B !	! !	!

231 234!

!	B !	! !	!

235 238!

!	B !	! !	!

1!

!	B !	! !	!

!	B !	! !	!

2!

!	B !	! !	!

3!

!	B !	! !	!

4!

!	B !	! !	!

!	B !	! !	!

5!

!	B !	! !	!

!	B !	! !	!

6!

!	B !	! !	!

7!

!	B !	! !	!

8!

!	B !	! !	!

!	B !	! !	!

9!

!	B !	! !	!

!	B !	! !	!

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!	B !	! !	!

!	B !	! !	!

21!

!	B !	! !	!

!	B !	! !	!

23!

!	B !	! !	!

!	B !	! !	!

24!

!	B !	! !	!

!	B !	! !	!

25!

!	B !	! !	!

!	B !	! !	!

26!

!	B !	! !	!

!	B !	! !	!

1!

!	B !	! !	!

2!

!	B !	! !	!

1!

!	B !	! !	!

!	B !	! !	!

2!

!	B !	! !	!

1!

!	B !	! !	!

2!

!	B !	! !	!

1!

!	B !	! !	!

2!

!	B !	! !	!

!	B !	! !	!

3!

!	B !	! !	!

!	B !	! !	!

4!

!	B !	! !	!

5!

!	B !	! !	!

!	B !	! !	!

!

!	B !	! !	!

1!

!	B !	! !	!

2!

!	B !	! !	!

3!

!	B !	! !	!

4!

!	B !	! !	!

5!

!	B !	! !	!

!	B !	! !	!

6!

!	B !	! !	!

7!

!	B !	! !	!

!
!

8!

!	B !	! !	!

!	B !	! !	!

B 1!

!	B !	! !	!

B 2!

!	B !	! !	!

3/8 B ! !

3/8/2 ! !

B/ ! ! ! !

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3/8/3 ! ! ! ! ! !

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3.8.4 ! ! !

Table 2-1 Source Clock Limitation of Fractional Divider

3.8.5 61! ! !

3.8.6 6! ! !

3.8.7 ! ! !

!4 ! !

4/2 !

4/2/2 !

-
-

4/2/3 ! ! ! !

!	!B !

4/3 ! !

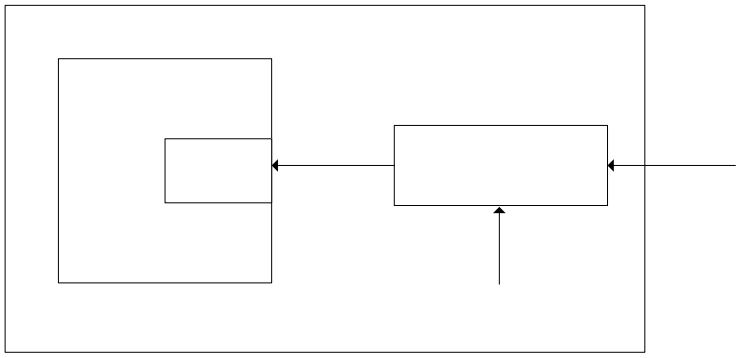

Fig. 3-1 Debug system structure

4/4 ! !

4/4/2 B !

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-

4/5 ! !

4/6 ! !

4/6/2 B ! . ! !

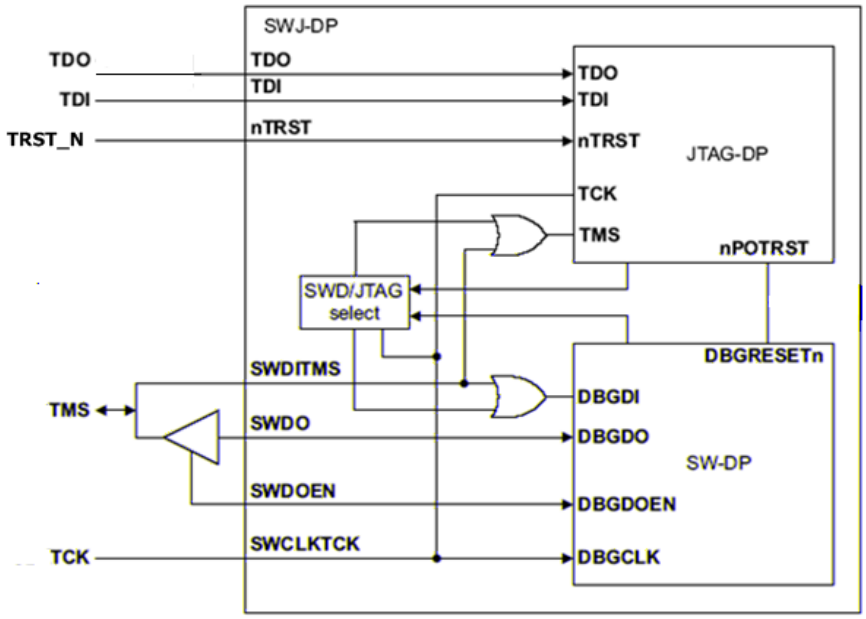

Fig. 3-2 DAP SWJ interface

4/6/3 B ! . ! !

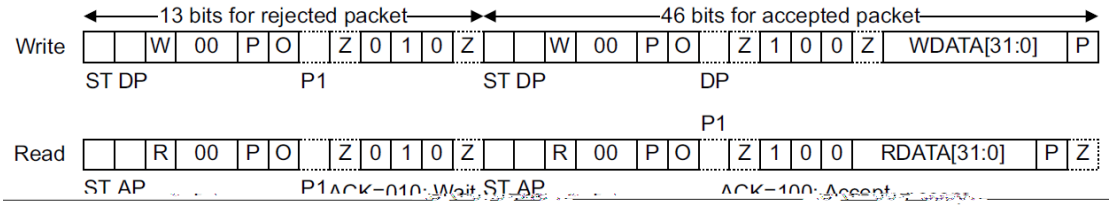

Fig. 3-3 SW-DP acknowledgement timing

Table 3-1 SW-DP Interface Description

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!5 ! ! !) !

5/2 !

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-
-

5/3 ! !

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-
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-
-

Table 4-1 GRF Address Mapping Table

5/4 ! !

5/4/2 ! !

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_____				

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

5/4/3 ! ! !

2B !

!	B !	! !	!

2B !

!	B !	! !	!

2 !

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

3B !

!	B !	! !	!

!	B !	! !	!

3 !

!	B !	! !	!

3 !

!	B !	! !	!

3 !

!	B !	! !	!

!	B !	! !	!

3 !

!	B !	! !	!

3 !

!	B !	! !	!

4B !

!	B !	! !	!

4B !

!	B !	! !	!

4 !

!	B !	! !	!

!	B !	! !	!

4 !

!	B !	! !	!

4 !

!	B !	! !	!

4 !

!	B !	! !	!

!	B !	! !	!

5B !

!	B !	! !	!

!	B !	! !	!

5 !

!	B !	! !	!

5 !

!	B !	! !	!

5 !

!	B !	! !	!

!	B !	! !	!

5 !

!	B !	! !	!

2B !

!	B !	! !	!

!	B !	! !	!

2 !

!	B !	! !	!

!	B !	! !	!

3B !

!	B !	! !	!

!	B !	! !	!

3 !

!	B !	! !	!

3 !

!	B !	! !	!

!	B !	! !	!

3 !

!	B !	! !	!

4B !

!	B !	! !	!

4 !

!	B !	! !	!

!	B !	! !	!

4 !

!	B !	! !	!

5B !

!	B !	! !	!

5 !

!	B !	! !	!

5 !

!	B !	! !	!

2B !

!	B !	! !	!

2 !

!	B !	! !	!

!	B !	! !	!

3B !

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

3 !

!	B !	! !	!

3 !

!	B !	! !	!

!	B !	! !	!

4B !

!	B !	! !	!

!	B !	! !	!

4 !

!	B !	! !	!

4 !

!	B !	! !	!

4 !

!	B !	! !	!

!	B !	! !	!

5B !

!	B !	! !	!

!	B !	! !	!

5 !

!	B !	! !	!

5 !

!	B !	! !	!

2B !

!	B !	! !	!

!	B !	! !	!

2 !

!	B !	! !	!

!	B !	! !	!

2 !

!	B !	! !	!

2 !

!	B !	! !	!

!	B !	! !	!

3 !

!	B !	! !	!

!	B !	! !	!

3 !

!	B !	! !	!

3 !

!	B !	! !	!

4B !

!	B !	! !	!

!	B !	! !	!

4 !

!	B !	! !	!

!	B !	! !	!

4 !

!	B !	! !	!

!
!
!
!
4 !

!	B !	! !	!

5B !

!	B !	! !	!

!	B !	! !	!

5 !

!	B !	! !	!

!	B !	! !	!

5 !

!	B !	! !	!

2B !

!	B !	! !	!

!	B !	! !	!

2 !

!	B !	! !	!

!	B !	! !	!

3 !

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

3 !

!	B !	! !	!

!	B !	!	!	!

!	B !	! !	!

4B !

!	B !	! !	!

!	B !	! !	!

4 !

!	B !	! !	!

!	B !	! !	!

4 !

!	B !	! !	!

!	B !	! !	!

4 !

!	B !	! !	!

!	B !	! !	!

5B !

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

5 !

!	B !	! !	!

!	B !	! !	!

5 !

!	B !	! !	!

!	B !	! !	!

1!

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

1!

!	B !	! !	!

2!

!	B !	! !	!

!	B !	! !	!

3!

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

5!

!	B !	! !	!

6!

!	B !	! !	!

1!

!	B !	! !	!

!	B !	! !	!

2!

!	B !	! !	!

!	B !	! !	!

B !

!	B !	! !	!

1!

!	B !	! !	!

2!

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

B 1!

!	B !	! !	!

!	B !	! !	!

1!

!	B !	! !	!

!	B !	! !	!

2!

!	B !	! !	!

!	B !	! !	!

3!

!	B !	! !	!

!	B !	! !	!

B 1!

!	B !	! !	!

B 2!

!	B !	! !	!

!	B !	! !	!

1!

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

2!

!	B !	! !	!

!	B !	! !	!

3!

!	B !	! !	!

!	B !	! !	!

B 1!

!	B !	! !	!

B 2!

!	B !	! !	!

!	B !	! !	!

B 3!

!	B !	! !	!

B 4!

!	B !	! !	!

B 5!

!	B !	! !	!

!	B !	! !	!

2!

!	B !	! !	!

B 1!

!	B !	! !	!

B 2!

!	B !	! !	!

!

!	B !	! !	!

B 1!

!	B !	! !	!

B 2!

!	B !	! !	!

5.5 3 ! !

5.5.2 ! !

!	!	!	! !	!

!	!	!	! !	!

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

5/5/3 ! ! !

3 1!

!	B !	! !	!

3 2!

!	B !	! !	!

3 3!

!	B !	! !	!

3 4!

!	B !	! !	!

3 5!

!	B !	! !	!

3 6!

!	B !	! !	!

3 7!

!	B !	! !	!

3 8!

!	B !	! !	!

3 9!

!	B !	! !	!

3 : !

!	B !	! !	!

3 21!

!	B !	! !	!

3 22!

!	B !	! !	!

!	B !	! !	!

3 23!

!	B !	! !	!

3 24!

!	B !	! !	!

3 25!

!	B !	! !	!

3 26!

!	B !	! !	!

3 27!

!	B !	! !	!

3 28!

!	B !	! !	!

3 29!

!	B !	! !	!

3 2: !

!	B !	! !	!

3 31!

!	B !	! !	!

!	B !	! !	!

3 32!

!	B !	! !	!

3 33!

!	B !	! !	!

3 34!

!	B !	! !	!

3 1!

!	B !	! !	!

!	B !	! !	!

3 2!

!	B !	! !	!

!	B !	! !	!

3 3!

!	B !	! !	!

3 4!

!	B !	! !	!

!

3 B !

!	B !	! !	!

3 B !

!	B !	! !	!

!	B !	! !	!

3 B !

!	B !	! !	!

3 B !

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

3 !

!	B !	! !	!

3 B !

!	B !	! !	!

3 !

!	B !	! !	!

3 5!

!	B !	! !	!

5/6 4 ! !

5/6/2 ! !

!	!	!	! !	!
_____ _____				
_____ _____				
_____ _____				
_____ _____				
_____ _____				
_____ _____				
_____ _____				

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

5/6/3 ! ! !

4 1!

!	B !	! !	!

!	B !	! !	!

!	B !	!	!	!

4 2!

!	B !	!	!	!

!	B !	! !	!

4 3!

!	B !	! !	!

!	B !	! !	!

4 4!

!	B !	! !	!

!	B !	! !	!

4 5!

!	B !	! !	!

!	B !	! !	!

4 B 1!

!	B !	! !	!

4 B 2!

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

5/7 ! !

5/7/2 ! !

!	!	!	! !	!

!	!	!	! !	!
_____				
_____				
_____				
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_____				
_____ _____				
_____ _____				
_____ ___				
_____ _____				
_____ _____				
_____ _____				

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

5/7/3 ! ! !

1B !

!	B !	! !	!

!	B !	! !	!

1 !

!	B !	! !	!

!	B !	! !	!

1 !

!	B !	! !	!

1B !

!	B !	! !	!

1 !

!	B !	! !	!

!	B !	! !	!

1B !

!	B !	! !	!

!	B !	! !	!

1 !

!	B !	! !	!

!	B !	! !	!

1 !

!	B !	! !	!

1B !

!	B !	! !	!

1 !

!	B !	! !	!

1 !

!	B !	! !	!

1B !

!	B !	! !	!

1 !

!	B !	! !	!

!	B !	! !	!

1 !

!	B !	! !	!

!	B !	! !	!

1!

!	B !	! !	!

!	B !	! !	!

2!

!	B !	! !	!

!

3!

!	B !	! !	!

!

4!

!	B !	! !	!

5!

!	B !	! !	!

B !

!	B !	! !	!

1!

!	B !	! !	!

!	B !	! !	!

2!

!	B !	! !	!

!	B !	! !	!

B !

!	B !	! !	!

!	B !	! !	!

B 1!

!	B !	! !	!

B 2!

!	B !	! !	!

1!

!	B !	! !	!

2!

!	B !	! !	!

3!

!	B !	! !	!

4!

!	B !	! !	!

5!

!	B !	! !	!

6!

!	B !	! !	!

7!

!	B !	! !	!

8!

!	B !	! !	!

9!

!	B !	! !	!

: !

!	B !	! !	!

21!

!	B !	! !	!

22!

!	B !	! !	!

B !

!	B !	! !	!

!

!	B !	! !	!

!

!	B !	! !	!

B !

!	B !	! !	!

B B !

!	B !	! !	!

!

!	B !	! !	!

5.8 ! !

5.8.2 ! !

!	!	!	! !	!
_____				
_____				
_____				
_____				
_____				
_____				
_____				
_____				
_____				
_____				
_____				
_____				
_____				

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

5.8.3 ! ! !

_____1!

!	B !	! !	!

!	B !	! !	!

2!

!	B !	! !	!

!	B !	! !	!

_____!

!	B !	! !	!

!	B !	! !	!

_____!

!	B !	! !	!

_____B 1!

!	B !	! !	!

B 2!

!	B !	! !	!

B 3!

!	B !	! !	!

B 4!

!	B !	! !	!

B 5!

!	B !	! !	!

B 6!

!	B !	! !	!

B 7!

!	B !	! !	!

B 8!

!	B !	! !	!

B 9!

!	B !	! !	!

B : !

!	B !	! !	!

!	B !	! !	!

5.9 ! !

5.9.2 ! !

!	!	!	! !	!

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

5.9.3 ! ! !

1!

!	B !	! !	!

!	B !	! !	!

4 2!

!	B !	! !	!

!	B !	! !	!

4 B 1!

!	B !	! !	!

4 B 2!

!	B !	! !	!

4 B 3!

!	B !	! !	!

1 1!

!	B !	! !	!

1 2!

!	B !	! !	!

1 B !

!	B !	! !	!

5/ ! !

5/ /2 ! !

!	!	!	! !	!

!	!	!	! !	!
_____ ___				
_____ ___				
_____ ___				
_____ ___				
_____ ___				
_____ ___				
_____ _____				
_____ _____				
_____ _____				
_____ _____				
_____ _____				
_____ _____				
_____ _____				
_____ _____				
_____ _____				
_____ _____				
_____ _____				
_____ _____				

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

5/ /3 ! ! !

_____ 1!

!	B !	! !	!

!	B !	! !	!

2!

!	B !	! !	!

3!

!	B !	! !	!

4!

!	B !	! !	!

5!

!	B !	! !	!

6!

!	B !	! !	!

7!

!	B !	! !	!

8!

!	B !	! !	!

9!

!	B !	! !	!

B !

!	B !	! !	!

B B !

!	B !	! !	!

B B !

!	B !	! !	!

B B !

!	B !	! !	!

B B !

!	B !	! !	!

B B !

!	B !	! !	!

!

!	B !	! !	!

B !

!	B !	! !	!

1!

!	B !	! !	!

2!

!	B !	! !	!

B 1!

!	B !	! !	!

B 2!

!	B !	! !	!

!6 .B46!

6/2 !

-
-
-
-

-
-
-
-

-
-
-

-

Table 5-1 CPU Configuration

6/3 ! !

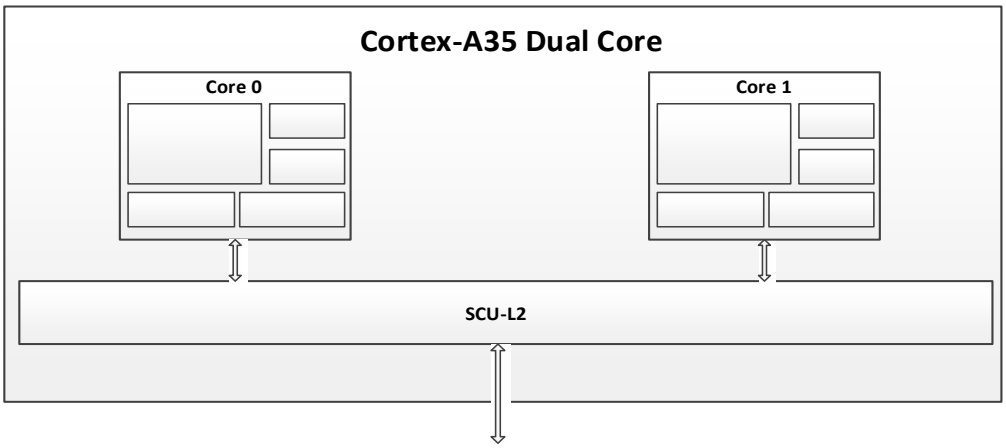

Fig. 5-1 Block Diagram

6.4 ! !

!7 ! !B ! !) B !

7/2 !

-
-
-
-
-
-
-

Table 6-1 DMAC Request Mapping Table

! !	!	!

7.3 ! !

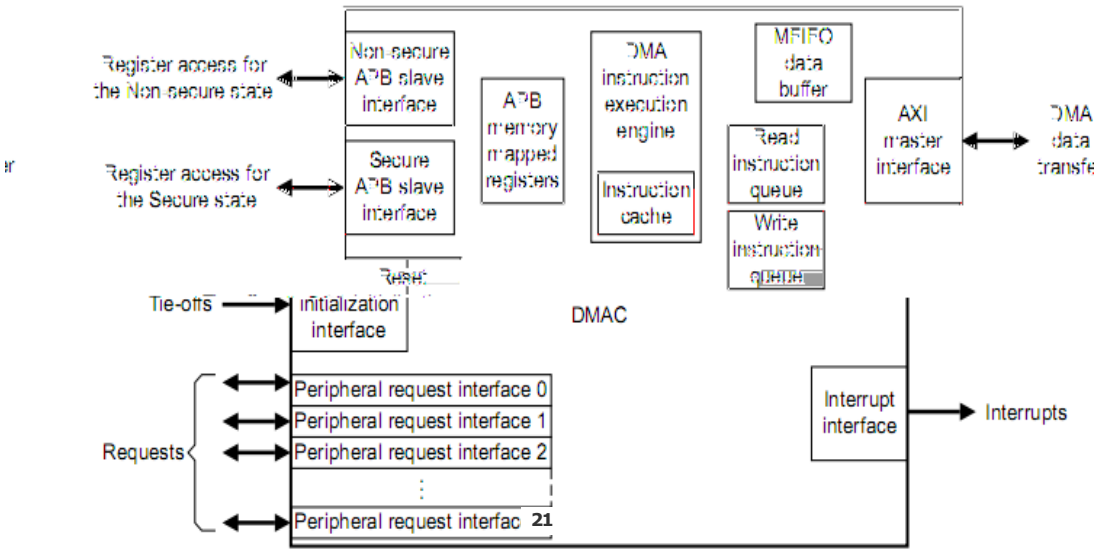

Fig. 6-1 Block diagram of DMAC

7.4 ! !

7.4.2 !

7.4.3 ! !

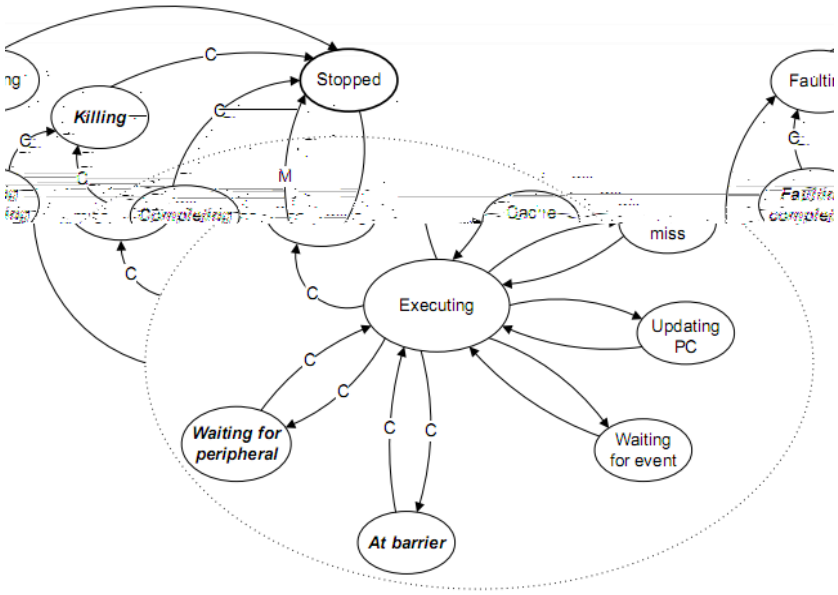

Fig. 6-2 DMAC operation states

Notes: arcs with no letter designator indicate state transitions for the DMA manager and DMA channel threads, otherwise use is restricted as follows:
C DMA channel threads only.
M DMA manager thread only.

7 /5 ! !

7 /5 /2 !B ! !

7 /5 /3 ! !

!	!	!	! !	!

!	!	!	! !	!
_____				
_____				
_____				

_____

!	!	!	! !	!
_____				
_____				
_____				
_____				
_____				
_____				
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_____				
_____				
_____				
_____				
_____				
_____				
_____				
_____				
_____				
_____				
_____				
_____				
_____				

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

7/5/4 ! ! !

B

!	B !	! !	!

B

!	B !	! !	!

B

!	B !	! !	!

B

!	B !	! !	!

B

!	B !	! !	!

B

!	B !	! !	!

B

!	B !	! !	!

B

!	B !	! !	!

B

!	B !	! !	!

B 1

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

B 2

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

B 3

!	B !	! !	!

!	B !	! !	!

B 4

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

B 5

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

B 6

!	B !	! !	!

!	B !	! !	!

B 1

!	B !	! !	!

!	B !	! !	!

B 1

!	B !	! !	!

B 2

!	B !	! !	!

!	B !	! !	!

B 2

!	B !	! !	!

B 3

!	B !	! !	!

!	B !	! !	!

B 3

!	B !	! !	!

B 4

!	B !	! !	!

!	B !	! !	!

B 4

!	B !	! !	!

B 5

!	B !	! !	!

!	B !	! !	!

B 5

!	B !	! !	!

B 6

!	B !	! !	!

!	B !	! !	!

B 6

!	B !	! !	!

B B 1

!	B !	! !	!

B B 1

!	B !	! !	!

B 1

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

B 1 1

!	B !	! !	!

B 2 1

!	B !	! !	!

B B 2

!	B !	! !	!

B B 2

!	B !	! !	!

B 2

!	B !	! !	!

!	B !	! !	!

B 1 2

!	B !	! !	!

B 2 2

!	B !	! !	!

B B 3

!	B !	! !	!

B B 3

!	B !	! !	!

B 3

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

B 1 3

!	B !	! !	!

B 2 3

!	B !	! !	!

B B 4

!	B !	! !	!

B B 4

!	B !	! !	!

B 4

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

B 1 4

!	B !	! !	!

B 2 4

!	B !	! !	!

B B 5

!	B !	! !	!

B B 5

!	B !	! !	!

B 5

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

B 1 5

!	B !	! !	!

B 2 5

!	B !	! !	!

B B 6

!	B !	! !	!

B B 6

!	B !	! !	!

B 6

!	B !	! !	!

!	B !	! !	!

B 1 6

!	B !	! !	!

B 2 6

!	B !	! !	!

B B

!	B !	! !	!

B

!	B !	! !	!

B 1

!	B !	! !	!

B 2

!	B !	! !	!

B 1

!	B !	! !	!

B 2

!	B !	! !	!

B 3

!	B !	! !	!

B 4

!	B !	! !	!

B 5

!	B !	! !	!

B

!	B !	! !	!

!	B !	! !	!

B

!	B !	! !	!

7/6 ! !

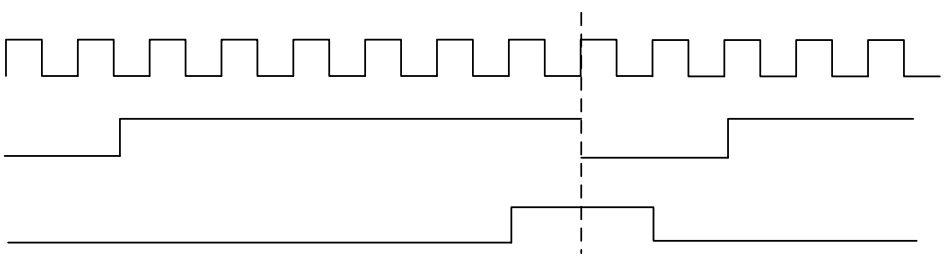

Fig. 6-3 DMAC request and acknowledge timing

7 /7 ! !

Table 6-2 DMAC boot interface

!	! !	! !

!	! !	! !

!

!

!

!

= !

7/8 B ! !

7/8/2 ! !B ! ! !

-
-
-

7/8/3 ! !

- B! ! ! ! ! ! ! !
  - B
  - B
  - B !
- B! ! ! ! ! . ! !
  - B !!!

■ B !

■ B !

!

● B! ! ! ! ! ! ! !

■ B !!!

■ B !!!

■ B !

■ B -! B !!

■ B !

● B! ! ! ! ! ! . ! !

■ **B !**

■ **B !**

■ **B !!**

■ **B -! B !**

■ **B !!!**

7/8/4 ! !
! ! !

-
-

-
-

! ! ! !

! B! ! ! ! ! ! B! !

! ! ! B! !

7/8/5 ! ! ! ! !

! !!

-
-

Table 6-3Source size in CCRn

! ! ! !	B ! ! ! B ! ! B !

7.8.6 ! ! ! !

7.8.7 ! !

Table 6-4 DMAC Instruction sets

!	!	! !

!	!	! !

Notes:Thread usage:C=DMA channel M=DMA manager

7/8/8 B ! !

BB !

Table 6-5 DMAC instruction encoding

B ! !

!8 ! ! !) !

8/2 !

Table 7-1 GIC-500 configuration

-
-
-
  -
  -
  -
  -
-
-
-
-
-
  -
  -
  -
-
-

8/3 ! !

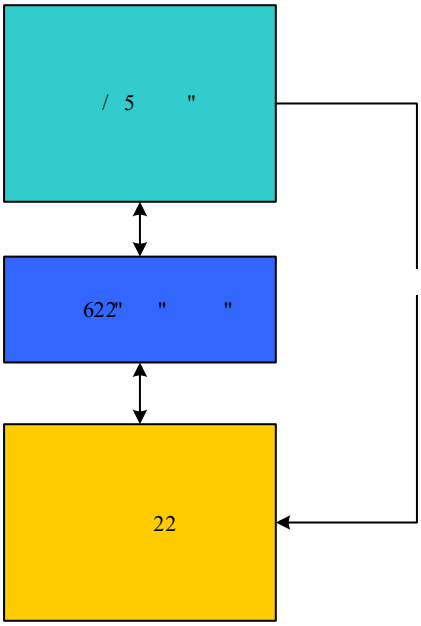

Fig. 7-1 Block Diagram

8/4 ! !

!9 ! ! !) !

9/2 !

9/2/2 !

- ,

9/3 ! !

9/3/2 ! !

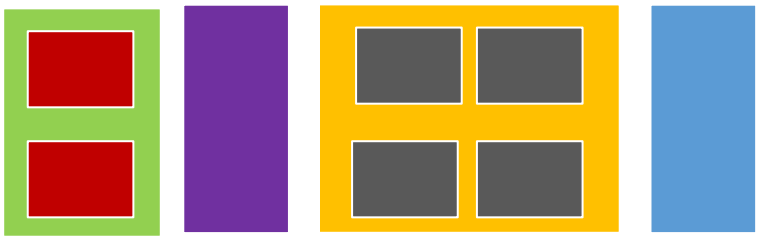

Fig. 8-1 Power Domain Partition

Table 8-1 Power Domain and Voltage Domain Summary

! !	!!	!

! !	!!	!

9.3.3 ! ! !

-
-
-

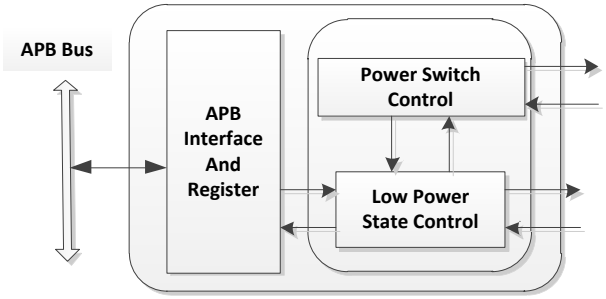

Fig. 8-2 PMU Bock Diagram

9.4 ! !

9/5 ! !

9/5/2 ! !

!	!		! !	!
_____				
_____				
_____				
_____				
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_____				
_____				
_____ _____				
_____ _____				
_____ _____				
_____ _____				
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_____				

!	!		! !	!
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_____ _____				
_____ _____				
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_____				

!	!		! !	!
_____				
_____				
_____				
_____ _____				
_____ _____				
_____ _____				
_____ _____				
_____				
_____				
_____				
_____				
_____				

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

9/5/3 ! ! !
_____ B 1 !

!	B !	! !	!

B 1 !

!	B !	! !	!

B 2 !

!	B !	! !	!

B 2 !

!	B !	! !	!

B 3 !

!	B !	! !	!

!	B !	! !	!

!

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

!

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

_____!

!	B !	! !	!

!	B !	! !	!

!

!	B !	! !	!

!	B !	! !	!

_____!

!	B !	! !	!

!	B !	! !	!

!

!

!	B !	! !	!

!	B !	! !	!

_____!

!	B !	! !	!

_____!

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

!

!	B !	! !	!

_____!

!	B !	! !	!

_____!

!	B !	! !	!

_____!

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

2!

!	B !	! !	!

!	B !	! !	!

_____!

!	B !	! !	!

_____!

!	B !	! !	!

_____!

!	B !	! !	!

!	B !	! !	!

_____!

!	B !	! !	!

_____!

!	B !	! !	!

_____!

!	B !	! !	!

_____B_____!

!	B !	! !	!

B !

!	B !	! !	!

B !

!	B !	! !	!

B !

!	B !	! !	!

!

!	**B !**	**! !**	**!**

1 !

!	**B !**	**! !**	**!**

1 !

!	**B !**	**! !**	**!**

2 !

!	**B !**	**! !**	**!**

2 !

!	B !	! !	!

3 !

!	B !	! !	!

3 !

!	B !	! !	!

4 !

!	B !	! !	!

4 !

!	B !	! !	!

_____!

!	B !	! !	!

_____!

!	B !	! !	!

_____!

!	B !	! !	!

_____!

!	B !	! !	!

_____!

!	B !	! !	!

_____!

!	B !	! !	!

_____1B_____!

!	B !	! !	!

2B !

!	B !	! !	!

!

!	B !	! !	!

9/6 ! !

9/6/2 ! ! ! ! !

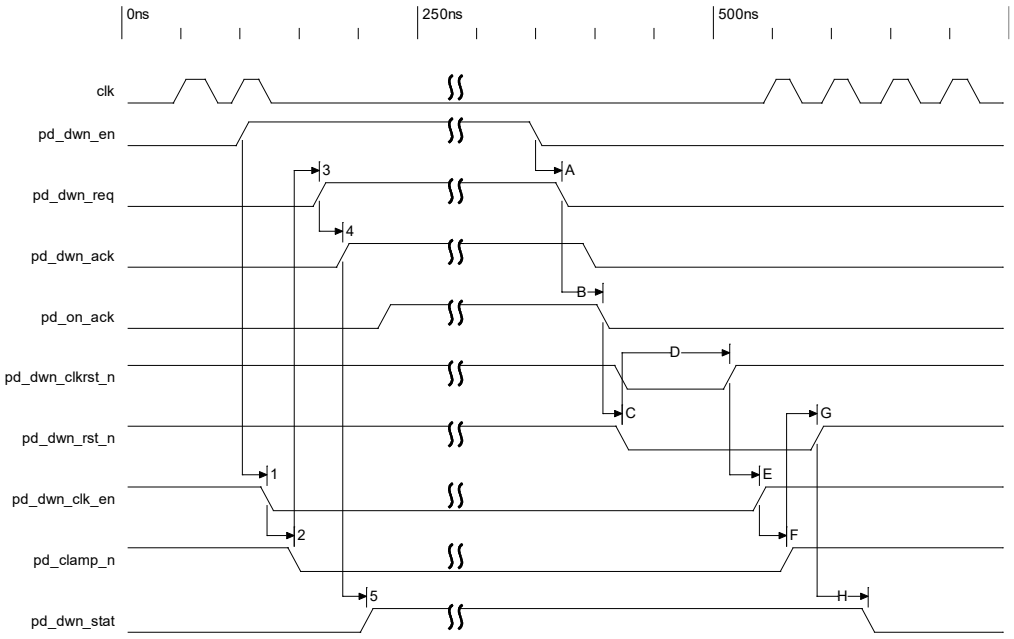

Fig. 8-3 Each Domain Power Switch Timing

9/6/3 ! ! B ! !

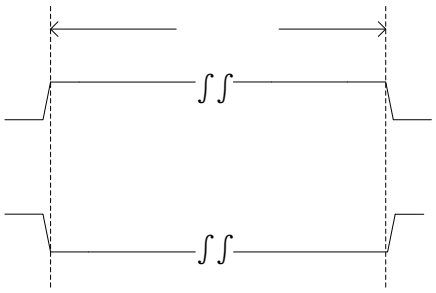

Fig. 8-4 External Wakeup Source PAD Timing

9/7!B ! !

9/7/2 ! ! !

Table 8-2 Low Power State

9/7/3 ! !

Table 8-3 Low Power State

		IO_UART0tx_PMUdebug0_GPIO0B2pmuio2	
		IO_UART0rx_PMUdebug1_GPIO0B3pmuio2	
		IO_UART0cts_PMUdebug2_PMUdebug_sout_GPIO0B4pmuio2	
		IO_PWM1_UART3txm0_PMUdebug3_GPIO0C3pmuio2	
		IO_PWM3_UART3rxm0_PMUdebug4_GPIO0C4pmuio2	
		IO_I2C1scl_PMUdebug5_GPIO0C0pmuio2	
		IO_UART0cts_PMUdebug2_PMUdebug_sout_GPIO0B4pmuio2	

!: ! ! ! !) !

: /2 !

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  -

: /3 ! !

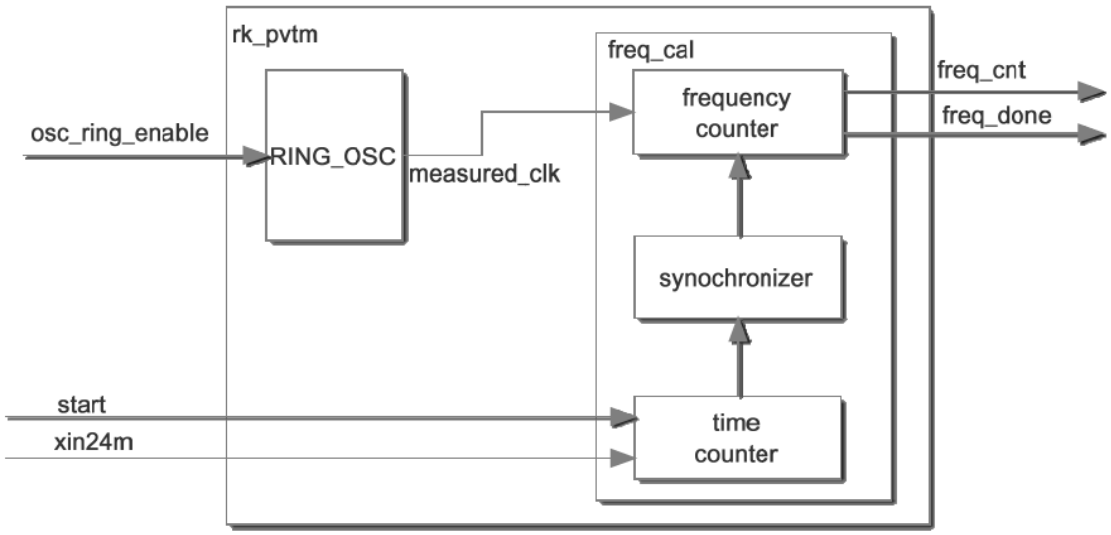

Fig. 9-1 PVTM Block Diagram

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-

: /4 ! !

: /4/2 ! !

: /4/3 ! ! ! ! !

Table 9-1 Core_pvtm control source and result destination

!	! !	! 0 ! !

!	! !	! 0 ! !

Table 9-2 PMU_pvtm control source and result destination

!	! !	! 0 ! !

Table 9-3 NPU_pvtm control source and result destination

!	! !	! 0 ! !

: /4/4 ! !

: /5 B ! !

: /5/2 ! ! !

!21 B ! ! ! !)B ! !

21 /2 !

- " " ""
  - " " " " " " "
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- " " " " " " " " " "
  - " " " " " " " " " " " " " "
  - " " " " " " " " " " " " " "
  - " 0

21 /3 ! !

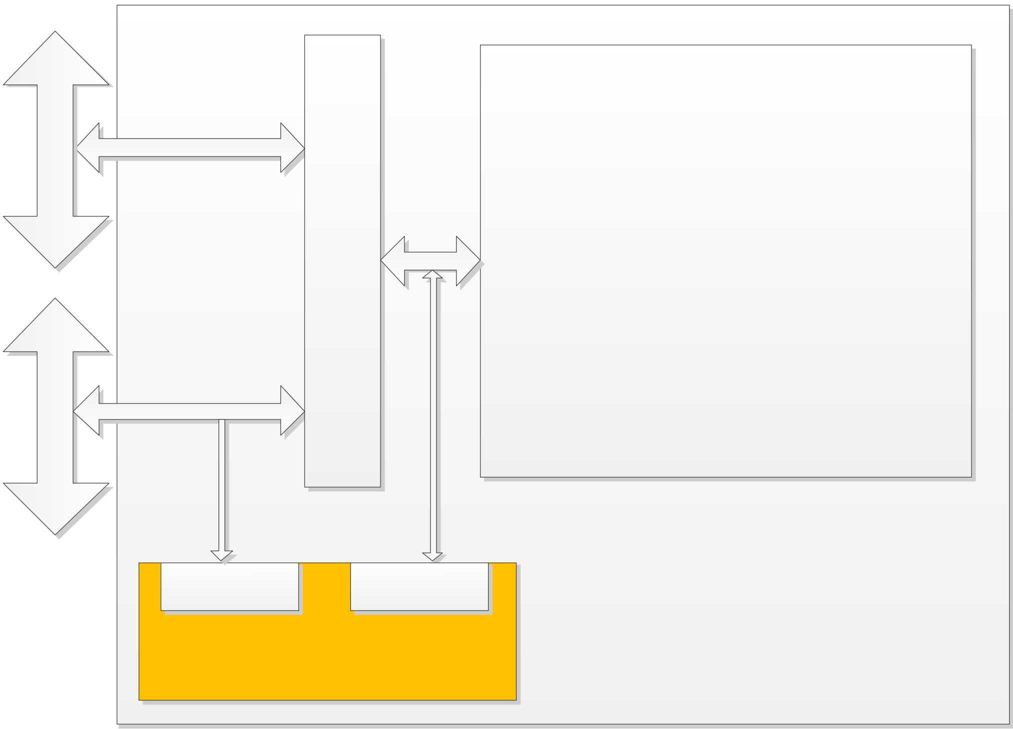

Fig. 10-1 AXI_PERF block diagram

21 /4 ! !

21 /4 /2 ! !

!	!	!	! !	!

!	!	!	! !	!

!	B !	! !	!

!
!

!

B 2!

!	B !	! !	!

B 3!

!	B !	! !	!

B 4!

!	B !	! !	!

B 5!

B 7!

!	B !	! !	!

B 8!

!	B !	! !	!

B 9!

!	B !	! !	!

B B B !

!	B !	! !	!

B B B !

!	B !	! !	!

B B B !

!	B !	! !	!

B B B !

!	B !	! !	!

B B B !

!	B !	!	!	!

B !

!	B !	!	!	!

B B !

!	B !	!	!	!

21.5 B ! !

21.5.2 ! ! ! !!

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21.5.3 ! ! ! !

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21/5/4 ! ! !

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21/5/5 ! ! ! ! ! ! !

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21/5/6 ! ! ! ! ! !

!22 ! ! ! !

22/2 !

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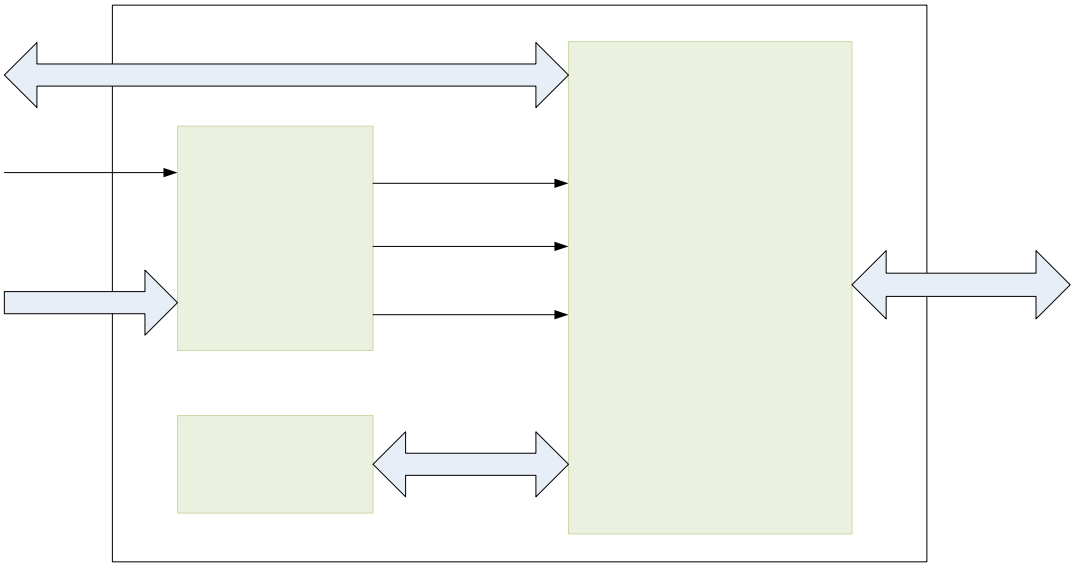
22/3 ! !



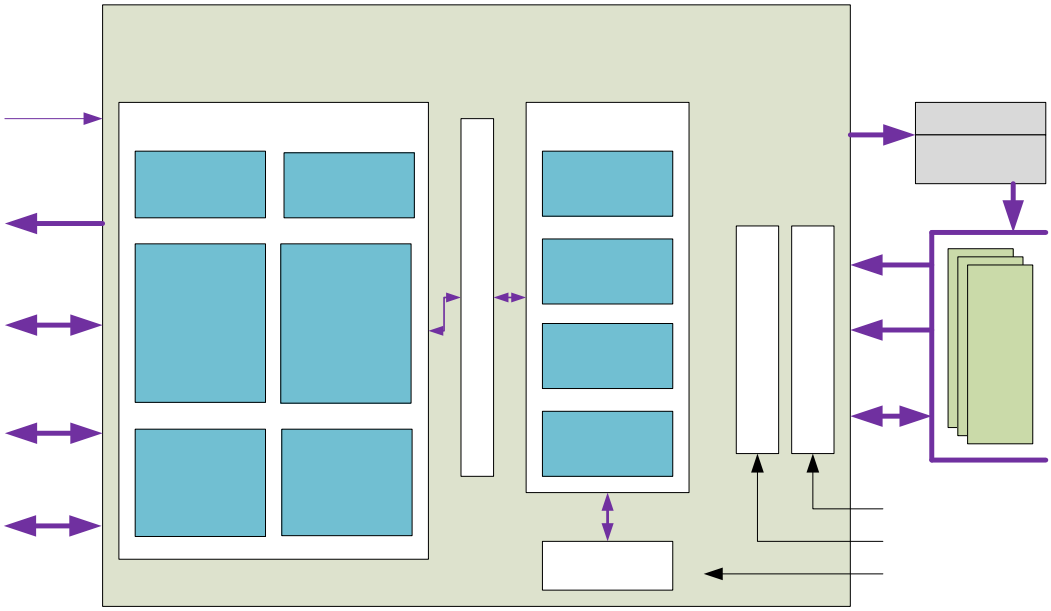


Fig. 11-1 Host Controller Block Diagram

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22/4 ! !

22/4/2 ! ! !

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2/ ! ! !

3/ ! !

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4 ! ! !

!	!	!

!	!	!
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		●
		●
		●

5/ ! ! !

Notes: The FIFO controller does not support simultaneous read/write access from the same port. For debugging purposes, the software may try to write into the FIFO and read back the data; results are indeterminate, since the design does not support read/write access from the same port.

6/ ! ! ! ! ! !

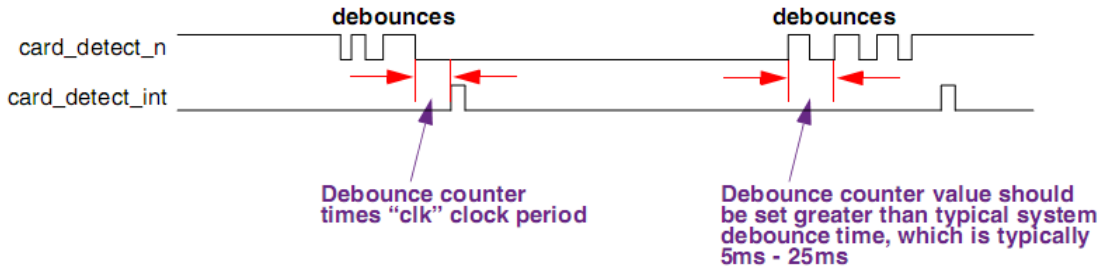

Fig. 11-2 SD/MMC Card-Detect Signal

7/ B! ! !

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22/4/3 ! ! !

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2A ! !

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! ! !

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! ! ! ! !

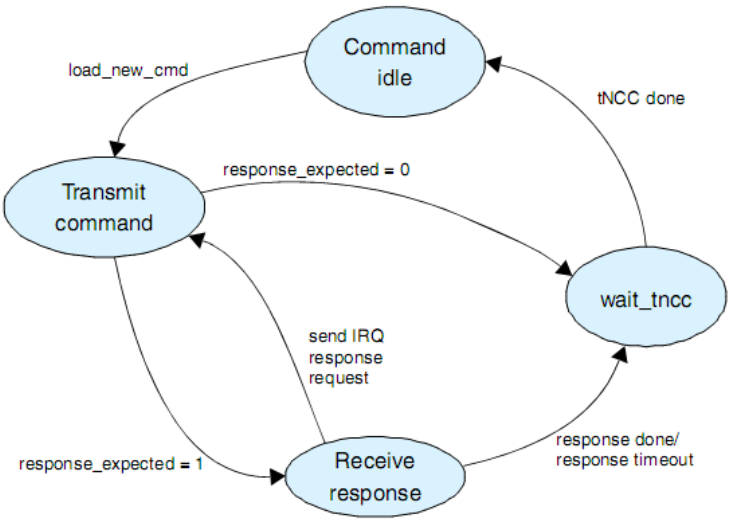

Fig. 11-3 Host Controller Command Path State Machine

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! ! ! !

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! ! ! !

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3/ ! !

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  ! !

Fig. 11-4 Host Controller Data Transmit State Machine

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! !

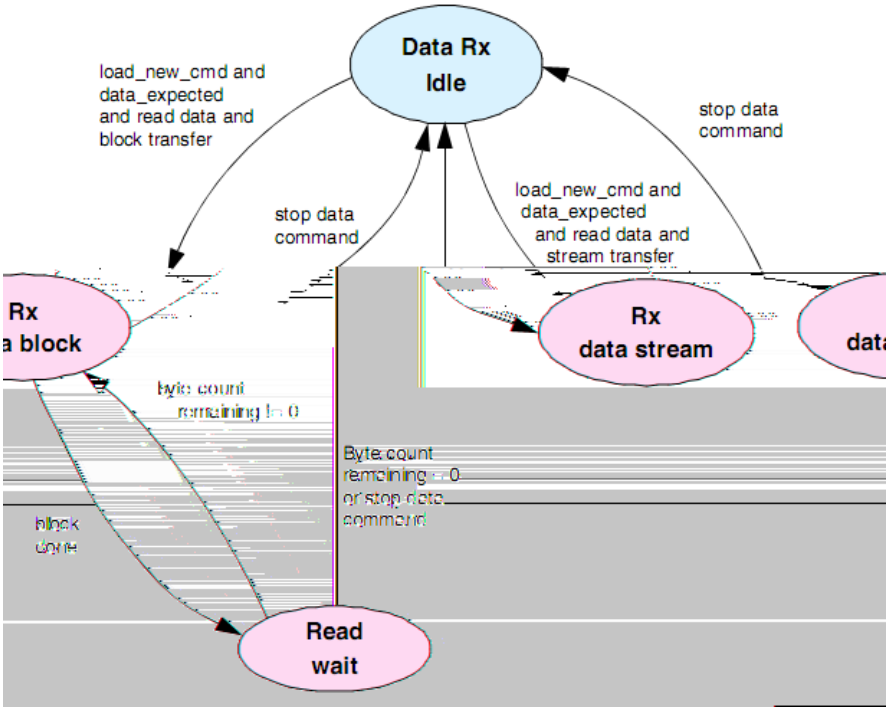

Fig. 11-5 Host Controller Data Receive State Machine

! ! !

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. ! ! !

B . !

Table 11-2 Auto-Stop Generation

! !	! !	! !	! ! !	!
			○	
			○	

! !	! !	! !	! ! !	!

○ *The condition under which the transfer mode is set to block transfer and byte_count is equal to block size is treated as a single-block data transfer command for both MMC and SD cards. If byte_count = n*block_size (n = 2, 3, …), the condition is treated as a predefined multiple-block data transfer command. In the case of an MMC card, the host software can perform a predefined data transfer in two ways: 1) Issue the CMD23 command before issuing CMD18/CMD25 commands to the card – in this case, issue MD18/CMD25 commands without setting the send_auto_stop bit. 2) Issue CMD18/CMD25 commands without issuing CMD23 command to the card, with the send_auto_stop bit set. In this case, the multiple-block data transfer is terminated by an internally-generated auto-stop command after the programmed byte count.*

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4/ . ! ! ! ! ! ! !

Table 11-3 Non-data Transfer Commands and Requirements

!B ! 23 9 !	! 38!	! 41!	! 53!	B ! 24!	B ! 33!	B ! 62!
! !						
!B ! !						
! ! !						
			○			
! !						
			○			

○ *Num_bytes = No. of bytes specified as per the lock card data structure (Refer to the SD specification and the MMC specification)*

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6.1 ! !

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7.1 ! !

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- ■
- ●
  - ■
    - ◆
    - ◆
    - ◆
  - ■
  - ■
- ●
  - ■
    - ◆
    - ◆
    - ◆
  - ■
  - ■
  - ■
  - ■

22/4/4 ! ! !B ! !) B !

2/ B ! !B !

3/ !

●

■

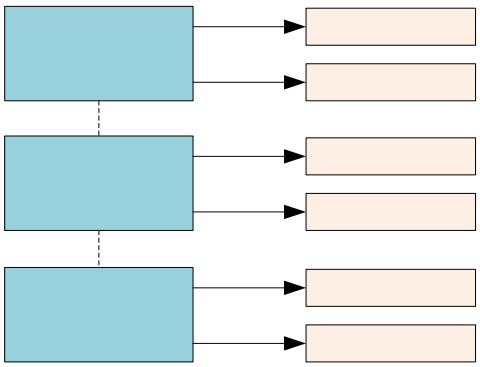

Fig. 11-6 Dual-Buffer Descriptor Structure

■

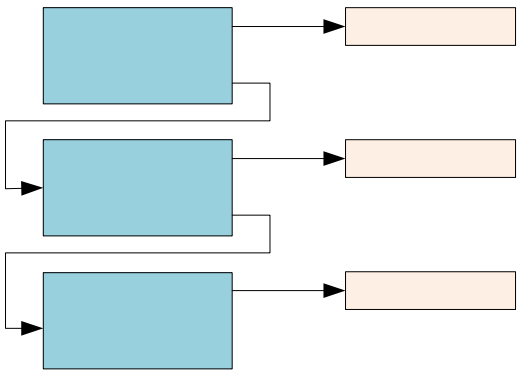

Fig. 11-7 Chain Descriptor Structure

●

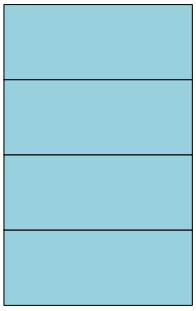

Fig. 11-8 Descriptor Formats for 32-bit AHB Address Bus Width

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Table 11-4 Bits in IDMAC DES0 Element

!	!	!
		● ● ● ● ● ● ●

!	!	!

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Table 11-5 Bits in IDMAC DES1 Element

!	!	!

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Table 11-6 Bits in IDMAC DES2 Element

!	!	!

■

Table 11-7 Bits in IDMAC DES3 Element

!	!	!

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4/ !

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22.5 ! !

22.5.2 ! !

!	!	!	! !	!
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_____				
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!	!	!	! !	!
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*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

22.5.3 ! ! !
_____!

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

!

B!

!	B !	! !	!

!

!	B !	! !	!

!

!	B !	! !	!

_____!

!	**B !**	**! !**	**!**

_____!

!	**B !**	**! !**	**!**

_____B !

!	**B !**	**! !**	**!**

!	B !	! !	!

B !

!	B !	! !	!

!

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

1!

!	B !	! !	!

2!

!	B !	! !	!

3!

!	B !	! !	!

4!

!	B !	! !	!

!

!	B !	! !	!

!	B !	! !	!

_____!

!	B !	! !	!

!	B !	! !	!

B !

!	B !	! !	!

!	B !	! !	!

_____!

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

_____!

!	B !	! !	!

_____!

!	B !	! !	!

_____!

!	B !	! !	!

_____!

!	B !	! !	!

_____!

!	B !	! !	!

[redacted]

!	B !	! !	!

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!	B !	! !	!

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!	B !	! !	!

[redacted]

!	B !	! !	!

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!	B !	! !	!

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!	B !	! !	!

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!	B !	! !	!

!	B !	! !	!

_____!

!	B !	! !	!

_____B ____!

!	B !	! !	!

_____!

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

_____!

!	B !	! !	!

!	B !	! !	!

B !

!	B !	! !	!

B !

!	B !	! !	!

B !

!	B !	! !	!

B !

!	B !	! !	!

!

!	B !	! !	!

_____!

!

Table 11-8 SDMMC Interface Description

! !	!	! !	! !

Notes: I=input, O=output, I/O=input/output, bidirectional

Table 11-9 SDIO Interface Description

! !	!	! !	! !

Notes: I=input, O=output, I/O=input/output, bidirectional

Table 11-10 EMMC Interface Description

! !	!	! !	! !

Notes: I=input, O=output, I/O=input/output, bidirectional

22.7 B ! !

22.7.2 . ! ! . ! !

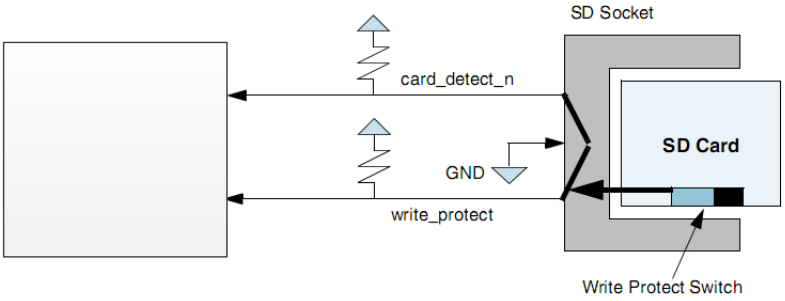

Fig. 11-9 SD/MMC Card-Detect and Write-Protect

22.7.3 0 ! ! !

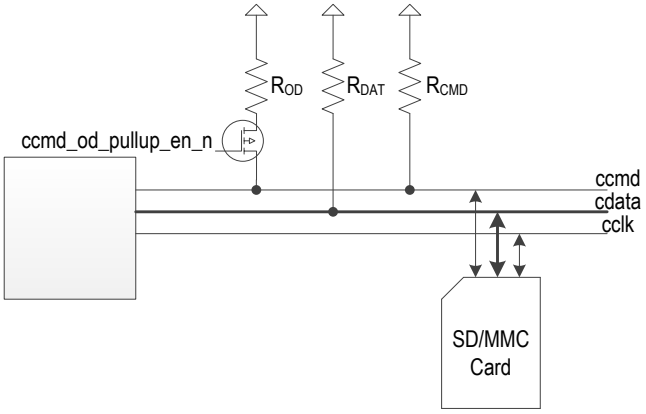

Fig. 11-10 SD/MMC Card Termination

22.7.4 0 ! !

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22/7/5 ! !
2/ !

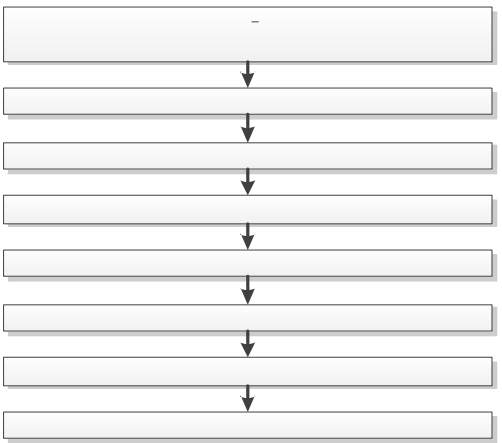

Fig. 11-11 Host Controller Initialization Sequence

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4/ ! !

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5/ ! !

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6/ . ! ! ! ! ! !

Table 11-11 Command Settings for No-Data Command

!	!	!
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7/ ! ! !

8/ . ! ! . ! !

Table 11-12 Command Setting for Single or Multiple-Block Read

!	!	!
.		

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-
-

9/ . ! ! . ! !

Table 11-13 Command Settings for Single or Multiple-Block Write

!	!	!
.		

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-
-

: ⁄ ! !

! 21 ⁄ ! !

22/ ! !

- →
- → → →

23/ ! ! !B ! ! ! ! !

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26.! ! ! !

27.! ! !

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Notes: During a multiple-block data transfer, if a negative CRC status is received from the device, the data path signals a data CRC error to the BIU by setting the data CRC error bit in the SDMMC_RINTSTS register. It then continues further data transmission until all the bytes are transmitted.

22/7/6 ! !

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2/ ! ! !

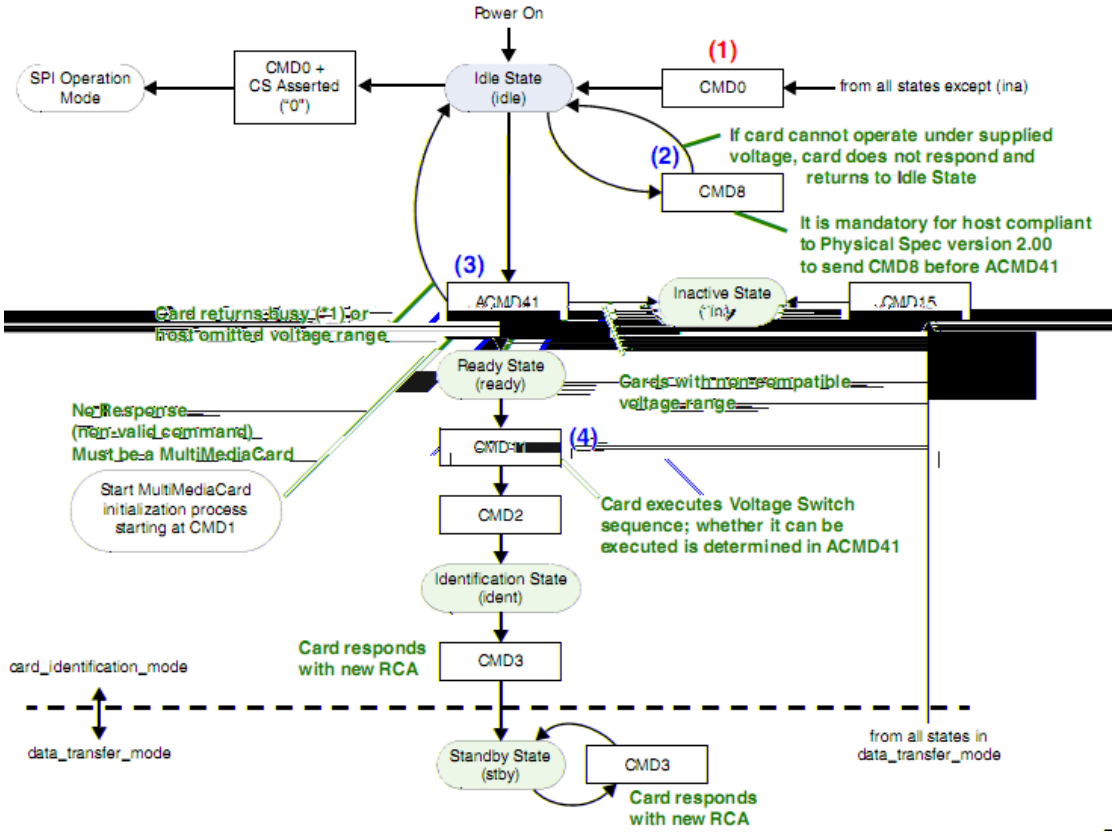
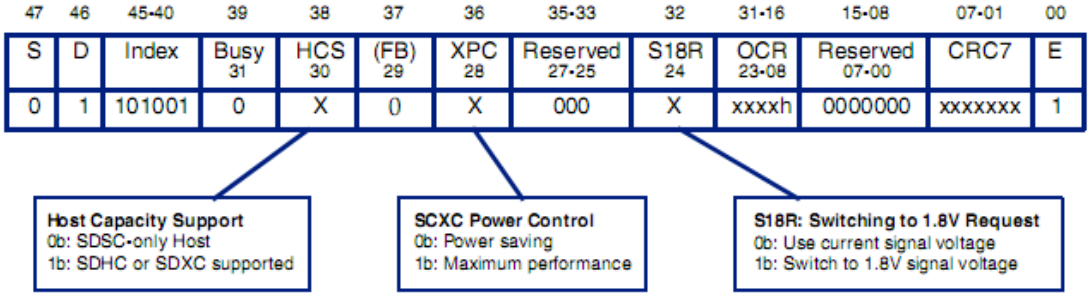


Fig. 11-12 Voltage Switching Command Flow Diagram



47	46	45-40	39	38	37	36	35-33	32	31-16	15-08	07-01	00
S	D	Index	Busy 31	HCS 30	(FB) 29	XPC 28	Reserved 27-25	S18R 24	OCR 23-08	Reserved 07-00	CRC7	E
0	1	101001	0	X	0	X	000	X	xxxxh	0000000	xxxxxxx	1

Host Capacity Support
0b: SDSC-only Host
1b: SDHC or SDXC supported

SCXC Power Control
0b: Power saving
1b: Maximum performance

S18R: Switching to 1.8V Request
0b: Use current signal voltage
1b: Switch to 1.8V signal voltage

Fig. 11-13 ACMD41 Argument

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-
-

47	46	45-40	39	38	37	36-33	32	31-16	15-08	07-01	00
S	D	Index	Busy 31	CCS 30	Rsvd 29	Reserved 28-25	S18R 24	OCR 23-08	Reserved 07-00	CRC7	E
0	0	111111	X	X	0	0000	X	xxxxh	0000000	1111111	1

Busy Status
0b: On Initialization
1b: Initialization complete

Card Capacity Status
0b: SDSC
1b: SCHC or SCXC

S18R: Switching to 1.8V Accepted
0b: Continues current voltage signalling
1b: Ready for switching signal voltage

Fig. 11-14 ACMD41 Response(R3)

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3. ! ! ! !

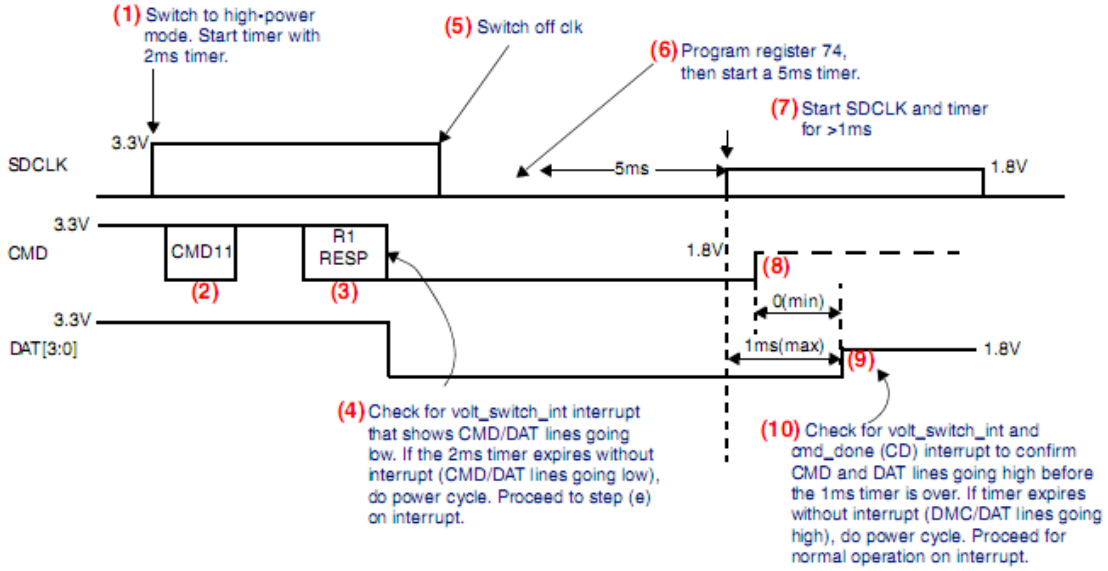

Fig. 11-15 Voltage Switch Normal Scenario

Note: Before doing a power cycle, switch off the card clock by programming SDMMC_CLKENA register

Note: This interrupt must be cleared once this interrupt is received. Additionally, this interrupt should not be masked during the voltage switch sequence.

Note: The card checks voltages of its own regulator output and host signals to ensure they are less than 2. 5V. Errors are indicated by (1) and (2).

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Note: No other CMD should be driven before the voltage switching operation is completed and Command Done is received.

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22/7/7 ! !
2/5. ! ! !

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-

3/9. ! ! ! !

4/ 5/6! ! B ! !

Notes: The Host Controller does not support a START bit duration higher than one clock cycle. START bit durations of one or less than one clock cycle are supported and can be defined at the time of startup by programming the SDMMC_EMMCDDR_REG register.

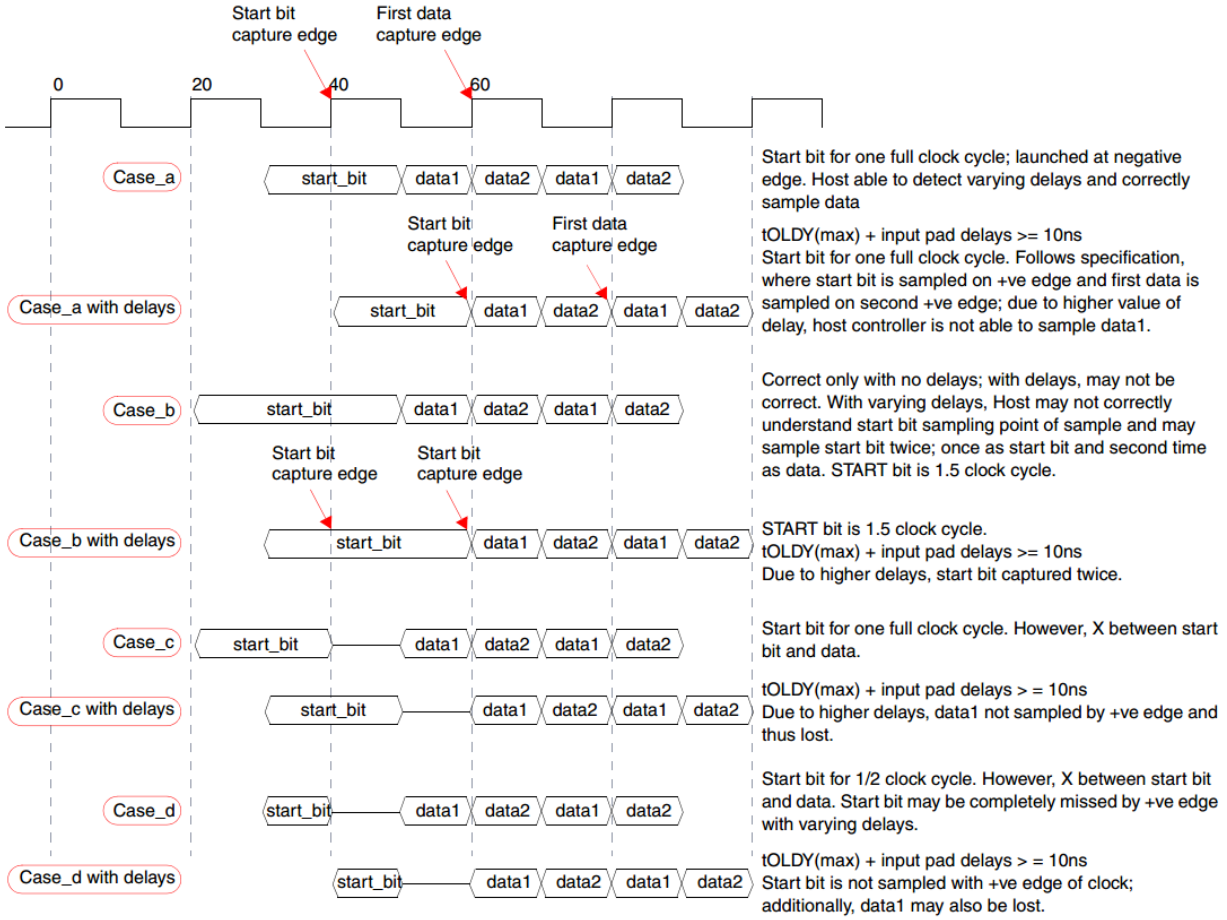

Fig. 11-17 CASES for eMMC 4.5 START bit

5/ ! 0 ! ! 61! ! 23!

Note: The voltage register should not be programmed to 0 while switching from DDR50 to SDR12, since the card is still operating in 1.8V mode after receiving CMD0.

22/7/8 0 ! ! !

0 ! ! ! !

-
-

Note: The above steps are required only if a transfer is in process.

Note: For backward compatibility, the RST_N signal is temporarily disabled in the card by default. The host may need to set the signal as either permanently enabled or permanently disabled before it uses the card.

22/7/9 ! !

-
-

2/ ! ! ! !

-

-

3/ ! ! ! ! ! !

Table 11-14 PBL and Watermark Levels

!) ! ! !	0 ! ! !

-
  -
  -
-
  -
  -
-
-

! 0 ! !

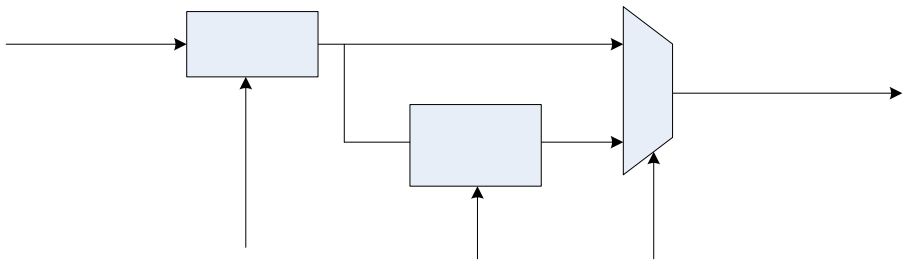

Fig. 11-18 Clock Generation Unit

Table 11-15 Configuration for SDMMC Clock Generation

! !	!	!	!

Table 11-16 Configuration for SDIO Clock Generation

! !	!	!	!

! !	!	!	!

Table 11-17 Configuration for EMMC Clock Generation

! !	!	!	!

22/7/21 ! ! !

-
-

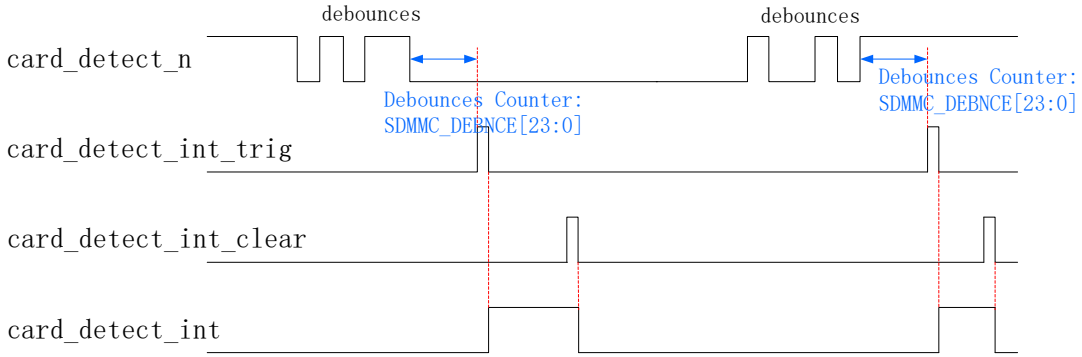

Fig. 11-19 Card Detection Method 2

●

Table 11-18 Register for SDMMC Card Detection Method 3

! !	!	!	!

●

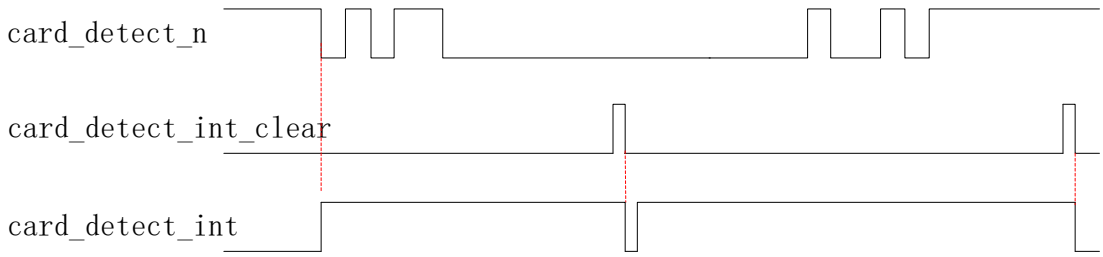

Fig. 11-20 Card Detection Method 4

22/7/22 ! ! ! B !

-

-

22/7/23 ! !

!23 ! ! !) !

23/2 !

-
-
-
-
-
-
-

23/3 ! !

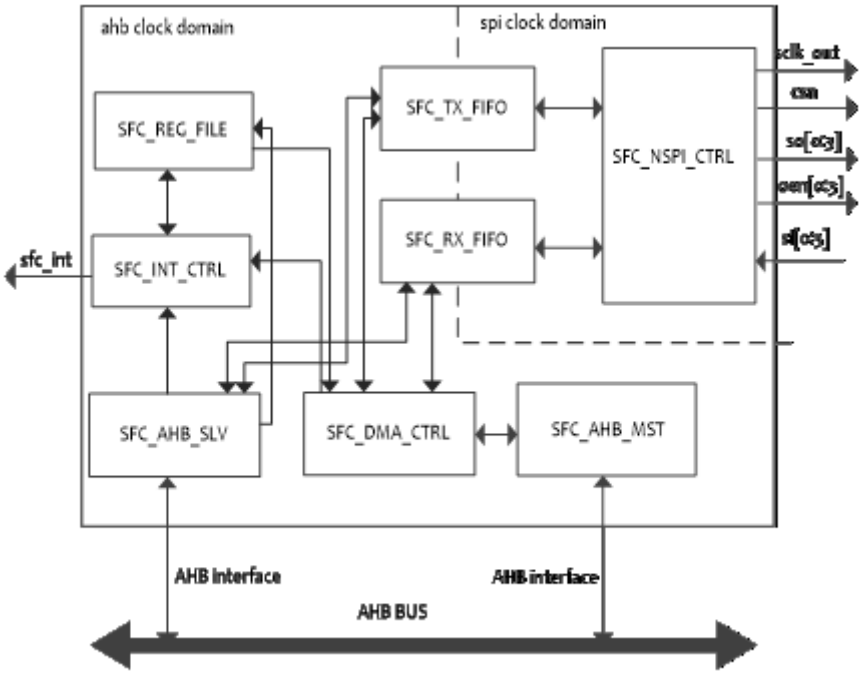

Fig. 12-1 SFC Architecture

23/4 ! !

23/4/2 !B ! !

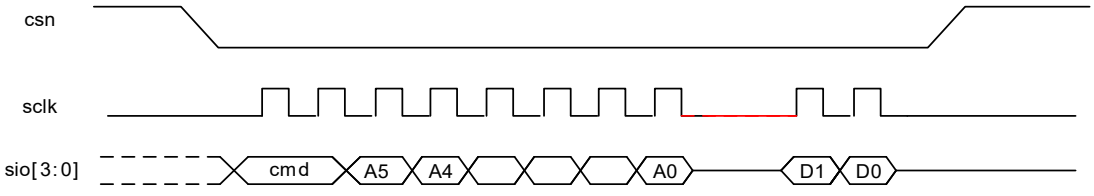

Fig. 12-2 Idle cycles

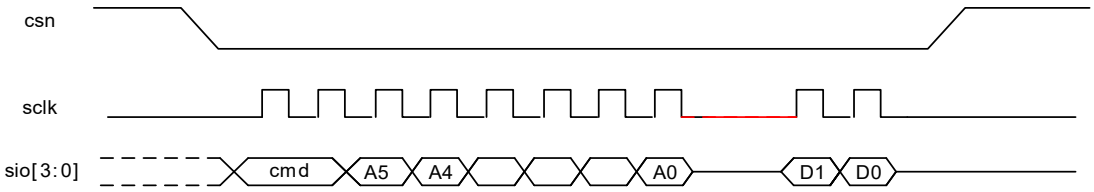

Fig. 12-3 SPI mode

23.5 ! !

23.5.2 ! !

!	!	!	! !	!
_____				
_____				
_____				
_____				
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_____				
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_____				
_____				
_____				
_____				
_____				
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_____				
_____				
_____				
_____				

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

23.5.3 ! ! !

_____!

!	B !	! !	!

!	B !	! !	!

_____!

!	B !	! !	!

!	B !	! !	!

_____!

!	B !	! !	!

_____!

!	B !	! !	!

_____!

!	B !	! !	!

_____B !

!	B !	! !	!

B !

!	B !	! !	!

!

!	B !	! !	!

!	B !	! !	!

_____!

!	B !	! !	!

_____!

!	B !	! !	!

_____!

!	B !	! !	!

_____!

!	**B !**	**! !**	**!**

_____!

!	**B !**	**! !**	**!**

_____B !

!	**B !**	**! !**	**!**

_____BB !

!	**B !**	**! !**	**!**

_____!

!	B !	! !	!

B !

!	B !	! !	!

B B!

!	B !	! !	!

23/6 ! !

Table 12-1 SFC interface description

! !	!	! !	! !

! !	!	! !	! !

Notes: I=input, O=output, I/O=input/output, bidirectional.

23/7 B ! !

23/7/2 B ! ! ! ! !) . B! !

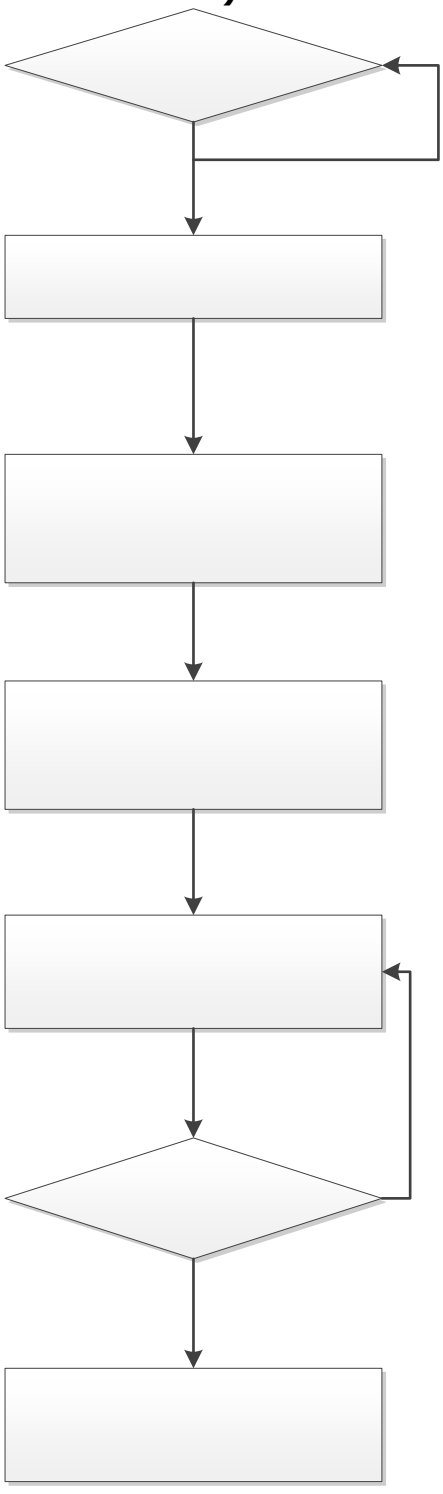

Fig. 12-4 Slave mode write

23/7/3 B ! ! ! ! !) . B! !

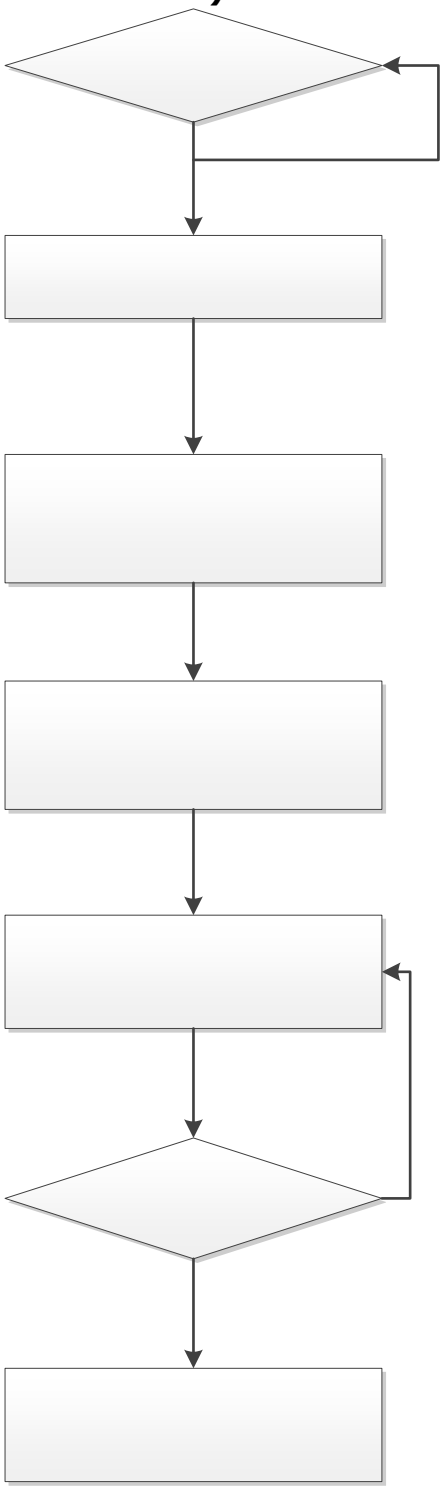

Fig. 12-5 Slave mode read

23.7.4 B ! B! ! !) B! !

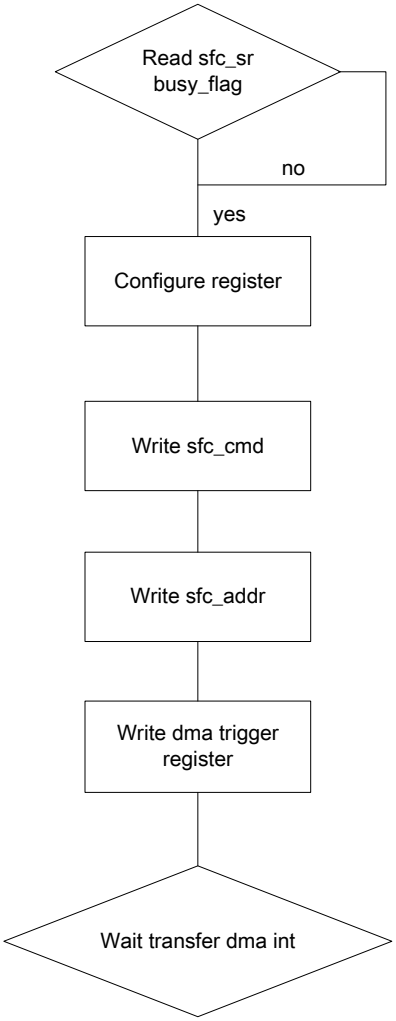

Fig. 12-6 Master mode flow

23.7.5 ! ! ! ! !

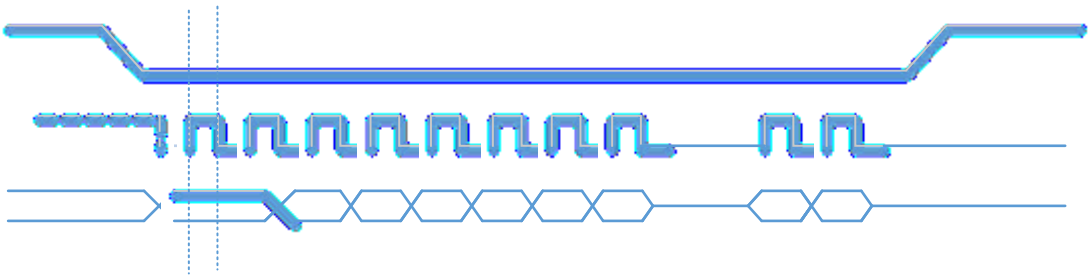

Fig. 12-7 SPI mode

23.7.6 ! !

!24 ! B !

24/2 !

24/2/2 ! !

- ■
- ■
- ■

- ■
- ■

24/3 ! !

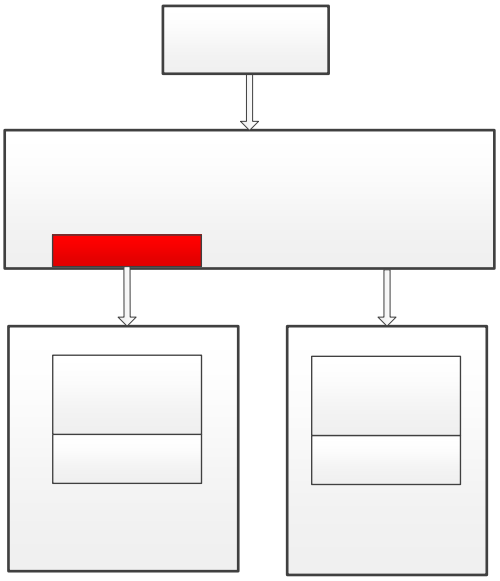

Fig. 13-1 Embedded SRAM block diagram

24/4 ! !

24/4/2 B ! ! ! ! B !

24/4/3 B ! ! ! ! B !

24/4/4 ! B ! ! !

!25 !

25/2 !

25/3 ! !!

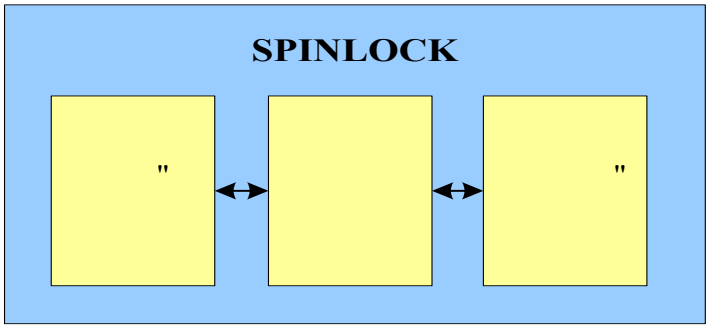

Fig. 14-1 Spinlock Block Diagram

-
-
-

25/4 ! !

25/5 ! !

25/5/2 !B ! !

25/5/3 ! !

!	!	!	! !	!

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

25/5/4 ! ! !

!

!	B !	! !	!

25/6 ! !

!26 ! ! !) !

26/2 !

26/3 ! !

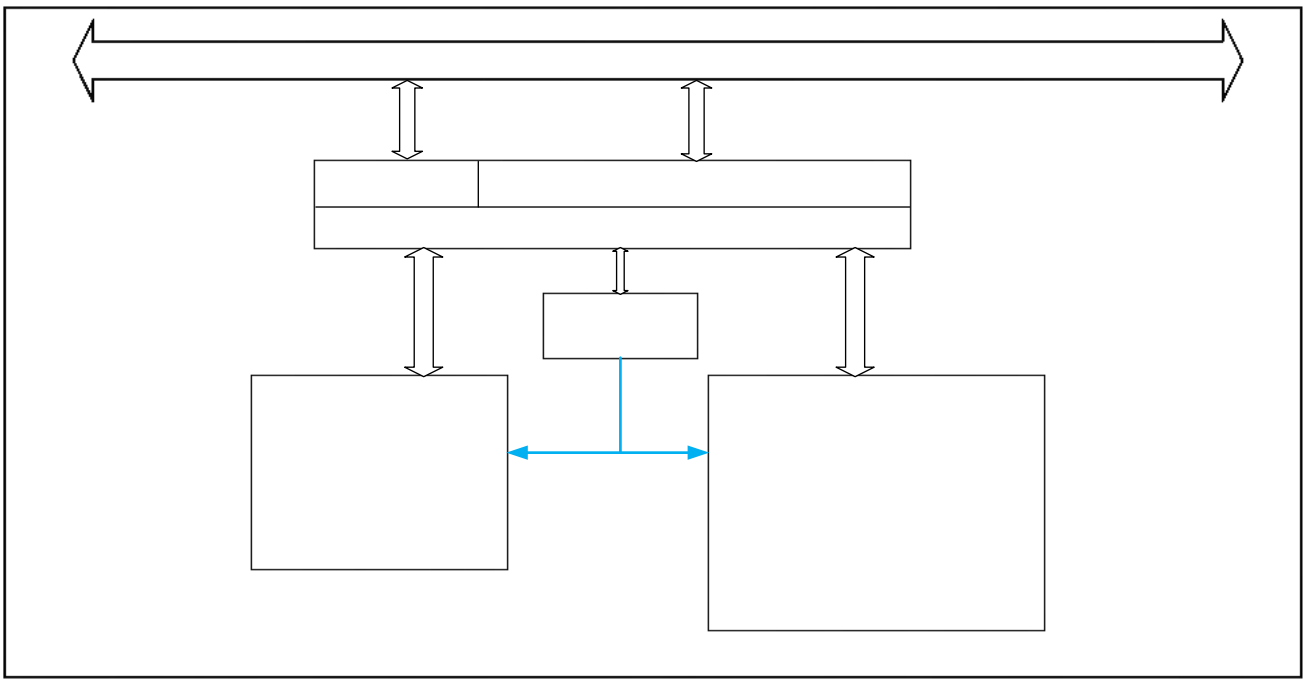

Fig. 15-1 NPU Block Diagram

26.4 ! !

26.4.2 ! !

26.4.3 ! !

26.4.4 ! ! !

26.4.5 ! ! !

26/5 ! !

26/5/2 !B ! !

Table 15-1 NPU Address Mapping

!B 23 9 !	!	B ! !	!B ! !

!27 ! !) !

27 /2 !

27 /3 ! !

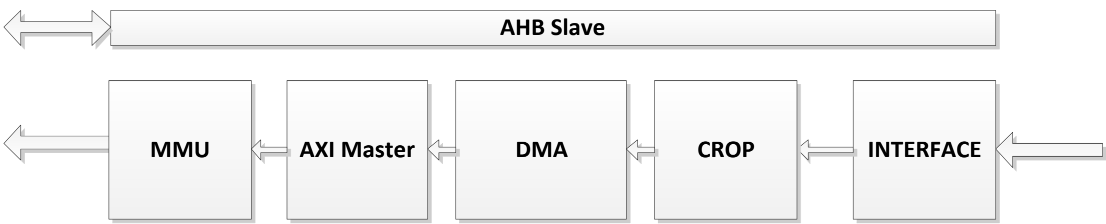

Fig. 16-1 VIP Block Diagram

27 /4 ! !

27 /4 /2 !

27 /4 /3 !

27 /4 /4 B!

27/4/5 B ! !

27/4/6 !

27/5 ! !

27/5/2 ! !

!			!	!
_____				
_____				
_____				
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!			!	!

!			!	!

!			!	!
_____				
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_____				
_____				
_____				

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

27/5/3 ! ! !
_____!

!	B !	! !	!

_____!

!	B !	! !	!

!	B !	! !	!

B !

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!
			:

B !

!	B !	! !	!

1 B !

!	B !	! !	!

1 B !

!	B !	! !	!

2 B !

!	B !	! !	!

2 B !

!	B !	! !	!

_____!

!	B !	! !	!

_____!

!	B !	! !	!

_____!

!	B !	! !	!
			菔 蔔

_____!

!	B !	! !	!

_____!

!	B !	! !	!

B !

!	B !	! !	!

!

!	B !	! !	!

B B !

!	B !	!	!	!

!	B !	! !	!

1 2!

!	B !	! !	!
			,

2 1!

!	B !	! !	!

2 2!

!	B !	! !	!
			,

3 1!

!	B !	! !	!

3 2!

!	B !	! !	!
			,

4 1!

!	B !	! !	!

4 2!

!	B !	! !	!
			,

B !

!	B !	! !	!

B 1 B 1!

!	B !	! !	!

B 2 B 1!

!	B !	! !	!

B 1 B 1!

!	B !	! !	!

B 2 B 1!

!	B !	! !	!

B 1 1!

!	B !	! !	!

B 2 1!

!	B !	! !	!

B 1 1!

!	B !	! !	!

B 2 1!

!	B !	! !	!

B 1 B 2!

!	B !	! !	!

B 2 B 2!

!	B !	! !	!

B 1 B 2!

!	B !	! !	!

B 2 B 2!

!	B !	! !	!

B 1 2!

!	B !	! !	!

B 2 2!

!	B !	! !	!

B 1 2!

!	B !	! !	!

B 2 2!

!	B !	! !	!

B 1 B 3!

!	B !	! !	!

B 2 B 3!

!	B !	! !	!

B 1 B 3!

!	B !	! !	!

B 2 B 3!

!	B !	! !	!

B 1 3!

!	B !	! !	!

B 2 3

!	B !	! !	!

B 1 3!

!	B !	! !	!

B 2 3!

!	B !	! !	!

B 1 B 4!

!	B !	! !	!

B 2 B 4!

!	B !	! !	!

B 1 B 4!

!	B !	! !	!

B 2 B 4!

!	B !	! !	!

B 1 4!

!	B !	! !	!

B 2 4!

!	B !	! !	!

B 1 4!

!	B !	! !	!

B 2 4!

!	B !	! !	!

!

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

B !

!	B !	! !	!

!	B !	! !	!

1 2!

!	B !	! !	!
			蔹 蔔
			蔹 蔔

3 4!

!	B !	! !	!
			蔹 蔔
			蔹 蔔

1 2!

!	B !	! !	!

3 4!

!	B !	! !	!

1 B !

!	B !	! !	!
			,

2 B !

!	B !	! !	!
			,

3 B !

!	B !	! !	!
			,

4 B !

!	B !	! !	!
			,

B !

!	B !	! !	!

B !

!	B !	! !	!

B !

!	B !	!	!	!

B B B !

!	B !	!	!	!

B !

!	B !	!	!	!

B B !

!	B !	!	!	!

B !

!	B !	!	!	!

!
!
B !

!	B !	! !	!

B !

!	B !	! !	!

B B !

!	B !	! !	!

27/6 ! !

Table 16-1 VIP Interface Description

! !	!	! !	! !

! !	!	! !	! !
			!

27 /7 B ! !

27 /7 /2 !B

27 /7 /3 !B

!28 B ! ! !

28/2 !

28/2/2 !

-
-

28.3 ! !

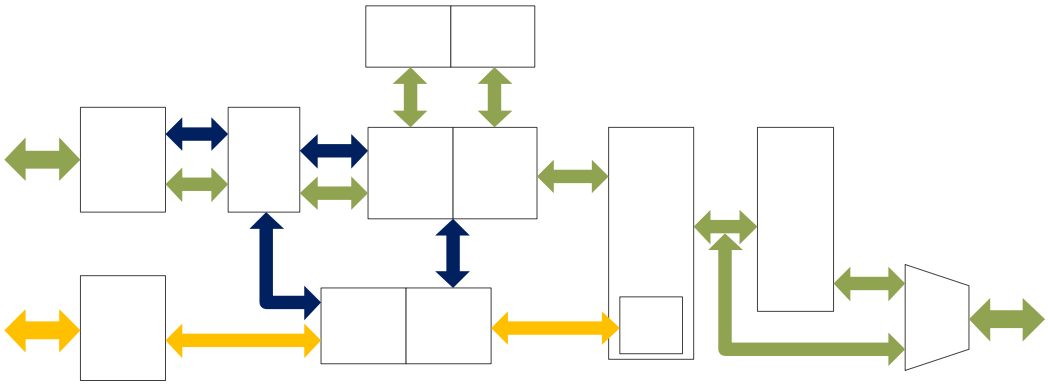

Fig. 17-1 GMACArchitecture

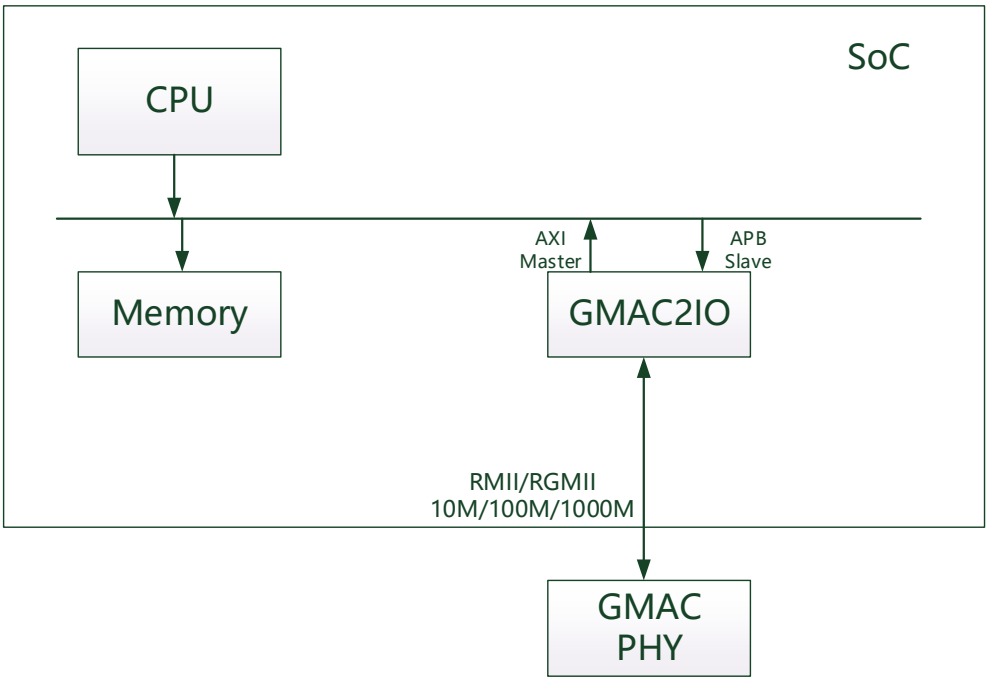

Fig. 17-2 GMAC Architecture

-

28.4 ! !

28.4.2 ! !

Fig. 17-3 MAC Block Diagram

28.4.3 ! ! ! !

-
-

! ! !

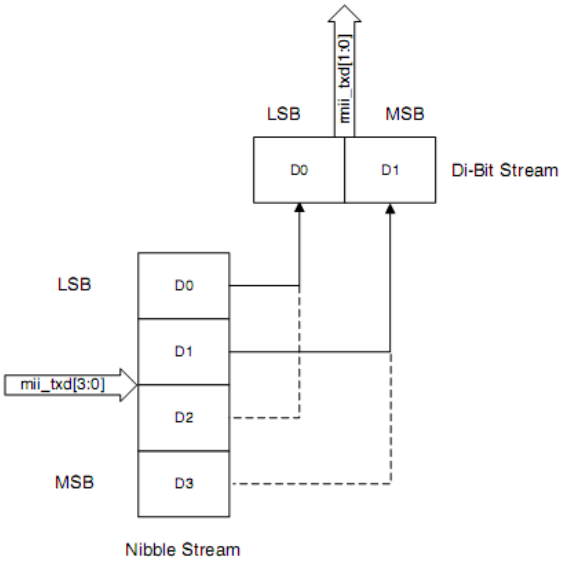

Fig. 17-4 RMII transmission bit ordering

! ! ! !

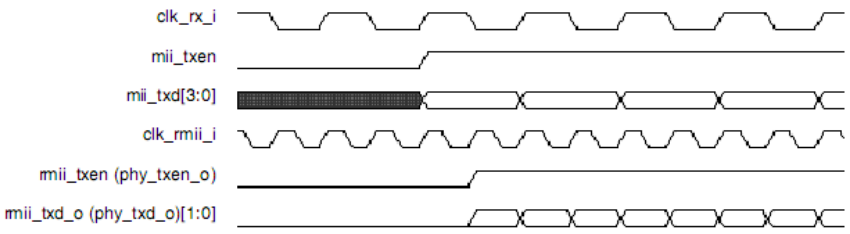

Fig. 17-5 Start of MII and RMII transmission in 100-Mbps mode

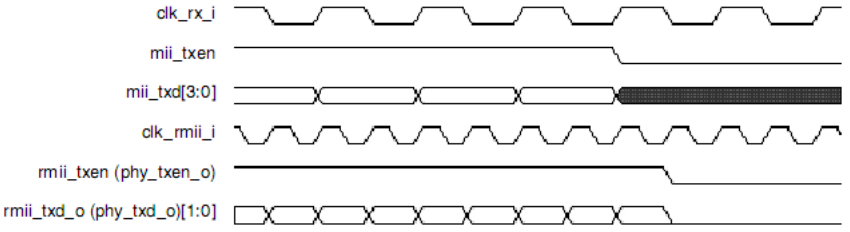

Fig. 17-6 End of MII and RMII Transmission in 100-Mbps Mode

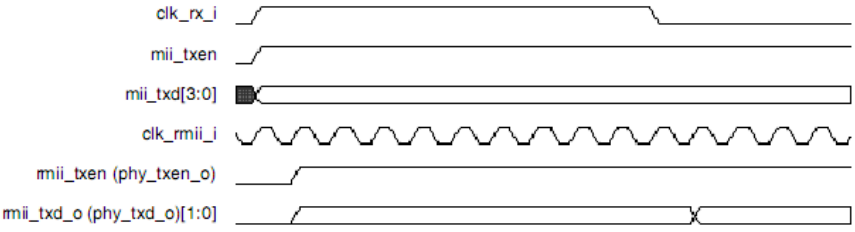

Fig. 17-7 Start of MII and RMII Transmission in 10-Mbps Mode

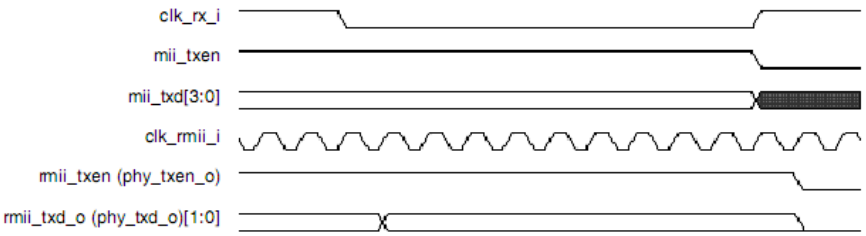

Fig. 17-5 End of MII and RMII Transmission in 10-Mbps Mode

! ! !

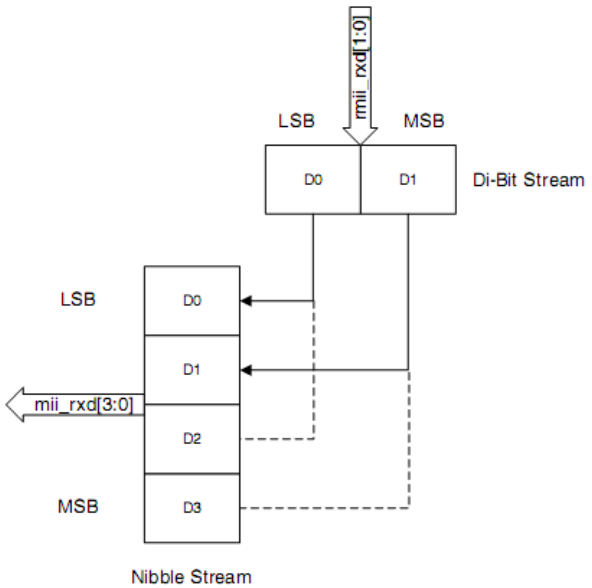

Fig. 17-6 RMII receive bit ordering

28/4/4 ! !

-
-

-

28/4/5 ! !

!!!!!! !!!!! ! !

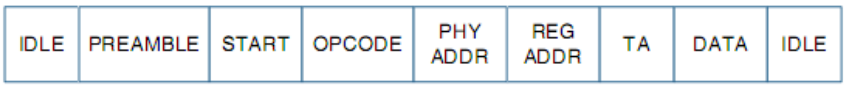

Fig. 17-7 MDIO frame structure

28/4/6 ! ! !

! . ! ! !

! ! !

...

28/4/7 B ! ! !

28.5 ! !

28.5.2 ! !

!	!	!	! !	!
_____				
_____				
_____				
_____				
_____				
_____				
_____				
_____				

!	!	!	! !	!
_____				
_____				
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_____				

!	!	!	! !	!
_____				
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_____				
_____				

!	!	!	! !	!

!	!	!	! !	!
_____				
_____ ___				
_____ __				
_____ ___				
_____ _____				
_____ ____				
_____ ____				
_____				
_____				
_____ ___				
_____ __				

!	!	!	! !	!

!	!	!	! !	!

!	!	!	! !	!
_____				
_____				
_____ ___				
_____ ___				
_____ _____				
_____ _____				

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

28/5/3 ! ! !
B B !

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

B B !

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

B B B !

!	B !	! !	!

B B B !

!	B !	! !	!

B B !

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

B B B!

!	B !	! !	!

B !

!	B !	! !	!

!	B !	! !	!

B !

!	B !	! !	!

!	B !	! !	!

B B!

!	B !	! !	!

!	B !	! !	!

B B !

!	B !	! !	!

!	B !	! !	!

B B !

!	B !	! !	!

B B B 1 !

!	B !	! !	!

B B B 1 !

!	B !	! !	!

B B !

!	B !	! !	!

B B B !

!	B !	! !	!

B B B !

!	B !	! !	!

B B B B !

!	B !	! !	!

B B !

!	B !	! !	!

!	B !	! !	!

B B!

!	B !	! !	!

B !

!	B !	! !	!

!	B !	! !	!

B !

!	B !	! !	!

!	B !	! !	!

B !

!	B !	! !	!

B !

!	B !	! !	!

!	B !	! !	!

B !

!	B !	! !	!

!	B !	! !	!

B !

!	B !	! !	!

B !

!	B !	! !	!

B !

!	B !	! !	!

B B !

!	B !	!	!	!

B !

!	B !	!	!	!

B !

!	B !	!	!	!

B !

!	B !	!	!	!

B !

!	B !	!	!	!

B !

!	B !	!	!	!

B !

!	B !	!	!	!

B !

!	B !	!	!

B !

!	B !	!	!

B !

!	B !	!	!

B !

!	B !	!	!

!	B !	! !	!

B !

!	B !	! !	!

!	B !	! !	!

B 5 !

!	B !	! !	!

B 5 !

!	B !	! !	!

B 7 !

!	B !	! !	!

B 7 !

!	B !	! !	!

B !

!	B !	! !	!

B !

!	B !	!	!	!

B !

!	B !	!	!	!

B 5 !

!	B !	!	!	!

B 7 !

!	B !	!	!	!

B !

!	B !	!	!	!

B !

!	B !	!	!	!

B !

!	B !	! !	!

B !

!	B !	! !	!

!	B !	! !	!

B B !

!	B !	! !	!

B B !

!	B !	! !	!

B B !

!	B !	! !	!

B B !

!	B !	! !	!

B B !

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

B !

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

B B!

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

B !

!	B !	! !	!

B !

!	B !	! !	!

B B !

!	B !	! !	!

!	B !	! !	!

!	B !	!	!	!

B B B !

!	B !	!	!	!

B !

!	B !	!	!	!

B !

!	B !	!	!	!

B B !

!	B !	!	!	!

B B !

!	B !	! !	!

28/6 ! !

Table 17-1 RGMII Interface Description

! !!	!	! !	! !

Notes: I=input, O=output, I/O=input/output, bidirectional

28.7 B ! !

28.7.2 !

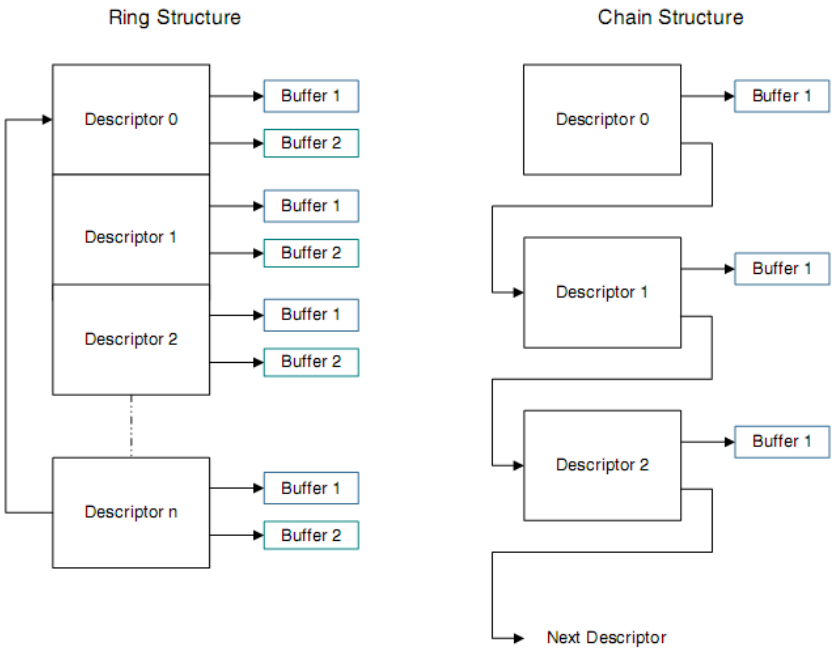

Fig. 17-8 Descriptor Ring and Chain Structure

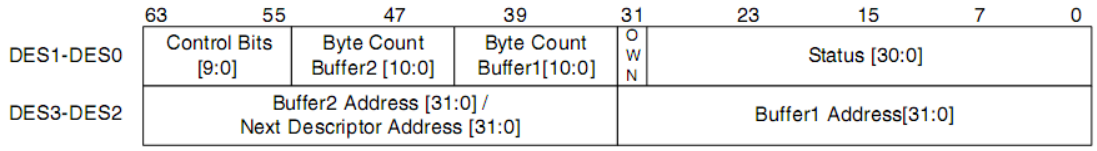

Fig. 17-9 Rx/Tx Descriptors definition

28.7.3 ! !

!

! !1!) 1 !

Table 17-2 Receive Descriptor 0

!	!
	• • • • • • • • •

!	!
	≠

!

! !2!) 2 !

Table 17-3 Receive Descriptor 1

!	!

! !3!) 3 !

Table 17-4 Receive Descriptor 2

!	!

! !4!) 4 !

Table 17-5 Receive Descriptor 3

!	!

28/7/4 ! !

! !1!) 1 !

Table 17-6 Transmit Descriptor 0

!	!
	• • • • • • • •

!	!

! !2!) 2 !

Table 17-7 Transmit Descriptor 1

!	!

!	!
	• • • •

! !3!) 3 !

Table 17-8 Transmit Descriptor 2

!	!

! !4!) 4 !

Table 17-9 Transmit Descriptor 3

!	!

28/7/5 ! !
B! ! ! ! !

B ! !

! ! ! ! !

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-
-

! ! ! !

28/7/6 !B !

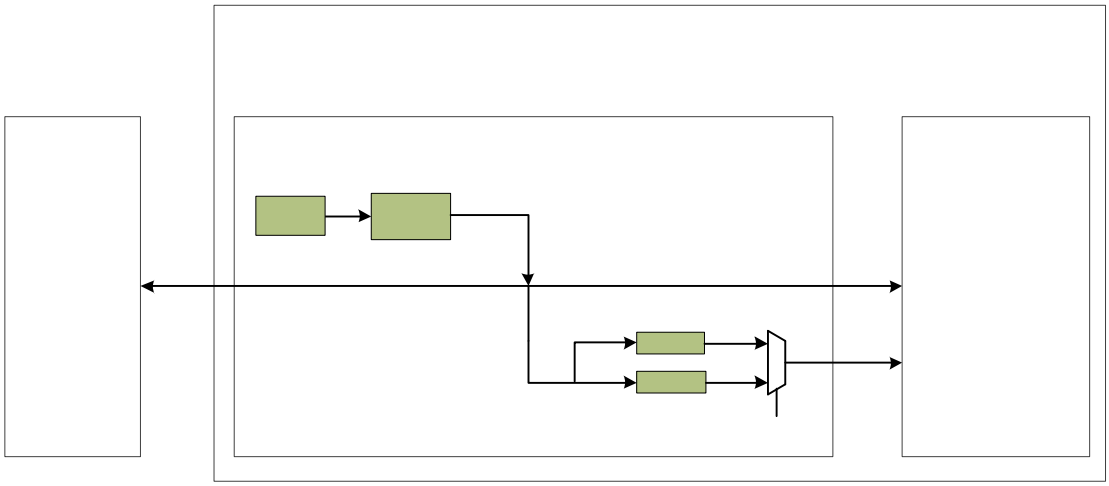

Fig. 17-10 RMII clock architecture when clock source from CRU

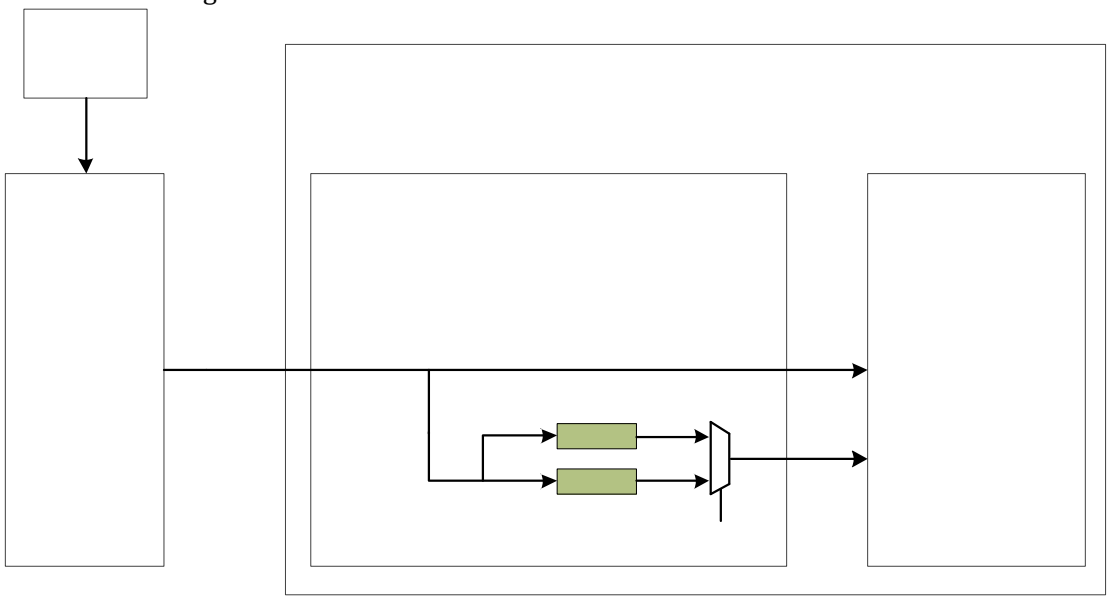

Fig. 17-11 RMII clock architecture when clock source from external OSC

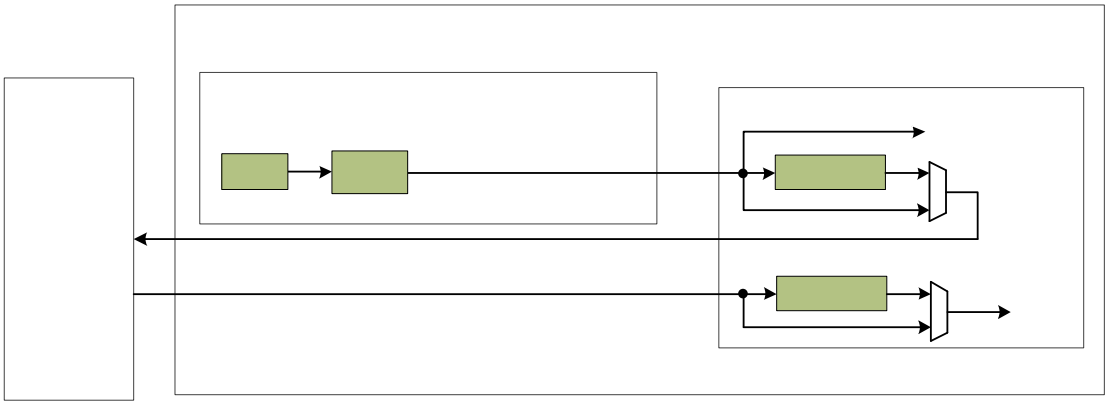

Fig. 17-12 RGMII clock architecture when clock source from CRU

28/7 /7 ! . ! ! ! !

wkupfmfilter_reg0	Filter 0 Byte Mask							
wkupfmfilter_reg1	Filter 1 Byte Mask							
wkupfmfilter_reg2	Filter 2 Byte Mask							
wkupfmfilter_reg3	Filter 3 Byte Mask							
wkupfmfilter_reg4	RSVD	Filter 3 Command	RSVD	Filter 2 Command	RSVD	Filter 1 Command	RSVD	Filter 0 Command
wkupfmfilter_reg5	Filter 3 Offset		Filter 2 Offset		Filter 1 Offset		Filter 0 Offset	
wkupfmfilter_reg6	Filter 1 CRC - 16				Filter 0 CRC - 16			
wkupfmfilter_reg7	Filter 3 CRC - 16				Filter 2 CRC - 16			

Fig. 17-13 Wake-Up Frame Filter Register

Filter i Byte Mask

Filter i Command

Filter i Offset

Filter i CRC-16

28/7/8 ! ! ! . !

28/7/9 ! ! !

B 3 !	
! !	! !

!29 ! ! ! ! !

29/2 !

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-

-
-
-

29/3 ! !

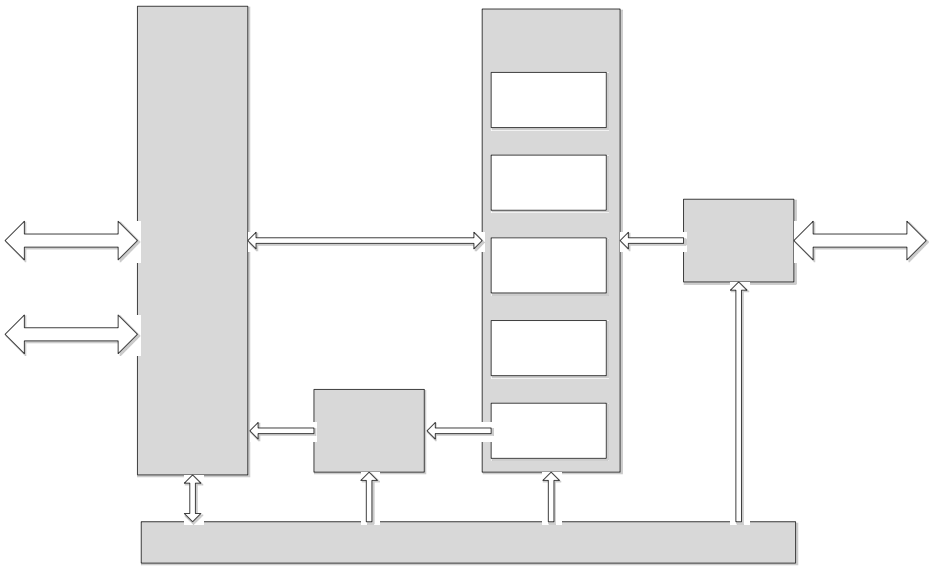

Fig. 18-1 PDM Block Diagram

! !

! !!

!!

! !

B ! !

29/4 ! !

29/4/2 B ! !

SYSTEM_RAMs 错误 未找到引用源。

29/4/3 ! !

错误 未找到引用源。 错误 未找到引用源。

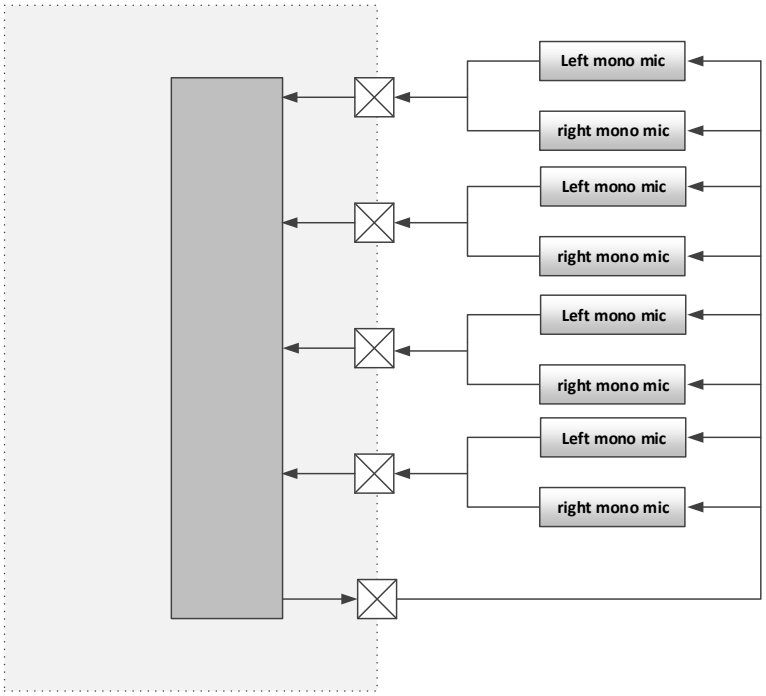

Fig. 18-2 PDM with Eight Mono MIC

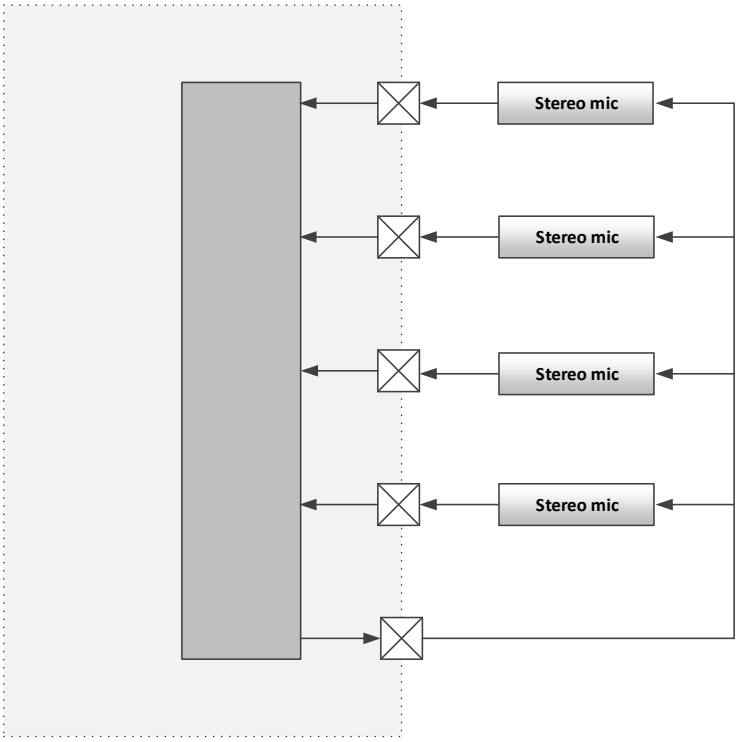

Fig. 18-3 PDM with Four Stereo MIC

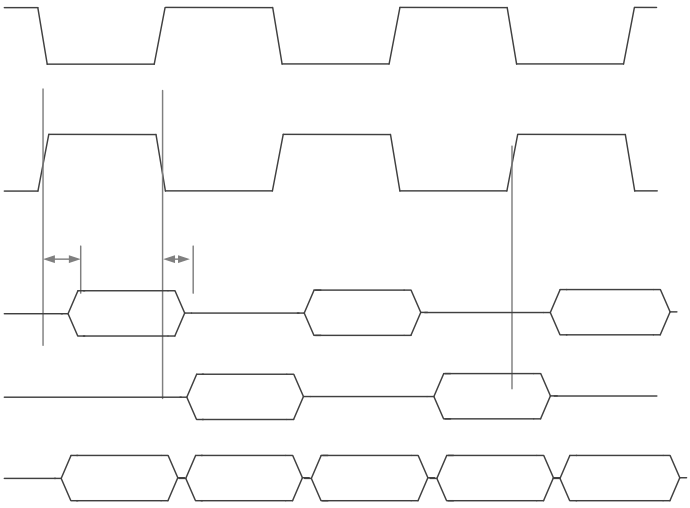

Fig. 18-4 PDM interface diagram with external MIC

29.4.4 ! !

29.4.5 ! !

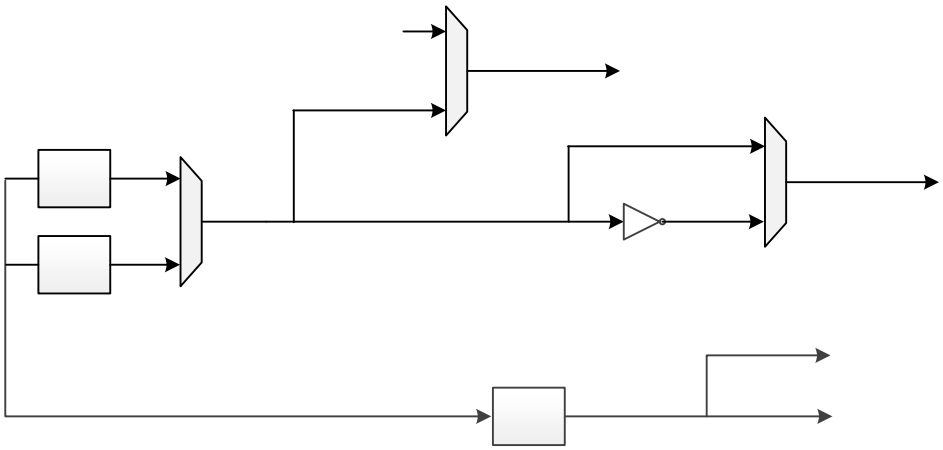

Fig. 18-5 PDM Clock Structure

Table 18-1 Relation between PDM_CLK and sample rate

29.5 ! !

29.5.2 ! !

!	!	!	! !	!
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!	!	!	! !	!
_____				
_____				
_____				
_____				
_____				
_____				

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

29/5/3 ! ! !
_____!

!	B !	! !	!

_____1!

!	B !	! !	!

!	B !	! !	!

2!

!	B !	! !	!

_____!

!	B !	! !	!

_____!

!	B !	! !	!

!	B !	! !	!

!

!	B !	! !	!

B !

!	B !	! !	!

!	B !	! !	!

!

!	B !	! !	!

!

!	B !	! !	!

!

!	B !	! !	!

B B !

!	B !	!	!	!

B B1 !

!	B !	!	!	!

B B1 !

!	B !	!	!	!

B B2 !

!	B !	!	!	!

B B2 !

!	B !	!	!	!

B B3 !

!	B !	!	!	!

B B3 !

!	B !	!	!	!

B B4 !

!	B !	! !	!

B B4 !

!	B !	! !	!

B B B !

!	B !	! !	!

!

!	B !	! !	!

!

!	B !	! !	!

29/6 ! !

Table 18-2 PDM Interface Description

! !	!	! !	! !

Notes: I=input, O=output, I/O=input/output, bidirectional
When use IO_I2S08CHmclk_VCCIO2gpio2a4, the output enable is control by pmic_sleep

29 /7 B ! !

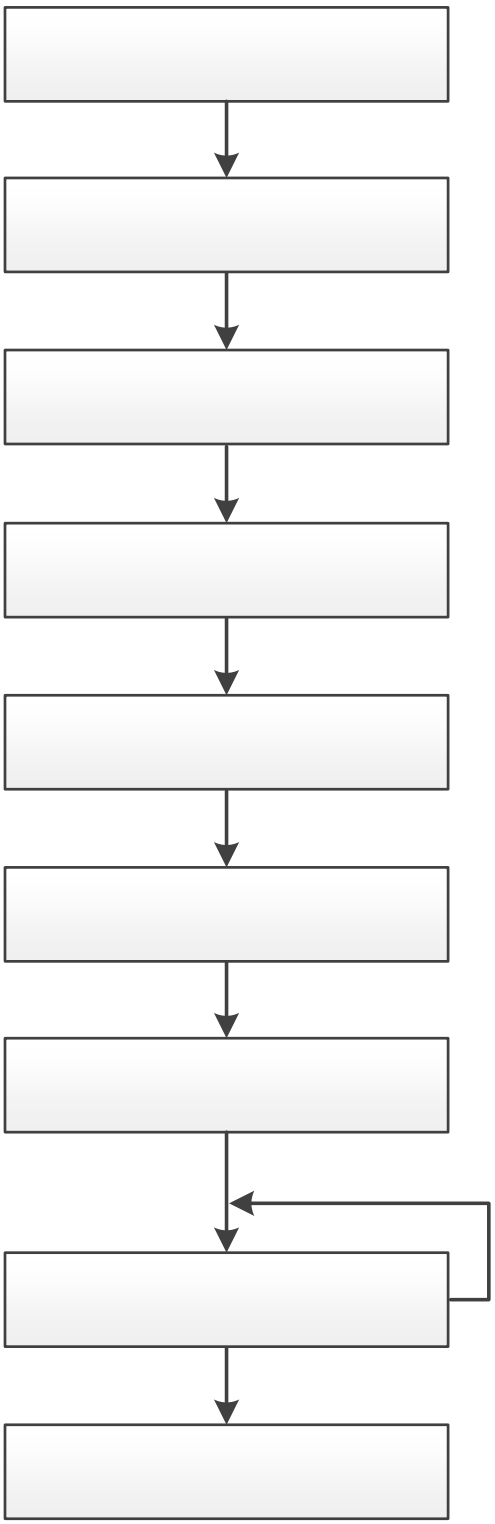

Fig. 18-6 PDM operation flow

!2: 3 !3. !

2: /2 !

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-
-
-
-
-
-
-
-

2: /3 ! !

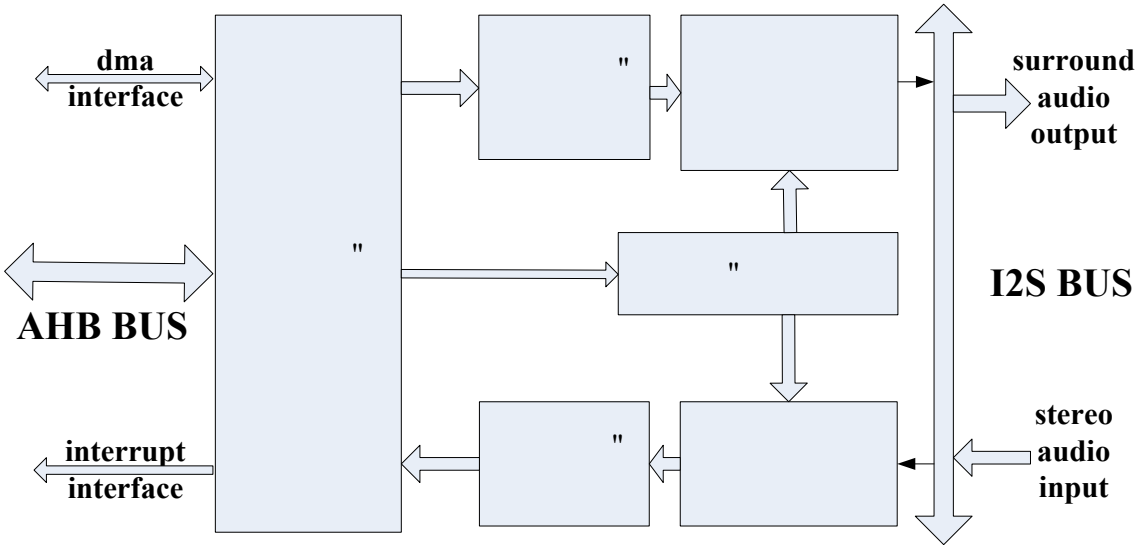

Fig. 19-1 I2S/PCM controller (2 channel) Block Diagram

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! !!

!

!!

! !

! !

2: /4 ! !

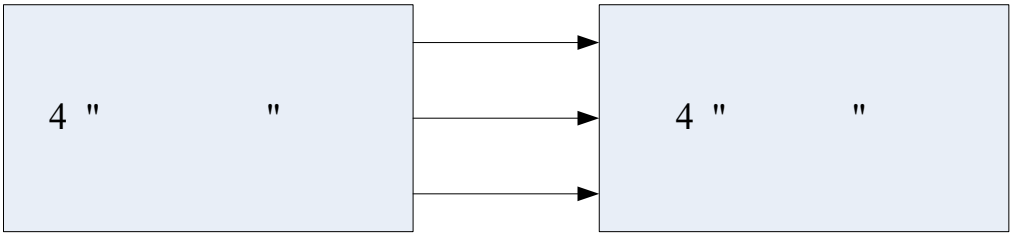

Fig. 19-2 I2S transmitter-master & receiver-slave condition

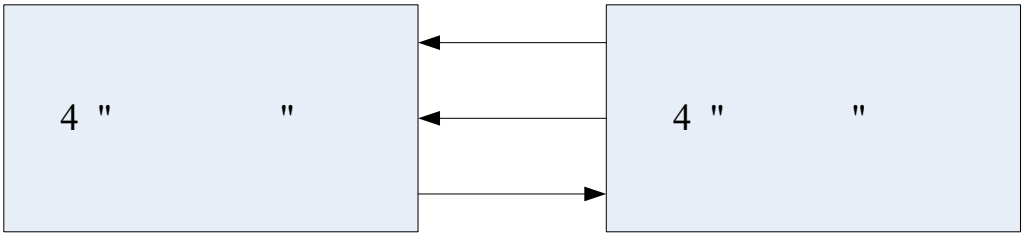

Fig. 19-3 I2S transmitter-slave& receiver-master condition

2: /4/2 3 ! ! !

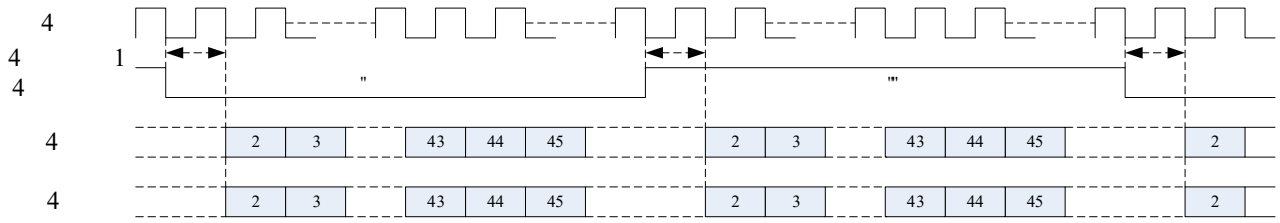

Fig. 19-4 I2S normal mode timing format

2: /4/3 3 ! ! ! !

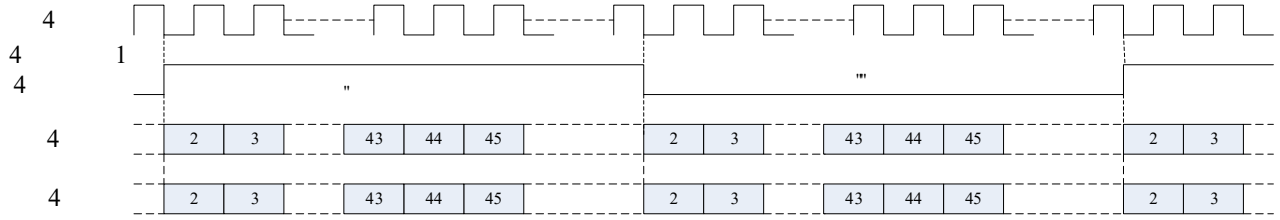

Fig. 19-5 I2S left justified mode timing format

2: /4/4 3 ! ! ! !

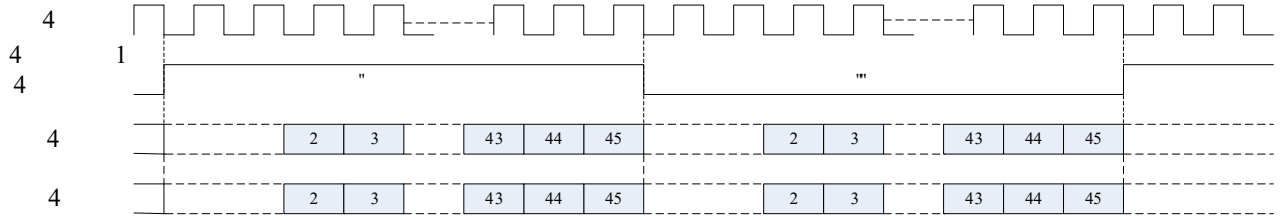

Fig. 19-6 I2S right justified mode timing format

2: /4/5 ! ! !

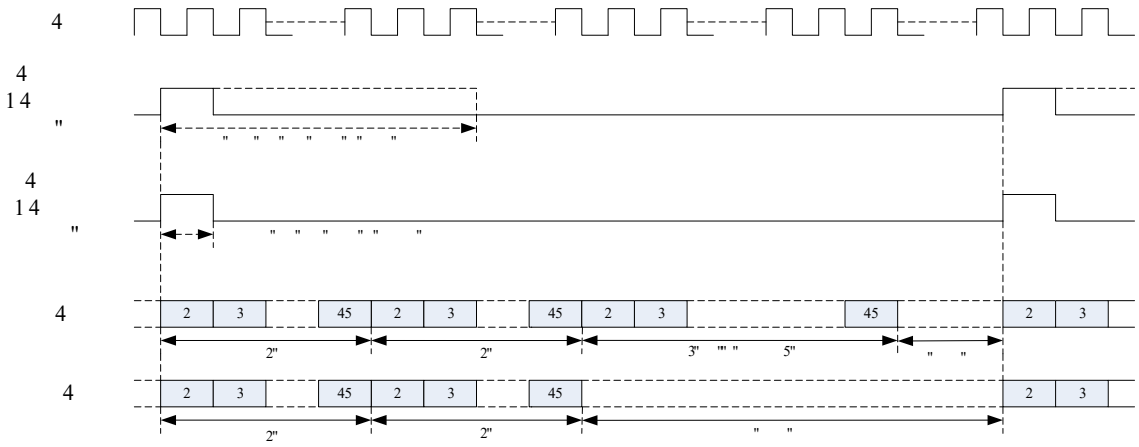

Fig. 19-7 PCM early mode timing format

2: /4/6 ! 2! !

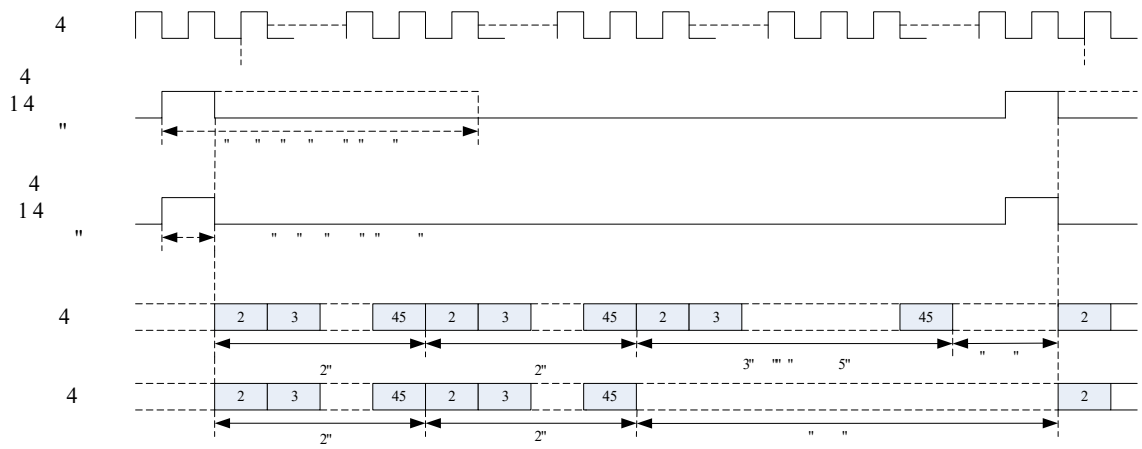

Fig. 19-8 PCM late1 mode timing format

2: /4/7 ! 3! !

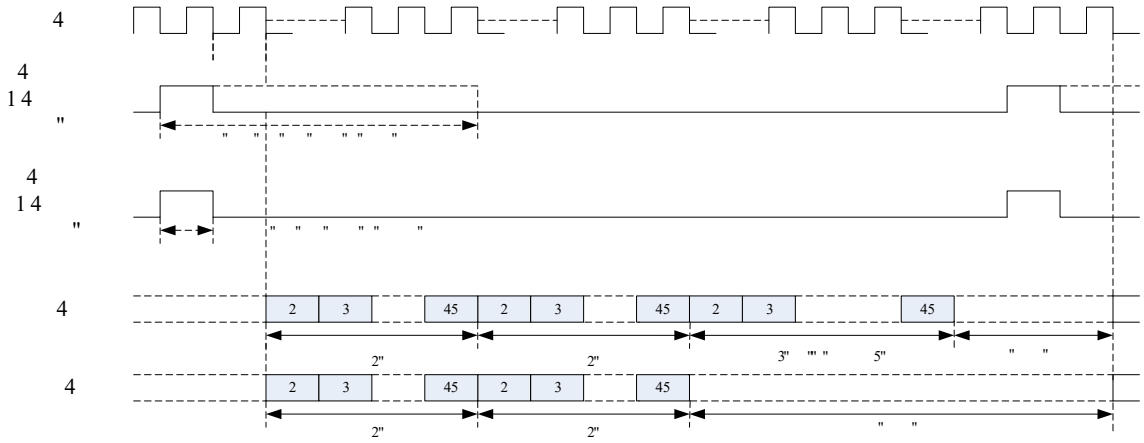

Fig. 19-9 PCM late2 mode timing format

2: /4/8 ! 4! !

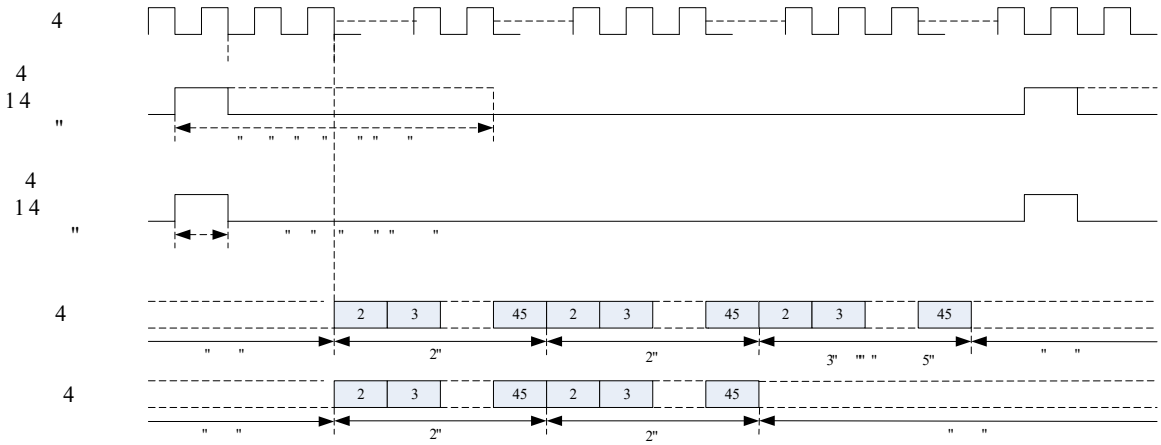

Fig. 19-10 PCM late3 mode timing format

2: /5 ! !

2: /5/2 ! !

!	!	!	! !	!
_____				
_____				
_____				
_____				
_____				
_____				
_____				
_____				
_____				
_____				
_____				

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

2: /5/3 ! ! !

3 !

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

3 !

!	B !	! !	!

!	B !	! !	!

3 !

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

3 !

!	B !	! !	!

3 B !

!	B !	! !	!

!	B !	! !	!

3 !

!	B !	! !	!

3 !

!	B !	! !	!

!	B !	! !	!

3 !

!	B !	! !	!

3 !

!	B !	! !	!

3 !

!	B !	! !	!

3 !

!	B !	! !	!

2: /6 ! !

Table 19-1 I2S_2CH Interface Description

! !	!	! !	! !

Notes: I=input, O=output, I/O=input/output, bidirectional

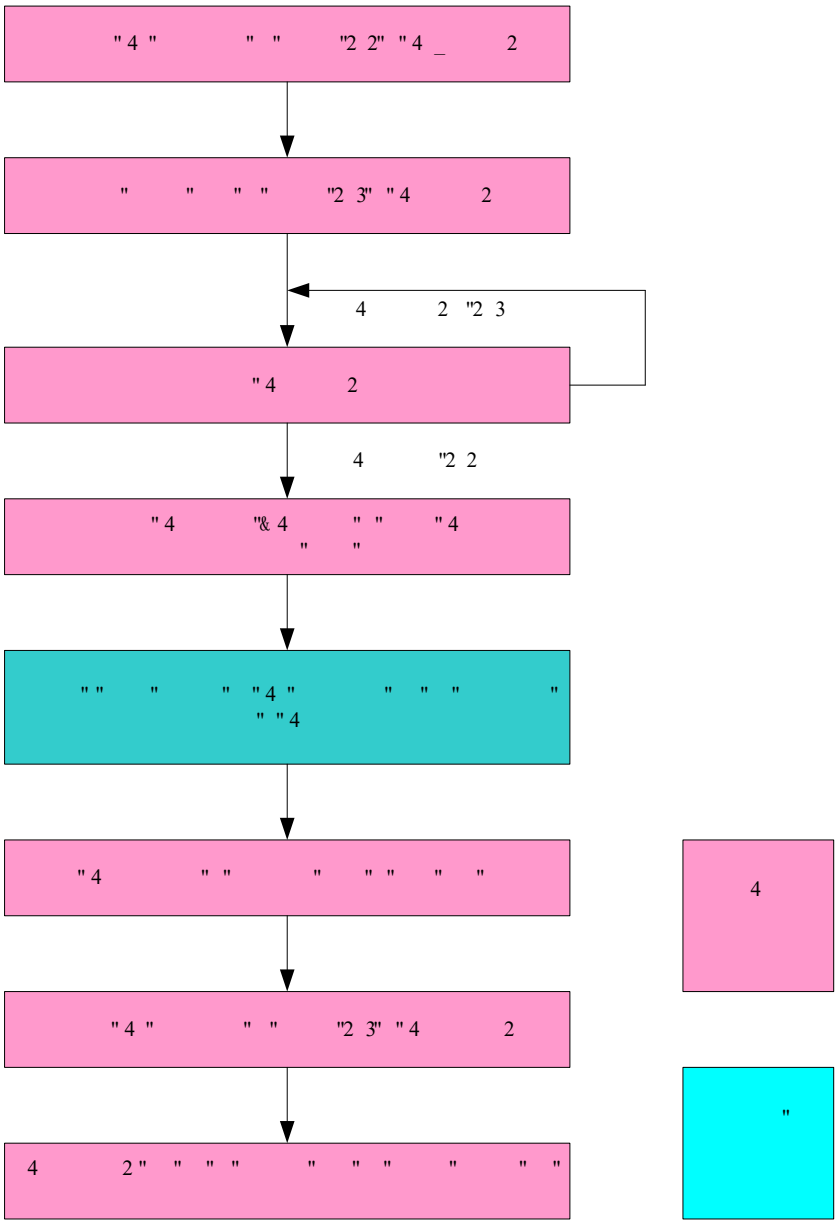

Fig. 19-11 I2S/PCM controller transmit operation flow chart

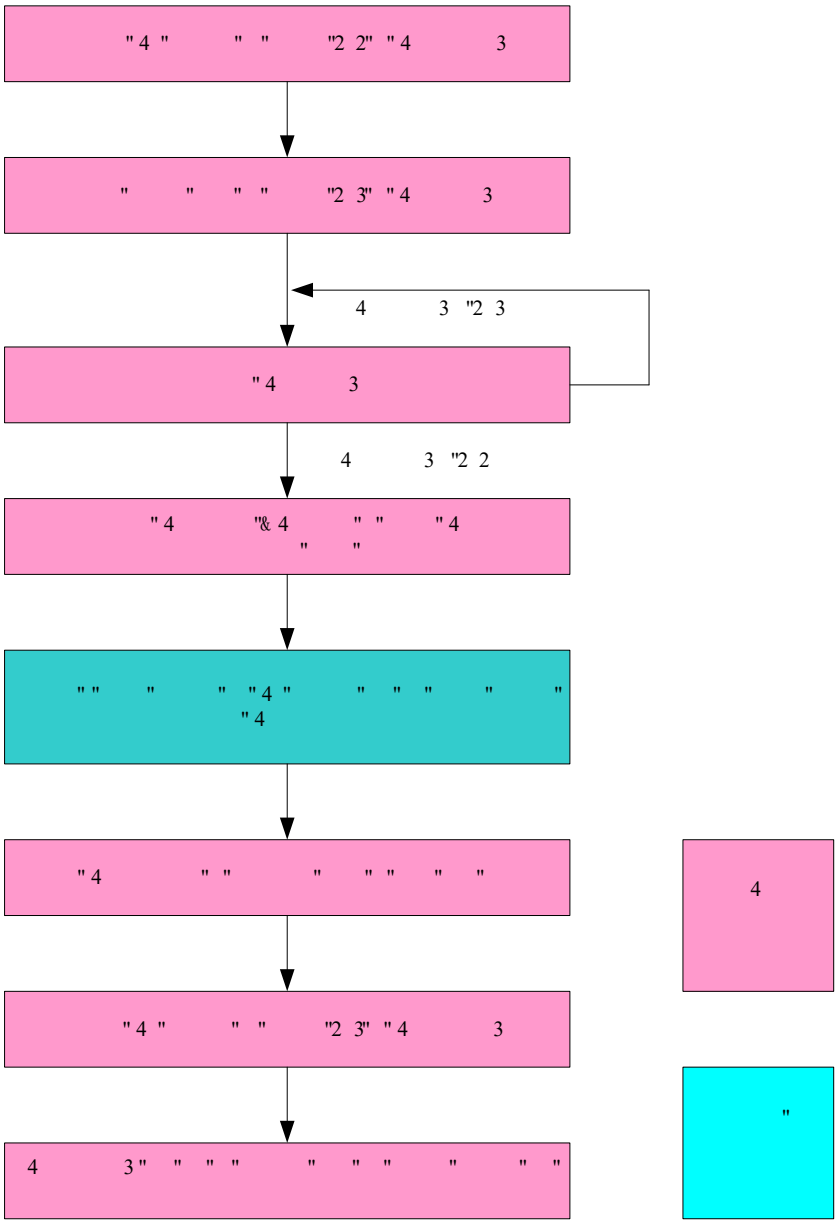

Fig. 19-12 I2S/PCM controller receive operation flow chart

!31 3 !9. !

31/2 !

31/2/2 !

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-
-

31.3 ! !

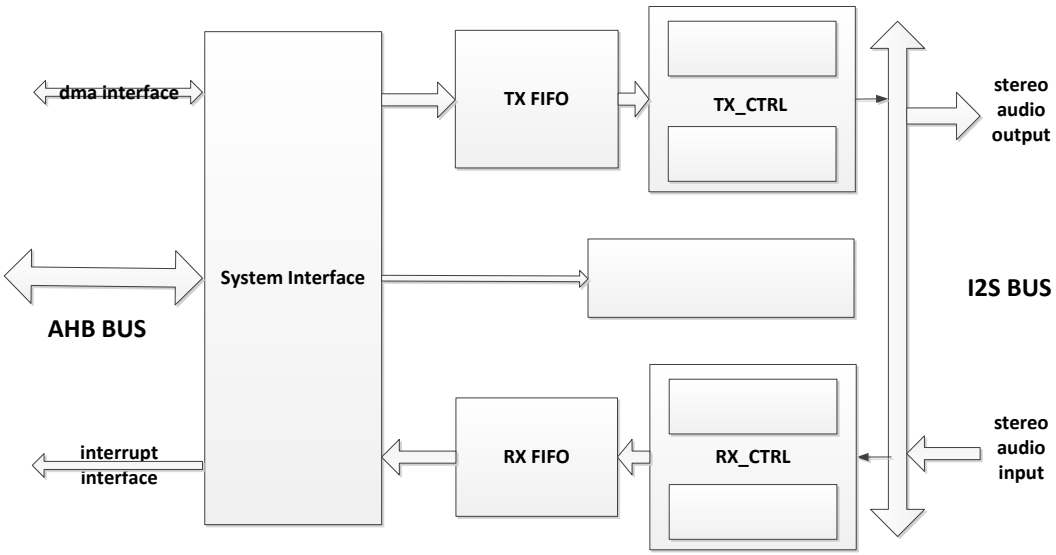


Fig. 20-1 I2S/PCM/TDM controller (8 channel) Block Diagram

! !

! !!

!

!!

! !

! !

31.4 ! !

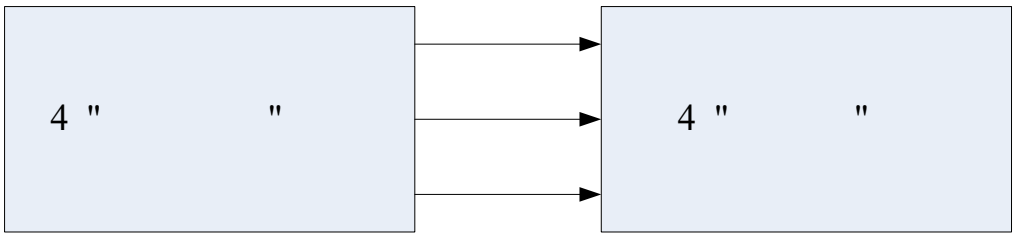


Fig. 20-2 I2S transmitter-master & receiver-slave condition

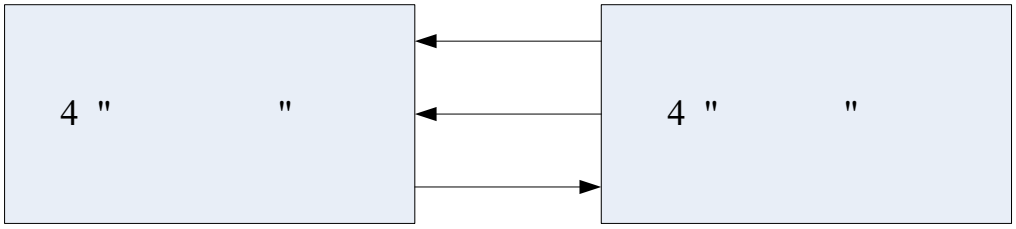


Fig. 20-3 I2S transmitter-slave & receiver-master condition

31.4.2 3 ! ! !

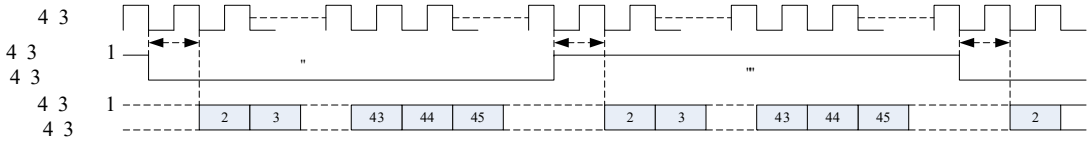


Fig. 20-4 I2S normal mode timing format

31.4.3 3 ! ! ! !

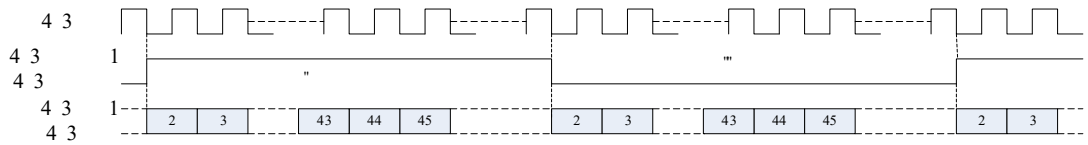


Fig. 20-5 I2S left justified mode timing format

31.4.4 3 ! ! ! !

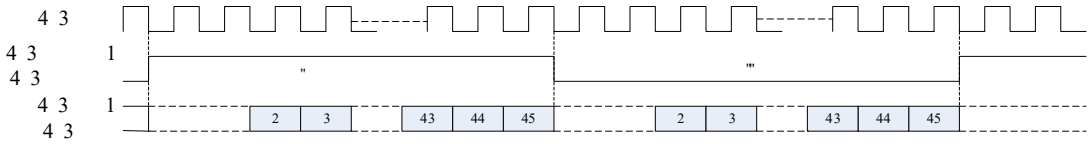


Fig. 20-6 I2S right justified mode timing format

31 /4 /5 ! ! !

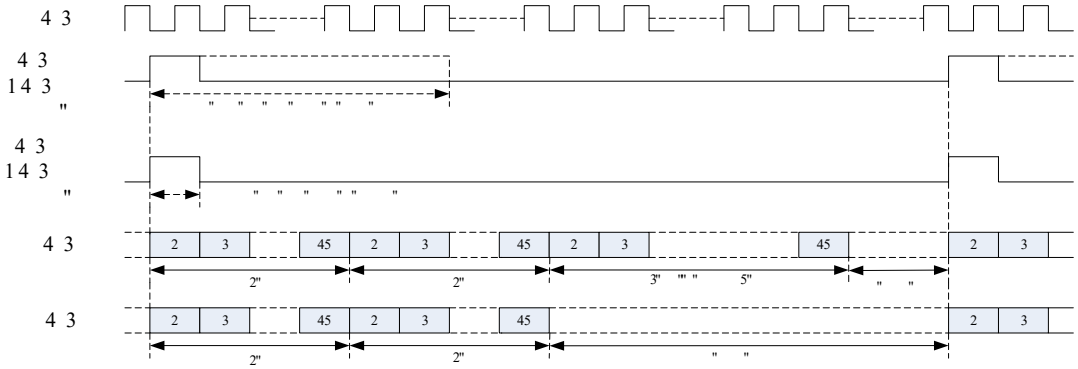


Fig. 20-7 PCM early mode timing format

31 /4 /6 ! 2! !

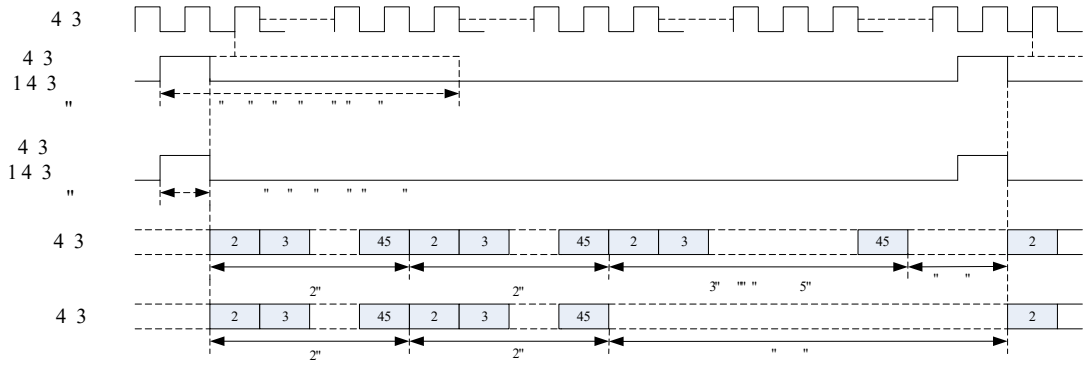


Fig. 20-8 PCM late1 mode timing format

31 /4 /7 ! 3! !

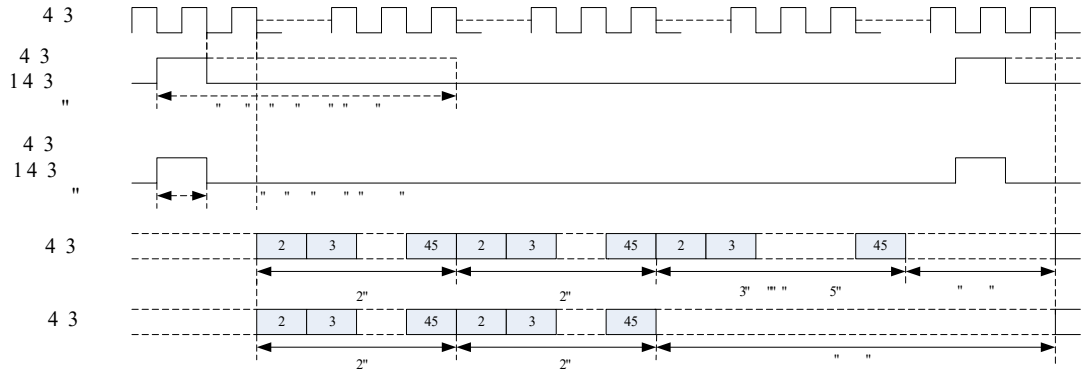


Fig. 20-9 PCM late2 mode timing format

31/4/8 ! 4! !

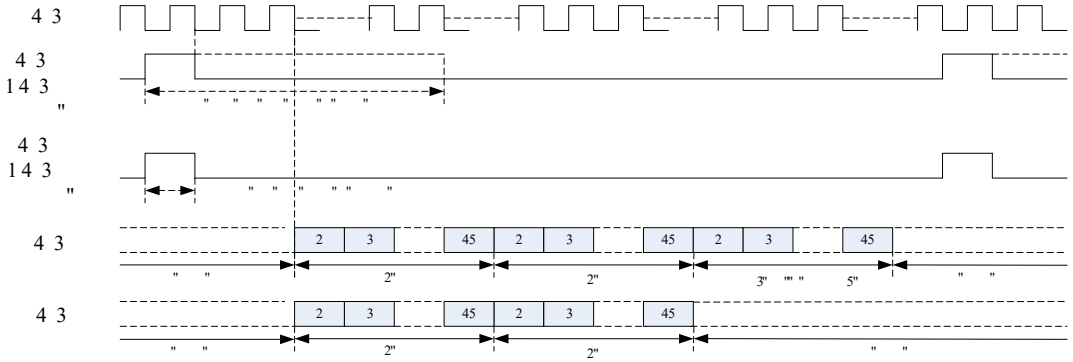
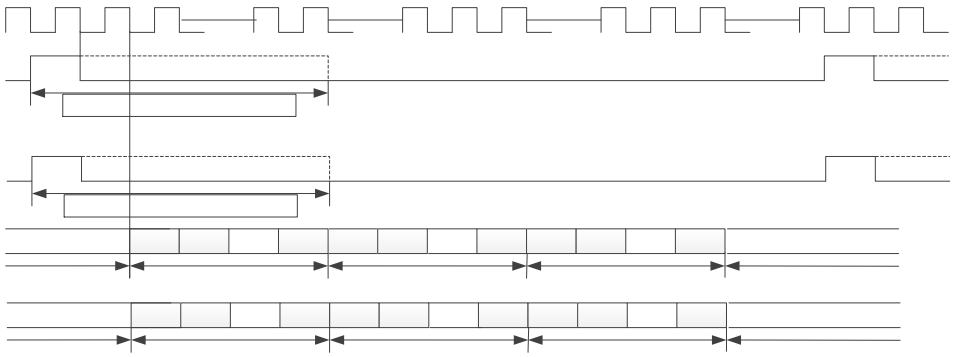
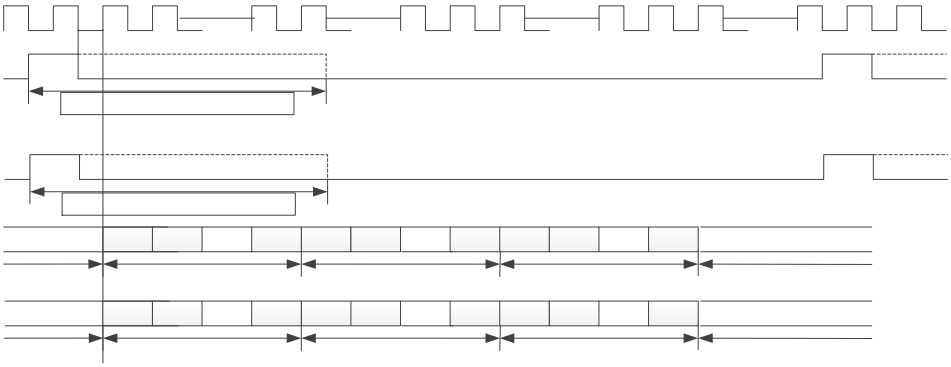


Fig. 20-10 PCM late3 mode timing format

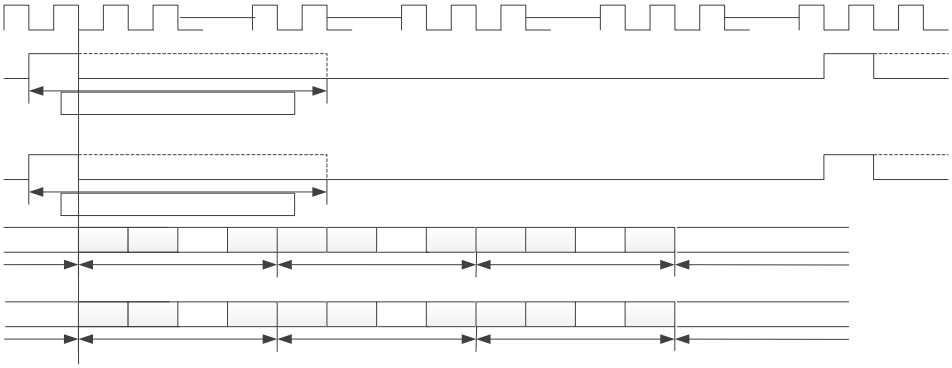
31/4/9 ! ! !) ! !



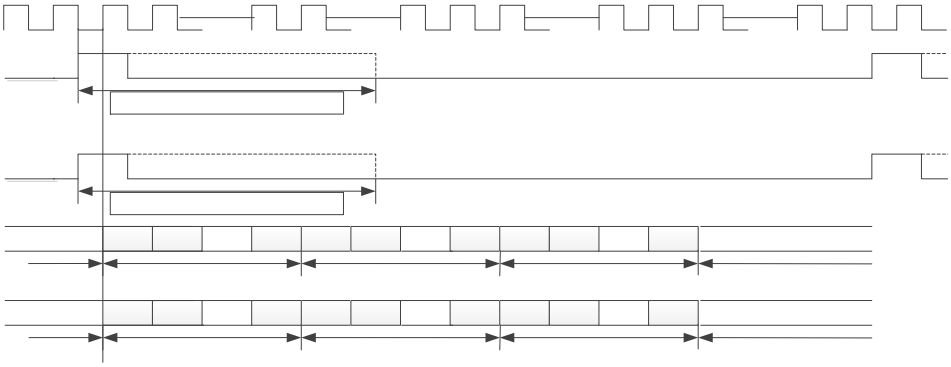
31/4/: ! ! ! 1!) ! !



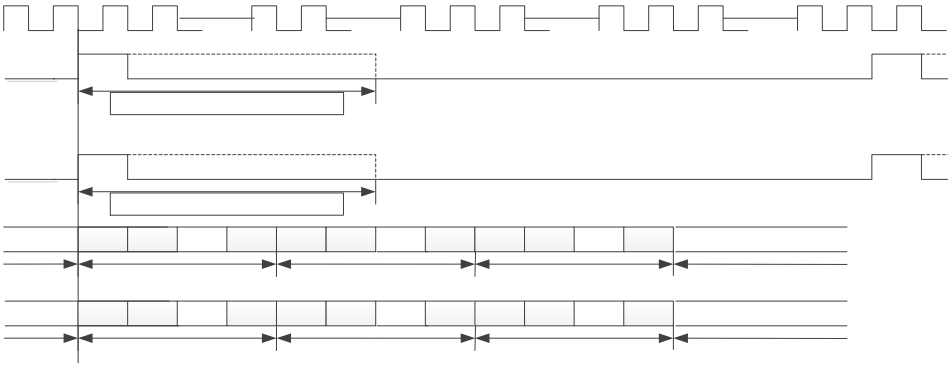
31/4/21 ! ! ! 2!) ! !



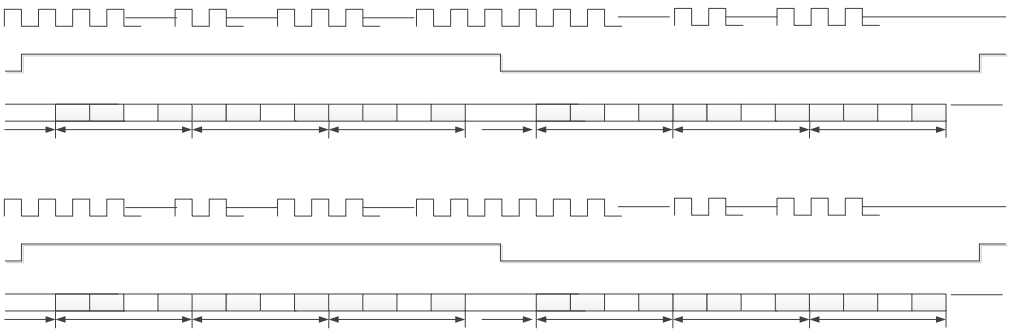
31/4/22 ! ! ! 3!) ! !



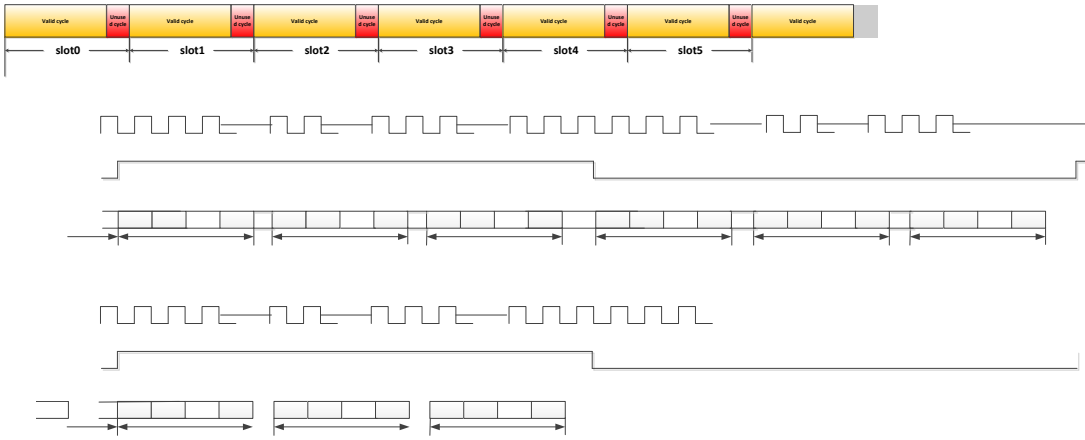
31/4/23 ! ! ! 4!) ! !



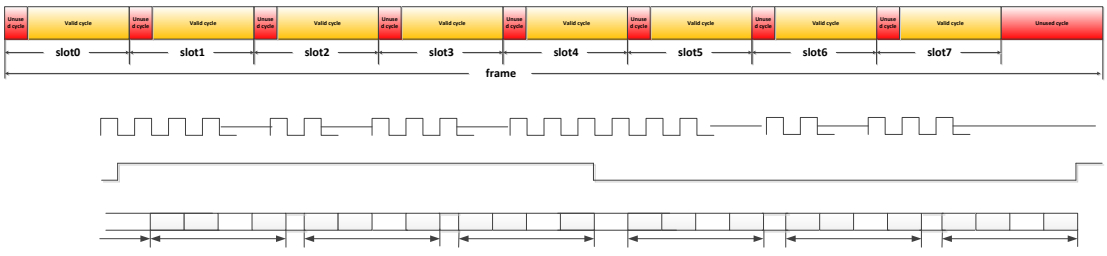
31/4/24 ! ! !) 3 ! !

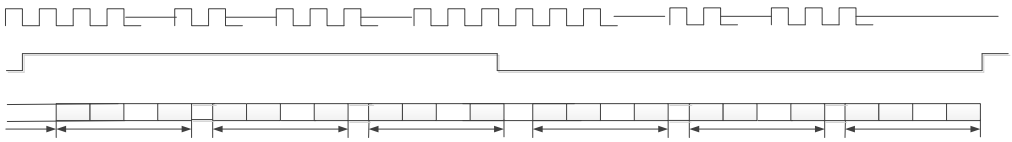


31/4/25 ! ! ! !) 3 ! !



31/4/26 ! ! ! !) 3 ! !





31.5 ! !

31.5.2 ! !

!	!	!	! !	!

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

31.5.3 ! ! !

3 9 !

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

3 9 !

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

3 9 !

!	B !	! !	!

!	B !	! !	!

3 9 B !

!	B !	! !	!

3 9 !

!	B !	! !	!

!	B !	! !	!

3 9 !

!	B !	! !	!

!	B !	! !	!

3 9 !

!	B !	! !	!

3 9 !

!	B !	! !	!

3 9 !

!	B !	! !	!

3 9 !

!	B !	! !	!

3 9 !

!	B !	! !	!

3 9 !

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

3 9 !

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

3 9 !

!	B !	! !	!

3 9 !

!	B !	! !	!

31.6 ! !

Table 20-1 I2S_8CH_TDM Interface Description

! !	!	! !	! !

! !	!	! !	! !

31 /7 B ! !

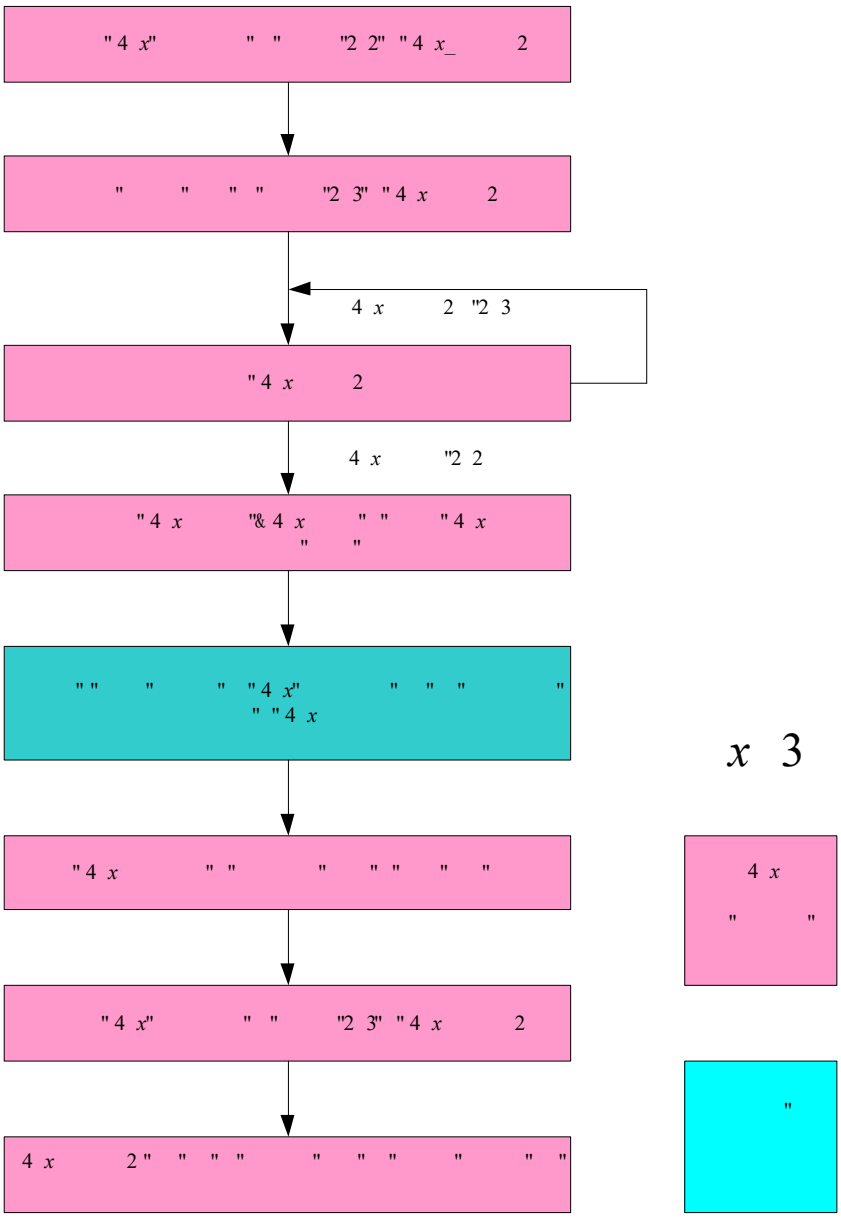


Fig. 20-11 I2S/PCM/TDM controller transmit operation flow chart

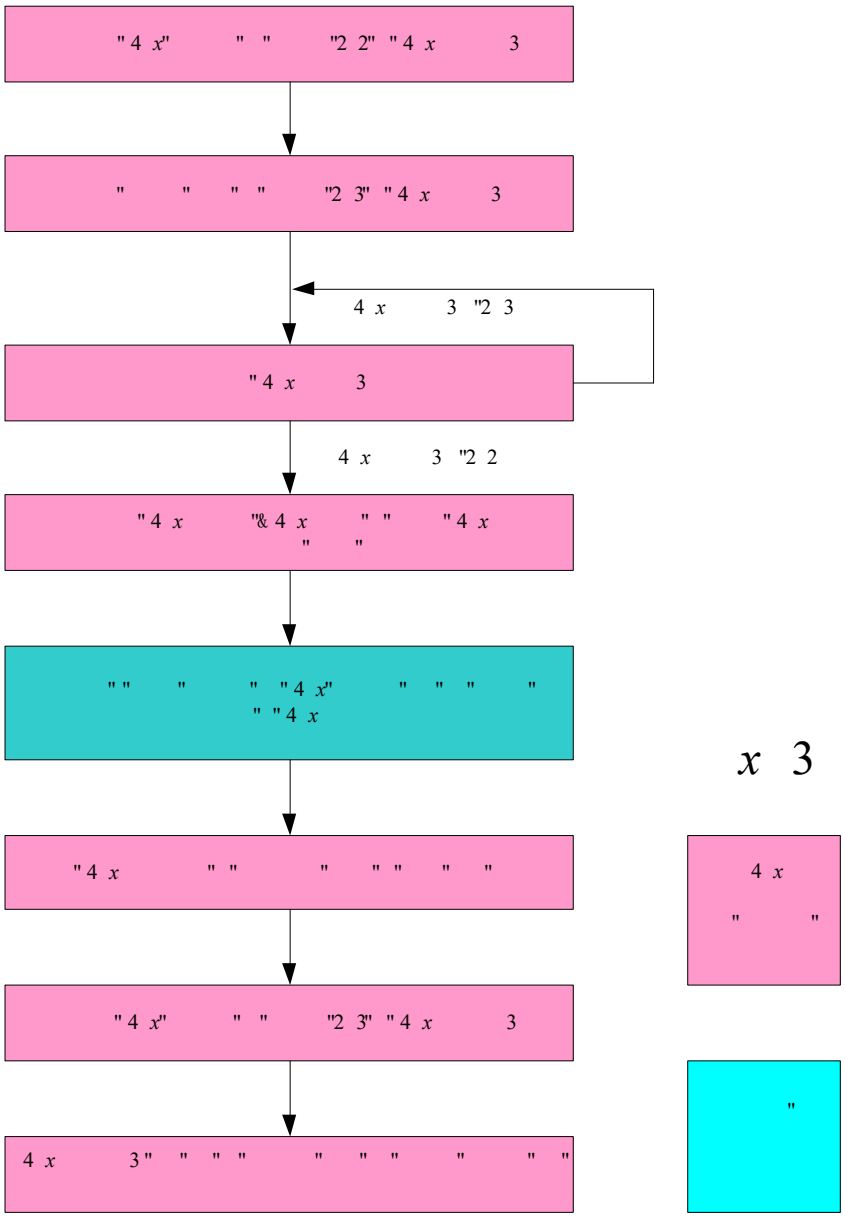


Fig. 20-12 I2S/PCM/TDM controller receive operation flow chart

Note: User should clear TX/RX logical by CLR[0]/CLR[1] and wait clear operation done before configure the other registers.

!32 3B !

32/2 !

-
-
-

32/3 ! !

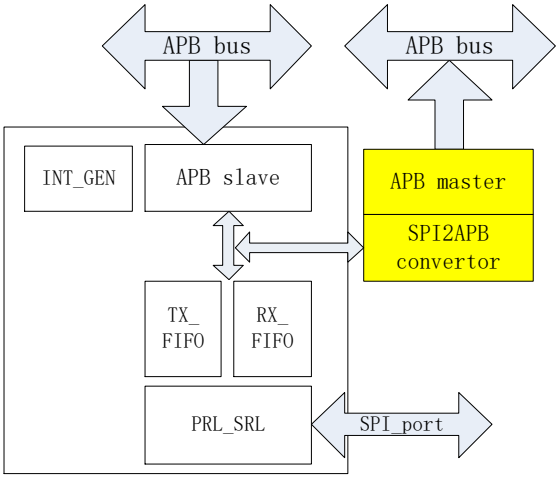


Fig. 21-1 SPI2APBBlock Diagram

32/4 ! !

32/4/2 !

32/4/3 ! !

!

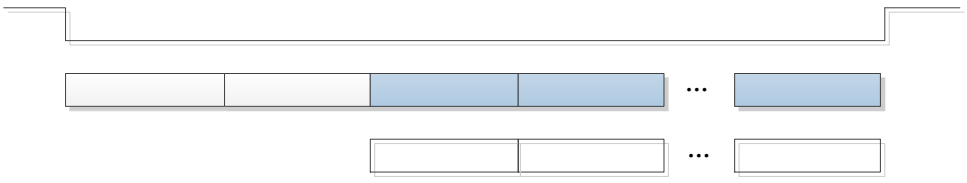


Fig. 21-2 Write operation

!

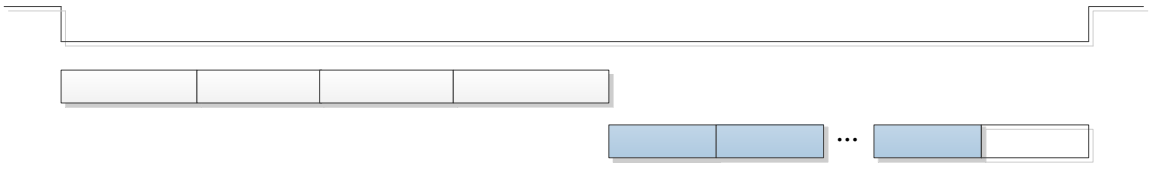


Fig. 21-3 Read operation

!

Fig. 21-4 Query operation

!!	B !	! !	!!

!

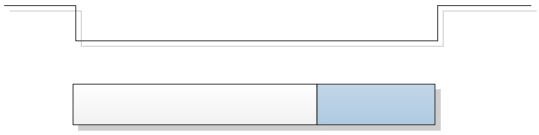


Fig. 21-5 Write message operation

! !

!	!	!

!

32/5 ! !

32/5/2 ! !

!	!	!	! !	!
_____				
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_____				
_____				
_____				

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

32/5/3 ! ! !

3B !

!	B !	! !	!

3B !

!	B !	! !	!

!	B !	! !	!

3B !

!	B !	! !	!

3B !

!	B !	! !	!

3B !

!	B !	! !	!

3B B 1!

!	B !	! !	!

3B B 2!

!	B !	! !	!

3B B 3!

!	B !	! !	!

32/6 ! !

Table 21-1 SPI2APB interface description

! !	!	! !	! !

32/7 B ! !

!33 ! ! !) !

33/2 !

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-
-

33/3 ! !

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-
-
-

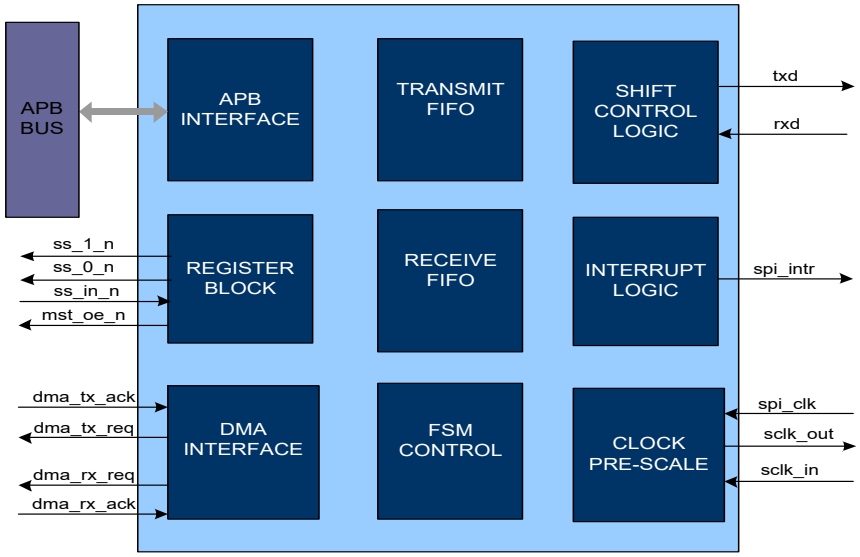

Fig. 22-1 SPI Controller Block diagram

B ! B !

B! B !

! !

! !

! !

! !

33/4 ! !

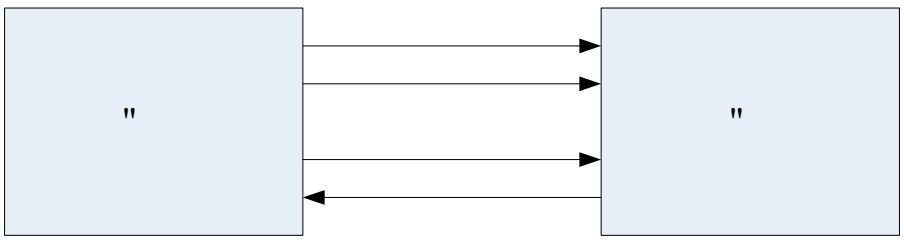

Fig. 22-2 SPI Master and Slave Interconnection

! !

! !

! !

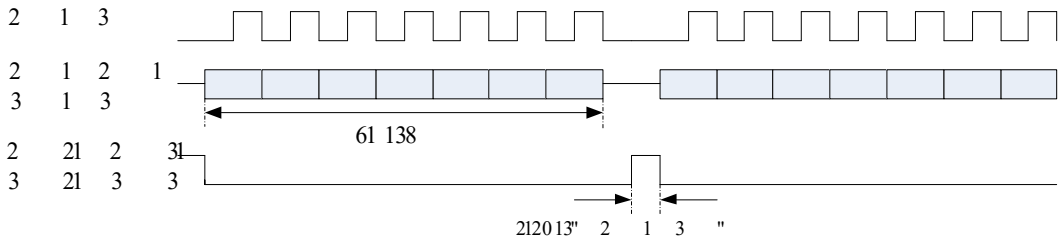

Fig. 22-3 SPI Format (SCPH=0 SCPOL=0)

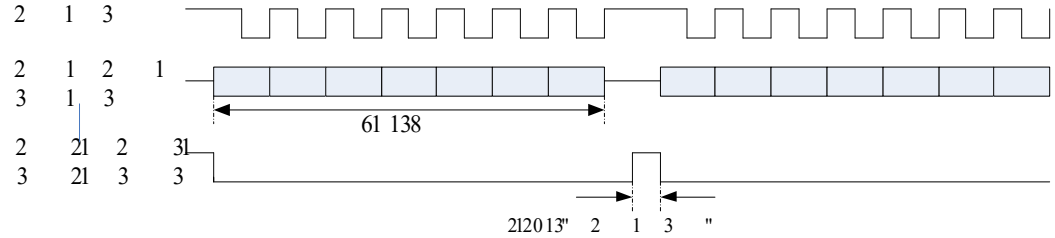

Fig. 22-4 SPI Format (SCPH=0 SCPOL=1)

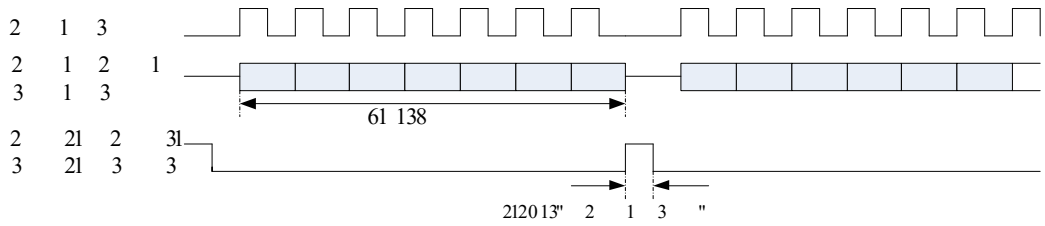

Fig. 22-5 SPI Format (SCPH=1 SCPOL=0)

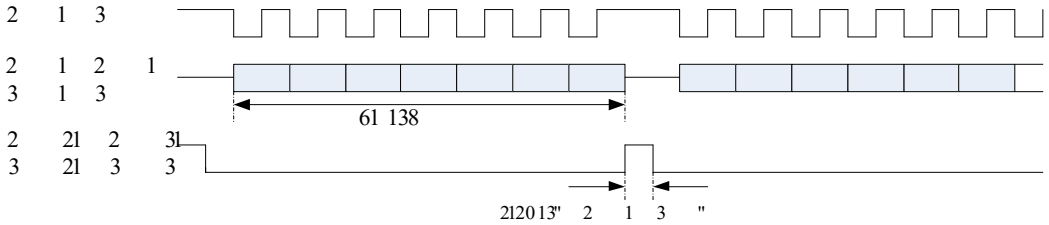

Fig. 22-6 SPI Format (SCPH=1 SCPOL=1)

33.5 ! !

33.5.2 ! !

!	!	!	! !	!
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_____				
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_____				
_____				

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

33/5/3 ! ! !

1!

!	B !	! !	!

!	B !	! !	!

!	!	!

2!

!	!	!

!	B !	! !	!

_____!

!	B !	! !	!

_____B____!

!	B !	! !	!

_____!

!	B !	! !	!

_____!

!	B !	! !	!

_____!

!	B !	! !	!

_____!

!	B !	! !	!

_____!

!	B !	! !	!

_____!

!	B !	! !	!

_____!

!	B !	! !	!

_____!

!	B !	! !	!

!	B !	! !	!

_____!

!	B !	! !	!

!	B !	! !	!

!

!	B !	! !	!

B !

!	B !	! !	!

B !

!	B !	! !	!

B !

!	B !	! !	!

3B !

!	B !	! !	!

1!

!	B !	! !	!

2!

!	B !	! !	!

3!

!	B !	! !	!

!

!	B !	! !	!

!

!	B !	! !	!

33/6 ! !

Table 22-1 SPI1/SPI2 interface description

! !	!	! !	! !

! !	!	! !	! !

Notes: I=input, O=output, I/O=input/output, bidirectional. spi_csn1 can only be used in master mode

33/7 B ! !

! !

! ! !

! ! !

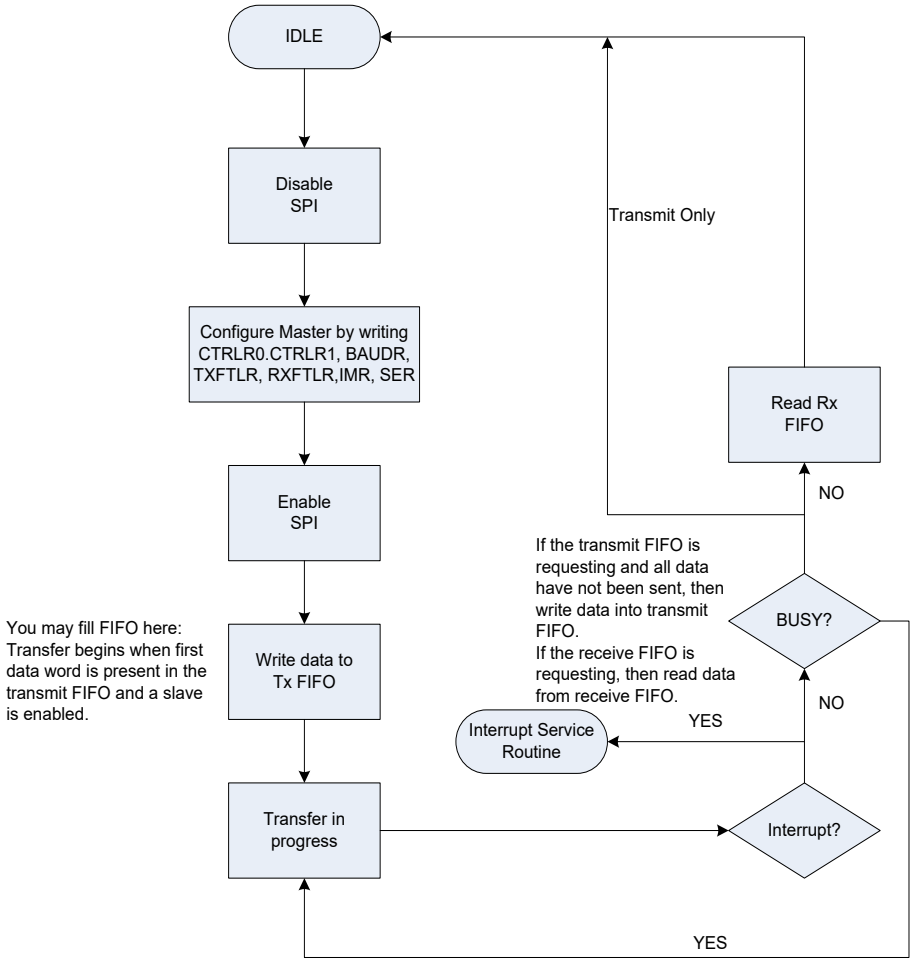

Fig. 22-7 SPI Master transfer flow diagram

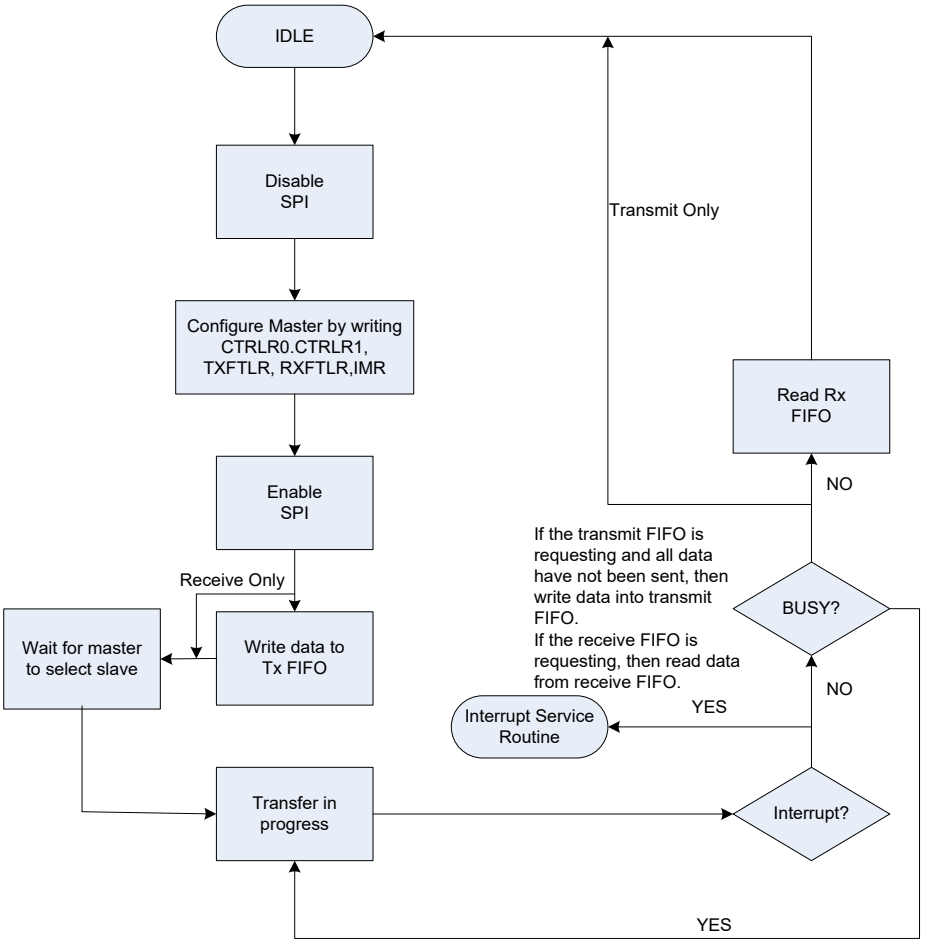

Fig. 22-8 SPI Slave transfer flow diagram

!34 !B ! 0 !
) B !

34/2 !

-
-
-
-
-
-
-

34/3 ! !

-
-
-
-
-

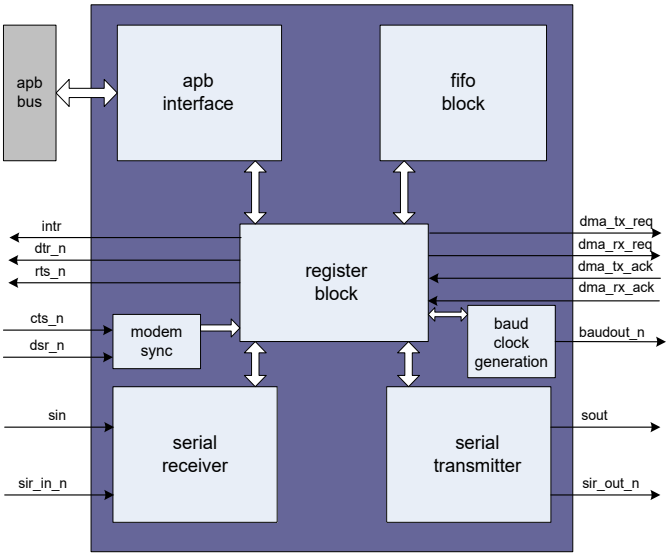

Fig. 23-1 UART Architecture

B ! B !

UART

UART

! !

! ! !

! !!

! ! !!

! !

! !

34/4 ! !

B !) 343 ! ! !

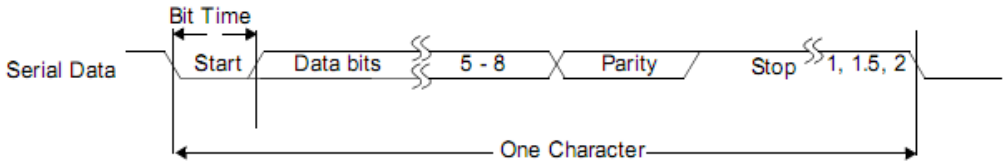

Fig. 23-2 UART Serial protocol

B!2/1! ! !

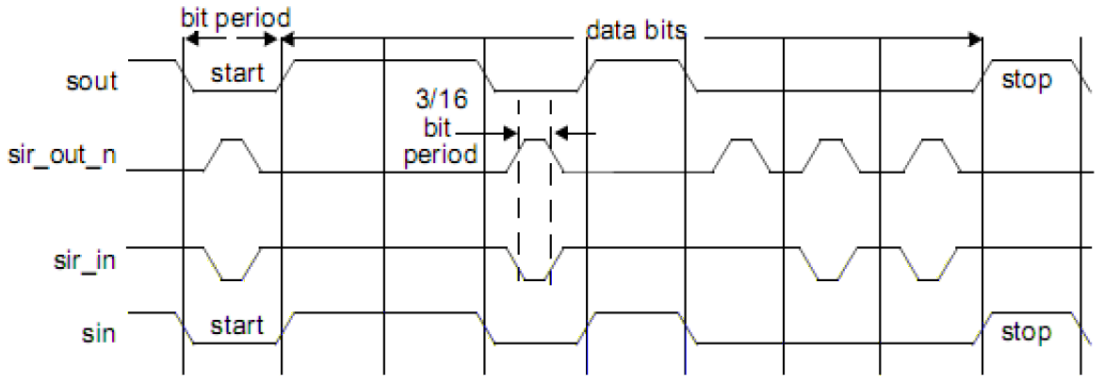

Fig. 23-3 IrDA 1.0

! !

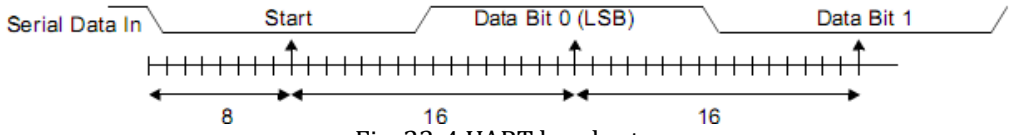

Fig. 23-4 UART baud rate

!

! !

2/ ! ! !

3/ ! !

UART1/UART2/UART3/UART4/UART5/UART6/UART7

!

-
-
-
-

-

B! !

-
-

-

-

-

B ! ! !

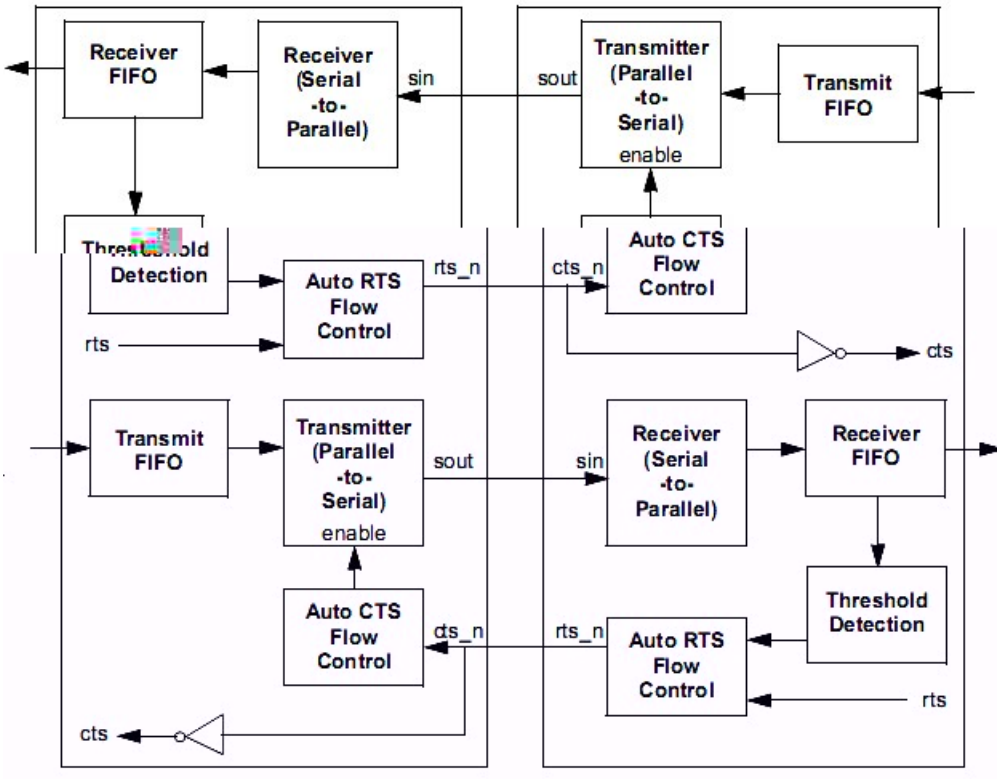

Fig. 23-5 UART Auto flow control block diagram

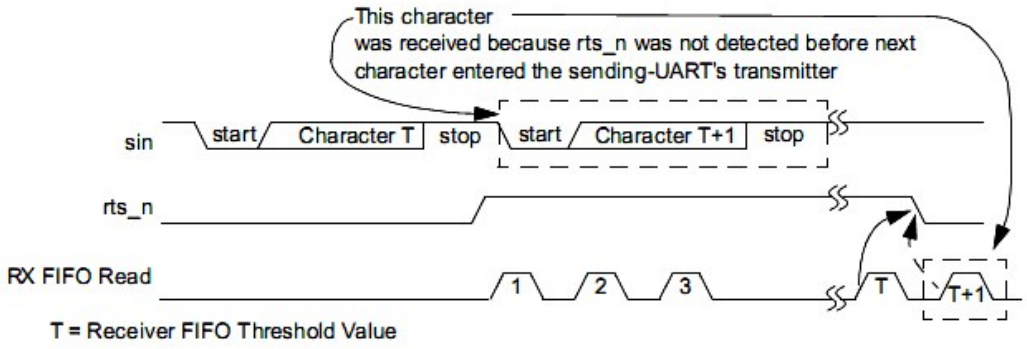

Fig. 23-6 UART AUTO RTS TIMING

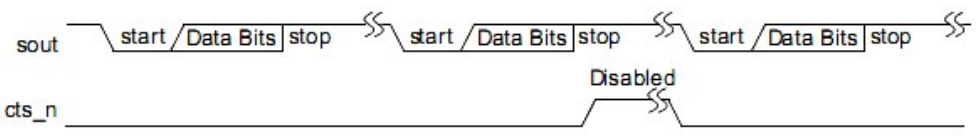

Fig. 23-7 UART AUTO CTS TIMING

34/5 ! !

34/5/2 !B ! !

34/5/3 ! !

!	!	!	! !	!

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

34/5/4 ! ! !

B !

!	B !	! !	!

B !

!	B !	! !	!

B !

!	B !	! !	!

B !

!	B !	! !	!

B !

!	B !	! !	!

B !

!	B !	! !	!

!	B !	! !	!

B !

!	B !	! !	!

!	B !	! !	!

B !

!	B !	! !	!

!	B !	! !	!

!	B !	! !	!

B !

!	B !	! !	!

!	B !	! !	!

B !

!	B !	! !	!

!	B !	! !	!

B !

!	B !	! !	!

!	B !	! !	!

B !

!	B !	! !	!

B !

!	B !	! !	!

B !

!	B !	! !	!

B B !

!	B !	! !	!

B !

!	B !	! !	!

B !

!	B !	! !	!

B !

!	B !	! !	!

B !

!	B !	! !	!

B !

!	B !	! !	!

!	B !	! !	!

B !

!	B !	! !	!

B !

!	B !	! !	!

B !

!	B !	! !	!

B B !

!	B !	! !	!

!	B !	! !	!

B !

!	B !	! !	!

B !

!	B !	! !	!

B !

!	B !	! !	!

B !

!	B !	! !	!

B B B!

!	B !	! !	!

!	B !	! !	!

B !

!	B !	! !	!

!	B !	! !	!

B !

!	B !	! !	!

B !

!	B !	! !	!

34/6 ! !

!

!	!	! !	!
B 1!			
B 2 1!			
B 2 2!			

!	!	! !	!
B 3 1!			
B 3 2!			
B 3 3!			
B 4 1!			
B 5!			
B 6!			
B 7!			
B 8!			

34/7 B ! !

34/7/2 ! ! ! ! !

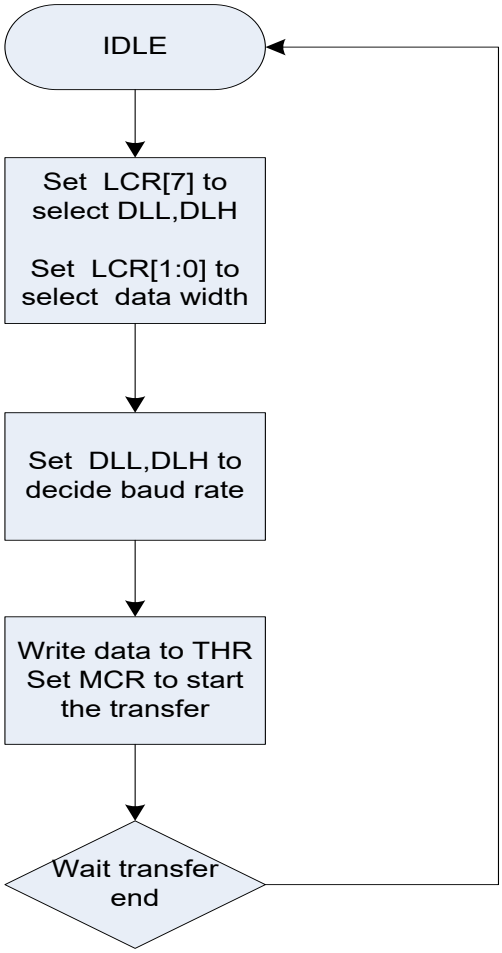

Fig. 23-8 UART none fifo mode

34/7/3 ! ! ! !

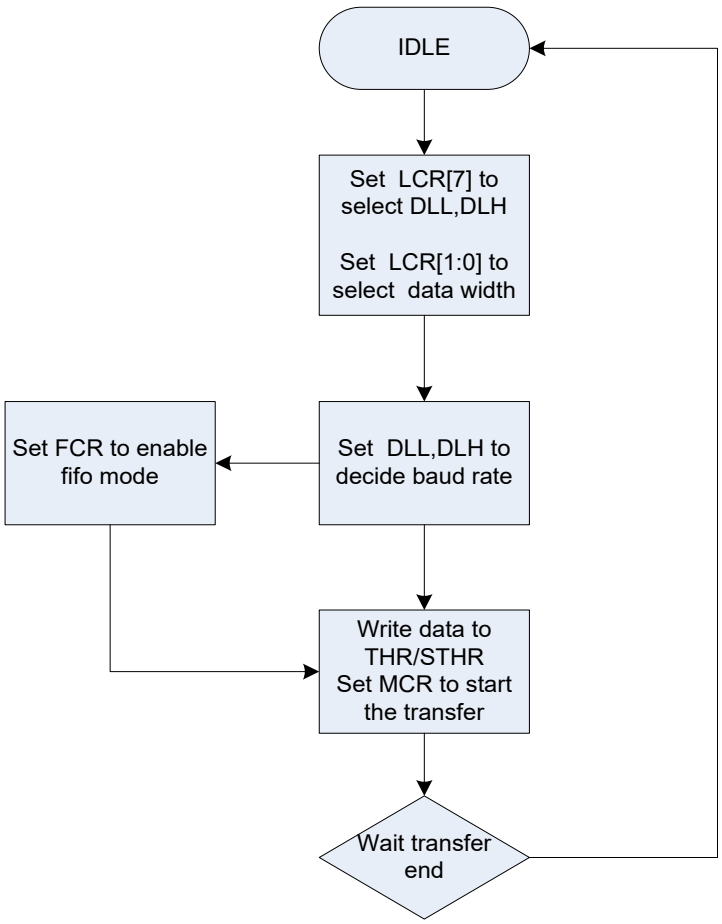

Fig. 23-9 UART fifo mode

34/7/4 ! ! !

B ! ! !

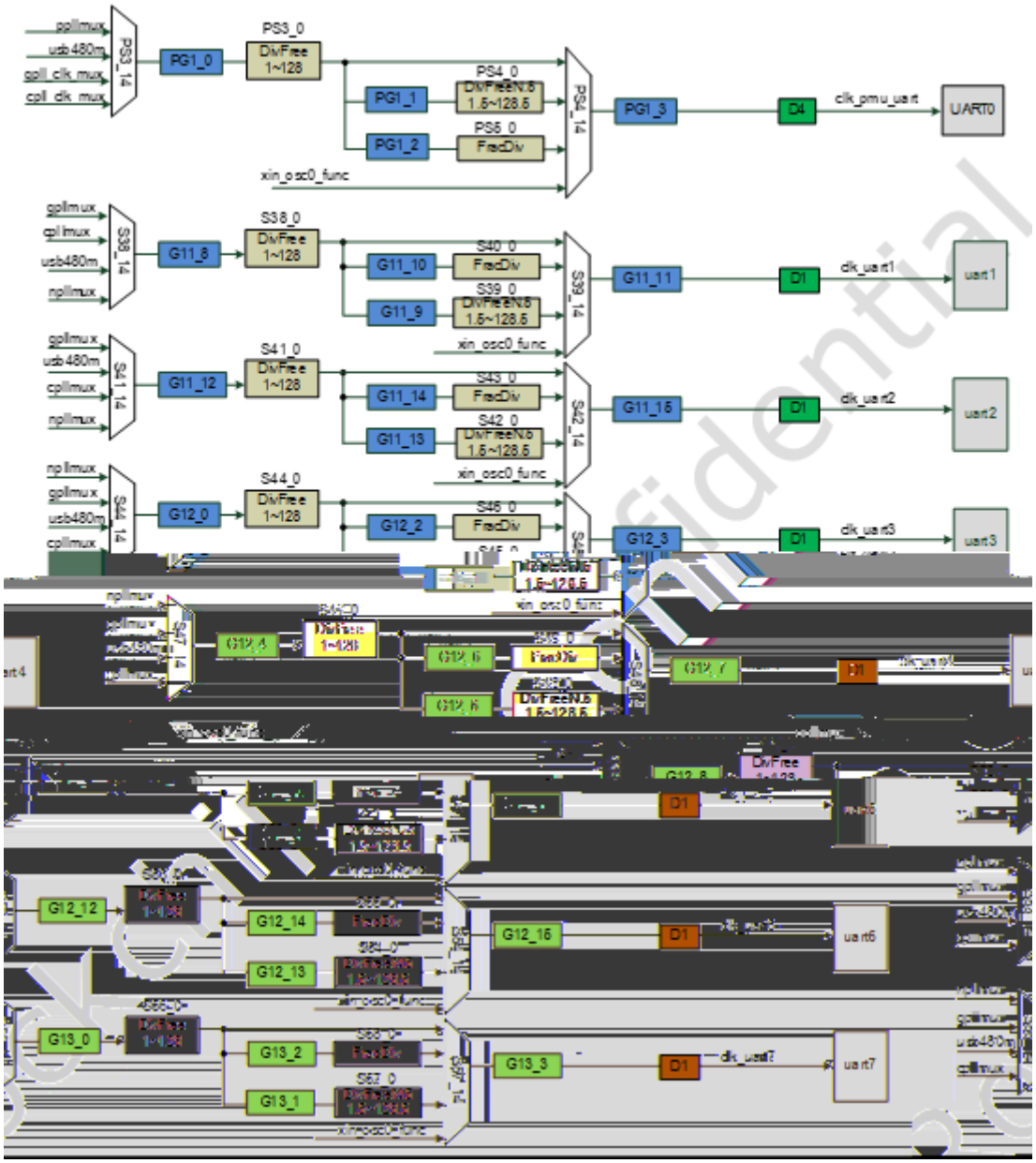

Fig. 23-10 UART clock generation

B ! ! ! !

Table 23-2 UART baud rate configuration

! !	! !

! !	! !

34/7/5 ! ! ! ! !

-
-

Table 23-3 UART cts_n and rts_n polarity configuration

B !	B !	B !

!35 3 ! !

35/2 !

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-
-
-
-
-
-
-

35/3 ! !

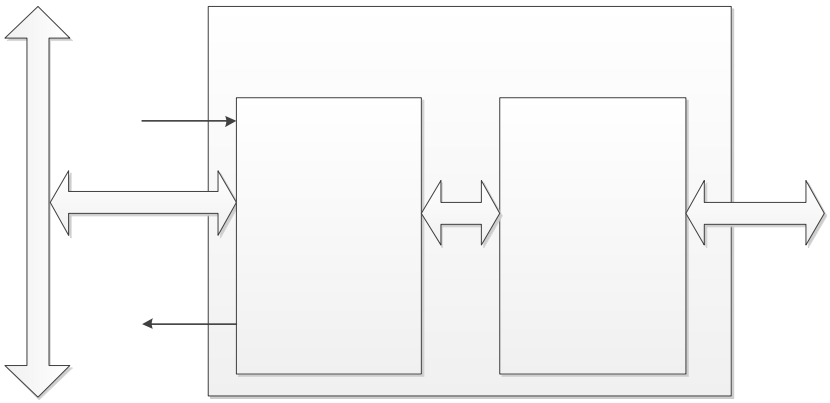

Fig. 24-1 I2C architecture

35/3/2 3 !

35/3/3 3 !

35/3/4 3 !

35/4 ! !

35.4.2 !

-
-

35.4.3 ! ! !

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  -
  -
-
  -
  -

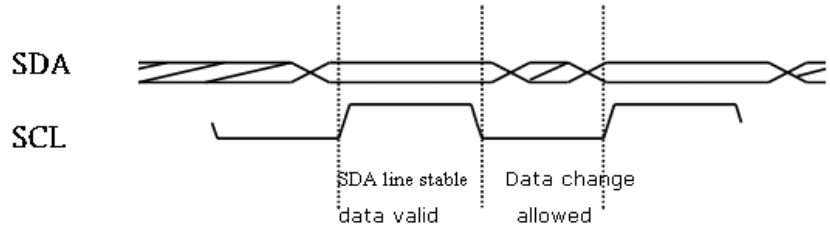


Fig. 24-2 I2C DATA Validity

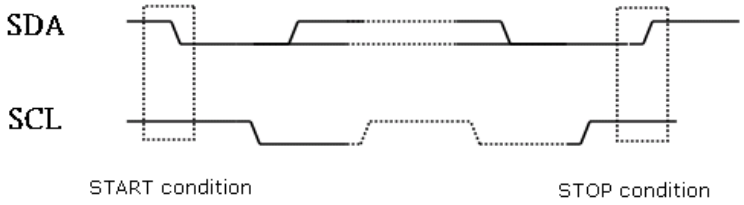


Fig. 24-3 I2C Start and stop conditions

◆

➢

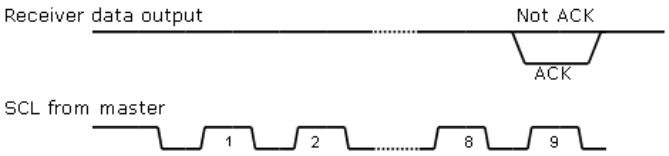


Fig. 24-4 I2C Acknowledge

➢

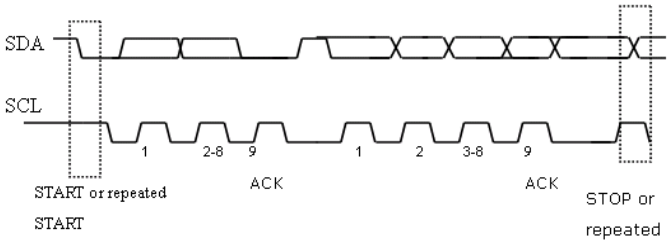


Fig. 24-5 I2C byte transfer

35.5 ! !

35.5.2 ! !

!	!	!	! !	!
_____				
_____				,
_____				
_____				
_____				
_____				
_____				
_____				

!	!	!	! !	!
_____				
_____				
_____				
_____				
_____				
_____				
_____				
_____				
_____				
_____				
_____				
_____				
_____				
_____				
_____				
_____				
_____				
_____				
_____				
_____				

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

35/5/3 ! ! !
3 !

!	B !	! !	!

!	B !	! !	!

3 !

!	B !	! !	!

3 B !

!	B !	! !	!

3 B !

!	B !	! !	!

3 !

!	B !	! !	!

3 !

!	B !	! !	!

3 !

!	B !	! !	!

3 !

!	B !	! !	!

!	B !	! !	!

3 !

!	B !	! !	!

3 !

!	B !	! !	!

!	B !	! !	!

3 B B1!

!	B !	! !	!

3 B B2!

!	B !	! !	!

3 B B3!

!	B !	! !	!

3 B B4!

!	B !	! !	!

3 B B5!

!	B !	! !	!

3 B B6!

!	B !	! !	!

3 B B7!

!	B !	! !	!

3 B B8!

!	B !	! !	!

3 B B1!

!	B !	! !	!

3 B B2!

!	B !	! !	!

3 B B3!

!	B !	! !	!

3 B B4!

!	B !	! !	!

3 B B5!

!	B !	! !	!

3 B B6!

!	B !	! !	!

3 B B7!

!	B !	! !	!

3 B B8!

!	B !	! !	!

3 !

!	B !	! !	!

3 !

!	B !	! !	!

!	B !	! !	!

35/6 ! !

Table 24-1 I2C Interface Description

! !	!	! !	!
3 1! !			
3 2! !			
3 3! !			
3 4! 1! !			
3 4! 2! !			

35/7 B ! !

-

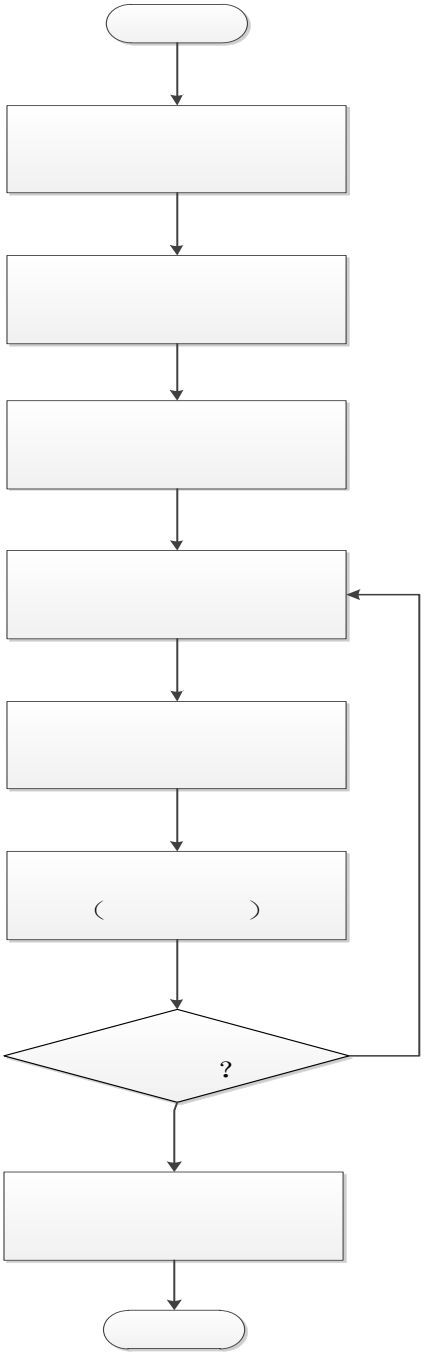


Fig. 24-6 I2C Flow chat for transmit only mode

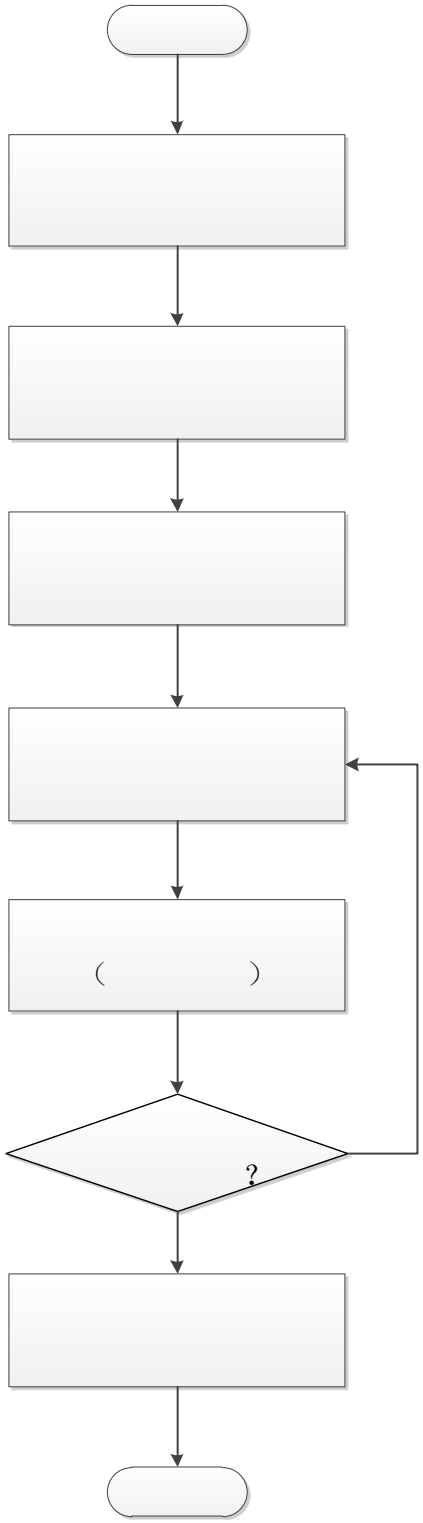


Fig. 24-7 I2C Flow chat for receive only mode

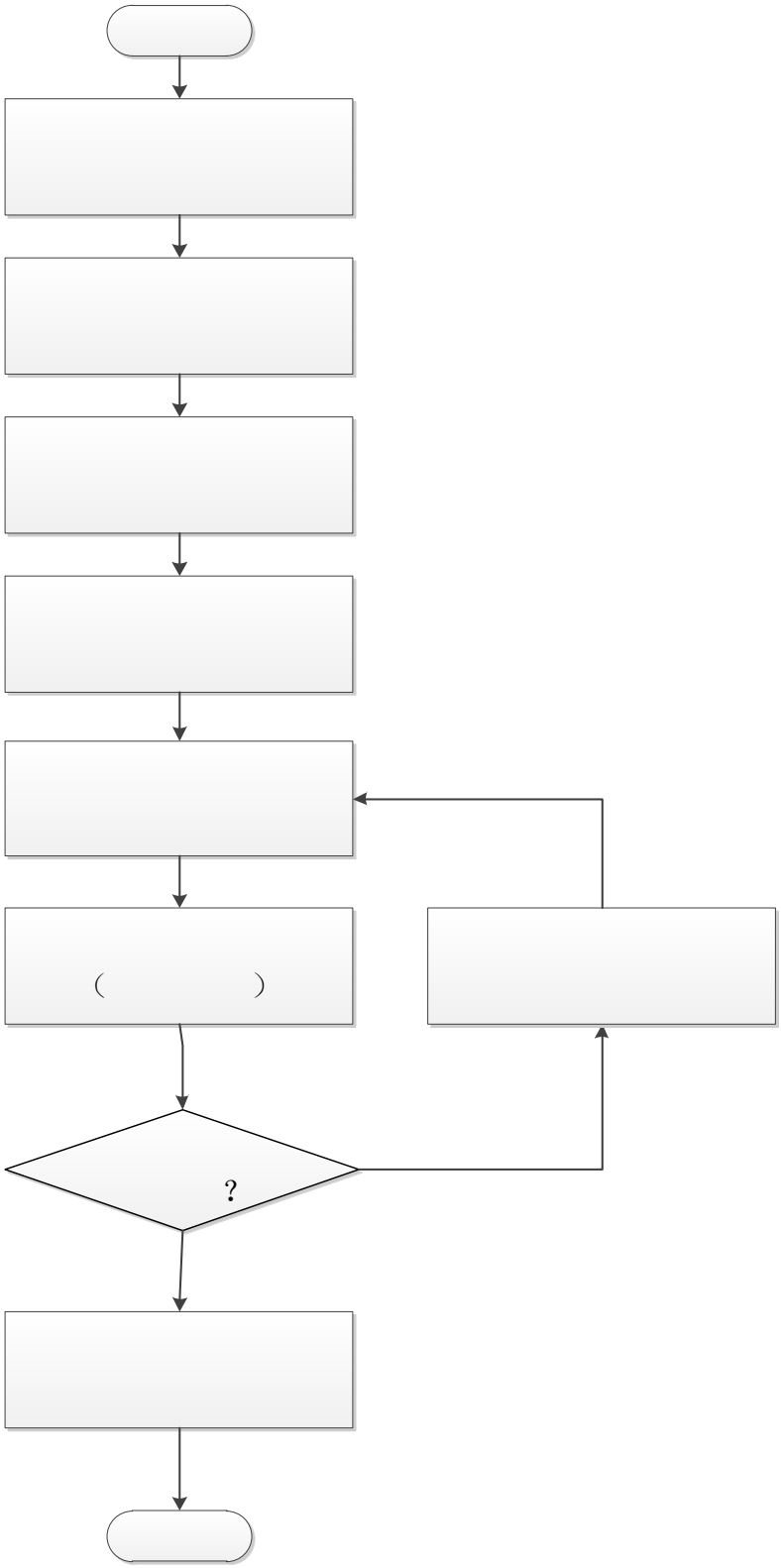


Fig. 24-8 I2C Flow chat for mix mode

!36 !

36/2 !

-
-
-
-
-

36/3 ! !

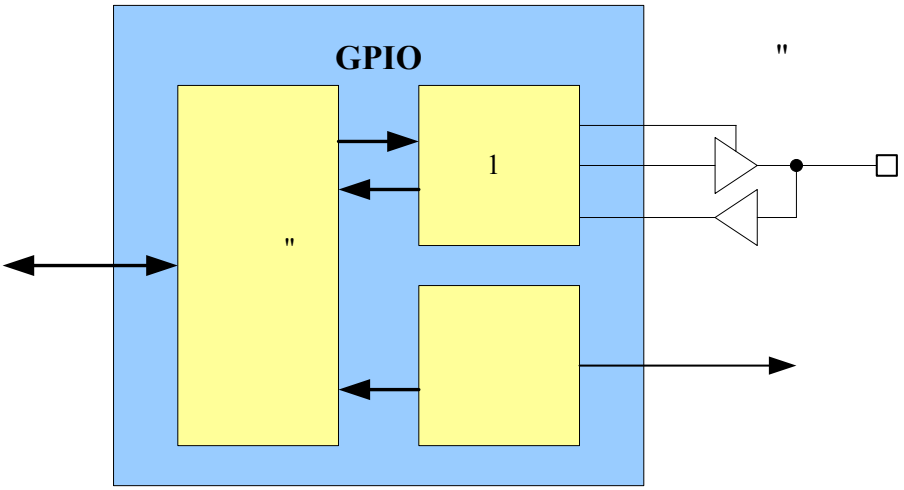


Fig. 25-1 GPIO block diagram

! !
B ! !

! 0 ! !

"

! !

0

36/4 ! !

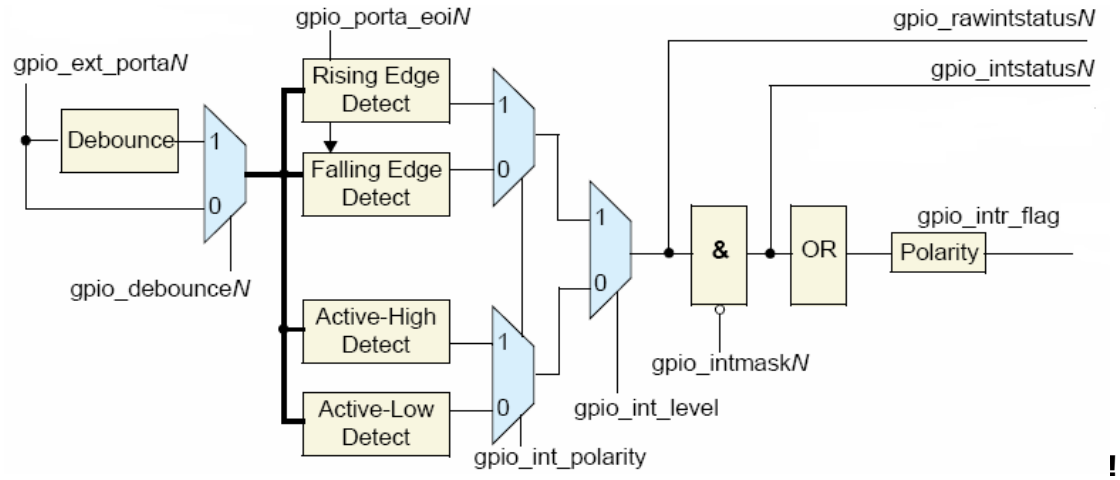
36/4/2 !

! !) !

! ! !

!

-
-
-
-
-



!

Fig. 25-2 GPIO Interrupt RTL Block Diagram

! !

! ! ! ! ! ! ! !

36.4.3 ! !

! !

-
-

-

! ! ! ! !

36.5 ! !

36.5.2 ! !

!	!	!	! !	!
_____				
_____				
_____				
_____				
_____				
_____				
_____				
_____				
_____				
_____				
_____				
_____				
_____				

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

36.5.3 ! ! !

_____B ____!

!	B !	! !	!

B !

!	B !	! !	!

!

!	B !	! !	!

B !

!	B !	! !	!

!

!	B !	! !	!

B !

!	B !	! !	!

B !

!	B !	! !	!

B B !

!	B !	! !	!

!

!	B !	! !	!

B !

!	B !	! !	!

B!

!	B !	! !	!

!

!	B !	! !	!

!

!	B !	! !	!

36/6 ! !

Table 25-1 GPIO interface description

! !	!	! !	! !
! 1! !			
2! !			

! !	!	! !	! !
3! !			
4!			
5!			

36/7 B ! !

! ! ! ! !

-
-
  ! ! ! ! !
-
-
  ! ! ! ! !
-
-
  ! ! ! ! ! ! !

-
-

-

Note: Please switch iomux to GPIO mode first!

!37 !

37/2 !

RK1808

-
-
-

37/3 ! !

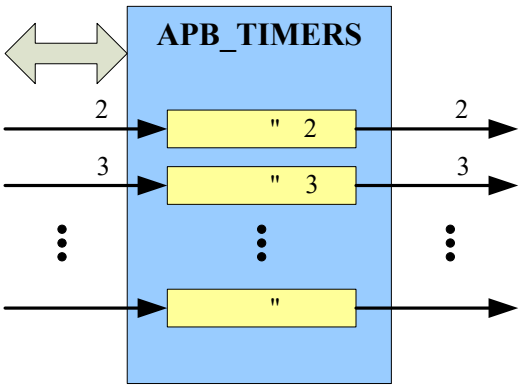


Fig. 26-1 Timer Block Diagram

37/4 ! !

37/4/2 ! !

37/4/3 ! !

⩽ ⩽

-
-
-

⩽ ⩽

⩽ ⩽

⩽ ⩽

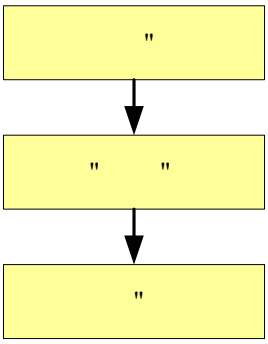


Fig. 26-2 Timer Usage Flow

37.4.4 ! ! ! ! !

-
-

-
-

37.4.5 ! ! !

-

-

37.5 ! !

37.5.2 ! !

!	!	!	! !	!

!	!	!	! !	!

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

37/5/3 ! ! !

B 1!

!	B !	!	!	!

B 2!

!	B !	!	!	!

B 1!

!	B !	!	!	!

B 2!

!	B !	!	!	!

!

!	B !	!	!	!

!	B !	! !	!

B !

!	B !	! !	!

37/6 B ! !

37/7 ! !B !

Table 26-1 Register Base Address

!!	!	!B !

37/8 ! ! !

⩽ ⩽

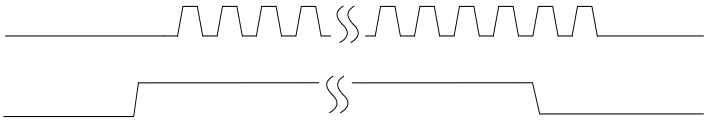


Fig. 26-3 Timing between timer_en and timer_clk

!38 ! ! !) !

38/2 !

-
-
  -
  -
  -
  -
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  -
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  -
  -
  -
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  -
  -
  -
-
-

38/3 ! !

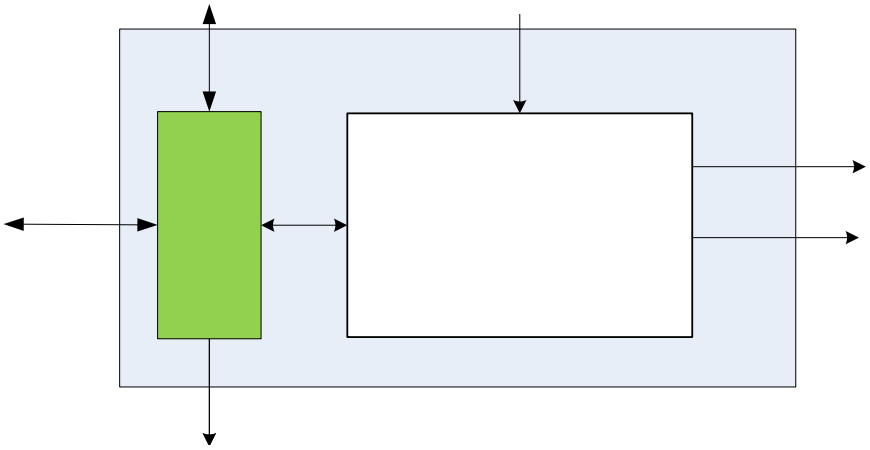

Fig. 27-1 PWM Block Diagram

38.4 ! !

38.4.2 ! !

Notes: the PWM input waveform is doubled buffered when the PWM channel is working in order to filter unexpected shot-time polarity transition, and therefore the interrupt is asserted several cycles after the input waveform polarity changes, and so does the change of the values of PWMx_PERIOD_HPC and PWMx_DUTY_LPC.

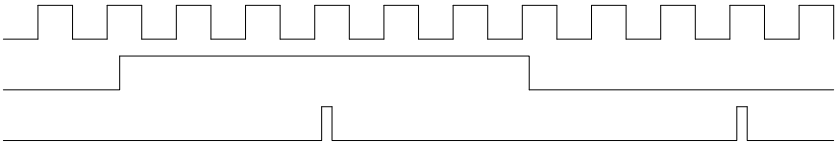

Fig. 27-2 PWM Capture Mode

38.4.3 ! !

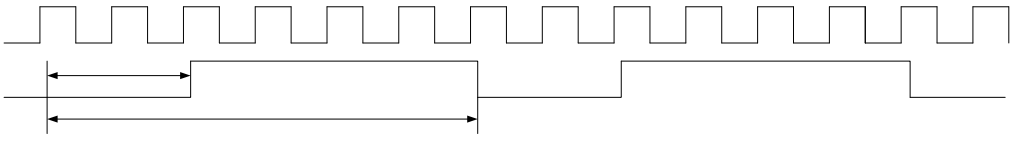

Fig. 27-3 PWM Continuous Left-aligned Output Mode

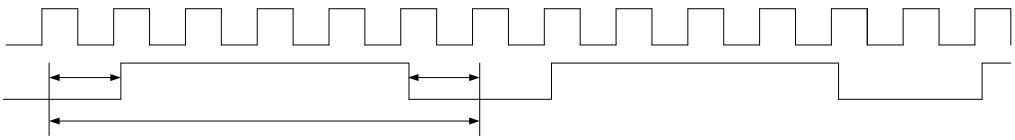

Fig. 27-4 PWM Continuous Center-aligned Output Mode

38.4.4 . ! !

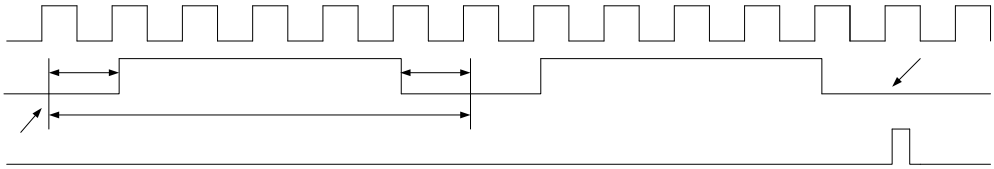

Fig. 27-5 PWM One-shot Center-aligned Output Mode

38.5 ! !

38.5.2 ! !

!	!	!	! !	!

!	!	!	! !	!

!	!	!	! !	!

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

38/5/3 ! ! !

1 !

!	B !	! !	!

1 !

!	B !	! !	!

1 !

!	B !	! !	!

1 !

!	B !	! !	!

!	B !	! !	!

2 !

!	B !	! !	!

2 !

!	B !	! !	!

!

2 !

!	B !	! !	!

2 !

!	B !	! !	!

!	B !	! !	!

3 !

!	B !	! !	!

!

3 !

!	B !	! !	!

3 !

!	B !	! !	!

3 !

!	B !	! !	!

!	B !	! !	!

4 !

!	B !	! !	!

4 !

!	B !	! !	!

4 !

!	B !	! !	!

4 !

!	B !	! !	!

!	B !	! !	!

!	B !	!	!	!

!	B !	! !	!

_____!

!	B !	! !	!

!	B !	! !	!

_____!

!	B !	! !	!

!	B !	! !	!

_____!

!	B !	! !	!

_____!

!	B !	! !	!

_____!

!	B !	! !	!

_____!

!	B !	! !	!

B !

!	B !	! !	!

B !

!	B !	! !	!

B !

!	B !	!	!	!

B !

!	B !	!	!	!

B !

!	B !	!	!	!

B !

!	B !	!	!	!

B B 1!

!	B !	!	!	!

B B 2!

!	B !	!	!	!

B B 3!

!	B !	!	!	!

B B 4!

!	B !	!	!	!

B B 5!

!	B !	!	!	!

B B 6!

!	B !	!	!	!

B B 7!

!	B !	!	!	!

B B 8!

!	B !	!	!	!

B B 9!

!	B !	!	!	!

B B : !

!	B !	!	!	!

4 B B !

!	B !	! !	!

!

!	B !	! !	!

38/6 ! !

Table 27-1 PWM Interface Description

! !	!	! !	! !

! !	!	! !	! !

Notes: I=input, O=output, I/O=input/output.

38/7 B ! !

38/7/2 ! ! ! ! ! !

38/7/3 ! ! B! ! ! ! !

38/7/4 ! ! ! ! ! ! ! !

!

38/7/5 ! . ! 0 ! ! ! !

38/7/6 . ! ! !

38/7/7 ! !

!39 !) !

39/2 !

RK1808

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-
-
-
  -
  -
-
-

39/3 ! !

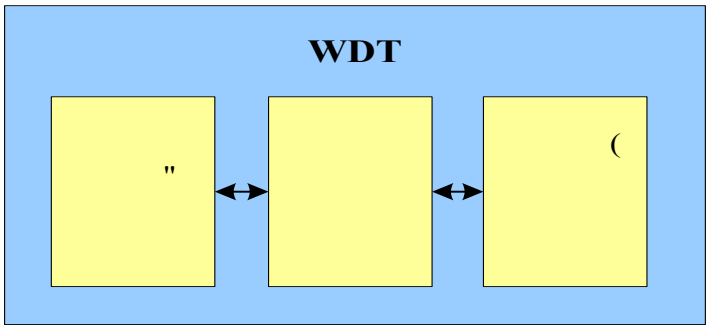

Fig. 28-1 WDT block diagram

! !

-
-
-

39/4 ! !

39/4/2 !

!

!

! !

! ! !

39/4/3 ! !
! ! !) ! >2 !

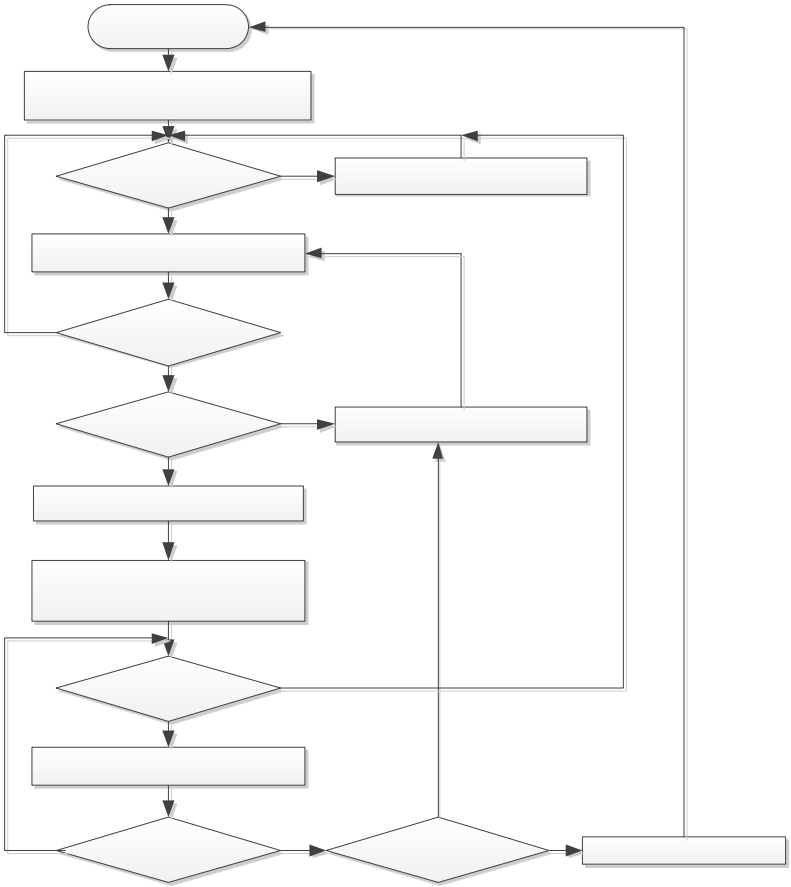

Fig. 28-2 WDT Operation Flow

39/5 ! !

39/5/2 ! !

!	!	!	! !	!
_____				

!	!	!	! !	!
_____				
_____				
_____				
_____				
_____				

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

39/5/3 ! ! !
_____!

!	B !	! !	!

_____!

!	B !	! !	!

!	B !	! !	!

_____!

!	B !	! !	!

_____!

!	B !	! !	!

_____B !

!	B !	! !	!

_____!

!	B !	! !	!

39/6 B ! !

!3: !B ! !B) B B !

3: /2 !

3: /3 ! !

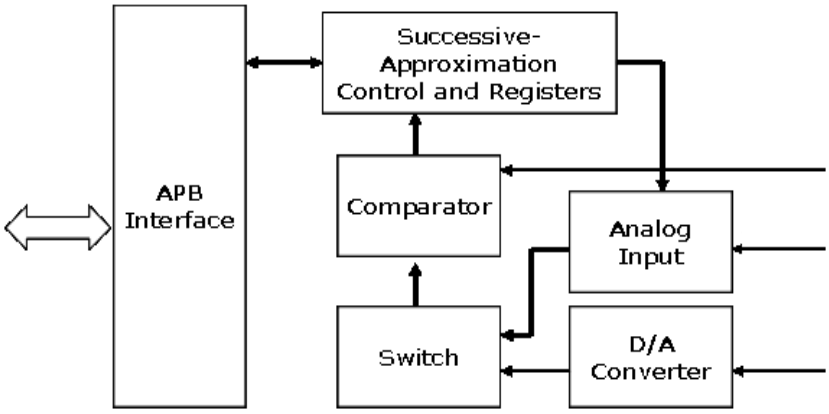

Fig. 29-1 SARADC block diagram

.B ! ! ! ! ! !

! !

3: /4 ! !

3: /4/2 B ! !

3: /5 ! !

3: /5/2 ! !

!	!	!	! !	!
_____				
_____				
_____				
_____				

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

3: /5/3 ! ! !
B B B B!

!	B !	! !	!

B B B !

!	B !	! !	!

B B !

!	B !	! !	!

B B !

!	B !	! !	!

!

3: /6 ! !

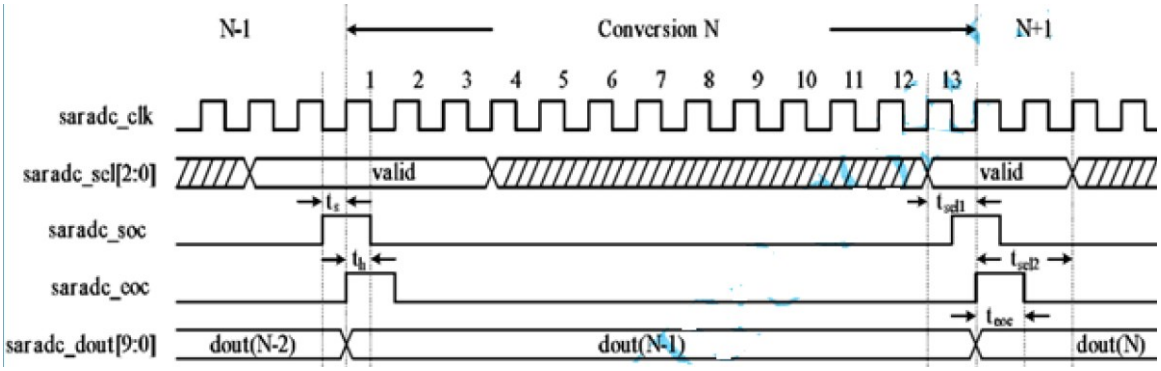

Fig. 29-2 SAR-ADC timing diagram in single-sample conversion mode

3: /7 B ! !

-
-
-
-
-

-

Note: The A/D converter was designed to operate at maximum 1MHZ.

!41 ! !B) B !

41 /2 !

-
-
-
-
-
-
-
-
-

41 /3 ! !

-
-

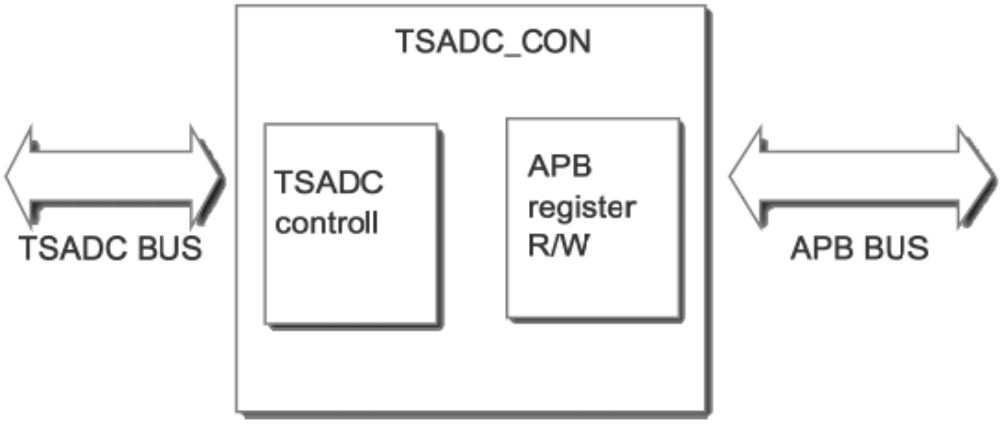

Fig. 30-1 TSADC Controller Block Diagram

41 /4 ! !

41 /4 /2 B ! !

41 /4 /3 B ! !

41.5 ! !

41.5.2 ! !

!			!	!
2				
2				
2				
2				

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

41.5.3 ! ! !

B !

!	B !	! !	!

!	B !	! !	!

B B !

!	B !	! !	!

B !

!	B !	! !	!

B !

!	B !	! !	!

!	B !	! !	!

B B B1!

!	B !	! !	!

B 1 !

!	B !	! !	!

B 1 !

!	B !	! !	!

B !

!	B !	! !	!

B !

!	B !	! !	!

B B !

!	B !	! !	!

B B !

!	B !	! !	!

B 1 !

!	B !	! !	!

41 /6 B ! !

41 /6 /2 . ! !

●

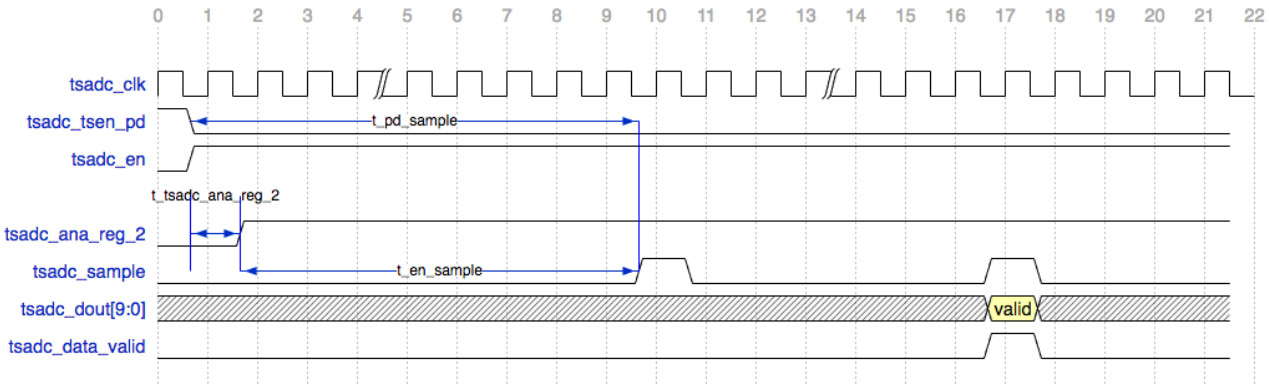

Fig. 30-2 The start flow to enable the Sensor and ADC

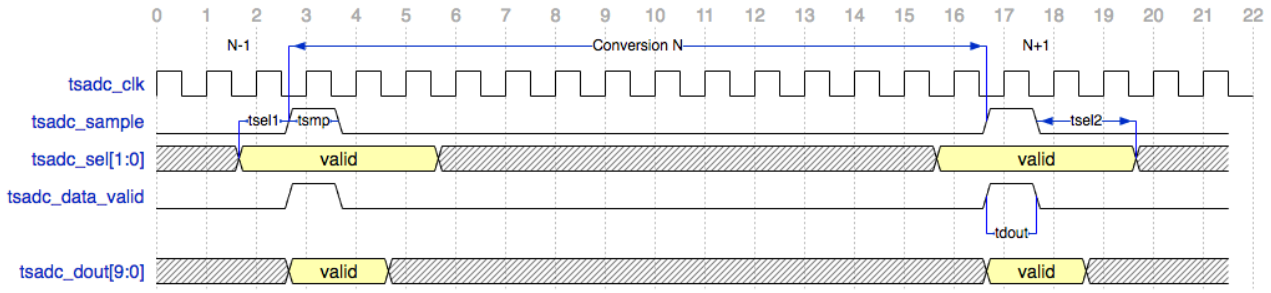

Fig. 30-3 TSADC timing diagram in bypass mode

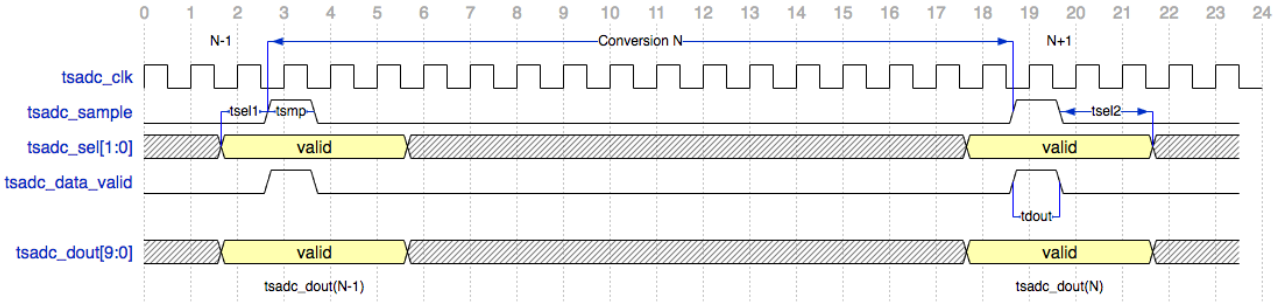

Fig. 30-4 TSADC timing diagram in normal mode with tsadc_clk_sel = 1'b0

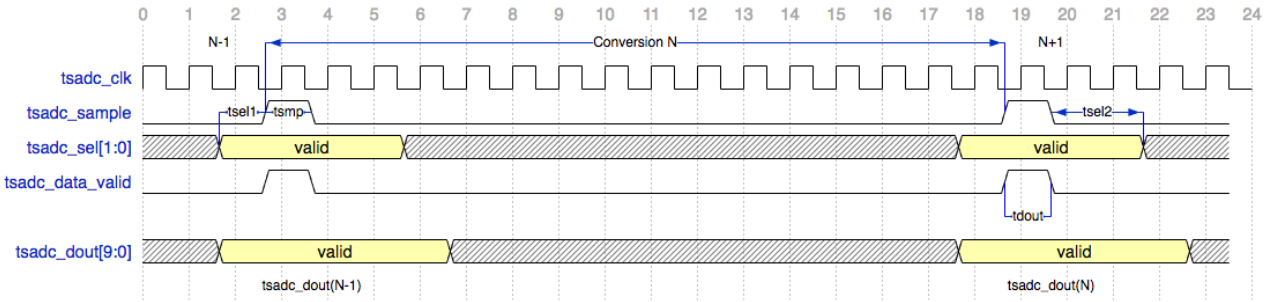

Fig. 30-5 TSADC timing diagram in normal mode with tsadc_clk_sel = 1'b1

41 /6 /3 . . ! !

Table 30-1 Temperature Code Mapping

0 !	**B ! ! !**		

0 !	B ! ! !		

Note: Table may be changed according to actually tested results.

41/6/4 . ! !

-

-

-

41/6/5 B ! !

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- ,
-
-
-
-

-
-