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2016-7-27	1.0	Update
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Chapter 1 Graphics Process Unit (GPU)

1.1 Overview

GPU provides a complete graphics acceleration platform based on open standards, With support for 2D graphics, 3D graphics, and GPGPU computing
The GPU supports the following graphics standards:

- OpenGL ES 3.0
- OpenGL ES 2.0
- OpenGL ES 1.1
- OpenCL 1.2
- OpenCL 1.1
- OpenCL 1.0
- DirectX 11.1
- DirectX 9

The GPU consists of:

- 4 Shader Cores
- 1 256KB Level2 Cache Memory Subsystem
- 1 Memory Management Unit
- 1 Job Manager
- 1 Hierarchical Tiler
- 1 Core Group

The GPU contains a 32-bit APB bus and a 128-bit AXI bus. CPU configures GPU through APB bus, GPU read and write data through AXI bus.
The GPU includes the following features:

- A rich API feature set with high-performance support for both shader-based and fixed-function graphics APIs.
- Anti-aliasing capabilities.
- An effective core for General Purpose computing on GPU (GPGPU) applications.
- High memory bandwidth and low power consumption for 3D graphics content.
- Scalability for products from smart phones to high-end mobile computing.
- Performance leading 3D graphics.
- Image quality using double-precision FP64.
- Standard bus interfaces.
- Latency tolerance.
- Compressed texture formats.
- Frame buffer compression.
- 10-bit and 16-bit YUV input and output formats.

1.2 Block Diagram

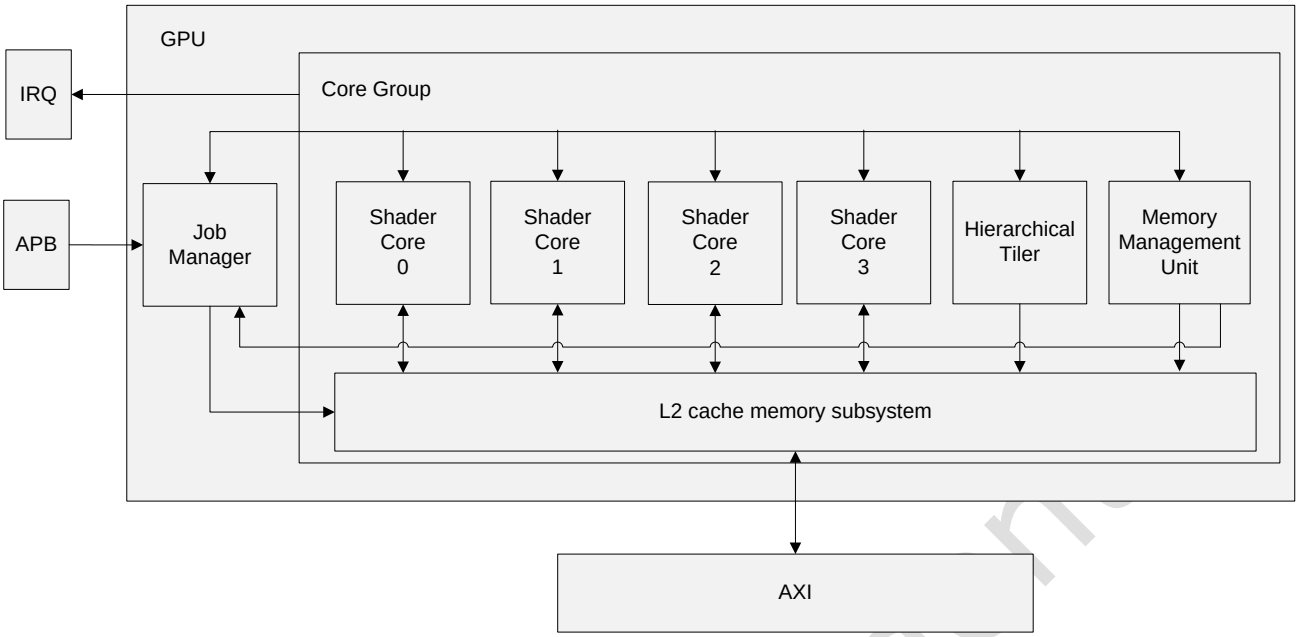


Fig. 1-1 GPU block diagram

• When the application software uses the graphics device driver to send a graphics job to the GPU. The job manager receives the job, interprets it, and then sends a series of graphics tasks to the functional units within the GPU.
• The shader cores are the main processing engines of the GPU. The shader cores carry out all the rendering and computation operations.
• The tiler creates lists of all the objects in a scene, so that the shader cores process the objects efficiently.
• The memory management unit performs virtual address to physical address translation of external AXI interface accesses.
• The level 2 cache memory subsystem provides additional caching for all internal master blocks.
• The interrupts are generated for job handling, memory management, and events not tied to a specific shader core.

1.3 Function Description

When the application software, running on the application processor, schedules a job to be sent to the GPU, the following actions take place:
1. The application processor graphics device driver takes graphics data from a user application, packages it, and sends it as a series of graphics jobs to the job manager.
2. The graphics device driver places the description and data to be used for the graphics jobs into the shared memory in the form of job descriptors stored in defined data structures.
3. The graphics device driver also sets up the high-level configuration of the GPU using configuration registers that communicate with the job manager using the register interface.
4. The job manager reads the descriptions of the graphics jobs from shared memory.
5. The job manager converts the graphics jobs into multiple small GPU tasks that are then distributed to the GPU modules where they are processed.
6. When the tasks complete, the results of the graphics jobs are placed back into shared memory.
7. The application processor is notified that the jobs are complete.
When a graphics job starts, it proceeds to completion without having to refer back to the application processor for more information. When the job is complete it can, if necessary, start the next graphics job without further interaction with the application processor.
There are three top level interrupts raised by the GPU:
• GPU interrupts Exceptions that are not associated with specific jobs.
• Job interrupts Signals the completion or failure of a job running on the GPU.

• MMU interrupts Exceptions caused by memory management.
The application processor interprets the interrupts generated by the GPU . The software queries the states of the registers in the job manager to determine what must be done to handle the interrupt. The job manager is not required to wait for the result of the interrupt, it can be starting on the next set of jobs to be executed.

1.4 Timing Diagram

The GPU only has a clock input, which is called aclk_gpu. aclk_gpu is generated from the CRU module as shows below

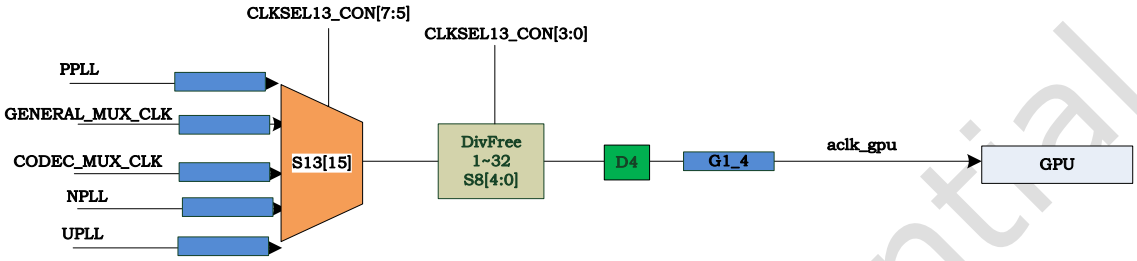


Fig. 1-2 ACLK_GPU generate block diagram

We can configure CPLL, GPLL, NPLL, PPLL,UPLL and CRU register CRU_CLKSEL13_CON to control the gpu_aclk frequency.

1.5 Register Description

The GPU base addressis 0xff9a_0000.

Chapter 2 Raster Graphic Acceleration (RGA)

2

2.1 Overview

RGA is a separate 2D raster graphic acceleration unit. It accelerates 2D graphics operations, such as point/line drawing, image scaling, rotation, BitBLT, alpha blending and image blur/sharpness.
RGA supports the following features:

- **Data format**
  - Input data:
    ARGB/RGB888/RGB565/RGB4444/RGB5551/YUV420/YUV422
    Support YUV422SP10bit/YUV420SP10bit
  - Output data:
    ARGB/RGB888/RGB565/RGB4444/RGB5551/YUV420/YUV422
    Support YVYU422/420 output in enhanced version(RGA2E)
  - Pixel Format conversion, BT.601/BT.709
  - Dither operation
  - Max resolution: 8192x8192 source, 4096x4096 destination
- **Scaling**
  - Down-scaling: Average filter
  - Up-scaling: Bi-cubic filter(source>2048 would use Bi-linear)
  - Arbitrary non-integer scaling ratio，from 1/16 to 16
- **Rotation**
  - 0, 90, 180, 270 degree rotation
  - x-mirror, y-mirror & rotation operation
- **BitBLT**
  - Block transfer
  - Color palette/Color fill, support with alpha
  - Transparency mode (color keying/stencil test, specified value/value range)
  - Two source BitBLT:
  - A+B=B only BitBLT, A support rotate&scale when B fixed
  - A+B=C second source (B) has same attribute with (C) plus rotation function
- **Alpha Blending**
  - New comprehensive per-pixel alpha(color/alpha channel separately)
  - Fading
- **Raster operation**
  - ROP2/ROP3/ROP4
- **MMU**
  - 4k/64k page size
  - Four channel: SRC/SRC1/DST/CMD, individual base address and enable control bit
  - TLB pre-fetch

2.2 Block Diagram

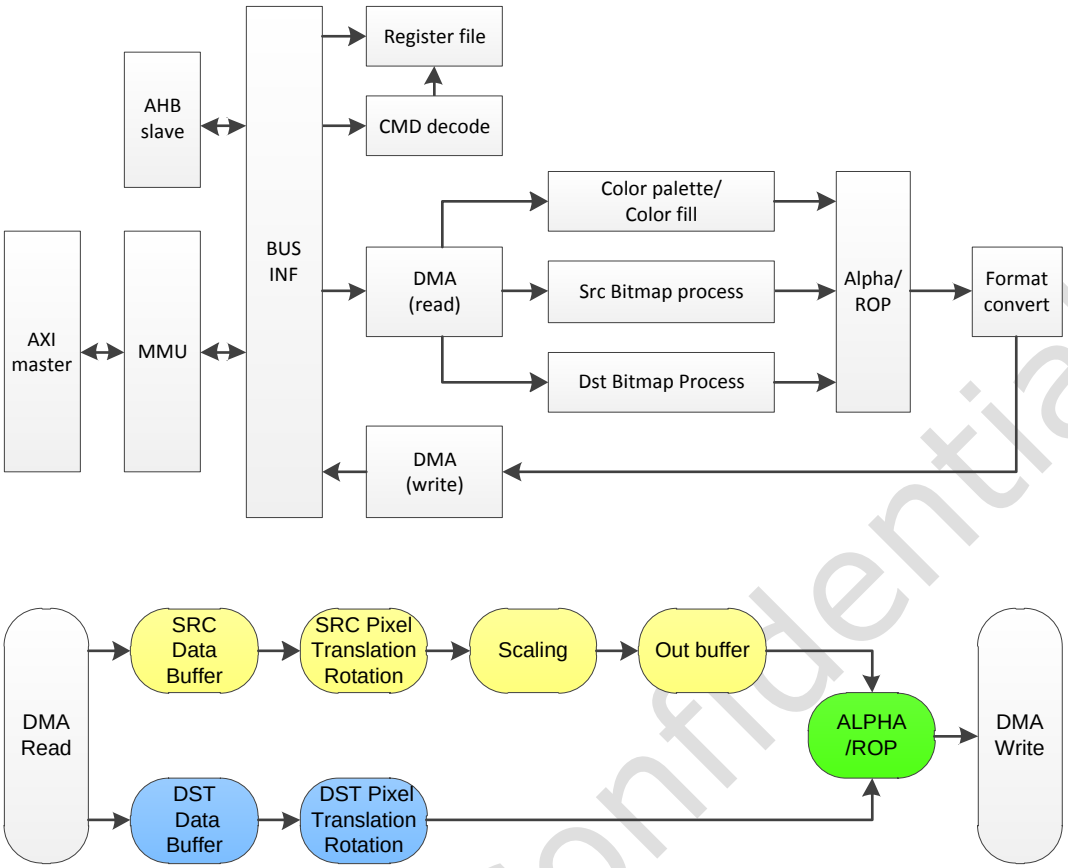


Fig. 2-1 RGA Block Diagram

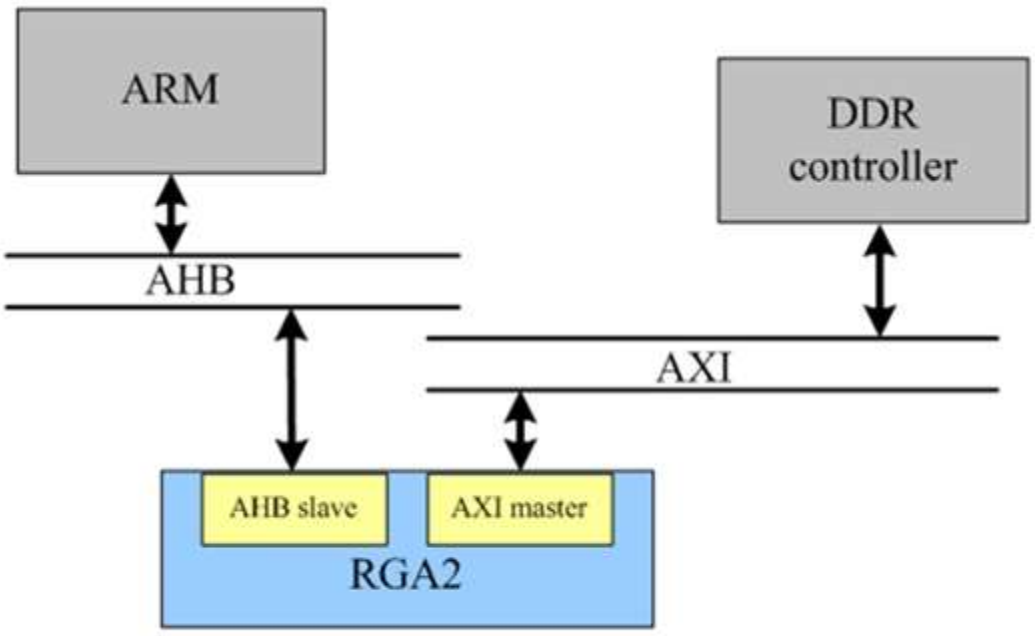


Fig. 2-2 RGA2 in SOC

2.3 Function Description

2.3.1 Data Format

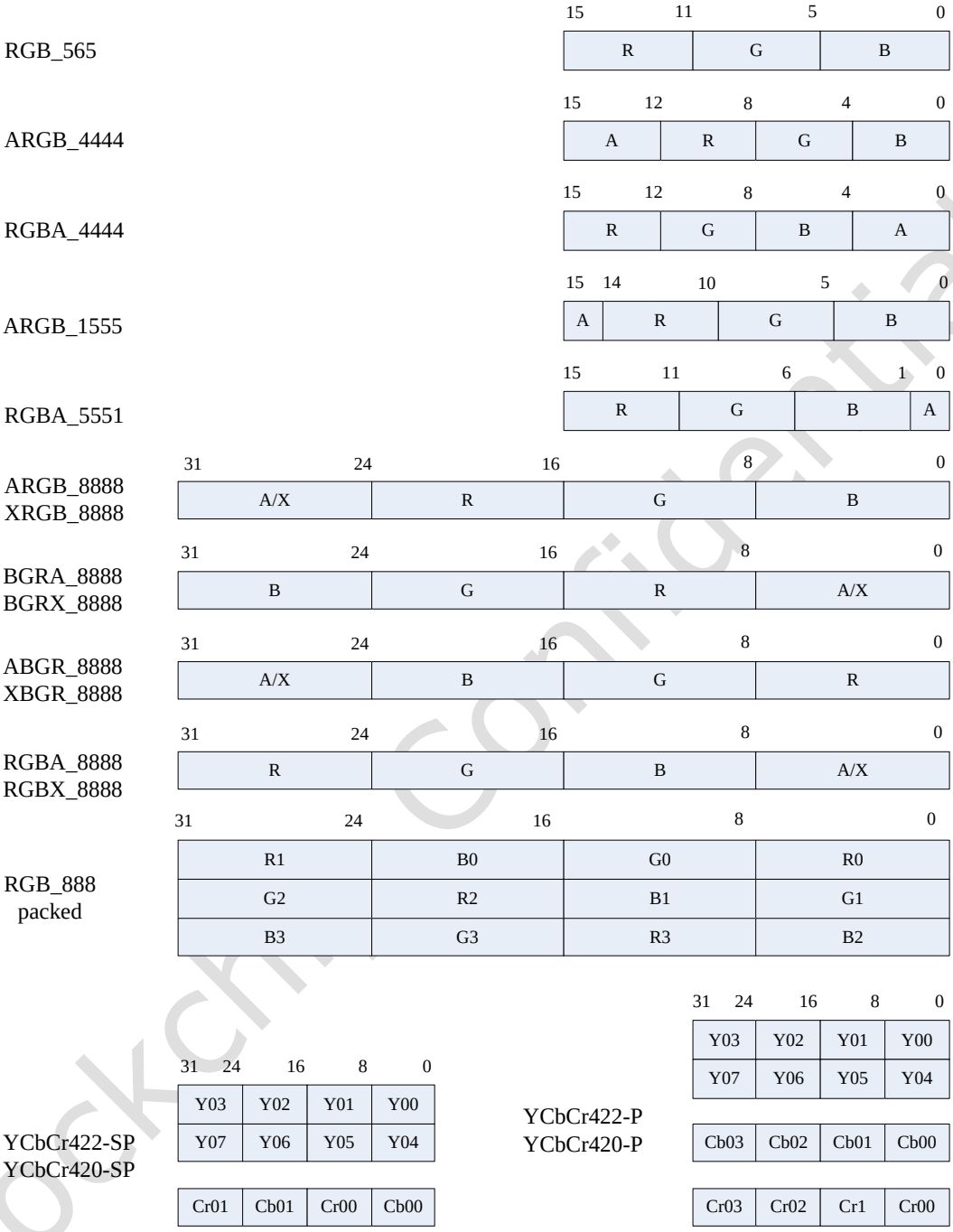


Fig. 2-3 RGA Input Data Format

All input datas (defined by SRC_IN_FMT/DST_IN_FMT) are converted to ABGR8888. The results are converted to the output data format (defined by DST_OUT_FMT).

2.3.2 Dithering

There could have dithering operation for source image when the source image format is not RGB565 and the destination format is RGB565.
The down-dithering is done using Dither Allegro.

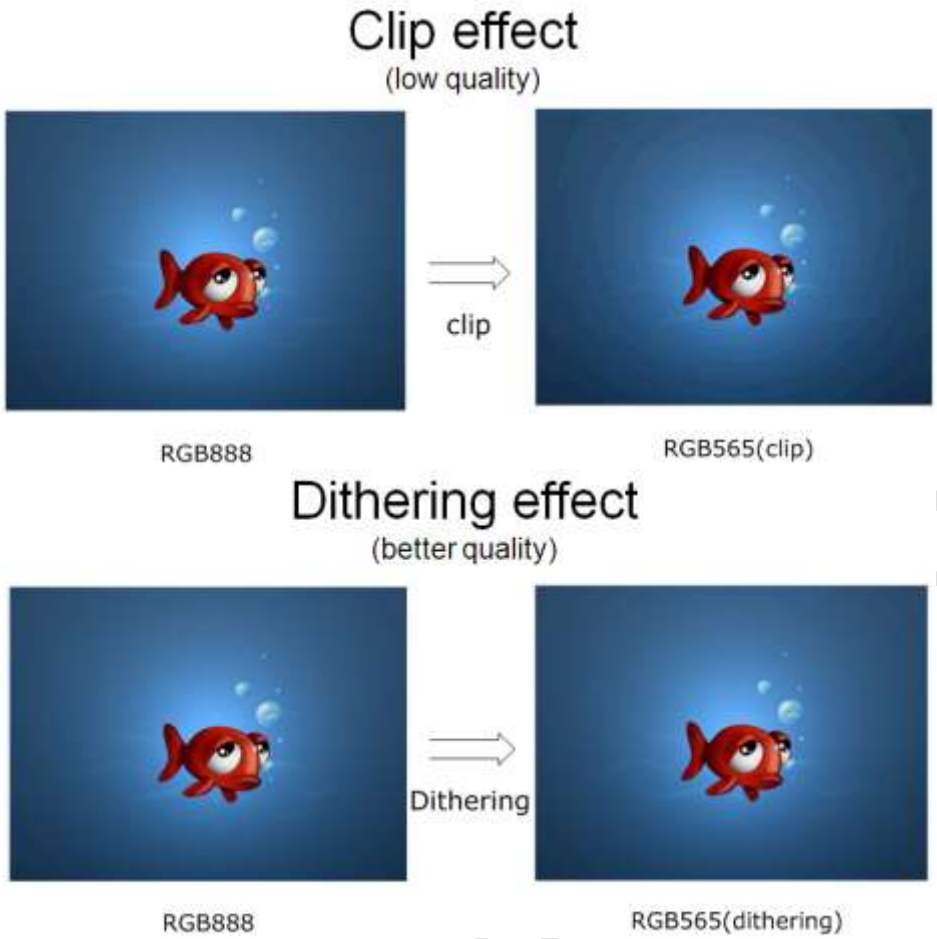
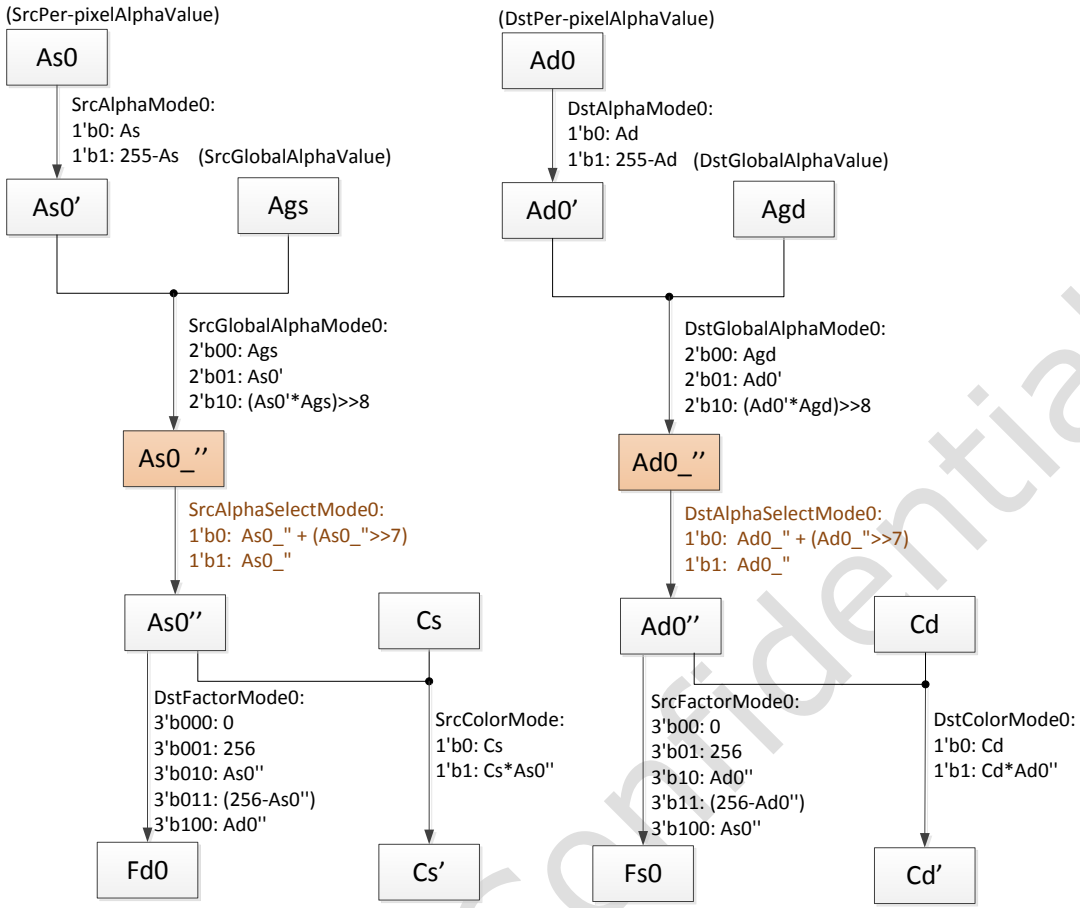


Fig. 2-4 RGA Dither effect

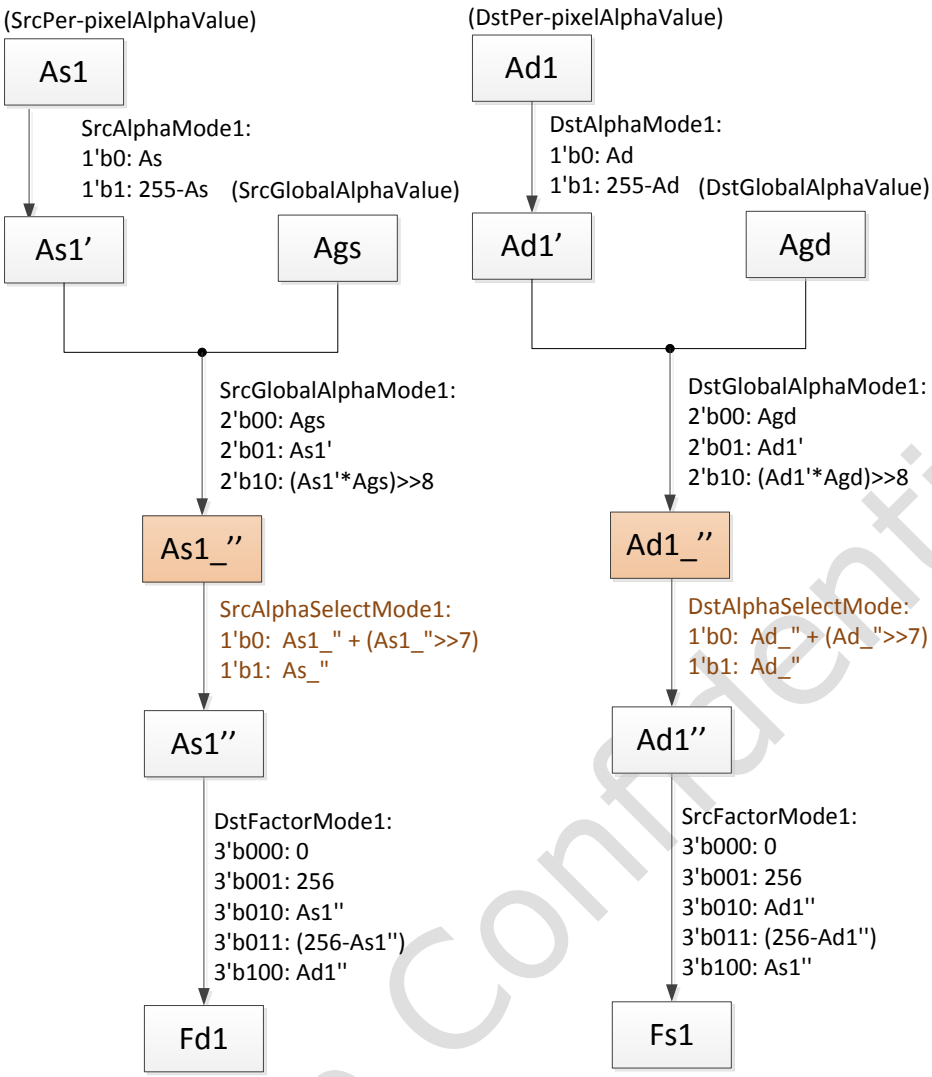
2.3.3 Alpha mode



$$Cd = Fs0 * Cs' + Fd0 * Cd' \quad (1)$$

(Cd – dst color, Fs0 – color src factor0, Cs' – src color', Fd0 – color dst factor0, Cd' – dst color')

Fig. 2-5 layer0 alpha blending calculate flow



$$Ad = Fs1 * As1'' + Fd1 * Ad1'' \quad (2)$$

(Ad – dst alpha, Fs1 – alpha src factor1, As1'' – src alpha'', Fd1 – alpha dst factor1, Ad1' – dst alpha'')

Fig. 2-6 layer1 alpha blending calculate flow

2.3.4 Color fill

Two modes of color fill can be done by RGA: solid fill and gradient fill.

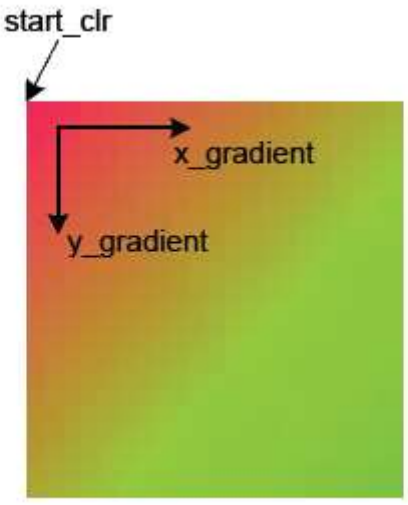


Fig. 2-7 RGA Gradient Fill

Gradient fill using following equations for ARGB calculation of every pixel in different

coordinary.

A_cur = (A_start + x*x_A_gradient) +y*y_A_gradient;
R_cur = (R_start + x*x_R_gradient) +y*y_R_gradient;
G_cur = (G_start + x*x_G_gradient) +y*y_G_gradient;
B_cur = (B_start + x*x_B_gradient) +y*y_B_gradient;

A_start, R_start, G_start, B_start is the ARGB value of start point. There are four pairs of values for horizontal and vertical gradient. Saturation operation could be enabled or disabled if the color overflows 255 or underflows 0.

2.3.5 Raster Operation (ROP)

Raster operation (ROP) is a Boolean operation between operands, which involve AND, OR, XOR, and NOT operations. For ROP2, operands are P (select pan) and D (Destination bitmap). For ROP3, operands are P (pattern), S (source bitmap) and D (Destination bitmap). For ROP4, operands are P (pattern), S (source bitmap), D (Destination bitmap) and MASK.

Table 2-1 RGA ROP Boolean operations

Operator	Meaning
a	Bitwise AND
n	Bitwise NOT (inverse)
o	Bitwise OR
x	Bitwise exclusive OR (XOR)

2.3.6 Scaling

The scaling operation is the image resizing processing of source image. Scaling is done base on ARGB8888 format.
There are three scale modes: scale down (bilinear, Average); scale up(bilinear, Bi-cubic);

2.4 Register Description

2.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

2.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
RGA2_SYS_CTRL	0x0000	W	0x00000044	RGA system control register
RGA2_CMD_CTRL	0x0004	W	0x00000000	RGA command control register
RGA2_CMD_BASE	0x0008	W	0x12345678	RGA command codes base address register
RGA2_STATUS1	0x000c	W	0x00000000	RGA status register
RGA2_INT	0x0010	W	0x00000000	RGA interrupt register
RGA2_MMU_CTRL0	0x0014	W	0x00000000	RGA MMU control 0 register
RGA2_MMU_CMD_BASE	0x0018	W	0x00000000	Register0000 Abstract
RGA2_STATUS2	0x001c	W	0x00000000	RGA status register
RGA2_WORK_CNT	0x0020	W	0x00000000	work counter
RGA2_VERSION_INFO	0x0028	W	0x00000000	Version number for rga
RGA2_PERF_LATENCY_CTRL0	0x0040	W	0x00000028	Axi performance latency module contrl register0
RGA2_PERF_LATENCY_CTRL1	0x0044	W	0x00000021	PERF_LATENCY_CTRL1
RGA2_PERF_RD_MAX_LATENCY_NUM0	0x0048	W	0x00000000	Read max latency number

Name	Offset	Size	Reset Value	Description
RGA2_PERF_RD_LATENCY_SAMP_NUM	0x004c	W	0x00000000	The number of bigger than configed threshold value
RGA2_PERF_RD_LATENCY_ACC_SUM	0x0050	W	0x00000000	Total sample number
RGA2_PERF_RD_AXI_TOTAL_BYTE	0x0054	W	0x00000000	perf_rd_axi_total_byte
RGA2_PERF_WR_AXI_TOTAL_BYTE	0x0058	W	0x00000000	perf_wr_axi_total_byte
RGA2_PERF_WORKING_CNT	0x005c	W	0x00000000	perf_working_cnt
RGA2_MODE_CTRL	0x0100	W	0x00000000	RGA mode control register
RGA2_SRC_INFO	0x0104	W	0x00000000	RGA source information register
RGA2_SRC_BASE0	0x0108	W	0x00000000	source image Y/RGB base address
RGA2_SRC_BASE1	0x010c	W	0x00000000	RGA source image Cb/Cbr base address register
RGA2_SRC_BASE2	0x0110	W	0x00000000	RGA source image Cr base address register
RGA2_SRC_BASE3	0x0114	W	0x00000000	RGA source image 1 base address register
RGA2_SRC_VIR_INFO	0x0118	W	0x00000000	RGA source image virtual stride / RGA source image tile number
RGA2_SRC_ACT_INFO	0x011c	W	0x00000000	RGA source image active width/height register
RGA2_SRC_X_FACTOR	0x0120	W	0x00000000	RGA source image horizontal scaling factor
RGA2_SRC_Y_FACTOR	0x0124	W	0x00000000	RGA source image vertical scaling factor
RGA2_SRC_BG_COLOR	0x0128	W	0x00000000	RGA source image background color
RGA2_SRC_FG_COLOR	0x012c	W	0x00000000	RGA source image foreground color
RGA2_SRC_TR_COLOR0	0x0130	W	0x00000000	RGA source image transparency color min value
RGA2_CP_GR_A	0x0130	W	0x00000000	RGA source image transparency color min value
RGA2_SRC_TR_COLOR1	0x0134	W	0x00000000	Register0000 Abstract
RGA2_CP_GR_B	0x0134	W	0x00000000	RGA source image transparency color max value
RGA2_DST_INFO	0x0138	W	0x00000000	RGA destination format register
RGA2_DST_BASE0	0x013c	W	0x00000000	RGA destination image base address 0 register
RGA2_DST_BASE1	0x0140	W	0x00000000	RGA destination image base address 1 register
RGA2_DST_BASE2	0x0144	W	0x00000000	RGA destination image base address 2 register

Name	Offset	Size	Reset Value	Description
RGA2_DST_VIR_INFO	0x0148	W	0x00000000	RGA destination image virtual width/height register
RGA2_DST_ACT_INFO	0x014c	W	0x00000000	RGA destination image active width/height register
RGA2_ALPHA_CTRL0	0x0150	W	0x00000000	Alpha control register 0
RGA2_ALPHA_CTRL1	0x0154	W	0x00000000	Register0000 Abstract
RGA2_FADING_CTRL	0x0158	W	0x00000000	Fading control register
RGA2_PAT_CON	0x015c	W	0x00000000	Pattern size/offset register
RGA2_ROP_CON0	0x0160	W	0x00000000	ROP code 0 control register
RGA2_CP_GR_G	0x0160	W	0x00000000	RGA color gradient fill step register (color fill mode)
RGA2_ROP_CON1	0x0164	W	0x00000000	ROP code 1 control register
RGA2_CP_GR_R	0x0164	W	0x00000000	RGA color gradient fill step register (color fill mode)
RGA2_MASK_BASE	0x0168	W	0x00000000	RGA mask base address register
RGA2_MMU_CTRL1	0x016c	W	0x00000000	RGA MMU control register 1
RGA2_MMU_SRC_BASE	0x0170	W	0x00000000	RGA source MMU TLB base address
RGA2_MMU_SRC1_BASE	0x0174	W	0x00000000	RGA source1 MMU TLB base address
RGA2_MMU_DST_BASE	0x0178	W	0x00000000	RGA destination MMU TLB base address
RGA2_MMU_ELS_BASE	0x017c	W	0x00000000	RGA ELSE MMU TLB base address

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

2.4.3 Detail Register Description

RGA2_SYS_CTRL

Address: Operational Base + offset (0x0000)

RGA system control register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x0	sw_rst_handsave_p it would save protect-rstn into initial status if long time dead in protect-rstn status. (auto clear into '0')
6	RW	0x1	sw_rst_protect_e protect-rstn mode enable. it would be ensure all axi write/read operation into completion status when sw_cclk_sreset_p or sw_aclk_sreset_p valid.
5	RW	0x0	sw_auto_rst it would auto-resetn after one frame finish. 0: disable 1: enable
4	RW	0x0	sw_cclk_sreset_p RGA core clk domain Soft reset, write '1' to this would reset the RGA engine except config registers.

Bit	Attr	Reset Value	Description
3	WO	0x0	sw_aclk_sreset_p RGA aclk domain Soft reset, write '1' to this would reset the RGA engine except config registers.
2	WO	0x1	sw_auto_ckg RGA auto clock gating enable bit 0：disable 1：enable
1	WO	0x0	sw_cmd_mode RGA command mode 0：slave mode 1：master mode
0	W1C	0x0	sw_cmd_op_st_p RGA operation start bit Only used in passive (slave) control mode

RGA2_CMD_CTRL
Address: Operational Base + offset (0x0004)
RGA command control register

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:3	RW	0x000	sw_cmd_incr_num RGA command increment number
2	WO	0x0	sw_cmd_stop RGA command stop mode Command execution would stop after the current graphic operation finish if set this bit to 1
1	WO	0x0	sw_cmd_incr_valid_p RGA command increment valid (Auto cleared) When setting this bit, 1. The total cmd number would increase by the RGA_INCR_CMD_NUM. 2. RGA would continue running if idle.
0	RW	0x0	sw_cmd_line_st_p RGA command line fetch start (command line reset) (Auto cleared) When fetch start, the total cmd number would reset to RGA_INCR_CMD_NUM.

RGA2_CMD_BASE
Address: Operational Base + offset (0x0008)
RGA command codes base address register

Bit	Attr	Reset Value	Description
31:0	RW	0x12345678	sw_cmd_base RGA command codes base address

RGA2_STATUS1

Address: Operational Base + offset (0x000c)
RGA status register

Bit	Attr	Reset Value	Description
31:20	RO	0x000	sw_cmd_total_num RGA command total number
19:8	RO	0x000	sw_cmd_cur_num RGA command current number
7:1	RO	0x00	Reserved Reserved
0	RO	0x0	sw_rga_sta RGA engine status 0: idle 1: working

RGA2_INT
Address: Operational Base + offset (0x0010)
RGA interrupt register

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10	RW	0x0	sw_intr_af_e All command finished interrupt enable
9	RW	0x0	sw_intr_mmu_e MMU interrupt enable
8	RW	0x0	sw_intr_err_e Error interrupt enable
7	WO	0x0	sw_intr_cf_clr Current command finished interrupt clear
6	WO	0x0	sw_intr_af_clr All command finished interrupt clear
5	WO	0x0	sw_intr_mmu_clr MMU interrupt clear
4	WO	0x0	sw_intr_err_clr Error interrupt clear
3	RO	0x0	sw_intr_cf Current command finished interrupt flag
2	RO	0x0	sw_intr_af All command finished interrupt flag
1	RO	0x0	sw_intr_mmu MMU interrupt
0	RO	0x0	sw_intr_err Error interrupt flag

RGA2_MMU_CTRL0
Address: Operational Base + offset (0x0014)
RGA MMU control 0 register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:11	RW	0x000000	Reserved Reserved
10:9	RW	0x0	sw_els_ch_priority sw_els_ch_priority
8:7	RW	0x0	sw_dst_ch_priority sw_dst_ch_priority
6:5	RW	0x0	sw_src1_ch_priority sw_src1_ch_priority
4:3	RW	0x0	sw_src_ch_priority sw_src_ch_priority
2	RW	0x0	sw_cmd_mmu_flush RGA CMD channel MMU TLB flush: Set 1 to this bit to flush MMU TLB, auto clear
1	RW	0x0	sw_cmd_mmu_en RGA CMD channel MMU enable 0: disable 1: enable
0	RW	0x0	sw_mmu_page_size RGA MMU Page table size 0: 4KB page 1: 64KB page

RGA2_MMU_CMD_BASE
Address: Operational Base + offset (0x0018)
Register0000 Abstract

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_mmu_cmd_base RGA command MMU TLB base address (word)

RGA2_STATUS2
Address: Operational Base + offset (0x001c)
RGA status register

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	Reserved
12:11	RO	0x0	rpp_mkram_rready rpp_mkram_rready
10:6	RO	0x00	dstrpp_outbuf_rready dstrpp_outbuf_rready
5:2	RO	0x0	srcrpp_outbuf_rready dstrpp_outbuf_rready
1	RO	0x0	bus_error

Bit	Attr	Reset Value	Description
0	RO	0x0	rpp_error

RGA2_WORK_CNT
Address: Operational Base + offset (0x0020)
work counter

Bit	Attr	Reset Value	Description
31:27	RW	0x00	Reserved
26:0	RO	0x0000000	sw_work_cnt working counter register RGA total working counter

RGA2_VERSION_INFO
Address: Operational Base + offset (0x0028)
Version number for rga

Bit	Attr	Reset Value	Description
31:24	RW	0x00	major IP major vertion used for IP structure version infomation
23:20	RW	0x0	minor minor vertion big feature change under same structure
19:0	RW	0x00000	svnbuild rtl current svn number

RGA2_PERF_LATENCY_CTRL0
Address: Operational Base + offset (0x0040)
Axi performance latency module contrl register0

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:8	RW	0x000	sw_rd_latency_thr
7:4	RW	0x2	sw_rd_latency_id
3	RW	0x0	sw_axi_cnt_type
2	RW	0x1	sw_axi_perf_frm_type latency mode 1'b0: clear by software configuration 1'b1: clear by frame end
1	RW	0x0	sw_axi_perf_clr_e 1'b0: software clear disable 1'b1: software clear enalbe

Bit	Attr	Reset Value	Description
0	RW	0x0	sw_axi_perf_work_e 1'b0: disable 1'b1: enable

RGA2_PERF_LATENCY_CTRL1
Address: Operational Base + offset (0x0044)
PERF_LATENCY_CTRL1

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:8	RW	0x0	sw_aw_count_id
7:4	RW	0x2	sw_ar_count_id
3	RW	0x0	sw_aw_cnt_id_type
2	RW	0x0	sw_ar_cnt_id_type
1:0	RW	0x1	sw_addr_align_type

RGA2_PERF_RD_MAX_LATENCY_NUM0
Address: Operational Base + offset (0x0048)
Read max latency number

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RO	0x0000	rd_max_latency_num_ch0 read max latency value of channel 0

RGA2_PERF_RD_LATENCY_SAMP_NUM
Address: Operational Base + offset (0x004c)
The number of bigger than configed threshold value

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rd_latency_thr_num_ch0 read latency thr number channel 0

RGA2_PERF_RD_LATENCY_ACC_SUM
Address: Operational Base + offset (0x0050)
Total sample number

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rd_latency_acc_sum

RGA2_PERF_RD_AXI_TOTAL_BYTE
Address: Operational Base + offset (0x0054)
perf_rd_axi_total_byte

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_rd_axi_total_byte

RGA2_PERF_WR_AXI_TOTAL_BYTE
Address: Operational Base + offset (0x0058)
perf_wr_axi_total_byte

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_wr_axi_total_byte

RGA2_PERF_WORKING_CNT
Address: Operational Base + offset (0x005c)
perf_working_cnt

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_working_cnt

RGA2_MODE_CTRL
Address: Operational Base + offset (0x0100)
RGA mode control register

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved Reserved
7	RW	0x0	sw_intr_cf_e Current command finished interrupt enable
6	RW	0x0	sw_gradient_sat Gradient saturation calculation mode 0:clip 1:not-clip
5	RW	0x0	sw_alpha_zero_key ARGB888 alpha zero key mode 0x000000 would be changed to 0x000100(RGB888)/0x0020(RGB565)for ARGB888 to RGBX/RGB565 color key 0: disable 1: enable
4	RW	0x0	sw_cf_rop4_pat Color fill/ROP4 pattern 0: solid color 1: pattern color
3	RW	0x0	sw_bb_mode Bitblt mode 0: SRC + DST => DST 1: SRC + SRC1 => DST

Bit	Attr	Reset Value	Description
2:0	RW	0x0	sw_render_mode RGA 2D render mode 000: Bitblt 001: Color palette 010: Rectangle fill 011: Update palette LUT/pattern ram

RGA2_SRC_INFO
Address: Operational Base + offset (0x0104)
RGA source information register

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	sw_src_yuv10_round_e this bit valid when RGA support yuv 10bit picture input 0: yuv 10bit to 8bit round disable 1: yuv 10bit to 8bit round enable
27	RW	0x0	sw_src_yuv10_e this bit valid when RGA support yuv 10bit picture input 0: yuv 10bit disable 1: yuv 10bit enalbe
26	RW	0x0	sw_vsp_mode 0:by-cubic 1:bi-linear
25:24	RW	0x0	sw_bic_coe_sel SRC bicubic scaling coefficient select 00: CATROM 01: MITCHELL 10: HERMITE 11: B-SPLINE
23	RW	0x0	sw_src_dither_up SRC dither up enable 0:disable 1:enable
22:19	RW	0x0	sw_src_trans_e Source transparency enable bits [3]: A value stencil test enable bit [2]: B value stencil test enable bit [1]: G value stencil test enable bit [0]: R value stencil test enable bit
18	RW	0x0	sw_src_trans_mode Source transparency mode 0: normal stencil test (color key) 1: inverted stencil test

Bit	Attr	Reset Value	Description
17:16	RW	0x0	sw_src_vscl_mode SRC vertical scaling mode 00：no scaling 01: down-scaling 10: up-scaling
15:14	RW	0x0	sw_src_hscl_mode SRC horizontal scaling mode 00：no scaling 01: down-scaling 10: up-scaling
13:12	RW	0x0	sw_src_mir_mode SRC mirror mode 00: no mirror 01: x mirror 10: y mirror 11: x mirror + y mirror
11:10	RW	0x0	sw_src_rot_mode SRC rotation mode 00: 0 degree 01: 90 degree 10: 180 degree 11: 270 degree
9:8	RW	0x0	sw_src_csc_mode Source bitmap YUV2RGB conversion mode 00: bypass 01: BT.601-range0 10: BT.601-range1 11: BT.709-range0
7	RW	0x0	sw_cp_endian Source Color palette endian swap 0: big endian 1: little endian
6	RW	0x0	sw_src_uvswap Source Cb-Cr swap 0: CrCb 1: CbCr
5	RW	0x0	sw_src_alpha_swap Source bitmap data alpha swap 0: ABGR 1: BGRA
4	RW	0x0	sw_src_rbswap Source bitmap data RB swap 0: BGR 1: RGB

Bit	Attr	Reset Value	Description
3:0	RW	0x0	sw_src_fmt Source bitmap data format 0000: ABGR888 0001: XBGR888 0010: BGR packed 0100: RGB565 0101: ARGB1555 0110: ARGB4444 1000: YUV422SP 1001: YUV422P 1010: YUV420SP 1011: YUV420P 1100: 1BPP (color palette) 1101: 2BPP (color palette) 1110: 4BPP (color palette) 1111: 8BPP (color palette)

RGA2_SRC_BASE0
Address: Operational Base + offset (0x0108)
source image Y/RGB base address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_base0 source image Y/RGB base address

RGA2_SRC_BASE1
Address: Operational Base + offset (0x010c)
RGA source image Cb/Cbr base address register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_base1 source image Cb base address (YUV422/420-P) source image Cb/Cr base address (YU,V422/420-SP)

RGA2_SRC_BASE2
Address: Operational Base + offset (0x0110)
RGA source image Cr base address register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	sw_src_base2 source image Cr base address (YUV422/420-P)

RGA2_SRC_BASE3
Address: Operational Base + offset (0x0114)
RGA source image 1 base address register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	sw_src_base3 source image 1 RGB base address (source bitblt mode1)

RGA2_SRC_VIR_INFO
Address: Operational Base + offset (0x0118)
RGA source image virtual stride / RGA source image tile number

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved
25:16	RW	0x000	sw_mask_vir_stride mask image virtual stride (words)
15	RW	0x0	Reserved Reserved
14:0	RW	0x0000	sw_src_vir_stride src image virtual stride (words)

RGA2_SRC_ACT_INFO
Address: Operational Base + offset (0x011c)
RGA source image active width/height register

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved2 Reserved
28:16	RW	0x0000	sw_src_act_height source image active height
15:13	RW	0x0	Reserved1 Reserved
12:0	RW	0x0000	sw_src_act_width source image active width

RGA2_SRC_X_FACTOR
Address: Operational Base + offset (0x0120)
RGA source image horizontal scaling factor

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_src_hsp_factor Source image horizontal up-scaling factor =(DST_ACT_WIDTH/SRC_ACT_WIDTH) * 65536
15:0	RW	0x0000	sw_src_hsd_factor Source image horizontal down-scaling factor =(SRC_ACT_WIDTH/DST_ACT_WIDTH) * 65536

RGA2_SRC_Y_FACTOR
Address: Operational Base + offset (0x0124)
RGA source image vertical scaling factor

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_src_vsp_factor Source image vertical up-scaling factor (DST_ACT_HEIGHT/SRC_ACT_HEIGHT) * 65536
15:0	RW	0x0000	sw_src_vsd_factor Source image vertical down-scaling factor (SRC_ACT_HEIGHT/DST_ACT_HEIGHT) * 65536

RGA2_SRC_BG_COLOR
Address: Operational Base + offset (0x0128)
RGA source image background color

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_bg_color Source image background color ("0" bit color for mono expansion.)

RGA2_SRC_FG_COLOR
Address: Operational Base + offset (0x012c)
RGA source image foreground color

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_fg_color Source image foreground color Source image foreground color ("1" bit color for mono expansion.) Color fill color, Pan color

RGA2_SRC_TR_COLOR0
Address: Operational Base + offset (0x0130)
RGA source image transparency color min value

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_src_trans_amin source image transparency color A min value
23:16	RW	0x00	sw_src_trans_bmin source image transparency color B min value
15:8	RW	0x00	sw_src_trans_gmin source image transparency color G min value
7:0	RW	0x00	sw_src_trans_rmin source image transparency color R min value

RGA2_CP_GR_A
Address: Operational Base + offset (0x0130)
RGA source image transparency color min value

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_gradient_y_a Y gradient value of Alpha (signed 8.8)

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	sw_gradient_x_a X gradient value of Alpha (signed 8.8)

RGA2_SRC_TR_COLOR1
Address: Operational Base + offset (0x0134)
Register0000 Abstract

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_src_trans_amax source image transparency color A max value
23:16	RW	0x00	sw_src_trans_bmax source image transparency color B max value
15:8	RW	0x00	sw_src_trans_gmax source image transparency color G max value
7:0	RW	0x00	sw_src_trans_rmax source image transparency color R max value

RGA2_CP_GR_B
Address: Operational Base + offset (0x0134)
RGA source image transparency color max value

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_gradient_y_b Y gradient value of Blue (signed 8.8)
15:0	RW	0x0000	sw_gradient_x_b X gradient value of Blue (signed 8.8)

RGA2_DST_INFO
Address: Operational Base + offset (0x0138)
RGA destination format register

Bit	Attr	Reset Value	Description
31:19	RW	0x0000	Reserved Reserved
18	RW	0x0	sw_dst_csc_clip BGR2YUV Clip mode(from 0~255 clip to 36~235) 1: clip enable; 0: unclip
17:16	RW	0x0	sw_dst_csc_mode DST bitmap RGB2YUV conversion mode 00: Bypass 01: BT.601-range0 10: BT.601-range1 11: BT.709-range0

Bit	Attr	Reset Value	Description
15:14	RW	0x0	sw_dither_mode DST dither down bit mode 00: 888 to 666 01: 888 to 565 10: 888 to 555 11: 888 to 444
13	RW	0x0	sw_dither_down DST dither down enable 0:disable 1:enable
12	RW	0x0	sw_src1_dither_up DST/SRC1 dither up enable 0:disable 1:enable
11	RW	0x0	sw_src1_alpha_swap Source 1 bitmap data alpha swap 0: ABGR 1: BGRA
10	RW	0x0	sw_src1_rbswap Source 1 bitmap data RB swap 0: BGR 1: RGB
9:7	RW	0x0	sw_src1_fmt Source 1 bitmap data format 000: ABGR888 001: XBGR888 010: BGR packed 100: RGB565 101: ARGB1555 110: ARGB4444
6	RW	0x0	sw_dst_uvswap Destination Cb-Cr swap 0: CrCb 1: CbCr
5	RW	0x0	sw_dst_alpha_swap Destination bitmap data alpha swap 0: ABGR 1: BGRA
4	RW	0x0	sw_dst_rbswap Destination bitmap data RB swap 0: BGR 1: RGB

Bit	Attr	Reset Value	Description
3:0	RW	0x0	sw_dst_fmt Destination bitmap data format 0000: ABGR888 0001: XBGR888 0010: BGR packed 0100: RGB565 0101: ARGB1555 0110: ARGB4444 1000: YUV422SP 1001: YUV422P 1010: YUV420SP 1011: YUV420P If RGA has yuyv output format feature: 1100: YVYU422(U, LSB) 1101: YVYU420(U, LSB) 1110: VYUY422(Y, LSB) 1111: VYUY420(Y, LSB)

RGA2_DST_BASE0
Address: Operational Base + offset (0x013c)
RGA destination image base address 0 register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dst_base0 destination image Y/RGB base address

RGA2_DST_BASE1
Address: Operational Base + offset (0x0140)
RGA destination image base address 1 register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dst_base1 destination image Cb/CbCr base address

RGA2_DST_BASE2
Address: Operational Base + offset (0x0144)
RGA destination image base address 2 register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dst_base2 destination image Cr base address

RGA2_DST_VIR_INFO
Address: Operational Base + offset (0x0148)
RGA destination image virtual width/height register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved2 Reserved
27:16	RW	0x000	sw_src1_vir_stride source image 1 virtual stride (words)
15:12	RW	0x0	Reserved1 Reserved
11:0	RW	0x000	sw_dst_vir_stride destination image virtual stride(words)

RGA2_DST_ACT_INFO
Address: Operational Base + offset (0x014c)
RGA destination image active width/height register

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved2 Reserved
27:16	RW	0x000	sw_dst_act_height Destination image active height
15:12	RW	0x0	Reserved1 Reserved
11:0	RW	0x000	sw_dst_act_width Destination image active width

RGA2_ALPHA_CTRL0
Address: Operational Base + offset (0x0150)
Alpha control register 0

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved Reserved
20	RW	0x0	sw_mask_endian ROP4 mask endian swap 0: big endian 1: little endian
19:12	RW	0x00	sw_dst_global_alpha global alpha value of DST(Agd)
11:4	RW	0x00	sw_src_global_alpha global alpha value of SRC(Ags) fading value in fading mod
3:2	RW	0x0	sw_rop_mode ROP mode select 00: ROP 2 01: ROP 3 10: ROP 4

Bit	Attr	Reset Value	Description
1	RW	0x0	sw_alpha_rop_sel Alpha or ROP select 0: alpha 1: ROP
0	RW	0x0	sw_alpha_rop_e Alpha or ROP enable 0: disable 1: enable

RGA2_ALPHA_CTRL1
Address: Operational Base + offset (0x0154)
Register0000 Abstract

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved Reserved
29	RW	0x0	sw_src_alpha_m1 Src Transparent/opaque of alpha channel (As1') 0: As 1: 255-As
28	RW	0x0	sw_dst_alpha_m1 Dst Transparent/opaque of alpha channel (Ad1') 0: Ad 1: 255-Ad
27:26	RW	0x0	sw_src_blend_m1 Alpha src blend mode select of alpha channel (As1_'') 00: Ags 01: As1' 10: (As1'*Ags)>>8 11: reserved
25:24	RW	0x0	sw_dst_blend_m1 Alpha dst blend mode select of alpha channel(Ad1_'') 00: Agd 01: Ad1' 10: (Ad1'*Agd)>>8 11: reserved
23	RW	0x0	sw_src_alpha_cal_m1 Alpha src calculate mode of alpha channel(As1'') 0: As1''= As1_''+ (As1_''>>7) 1: As1''= As1 _''
22	RW	0x0	sw_dst_alpha_cal_m1 Alpha dst calculate mode of alpha channel(Ad1'') 0: Ad1''= Ad1_'' + (Ad1_''>>7) 1: Ad1''= Ad1_''

Bit	Attr	Reset Value	Description
21:19	RW	0x0	w_src_factor_m1 Src factore mode of alpha channel(Fs1) 000: 0 001: 256 010: Ad1'' 011: 256-Ad1'' 100: As1''
18:16	RW	0x0	sw_dst_factor_m1 Dst factore mode of alpha channel(Fd1) 000: 0 001: 256 010: As1'' 011: 256-As1'' 100: Ad1''
15	RW	0x0	sw_src_alpha_m0 Src Transparent/opaque of color channel (As0') 0: As 1: 255-As
14	RW	0x0	sw_dst_alpha_m0 Dst Transparent/opaque of color channel (Ad0') 0: Ad 1: 255-Ad
13:12	RW	0x0	sw_src_blend_m0 Alpha src blend mode select of color channel (As0_'') 00: Ags 01: As0' 10: (As0'*Ags)>>8 11: reserved
11:10	RW	0x0	sw_dst_blend_m0 Alpha dst blend mode select of color channel(Ad0_'') 00: Agd 01: Ad0' 10: (Ad0'*Agd)>>8 11: reserved
9	RW	0x0	sw_src_alpha_cal_m0 Alpha src calculate mode of color channel(As0'') 0: As0''= As0_''+ (As0_''>>7) 1: As0''= As0 _''
8	RW	0x0	sw_dst_alpha_cal_m0 Alpha dst calculate mode of color channel(Ad0'') 0: Ad0''= Ad0_'' + (Ad0_''>>7) 1: Ad0''= Ad0_''

Bit	Attr	Reset Value	Description
7:5	RW	0x0	sw_src_factor_m0 Src factore mode of color channel(Fs0) 000: 0 001: 256 010: Ad0'' 011: 256-Ad0'' 100: As0''
4:2	RW	0x0	sw_dst_factor_m0 Dst factore mode of color channel(Fd0) 000: 0 001: 256 010: As0'' 011: 256-As0'' 100: Ad0''
1	RW	0x0	sw_src_color_m0 SRC color select(Cs') 0: Cs 1: Cs * As0''
0	RW	0x0	sw_dst_color_m0 SRC color select(Cd') 0: Cd 1: Cd * Ad0''

RGA2_FADING_CTRL
Address: Operational Base + offset (0x0158)
Fading control register

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved Reserved
24	RW	0x0	sw_fading_en Fading enable
23:16	RW	0x00	sw_fading_offset_b Fading offset B value
15:8	RW	0x00	sw_fading_offset_g Fading offset G value (Pattern total number when pattern loading)
7:0	RW	0x00	sw_fading_offset_r Fading offset R value (Start point of pattern ram in pattern mode)

RGA2_PAT_CON
Address: Operational Base + offset (0x015c)
Pattern size/offset register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_pat_offset_y Pattern y offset
23:16	RW	0x00	sw_pat_offset_x Pattern x offset
15:8	RW	0x00	sw_pat_height Pattern height
7:0	RW	0x00	sw_pat_width Pattern width

RGA2_ROP_CON0
Address: Operational Base + offset (0x0160)
ROP code 0 control register

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved Reserved
24:0	RW	0x0000000	sw_rop3_code0 Rop3 code 0 control bits

RGA2_CP_GR_G
Address: Operational Base + offset (0x0160)
RGA color gradient fill step register (color fill mode)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_gradient_y_g Y gradient value of Green (signed 8.8)
15:0	RW	0x0000	sw_gradient_x_g X gradient value of Green (signed 8.8)

RGA2_ROP_CON1
Address: Operational Base + offset (0x0164)
ROP code 1 control register

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved Reserved
24:0	RW	0x0000000	sw_rop3_code1 Rop3 code 1 control bits

RGA2_CP_GR_R
Address: Operational Base + offset (0x0164)
RGA color gradient fill step register (color fill mode)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_gradient_y_r Y gradient value of Red(signed 8.8)
15:0	RW	0x0000	sw_gradient_x_r X gradient value of Red(signed 8.8)

RGA2_MASK_BASE
Address: Operational Base + offset (0x0168)
RGA mask base address register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_mask_base mask base address in ROP4 mode LUT/ pattern load base address

RGA2_MMU_CTRL1
Address: Operational Base + offset (0x016c)
RGA MMU control register 1

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	Reserved
13	RW	0x0	sw_els_mmu_flush RGA ELSE channel MMU TLB flush: Set 1 to this bit to flush MMU TLB, auto clear
12	RW	0x0	sw_els_mmu_en RGA ELSE channel MMU enable 0: disable 1: enable
11	RW	0x0	sw_dst_mmu_prefetch_dir 0:forward 1:backward
10	RW	0x0	sw_dst_mmu_prefetch_en 0:disable 1:enable
9	RW	0x0	sw_dst_mmu_flush RGA DST channel MMU TLB flush: Set 1 to this bit to flush MMU TLB, auto clear
8	RW	0x0	sw_dst_mmu_en RGA DST channel MMU enable 0: disable 1: enable
7	RW	0x0	sw_src1_mmu_prefetch_dir 0:forward 1:backward
6	RW	0x0	sw_src1_mmu_prefetch_en 0:disable 1:enable
5	RW	0x0	sw_src1_mmu_flush RGA SRC1 channel MMU TLB flush: Set 1 to this bit to flush MMU TLB, auto clear
4	RW	0x0	sw_src1_mmu_en RGA SRC1 channel MMU enable 0: disable 1: enable

Bit	Attr	Reset Value	Description
3	RW	0x0	sw_src_mmu_prefetch_dir 0:forward 1:backward
2	RW	0x0	sw_src_mmu_prefetch_en 0:disable 1:enable
1	RW	0x0	sw_src_mmu_flush RGA SRC channel MMU TLB flush: Set 1 to this bit to flush MMU TLB, auto clear
0	RW	0x0	sw_src_mmu_en RGA SRC channel MMU enable 0: disable 1: enable

RGA2_MMU_SRC_BASE
Address: Operational Base + offset (0x0170)
RGA source MMU TLB base address

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_mmu_src_base RGA source MMU TLB base address (128-bit)

RGA2_MMU_SRC1_BASE
Address: Operational Base + offset (0x0174)
RGA source1 MMU TLB base address

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_mmu_src1_base RGA source1 MMU TLB base address (128-bit)

RGA2_MMU_DST_BASE
Address: Operational Base + offset (0x0178)
RGA destination MMU TLB base address

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_mmu_dst_base RGA destination MMU TLB base address (128-bit)

RGA2_MMU_ELS_BASE
Address: Operational Base + offset (0x017c)
RGA ELSE MMU TLB base address

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_mmu_els_base RGA destination MMU TLB base address (128-bit)

2.5 Application Notes

2.5.1 Register Partition

There are two types of register in RGA. The first 8 registers (0x0 - 0x1C) are general registers for system configuration including command mode, command parameter, RGA status, general interrupts. The other registers (from 0x100) are command registers for command codes.

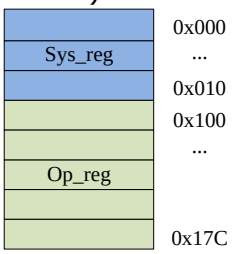


Fig. 2-8 RGA software main register-region

2.5.2 Command Modes

RGA has two command modes: slave mode and master mode. In salve mode (RGA_SYS_CTRL[1] = 1'b0), 2D graphic command only could be run one by one. CPU set all the command registers in RGA and then start RGA running by setting RGA_SYS_CTRL[0] to '1'. In master mode (RGA_SYS_CTRL[1] = 1'b1), 2D graphic commands could be run sequentially. After setting command's number to RGA_CMD_CTRL[12:3], writing '1' to RGA_CMD_CTRL[0] will start the command fetch, then Internal command DMA fetch commands from external command line.
Command line is a collection of several command codes with continuous address. At the first start, the command start address (RGA_CMD_ADDR) and command number (RGA_CMD_CTRL[12:3]) should be set, then write '1' to cmd_line_st (RGA_CMD_CTRL[0]) to start the command line fetch. Incremental command is supported by setting cmd_incr_num (RGA_CMD_CTRL[12:3]) and cmd_incr_valid (RGA_CMD_CTRL[1]=1'b1)

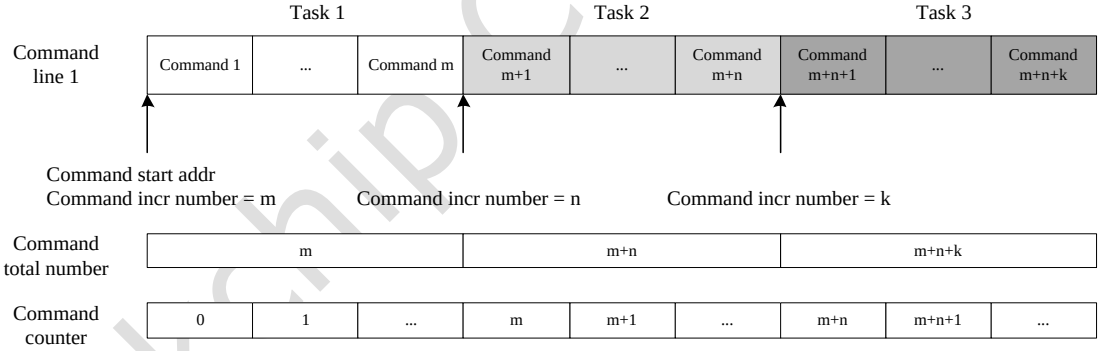


Fig. 2-9 RGA command line and command counter

2.5.3 Command Sync

In slave command mode, command sync is controlled by CPU.
In master command mode, user can enable the current_cmd_int (sw_intr_cf), command by command to generate a interrupt at the end point of target command operation.

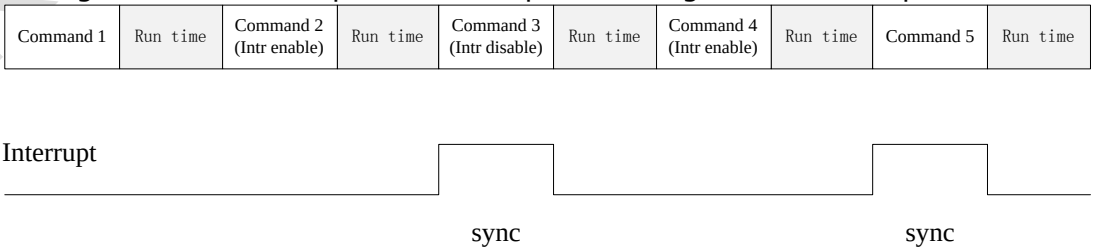


Fig. 2-10 RGA command sync generation

2.5.4 ColorPalette Application Notes

1. Palette/LUT Load into special RAM in ELS_BUF_CTRL;

2. ColorPalette/Pattern interval operations no need to initial LUT/pattern ram if LUT/pattern content no update;

2.5.5 Some special application constraint

1. The algorithm of vertical scale up: must select bicubic algorithm when source picture is smaller or equal to 2k and must select bilinear when bigger than 2k

2. The effects that The output's definition is near 2k or 4k may not very well when at the scenario that the vertical side is scale up and the horizontal is scale down within range of 2%(such as:2048x32→2008x64)

3. At the scenario A+B->C, the size among the A B C has some constraint :
   A's size must be equal to C. C's size must equal to B when A+C is no rotation. C's rotation (90degree)size must equal to B1 when A+C is rotation 90 degree .

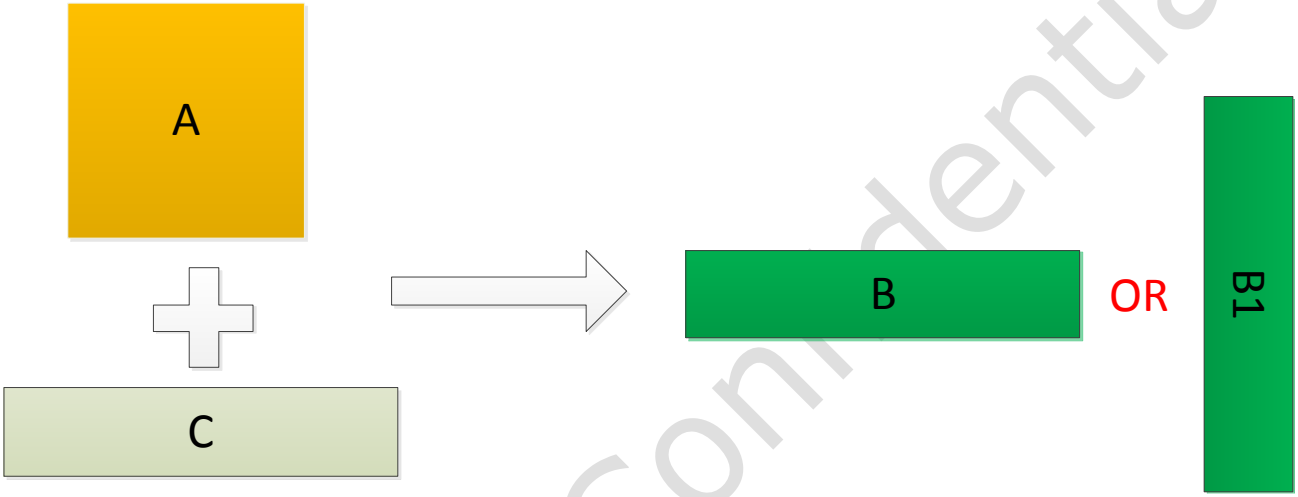


Fig. 2-11 the size constraint among A B C

4. YUV420/422-8bit virtual stride need 8byte align，xoff/yoff need 2byte algin；

5. YUV420/422-10bit virtual stride need 16byte align，not support xoff/yoff；

6. Vertical scale down or not && Horizontal bi-cubic scale up src0 width<=2048；
   Vertical scale up && Horizontal bi-cubic scale up src0 width<=1928；

7. Vertical scale down or not && Horizontal bilinear scale up src0 width<=4096；
   Vertical scale up && Horizontal bilinear scale up src0 width<=3856；

Chapter 3 Video Output Processor (VOP)

3.1 Overview

VOP is the display interface from memory frame buffer to display device. VOP is connected to an AHB bus through an AHB slave and AXI bus through an AXI master. The register setting is configured through the AHB slave interface and the display frame data is read through the AXI master interface. There are two VOP in the chip, respectively VOP_BIG and VOP_LIT.

3.1.1 Features

The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

The features of VOP_BIG are shown as follow:

- Display interface
  - HDMI interface
    - Support 480p/480i/576p/576i/720p/1080p/1080i/4k
    - Support RGB/YUV420(up to 10bit) format
  - Parallel RGB LCD Interface
    - RGB888,RGB666,RGB565
  - DP interface
    - Support progressive/interlace
    - Support RGB/YUV420/YUV422/YUV444(up to 10bit) format
  - MIPI interface
    - MIPI DCS command mode
    - Dual-MIPI
  - EDP interface
  - Max resolution
    - Max input resolution：4096x2304
    - Max output resolution：4096x2160
  - Scaning timing 8192x4096
  - Support configurable polarity of DCLK/HSYNC/VSYNC/DEN
- Display process
  - CABC
  - BCSH,10bit
    - Brightness,Contrast,Saturation,Hue adjustment
    - YUV-10bit，RGB-10bit
  - Support display data swap
    - BG swap, RB swap, RG swap, dummy swap.
  - Support YUV2RGB transition modes:
    - 10bit-YUV: bt601-f / bt709-l/bt601-l/bt2020
  - Support RGB2YUV transition modes:
    - 10bit-RGB: bt601-f/bt709-l/bt601-l/bt2020
  - Support YUV2YUV
  - GAMMA
    - Dual-GAMMA
  - blank display
  - black display
  - standby mode
  - X-MIRROR,Y-MIRROR for win0/win1/win2/win3/hwc
  - scale down for TV overscan
    - after overlay
    - arbitrary non-integer scaling ratio
    - horizontal scale down using bilinear, 0.5~1.0

- vertical scale down using bilinear, 0.5~1.0

- Layer process
  - ① Background layer
    - programmable 30 bit color，10 bit per-channel
  - ② Afbcd
    - format:ARGB8888/RGB888/RGB565
    - Support block split
    - win_sel(win0/win1/win2/win3)
    - max_outstanding_num(max 32)
  - ③ Win0/Win1 layer
    - Support data format
      - RGB888, ARGB888, RGB565,
      - YCbCr420SP, YCbCr422SP,CbCr444SP,YUYV420,YUYV422, YVYU420,YVYU422
      - RGB(8bit),YUV(8bit/10bit),YVYU/YUYV(8bit)
    - YUV clip
      - Y-8bit: 16~235;UV-8bit: 16~240
      - Y-10bit: 64~940;UV-10bit: 64~960
    - CSC
      - RGB2YUV
      - YUV2RGB
      - RGB2RGB
      - YUV2YUV
    - Support max input resolution 4096x8192
    - Support max output resolution 4096x2160
    - Support virtual display
    - Support 1/8 to 8 scaling-down and scaling-up engine
      - scale up using bicubic and bilinear
      - scale down using bilinear and average
      - per-pix alpha + scale
    - Support data swap
      - RGB/BPP: rb_swap
      - YUV: mid_swap,uv_swap
    - transparency color key, prior to alpha blending and fading
    - Support fading/alpha blending
    - Support interlace output
  - Win2/Win3 layer
    - Support data format
      - RGB888, ARGB888, RGB565
      - 8BPP
      - little endian and big endian for BPP
      - BYPASS and LUT mode(32bit LUT，8bit AA+8bit-RGB) for BPP
    - CSC
      - RGB2YUV
      - RGB2RGB
    - 4 display regions
      - only one region at one scanning line
    - Support data swap
      - RGB/BPP:rb_swap
    - Support transparency color key, prior to alpha blending and fading
    - Support fading/alpha blending
    - Support interlace output
  - ④ Hardware Cursor layer
    - Support data format
      - RGB888, ARGB888, RGB565
      - 8BPP
      - little endian and big endian for BPP

- ✧ BYPASS and LUT mode(32bit LUT，8bit AA+8bit-RGB)for BPP
- ◆ CSC
  - ✧ RGB2YUV
- ◆ Support four hwc size: 32x32,64x64,96x96,128x128
- ◆ Support 2 color modes: normal and reversed color
- ◆ Support fading/alpha blending
- ◆ Support displaying out of panel,right or bottom
- ◆ Support interlace output

■ Support p2i

⑤ Overlay

- ◆ support RGB and YUV domain overlay
- ◆ Support 6 layers,background/win0/win1/win2/win3/hwc
- ◆ Win0/Win1/Win2/Win3 overlay position exchangeable
- ◆ Alpha blending
  - ✧ Support multi alpha blending modes
  - ✧ Support pre-multiplied alpha
  - ✧ Support global alpha and per_pix alpha
  - ✧ Support 256 level alpha
  - ✧ Layer0/layer1/layer2/layer3/hwc support alpha

- Write back
  - ■ Support format
    - ◆ RGB565(8bit),RGB888P(8bit)
    - ◆ YUV420(8bit)
  - ■ Support scale
    - ◆ horizontal scale down using bilinear, 0.25~1.0
    - ◆ vertical throw odd/even line
- Bus interface
  - ■ Support AMBA 2.0 AHB slave interface for accessing internal registers and LUT memories，32bit data bus width
  - ■ Support AMBA 3.0 AXI master read interface for loading frame data
    - ◆ 128bit data bus width
  - ■ Support MMU
  - ■ Support two transfer modes
    - ◆ auto outstanding transfer
    - ◆ configuruable outstanding transfer(gather transfer)
  - ■ Support QOS request for higher bus priority for win2/win3
  - ■ Support NOC hurry for higher bus prioirity for win0/win1
  - ■ Support DMA stop mode
  - ■ Win AXI read ID configurable
  - ■ Max read outstanding number
    - ◆ 32 when MMU disable
    - ◆ 31 when MMU enable
- Interrupt
  - ■ One combined interrupt
    - ◆ high active
    - ◆ raw status readable
    - ◆ combinational with interrupt sources

The features of VOP_LIT are shown as follow:

- Display interface
  - ■ HDMI interface
    - ◆ Support 480p/480i/576p/576i/720p/1080p/1080i
    - ◆ Support RGB format
  - ■ Parallel RGB LCD Interface
    - ◆ RGB888,RGB666,RGB565
  - ■ DP interface
    - ◆ Support progressive/interlace

- Support RGB/YUV420/YUV422/YUV444 format
- MIPI interface
  - MIPI DCS command mode
  - Dual-MIPI
- EDP interface
- Max resolution
  - Max input resolution：4096x2304
  - Max output resolution：2560x1600
- Scaning timing 8192x4096
- Support configurable polarity of DCLK/HSYNC/VSYNC/DEN
- Only support to 8bit output

- Display process
  - CABC
  - BCSH,10bit
    - Brightness,Contrast,Saturation,Hue adjustment
    - YUV-8bit，RGB-8bit
  - Support display data swap
    - BG swap, RB swap, RG swap, dummy swap.
  - Support YUV2RGB transition modes:
    - 10bit-YUV: bt601-f/bt709-l/bt601-l
  - Support RGB2YUV transition modes:
    - 10bit-RGB: bt601-f/bt709-l
  - Support YUV2YUV
  - GAMMA
    - Dual-GAMMA
  - blank display
  - black display
  - standby mode
  - X-MIRROR,Y-MIRROR for win0/win2/hwc
  - scale down for TV overscan
    - after overlay
    - arbitrary non-integer scaling ratio
    - horizontal scale down using bilinear, 0.5~1.0
    - vertical scale down using bilinear, 0.5~1.0
- Layer process
  - ⑥ Background layer
    - programmable 30 bit color
  - ⑦ Win0 layer
    - Support data format
      - RGB888, ARGB888, RGB565,
      - YCbCr420SP, YCbCr422SP,CbCr444SP,YUYV420,YUYV422, YVYU420,YVYU422
      - RGB(8bit),YUV(8bit),YVYU/YUYV(8bit)
    - YUV clip
      - Y-8bit: 16~235;UV-8bit: 16~240
    - CSC
      - RGB2YUV
      - YUV2RGB
      - RGB2RGB
      - YUV2YUV
    - Support max input resolution 4096x8192
    - Support max output resolution 2560x1600
    - Support virtual display
    - Support 1/8 to 8 scaling-down and scaling-up engine
      - scale up using bicubic and bilinear

- ✧ scale down using bilinear and average
- ✧ per-pix alpha + scale
- ◆ Support data swap
  - ✧ RGB/BPP: rb_swap
  - ✧ YUV: mid_swap,uv_swap
- ◆ transparency color key,prior to alpha blending and fading
- ◆ Support fading/alpha blending
- ◆ Support interlace output

■ Win2 layer
- ◆ Support data format
  - ✧ RGB888, ARGB888, RGB565
  - ✧ 8BPP
  - ✧ little endian and big endian for BPP
  - ✧ BYPASS and LUT mode(32bit LUT，8bit AA+8bit-RGB) for BPP
- ◆ CSC
  - ✧ RGB2YUV
  - ✧ RGB2RGB
- ◆ 4 display regions
  - ✧ only one region at one scanning line
- ◆ Support data swap
  - ✧ RGB/BPP:rb_swap
- ◆ Support transparency color key,prior to alpha blending and fading
- ◆ Support fading/alpha blending
- ◆ Support interlace output

⑧ Hardware Cursor layer
- ◆ Support data format
  - ✧ RGB888, ARGB888, RGB565
  - ✧ 8BPP
  - ✧ little endian and big endian for BPP
  - ✧ BYPASS and LUT mode(32bit LUT，8bit AA+8bit-RGB)for BPP
- ◆ CSC
  - ✧ RGB2YUV
- ◆ Support four hwc size: 32x32,64x64,96x96,128x128
- ◆ Support 2 color modes: normal and reversed color
- ◆ Support fading/alpha blending
- ◆ Support displaying out of panel,right or bottom
- ◆ Support NORMAL color and REVERSE color mode
- ◆ Support interlace output

■ Support p2i
- ◆ Support display field polarity

⑨ Overlay
- ◆ support RGB and YUV domain overlay
- ◆ Support 6 layers,background/win0/win2/hwc
- ◆ Win0/Win2 overlay position exchangeable
- ◆ Alpha blending
  - ✧ Support multi alpha blending modes
  - ✧ Support pre-multiplied alpha
  - ✧ Support global alpha and per_pix alpha
  - ✧ Support 256 level alpha
  - ✧ Layer0/layer2/hwc support alpha

● Bus interface

■ Support AMBA 2.0 AHB slave interface for accessing internal registers and LUT memories，32bit data bus width

■ Support AMBA 3.0 AXI master read interface for loading frame data
- ◆ 128bit data bus width

■ Support MMU

■ Support two transfer modes

- auto outstanding transfer
- configuruable outstanding transfer(gather transfer)

- Support QOS request for higher bus priority for win2
- Support NOC hurry for higher bus prioirity for win0
- Support DMA stop mode
- Win AXI read ID configurable
- Max read outstanding number
  - 32 when MMU disable
  - 31 when MMU enable

- Interrupt
  - One combined interrupt
    - high active
    - raw status readable
    - combinational with interrupt sources

3.2 Block Diagram

The architecture is shown in the following figure .

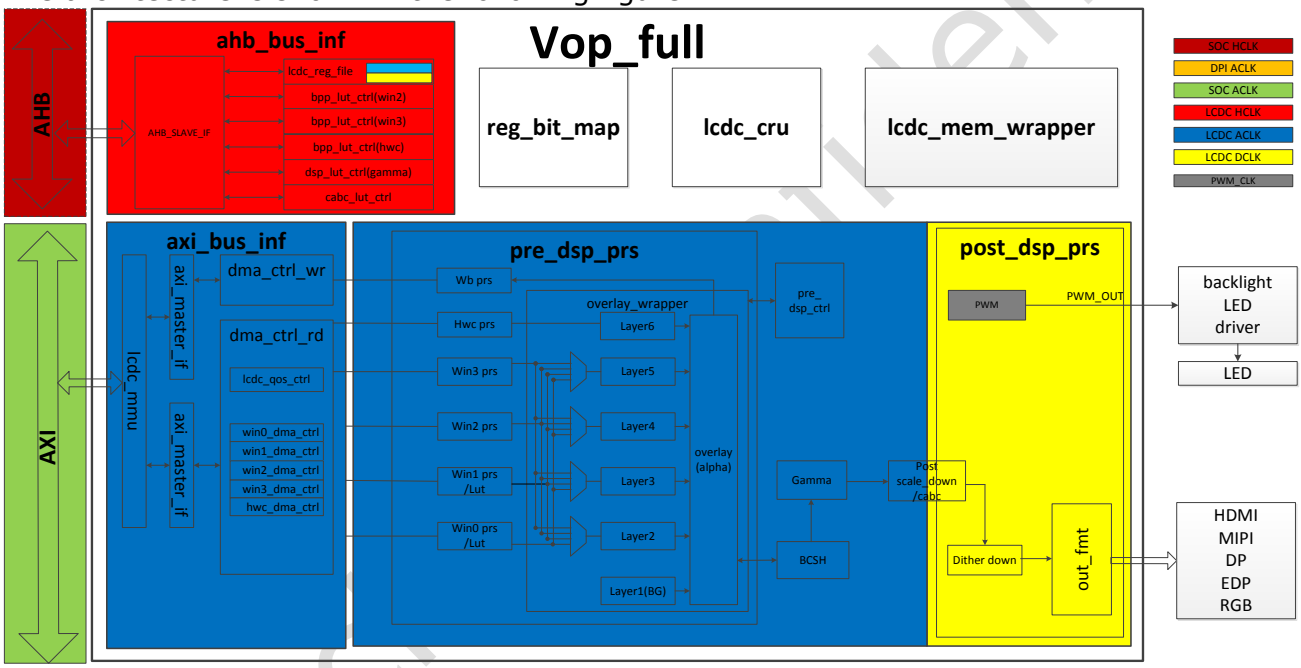


Fig. 3-1 VOP_BIG Block Diagram

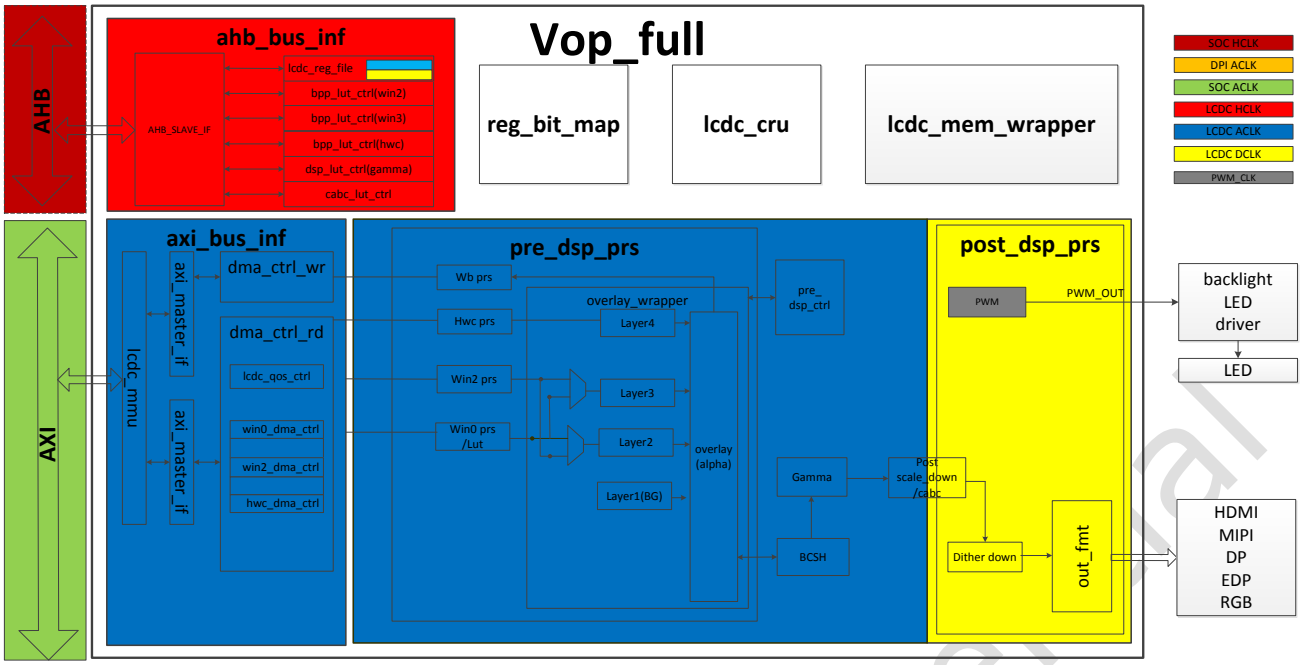


Fig. 3-2 VOP_LIT Block Diagram

3.3 Function Description

3.3.1 Pixel format

1.RGB

RGB888

31–24	23–16	15–8	7–0
B1	R0	G0	B0
G2	B2	R1	G1
R3	G3	B3	R2

ARGB888

31–24	23–16	15–8	7–0
A	R	G	B

RGB565

31–27	26–21	20–16	15–11	10–5	4–0
R1	G1	B1	R0	G0	B0

Fig. 3-2 RGB data format

2.YCbCr(8bit)

YCbCr just support SP format,YCbCr-8bit need 32bit align.

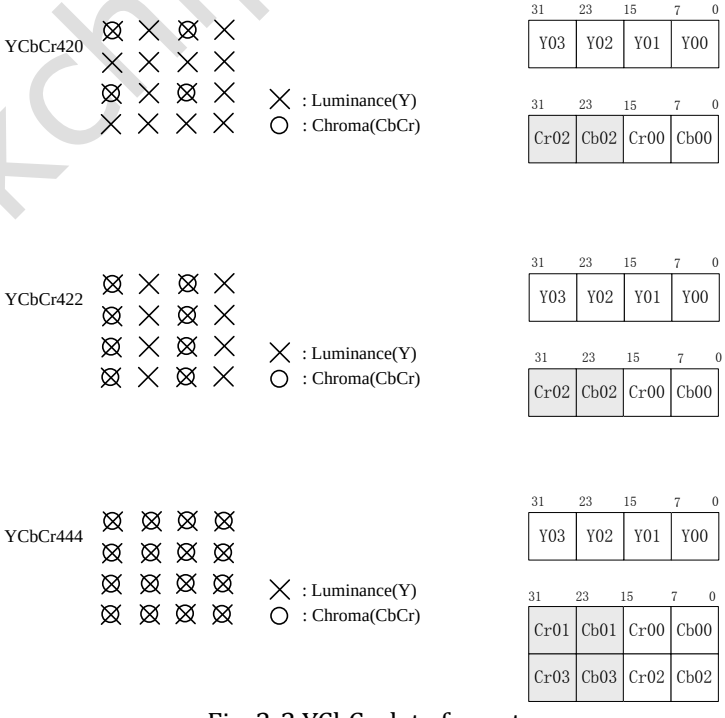


Fig. 3-3 YCbCr data format

2.YCbCr(10bit)

YCbCr-10bit is the same as YCbCr-8bit except it is 640bit align(64 pixels align).

3.BPP

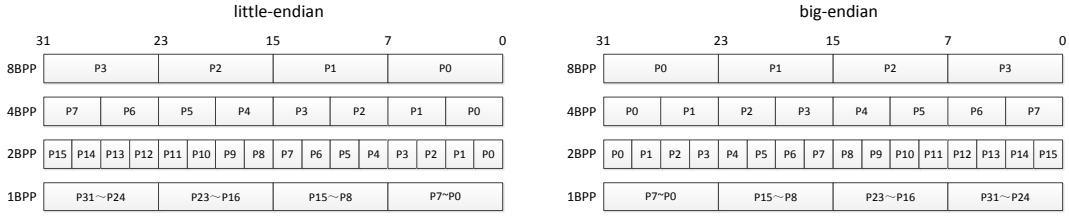


Fig. 3-4 BPP little/big endian data format

3.3.2 Pixel Data Path

There are only one data input path for VOP to get display layers' pixel data: internal DMA.

1.Internal DMA

Internal DMA can fetch the pixel data through AXI bus from system memory (DDR) for all the display layers. Data fetching is driven by display output requirement.

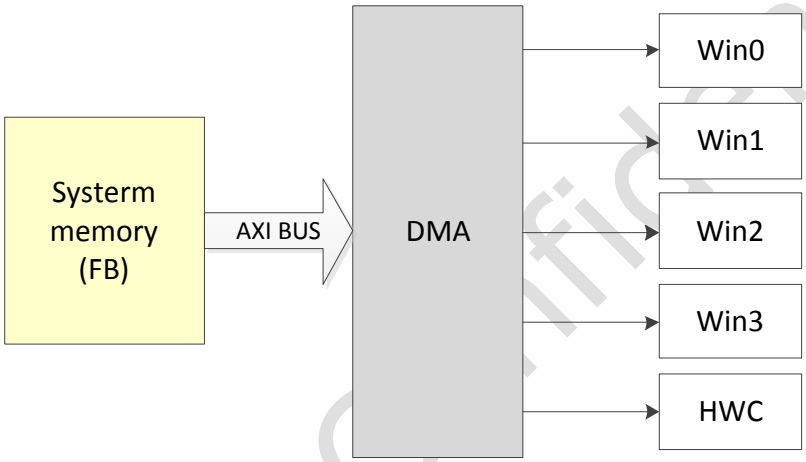


Fig. 3-5 VOP Internal DMA

3.3.3 Win Scaling

The scaling operation is the image resizing process by scaling-up or scaling-down the source image from active window size to display window size for displaying on LCD panel or TV set. Horizontal scaling and vertical scaling are realized independently.

1.Scaling factor

(1)scale down or scale up using bilinear
Factor = ((src*2-3)<<11)/(dst-1);
(2)scale up using bicubic
Factor = ((src*2-3)<<15)/(dst-1);
(3)scale down using average
Factor = (dst<<17)/(src*2-1);

2.win scale line buffer mode

For YUV422/YUV420,
(1)LB_YUV_4096X5
If horizontal scale down and dsp_width is greater than 2560 or if horizontal scale up and act_width is greater than 2560,please config win_lb_mode as LB_YUV_4096X5;
(2)LB_YUV_2560X8
If horizontal scale down and dsp_width is less or equal than 2560 or if horizontal scale up and act_width is less or equal than 2560,please config win_lb_mode as LB_YUV_4096X5;
For YUV444/RGB,
(1)LB_RGB_4096X2
If horizontal scale down and dsp_width is greater than 2560 or if horizontal scale up and act_width is greater than 2560,please config win_lb_mode as LB_YUV_4096X2;

This mode does not support vertical scale.
(2)LB_RGB_2560X4
horizontal scale down and dsp_width is greater than 1920 or if horizontal scale up and act_width is greater than 1920,please config win_lb_mode as LB_RGB_2560X4;
This mode only support bilinear for vertical scale up.
(3)LB_RGB_1920X5
horizontal scale down and dsp_width is greater than 1280 or if horizontal scale up and act_width is greater than 1280,please config win_lb_mode as LB_RGB_1920X5;
(4)LB_RGB_1280X8
horizontal scale down and dsp_width is less or equal than 2560 or if horizontal scale up and act_width is less or equal than 2560,please config win_lb_mode as LB_RGB_1280X8;

3.3.4 P2I

It is necessary to display a non-interlaced video signal on an interlaced display panel (such as TV set). Thus "progressive-to-interlaced conversion" is required (P2I).
When interlaced is required, no matter even field or odd field, we get the whole image from bus. After overlay, we discard the odd lines when even field (even lines when odd field). This method can be better.

3.3.5 Virtual display

When in virtual display, the active image is part of the virtual (original) image in frame buffer memory.
The virtual width is indicated by setting VIR_STRIDE for different data format. Note that RGB/BPP has one stride (yrgb_vir_stride), YCbCr has two virtual stride (yrgb_vir_stride and cbcr_vir_stride).
For RGB-8bit and YUV-8bit，the stride should be multiples of word (32-bit), with dummy bytes in the end of virtual line if the original width is not 32-bit aligned.

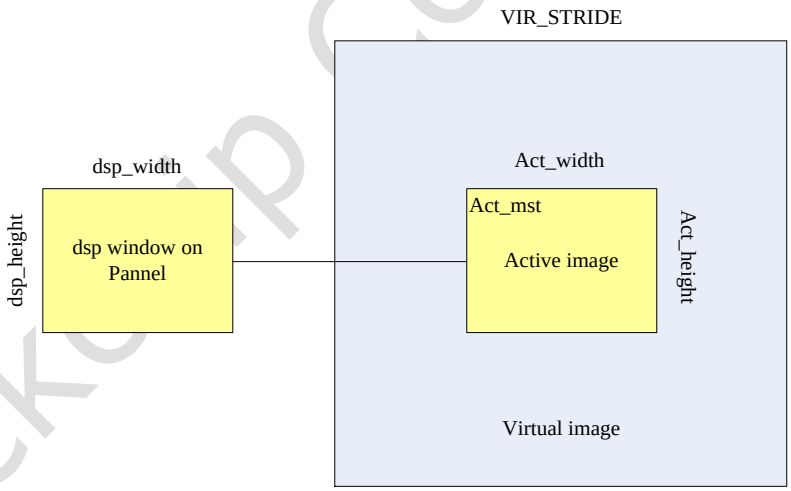


Fig. 3-6 Virtual display

3.3.6 MIRROR display

Mirror display is necessary for the panel with mirror timing interface. There are two types of mirror mode: horizontal mirror(X-mirror) and vertical mirror(Y-mirror).
Win0/1 support X-mirror and Y-mirror;
VOP support X-mirror and Y-mirror after overlay.
The default display order is from left to right(L2R) in horizontal direction and from top to bottom(T2B) in vertical direction. However, when X-Mirror is enable, the horizontal display order is from right to left(R2L); when Y-MIRROR is enable, the vertical display order is from bottom to top(B2T).

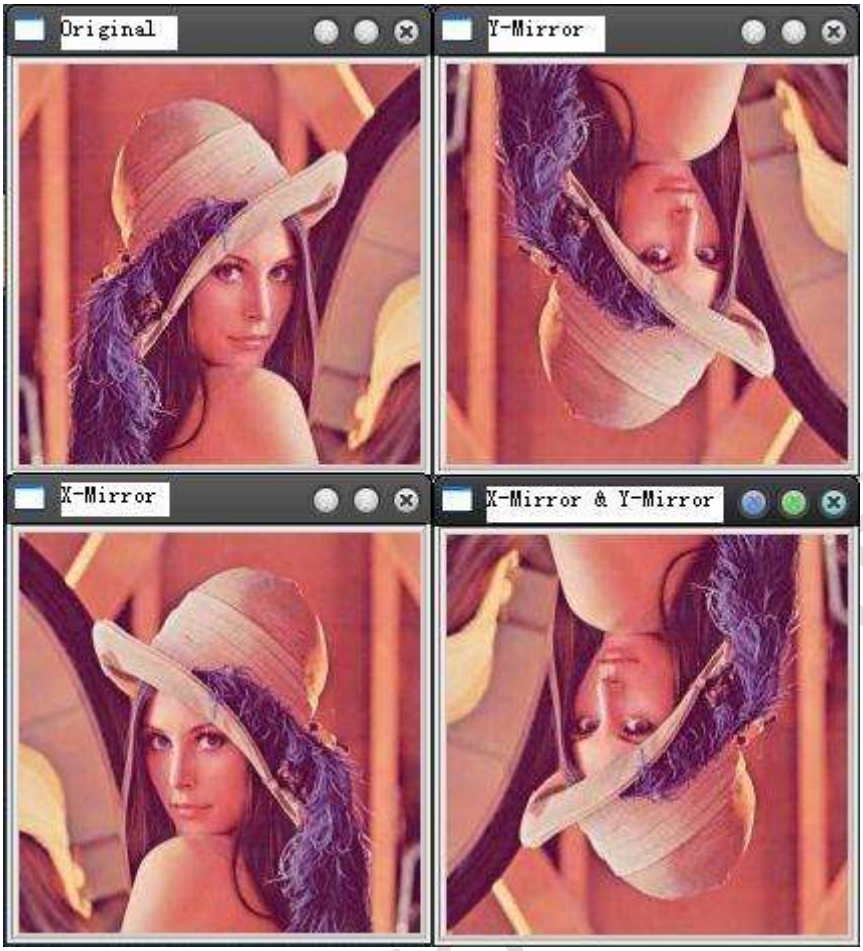


Fig. 3-7 X-Mirror and Y-Mirror

3.3.7 Display process

1. Overlay display

There are totally 6 layers for overlay display: Background, layer0, layer1, layer2, layer3 and hardware cursor layer(HWC).
Background is a programmable solid color layer, which is always in the bottom of the display screen.
HWC is always on the top of the display screen.

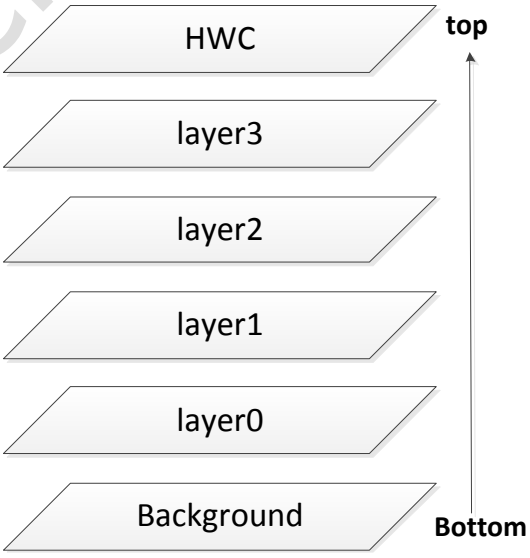


Fig. 3-8 overlay

Following figure is an example of overlay display for win0,win1 and hwc.

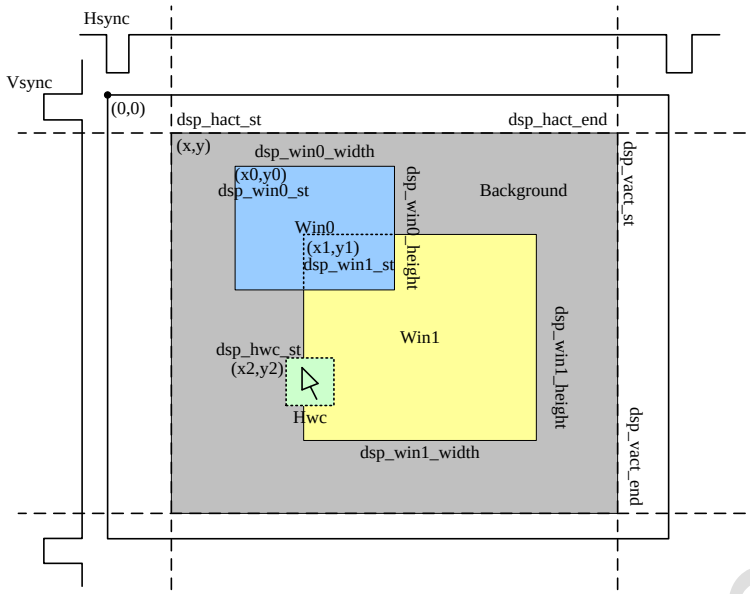


Fig. 3-9 overlay timing

2. Post scale down

Post scale down after overlay is supported to fix overscan ,that draws the borders of the image beyond the normally visiable area on the screen.

The scale ratio of post scale down is 0.5~1.

Post timing setting

The post scale parameter ,such as,post_dsp_hact_st,post_dsp_hact_end, post_dsp_vact_st,post_dsp_vact_end can be configured.

When post scaling equal "1" ,the post scaler parameter are the same as dsp timing parameter.

eg:

post_dsp_hact_st = dsp_hact_st

post_dsp_hact_end = dap_hact_end

post_dsp_vact_st = dsp_vact_st

post_dsp_vact_end = dsp_vact_end

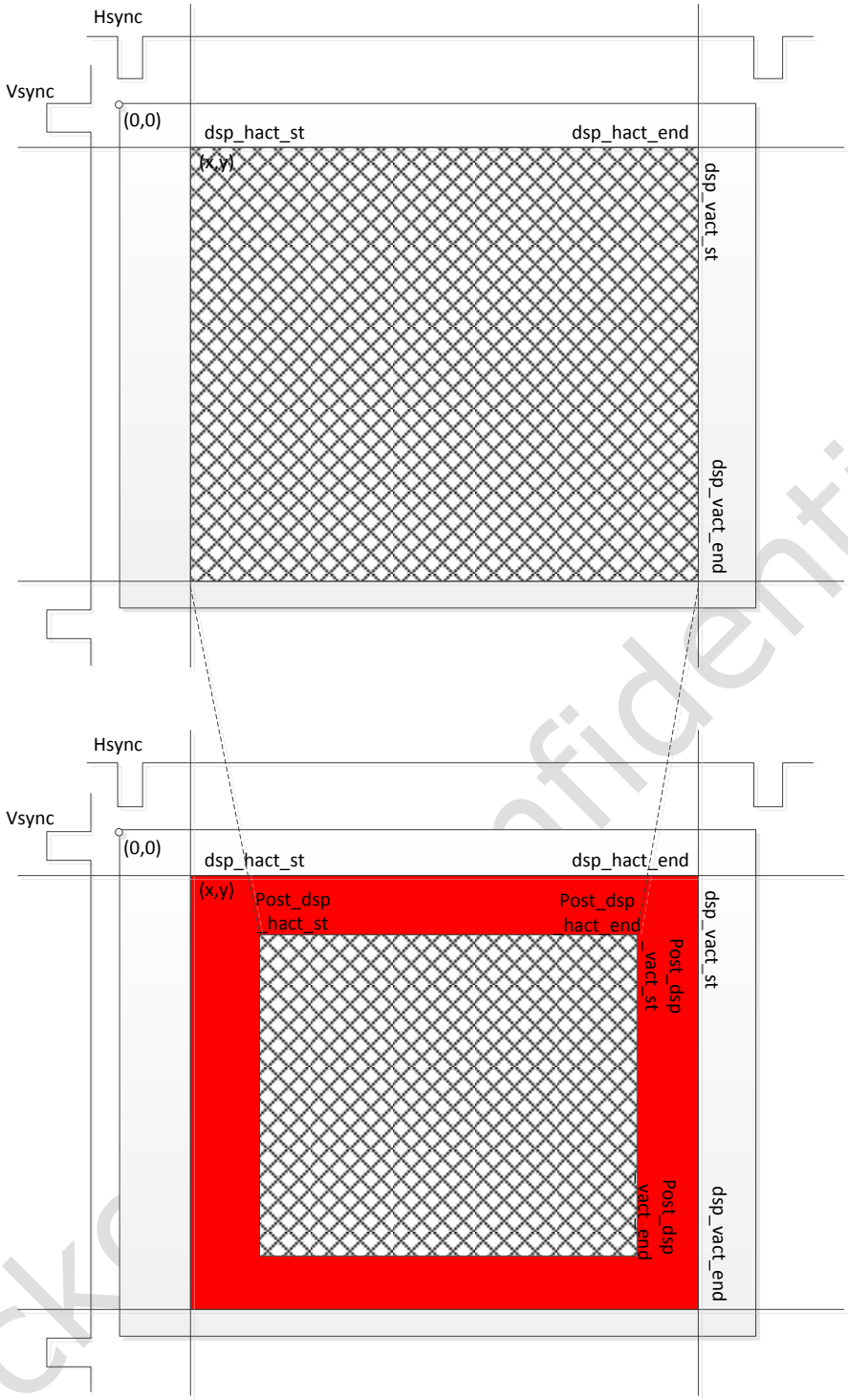


Fig. 3-10 post scaling timing

Post scale down factor

For horizontal scale down,factor = ((src_width*2-3)<<11)/(dst_width-1).
For vertical scale down,factor = ((src_width*2-3)<<11)/(dst_width-1).

3. Transparency color key

The transparency color key value defines the pixel treated as transparent pixel. The pixel whose value is equal to the color key value could not be visible on the screen, instead of the pixel in the under layer or solid background color.
There are two transparency color key for win0 layer and win1 layer respectively. When color key is enable, the transparency process is done after scaling but before YUV2RGB color space converter.
Moreover, transparency color key is just available for non-scaling mode.

Following figure is an example of transparency color key for win0 and win1.

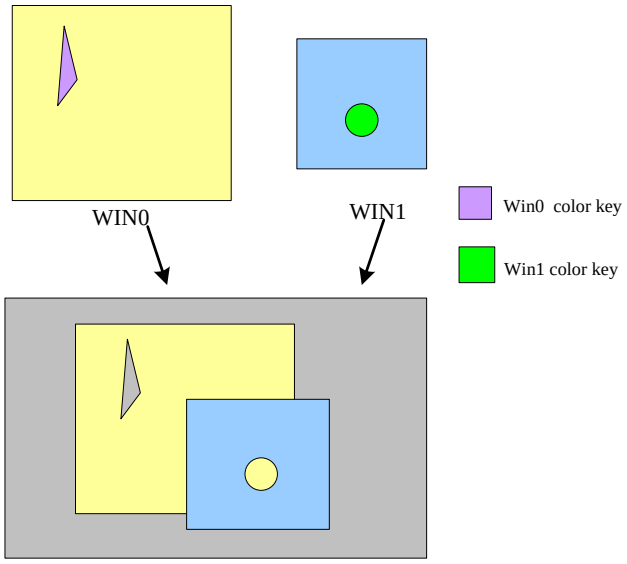


Fig. 3-11 Transparency Color Key

4. Replication(dither up)

If the size of panel data bus is lager than the size of source pixel data,i.e, the source input format is RGB565 and display output format is RGB888, you could do bit replication by replicating MSBs to LSBs if replication is enable (VOP_DSP_CTRL0[9]=1) or filling with "0" to LSBs if replication is disable (VOP_DSP_CTRL0[9]=0).

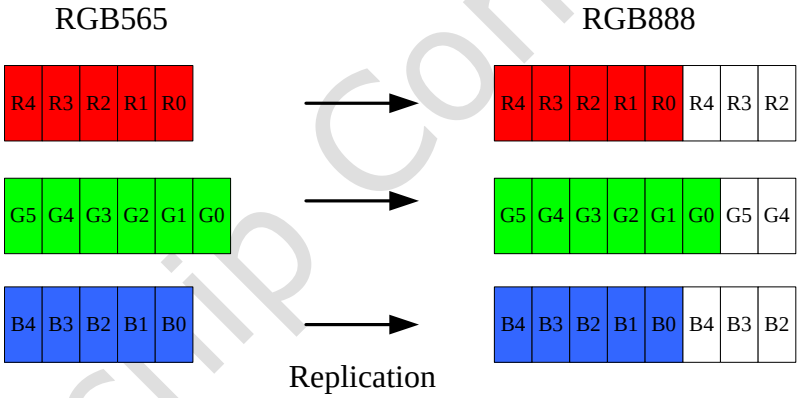


Fig. 3-12 Dither Up

5. Alpha blending

There are 12 alpha blending mode between two overlay layers for layer0/layer1/layer2/hwc. Layer0 support basic alpha blending with background.VOP supports overlay on RGB or YUV domain.

When in per-pixel mode, the alpha value for every pixel is following with the pixel data. i.e, aRGB, and can be scaled like RGB data. Therefore it is just suitable for win0/win1/hwc layer with ARGB data format.

The alpha blending architechture is shown as follows.

Table 3-1 alpha blending mode settings

Blending Mode	Cs’	Fs	Cd’	Fd
AA_USER_DEFINED	X	User defined	Cd	User defined
AA_CLEAR	X	0	Cd	0
AA_SRC	X	0	Cd	1
AA_DST	X	1	Cd	1
AA_SRC_OVER	Cs	1	Cd	1-As’’
AA_DST_OVER	Cs	1-As’’	Cd	1
AA_SRC_IN	Cs	As’’	Cd	0

AA_DST_IN	X	0	Cd	As''
AA_SRC_OUT	Cs	1-As''	Cd	0
AA_DST_OUT	X	0	Cd	1-As''
AA_SRC_ATOP	Cs	As''	Cd	1-As''
AA_DST_ATOP	Cs	1-As''	Cd	As''
AA_XOR	Cs	1-As''	Cd	1-As''
AA_SRC_OVER_GLOBAL	Cs*As''	Ags''	Cd	1-As''

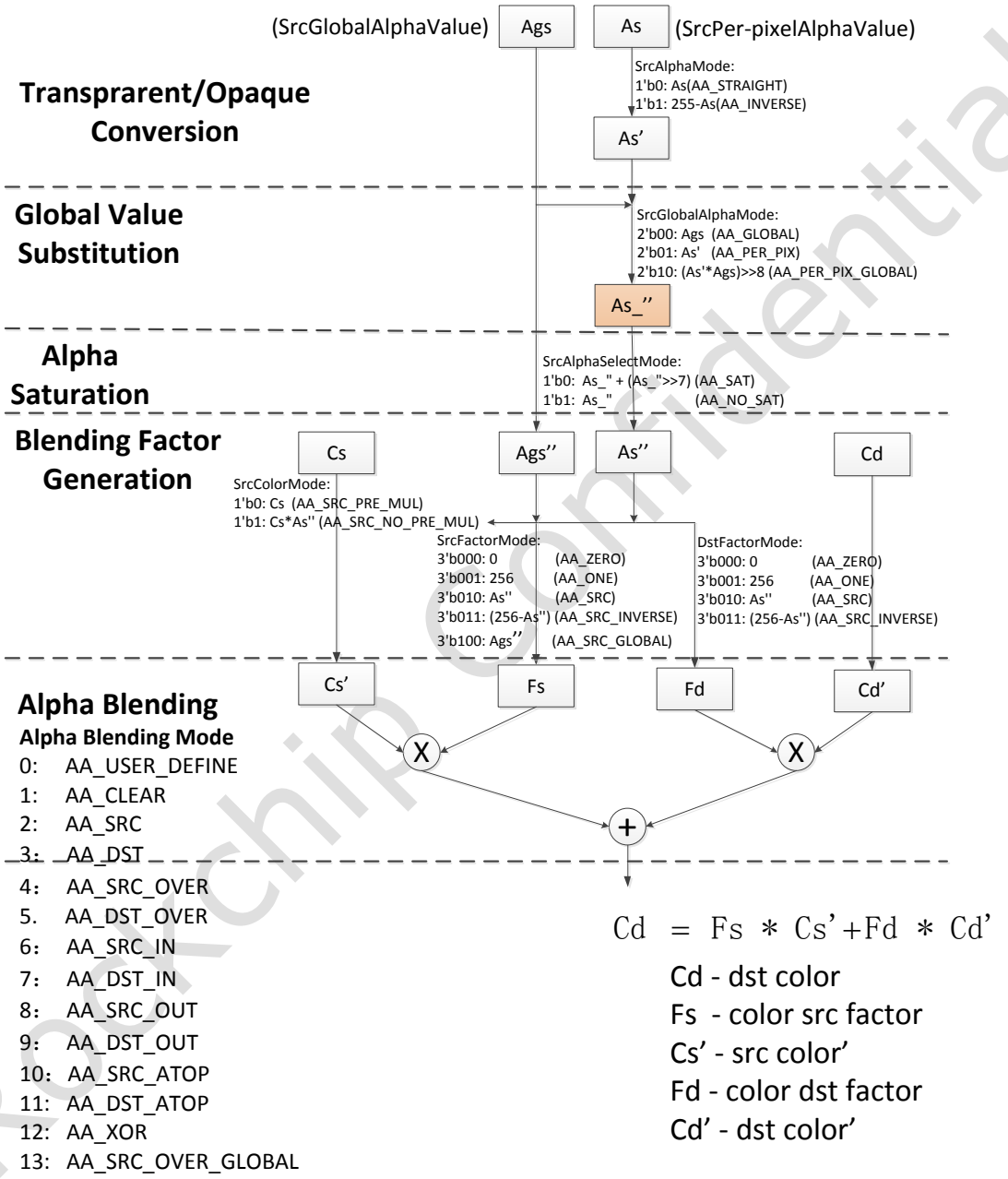


Fig. 3-13 alpha configuration flow

Pseudo Code:

```
switch(alpha_config->alpha_blending_mode)
{
    case AA_USER_DEFINE:
    break;
    case AA_CLEAR:
    alpha_config->src_factor_mode=AA_ZERO;
    alpha_config->dst_factor_mode=AA_ZERO;
    break;
```

```
case AA_SRC:
alpha_config->src_factor_mode=AA_ONE;
alpha_config->dst_factor_mode=AA_ZERO;
break;
case AA_DST:
alpha_config->src_factor_mode=AA_ZERO;
alpha_config->dst_factor_mode=AA_ONE;
break;
case AA_SRC_OVER:
alpha_config->src_color_mode=AA_SRC_PRE_MUL;
alpha_config->src_factor_mode=AA_ONE;
alpha_config->dst_factor_mode=AA_SRC_INVERSE;
break;
case AA_DST_OVER:
alpha_config->src_color_mode=AA_SRC_PRE_MUL;
alpha_config->src_factor_mode=AA_SRC_INVERSE;
alpha_config->dst_factor_mode=AA_ONE;
break;
case AA_SRC_IN:
alpha_config->src_color_mode=AA_SRC_PRE_MUL;
alpha_config->src_factor_mode=AA_SRC;
alpha_config->dst_factor_mode=AA_ZERO;
break;
case AA_DST_IN:
alpha_config->src_factor_mode=AA_ZERO;
alpha_config->dst_factor_mode=AA_SRC;
break;
case AA_SRC_OUT:
alpha_config->src_color_mode=AA_SRC_PRE_MUL;
alpha_config->src_factor_mode=AA_SRC_INVERSE;
alpha_config->dst_factor_mode=AA_ZERO;
break;
case AA_DST_OUT:
alpha_config->src_factor_mode=AA_ZERO;
alpha_config->dst_factor_mode=AA_SRC_INVERSE;
break;
case AA_SRC_ATOP:
alpha_config->src_color_mode=AA_SRC_PRE_MUL;
alpha_config->src_factor_mode=AA_SRC;
alpha_config->dst_factor_mode=AA_SRC_INVERSE;
break;
case AA_DST_ATOP:
alpha_config->src_color_mode=AA_SRC_PRE_MUL;
alpha_config->src_factor_mode=AA_SRC_INVERSE;
alpha_config->dst_factor_mode=AA_SRC;
break;
case AA_XOR:
alpha_config->src_color_mode=AA_SRC_PRE_MUL;
alpha_config->src_factor_mode=AA_SRC_INVERSE;
alpha_config->dst_factor_mode=AA_SRC_INVERSE;
break;
case AA_SRC_OVER_GLOBAL:
alpha_config->src_global_alpha_mode=AA_PER_PIX_GLOBAL;
alpha_config->src_color_mode=AA_SRC_NO_PRE_MUL;
alpha_config->src_factor_mode=AA_SRC_GLOBAL;
alpha_config->dst_factor_mode=AA_SRC_INVERSE;
break;
```

```
        default:
            printf("alpha mode error\n");
            break;
    }
```

6. CABC

CABC(Content Adaptive Backlight Control) is used to increase the contrast of such LCD-screens the backlight can be (globally) dimmed when the image to be displayed is dark (i.e. not comprising high intensity image data) while the image data is numerically corrected and adapted to the reduced backlight intensity.
There are 3x7 Gaussian filter tables in reg 0x1d0~0x1e4.
default value as follow:
0x1c8 : 0x15110903
0x1cc : 0x00030911
0x1d0 : 0x1a150b04
0x1d4 : 0x00040b15
0x1d8 : 0x15110903
0x1dc : 0x00030911
program guide：
step1: Config the panel total pixel number to register CABC_CTRL0 [26:4],and config the calc pixel num to register CABC_CTRL1 [26:4].
(typical: calc_pixel_num / total_pixel_num = 95% ~98%).
step2: Config pwm_config_mode ,cabc_handle_en to register CABC_CTRL0 .
step3: Config CABC_CTRL2 and CABC_CTRL3 register.
step4: write pwm gamma lut to CABC_GAMMA_LUT_ADDR (vop_base_addr + 0x1800),typical gamma value = 2.2(typical)
step5: Config cabc_lut_en and cabc_en to register CABC_CTRL1 [0] and CABC_CTRL0 [0].
step6: Config done.

7. BCSH

BCSH is used to adjust "Brightness,Contrast,Saturation,Hue",like IEP BCSH-10bit. For details,please refer to IEP chapter. The brightness adjust support (-64,63).The yuv data of color bar are 10bits.

8. Color space conversion

CSC after overlay:
There are 4 standards for YUV2RGB and RGB2YUV. For yuv2yuv ,we can use change among BT601L, BT601F, BT709L, BT2020 using coefficient registers.
YUV2RGB:
1. yuv to rgb (BT601L)
R = 1.164(Y-16) + 1.596(V-128)
G = 1.164(Y-16) - 0.391(U-128) - 0.813(V-128)
B = 1.164(Y-16) + 2.018(U-128)

2. yuv to rgb (BT601F)
R = (Y-16) + 1.402(V-128)
G = (Y-16) - 0.344(U-128) - 0.714(V-128)
B = (Y-16) + 1.772(U-128)

3. yuv to rgb (BT709L)
R = 1.164(Y-16) + 1.793(V-128)
G = 1.164(Y-16) - 0.213(U-128) - 0.534(V-128)
B = 1.164(Y-16) + 2.115(U-128)

4. yuv to rgb(BT2020)
R = 1.1636(Y-64) + 1.6778(V-512)
G = 1.1636(Y-64) - 0.1872(U-512) - 0.6501(V-512)
B = 1.1636(Y-64) + 2.1406(U-512)

RGB2YUV:

1. rgb to yuv(BT601L)
Y = 0.257R + 0.504G + 0.098B + 16
Cb =-0.148R - 0.291G + 0.439B + 128
Cr = 0.439R - 0.368G - 0.071B + 128

2. rgb to yuv(BT601F)
Y = 0.299R + 0.5870G + 0.1140B + 0
Cb = -0.1687R - 0.3313G + 0.5000B + 512
Cr = 0.500R - 0.4187G - 0.0813B + 512

3. rgb to yuv(BT709L)
Y = 0.183R + 0.614G + 0.062B + 16
Cb =-0.101R - 0.338G + 0.439B + 128
Cr = 0.439R - 0.399G - 0.040B + 128

4.rgb to yuv(BT2020)
Y = 0.2250R + 0.5807G + 0.0508B + 64
Cb = -0.1223R - 0.3157G + 0.4380B + 512
Cr = 0.4380R - 0.4028G - 0.0352B + 512

CSC in win0/win1:
The CSC module in win0/win1 is shown as follows . The coefficient of every 3x4 matrix is configurable , so it can realize conventional color space conversion . The CSC module in win2/win1 is the same as win2/win3 , except it don't have Y2R module .

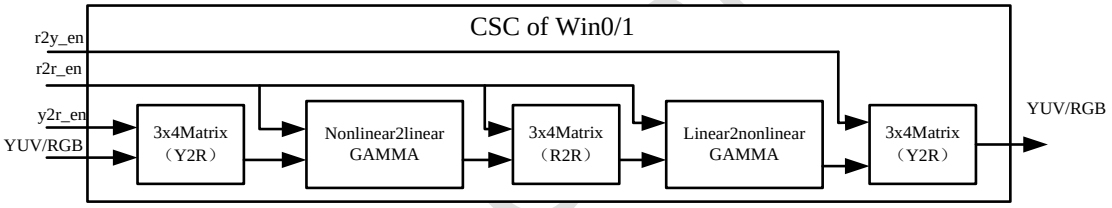


Fig. 3-14 YUV2YUV diagram

Detail configure is shown as follows .

Feature	y2r_en	r2r_en	r2y_en
YUV BYPASS	0	0	0
YUV TO RGB	1	0	0
YUV2020TOYUV709	1	1	1
YUV2020TORGB709	1	1	0
YUV709TOYUV2020	1	1	1
YUV709TORGB2020	1	1	0
RGB BYPASS	0	0	0
RGB TO YUV	0	0	1
RGB2020TOYUV709	0	1	1
RGB2020TORGB709	0	1	0
RGB709TOYUV2020	0	1	1
RGB709TORGB2020	0	1	0

9. Pre-Dither Down

Dithering is an intentional applied form of noise , using to randomize quantization error, and thereby preventing large-scaling patterns such as "banding".
The pixel value is used by dithering process to display the data in a lower color depth on the LCD panel, i.e, the source input format is RGB101010 and display output format is RGB888. When dithering is enable(VOP_DSP_CTRL0[2]=1), the output data is generated by dithering algorithm based on the pixel position and the value of removed bits. Otherwise, the MSBs of the pixel color components are output as display data.

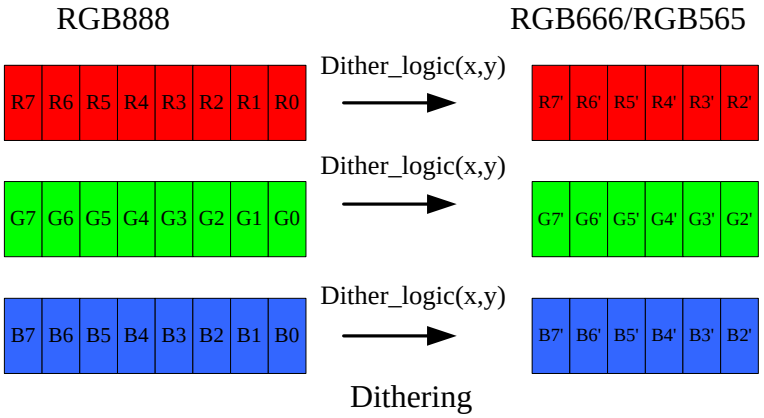


Fig. 3-17 Pre-Dither Down

10. Gamma Correction

Gamma Correction is necessary because most monitors don't have a linear relationship between the voltage and the brightness, which results in your scene looking like it has too much contrast and the light falling off from the source outward, happens too quickly. The result can also be problematic if you are going into a composition program.

You can correct this by "Gamma Correction", which allows you to display the images and textures on your computer in an accurate manner.

Your screen is not linear, in that it displays the brightness unevenly. As a result, the image looks to be more high contrast than it should, you end up adding more lights or turning up the intensity, or you don't use the lighting in a realistic way that matches well with live action scenes. It also creates problems for you if you use compositing software.

There are three 1024x10bits line buffers separately for 8bit-R/G/B gamma correction. You can write gamma correction LUT through register" GAMMA_LUT_ADDR" one by one.

11. Output format

Config dsp_out_mode register to adapt a variety of panel interface. As follow:

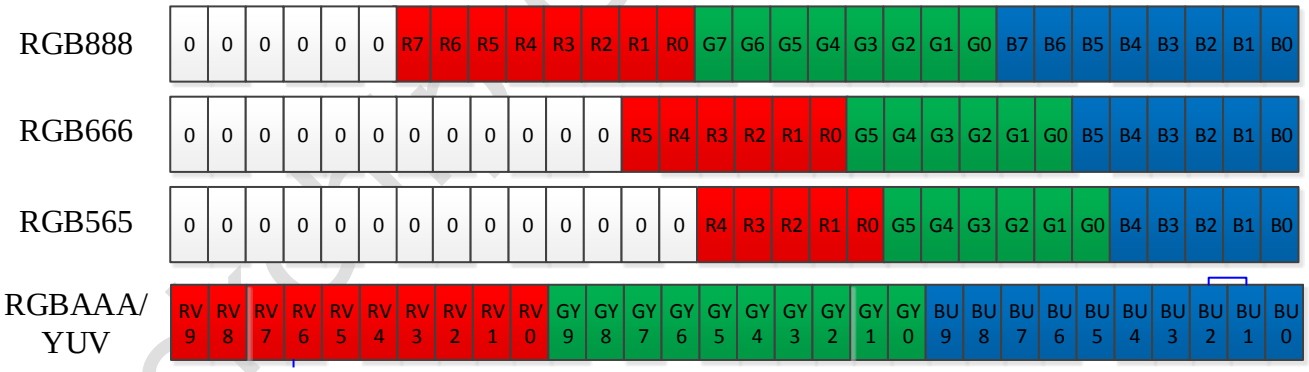


Fig. 3-15 dsp_out_mode description

12. DDR Frequency Conversion

program guide:

Step1:Enable intr_en_dsp_hold_valid in INTR_EN0

Step2:Enable dsp_fp_standy in SYS_CTRL1

Step3:Wait for dsp_hold_valid interrupt

Step4:Convert DDR frequency

Step5:Disable dsp_fp_standy in SYS_CTRL1

3.3.8 Write back

There is a WB module for writing overlay data to ddr.

program guide:

step1: Configure the dst ddr address to register WB_YRGB_MST(RGB or YUV) and WB_CBR_MST(YUV 420 only).

step2: Configure WB_CTRL0.
step3: Configure WB_CTRL1.
step4: Configure done.
step5: Check dma_finish interrupt,and check there is no wb error interrupt.
Then,writeback data is valid.

If overlay mode is YUV444 , the WB format must be YUV420 . If overlay mode is RGB888 and WB format is YUV420 , the wb_r2y_en should be 1 .

3.3.9 AFBCD

This compression format is designed to be used for textures and frame buffers. It has been optimized to decrease external bandwidth as well as being random access and decodable at line speed for the texture cache.
The config for AFBCD is relative to the format of the source data . For example , if the AFBCD source data is "block split" compression , the afbcd_hreg_block_split of AFBCD_CTRL0 must be 1 .

3.4 VOP_BIG Register Description

3.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

3.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
VOP_REG_CFG_DONE	0x0000	W	0x00000000	Register config done flag
VOP_VERSION_INFO	0x0004	W	0x00000000	Version for vop
VOP_SYS_CTRL	0x0008	W	0x00801800	System control register0
VOP_SYS_CTRL1	0x000c	W	0x0003a000	System control register1
VOP_DSP_CTRL0	0x0010	W	0x00000000	
VOP_DSP_CTRL1	0x0014	W	0x0000e400	Display control register1
VOP_DSP_BG	0x0018	W	0x00000000	Background color
VOP_MCU_CTRL	0x001c	W	0x00711c08	MCU mode control register
VOP_WB_CTRL0	0x0020	W	0xed000000	write back ctrl0
VOP_WB_CTRL1	0x0024	W	0x00000000	write back ctrl1
VOP_WB_YRGB_MST	0x0028	W	0x00000000	write back yrgb mst
VOP_WB_CBR_MST	0x002c	W	0x00000000	write back cbr mst
VOP_WIN0_CTRL0	0x0030	W	0x3a000040	Win0 ctrl register0
VOP_WIN0_CTRL1	0x0034	W	0x00000000	Win0 ctrl register1
VOP_WIN0_COLOR_KEY	0x0038	W	0x00000000	Win0 color key register
VOP_WIN0_VIR	0x003c	W	0x01400140	Win0 virtual stride
VOP_WIN0_YRGB_MST	0x0040	W	0x00000000	Win0 YRGB memory start address
VOP_WIN0_CBR_MST	0x0044	W	0x00000000	Win0 Cbr memory start address
VOP_WIN0_ACT_INFO	0x0048	W	0x00ef013f	Win0 active window width/height
VOP_WIN0_DSP_INFO	0x004c	W	0x00ef013f	Win0 display width/height on panel
VOP_WIN0_DSP_ST	0x0050	W	0x000a000a	Win0 display start point on panel
VOP_WIN0_SCL_FACTOR_YRGB	0x0054	W	0x10001000	Win0 YRGB scaling factor
VOP_WIN0_SCL_FACTOR_CBR	0x0058	W	0x10001000	Win0 Cbr scaling factor

Name	Offset	Size	Reset Value	Description
VOP_WIN0_SCL_OFFSET	0x005c	W	0x00000000	Win0 scaling start point offset
VOP_WIN0_SRC_ALPHA_CTRL	0x0060	W	0x00000000	Win0 alpha source control register
VOP_WIN0_DST_ALPHA_CTRL	0x0064	W	0x00000000	Win0 alpha destination control register
VOP_WIN0_FADING_CTRL	0x0068	W	0x00000000	Win0 fading contrl register
VOP_WIN0_CTRL2	0x006c	W	0x00000021	Win0 ctrl register2
VOP_WIN1_CTRL0	0x0070	W	0x3a000040	Win1 ctrl register0
VOP_WIN1_CTRL1	0x0074	W	0x00000000	Win1 ctrl register1
VOP_WIN1_COLOR_KEY	0x0078	W	0x00000000	Win1 color key register
VOP_WIN1_VIR	0x007c	W	0x01400140	win1 virtual stride
VOP_WIN1_YRGB_MST	0x0080	W	0x00000000	Win1 YRGB memory start address
VOP_WIN1_CBR_MST	0x0084	W	0x00000000	Win1 Cbr memory start address
VOP_WIN1_ACT_INFO	0x0088	W	0x00ef013f	Win1 active window width/height
VOP_WIN1_DSP_INFO	0x008c	W	0x00ef013f	Win1 display width/height on panel
VOP_WIN1_DSP_ST	0x0090	W	0x000a000a	Win1 display start point on panel
VOP_WIN1_SCL_FACTOR_YRGB	0x0094	W	0x10001000	Win1 YRGB scaling factor
VOP_WIN1_SCL_FACTOR_CBR	0x0098	W	0x10001000	Win1 Cbr scaling factor
VOP_WIN1_SCL_OFFSET	0x009c	W	0x00000000	Win1 scaling start point offset
VOP_WIN1_SRC_ALPHA_CTRL	0x00a0	W	0x00000000	Win1 alpha source control register
VOP_WIN1_DST_ALPHA_CTRL	0x00a4	W	0x00000000	Win1 alpha destination control register
VOP_WIN1_FADING_CTRL	0x00a8	W	0x00000000	Win1 fading contrl register
VOP_WIN1_CTRL2	0x00ac	W	0x00000043	Win1 ctrl register2
VOP_WIN2_CTRL0	0x00b0	W	0x00000000	win2 ctrl register0
VOP_WIN2_CTRL1	0x00b4	W	0x00501d00	win2 ctrl register1
VOP_WIN2_VIR0_1	0x00b8	W	0x01400140	Win2 virtual stride0 and virtaul stride1
VOP_WIN2_VIR2_3	0x00bc	W	0x01400140	Win2 virtual stride2 and virtaul stride3
VOP_WIN2_MST0	0x00c0	W	0x00000000	Win2 memory start address0
VOP_WIN2_DSP_INFO0	0x00c4	W	0x00ef013f	Win2 display width0/height0 on panel
VOP_WIN2_DSP_ST0	0x00c8	W	0x000a000a	Win2 display start point0 on panel
VOP_WIN2_COLOR_KEY	0x00cc	W	0x00000000	Win2 color key register
VOP_WIN2_MST1	0x00d0	W	0x00000000	Win2 memory start address1
VOP_WIN2_DSP_INFO1	0x00d4	W	0x00ef013f	Win2 display width1/height1 on panel
VOP_WIN2_DSP_ST1	0x00d8	W	0x000a000a	Win2 display start point1 on panel
VOP_WIN2_SRC_ALPHA_CTRL	0x00dc	W	0x00000000	Win2 alpha source control register

Name	Offset	Size	Reset Value	Description
VOP_WIN2_MST2	0x00e0	W	0x00000000	Win2 memory start address2
VOP_WIN2_DSP_INFO2	0x00e4	W	0x00ef013f	Win2 display width2/height2 on panel
VOP_WIN2_DSP_ST2	0x00e8	W	0x000a000a	Win2 display start point2 on panel
VOP_WIN2_DST_ALPHA_CTRL	0x00ec	W	0x00000000	Win2 alpha destination control register
VOP_WIN2_MST3	0x00f0	W	0x00000000	Win2 memory start address3
VOP_WIN2_DSP_INFO3	0x00f4	W	0x00ef013f	Win2 display width3/height3 on panel
VOP_WIN2_DSP_ST3	0x00f8	W	0x000a000a	Win2 display start point3 on panel
VOP_WIN2_FADING_CTRL	0x00fc	W	0x00000000	Win2 fading contrl register
VOP_WIN3_CTRL0	0x0100	W	0x00000000	Win3 ctrl register0
VOP_WIN3_CTRL1	0x0104	W	0x00601d00	Win3 ctrl register1
VOP_WIN3_VIR0_1	0x0108	W	0x01400140	Win3 virtual stride0 and virtaul stride1
VOP_WIN3_VIR2_3	0x010c	W	0x01400140	Win3 virtual stride2 and virtaul stride3
VOP_WIN3_MST0	0x0110	W	0x00000000	Win3 memory start address0
VOP_WIN3_DSP_INFO0	0x0114	W	0x00ef013f	Win3 display width0/height0 on panel
VOP_WIN3_DSP_ST0	0x0118	W	0x000a000a	Win3 display start point0 on panel
VOP_WIN3_COLOR_KEY	0x011c	W	0x00000000	Win3 color key register
VOP_WIN3_MST1	0x0120	W	0x00000000	Win3 memory start address1
VOP_WIN3_DSP_INFO1	0x0124	W	0x00ef013f	Win3 display width1/height1 on panel
VOP_WIN3_DSP_ST1	0x0128	W	0x000a000a	Win3 display start point1 on panel
VOP_WIN3_SRC_ALPHA_CTRL	0x012c	W	0x00000000	Win3 alpha source control register
VOP_WIN3_MST2	0x0130	W	0x00000000	Win3 memory start address2
VOP_WIN3_DSP_INFO2	0x0134	W	0x00ef013f	Win3 display width2/height2 on panel
VOP_WIN3_DSP_ST2	0x0138	W	0x000a000a	Win3 display start point2 on panel
VOP_WIN3_DST_ALPHA_CTRL	0x013c	W	0x00000000	Win3 alpha destination control register
VOP_WIN3_MST3	0x0140	W	0x00000000	Win3 memory start address3
VOP_WIN3_DSP_INFO3	0x0144	W	0x00ef013f	Win3 display width3/height3 on panel
VOP_WIN3_DSP_ST3	0x0148	W	0x000a000a	Win3 display start point3 on panel
VOP_WIN3_FADING_CTRL	0x014c	W	0x00000000	Win3 fading contrl register
VOP_HWC_CTRL0	0x0150	W	0x00000000	Hwc ctrl register0
VOP_HWC_CTRL1	0x0154	W	0x00701d00	Hwc ctrl register1
VOP_HWC_MST	0x0158	W	0x00000000	Hwc memory start address
VOP_HWC_DSP_ST	0x015c	W	0x000a000a	Hwc display start point on panel

Name	Offset	Size	Reset Value	Description
VOP_HWC_SRC_ALPHA_CTRL	0x0160	W	0x00000000	Hwc alpha source control register
VOP_HWC_DST_ALPHA_CTRL	0x0164	W	0x00000000	Hwc alpha destination control register
VOP_HWC_FADING_CTRL	0x0168	W	0x00000000	Hwc fading contrl register
VOP_HWC_RESERVED1	0x016c	W	0x00000000	Hwc reserved
VOP_POST_DSP_HACT_INFO	0x0170	W	0x000a014a	Post scaler down horizontal start and end
VOP_POST_DSP_VACT_INFO	0x0174	W	0x000a00fa	Panel active horizontal scanning start point and end point
VOP_POST_SCL_FACTOR_YRGB	0x0178	W	0x10001000	Post yrgb scaling factor
VOP_POST_RESERVED	0x017c	W	0x00000000	Post reserved
VOP_POST_SCL_CTRL	0x0180	W	0x00000000	Post scaling start point offset
VOP_POST_DSP_VACT_INFO_F1	0x0184	W	0x000a00fa	Panel active horizontal scanning start point and end point F1
VOP_DSP_HTOTAL_HS_END	0x0188	W	0x014a000a	Panel scanning horizontal width and hsync pulse end point
VOP_DSP_HACT_ST_END	0x018c	W	0x000a014a	Panel active horizontal scanning start point and end point
VOP_DSP_VTOTAL_VS_END	0x0190	W	0x00fa000a	Panel scanning vertical height and vsync pulse end point
VOP_DSP_VACT_ST_END	0x0194	W	0x000a00fa	Panel active vertical scanning start point and end point
VOP_DSP_VS_ST_END_F1	0x0198	W	0x00000000	Vertical scanning start point and vsync pulse end point of even filed in interlace mode
VOP_DSP_VACT_ST_END_F1	0x019c	W	0x00000000	Vertical scanning active start point and end point of even filed in interlace mode
VOP_PWM_CTRL	0x01a0	W	0x0000200a	PWM Control Register
VOP_PWM_PERIOD_HPR	0x01a4	W	0x00000000	PWM Period Register/High Polarity Capture Register
VOP_PWM_DUTY_LPR	0x01a8	W	0x00000000	PWM Duty Register/Low Polarity Capture Register
VOP_PWM_CNT	0x01ac	W	0x00000000	PWM Counter Register
VOP_BCSH_COLOR_BAR	0x01b0	W	0x00000000	Color bar config register
VOP_BCSH_BCS	0x01b4	W	0xd0010000	Brightness contrast saturation*contrast config register
VOP_BCSH_H	0x01b8	W	0x01000000	Sin hue and cos hue config register
VOP_BCSH_CTRL	0x01bc	W	0x00000000	BCSH contrl register
VOP_CABC_CTRL0	0x01c0	W	0x00ed8000	Content Adaptive Backlight Control register0
VOP_CABC_CTRL1	0x01c4	W	0x00fa0000	Content Adaptive Backlight Control register1

Name	Offset	Size	Reset Value	Description
VOP_CABC_CTRL2	0x01c8	W	0x000110f0	Content Adaptive Backlight Control register2
VOP_CABC_CTRL3	0x01cc	W	0x00000000	Content Adaptive Backlight Control register3
VOP_CABC_GAUSS_LINE0_0	0x01d0	W	0x15110903	CABC gauss line config register00
VOP_CABC_GAUSS_LINE0_1	0x01d4	W	0x00030911	CABC gauss line config register01
VOP_CABC_GAUSS_LINE1_0	0x01d8	W	0x1a150b04	CABC gauss line config register10
VOP_CABC_GAUSS_LINE1_1	0x01dc	W	0x00040b15	CABC gauss line config register11
VOP_CABC_GAUSS_LINE2_0	0x01e0	W	0x15110903	CABC gauss line config register20
VOP_CABC_GAUSS_LINE2_1	0x01e4	W	0x00030911	CABC gauss line config register21
VOP_FRC_LOWER01_0	0x01e8	W	0x12844821	FRC lookup table config register010
VOP_FRC_LOWER01_1	0x01ec	W	0x21488412	FRC lookup table config register011
VOP_FRC_LOWER10_0	0x01f0	W	0xa55a9696	FRC lookup table config register100
VOP_FRC_LOWER10_1	0x01f4	W	0x5aa56969	FRC lookup table config register101
VOP_FRC_LOWER11_0	0x01f8	W	0xdeb77bed	FRC lookup table config register110
VOP_FRC_LOWER11_1	0x01fc	W	0xed7bb7de	FRC lookup table config register111
VOP_AFBCD0_CTRL	0x0200	W	0x00000000	AFBCD0 control register
VOP_AFBCD0_HDR_PTR	0x0204	W	0x00000000	AFBCD0 memory start address
VOP_AFBCD0_PIC_SIZE	0x0208	W	0x00000000	AFBCD0 pic size
VOP_AFBCD0_STATUS	0x020c	W	0x00000000	AFBCD0 status
VOP_INTR_EN0	0x0280	W	0x00000000	Interrupt enable register
VOP_INTR_CLEAR0	0x0284	W	0x00000000	Interrupt clear register
VOP_INTR_STATUS0	0x0288	W	0x00000000	interrupt status
VOP_INTR_RAW_STATUS0	0x028c	W	0x00000000	raw interrupt status
VOP_INTR_EN1	0x0290	W	0x00000000	Interrupt enable register
VOP_INTR_CLEAR1	0x0294	W	0x00000000	Interrupt clear register
VOP_INTR_STATUS1	0x0298	W	0x00000000	interrupt status
VOP_INTR_RAW_STATUS1	0x029c	W	0x00000000	raw interrupt status
VOP_LINE_FLAG	0x02a0	W	0x00000000	Line flag config register
VOP_VOP_STATUS	0x02a4	W	0x00000000	vop status register

Name	Offset	Size	Reset Value	Description
VOP_BLANKING_VALUE	0x02a8	W	0x00000000	Register0000 Abstract
VOP_MCU_BYPASS_PORT	0x02ac	W	0x00000000	MCU bypass port
VOP_WIN0_DSP_BG	0x02b0	W	0x00000000	Win0 layer background color
VOP_WIN1_DSP_BG	0x02b4	W	0x00000000	Win1 layer background color
VOP_WIN2_DSP_BG	0x02b8	W	0x00000000	Win2 layer background color
VOP_WIN3_DSP_BG	0x02bc	W	0x00000000	Win3 layer background color
VOP_YUV2YUV_WIN	0x02c0	W	0x00000000	win yuv2yuv control register
VOP_AUTO_GATING_EN	0x02cc	W	0x00000000	Auto gating enable
VOP_WIN0_YUV2YUV_Y2R_COE0	0x04e0	W	0x00000000	WIN0 yuv2yuv y2r cofficient
VOP_WIN0_YUV2YUV_Y2R_COE1	0x04e4	W	0x00000000	WIN0 yuv2yuv y2r cofficient
VOP_WIN0_YUV2YUV_Y2R_COE2	0x04e8	W	0x00000000	WIN0 yuv2yuv y2r cofficient
VOP_WIN0_YUV2YUV_Y2R_COE3	0x04ec	W	0x00000000	WIN0yuv2yuv y2r cofficient
VOP_WIN0_YUV2YUV_Y2R_COE4	0x04f0	W	0x00000000	WIN0 yuv2yuv y2r cofficient
VOP_WIN0_YUV2YUV_Y2R_COE5	0x04f4	W	0x00000000	WIN0 yuv2yuv y2r cofficient
VOP_WIN0_YUV2YUV_Y2R_COE6	0x04f8	W	0x00000000	WIN0 yuv2yuv y2r cofficient
VOP_WIN0_YUV2YUV_Y2R_COE7	0x04fc	W	0x00000000	WIN0 yuv2yuv y2r cofficient
VOP_WIN0_YUV2YUV_R2R_COE0	0x0500	W	0x00000000	WIN0 yuv2yuv r2r cofficient
VOP_WIN0_YUV2YUV_R2R_COE1	0x0504	W	0x00000000	WIN0 yuv2yuv r2r cofficient
VOP_WIN0_YUV2YUV_R2R_COE2	0x0508	W	0x00000000	WIN0 yuv2yuv r2r cofficient
VOP_WIN0_YUV2YUV_R2R_COE3	0x050c	W	0x00000000	WIN0 yuv2yuv r2r cofficient
VOP_WIN0_YUV2YUV_R2R_COE4	0x0510	W	0x00000000	WIN0 yuv2yuv r2r cofficient
VOP_WIN0_YUV2YUV_R2R_COE5	0x0514	W	0x00000000	WIN0 yuv2yuv r2r cofficient
VOP_WIN0_YUV2YUV_R2R_COE6	0x0518	W	0x00000000	WIN0 yuv2yuv r2r cofficient
VOP_WIN0_YUV2YUV_R2R_COE7	0x051c	W	0x00000000	WIN0 yuv2yuv r2r cofficient
VOP_WIN0_YUV2YUV_R2Y_COE0	0x0520	W	0x00000000	WIN0 yuv2yuv r2y cofficient
VOP_WIN0_YUV2YUV_R2Y_COE1	0x0524	W	0x00000000	WIN0 yuv2yuv r2y cofficient

Name	Offset	Size	Reset Value	Description
VOP_WIN0_YUV2YUV_R2Y_COE2	0x0528	W	0x00000000	WIN0 yuv2yuv r2y cofficient
VOP_WIN0_YUV2YUV_R2Y_COE3	0x052c	W	0x00000000	WIN0 yuv2yuv r2y cofficient
VOP_WIN0_YUV2YUV_R2Y_COE4	0x0530	W	0x00000000	WIN0 yuv2yuv r2y cofficient
VOP_WIN0_YUV2YUV_R2Y_COE5	0x0534	W	0x00000000	WIN0 yuv2yuv r2y cofficient
VOP_WIN0_YUV2YUV_R2Y_COE6	0x0538	W	0x00000000	WIN0 yuv2yuv r2y cofficient
VOP_WIN0_YUV2YUV_R2Y_COE7	0x053c	W	0x00000000	WIN0 yuv2yuv r2y cofficient
VOP_WIN1_YUV2YUV_Y2R_COE0	0x0540	W	0x00000000	WIN1 yuv2yuv y2r cofficient
VOP_WIN1_YUV2YUV_Y2R_COE1	0x0544	W	0x00000000	WIN1 yuv2yuv y2r cofficient
VOP_WIN1_YUV2YUV_Y2R_COE2	0x0548	W	0x00000000	WIN1 yuv2yuv y2r cofficient
VOP_WIN1_YUV2YUV_Y2R_COE3	0x054c	W	0x00000000	WIN1 yuv2yuv y2r cofficient
VOP_WIN1_YUV2YUV_Y2R_COE4	0x0550	W	0x00000000	WIN1 yuv2yuv y2r cofficient
VOP_WIN1_YUV2YUV_Y2R_COE5	0x0554	W	0x00000000	WIN1 yuv2yuv y2r cofficient
VOP_WIN1_YUV2YUV_Y2R_COE6	0x0558	W	0x00000000	WIN1 yuv2yuv y2r cofficient
VOP_WIN1_YUV2YUV_Y2R_COE7	0x055c	W	0x00000000	WIN1 yuv2yuv y2r cofficient
VOP_WIN1_YUV2YUV_R2R_COE0	0x0560	W	0x00000000	WIN0 yuv2yuv r2r cofficient
VOP_WIN1_YUV2YUV_R2R_COE1	0x0564	W	0x00000000	WIN1 yuv2yuv r2r cofficient
VOP_WIN1_YUV2YUV_R2R_COE2	0x0568	W	0x00000000	WIN1 yuv2yuv r2r cofficient
VOP_WIN1_YUV2YUV_R2R_COE3	0x056c	W	0x00000000	WIN1 yuv2yuv r2r cofficient
VOP_WIN1_YUV2YUV_R2R_COE4	0x0570	W	0x00000000	WIN1 yuv2yuv r2r cofficient
VOP_WIN1_YUV2YUV_R2R_COE5	0x0574	W	0x00000000	WIN1 yuv2yuv r2r cofficient
VOP_WIN1_YUV2YUV_R2R_COE6	0x0578	W	0x00000000	WIN1 yuv2yuv r2r cofficient
VOP_WIN1_YUV2YUV_R2R_COE7	0x057c	W	0x00000000	WIN1 yuv2yuv r2r cofficient

Name	Offset	Size	Reset Value	Description
VOP_WIN1_YUV2YUV_R2Y_COE0	0x0580	W	0x00000000	WIN1 yuv2yuv r2y cofficient
VOP_WIN1_YUV2YUV_R2Y_COE1	0x0584	W	0x00000000	WIN1 yuv2yuv r2y cofficient
VOP_WIN1_YUV2YUV_R2Y_COE2	0x0588	W	0x00000000	WIN1 yuv2yuv r2y cofficient
VOP_WIN1_YUV2YUV_R2Y_COE3	0x058c	W	0x00000000	WIN1 yuv2yuv r2y cofficient
VOP_WIN1_YUV2YUV_R2Y_COE4	0x0590	W	0x00000000	WIN1 yuv2yuv r2y cofficient
VOP_WIN1_YUV2YUV_R2Y_COE5	0x0594	W	0x00000000	WIN1 yuv2yuv r2y cofficient
VOP_WIN1_YUV2YUV_R2Y_COE6	0x0598	W	0x00000000	WIN1 yuv2yuv r2y cofficient
VOP_WIN1_YUV2YUV_R2Y_COE7	0x059c	W	0x00000000	WIN1 yuv2yuv r2y cofficient
VOP_WIN2_YUV2YUV_Y2R_COE0	0x05a0	W	0x00000000	WIN2 yuv2yuv y2r cofficient
VOP_WIN2_YUV2YUV_Y2R_COE1	0x05a4	W	0x00000000	WIN2 yuv2yuv y2r cofficient
VOP_WIN2_YUV2YUV_Y2R_COE2	0x05a8	W	0x00000000	WIN2 yuv2yuv y2r cofficient
VOP_WIN2_YUV2YUV_Y2R_COE3	0x05ac	W	0x00000000	WIN2 yuv2yuv y2r cofficient
VOP_WIN2_YUV2YUV_Y2R_COE4	0x05b0	W	0x00000000	WIN2 yuv2yuv y2r cofficient
VOP_WIN2_YUV2YUV_Y2R_COE5	0x05b4	W	0x00000000	WIN2 yuv2yuv y2r cofficient
VOP_WIN2_YUV2YUV_Y2R_COE6	0x05b8	W	0x00000000	WIN2 yuv2yuv y2r cofficient
VOP_WIN2_YUV2YUV_Y2R_COE7	0x05bc	W	0x00000000	WIN2 yuv2yuv y2r cofficient
VOP_WIN2_YUV2YUV_R2R_COE0	0x05c0	W	0x00000000	WIN2 yuv2yuv r2r cofficient
VOP_WIN2_YUV2YUV_R2R_COE1	0x05c4	W	0x00000000	WIN2 yuv2yuv r2r cofficient
VOP_WIN2_YUV2YUV_R2R_COE2	0x05c8	W	0x00000000	WIN2 yuv2yuv r2r cofficient
VOP_WIN2_YUV2YUV_R2R_COE3	0x05cc	W	0x00000000	WIN2 yuv2yuv r2r cofficient
VOP_WIN2_YUV2YUV_R2R_COE4	0x05d0	W	0x00000000	WIN2 yuv2yuv r2r cofficient
VOP_WIN2_YUV2YUV_R2R_COE5	0x05d4	W	0x00000000	WIN2 yuv2yuv r2r cofficient

Name	Offset	Size	Reset Value	Description
VOP_WIN2_YUV2YUV_R2R_COE6	0x05d8	W	0x00000000	WIN2 yuv2yuv r2r cofficient
VOP_WIN2_YUV2YUV_R2R_COE7	0x05dc	W	0x00000000	WIN2 yuv2yuv r2r cofficient
VOP_WIN2_YUV2YUV_R2Y_COE0	0x05e0	W	0x00000000	WIN2 yuv2yuv r2y cofficient
VOP_WIN2_YUV2YUV_R2Y_COE1	0x05e4	W	0x00000000	WIN2 yuv2yuv r2y cofficient
VOP_WIN2_YUV2YUV_R2Y_COE2	0x05e8	W	0x00000000	WIN2 yuv2yuv r2y cofficient
VOP_WIN2_YUV2YUV_R2Y_COE3	0x05ec	W	0x00000000	WIN2 yuv2yuv r2y cofficient
VOP_WIN2_YUV2YUV_R2Y_COE4	0x05f0	W	0x00000000	WIN2 yuv2yuv r2y cofficient
VOP_WIN2_YUV2YUV_R2Y_COE5	0x05f4	W	0x00000000	WIN2 yuv2yuv r2y cofficient
VOP_WIN2_YUV2YUV_R2Y_COE6	0x05f8	W	0x00000000	WIN2 yuv2yuv r2y cofficient
VOP_WIN2_YUV2YUV_R2Y_COE7	0x05fc	W	0x00000000	WIN2 yuv2yuv r2y cofficient
VOP_WIN3_YUV2YUV_Y2R_COE0	0x0600	W	0x00000000	WIN3 yuv2yuv y2r cofficient
VOP_WIN3_YUV2YUV_Y2R_COE1	0x0604	W	0x00000000	WIN3 yuv2yuv y2r cofficient
VOP_WIN3_YUV2YUV_Y2R_COE2	0x0608	W	0x00000000	WIN3 yuv2yuv y2r cofficient
VOP_WIN3_YUV2YUV_Y2R_COE3	0x060c	W	0x00000000	WIN3 yuv2yuv y2r cofficient
VOP_WIN3_YUV2YUV_Y2R_COE4	0x0610	W	0x00000000	WIN3 yuv2yuv y2r cofficient
VOP_WIN3_YUV2YUV_Y2R_COE5	0x0614	W	0x00000000	WIN3 yuv2yuv y2r cofficient
VOP_WiN3_YUV2YUV_Y2R_COE6	0x0618	W	0x00000000	WIN3 yuv2yuv y2r cofficient
VOP_WIN3_YUV2YUV_Y2R_COE7	0x061c	W	0x00000000	WIN3 yuv2yuv y2r cofficient
VOP_WIN3_YUV2YUV_R2R_COE0	0x0620	W	0x00000000	WIN3 yuv2yuv r2r cofficient
VOP_WIN3_YUV2YUV_R2R_COE1	0x0624	W	0x00000000	WIN3 yuv2yuv r2r cofficient
VOP_WIN3_YUV2YUV_R2R_COE2	0x0628	W	0x00000000	WIN3 yuv2yuv r2r cofficient
VOP_WIN3_YUV2YUV_R2R_COE3	0x062c	W	0x00000000	WIN3 yuv2yuv r2r cofficient

Name	Offset	Size	Reset Value	Description
VOP_WIN3_YUV2YUV_R2R_COE4	0x0630	W	0x00000000	WIN3 yuv2yuv r2r cofficient
VOP_WIN3_YUV2YUV_R2R_COE5	0x0634	W	0x00000000	WIN3 yuv2yuv r2r cofficient
VOP_WIN3_YUV2YUV_R2R_COE6	0x0638	W	0x00000000	WIN3 yuv2yuv r2r cofficient
VOP_WIN3_YUV2YUV_R2R_COE7	0x063c	W	0x00000000	WIN3 yuv2yuv r2r cofficient
VOP_WIN3_YUV2YUV_R2Y_COE0	0x0640	W	0x00000000	WIN3 yuv2yuv r2y cofficient
VOP_WIN3_YUV2YUV_R2Y_COE1	0x0644	W	0x00000000	WIN3 yuv2yuv r2y cofficient
VOP_WIN3_YUV2YUV_R2Y_COE2	0x0648	W	0x00000000	WIN3 yuv2yuv r2y cofficient
VOP_WIN3_YUV2YUV_R2Y_COE3	0x064c	W	0x00000000	WIN3 yuv2yuv cofficient
VOP_WIN3_YUV2YUV_R2Y_COE4	0x0650	W	0x00000000	WIN3 yuv2yuv r2y cofficient
VOP_WIN3_YUV2YUV_R2Y_COE5	0x0654	W	0x00000000	WIN3 yuv2yuv r2y cofficient
VOP_WIN3_YUV2YUV_R2Y_COE6	0x0658	W	0x00000000	WIN3 yuv2yuv r2y cofficient
VOP_WIN3_YUV2YUV_R2Y_COE7	0x065c	W	0x00000000	WIN3 yuv2yuv r2y cofficient
VOP_WIN2_LUT_ADDR	0x1000	W	0x00000000	Win2 lut base address
VOP_WIN3_LUT_ADDR	0x1400	W	0x00000000	Win3 lut base address
VOP_HWC_LUT_ADDR	0x1800	W	0x00000000	Hwc lut base address
VOP_CABC_GAMMA_LUT_ADDR	0x1c00	W	0x00000000	CABC GAMMA lut base address
VOP_GAMMA_LUT_ADDR	0x2000	W	0x00000000	GAMMA lut base address
VOP_MMU_DTE_ADDR	0x3f00	W	0x00000000	MMU current page Table address
VOP_MMU_STATUS	0x3f04	W	0x00000000	MMU status register
VOP_MMU_COMMAND	0x3f08	W	0x00000000	MMU command register
VOP_MMU_PAGE_FAULT_ADDR	0x3f0c	W	0x00000000	MMU logical address of last page fault
VOP_MMU_ZAP_ONE_LINE	0x3f10	W	0x00000000	MMU Zap cache line register
VOP_MMU_INT_RAWSTAT	0x3f14	W	0x00000000	MMU raw interrupt status register
VOP_MMU_INT_CLEAR	0x3f18	W	0x00000000	MMU raw interrupt status register
VOP_MMU_INT_MASK	0x3f1c	W	0x00000000	MMU raw interrupt status register
VOP_MMU_INT_STATUS	0x3f20	W	0x00000000	MMU raw interrupt status register
VOP_MMU_AUTO_GATING	0x3f24	W	0x00000000	MMU auto gating

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

3.4.3 Detail Register Description

VOP_REG_CFG_DONE
Address: Operational Base + offset (0x0000)
Register config done flag

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:9	RO	0x0	reserved
8	RW	0x0	reg_load_sys_en vop system register config done flag In the first setting of the register, the new value was saved into the mirror register. When all the system register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
7	RW	0x0	reg_load_fbdc_en vop fbdc register config done flag In the first setting of the register, the new value was saved into the mirror register. When all the fbdc register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
6	RW	0x0	reg_load_iep_en vop iep register config done flag In the first setting of the register, the new value was saved into the mirror register. When all the iep register config finish(only 2 signals direct_path_en,direct_path_layer_sel), writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
5	RW	0x0	reg_load_hwc_en vop hwc register config done flag In the first setting of the register, the new value was saved into the mirror register. When all the hwc register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
4	RW	0x0	reg_load_win3_en vop win3 register config done flag In the first setting of the register, the new value was saved into the mirror register. When all the win3 register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.

Bit	Attr	Reset Value	Description
3	RW	0x0	reg_load_win2_en vop win2 register config done flag In the first setting of the register, the new value was saved into the mirror register. When all the win2 register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
2	RW	0x0	reg_load_win1_en vop win1 register config done flag In the first setting of the register, the new value was saved into the mirror register. When all the win1 register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
1	RW	0x0	reg_load_win0_en vop win0 register config done flag In the first setting of the register, the new value was saved into the mirror register. When all the win0 register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
0	WO	0x0	reg_load_en vop register config done flag In the first setting of the register, the new value was saved into the mirror register. When all the register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.

VOP_VERSION_INFO
Address: Operational Base + offset (0x0004)
Version for vop

Bit	Attr	Reset Value	Description
31:24	RO	0x00	major IP major vertion used for IP structure
23:16	RO	0x00	minor minor vertion big feature change under same structure
15:0	RO	0x0000	svnbuild rtl current svn number

VOP_SYS_CTRL
Address: Operational Base + offset (0x0008)
System control register0

Bit	Attr	Reset Value	Description
31	RW	0x0	io_pad_clk_sel
30	RO	0x0	vop_field_tve_pol
29	RW	0x0	dac_sel dac output sel for tve in fpga dac output sel for tve in fpga 1'b0:dac 3 1'b1:dac 1
28	RW	0x0	genlock genlock for tve genlock for tve in fpga 1'b0:master mode 1'b1:slave mode
27	RW	0x0	uv_offset_en uv offset enable uv offset enable
26	RW	0x0	tve_mode tve mode 1'b0:NTSC 1'b1:PAL
25	RW	0x0	imd_tve_dclk_pol tve dclk pol tve dclk pol
24	RW	0x0	imd_tve_dclk_en tve dclk enable tve dclk enable
23	RW	0x1	auto_gating_en LCDC layer axi-clk auto gating enable 1'b0 : disable auto gating 1'b1 : enable auto gating default auto gating enable
22	RW	0x0	vop_standby_en LCDC standby mode Writing "1" to turn LCDC into standby mode, All the layer would disable and the data transfer from frame buffer memory would stop at the end of current frame. The output would be blank. When writing "0" to this bit, standby mode would disable and the LCDC go back to work immediately. 1'b0 : disable 1'b1 : enable * Black display is recommended before setting standby mode enable.

Bit	Attr	Reset Value	Description
21	RW	0x0	vop_dma_stop VOP DMA stop mode 1'b0 : disable 1'b1 : enable * If DMA is working, the stop mode would not be active until current bus transfer is finished.
20	RW	0x0	vop_field_tve_timing_pol
19	RW	0x0	win23_pri_opt_mode 1'b0: win2 win3 dma priority enalbe 1'b1: win2 win3 dma priority disable
18	RW	0x0	post_lb_mode 1'b0 : 4x4096 1'b1 : 8x2048
17	RO	0x0	reserved
16	RW	0x0	overlay_mode 1'b0: RGB overlay 1'b1: YUV overlay
15	RW	0x0	mipi_out_en 1'b0 : gating output clk ,data and control signal 1'b1 : mipi interface enable
14	RW	0x0	edp_out_en 1'b0 : gating output clk ,data and control signal 1'b1 : edp interface enable
13	RW	0x0	hdmi_out_en 1'b0 : gating output clk ,data and control signal 1'b1 : hdmi interface enable
12	RW	0x1	rgb_out_en 1'b0 : gating output clk ,data and control signal 1'b1 : rgb/lvds interface enable
11	RW	0x1	dp_out_en 1'b0 : gating output clk ,data and control signal 1'b1 : dp interface enable
10	RW	0x0	edpi_wms_fs edpi wms mode ， frame st signal write "1": edpi_wms_mode frame start (when other register is config done) read : wms mode hold status
9	RW	0x0	edpi_wms_mode 1'b1: mipi command mode
8	RW	0x0	edpi_halt_en mipi flow ctrl enable
7:3	RO	0x0	reserved

Bit	Attr	Reset Value	Description
2:1	RW	0x0	direct_path_layer_sel direct path layer select 2'b00 : select win0 2'b01 : select win1 2'b10 : select win2 2'b11 : select win3
0	RW	0x0	direct_path_en iep direct path enable signal 1'b0 : disable iep direct path 1'b1 : enable iep direct path

VOP_SYS_CTRL1
Address: Operational Base + offset (0x000c)
System control register1

Bit	Attr	Reset Value	Description
31	RW	0x0	dsp_fp_standby
30:25	RO	0x0	reserved
24	RW	0x0	reg_done_frm 1'b0: every frame valid 1'b1: every field valid
23:22	RW	0x0	noc_hurry_w_value 2'b00: low priority 2'b11: high priority
21:20	RW	0x0	noc_hurry_w_mode 2'b00: noc_hurry_w disable 2'b01: left 1/4 fifo empty 2'b10: left 1/2 fifo empty 2'b11: left 3/4 fifo empty
19:18	RO	0x0	reserved
17:13	RW	0x1d	axi_outstanding_max_num axi bus max outstanding number
12	RW	0x0	axi_max_outstanding_en axi bus max outstanding enable
11:10	RW	0x0	noc_win_qos Noc win qos
9	RW	0x0	noc_qos_en Noc qos enable
8:3	RW	0x00	noc_hurry_threshold Noc hurry threshold value
2:1	RW	0x0	noc_hurry_value Noc hurry value
0	RW	0x0	noc_hurry_en Noc hurry enable

VOP_DSP_CTRL0
Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31	RO	0x0	dsp_field
30:26	RO	0x0	reserved
25	RW	0x0	sw_tve_output_sel
24	RO	0x0	reserved
23	RW	0x0	dsp_y_mir_en 1'b0 : no y_mirror 1'b1 : y_mirror
22	RW	0x0	dsp_x_mir_en 1'b0 : no x_mirror 1'b1 : x_mirror
21	RW	0x0	dsp_yuv_clip YCrCb clip 1'b0 : disable, YCbCr no clip 1'b1 : enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
20	RW	0x0	dsp_ccir656_avg Cb-Cr filter in CCIR656 mode 1'b0 : drop mode 1'b1 : average mode
19	RW	0x0	dsp_black_en Black display mode When this bit enable, the pixel data output is all black (0x000000)
18	RW	0x0	dsp_blank_en Blank display mode When this bit enable, the Hsync/Vsync/Den output is blank
17	RW	0x0	dsp_out_zero Hsync/Vsync/Den output software ctrl 1'b0 : normal output 1'b1 : all output '0'
16	RW	0x0	dsp_dummy_swap Display dummy swap enable 1'b0 : B+G+R+dummy 1'b1 : dummy+B+G+R
15	RW	0x0	dsp_delta_swap Display delta swap enable 1'b0 : disable 1'b1 : enable *See detail description in Delta display charpter.

Bit	Attr	Reset Value	Description
14	RW	0x0	dsp_rg_swap Display output red and green swap enable 1'b0 : RGB 1'b1 : GRB
13	RW	0x0	dsp_rb_swap Display output red and blue swap enable 1'b0 : RGB 1'b1 : BGR
12	RW	0x0	dsp_bg_swap Display output blue and green swap enable 1'b0 : RGB 1'b1 : RBG
11	RW	0x0	dsp_field_pol field polarity when interlace dsp 1'b0 : normal 1'b1 : invert
10	RW	0x0	dsp_interlace Interlace display enable 1'b0 : disable 1'b1 : enable *This mode is related to the ITU-R656 output, the display timing of odd field must be set correctly. (lcdc_dsp_vs_st_end_f1/lcdc_dsp_vact_end_f1)
9	RW	0x0	dsp_ddr_phase dclk phase lock 1'b0 : no lock 1'b1 : lock every line
8	RW	0x0	dsp_dclk_ddr dclk output mode 1'b0 : SDR 1'b1 : DDR
7:6	RO	0x0	reserved
5	RW	0x0	p2i_en
4	RW	0x0	sw_core_dclk_sel 1'b0: dclk_core sel dclk 1'b1: dclk_core sel dclk div2

Bit	Attr	Reset Value	Description
3:0	RW	0x0	dsp_out_mode Display output format 4'b0000: Parallel 24-bit RGB888 output R[7:0],G[7:0],B[7:0] 4'b0001: Parallel 18-bit RGB666 output 6'b0,R[5:0],G[5:0],B[5:0] 4'b0010: Parallel 16-bit RGB565 output 8'b0,R[4:0],G[5:0],B[4:0] 4'b0011: Parallel 24-bit RGB888 double pixel mix out phase0:G1[3:0],B1[7:0],G0[3:0],B0[7:0] phase1:R1[7:0],G1[7:4],R0[7:0],G0[7:4] 4'b0100: Serial 2x12-bit 12'b0,G[3:0],B[7:0] + 12'b0,R[7:0],G[7:4] 4'b0101: ITU-656 output mode0 16'b0,pixel_data[7:0] 4'b0110: ITU-656 output mode1 8'b0,pixel_data[7:0],8'b0 4'b0111: ITU-656 output mode2 9'b0,pixel_data[7:0],7'b0 4'b1000: Serial 3x8-bit RGB888 16'b0, B[7:0]+16'b0,G[7:0]+16'b0,R[7:0] 4'b1100: Serial 3x8-bit RGB888 + dummy 16'b0, B[7:0]+16'b0,G[7:0]+16'b0,R[7:0] + dummy 4'b1110: YUV420 output for HDMI 4'b1100: DP_YUV422 4'b1101: DP_YUV420 4'b1111: Parallel 30-bit RGBaaa output R[9:0],G[9:0],B[9:0] Others: Reserved.

VOP_DSP_CTRL1
Address: Operational Base + offset (0x0014)
Display control register1

Bit	Attr	Reset Value	Description
31	RW	0x0	mipi_dclk_pol DCLK invert enable 1'b0 : normal 1'b1 : invert default dclk invert
30	RW	0x0	mipi_den_pol DEN polarity 1'b0 : positive 1'b1 : negative

Bit	Attr	Reset Value	Description
29	RW	0x0	mipi_vsync_pol VSYNC polarity 1'b0 : negative 1'b1 : positive
28	RW	0x0	mipi_hsync_pol HSYNC polarity 1'b0 : negative 1'b1 : positive
27	RW	0x0	edp_dclk_pol DCLK invert enable 1'b0 : normal 1'b1 : invert default dclk invert
26	RW	0x0	edp_den_pol DEN polarity 1'b0 : positive 1'b1 : negative
25	RW	0x0	edp_vsync_pol VSYNC polarity 1'b0 : negative 1'b1 : positive
24	RW	0x0	edp_hsync_pol HSYNC polarity 1'b0 : negative 1'b1 : positive
23	RW	0x0	hdmi_dclk_pol DCLK invert enable 1'b0 : normal 1'b1 : invert default dclk invert
22	RW	0x0	hdmi_den_pol DEN polarity 1'b0 : positive 1'b1 : negative
21	RW	0x0	hdmi_vsync_pol VSYNC polarity 1'b0 : negative 1'b1 : positive
20	RW	0x0	hdmi_hsync_pol HSYNC polarity 1'b0 : negative 1'b1 : positive

Bit	Attr	Reset Value	Description
19	RW	0x0	dp_lvds_dclk_pol DCLK invert enable 1'b0 : normal 1'b1 : invert default dclk invert
18	RW	0x0	dp_lvds_den_pol DEN polarity 1'b0 : positive 1'b1 : negative
17	RW	0x0	dp_lvds_vsync_pol VSYNC polarity 1'b0 : negative 1'b1 : positive
16	RW	0x0	dp_lvds_hsync_pol HSYNC polarity 1'b0 : negative 1'b1 : positive
15:14	RW	0x3	dsp_layer3_sel layer3 selection
13:12	RW	0x2	dsp_layer2_sel layer2 selection
11:10	RW	0x1	dsp_layer1_sel layer1 selection
9:8	RW	0x0	dsp_layer0_sel layer0 selection
7	RW	0x0	update_gamma_lut 1'b0:no update gamma_lut 1'b1:update gamma_lut
6	RW	0x0	dither_up_en 1'b0 : no dither up 1'b1 : rgb565 dither up to rgb888
5	RO	0x0	reserved
4	RW	0x0	dither_down_sel dither down mode select 2'b0 : allegro 2'b1 : FRC
3	RW	0x0	dither_down_mode Dither-down mode 1'b0 : RGB888 to RGB565 1'b1 : RGB888 to RGB666
2	RW	0x0	dither_down_en Dither-down enable 1'b0 : disable 1'b1 : enable

Bit	Attr	Reset Value	Description
1	RW	0x0	pre_dither_down_en 10bit -> 8bit (allegro)
0	RW	0x0	dsp_lut_en Display LUT ram enable 1'b0 : disable 1'b1 : enable *This bit should be "0" when CPU updates the LUT, and should be "1" when Display LUT mode enable.

VOP_DSP_BG
Address: Operational Base + offset (0x0018)
Background color

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	dsp_bg_red Background Red color 8bit red color
15:8	RW	0x00	dsp_bg_green Background Green color 8bit green color
7:0	RW	0x00	dsp_bg_blue Background Blue color 8bit blue color

VOP_MCU_CTRL
Address: Operational Base + offset (0x001c)
MCU mode control register

Bit	Attr	Reset Value	Description
31	RW	0x0	mcu_type MCU LCD output SELECT
30	RW	0x0	mcu_bypass MCU LCD BYPASS MODE Select
29	RW	0x0	mcu_rs MCU LCD RS Select
28	W1C	0x0	mcu_frame_st Write"1" : MCU HOLD Mode Frame Start Read : MCU/LCDC standby HOLD status
27	RW	0x0	mcu_hold_mode MCU HOLD Mode Select
26	RW	0x0	mcu_clk_sel MCU_CLK_SEL for MCU bypass 1'b1 : MCU BYPASS sync with DCLK 1'b0 : MCU BYPASS sync with HCLK
25:20	RW	0x07	mcu_rw_pend MCU_RW signal end point (0-63)

Bit	Attr	Reset Value	Description
19:16	RW	0x1	mcu_rw_pst MCU_RW signal start point (0-15)
15:10	RW	0x07	mcu_cs_pend MCU_CS signal end point (0-63)
9:6	RW	0x0	mcu_cs_pst MCU_CS signal start point (0-15)
5:0	RW	0x08	mcu_pix_total MCU LCD Interface writing period (1-63)

VOP_WB_CTRL0
Address: Operational Base + offset (0x0020)
write back ctrl0

Bit	Attr	Reset Value	Description
31:28	RW	0xe	wb_uv_id axi bus write back yrgb id use default 0xe.
27:24	RW	0xd	wb_yrgb_id axi bus write back yrgb id use default 0xd.
23:12	RO	0x0	reserved
11	RW	0x0	wb_handshake_mode 1'b0 : full handshake 1'b1 : half handshake
10	RO	0x0	reserved
9	RW	0x0	wb_ythrow_mode 1'b0 : throw odd line 1'b1 : throw even line
8	RW	0x0	wb_ythrow_en write back y direction throw line enable 1'b0 : disable 1'b1 : enable
7	RW	0x0	wb_xpsd_bil_en write back X direction bilinear scale enable 1'b0 : enable scale 1'b1 : disable scale
6	RW	0x0	wb_rgb2yuv_mode write back rgb to yuv mode 1'b0 : BT601 1'b1 : BT709
5	RW	0x0	wb_rgb2yuv_en write back rgb to yuv enable 1'b0 : disable 1'b1 : enable

Bit	Attr	Reset Value	Description
4	RW	0x0	wb_dither_en write back dither enable when wb_fmt is RGB565. 1'b0 : no dither ,RGB888 clip to RGB565 1'b1 : with dither,RGB888 dither to RGB565
3:1	RW	0x0	wb_fmt write back format 3'b000 : ARGB888 3'b001 : RGB888 3'b010 : RGB565 3'b100 : YcbCr420 other : reserved
0	RW	0x0	wb_en write back enable 1'b0 : disable 1'b1 : enable

VOP_WB_CTRL1
Address: Operational Base + offset (0x0024)
write back ctrl1

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	wb_xpsd_bil_factor factor=((src_width[11:0])/(dst_width[11:0]))*2^12
15:0	RO	0x0	reserved

VOP_WB_YRGB_MST
Address: Operational Base + offset (0x0028)
write back yrgb mst

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wb_yrgb_mst YRGB mst address

VOP_WB_CBR_MST
Address: Operational Base + offset (0x002c)
write back cbr mst

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wb_cbr_mst CBR mst adress

VOP_WIN0_CTRL0
Address: Operational Base + offset (0x0030)
Win0 ctrl register0

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:30	RW	0x0	win0_dma_burst_length WIN0 DMA read Burst length 2'b00 : burst16 (burst 15 in rgb888 pack mode) 2'b01 : burst8 (burst 12 in rgb888 pack mode) 2'b10 : burst4 (burst 6 in rgb888 pack mode) 2'b11 : reserved
29:25	RW	0x1d	win0_axi_outstanding_max_num win0 out standing max number
24	RW	0x0	win0_axi_max_outstanding_en 1'b0 : disable 1'b1 : enable
23	RO	0x0	reserved
22	RW	0x0	win0_y_mir_en 1'b0 : no y_mirror 1'b1 : y_mirror
21	RW	0x0	win0_x_mir_en 1'b0 : no x_mirror 1'b1 : x_mirror
20	RW	0x0	win0_yuv_clip YCrCb clip 1'b0 : disable, YCbCr no clip 1'b1 : enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
19	RW	0x0	win0_cbr_deflick Win0 Cbr deflick mode 1'b0 : disable 1'b1 : enable
18	RW	0x0	win0_yrgb_deflick win0 YRGB deflick mode 1'b0 : disable 1'b1 : enable
17	RW	0x0	win0_yuyv win0_data_fmt[3]
16	RW	0x0	win0_hw_pre_mul_en 1'b0: no hardware pre multiply mode 1'b1: hardware pre multiply mode
15	RW	0x0	win0_uv_swap Win0 CbCr swap 1'b0 : CrCb 1'b1 : CbCr
14	RW	0x0	win0_mid_swap Win0 Y middle swap 1'b0 : Y3Y2Y1Y0 1'b1 : Y3Y1Y2Y0

Bit	Attr	Reset Value	Description
13	RW	0x0	win0_alpha_swap win0 alpha swap 1'b0 : ARGB 1'b1 : RGBA
12	RW	0x0	win0_rb_swap win0 RGB RED and BLUE swap 1'b0 : RGB 1'b1 : BGR
11:10	RW	0x0	win0_csc_mode Win0 YUV2RGB or RGB2YUV Color space conversion(YUV2RGB): 2'b00 : mpeg 2'b01 : jpeg 2'b10 : hd 2'b11 : mpeg Color space conversion(RGB2YUV): 2'bx0: BT601 2'bx1: BT709
9	RW	0x0	win0_no_outstanding win0 AXI master read outstanding 1'b0 : enable 1'b1 : disable
8	RW	0x0	win0_interlace_read Win0 interlace read mode 1'b0 : disable 1'b1 : enable
7:5	RW	0x2	win0_lb_mode win0 line buffer mode,calc by driver.
4	RW	0x0	win0_fmt_10 0: yuv 8bit fmt mode 1: yuv 10bit fmt mode
3:1	RW	0x0	win0_data_fmt vld_reg 4'b0000 : ARGB888 4'b0001 : RGB888 4'b0010 : RGB565 4'b0100 : YcbCr420 4'b0101 : YcbCr422 4'b0110 : YcbCr444 4'b1000: YCrYCb422 4'b1001: YCrYCb420 4'b1010: CrYCbY422 4'b1011: CrYCbY420

Bit	Attr	Reset Value	Description
0	RW	0x0	win0_en 1'b0 : disable 1'b1 : enable

VOP_WIN0_CTRL1
Address: Operational Base + offset (0x0034)
Win0 ctrl register1

Bit	Attr	Reset Value	Description
31	RW	0x0	win0_cbr_vsd_mode win0 vertical scaler down mode select 1'b0 : bilinear 1'b1 : average
30	RW	0x0	win0_cbr_vsu_mode win0 vertical scaler down mode select 1'b0 : bilinear 1'b1 : bicubic
29:28	RW	0x0	win0_cbr_hsd_mode win0 horizontal scaler down mode select 2'b00 : bilinear 2'b01 : bicubic 2'b10 : average
27:26	RW	0x0	win0_cbr_ver_scl_mode 2'b00 : no scale 2'b01 : scale up 2'b10 : scale down 2'b11 : no scale
25:24	RW	0x0	win0_cbr_hor_scl_mode 2'b00 : no scale 2'b01 : scale up 2'b10 : scale down 2'b11 : no scale
23	RW	0x0	win0_yrgb_vsd_mode win0 vertical scaler down mode select 1'b0 : bilinear 1'b1 : average
22	RW	0x0	win0_yrgb_vsu_mode win0 vertical scaler down mode select 1'b0 : bilinear 1'b1 : bicubic
21:20	RW	0x0	win0_yrgb_hsd_mode win0 horizontal scaler down mode select 2'b00 : bilinear 2'b01 : average

Bit	Attr	Reset Value	Description
19:18	RW	0x0	win0_yrgb_ver_scl_mode 2'b00 : no scale 2'b01 : scale up 2'b10 : scale down 2'b11 : no scale
17:16	RW	0x0	win0_yrgb_hor_scl_mode 2'b00 : no scale 2'b01 : scale up 2'b10 : scale down 2'b11 : no scale
15	RW	0x0	win0_line_load_mode when yuv fmt, 1'b0: load data by axi trans 1'b1: load data by lines
14:12	RW	0x0	win0_cbr_axi_gather_num win0 axi cbr data transfer gather number
11:8	RW	0x0	win0_yrgb_axi_gather_num win0 axi yrgb data transfer gather number
7	RW	0x0	win0_vsd_cbr_gt2 cbr_src/cbr_dst >= 2
6	RW	0x0	win0_vsd_cbr_gt4 cbr_src/cbr_dst >= 4
5	RW	0x0	win0_vsd_yrgb_gt2 yrgb_src/yrgb_dst >= 2
4	RW	0x0	win0_vsd_yrgb_gt4 yrgb_src/yrgb_dst >= 4
3:2	RW	0x0	win0_bic_coe_sel 2'b00 : PRECISE 2'b01 : SPLINE 2'b10 : CATROM 2'b11 : MITCHELL
1	RW	0x0	win0_cbr_axi_gather_en win0 axi bus cbr data gather transfer enable
0	RW	0x0	win0_yrgb_axi_gather_en win0 axi bus yrgb data gather transfer enable

VOP_WIN0_COLOR_KEY

Address: Operational Base + offset (0x0038)

Win0 color key register

Bit	Attr	Reset Value	Description
31	RW	0x0	win0_key_en Win0 transparency color key enable 1'b0 : disable; 1'b1 : enable;
30:24	RO	0x0	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0x000000	win0_key_color Win0 key color 24 bit RGB888

VOP_WIN0_VIR
Address: Operational Base + offset (0x003c)
Win0 virtual stride

Bit	Attr	Reset Value	Description
31:16	RW	0x0140	win0_vir_stride_uv Number of words of Win0 uv Virtual width
15:0	RW	0x0140	win0_vir_stride Win0 Virtual stride Number of words of Win0 yrgb Virtual width ARGB888 : win0_vir_width RGB888 : (win0_vir_width*3/4) + (win0_vir_width%3) RGB565 : ceil(win0_vir_width/2) YUV : ceil(win0_vir_width/4)

VOP_WIN0_YRGB_MST
Address: Operational Base + offset (0x0040)
Win0 YRGB memory start address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win0_yrgb_mst win0 YRGB frame buffer memory start address

VOP_WIN0_CBR_MST
Address: Operational Base + offset (0x0044)
Win0 Cbr memory start address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win0_cbr_mst win0 CBR frame buffer memory start address

VOP_WIN0_ACT_INFO
Address: Operational Base + offset (0x0048)
Win0 active window width/height

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x00ef	win0_act_height Win0 active(original) window height win_act_height = (win0 vertical size -1)
15:13	RO	0x0	reserved
12:0	RW	0x013f	win0_act_width Win0 active(original) window width win_act_width = (win0 horizontial size -1)

VOP_WIN0_DSP_INFO
Address: Operational Base + offset (0x004c)
Win0 display width/height on panel

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0ef	win0_dsp_height Win0 display window height win0_dsp_height = (win0 vertical size -1)
15:12	RO	0x0	reserved
11:0	RW	0x13f	win0_dsp_width Win0 display window width win0_dsp_width = (win0 horizontial size -1)

VOP_WIN0_DSP_ST
Address: Operational Base + offset (0x0050)
Win0 display start point on panel

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	win0_dsp_yst Win0 vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x000a	win0_dsp_xst Win0 horizontal start point(x) of the Panel scanning

VOP_WIN0_SCL_FACTOR_YRGB
Address: Operational Base + offset (0x0054)
Win0 YRGB scaling factor

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	win0_vs_factor_yrgb Win0 YRGB vertical scaling factor: factor=((LCDC_WIN0_ACT_INFO[31:16]) /(LCDC_WIN0_DSP_INFO[31:16]))*2^12
15:0	RW	0x1000	win0_hs_factor_yrgb Win0 YRGB horizontal scaling factor: factor=((LCDC_WIN0_ACT_INFO[15:0]) /(LCDC_WIN0_DSP_INFO[15:0]))*2^12

VOP_WIN0_SCL_FACTOR_CBR
Address: Operational Base + offset (0x0058)
Win0 Cbr scaling factor

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	win0_vs_factor_cbr Win0 CBR vertical scaling factor: YCbCr420: factor=((LCDC_WIN0_ACT_INFO[31:16]/ 2) /(LCDC_WIN0_DSP_INFO[31:16]))*2^12 YCbCr422,YCbCr444: factor=((LCDC_WIN0_ACT_INFO[31:16]) /(LCDC_WIN0_DSP_INFO[31:16]))*2^12
15:0	RW	0x1000	win0_hs_factor_cbr Win0 CBR horizontal scaling factor: YCbCr422,YCbCr420: factor=((LCDC_WIN0_ACT_INFO[15:0]/2) /(LCDC_WIN0_DSP_INFO[15:0]))*2^12 YCbCr444: factor=((LCDC_WIN0_ACT_INFO[15:0]) /(LCDC_WIN0_DSP_INFO[15:0]))*2^12

VOP_WIN0_SCL_OFFSET
Address: Operational Base + offset (0x005c)
Win0 scaling start point offset

Bit	Attr	Reset Value	Description
31:24	RW	0x00	win0_vs_offset_cbr Cbr Vertical scaling start point offset (0x00~0xff)/0x100 = 0~0.99
23:16	RW	0x00	win0_vs_offset_yrgb Y Vertical scaling start point offset (0x00~0xff)/0x100 = 0~0.99
15:8	RW	0x00	win0_hs_offset_cbr Cbr Horizontal scaling start point offset (0x00~0xff)/0x100 = 0~0.99
7:0	RW	0x00	win0_hs_offset_yrgb Y Horizontal scaling start point offset (0x00~0xff)/0x100 = 0~0.99

VOP_WIN0_SRC_ALPHA_CTRL
Address: Operational Base + offset (0x0060)
Win0 alpha source control register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	win0_fading_value win0 fading value ,8bits
23:16	RW	0x00	win0_src_global_alpha src global alpha
15:9	RO	0x0	reserved
8:6	RW	0x0	win0_src_factor_mode src factor mode

Bit	Attr	Reset Value	Description
5	RW	0x0	win0_src_alpha_cal_mode src alpha calc mode
4:3	RW	0x0	win0_src_blend_mode src blend mode
2	RW	0x0	win0_src_alpha_mode src alpha mode
1	RW	0x0	win0_src_color_mode src color mode
0	RW	0x0	win0_src_alpha_en src alpha en

VOP_WIN0_DST_ALPHA_CTRL
Address: Operational Base + offset (0x0064)
Win0 alpha destination control register

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:6	RW	0x0	win0_dst_factor_mode dst factor mode
5:0	RW	0x00	win0_dst_m0_reserved reserved

VOP_WIN0_FADING_CTRL
Address: Operational Base + offset (0x0068)
Win0 fading contrl register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	layer0_fading_en fading enable
23:16	RW	0x00	layer0_fading_offset_b fading offset blue value
15:8	RW	0x00	layer0_fading_offset_g fading offset green value
7:0	RW	0x00	layer0_fading_offset_r fading offset red value

VOP_WIN0_CTRL2
Address: Operational Base + offset (0x006c)
Win0 ctrl register2

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x2	win_rid_win0_cbr axi read id of win0 cbr channel
3:0	RW	0x1	win_rid_win0_yrgb axi read id of win0 yrgb channel

VOP_WIN1_CTRL0
Address: Operational Base + offset (0x0070)
Win1 ctrl register0

Bit	Attr	Reset Value	Description
31:30	RW	0x0	win1_dma_burst_length WIN1 DMA read Burst length 2'b00 : burst16 (burst 15 in rgb888 pack mode) 2'b01 : burst8 (burst 12 in rgb888 pack mode) 2'b10 : burst4 (burst 6 in rgb888 pack mode) 2'b11 : reserved
29:25	RW	0x1d	win1_axi_max_outstanding_num win1 out standing max number
24	RW	0x0	win1_axi_max_outstanding_en 1'b0 : disable 1'b1 : enable
23	RO	0x0	reserved
22	RW	0x0	win1_y_mir_en 1'b0 : no y_mirror 1'b1 : y_mirror
21	RW	0x0	win1_x_mir_en 1'b0 : no x_mirror 1'b1 : x_mirror
20	RW	0x0	win1_yuv_clip YCrCb clip 1'b0 : disable, YCbCr no clip 1'b1 : enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
19	RW	0x0	win1_cbr_deflick Win1 Cbr deflick mode 1'b0 : disable 1'b1 : enable
18	RW	0x0	win1_yrgb_deflick win1 YRGB deflick mode 1'b0 : disable 1'b1 : enable
17	RW	0x0	win1_yuyv win1_data_fmt[3]
16	RW	0x0	win1_hw_pre_mul_en 1'b0: no hardware pre multiply mode 1'b1: hardware pre multiply mode
15	RW	0x0	win1_uv_swap Win1 CbCr swap 1'b0 : CrCb 1'b1 : CbCr

Bit	Attr	Reset Value	Description
14	RW	0x0	win1_mid_swap Win1 Y middle 8-bit swap 1'b0 : Y3Y2Y1Y0 1'b1 : Y3Y1Y2Y0
13	RW	0x0	win1_alpha_swap win1 alpha swap 1'b0 : ARGB 1'b1 : RGBA
12	RW	0x0	win1_rb_swap win1 RGB RED and BLUE swap 1'b0 : RGB 1'b1 : BGR
11:10	RW	0x0	win1_csc_mode Win1 YUV2RGB or RGB2YUV Color space conversion(YUV2RGB): 2'b00 : mpeg 2'b01 : jpeg 2'b10 : hd 2'b11 : mpeg Color space conversion(RGB2YUV): 2'bx0: BT601 2'bx1: BT709
9	RW	0x0	win1_no_outstanding win1 AXI master read outstanding 1'b0 : enable 1'b1 : disable
8	RW	0x0	win1_interlace_read Win1 interlace read mode 1'b0 : disable 1'b1 : enable
7:5	RW	0x2	win1_lb_mode win1 line buffer mode,calc by driver.
4	RW	0x0	win1_fmt_10 1'b0: yuv 8bit fmt mode 1'b1: yuv 10bit fmt mode
3:1	RW	0x0	win1_data_fmt 3'b000 : ARGB888 3'b001 : RGB888 3'b010 : RGB565 3'b100 : YcbCr420 3'b101 : YcbCr422 3'b110 : YcbCr444
0	RW	0x0	win1_en 1'b0 : disable 1'b1 : enable

VOP_WIN1_CTRL1
Address: Operational Base + offset (0x0074)
Win1 ctrl register1

Bit	Attr	Reset Value	Description
31	RW	0x0	win1_cbr_vsd_mode win1 vertical scaler down mode select 1'b0 : bilinear 1'b1 : average
30	RW	0x0	win1_cbr_vsu_mode win1 vertical scaler up mode select 1'b0 : bilinear 1'b1 : bicubic
29:28	RW	0x0	win1_cbr_hsd_mode win1 horizontal scaler down mode select 2'b00 : bilinear 2'b01 : bicubic 2'b10 : average
27:26	RW	0x0	win1_cbr_ver_scl_mode 2'b00 : no scale 2'b01 : scale up 2'b10 : scale down 2'b11 : no scale
25:24	RW	0x0	win1_cbr_hor_scl_mode 2'b00 : no scale 2'b01 : scale up 2'b10 : scale down 2'b11 : no scale
23	RW	0x0	win1_yrgb_vsd_mode win1 vertical scaler down mode select 1'b0 : bilinear 1'b1 : average
22	RW	0x0	win1_yrgb_vsu_mode win1 vertical scaler up mode select 1'b0 : bilinear 1'b1 : bicubic
21:20	RW	0x0	win1_yrgb_hsd_mode win1 horizontal scaler down mode select 2'b00 : bilinear 2'b01 : average
19:18	RW	0x0	win1_yrgb_ver_scl_mode 2'b00 : no scale 2'b01 : scale up 2'b10 : scale down 2'b11 : no scale

Bit	Attr	Reset Value	Description
17:16	RW	0x0	win1_yrgb_hor_scl_mode 2'b00 : no scale 2'b01 : scale up 2'b10 : scale down 2'b11 : no scale
15	RW	0x0	win1_line_load_mode when yuv fmt, 1'b0: load data by pixels 1'b1: load data by lines
14:12	RW	0x0	win1_cbr_axi_gather_num win1 axi cbr data transfer gather number
11:8	RW	0x0	win1_yrgb_axi_gather_num win1 axi yrgb data transfer gather number
7	RW	0x0	win1_vsd_cbr_gt2 cbr_src/cbr_dst >= 2
6	RW	0x0	win1_vsd_cbr_gt4 cbr_src/cbr_dst >= 4
5	RW	0x0	win1_vsd_yrgb_gt2 yrgb_src/yrgb_dst >= 2
4	RW	0x0	win1_vsd_yrgb_gt4 yrgb_src/yrgb_dst >= 4
3:2	RW	0x0	win1_bic_coe_sel 2'b00 : PRECISE 2'b01 : SPLINE 2'b10 : CATROM 2'b11 : MITCHELL
1	RW	0x0	win1_cbr_axi_gather_en win1 cbr axi bus gather enable
0	RW	0x0	win1_yrgb_axi_gather_en win1 yrgb axi bus gather enable

VOP_WIN1_COLOR_KEY
Address: Operational Base + offset (0x0078)
Win1 color key register

Bit	Attr	Reset Value	Description
31	RW	0x0	win1_key_en Win1 transparency color key enable 1'b0 : disable; 1'b1 : enable;
30:24	RO	0x0	reserved
23:0	RW	0x000000	win1_key_color Win1 key color 24 bit RGB888

VOP_WIN1_VIR

Address: Operational Base + offset (0x007c)
win1 virtual stride

Bit	Attr	Reset Value	Description
31:16	RW	0x0140	win1_vir_stride_uv Number of words of Win1 uv Virtual width
15:0	RW	0x0140	win1_vir_stride Win1 Virtual stride Number of words of Win1 yrgb Virtual width ARGB888 : win1_vir_width RGB888 : (win1_vir_width*3/4) + (win1_vir_width%3) RGB565 : ceil(win1_vir_width/2) YUV : ceil(win1_vir_width/4)

VOP_WIN1_YRGB_MST
Address: Operational Base + offset (0x0080)
Win1 YRGB memory start address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win1_yrgb_mst win1 YRGB frame buffer memory start address

VOP_WIN1_CBR_MST
Address: Operational Base + offset (0x0084)
Win1 Cbr memory start address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win1_cbr_mst win1 CBR frame buffer memory start address

VOP_WIN1_ACT_INFO
Address: Operational Base + offset (0x0088)
Win1 active window width/height

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x00ef	win1_act_height Win1 active(original) window height win_act_height = (win1 vertical size -1)
15:13	RO	0x0	reserved
12:0	RW	0x013f	win1_act_width Win1 active(original) window width win_act_width = (win1 horizontial size -1)

VOP_WIN1_DSP_INFO
Address: Operational Base + offset (0x008c)
Win1 display width/height on panel

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27:16	RW	0x0ef	win1_dsp_height Win1 display window height win1_dsp_height = (win1 vertical size -1)
15:12	RO	0x0	reserved
11:0	RW	0x13f	win1_dsp_width Win1 display window width win1_dsp_width = (win1 horizontial size -1)

VOP_WIN1_DSP_ST
Address: Operational Base + offset (0x0090)
Win1 display start point on panel

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	win1_dsp_yst Win1 vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x000a	win1_dsp_xst Win1 horizontal start point(x) of the Panel scanning

VOP_WIN1_SCL_FACTOR_YRGB
Address: Operational Base + offset (0x0094)
Win1 YRGB scaling factor

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	win1_vs_factor_yrgb Win1 YRGB vertical scaling factor: factor=((LCDC_WIN1_ACT_INFO[31:16]) /(LCDC_WIN1_DSP_INFO[31:16]))*2^12
15:0	RW	0x1000	win1_hs_factor_yrgb Win1 YRGB horizontal scaling factor: factor=((LCDC_WIN1_ACT_INFO[15:0]) /(LCDC_WIN1_DSP_INFO[15:0]))*2^12

VOP_WIN1_SCL_FACTOR_CBR
Address: Operational Base + offset (0x0098)
Win1 Cbr scaling factor

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	win1_vs_factor_cbr Win1 CBR vertical scaling factor: YCbCr420: factor=((LCDC_WIN1_ACT_INFO[31:16]/ 2) /(LCDC_WIN1_DSP_INFO[31:16]))*2^12 YCbCr422,YCbCr444: factor=((LCDC_WIN1_ACT_INFO[31:16]) /(LCDC_WIN1_DSP_INFO[31:16]))*2^12

Bit	Attr	Reset Value	Description
15:0	RW	0x1000	win1_hs_factor_cbr Win1 Cbr horizontal scaling factor: YCbCr422,YCbCr420: factor=((LCDC_WIN1_ACT_INFO[15:0]/2) /(LCDC_WIN1_DSP_INFO[15:0]))*2^12 YCbCr444: factor=((LCDC_WIN1_ACT_INFO[15:0]) /(LCDC_WIN1_DSP_INFO[15:0]))*2^12

VOP_WIN1_SCL_OFFSET
Address: Operational Base + offset (0x009c)
Win1 scaling start point offset

Bit	Attr	Reset Value	Description
31:24	RW	0x00	win1_vs_offset_cbr Cbr Vertical scaling start point offset (0x00~0xff)/0x100 = 0~0.99
23:16	RW	0x00	win1_vs_offset_yrgb Y Vertical scaling start point offset (0x00~0xff)/0x100 = 0~0.99
15:8	RW	0x00	win1_hs_offset_cbr Cbr Horizontal scaling start point offset (0x00~0xff)/0x100 = 0~0.99
7:0	RW	0x00	win1_hs_offset_yrgb Y Horizontal scaling start point offset (0x00~0xff)/0x100 = 0~0.99

VOP_WIN1_SRC_ALPHA_CTRL
Address: Operational Base + offset (0x00a0)
Win1 alpha source control register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	win1_fading_value fading value,8bit
23:16	RW	0x00	win1_src_global_alpha src global alpha
15:9	RO	0x0	reserved
8:6	RW	0x0	win1_src_factor_mode src factor mode
5	RW	0x0	win1_src_alpha_cal_mode src alpha calc mode
4:3	RW	0x0	win1_src_blend_mode src blend mode
2	RW	0x0	win1_src_alpha_mode src alpha mode

Bit	Attr	Reset Value	Description
1	RW	0x0	win1_src_color_mode src color mode
0	RW	0x0	win1_src_alpha_en src alpha en

VOP_WIN1_DST_ALPHA_CTRL
Address: Operational Base + offset (0x00a4)
Win1 alpha destination control register

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:6	RW	0x0	win1_dst_factor_m0 dst factor mode
5:0	RW	0x00	win1_dsp_m0_reserved reserved

VOP_WIN1_FADING_CTRL
Address: Operational Base + offset (0x00a8)
Win1 fading contrl register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	win1_fading_en fading enable
23:16	RW	0x00	win1_fading_offset_b fading offset blue value
15:8	RW	0x00	win1_fading_offset_g fading offset green value
7:0	RW	0x00	win1_fading_offset_r fading offset red value

VOP_WIN1_CTRL2
Address: Operational Base + offset (0x00ac)
Win1 ctrl register2

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x4	win_rid_win1_cbr axi read id of win1 cbr channel
3:0	RW	0x3	win_rid_win1_yrgb axi read id of win1 yrgb channel

VOP_WIN2_CTRL0
Address: Operational Base + offset (0x00b0)
win2 ctrl register0

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31	RW	0x0	win2_endian_swap3 Win2 region3 8pp palette data Big-endian/ Little-endian select 1'b0 : Big-endian 1'b1 : Little-endian
30	RW	0x0	win2_alpha_swap3 Win2 region3 RGB alpha swap 1'b0 : ARGB 1'b1 : RGBA
29	RW	0x0	win2_rb_swap3 Win2 region3 RGB Red and Blue swap 1'b0 : RGB 1'b1 : BGR
28	RW	0x0	win2_endian_swap2 Win2 region2 8pp palette data Big-endian/ Little-endian select 1'b0 : Big-endian 1'b1 : Little-endian
27	RW	0x0	win2_alpha_swap2 Win2 region2 RGB alpha swap 1'b0 : ARGB 1'b1 : RGBA
26	RW	0x0	win2_rb_swap2 Win2 region2 RGB Red and Blue swap 1'b0 : RGB 1'b1 : BGR
25	RW	0x0	win2_endian_swap1 Win2 region1 8pp palette data Big-endian/ Little-endian select 1'b0 : Big-endian 1'b1 : Little-endian
24	RW	0x0	win2_alpha_swap1 Win2 region1 RGB alpha swap 1'b0 : ARGB 1'b1 : RGBA
23	RW	0x0	win2_rb_swap1 Win2 region1 RGB Red and Blue swap 1'b0 : RGB 1'b1 : BGR
22	RW	0x0	win2_endian_swap0 Win2 region0 8pp palette data Big-endian/ Little-endian select 1'b0 : Big-endian 1'b1 : Little-endian
21	RW	0x0	win2_alpha_swap0 Win2 region0 RGB alpha swap 1'b0 : ARGB 1'b1 : RGBA

Bit	Attr	Reset Value	Description
20	RW	0x0	win2_rb_swap0 Win2 region0 RGB Red and Blue swap 1'b0 : RGB 1'b1 : BGR
19	RO	0x0	reserved
18:17	RW	0x0	win2_data_fmt3 Win2 region 3 data format 2'b00 : ARGB888 2'b01 : RGB888 2'b10 : RGB565 2'b11 : 8bpp
16	RW	0x0	win2_mst3_en win2 master3 enable 1'b0 : disable 1'b1 : enable
15	RO	0x0	reserved
14:13	RW	0x0	win2_data_fmt2 Win2 region 2 data format 2'b00 : ARGB888 2'b01 : RGB888 2'b10 : RGB565 2'b11 : 8bpp
12	RW	0x0	win2_mst2_en win2 master2 enable 1'b0 : disable 1'b1 : enable
11	RO	0x0	reserved
10:9	RW	0x0	win2_data_fmt1 Win2 region 1 data format 2'b00 : ARGB888 2'b01 : RGB888 2'b10 : RGB565 2'b11 : 8bpp
8	RW	0x0	win2_mst1_en win2 master1 enable 1'b0 : disable 1'b1 : enable
7	RO	0x0	reserved
6:5	RW	0x0	win2_data_fmt0 Win2 region 0 data format 2'b00 : ARGB888 2'b01 : RGB888 2'b10 : RGB565 2'b11 : 8bpp

Bit	Attr	Reset Value	Description
4	RW	0x0	win2_mst0_en win2 master0 enable 1'b0 : disable 1'b1 : enable
3:2	RW	0x0	win2_csc_mode Win2 RGB2YUV conversion mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
1	RW	0x0	win2_interlace_read Win2 interlace read mode 1'b0 : disable 1'b1 : enable
0	RW	0x0	win2_en 1'b0 : disable 1'b1 : enable

VOP_WIN2_CTRL1
Address: Operational Base + offset (0x00b4)
win2 ctrl register1

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:20	RW	0x5	win_rid_win2 axi read id of win2 channel
19:17	RO	0x0	reserved
16	RW	0x0	win2_lut_en Win2 LUT ram enable 1'b0 : disable 1'b1 : enable *This bit should be "0" when CPU updates the LUT, and should be "1" when Win2 LUT mode enable.
15	RW	0x0	win2_y_mir_en 1'b0 : no y_mirror 1'b1 : y_mirror
14	RW	0x0	win2_no_outstanding Win2 AXI master read outstanding 1'b0 : enable 1'b1 : disable
13	RO	0x0	reserved
12:8	RW	0x1d	win2_axi_max_outstanding_num win2 axi max outstanding number
7:4	RW	0x0	win2_axi_gather_num win2 axi gather transfer number

Bit	Attr	Reset Value	Description
3:2	RW	0x0	win2_dma_burst_length WIN2 DMA read Burst length 2'b00 : burst16 (burst 15 in rgb888 pack mode) 2'b01 : burst8 (burst 12 in rgb888 pack mode) 2'b10 : burst4 (burst 6 in rgb888 pack mode) 2'b11 : reserved
1	RW	0x0	win2_axi_max_outstanding_en 1'b0 : disable 1'b1 : enable
0	RW	0x0	win2_axi_gather_en 1'b0 : disable 1'b1 : enable

VOP_WIN2_VIR0_1
Address: Operational Base + offset (0x00b8)
Win2 virtual stride0 and virtaul stride1

Bit	Attr	Reset Value	Description
31:16	RW	0x0140	win2_vir_stride1 Win2 Virtual stride1 Number of words of Win2 Virtual1 width ARGB888 : win2_vir_width1 RGB888 : (win2_vir_width1 * 3/4) + (win2_vir_width1 % 3) RGB565 : ceil(win2_vir_width1 / 2) 8BPP : ceil(win2_vir_width1 / 4) 4BPP : ceil(win2_vir_width1 / 8) 2BPP : ceil(win2_vir_width1 / 16) 1BPP : ceil(win2_vir_width1 / 32)
15:0	RW	0x0140	win2_vir_stride0 Win2 Virtual stride0 Number of words of Win2 Virtual0 width ARGB888 : win2_vir_width0 RGB888 : (win2_vir_width0 * 3/4) + (win2_vir_width0 % 3) RGB565 : ceil(win2_vir_width0 / 2) 8BPP : ceil(win2_vir_width0 / 4) 4BPP : ceil(win2_vir_width0 / 8) 2BPP : ceil(win2_vir_width0 / 16) 1BPP : ceil(win2_vir_width0 / 32)

VOP_WIN2_VIR2_3
Address: Operational Base + offset (0x00bc)
Win2 virtual stride2 and virtaul stride3

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0140	win2_vir_stride3 Win2 Virtual stride3 Number of words of Win2 Virtual3 width ARGB888 : win2_vir_width3 RGB888 : (win2_vir_width3 * 3/4) + (win2_vir_width3 % 3) RGB565 : ceil(win2_vir_width3 / 2) 8BPP : ceil(win2_vir_width3 / 4) 4BPP : ceil(win2_vir_width3 / 8) 2BPP : ceil(win2_vir_width3 / 16) 1BPP : ceil(win1_vir_width3 / 32)
15:0	RW	0x0140	win2_vir_stride2 Win2 Virtual stride2 Number of words of Win2 Virtual2 width ARGB888 : win2_vir_width2 RGB888 : (win2_vir_width2 * 3/4) + (win2_vir_width2 % 3) RGB565 : ceil(win2_vir_width2 / 2) 8BPP : ceil(win2_vir_width2 / 4) 4BPP : ceil(win2_vir_width2 / 8) 2BPP : ceil(win2_vir_width2 / 16) 1BPP : ceil(win1_vir_width2 / 32)

VOP_WIN2_MST0
Address: Operational Base + offset (0x00c0)
Win2 memory start address0

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win2_mst0 Win2 frame buffer memory start address0 *must be alianed to 8byte address

VOP_WIN2_DSP_INFO0
Address: Operational Base + offset (0x00c4)
Win2 display width0/height0 on panel

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0ef	win2_dsp_height0 Win2 display window height0 win2_dsp_height0 = size -1
15:12	RO	0x0	reserved
11:0	RW	0x13f	win2_dsp_width0 Win2 display window width0 win2_dsp_width = size -1

VOP_WIN2_DSP_ST0
Address: Operational Base + offset (0x00c8)
Win2 display start point0 on panel

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	win2_dsp_yst0 Win2 vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x000a	win2_dsp_xst0 Win2 horizontal start point(x) of the Panel scanning

VOP_WIN2_COLOR_KEY
Address: Operational Base + offset (0x00cc)
Win2 color key register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	win2_key_en Win2 transparency color key enable 1'b0 : disable; 1'b1 : enable;
23:0	RW	0x000000	win2_key_color Win2 key color

VOP_WIN2_MST1
Address: Operational Base + offset (0x00d0)
Win2 memory start address1

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win2_mst1 Win2 frame buffer memory start address1 *must be alianed to 8byte address

VOP_WIN2_DSP_INFO1
Address: Operational Base + offset (0x00d4)
Win2 display width1/height1 on panel

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0ef	win2_dsp_height1 Win2 display window height1 win2_dsp_height0 = size -1
15:12	RO	0x0	reserved
11:0	RW	0x13f	win2_dsp_width1 Win2 display window width1 win2_dsp_width = size -1

VOP_WIN2_DSP_ST1
Address: Operational Base + offset (0x00d8)
Win2 display start point1 on panel

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	win2_dsp_yst1 Win2 vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x000a	win2_dsp_xst1 Win2 horizontal start point(x) of the Panel scanning

VOP_WIN2_SRC_ALPHA_CTRL
Address: Operational Base + offset (0x00dc)
Win2 alpha source control register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	win2_fading_value fading value,8bits
23:16	RW	0x00	win2_src_global_alpha src global alpha
15:9	RO	0x0	reserved
8:6	RW	0x0	win2_src_factor_mode src factor mode
5	RW	0x0	win2_src_alpha_cal_mode src alpha cal mode
4:3	RW	0x0	win2_src_blend_mode src blend mode
2	RW	0x0	win2_src_alpha_mode src alpha mode
1	RW	0x0	win2_src_color_mode src color mode
0	RW	0x0	win2_src_alpha_en src alpha en

VOP_WIN2_MST2
Address: Operational Base + offset (0x00e0)
Win2 memory start address2

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win2_mst2 Win2 frame buffer memory start address2 *must be alianed to 8byte address

VOP_WIN2_DSP_INFO2
Address: Operational Base + offset (0x00e4)
Win2 display width2/height2 on panel

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27:16	RW	0x0ef	win2_dsp_height2 Win2 display window height2 win2_dsp_height0 = size -1
15:12	RO	0x0	reserved
11:0	RW	0x13f	win2_dsp_width2 Win2 display window width2 win2_dsp_width = size -1

VOP_WIN2_DSP_ST2
Address: Operational Base + offset (0x00e8)
Win2 display start point2 on panel

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	win2_dsp_yst2 Win2 vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x000a	win2_dsp_xst2 Win2 horizontal start point(x) of the Panel scanning

VOP_WIN2_DST_ALPHA_CTRL
Address: Operational Base + offset (0x00ec)
Win2 alpha destination control register

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:6	RW	0x0	win2_dst_factor_mode dst factor mode
5:0	RW	0x00	win2_dst_m0_reserved reserved

VOP_WIN2_MST3
Address: Operational Base + offset (0x00f0)
Win2 memory start address3

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win2_mst3 Win2 frame buffer memory start address3 *must be alianed to 8byte address

VOP_WIN2_DSP_INFO3
Address: Operational Base + offset (0x00f4)
Win2 display width3/height3 on panel

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27:16	RW	0x0ef	win2_dsp_height3 Win2 display window height3 win2_dsp_height0 = size -1
15:12	RO	0x0	reserved
11:0	RW	0x13f	win2_dsp_width3 Win2 display window width3 win2_dsp_width = size -1

VOP_WIN2_DSP_ST3
Address: Operational Base + offset (0x00f8)
Win2 display start point3 on panel

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	win2_dsp_yst3 Win2 vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x000a	win2_dsp_xst3 Win2 horizontal start point(x) of the Panel scanning

VOP_WIN2_FADING_CTRL
Address: Operational Base + offset (0x00fc)
Win2 fading contrl register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	win2_fading_en fading enable 1'b0 : disable 1'b1 : enable
23:16	RW	0x00	win2_fading_offset_b fading offset blue
15:8	RW	0x00	win2_fading_offset_g fading offset green
7:0	RW	0x00	win2_fading_offset_r fading offset red

VOP_WIN3_CTRL0
Address: Operational Base + offset (0x0100)
Win3 ctrl register0

Bit	Attr	Reset Value	Description
31	RW	0x0	win3_endian_swap3 Win3 region3 8pp palette data Big-endian/ Little-endian select 1'b0 : Big-endian 1'b1 : Little-endian

Bit	Attr	Reset Value	Description
30	RW	0x0	win3_alpha_swap3 Win3 region3 RGB alpha swap 1'b0 : ARGB 1'b1 : RGBA
29	RW	0x0	win3_rb_swap3 Win3 region3 RGB Red and Blue swap 1'b0 : RGB 1'b1 : BGR
28	RW	0x0	win3_endian_swap2 Win3 region2 8pp palette data Big-endian/ Little-endian select 1'b0 : Big-endian 1'b1 : Little-endian
27	RW	0x0	win3_alpha_swap2 Win3 region2 RGB alpha swap 1'b0 : ARGB 1'b1 : RGBA
26	RW	0x0	win3_rb_swap2 Win3 region2 RGB Red and Blue swap 1'b0 : RGB 1'b1 : BGR
25	RW	0x0	win3_endian_swap1 Win3 region1 8pp palette data Big-endian/ Little-endian select 1'b0 : Big-endian 1'b1 : Little-endian
24	RW	0x0	win3_alpha_swap1 Win3 region1 RGB alpha swap 1'b0 : ARGB 1'b1 : RGBA
23	RW	0x0	win3_rb_swap1 Win3 region1 RGB Red and Blue swap 1'b0 : RGB 1'b1 : BGR
22	RW	0x0	win3_endian_swap0 Win3 region0 8pp palette data Big-endian/ Little-endian select 1'b0 : Big-endian 1'b1 : Little-endian
21	RW	0x0	win3_alpha_swap0 Win3 region0 RGB alpha swap 1'b0 : ARGB 1'b1 : RGBA
20	RW	0x0	win3_rb_swap0 Win3 region0 RGB Red and Blue swap 1'b0 : RGB 1'b1 : BGR
19	RO	0x0	reserved

Bit	Attr	Reset Value	Description
18:17	RW	0x0	win3_data_fmt3 Win3 region 3 data format 2'b00 : ARGB888 2'b01 : RGB888 2'b10 : RGB565 2'b11 : 8bpp
16	RW	0x0	win3_mst3_en win3 master3 enable 1'b0 : disable 1'b1 : enable
15	RO	0x0	reserved
14:13	RW	0x0	win3_data_fmt2 Win3 region 2 data format 2'b00 : ARGB888 2'b01 : RGB888 2'b10 : RGB565 2'b11 : 8bpp
12	RW	0x0	win3_mst2_en win3 master2 enable 1'b0 : disable 1'b1 : enable
11	RO	0x0	reserved
10:9	RW	0x0	win3_data_fmt1 Win3 region 1 data format 2'b00 : ARGB888 2'b01 : RGB888 2'b10 : RGB565 2'b11 : 8bpp
8	RW	0x0	win3_mst1_en win3 master1 enable 1'b0 : disable 1'b1 : enable
7	RO	0x0	reserved
6:5	RW	0x0	win3_data_fmt0 Win3 region 0 data format 2'b00 : ARGB888 2'b01 : RGB888 2'b10 : RGB565 2'b11 : 8bpp
4	RW	0x0	win3_mst0_en Win3 master0 enable 1'b0 : disable 1'b1 : enable

Bit	Attr	Reset Value	Description
3:2	RW	0x0	win3_csc_mode Win3 RGB2YUV conversion mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
1	RW	0x0	win3_interlace_read Win3 interlace read mode 1'b0 : disable 1'b1 : enable
0	RW	0x0	win3_en 1'b0 : disable 1'b1 : enable

VOP_WIN3_CTRL1
Address: Operational Base + offset (0x0104)
Win3 ctrl register1

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:20	RW	0x6	win_rid_win3 axi read id of win3 channel
19:17	RO	0x0	reserved
16	RW	0x0	win3_lut_en Win3 LUT ram enable 1'b0 : disable 1'b1 : enable *This bit should be "0" when CPU updates the LUT, and should be "1" when Win1 LUT mode enable.
15	RW	0x0	win3_y_mir_en 1'b0 : no y_mirror 1'b1 : y_mirror
14	RW	0x0	win3_no_outstanding Win3 AXI master read outstanding 1'b0 : enable 1'b1 : disable
13	RO	0x0	reserved
12:8	RW	0x1d	win3_axi_max_outstanding_num win3 axi bus max outstanding number
7:4	RW	0x0	win3_axi_gather_num win3 axi gather transfer number

Bit	Attr	Reset Value	Description
3:2	RW	0x0	win3_dma_burst_length WIN3 DMA read Burst length 2'b00 : burst16 (burst 15 in rgb888 pack mode) 2'b01 : burst8 (burst 12 in rgb888 pack mode) 2'b10 : burst4 (burst 6 in rgb888 pack mode) 2'b11 : reserved
1	RW	0x0	win3_axi_max_outstanding_en 1'b0 : disable 1'b1 : enable
0	RW	0x0	win3_axi_gather_en 1'b0 : disable 1'b1 : enable

VOP_WIN3_VIR0_1
Address: Operational Base + offset (0x0108)
Win3 virtual stride0 and virtaul stride1

Bit	Attr	Reset Value	Description
31:16	RW	0x0140	win3_vir_stride1 Win3 Virtual stride1 Number of words of Win3 Virtual1 width ARGB888 : win3_vir_width1 RGB888 : (win3_vir_width1 * 3/4) + (win3_vir_width1 % 3) RGB565 : ceil(win3_vir_width1 / 2) 8BPP : ceil(win3_vir_width1 / 4) 4BPP : ceil(win3_vir_width1 / 8) 2BPP : ceil(win3_vir_width1 / 16) 1BPP : ceil(win3_vir_width1 / 32)
15:0	RW	0x0140	win3_vir_stride0 Win3 Virtual stride0 Number of words of Win3 Virtual1 width ARGB888 : win3_vir_width1 RGB888 : (win3_vir_width1 * 3/4) + (win3_vir_width1 % 3) RGB565 : ceil(win3_vir_width1 / 2) 8BPP : ceil(win3_vir_width1 / 4) 4BPP : ceil(win3_vir_width1 / 8) 2BPP : ceil(win3_vir_width1 / 16) 1BPP : ceil(win3_vir_width1 / 32)

VOP_WIN3_VIR2_3
Address: Operational Base + offset (0x010c)
Win3 virtual stride2 and virtaul stride3

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0140	win3_vir_stride3 Win3 Virtual stride3 Number of words of Win3 Virtual1 width ARGB888 : win3_vir_width1 RGB888 : (win3_vir_width1 * 3/4) + (win3_vir_width1 % 3) RGB565 : ceil(win3_vir_width1 / 2) 8BPP : ceil(win3_vir_width1 / 4) 4BPP : ceil(win3_vir_width1 / 8) 2BPP : ceil(win3_vir_width1 / 16) 1BPP : ceil(win3_vir_width1 / 32)
15:0	RW	0x0140	win3_vir_stride2 Win3 Virtual stride2 Number of words of Win3 Virtual1 width ARGB888 : win3_vir_width1 RGB888 : (win3_vir_width1 * 3/4) + (win3_vir_width1 % 3) RGB565 : ceil(win3_vir_width1 / 2) 8BPP : ceil(win3_vir_width1 / 4) 4BPP : ceil(win3_vir_width1 / 8) 2BPP : ceil(win3_vir_width1 / 16) 1BPP : ceil(win3_vir_width1 / 32)

VOP_WIN3_MST0
Address: Operational Base + offset (0x0110)
Win3 memory start address0

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win3_mst0 Win3 frame buffer memory start address0 *must be alianed to 8byte address

VOP_WIN3_DSP_INFO0
Address: Operational Base + offset (0x0114)
Win3 display width0/height0 on panel

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0ef	win3_dsp_height0 Win3 display window height0 win3_dsp_height0 = size -1
15:12	RO	0x0	reserved
11:0	RW	0x13f	win3_dsp_width0 Win3 display window width0 win3_dsp_width = size -1

VOP_WIN3_DSP_ST0
Address: Operational Base + offset (0x0118)
Win3 display start point0 on panel

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	win3_dsp_yst0 Win3 vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x000a	win3_dsp_xst0 Win3 horizontal start point(x) of the Panel scanning

VOP_WIN3_COLOR_KEY
Address: Operational Base + offset (0x011c)
Win3 color key register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	win3_key_en Win3 transparency color key enable 1'b0 : disable; 1'b1 : enable;
23:0	RW	0x000000	win3_key_color Win3 key color

VOP_WIN3_MST1
Address: Operational Base + offset (0x0120)
Win3 memory start address1

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win3_mst1 Win3 frame buffer memory start address1 *must be alianed to 8byte address

VOP_WIN3_DSP_INFO1
Address: Operational Base + offset (0x0124)
Win3 display width1/height1 on panel

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0ef	win3_dsp_height1 Win3 display window height1 win3_dsp_height0 = size -1
15:12	RO	0x0	reserved
11:0	RW	0x13f	win3_dsp_width1 Win3 display window width1 win3_dsp_width = size -1

VOP_WIN3_DSP_ST1
Address: Operational Base + offset (0x0128)
Win3 display start point1 on panel

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	win3_dsp_yst1 Win3 vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x000a	win3_dsp_xst1 Win3 horizontal start point(x) of the Panel scanning

VOP_WIN3_SRC_ALPHA_CTRL
Address: Operational Base + offset (0x012c)
Win3 alpha source control register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	win3_fading_value fading value
23:16	RW	0x00	win3_src_global_alpha src global alpha
15:9	RO	0x0	reserved
8:6	RW	0x0	win3_src_factor_mode src factor mode
5	RW	0x0	win3_src_alpha_cal_mode src alpha cal mode
4:3	RW	0x0	win3_src_blend_mode src blend mode
2	RW	0x0	win3_src_alpha_mode src alpha mode
1	RW	0x0	win3_src_color_mode src color mode
0	RW	0x0	win3_src_alpha_en src alpha en

VOP_WIN3_MST2
Address: Operational Base + offset (0x0130)
Win3 memory start address2

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win3_mst2 Win3 frame buffer memory start address2 *must be alianed to 8byte address

VOP_WIN3_DSP_INFO2
Address: Operational Base + offset (0x0134)
Win3 display width2/height2 on panel

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27:16	RW	0x0ef	win3_dsp_height2 Win3 display window height2 win3_dsp_height0 = size -1
15:12	RO	0x0	reserved
11:0	RW	0x13f	win3_dsp_width2 Win3 display window width2 win3_dsp_width = size -1

VOP_WIN3_DSP_ST2
Address: Operational Base + offset (0x0138)
Win3 display start point2 on panel

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	win3_dsp_yst2 Win3 vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x000a	win3_dsp_xst2 Win3 horizontal start point(x) of the Panel scanning

VOP_WIN3_DST_ALPHA_CTRL
Address: Operational Base + offset (0x013c)
Win3 alpha destination control register

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:6	RW	0x0	win3_dst_factor_mode dst factor mode
5:0	RW	0x00	win3_dst_factor_reserved reserved

VOP_WIN3_MST3
Address: Operational Base + offset (0x0140)
Win3 memory start address3

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win3_mst3 Win3 frame buffer memory start address3 *must be alianed to 8byte address

VOP_WIN3_DSP_INFO3
Address: Operational Base + offset (0x0144)
Win3 display width3/height3 on panel

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27:16	RW	0x0ef	win3_dsp_height3 Win3 display window height3 win3_dsp_height0 = size -1
15:12	RO	0x0	reserved
11:0	RW	0x13f	win3_dsp_width3 Win3 display window width3 win3_dsp_width = size -1

VOP_WIN3_DSP_ST3
Address: Operational Base + offset (0x0148)
Win3 display start point3 on panel

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	win3_dsp_yst3 Win3 vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x000a	win3_dsp_xst3 Win3 horizontal start point(x) of the Panel scanning

VOP_WIN3_FADING_CTRL
Address: Operational Base + offset (0x014c)
Win3 fading contrl register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	win3_fading_en fadfing enable 1'b0 : disable 1'b1 : enable
23:16	RW	0x00	win3_fading_offset_b fading offset blue
15:8	RW	0x00	win3_fading_offset_g fading offset green
7:0	RW	0x00	win3_fading_offset_r fading offset red

VOP_HWC_CTRL0
Address: Operational Base + offset (0x0150)
Hwc ctrl register0

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14	RW	0x0	hwc_endian_swap hwc 8pp palette data Big-endian/ Little-endian select 1'b0 : Big-endian 1'b1 : Little-endian

Bit	Attr	Reset Value	Description
13	RW	0x0	hwc_alpha_swap hwc RGB alpha swap 1'b0 : ARGB 1'b1 : RGBA
12	RW	0x0	hwc_rb_swap hwc RGB Red and Blue swap 1'b0 : RGB 1'b1 : BGR
11:10	RW	0x0	hwc_csc_mode hwc RGB2YUV Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
9	RO	0x0	reserved
8	RW	0x0	hwc_interlace_read hwc interlace read mode 1'b0 : disable 1'b1 : enable
7	RO	0x0	reserved
6:5	RW	0x0	hwc_size 2'b00 : 32x32 2'b01 : 64x64 2'b10 : 96x96 2'b11 : 128x128
4	RW	0x0	hwc_mode hwc color mode 1'b0 : normal color mode 1'b1 : reversed color mode
3:1	RW	0x0	hwc_data_fmt 3'b000 : ARGB888 3'b001 : RGB888 3'b010 : RGB565 3'b100: 8bpp 3'b101: 4bpp 3'b110: 2bpp 3'b111: 1bpp
0	RW	0x0	hwc_en 1'b0 : disable 1'b1 : enable

VOP_HWC_CTRL1
Address: Operational Base + offset (0x0154)
Hwc ctrl register1

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:20	RW	0x7	win_rid_hwc axi read id of hwc channel
19:17	RO	0x0	reserved
16	RW	0x0	hwc_lut_en 1'b0 : disable 1'b1 : enable
15	RW	0x0	hwc_y_mir_en 1'b0 : no y_mirror 1'b1 : y_mirror
14	RW	0x0	hwc_no_outstanding hwc AXI master read outstanding 1'b0 : enable 1'b1 : disable
13	RW	0x0	hwc_rgb2yuv_en 1'b0 : enable 1'b1 : disable
12:8	RW	0x1d	hwc_axi_max_outstanding_num hwc axi bus max outstanding number
7	RO	0x0	reserved
6:4	RW	0x0	hwc_axi_gather_num hwc axi gather transfer number
3:2	RW	0x0	hwc_dma_burst_length HWC DMA read Burst length 2'b00 : burst16 (burst 15 in rgb888 pack mode) 2'b01 : burst8 (burst 12 in rgb888 pack mode) 2'b10 : burst4 (burst 6 in rgb888 pack mode) 2'b11 : reserved
1	RW	0x0	hwc_axi_max_outstanding_en 1'b0 : disable 1'b1 : enable
0	RW	0x0	hwc_axi_gather_en 1'b0 : disable 1'b1 : enable

VOP_HWC_MST
Address: Operational Base + offset (0x0158)
Hwc memory start address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hwc_mst HWC data memory start address

VOP_HWC_DSP_ST
Address: Operational Base + offset (0x015c)
Hwc display start point on panel

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	hwc_dsp_yst HWC vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x000a	hwc_dsp_xst HWC horizontal start point(x) of the Panel scanning

VOP_HWC_SRC_ALPHA_CTRL
Address: Operational Base + offset (0x0160)
Hwc alpha source control register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	hwc_fading_value fading value
23:16	RW	0x00	hwc_src_global_alpha src global alpha
15:9	RO	0x0	reserved
8:6	RW	0x0	hwc_src_factor_mode src factor mode
5	RW	0x0	hwc_src_alpha_cal_mode src alpha calc mode
4:3	RW	0x0	hwc_src_blend_mode src blend mode
2	RW	0x0	hwc_src_alpha_mode src alpha mode
1	RW	0x0	hwc_src_color_mode src color mode
0	RW	0x0	hwc_src_alpha_en src alpha enable

VOP_HWC_DST_ALPHA_CTRL
Address: Operational Base + offset (0x0164)
Hwc alpha destination control register

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:6	RW	0x0	hwc_dst_factor_mode dst factor mode
5:0	RW	0x00	hwc_dst_m0_reserved reserved

VOP_HWC_FADING_CTRL
Address: Operational Base + offset (0x0168)
Hwc fading contrl register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved

Bit	Attr	Reset Value	Description
24	RW	0x0	hwc_fading_en 1'b0 : disable 1'b1 : enable
23:16	RW	0x00	hwc_fading_offset_b fading offset blue
15:8	RW	0x00	hwc_fading_offset_g fading offset green
7:0	RW	0x00	hwc_fading_offset_r fading offset red

VOP_HWC_RESERVED1
Address: Operational Base + offset (0x016c)
Hwc reserved

Bit	Attr	Reset Value	Description
31:0	RO	0x0	reserved

VOP_POST_DSP_HACT_INFO
Address: Operational Base + offset (0x0170)
Post scaler down horizontal start and end

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	dsp_hact_st_post Panel display scanning horizontal active start point
15:13	RO	0x0	reserved
12:0	RW	0x014a	dsp_hact_end_post Panel display scanning horizontal active end point

VOP_POST_DSP_VACT_INFO
Address: Operational Base + offset (0x0174)
Panel active horizontal scanning start point and end point

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	dsp_vact_st_post Panel display scanning horizontal active start point
15:13	RO	0x0	reserved
12:0	RW	0x00fa	dsp_vact_end_post Panel display scanning horizontal active end point

VOP_POST_SCL_FACTOR_YRGB
Address: Operational Base + offset (0x0178)
Post yrgb scaling factor

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	post_vs_factor_yrgb post YRGB vertical scaling factor: factor=((src_height[31:16]) /(dst_height[31:16]))*2^12
15:0	RW	0x1000	post_hs_factor_yrgb Post YRGB horizontal scaling factor: factor=((src_width[15:0]) /(dst_width[15:0]))*2^12

VOP_POST_RESERVED
Address: Operational Base + offset (0x017c)
Post reserved

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	RW	0x0	Field0000 Abstract Field0000 Description
1:0	RO	0x0	reserved

VOP_POST_SCL_CTRL
Address: Operational Base + offset (0x0180)
Post scaling start point offset

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	post_ver_sd_en 1'b0 : post ver scl down disable 1'b1 : post ver scl down enable
0	RW	0x0	post_hor_sd_en 1'b0 : post hor scl down disable 1'b1 : post hor scl down enable

VOP_POST_DSP_VACT_INFO_F1
Address: Operational Base + offset (0x0184)
Panel active horizontal scanning start point and end point F1

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	dsp_vact_st_post Panel display scanning horizontal active start point
15:13	RO	0x0	reserved
12:0	RW	0x00fa	dsp_vact_end_post Panel display scanning horizontal active end point

VOP_DSP_HTOTAL_HS_END
Address: Operational Base + offset (0x0188)
Panel scanning horizontal width and hsync pulse end point

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x014a	dsp_htotal Panel display scanning horizontal period
15:13	RO	0x0	reserved
12:0	RW	0x000a	dsp_hs_end Panel display scanning hsync pulse width

VOP_DSP_HACT_ST_END
Address: Operational Base + offset (0x018c)
Panel active horizontal scanning start point and end point

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	dsp_hact_st Panel display scanning horizontal active start point
15:13	RO	0x0	reserved
12:0	RW	0x014a	dsp_hact_end Panel display scanning horizontal active end point

VOP_DSP_VTOTAL_VS_END
Address: Operational Base + offset (0x0190)
Panel scanning vertical height and vsync pulse end point

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x00fa	dsp_vtotal Panel display scanning vertical period.
15	RW	0x0	sw_dsp_vtotal_imd dsp vtotal number valid immediately enable. 1'b0 : valid after frame start 1'b1 : valid immediately
14:13	RO	0x0	reserved
12:0	RW	0x000a	dsp_vs_end Panel display scanning vsync pulse width

VOP_DSP_VACT_ST_END
Address: Operational Base + offset (0x0194)
Panel active vertical scanning start point and end point

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	dsp_vact_st Panel display scanning vertical active start point
15:13	RO	0x0	reserved
12:0	RW	0x00fa	dsp_vact_end Panel display scanning vertical active end point

VOP_DSP_VS_ST_END_F1
Address: Operational Base + offset (0x0198)
Vertical scanning start point and vsync pulse end point of even filed in interlace mode

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vs_st_f1 Panel display scanning vertical vsync start point of 2nd field (interlace display mode)
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vs_end_f1 Panel display scanning vertical vsync end point of 2nd field(interlace display mode)

VOP_DSP_VACT_ST_END_F1
Address: Operational Base + offset (0x019c)
Vertical scanning active start point and end point of even filed in interlace mode

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vact_st_f1 Panel display scanning vertical active start point of 2nd field (interlace display mode)
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vact_end_f1 Panel display scanning vertical active end point of 2nd field (interlace display mode)

VOP_PWM_CTRL
Address: Operational Base + offset (0x01a0)
PWM Control Register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	rpt Repeat Counter This field defines the repeated effective periods of output waveform in one-shot mode. The value N means N+1 repeated effective periods.
23:16	RW	0x00	scale Scale Factor This fields defines the scale factor applied to prescaled clock. The value N means the clock is divided by 2*N. If N is 0, it means that the clock is divided by 512(2*256).
15	RO	0x0	reserved
14:12	RW	0x2	prescale Prescale Factor This field defines the prescale factor applied to input clock. The value N means that the input clock is divided by 2^N.
11:10	RO	0x0	reserved

Bit	Attr	Reset Value	Description
9	RW	0x0	clk_sel Clock Source Select 1'b0: non-scaled clock is selected as PWM clock source. It means that the prescale clock is directly used as the PWM clock source 1'b1: scaled clock is selected as PWM clock source
8	RW	0x0	lp_en Low Power Mode Enable 1'b0: disabled 1'b1: enabled When PWM channel is inactive state and Low Power Mode is enabled, the path to PWM Clock prescale module is blocked to reduce power consumption.
7:6	RO	0x0	reserved
5	RW	0x0	output_mode PWM Output mode 1'b0: left aligned mode 1'b1: center aligned mode
4	RW	0x0	inactive_pol Inactive State Output Polarity This defines the output waveform polarity when PWM channel is in inactive state. The inactive state means that PWM finishes the complete waveform in one-shot mode or PWM channel is disabled. 1'b0: negative 1'b1: positive
3	RW	0x1	duty_pol Duty Cycle Output Polarity This defines the polarity for duty cycle. PWM starts the output waveform with duty cycle. 1'b0: negative 1'b1: positive
2:1	RW	0x1	pwm_mode PWM Operation Mode 2'b00: One shot mode. PWM produces the waveform within the repeated times defined by PWMx_CTRL_rpt . 2'b01: Continuous mode. PWM produces the waveform continuously 2'b10: Capture mode. PWM measures the cycles of high/low polarity of input waveform. 2'b11: reserved
0	RW	0x0	pwm_en PWM channel enable 1'b0: disabled 1'b1: enabled. If the PWM is worked the one-shot mode, this bit will be cleared at the end of operation

VOP_PWM_PERIOD_HPR
Address: Operational Base + offset (0x01a4)
PWM Period Register/High Polarity Capture Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwm_period Output Waveform Period/Input Waveform High Polarity Cycle If PWM is operated at the continuous mode or one-shot mode, this value defines the period of the output waveform. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the bit [31:1] is taken into account and bit [0] always considered as 0. If PWM is operated at the capture mode, this value indicates the effective high polarity cycles of input waveform. This value is based on the PWM clock. The value ranges from 0 to (2^32-1).

VOP_PWM_DUTY_LPR
Address: Operational Base + offset (0x01a8)
PWM Duty Register/Low Polarity Capture Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwm_duty Output Waveform Duty Cycle/Input Waveform Low Polarity Cycle If PWM is operated at the continuous mode or one-shot mode, this value defines the duty cycle of the output waveform. The PWM starts the output waveform with duty cycle. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the [31:1] is taken into account. If PWM is operated at the capture mode, this value indicates the effective low polarity cycles of input waveform. This value is based on the PWM clock. The value ranges from 0 to (2^32-1).

VOP_PWM_CNT
Address: Operational Base + offset (0x01ac)
PWM Counter Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pwm_cnt Timer Counter The 32-bit indicates current value of PWM Channel 0 counter. The counter runs at the rate of PWM clock. The value ranges from 0 to (2^32-1).

VOP_BCSH_COLOR_BAR
Address: Operational Base + offset (0x01b0)
Color bar config register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:24	RW	0x00	color_bar_v v color value
23:16	RW	0x00	color_bar_u u color value
15:8	RW	0x00	color_bar_y y color value
7:1	RO	0x0	reserved
0	RW	0x0	bcsh_en 1'b0 : bcsh bypass 1'b1 : bcsh enable

VOP_BCSH_BCS
Address: Operational Base + offset (0x01b4)
Brightness contrast saturation*contrast config register

Bit	Attr	Reset Value	Description
31:30	RW	0x3	out_mode video out mode config register 2'b00 : black 2'b01 : blue 2'b10 : color bar 2'b11 : normal video
29:20	RW	0x100	sat_con Saturation*Contrast*256 : 0,1.992*1.992
19:17	RO	0x0	reserved
16:8	RW	0x100	contrast Contrast*256 : 0,1.992
7:0	RW	0x00	brightness Brightness : -32,31

VOP_BCSH_H
Address: Operational Base + offset (0x01b8)
Sin hue and cos hue config register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x100	cos_hue cos hue value
15:9	RO	0x0	reserved
8:0	RW	0x000	sin_hue sin hue value

VOP_BCSH_CTRL
Address: Operational Base + offset (0x01bc)
BCSH contrl register

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6	RW	0x0	bcsh_r2y_csc_mode Color space conversion: 1'b0: BT601 1'b1: BT709
5	RO	0x0	reserved
4	RW	0x0	bcsh_r2y_en 1'b0:bypass 1'b1:enable
3:2	RW	0x0	bcsh_y2r_csc_mode Color space conversion(YUV2RGB): 2'b00/01 : mpeg 2'b10 : jpeg 2'b11 : hd
1	RO	0x0	reserved
0	RW	0x0	bcsh_y2r_en 1'b0:bypass 1'b1:enable

VOP_CABC_CTRL0
Address: Operational Base + offset (0x01c0)
Content Adaptive Backlight Control register0

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:4	RW	0x0ed800	cabc_calc_pixel_num cabc calc pixel numbers = x % * cabc_total_num
3:2	RW	0x0	pwm_config_mode 2'b00 : last frame pwm value 2'b01 : cur frame pwm value 2'b1x : stage by stage
1	RW	0x0	cabc_handle_en cabc control pwm
0	RW	0x0	cabc_en 1'b0 : cabc disable 1'b1 : cabc enable

VOP_CABC_CTRL1
Address: Operational Base + offset (0x01c4)
Content Adaptive Backlight Control register1

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:4	RW	0x0fa000	cabc_total_num cabc totala numbers = h_vd * v_vd
3:1	RO	0x0	reserved
0	RW	0x0	cabc_lut_en cabc pwm lut enable

VOP_CABC_CTRL2
Address: Operational Base + offset (0x01c8)
Content Adaptive Backlight Control register2

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19	RW	0x0	cabc_stage_up_mode 1'b0: mul mode 1'b1: add mode
18:17	RO	0x0	reserved
16:8	RW	0x110	cabc_stage_up when mul mode ,scale stage up (1~1.5 * 256). when add mode ,scale stage up (0x00~0xff).
7:0	RW	0xf0	cabc_stage_down when mul mode ,scale stage down (0.667~1 * 256). when add mode ,scale stage down (0x00~0xff).

VOP_CABC_CTRL3
Address: Operational Base + offset (0x01cc)
Content Adaptive Backlight Control register3

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8	RW	0x0	cabc_global_dn_limit_en cabc global scale down limit enable.
7:0	RW	0x00	cabc_global_dn cabc global scale down value.

VOP_CABC_GAUSS_LINE0_0
Address: Operational Base + offset (0x01d0)
CABC gauss line config register00

Bit	Attr	Reset Value	Description
31:24	RW	0x15	t_line0_3 gauss parameter t_line0_3
23:16	RW	0x11	t_line0_2 gauss parameter t_line0_2
15:8	RW	0x09	t_line0_1 gauss parameter t_line0_1
7:0	RW	0x03	t_line0_0 gauss parameter t_line0_0

VOP_CABC_GAUSS_LINE0_1
Address: Operational Base + offset (0x01d4)
CABC gauss line config register01

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved

Bit	Attr	Reset Value	Description
23:16	RW	0x03	t_line0_6 gauss parameter t_line0_6
15:8	RW	0x09	t_line0_5 gauss parameter t_line0_5
7:0	RW	0x11	t_line0_4 gauss parameter t_line0_4

VOP_CABC_GAUSS_LINE1_0
Address: Operational Base + offset (0x01d8)
CABC gauss line config register10

Bit	Attr	Reset Value	Description
31:24	RW	0x1a	t_line1_3 gauss parameter t_line1_3
23:16	RW	0x15	t_line1_2 gauss parameter t_line1_2
15:8	RW	0x0b	t_line1_1 gauss parameter t_line1_1
7:0	RW	0x04	t_line1_0 gauss parameter t_line1_0

VOP_CABC_GAUSS_LINE1_1
Address: Operational Base + offset (0x01dc)
CABC gauss line config register11

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x04	t_line1_6 gauss parameter t_line1_6
15:8	RW	0x0b	t_line1_5 gauss parameter t_line1_5
7:0	RW	0x15	t_line1_4 gauss parameter t_line1_4

VOP_CABC_GAUSS_LINE2_0
Address: Operational Base + offset (0x01e0)
CABC gauss line config register20

Bit	Attr	Reset Value	Description
31:24	RW	0x15	t_line2_3 gauss parameter t_line2_3
23:16	RW	0x11	t_line2_2 gauss parameter t_line2_2
15:8	RW	0x09	t_line2_1 gauss parameter t_line2_1
7:0	RW	0x03	t_line2_0 gauss parameter t_line2_0

VOP_CABC_GAUSS_LINE2_1
Address: Operational Base + offset (0x01e4)
CABC gauss line config register21

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x03	t_line2_6 gauss parameter t_line2_6
15:8	RW	0x09	t_line2_5 gauss parameter t_line2_5
7:0	RW	0x11	t_line2_4 gauss parameter t_line2_4

VOP_FRC_LOWER01_0
Address: Operational Base + offset (0x01e8)
FRC lookup table config register010

Bit	Attr	Reset Value	Description
31:16	RW	0x1284	lower01_frm1 frc parameter lowerbit = 2'b01,frm1
15:0	RW	0x4821	lower01_frm0 frc parameter lowerbit = 2'b01,frm0

VOP_FRC_LOWER01_1
Address: Operational Base + offset (0x01ec)
FRC lookup table config register011

Bit	Attr	Reset Value	Description
31:16	RW	0x2148	lower01_frm3 frc parameter lowerbit = 2'b01,frm3
15:0	RW	0x8412	lower01_frm2 frc parameter lowerbit = 2'b01,frm2

VOP_FRC_LOWER10_0
Address: Operational Base + offset (0x01f0)
FRC lookup table config register100

Bit	Attr	Reset Value	Description
31:16	RW	0xa55a	lower10_frm1 frc parameter lowerbit = 2'b10,frm1
15:0	RW	0x9696	lower10_frm0 frc parameter lowerbit = 2'b10,frm0

VOP_FRC_LOWER10_1
Address: Operational Base + offset (0x01f4)
FRC lookup table config register101

Bit	Attr	Reset Value	Description
31:16	RW	0x5aa5	lower10_frm3 frc parameter lowerbit = 2'b10,frm3

Bit	Attr	Reset Value	Description
15:0	RW	0x6969	lower10_frm2 frc parameter lowerbit = 2'b10,frm2

VOP_FRC_LOWER11_0
Address: Operational Base + offset (0x01f8)
FRC lookup table config register110

Bit	Attr	Reset Value	Description
31:16	RW	0xdeb7	lower11_frm1 frc parameter lowerbit = 2'b11,frm1
15:0	RW	0x7bed	lower11_frm0 frc parameter lowerbit = 2'b11,frm0

VOP_FRC_LOWER11_1
Address: Operational Base + offset (0x01fc)
FRC lookup table config register111

Bit	Attr	Reset Value	Description
31:16	RW	0xed7b	lower11_frm3 frc parameter lowerbit = 2'b11,frm3
15:0	RW	0xb7de	lower11_frm2 frc parameter lowerbit = 2'b11,frm2

VOP_AFBCD0_CTRL
Address: Operational Base + offset (0x0200)
AFBCD0 control register

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21	RW	0x0	afbcd_hreg_block_split
20:16	RW	0x00	afbcd_hreg_pixel_packing_fmt
15:12	RW	0x0	fbdc_rid
11:10	RO	0x0	reserved
9	RW	0x0	vop_fbdc_axi_max_outstanding_en
8:4	RW	0x00	vop_fbdc_axi_max_outstanding_num
3	RW	0x0	fbdc_rstn
2:1	RW	0x0	vop_fbdc_win_sel seleclt fbdc to layer 2'bxx
0	RW	0x0	vop_fbdc_en 1'b0 : disable 1'b1 : enable

VOP_AFBCD0_HDR_PTR
Address: Operational Base + offset (0x0204)
AFBCD0 memory start address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	afbcd_hreg_hdr_ptr

VOP_AFBCD0_PIC_SIZE
Address: Operational Base + offset (0x0208)
AFBCD0 pic size

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	afbcd_hreg_pic_height
15:0	RW	0x0000	afbcd_hreg_pic_width

VOP_AFBCD0_STATUS
Address: Operational Base + offset (0x020c)
AFBCD0 status

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	RW	0x0	afbcd_hreg_axi_rresp
1	RW	0x0	afbcd_hreg_dec_resp
0	RW	0x0	afbcd_hreg_idle_n

VOP_INTR_EN0
Address: Operational Base + offset (0x0280)
Interrupt enable register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	intr_en_dma_finish 1'b0: disable 1'b1: enable
14	RW	0x0	intr_en_mmu 1'b0: disable 1'b1: enable
13	RW	0x0	intr_en_dsp_hold_valid display hold valid interrupt enable 1'b0: disable 1'b1: enable

Bit	Attr	Reset Value	Description
12	RW	0x0	intr_en_fs_field field interrupt enable 1'b0: disable 1'b1: enable
11	RW	0x0	intr_en_post_buf_empty post buffer empty interrupt enable 1'b0: disable 1'b1: enable
10	RW	0x0	intr_en_hwc_empty hwc data empty interrupt enable 1'b0: disable 1'b1: enable
9	RW	0x0	intr_en_win3_empty win3 data empty interrupt enable 1'b0: disable 1'b1: enable
8	RW	0x0	intr_en_win2_empty win2 data empty interrupt enable 1'b0: disable 1'b1: enable
7	RW	0x0	intr_en_win1_empty win1 data empty interrupt enable 1'b0: disable 1'b1: enable
6	RW	0x0	intr_en_win0_empty win0 data empty interrupt enable 1'b0: disable 1'b1: enable
5	RW	0x0	intr_en_bus_error Bus error Interrupt enable 1'b0: disable 1'b1: enable
4	RW	0x0	intr_en_line_flag1 Line flag 1 Interrupt enable 1'b0: disable 1'b1: enable
3	RW	0x0	intr_en_line_flag0 Line flag 0 Interrupt enable 1'b0: disable 1'b1: enable
2	RW	0x0	intr_en_addr_same memory start addr same interruption enable 1'b0: disable 1'b1: enable

Bit	Attr	Reset Value	Description
1	RW	0x0	intr_en_fs_new Frame new start interrupt enable 1'b0: disable 1'b1: enable
0	RW	0x0	intr_en_fs Frame start interrupt enable 1'b0: disable 1'b1: enable

VOP_INTR_CLEAR0
Address: Operational Base + offset (0x0284)
Interrupt clear register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	int_clr_dma_finish dma finish interrupt clear(Auto clear)
14	RW	0x0	int_clr_mmu mmu interrupt clear(Auto clear)
13	W1C	0x0	int_clr_dsp_hold_valid display hold valid interrupt clear(Auto clear)
12	W1C	0x0	int_clr_fs_field field start interrupt clear(Auto clear) Field start interrupt clear (Auto clear)
11	W1C	0x0	int_clr_post_buf_empty post buffer empty interrupt clear(Auto clear)
10	W1C	0x0	int_clr_hwc_empty hwc data empty interrupt clear(Auto clear)
9	W1C	0x0	int_clr_win3_empty win3 data empty interrupt clear(Auto clear)
8	W1C	0x0	int_clr_win2_empty win2 data empty interrupt clear(Auto clear)
7	W1C	0x0	int_clr_win1_empty win1 data empty interrupt clear(Auto clear)
6	W1C	0x0	int_clr_win0_empty win0 data empty interrupt clear(Auto clear)
5	W1C	0x0	int_clr_bus_error Bus error Interrupt clear(Auto clear)
4	W1C	0x0	int_clr_line_flag1 Line flag 1 Interrupt clear(Auto clear)
3	W1C	0x0	int_clr_line_flag0 Line flag 0 Interrupt clear(Auto clear)
2	W1C	0x0	int_clr_addr_same memory start addr same interruption clear(Auto clear)

Bit	Attr	Reset Value	Description
1	W1C	0x0	int_clr_fs_new Frame new start interrupt clear (Auto clear)
0	W1C	0x0	int_clr_fs Frame start interrupt clear (Auto clear)

VOP_INTR_STATUS0

Address: Operational Base + offset (0x0288)

interrupt status

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15	RW	0x0	int_status_dma_finish dma finish interrupt status
14	RW	0x0	int_status_mmu mmu interrupt status
13	RO	0x0	int_status_dsp_hold_valid display hold valid interrupt status
12	RO	0x0	int_status_fs_field Field start interrupt status
11	RO	0x0	int_status_post_buf_empty post buffer empty interrupt status
10	RO	0x0	int_status_hwc_empty hwc data empty interrupt status
9	RO	0x0	int_status_win3_empty win3 data empty interrupt status
8	RO	0x0	int_status_win2_empty win2 data empty interrupt status
7	RO	0x0	int_status_win1_empty win1 data empty interrupt status
6	RO	0x0	int_status_win0_empty win0 data empty interrupt status
5	RO	0x0	int_status_bus_error Bus error Interrupt status
4	RO	0x0	int_status_line_flag1 Line flag 1 Interrupt status
3	RO	0x0	int_status_line_flag0 Line flag 0 Interrupt status
2	RW	0x0	int_status_addr_same memory start addr same interruption status
1	RO	0x0	int_status_fs_new Frame start interrupt status(when memory start addr are same,no interruption)
0	RO	0x0	int_status_fs Frame start interrupt status

VOP_INTR_RAW_STATUS0
Address: Operational Base + offset (0x028c)
raw interrupt status

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15	RO	0x0	int_raw_status_dma_finish dma finish interrupt raw status
14	RO	0x0	int_raw_status_mmu mmu interrupt raw status
13	RO	0x0	int_raw_status_dsp_hold_valid display hold valid interrupt raw status
12	RO	0x0	int_raw_status_fs_field Field start raw interrupt status
11	RO	0x0	int_raw_status_post_buf_empty post buffer empty interrupt raw status
10	RO	0x0	int_raw_status_hwc_empty hwc data empty interrupt raw status
9	RO	0x0	int_raw_status_win3_empty win3 data empty interrupt raw status
8	RO	0x0	int_raw_status_win2_empty win2 data empty interrupt raw status
7	RO	0x0	int_raw_status_win1_empty win1 data empty interrupt raw status
6	RO	0x0	int_raw_status_win0_empty win0 data empty interrupt raw status
5	RO	0x0	int_raw_status_bus_error Bus error Interrupt raw status
4	RO	0x0	int_raw_status_line_frag1 Line flag 1 Interrupt raw status
3	RO	0x0	int_raw_status_line_frag0 Line flag 0 Interrupt raw status
2	RO	0x0	int_raw_status_addr_same memory start addr same interruption raw status
1	RO	0x0	int_raw_status_fs_new Frame start interrupt raw status(when memory start addr are same)
0	RO	0x0	int_raw_status_fs Frame start raw interrupt status Frame start raw interrupt status

VOP_INTR_EN1
Address: Operational Base + offset (0x0290)
Interrupt enable register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask

Bit	Attr	Reset Value	Description
15	RW	0x0	int_en_vfp
14	RW	0x0	int_en_wb_finish 1'b0: disable 1'b1: enable
13	RW	0x0	int_en_wb_uv_fifo_full 1'b0: disable 1'b1: enable
12	RW	0x0	int_en_wb_yrgb_fifo_full 1'b0: disable 1'b1: enable
11	RW	0x0	int_en_afbcd3_hreg_axi_rresp 1'b0: disable 1'b1: enable
10	RW	0x0	int_en_afbcd3_hreg_dec_resp 1'b0: disable 1'b1: enable
9	RW	0x0	int_en_afbcd2_hreg_axi_rresp 1'b0: disable 1'b1: enable
8	RW	0x0	int_en_afbcd2_hreg_dec_resp 1'b0: disable 1'b1: enable
7	RW	0x0	int_en_afbcd1_hreg_axi_rresp 1'b0: disable 1'b1: enable
6	RW	0x0	int_en_afbcd1_hreg_dec_resp 1'b0: disable 1'b1: enable
5	RW	0x0	int_en_afbcd0_hreg_axi_rresp 1'b0: disable 1'b1: enable
4	RW	0x0	int_en_afbcd0_hreg_dec_resp 1'b0: disable 1'b1: enable
3	RW	0x0	int_en_fbcd3 1'b0: disable 1'b1: enable
2	RW	0x0	int_en_fbcd2 1'b0: disable 1'b1: enable
1	RW	0x0	int_en_fbcd1 1'b0: disable 1'b1: enable

Bit	Attr	Reset Value	Description
0	RW	0x0	int_en_fbcd0 1'b0: disable 1'b1: enable

VOP_INTR_CLEAR1
Address: Operational Base + offset (0x0294)
Interrupt clear register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15	RW	0x0	int_clr_vfp
14	RW	0x0	int_clr_wb_dma_finish •
13	RW	0x0	int_clr_wb_uv_fifo_full
12	RW	0x0	int_clr_wb_yrgb_fifo_full
11	RW	0x0	int_clr_afbcd3_hreg_axi_rresp interrupt clear (Auto clear)
10	RW	0x0	int_clr_afbcd3_hreg_dec_resp interrupt clear (Auto clear)
9	RW	0x0	int_clr_afbcd2_hreg_axi_rresp interrupt clear (Auto clear)
8	RW	0x0	int_clr_afbcd2_hreg_dec_resp interrupt clear (Auto clear)
7	RW	0x0	int_clr_afbcd1_hreg_axi_rresp interrupt clear (Auto clear)
6	RW	0x0	int_clr_afbcd1_hreg_dec_resp interrupt clear (Auto clear)
5	RW	0x0	int_clr_afbcd0_hreg_axi_rresp interrupt clear (Auto clear)
4	RW	0x0	int_clr_afbcd0_hreg_dec_resp interrupt clear (Auto clear)
3	RW	0x0	int_clr_fbcd3 interrupt clear (Auto clear)
2	RW	0x0	int_clr_fbcd2 interrupt clear (Auto clear)
1	W1C	0x0	int_clr_fbcd1 interrupt clear (Auto clear)
0	W1C	0x0	int_clr_fbcd0 interrupt clear (Auto clear)

VOP_INTR_STATUS1
Address: Operational Base + offset (0x0298)
interrupt status

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15	RW	0x0	int_status_vfp
14	RW	0x0	int_status_wb_dma_finish
13	RW	0x0	int_status_wb_uv_fifo_full •
12	RW	0x0	int_status_wb_yrgb_fifo_full
11	RW	0x0	int_status_afbcd4_hreg_dec_resp interrupt status
10	RW	0x0	int_status_afbcd3_hreg_dec_resp interrupt status
9	RW	0x0	int_status_afbcd2_hreg_axi_rresp interrupt status
8	RW	0x0	int_status_afbcd2_hreg_dec_resp interrupt status
7	RW	0x0	int_status_afbcd1_hreg_axi_rresp interrupt status
6	RW	0x0	int_status_afbcd1_hreg_dec_resp interrupt status
5	RW	0x0	int_status_afbcd0_hreg_axi_rresp interrupt status
4	RW	0x0	int_status_afbcd0_hreg_dec_resp interrupt status
3	RW	0x0	int_status_fbcd3 interrupt status
2	RW	0x0	int_status_fbcd2 interrupt status
1	RO	0x0	int_status_fbcd1 interrupt status
0	RO	0x0	int_status_fbcd0 interrupt status

VOP_INTR_RAW_STATUS1
Address: Operational Base + offset (0x029c)
raw interrupt status

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15	RW	0x0	int_raw_status_vfp
14	RW	0x0	int_raw_status_wb_dma_finish
13	RW	0x0	int_raw_status_wb_uv_fifo_full

Bit	Attr	Reset Value	Description
12	RW	0x0	int_raw_status_wb_yrgb_fifo_full •
11	RW	0x0	int_raw_status_afbcd3_hreg_axi_rresp interrupt raw status
10	RW	0x0	int_raw_status_afbcd3_hreg_dec_resp interrupt raw status
9	RW	0x0	int_raw_status_afbcd2_hreg_axi_rresp interrupt raw status
8	RW	0x0	int_raw_status_afbcd2_hreg_dec_resp interrupt raw status
7	RW	0x0	int_raw_status_afbcd1_hreg_axi_rresp interrupt raw status
6	RW	0x0	int_raw_status_afbcd1_hreg_dec_resp interrupt raw status
5	RW	0x0	int_raw_status_afbcd0_hreg_axi_rresp interrupt raw status
4	RW	0x0	int_raw_status_afbcd0_hreg_dec_resp interrupt raw status
3	RW	0x0	int_raw_status_fbcd3 interrupt raw status
2	RW	0x0	int_raw_status_fbcd2 interrupt raw status
1	RW	0x0	int_raw_status_fbcd1 interrupt raw status
0	RO	0x0	int_raw_status_fbcd0 interrupt raw status

VOP_LINE_FLAG
Address: Operational Base + offset (0x02a0)
Line flag config register

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_line_flag_num_1 Line number of the Line flag interrupt 1 The display line number when the flag interrupt 1 occur, the range is (0~ DSP_VTOTAL-1).
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_line_flag_num_0 Line number of the Line flag interrupt 0 The display line number when the flag interrupt occur, the range is (0~ DSP_VTOTAL-1).

VOP_VOP_STATUS
Address: Operational Base + offset (0x02a4)
vop status register

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17	RW	0x0	dma_stop_valid dma stop valid
16	RW	0x0	mmu_idle mmu idle status
15:13	RO	0x0	reserved
12:0	RO	0x0000	dsp_vcnt read the dsp vertical counter

VOP_BLANKING_VALUE
Address: Operational Base + offset (0x02a8)
Register0000 Abstract

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	blanking_value_config_en 1'b0 : disable blanking value when vop blank 1'b1 : enable blanking value when vop blank
23:0	RW	0x000000	blanking_value vop output data value when blanking,24bits

VOP_MCU_BYPASS_PORT
Address: Operational Base + offset (0x02ac)
MCU bypass port

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	Field0000 Abstract Field0000 Description

VOP_WIN0_DSP_BG
Address: Operational Base + offset (0x02b0)
Win0 layer background color

Bit	Attr	Reset Value	Description
31	RW	0x0	win0_bg_en Win0 layer background enable 1'b0 : disable 1'b1 : enable
30:24	RO	0x0	reserved
23:16	RW	0x00	win0_dsp_bg_red Win0 layer Background Red color
15:8	RW	0x00	win0_dsp_bg_green Win0 layer Background Green color
7:0	RW	0x00	win0_dsp_bg_blue Win0 layer Background Blue color

VOP_WIN1_DSP_BG
Address: Operational Base + offset (0x02b4)
Win1 layer background color

Bit	Attr	Reset Value	Description
31	RW	0x0	win1_bg_en Win1 layer background enable 1'b0 : disable 1'b1 : enable
30:24	RO	0x0	reserved
23:16	RW	0x00	win1_dsp_bg_red Win1 layer Background Red color
15:8	RW	0x00	win1_dsp_bg_green Win1 layer Background Green color
7:0	RW	0x00	win1_dsp_bg_blue Win1 layer Background Blue color

VOP_WIN2_DSP_BG
Address: Operational Base + offset (0x02b8)
Win2 layer background color

Bit	Attr	Reset Value	Description
31	RW	0x0	win2_bg_en Win2 layer background enable 1'b0 : disable 1'b1 : enable
30:24	RO	0x0	reserved
23:16	RW	0x00	win2_dsp_bg_red Win2 layer Background Red color
15:8	RW	0x00	win2_dsp_bg_green Win2 layer Background Green color
7:0	RW	0x00	win2_dsp_bg_blue Win2 layer Background Blue color

VOP_WIN3_DSP_BG
Address: Operational Base + offset (0x02bc)
Win3 layer background color

Bit	Attr	Reset Value	Description
31	RW	0x0	win3_bg_en Win3 layer background enable 1'b0 : disable 1'b1 : enable
30:24	RO	0x0	reserved
23:16	RW	0x00	win3_dsp_bg_red Win3 layer Background Red color
15:8	RW	0x00	win3_dsp_bg_green Win3 layer Background Green color

Bit	Attr	Reset Value	Description
7:0	RW	0x00	win3_dsp_bg_blue Win3 layer Background Blue color

VOP_YUV2YUV_WIN

Address: Operational Base + offset (0x02c0)

win yuv2yuv control register

Bit	Attr	Reset Value	Description
31:30	RW	0x0	win3_yuv2yuv_r2y_mode 2'b00 : bt601_l 2'b01 : bt709_l 2'b10 : bt601_f 2'b11 : bt2020
29:28	RO	0x0	reserved
27	RW	0x0	win3_yuv2yuv_gamma_mode 1'b0 : bt2020 to bt709 or bt709 to bt2020 1'b1 : bt2020 to srgb or srgb to bt2020
26	RW	0x0	win3_yuv2yuv_r2y_en 1'b0 : disable 1'b1 : enable
25	RO	0x0	reserved
24	RW	0x0	win3_yuv2yuv_en 1'b0 : disable 1'b1 : enable
23:22	RW	0x0	win2_yuv2yuv_r2y_mode •2'b00 : bt601_l 2'b01 : bt709_l 2'b10 : bt601_f 2'b11 : bt2020
21:20	RO	0x0	reserved
19	RW	0x0	win2_yuv2yuv_gamma_mode 1'b0 : bt2020 to bt709 or bt709 to bt2020 1'b1 : bt2020 to srgb or srgb to bt2020
18	RW	0x0	win2_yuv2yuv_r2y_en 1'b0 : disable 1'b1 : enable
17	RO	0x0	reserved
16	RW	0x0	win2_yuv2yuv_en 1'b0 : disable 1'b1 : enable
15:14	RW	0x0	win1_yuv2yuv_r2y_mode 1'b0 : disable 1'b1 : enable
13:12	RW	0x0	win1_yuv2yuv_y2r_mode 1'b0 : disable 1'b1 : enable

Bit	Attr	Reset Value	Description
11	RW	0x0	win1_yuv2yuv_gamma_mode 1'b0 : bt2020 to bt709 or bt709 to bt2020 1'b1 : bt2020 to srgb or srgb to bt2020
10	RW	0x0	win1_yuv2yuv_r2y_en 1'b0 : disable 1'b1 : enable
9	RW	0x0	win1_yuv2yuv_y2r_en •
8	RW	0x0	win1_yuv2yuv_en 1'b0 : disable 1'b1 : enable
7:6	RW	0x0	win0_yuv2yuv_r2y_mode 2'b00 : bt601_l 2'b01 : bt709_l 2'b10 : bt601_f 2'b11 : bt2020
5:4	RW	0x0	win0_yuv2yuv_y2r_mode 2'b00 : bt601_l 2'b01 : bt709_l 2'b10 : bt601_f 2'b11 : bt2020
3	RW	0x0	win0_yuv2yuv_gamma_mode 1'b0 : bt2020 to bt709 or bt709 to bt2020 1'b1 : bt2020 to srgb or srgb to bt2020
2	RW	0x0	win0_yuv2yuv_r2y_en 1'b0 : disable 1'b1 : enable
1	RW	0x0	win0_yuv2yuv_y2r_en 1'b0 : disable 1'b1 : enable
0	RW	0x0	win0_yuv2yuv_en 1'b0 : disable 1'b1 : enable

VOP_AUTO_GATING_EN
Address: Operational Base + offset (0x02cc)
Auto gating enable

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15	RW	0x0	fbcd3_aclk_gating_en
14	RW	0x0	fbcd2_aclk_gating_en
13	RW	0x0	fbcd1_aclk_gating_en

Bit	Attr	Reset Value	Description
12	RW	0x0	fbcd0_aclk_gating_en
11	RO	0x0	reserved
10	RW	0x0	direct_path_aclk_gating_en
9	RW	0x0	pwm_pwmclk_gating_en
8	RW	0x0	wb_aclk_gating_en
7	RW	0x0	cabc_aclk_gating_en
6	RW	0x0	gamma_aclk_gating_en •
5	RW	0x0	overlay_aclk_gating_en
4	RW	0x0	hwc_aclk_gating_en
3	RW	0x0	win3_aclk_gating_en •
2	RW	0x0	win2_aclk_gating_en
1	RW	0x0	win1_aclk_gating_en
0	RW	0x0	win0_aclk_gating_en

VOP_WIN0_YUV2YUV_Y2R_COE0
Address: Operational Base + offset (0x04e0)
WIN0 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe01 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe00 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_Y2R_COE1
Address: Operational Base + offset (0x04e4)
WIN0 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe10 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe02 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_Y2R_COE2
Address: Operational Base + offset (0x04e8)
WIN0 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe12 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe11 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_Y2R_COE3
Address: Operational Base + offset (0x04ec)
WIN0yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe21 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe20 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_Y2R_COE4
Address: Operational Base + offset (0x04f0)
WIN0 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	csc_coe22 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_Y2R_COE5
Address: Operational Base + offset (0x04f4)
WIN0 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset0 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_Y2R_COE6
Address: Operational Base + offset (0x04f8)
WIN0 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset1 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_Y2R_COE7
Address: Operational Base + offset (0x04fc)
WIN0 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset2 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_R2R_COE0
Address: Operational Base + offset (0x0500)
WIN0 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe01 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe00 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_R2R_COE1
Address: Operational Base + offset (0x0504)
WIN0 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe10 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe02 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_R2R_COE2
Address: Operational Base + offset (0x0508)
WIN0 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe12 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe11 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_R2R_COE3
Address: Operational Base + offset (0x050c)
WIN0 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe21 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe20 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_R2R_COE4
Address: Operational Base + offset (0x0510)
WIN0 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	csc_coe22 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_R2R_COE5
Address: Operational Base + offset (0x0514)
WIN0 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset0 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_R2R_COE6
Address: Operational Base + offset (0x0518)
WIN0 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset1 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_R2R_COE7
Address: Operational Base + offset (0x051c)
WIN0 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset2 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_R2Y_COE0
Address: Operational Base + offset (0x0520)
WIN0 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe01 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe00 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_R2Y_COE1
Address: Operational Base + offset (0x0524)
WIN0 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe10 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe02 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_R2Y_COE2
Address: Operational Base + offset (0x0528)
WIN0 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe12 coefficient of 3x4 matrix

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	csc_coe11 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_R2Y_COE3
Address: Operational Base + offset (0x052c)
WIN0 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe21 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe20 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_R2Y_COE4
Address: Operational Base + offset (0x0530)
WIN0 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	csc_coe22 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_R2Y_COE5
Address: Operational Base + offset (0x0534)
WIN0 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset0 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_R2Y_COE6
Address: Operational Base + offset (0x0538)
WIN0 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset1 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_R2Y_COE7
Address: Operational Base + offset (0x053c)
WIN0 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset2 coefficient of 3x4 matrix

VOP_WIN1_YUV2YUV_Y2R_COE0
Address: Operational Base + offset (0x0540)
WIN1 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe01 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe00 coefficient of 3x4 matrix

VOP_WIN1_YUV2YUV_Y2R_COE1
Address: Operational Base + offset (0x0544)
WIN1 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe10 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe02 coefficient of 3x4 matrix

VOP_WIN1_YUV2YUV_Y2R_COE2
Address: Operational Base + offset (0x0548)
WIN1 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe12 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe11 coefficient of 3x4 matrix

VOP_WIN1_YUV2YUV_Y2R_COE3
Address: Operational Base + offset (0x054c)
WIN1 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe21 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe20 coefficient of 3x4 matrix

VOP_WIN1_YUV2YUV_Y2R_COE4
Address: Operational Base + offset (0x0550)
WIN1 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	csc_coe22 coefficient of 3x4 matrix

VOP_WIN1_YUV2YUV_Y2R_COE5
Address: Operational Base + offset (0x0554)
WIN1 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset0 coefficient of 3x4 matrix

VOP_WIN1_YUV2YUV_Y2R_COE6
Address: Operational Base + offset (0x0558)
WIN1 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset1 coefficient of 3x4 matrix

VOP_WIN1_YUV2YUV_Y2R_COE7
Address: Operational Base + offset (0x055c)
WIN1 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset2 coefficient of 3x4 matrix

VOP_WIN1_YUV2YUV_R2R_COE0
Address: Operational Base + offset (0x0560)
WIN0 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe01 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe00 coefficient of 3x4 matrix

VOP_WIN1_YUV2YUV_R2R_COE1
Address: Operational Base + offset (0x0564)
WIN1 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe10 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe02 coefficient of 3x4 matrix

VOP_WIN1_YUV2YUV_R2R_COE2
Address: Operational Base + offset (0x0568)
WIN1 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe12 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe11 coefficient of 3x4 matrix

VOP_WIN1_YUV2YUV_R2R_COE3
Address: Operational Base + offset (0x056c)
WIN1 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe21 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe20 coefficient of 3x4 matrix

VOP_WIN1_YUV2YUV_R2R_COE4
Address: Operational Base + offset (0x0570)
WIN1 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	csc_coe22 coefficient of 3x4 matrix

VOP_WIN1_YUV2YUV_R2R_COE5
Address: Operational Base + offset (0x0574)
WIN1 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset0 coefficient of 3x4 matrix

VOP_WIN1_YUV2YUV_R2R_COE6
Address: Operational Base + offset (0x0578)
WIN1 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset1 coefficient of 3x4 matrix

VOP_WIN1_YUV2YUV_R2R_COE7
Address: Operational Base + offset (0x057c)
WIN1 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset2 coefficient of 3x4 matrix

VOP_WIN1_YUV2YUV_R2Y_COE0
Address: Operational Base + offset (0x0580)
WIN1 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe01 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe00 coefficient of 3x4 matrix

VOP_WIN1_YUV2YUV_R2Y_COE1
Address: Operational Base + offset (0x0584)
WIN1 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe10 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe02 coefficient of 3x4 matrix

VOP_WIN1_YUV2YUV_R2Y_COE2
Address: Operational Base + offset (0x0588)
WIN1 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe12 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe11 coefficient of 3x4 matrix

VOP_WIN1_YUV2YUV_R2Y_COE3
Address: Operational Base + offset (0x058c)
WIN1 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe21 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe20 coefficient of 3x4 matrix

VOP_WIN1_YUV2YUV_R2Y_COE4
Address: Operational Base + offset (0x0590)
WIN1 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	csc_coe22 coefficient of 3x4 matrix

VOP_WIN1_YUV2YUV_R2Y_COE5
Address: Operational Base + offset (0x0594)
WIN1 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset0 coefficient of 3x4 matrix

VOP_WIN1_YUV2YUV_R2Y_COE6
Address: Operational Base + offset (0x0598)

WIN1 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset1 coefficient of 3x4 matrix

VOP_WIN1_YUV2YUV_R2Y_COE7
Address: Operational Base + offset (0x059c)
WIN1 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset2 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_Y2R_COE0
Address: Operational Base + offset (0x05a0)
WIN2 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe01 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe00 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_Y2R_COE1
Address: Operational Base + offset (0x05a4)
WIN2 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe10 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe02 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_Y2R_COE2
Address: Operational Base + offset (0x05a8)
WIN2 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe12 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe11 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_Y2R_COE3
Address: Operational Base + offset (0x05ac)
WIN2 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe21 coefficient of 3x4 matrix

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	csc_coe20 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_Y2R_COE4
Address: Operational Base + offset (0x05b0)
WIN2 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	csc_coe22 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_Y2R_COE5
Address: Operational Base + offset (0x05b4)
WIN2 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset0 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_Y2R_COE6
Address: Operational Base + offset (0x05b8)
WIN2 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset1 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_Y2R_COE7
Address: Operational Base + offset (0x05bc)
WIN2 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset2 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_R2R_COE0
Address: Operational Base + offset (0x05c0)
WIN2 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe01 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe00 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_R2R_COE1
Address: Operational Base + offset (0x05c4)
WIN2 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe10 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe02 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_R2R_COE2
Address: Operational Base + offset (0x05c8)
WIN2 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe12 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe11 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_R2R_COE3
Address: Operational Base + offset (0x05cc)
WIN2 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe21 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe20 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_R2R_COE4
Address: Operational Base + offset (0x05d0)
WIN2 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	csc_coe22 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_R2R_COE5
Address: Operational Base + offset (0x05d4)
WIN2 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset0 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_R2R_COE6
Address: Operational Base + offset (0x05d8)
WIN2 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset1 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_R2R_COE7
Address: Operational Base + offset (0x05dc)
WIN2 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset2 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_R2Y_COE0
Address: Operational Base + offset (0x05e0)
WIN2 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe01 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe00 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_R2Y_COE1
Address: Operational Base + offset (0x05e4)
WIN2 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe10 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe02 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_R2Y_COE2
Address: Operational Base + offset (0x05e8)
WIN2 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe12 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe11 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_R2Y_COE3
Address: Operational Base + offset (0x05ec)
WIN2 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe21 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe20 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_R2Y_COE4
Address: Operational Base + offset (0x05f0)

WIN2 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	csc_coe22 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_R2Y_COE5
Address: Operational Base + offset (0x05f4)
WIN2 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset0 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_R2Y_COE6
Address: Operational Base + offset (0x05f8)
WIN2 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset1 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_R2Y_COE7
Address: Operational Base + offset (0x05fc)
WIN2 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset2 coefficient of 3x4 matrix

VOP_WIN3_YUV2YUV_Y2R_COE0
Address: Operational Base + offset (0x0600)
WIN3 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe01 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe00 coefficient of 3x4 matrix

VOP_WIN3_YUV2YUV_Y2R_COE1
Address: Operational Base + offset (0x0604)
WIN3 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe10 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe02 coefficient of 3x4 matrix

VOP_WIN3_YUV2YUV_Y2R_COE2
Address: Operational Base + offset (0x0608)
WIN3 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe12 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe11 coefficient of 3x4 matrix

VOP_WIN3_YUV2YUV_Y2R_COE3
Address: Operational Base + offset (0x060c)
WIN3 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe21 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe20 coefficient of 3x4 matrix

VOP_WIN3_YUV2YUV_Y2R_COE4
Address: Operational Base + offset (0x0610)
WIN3 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	csc_coe22 coefficient of 3x4 matrix

VOP_WIN3_YUV2YUV_Y2R_COE5
Address: Operational Base + offset (0x0614)
WIN3 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset0 coefficient of 3x4 matrix

VOP_WiN3_YUV2YUV_Y2R_COE6
Address: Operational Base + offset (0x0618)
WIN3 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset1 coefficient of 3x4 matrix

VOP_WIN3_YUV2YUV_Y2R_COE7
Address: Operational Base + offset (0x061c)
WIN3 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset2 coefficient of 3x4 matrix

VOP_WIN3_YUV2YUV_R2R_COE0
Address: Operational Base + offset (0x0620)
WIN3 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe01 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe00 coefficient of 3x4 matrix

VOP_WIN3_YUV2YUV_R2R_COE1
Address: Operational Base + offset (0x0624)
WIN3 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe10 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe02 coefficient of 3x4 matrix

VOP_WIN3_YUV2YUV_R2R_COE2
Address: Operational Base + offset (0x0628)
WIN3 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe12 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe11 coefficient of 3x4 matrix

VOP_WIN3_YUV2YUV_R2R_COE3
Address: Operational Base + offset (0x062c)
WIN3 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe21 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe20 coefficient of 3x4 matrix

VOP_WIN3_YUV2YUV_R2R_COE4
Address: Operational Base + offset (0x0630)
WIN3 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	csc_coe22 coefficient of 3x4 matrix

VOP_WIN3_YUV2YUV_R2R_COE5
Address: Operational Base + offset (0x0634)
WIN3 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset0 coefficient of 3x4 matrix

VOP_WIN3_YUV2YUV_R2R_COE6
Address: Operational Base + offset (0x0638)
WIN3 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset1 coefficient of 3x4 matrix

VOP_WIN3_YUV2YUV_R2R_COE7
Address: Operational Base + offset (0x063c)
WIN3 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset2 coefficient of 3x4 matrix

VOP_WIN3_YUV2YUV_R2Y_COE0
Address: Operational Base + offset (0x0640)
WIN3 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe01 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe00 coefficient of 3x4 matrix

VOP_WIN3_YUV2YUV_R2Y_COE1
Address: Operational Base + offset (0x0644)
WIN3 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe10 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe02 coefficient of 3x4 matrix

VOP_WIN3_YUV2YUV_R2Y_COE2
Address: Operational Base + offset (0x0648)
WIN3 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe12 coefficient of 3x4 matrix

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	csc_coe11 coefficient of 3x4 matrix

VOP_WIN3_YUV2YUV_R2Y_COE3
Address: Operational Base + offset (0x064c)
WIN3 yuv2yuv cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe21 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe20 coefficient of 3x4 matrix

VOP_WIN3_YUV2YUV_R2Y_COE4
Address: Operational Base + offset (0x0650)
WIN3 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	csc_coe22 coefficient of 3x4 matrix

VOP_WIN3_YUV2YUV_R2Y_COE5
Address: Operational Base + offset (0x0654)
WIN3 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset0 coefficient of 3x4 matrix

VOP_WIN3_YUV2YUV_R2Y_COE6
Address: Operational Base + offset (0x0658)
WIN3 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset1 coefficient of 3x4 matrix

VOP_WIN3_YUV2YUV_R2Y_COE7
Address: Operational Base + offset (0x065c)
WIN3 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset2 coefficient of 3x4 matrix

VOP_WIN2_LUT_ADDR
Address: Operational Base + offset (0x1000)
Win2 lut base address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win2_lut_addr the head of win2 lut address

VOP_WIN3_LUT_ADDR
Address: Operational Base + offset (0x1400)
Win3 lut base address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win3_lut_addr the head of win3 lut address

VOP_HWC_LUT_ADDR
Address: Operational Base + offset (0x1800)
Hwc lut base address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hwc_lut_addr the head of hwc lut address

VOP_CABC_GAMMA_LUT_ADDR
Address: Operational Base + offset (0x1c00)
CABC GAMMA lut base address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	gamma_lut_addr the head of gamma lut address

VOP_GAMMA_LUT_ADDR
Address: Operational Base + offset (0x2000)
GAMMA lut base address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	gamma_lut_addr the head of gamma lut address

VOP_MMU_DTE_ADDR
Address: Operational Base + offset (0x3f00)
MMU current page Table address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MMU_DTE_ADDR MMU DTE ADDR

VOP_MMU_STATUS
Address: Operational Base + offset (0x3f04)
MMU status register

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10:6	RO	0x00	PAGE_FAULT_BUS_ID Index of master reponsible for last page fault
5	RO	0x0	PAGE_FAULT_IS_WRITE The direction of access for last page fault: 1'b0 = Read 1'b1 = Write
4	RO	0x0	REPLAY_BUFFER_EMPTY The MMU replay buffer is empty
3	RO	0x0	MMU_IDLE The MMU is idle when accesses are being translated and there are no unfinished translated accesses.
2	RO	0x0	STAIL_ACTIVE MMU stall mode currently enabled. The mode is enabled by command
1	RO	0x0	PAGE_FAULT_ACTIVE MMU page fault mode currently enabled . The mode is enabled by command.
0	RO	0x0	PAGING_ENABLED Paging is enabled

VOP_MMU_COMMAND
Address: Operational Base + offset (0x3f08)
MMU command register

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2:0	WO	0x0	MMU_CMD MMU_CMD. This can be: 0: MMU_ENABLE_PAGING 1: MMU_DISABLE_PAGING 2: MMU_ENABLE_STALL 3: MMU_DISABLE_STALL 4: MMU_ZAP_CACHE 5: MMU_PAGE_FAULT_DONE 6: MMU_FORCE_RESET

VOP_MMU_PAGE_FAULT_ADDR
Address: Operational Base + offset (0x3f0c)
MMU logical address of last page fault

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	PAGE_FAULT_ADDR address of last page fault

VOP_MMU_ZAP_ONE_LINE
Address: Operational Base + offset (0x3f10)

MMU Zap cache line register

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	MMU_ZAP_ONE_LINE address to be invalidated from the page table cache

VOP_MMU_INT_RAWSTAT

Address: Operational Base + offset (0x3f14)

MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	READ_BUS_ERROR read bus error
0	RW	0x0	PAGE_FAULT page fault

VOP_MMU_INT_CLEAR

Address: Operational Base + offset (0x3f18)

MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	WO	0x0	READ_BUS_ERROR read bus error
0	WO	0x0	PAGE_FAULT page fault

VOP_MMU_INT_MASK

Address: Operational Base + offset (0x3f1c)

MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	READ_BUS_ERROR read bus error
0	RW	0x0	PAGE_FAULT page fault

VOP_MMU_INT_STATUS

Address: Operational Base + offset (0x3f20)

MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RO	0x0	READ_BUS_ERROR read bus error
0	RO	0x0	PAGE_FAULT page fault

VOP_MMU_AUTO_GATING
Address: Operational Base + offset (0x3f24)
MMU auto gating

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	mmu_auto_gating mmu auto gating when it is 1'b1, the mmu will auto gating it self

3.5 VOP_LIT Register Description

3.5.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

3.5.2 Registers Summary

Name	Offset	Size	Reset Value	Description
VOP_REG_CFG_DONE	0x0000	W	0x00000000	Register config done flag
VOP_VERSION_INFO	0x0004	W	0x00000000	Version for vop
VOP_SYS_CTRL	0x0008	W	0x00801800	System control register0
VOP_SYS_CTRL1	0x000c	W	0x0003a000	System control register1
VOP_DSP_CTRL0	0x0010	W	0x00000000	
VOP_DSP_CTRL1	0x0014	W	0x0000e400	Display control register1
VOP_DSP_BG	0x0018	W	0x00000000	Background color
VOP_MCU_CTRL	0x001c	W	0x00711c08	MCU mode control register
VOP_WIN0_CTRL0	0x0030	W	0x3a000040	Win0 ctrl register0
VOP_WIN0_CTRL1	0x0034	W	0x00000000	Win0 ctrl register1
VOP_WIN0_COLOR_KEY	0x0038	W	0x00000000	Win0 color key register
VOP_WIN0_VIR	0x003c	W	0x01400140	Win0 virtual stride
VOP_WIN0_YRGB_MST	0x0040	W	0x00000000	Win0 YRGB memory start address
VOP_WIN0_CBR_MST	0x0044	W	0x00000000	Win0 Cbr memory start address
VOP_WIN0_ACT_INFO	0x0048	W	0x00ef013f	Win0 active window width/height
VOP_WIN0_DSP_INFO	0x004c	W	0x00ef013f	Win0 display width/height on panel
VOP_WIN0_DSP_ST	0x0050	W	0x000a000a	Win0 display start point on panel
VOP_WIN0_SCL_FACTOR_YRGB	0x0054	W	0x10001000	Win0 YRGB scaling factor
VOP_WIN0_SCL_FACTOR_CBR	0x0058	W	0x10001000	Win0 Cbr scaling factor
VOP_WIN0_SCL_OFFSET	0x005c	W	0x00000000	Win0 scaling start point offset
VOP_WIN0_SRC_ALPHA_CTRL	0x0060	W	0x00000000	Win0 alpha source control register
VOP_WIN0_DST_ALPHA_CTRL	0x0064	W	0x00000000	Win0 alpha destination control register
VOP_WIN0_FADING_CTRL	0x0068	W	0x00000000	Win0 fading contrl register
VOP_WIN0_CTRL2	0x006c	W	0x00000021	Win0 ctrl register2
VOP_WIN1_CTRL0	0x0070	W	0x3a000040	Win1 ctrl register0
VOP_WIN1_CTRL1	0x0074	W	0x00000000	Win1 ctrl register1

Name	Offset	Size	Reset Value	Description
VOP_WIN1_COLOR_KEY	0x0078	W	0x00000000	Win1 color key register
VOP_WIN1_VIR	0x007c	W	0x01400140	win1 virtual stride
VOP_WIN1_YRGB_MST	0x0080	W	0x00000000	Win1 YRGB memory start address
VOP_WIN1_CBR_MST	0x0084	W	0x00000000	Win1 Cbr memory start address
VOP_WIN1_ACT_INFO	0x0088	W	0x00ef013f	Win1 active window width/height
VOP_WIN1_DSP_INFO	0x008c	W	0x00ef013f	Win1 display width/height on panel
VOP_WIN1_DSP_ST	0x0090	W	0x000a000a	Win1 display start point on panel
VOP_WIN1_SCL_FACTOR_YRGB	0x0094	W	0x10001000	Win1 YRGB scaling factor
VOP_WIN1_SCL_FACTOR_CBR	0x0098	W	0x10001000	Win1 Cbr scaling factor
VOP_WIN1_SCL_OFFSET	0x009c	W	0x00000000	Win1 scaling start point offset
VOP_WIN1_SRC_ALPHA_CTRL	0x00a0	W	0x00000000	Win1 alpha source control register
VOP_WIN1_DST_ALPHA_CTRL	0x00a4	W	0x00000000	Win1 alpha destination control register
VOP_WIN1_FADING_CTRL	0x00a8	W	0x00000000	Win1 fading contrl register
VOP_WIN1_CTRL2	0x00ac	W	0x00000043	Win1 ctrl register2
VOP_WIN2_CTRL0	0x00b0	W	0x00000000	win2 ctrl register0
VOP_WIN2_CTRL1	0x00b4	W	0x00501d00	win2 ctrl register1
VOP_WIN2_VIR0_1	0x00b8	W	0x01400140	Win2 virtual stride0 and virtaul stride1
VOP_WIN2_VIR2_3	0x00bc	W	0x01400140	Win2 virtual stride2 and virtaul stride3
VOP_WIN2_MST0	0x00c0	W	0x00000000	Win2 memory start address0
VOP_WIN2_DSP_INFO0	0x00c4	W	0x00ef013f	Win2 display width0/height0 on panel
VOP_WIN2_DSP_ST0	0x00c8	W	0x000a000a	Win2 display start point0 on panel
VOP_WIN2_COLOR_KEY	0x00cc	W	0x00000000	Win2 color key register
VOP_WIN2_MST1	0x00d0	W	0x00000000	Win2 memory start address1
VOP_WIN2_DSP_INFO1	0x00d4	W	0x00ef013f	Win2 display width1/height1 on panel
VOP_WIN2_DSP_ST1	0x00d8	W	0x000a000a	Win2 display start point1 on panel
VOP_WIN2_SRC_ALPHA_CTRL	0x00dc	W	0x00000000	Win2 alpha source control register
VOP_WIN2_MST2	0x00e0	W	0x00000000	Win2 memory start address2
VOP_WIN2_DSP_INFO2	0x00e4	W	0x00ef013f	Win2 display width2/height2 on panel
VOP_WIN2_DSP_ST2	0x00e8	W	0x000a000a	Win2 display start point2 on panel
VOP_WIN2_DST_ALPHA_CTRL	0x00ec	W	0x00000000	Win2 alpha destination control register
VOP_WIN2_MST3	0x00f0	W	0x00000000	Win2 memory start address3
VOP_WIN2_DSP_INFO3	0x00f4	W	0x00ef013f	Win2 display width3/height3 on panel

Name	Offset	Size	Reset Value	Description
VOP_WIN2_DSP_ST3	0x00f8	W	0x000a000a	Win2 display start point3 on panel
VOP_WIN2_FADING_CTRL	0x00fc	W	0x00000000	Win2 fading contrl register
VOP_WIN3_CTRL0	0x0100	W	0x00000000	Win3 ctrl register0
VOP_WIN3_CTRL1	0x0104	W	0x00601d00	Win3 ctrl register1
VOP_WIN3_VIR0_1	0x0108	W	0x01400140	Win3 virtual stride0 and virtaul stride1
VOP_WIN3_VIR2_3	0x010c	W	0x01400140	Win3 virtual stride2 and virtaul stride3
VOP_WIN3_MST0	0x0110	W	0x00000000	Win3 memory start address0
VOP_WIN3_DSP_INFO0	0x0114	W	0x00ef013f	Win3 display width0/height0 on panel
VOP_WIN3_DSP_ST0	0x0118	W	0x000a000a	Win3 display start point0 on panel
VOP_WIN3_COLOR_KEY	0x011c	W	0x00000000	Win3 color key register
VOP_WIN3_MST1	0x0120	W	0x00000000	Win3 memory start address1
VOP_WIN3_DSP_INFO1	0x0124	W	0x00ef013f	Win3 display width1/height1 on panel
VOP_WIN3_DSP_ST1	0x0128	W	0x000a000a	Win3 display start point1 on panel
VOP_WIN3_SRC_ALPHA_CTRL	0x012c	W	0x00000000	Win3 alpha source control register
VOP_WIN3_MST2	0x0130	W	0x00000000	Win3 memory start address2
VOP_WIN3_DSP_INFO2	0x0134	W	0x00ef013f	Win3 display width2/height2 on panel
VOP_WIN3_DSP_ST2	0x0138	W	0x000a000a	Win3 display start point2 on panel
VOP_WIN3_DST_ALPHA_CTRL	0x013c	W	0x00000000	Win3 alpha destination control register
VOP_WIN3_MST3	0x0140	W	0x00000000	Win3 memory start address3
VOP_WIN3_DSP_INFO3	0x0144	W	0x00ef013f	Win3 display width3/height3 on panel
VOP_WIN3_DSP_ST3	0x0148	W	0x000a000a	Win3 display start point3 on panel
VOP_WIN3_FADING_CTRL	0x014c	W	0x00000000	Win3 fading contrl register
VOP_HWC_CTRL0	0x0150	W	0x00000000	Hwc ctrl register0
VOP_HWC_CTRL1	0x0154	W	0x00701d00	Hwc ctrl register1
VOP_HWC_MST	0x0158	W	0x00000000	Hwc memory start address
VOP_HWC_DSP_ST	0x015c	W	0x000a000a	Hwc display start point on panel
VOP_HWC_SRC_ALPHA_CTRL	0x0160	W	0x00000000	Hwc alpha source control register
VOP_HWC_DST_ALPHA_CTRL	0x0164	W	0x00000000	Hwc alpha destination control register
VOP_HWC_FADING_CTRL	0x0168	W	0x00000000	Hwc fading contrl register
VOP_HWC_RESERVED1	0x016c	W	0x00000000	Hwc reserved
VOP_POST_DSP_HACT_INFO	0x0170	W	0x000a014a	Post scaler down horizontal start and end
VOP_POST_DSP_VACT_INFO	0x0174	W	0x000a00fa	Panel active horizontal scanning start point and end point

Name	Offset	Size	Reset Value	Description
VOP_POST_SCL_FACTOR_YRGB	0x0178	W	0x10001000	Post yrgb scaling factor
VOP_POST_RESERVED	0x017c	W	0x00000000	Post reserved
VOP_POST_SCL_CTRL	0x0180	W	0x00000000	Post scaling start point offset
VOP_POST_DSP_VACT_INFO_F1	0x0184	W	0x000a00fa	Panel active horizontal scanning start point and end point F1
VOP_DSP_HTOTAL_HS_END	0x0188	W	0x014a000a	Panel scanning horizontal width and hsync pulse end point
VOP_DSP_HACT_ST_END	0x018c	W	0x000a014a	Panel active horizontal scanning start point and end point
VOP_DSP_VTOTAL_VS_END	0x0190	W	0x00fa000a	Panel scanning vertical height and vsync pulse end point
VOP_DSP_VACT_ST_END	0x0194	W	0x000a00fa	Panel active vertical scanning start point and end point
VOP_DSP_VS_ST_END_F1	0x0198	W	0x00000000	Vertical scanning start point and vsync pulse end point of even filed in interlace mode
VOP_DSP_VACT_ST_END_F1	0x019c	W	0x00000000	Vertical scanning active start point and end point of even filed in interlace mode
VOP_PWM_CTRL	0x01a0	W	0x0000200a	PWM Control Register
VOP_PWM_PERIOD_HPR	0x01a4	W	0x00000000	PWM Period Register/High Polarity Capture Register
VOP_PWM_DUTY_LPR	0x01a8	W	0x00000000	PWM Duty Register/Low Polarity Capture Register
VOP_PWM_CNT	0x01ac	W	0x00000000	PWM Counter Register
VOP_BCSH_COLOR_BAR	0x01b0	W	0x00000000	Color bar config register
VOP_BCSH_BCS	0x01b4	W	0xd0010000	Brightness contrast saturation*contrast config register
VOP_BCSH_H	0x01b8	W	0x01000000	Sin hue and cos hue config register
VOP_BCSH_CTRL	0x01bc	W	0x00000000	BCSH contrl register
VOP_CABC_CTRL0	0x01c0	W	0x00ed8000	Content Adaptive Backlight Control register0
VOP_CABC_CTRL1	0x01c4	W	0x00fa0000	Content Adaptive Backlight Control register1
VOP_CABC_CTRL2	0x01c8	W	0x000110f0	Content Adaptive Backlight Control register2
VOP_CABC_CTRL3	0x01cc	W	0x00000000	Content Adaptive Backlight Control register3
VOP_CABC_GAUSS_LINE0_0	0x01d0	W	0x15110903	CABC gauss line config register00
VOP_CABC_GAUSS_LINE0_1	0x01d4	W	0x00030911	CABC gauss line config register01
VOP_CABC_GAUSS_LINE1_0	0x01d8	W	0x1a150b04	CABC gauss line config register10

Name	Offset	Size	Reset Value	Description
VOP_CABC_GAUSS_LINE1_1	0x01dc	W	0x00040b15	CABC gauss line config register11
VOP_CABC_GAUSS_LINE2_0	0x01e0	W	0x15110903	CABC gauss line config register20
VOP_CABC_GAUSS_LINE2_1	0x01e4	W	0x00030911	CABC gauss line config register21
VOP_FRC_LOWER01_0	0x01e8	W	0x12844821	FRC lookup table config register010
VOP_FRC_LOWER01_1	0x01ec	W	0x21488412	FRC lookup table config register011
VOP_FRC_LOWER10_0	0x01f0	W	0xa55a9696	FRC lookup table config register100
VOP_FRC_LOWER10_1	0x01f4	W	0x5aa56969	FRC lookup table config register101
VOP_FRC_LOWER11_0	0x01f8	W	0xdeb77bed	FRC lookup table config register110
VOP_FRC_LOWER11_1	0x01fc	W	0xed7bb7de	FRC lookup table config register111
VOP_INTR_EN0	0x0280	W	0x00000000	Interrupt enable register
VOP_INTR_CLEAR0	0x0284	W	0x00000000	Interrupt clear register
VOP_INTR_STATUS0	0x0288	W	0x00000000	interrupt status
VOP_INTR_RAW_STATUS0	0x028c	W	0x00000000	raw interrupt status
VOP_LINE_FLAG	0x02a0	W	0x00000000	Line flag config register
VOP_VOP_STATUS	0x02a4	W	0x00000000	vop status register
VOP_BLANKING_VALUE	0x02a8	W	0x00000000	Register0000 Abstract
VOP_MCU_BYPASS_PORT	0x02ac	W	0x00000000	MCU bypass port
VOP_WIN0_DSP_BG	0x02b0	W	0x00000000	Win0 layer background color
VOP_WIN1_DSP_BG	0x02b4	W	0x00000000	Win1 layer background color
VOP_WIN2_DSP_BG	0x02b8	W	0x00000000	Win2 layer background color
VOP_WIN3_DSP_BG	0x02bc	W	0x00000000	Win3 layer background color
VOP_YUV2YUV_WIN	0x02c0	W	0x00000000	win yuv2yuv control register
VOP_AUTO_GATING_EN	0x02cc	W	0x00000000	Auto gating enable
VOP_WIN0_YUV2YUV_Y2R_COE0	0x04e0	W	0x00000000	WIN0 yuv2yuv y2r cofficient
VOP_WIN0_YUV2YUV_Y2R_COE1	0x04e4	W	0x00000000	WIN0 yuv2yuv y2r cofficient
VOP_WIN0_YUV2YUV_Y2R_COE2	0x04e8	W	0x00000000	WIN0 yuv2yuv y2r cofficient
VOP_WIN0_YUV2YUV_Y2R_COE3	0x04ec	W	0x00000000	WIN0yuv2yuv y2r cofficient
VOP_WIN0_YUV2YUV_Y2R_COE4	0x04f0	W	0x00000000	WIN0 yuv2yuv y2r cofficient

Name	Offset	Size	Reset Value	Description
VOP_WIN0_YUV2YUV_Y2R_COE5	0x04f4	W	0x00000000	WIN0 yuv2yuv y2r cofficient
VOP_WIN0_YUV2YUV_Y2R_COE6	0x04f8	W	0x00000000	WIN0 yuv2yuv y2r cofficient
VOP_WIN0_YUV2YUV_Y2R_COE7	0x04fc	W	0x00000000	WIN0 yuv2yuv y2r cofficient
VOP_WIN0_YUV2YUV_R2R_COE0	0x0500	W	0x00000000	WIN0 yuv2yuv r2r cofficient
VOP_WIN0_YUV2YUV_R2R_COE1	0x0504	W	0x00000000	WIN0 yuv2yuv r2r cofficient
VOP_WIN0_YUV2YUV_R2R_COE2	0x0508	W	0x00000000	WIN0 yuv2yuv r2r cofficient
VOP_WIN0_YUV2YUV_R2R_COE3	0x050c	W	0x00000000	WIN0 yuv2yuv r2r cofficient
VOP_WIN0_YUV2YUV_R2R_COE4	0x0510	W	0x00000000	WIN0 yuv2yuv r2r cofficient
VOP_WIN0_YUV2YUV_R2R_COE5	0x0514	W	0x00000000	WIN0 yuv2yuv r2r cofficient
VOP_WIN0_YUV2YUV_R2R_COE6	0x0518	W	0x00000000	WIN0 yuv2yuv r2r cofficient
VOP_WIN0_YUV2YUV_R2R_COE7	0x051c	W	0x00000000	WIN0 yuv2yuv r2r cofficient
VOP_WIN0_YUV2YUV_R2Y_COE0	0x0520	W	0x00000000	WIN0 yuv2yuv r2y cofficient
VOP_WIN0_YUV2YUV_R2Y_COE1	0x0524	W	0x00000000	WIN0 yuv2yuv r2y cofficient
VOP_WIN0_YUV2YUV_R2Y_COE2	0x0528	W	0x00000000	WIN0 yuv2yuv r2y cofficient
VOP_WIN0_YUV2YUV_R2Y_COE3	0x052c	W	0x00000000	WIN0 yuv2yuv r2y cofficient
VOP_WIN0_YUV2YUV_R2Y_COE4	0x0530	W	0x00000000	WIN0 yuv2yuv r2y cofficient
VOP_WIN0_YUV2YUV_R2Y_COE5	0x0534	W	0x00000000	WIN0 yuv2yuv r2y cofficient
VOP_WIN0_YUV2YUV_R2Y_COE6	0x0538	W	0x00000000	WIN0 yuv2yuv r2y cofficient
VOP_WIN0_YUV2YUV_R2Y_COE7	0x053c	W	0x00000000	WIN0 yuv2yuv r2y cofficient
VOP_WIN2_YUV2YUV_Y2R_COE0	0x05a0	W	0x00000000	WIN2 yuv2yuv y2r cofficient
VOP_WIN2_YUV2YUV_Y2R_COE1	0x05a4	W	0x00000000	WIN2 yuv2yuv y2r cofficient
VOP_WIN2_YUV2YUV_Y2R_COE2	0x05a8	W	0x00000000	WIN2 yuv2yuv y2r cofficient

Name	Offset	Size	Reset Value	Description
VOP_WIN2_YUV2YUV_Y2R_COE3	0x05ac	W	0x00000000	WIN2 yuv2yuv y2r cofficient
VOP_WIN2_YUV2YUV_Y2R_COE4	0x05b0	W	0x00000000	WIN2 yuv2yuv y2r cofficient
VOP_WIN2_YUV2YUV_Y2R_COE5	0x05b4	W	0x00000000	WIN2 yuv2yuv y2r cofficient
VOP_WIN2_YUV2YUV_Y2R_COE6	0x05b8	W	0x00000000	WIN2 yuv2yuv y2r cofficient
VOP_WIN2_YUV2YUV_Y2R_COE7	0x05bc	W	0x00000000	WIN2 yuv2yuv y2r cofficient
VOP_WIN2_YUV2YUV_R2R_COE0	0x05c0	W	0x00000000	WIN2 yuv2yuv r2r cofficient
VOP_WIN2_YUV2YUV_R2R_COE1	0x05c4	W	0x00000000	WIN2 yuv2yuv r2r cofficient
VOP_WIN2_YUV2YUV_R2R_COE2	0x05c8	W	0x00000000	WIN2 yuv2yuv r2r cofficient
VOP_WIN2_YUV2YUV_R2R_COE3	0x05cc	W	0x00000000	WIN2 yuv2yuv r2r cofficient
VOP_WIN2_YUV2YUV_R2R_COE4	0x05d0	W	0x00000000	WIN2 yuv2yuv r2r cofficient
VOP_WIN2_YUV2YUV_R2R_COE5	0x05d4	W	0x00000000	WIN2 yuv2yuv r2r cofficient
VOP_WIN2_YUV2YUV_R2R_COE6	0x05d8	W	0x00000000	WIN2 yuv2yuv r2r cofficient
VOP_WIN2_YUV2YUV_R2R_COE7	0x05dc	W	0x00000000	WIN2 yuv2yuv r2r cofficient
VOP_WIN2_YUV2YUV_R2Y_COE0	0x05e0	W	0x00000000	WIN2 yuv2yuv r2y cofficient
VOP_WIN2_YUV2YUV_R2Y_COE1	0x05e4	W	0x00000000	WIN2 yuv2yuv r2y cofficient
VOP_WIN2_YUV2YUV_R2Y_COE2	0x05e8	W	0x00000000	WIN2 yuv2yuv r2y cofficient
VOP_WIN2_YUV2YUV_R2Y_COE3	0x05ec	W	0x00000000	WIN2 yuv2yuv r2y cofficient
VOP_WIN2_YUV2YUV_R2Y_COE4	0x05f0	W	0x00000000	WIN2 yuv2yuv r2y cofficient
VOP_WIN2_YUV2YUV_R2Y_COE5	0x05f4	W	0x00000000	WIN2 yuv2yuv r2y cofficient
VOP_WIN2_YUV2YUV_R2Y_COE6	0x05f8	W	0x00000000	WIN2 yuv2yuv r2y cofficient
VOP_WIN2_YUV2YUV_R2Y_COE7	0x05fc	W	0x00000000	WIN2 yuv2yuv r2y cofficient
VOP_HWC_LUT_ADDR	0x1800	W	0x00000000	Hwc lut base address
VOP_CABC_GAMMA_LUT_ADDR	0x1c00	W	0x00000000	CABC GAMMA lut base address

Name	Offset	Size	Reset Value	Description
VOP_GAMMA_LUT_ADDR	0x2000	W	0x00000000	GAMMA lut base address
VOP_MMU_DTE_ADDR	0x3f00	W	0x00000000	MMU current page Table address
VOP_MMU_STATUS	0x3f04	W	0x00000000	MMU status register
VOP_MMU_COMMAND	0x3f08	W	0x00000000	MMU command register
VOP_MMU_PAGE_FAULT_ADDR	0x3f0c	W	0x00000000	MMU logical address of last page fault
VOP_MMU_ZAP_ONE_LINE	0x3f10	W	0x00000000	MMU Zap cache line register
VOP_MMU_INT_RAWSTAT	0x3f14	W	0x00000000	MMU raw interrupt status register
VOP_MMU_INT_CLEAR	0x3f18	W	0x00000000	MMU raw interrupt status register
VOP_MMU_INT_MASK	0x3f1c	W	0x00000000	MMU raw interrupt status register
VOP_MMU_INT_STATUS	0x3f20	W	0x00000000	MMU raw interrupt status register
VOP_MMU_AUTO_GATING	0x3f24	W	0x00000000	MMU auto gating

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

3.5.3 Detail Register Description

VOP_REG_CFG_DONE
Address: Operational Base + offset (0x0000)
Register config done flag

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:9	RO	0x0	reserved
8	RW	0x0	reg_load_sys_en vop system register config done flag In the first setting of the register, the new value was saved into the mirror register. When all the system register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
7	RW	0x0	reg_load_fbdc_en vop fbdc register config done flag In the first setting of the register, the new value was saved into the mirror register. When all the fbdc register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
6	RW	0x0	reg_load_iep_en vop iep register config done flag In the first setting of the register, the new value was saved into the mirror register. When all the iep register config finish(only 2 signals direct_path_en,direct_path_layer_sel), writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.

Bit	Attr	Reset Value	Description
5	RW	0x0	reg_load_hwc_en vop hwc register config done flag In the first setting of the register, the new value was saved into the mirror register. When all the hwc register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
4	RW	0x0	reg_load_win3_en vop win3 register config done flag In the first setting of the register, the new value was saved into the mirror register. When all the win3 register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
3	RW	0x0	reg_load_win2_en vop win2 register config done flag In the first setting of the register, the new value was saved into the mirror register. When all the win2 register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
2	RW	0x0	reg_load_win1_en vop win1 register config done flag In the first setting of the register, the new value was saved into the mirror register. When all the win1 register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
1	RW	0x0	reg_load_win0_en vop win0 register config done flag In the first setting of the register, the new value was saved into the mirror register. When all the win0 register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.
0	WO	0x0	reg_load_en vop register config done flag In the first setting of the register, the new value was saved into the mirror register. When all the register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame.

VOP_VERSION_INFO
Address: Operational Base + offset (0x0004)

Version for vop

Bit	Attr	Reset Value	Description
31:24	RO	0x00	major IP major vertion used for IP structure
23:16	RO	0x00	minor minor vertion big feature change under same structure
15:0	RO	0x0000	svnbuild rtl current svn number

VOP_SYS_CTRL

Address: Operational Base + offset (0x0008)

System control register0

Bit	Attr	Reset Value	Description
31	RW	0x0	io_pad_clk_sel
30	RO	0x0	vop_field_tve_pol
29	RW	0x0	dac_sel dac output sel for tve in fpga dac output sel for tve in fpga 1'b0:dac 3 1'b1:dac 1
28	RW	0x0	genlock genlock for tve genlock for tve in fpga 1'b0:master mode 1'b1:slave mode
27	RW	0x0	uv_offset_en uv offset enable uv offset enable
26	RW	0x0	tve_mode tve mode 1'b0:NTSC 1'b1:PAL
25	RW	0x0	imd_tve_dclk_pol tve dclk pol tve dclk pol
24	RW	0x0	imd_tve_dclk_en tve dclk enable tve dclk enable

Bit	Attr	Reset Value	Description
23	RW	0x1	auto_gating_en LCDC layer axi-clk auto gating enable 1'b0 : disable auto gating 1'b1 : enable auto gating default auto gating enable
22	RW	0x0	vop_standby_en LCDC standby mode Writing "1" to turn LCDC into standby mode, All the layer would disable and the data transfer from frame buffer memory would stop at the end of current frame. The output would be blank. When writing "0" to this bit, standby mode would disable and the LCDC go back to work immediately. 1'b0 : disable 1'b1 : enable * Black display is recommended before setting standby mode enable.
21	RW	0x0	vop_dma_stop VOP DMA stop mode 1'b0 : disable 1'b1 : enable * If DMA is working, the stop mode would not be active until current bus transfer is finished.
20	RW	0x0	vop_field_tve_timing_pol
19	RW	0x0	win23_pri_opt_mode 1'b0: win2 win3 dma priority enalbe 1'b1: win2 win3 dma priority disable
18	RW	0x0	post_lb_mode 1'b0 : 4x4096 1'b1 : 8x2048
17	RO	0x0	reserved
16	RW	0x0	overlay_mode 1'b0: RGB overlay 1'b1: YUV overlay
15	RW	0x0	mipi_out_en 1'b0 : gating output clk ,data and control signal 1'b1 : mipi interface enable
14	RW	0x0	edp_out_en 1'b0 : gating output clk ,data and control signal 1'b1 : edp interface enable
13	RW	0x0	hdmi_out_en 1'b0 : gating output clk ,data and control signal 1'b1 : hdmi interface enable

Bit	Attr	Reset Value	Description
12	RW	0x1	rgb_out_en 1'b0 : gating output clk ,data and control signal 1'b1 : rgb/lvds interface enable
11	RW	0x1	dp_out_en 1'b0 : gating output clk ,data and control signal 1'b1 : dp interface enable
10	RW	0x0	edpi_wms_fs edpi wms mode ， frame st signal write "1": edpi_wms_mode frame start (when other register is config done) read : wms mode hold status
9	RW	0x0	edpi_wms_mode 1'b1: mipi command mode
8	RW	0x0	edpi_halt_en mipi flow ctrl enable
7:3	RO	0x0	reserved
2:1	RW	0x0	direct_path_layer_sel direct path layer select 2'b00 : select win0 2'b01 : select win1 2'b10 : select win2 2'b11 : select win3
0	RW	0x0	direct_path_en iep direct path enable signal 1'b0 : disable iep direct path 1'b1 : enable iep direct path

VOP_SYS_CTRL1
Address: Operational Base + offset (0x000c)
System control register1

Bit	Attr	Reset Value	Description
31	RW	0x0	dsp_fp_standby
30:25	RO	0x0	reserved
24	RW	0x0	reg_done_frm 1’b0: every frame valid 1’b1: every field valid
23:22	RW	0x0	noc_hurry_w_value 2'b00: low priority 2'b11: high priority
21:20	RW	0x0	noc_hurry_w_mode 2'b00: noc_hurry_w disable 2'b01: left 1/4 fifo empty 2'b10: left 1/2 fifo empty 2'b11: left 3/4 fifo empty

Bit	Attr	Reset Value	Description
19:18	RO	0x0	reserved
17:13	RW	0x1d	axi_outstanding_max_num axi bus max outstanding number
12	RW	0x0	axi_max_outstanding_en axi bus max outstanding enable
11:10	RW	0x0	noc_win_qos Noc win qos
9	RW	0x0	noc_qos_en Noc qos enable
8:3	RW	0x00	noc_hurry_threshold Noc hurry threshold value
2:1	RW	0x0	noc_hurry_value Noc hurry value
0	RW	0x0	noc_hurry_en Noc hurry enable

VOP_DSP_CTRL0
Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31	RO	0x0	dsp_field
30:26	RO	0x0	reserved
25	RW	0x0	sw_tve_output_sel
24	RO	0x0	reserved
23	RW	0x0	dsp_y_mir_en 1'b0 : no y_mirror 1'b1 : y_mirror
22	RW	0x0	dsp_x_mir_en 1'b0 : no x_mirror 1'b1 : x_mirror
21	RW	0x0	dsp_yuv_clip YCrCb clip 1'b0 : disable, YCbCr no clip 1'b1 : enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
20	RW	0x0	dsp_ccir656_avg Cb-Cr filter in CCIR656 mode 1'b0 : drop mode 1'b1 : average mode
19	RW	0x0	dsp_black_en Black display mode When this bit enable, the pixel data output is all black (0x000000)

Bit	Attr	Reset Value	Description
18	RW	0x0	dsp_blank_en Blank display mode When this bit enable, the Hsync/Vsync/Den output is blank
17	RW	0x0	dsp_out_zero Hsync/Vsync/Den output software ctrl 1'b0 : normal output 1'b1 : all output '0'
16	RW	0x0	dsp_dummy_swap Display dummy swap enable 1'b0 : B+G+R+dummy 1'b1 : dummy+B+G+R
15	RW	0x0	dsp_delta_swap Display delta swap enable 1'b0 : disable 1'b1 : enable *See detail description in Delta display charpter.
14	RW	0x0	dsp_rg_swap Display output red and green swap enable 1'b0 : RGB 1'b1 : GRB
13	RW	0x0	dsp_rb_swap Display output red and blue swap enable 1'b0 : RGB 1'b1 : BGR
12	RW	0x0	dsp_bg_swap Display output blue and green swap enable 1'b0 : RGB 1'b1 : RBG
11	RW	0x0	dsp_field_pol field polarity when interlace dsp 1'b0 : normal 1'b1 : invert
10	RW	0x0	dsp_interlace Interlace display enable 1'b0 : disable 1'b1 : enable *This mode is related to the ITU-R656 output, the display timing of odd field must be set correctly. (lcdc_dsp_vs_st_end_f1/lcdc_dsp_vact_end_f1)
9	RW	0x0	dsp_ddr_phase dclk phase lock 1'b0 : no lock 1'b1 : lock every line

Bit	Attr	Reset Value	Description
8	RW	0x0	dsp_dclk_ddr dclk output mode 1'b0 : SDR 1'b1 : DDR
7:6	RO	0x0	reserved
5	RW	0x0	p2i_en
4	RW	0x0	sw_core_dclk_sel 1'b0: dclk_core sel dclk 1'b1: dclk_core sel dclk div2
3:0	RW	0x0	dsp_out_mode Display output format 4'b0000: Parallel 24-bit RGB888 output R[7:0],G[7:0],B[7:0] 4'b0001: Parallel 18-bit RGB666 output 6'b0,R[5:0],G[5:0],B[5:0] 4'b0010: Parallel 16-bit RGB565 output 8'b0,R[4:0],G[5:0],B[4:0] 4'b0011: Parallel 24-bit RGB888 double pixel mix out phase0:G1[3:0],B1[7:0],G0[3:0],B0[7:0] phase1:R1[7:0],G1[7:4],R0[7:0],G0[7:4] 4'b0100: Serial 2x12-bit 12'b0,G[3:0],B[7:0] + 12'b0,R[7:0],G[7:4] 4'b0101: ITU-656 output mode0 16'b0,pixel_data[7:0] 4'b0110: ITU-656 output mode1 8'b0,pixel_data[7:0],8'b0 4'b0111: ITU-656 output mode2 9'b0,pixel_data[7:0],7'b0 4'b1000: Serial 3x8-bit RGB888 16'b0, B[7:0]+16'b0,G[7:0]+16'b0,R[7:0] 4'b1100: Serial 3x8-bit RGB888 + dummy 16'b0, B[7:0]+16'b0,G[7:0]+16'b0,R[7:0] + dummy 4'b1110: YUV420 output for HDMI 4'b1100: DP_YUV422 4'b1101: DP_YUV420 4'b1111: Parallel 30-bit RGBaaa output R[9:0],G[9:0],B[9:0] Others: Reserved.

VOP_DSP_CTRL1
Address: Operational Base + offset (0x0014)
Display control register1

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31	RW	0x0	mipi_dclk_pol DCLK invert enable 1'b0 : normal 1'b1 : invert default dclk invert
30	RW	0x0	mipi_den_pol DEN polarity 1'b0 : positive 1'b1 : negative
29	RW	0x0	mipi_vsync_pol VSYNC polarity 1'b0 : negative 1'b1 : positive
28	RW	0x0	mipi_hsync_pol HSYNC polarity 1'b0 : negative 1'b1 : positive
27	RW	0x0	edp_dclk_pol DCLK invert enable 1'b0 : normal 1'b1 : invert default dclk invert
26	RW	0x0	edp_den_pol DEN polarity 1'b0 : positive 1'b1 : negative
25	RW	0x0	edp_vsync_pol VSYNC polarity 1'b0 : negative 1'b1 : positive
24	RW	0x0	edp_hsync_pol HSYNC polarity 1'b0 : negative 1'b1 : positive
23	RW	0x0	hdmi_dclk_pol DCLK invert enable 1'b0 : normal 1'b1 : invert default dclk invert
22	RW	0x0	hdmi_den_pol DEN polarity 1'b0 : positive 1'b1 : negative

Bit	Attr	Reset Value	Description
21	RW	0x0	hdmi_vsync_pol VSYNC polarity 1'b0 : negative 1'b1 : positive
20	RW	0x0	hdmi_hsync_pol HSYNC polarity 1'b0 : negative 1'b1 : positive
19	RW	0x0	dp_lvds_dclk_pol DCLK invert enable 1'b0 : normal 1'b1 : invert default dclk invert
18	RW	0x0	dp_lvds_den_pol DEN polarity 1'b0 : positive 1'b1 : negative
17	RW	0x0	dp_lvds_vsync_pol VSYNC polarity 1'b0 : negative 1'b1 : positive
16	RW	0x0	dp_lvds_hsync_pol HSYNC polarity 1'b0 : negative 1'b1 : positive
15:14	RW	0x3	dsp_layer3_sel layer3 selection
13:12	RW	0x2	dsp_layer2_sel layer2 selection
11:10	RW	0x1	dsp_layer1_sel layer1 selection
9:8	RW	0x0	dsp_layer0_sel layer0 selection
7	RW	0x0	update_gamma_lut 1'b0:no update gamma_lut 1'b1:update gamma_lut
6	RW	0x0	dither_up_en 1'b0 : no dither up 1'b1 : rgb565 dither up to rgb888
5	RO	0x0	reserved
4	RW	0x0	dither_down_sel dither down mode select 2'b0 : allegro 2'b1 : FRC

Bit	Attr	Reset Value	Description
3	RW	0x0	dither_down_mode Dither-down mode 1'b0 : RGB888 to RGB565 1'b1 : RGB888 to RGB666
2	RW	0x0	dither_down_en Dither-down enable 1'b0 : disable 1'b1 : enable
1	RW	0x0	pre_dither_down_en 10bit -> 8bit (allegro)
0	RW	0x0	dsp_lut_en Display LUT ram enable 1'b0 : disable 1'b1 : enable *This bit should be "0" when CPU updates the LUT, and should be "1" when Display LUT mode enable.

VOP_DSP_BG
Address: Operational Base + offset (0x0018)
Background color

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	dsp_bg_red Background Red color 8bit red color
15:8	RW	0x00	dsp_bg_green Background Green color 8bit green color
7:0	RW	0x00	dsp_bg_blue Background Blue color 8bit blue color

VOP_MCU_CTRL
Address: Operational Base + offset (0x001c)
MCU mode control register

Bit	Attr	Reset Value	Description
31	RW	0x0	mcu_type MCU LCD output SELECT
30	RW	0x0	mcu_bypass MCU LCD BYPASS MODE Select
29	RW	0x0	mcu_rs MCU LCD RS Select
28	W1C	0x0	mcu_frame_st Write"1" : MCU HOLD Mode Frame Start Read : MCU/LCDC standby HOLD status

Bit	Attr	Reset Value	Description
27	RW	0x0	mcu_hold_mode MCU HOLD Mode Select
26	RW	0x0	mcu_clk_sel MCU_CLK_SEL for MCU bypass 1'b1 : MCU BYPASS sync with DCLK 1'b0 : MCU BYPASS sync with HCLK
25:20	RW	0x07	mcu_rw_pend MCU_RW signal end point (0-63)
19:16	RW	0x1	mcu_rw_pst MCU_RW signal start point (0-15)
15:10	RW	0x07	mcu_cs_pend MCU_CS signal end point (0-63)
9:6	RW	0x0	mcu_cs_pst MCU_CS signal start point (0-15)
5:0	RW	0x08	mcu_pix_total MCU LCD Interface writing period (1-63)

VOP_WIN0_CTRL0
Address: Operational Base + offset (0x0030)
Win0 ctrl register0

Bit	Attr	Reset Value	Description
31:30	RW	0x0	win0_dma_burst_length WIN0 DMA read Burst length 2'b00 : burst16 (burst 15 in rgb888 pack mode) 2'b01 : burst8 (burst 12 in rgb888 pack mode) 2'b10 : burst4 (burst 6 in rgb888 pack mode) 2'b11 : reserved
29:25	RW	0x1d	win0_axi_outstanding_max_num win0 out standing max number
24	RW	0x0	win0_axi_max_outstanding_en 1'b0 : disable 1'b1 : enable
23	RO	0x0	reserved
22	RW	0x0	win0_y_mir_en 1'b0 : no y_mirror 1'b1 : y_mirror
21	RW	0x0	win0_x_mir_en 1'b0 : no x_mirror 1'b1 : x_mirror
20	RW	0x0	win0_yuv_clip YCrCb clip 1'b0 : disable, YCbCr no clip 1'b1 : enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239

Bit	Attr	Reset Value	Description
19	RW	0x0	win0_cbr_deflick Win0 Cbr deflick mode 1'b0 : disable 1'b1 : enable
18	RW	0x0	win0_yrgb_deflick win0 YRGB deflick mode 1'b0 : disable 1'b1 : enable
17	RW	0x0	win0_yuyv win0_data_fmt[3]
16	RW	0x0	win0_hw_pre_mul_en 1'b0: no hardware pre multiply mode 1'b1: hardware pre multiply mode
15	RW	0x0	win0_uv_swap Win0 CbCr swap 1'b0 : CrCb 1'b1 : CbCr
14	RW	0x0	win0_mid_swap Win0 Y middle swap 1'b0 : Y3Y2Y1Y0 1'b1 : Y3Y1Y2Y0
13	RW	0x0	win0_alpha_swap win0 alpha swap 1'b0 : ARGB 1'b1 : RGBA
12	RW	0x0	win0_rb_swap win0 RGB RED and BLUE swap 1'b0 : RGB 1'b1 : BGR
11:10	RW	0x0	win0_csc_mode Win0 YUV2RGB or RGB2YUV Color space conversion(YUV2RGB): 2'b00 : mpeg 2'b01 : jpeg 2'b10 : hd 2'b11 : mpeg Color space conversion(RGB2YUV): 2'bx0: BT601 2'bx1: BT709
9	RW	0x0	win0_no_outstanding win0 AXI master read outstanding 1'b0 : enable 1'b1 : disable

Bit	Attr	Reset Value	Description
8	RW	0x0	win0_interlace_read Win0 interlace read mode 1'b0 : disable 1'b1 : enable
7:5	RW	0x2	win0_lb_mode win0 line buffer mode,calc by driver.
4	RW	0x0	win0_fmt_10 0: yuv 8bit fmt mode 1: yuv 10bit fmt mode
3:1	RW	0x0	win0_data_fmt vld_reg 4'b0000 : ARGB888 4'b0001 : RGB888 4'b0010 : RGB565 4'b0100 : YcbCr420 4'b0101 : YcbCr422 4'b0110 : YcbCr444 4'b1000: YCrYCb422 4'b1001: YCrYCb420 4'b1010: CrYCbY422 4'b1011: CrYCbY420
0	RW	0x0	win0_en 1'b0 : disable 1'b1 : enable

VOP_WIN0_CTRL1
Address: Operational Base + offset (0x0034)
Win0 ctrl register1

Bit	Attr	Reset Value	Description
31	RW	0x0	win0_cbr_vsd_mode win0 vertical scaler down mode select 1'b0 : bilinear 1'b1 : average
30	RW	0x0	win0_cbr_vsu_mode win0 vertical scaler down mode select 1'b0 : bilinear 1'b1 : bicubic
29:28	RW	0x0	win0_cbr_hsd_mode win0 horizontal scaler down mode select 2'b00 : bilinear 2'b01 : bicubic 2'b10 : average

Bit	Attr	Reset Value	Description
27:26	RW	0x0	win0_cbr_ver_scl_mode 2'b00 : no scale 2'b01 : scale up 2'b10 : scale down 2'b11 : no scale
25:24	RW	0x0	win0_cbr_hor_scl_mode 2'b00 : no scale 2'b01 : scale up 2'b10 : scale down 2'b11 : no scale
23	RW	0x0	win0_yrgb_vsd_mode win0 vertical scaler down mode select 1'b0 : bilinear 1'b1 : average
22	RW	0x0	win0_yrgb_vsu_mode win0 vertical scaler down mode select 1'b0 : bilinear 1'b1 : bicubic
21:20	RW	0x0	win0_yrgb_hsd_mode win0 horizontal scaler down mode select 2'b00 : bilinear 2'b01 : average
19:18	RW	0x0	win0_yrgb_ver_scl_mode 2'b00 : no scale 2'b01 : scale up 2'b10 : scale down 2'b11 : no scale
17:16	RW	0x0	win0_yrgb_hor_scl_mode 2'b00 : no scale 2'b01 : scale up 2'b10 : scale down 2'b11 : no scale
15	RW	0x0	win0_line_load_mode when yuv fmt, 1'b0: load data by axi trans 1'b1: load data by lines
14:12	RW	0x0	win0_cbr_axi_gather_num win0 axi cbr data transfer gather number
11:8	RW	0x0	win0_yrgb_axi_gather_num win0 axi yrgb data transfer gather number
7	RW	0x0	win0_vsd_cbr_gt2 cbr_src/cbr_dst >= 2
6	RW	0x0	win0_vsd_cbr_gt4 cbr_src/cbr_dst >= 4

Bit	Attr	Reset Value	Description
5	RW	0x0	win0_vsd_yrgb_gt2 yrgb_src/yrgb_dst >= 2
4	RW	0x0	win0_vsd_yrgb_gt4 yrgb_src/yrgb_dst >= 4
3:2	RW	0x0	win0_bic_coe_sel 2'b00 : PRECISE 2'b01 : SPLINE 2'b10 : CATROM 2'b11 : MITCHELL
1	RW	0x0	win0_cbr_axi_gather_en win0 axi bus cbr data gather transfer enable
0	RW	0x0	win0_yrgb_axi_gather_en win0 axi bus yrgb data gather transfer enable

VOP_WIN0_COLOR_KEY
Address: Operational Base + offset (0x0038)
Win0 color key register

Bit	Attr	Reset Value	Description
31	RW	0x0	win0_key_en Win0 transparency color key enable 1'b0 : disable; 1'b1 : enable;
30:24	RO	0x0	reserved
23:0	RW	0x000000	win0_key_color Win0 key color 24 bit RGB888

VOP_WIN0_VIR
Address: Operational Base + offset (0x003c)
Win0 virtual stride

Bit	Attr	Reset Value	Description
31:16	RW	0x0140	win0_vir_stride_uv Number of words of Win0 uv Virtual width
15:0	RW	0x0140	win0_vir_stride Win0 Virtual stride Number of words of Win0 yrgb Virtual width ARGB888 : win0_vir_width RGB888 : (win0_vir_width*3/4) + (win0_vir_width%3) RGB565 : ceil(win0_vir_width/2) YUV : ceil(win0_vir_width/4)

VOP_WIN0_YRGB_MST
Address: Operational Base + offset (0x0040)
Win0 YRGB memory start address

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win0_yrgb_mst win0 YRGB frame buffer memory start address

VOP_WIN0_CBR_MST
Address: Operational Base + offset (0x0044)
Win0 Cbr memory start address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win0_cbr_mst win0 CBR frame buffer memory start address

VOP_WIN0_ACT_INFO
Address: Operational Base + offset (0x0048)
Win0 active window width/height

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x00ef	win0_act_height Win0 active(original) window height win_act_height = (win0 vertical size -1)
15:13	RO	0x0	reserved
12:0	RW	0x013f	win0_act_width Win0 active(original) window width win_act_width = (win0 horizontial size -1)

VOP_WIN0_DSP_INFO
Address: Operational Base + offset (0x004c)
Win0 display width/height on panel

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0ef	win0_dsp_height Win0 display window height win0_dsp_height = (win0 vertical size -1)
15:12	RO	0x0	reserved
11:0	RW	0x13f	win0_dsp_width Win0 display window width win0_dsp_width = (win0 horizontial size -1)

VOP_WIN0_DSP_ST
Address: Operational Base + offset (0x0050)
Win0 display start point on panel

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	win0_dsp_yst Win0 vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12:0	RW	0x000a	win0_dsp_xst Win0 horizontal start point(x) of the Panel scanning

VOP_WIN0_SCL_FACTOR_YRGB
Address: Operational Base + offset (0x0054)
Win0 YRGB scaling factor

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	win0_vs_factor_yrgb Win0 YRGB vertical scaling factor: factor=((LCDC_WIN0_ACT_INFO[31:16]) /(LCDC_WIN0_DSP_INFO[31:16]))*2^12
15:0	RW	0x1000	win0_hs_factor_yrgb Win0 YRGB horizontal scaling factor: factor=((LCDC_WIN0_ACT_INFO[15:0]) /(LCDC_WIN0_DSP_INFO[15:0]))*2^12

VOP_WIN0_SCL_FACTOR_CBR
Address: Operational Base + offset (0x0058)
Win0 Cbr scaling factor

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	win0_vs_factor_cbr Win0 CBR vertical scaling factor: YCbCr420: factor=((LCDC_WIN0_ACT_INFO[31:16]/ 2) /(LCDC_WIN0_DSP_INFO[31:16]))*2^12 YCbCr422,YCbCr444: factor=((LCDC_WIN0_ACT_INFO[31:16]) /(LCDC_WIN0_DSP_INFO[31:16]))*2^12
15:0	RW	0x1000	win0_hs_factor_cbr Win0 CBR horizontal scaling factor: YCbCr422,YCbCr420: factor=((LCDC_WIN0_ACT_INFO[15:0]/2) /(LCDC_WIN0_DSP_INFO[15:0]))*2^12 YCbCr444: factor=((LCDC_WIN0_ACT_INFO[15:0]) /(LCDC_WIN0_DSP_INFO[15:0]))*2^12

VOP_WIN0_SCL_OFFSET
Address: Operational Base + offset (0x005c)
Win0 scaling start point offset

Bit	Attr	Reset Value	Description
31:24	RW	0x00	win0_vs_offset_cbr Cbr Vertical scaling start point offset (0x00~0xff)/0x100 = 0~0.99

Bit	Attr	Reset Value	Description
23:16	RW	0x00	win0_vs_offset_yrgb Y Vertical scaling start point offset (0x00~0xff)/0x100 = 0~0.99
15:8	RW	0x00	win0_hs_offset_cbr Cbr Horizontal scaling start point offset (0x00~0xff)/0x100 = 0~0.99
7:0	RW	0x00	win0_hs_offset_yrgb Y Horizontal scaling start point offset (0x00~0xff)/0x100 = 0~0.99

VOP_WIN0_SRC_ALPHA_CTRL
Address: Operational Base + offset (0x0060)
Win0 alpha source control register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	win0_fading_value win0 fading value ,8bits
23:16	RW	0x00	win0_src_global_alpha src global alpha
15:9	RO	0x0	reserved
8:6	RW	0x0	win0_src_factor_mode src factor mode
5	RW	0x0	win0_src_alpha_cal_mode src alpha calc mode
4:3	RW	0x0	win0_src_blend_mode src blend mode
2	RW	0x0	win0_src_alpha_mode src alpha mode
1	RW	0x0	win0_src_color_mode src color mode
0	RW	0x0	win0_src_alpha_en src alpha en

VOP_WIN0_DST_ALPHA_CTRL
Address: Operational Base + offset (0x0064)
Win0 alpha destination control register

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:6	RW	0x0	win0_dst_factor_mode dst factor mode
5:0	RW	0x00	win0_dst_m0_reserved reserved

VOP_WIN0_FADING_CTRL
Address: Operational Base + offset (0x0068)
Win0 fading contrl register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	layer0_fading_en fading enable
23:16	RW	0x00	layer0_fading_offset_b fading offset blue value
15:8	RW	0x00	layer0_fading_offset_g fading offset green value
7:0	RW	0x00	layer0_fading_offset_r fading offset red value

VOP_WIN0_CTRL2
Address: Operational Base + offset (0x006c)
Win0 ctrl register2

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x2	win_rid_win0_cbr axi read id of win0 cbr channel
3:0	RW	0x1	win_rid_win0_yrgb axi read id of win0 yrgb channel

VOP_WIN1_CTRL0
Address: Operational Base + offset (0x0070)
Win1 ctrl register0

Bit	Attr	Reset Value	Description
31:30	RW	0x0	win1_dma_burst_length WIN1 DMA read Burst length 2'b00 : burst16 (burst 15 in rgb888 pack mode) 2'b01 : burst8 (burst 12 in rgb888 pack mode) 2'b10 : burst4 (burst 6 in rgb888 pack mode) 2'b11 : reserved
29:25	RW	0x1d	win1_axi_max_outstanding_num win1 out standing max number
24	RW	0x0	win1_axi_max_outstanding_en 1'b0 : disable 1'b1 : enable
23	RO	0x0	reserved
22	RW	0x0	win1_y_mir_en 1'b0 : no y_mirror 1'b1 : y_mirror
21	RW	0x0	win1_x_mir_en 1'b0 : no x_mirror 1'b1 : x_mirror

Bit	Attr	Reset Value	Description
20	RW	0x0	win1_yuv_clip YCrCb clip 1'b0 : disable, YCbCr no clip 1'b1 : enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CbCr clip: 16~239
19	RW	0x0	win1_cbr_deflick Win1 Cbr deflick mode 1'b0 : disable 1'b1 : enable
18	RW	0x0	win1_yrgb_deflick win1 YRGB deflick mode 1'b0 : disable 1'b1 : enable
17	RW	0x0	win1_yuyv win1_data_fmt[3]
16	RW	0x0	win1_hw_pre_mul_en 1'b0: no hardware pre multiply mode 1'b1: hardware pre multiply mode
15	RW	0x0	win1_uv_swap Win1 CbCr swap 1'b0 : CrCb 1'b1 : CbCr
14	RW	0x0	win1_mid_swap Win1 Y middle 8-bit swap 1'b0 : Y3Y2Y1Y0 1'b1 : Y3Y1Y2Y0
13	RW	0x0	win1_alpha_swap win1 alpha swap 1'b0 : ARGB 1'b1 : RGBA
12	RW	0x0	win1_rb_swap win1 RGB RED and BLUE swap 1'b0 : RGB 1'b1 : BGR
11:10	RW	0x0	win1_csc_mode Win1 YUV2RGB or RGB2YUV Color space conversion(YUV2RGB): 2'b00 : mpeg 2'b01 : jpeg 2'b10 : hd 2'b11 : mpeg Color space conversion(RGB2YUV): 2'bx0: BT601 2'bx1: BT709

Bit	Attr	Reset Value	Description
9	RW	0x0	win1_no_outstanding win1 AXI master read outstanding 1'b0 : enable 1'b1 : disable
8	RW	0x0	win1_interlace_read Win1 interlace read mode 1'b0 : disable 1'b1 : enable
7:5	RW	0x2	win1_lb_mode win1 line buffer mode,calc by driver.
4	RW	0x0	win1_fmt_10 1'b0: yuv 8bit fmt mode 1'b1: yuv 10bit fmt mode
3:1	RW	0x0	win1_data_fmt 3'b000 : ARGB888 3'b001 : RGB888 3'b010 : RGB565 3'b100 : YcbCr420 3'b101 : YcbCr422 3'b110 : YcbCr444
0	RW	0x0	win1_en 1'b0 : disable 1'b1 : enable

VOP_WIN1_CTRL1
Address: Operational Base + offset (0x0074)
Win1 ctrl register1

Bit	Attr	Reset Value	Description
31	RW	0x0	win1_cbr_vsd_mode win1 vertical scaler down mode select 1'b0 : bilinear 1'b1 : average
30	RW	0x0	win1_cbr_vsu_mode win1 vertical scaler up mode select 1'b0 : bilinear 1'b1 : bicubic
29:28	RW	0x0	win1_cbr_hsd_mode win1 horizontal scaler down mode select 2'b00 : bilinear 2'b01 : bicubic 2'b10 : average

Bit	Attr	Reset Value	Description
27:26	RW	0x0	win1_cbr_ver_scl_mode 2'b00 : no scale 2'b01 : scale up 2'b10 : scale down 2'b11 : no scale
25:24	RW	0x0	win1_cbr_hor_scl_mode 2'b00 : no scale 2'b01 : scale up 2'b10 : scale down 2'b11 : no scale
23	RW	0x0	win1_yrgb_vsd_mode win1 vertical scaler down mode select 1'b0 : bilinear 1'b1 : average
22	RW	0x0	win1_yrgb_vsu_mode win1 vertical scaler up mode select 1'b0 : bilinear 1'b1 : bicubic
21:20	RW	0x0	win1_yrgb_hsd_mode win1 horizontal scaler down mode select 2'b00 : bilinear 2'b01 : average
19:18	RW	0x0	win1_yrgb_ver_scl_mode 2'b00 : no scale 2'b01 : scale up 2'b10 : scale down 2'b11 : no scale
17:16	RW	0x0	win1_yrgb_hor_scl_mode 2'b00 : no scale 2'b01 : scale up 2'b10 : scale down 2'b11 : no scale
15	RW	0x0	win1_line_load_mode when yuv fmt, 1'b0: load data by pixels 1'b1: load data by lines
14:12	RW	0x0	win1_cbr_axi_gather_num win1 axi cbr data transfer gather number
11:8	RW	0x0	win1_yrgb_axi_gather_num win1 axi yrgb data transfer gather number
7	RW	0x0	win1_vsd_cbr_gt2 cbr_src/cbr_dst >= 2
6	RW	0x0	win1_vsd_cbr_gt4 cbr_src/cbr_dst >= 4

Bit	Attr	Reset Value	Description
5	RW	0x0	win1_vsd_yrgb_gt2 yrgb_src/yrgb_dst >= 2
4	RW	0x0	win1_vsd_yrgb_gt4 yrgb_src/yrgb_dst >= 4
3:2	RW	0x0	win1_bic_coe_sel 2'b00 : PRECISE 2'b01 : SPLINE 2'b10 : CATROM 2'b11 : MITCHELL
1	RW	0x0	win1_cbr_axi_gather_en win1 cbr axi bus gather enable
0	RW	0x0	win1_yrgb_axi_gather_en win1 yrgb axi bus gather enable

VOP_WIN1_COLOR_KEY
Address: Operational Base + offset (0x0078)
Win1 color key register

Bit	Attr	Reset Value	Description
31	RW	0x0	win1_key_en Win1 transparency color key enable 1'b0 : disable; 1'b1 : enable;
30:24	RO	0x0	reserved
23:0	RW	0x000000	win1_key_color Win1 key color 24 bit RGB888

VOP_WIN1_VIR
Address: Operational Base + offset (0x007c)
win1 virtual stride

Bit	Attr	Reset Value	Description
31:16	RW	0x0140	win1_vir_stride_uv Number of words of Win1 uv Virtual width
15:0	RW	0x0140	win1_vir_stride Win1 Virtual stride Number of words of Win1 yrgb Virtual width ARGB888 : win1_vir_width RGB888 : (win1_vir_width*3/4) + (win1_vir_width%3) RGB565 : ceil(win1_vir_width/2) YUV : ceil(win1_vir_width/4)

VOP_WIN1_YRGB_MST
Address: Operational Base + offset (0x0080)
Win1 YRGB memory start address

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win1_yrgb_mst win1 YRGB frame buffer memory start address

VOP_WIN1_CBR_MST
Address: Operational Base + offset (0x0084)
Win1 Cbr memory start address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win1_cbr_mst win1 CBR frame buffer memory start address

VOP_WIN1_ACT_INFO
Address: Operational Base + offset (0x0088)
Win1 active window width/height

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x00ef	win1_act_height Win1 active(original) window height win_act_height = (win1 vertical size -1)
15:13	RO	0x0	reserved
12:0	RW	0x013f	win1_act_width Win1 active(original) window width win_act_width = (win1 horizontial size -1)

VOP_WIN1_DSP_INFO
Address: Operational Base + offset (0x008c)
Win1 display width/height on panel

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0ef	win1_dsp_height Win1 display window height win1_dsp_height = (win1 vertical size -1)
15:12	RO	0x0	reserved
11:0	RW	0x13f	win1_dsp_width Win1 display window width win1_dsp_width = (win1 horizontial size -1)

VOP_WIN1_DSP_ST
Address: Operational Base + offset (0x0090)
Win1 display start point on panel

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	win1_dsp_yst Win1 vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12:0	RW	0x000a	win1_dsp_xst Win1 horizontal start point(x) of the Panel scanning

VOP_WIN1_SCL_FACTOR_YRGB
Address: Operational Base + offset (0x0094)
Win1 YRGB scaling factor

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	win1_vs_factor_yrgb Win1 YRGB vertical scaling factor: factor=((LCDC_WIN1_ACT_INFO[31:16]) /(LCDC_WIN1_DSP_INFO[31:16]))*2^12
15:0	RW	0x1000	win1_hs_factor_yrgb Win1 YRGB horizontal scaling factor: factor=((LCDC_WIN1_ACT_INFO[15:0]) /(LCDC_WIN1_DSP_INFO[15:0]))*2^12

VOP_WIN1_SCL_FACTOR_CBR
Address: Operational Base + offset (0x0098)
Win1 Cbr scaling factor

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	win1_vs_factor_cbr Win1 CBR vertical scaling factor: YCbCr420: factor=((LCDC_WIN1_ACT_INFO[31:16]/ 2) /(LCDC_WIN1_DSP_INFO[31:16]))*2^12 YCbCr422,YCbCr444: factor=((LCDC_WIN1_ACT_INFO[31:16]) /(LCDC_WIN1_DSP_INFO[31:16]))*2^12
15:0	RW	0x1000	win1_hs_factor_cbr Win1 Cbr horizontal scaling factor: YCbCr422,YCbCr420: factor=((LCDC_WIN1_ACT_INFO[15:0]/2) /(LCDC_WIN1_DSP_INFO[15:0]))*2^12 YCbCr444: factor=((LCDC_WIN1_ACT_INFO[15:0]) /(LCDC_WIN1_DSP_INFO[15:0]))*2^12

VOP_WIN1_SCL_OFFSET
Address: Operational Base + offset (0x009c)
Win1 scaling start point offset

Bit	Attr	Reset Value	Description
31:24	RW	0x00	win1_vs_offset_cbr Cbr Vertical scaling start point offset (0x00~0xff)/0x100 = 0~0.99

Bit	Attr	Reset Value	Description
23:16	RW	0x00	win1_vs_offset_yrgb Y Vertical scaling start point offset (0x00~0xff)/0x100 = 0~0.99
15:8	RW	0x00	win1_hs_offset_cbr Cbr Horizontal scaling start point offset (0x00~0xff)/0x100 = 0~0.99
7:0	RW	0x00	win1_hs_offset_yrgb Y Horizontal scaling start point offset (0x00~0xff)/0x100 = 0~0.99

VOP_WIN1_SRC_ALPHA_CTRL
Address: Operational Base + offset (0x00a0)
Win1 alpha source control register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	win1_fading_value fading value,8bit
23:16	RW	0x00	win1_src_global_alpha src global alpha
15:9	RO	0x0	reserved
8:6	RW	0x0	win1_src_factor_mode src factor mode
5	RW	0x0	win1_src_alpha_cal_mode src alpha calc mode
4:3	RW	0x0	win1_src_blend_mode src blend mode
2	RW	0x0	win1_src_alpha_mode src alpha mode
1	RW	0x0	win1_src_color_mode src color mode
0	RW	0x0	win1_src_alpha_en src alpha en

VOP_WIN1_DST_ALPHA_CTRL
Address: Operational Base + offset (0x00a4)
Win1 alpha destination control register

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:6	RW	0x0	win1_dst_factor_m0 dst factor mode
5:0	RW	0x00	win1_dsp_m0_reserved reserved

VOP_WIN1_FADING_CTRL
Address: Operational Base + offset (0x00a8)
Win1 fading contrl register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	win1_fading_en fading enable
23:16	RW	0x00	win1_fading_offset_b fading offset blue value
15:8	RW	0x00	win1_fading_offset_g fading offset green value
7:0	RW	0x00	win1_fading_offset_r fading offset red value

VOP_WIN1_CTRL2
Address: Operational Base + offset (0x00ac)
Win1 ctrl register2

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x4	win_rid_win1_cbr axi read id of win1 cbr channel
3:0	RW	0x3	win_rid_win1_yrgb axi read id of win1 yrgb channel

VOP_WIN2_CTRL0
Address: Operational Base + offset (0x00b0)
win2 ctrl register0

Bit	Attr	Reset Value	Description
31	RW	0x0	win2_endian_swap3 Win2 region3 8pp palette data Big-endian/ Little-endian select 1'b0 : Big-endian 1'b1 : Little-endian
30	RW	0x0	win2_alpha_swap3 Win2 region3 RGB alpha swap 1'b0 : ARGB 1'b1 : RGBA
29	RW	0x0	win2_rb_swap3 Win2 region3 RGB Red and Blue swap 1'b0 : RGB 1'b1 : BGR
28	RW	0x0	win2_endian_swap2 Win2 region2 8pp palette data Big-endian/ Little-endian select 1'b0 : Big-endian 1'b1 : Little-endian
27	RW	0x0	win2_alpha_swap2 Win2 region2 RGB alpha swap 1'b0 : ARGB 1'b1 : RGBA

Bit	Attr	Reset Value	Description
26	RW	0x0	win2_rb_swap2 Win2 region2 RGB Red and Blue swap 1'b0 : RGB 1'b1 : BGR
25	RW	0x0	win2_endian_swap1 Win2 region1 8pp palette data Big-endian/ Little-endian select 1'b0 : Big-endian 1'b1 : Little-endian
24	RW	0x0	win2_alpha_swap1 Win2 region1 RGB alpha swap 1'b0 : ARGB 1'b1 : RGBA
23	RW	0x0	win2_rb_swap1 Win2 region1 RGB Red and Blue swap 1'b0 : RGB 1'b1 : BGR
22	RW	0x0	win2_endian_swap0 Win2 region0 8pp palette data Big-endian/ Little-endian select 1'b0 : Big-endian 1'b1 : Little-endian
21	RW	0x0	win2_alpha_swap0 Win2 region0 RGB alpha swap 1'b0 : ARGB 1'b1 : RGBA
20	RW	0x0	win2_rb_swap0 Win2 region0 RGB Red and Blue swap 1'b0 : RGB 1'b1 : BGR
19	RO	0x0	reserved
18:17	RW	0x0	win2_data_fmt3 Win2 region 3 data format 2'b00 : ARGB888 2'b01 : RGB888 2'b10 : RGB565 2'b11 : 8bpp
16	RW	0x0	win2_mst3_en win2 master3 enable 1'b0 : disable 1'b1 : enable
15	RO	0x0	reserved

Bit	Attr	Reset Value	Description
14:13	RW	0x0	win2_data_fmt2 Win2 region 2 data format 2'b00 : ARGB888 2'b01 : RGB888 2'b10 : RGB565 2'b11 : 8bpp
12	RW	0x0	win2_mst2_en win2 master2 enable 1'b0 : disable 1'b1 : enable
11	RO	0x0	reserved
10:9	RW	0x0	win2_data_fmt1 Win2 region 1 data format 2'b00 : ARGB888 2'b01 : RGB888 2'b10 : RGB565 2'b11 : 8bpp
8	RW	0x0	win2_mst1_en win2 master1 enable 1'b0 : disable 1'b1 : enable
7	RO	0x0	reserved
6:5	RW	0x0	win2_data_fmt0 Win2 region 0 data format 2'b00 : ARGB888 2'b01 : RGB888 2'b10 : RGB565 2'b11 : 8bpp
4	RW	0x0	win2_mst0_en win2 master0 enable 1'b0 : disable 1'b1 : enable
3:2	RW	0x0	win2_csc_mode Win2 RGB2YUV conversion mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
1	RW	0x0	win2_interlace_read Win2 interlace read mode 1'b0 : disable 1'b1 : enable

Bit	Attr	Reset Value	Description
0	RW	0x0	win2_en 1'b0 : disable 1'b1 : enable

VOP_WIN2_CTRL1
Address: Operational Base + offset (0x00b4)
win2 ctrl register1

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:20	RW	0x5	win_rid_win2 axi read id of win2 channel
19:17	RO	0x0	reserved
16	RW	0x0	win2_lut_en Win2 LUT ram enable 1'b0 : disable 1'b1 : enable *This bit should be "0" when CPU updates the LUT, and should be "1" when Win2 LUT mode enable.
15	RW	0x0	win2_y_mir_en 1'b0 : no y_mirror 1'b1 : y_mirror
14	RW	0x0	win2_no_outstanding Win2 AXI master read outstanding 1'b0 : enable 1'b1 : disable
13	RO	0x0	reserved
12:8	RW	0x1d	win2_axi_max_outstanding_num win2 axi max outstanding number
7:4	RW	0x0	win2_axi_gather_num win2 axi gather transfer number
3:2	RW	0x0	win2_dma_burst_length WIN2 DMA read Burst length 2'b00 : burst16 (burst 15 in rgb888 pack mode) 2'b01 : burst8 (burst 12 in rgb888 pack mode) 2'b10 : burst4 (burst 6 in rgb888 pack mode) 2'b11 : reserved
1	RW	0x0	win2_axi_max_outstanding_en 1'b0 : disable 1'b1 : enable
0	RW	0x0	win2_axi_gather_en 1'b0 : disable 1'b1 : enable

VOP_WIN2_VIR0_1
Address: Operational Base + offset (0x00b8)

Win2 virtual stride0 and virtaul stride1

Bit	Attr	Reset Value	Description
31:16	RW	0x0140	win2_vir_stride1 Win2 Virtual stride1 Number of words of Win2 Virtual1 width ARGB888 : win2_vir_width1 RGB888 : (win2_vir_width1 * 3/4) + (win2_vir_width1 % 3) RGB565 : ceil(win2_vir_width1 / 2) 8BPP : ceil(win2_vir_width1 / 4) 4BPP : ceil(win2_vir_width1 / 8) 2BPP : ceil(win2_vir_width1 / 16) 1BPP : ceil(win2_vir_width1 / 32)
15:0	RW	0x0140	win2_vir_stride0 Win2 Virtual stride0 Number of words of Win2 Virtual0 width ARGB888 : win2_vir_width0 RGB888 : (win2_vir_width0 * 3/4) + (win2_vir_width0 % 3) RGB565 : ceil(win2_vir_width0 / 2) 8BPP : ceil(win2_vir_width0 / 4) 4BPP : ceil(win2_vir_width0 / 8) 2BPP : ceil(win2_vir_width0 / 16) 1BPP : ceil(win2_vir_width0 / 32)

VOP_WIN2_VIR2_3

Address: Operational Base + offset (0x00bc)

Win2 virtual stride2 and virtaul stride3

Bit	Attr	Reset Value	Description
31:16	RW	0x0140	win2_vir_stride3 Win2 Virtual stride3 Number of words of Win2 Virtual3 width ARGB888 : win2_vir_width3 RGB888 : (win2_vir_width3 * 3/4) + (win2_vir_width3 % 3) RGB565 : ceil(win2_vir_width3 / 2) 8BPP : ceil(win2_vir_width3 / 4) 4BPP : ceil(win2_vir_width3 / 8) 2BPP : ceil(win2_vir_width3 / 16) 1BPP : ceil(win1_vir_width3 / 32)
15:0	RW	0x0140	win2_vir_stride2 Win2 Virtual stride2 Number of words of Win2 Virtual2 width ARGB888 : win2_vir_width2 RGB888 : (win2_vir_width2 * 3/4) + (win2_vir_width2 % 3) RGB565 : ceil(win2_vir_width2 / 2) 8BPP : ceil(win2_vir_width2 / 4) 4BPP : ceil(win2_vir_width2 / 8) 2BPP : ceil(win2_vir_width2 / 16) 1BPP : ceil(win1_vir_width2 / 32)

VOP_WIN2_MST0
Address: Operational Base + offset (0x00c0)
Win2 memory start address0

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win2_mst0 Win2 frame buffer memory start address0 *must be alianed to 8byte address

VOP_WIN2_DSP_INFO0
Address: Operational Base + offset (0x00c4)
Win2 display width0/height0 on panel

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0ef	win2_dsp_height0 Win2 display window height0 win2_dsp_height0 = size -1
15:12	RO	0x0	reserved
11:0	RW	0x13f	win2_dsp_width0 Win2 display window width0 win2_dsp_width = size -1

VOP_WIN2_DSP_ST0
Address: Operational Base + offset (0x00c8)
Win2 display start point0 on panel

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	win2_dsp_yst0 Win2 vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x000a	win2_dsp_xst0 Win2 horizontal start point(x) of the Panel scanning

VOP_WIN2_COLOR_KEY
Address: Operational Base + offset (0x00cc)
Win2 color key register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	win2_key_en Win2 transparency color key enable 1'b0 : disable; 1'b1 : enable;
23:0	RW	0x000000	win2_key_color Win2 key color

VOP_WIN2_MST1
Address: Operational Base + offset (0x00d0)
Win2 memory start address1

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win2_mst1 Win2 frame buffer memory start address1 *must be alianed to 8byte address

VOP_WIN2_DSP_INFO1
Address: Operational Base + offset (0x00d4)
Win2 display width1/height1 on panel

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0ef	win2_dsp_height1 Win2 display window height1 win2_dsp_height0 = size -1
15:12	RO	0x0	reserved
11:0	RW	0x13f	win2_dsp_width1 Win2 display window width1 win2_dsp_width = size -1

VOP_WIN2_DSP_ST1
Address: Operational Base + offset (0x00d8)
Win2 display start point1 on panel

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	win2_dsp_yst1 Win2 vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x000a	win2_dsp_xst1 Win2 horizontal start point(x) of the Panel scanning

VOP_WIN2_SRC_ALPHA_CTRL
Address: Operational Base + offset (0x00dc)
Win2 alpha source control register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	win2_fading_value fading value,8bits
23:16	RW	0x00	win2_src_global_alpha src global alpha
15:9	RO	0x0	reserved
8:6	RW	0x0	win2_src_factor_mode src factor mode
5	RW	0x0	win2_src_alpha_cal_mode src alpha cal mode

Bit	Attr	Reset Value	Description
4:3	RW	0x0	win2_src_blend_mode src blend mode
2	RW	0x0	win2_src_alpha_mode src alpha mode
1	RW	0x0	win2_src_color_mode src color mode
0	RW	0x0	win2_src_alpha_en src alpha en

VOP_WIN2_MST2
Address: Operational Base + offset (0x00e0)
Win2 memory start address2

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win2_mst2 Win2 frame buffer memory start address2 *must be alianed to 8byte address

VOP_WIN2_DSP_INFO2
Address: Operational Base + offset (0x00e4)
Win2 display width2/height2 on panel

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0ef	win2_dsp_height2 Win2 display window height2 win2_dsp_height0 = size -1
15:12	RO	0x0	reserved
11:0	RW	0x13f	win2_dsp_width2 Win2 display window width2 win2_dsp_width = size -1

VOP_WIN2_DSP_ST2
Address: Operational Base + offset (0x00e8)
Win2 display start point2 on panel

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	win2_dsp_yst2 Win2 vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x000a	win2_dsp_xst2 Win2 horizontal start point(x) of the Panel scanning

VOP_WIN2_DST_ALPHA_CTRL
Address: Operational Base + offset (0x00ec)
Win2 alpha destination control register

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:6	RW	0x0	win2_dst_factor_mode dst factor mode
5:0	RW	0x00	win2_dst_m0_reserved reserved

VOP_WIN2_MST3
Address: Operational Base + offset (0x00f0)
Win2 memory start address3

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win2_mst3 Win2 frame buffer memory start address3 *must be alianed to 8byte address

VOP_WIN2_DSP_INFO3
Address: Operational Base + offset (0x00f4)
Win2 display width3/height3 on panel

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0ef	win2_dsp_height3 Win2 display window height3 win2_dsp_height0 = size -1
15:12	RO	0x0	reserved
11:0	RW	0x13f	win2_dsp_width3 Win2 display window width3 win2_dsp_width = size -1

VOP_WIN2_DSP_ST3
Address: Operational Base + offset (0x00f8)
Win2 display start point3 on panel

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	win2_dsp_yst3 Win2 vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x000a	win2_dsp_xst3 Win2 horizontal start point(x) of the Panel scanning

VOP_WIN2_FADING_CTRL
Address: Operational Base + offset (0x00fc)
Win2 fading contrl register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved

Bit	Attr	Reset Value	Description
24	RW	0x0	win2_fading_en fading enable 1'b0 : disable 1'b1 : enable
23:16	RW	0x00	win2_fading_offset_b fading offset blue
15:8	RW	0x00	win2_fading_offset_g fading offset green
7:0	RW	0x00	win2_fading_offset_r fading offset red

VOP_WIN3_CTRL0
Address: Operational Base + offset (0x0100)
Win3 ctrl register0

Bit	Attr	Reset Value	Description
31	RW	0x0	win3_endian_swap3 Win3 region3 8pp palette data Big-endian/ Little-endian select 1'b0 : Big-endian 1'b1 : Little-endian
30	RW	0x0	win3_alpha_swap3 Win3 region3 RGB alpha swap 1'b0 : ARGB 1'b1 : RGBA
29	RW	0x0	win3_rb_swap3 Win3 region3 RGB Red and Blue swap 1'b0 : RGB 1'b1 : BGR
28	RW	0x0	win3_endian_swap2 Win3 region2 8pp palette data Big-endian/ Little-endian select 1'b0 : Big-endian 1'b1 : Little-endian
27	RW	0x0	win3_alpha_swap2 Win3 region2 RGB alpha swap 1'b0 : ARGB 1'b1 : RGBA
26	RW	0x0	win3_rb_swap2 Win3 region2 RGB Red and Blue swap 1'b0 : RGB 1'b1 : BGR
25	RW	0x0	win3_endian_swap1 Win3 region1 8pp palette data Big-endian/ Little-endian select 1'b0 : Big-endian 1'b1 : Little-endian

Bit	Attr	Reset Value	Description
24	RW	0x0	win3_alpha_swap1 Win3 region1 RGB alpha swap 1'b0 : ARGB 1'b1 : RGBA
23	RW	0x0	win3_rb_swap1 Win3 region1 RGB Red and Blue swap 1'b0 : RGB 1'b1 : BGR
22	RW	0x0	win3_endian_swap0 Win3 region0 8pp palette data Big-endian/ Little-endian select 1'b0 : Big-endian 1'b1 : Little-endian
21	RW	0x0	win3_alpha_swap0 Win3 region0 RGB alpha swap 1'b0 : ARGB 1'b1 : RGBA
20	RW	0x0	win3_rb_swap0 Win3 region0 RGB Red and Blue swap 1'b0 : RGB 1'b1 : BGR
19	RO	0x0	reserved
18:17	RW	0x0	win3_data_fmt3 Win3 region 3 data format 2'b00 : ARGB888 2'b01 : RGB888 2'b10 : RGB565 2'b11 : 8bpp
16	RW	0x0	win3_mst3_en win3 master3 enable 1'b0 : disable 1'b1 : enable
15	RO	0x0	reserved
14:13	RW	0x0	win3_data_fmt2 Win3 region 2 data format 2'b00 : ARGB888 2'b01 : RGB888 2'b10 : RGB565 2'b11 : 8bpp
12	RW	0x0	win3_mst2_en win3 master2 enable 1'b0 : disable 1'b1 : enable
11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10:9	RW	0x0	win3_data_fmt1 Win3 region 1 data format 2'b00 : ARGB888 2'b01 : RGB888 2'b10 : RGB565 2'b11 : 8bpp
8	RW	0x0	win3_mst1_en win3 master1 enable 1'b0 : disable 1'b1 : enable
7	RO	0x0	reserved
6:5	RW	0x0	win3_data_fmt0 Win3 region 0 data format 2'b00 : ARGB888 2'b01 : RGB888 2'b10 : RGB565 2'b11 : 8bpp
4	RW	0x0	win3_mst0_en Win3 master0 enable 1'b0 : disable 1'b1 : enable
3:2	RW	0x0	win3_csc_mode Win3 RGB2YUV conversion mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
1	RW	0x0	win3_interlace_read Win3 interlace read mode 1'b0 : disable 1'b1 : enable
0	RW	0x0	win3_en 1'b0 : disable 1'b1 : enable

VOP_WIN3_CTRL1

Address: Operational Base + offset (0x0104)

Win3 ctrl register1

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:20	RW	0x6	win_rid_win3 axi read id of win3 channel
19:17	RO	0x0	reserved

Bit	Attr	Reset Value	Description
16	RW	0x0	win3_lut_en Win3 LUT ram enable 1'b0 : disable 1'b1 : enable *This bit should be "0" when CPU updates the LUT, and should be "1" when Win1 LUT mode enable.
15	RW	0x0	win3_y_mir_en 1'b0 : no y_mirror 1'b1 : y_mirror
14	RW	0x0	win3_no_outstanding Win3 AXI master read outstanding 1'b0 : enable 1'b1 : disable
13	RO	0x0	reserved
12:8	RW	0x1d	win3_axi_max_outstanding_num win3 axi bus max outstanding number
7:4	RW	0x0	win3_axi_gather_num win3 axi gather transfer number
3:2	RW	0x0	win3_dma_burst_length WIN3 DMA read Burst length 2'b00 : burst16 (burst 15 in rgb888 pack mode) 2'b01 : burst8 (burst 12 in rgb888 pack mode) 2'b10 : burst4 (burst 6 in rgb888 pack mode) 2'b11 : reserved
1	RW	0x0	win3_axi_max_outstanding_en 1'b0 : disable 1'b1 : enable
0	RW	0x0	win3_axi_gather_en 1'b0 : disable 1'b1 : enable

VOP_WIN3_VIR0_1
Address: Operational Base + offset (0x0108)
Win3 virtual stride0 and virtaul stride1

Bit	Attr	Reset Value	Description
31:16	RW	0x0140	win3_vir_stride1 Win3 Virtual stride1 Number of words of Win3 Virtual1 width ARGB888 : win3_vir_width1 RGB888 : (win3_vir_width1 * 3/4) + (win3_vir_width1 % 3) RGB565 : ceil(win3_vir_width1 / 2) 8BPP : ceil(win3_vir_width1 / 4) 4BPP : ceil(win3_vir_width1 / 8) 2BPP : ceil(win3_vir_width1 / 16) 1BPP : ceil(win3_vir_width1 / 32)

Bit	Attr	Reset Value	Description
15:0	RW	0x0140	win3_vir_stride0 Win3 Virtual stride0 Number of words of Win3 Virtual1 width ARGB888 : win3_vir_width1 RGB888 : (win3_vir_width1 * 3/4) + (win3_vir_width1 % 3) RGB565 : ceil(win3_vir_width1 / 2) 8BPP : ceil(win3_vir_width1 / 4) 4BPP : ceil(win3_vir_width1 / 8) 2BPP : ceil(win3_vir_width1 / 16) 1BPP : ceil(win3_vir_width1 / 32)

VOP_WIN3_VIR2_3
Address: Operational Base + offset (0x010c)
Win3 virtual stride2 and virtaul stride3

Bit	Attr	Reset Value	Description
31:16	RW	0x0140	win3_vir_stride3 Win3 Virtual stride3 Number of words of Win3 Virtual1 width ARGB888 : win3_vir_width1 RGB888 : (win3_vir_width1 * 3/4) + (win3_vir_width1 % 3) RGB565 : ceil(win3_vir_width1 / 2) 8BPP : ceil(win3_vir_width1 / 4) 4BPP : ceil(win3_vir_width1 / 8) 2BPP : ceil(win3_vir_width1 / 16) 1BPP : ceil(win3_vir_width1 / 32)
15:0	RW	0x0140	win3_vir_stride2 Win3 Virtual stride2 Number of words of Win3 Virtual1 width ARGB888 : win3_vir_width1 RGB888 : (win3_vir_width1 * 3/4) + (win3_vir_width1 % 3) RGB565 : ceil(win3_vir_width1 / 2) 8BPP : ceil(win3_vir_width1 / 4) 4BPP : ceil(win3_vir_width1 / 8) 2BPP : ceil(win3_vir_width1 / 16) 1BPP : ceil(win3_vir_width1 / 32)

VOP_WIN3_MST0
Address: Operational Base + offset (0x0110)
Win3 memory start address0

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win3_mst0 Win3 frame buffer memory start address0 *must be alianed to 8byte address

VOP_WIN3_DSP_INFO0

Address: Operational Base + offset (0x0114)
Win3 display width0/height0 on panel

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0ef	win3_dsp_height0 Win3 display window height0 win3_dsp_height0 = size -1
15:12	RO	0x0	reserved
11:0	RW	0x13f	win3_dsp_width0 Win3 display window width0 win3_dsp_width = size -1

VOP_WIN3_DSP_ST0
Address: Operational Base + offset (0x0118)
Win3 display start point0 on panel

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	win3_dsp_yst0 Win3 vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x000a	win3_dsp_xst0 Win3 horizontal start point(x) of the Panel scanning

VOP_WIN3_COLOR_KEY
Address: Operational Base + offset (0x011c)
Win3 color key register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	win3_key_en Win3 transparency color key enable 1'b0 : disable; 1'b1 : enable;
23:0	RW	0x000000	win3_key_color Win3 key color

VOP_WIN3_MST1
Address: Operational Base + offset (0x0120)
Win3 memory start address1

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win3_mst1 Win3 frame buffer memory start address1 *must be alianed to 8byte address

VOP_WIN3_DSP_INFO1
Address: Operational Base + offset (0x0124)
Win3 display width1/height1 on panel

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0ef	win3_dsp_height1 Win3 display window height1 win3_dsp_height0 = size -1
15:12	RO	0x0	reserved
11:0	RW	0x13f	win3_dsp_width1 Win3 display window width1 win3_dsp_width = size -1

VOP_WIN3_DSP_ST1
Address: Operational Base + offset (0x0128)
Win3 display start point1 on panel

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	win3_dsp_yst1 Win3 vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x000a	win3_dsp_xst1 Win3 horizontal start point(x) of the Panel scanning

VOP_WIN3_SRC_ALPHA_CTRL
Address: Operational Base + offset (0x012c)
Win3 alpha source control register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	win3_fading_value fading value
23:16	RW	0x00	win3_src_global_alpha src global alpha
15:9	RO	0x0	reserved
8:6	RW	0x0	win3_src_factor_mode src factor mode
5	RW	0x0	win3_src_alpha_cal_mode src alpha cal mode
4:3	RW	0x0	win3_src_blend_mode src blend mode
2	RW	0x0	win3_src_alpha_mode src alpha mode
1	RW	0x0	win3_src_color_mode src color mode
0	RW	0x0	win3_src_alpha_en src alpha en

VOP_WIN3_MST2
Address: Operational Base + offset (0x0130)
Win3 memory start address2

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win3_mst2 Win3 frame buffer memory start address2 *must be alianed to 8byte address

VOP_WIN3_DSP_INFO2
Address: Operational Base + offset (0x0134)
Win3 display width2/height2 on panel

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0ef	win3_dsp_height2 Win3 display window height2 win3_dsp_height0 = size -1
15:12	RO	0x0	reserved
11:0	RW	0x13f	win3_dsp_width2 Win3 display window width2 win3_dsp_width = size -1

VOP_WIN3_DSP_ST2
Address: Operational Base + offset (0x0138)
Win3 display start point2 on panel

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	win3_dsp_yst2 Win3 vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x000a	win3_dsp_xst2 Win3 horizontal start point(x) of the Panel scanning

VOP_WIN3_DST_ALPHA_CTRL
Address: Operational Base + offset (0x013c)
Win3 alpha destination control register

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:6	RW	0x0	win3_dst_factor_mode dst factor mode
5:0	RW	0x00	win3_dst_factor_reserved reserved

VOP_WIN3_MST3
Address: Operational Base + offset (0x0140)
Win3 memory start address3

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win3_mst3 Win3 frame buffer memory start address3 *must be alianed to 8byte address

VOP_WIN3_DSP_INFO3
Address: Operational Base + offset (0x0144)
Win3 display width3/height3 on panel

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0ef	win3_dsp_height3 Win3 display window height3 win3_dsp_height0 = size -1
15:12	RO	0x0	reserved
11:0	RW	0x13f	win3_dsp_width3 Win3 display window width3 win3_dsp_width = size -1

VOP_WIN3_DSP_ST3
Address: Operational Base + offset (0x0148)
Win3 display start point3 on panel

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	win3_dsp_yst3 Win3 vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x000a	win3_dsp_xst3 Win3 horizontal start point(x) of the Panel scanning

VOP_WIN3_FADING_CTRL
Address: Operational Base + offset (0x014c)
Win3 fading contrl register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	win3_fading_en fadfing enable 1'b0 : disable 1'b1 : enable
23:16	RW	0x00	win3_fading_offset_b fading offset blue
15:8	RW	0x00	win3_fading_offset_g fading offset green
7:0	RW	0x00	win3_fading_offset_r fading offset red

VOP_HWC_CTRL0
Address: Operational Base + offset (0x0150)
Hwc ctrl register0

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14	RW	0x0	hwc_endian_swap hwc 8pp palette data Big-endian/ Little-endian select 1'b0 : Big-endian 1'b1 : Little-endian
13	RW	0x0	hwc_alpha_swap hwc RGB alpha swap 1'b0 : ARGB 1'b1 : RGBA
12	RW	0x0	hwc_rb_swap hwc RGB Red and Blue swap 1'b0 : RGB 1'b1 : BGR
11:10	RW	0x0	hwc_csc_mode hwc RGB2YUV Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
9	RO	0x0	reserved
8	RW	0x0	hwc_interlace_read hwc interlace read mode 1'b0 : disable 1'b1 : enable
7	RO	0x0	reserved
6:5	RW	0x0	hwc_size 2'b00 : 32x32 2'b01 : 64x64 2'b10 : 96x96 2'b11 : 128x128
4	RW	0x0	hwc_mode hwc color mode 1'b0 : normal color mode 1'b1 : reversed color mode
3:1	RW	0x0	hwc_data_fmt 3'b000 : ARGB888 3'b001 : RGB888 3'b010 : RGB565 3'b100: 8bpp 3'b101: 4bpp 3'b110: 2bpp 3'b111: 1bpp

Bit	Attr	Reset Value	Description
0	RW	0x0	hwc_en 1'b0 : disable 1'b1 : enable

VOP_HWC_CTRL1
Address: Operational Base + offset (0x0154)
Hwc ctrl register1

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:20	RW	0x7	win_rid_hwc axi read id of hwc channel
19:17	RO	0x0	reserved
16	RW	0x0	hwc_lut_en 1'b0 : disable 1'b1 : enable
15	RW	0x0	hwc_y_mir_en 1'b0 : no y_mirror 1'b1 : y_mirror
14	RW	0x0	hwc_no_outstanding hwc AXI master read outstanding 1'b0 : enable 1'b1 : disable
13	RW	0x0	hwc_rgb2yuv_en 1'b0 : enable 1'b1 : disable
12:8	RW	0x1d	hwc_axi_max_outstanding_num hwc axi bus max outstanding number
7	RO	0x0	reserved
6:4	RW	0x0	hwc_axi_gather_num hwc axi gather transfer number
3:2	RW	0x0	hwc_dma_burst_length HWC DMA read Burst length 2'b00 : burst16 (burst 15 in rgb888 pack mode) 2'b01 : burst8 (burst 12 in rgb888 pack mode) 2'b10 : burst4 (burst 6 in rgb888 pack mode) 2'b11 : reserved
1	RW	0x0	hwc_axi_max_outstanding_en 1'b0 : disable 1'b1 : enable
0	RW	0x0	hwc_axi_gather_en 1'b0 : disable 1'b1 : enable

VOP_HWC_MST
Address: Operational Base + offset (0x0158)

Hwc memory start address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hwc_mst HWC data memory start address

VOP_HWC_DSP_ST

Address: Operational Base + offset (0x015c)

Hwc display start point on panel

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	hwc_dsp_yst HWC vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x000a	hwc_dsp_xst HWC horizontal start point(x) of the Panel scanning

VOP_HWC_SRC_ALPHA_CTRL

Address: Operational Base + offset (0x0160)

Hwc alpha source control register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	hwc_fading_value fading value
23:16	RW	0x00	hwc_src_global_alpha src global alpha
15:9	RO	0x0	reserved
8:6	RW	0x0	hwc_src_factor_mode src factor mode
5	RW	0x0	hwc_src_alpha_cal_mode src alpha calc mode
4:3	RW	0x0	hwc_src_blend_mode src blend mode
2	RW	0x0	hwc_src_alpha_mode src alpha mode
1	RW	0x0	hwc_src_color_mode src color mode
0	RW	0x0	hwc_src_alpha_en src alpha enable

VOP_HWC_DST_ALPHA_CTRL

Address: Operational Base + offset (0x0164)

Hwc alpha destination control register

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:6	RW	0x0	hwc_dst_factor_mode dst factor mode

Bit	Attr	Reset Value	Description
5:0	RW	0x00	hwc_dst_m0_reserved reserved

VOP_HWC_FADING_CTRL
Address: Operational Base + offset (0x0168)
Hwc fading contrl register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	hwc_fading_en 1'b0 : disable 1'b1 : enable
23:16	RW	0x00	hwc_fading_offset_b fading offset blue
15:8	RW	0x00	hwc_fading_offset_g fading offset green
7:0	RW	0x00	hwc_fading_offset_r fading offset red

VOP_HWC_RESERVED1
Address: Operational Base + offset (0x016c)
Hwc reserved

Bit	Attr	Reset Value	Description
31:0	RO	0x0	reserved

VOP_POST_DSP_HACT_INFO
Address: Operational Base + offset (0x0170)
Post scaler down horizontal start and end

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	dsp_hact_st_post Panel display scanning horizontal active start point
15:13	RO	0x0	reserved
12:0	RW	0x014a	dsp_hact_end_post Panel display scanning horizontal active end point

VOP_POST_DSP_VACT_INFO
Address: Operational Base + offset (0x0174)
Panel active horizontal scanning start point and end point

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	dsp_vact_st_post Panel display scanning horizontal active start point
15:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12:0	RW	0x00fa	dsp_vact_end_post Panel display scanning horizontal active end point

VOP_POST_SCL_FACTOR_YRGB
Address: Operational Base + offset (0x0178)
Post yrgb scaling factor

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	post_vs_factor_yrgb post YRGB vertical scaling factor: factor=((src_height[31:16]) /(dst_height[31:16]))*2^12
15:0	RW	0x1000	post_hs_factor_yrgb Post YRGB horizontal scaling factor: factor=((src_width[15:0]) /(dst_width[15:0]))*2^12

VOP_POST_RESERVED
Address: Operational Base + offset (0x017c)
Post reserved

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	RW	0x0	Field0000 Abstract Field0000 Description
1:0	RO	0x0	reserved

VOP_POST_SCL_CTRL
Address: Operational Base + offset (0x0180)
Post scaling start point offset

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	post_ver_sd_en 1'b0 : post ver scl down disable 1'b1 : post ver scl down enable
0	RW	0x0	post_hor_sd_en 1'b0 : post hor scl down disable 1'b1 : post hor scl down enable

VOP_POST_DSP_VACT_INFO_F1
Address: Operational Base + offset (0x0184)
Panel active horizontal scanning start point and end point F1

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	dsp_vact_st_post Panel display scanning horizontal active start point
15:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12:0	RW	0x00fa	dsp_vact_end_post Panel display scanning horizontal active end point

VOP_DSP_HTOTAL_HS_END
Address: Operational Base + offset (0x0188)
Panel scanning horizontal width and hsync pulse end point

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x014a	dsp_htotal Panel display scanning horizontal period
15:13	RO	0x0	reserved
12:0	RW	0x000a	dsp_hs_end Panel display scanning hsync pulse width

VOP_DSP_HACT_ST_END
Address: Operational Base + offset (0x018c)
Panel active horizontal scanning start point and end point

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	dsp_hact_st Panel display scanning horizontal active start point
15:13	RO	0x0	reserved
12:0	RW	0x014a	dsp_hact_end Panel display scanning horizontal active end point

VOP_DSP_VTOTAL_VS_END
Address: Operational Base + offset (0x0190)
Panel scanning vertical height and vsync pulse end point

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x00fa	dsp_vtotal Panel display scanning vertical period.
15	RW	0x0	sw_dsp_vtotal_imd dsp vtotal number valid immediately enable. 1'b0 : valid after frame start 1'b1 : valid immediately
14:13	RO	0x0	reserved
12:0	RW	0x000a	dsp_vs_end Panel display scanning vsync pulse width

VOP_DSP_VACT_ST_END
Address: Operational Base + offset (0x0194)
Panel active vertical scanning start point and end point

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	dsp_vact_st Panel display scanning vertical active start point
15:13	RO	0x0	reserved
12:0	RW	0x00fa	dsp_vact_end Panel display scanning vertical active end point

VOP_DSP_VS_ST_END_F1
Address: Operational Base + offset (0x0198)
Vertical scanning start point and vsync pulse end point of even filed in interlace mode

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vs_st_f1 Panel display scanning vertical vsync start point of 2nd field (interlace display mode)
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vs_end_f1 Panel display scanning vertical vsync end point of 2nd field(interlace display mode)

VOP_DSP_VACT_ST_END_F1
Address: Operational Base + offset (0x019c)
Vertical scanning active start point and end point of even filed in interlace mode

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_vact_st_f1 Panel display scanning vertical active start point of 2nd field (interlace display mode)
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_vact_end_f1 Panel display scanning vertical active end point of 2nd field (interlace display mode)

VOP_PWM_CTRL
Address: Operational Base + offset (0x01a0)
PWM Control Register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	rpt Repeat Counter This field defines the repeated effective periods of output waveform in one-shot mode. The value N means N+1 repeated effective periods.

Bit	Attr	Reset Value	Description
23:16	RW	0x00	scale Scale Factor This fields defines the scale factor applied to prescaled clock. The value N means the clock is divided by 2*N. If N is 0, it means that the clock is divided by 512(2*256).
15	RO	0x0	reserved
14:12	RW	0x2	prescale Prescale Factor This field defines the prescale factor applied to input clock. The value N means that the input clock is divided by 2^N.
11:10	RO	0x0	reserved
9	RW	0x0	clk_sel Clock Source Select 1'b0: non-scaled clock is selected as PWM clock source. It means that the prescale clock is directly used as the PWM clock source 1'b1: scaled clock is selected as PWM clock source
8	RW	0x0	lp_en Low Power Mode Enable 1'b0: disabled 1'b1: enabled When PWM channel is inactive state and Low Power Mode is enabled, the path to PWM Clock prescale module is blocked to reduce power consumption.
7:6	RO	0x0	reserved
5	RW	0x0	output_mode PWM Output mode 1'b0: left aligned mode 1'b1: center aligned mode
4	RW	0x0	inactive_pol Inactive State Output Polarity This defines the output waveform polarity when PWM channel is in inactive state. The inactive state means that PWM finishes the complete waveform in one-shot mode or PWM channel is disabled. 1'b0: negative 1'b1: positive
3	RW	0x1	duty_pol Duty Cycle Output Polarity This defines the polarity for duty cycle. PWM starts the output waveform with duty cycle. 1'b0: negative 1'b1: positive

Bit	Attr	Reset Value	Description
2:1	RW	0x1	pwm_mode PWM Operation Mode 2'b00: One shot mode. PWM produces the waveform within the repeated times defined by PWMx_CTRL_rpt . 2'b01: Continuous mode. PWM produces the waveform continuously 2'b10: Capture mode. PWM measures the cycles of high/low polarity of input waveform. 2'b11: reserved
0	RW	0x0	pwm_en PWM channel enable 1'b0: disabled 1'b1: enabled. If the PWM is worked the one-shot mode, this bit will be cleared at the end of operation

VOP_PWM_PERIOD_HPR
Address: Operational Base + offset (0x01a4)
PWM Period Register/High Polarity Capture Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwm_period Output Waveform Period/Input Waveform High Polarity Cycle If PWM is operated at the continuous mode or one-shot mode, this value defines the period of the output waveform. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the bit [31:1] is taken into account and bit [0] always considered as 0. If PWM is operated at the capture mode, this value indicates the effective high polarity cycles of input waveform. This value is based on the PWM clock. The value ranges from 0 to (2^32-1).

VOP_PWM_DUTY_LPR
Address: Operational Base + offset (0x01a8)
PWM Duty Register/Low Polarity Capture Register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwm_duty Output Waveform Duty Cycle/Input Waveform Low Polarity Cycle If PWM is operated at the continuous mode or one-shot mode, this value defines the duty cycle of the output waveform. The PWM starts the output waveform with duty cycle. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the [31:1] is taken into account. If PWM is operated at the capture mode, this value indicates the effective low polarity cycles of input waveform. This value is based on the PWM clock. The value ranges from 0 to (2^32-1).

VOP_PWM_CNT
Address: Operational Base + offset (0x01ac)
PWM Counter Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pwm_cnt Timer Counter The 32-bit indicates current value of PWM Channel 0 counter. The counter runs at the rate of PWM clock. The value ranges from 0 to (2^32-1).

VOP_BCSH_COLOR_BAR
Address: Operational Base + offset (0x01b0)
Color bar config register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	color_bar_v v color value
23:16	RW	0x00	color_bar_u u color value
15:8	RW	0x00	color_bar_y y color value
7:1	RO	0x0	reserved
0	RW	0x0	bcsh_en 1'b0 : bcsh bypass 1'b1 : bcsh enable

VOP_BCSH_BCS
Address: Operational Base + offset (0x01b4)
Brightness contrast saturation*contrast config register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:30	RW	0x3	out_mode video out mode config register 2'b00 : black 2'b01 : blue 2'b10 : color bar 2'b11 : normal video
29:20	RW	0x100	sat_con Saturation*Contrast*256 : 0,1.992*1.992
19:17	RO	0x0	reserved
16:8	RW	0x100	contrast Contrast*256 : 0,1.992
7:0	RW	0x00	brightness Brightness : -32,31

VOP_BCSH_H
Address: Operational Base + offset (0x01b8)
Sin hue and cos hue config register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x100	cos_hue cos hue value
15:9	RO	0x0	reserved
8:0	RW	0x000	sin_hue sin hue value

VOP_BCSH_CTRL
Address: Operational Base + offset (0x01bc)
BCSH contrl register

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RW	0x0	bcsh_r2y_csc_mode Color space conversion: 1'b0: BT601 1'b1: BT709
5	RO	0x0	reserved
4	RW	0x0	bcsh_r2y_en 1'b0:bypass 1'b1:enable
3:2	RW	0x0	bcsh_y2r_csc_mode Color space conversion(YUV2RGB): 2'b00/01 : mpeg 2'b10 : jpeg 2'b11 : hd
1	RO	0x0	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	bcsh_y2r_en 1'b0:bypass 1'b1:enable

VOP_CABC_CTRL0
Address: Operational Base + offset (0x01c0)
Content Adaptive Backlight Control register0

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:4	RW	0x0ed800	cabc_calc_pixel_num cabc calc pixel numbers = x % * cabc_total_num
3:2	RW	0x0	pwm_config_mode 2'b00 : last frame pwm value 2'b01 : cur frame pwm value 2'b1x : stage by stage
1	RW	0x0	cabc_handle_en cabc control pwm
0	RW	0x0	cabc_en 1'b0 : cabc disable 1'b1 : cabc enable

VOP_CABC_CTRL1
Address: Operational Base + offset (0x01c4)
Content Adaptive Backlight Control register1

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:4	RW	0x0fa000	cabc_total_num cabc totala numbers = h_vd * v_vd
3:1	RO	0x0	reserved
0	RW	0x0	cabc_lut_en cabc pwm lut enable

VOP_CABC_CTRL2
Address: Operational Base + offset (0x01c8)
Content Adaptive Backlight Control register2

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19	RW	0x0	cabc_stage_up_mode 1'b0: mul mode 1'b1: add mode
18:17	RO	0x0	reserved
16:8	RW	0x110	cabc_stage_up when mul mode ,scale stage up (1~1.5 * 256). when add mode ,scale stage up (0x00~0xff).

Bit	Attr	Reset Value	Description
7:0	RW	0xf0	cabc_stage_down when mul mode ,scale stage down (0.667~1 * 256). when add mode ,scale stage down (0x00~0xff).

VOP_CABC_CTRL3
Address: Operational Base + offset (0x01cc)
Content Adaptive Backlight Control register3

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8	RW	0x0	cabc_global_dn_limit_en cabc global scale down limit enable.
7:0	RW	0x00	cabc_global_dn cabc global scale down value.

VOP_CABC_GAUSS_LINE0_0
Address: Operational Base + offset (0x01d0)
CABC gauss line config register00

Bit	Attr	Reset Value	Description
31:24	RW	0x15	t_line0_3 gauss parameter t_line0_3
23:16	RW	0x11	t_line0_2 gauss parameter t_line0_2
15:8	RW	0x09	t_line0_1 gauss parameter t_line0_1
7:0	RW	0x03	t_line0_0 gauss parameter t_line0_0

VOP_CABC_GAUSS_LINE0_1
Address: Operational Base + offset (0x01d4)
CABC gauss line config register01

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x03	t_line0_6 gauss parameter t_line0_6
15:8	RW	0x09	t_line0_5 gauss parameter t_line0_5
7:0	RW	0x11	t_line0_4 gauss parameter t_line0_4

VOP_CABC_GAUSS_LINE1_0
Address: Operational Base + offset (0x01d8)
CABC gauss line config register10

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:24	RW	0x1a	t_line1_3 gauss parameter t_line1_3
23:16	RW	0x15	t_line1_2 gauss parameter t_line1_2
15:8	RW	0x0b	t_line1_1 gauss parameter t_line1_1
7:0	RW	0x04	t_line1_0 gauss parameter t_line1_0

VOP_CABC_GAUSS_LINE1_1
Address: Operational Base + offset (0x01dc)
CABC gauss line config register11

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x04	t_line1_6 gauss parameter t_line1_6
15:8	RW	0x0b	t_line1_5 gauss parameter t_line1_5
7:0	RW	0x15	t_line1_4 gauss parameter t_line1_4

VOP_CABC_GAUSS_LINE2_0
Address: Operational Base + offset (0x01e0)
CABC gauss line config register20

Bit	Attr	Reset Value	Description
31:24	RW	0x15	t_line2_3 gauss parameter t_line2_3
23:16	RW	0x11	t_line2_2 gauss parameter t_line2_2
15:8	RW	0x09	t_line2_1 gauss parameter t_line2_1
7:0	RW	0x03	t_line2_0 gauss parameter t_line2_0

VOP_CABC_GAUSS_LINE2_1
Address: Operational Base + offset (0x01e4)
CABC gauss line config register21

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x03	t_line2_6 gauss parameter t_line2_6
15:8	RW	0x09	t_line2_5 gauss parameter t_line2_5

Bit	Attr	Reset Value	Description
7:0	RW	0x11	t_line2_4 gauss parameter t_line2_4

VOP_FRC_LOWER01_0
Address: Operational Base + offset (0x01e8)
FRC lookup table config register010

Bit	Attr	Reset Value	Description
31:16	RW	0x1284	lower01_frm1 frc parameter lowerbit = 2'b01,frm1
15:0	RW	0x4821	lower01_frm0 frc parameter lowerbit = 2'b01,frm0

VOP_FRC_LOWER01_1
Address: Operational Base + offset (0x01ec)
FRC lookup table config register011

Bit	Attr	Reset Value	Description
31:16	RW	0x2148	lower01_frm3 frc parameter lowerbit = 2'b01,frm3
15:0	RW	0x8412	lower01_frm2 frc parameter lowerbit = 2'b01,frm2

VOP_FRC_LOWER10_0
Address: Operational Base + offset (0x01f0)
FRC lookup table config register100

Bit	Attr	Reset Value	Description
31:16	RW	0xa55a	lower10_frm1 frc parameter lowerbit = 2'b10,frm1
15:0	RW	0x9696	lower10_frm0 frc parameter lowerbit = 2'b10,frm0

VOP_FRC_LOWER10_1
Address: Operational Base + offset (0x01f4)
FRC lookup table config register101

Bit	Attr	Reset Value	Description
31:16	RW	0x5aa5	lower10_frm3 frc parameter lowerbit = 2'b10,frm3
15:0	RW	0x6969	lower10_frm2 frc parameter lowerbit = 2'b10,frm2

VOP_FRC_LOWER11_0
Address: Operational Base + offset (0x01f8)
FRC lookup table config register110

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0xdeb7	lower11_frm1 frc parameter lowerbit = 2'b11,frm1
15:0	RW	0x7bed	lower11_frm0 frc parameter lowerbit = 2'b11,frm0

VOP_FRC_LOWER11_1
Address: Operational Base + offset (0x01fc)
FRC lookup table config register111

Bit	Attr	Reset Value	Description
31:16	RW	0xed7b	lower11_frm3 frc parameter lowerbit = 2'b11,frm3
15:0	RW	0xb7de	lower11_frm2 frc parameter lowerbit = 2'b11,frm2

VOP_INTR_EN0
Address: Operational Base + offset (0x0280)
Interrupt enable register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	intr_en_dma_finish 1'b0: disable 1'b1: enable
14	RW	0x0	intr_en_mmu 1'b0: disable 1'b1: enable
13	RW	0x0	intr_en_dsp_hold_valid display hold valid interrupt enable 1'b0: disable 1'b1: enable
12	RW	0x0	intr_en_fs_field field interrupt enable 1'b0: disable 1'b1: enable
11	RW	0x0	intr_en_post_buf_empty post buffer empty interrupt enable 1'b0: disable 1'b1: enable
10	RW	0x0	intr_en_hwc_empty hwc data empty interrupt enable 1'b0: disable 1'b1: enable

Bit	Attr	Reset Value	Description
9	RW	0x0	intr_en_win3_empty win3 data empty interrupt enable 1'b0: disable 1'b1: enable
8	RW	0x0	intr_en_win2_empty win2 data empty interrupt enable 1'b0: disable 1'b1: enable
7	RW	0x0	intr_en_win1_empty win1 data empty interrupt enable 1'b0: disable 1'b1: enable
6	RW	0x0	intr_en_win0_empty win0 data empty interrupt enable 1'b0: disable 1'b1: enable
5	RW	0x0	intr_en_bus_error Bus error Interrupt enable 1'b0: disable 1'b1: enable
4	RW	0x0	intr_en_line_flag1 Line flag 1 Interrupt enable 1'b0: disable 1'b1: enable
3	RW	0x0	intr_en_line_flag0 Line flag 0 Interrupt enable 1'b0: disable 1'b1: enable
2	RW	0x0	intr_en_addr_same memory start addr same interruption enable 1'b0: disable 1'b1: enable
1	RW	0x0	intr_en_fs_new Frame new start interrupt enable 1'b0: disable 1'b1: enable
0	RW	0x0	intr_en_fs Frame start interrupt enable 1'b0: disable 1'b1: enable

VOP_INTR_CLEAR0
Address: Operational Base + offset (0x0284)
Interrupt clear register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	int_clr_dma_finish dma finish interrupt clear(Auto clear)
14	RW	0x0	int_clr_mmu mmu interrupt clear(Auto clear)
13	W1C	0x0	int_clr_dsp_hold_valid display hold valid interrupt clear(Auto clear)
12	W1C	0x0	int_clr_fs_field field start interrupt clear(Auto clear) Field start interrupt clear (Auto clear)
11	W1C	0x0	int_clr_post_buf_empty post buffer empty interrupt clear(Auto clear)
10	W1C	0x0	int_clr_hwc_empty hwc data empty interrupt clear(Auto clear)
9	W1C	0x0	int_clr_win3_empty win3 data empty interrupt clear(Auto clear)
8	W1C	0x0	int_clr_win2_empty win2 data empty interrupt clear(Auto clear)
7	W1C	0x0	int_clr_win1_empty win1 data empty interrupt clear(Auto clear)
6	W1C	0x0	int_clr_win0_empty win0 data empty interrupt clear(Auto clear)
5	W1C	0x0	int_clr_bus_error Bus error Interrupt clear(Auto clear)
4	W1C	0x0	int_clr_line_flag1 Line flag 1 Interrupt clear(Auto clear)
3	W1C	0x0	int_clr_line_flag0 Line flag 0 Interrupt clear(Auto clear)
2	W1C	0x0	int_clr_addr_same memory start addr same interruption clear(Auto clear)
1	W1C	0x0	int_clr_fs_new Frame new start interrupt clear (Auto clear)
0	W1C	0x0	int_clr_fs Frame start interrupt clear (Auto clear)

VOP_INTR_STATUS0

Address: Operational Base + offset (0x0288)

interrupt status

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15	RW	0x0	int_status_dma_finish dma finish interrupt status

Bit	Attr	Reset Value	Description
14	RW	0x0	int_status_mmu mmu interrupt status
13	RO	0x0	int_status_dsp_hold_valid display hold valid interrupt status
12	RO	0x0	int_status_fs_field Field start interrupt status
11	RO	0x0	int_status_post_buf_empty post buffer empty interrupt status
10	RO	0x0	int_status_hwc_empty hwc data empty interrupt status
9	RO	0x0	int_status_win3_empty win3 data empty interrupt status
8	RO	0x0	int_status_win2_empty win2 data empty interrupt status
7	RO	0x0	int_status_win1_empty win1 data empty interrupt status
6	RO	0x0	int_status_win0_empty win0 data empty interrupt status
5	RO	0x0	int_status_bus_error Bus error Interrupt status
4	RO	0x0	int_status_line_flag1 Line flag 1 Interrupt status
3	RO	0x0	int_status_line_flag0 Line flag 0 Interrupt status
2	RW	0x0	int_status_addr_same memory start addr same interruption status
1	RO	0x0	int_status_fs_new Frame start interrupt status(when memory start addr are same,no interruption)
0	RO	0x0	int_status_fs Frame start interrupt status

VOP_INTR_RAW_STATUS0
Address: Operational Base + offset (0x028c)
raw interrupt status

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15	RO	0x0	int_raw_status_dma_finish dma finish interrupt raw status
14	RO	0x0	int_raw_status_mmu mmu interrupt raw status
13	RO	0x0	int_raw_status_dsp_hold_valid display hold valid interrupt raw status
12	RO	0x0	int_raw_status_fs_field Field start raw interrupt status

Bit	Attr	Reset Value	Description
11	RO	0x0	int_raw_status_post_buf_empty post buffer empty interrupt raw status
10	RO	0x0	int_raw_status_hwc_empty hwc data empty interrupt raw status
9	RO	0x0	int_raw_status_win3_empty win3 data empty interrupt raw status
8	RO	0x0	int_raw_status_win2_empty win2 data empty interrupt raw status
7	RO	0x0	int_raw_status_win1_empty win1 data empty interrupt raw status
6	RO	0x0	int_raw_status_win0_empty win0 data empty interrupt raw status
5	RO	0x0	int_raw_status_bus_error Bus error Interrupt raw status
4	RO	0x0	int_raw_status_line_frag1 Line flag 1 Interrupt raw status
3	RO	0x0	int_raw_status_line_frag0 Line flag 0 Interrupt raw status
2	RO	0x0	int_raw_status_addr_same memory start addr same interruption raw status
1	RO	0x0	int_raw_status_fs_new Frame start interrupt raw status(when memory start addr are same)
0	RO	0x0	int_raw_status_fs Frame start raw interrupt status Frame start raw interrupt status

VOP_LINE_FLAG
Address: Operational Base + offset (0x02a0)
Line flag config register

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dsp_line_flag_num_1 Line number of the Line flag interrupt 1 The display line number when the flag interrupt 1 occur, the range is (0~ DSP_VTOTAL-1).
15:13	RO	0x0	reserved
12:0	RW	0x0000	dsp_line_flag_num_0 Line number of the Line flag interrupt 0 The display line number when the flag interrupt occur, the range is (0~ DSP_VTOTAL-1).

VOP_VOP_STATUS
Address: Operational Base + offset (0x02a4)
vop status register

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17	RW	0x0	dma_stop_valid dma stop valid
16	RW	0x0	mmu_idle mmu idle status
15:13	RO	0x0	reserved
12:0	RO	0x0000	dsp_vcnt read the dsp vertical counter

VOP_BLANKING_VALUE
Address: Operational Base + offset (0x02a8)
Register0000 Abstract

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	blanking_value_config_en 1'b0 : disable blanking value when vop blank 1'b1 : enable blanking value when vop blank
23:0	RW	0x000000	blanking_value vop output data value when blanking,24bits

VOP_MCU_BYPASS_PORT
Address: Operational Base + offset (0x02ac)
MCU bypass port

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	Field0000 Abstract Field0000 Description

VOP_WIN0_DSP_BG
Address: Operational Base + offset (0x02b0)
Win0 layer background color

Bit	Attr	Reset Value	Description
31	RW	0x0	win0_bg_en Win0 layer background enable 1'b0 : disable 1'b1 : enable
30:24	RO	0x0	reserved
23:16	RW	0x00	win0_dsp_bg_red Win0 layer Background Red color
15:8	RW	0x00	win0_dsp_bg_green Win0 layer Background Green color
7:0	RW	0x00	win0_dsp_bg_blue Win0 layer Background Blue color

VOP_WIN1_DSP_BG
Address: Operational Base + offset (0x02b4)
Win1 layer background color

Bit	Attr	Reset Value	Description
31	RW	0x0	win1_bg_en Win1 layer background enable 1'b0 : disable 1'b1 : enable
30:24	RO	0x0	reserved
23:16	RW	0x00	win1_dsp_bg_red Win1 layer Background Red color
15:8	RW	0x00	win1_dsp_bg_green Win1 layer Background Green color
7:0	RW	0x00	win1_dsp_bg_blue Win1 layer Background Blue color

VOP_WIN2_DSP_BG
Address: Operational Base + offset (0x02b8)
Win2 layer background color

Bit	Attr	Reset Value	Description
31	RW	0x0	win2_bg_en Win2 layer background enable 1'b0 : disable 1'b1 : enable
30:24	RO	0x0	reserved
23:16	RW	0x00	win2_dsp_bg_red Win2 layer Background Red color
15:8	RW	0x00	win2_dsp_bg_green Win2 layer Background Green color
7:0	RW	0x00	win2_dsp_bg_blue Win2 layer Background Blue color

VOP_WIN3_DSP_BG
Address: Operational Base + offset (0x02bc)
Win3 layer background color

Bit	Attr	Reset Value	Description
31	RW	0x0	win3_bg_en Win3 layer background enable 1'b0 : disable 1'b1 : enable
30:24	RO	0x0	reserved
23:16	RW	0x00	win3_dsp_bg_red Win3 layer Background Red color
15:8	RW	0x00	win3_dsp_bg_green Win3 layer Background Green color

Bit	Attr	Reset Value	Description
7:0	RW	0x00	win3_dsp_bg_blue Win3 layer Background Blue color

VOP_YUV2YUV_WIN
Address: Operational Base + offset (0x02c0)
win yuv2yuv control register

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:22	RW	0x0	win2_yuv2yuv_r2y_mode •2'b00 : bt601_l 2'b01 : bt709_l 2'b10 : bt601_f 2'b11 : bt2020
21:20	RO	0x0	reserved
19	RW	0x0	win2_yuv2yuv_gamma_mode 1'b0 : bt2020 to bt709 or bt709 to bt2020 1'b1 : bt2020 to srgb or srgb to bt2020
18	RW	0x0	win2_yuv2yuv_r2y_en 1'b0 : disable 1'b1 : enable
17	RO	0x0	reserved
16	RW	0x0	win2_yuv2yuv_en 1'b0 : disable 1'b1 : enable
15:8	RO	0x0	reserved
7:6	RW	0x0	win0_yuv2yuv_r2y_mode 2'b00 : bt601_l 2'b01 : bt709_l 2'b10 : bt601_f 2'b11 : bt2020
5:4	RW	0x0	win0_yuv2yuv_y2r_mode 2'b00 : bt601_l 2'b01 : bt709_l 2'b10 : bt601_f 2'b11 : bt2020
3	RW	0x0	win0_yuv2yuv_gamma_mode 1'b0 : bt2020 to bt709 or bt709 to bt2020 1'b1 : bt2020 to srgb or srgb to bt2020
2	RW	0x0	win0_yuv2yuv_r2y_en 1'b0 : disable 1'b1 : enable
1	RW	0x0	win0_yuv2yuv_y2r_en 1'b0 : disable 1'b1 : enable

Bit	Attr	Reset Value	Description
0	RW	0x0	win0_yuv2yuv_en 1'b0 : disable 1'b1 : enable

VOP_AUTO_GATING_EN
Address: Operational Base + offset (0x02cc)
Auto gating enable

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15	RW	0x0	fbcd3_aclk_gating_en
14	RW	0x0	fbcd2_aclk_gating_en
13	RW	0x0	fbcd1_aclk_gating_en
12	RW	0x0	fbcd0_aclk_gating_en
11	RO	0x0	reserved
10	RW	0x0	direct_path_aclk_gating_en
9	RW	0x0	pwm_pwmclk_gating_en
8	RW	0x0	wb_aclk_gating_en
7	RW	0x0	cabc_aclk_gating_en
6	RW	0x0	gamma_aclk_gating_en •
5	RW	0x0	overlay_aclk_gating_en
4	RW	0x0	hwc_aclk_gating_en
3	RW	0x0	win3_aclk_gating_en •
2	RW	0x0	win2_aclk_gating_en
1	RW	0x0	win1_aclk_gating_en
0	RW	0x0	win0_aclk_gating_en

VOP_WIN0_YUV2YUV_Y2R_COE0
Address: Operational Base + offset (0x04e0)
WIN0 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe01 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe00 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_Y2R_COE1
Address: Operational Base + offset (0x04e4)
WIN0 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe10 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe02 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_Y2R_COE2
Address: Operational Base + offset (0x04e8)
WIN0 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe12 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe11 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_Y2R_COE3
Address: Operational Base + offset (0x04ec)
WIN0yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe21 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe20 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_Y2R_COE4
Address: Operational Base + offset (0x04f0)
WIN0 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	csc_coe22 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_Y2R_COE5
Address: Operational Base + offset (0x04f4)
WIN0 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset0 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_Y2R_COE6
Address: Operational Base + offset (0x04f8)
WIN0 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset1 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_Y2R_COE7
Address: Operational Base + offset (0x04fc)
WIN0 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset2 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_R2R_COE0
Address: Operational Base + offset (0x0500)
WIN0 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe01 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe00 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_R2R_COE1
Address: Operational Base + offset (0x0504)
WIN0 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe10 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe02 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_R2R_COE2
Address: Operational Base + offset (0x0508)
WIN0 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe12 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe11 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_R2R_COE3
Address: Operational Base + offset (0x050c)
WIN0 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe21 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe20 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_R2R_COE4
Address: Operational Base + offset (0x0510)
WIN0 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	csc_coe22 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_R2R_COE5
Address: Operational Base + offset (0x0514)
WIN0 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset0 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_R2R_COE6
Address: Operational Base + offset (0x0518)
WIN0 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset1 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_R2R_COE7
Address: Operational Base + offset (0x051c)
WIN0 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset2 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_R2Y_COE0
Address: Operational Base + offset (0x0520)
WIN0 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe01 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe00 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_R2Y_COE1
Address: Operational Base + offset (0x0524)
WIN0 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe10 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe02 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_R2Y_COE2
Address: Operational Base + offset (0x0528)
WIN0 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe12 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe11 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_R2Y_COE3
Address: Operational Base + offset (0x052c)
WIN0 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe21 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe20 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_R2Y_COE4
Address: Operational Base + offset (0x0530)
WIN0 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	csc_coe22 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_R2Y_COE5
Address: Operational Base + offset (0x0534)
WIN0 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset0 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_R2Y_COE6
Address: Operational Base + offset (0x0538)

WIN0 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset1 coefficient of 3x4 matrix

VOP_WIN0_YUV2YUV_R2Y_COE7
Address: Operational Base + offset (0x053c)
WIN0 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset2 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_Y2R_COE0
Address: Operational Base + offset (0x05a0)
WIN2 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe01 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe00 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_Y2R_COE1
Address: Operational Base + offset (0x05a4)
WIN2 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe10 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe02 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_Y2R_COE2
Address: Operational Base + offset (0x05a8)
WIN2 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe12 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe11 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_Y2R_COE3
Address: Operational Base + offset (0x05ac)
WIN2 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe21 coefficient of 3x4 matrix

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	csc_coe20 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_Y2R_COE4
Address: Operational Base + offset (0x05b0)
WIN2 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	csc_coe22 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_Y2R_COE5
Address: Operational Base + offset (0x05b4)
WIN2 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset0 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_Y2R_COE6
Address: Operational Base + offset (0x05b8)
WIN2 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset1 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_Y2R_COE7
Address: Operational Base + offset (0x05bc)
WIN2 yuv2yuv y2r cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset2 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_R2R_COE0
Address: Operational Base + offset (0x05c0)
WIN2 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe01 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe00 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_R2R_COE1
Address: Operational Base + offset (0x05c4)
WIN2 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe10 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe02 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_R2R_COE2
Address: Operational Base + offset (0x05c8)
WIN2 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe12 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe11 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_R2R_COE3
Address: Operational Base + offset (0x05cc)
WIN2 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe21 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe20 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_R2R_COE4
Address: Operational Base + offset (0x05d0)
WIN2 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	csc_coe22 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_R2R_COE5
Address: Operational Base + offset (0x05d4)
WIN2 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset0 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_R2R_COE6
Address: Operational Base + offset (0x05d8)
WIN2 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset1 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_R2R_COE7
Address: Operational Base + offset (0x05dc)
WIN2 yuv2yuv r2r cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset2 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_R2Y_COE0
Address: Operational Base + offset (0x05e0)
WIN2 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe01 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe00 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_R2Y_COE1
Address: Operational Base + offset (0x05e4)
WIN2 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe10 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe02 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_R2Y_COE2
Address: Operational Base + offset (0x05e8)
WIN2 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe12 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe11 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_R2Y_COE3
Address: Operational Base + offset (0x05ec)
WIN2 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	csc_coe21 coefficient of 3x4 matrix
15:0	RW	0x0000	csc_coe20 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_R2Y_COE4
Address: Operational Base + offset (0x05f0)

WIN2 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	csc_coe22 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_R2Y_COE5
Address: Operational Base + offset (0x05f4)
WIN2 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset0 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_R2Y_COE6
Address: Operational Base + offset (0x05f8)
WIN2 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset1 coefficient of 3x4 matrix

VOP_WIN2_YUV2YUV_R2Y_COE7
Address: Operational Base + offset (0x05fc)
WIN2 yuv2yuv r2y cofficient

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	csc_offset2 coefficient of 3x4 matrix

VOP_HWC_LUT_ADDR
Address: Operational Base + offset (0x1800)
Hwc lut base address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hwc_lut_addr the head of hwc lut address

VOP_CABC_GAMMA_LUT_ADDR
Address: Operational Base + offset (0x1c00)
CABC GAMMA lut base address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	gamma_lut_addr the head of gamma lut address

VOP_GAMMA_LUT_ADDR
Address: Operational Base + offset (0x2000)
GAMMA lut base address

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	gamma_lut_addr the head of gamma lut address

VOP_MMU_DTE_ADDR
Address: Operational Base + offset (0x3f00)
MMU current page Table address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MMU_DTE_ADDR MMU DTE ADDR

VOP_MMU_STATUS
Address: Operational Base + offset (0x3f04)
MMU status register

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:6	RO	0x00	PAGE_FAULT_BUS_ID Index of master reponsible for last page fault
5	RO	0x0	PAGE_FAULT_IS_WRITE The direction of access for last page fault: 1'b0 = Read 1'b1 = Write
4	RO	0x0	REPLAY_BUFFER_EMPTY The MMU replay buffer is empty
3	RO	0x0	MMU_IDLE The MMU is idle when accesses are being translated and there are no unfinished translated accesses.
2	RO	0x0	STAIL_ACTIVE MMU stall mode currently enabled. The mode is enabled by command
1	RO	0x0	PAGE_FAULT_ACTIVE MMU page fault mode currently enabled . The mode is enabled by command.
0	RO	0x0	PAGING_ENABLED Paging is enabled

VOP_MMU_COMMAND
Address: Operational Base + offset (0x3f08)
MMU command register

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved

Bit	Attr	Reset Value	Description
2:0	WO	0x0	MMU_CMD MMU_CMD. This can be: 0: MMU_ENABLE_PAGING 1: MMU_DISABLE_PAGING 2: MMU_ENABLE_STALL 3: MMU_DISABLE_STALL 4: MMU_ZAP_CACHE 5: MMU_PAGE_FAULT_DONE 6: MMU_FORCE_RESET

VOP_MMU_PAGE_FAULT_ADDR
Address: Operational Base + offset (0x3f0c)
MMU logical address of last page fault

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	PAGE_FAULT_ADDR address of last page fault

VOP_MMU_ZAP_ONE_LINE
Address: Operational Base + offset (0x3f10)
MMU Zap cache line register

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	MMU_ZAP_ONE_LINE address to be invalidated from the page table cache

VOP_MMU_INT_RAWSTAT
Address: Operational Base + offset (0x3f14)
MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	READ_BUS_ERROR read bus error
0	RW	0x0	PAGE_FAULT page fault

VOP_MMU_INT_CLEAR
Address: Operational Base + offset (0x3f18)
MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	WO	0x0	READ_BUS_ERROR read bus error
0	WO	0x0	PAGE_FAULT page fault

VOP_MMU_INT_MASK
Address: Operational Base + offset (0x3f1c)
MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	READ_BUS_ERROR read bus error
0	RW	0x0	PAGE_FAULT page fault

VOP_MMU_INT_STATUS
Address: Operational Base + offset (0x3f20)
MMU raw interrupt status register

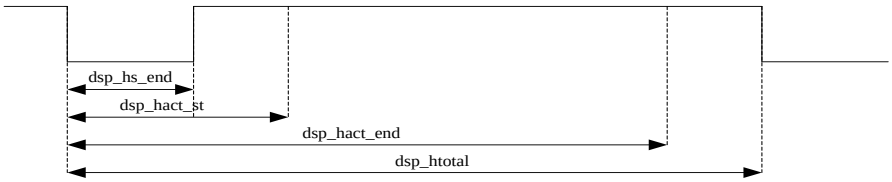
Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RO	0x0	READ_BUS_ERROR read bus error
0	RO	0x0	PAGE_FAULT page fault

VOP_MMU_AUTO_GATING
Address: Operational Base + offset (0x3f24)
MMU auto gating

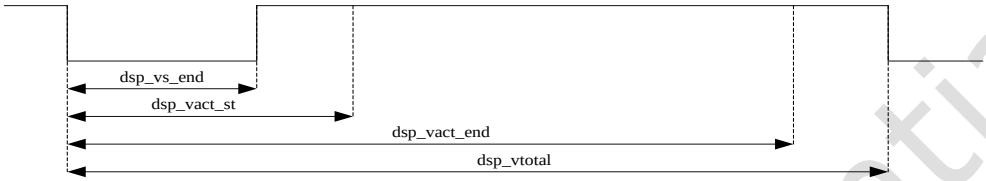
Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	mmu_auto_gating mmu auto gating when it is 1'b1, the mmu will auto gating it self

3.6 Timing Diagram

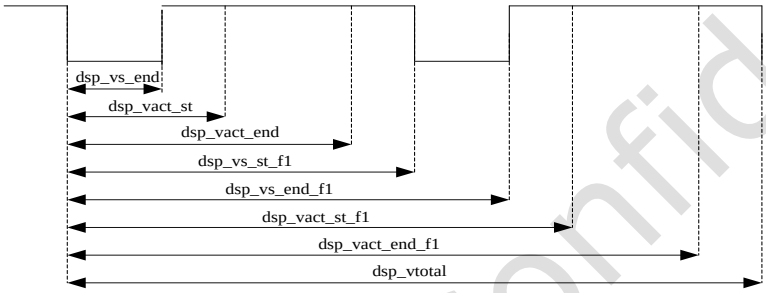
3.6.1 RGB LCD interface timing



Horizontal timing



Vertical timing(Progressive mode)



Vertical timing(Interlace mode)

Fig. 3-16 VOP RGB interface timing (SDR)

3.7 Application Notes

3.7.1 DMA transfer mode

There are three DMA transfer modes for loading win0 or win1 frame data determined by following parameters(X=0,1,2,3):
dma_burst_length
winX_no_outstanding
winX_gather_en
winX_gather_thres

1. auto outstanding transfer mode(random transfer)

When winX_no_outstanding is 0, multi-bursts transfer command could be sent out to AXI master interface continuously if the internal memory has enough space to store new data. The continuous random burst number is in the range of 1 to 4, mainly depending on the empty level of internal memory, dma_burst_length, data format and active image width.

2. configured outstanding transfer mode(fixed transfer)

When winX_gather_en is 1, fixed-number of bursts transfer command should be sent out to AXI master interface continuously if the internal memory has enough space to store new data. The fixed-number is determined by winX_gather_thres. Since the internal memory size is limited, there is some restriction for the winX_gather_thres as follows.

Table 3-2 Gather configuration for all format

Gather Threshold	dma_burst_length =2'b00(burst16)	dma_burst_length =2'b01(burst8)	dma_burst_length =2'b10(burst4)
YUV420 YUV422 YUV444	0	0,1,2	0,1,2,3
ARGB888			

RGB888 RGB565	0,1,2,3	0,1,2,3	0,1,2,3
8BPP 4BPP 2BPP 1BPP	0,1,2,3	0,1,2,3	0,1,2,3

3.7.2 Win0/Win1 dma load mode

If you want to improve the efficiency of accessing external memory for loading winX frame data, you could assert winX_dma_load. When winX_dma_load is high, winX frame data is loaded in the unit of line composing with one or more burst transfers; otherwise, loaded in the unit of burst transfer. However, it is not suitable for data format YUV420, no-scaling and active width less than 256.

3.7.3 WIN BPP LUT

WIN1 LUT/DSP LUT should be configured before displaying if win2/3_lut_en/dsp_lut_en is high. You could only update these LUTs by software.
When win1_lut_load_en is 0, the WIN LUT data should be refreshed by software,i.e, writing win1 lut data to the internal memory with the start address WIN1_LUT_MST. The memory size is 256x25, i.e, lower 25bits valid, and the writing data number is determined by software, .
When dsp_lut_load_en is 0, the DSP LUT data should be refreshed by software,i.e, writing dsp lut data to the internal memory with the start address DSP_LUT_MST. The memory size is 256x24, i.e, lower 25bits valid, and the writing data number is determined by software.The program model for CABC gamma LUT is similar.

3.7.4 DMA QoS request

If you want to get higher priority for VOP to access external memory when the frame data is urgent, a QoS request can be generated and sent out basing on the configured values:
noc_hurry_en
noc_hurry_value
noc_qos_en
noc_win_qos
If noc_qos_en is enable, a win0/1_qos_req is asserted when the empty level of win0/1's linebuffer is greater than the threshold configured in noc_win_qos. And it will be disserted when the empty level is smaller than the threshold or noc_qos_en is disable.
If noc_qos_en is enable, a win0/1_hurry_req is asserted when the empty level of win2/3's fifo is greater than the threshold configured in noc_win_qos. And it will be disserted when the empty level is smaller than the threshold or noc_qos_en is disable.
Either win0/1_qos_req or win2/3_hurry_req is high, a QoS request will be sent out for VOP.

3.7.5 Mirror display

If Y-Mirror display is enable, the frame data is loaded from last line to first line, where the start address of first pixel in last line is defined in
WIN0/1_YRGB0_MST/WIN0/1_CBR0_MST/WIN0/1_YRGB1_MST/WIN0/1_CBR_MST for win0/1/2/3 respectively.
Otherwise, the win's frame line data width and virtual stride should be 64bit-aligned for 8bit-RGB/YUV or 128bit-aligned for 10bit YUV if X-Mirror or Y-Mirror display is enable.

3.7.6 DDR interface

LCD DDR interface is just suitable for Parallel RGB LCD panel and Serial RGB LCD 2x12 panel.
If LCD DDR interface is enable, the timing parameters for LCD panel should be even.
Otherwise, you can synchronize output clock with VSYNC or HSYNC depending on dclk_ddr_sync.

3.7.7 Interrupt

VOP has three interrupt, respectively vop_intr, vop_intr_ddr and dma_finish.
Vop_intr is comprised of 20 interrupt sources:

frame start interrupt
frame start new interrupt
same frame address interrupt
line flag0 interrupt
line flag1 interrupt
bus error interrupt
win0 empty interrupt
win1 empty interrupt
win2 empty interrupt
win3 empty interrupt
hwc empty interrupt
post empty interrupt
field interrupt
hold interrupt
irq_mmu
dma finish interrupt
afbcd interrupt
afbcd decode response interrupt
write back yrbg fifo full interrupt
write back cbcr fifo full interrupt
Vertical fp interrupt
Vop_intr_ddr is comprised of 3 interrupt sources:
line flag1 interrupt
dma finish interrupt
write back dma finish interrupt
Every interrupt has independent interrupt enable (VOP_INT_EN,with bit write mask), interrupt clear (VOP_INT_CLR,with bit write mask), interrupt status (VOP_INT_STATUS).

3.7.8 RGB display mode

RGB display mode is used for RGB panel display and CCIR656 output. It is a continuous frames display mode.

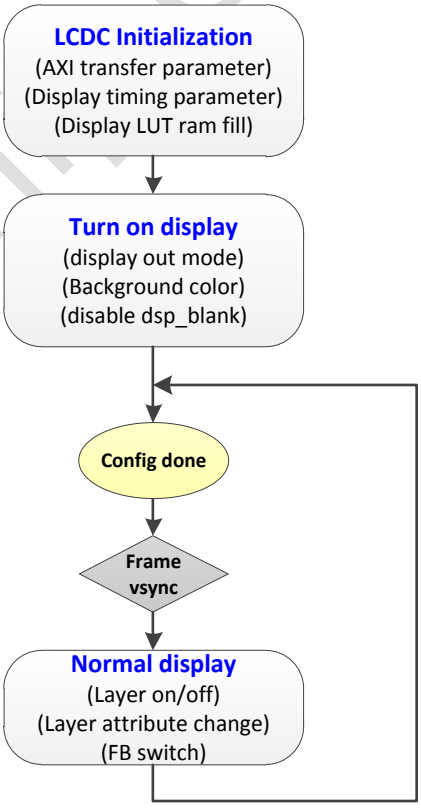


Fig. 3-17 VOP RGB mode Programming flow

1.VOP initialization

VOP initialization should be done before turning display on.
First, AXI bus parameter (VOP_SYS_CTRL) should be set for DMA transfer.
Second, display panel/interface timing should be set for display output. The registers are: VOP_DSP_HTOTAL_HS_END/ VOP_DSP_HACT_ST_END/ VOP_DSP_VTOTAL_HS_END/ VOP_DSP_VACT_ST_END/ VOP_DSP_VS_ST_END_F1/ VOP_DSP_VACT_ST_END_F1

2.Background display

Before normal display, the background display could be turn on.
First, set display output mode (VOP_DSP_CTRL0/1) according to display device.
Second, disable dsp_blank mode, which would not be enable until frame synchronization.
Finally, writing '1' to "VOP_REG_CFG_DONE" register then all the frame-sync registers will be enable at the beginning of next frame.

3.Normal display

In normal display, all the display layers' attribute could be different according display scenario. So there is a programming loop in this mode.
First, configure all the display layers' attribute registers for the change of image format, location, size, scaling factor, alpha and overlay and so on. Those register would not be enable until frame synchronization.
Finally, write '1' to "VOP_REG_CFG_DONE" register then all the frame-sync registers will be enable at the beginning of next frame.

Immediately control register

There are two type register in VOP , one type is effective immediately,the other is effective by frame sync.
Effective immediately registers list as follows,other registers are all effective by frame sync.

Table 3-3 effective immediately register table

register address	**Description**
0x008[23:21],0x008[15:8]	some dsp ctrl function bit
0x00c	sys ctrl1 register
0x018	background color register
0x01c	mcu ctrl register
0x038	win0 color key register
0x078	win1 color key register
0x188~0x19c	dsp_timing ctrl registers
0x1a0~0x1a8	pwm ctrl registers
0x1c8~0x1dc	cabc_gauss_parameter registers
0x1ec~0x1f4	frc pattern parameter registers

Chapter 4 Image Enhancement Processor（IEP）

4

4.1 Overview

The Image Enhancement Processor (IEP) receives data from and transmits data to system main memory by AXI bus, or output the data to Video Output Processor (VOP) directly.
The features of IEP are as follow:

- Image format
  - Input data: XRGB/RGB565/YUV420/YUV422
  - Output data: ARGB/RGB565/YUV420/YUV422
  - ARGB/XRGB/RGB565/YUV swap
  - YUV semi-planar/planar
  - BT601_l/BT601_f/BT709_l/BT709_f color space conversion
  - RGB dither up/down conversion
  - YUV up/down sampling conversion
  - Max resolution for static image up to 8192x8192
  - Max resolution for dynamic image
    - Deinterlace: 1920x1080
    - Sampling noise reduction: 1920x1080
    - Compression noise reduction: 4096x2304
    - Enhancement: 4096x2304
- Enhancement
  - Gamma adjustment with programmable mapping table
  - Hue/Saturation/Brightness/Contrast enhancement
  - Color enhancement with programmable coefficient
  - Detail enhancement with filter matrix up to 7x7
  - Edge enhancement with filter matrix up to 7x7
  - Programmable difference table for detail enhancement
  - Programmable distance table for detail and edge enhancement
- Noise reduction
  - Compression noise reduction with filter matrix up to 7x7
  - Programmable difference table for compression noise reduction
  - Programmable distance table for compression noise reduction
  - Spatial sampling noise reduction
  - Temporal sampling noise reduction
  - Optional coefficient for sampling noise reduction
- De-interlace
  - Input 4 fields, output 2 frames mode
  - Input 4 fields, output 1 frames mode
  - Input 2 fields, output 1 frames mode
  - Programmable motion detection coefficient
  - Programmable high frequency factor
  - Programmable edge interpolation parameter
- Interface
  - Programmable direct path to VOP
  - 32bit AHB bus slave
  - 64bit AXI bus master
  - Combined interrupt output

4.2 Block Diagram

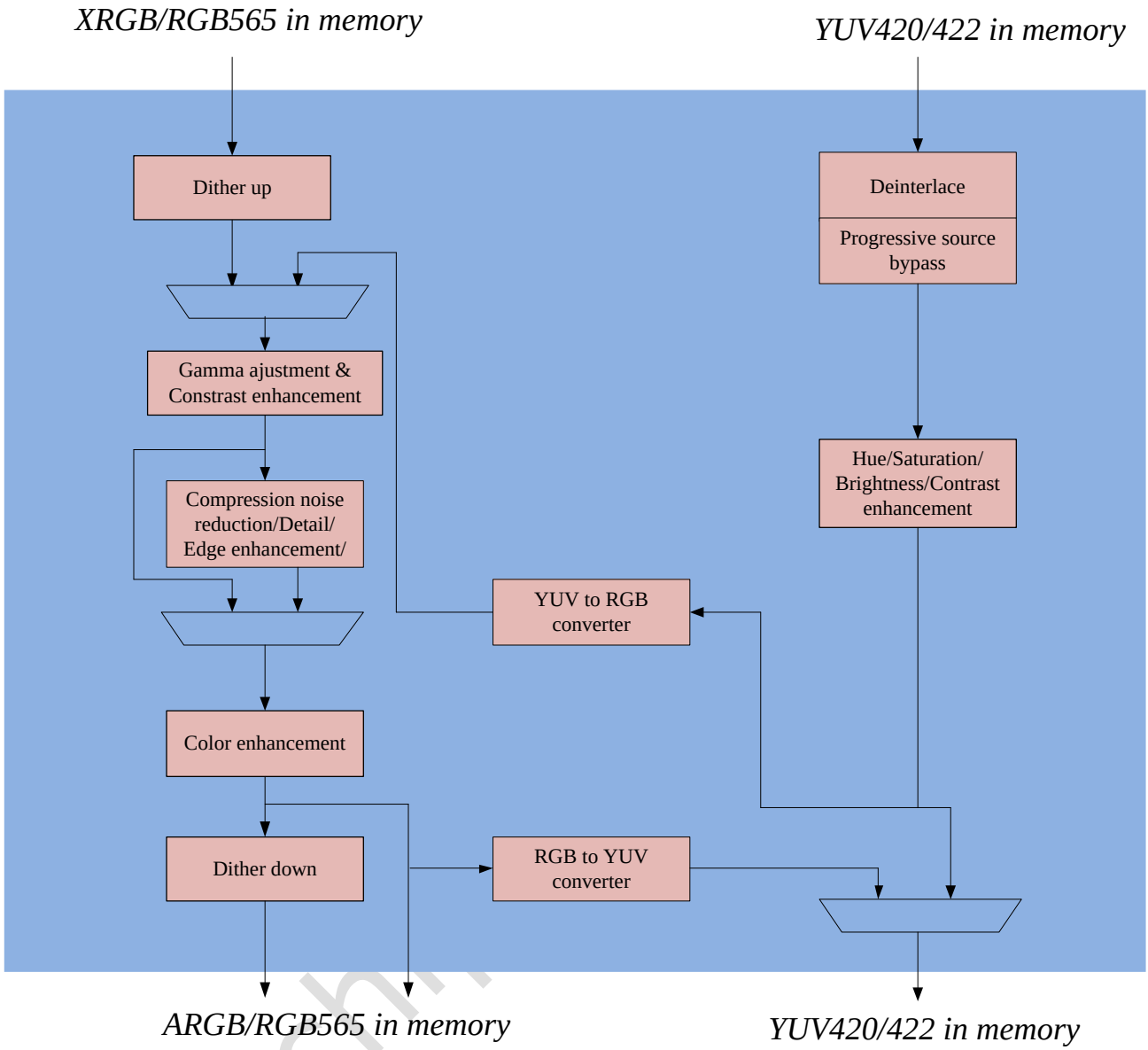


Fig. 4-1 IEP block diagram

The data path in IEP is in the previously diagram. The IEP comprises with:

- Deinterlace

There are five deinterlace mode including I4O2 (input 4 fields and output 2 frames once), I4O1B, I4O1T, I2O1B, I2O1T in the deinterlace block. YUV bypass is also supported. Pay attention if compression noise reduction, detail or edge enhancement work together with deinterlace is not allowed.

- Enhancement

Not only hue, saturation, brightness, contrast enhancement, but also blue screen, black screen and color bar are supported in YUV domain enhancement block. Gamma adjustment, edge enhancement, detail enhancement and color enhancement are supported in RGB domain enhancement block.

- Noise Reduction

Spatial and temporal sampling noise can be reduced in YUV domain noise reduction block. Compression noise can be reduced in RGB domain noise reduction block.

4.3 Function Description

4.3.1 Deinterlace

There are five deinterlace mode including I4O2, I4O1B, I4O1T, I2O1B and I2O1T in the deinterlace block. The I4O2 mode represents for 4 fields of input images and 2 frames of output images, so all of the two groups of source address registers and two groups of destination address registers need to be configured. For example, if source and destination format are both YUV420, the source address register IEP_SRC_ADDR_YRGB, IEP_SRC_ADDR_CBCR are used for source field0 and field 1, the source address register IEP_SRC_ADDR_Y1, IEP_SRC_ADDR_CBCR1 are used for source field2 and field3. The I4O1B and I4O1T mode have the same input images as the I4O2 mode, but only one frame output is generated once. The I2O1B and I2O1T mode have the same output as I4O1B and I4O1T mode, but only two fields input are needed. If bypass mode is selected, there are not any deinterlace operations. The parameter dil_ei_sel, dil_ei_radius, dil_ei_smooth, dil_ei_mode, dil_hf_en and dil_hf_fct in register IEP_CONFIG0 and registers IEP_DIL_MTN_TAB0~7 may have different influence in deinterlace effect depend on the type of the image source.

4.3.2 Noise reduction

Compression noise reduction is used for reducing the noise after the decompression of picture or video. Before the compression noise reduction is enabled, the IEP_ENH_DDE_COE0/1 from address 0x400 to 0x5FC for difference and distance coefficients must be written firstly. The filter matrix can be selected from 3x3/5x5 and the filter weight can be programmed by configuring IEP_ENH_RGB_CNFG.

4.3.3 Enhancement

Not only hue, saturation, brightness, contrast enhancement, but also blue screen, black screen and color bar are supported in this block. IEP_ENH_YUV_CNFG_0/1/2 registers can be configured to modify the YUV enhance parameters to satisfied with the requirement.
Before the gamma adjustment or contrast enhancement is enabled in RGB domain, the IEP_ENH_CG_TAB from address 0x100 to 0x3FC for B, G, R mapping must be written firstly.
If the color enhancement is enabled, the IEP_ENH_C_COE must be written the required value.
Before the edge or detail enhancement is enabled, the IEP_ENH_DDE_COE0/1 from address 0x400 to 0x5FC for difference and distance coefficients must be written firstly. The filter matrix can be selected from 3x3/5x5 and the filter weight can be programmed by configuring IEP_ENH_RGB_CNFG.

4.3.4 Format conversion

The color space conversion either from RGB to YUV or from YUV to RGB has the selections including BT601/709_L/F mode, and the input can be clipped or not.
If the source format is RGB565, dither up must be enabled. In contrary to the destination format is RGB565, dither down must be enabled.

4.3.5 Shadow registers

The configuration registers can be configured at any time, but they cannot have any effect immediately unless config_done is available and a new frame_start is enabled. The registers IEP_RAW_CONFIG0/1, IEP_RAW_VIR_IMG_WIDTH, IEP_RAW_IMG_SCL_FCT, IEP_RAW_SRC_IMG_SIZE, IEP_RAW_ENH_YUV_CNFG_0/1/2 corresponding to the registers have the similar names but without letters _RAW. They are used for raw register value reading before the configurations really have effect on the new frame.

4.3.6 VOP direct path

The IEP_DST_ADDR for DMA writing is useless if vop_path_en bit is set, because all RGB or YUV data is supplied for VOP directly from local bus via VOP and IEP.

4.4 Register Description

4.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
IEP_CONFIG0	0x0000	W	0x00000000	configuration register0
IEP_CONFIG1	0x0004	W	0x00000000	configuration register1
IEP_STATUS	0x0008	W	0x00000000	status register
IEP_INT	0x000c	W	0x00000000	interrupt register
IEP_FRM_START	0x0010	W	0x00000000	frame start
IEP_CONFIG_DONE	0x0018	W	0x00000000	configuration done
IEP_FRM_CNT	0x001c	W	0x00000000	frame counter
IEP_VIR_IMG_WIDTH	0x0020	W	0x01400140	Image virtual width
IEP_SRC_IMG_SIZE	0x0028	W	0x00ef013f	Source image width/height
IEP_DST_IMG_SIZE	0x002c	W	0x00ef013f	Destination image width/height
IEP_DST_IMG_WIDTH_TILE0	0x0030	W	0x00000000	Destination image tile0 width
IEP_DST_IMG_WIDTH_TILE1	0x0034	W	0x00000000	Destination image tile1 width
IEP_DST_IMG_WIDTH_TILE2	0x0038	W	0x00000000	Destination image tile2 width
IEP_DST_IMG_WIDTH_TILE3	0x003c	W	0x00000000	Destination image tile3 width
IEP_ENH_YUV_CNFG_0	0x0040	W	0x00000000	brightness,contrast,saturation adjustment
IEP_ENH_YUV_CNFG_1	0x0044	W	0x00000000	Hue configuration
IEP_ENH_YUV_CNFG_2	0x0048	W	0x00000000	color bar configuration
IEP_ENH_RGB_CNFG	0x004c	W	0x00000000	enhancement RGB configuration
IEP_ENH_C_COE	0x0050	W	0x00000000	rgb color enhancement coefficient
IEP_VERSION_INFO	0x0054	W	0x00000000	Version number for iep
IEP_RAW_CONFIG0	0x0058	W	0x00000000	configuration register0
IEP_RAW_CONFIG1	0x005c	W	0x00000000	configuration register1
IEP_RAW_VIR_IMG_WIDTH	0x0060	W	0x01400140	Image virtual width
IEP_RAW_SRC_IMG_SIZE	0x0068	W	0x00f00140	Source image width/height
IEP_RAW_DST_IMG_SIZE	0x006c	W	0x00f00140	Destination image width/height
IEP_RAW_ENH_YUV_CNFG_0	0x0070	W	0x00000000	brightness,contrast,saturation adjustment
IEP_RAW_ENH_YUV_CNFG_1	0x0074	W	0x00000000	Hue configuration
IEP_RAW_ENH_YUV_CNFG_2	0x0078	W	0x00000000	color bar configuration
IEP_RAW_ENH_RGB_CNFG	0x007c	W	0x00000000	enhancement RGB configuration
IEP_SRC_ADDR_YRGB	0x0080	W	0x00000000	Start address of source image(Y/RGB)

Name	Offset	Size	Reset Value	Description
IEP_SRC_ADDR_CBCR	0x0084	W	0x00000000	Start address of source image(Cb/Cr)
IEP_SRC_ADDR_CR	0x0088	W	0x00000000	Start address of source image(Cr)
IEP_SRC_ADDR_Y1	0x008c	W	0x00000000	Start address of source image(Y)
IEP_SRC_ADDR_CBCR1	0x0090	W	0x00000000	Start address of source image(Cb/Cr)
IEP_SRC_ADDR_CR1	0x0094	W	0x00000000	Start address of source image(Cr)
IEP_SRC_ADDR_Y_ITEMP	0x0098	W	0x00000000	Start address of source image(Y integer part)
IEP_SRC_ADDR_CBCR_ITEMP	0x009c	W	0x00000000	Start address of source image(CBCR integer part)
IEP_SRC_ADDR_CR_ITEMP	0x00a0	W	0x00000000	Start address of source image(CR integer part)
IEP_SRC_ADDR_Y_FTEMP	0x00a4	W	0x00000000	Start address of source image(Y fraction part)
IEP_SRC_ADDR_CBCR_FTEMP	0x00a8	W	0x00000000	Start address of source image(CBCR fraction part)
IEP_SRC_ADDR_CR_FTEMP	0x00ac	W	0x00000000	Start address of source image(CR fraction part)
IEP_DST_ADDR_YRGB	0x00b0	W	0x00000000	Start address of destination image(Y/RGB)
IEP_DST_ADDR_CBCR	0x00b4	W	0x00000000	Start address of destination image(Cb/Cr)
IEP_DST_ADDR_CR	0x00b8	W	0x00000000	Start address of destination image(Cr)
IEP_DST_ADDR_Y1	0x00bc	W	0x00000000	Start address of destination image(Y)
IEP_DST_ADDR_CBCR1	0x00c0	W	0x00000000	Start address of destination image(Cb/Cr)
IEP_DST_ADDR_CR1	0x00c4	W	0x00000000	Start address of destination image(Cr)
IEP_DST_ADDR_Y_ITEMP	0x00c8	W	0x00000000	Start address of destination image(Y integer part)
IEP_DST_ADDR_CBCR_ITEMP	0x00cc	W	0x00000000	Start address of destination image(CBCR integer part)
IEP_DST_ADDR_CR_ITEMP	0x00d0	W	0x00000000	Start address of destination image(CR integer part)
IEP_DST_ADDR_Y_FTEMP	0x00d4	W	0x00000000	Start address of destination image(Y fraction part)
IEP_DST_ADDR_CBCR_FTEMP	0x00d8	W	0x00000000	Start address of destination image(CBCR fraction part)
IEP_DST_ADDR_CR_FTEMP	0x00dc	W	0x00000000	Start address of destination image(CR fraction part)
IEP_DIL_MTN_TAB0	0x00e0	W	0x00000000	Deinterlace motion table0
IEP_DIL_MTN_TAB1	0x00e4	W	0x00000000	Deinterlace motion table1

Name	Offset	Size	Reset Value	Description
IEP_DIL_MTN_TAB2	0x00e8	W	0x00000000	Deinterlace motion table2
IEP_DIL_MTN_TAB3	0x00ec	W	0x00000000	Deinterlace motion table3
IEP_DIL_MTN_TAB4	0x00f0	W	0x00000000	Deinterlace motion table4
IEP_DIL_MTN_TAB5	0x00f4	W	0x00000000	Deinterlace motion table5
IEP_DIL_MTN_TAB6	0x00f8	W	0x00000000	Deinterlace motion table6
IEP_DIL_MTN_TAB7	0x00fc	W	0x00000000	Deinterlace motion table7
IEP_ENH_CG_TAB	0x0100	W	0x00000000	contrast and gamma enhancement table
IEP_ENH_DDE_COE0	0x0400	W	0x00000000	denoise,detail and edge enhancement coefficient
IEP_ENH_DDE_COE1	0x0500	W	0x00000000	denoise,detail and edge enhancement coefficient
IEP_PERF_LATENCY_CTRL0	0x0600	W	0x00000014	Axi performance latency module contrl register0
IEP_PERF_LATENCY_CTRL1	0x0604	W	0x00000011	PERF_LATENCY_CTRL1
IEP_PERF_RD_MAX_LATENCY_NUM0	0x0608	W	0x00000000	Read max latency number
IEP_PERF_RD_LATENCY_SAMP_NUM	0x060c	W	0x00000000	The number of bigger than configed threshold value
IEP_PERF_RD_LATENCY_ACC_SUM	0x0610	W	0x00000000	Total sample number
IEP_PERF_WR_AXI_TOTAL_BYTE	0x0614	W	0x00000000	perf_wr_axi_total_byte
IEP_PERF_WORKING_CNT	0x0618	W	0x00000000	perf_working_cnt
IEP_PERF_RD_AXI_TOTAL_BYTE	0x061c	W	0x00000000	perf_rd_axi_total_byte
IEP_MMU_DTE_ADDR	0x0800	W	0x00000000	MMU current page table address
IEP_MMU_STATUS	0x0804	W	0x00000018	MMU status register
IEP_MMU_CMD	0x0808	W	0x00000000	MMU command register
IEP_MMU_PAGE_FAULT_ADDR	0x080c	W	0x00000000	MMU logic address of last page fault
IEP_MMU_ZAP_ONE_LINE	0x0810	W	0x00000000	MMU zap cache line register
IEP_MMU_INT_RAWSTAT	0x0814	W	0x00000000	MMU raw interrupt status register
IEP_MMU_INT_CLEAR	0x0818	W	0x00000000	MMU interrupt clear register
IEP_MMU_INT_MASK	0x081c	W	0x00000000	MMU interrupt mask register
IEP_MMU_INT_STATUS	0x0820	W	0x00000000	MMU interrupt status register
IEP_MMU_AUTO_GATING	0x0824	W	0x00000001	MMU clock auto gating register

4.4.2 Detail Register Description

IEP_CONFIG0

Address: Operational Base + offset (0x0000)

configuration register0

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved

Bit	Attr	Reset Value	Description
23	RW	0x0	dil_ei_sel deinterlace edge interpolation select
22:21	RW	0x0	dil_ei_radius deinterlace edge interpolation radius
20	RW	0x0	rgb_con_gam_order RGB contrast enhancement and gamma adjustment operation order select. 0:CG prior to DDE 1:DDE prior to CG (CG represent for contrast & gamma operation, and DDE represent for denoise, detail or edge enhancement operation)
19:18	RW	0x0	rgb_enh_sel RGB enhancement select 00: no operation 01: denoise 10: detail enhancement 11: edge enhancement
17	RW	0x0	rgb_con_gam_en RGB contrast enhancement and gamma adjustment enable 0:disable 1:enable
16	RW	0x0	rgb_color_enh_en RGB color enhancement enable 0:disable 1:enable
15	RW	0x0	dil_ei_smooth deinterlace edge interpolation for smooth effect 0: disable 1: enable
14	RW	0x0	yuv_enh_en yuv enhancement enable 0:disable 1:enable
13	RW	0x0	yuv_dns_en YUV 3D denoise enable 0:disable 1:enable
12	RW	0x0	dil_ei_mode deinterlace edge interpolation 0: disable 1: enable
11	RW	0x0	dil_hf_en deinterlace high frequency calculation enable 0: disable 1: enable

Bit	Attr	Reset Value	Description
10:8	RW	0x0	dil_mode Deinterlace mode select: 000: YUV deinterlace and bypass path disable; 001: I4O2 mode 010: I4O1B mode 011: I4O1T mode 100: I2O1B mode 101: I2O1T mode 110: bypass mode
7:1	RW	0x00	dil_hf_fct deinterlace high frequency factor
0	RW	0x0	vop_path_en VOP direct path enable 0:disable 1:enable

IEP_CONFIG1
Address: Operational Base + offset (0x0004)
configuration register1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	glb_alpha global alpha value only valid when destination format is ARGB
23	RW	0x0	rgb2yuv_input_clip RGB to YUV input range 0:R/G/B=[0,255] 1:R/G/B=[16,235]
22	RW	0x0	yuv2rgb_input_clip YUV to RGB input range 0:Y/U/V=[0,255] 1:Y=[16,235],U/V=[16,240]
21	RW	0x0	rgb_to_yuv_en RGB to YUV conversion enable 0: disable 1: enable
20	RW	0x0	yuv_to_rgb_en YUV to RGB conversion enable 0: disable 1: enable
19:18	RW	0x0	rgb2yuv_coe_sel rgb2yuv coefficient select 00:bt601_1 01:bt601_f 10:bt709_1 11:bt709_f

Bit	Attr	Reset Value	Description
17:16	RW	0x0	yuv2rgb_coe_sel yuv2rgb coefficient select 00:bt601_1 01:bt601_f 10:bt709_1 11:bt709_f
15	RW	0x0	dthr_down_en dither down enable 0: disable 1: enable
14	RW	0x0	dthr_up_en dither up enable 0: disable 1: enable
13:12	RW	0x0	dst_yuv_swap destination YUV swap 00:SP UV 01:SP VU 10, 11:P
11:10	RW	0x0	dst_rgb_swap destination RGB swap ARGB destination 00:ARGB 01:ABGR 10:RGBA 11:BGRA RGB565 destination 00,10:RGB 01,11:BGR
9:8	RW	0x0	dst_fmt Ouput image Format 00 : ARGB 01 : RGB565 10 : YUV422 11 : YUV420
7:6	RO	0x0	reserved
5:4	RW	0x0	src_yuv_swap source YUV swap 00:SP UV 01:SP VU 10, 11:P

Bit	Attr	Reset Value	Description
3:2	RW	0x0	src_rgb_swap source RGB swap XRGB source 00:XRGB 01:XBGR 10:RGBX 11:BGRX RGB565 source 00,10:RGB 01,11:BGR
1:0	RW	0x0	src_fmt Input image Format 00 : XRGB 01 : RGB565 10 : YUV422 11 : YUV420

IEP_STATUS
Address: Operational Base + offset (0x0008)
status register

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19	RW	0x0	rrgb_idle_ack RGB read DMA idle acknowlege
18	RW	0x0	wrgb_idle_ack RGB write DMA idle acknowlege
17	RW	0x0	ryuv_idle_ack YUV read DMA idle acknowlege
16	RW	0x0	wyuv_idle_ack YUV write DMA idle acknowlege
15:9	RO	0x0	reserved
8	RO	0x0	voi_sts vop direct path status 00:idle 01:working
7	RO	0x0	rrgb_sts RGB DMA read status 00:idle 01:working
6	RO	0x0	wrgb_sts RGB DMA write status 00:idle 01:working

Bit	Attr	Reset Value	Description
5	RO	0x0	ryuv_sts YUV DMA read status 00:idle 01:working
4	RO	0x0	wyuv_sts YUV DMA write status 00:idle 01:working
3	RO	0x0	dde_sts RGB denoise/enhancement status 00:idle 01:working
2	RO	0x0	dil_sts de-interlace or yuv bypass status 00:idle 01:working
1	RO	0x0	reserved
0	RO	0x0	dns_sts YUV 3D denoise status 00:idle 01:working

IEP_INT
Address: Operational Base + offset (0x000c)
interrupt register

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	W1C	0x0	frm_done_int_clr Frame process done interrupt clear After be set to 1, this bit will be clear automatically.
15:9	RO	0x0	reserved
8	RW	0x0	frm_done_int_en Frame process done interrupt enable: 0: disable; 1: enable;
7:1	RO	0x0	reserved
0	RO	0x0	frm_done_int Frame process done interrupt 0: inactive; 1: active;

IEP_FRM_START
Address: Operational Base + offset (0x0010)
frame start

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	W1C	0x0	frm_start frame start Write 1, self clear.

IEP_CONFIG_DONE
Address: Operational Base + offset (0x0018)
configuration done

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	config_done configuration done Wait for frame start to update raw register configuration to really used registers.

IEP_FRM_CNT
Address: Operational Base + offset (0x001c)
frame counter

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	frm_cnt frame counter Self increase one after a frame operation is finished. Write arbitrary value to clear to zero.

IEP_VIR_IMG_WIDTH
Address: Operational Base + offset (0x0020)
Image virtual width

Bit	Attr	Reset Value	Description
31:16	RW	0x0140	dst_vir_image_width Destination virtual image width
15:0	RW	0x0140	src_vir_image_width Source virtual image width

IEP_SRC_IMG_SIZE
Address: Operational Base + offset (0x0028)
Source image width/height

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x00ef	src_image_height source image height
15:13	RO	0x0	reserved
12:0	RW	0x013f	src_image_width source image width

IEP_DST_IMG_SIZE
Address: Operational Base + offset (0x002c)
Destination image width/height

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x00ef	dst_image_height Destination image height
15:13	RO	0x0	reserved
12:0	RW	0x013f	dst_image_width Destination image width

IEP_DST_IMG_WIDTH_TILE0
Address: Operational Base + offset (0x0030)
Destination image tile0 width

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	dst_image_width_tile0 Destination image tile0 width

IEP_DST_IMG_WIDTH_TILE1
Address: Operational Base + offset (0x0034)
Destination image tile1 width

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:0	RW	0x000	dst_image_width_tile1 Destination image tile1 width

IEP_DST_IMG_WIDTH_TILE2
Address: Operational Base + offset (0x0038)
Destination image tile2 width

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:0	RW	0x000	dst_image_width_tile2 Destination image tile2 width

IEP_DST_IMG_WIDTH_TILE3
Address: Operational Base + offset (0x003c)
Destination image tile3 width

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:0	RW	0x000	dst_image_width_tile3 Destination image tile3 width

IEP_ENH_YUV_CNFG_0
Address: Operational Base + offset (0x0040)
brightness,contrast,saturation adjustment

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	sat_con YUV saturation and contrast adjustment saturation * contrast range from 0 to 1.992*1.992, and this value is saturation* contrast * 128
15:8	RW	0x00	contrast YUV contrast adjustment contrast value range from 0 to 1.992, and this value is contrast*128.
7:6	RO	0x0	reserved
5:0	RW	0x00	brightness YUV brightness adjustment range from -32 to 31 000000:0; 000001:1; …… 011111:31; 100000:-32; 100001:-31; …… 111110:-2; 111111:-1;

IEP_ENH_YUV_CNFG_1
Address: Operational Base + offset (0x0044)
Hue configuration

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:8	RW	0x00	cos_hue the cos function value for hue adjustment sin function value range from 0.866 to 1 ,and this value is cos * 128 ,no sign bit
7:0	RW	0x00	sin_hue the sin function value for hue adjustment sin function value range from -0.5 to 0.5 ,and this value is sin * 128 ,and the high bit is sign bit

IEP_ENH_YUV_CNFG_2
Address: Operational Base + offset (0x0048)
color bar configuration

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved

Bit	Attr	Reset Value	Description
25:24	RW	0x0	video_mode video mode 00:black screen 01:blue screen 10:color bars 11:normal video
23:16	RW	0x00	color_bar_v color bar v value
15:8	RW	0x00	color_bar_u color bar u value
7:0	RW	0x00	color_bar_y color bar y value

IEP_ENH_RGB_CNFG
Address: Operational Base + offset (0x004c)
enhancement RGB configuration

Bit	Attr	Reset Value	Description
31:30	RW	0x0	luma_spat_sel 3D denoise luma spatial coefficient select
29:28	RW	0x0	luma_temp_sel 3D denoise luma temporal coefficient select
27:26	RW	0x0	chroma_spat_sel 3D denoise chroma spatial coefficient select
25:24	RW	0x0	chroma_temp_sel 3D denoise chroma temporal coefficient select
23:16	RW	0x00	enh_threshold enhancement threshold In denoise and detail enhancement operation, more than the threshold, considering as detail; but if less than the threshold, considering as noise, need to to be filtered.
15	RO	0x0	reserved

Bit	Attr	Reset Value	Description
14:8	RW	0x00	enh_alpha enhancement alpha value 0000000:0 0000001:1/16 0000010:2/16 …… 0001111:15/16 0010000:1 0010001:1+1/16; 0010010:1+2/16; 0010011:1+3/16; …… 0100000:2; …… 0110000:3; …… 1000000:4; …… 1010000:5; …… 1100000:6; other : reserved
7:2	RO	0x0	reserved
1:0	RW	0x0	enh_radius enhancement radius 00:R=1 01:R=2 10:R=3 11:R=4

IEP_ENH_C_COE
Address: Operational Base + offset (0x0050)
rgb color enhancement coefficient

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6:5	RW	0x0	c_int_coe color enhancement integer coefficient
4:0	RW	0x00	c_frac_coe color enhancement fraction coefficient

IEP_VERSION_INFO
Address: Operational Base + offset (0x0054)
Version number for iep

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:28	RW	0x0	major IP major vertion used for IP structure version infomation
27:20	RW	0x0	minor minor vertion big feature change under same structure
19:0	RW	0x000000	svnbuild rtl current svn number

IEP_RAW_CONFIG0
Address: Operational Base + offset (0x0058)
configuration register0

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23	RW	0x0	dil_ei_sel deinterlace edge interpolation select
22:21	RW	0x0	dil_ei_radius deinterlace edge interpolation radius
20	RW	0x0	rgb_con_gam_order RGB contrast enhancement and gamma adjustment operation order select. 0:CG prior to DDE 1:DDE prior to CG (CG represent for contrast & gamma operation, and DDE represent for de-noise, detail or edge enhancement operation)
19:18	RW	0x0	rgb_enh_sel RGB enhancement select 00: no operation 01: denoise 10: detail enhancement 11: edge enhancement
17	RW	0x0	rgb_con_gam_en RGB contrast enhancement and gamma adjustment enable 0:disable 1:enable
16	RW	0x0	rgb_color_enh_en RGB color enhancement enable 0:disable 1:enable
15	RW	0x0	dil_ei_smooth deinterlace edge interpolation for smooth effect 0: disable 1: enable

Bit	Attr	Reset Value	Description
14	RW	0x0	yuv_enh_en yuv enhancement enable 0:disable 1:enable
13	RW	0x0	yuv_dns_en YUV 3D denoise enable 0:disable 1:enable
12	RW	0x0	dil_ei_mode deinterlace edge interpolation 0: disable 1: enable
11	RW	0x0	dil_hf_en deinterlace high frequency calculation enable 0: disable 1: enable
10:8	RW	0x0	dil_mode Deinterlace mode select: 000: YUV deinterlace and bypass path disable; 001: I4O2 mode 010: I4O1B mode 011: I4O1T mode 100: I2O1B mode 101: I2O1T mode 110: bypass mode
7:1	RW	0x00	dil_hf_fct deinterlace high frequency factor
0	RW	0x0	vop_path_en VOP direct path enable 0:disable 1:enable

IEP_RAW_CONFIG1

Address: Operational Base + offset (0x005c)

configuration register1

Bit	Attr	Reset Value	Description
31:24	RO	0x00	glb_alpha global alpha value only valid when destination format is ARGB
23	RO	0x0	rgb2yuv_input_clip RGB to YUV input range 0:R/G/B=[0,255] 1:R/G/B=[16,235]

Bit	Attr	Reset Value	Description
22	RO	0x0	yuv2rgb_input_clip YUV to RGB input range 0:Y/U/V=[0,255] 1:Y=[16,235],U/V=[16,240]
21	RO	0x0	rgb_to_yuv_en RGB to YUV conversion enable 0: disable 1: enable
20	RO	0x0	yuv_to_rgb_en YUV to RGB conversion enable 0: disable 1: enable
19:18	RO	0x0	rgb2yuv_coe_sel rgb2yuv coefficient select 00:bt601_1 01:bt601_f 10:bt709_1 11:bt709_f
17:16	RO	0x0	yuv2rgb_coe_sel yuv2rgb coefficient select 00:bt601_1 01:bt601_f 10:bt709_1 11:bt709_f
15	RO	0x0	dthr_down_en dither down enable 0: disable 1: enable
14	RO	0x0	dthr_up_en dither up enable 0: disable 1: enable
13:12	RO	0x0	dst_yuv_swap destination YUV swap 00:SP UV 01:SP VU 10, 11:P

Bit	Attr	Reset Value	Description
11:10	RO	0x0	dst_rgb_swap destination RGB swap ARGB destination 00:ARGB 01:ABGR 10:RGBA 11:BGRA RGB565 destination 00,10:RGB 01,11:BGR
9:8	RO	0x0	dst_fmt Ouput image Format 00 : ARGB 01 : RGB565 10 : YUV422 11 : YUV420
7:6	RO	0x0	reserved
5:4	RO	0x0	src_yuv_swap source YUV swap 00:SP UV 01:SP VU 10, 11:P
3:2	RO	0x0	src_rgb_swap source RGB swap XRGB source 00:XRGB 01:XBGR 10:RGBX 11:BGRX RGB565 source 00,10:RGB 01,11:BGR
1:0	RO	0x0	src_fmt Input image Format 00 : XRGB 01 : RGB565 10 : YUV422 11 : YUV420

IEP_RAW_VIR_IMG_WIDTH
Address: Operational Base + offset (0x0060)
Image virtual width

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RO	0x0140	dst_vir_image_width Destination virtual image width
15:0	RO	0x0140	src_vir_image_width Source virtual image width

IEP_RAW_SRC_IMG_SIZE
Address: Operational Base + offset (0x0068)
Source image width/height

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RO	0x00f0	src_image_height source image height
15:13	RO	0x0	reserved
12:0	RO	0x0140	src_image_width source image width

IEP_RAW_DST_IMG_SIZE
Address: Operational Base + offset (0x006c)
Destination image width/height

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RO	0x00f0	dst_image_height Destination image height
15:13	RO	0x0	reserved
12:0	RO	0x0140	dst_image_width Destination image width

IEP_RAW_ENH_YUV_CNFG_0
Address: Operational Base + offset (0x0070)
brightness,contrast,saturation adjustment

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RO	0x000	sat_con YUV saturation and contrast adjustment saturation * contrast range from 0 to 1.992*1.992, and this value is saturation* contrast * 128
15:8	RO	0x00	contrast YUV contrast adjustment contrast value range from 0 to 1.992, and this value is contrast*128.
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:0	RO	0x00	brightness YUV brightness adjustment range from -32 to 31 000000:0; 000001:1; …… 011111:31; 100000:-32; 100001:-31; …… 111110:-2; 111111:-1;

IEP_RAW_ENH_YUV_CNFG_1
Address: Operational Base + offset (0x0074)
Hue configuration

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:8	RO	0x00	cos_hue the cos function value for hue adjustment sin function value range from 0.866 to 1 ,and this value is cos * 128 ,no sign bit
7:0	RO	0x00	sin_hue the sin function value for hue adjustment sin function value range from -0.5 to 0.5 ,and this value is sin * 128 ,and the high bit is sign bit

IEP_RAW_ENH_YUV_CNFG_2
Address: Operational Base + offset (0x0078)
color bar configuration

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:24	RO	0x0	video_mode video mode 00:black screen 01:blue screen 10:color bars 11:normal video
23:16	RO	0x00	color_bar_v color bar v value
15:8	RO	0x00	color_bar_u color bar u value
7:0	RO	0x00	color_bar_y color bar y value

IEP_RAW_ENH_RGB_CNFG
Address: Operational Base + offset (0x007c)
enhancement RGB configuration

Bit	Attr	Reset Value	Description
31:30	RW	0x0	luma_spat_sel 3D denoise luma spatial coefficient select
29:28	RW	0x0	luma_temp_sel 3D denoise luma temporal coefficient select
27:26	RW	0x0	chroma_spat_sel 3D denoise chroma spatial coefficient select
25:24	RW	0x0	chroma_temp_sel 3D denoise chroma temporal coefficient select
23:16	RW	0x00	enh_threshold enhancement threshold In denoise and detail enhancement operation, more than the threshold, considering as detail; but if less than the threshold, considering as noise, need to to be filtered.
15	RO	0x0	reserved
14:8	RW	0x00	enh_alpha enhancement alpha value 0000000:0 0000001:1/16 0000010:2/16 …… 0001111:15/16 0010000:1 0010001:1+1/16; 0010010:1+2/16; 0010011:1+3/16; …… 0100000:2; …… 0110000:3; …… 1000000:4; …… 1010000:5; …… 1100000:6; other : reserved
7:2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1:0	RW	0x0	enh_radius enhancement radius 00:R=1 01:R=2 10:R=3 11:R=4

IEP_SRC_ADDR_YRGB
Address: Operational Base + offset (0x0080)
Start address of source image(Y/RGB)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_image_yrgb_mst Source image data YRGB start address in Memory

IEP_SRC_ADDR_CBCR
Address: Operational Base + offset (0x0084)
Start address of source image(Cb/Cr)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_image_cbcr_mst Source image data CbCr start address in Memory

IEP_SRC_ADDR_CR
Address: Operational Base + offset (0x0088)
Start address of source image(Cr)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_image_cr_mst Source image data Cr start address in Memory

IEP_SRC_ADDR_Y1
Address: Operational Base + offset (0x008c)
Start address of source image(Y)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_image_y_mst Source image data Y start address in Memory

IEP_SRC_ADDR_CBCR1
Address: Operational Base + offset (0x0090)
Start address of source image(Cb/Cr)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_image_cbcr_mst Source image data CbCr start address in Memory

IEP_SRC_ADDR_CR1
Address: Operational Base + offset (0x0094)
Start address of source image(Cr)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_image_cr_mst Source image data Cr start address in Memory

IEP_SRC_ADDR_Y_ITEMP
Address: Operational Base + offset (0x0098)
Start address of source image(Y integer part)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_image_y_mst_itemp Interger part source image data Y start address in Memory

IEP_SRC_ADDR_CBCR_ITEMP
Address: Operational Base + offset (0x009c)
Start address of source image(CBCR integer part)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_image_cbcr_mst_cbcr_itemp Interger part source image data CBCR start address in Memory

IEP_SRC_ADDR_CR_ITEMP
Address: Operational Base + offset (0x00a0)
Start address of source image(CR integer part)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_image_cr_mst_cr_itemp Interger part source image data CR start address in Memory

IEP_SRC_ADDR_Y_FTEMP
Address: Operational Base + offset (0x00a4)
Start address of source image(Y fraction part)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_image_y_mst_ftemp Fraction part source image data Y start address in Memory

IEP_SRC_ADDR_CBCR_FTEMP
Address: Operational Base + offset (0x00a8)
Start address of source image(CBCR fraction part)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_image_cbcr_mst_ftemp Fraction part source image data CBCR start address in Memory

IEP_SRC_ADDR_CR_FTEMP
Address: Operational Base + offset (0x00ac)
Start address of source image(CR fraction part)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_image_cr_mst_ftemp Fraction part source image data CR start address in Memory

IEP_DST_ADDR_YRGB
Address: Operational Base + offset (0x00b0)
Start address of destination image(Y/RGB)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_image_yrgb_mst Destination image data YRGB start address in Memory

IEP_DST_ADDR_CBCR
Address: Operational Base + offset (0x00b4)
Start address of destination image(Cb/Cr)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_image_cbcr_mst Destination image data CBCR start address in Memory

IEP_DST_ADDR_CR
Address: Operational Base + offset (0x00b8)
Start address of destination image(Cr)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_image_cr_mst Destination image data CR start address in Memory

IEP_DST_ADDR_Y1
Address: Operational Base + offset (0x00bc)
Start address of destination image(Y)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_image_y_mst Destination image data Y start address in Memory

IEP_DST_ADDR_CBCR1
Address: Operational Base + offset (0x00c0)
Start address of destination image(Cb/Cr)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_image_cbcr_mst Destination image data CbCr start address in Memory

IEP_DST_ADDR_CR1
Address: Operational Base + offset (0x00c4)
Start address of destination image(Cr)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_image_cr_mst Destination image data Cr start address in Memory

IEP_DST_ADDR_Y_ITEMP
Address: Operational Base + offset (0x00c8)
Start address of destination image(Y integer part)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_image_y_mst_itemp Interger part destination image data Y start address in Memory

IEP_DST_ADDR_CBCR_ITEMP
Address: Operational Base + offset (0x00cc)
Start address of destination image(CBCR integer part)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_image_cbcr_mst_itemp Int part destination image data CBCR start address in Memory

IEP_DST_ADDR_CR_ITEMP
Address: Operational Base + offset (0x00d0)
Start address of destination image(CR integer part)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_image_cr_mst_itemp Interger part destination image data CR start address in Memory

IEP_DST_ADDR_Y_FTEMP
Address: Operational Base + offset (0x00d4)
Start address of destination image(Y fraction part)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_image_y_mst_ftemp Fraction part destination image data Y start address in Memory

IEP_DST_ADDR_CBCR_FTEMP
Address: Operational Base + offset (0x00d8)
Start address of destination image(CBCR fraction part)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_image_cbcr_mst_ftemp Fraction part destination image data CBCR start address in Mem

IEP_DST_ADDR_CR_FTEMP
Address: Operational Base + offset (0x00dc)
Start address of destination image(CR fraction part)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_image_cr_mst_ftemp Fraction part destination image data CR start address

IEP_DIL_MTN_TAB0
Address: Operational Base + offset (0x00e0)
Deinterlace motion table0

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

Bit	Attr	Reset Value	Description
30:24	RW	0x00	mtn_sub_tab3 motion sub table3
23	RO	0x0	reserved
22:16	RW	0x00	mtn_sub_tab2 motion sub table2
15	RO	0x0	reserved
14:8	RW	0x00	mtn_sub_tab1 motion sub table1
7	RO	0x0	reserved
6:0	RW	0x00	mtn_sub_tab0 motion sub table0

IEP_DIL_MTN_TAB1
Address: Operational Base + offset (0x00e4)
Deinterlace motion table1

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	mtn_sub_tab3 motion sub table3
23	RO	0x0	reserved
22:16	RW	0x00	mtn_sub_tab2 motion sub table2
15	RO	0x0	reserved
14:8	RW	0x00	mtn_sub_tab1 motion sub table1
7	RO	0x0	reserved
6:0	RW	0x00	mtn_sub_tab0 motion sub table0

IEP_DIL_MTN_TAB2
Address: Operational Base + offset (0x00e8)
Deinterlace motion table2

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	mtn_sub_tab3 motion sub table3
23	RO	0x0	reserved
22:16	RW	0x00	mtn_sub_tab2 motion sub table2
15	RO	0x0	reserved
14:8	RW	0x00	mtn_sub_tab1 motion sub table1
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:0	RW	0x00	mtn_sub_tab0 motion sub table0

IEP_DIL_MTN_TAB3
Address: Operational Base + offset (0x00ec)
Deinterlace motion table3

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	mtn_sub_tab3 motion sub table3
23	RO	0x0	reserved
22:16	RW	0x00	mtn_sub_tab2 motion sub table2
15	RO	0x0	reserved
14:8	RW	0x00	mtn_sub_tab1 motion sub table1
7	RO	0x0	reserved
6:0	RW	0x00	mtn_sub_tab0 motion sub table0

IEP_DIL_MTN_TAB4
Address: Operational Base + offset (0x00f0)
Deinterlace motion table4

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	mtn_sub_tab3 motion sub table3
23	RO	0x0	reserved
22:16	RW	0x00	mtn_sub_tab2 motion sub table2
15	RO	0x0	reserved
14:8	RW	0x00	mtn_sub_tab1 motion sub table1
7	RO	0x0	reserved
6:0	RW	0x00	mtn_sub_tab0 motion sub table0

IEP_DIL_MTN_TAB5
Address: Operational Base + offset (0x00f4)
Deinterlace motion table5

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	mtn_sub_tab3 motion sub table3

Bit	Attr	Reset Value	Description
23	RO	0x0	reserved
22:16	RW	0x00	mtn_sub_tab2 motion sub table2
15	RO	0x0	reserved
14:8	RW	0x00	mtn_sub_tab1 motion sub table1
7	RO	0x0	reserved
6:0	RW	0x00	mtn_sub_tab0 motion sub table0

IEP_DIL_MTN_TAB6
Address: Operational Base + offset (0x00f8)
Deinterlace motion table6

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	mtn_sub_tab3 motion sub table3
23	RO	0x0	reserved
22:16	RW	0x00	mtn_sub_tab2 motion sub table2
15	RO	0x0	reserved
14:8	RW	0x00	mtn_sub_tab1 motion sub table1
7	RO	0x0	reserved
6:0	RW	0x00	mtn_sub_tab0 motion sub table0

IEP_DIL_MTN_TAB7
Address: Operational Base + offset (0x00fc)
Deinterlace motion table7

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	mtn_sub_tab3 motion sub table3
23	RO	0x0	reserved
22:16	RW	0x00	mtn_sub_tab2 motion sub table2
15	RO	0x0	reserved
14:8	RW	0x00	mtn_sub_tab1 motion sub table1
7	RO	0x0	reserved
6:0	RW	0x00	mtn_sub_tab0 motion sub table0

IEP_ENH_CG_TAB
Address: Operational Base + offset (0x0100)
contrast and gamma enhancement table

Bit	Attr	Reset Value	Description
31:24	RW	0x00	cg_tab_3 cg table 3 pixel value 3,7,11,15,……mapping
23:16	RW	0x00	cg_tab_2 cg table 2 pixel value 2,6,10,14,……mapping
15:8	RW	0x00	cg_tab_1 cg table 1 pixel value 1,5,9,13,……mapping
7:0	RW	0x00	cg_tab_0 cg table 0 256x8bit contrast & gamma mapping table pixel value 0,4,8,12,……mapping

IEP_ENH_DDE_COE0
Address: Operational Base + offset (0x0400)
denoise,detail and edge enhancement coefficient

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	dde_coe_3 dde coefficient 3 coefficient number 3,7,11,15,……
23:22	RO	0x0	reserved
21:16	RW	0x00	dde_coe_2 dde coefficient 2 coefficient number 2,6,10,14,……
15:14	RO	0x0	reserved
13:8	RW	0x00	dde_coe_1 dde coefficient 1 coefficient number 1,5,9,13,……
7:6	RO	0x0	reserved
5:0	RW	0x00	dde_coe_0 dde coefficient 0 256x6bit cofficient for denoise and detail enhancement coefficient number 0,4,8,12,……

IEP_ENH_DDE_COE1
Address: Operational Base + offset (0x0500)
denoise,detail and edge enhancement coefficient

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

Bit	Attr	Reset Value	Description
29:24	RW	0x00	dde_coe_3 dde coefficient 3 coefficient number 3,7,11,15,……
23:22	RO	0x0	reserved
21:16	RW	0x00	dde_coe_2 dde coefficient 3 coefficient number 2,6,10,14,……
15:14	RO	0x0	reserved
13:8	RW	0x00	dde_coe_1 dde coefficient 1 coefficient number 1,5,9,13,……
7:6	RO	0x0	reserved
5:0	RW	0x00	dde_coe_0 dde coefficient 1 81x6bit cofficient for denoise and detail enhancement coefficient number 0,4,8,12,……

IEP_PERF_LATENCY_CTRL0
Address: Operational Base + offset (0x0600)
Axi performance latency module contrl register0

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:8	RW	0x000	sw_rd_latency_thr
7:4	RW	0x1	sw_rd_latency_id
3	RW	0x0	sw_axi_cnt_type
2	RW	0x1	sw_axi_perf_frm_type latency mode 1'b0: clear by software configuration 1'b1: clear by frame end
1	RW	0x0	sw_axi_perf_clr_e 1'b0: software clear disable 1'b1: software clear enalbe
0	RW	0x0	sw_axi_perf_work_e 1'b0: disable 1'b1: enable

IEP_PERF_LATENCY_CTRL1
Address: Operational Base + offset (0x0604)
PERF_LATENCY_CTRL1

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:8	RW	0x0	sw_aw_count_id
7:4	RW	0x1	sw_ar_count_id
3	RW	0x0	sw_aw_cnt_id_type
2	RW	0x0	sw_ar_cnt_id_type

Bit	Attr	Reset Value	Description
1:0	RW	0x1	sw_addr_align_type

IEP_PERF_RD_MAX_LATENCY_NUM0
Address: Operational Base + offset (0x0608)
Read max latency number

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RO	0x0000	rd_max_latency_num_ch0 read max latency value of channel 0

IEP_PERF_RD_LATENCY_SAMP_NUM
Address: Operational Base + offset (0x060c)
The number of bigger than configed threshold value

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rd_latency_thr_num_ch0 read latency thr number channel 0

IEP_PERF_RD_LATENCY_ACC_SUM
Address: Operational Base + offset (0x0610)
Total sample number

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rd_latency_acc_sum

IEP_PERF_WR_AXI_TOTAL_BYTE
Address: Operational Base + offset (0x0614)
perf_wr_axi_total_byte

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_wr_axi_total_byte

IEP_PERF_WORKING_CNT
Address: Operational Base + offset (0x0618)
perf_working_cnt

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_working_cnt

IEP_PERF_RD_AXI_TOTAL_BYTE
Address: Operational Base + offset (0x061c)
perf_rd_axi_total_byte

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_rd_axi_total_byte

IEP_MMU_DTE_ADDR
Address: Operational Base + offset (0x0800)
MMU current page table address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_dte_addr page table address

IEP_MMU_STATUS
Address: Operational Base + offset (0x0804)
MMU status register

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:6	RW	0x00	mmu_page_fault_bus_id Index of master responsible for the last page fault
5	RW	0x0	mmu_page_fault_is_write The direction of access for last page fault: 0: read 1:write
4	RW	0x1	mmu_replay_buffer_empty The MMU replay buffer is empty.
3	RW	0x1	mmu_idle the MMU is idle when accesses are being translated and there are no unfinished translated access. The MMU_IDLE signal only reports idle when the MMU processor is idle and accesses are active on the external bus. Note: the MMU can be idle in page fault mode.
2	RW	0x0	mmu_stall_active MMU stall mode currently enabled. The mode is enabled by command.
1	RW	0x0	mmu_page_fault_active MMU page fault mode currently enabled.The mode is enabled by command
0	RW	0x0	mmu_paging_enabled mmu paging is enabled

IEP_MMU_CMD
Address: Operational Base + offset (0x0808)
MMU command register

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved

Bit	Attr	Reset Value	Description
2:0	RW	0x0	mmu_cmd 0: MMU_ENABLE_PAGING. enable paging. 1: MMU_DISABLE_PAGING. disable paging. 2: MMU_ENABLE_STALL. turn on stall mode. 3: MMU_DISABLE_STALL. turn off stall mode. 4: MMU_ZAP_CACHE. zap the entire page table cache. 5: MMU_PAGE_FAULT_DONE. leave page fault mode. 6: MMU_FORCE_RESET. reset the mmu. The MMU_ENABLE_STALL command can always be issued. Other commands are ignored unless the MMU is idle or stalled.

IEP_MMU_PAGE_FAULT_ADDR
Address: Operational Base + offset (0x080c)
MMU logic address of last page fault

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_page_fault_addr address of last page fault

IEP_MMU_ZAP_ONE_LINE
Address: Operational Base + offset (0x0810)
MMU zap cache line register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	mmu_zap_one_line address to be invalidated from the page table cache.

IEP_MMU_INT_RAWSTAT
Address: Operational Base + offset (0x0814)
MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	read_bus_error read bus error
0	RW	0x0	page_fault page fault

IEP_MMU_INT_CLEAR
Address: Operational Base + offset (0x0818)
MMU interrupt clear register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	read_bus_error_clear read bus error interrupt clear. write 1 to this register can clear read bus error interrupt.

Bit	Attr	Reset Value	Description
0	RW	0x0	page_fault_clear page fault interrupt clear, write 1 to this register can clear page fault interrupt.

IEP_MMU_INT_MASK
Address: Operational Base + offset (0x081c)
MMU interrupt mask register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	read_bus_error_int_en read bus error interrupt enable
0	RW	0x0	page_fault_int_en page fault interrupt enable

IEP_MMU_INT_STATUS
Address: Operational Base + offset (0x0820)
MMU interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	read_bus_error read bus error interrupt
0	RW	0x0	page_fault page fault interrupt

IEP_MMU_AUTO_GATING
Address: Operational Base + offset (0x0824)
MMU clock auto gating register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x1	mmu_auto_gating mmu clock auto gating when it is 1, the mmu will auto gating itself

4.5 Application Notes

4.5.1 VOP path disabled configure flow

1. Keep IEP direct path disabled.
2. Configure all registers which are needed at any time.
3. Configure IEP_CONFIG_DONE.
4. Configure IEP_FRM_START.

4.5.2 VOP path enabled configure flow

1. Keep IEP direct path enabled.
2. Configure all IEP registers which are needed.
3. Configure VOP related registers which are needed.
4. Configure CONFIG_DONE register in VOP only.
5. Wait for frame start from VOP and IEP direct path.

4.5.3 VOP path turn on flow

1. Configure all IEP registers which are needed.
2. Configure VOP related registers which are needed.
3. Enable IEP direct path.
4. Enable VOP direct path.
5. Configure CONFIG_DONE register in VOP only.
6. Wait for frame start from VOP and IEP direct path.

4.5.4 VOP path turn off flow

1. Disable VOP direct path.
2. Disable IEP direct path, so IEP do not receive any other CONFIG_DONE and frame start from VOP immediately.
3. Configure CONFIG_DONE register in VOP.
4. Wait for frame start from VOP and IEP direct path, so VOP quit direct path mode completely.
5. Configure IEP registers which are needed at any time.
6. Configure IEP_CONFIG_DONE.
7. Configure IEP_FRM_START, IEP is working at write back mode now.

Chapter 5 Multi-format Video Decoder And Encoder

5.1 Overview

The multi-format video codec (referred as codec in the following paragraph) supports three main world-wide advanced video coding standard (H264/VP9/HEVC) with high decoding performance @4K and h264/jpeg encoding.
The codec is connected to the AHB bus through an AHB slave and the AXI bus through an AXI master. The register configuration is fed into the decoder through the AHB slave interface while the large data such as stream data are transacted between DDR and the decoder through the AXI master interface.
In order to improve large data transaction performance, codec embeds MMU (memory management unit) and supports the cacheable bus operation.
The codec supports the following features:

- Supports HEVC decoding
  - Main and Main10 Profile up to Level 5.1 High Tier: 4096x2304@60 fps
  - Supports frame timeout interrupt , frame finish interrupt, bus error interrupt and bitstream error interrupt
  - Supports RLC write mode, RLC mode and Normal Mode
- Supports H264 decoding
  - The following profiles up to Level 5.1 : 4096x2304 @30fps
    - Baseline Profile
    - Main Profile
    - High Profile
    - High 10 profile
    - High 4:2:2 Profile(the MBAFF feature is not supported)
  - Supports frame timeout interrupt, frame finish interrupt and bitstream error interrupt, buffer empty interrupt
  - Supports slice by slice or random size stream decoding
  - Supports error-mode decoding and error info output
  - Supports RLC write mode, RLC mode and Normal Mode
- Supports VP9 decoding
  - Profile 0: 4096x2304 @30fps
  - Supports frame timeout interrupt, frame finish interrupt and bitstream error interrupt
  - Supports RLC mode and Normal Mode
- MMU embedded with MMU interrupt support
- Supports MPEG-4 decoding
  - 60fps at 1920x1088
  - Simple Profile, levels 0-6
  - Advanced Simple Profile, levels 0-5
- MPEG-2/ MPEG-1
  - 60fps at 1920x1088
  - Main Profile, low, medium and high levels
- Supports JPEG decoding
  - 48x48 to 8176x8176(66.8 Mpixels)，Step size 8 pixels
  - Baseline interleaved, and supports ROI (region of image) decode
- Built-in post processor in H.264(1080p) decoder supports
  - Stand-alone mode: rotation, RGB conversion, scaling, dithering
  - Pipe-ling mode:, RGB conversion, scaling, dithering and alpha blending
- Supports encoding of the following standards:
  - H.264: up to HP level 4.1
  - JPEG: Baseline (DCT sequential)
- Built-in pre-processor in common video encoder supports:
  - rotation, YCbCr conversion

5.2 Block Diagram

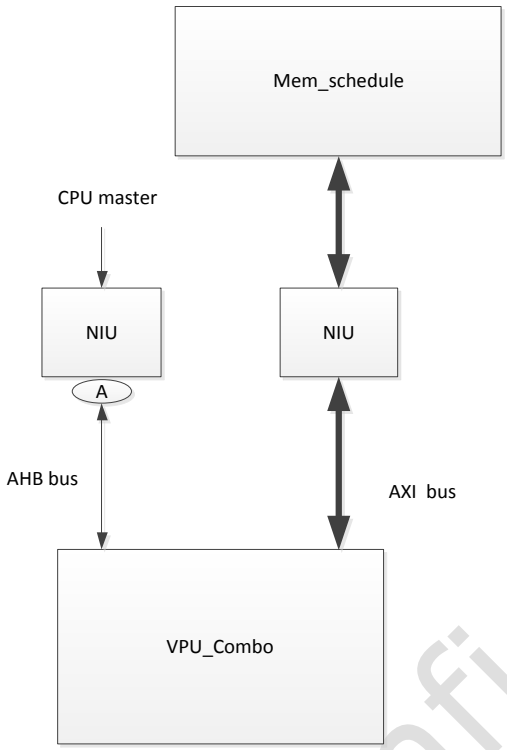


Fig. 5-1 Decoder in SOC

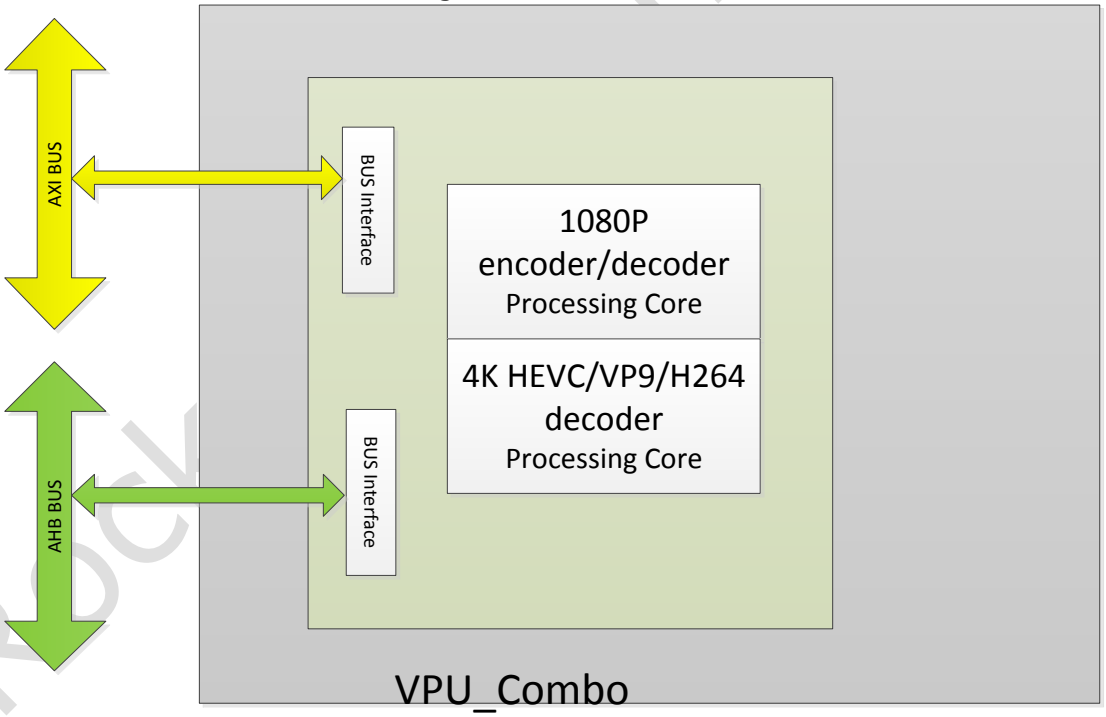


Fig. 5-2 VPU Block Diagram

As shown in the figures above, CPU accesses to the decoder register bank through AHB bus. Bitstream and other necessary data are fed into processing core though AXI read channel, and after several steps of decoding process, decoded pictures and other information data are transferred to designated location in the DDR through AXI write channel.

5.3 Video frame format

This chapter describes different input and output video frame formats supported by VCODEC. Each function module has its own supported video frame formats, and this chapter describes all the video frame formats.

5.3.1 YCbCr 4:2:0 Planar Format

In the planar format, each video sample component forms one memory plane. Within one plane, the data has to be stored linearly and contiguously in the memory as shown in Fig. 5-3. The luminance samples are stored in raster-scan order (Y0Y1 Y2Y3 Y4….). The chrominance samples are stored in two planes also in raster scan order (Cb0Cb1 Cb2Cb3 Cb4…. and Cr0Cr1 Cr2Cr3 Cr4….). In this format each pixel takes 12 bits of memory.

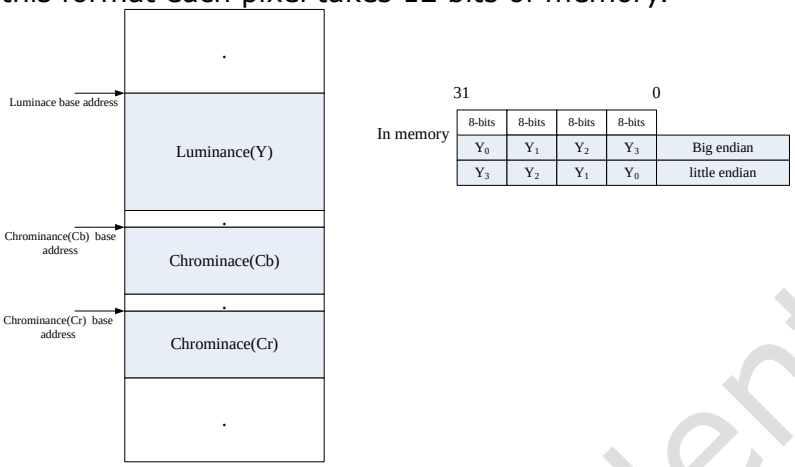


Fig. 5-3 VCODEC YCbCr 4:2:0 planar format

5.3.2 YCbCr 4:2:0 Semi-Planar format

In semi-planar YcbCr4:2:0 format the luminance samples from one plane in memory, and chrominance samples from another. Within one plane, the data has to be stored linearly and contiguously in the memory. The luminance pixels are stored in raster-scan order (Y0Y1 Y2Y3 Y4….). The interleaved chrominance CbCr samples are stored in raster-scan order in memory as Cb0Cr0 Cb1Cr1 Cb2 Cr2 Cb3Cr3 Cb4 Cr4….
Semi-Planar format supports both progressive and interlaced format as presented in Fig. 5-4.The interlaced format may be alternative line or each line.

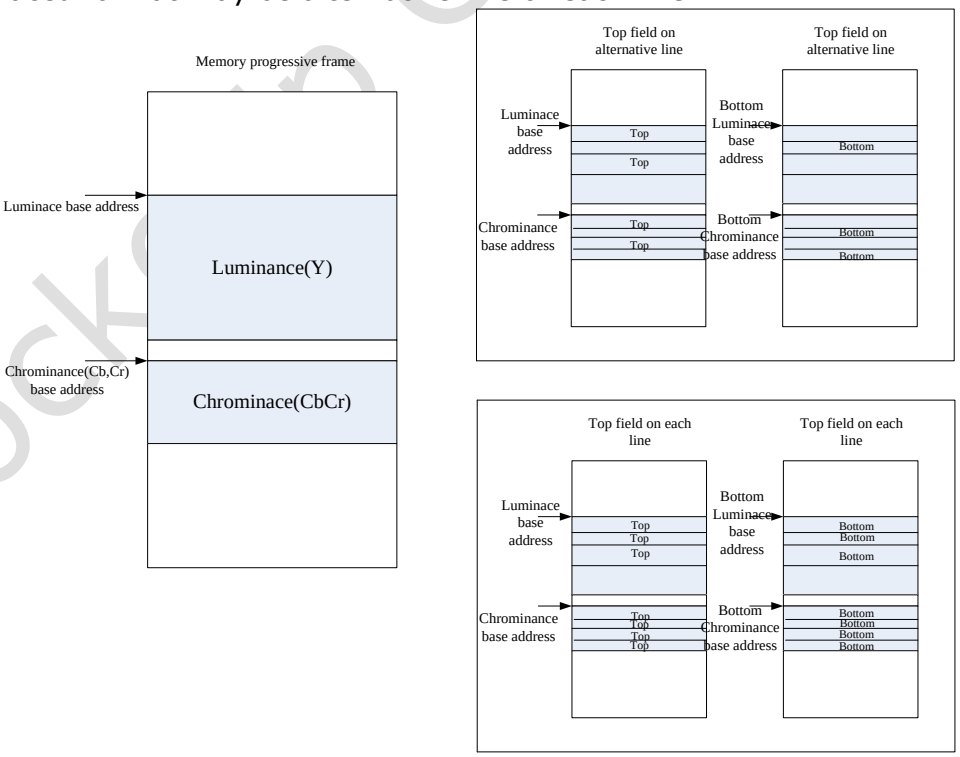


Fig. 5-4 VCODEC YCbCr 4:2:0 Semi-planar format

5.3.3 YCbCr 4:2:0 Tiled Semi-Planar Format

Like the YCbCr 4:2:0 semi-planar format, the tiled semi-planar format is also organized in the

memory on two separate planes. The difference between these formats is that in tiled format the pixel samples are not anymore in raster-scan order but are stored macroblock(16x16 pixels) by macroblock. The samples of each macroblock are stored in consecutive addresses and the macroblocks are ordered from left to right and from top to down as Fig. 5-5. When this format used as input data format, it causes the lowest bus load to the system as there is minimal amount of non-sequential memory addressing required when reading the input data to the post-processor.

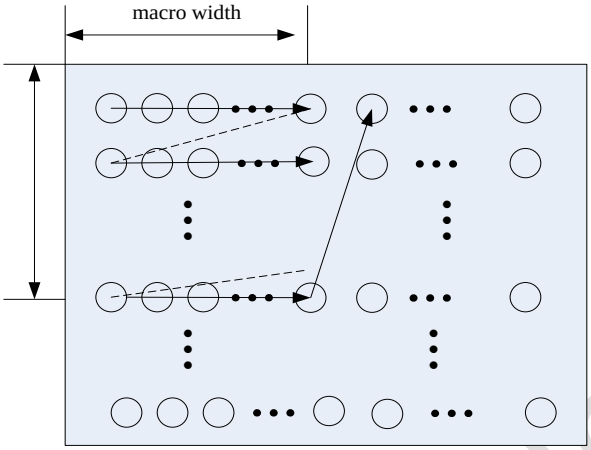


Fig. 5-5 VCODEC Tile scan mode

5.3.4 YCbCr 4:2:2 Interleaved Format

In the interleaved YCbCr 4:2:2 format the pixel samples from a single plane in which the data has to be stored linearly and contiguously as shown in Fig. 5-6. The pixel data is in raster scan order and the chrominance samples are interleaved between the luminance samples as Y0Cb0 Y1Cr0 Y2 Cb1 Y3Cr1 Y4 Cb2…. YCrCb, CbYCrY and CrYCbY component orders are supported also. In this format, each pixel takes 16 bits in the memory.

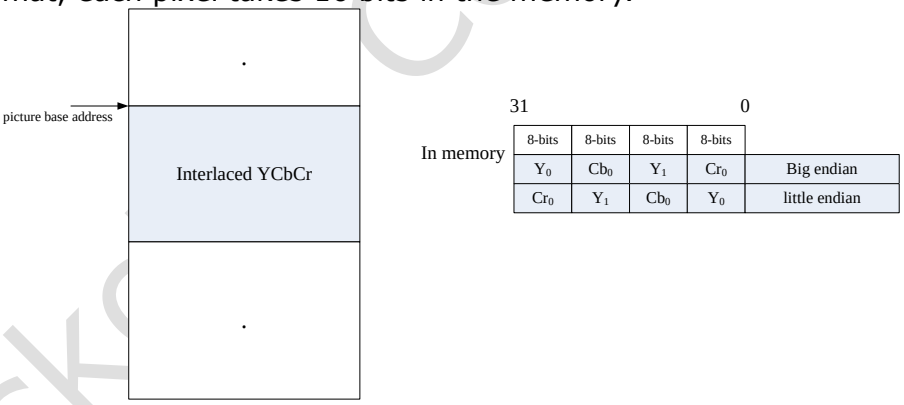


Fig. 5-6 VCODEC YCbCr4:2:2 Interleaved format

5.3.5 AYCbCr 4:4:4 Interleaved Format

In the interleaved YcbCr 4:2:2 format, the pixel samples from a single plane in which the data has to be stored linearly and contiguously as show in Fig. 5-7. The pixel data is in raster scan order and the chrominance and alpha channel samples are interleaved between the luminance samples as A0Y0 Cb0Cr0 A1 Y1 Cb1Cr1….

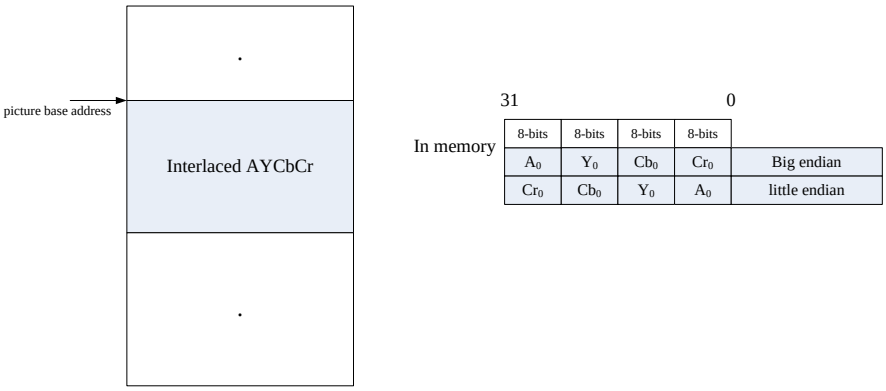


Fig. 5-7 VCODEC AYCbCr 4:4:4 Interleaved format

5.3.6 RGB 16bpp Format

In this format each pixel is represented by 16 or less bits containing the red, blue and green samples. There are several 16bpp formats which use different number of bits for each sample. For example the RGB 5-5-5 format uses 5 bits for each sample and 1 bit is left unused or can represent a transparency flag, where RGB 5-6-5 uses 6 bits for the G sample and 5 bits for R and B samples. Common for all 16bpp types is that two pixels fit into one 32-bit space.

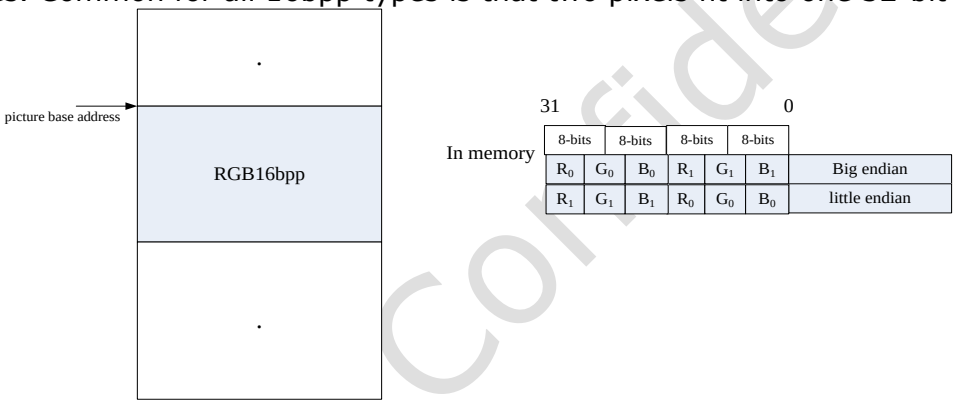


Fig. 5-8 VCODEC RGB 16bpp format

5.3.7 RGB 32bpp Format

Any RGB format that has its pixels represented by more than 16bits each is considered to be of 32bpp type. Typically in this format each pixel is represented by three bytes containing a red, blue and green sample and a 4th byte which can be empty or hold an alpha blending value. Common for all 32bpp types is that only one pixel fit into one 32-bit space. The data has to be stored linearly and contiguously in the memory.

5.4 Function Description

5.4.1 HEVC Standard

High Efficiency Video Coding (HEVC) is a video compression standard, a successor to H.264/MPEG-4 AVC (Advanced Video Coding), that was jointly developed by the ISO/IEC Moving Picture Experts Group (MPEG) and ITU-T Video Coding Experts Group (VCEG) as ISO/IEC 23008-2 MPEG-H Part 2 and ITU-T H.265. MPEG and VCEG established a Joint Collaborative Team on Video Coding (JCT-VC) to develop the HEVC standard.
HEVC was designed to substantially improve coding efficiency compared to H.264/MPEG-4 AVC HP, i.e. to reduce bitrate requirements by half with comparable image quality, at the expense of increased computational complexity. HEVC was designed with the goal of allowing video content to have a data compression ratio of up to 1000:1. Depending on the application requirements HEVC encoders can trade off computational complexity, compression rate, robustness to errors, and encoding delay time.Two of the key features where HEVC was improved compared to H.264/MPEG-4 AVC was support for higher resolution video and improved parallel processing methods.

5.4.2 H264 Standard

H.264 or MPEG-4 Part 10, Advanced Video Coding (MPEG-4 AVC) is a video compression format that is currently one of the most commonly used formats for the recording, compression, and distribution of video content. The final drafting work on the first version of the standard was completed in May 2003, and various extensions of its capabilities have been added in subsequent editions.
H.264/MPEG-4 AVC is a block-oriented motion-compensation-based video compression standard developed by the ITU-T Video Coding Experts Group (VCEG) together with the ISO/IEC JTC1 Moving Picture Experts Group (MPEG). The project partnership effort is known as the Joint Video Team (JVT). The ITU-T H.264 standard and the ISO/IEC MPEG-4 AVC standard (formally, ISO/IEC 14496-10 – MPEG-4 Part 10, Advanced Video Coding) are jointly maintained so that they have identical technical content.

5.4.3 VP9 Standard

VP9 is an open and royalty free video coding format being developed by Google. VP9 is a successor to VP8. Chromium, Chrome, Firefox, and Opera support playing VP9 video format in the HTML5 video tag. Development of VP9 started in Q3 2011. One of the goals for VP9 is to reduce the bit rate by 50% compared to VP8 while having the same video quality. Another goal for VP9 is to improve it to the point where it would have better compression efficiency than High Efficiency Video Coding.

5.4.4 MMU

The MMU divides memory into 4KB pages, where each page can be individually configured. For each page the following parameters are specified:

- Address translation of virtual memory, this enables the processor to work using address that differ from the physical address in the memory system.
- The permitted types of accesses to that page. Each page can permit read, write, both, or none.

The MMU use 2-level page table structure:
1. The first level, the page directory consists of 1024 directory table entries(DTEs), each pointing to a page table.
2. The second level, the page table consists of 1024 page table entries(PTEs), each pointing to a page in memory.

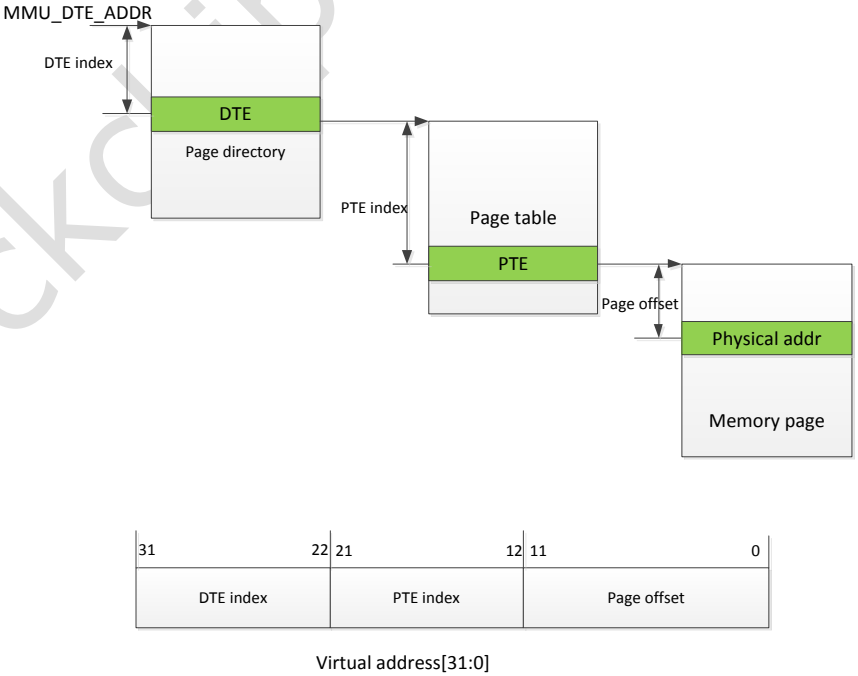


Fig. 5-9 structure of two-level page table

5.4.5 HEVC Working Mode

There are there working modes to be selected for HEVC decoder: RLC Mode, RLC Write Mode, and Normal Mode.

The key differences among three working modes are whether CABAC module and Post-CABAC module are involved into the hardware decoding process.
For RLC mode, CABAC are bypassed and the input bitstream to the Post-CABAC module should be already decoded.
For RLC write mode, the decoded results by CABAC are output to the DDR, and the following decoding processes are stopped.
As for the normal mode, all the modules are involved into the decoding process, and complete decoding results are output. Normally, this mode should be selected.

5.4.6 H264 Working Mode

There are there working modes which can be chosen when decoding HEVC: RLC Mode, RLC Write Mode, and Normal Mode.
The key differences among three working modes are whether stream-parse module and post-stream-parse modules are involved into the hardware decoding process.
For RLC mode, stream-parse module is bypassed and the input data to the Post-CABAC module should be already parsed which can be recognized by the post-stream-parse modules.
For RLC write mode, the parsed results by stream-parse module are output to the DDR, and the following decoding processes are stopped.
As for the normal mode, all the modules are involved into the decoding process, and complete decoding results are output. Normally, this mode should be selected.

5.4.7 VP9 Working Mode

There are two working modes to be selected for VP9 decoder: RLC Mode, Normal Mode.
The key differences among these two working modes are whether strmd module is involved into the hardware decoding process.
For RLC mode, strmd is bypassed and the input dec_ctrl cmd and inter cmd to the Post-strmd module should be already decoded. The dec_ctrl cmd should be put on the address swreg4_strm_rlc_base while the inter cmd should be put on the address swreg34_vp9_intercmd_base.
As for the normal mode, all the modules are involved into the decoding process, and complete decoding results are output. Normally, this mode should be selected.

5.4.8 Input Data Format for HEVC

When the decoder works in RLC mode, the parsed stream info (which can be called dec_ctrl commands) must be needed, which should be 128bit aligned.
When the decoder works in normal mode or RLC write mode, the bitstream, tbl ,pps and rps are needed for decoding.
1. bitstream
The bitstream must be 128bit align.
2. hevc table
hevc table is used for hevc context initialization, and it contains 156 units of 160-byte data.
3. hevc pps
Hevc pps contains 64 units of 80-byte data.

Table 5-1 sps format

video_parameter_set_id	4bit
seq_parameter_set_id	4bit
chroma_format_idc	2bit
pic_width_in_luma_samples	13bit
pic_height_in_luma_samples	13bit
bit_depth_luma	4bit
bit_depth_chroma	4bit
log2_max_pic_order_cnt_lsb	5bit
log2_diff_max_min_luma_coding_block_size	3bit
log2_min_luma_coding_block_size	3bit
log2_min_transform_block_size	3bit

log2_diff_max_min_transform_block_size	2bit
max_transform_hierarchy_depth_inter	3bit
max_transform_hierarchy_depth_intra	3bit
scaling_list_enabled_flag	1bit
amp_enabled_flag	1bit
sample_adaptive_offset_enabled_flag	1bit
pcm_enabled_flag	1bit
pcm_sample_bit_depth_luma	4bit
pcm_sample_bit_depth_chroma	4bit
pcm_loop_filter_disabled_flag	1bit
log2_diff_max_min_pcm_luma_coding_block_size	3bit
log2_min_pcm_luma_coding_block_size	3bit
num_short_term_ref_pic_sets	7bit
long_term_ref_pics_present_flag	1bit
num_long_term_ref_pics_sps	6bit
sps_temporal_mvp_enabled_flag	1bit
strong_intra_smoothing_enabled_flag	1bit
Transform_skip_rotation_enabled_flag	1bit
Transform_skip_context_enabled_flag	1bit
intra_block_copy_enabled_flag	1bit
residual_dpcm_intra_enabled_flag	1bit
residual_dpcm_inter_enabled_flag	1bit
extended_precision_processing_flag	1bit
intra_smoothing_disabled_flag	1bit
Reserved	32bit

Table 5-2 pps format

pps_pic_parameter_set_id	6bit
pps_seq_parameter_set_id	4bit
dependent_slice_segments_enabled_flag	1bit
output_flag_present_flag	1bit
num_extra_slice_header_bits	3bit//?
sign_data_hiding_flag	1bit
cabac_init_present_flag	1bit
num_ref_idx_l0_default_active	4bit
num_ref_idx_l1_default_active	4bit
init_qp_minus26	6bit
constrained_intra_pred_flag	1bit
transform_skip_enabled_flag	1bit
cu_qp_delta_enabled_flag	1bit
Log2MinCuQpDeltaSize	3bit
pps_cb_qp_offset	5bit
pps_cr_qp_offset	5bit
pps_slice_chroma_qp_offsets_present_flag	1bit
weighted_pred_flag	1bit
weighted_bipred_flag	1bit
transquant_bypass_enabled_flag	1bit

tiles_enabled_flag	1bit
entropy_coding_sync_enabled_flag	1bit
pps_loop_filter_across_slices_enabled_flag	1bit
loop_filter_across_tiles_enabled_flag	1bit
deblocking_filter_override_enabled_flag	1bit
pps_deblocking_filter_disabled_flag	1bit
pps_beta_offset_div2	4bit
pps_tc_offset_div2	4bit
lists_modification_present_flag	1bit
log2_parallel_merge_level	3bit
slice_segment_header_extension_present_flag	1bit
log2_transform_skip_max_size_minus2	3bit
If(tiles_enable_flag) {	
num_tile_columns	5bit
num_tile_rows	5bit
column_width[20]	8 * 20bits
column_height[22]	8 * 22 bit
}	
Scaleing_address	32bit

4. HEVC rps
HEVC rps contains a number of slice data composed by 2 units of 32-byte data.

5.4.9 Input Data for H264

When in RLC mode, dec_ctrl cmds are needed, and they all should be 128bit aligned.
When in normal mode or direct write mode, bitstream, tbl ,pps and rps are need, which should be 128bit aligned.
1. bitstream
The bitstream data should be put on the address, which are set as swreg4_strm_rlc_base.
The bitstream data should be 128bit aligned, and there are three modes to fetch bitstream: frame by frame, slice by slice, and random.
For frame by frame mode, swreg2_sysctrl[25] must be configured as 1'b0,and swreg2_sysctrl[28] must be configured as 1'b0. The bitstream of whole frame must be send to the decoder completely.
For slice by slice mode, swreg2_sysctrl[25] must be configured as 1'b0, swreg2_sysctrl[28] must be configured as 1'b1, and swreg1_int[6] must be configured as 1'b1. The bitstream will be split into one or more slices. When swreg1_int[16] is 1,we must send the next slice pack to the decoder, and then configure swreg1_int[10] as 1'b1. Repeat step mention above until the whole slice pack is sent completely.
For random mode, swreg2_sysctrl[25] must be configured as 1'b1, and swreg1_int[6] must be configured as 1'b1. The bitstream will be split into random pack .when swreg1_int[16] is 1,we must send the next pack to the decoder, and then configure swreg1_int[10] as 1'b1. Repeat the operation until the whole pack is sent completely. When sending a packet at the end of the bitstream, we must configure config[26] as 1'b1.
2. H264 table
H264 table is used for h264 context initialization. It contains four parts, and each part is 128bit align.

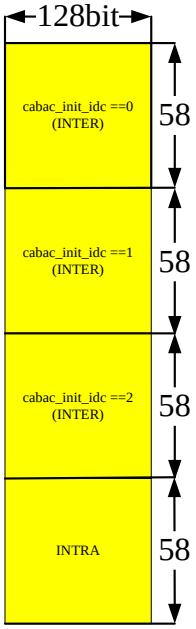


Fig. 5-10 h264 table

3. h264 pps
There are 256 units of 256bit data.

Table 5-3 pps format

seq_parameter_set_id	4bit
profile_idc	8bit
constraint_set3_flag	1bit
chroma_format_idc	2bit
bit_depth_luma_minus	3bit
bit_depth_chroma_minus	3bit
qpprime_y_zero_transform_bypass_flag	1bit
log2_max_frame_num_minus4	4bit
max_num_ref_frames	4bit
pic_order_cnt_type	2bit
log2_max_pic_order_cnt_lsb_minus4	4bit
delta_pic_order_always_zero_flag	1bit
pic_width_in_mbs	9bit
pic_height_in_mbs	9bit
frame_mbs_only_flag	1bit
mb_adaptive_frame_field_flag	1bit
direct_8x8_inference_flag	1bit
mvc_extension_enable	1bit
num_views	2bit
view_id[0]	10bit
view_id[1]	10bit
num_anchor_refs_l0	1bit
anchor_ref_l0	10bit
num_anchor_refs_l1	1bit
anchor_ref_l1	10bit
num_non_anchor_refs_l0	1bit
non_anchor_ref_l0	10bit

num_non_anchor_refs_l1	1bit
non_anchor_ref_l1	10bit
Align(128)	3bit
pps_pic_parameter_set_id	8bit
pps_seq_parameter_set_id	5bit
entropy_coding_mode_flag	1bit
bottom_field_pic_order_in_frame_present_flag	1bit
num_ref_idx_l0_default_active_minus1	5bit
num_ref_idx_l1_default_active_minus1	5bit
weighted_pred_flag	1bit
weighted_bipred_idc	2bit
pic_init_qp_minus26	7bit
pic_init_qs_minus26	6bit
chroma_qp_index_offset	5bit
deblocking_filter_control_present_flag	1bit
constrained_intra_pred_flag	1bit
redundant_pic_cnt_present_flag	1bit
transform_8x8_mode_flag	1bit
second_chroma_qp_index_offset	5bit
Scaling_list_enable_flag	1bit
Scaleing_list_address	32bit
Is_long_term[16]	16bit
Voidx	16bit
Align(128)	8bit

4. h264 rps

The data should be 128bit aligned, and there are two modes to reorder ref pic: software and hardware.

For hardware mode, swreg2_sysctrl[24] must be configured as 1'b1, and there is 8 data (the unit is 128bit) for rps initialization in one frame. For software mode, swreg2_sysctrl[24] must be configured as 1'b0, there is 3 data(the unit is 128bit) in one slice, So a frame including the slices number multiplied by 3 the amount of data.

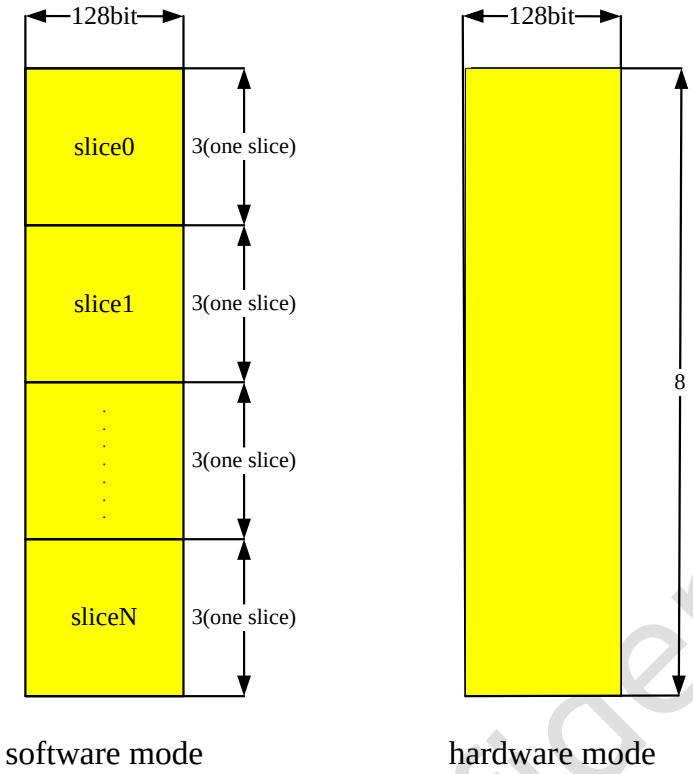


Fig. 5-11 h264 rps data format

For software mode,Each Specific data are listed in the following table:

Table 5-4 software rps format

for(j = 0; j < 2; j++)	
{	
for(i = 0; i < 32; i++)	
{	
dbp_idx[m][j][i]	5bit
bottom_flag[m][j][i]	1bit
View_id	1bit
}	
}	
Align(128)	

For hardware mode, Each Specific data are listed in the following table:

Table 5-5 hardware rps format

Framenum_wrap	256bit
No used	16bit
No used	16bit
for(j = 0; j <3; j++)	list p,list b0,listb1
{	
for(i = 0; i < 32; i++)	
{	
dbp_idx[j][i]	5bit
bottom_flag[j][i]	1bit
view_id[j][i]	1bit
}	
}	

Align(128)	

5.4.10 Input Data for VP9

When in RLC mode, two data inputs are needed, which are dec_ctrl cmd and inter cmd, and they all should be 128bit aligned.
When in normal mode, three data inputs are needed, which are bitstream, prob and segid from last frame.
1. vp9 prob data format:
For intra_only frame, there are 149 units of 128bit data; for inter frame, there are 153 units of 128bit data.

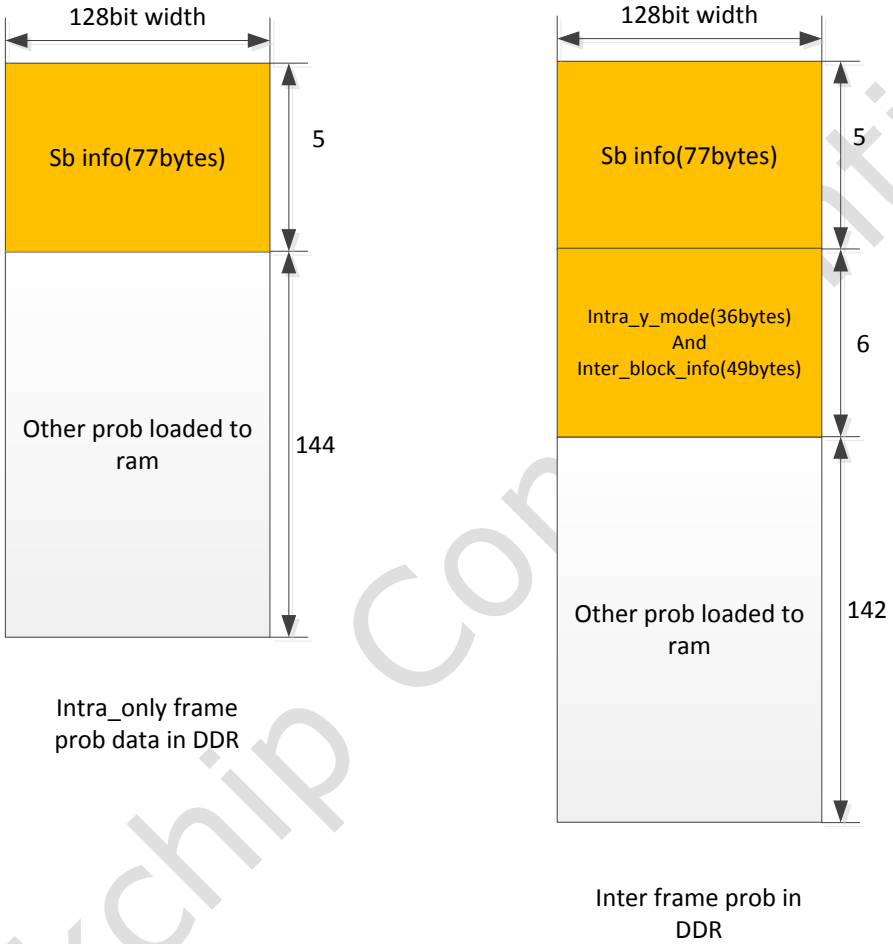
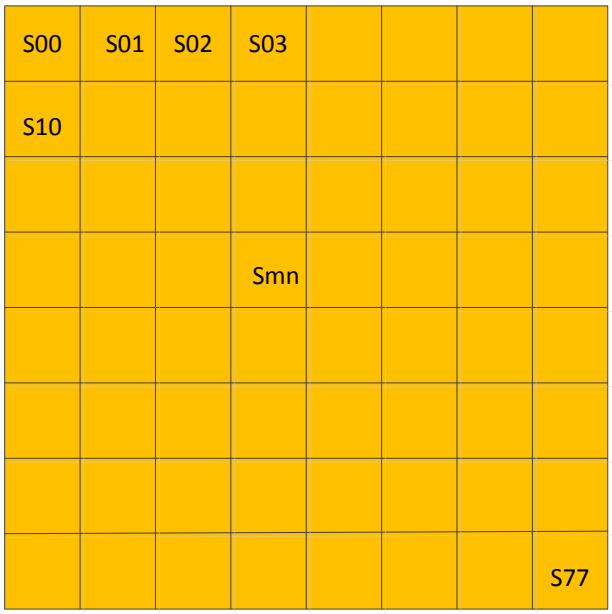


Fig. 5-12 vp9 prob data format

2. the format of segid from last frame data format
The segid data is store with CTU raster scan mode, every CTU contain two 128bits. In the CTU, every 8x8 block has a segid data (Smn) which is 4 bits.



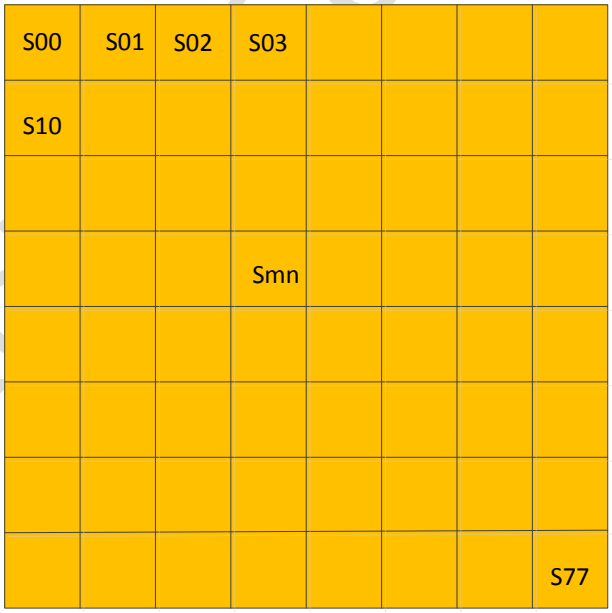
Segid data format in
a CTU

Fig. 5-13 vp9 segid data format

5.4.11 Output Data Format

1. Decoded frame data format

The decoded frame data are stored in the location with raster scan order where designated in the register configuration. Y component of the video data are stored first, and then UV component of the video data are stored.



Segid data format in
a CTU

Fig. 5-14 Data format in the DDR of Dec_out_base vp9

2. COLMV data

COLMV data, which are needed for inter prediction , are in the DDR space following the YUV data.

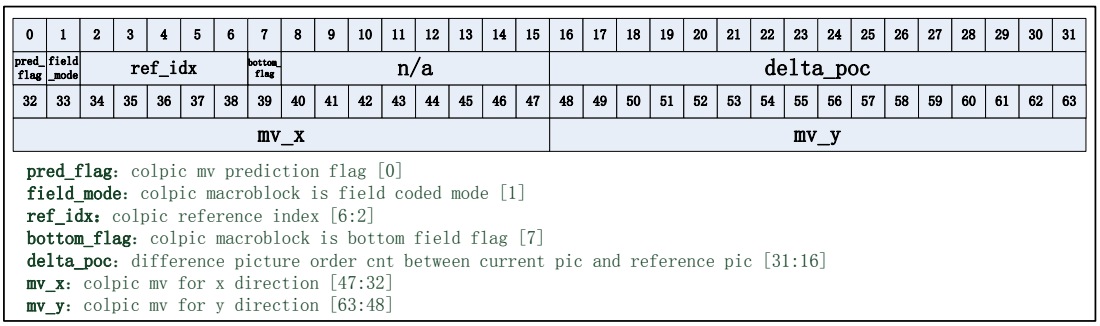


Fig. 5-15 H264 colmv output format

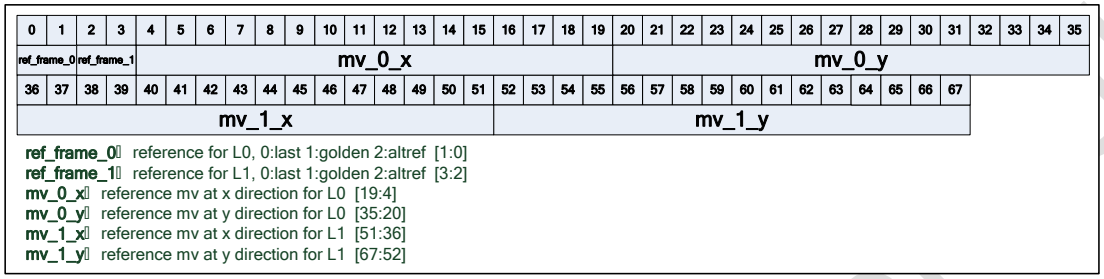


Fig. 5-16 VP9 colmv output format

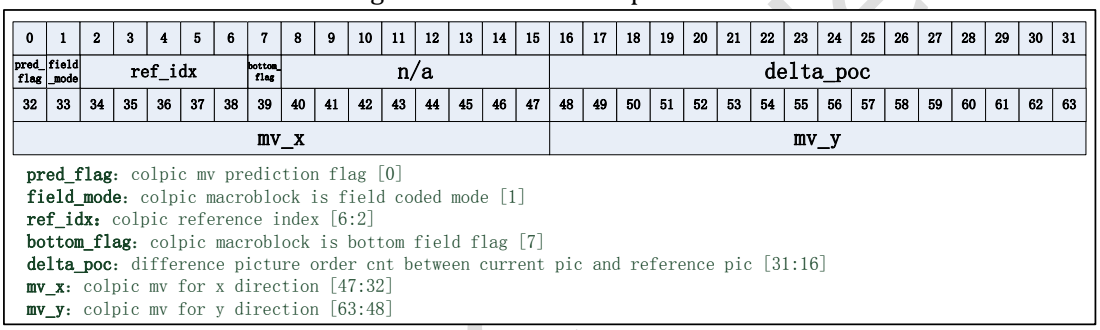


Fig. 5-17 HEVC colmv output format

3. Only for VP9
(1) Cur segid output:
The cur segid output data format is the same with segid from last frame.
(2) Cur count output:
For intra only frame, there are 98 words for no coeff count and 1440 words for coeff count.
For inter frame, there are 426 words for no coeff count and 2880 words for coeff count.
For every count, its real valid bits are 24, but it used 32bits in the DDR.
Segid data are output only when the decoder is decoding VP9.

5.4.12 H264 Error Process

For h264, it has two types of error. One is the normal error, and the other one is the a logic error. Whether it is a normal error or a logic error, the swreg76_h264_errorinfo_num[13:0] will record the number of slices in frame, swreg76_h264_errorinfo_num[15] will be set to 1,and swreg76_h264_errorinfo_num[29:16] will record the number of error slices in frame.
1. normal error
For the normal error, it is recorded by the detection of syntax that is beyond the scope. When swreg1_int[19] is configured as 1'd1, the hardware will wait the end signal of deblocking and then reset itself. And for normal error, the error info will be put on the address swreg4_strm_rlc_base. Specific data are listed in the following table:

Table 5-6 error info format

start_ctu_address	16bit	When it is inter error,it is error ctu assr,or it is the first ctu of current slice.
end_ctu_address	16bit	The last ctu of the current slice
error_type	16bit	When error_type[8] is equal to 1,it means that the slice is wrong.

		the error_type[7:0] see the 3-2 table
slice_byte_offset	24bit	The first byte of current slice in the bitstream

When The corresponding register shown in the following table is configured as 1'b0,it will not detect The corresponding error.

Table 5-7 normal error table

error_type	Syntax	enable
0	start_mb_nr(syntax)	swreg44_strmd_error_en[0]
1	slice_type	swreg44_strmd_error_en[1]
2	pic_parameter_set_id	swreg44_strmd_error_en[2]
3	Framenum	swreg44_strmd_error_en[3]
4	idr_pic_id	swreg44_strmd_error_en[4]
5	delta_pic_order_cnt_bottom	swreg44_strmd_error_en[5]
6	delta_pic_order_cnt	swreg44_strmd_error_en[6]
7	num_ref_idx_lx_active_minus1	swreg44_strmd_error_en[7]
8	Cabac_init_idc	swreg44_strmd_error_en[8]
9	Slice_qp_delta	swreg44_strmd_error_en[9]
10	disable_deblocking_filter_idc	swreg44_strmd_error_en[10]
11	slice_alpha_c0&beta_offset_div2	swreg44_strmd_error_en[11]
12	modification_of_pic_nums_idc	swreg44_strmd_error_en[12]
13	modification_of_pic_num	swreg44_strmd_error_en[13]
14	abs_diff_pic_num_minus1	swreg44_strmd_error_en[14]
15	abs_diff_pic_num_nonexist	swreg44_strmd_error_en[15]
16	long_term_pic_num	swreg44_strmd_error_en[16]
17	long_term_pic_num_nonexist	swreg44_strmd_error_en[17]
18	abs_diff_view_idx_minus1	swreg44_strmd_error_en[18]
19	memory_management_control_operation	swreg44_strmd_error_en[19]
20	difference_of_pic_nums_minus1	swreg44_strmd_error_en[20]
21	long_term_frame_idx	swreg44_strmd_error_en[21]
22	max_long_term_frame_idx_plus1	swreg44_strmd_error_en[22]
23	log2_weight_denom	swreg44_strmd_error_en[23]

error_type	Syntax	enable
24	pred_weight_offset	swreg44_strmd_error_en[24]
25	View_id	swreg44_strmd_error_en[25]
26	Skip_run	swreg77_h264_error_e[13]
27	Mb_type	swreg77_h264_error_e[14]
28	Coded_block_pattern	swreg77_h264_error_e[15]
29	Mb_qp_delta	swreg77_h264_error_e[16]
30	Ref_idx_lX	swreg77_h264_error_e[17]
31	Mvd_x	swreg77_h264_error_e[18]
32	Mvd_y	swreg77_h264_error_e[19]
33	Sub_mb_type	swreg77_h264_error_e[20]
34	Coeff_token	swreg77_h264_error_e[21]
35	Level_prefix	swreg77_h264_error_e[22]
36	Total_zero	swreg77_h264_error_e[23]
37	Run_before	swreg77_h264_error_e[24]
38	Coeff_abs_level_minus1	swreg77_h264_error_e[25]
39	Reserved	swreg77_h264_error_e[26]
40	Data_runout	swreg77_h264_error_e[28]
255	Inter error	

For normal error except inter error, When swreg1_int[19] is configured as 1'd0, the hardware will stop the decoder and reset itself.And the error_type in the table 3-2 will put on the sw_strmd_error_status[27:0],the current ctu_x will put on the swreg46_strmd_error_ctu[7:0], the current ctu_x will put on the swreg46_strmd_error_ctu[15:8]. The Inter error be put on the address swreg4_strm_rlc_base any ways.

2. logic error

For logic error, it is recorded by the detection of different slice of syntax elements that are the same.

When swreg1_int[19] is configured as 1'd1, when there is any stream error, the hardware will wait the end signal of deblocking and then reset itself. And the error_type in the table 3-3 will put on the sw_strmd_error_status[27:0],the current ctu_x will put on the swreg46_strmd_error_ctu[7:0], the current ctu_x will put on the swreg46_strmd_error_ctu[15:8].

Table 5-8 logic error table

Error_type	syntax	enable
43	Delta_pic_order_cnt	swreg44_strmd_error_en[27]
44	Delta_pic_order_cnt_bottom	swreg44_strmd_error_en[28]
45	Pic_order_cnt_lsb	swreg44_strmd_error_en[29]
46	idr_pic_id	swreg44_strmd_error_en[30]

Error_type	syntax	enable
47	Bottom_field_flag	swreg44_strmd_error_en[31]
48	Field_pic_flag	swreg77_h264_error_e[0]
49	Frame_num	swreg77_h264_error_e[1]
50	pps_id_logic	swreg77_h264_error_e[2]
51	Slice_type_logic	swreg77_h264_error_e[3]
52	First_mb_in_slice_logic	swreg77_h264_error_e[4]
53	Nal_ref_idc_logic	swreg77_h264_error_e[5]
54	Idr_flag_logic	swreg77_h264_error_e[6]
55	Inter_view_flag_logic	swreg77_h264_error_e[7]
56	Anchor_pic_flag_logic	swreg77_h264_error_e[8]
57	View_id_logic	swreg77_h264_error_e[9]

For logic error, When swreg1_int[19] is configured as 1'd0, the hardware will stop the decoder and reset itself.And the error_type shown above will put on the sw_strmd_error_status[27:0],the current ctu_x will put on the swreg46_strmd_error_ctu[7:0], the current ctu_x will put on the swreg46_strmd_error_ctu[15:8].

5.4.13 HEVC Error Process

For hevc, it has only one types of error. When an error is detected, the hardware will stop the decoder and reset itself. And the error_type in the table 3-3 will put on the sw_strmd_error_status[27:0],the current ctu_x will put on the swreg46_strmd_error_ctu[7:0], the current ctu_x will put on the swreg46_strmd_error_ctu[15:8].

5.4.14 MPEG-4 decoder

The features that video decoder supports about MPEG-4/H.263 shows as below.

Table 5-9 MPEG-4/H.263 feature

Feature	Decoder support
Input data format	MPEG-4/H.263 elementary video stream
Decoding scheme	Frame by frame(or field by field) Video packet by video packet
Output data format	YCbCr 4:2:0 semi-planar
Supported image size	48x48 to 1920x1088(MPEG-4, Sorenson Spark) 48x48 to 720x576(H.263) Step size 16 pixels
Maximum frame rate	60fps at 1920x1088
Maximum bit rate	As specified by MPEG-4 ASP level5
Error detection and concealment	Supported

The decoder of MPEG-4/H.263 has two operating modes: in the primary mode the HW performs entropy decoding, and in the secondary mode SW performs entropy decoding. Secondary mode is used in MPEG-4 data partitioned stream decoding.

5.4.15 MPEG-2/MPEG-1 decoder

The features of MPEG-2/MPEG-1 supported by decoder are shown as Table 5-10.

Table 5-10 MPEG-2/MPEG-1 features

Feature	Decoder support
Input data format	MPEG-2/MPEG-1 elementary video stream

Feature	Decoder support
Decoding scheme	Frame by frame(or field by field) Video packet by video packet
Output data format	YCbCr 4:2:0 semi-planar
Supported image size	48x48 to 1920x1088 Step size 16 pixels
Maximum frame rate	60fps at 1920x1088
Maximum bit rate	As specified by MPEG-2 MP high level
Error detection and concealment	Supported

The dataflow of MPEG-2/MPEG-1 is the same of H.264 HW performs entropy decoding as abover table showing

5.4.16 VC-1 decoder

The features of VC-1 supported by decoder are shown as Table 5-11.

Table 5-11 VC-1 features

Feature	Decoder support
Input data format	VC-1
Decoding scheme	Frame by frame(or field by field) Slice by slice
Output data format	YCbCr 4:2:0 semi-planar
Supported image size	48x48 to 1920x1088 Step size 16 pixels
Maximum frame rate	30fps at 1920x1088
Maximum bit rate	As specified by VC-1 AP level3
Error detection and concealment	Supported

The VC-1 decoder has only one operating mode in which the HW performs entropy decoding.

5.4.17 JPEG Decoder

JPEG features supported by decoder are as shown in Table 5-12.

Table 5-12 JPEG features

Feature	Decoder support
Input data format	JFIF file format 1.02 YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar
Decoding scheme	Input: buffer by buffer, from 5Kb to 8MB at a time① Output: from 1 MB row to 16 Mpixels at a time②
Output data format	YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar
Supported image size	48x48 to 8176x8176(66.8 Mpixels) Step size 8 pixels③
Maximum frame rate	Up to 76 million pixels pre second
Maximum bit rate	As specified by the Divx specification
Thumbnail decoding	JPEG compressed thumbnails supported
Error detection	Supported

①Programmable buffer size for optimizing performance and memory consumption. Interrupt will be issued when buffer runs empty, and the control software will load more streams to external memory.

②Programmable output slice for optimizing performance and memory consumption. Interrupt will be issued when the requested area decoded. The control software can be used to switch the decoder output address each time.
③Non-16x16 dividable resolutions will be filled to 16 pixel boundary.

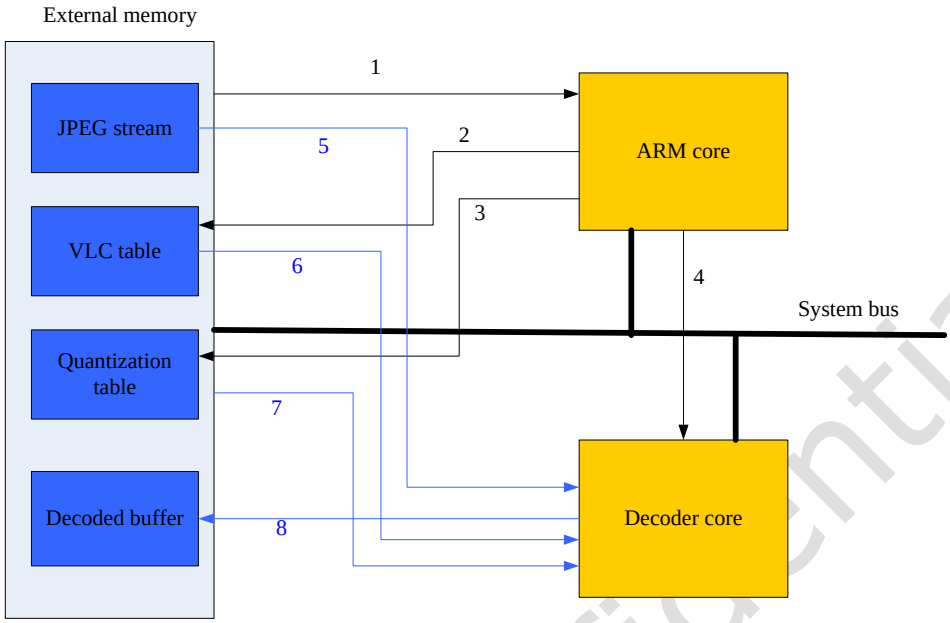


Fig. 5-18 The dataflow of JPEG decoder

The data flow of jpeg decoder is as Fig. 5-18 shown. The decoder software starts decoding the picture by parsing the stream headers (1) and then writes the following items to external memory:
VLC tables (2)
Quantization tables (3)
Last step for the software is to write the hardware control registers and to enable the hardware (4). After starting hardware, SW waits interrupt from HW.
Hardware decodes the picture by reading stream (5), VLC (6) and QP (7) tables. Hardware writes the decoded output picture memory one macroblock at a time (8). When the picture has been fully decoded, or the hardware has run out of stream data, it gives an interrupt with a proper status flag and provides stream end address for software to continue and returns to initial state.

5.4.18 Image Post-processor

The features supported by Post-processor are as show in Table 5-13.

Table 5-13 Post-processor features

Feature	Post-processor support
Input data format	Any format generated by the decoder in combined mode YCbCr 4:2:0 semi-planar YCbCr 4:2:0 planar YCbYCr 4:2:2 YCrYCb 4:2:2 CbYCrY 4:2:2 CrYCbY 4:2:2
Post-processor scheme	Frame by frame. Post-processor handles the image macroblock by macroblock, also in standalone mode.
Input image source	Internal source(combined mode) External source(standalone mode): e.g. a software decoder or camera interface
Output data format	YCbCr 4:2:0 semi-planar YCbCr 4:2:2

Feature	Post-processor support
	YCrYCb 4:2:2 CbYCrY 4:2:2 CrYCbY 4:2:2 Fully configurable ARGB channel lengths and locations inside 32 bits, e.g. ARGB 32-bit (8-8-8-8), RGB 16-bit(5-6-5), ARGB 16-ibt(4-4-4-4).
Input image size (combined mode)	48x48 to 8176x8176(66.8 Mpixels) Step size 16 pixels
Input image size (stand-alone mode)	Width from 48 to 8176 Height from 48 to 8176 Maximum size limited to 16.7 Mpixels Step size 16 pixels
Output image size	16x16 to 1920x1088 Horizontal step size 8 Vertical step size 2
Image up-scaling①	Bicubic polynomial interpolation with a four-tap horizontal kernel and a two-tap vertical kernel Arbitrary, non-integer scaling ratio, separately for both dimensions. Maximum output width is 3x the input width(within the maximum output image size limit) Maximum output height is 3x the input height -2 pixels (within the maximum output image size limit) Maximum output height is 2.5x the input height – 2 pixels (within the maximum output image size limit) when running RealVideo, VP8 format in pipeline
Image down-scaling①	Proprietary averaging filter Arbitrary, non-integer scaling ratio separately for both dimensions Unlimited down-scaling ratio
YCbCr to RGB color conversion	BT.601-5 compliant BT.709 compliant User definable conversion coefficient
Dithering	2x2 ordered spatial dithering for 4,5 and 6 bit RGB channel precision
Programmable alpha channel	Constant eight bit value can be set to the alpha channel of the 24-bit RGB output data to control the transparency of the output picture. The resulting 32-bit ARGB data can be used as input data for later alpha blending.
Alpha blending	Output image can be alpha blended with two rectangular areas. YCbCr semi-planar 4:2:0 PP output format is not supported when performing alpha blending. The supported overlay input formats are following. 8 bit alpha value + YCbCr 4:4:4, big endian channel order being A-Y-Cb-Cr, 8 bits each. 8 bit alpha value + 24 bit RGB, big endian channel order being

Feature	Post-processor support
	A-R-G-B, 8 bits each
Deinterlacing	Conditional spatial deinterlace filtering. Supports only YCbCr 4:2:0 input format. Usable in stand-alone post-processing mode only.
RGB image contrast adjustment	Segmented linear
RGB image brightness adjustment	Linear
RGB image color saturation adjustment	Linear
De-blocking filter for MPEG-4 simple profile /H.263 /Sorenson	Using a modified H.264 in-loop filter as a post-processing filter. Filtering has to be performed in combined mode
Image cropping / digital zoom	User definable start position, height and width. Can be used with scaling to perform digital zoom. Usable only for JPEG or stand-alone mode.
Picture in picture	Output image can be written to any location inside video memory. Up to 1920x1088 sized displays supported.
Output image masking	Output image writing can be prevented on two rectangular areas in the image. The masking feature is exclusive with alpha blending; however it is possible to have one masking area and one blending area.
Image rotation	Rotation 90,180, or 270 degrees Horizontal flip Vertical flip

①It is not allowed to perform horizontal up-scaling and vertical down-scaling (or vice versa) at the same. If needed, this kind of operation can be performed in two phases.
The PP has two modes: standalone mode and pipe-line mode. In standalone mode, picture processing is performed to any external source. The processing is done independently and asynchronously from the video decoder. The dataflow block gram is as Fig. 5-19 shows.

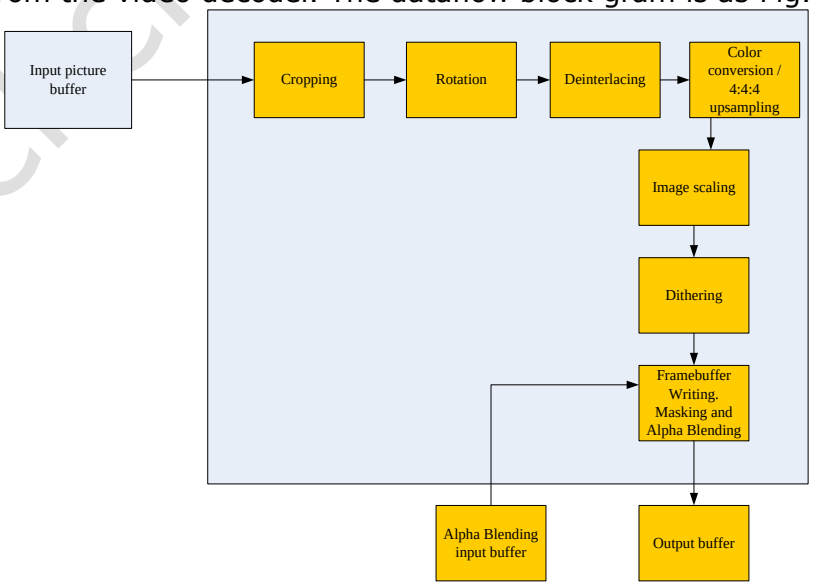


Fig. 5-19 Post-process standalone dataflow

In pipe-line mode, the post-processor works together with the multi-format decoder. The PP will take its input directly from the decoder. The post-processor doesn't have cropping function

in pipe-line mode other than combined with jpeg decoder. The dataflow is as Fig. 5-20 show. In the pipe-line mode, most decoder will also put the data to the decoder out buffer other than JPEG decoder. So, JPEG decoder with pipe-line mode will save bus bandwidth when it crops the input picture to a smaller picture.

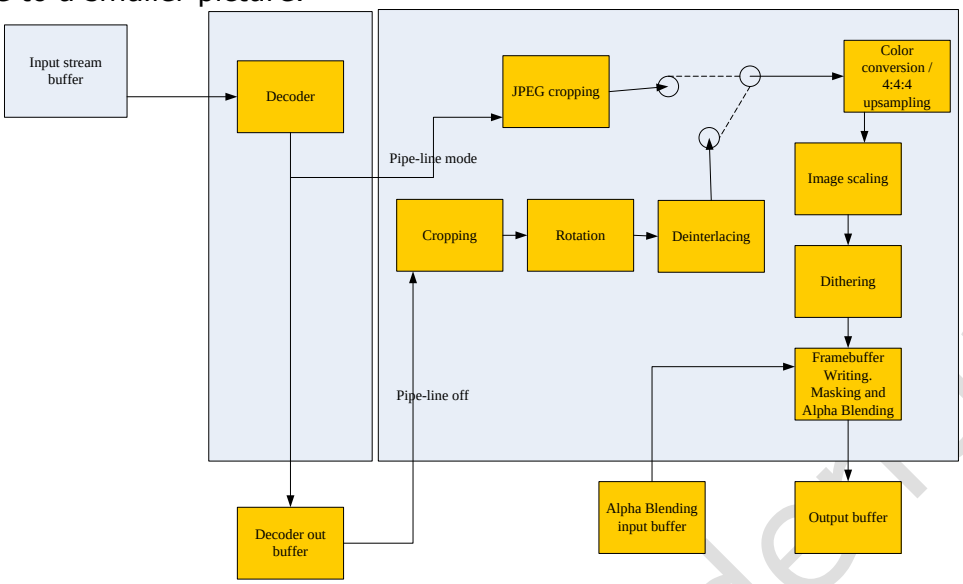


Fig. 5-20 Post-process Pipe-line Mode Dataflow

The post-processor has some restrictions in the input and output picture size. Table 5-14 presents the divisibility requirements for all the post-processor parameters.

Table 5-14 Requirements for post-processor

Output format / parameters	YCbCr 4:2:0	YCbCr 4:2:2	RGB16bpp	RGB32bpp
Input picture width and height	16	16	16	16
Cropped picture width and height	8	8	8	8
Cropping start coordinates(x,y)	16	16	16	16
Output picture width	8	8	8	8
Output picture height	2	2	2	2
Masks width and origin X	8	4	4	2
Masks width and origin Y	2	1	1	1
Frame buffer width and origin X	8	4	4	2
Frame buffer height and origin Y	2	1	1	1

5.4.19 Image Pre-processor

Pre-processor is pipelined with the encoder and it can be used only with the encoder. Pre-processor features are presented in Table 5-15.

Table 5-15 Post-processor features

Feature	**Encoder support**
RGB to YCbCr 4:2:0 color space conversion	BT.601, BT.709 or user defined coefficients conversion for RGB:

Feature	Encoder support
	RGB444 and BGR444 RGB555 and BRG555 RGB565 and BGR565 RGB888 and BRG888 RGB101010 and BRG101010
YCbCr 4:2:2 to YCbCr 4:2:0 color space conversion	YCbCr formats: YCbCr 4:2:0 planar YCbCr 4:2:0 semi-planar YCbYCr 4:2:2 CbYCrY 4:2:2 interleaved
Cropping	Video – from 8192x8192 to any supported encoding size
Rotation	90 or 270 degrees

5.4.20 H.264 Encoder

The H.264 features supported by encoder are as shown in Table 5-16 .

Table 5-16 Video encoder H.264 feature

Feature	Encoder support
Input data format	YCbCr formats: YCbCr 4:2:0 planar YCbCr 4:2:0 semi-planar YCbYCr 4:2:2① CbYCrY 4:2:2 Interleaved① RGB formats:① RGB444 to BGR444 RGB555 to BGR555 RGB565 to BGR565 RGB888 to BRG888 RGB101010 and BRG 101010
Output data format	H.264: Byte unit stream NAL unit stream
Supported image size	96x96 to 1920x1080(Full HD) Step size 4 pixels
Maximum frame rate	30 fps at 1920 x1080
Bit rate	Maximum 20Mbps Minimum 10kbps

①internally encoder handles image only in 4:2:0 format

Figure Fig. 5-21 illustrates the encoder data flow in H.264 encoding mode. The numbers present the following transactions:
Memory-mapped register writes and reads
Input image read
Reference image write
Reference image read

NAL sizes write from HW
NAL sizes read to SW
Output byte or NAL unit stream write from HW
Output byte or NAL unit stream headers write from SW

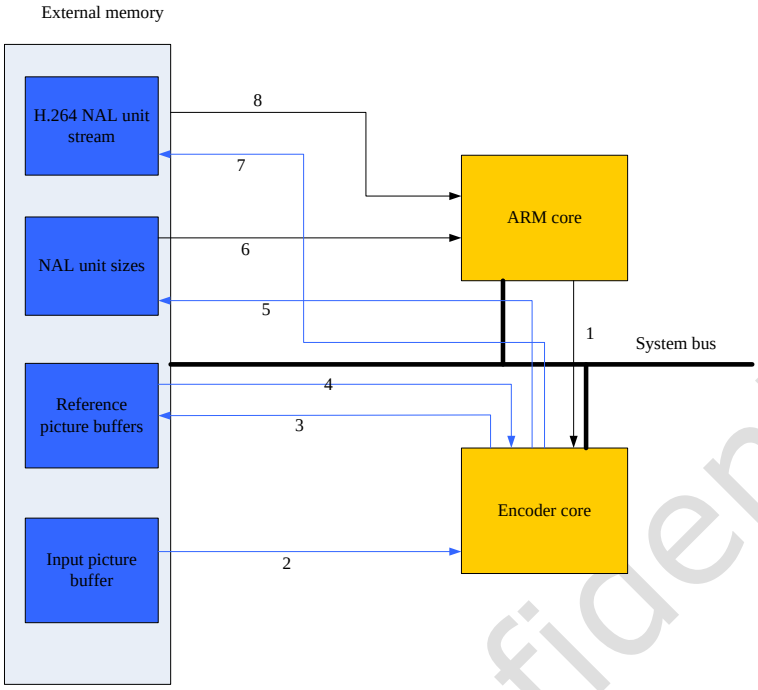


Fig. 5-21 Video Encoder Dataflow

The encoder software starts encoding the first picture by initializing hardware and writing the stream headers. After HW has encoded the image, SW calculates new quantization values for HW, and initializes HW again.

5.4.21 JPEG Encoder

The JPEG features supported by the encoder are as shown in Table 5-17.

Table 5-17 JPGE features

Feature	Encoder support
Input data format	YCbCr formats: YCbCr 4:2:0 planar YCbCr 4:2:0 semi-planar YCbCr 4:2:2① CbYCrY 4:2:2 Interleaved ① RGB formats:① RGB444 and BGR444 RGB555 and BGR555 RGB565 and BGR565 RGB888 and BRG888 RGB101010 and BRG101010
Output data format	JFIF ifle format 1.02 Non-progressive JPEG
Supported image size	96x32 to 8192x8192(64 million pixels) Step size 4 pixels
Maximum data rate	Up to 90 million pixels per second
Thumbnail insertion	RGB 8-bits, RGB 24-bits and JPEG compressed thumbnails supported

①internally encoder handles images only in 4:2:0 format

5.5 Register Description

5.5.1 Internal Address Mapping

This section describes the control/status registers of the codec.
If H264/VP9/HEVC decoder is chosen to work, the register base address is rkvdec_base. The reading MMU master register base address is rkvdec_base+0x480, the writing MMU register base address is rkvdec_base + 0x4c0, and the luma cache control register base address is rkvdec_base + 0x400, the chroma cache control register base address is rkvdec_base + 0x440.
If vepu is chosen to work, the base address is vpu_base. MMU base address is vpu +0x800, and cache control base address is vpu_base + 0xc00.
If other format is chosen to work, the base address is vpu_base + 0x400. MMU base address is vpu +0x800, and cache control base address is vpu_base + 0xc00.

5.5.2 H264/VP9/HEVC/Other Format Decoder Registers Summary

Name	Offset	Size	Reset Value	Description
rkvdec_swreg0_id	0x0000	W	0x68761f00	ID register (read only)
rkvdec_swreg1_int	0x0004	W	0x00000022	interrupt and decoder enable register
rkvdec_swreg2_sysctrl	0x0008	W	0x00000000	Data input and output endian setting and sys ctrl
rkvdec_swreg3_picpar	0x000c	W	0x00000000	picture parameters
rkvdec_swreg4_strm_rlc_base	0x0010	W	0x00000000	the stream or rlc data base address
rkvdec_swreg5_stream_rlc_len	0x0014	W	0x00000000	amount of stream bytes or rlc data byte in the input buffer or the
rkvdec_swreg6_cabactbl_prob_base	0x0018	W	0x00000000	the base address of cabac table
rkvdec_swreg7_decout_base	0x001c	W	0x00000000	base address of decoder output picture base address
rkvdec_swreg8_y_virstride	0x0020	W	0x00000000	the ouput picture y virtual stride
rkvdec_swreg9_yuv_virstride	0x0024	W	0x00000000	the ouput picture yuv virtual stride
rkvdec_swreg10_hevc_refer0_base	0x0028	W	0x00000000	base address for reference picture index 0
rkvdec_swreg10_h264_refer0_base	0x0028	W	0x00000000	base address for reference picture index 0
rkvdec_swreg10_vp9_cprheader_offset	0x0028	W	0x00000000	vp9 compressed header offset
rkvdec_swreg11_hevc_refer1_base	0x002c	W	0x00000000	base address for reference picture index 1
rkvdec_swreg11_h264_refer1_base	0x002c	W	0x00000000	base address for reference picture index 1
rkvdec_swreg11_vp9_referlast_base	0x002c	W	0x00000000	base address for last frame
rkvdec_swreg12_hevc_refer2_base	0x0030	W	0x00000000	base address for reference picture index 2

Name	Offset	Size	Reset Value	Description
rkvdec_swreg12_h264_refer2_base	0x0030	W	0x00000000	base address for reference picture index 2
rkvdec_swreg12_vp9_refergolden_base	0x0030	W	0x00000000	base address for golden frame
rkvdec_swreg13_hevc_refer3_base	0x0034	W	0x00000000	base address for reference picture index 3
rkvdec_swreg13_h264_refer3_base	0x0034	W	0x00000000	base address for reference picture index 3
rkvdec_swreg13_vp9_referalfter_base	0x0034	W	0x00000000	base address for referalfter frame
rkvdec_swreg14_hevc_refer4_base	0x0038	W	0x00000000	base address for reference picture index 4
rkvdec_swreg14_h264_refer4_base	0x0038	W	0x00000000	base address for reference picture index 4
rkvdec_swreg14_vp9count_base	0x0038	W	0x00000000	vp9 count base addr
rkvdec_swreg15_h264_refer5_base	0x003c	W	0x00000000	base address for reference picture index 5
rkvdec_swreg15_vp9_segidlast_base	0x003c	W	0x00000000	base address for last frame segment id
rkvdec_swreg15_hevc_refer5_base	0x003c	W	0x00000000	base address for reference picture index 5
rkvdec_swreg16_h264_refer6_base	0x0040	W	0x00000000	base address for reference picture index 6
rkvdec_swreg16_vp9_segidcur_base	0x0040	W	0x00000000	base address for cur frame segment id
rkvdec_swreg16_hevc_refer6_base	0x0040	W	0x00000000	base address for reference picture index 6
rkvdec_swreg17_h264_refer7_base	0x0044	W	0x00000000	base address for reference picture index 7
rkvdec_swreg17_vp9_frame_size_last	0x0044	W	0x00000000	vp9 last frame size
rkvdec_swreg17_hevc_refer7_base	0x0044	W	0x00000000	base address for reference picture index 7
rkvdec_swreg18_h264_refer8_base	0x0048	W	0x00000000	base address for reference picture index 8
rkvdec_swreg18_vp9_frame_size_golden	0x0048	W	0x00000000	vp9 golden frame size
rkvdec_swreg18_hevc_refer8_base	0x0048	W	0x00000000	base address for reference picture index 8
rkvdec_swreg19_h264_refer9_base	0x004c	W	0x00000000	base address for reference picture index 9
rkvdec_swreg19_vp9_frame_size_altref	0x004c	W	0x00000000	vp9 alfter frame size

Name	Offset	Size	Reset Value	Description
rkvdec_swreg19_hevc_refer9_base	0x004c	W	0x00000000	base address for reference picture index 9
rkvdec_swreg20_h264_refer10_base	0x0050	W	0x00000000	base address for reference picture index 10
rkvdec_swreg20_vp9_segid_grp0	0x0050	W	0x00000000	vp9 segid syntax grp0
rkvdec_swreg20_hevc_refer10_base	0x0050	W	0x00000000	base address for reference picture index 10
rkvdec_swreg21_h264_refer11_base	0x0054	W	0x00000000	base address for reference picture index 11
rkvdec_swreg21_vp9_segid_grp1	0x0054	W	0x00000000	vp9 segid syntax grp1
rkvdec_swreg21_hevc_refer11_base	0x0054	W	0x00000000	base address for reference picture index 11
rkvdec_swreg22_h264_refer12_base	0x0058	W	0x00000000	base address for reference picture index 12
rkvdec_swreg22_vp9_segid_grp2	0x0058	W	0x00000000	vp9 segid syntax grp2
rkvdec_swreg22_hevc_refer12_base	0x0058	W	0x00000000	base address for reference picture index 12
rkvdec_swreg23_h264_refer13_base	0x005c	W	0x00000000	base address for reference picture index 13
rkvdec_swreg23_vp9_segid_grp3	0x005c	W	0x00000000	vp9 segid syntax grp3
rkvdec_swreg23_hevc_refer13_base	0x005c	W	0x00000000	base address for reference picture index 13
rkvdec_swreg24_h264_refer14_base	0x0060	W	0x00000000	base address for reference picture index 14
rkvdec_swreg24_vp9_segid_grp4	0x0060	W	0x00000000	vp9 segid syntax grp4
rkvdec_swreg24_hevc_refer14_base	0x0060	W	0x00000000	base address for reference picture index 14
rkvdec_swreg25_vp9_segid_grp5	0x0064	W	0x00000000	vp9 segid syntax grp5
rkvdec_swreg25_refer0_poc	0x0064	W	0x00000000	the poc of reference picture index 0
rkvdec_swreg26_vp9_segid_grp6	0x0068	W	0x00000000	vp9 segid syntax grp6
rkvdec_swreg26_refer1_poc	0x0068	W	0x00000000	the poc of reference picture index 1
rkvdec_swreg27_vp9_segid_grp7	0x006c	W	0x00000000	vp9 segid syntax grp7
rkvdec_swreg27_refer2_poc	0x006c	W	0x00000000	the poc of reference picture index 2

Name	Offset	Size	Reset Value	Description
rkvdec_swreg28_vp9_cpr header_config	0x0070	W	0x00000000	vp9 compressed header config info
rkvdec_swreg28_refer3_p oc	0x0070	W	0x00000000	the poc of reference picture index 3
rkvdec_swreg29_vp9_lref _scale	0x0074	W	0x00000000	scaling factor for last reference picture
rkvdec_swreg29_refer4_p oc	0x0074	W	0x00000000	the poc of reference picture index 4
rkvdec_swreg30_vp9_gref _scale	0x0078	W	0x00000000	scaling factor for golden reference picture
rkvdec_swreg30_refer5_p oc	0x0078	W	0x00000000	the poc of reference picture index 5
rkvdec_swreg31_vp9_aref _scale	0x007c	W	0x00000000	scaling factor for alfter reference picture
rkvdec_swreg31_refer6_p oc	0x007c	W	0x00000000	the poc of reference picture index 6
rkvdec_swreg32_vp9_ref_ deltas_lastframe	0x0080	W	0x00000000	vp9 ref deltas
rkvdec_swreg32_refer7_p oc	0x0080	W	0x00000000	the poc of reference picture index 7
rkvdec_swreg33_vp9_info _lastframe	0x0084	W	0x00000000	vp9 info for lastframe
rkvdec_swreg33_refer8_p oc	0x0084	W	0x00000000	the poc of reference picture index 8
rkvdec_swreg34_vp9_inte rcmd_base	0x0088	W	0x00000000	inter cmd base addr
rkvdec_swreg34_refer9_p oc	0x0088	W	0x00000000	the poc of reference picture index 9
rkvdec_swreg35_vp9_inte rcmd_num	0x008c	W	0x00000000	vp9 intercmd num
rkvdec_swreg35_refer10_ poc	0x008c	W	0x00000000	the poc of reference picture index 10
rkvdec_swreg36_vp9_last tile_size	0x0090	W	0x00000000	vp9 lasttile size
rkvdec_swreg36_refer11_ poc	0x0090	W	0x00000000	the poc of reference picture index 11
rkvdec_swreg37_vp9_last f_hor_virstride	0x0094	W	0x00000000	Register0000 Abstract
rkvdec_swreg37_refer12_ poc	0x0094	W	0x00000000	the poc of reference picture index 12
rkvdec_swreg38_vp9_gol denf_hor_virstride	0x0098	W	0x00000000	vp9 golden frame horizontal virstride
rkvdec_swreg38_refer13_ poc	0x0098	W	0x00000000	the poc of reference picture index 13

Name	Offset	Size	Reset Value	Description
rkvdec_swreg39_vp9_altreff_hor_virstride	0x009c	W	0x00000000	vp9 altref frame horizontal virstride
rkvdec_swreg39_refer14_poc	0x009c	W	0x00000000	the poc of reference picture index 14
rkvdec_swreg40_cur_poc	0x00a0	W	0x00000000	the poc of cur picture
rkvdec_swreg41_rlcwrite_base	0x00a4	W	0x00000000	the base address or rlcwrite base addr
rkvdec_swreg42_pps_base	0x00a8	W	0x00000000	the base address of pps
rkvdec_swreg43_rps_base	0x00ac	W	0x00000000	the base address of rps
rkvdec_swreg44_strmd_error_en	0x00b0	W	0x00000000	cabac error enable config
rkvdec_swreg45_strmd_error_status	0x00b4	W	0x00000000	cabac error status
rkvdec_swreg45_vp9_error_info0	0x00b4	W	0x00000000	vp9 error info
rkvdec_swreg46_strmd_error_ctu	0x00b8	W	0x00400000	strmd error ctu
rkvdec_swreg47_sao_ctu_position	0x00bc	W	0x00000000	sao ctu position
rkvdec_swreg48_h264_refer15_base	0x00c0	W	0x00000000	base address for reference picture index 15
rkvdec_swreg48_vp9_last_ystride	0x00c0	W	0x00000000	last ref ystride
rkvdec_swreg49_h264_refer15_poc	0x00c4	W	0x00000000	the poc of reference picture index 15
rkvdec_swreg49_vp9_golden_ystride	0x00c4	W	0x00000000	golden ref ystride
rkvdec_swreg50_h264_refer16_poc	0x00c8	W	0x00000000	the poc of reference picture index 16
rkvdec_swreg50_vp9_altrefy_ystride	0x00c8	W	0x00000000	altref ref ystride
rkvdec_swreg51_h264_refer17_poc	0x00cc	W	0x00000000	the poc of reference picture index 17
rkvdec_swreg51_vp9_lastref_yuvstride	0x00cc	W	0x00000000	vp9 lastref yuv stride
rkvdec_swreg52_vp9_refcolmv_base	0x00d0	W	0x00000000	vp9 colmv ref base
rkvdec_swreg52_h264_refer18_poc	0x00d0	W	0x00000000	the poc of reference picture index 18
rkvdec_swreg53_h264_refer19_poc	0x00d4	W	0x00000000	the poc of reference picture index 19
rkvdec_swreg54_h264_refer20_poc	0x00d8	W	0x00000000	the poc of reference picture index 20

Name	Offset	Size	Reset Value	Description
rkvdec_swreg55_h264_refer21_poc	0x00dc	W	0x00000000	the poc of reference picture index 21
rkvdec_swreg56_h264_refer22_poc	0x00e0	W	0x00000000	the poc of reference picture index 22
rkvdec_swreg57_h264_refer23_poc	0x00e4	W	0x00000000	the poc of reference picture index 23
rkvdec_swreg58_h264_refer24_poc	0x00e8	W	0x00000000	the poc of reference picture index 24
rkvdec_swreg59_h264_refer25_poc	0x00ec	W	0x00000000	the poc of reference picture index 25
rkvdec_swreg60_h264_refer26_poc	0x00f0	W	0x00000000	the poc of reference picture index 26
rkvdec_swreg61_h264_refer27_poc	0x00f4	W	0x00000000	the poc of reference picture index 27
rkvdec_swreg62_h264_refer28_poc	0x00f8	W	0x00000000	the poc of reference picture index 28
rkvdec_swreg63_h264_refer29_poc	0x00fc	W	0x00000000	the poc of reference picture index 29
rkvdec_swreg64_performance_cycle	0x0100	W	0x00000000	hevc performance cycle
rkvdec_swreg65_axi_ddr_rdata	0x0104	W	0x00000000	axi ddr read data num
rkvdec_swreg66_axi_ddr_wdata	0x0108	W	0x00000000	axi ddr write data number
rkvdec_swreg68_performance_sel	0x0110	W	0x00000000	
rkvdec_swreg69_performance_cnt0	0x0114	W	0x00000000	
rkvdec_swreg70_performance_cnt1	0x0118	W	0x00000000	
rkvdec_swreg71_performance_cnt2	0x011c	W	0x00000000	
rkvdec_swreg72_h264_refer30_poc	0x0120	W	0x00000000	the poc of reference picture index 30
rkvdec_swreg73_h264_refer31_poc	0x0124	W	0x00000000	the poc of reference picture index 31
rkvdec_swreg74_h264_cur_poc1	0x0128	W	0x00000000	h264 cur poc for bottom filed
rkvdec_swreg75_h264_errorinfo_base	0x012c	W	0x00000000	h264 error info base addr
rkvdec_swreg76_h264_errorinfo_num	0x0130	W	0x00000000	h264 error info num
rkvdec_swreg77_h264_error_e	0x0134	W	0x00000000	h264 error enable high bits

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

Name	Offset	Size	Reset Value	Description
VDPU_SWREG0	0x0000	W	0x00010100	axi control
VDPU_SWREG1	0x0004	W	0x00000000	color coeff register
VDPU_SWREG2	0x0008	W	0x00000000	color coeff register
VDPU_SWREG3	0x000c	W	0x00000000	color coeff register
VDPU_SWREG4	0x0010	W	0x00000000	scl ctrl register
VDPU_SWREG5	0x0014	W	0x00000000	scl ctrl register
VDPU_SWREG6	0x0018	W	0x00000000	scl ctrl register
VDPU_SWREG7	0x001c	W	0x00000000	Amount of pixels beyond border
VDPU_SWREG8	0x0020	W	0x00000000	Amount of pixels beyond border
VDPU_SWREG9	0x0024	W	0x00000000	Rmask register
VDPU_SWREG10	0x0028	W	0x00000000	Gmask register
VDPU_SWREG11	0x002c	W	0x00000000	Bmask register
VDPU_SWREG12	0x0030	W	0x00000000	PP input picture base address for Y bottom field
VDPU_SWREG13	0x0034	W	0x00000000	PP input picture base for Ch bottom field
VDPU_SWREG14	0x0038	W	0x00000000	coordinate used in macroblock crop
VDPU_SWREG15	0x003c	W	0x00000000	range map register
VDPU_SWREG16	0x0040	W	0x00000000	total num of padded for RGB
VDPU_SWREG17	0x0044	W	0x00000000	hw support informan,read only
VDPU_SWREG18	0x0048	W	0x00000000	base address for reading post-processing input picture uminan
VDPU_SWREG19	0x004c	W	0x00000000	Base address for reading post-processing input picture Cb/Ch
VDPU_SWREG20	0x0050	W	0x00000000	input cr component address
VDPU_SWREG21	0x0054	W	0x00000000	Base address for writing post-processed picture luminance/RGB
VDPU_SWREG22	0x0058	W	0x00000000	Base address for writing post-processed picture Ch
VDPU_SWREG23	0x005c	W	0x00000000	Display width and PP input size extension register
VDPU_SWREG24	0x0060	W	0x00000000	alpha blending base address
VDPU_SWREG25	0x0064	W	0x00000000	ablend of pixels scanline
VDPU_SWREG26	0x0068	W	0x00000000	x-coordinate of mask area 1 for Horizontal start pixel
VDPU_SWREG27	0x006c	W	0x00000000	y-coordinate of mask area 1 for Horizontal start pixel
VDPU_SWREG28	0x0070	W	0x00000000	x-coordinate of mask area 2 for Horizontal start pixel

Name	Offset	Size	Reset Value	Description
VDPU_SWREG29	0x0074	W	0x00000000	y-coordinate of mask area 2 for Horizontal start pixel
VDPU_SWREG30	0x0078	W	0x00000000	register for deinterlace ctrl
VDPU_SWREG31	0x007c	W	0x00000000	contrast adjust threshold
VDPU_SWREG32	0x0080	W	0x00000000	contrast adjust offset
VDPU_SWREG33	0x0084	W	0xfc874780	Synthesis configuration register post-processor (read only)
VDPU_SWREG34	0x0088	W	0x00000000	PP input pic size register
VDPU_SWREG35	0x008c	W	0x00000000	PP output pic size register
VDPU_SWREG36	0x0090	W	0x00000000	the dither mode for RGB
VDPU_SWREG37	0x0094	W	0x00000000	PP input/output data format
VDPU_SWREG38	0x0098	W	0x00000000	PP input/output data format
VDPU_SWREG39	0x009c	W	0x00000000	Register0000 Abstract
VDPU_SWREG40	0x00a0	W	0x00000000	pp int register
VDPU_SWREG41	0x00a4	W	0x00000008	enable ctrl flag
VDPU_SWREG50	0x00c8	W	0x00000000	video decoder ctrl register
VDPU_SWREG51	0x00cc	W	0x00000000	the stream length
VDPU_SWREG52	0x00d0	W	0x00000000	error concealment case related
VDPU_SWREG53	0x00d4	W	0x00000000	decoder format
VDPU_SWREG54	0x00d8	W	0x00000000	endian for input/output data
VDPU_SWREG55	0x00dc	W	0x00000000	decoder int register
VDPU_SWREG56	0x00e0	W	0x00200101	axi ctrl for decoder
VDPU_SWREG57	0x00e4	W	0x00000010	enable flag for decoder
VDPU_SWREG58	0x00e8	W	0x00000000	soft reset register
VDPU_SWREG59	0x00ec	W	0x00000000	H264, MPEG4, VP6 Prediction filter tap
VDPU_SWREG60	0x00f0	W	0x00000000	additional chrominance address
VDPU_SWREG61	0x00f4	W	0x00000000	standard dependent tables start address
VDPU_SWREG62	0x00f8	W	0x00000000	Direct mode motion vector write/read start address
VDPU_SWREG63	0x00fc	W	0x00000000	write decoder output picture or field start address
VDPU_SWREG64	0x0100	W	0x00000000	rlc or vlc mode input data start addr
VDPU_SWREG65	0x0104	W	0x00000000	refbufferd related
VDPU_SWREG66	0x0108	W	0x67312688	ID register
VDPU_SWREG67	0x010c	W	0xe5da0000	Synthesis configuration register decoder 1(read only)
VDPU_SWREG68	0x0110	W	0x00000000	sum of partitions(read only)
VDPU_SWREG69	0x0114	W	0x00000000	sum information (read only)
VDPU_SWREG70	0x0118	W	0x00000000	sum of the decoded motion vector y-components(read only)
VDPU_SWREG71	0x011c	W	0xfbb56f80	information for read only register

Name	Offset	Size	Reset Value	Description
VDPU_SWREG72	0x0120	W	0x00000000	debug0
VDPU_SWREG73	0x0124	W	0x00000000	debug registers
VDPU_SWREG74	0x0128	W	0x00000000	MV address for h264
VDPU_SWREG75	0x012c	W	0x00000000	H.264 Intra prediction 4x4 mode start address
VDPU_SWREG76	0x0130	W	0x00000000	the number of referance pic
VDPU_SWREG77	0x0134	W	0x00000000	the number of referance pic
VDPU_SWREG78	0x0138	W	0x00000000	the number of referance pic
VDPU_SWREG79	0x013c	W	0x00000000	the number of referance pic
VDPU_SWREG80	0x0140	W	0x00000000	the number of referance pic
VDPU_SWREG81	0x0144	W	0x00000000	the number of referance pic
VDPU_SWREG82	0x0148	W	0x00000000	the number of referance pic
VDPU_SWREG83	0x014c	W	0x00000000	the number of referance pic
VDPU_SWREG84	0x0150	W	0x00000000	referance frame0 address for h264
VDPU_SWREG85	0x0154	W	0x00000000	referance frame1 address for h264
VDPU_SWREG86	0x0158	W	0x00000000	referance frame2 address for h264
VDPU_SWREG87	0x015c	W	0x00000000	referance frame3 address for h264
VDPU_SWREG88	0x0160	W	0x00000000	referance frame4 address for h264
VDPU_SWREG89	0x0164	W	0x00000000	referance frame5 address for h264
VDPU_SWREG90	0x0168	W	0x00000000	referance frame6 address for h264
VDPU_SWREG91	0x016c	W	0x00000000	referance frame7 address for h264
VDPU_SWREG92	0x0170	W	0x00000000	referance frame8 address for h264
VDPU_SWREG93	0x0174	W	0x00000000	referance frame9 address for h264
VDPU_SWREG94	0x0178	W	0x00000000	referance frame10 address for h264
VDPU_SWREG95	0x017c	W	0x00000000	referance frame11 address for h264
VDPU_SWREG96	0x0180	W	0x00000000	referance frame12 address for h264
VDPU_SWREG97	0x0184	W	0x00000000	referance frame13 address for h264
VDPU_SWREG98	0x0188	W	0x00000000	referance frame14 address for h264
VDPU_SWREG99	0x018c	W	0x00000000	referance frame15 address for h264
VDPU_SWREG100	0x0190	W	0x00000000	initial reference picture list related
VDPU_SWREG101	0x0194	W	0x00000000	initial reference picture list related
VDPU_SWREG102	0x0198	W	0x00000000	initial reference picture list related
VDPU_SWREG103	0x019c	W	0x00000000	initial reference picture list related
VDPU_SWREG104	0x01a0	W	0x00000000	initial reference picture list related
VDPU_SWREG105	0x01a4	W	0x00000000	initial reference picture list related
VDPU_SWREG106	0x01a8	W	0x00000000	initial reference picture list related
VDPU_SWREG107	0x01ac	W	0x00000000	long term flag for reference pictuure index

Name	Offset	Size	Reset Value	Description
VDPU_SWREG108	0x01b0	W	0x00000000	valid flag for reference picture index
VDPU_SWREG109	0x01b4	W	0x00000000	the stream start word for decoder
VDPU_SWREG110	0x01b8	W	0x00000000	h264 pic mb size
VDPU_SWREG111	0x01bc	W	0x00000000	h264 ctrl related
VDPU_SWREG112	0x01c0	W	0x00000000	current frame related
VDPU_SWREG113	0x01c4	W	0x00000000	reference picture related
VDPU_SWREG114	0x01c8	W	0x00000000	maximum reference
VDPU_SWREG115	0x01cc	W	0x00000000	enable flag
VDPU_SWREG120	0x01e0	W	0x00000000	multi format reuse register0
VDPU_SWREG121	0x01e4	W	0x00000000	multi format reuse register1
VDPU_SWREG122	0x01e8	W	0x00000000	multi format reuse register2
VDPU_SWREG123	0x01ec	W	0x00000000	multi format reuse register3
VDPU_SWREG124	0x01f0	W	0x00000000	multi format reuse register4
VDPU_SWREG125	0x01f4	W	0x00000000	multi format reuse register5
VDPU_SWREG126	0x01f8	W	0x00000000	multi format reuse register6
VDPU_SWREG127	0x01fc	W	0x00000000	multi format reuse register7
VDPU_SWREG128	0x0200	W	0x00000000	multi format reuse register8
VDPU_SWREG129	0x0204	W	0x00000000	multi format reuse register9
VDPU_SWREG130	0x0208	W	0x00000000	multi format reuse register10
VDPU_SWREG131	0x020c	W	0x00000000	multi format reuse register11
VDPU_SWREG132	0x0210	W	0x00000000	multi format reuse register12
VDPU_SWREG133	0x0214	W	0x00000000	multi format reuse register13
VDPU_SWREG134	0x0218	W	0x00000000	multi format reuse register14
VDPU_SWREG135	0x021c	W	0x00000000	multi format reuse register15
VDPU_SWREG136	0x0220	W	0x00000000	multi format reuse register16
VDPU_SWREG137	0x0224	W	0x00000000	multi format reuse register17
VDPU_SWREG138	0x0228	W	0x00000000	multi format reuse register18
VDPU_SWREG139	0x022c	W	0x00000000	multi format reuse register19
VDPU_SWREG140	0x0230	W	0x00000000	multi format reuse register20
VDPU_SWREG141	0x0234	W	0x00000000	multi format reuse register21
VDPU_SWREG142	0x0238	W	0x00000000	multi format reuse register22
VDPU_SWREG143	0x023c	W	0x00000000	multi format reuse register23
VDPU_SWREG144	0x0240	W	0x00000000	multi format reuse register24
VDPU_SWREG145	0x0244	W	0x00000000	multi format reuse register25
VDPU_SWREG146	0x0248	W	0x00000000	multi format reuse register26
VDPU_SWREG147	0x024c	W	0x00000000	multi format reuse register27
VDPU_SWREG148	0x0250	W	0x00000000	multi format reuse register28
VDPU_SWREG149	0x0254	W	0x00000000	multi format reuse register29
VDPU_SWREG150	0x0258	W	0x00000000	multi format reuse register30
VDPU_SWREG151	0x025c	W	0x00000000	multi format reuse register31
VDPU_SWREG152	0x0260	W	0x00000000	multi format reuse register32
VDPU_SWREG153	0x0264	W	0x00000000	multi format reuse register33
VDPU_SWREG154	0x0268	W	0x00000000	multi format reuse register34

Name	Offset	Size	Reset Value	Description
VDPU_SWREG155	0x026c	W	0x00000000	multi format reuse register35
VDPU_SWREG156	0x0270	W	0x00000000	multi format reuse register36
VDPU_SWREG157	0x0274	W	0x00000000	multi format reuse register37
VDPU_SWREG158	0x0278	W	0x00000000	multi format reuse register38
VDPU_SWREG164_PERF_LATENCY_CTRL0	0x0290	W	0x00000000	Axi performance latency module contrl register0
VDPU_SWREG165_PERF_LATENCY_CTRL1	0x0294	W	0x00000000	PERF_LATENCY_CTRL1
VDPU_SWREG166_PERF_RD_MAX_LATENCY_NUM0	0x0298	W	0x00000000	Read max latency number
VDPU_SWREG167_PERF_RD_LATENCY_SAMP_NUM	0x029c	W	0x00000000	The number of bigger than configed threshold value
VDPU_SWREG168_PERF_RD_LATENCY_ACC_SUM	0x02a0	W	0x00000000	Total sample number
VDPU_SWREG169_PERF_RD_AXI_TOTAL_BYTE	0x02a4	W	0x00000000	perf_rd_axi_total_byte
VDPU_SWREG170_PERF_WR_AXI_TOTAL_BYTE	0x02a8	W	0x00000000	perf_wr_axi_total_byte
VDPU_SWREG171_PERF_WORKING_CNT	0x02ac	W	0x00000000	perf_working_cnt

5.5.3 H264/VP9/HEVC/Others Decoder Detail Register Description

rkvdec_swreg0_id
Address: Operational Base + offset (0x0000)
ID register (read only)

Bit	Attr	Reset Value	Description
31:16	RO	0x6876	prod_num product number The ascii code of "hv", which is 0x6876
15	RO	0x0	reserved
14	RO	0x0	codec_flag codec flag 0: only dec 1: dec + enc
13	RO	0x0	reserved
12	RW	0x1	profile hevc profile 0: Main 1: Main10
11:9	RO	0x7	dec_support dec support bits bit0: HEVC support or not, when it is 1'b1, support bit1: H264 support or not bit2: VP9 support or not

Bit	Attr	Reset Value	Description
8	RO	0x1	level level 0: FHD 1: UHD
7:0	RO	0x00	minor_ver minor version minor version

rkvdec_swreg1_int
Address: Operational Base + offset (0x0004)
interrupt and decoder enable register

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	RW	0x0	sw_softreset_rdy when it is 1'b1, it says that softreset has been done
21	RO	0x0	reserved
20	RW	0x0	sw_softrst_en_p softreset enable softreset enable signal write 1 to soft reset, write 0 invalid puls register
19	RW	0x0	sw_h264orvp9_error_mode h264 or vp9 error mode for VP9: 1'b0: when there is any stream or colmv error, the hardware will stop the decode and reset itself 1'b1: when there is any stream or colmv error, the hardware will still decode the next slice it is recommend that when vp9 , it is configed to 1'b0 for H264: 1'b0: when there is any stream , the hardware will stop the decoder and reset itself 1'b1: when there is any stream error, the hardware will wait the end signal of deblocking and then reset itself
18	RW	0x0	sw_cabu_end_sta cabac decode end status hevc: cabac decode end status h264& vp9 : streamd decode status

Bit	Attr	Reset Value	Description
17	RW	0x0	sw_colmv_ref_error_sta colmv ref error status colmv ref error status hevc&vp9: when it is 1'b1, it means that inter module read the invalid dpb frame It will self reset the hardware h264: when it is 1'b1, it means that inter module read the invalid dpb frame. when sw_h264_error_mode is 1'b0, it will self reset the hardware, otherwise it will not
16	RW	0x0	sw_buf_empty_sta buffer empty sta buffer empty status, only when sw_buf_empty_en is 1'b1 , this bit is valid, now is for no valid
15	RW	0x0	sw_dec_timeout_sta decoder timeout interrupt status When high the decoder has been idling for too long. it will self reset the hardware only when sw_dec_timeout_e is 1'b1, this bit is valid
14	RW	0x0	sw_dec_error_sta status bit of input stream error hevc & vp9:when high, an error is found in input data stream decoding. It will self reset the hardware. h264: when high, an error is found in input data stream decoding.when sw_h264_error_mode is 1'b0, it will self reset the hardware, otherwise it will not
13	RW	0x0	sw_dec_bus_sta bus error status When this bit is high, there is error on the axi bus, it will self reset hardware
12	RW	0x0	sw_dec_rdy_sta decoder ready status when this bit is high, decoder has decoded a picture(the loop filter module send out a frame rdy)
11	RO	0x0	reserved
10	WO	0x0	sw_dec_e_rewrite_valid sw_de_e rewrite valid signal sw_dec_e rewrite valid signal maybe for only when buffer empty, restart the decoder use
9	RW	0x0	sw_dec_irq_raw the raw status of sw_dec_irq the raw status of sw_dec_irq,SW should reset this bit after interrupt is handled

Bit	Attr	Reset Value	Description
8	RO	0x0	sw_dec_irq decoder IRQ when high, decoder requests an interrrupt. sw_dec_irq = sw_dec_irq_raw && (sw_dec_irq_dis == 1'b0)
7	RW	0x0	sw_stmerror_waitdecfifo_empty whether the stream error process wait the decfifo empty when it is 1'b0, the stream error process will no wait the ca2decfifo empty when it is 1'b1, the stream error process will wait the ca2decfifo empty when sw_dec_mode is HEVC and VP9, it always take effect; when sw_dec_mode is H264, it only take effect when sw_h264_error_mode is 1'b0
6	RW	0x0	sw_buf_empty_en buffer empty int enable buffer empty interrupt enable, now is for no use
5	RW	0x1	sw_dec_timeout_e Timeout interrupt enable If enabled HW may return timeout interrupt in case HW gets stucked while decoding picture.
4	RW	0x0	sw_dec_irq_dis decoder IRQ disable When hight, there are no interrupts concerning decoder from HW. Polling must be used to see the interrupt status
3	RW	0x0	sw_timeout_mode time out mode timeout mode select 1'b0: TIMEOUT_CYCLES is 241'b1 1'b1: TIMEOUT_CYCLES is 181'b1
2	RO	0x0	reserved
1	RW	0x1	sw_dec_clkgate_e decoder dynamic clock gating enable 0 = clock is running for all structures 1 = clock is gated for decoder structures that are not used
0	RW	0x0	sw_dec_e decoder enable Decoder enable. Setting this bit high will start the decoding operation. HW will reset this when the picture is decoded ready or bus error or time out interrupt is given for all decode format. HW will reset this when picture is processed stream error for vp9 & hevc & (h264 when sw_h264_error_mode is 1'b0)

rkvdec_swreg2_sysctrl
Address: Operational Base + offset (0x0008)
Data input and output endian setting and sys ctrl

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	sw_h264_frame_orslice h264 frame or slice for H264 use 1'b0: frame 1'b1: slice when sw_h264_streamd_mode is 1'b0, this register is valid
27	RW	0x0	sw_h264_firstslice_flag firstslice flag 1'b1: first packet in the frame, for h264 decode to read rps/pps data because the first_mb_in_slice may be wrong, so need this syntax
26	RW	0x0	sw_h264_stream_lastpacket stream last packet flag when sw_h264_stream_mode is 1'b1 sw_h264_stream_lastpacket 1'b0: this packet is not the last packet of frame 1'b1: the packet is the last packet of frame
25	RW	0x0	sw_h264_stream_mode h264 stream mode 1'b0: stream packet is slice by slice or frame by frame, should use sw_h264_frame_orslice 1'b1: stream packet is random, should use sw_h264_stream_last
24	RW	0x0	sw_h264_rps_mode h264 rps mode 1'b0: hardware parse rps mode 1'b1: software parse rps mode
23:22	RO	0x0	reserved
21:20	RW	0x0	sw_dec_mode dec mode 2'd0: hevc 2'd1: h264 2'd2: vp9
19	RO	0x0	reserved
18:12	RW	0x00	sw_strm_start_bit exact bit of stream start exact bit of streamd start word where decoding can be started (asosiates with sw_str_rlc_base)
11	RW	0x0	sw_rlc_mode rlc mode enable 0 = HW decodes video from bit stream 1 = HW decodes video from RLC input data

Bit	Attr	Reset Value	Description
10	RW	0x0	sw_rlc_mode_direct_write cabac decode output direct write cabac decode output direct write enable when this bit is enable , all the module other than cabac and busifd are not work
9	RO	0x0	reserved
8	RW	0x0	sw_out_cbcr_swap output cbcr swap 1'b0: cb(u) is in the lower address, cr(v) is in the higher address 1'b1: cb(u) is in the higher address,cr(v) is in the lower address sw_in_cbcr_swap is the same with sw_out_cbcr_swap
7	RW	0x0	sw_out_swap32_e decoder output data and dpb input data 32bit swap may be used for 64 or 128 bit environment 0 = no swapping of 32 bit words 1 = 32 bit data words are swapped
6	RW	0x0	sw_out_endian dec output data and colmv , dpb data and colmv input endian 0 = little endian 1 = big endian for litter enadian , a data 0x12345678, 0x78 is stored in lower address, 0x12 is stored in higher address
5	RW	0x0	sw_str_swap64_e stream 64bit data swap may be used for 128 bit environment 0 = no swapping of 64 bit words 1 = 64 bit data words are swapped
4	RW	0x0	sw_str_swap32_e stream 32bit data swap may be used for 64 or 128 bit environment 0 = no swapping of 32 bit words 1 = 32 bit data words are swapped
3	RW	0x0	sw_str_endian stream data input endian mode 0 = little endian 1 = big endian for litter enadian , a data 0x12345678, 0x78 is stored in lower address, 0x12 is stored in higher address
2	RW	0x0	sw_in_swap64_e input 64bit data swap for other than stream and dpb data may be used for 128 bit environment 0 = no swapping of 64 bit words 1 = 64 bit data words are swapped

Bit	Attr	Reset Value	Description
1	RW	0x0	sw_in_swap32_e input 32bit data swap for other than stream and dpb data may be used for 64 or 128 bit environment 0 = no swapping of 32 bit words 1 = 32 bit data words are swapped
0	RW	0x0	sw_in_endian decoder input endian mode for other than stream and dpb data 0 = little endian 1 = big endian for litter enadian , a data 0x12345678, 0x78 is stored in lower address, 0x12 is stored in higher address

rkvdec_swreg3_picpar
Address: Operational Base + offset (0x000c)
picture parameters

Bit	Attr	Reset Value	Description
31:21	RW	0x000	sw_slice_num_lowbits slice number in a frame hevc:slice number in a frame (0~199, when it is 0, it real means 1 slice in a frame) just only used for rps read. 2013.11.27 change the meaning from count from 1, so it will be in 1~200 2013.11.30 sw_slice_num max value is change to 600, so sw_slice_num expand to 10bit h264:slice number in a frame (0~4095, when it is 1, it real means 1 slice in a frame), for H264, it means sw_slice_num_lowbits vp9: no use
20:12	RW	0x000	sw_uv_hor_virstride uv horizontal virstride picture horizontal virtual stride (the unit is 128bit) the max is (4096x1.5 + 128) /16 = 0x188 suggest this register to config to even for advance ddr performance
11	RW	0x0	sw_slice_num_highbit the highest bit of sw_slice_num the highest bit of sw_slice_num
10:9	RO	0x0	reserved
8:0	RW	0x000	sw_y_hor_virstride picture horizontal virtual stride picture horizontal virtual stride (the unit is 128bit) the max is (4096x1.5 + 128) /16 = 0x188 suggest this register to config to even for advance ddr performance

rkvdec_swreg4_strm_rlc_base

Address: Operational Base + offset (0x0010)
the stream or rlc data base address

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_strm_rlc_base the stream or rlc data base address when swreg2.sw_rlc_mode =1, it is base address for rlc data when swreg2.sw_rlc_mode =0, it is base address for stream , after a frame is decoded ready or error (stream error , time out , bus error) , it is the last address of the stream the address should 128bit align
3:0	RO	0x0	reserved

rkvdec_swreg5_stream_rlc_len
Address: Operational Base + offset (0x0014)
amount of stream bytes or rlc data byte in the input buffer or the

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:0	RW	0x0000000	sw_stream_len amount of stream (unit is 8bit) in the input buffer amount of stream 8bits in the input buffer the max of sw_stream_len : 4096x2304x1.5x1.5 = 0x1440000 128bits unit: 0x1440000/16 = 0x144000 it is count from 0 2013.10.15 change to 23bit for zty's suggestion 2013.10.28, amount of stream data bytes in input buffer. it is count from 1, change to 27bits

rkvdec_swreg6_cabactbl_prob_base
Address: Operational Base + offset (0x0018)
the base address of cabac table

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_cabactbl_base the base address of cabac table the base address of cabac table the address should 128bit align
3:0	RO	0x0	reserved

rkvdec_swreg7_decout_base
Address: Operational Base + offset (0x001c)
base address of decoder output picture base address

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_decout_base base address of decoder output picture addr base address of decoder output picture the address should be 128bit align in H264 decode format, the top field and bottom field are the same addr
3:0	RO	0x0	reserved

rkvdec_swreg8_y_virstride
Address: Operational Base + offset (0x0020)
the ouput picture y virtual stride

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	sw_y_virstride the output picture y virtual stride the output picture y virtual stride (the unit is 128bit) the max: (4096x1.5 +128) x 2304 = 0xdc8000 we can know the sw_uvout_base = sw_decout_base + (sw_y_virstride <<4)

rkvdec_swreg9_yuv_virstride
Address: Operational Base + offset (0x0024)
the ouput picture yuv virtual stride

Bit	Attr	Reset Value	Description
31:21	RO	0x0	reserved
20:0	RW	0x000000	sw_yuv_virstride the ouput picture yuv virtual stride the output picture yuv virtual stride (the unit is 128bit) the max : (4096x1.5 +128) x 2304 x1.5 = 0x14ac000 we can know the sw_mvout_base = sw_decout_base + (sw_yuv_virstride <<4) for yuv422: 4096x2304x2x1.25= 0x1680000

rkvdec_swreg10_hevc_refer0_base
Address: Operational Base + offset (0x0028)
base address for reference picture index 0

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer0_base base address for reference picture index0 base address for reference picture index 0 (the address should be 128bit align)
3:0	RW	0x0	sw_ref_valid_0_3 valid flag for picture index 0 ~3 valid flag for picture index 0 ~3

rkvdec_swreg10_h264_refer0_base
Address: Operational Base + offset (0x0028)
base address for reference picture index 0

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer0_base base address for reference picture index0 base address for reference picture index0 (the address should be 128bit align)
3	RW	0x0	sw_ref0_colmv_use_flag ref0 colmv use flag ref0 colmv use flag
2	RW	0x0	sw_ref0_botfield_used bottom field is used bottom field is used the same meaning with ref_valid
1	RW	0x0	sw_ref0_topfield_used top field is used top field is used the same meaning with ref_valid
0	RW	0x0	sw_ref0_field reference 0 picture field flag 1'b0: frame 1'b1: field

rkvdec_swreg10_vp9_cprheader_offset
Address: Operational Base + offset (0x0028)
vp9 compressed header offset

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	sw_vp9_cprheader_offset vp9 compressed header offset vp9 compressed header offset, at most 2000 probs, 10bit per prob, 20000 bit at most now is for no use, because it can read from the last syntax of the uncompressed header

rkvdec_swreg11_hevc_refer1_base
Address: Operational Base + offset (0x002c)
base address for reference picture index 1

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer1_base base address for reference picture index 1 base address for reference picture index 1 (the address should be 128bit align)

Bit	Attr	Reset Value	Description
3:0	RW	0x0	sw_ref_valid_4_7 valid flag for picture index 4 ~7 valid flag for picture index 4 ~7

rkvdec_swreg11_h264_refer1_base
Address: Operational Base + offset (0x002c)
base address for reference picture index 1

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer1_base base address for reference picture index1 base address for reference picture index1 (the address should be 128bit align)
3	RW	0x0	sw_ref1_colmv_use_flag sw_ref1_colmv_use_flag sw_ref1_colmv_use_flag
2	RW	0x0	sw_ref1_botfield_used ref1 bottom field is used ref1 bottom field is used
1	RW	0x0	sw_ref1_topfield_used ref1 topfield is used ref1 topfield is used
0	RW	0x0	sw_ref1_field reference 1 picture field flag 1'b0: frame 1'b1: field

rkvdec_swreg11_vp9_referlast_base
Address: Operational Base + offset (0x002c)
base address for last frame

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_vp9last_base base address for last frame base address for last (the address should be 128bit align)
3:0	RO	0x0	reserved

rkvdec_swreg12_hevc_refer2_base
Address: Operational Base + offset (0x0030)
base address for reference picture index 2

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer2_base base address for reference picture index 2 base address for reference picture index 2 (the address should be 128bit align)

Bit	Attr	Reset Value	Description
3:0	RW	0x0	sw_ref_valid_8_11 valid flag for picture index 8~11 valid flag for picture index 8~11

rkvdec_swreg12_h264_refer2_base
Address: Operational Base + offset (0x0030)
base address for reference picture index 2

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer2_base base address for reference picture index2 base address for reference picture index2 (the address should be 128bit align)
3	RW	0x0	sw_ref2_colmv_use_flag sw_ref2_colmv_use_flag sw_ref2_colmv_use_flag
2	RW	0x0	sw_ref2_botfield_used ref2 bottom field is used ref2 bottom field is used
1	RW	0x0	sw_ref2_topfield_used ref2 topfield is used ref2 topfield is used
0	RW	0x0	sw_ref2_field reference 2 picture field flag 1'b0: frame 1'b1: field

rkvdec_swreg12_vp9_refergolden_base
Address: Operational Base + offset (0x0030)
base address for golden frame

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_vp9golden_base base address for golden frame base address for golden (the address should be 128bit align)
3:0	RO	0x0	reserved

rkvdec_swreg13_hevc_refer3_base
Address: Operational Base + offset (0x0034)
base address for reference picture index 3

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer3_base base address for reference picture index 3 base address for reference picture index 3 (the address should be 128bit align)
3	RO	0x0	reserved

Bit	Attr	Reset Value	Description
2:0	RW	0x0	sw_ref_valid_12_14 valid flag for picture index 12~14 valid flag for picture index 12~14

rkvdec_swreg13_h264_refer3_base
Address: Operational Base + offset (0x0034)
base address for reference picture index 3

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer3_base base address for reference picture index3 base address for reference picture index3 (the address should be 128bit align)
3	RW	0x0	sw_ref3_colmv_use_flag sw_ref3_colmv_use_flag sw_ref3_colmv_use_flag
2	RW	0x0	sw_ref3_botfield_used ref3 bottom field is used ref3 bottom field is used
1	RW	0x0	sw_ref3_topfield_used ref3 topfield is used ref3 topfield is used
0	RW	0x0	sw_ref3_field reference 3 picture field flag 1'b0: frame 1'b1: field

rkvdec_swreg13_vp9_referalfter_base
Address: Operational Base + offset (0x0034)
base address for referalfter frame

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_vp9alfter_base base address for alfter frame base address for alfter (the address should be 128bit align)
3:0	RO	0x0	reserved

rkvdec_swreg14_hevc_refer4_base
Address: Operational Base + offset (0x0038)
base address for reference picture index 4

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer4_base base address for reference picture index 4 base address for reference picture index 4(the address should be 128bit align)
3:0	RO	0x0	reserved

rkvdec_swreg14_h264_refer4_base
Address: Operational Base + offset (0x0038)
base address for reference picture index 4

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer4_base base address for reference picture index4 base address for reference picture index4 (the address should be 128bit align)
3	RW	0x0	sw_ref4_colmv_use_flag sw_ref4_colmv_use_flag sw_ref4_colmv_use_flag
2	RW	0x0	sw_ref4_botfield_used ref4 bottom field is used ref4 bottom field is used
1	RW	0x0	sw_ref4_topfield_used ref4 topfield is used ref4 topfield is used
0	RW	0x0	sw_ref4_field reference 4 picture field flag 1'b0: frame 1'b1: field

rkvdec_swreg14_vp9count_base
Address: Operational Base + offset (0x0038)
vp9 count base addr

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	sw_vp9count_base vp9 count base addr vp9 count base addr
2:0	RO	0x0	reserved

rkvdec_swreg15_h264_refer5_base
Address: Operational Base + offset (0x003c)
base address for reference picture index 5

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer5_base base address for reference picture index5 base address for reference picture index5 (the address should be 128bit align)
3	RW	0x0	sw_ref5_colmv_use_flag sw_ref5_colmv_use_flag sw_ref5_colmv_use_flag
2	RW	0x0	sw_ref5_botfield_used ref5 bottom field is used ref5 bottom field is used

Bit	Attr	Reset Value	Description
1	RW	0x0	sw_ref5_topfield_used ref5 topfield is used ref5 topfield is used
0	RW	0x0	sw_ref5_field reference 5 picture field flag 1'b0: frame 1'b1: field

rkvdec_swreg15_vp9_segidlast_base
Address: Operational Base + offset (0x003c)
base address for last frame segment id

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_vp9segidlast_base base address for vp9 last frame segment id base address for vp9 last frame segment id (the address should be 128bit align)
3:0	RO	0x0	reserved

rkvdec_swreg15_hevc_refer5_base
Address: Operational Base + offset (0x003c)
base address for reference picture index 5

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer5_base base address for reference picture index 5 base address for reference picture index 5(the address should be 128bit align)
3:0	RO	0x0	reserved

rkvdec_swreg16_h264_refer6_base
Address: Operational Base + offset (0x0040)
base address for reference picture index 6

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer6_base base address for reference picture index6 base address for reference picture index6 (the address should be 128bit align)
3	RW	0x0	sw_ref6_colmv_use_flag sw_ref6_colmv_use_flag sw_ref6_colmv_use_flag
2	RW	0x0	sw_ref6_botfield_used ref6 botfield is used ref6 botfield is used
1	RW	0x0	sw_ref6_topfield_used ref6 topfield is used ref6 topfield is used

Bit	Attr	Reset Value	Description
0	RW	0x0	sw_ref6_field reference 6 picture field flag 1'b0: frame 1'b1: field

rkvdec_swreg16_vp9_segidcur_base
Address: Operational Base + offset (0x0040)
base address for cur frame segment id

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_vp9segidcur_base base address for vp9 cur frame segment id base address for vp9 cur frame segment id (the address should be 128bit align)
3:0	RO	0x0	reserved

rkvdec_swreg16_hevc_refer6_base
Address: Operational Base + offset (0x0040)
base address for reference picture index 6

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer6_base base address for reference picture index 6 base address for reference picture index 6(the address should be 128bit align)
3:0	RO	0x0	reserved

rkvdec_swreg17_h264_refer7_base
Address: Operational Base + offset (0x0044)
base address for reference picture index 7

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer7_base base address for reference picture index7 base address for reference picture index7 (the address should be 128bit align)
3	RW	0x0	sw_ref7_colmv_use_flag sw_ref7_colmv_use_flag sw_ref7_colmv_use_flag
2	RW	0x0	sw_ref7_botfield_used ref7 bottom field is used ref7 bottom field is used
1	RW	0x0	sw_ref7_topfield_used ref7 topfield is used ref7 topfield is used

Bit	Attr	Reset Value	Description
0	RW	0x0	sw_ref7_field reference 7 picture field flag 1'b0: frame 1'b1: field

rkvdec_swreg17_vp9_frame_size_last
Address: Operational Base + offset (0x0044)
vp9 last frame size

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_frameheight_last last frame frame_size_height last frame frame_size_height
15:0	RW	0x0000	sw_framewidth_last last frame frame_size_width last frame frame_size_width

rkvdec_swreg17_hevc_refer7_base
Address: Operational Base + offset (0x0044)
base address for reference picture index 7

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer7_base base address for reference picture index 7 base address for reference picture index 7(the address should be 128bit align)
3:0	RO	0x0	reserved

rkvdec_swreg18_h264_refer8_base
Address: Operational Base + offset (0x0048)
base address for reference picture index 8

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer8_base base address for reference picture index8 base address for reference picture index8 (the address should be 128bit align)
3	RW	0x0	sw_ref8_colmv_use_flag sw_ref8_colmv_use_flag sw_ref8_colmv_use_flag
2	RW	0x0	sw_ref8_botfield_used ref8 bottom field is used ref8 bottom field is used
1	RW	0x0	sw_ref8_topfiled_used ref8 topfield is used ref8 topfield is used

Bit	Attr	Reset Value	Description
0	RW	0x0	sw_ref8_field reference 8 picture field flag 1'b0: frame 1'b1: field

rkvdec_swreg18_vp9_frame_size_golden
Address: Operational Base + offset (0x0048)
vp9 golden frame size

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_frameheight_golden golden frame_size_height golden frame_size_height
15:0	RW	0x0000	sw_framewidth_golden golden frame_size_width golden frame_size_width

rkvdec_swreg18_hevc_refer8_base
Address: Operational Base + offset (0x0048)
base address for reference picture index 8

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer8_base base address for reference picture index 8 base address for reference picture index 8(the address should be 128bit align)
3:0	RO	0x0	reserved

rkvdec_swreg19_h264_refer9_base
Address: Operational Base + offset (0x004c)
base address for reference picture index 9

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer9_base base address for reference picture index9 base address for reference picture index9 (the address should be 128bit align)
3	RW	0x0	sw_ref9_colmv_use_flag sw_ref9_colmv_use_flag sw_ref9_colmv_use_flag
2	RW	0x0	sw_ref9_botfield_used ref9 bottom field is used ref9 bottom field is used
1	RW	0x0	sw_ref9_topfield_used ref9 topfield is used ref9 topfield is used

Bit	Attr	Reset Value	Description
0	RW	0x0	sw_ref9_field reference 9 picture field flag 1'b0: frame 1'b1: field

rkvdec_swreg19_vp9_frame_size_altref
Address: Operational Base + offset (0x004c)
vp9 alfter frame size

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_frameheight_alfter alfter frame_size_height alfter frame_size_height
15:0	RW	0x0000	sw_framewidth_alfter alfter frame_size_width alfter frame_size_width

rkvdec_swreg19_hevc_refer9_base
Address: Operational Base + offset (0x004c)
base address for reference picture index 9

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer9_base base address for reference picture index 9 base address for reference picture index 9(the address should be 128bit align)
3:0	RO	0x0	reserved

rkvdec_swreg20_h264_refer10_base
Address: Operational Base + offset (0x0050)
base address for reference picture index 10

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer10_base base address for reference picture index10 base address for reference picture index10 (the address should be 128bit align)
3	RW	0x0	sw_ref10_colmv_use_flag sw_ref10_colmv_use_flag sw_ref10_colmv_use_flag
2	RW	0x0	sw_ref10_botfield_used ref10 bottom field is used ref10 bottom field is used
1	RW	0x0	sw_ref10_topfield_used ref10 topfield is used ref10 topfield is used

Bit	Attr	Reset Value	Description
0	RW	0x0	sw_ref10_field reference 10 picture field flag 1'b0: frame 1'b1: field

rkvdec_swreg20_vp9_segid_grp0
Address: Operational Base + offset (0x0050)
vp9 segid syntax grp0

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	RW	0x0	sw_vp9segid0_frame_skip_en frame skip feature enable frame skip feature enable
21:20	RW	0x0	sw_vp9segid0_referinfo specifies segment i's reference_info which is used to get ref_frame[0] specifies segment i's reference_info which is used to get ref_frame[0]
19	RW	0x0	sw_vp9segid0_referinfo_en frame reference info enable frame reference info enable
18:12	RW	0x00	sw_vp9segid0_frame_loopfilter_value frame loopfitler value specifies segment i's loopfilter_delta value which is used to calculate filter level
11	RW	0x0	sw_vp9segid0_frame_loopfitler_value_en frame_loopfilter_value feature enable frame_loopfilter_value feature enable
10:2	RW	0x000	sw_vp9segid0_frame_qp_delta frame qp delta specifies segment i's qp_delta value which is used to calculate y_dequant and uv_dequant
1	RW	0x0	sw_vp9segid0_frame_qp_delta_en frame_qp_delta feature enable frame_qp_delta feature enable
0	RW	0x0	sw_vp9segid_abs_delta abs delta used to decide quant and loopfilter param

rkvdec_swreg20_hevc_refer10_base
Address: Operational Base + offset (0x0050)
base address for reference picture index 10

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer10_base base address for reference picture index 10 base address for reference picture index 10(the address should be 128bit align)
3:0	RO	0x0	reserved

rkvdec_swreg21_h264_refer11_base
Address: Operational Base + offset (0x0054)
base address for reference picture index 11

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer11_base base address for reference picture index11 base address for reference picture index11 (the address should be 128bit align)
3	RW	0x0	sw_ref11_colmv_use_flag sw_ref11_colmv_use_flag sw_ref11_colmv_use_flag
2	RW	0x0	sw_ref11_botfield_used ref11 bottom field is used ref11 bottom field is used
1	RW	0x0	sw_ref11_topfield_used ref11 topfield is used ref11 topfield is used
0	RW	0x0	sw_ref11_field reference 11 picture field flag 1'b0: frame 1'b1: field

rkvdec_swreg21_vp9_segid_grp1
Address: Operational Base + offset (0x0054)
vp9 segid syntax grp1

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	RW	0x0	sw_vp9segid1_frame_skip_en frame skip feature enable frame skip feature enable
21:20	RW	0x0	sw_vp9segid1_referinfo specifies segment i's reference_info which is used to get ref_frame[0] specifies segment i's reference_info which is used to get ref_frame[0]
19	RW	0x0	sw_vp9segid1_referinfo_en frame reference info enable frame reference info enable

Bit	Attr	Reset Value	Description
18:12	RW	0x00	sw_vp9segid1_frame_loopfilter_value frame loopfitler value specifies segment i's loopfilter_delta value which is used to calculate filter level
11	RW	0x0	sw_vp9segid1_frame_loopfitler_value_en frame_loopfilter_value feature enable frame_loopfilter_value feature enable
10:2	RW	0x000	sw_vp9segid1_frame_qp_delta frame qp delta specifies segment i's qp_delta value which is used to calculate y_dequant and uv_dequant
1	RW	0x0	sw_vp9segid1_frame_qp_delta_en frame_qp_delta feature enable frame_qp_delta feature enable
0	RO	0x0	reserved

rkvdec_swreg21_hevc_refer11_base
Address: Operational Base + offset (0x0054)
base address for reference picture index 11

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer11_base base address for reference picture index 11 base address for reference picture index 11(the address should be 128bit align)
3:0	RO	0x0	reserved

rkvdec_swreg22_h264_refer12_base
Address: Operational Base + offset (0x0058)
base address for reference picture index 12

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer12_base base address for reference picture index12 base address for reference picture index12 (the address should be 128bit align)
3	RW	0x0	sw_ref12_colmv_use_flag sw_ref12_colmv_use_flag sw_ref12_colmv_use_flag
2	RW	0x0	sw_ref12_botfield_used ref12 bottom field is used ref12 bottom field is used
1	RW	0x0	sw_ref12_topfield_used ref12 topfield is used ref12 topfield is used

Bit	Attr	Reset Value	Description
0	RW	0x0	sw_ref12_field reference 12 picture field flag 1'b0: frame 1'b1: field

rkvdec_swreg22_vp9_segid_grp2
Address: Operational Base + offset (0x0058)
vp9 segid syntax grp2

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	RW	0x0	sw_vp9segid2_frame_skip_en frame skip feature enable frame skip feature enable
21:20	RW	0x0	sw_vp9segid2_referinfo specifies segment i's reference_info which is used to get ref_frame[0] specifies segment i's reference_info which is used to get ref_frame[0]
19	RW	0x0	sw_vp9segid2_referinfo_en frame reference info enable frame reference info enable
18:12	RW	0x00	sw_vp9segid2_frame_loopfilter_value frame loopfitler value specifies segment i's loopfilter_delta value which is used to calculate filter level
11	RW	0x0	sw_vp9segid2_frame_loopfitler_value_en frame_loopfilter_value feature enable frame_loopfilter_value feature enable
10:2	RW	0x000	sw_vp9segid2_frame_qp_delta frame qp delta specifies segment i's qp_delta value which is used to calculate y_dequant and uv_dequant
1	RW	0x0	sw_vp9segid2_frame_qp_delta_en frame_qp_delta feature enable frame_qp_delta feature enable
0	RO	0x0	reserved

rkvdec_swreg22_hevc_refer12_base
Address: Operational Base + offset (0x0058)
base address for reference picture index 12

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer12_base base address for reference picture index 12 base address for reference picture index 12(the address should be 128bit align)

Bit	Attr	Reset Value	Description
3:0	RO	0x0	reserved

rkvdec_swreg23_h264_refer13_base
Address: Operational Base + offset (0x005c)
base address for reference picture index 13

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer13_base base address for reference picture index13 base address for reference picture index13 (the address should be 128bit align)
3	RW	0x0	sw_ref13_colmv_use_flag sw_ref13_colmv_use_flag sw_ref13_colmv_use_flag
2	RW	0x0	sw_ref13_botfield_used ref13 bottom field is used ref13 bottom field is used
1	RW	0x0	sw_ref13_topfield_used ref13 topfield is used ref13 topfield is used
0	RW	0x0	sw_ref13_field reference 13 picture field flag 1'b0: frame 1'b1: field

rkvdec_swreg23_vp9_segid_grp3
Address: Operational Base + offset (0x005c)
vp9 segid syntax grp3

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	RW	0x0	sw_vp9segid3_frame_skip_en frame skip feature enable frame skip feature enable
21:20	RW	0x0	sw_vp9segid3_referinfo specifies segment i's reference_info which is used to get ref_frame[0] specifies segment i's reference_info which is used to get ref_frame[0]
19	RW	0x0	sw_vp9segid3_referinfo_en frame reference info enable frame reference info enable
18:12	RW	0x00	sw_vp9segid3_frame_loopfilter_value frame loopfitler value specifies segment i's loopfilter_delta value which is used to calculate filter level

Bit	Attr	Reset Value	Description
11	RW	0x0	sw_vp9segid3_frame_loopfitler_value_en frame_loopfilter_value feature enable frame_loopfilter_value feature enable
10:2	RW	0x000	sw_vp9segid3_frame_qp_delta frame qp delta specifies segment i's qp_delta value which is used to calculate y_dequant and uv_dequant
1	RW	0x0	sw_vp9segid3_frame_qp_delta_en frame_qp_delta feature enable frame_qp_delta feature enable
0	RO	0x0	reserved

rkvdec_swreg23_hevc_refer13_base
Address: Operational Base + offset (0x005c)
base address for reference picture index 13

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer13_base base address for reference picture index 13 base address for reference picture index 13(the address should be 128bit align)
3:0	RO	0x0	reserved

rkvdec_swreg24_h264_refer14_base
Address: Operational Base + offset (0x0060)
base address for reference picture index 14

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer14_base base address for reference picture index14 base address for reference picture index14 (the address should be 128bit align)
3	RW	0x0	sw_ref14_colmv_use_flag sw_ref14_colmv_use_flag sw_ref14_colmv_use_flag
2	RW	0x0	sw_ref14_botfield_used ref14 bottom field is used ref14 bottom field is used
1	RW	0x0	sw_ref14_topfield_used ref14 topfield is used ref14 topfield is used
0	RW	0x0	sw_ref14_field reference 14 picture field flag 1'b0: frame 1'b1: field

rkvdec_swreg24_vp9_segid_grp4
Address: Operational Base + offset (0x0060)
vp9 segid syntax grp4

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	RW	0x0	sw_vp9segid4_frame_skip_en frame skip feature enable frame skip feature enable
21:20	RW	0x0	sw_vp9segid4_referinfo specifies segment i's reference_info which is used to get ref_frame[0] specifies segment i's reference_info which is used to get ref_frame[0]
19	RW	0x0	sw_vp9segid4_referinfo_en frame reference info enable frame reference info enable
18:12	RW	0x00	sw_vp9segid4_frame_loopfilter_value frame loopfitler value specifies segment i's loopfilter_delta value which is used to calculate filter level
11	RW	0x0	sw_vp9segid4_frame_loopfitler_value_en frame_loopfilter_value feature enable frame_loopfilter_value feature enable
10:2	RW	0x000	sw_vp9segid4_frame_qp_delta frame qp delta specifies segment i's qp_delta value which is used to calculate y_dequant and uv_dequant
1	RW	0x0	sw_vp9segid4_frame_qp_delta_en frame_qp_delta feature enable frame_qp_delta feature enable
0	RO	0x0	reserved

rkvdec_swreg24_hevc_refer14_base
Address: Operational Base + offset (0x0060)
base address for reference picture index 14

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer14_base base address for reference picture index 14 base address for reference picture index 14(the address should be 128bit align)
3:0	RO	0x0	reserved

rkvdec_swreg25_vp9_segid_grp5
Address: Operational Base + offset (0x0064)
vp9 segid syntax grp5

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	RW	0x0	sw_vp9segid5_frame_skip_en frame skip feature enable frame skip feature enable
21:20	RW	0x0	sw_vp9segid5_referinfo specifies segment i's reference_info which is used to get ref_frame[0] specifies segment i's reference_info which is used to get ref_frame[0]
19	RW	0x0	sw_vp9segid5_referinfo_en frame reference info enable frame reference info enable
18:12	RW	0x00	sw_vp9segid5_frame_loopfilter_value frame loopfitler value specifies segment i's loopfilter_delta value which is used to calculate filter level
11	RW	0x0	sw_vp9segid5_frame_loopfitler_value_en frame_loopfilter_value feature enable frame_loopfilter_value feature enable
10:2	RW	0x000	sw_vp9segid5_frame_qp_delta frame qp delta specifies segment i's qp_delta value which is used to calculate y_dequant and uv_dequant
1	RW	0x0	sw_vp9segid5_frame_qp_delta_en frame_qp_delta feature enable frame_qp_delta feature enable
0	RO	0x0	reserved

rkvdec_swreg25_refer0_poc
Address: Operational Base + offset (0x0064)
the poc of reference picture index 0

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer0_poc the poc of reference picture index 0 the poc of reference picture index 0

rkvdec_swreg26_vp9_segid_grp6
Address: Operational Base + offset (0x0068)
vp9 segid syntax grp6

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	RW	0x0	sw_vp9segid6_frame_skip_en frame skip feature enable frame skip feature enable

Bit	Attr	Reset Value	Description
21:20	RW	0x0	sw_vp9segid6_referinfo specifies segment i's reference_info which is used to get ref_frame[0] specifies segment i's reference_info which is used to get ref_frame[0]
19	RW	0x0	sw_vp9segid6_referinfo_en frame reference info enable frame reference info enable
18:12	RW	0x00	sw_vp9segid6_frame_loopfilter_value frame loopfitler value specifies segment i's loopfilter_delta value which is used to calculate filter level
11	RW	0x0	sw_vp9segid6_frame_loopfitler_value_en frame_loopfilter_value feature enable frame_loopfilter_value feature enable
10:2	RW	0x000	sw_vp9segid6_frame_qp_delta frame qp delta specifies segment i's qp_delta value which is used to calculate y_dequant and uv_dequant
1	RW	0x0	sw_vp9segid6_frame_qp_delta_en frame_qp_delta feature enable frame_qp_delta feature enable
0	RO	0x0	reserved

rkvdec_swreg26_refer1_poc
Address: Operational Base + offset (0x0068)
the poc of reference picture index 1

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer1_poc the poc of reference picture index 1 the poc of reference picture index 1

rkvdec_swreg27_vp9_segid_grp7
Address: Operational Base + offset (0x006c)
vp9 segid syntax grp7

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	RW	0x0	sw_vp9segid7_frame_skip_en frame skip feature enable frame skip feature enable
21:20	RW	0x0	sw_vp9segid7_referinfo specifies segment i's reference_info which is used to get ref_frame[0] specifies segment i's reference_info which is used to get ref_frame[0]

Bit	Attr	Reset Value	Description
19	RW	0x0	sw_vp9segid7_referinfo_en frame reference info enable frame reference info enable
18:12	RW	0x00	sw_vp9segid7_frame_loopfilter_value frame loopfitler value specifies segment i's loopfilter_delta value which is used to calculate filter level
11	RW	0x0	sw_vp9segid7_frame_loopfitler_value_en frame_loopfilter_value feature enable frame_loopfilter_value feature enable
10:2	RW	0x000	sw_vp9segid7_frame_qp_delta frame qp delta specifies segment i's qp_delta value which is used to calculate y_dequant and uv_dequant
1	RW	0x0	sw_vp9segid7_frame_qp_delta_en frame_qp_delta feature enable frame_qp_delta feature enable
0	RO	0x0	reserved

rkvdec_swreg27_refer2_poc
Address: Operational Base + offset (0x006c)
the poc of reference picture index 2

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer2_poc the poc of reference picture index 2 the poc of reference picture index 2

rkvdec_swreg28_vp9_cprheader_config
Address: Operational Base + offset (0x0070)
vp9 compressed header config info

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4:3	RW	0x0	sw_vp9_frame_reference_mode frame_reference_mode frame_reference_mode specifies frame reference mode. SINGLE_REFERENCE = 0, COMPOUND_REFERENCE = 1, REFERENCE_MODE_SELECT = 2, REFERENCE_MODES = 3, When frame_reference_mode_flag0 is not present ,it equal to 0 by default. When frame_reference_mode_flag1 is not present ,it equal to 0 by default. frame_reference_mode = frame_reference_mode_flag0 == 0 ? frame_reference_mode_flag1 == 0 ? REFERENCE_MODE_SELECT : COMPOUND_REFERENCE) : SINGLE_REFERENCE

2:0	RW	0x0	sw_vp9_tx_mode
			tx_mode
			tx_mode specifies frame transform mode.
			ONLY_4X4 = 0, // only 4x4 transform used
			ALLOW_8X8 = 1, // allow block transform size up to 8x8
			ALLOW_16X16 = 2, // allow block transform size up to 16x16
			ALLOW_32X32 = 3, // allow block transform size up to 32x32
			TX_MODE_SELECT = 4, // transform specified for each block

rkvdec_swreg28_refer3_poc
Address: Operational Base + offset (0x0070)
the poc of reference picture index 3

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer3_poc the poc of reference picture index 3 the poc of reference picture index 3

rkvdec_swreg29_vp9_lref_scale
Address: Operational Base + offset (0x0074)
scaling factor for last reference picture

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_vp9_lref_ver_scale vertical scaling factor for last reference picture vertical scaling factor for last reference picture

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	sw_vp9_lref_hor_scale horizontal scaling factor for last reference picture horizontal scaling factor for last reference picture sw_vp9_lref_hor_scale = (last_ref_width / cur_width) * 0x4000

rkvdec_swreg29_refer4_poc
Address: Operational Base + offset (0x0074)
the poc of reference picture index 4

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer4_poc the poc of reference picture index 4 the poc of reference picture index 4

rkvdec_swreg30_vp9_gref_scale
Address: Operational Base + offset (0x0078)
scaling factor for golden reference picture

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_vp9_gref_ver_scale vertical scaling factor for golden reference picture vertical scaling factor for golden reference picture
15:0	RW	0x0000	sw_vp9_gref_hor_scale horizontal scaling factor for golden reference picture horizontal scaling factor for golden reference picture sw_vp9_gref_hor_scale = (golden_ref_width / cur_width) * 0x4000

rkvdec_swreg30_refer5_poc
Address: Operational Base + offset (0x0078)
the poc of reference picture index 5

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer5_poc the poc of reference picture index 5 the poc of reference picture index 5

rkvdec_swreg31_vp9_aref_scale
Address: Operational Base + offset (0x007c)
scaling factor for alfter reference picture

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_vp9_aref_ver_scale vertical scaling factor for alfter reference picture vertical scaling factor for alfter reference picture
15:0	RW	0x0000	sw_vp9_aref_hor_scale horizontal scaling factor for alfter reference picture horizontal scaling factor for alfter reference picture sw_vp9_gref_hor_scale = (alfter_ref_width / cur_width) * 0x4000

rkvdec_swreg31_refer6_poc
Address: Operational Base + offset (0x007c)
the poc of reference picture index 6

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer6_poc the poc of reference picture index 6 the poc of reference picture index 6

rkvdec_swreg32_vp9_ref_deltas_lastframe
Address: Operational Base + offset (0x0080)
vp9 ref deltas

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_vp9_ref_deltas_lastframe vp9 ref deltas vp9 ref deltas of lastframe, for cal loopfilter filter type use

rkvdec_swreg32_refer7_poc
Address: Operational Base + offset (0x0080)
the poc of reference picture index 7

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer7_poc the poc of reference picture index 7 the poc of reference picture index 7

rkvdec_swreg33_vp9_info_lastframe
Address: Operational Base + offset (0x0084)
vp9 info for lastframe

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:20	RW	0x0	sw_vp9_color_space_lastkeyframe vp9 last keyframe color_space vp9 last keyframe color_space
19	RW	0x0	sw_vp9_last_widhheight_eqcur last width and height equal cur last width and height equal cur frame
18	RW	0x0	sw_vp9_last_intra_only last frame intra only flag vp9 last frame intra only flag to give inter command use it is for last_dec_frame
17	RW	0x0	sw_vp9_last_show_frame last show frame flag for cal the flag use_prev_in_find_mv_refs which is to inter cmd it is for last_dec_frame

Bit	Attr	Reset Value	Description
16	RW	0x0	sw_segmentation_enable_lstframe segmentation_enable for last frame 1'b1:sw_segmentation_enable for last frame it is for last_dec_frame
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_vp9_mode_deltas_lastframe vp9 mode deltas vp9 mode deltas it is for last dec frame

rkvdec_swreg33_refer8_poc
Address: Operational Base + offset (0x0084)
the poc of reference picture index 8

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer8_poc the poc of reference picture index 8 the poc of reference picture index 8

rkvdec_swreg34_vp9_intercmd_base
Address: Operational Base + offset (0x0088)
inter cmd base addr

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_vp9_intercmd_base vp9 intercmd base addr vp9 inter command base addr, when sw_rlc_mode is 1'b1; when sw_dec_mode is VP9 and sw_rlc_mode is 1'b1, when read this register, after a frame is decoded ready or error (stream error , time out , bus error) , it is the end address of the intercmd
3:0	RO	0x0	reserved

rkvdec_swreg34_refer9_poc
Address: Operational Base + offset (0x0088)
the poc of reference picture index 9

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer9_poc the poc of reference picture index 9 the poc of reference picture index 9

rkvdec_swreg35_vp9_intercmd_num
Address: Operational Base + offset (0x008c)
vp9 intercmd num

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0x000000	sw_vp9_intercmd_num sw_vp9_intercmd_num when rlc_mode is 1'b1, for sw_vp9_intercmd_num it's unit is 128bit it count from 1

rkvdec_swreg35_refer10_poc
Address: Operational Base + offset (0x008c)
the poc of reference picture index 10

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer10_poc the poc of reference picture index 10 the poc of reference picture index 10

rkvdec_swreg36_vp9_lasttile_size
Address: Operational Base + offset (0x0090)
vp9 lasttile size

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:0	RW	0x000000	sw_vp9_lasttile_size vp9 last tile size vp9 last tile size ofr cur frame its unit is byte The real meaning the current frame size

rkvdec_swreg36_refer11_poc
Address: Operational Base + offset (0x0090)
the poc of reference picture index 11

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer11_poc the poc of reference picture index 11 the poc of reference picture index 11

rkvdec_swreg37_vp9_lastf_hor_virstride
Address: Operational Base + offset (0x0094)
Register0000 Abstract

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	sw_vp9_lastfuv_hor_virstride sw_vp9_lastfuv_hor_virstride vp9 last frame uv horizontal virstride
15:9	RO	0x0	reserved
8:0	RW	0x000	sw_vp9_lastfy_hor_virstride vp9 last frame y horizontal virstride vp9 last frame y horizontal virstride

rkvdec_swreg37_refer12_poc
Address: Operational Base + offset (0x0094)
the poc of reference picture index 12

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer12_poc the poc of reference picture index 12 the poc of reference picture index 12

rkvdec_swreg38_vp9_goldenf_hor_virstride
Address: Operational Base + offset (0x0098)
vp9 golden frame horizontal virstride

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	sw_vp9_goldenuv_hor_virstride vp9 goldenuv horizontal virstride vp9 golden uv horizontal virstirde
15:9	RO	0x0	reserved
8:0	RW	0x000	sw_vp9_goldenfy_hor_virstride sw_vp9_goldenfy_hor_virstirde vp9 golden frame y horizontal virstride

rkvdec_swreg38_refer13_poc
Address: Operational Base + offset (0x0098)
the poc of reference picture index 13

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer13_poc the poc of reference picture index 13 the poc of reference picture index 13

rkvdec_swreg39_vp9_altreff_hor_virstride
Address: Operational Base + offset (0x009c)
vp9 altref frame horizontal virstride

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	sw_vp9_altreffuv_hor_virstride vp9 altreffuv horizontal virstride vp9 altreff uv horizontal virstirde
15:9	RO	0x0	reserved
8:0	RW	0x000	sw_vp9_altreffy_hor_virstride sw_vp9_altreffy_hor_virstirde vp9 altref frame y horizontal virstride

rkvdec_swreg39_refer14_poc
Address: Operational Base + offset (0x009c)
the poc of reference picture index 14

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer14_poc the poc of reference picture index 14 the poc of reference picture index 14

rkvdec_swreg40_cur_poc
Address: Operational Base + offset (0x00a0)
the poc of cur picture

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_cur_poc the poc of the cur picture the poc of the cur picture for H264, it may be cur frame poc or cur top field poc

rkvdec_swreg41_rlcwrite_base
Address: Operational Base + offset (0x00a4)
the base address or rlcwrite base addr

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	sw_rlcwrite_base the base address of rlcwrite the base address of rlcwrite(the address should 64bit align) cabac output write to this rlcwrite base address when sw_rlc_mode_direct_write in swreg2_sysctrl is valid
2:0	RO	0x0	reserved

rkvdec_swreg42_pps_base
Address: Operational Base + offset (0x00a8)
the base address of pps

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_pps_base the base address of pps the base address of pps (the address should 128bit align) it is for storing sps(sequence parameter set) and pps(picture parameter set)
3:0	RO	0x0	reserved

rkvdec_swreg43_rps_base
Address: Operational Base + offset (0x00ac)
the base address of rps

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_rps_base rps base address rps(reference picture set) base address (the address should 128bit align)
3:0	RO	0x0	reserved

rkvdec_swreg44_strmd_error_en
Address: Operational Base + offset (0x00b0)
cabac error enable config

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_strmd_error_e strmd error enable regs strmd error enable regs in HEVC,it is called sw_cabac_error_e for VP9, it use sw_strmd_error_e[3:0] sw_strmd_error_e[0] is for sw_vp9_tilesize_error sw_strmd_error_e[1] is for sw_vp9_segskip_error sw_strmd_error_e[2] is for sw_vp9_error_init_error sw_strmd_error_e[3] is for sw_vp9_uncpr sw_strmd_error_e[4] is for sw_vp9_refscale_erro, sw_vp9_refscale_erro now is no use

rkvdec_swreg45_strmd_error_status
Address: Operational Base + offset (0x00b4)
cabac error status

Bit	Attr	Reset Value	Description
31:28	RW	0x0	sw_colmv_error_ref_picidx colmv error ref picidx when sw_colmv_ref_error_sta is 1'b1, these bits are used for tell which dpb frame is invalid but is read by inter module it is for H264 and HEVC
27:0	RW	0x0000000	sw_strmd_error_status cabac error status strmd error status in HEVC & H264, it is called cabac error status

rkvdec_swreg45_vp9_error_info0
Address: Operational Base + offset (0x00b4)
vp9 error info

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	vp9_error_info0 vp9_error_info0 for vp9 16 tile cols, every cols contains 4bits vp9_error_info0[3:0] is for col 0 vp9_error_info0[1:0] is to tell tile_rows_cnt[1:0] vp9_error_info0[3:2] is to tell the error type 2'b00: no error 2'b01: tilesize error 2'b10: seg skip error 2'b11: ref scale error

rkvdec_swreg46_strmd_error_ctu

Address: Operational Base + offset (0x00b8)
strmd error ctu

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	sw_vp9_error_ctu0_en to tell whether is any error of vp9 1'b1: there is aleast a error in vp9 strmd now ,is no for use
23	RO	0x0	reserved
22:16	RW	0x40	sw_streamfifo_space2full stream fifo space to full It is for debug use, to tell the stream fifo space to full for HEVC , H264 and VP9
15:8	RW	0x00	sw_strmd_error_ctu_yoffset strmd error ctu yoffset strmd error ctu yoffset for HEVC , H264 and VP9 for VP9, it is the value of stsw_vp9_error_ctu0_y
7:0	RW	0x00	sw_strmd_error_ctu_xoffset strmd error ctu xoffset strmd error ctu xoffset for all HEVC and H264 and VP9 for vp9, it is the value of stsw_vp9_error_ctu0_x

rkvdec_swreg47_sao_ctu_position
Address: Operational Base + offset (0x00bc)
sao ctu position

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x000	sw_saowr_yoffset saowr y offset saowr y offset , its unit is 4 pixels
15:9	RO	0x0	reserved
8:0	RW	0x000	sw_saowr_xoffet saowr x address offset saowr x address offset, its unit is 128bit

rkvdec_swreg48_h264_refer15_base
Address: Operational Base + offset (0x00c0)
base address for reference picture index 15

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer15_base base address for reference picture index15 base address for reference picture index15 (the address should be 128bit align)

Bit	Attr	Reset Value	Description
3	RW	0x0	sw_ref15_colmv_use_flag sw_ref15_colmv_use_flag sw_ref15_colmv_use_flag
2	RW	0x0	sw_ref15_botfield_used ref15 bottom field is used ref15 bottom field is used
1	RW	0x0	sw_ref15_topfield_used ref15 topfield is used ref15 topfield is used
0	RW	0x0	sw_ref15_field reference 15 picture field flag 1'b0: frame 1'b1: field

rkvdec_swreg48_vp9_last_ystride
Address: Operational Base + offset (0x00c0)
last ref ystride

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	sw_vp9_lastfy_virstride last frame y virstride vp9 last frame y stride

rkvdec_swreg49_h264_refer15_poc
Address: Operational Base + offset (0x00c4)
the poc of reference picture index 15

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer15_poc the poc of reference picture index 15 the poc of reference picture index 15

rkvdec_swreg49_vp9_golden_ystride
Address: Operational Base + offset (0x00c4)
golden ref ystride

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	sw_vp9_goldeny_virstride golden frame y virstride vp9 golden frame y stride

rkvdec_swreg50_h264_refer16_poc
Address: Operational Base + offset (0x00c8)
the poc of reference picture index 16

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer16_poc the poc of reference picture index 16 the poc of reference picture index 16

rkvdec_swreg50_vp9_altrefy_ystride
Address: Operational Base + offset (0x00c8)
altref ref ystride

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	sw_vp9_altrefy_virstride altref frame y virstride vp9 altref frame y stride

rkvdec_swreg51_h264_refer17_poc
Address: Operational Base + offset (0x00cc)
the poc of reference picture index 17

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer17_poc the poc of reference picture index 17 the poc of reference picture index 17

rkvdec_swreg51_vp9_lastref_yuvstride
Address: Operational Base + offset (0x00cc)
vp9 lastref yuv stride

Bit	Attr	Reset Value	Description
31:21	RO	0x0	reserved
20:0	RW	0x000000	sw_vp9_lastref_yuv_virstride lastref frame yuv virstride vp9 lastref frame yuv vir stride

rkvdec_swreg52_vp9_refcolmv_base
Address: Operational Base + offset (0x00d0)
vp9 colmv ref base

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_vp9_refcolmv_base vp9 ref colmv base vp9 ref colmv base addr
3:0	RO	0x0	reserved

rkvdec_swreg52_h264_refer18_poc
Address: Operational Base + offset (0x00d0)
the poc of reference picture index 18

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer18_poc the poc of reference picture index 18 the poc of reference picture index 18

rkvdec_swreg53_h264_refer19_poc
Address: Operational Base + offset (0x00d4)
the poc of reference picture index 19

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer19_poc the poc of reference picture index 19 the poc of reference picture index 19

rkvdec_swreg54_h264_refer20_poc
Address: Operational Base + offset (0x00d8)
the poc of reference picture index 20

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer20_poc the poc of reference picture index 20 the poc of reference picture index 20

rkvdec_swreg55_h264_refer21_poc
Address: Operational Base + offset (0x00dc)
the poc of reference picture index 21

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer21_poc the poc of reference picture index 21 the poc of reference picture index 21

rkvdec_swreg56_h264_refer22_poc
Address: Operational Base + offset (0x00e0)
the poc of reference picture index 22

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer22_poc the poc of reference picture index 22 the poc of reference picture index 22

rkvdec_swreg57_h264_refer23_poc
Address: Operational Base + offset (0x00e4)
the poc of reference picture index 23

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer23_poc the poc of reference picture index 23 the poc of reference picture index 23

rkvdec_swreg58_h264_refer24_poc
Address: Operational Base + offset (0x00e8)
the poc of reference picture index 24

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer24_poc the poc of reference picture index 24 the poc of reference picture index 24

rkvdec_swreg59_h264_refer25_poc
Address: Operational Base + offset (0x00ec)
the poc of reference picture index 25

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer25_poc the poc of reference picture index 25 the poc of reference picture index 25

rkvdec_swreg60_h264_refer26_poc
Address: Operational Base + offset (0x00f0)
the poc of reference picture index 26

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer26_poc the poc of reference picture index 26 the poc of reference picture index 26

rkvdec_swreg61_h264_refer27_poc
Address: Operational Base + offset (0x00f4)
the poc of reference picture index 27

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer27_poc the poc of reference picture index 27 the poc of reference picture index 27

rkvdec_swreg62_h264_refer28_poc
Address: Operational Base + offset (0x00f8)
the poc of reference picture index 28

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer28_poc the poc of reference picture index 28 the poc of reference picture index 28

rkvdec_swreg63_h264_refer29_poc
Address: Operational Base + offset (0x00fc)
the poc of reference picture index 29

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer29_poc the poc of reference picture index 29 the poc of reference picture index 29

rkvdec_swreg64_performance_cycle
Address: Operational Base + offset (0x0100)
hevc performance cycle

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_performance_cycle hevc running cycle hevc running cycle if just want to analys a frame performance cycle, should set the register 0 before start a frame

rkvdec_swreg65_axi_ddr_rdata
Address: Operational Base + offset (0x0104)
axi ddr read data num

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_axi_ddr_rdata axi ddr rdata num axi ddr rdata num, the unit is byte

rkvdec_swreg66_axi_ddr_wdata
Address: Operational Base + offset (0x0108)
axi ddr write data number

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_axi_ddr_wdata hevc write data byte num hevc write data byte num

rkvdec_swreg68_performance_sel
Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved

Bit	Attr	Reset Value	Description
21:16	RW	0x00	perf_cnt2_sel Field0000 Abstract 0 : don't work; 1 : cycles counter for cabac in buffer empty; 2 : cycles counter for cabac in buffer full; 3 : cycles counter for cabac out buffer empty; 4 : cycles counter for cabac out buffer full; 5 : cycles counter for transd input data ready; 6 : cycles counter for transd write data to recon allow; 7 : cycles counter for dec2transd cmd empty; 8 : cycles counter for dec2transd cmd full; 9 : cycles counter for transd2dblk bs fifo empty; 10: cycles counter for transd2dblk bs fifo full; 11: cycles counter for dec2intra cmd fifo empty; 12: cycles counter for dec2intra cmd fifo full; 13: cycles counter for mc2recon cmd fifo empty; 14: cycles counter for mc2recon cmd fifo full; 15: cycles counter for mc2recon data fifo empty; 16: cycles counter for mc2recon data fifo full; 17: cycles counter for recon2filter data write allow; 18: cycles counter for inter2busifd cmd fifo empty; 19: cycles counter for inter2busifd cmd fifo full; 20: cycles counter for busifd2mc data fifo empty; 21: cycles counter for busifd2mc data fifo full; 22: cycles counter for bus working status; 23: cycles counter for dec2inter cmd fifo empty; 24: cycles counter for dec2inter cmd fifo full; 25: cycles counter for inter2mc cmd fifo empty; 26: cycles counter for inter2mc cmd fifo full; 27: cycles counter for inter2dblk bs fifo empty; 28: cycles counter for inter2dblk bs fifo full; 29: cycles counter for colmv_rbuf_empty; 30: cycles counter for colmv_rbuf_full; 31: cycles counter for colmv_wbuf_empty; 32: cycles counter for colmv_wbuf_da_full; 33: cycles counter for dblk input data valid; 34: cycles counter for dblk can't write data to sao; 35: cycles counter for dec2loopfilter cmd fifo empty; 36: cycles counter for dec2loopfilter cmd fifo full; 37: cycles counter for sao input data valid; 38: cycles counter for busifd hold back sao write data; 39: cycles counter for sao output data valid; 40: counter for dec_ctrl read cmd num
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:8	RW	0x00	perf_cnt1_sel Field0000 Abstract 0 : don't work; 1 : cycles counter for cabac in buffer empty; 2 : cycles counter for cabac in buffer full; 3 : cycles counter for cabac out buffer empty; 4 : cycles counter for cabac out buffer full; 5 : cycles counter for transd input data ready; 6 : cycles counter for transd write data to recon allow; 7 : cycles counter for dec2transd cmd empty; 8 : cycles counter for dec2transd cmd full; 9 : cycles counter for transd2dblk bs fifo empty; 10: cycles counter for transd2dblk bs fifo full; 11: cycles counter for dec2intra cmd fifo empty; 12: cycles counter for dec2intra cmd fifo full; 13: cycles counter for mc2recon cmd fifo empty; 14: cycles counter for mc2recon cmd fifo full; 15: cycles counter for mc2recon data fifo empty; 16: cycles counter for mc2recon data fifo full; 17: cycles counter for recon2filter data write allow; 18: cycles counter for inter2busifd cmd fifo empty; 19: cycles counter for inter2busifd cmd fifo full; 20: cycles counter for busifd2mc data fifo empty; 21: cycles counter for busifd2mc data fifo full; 22: cycles counter for bus working status; 23: cycles counter for dec2inter cmd fifo empty; 24: cycles counter for dec2inter cmd fifo full; 25: cycles counter for inter2mc cmd fifo empty; 26: cycles counter for inter2mc cmd fifo full; 27: cycles counter for inter2dblk bs fifo empty; 28: cycles counter for inter2dblk bs fifo full; 29: cycles counter for colmv_rbuf_empty; 30: cycles counter for colmv_rbuf_full; 31: cycles counter for colmv_wbuf_empty; 32: cycles counter for colmv_wbuf_da_full; 33: cycles counter for dblk input data valid; 34: cycles counter for dblk can't write data to sao; 35: cycles counter for dec2loopfilter cmd fifo empty; 36: cycles counter for dec2loopfilter cmd fifo full; 37: cycles counter for sao input data valid; 38: cycles counter for busifd hold back sao write data; 39: cycles counter for sao output data valid; 40: counter for dec_ctrl read cmd num
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x00	perf_cnt0_sel sel counter0 to cal which signal 0 : don't work; 1 : cycles counter for cabac in buffer empty; 2 : cycles counter for cabac in buffer full; 3 : cycles counter for cabac out buffer empty; 4 : cycles counter for cabac out buffer full; 5 : cycles counter for transd input data ready; 6 : cycles counter for transd write data to recon allow; 7 : cycles counter for dec2transd cmd empty; 8 : cycles counter for dec2transd cmd full; 9 : cycles counter for transd2dblk bs fifo empty; 10: cycles counter for transd2dblk bs fifo full; 11: cycles counter for dec2intra cmd fifo empty; 12: cycles counter for dec2intra cmd fifo full; 13: cycles counter for mc2recon cmd fifo empty; 14: cycles counter for mc2recon cmd fifo full; 15: cycles counter for mc2recon data fifo empty; 16: cycles counter for mc2recon data fifo full; 17: cycles counter for recon2filter data write allow; 18: cycles counter for inter2busifd cmd fifo empty; 19: cycles counter for inter2busifd cmd fifo full; 20: cycles counter for busifd2mc data fifo empty; 21: cycles counter for busifd2mc data fifo full; 22: cycles counter for bus working status; 23: cycles counter for dec2inter cmd fifo empty; 24: cycles counter for dec2inter cmd fifo full; 25: cycles counter for inter2mc cmd fifo empty; 26: cycles counter for inter2mc cmd fifo full; 27: cycles counter for inter2dblk bs fifo empty; 28: cycles counter for inter2dblk bs fifo full; 29: cycles counter for colmv_rbuf_empty; 30: cycles counter for colmv_rbuf_full; 31: cycles counter for colmv_wbuf_empty; 32: cycles counter for colmv_wbuf_da_full; 33: cycles counter for dblk input data valid; 34: cycles counter for dblk can't write data to sao; 35: cycles counter for dec2loopfilter cmd fifo empty; 36: cycles counter for dec2loopfilter cmd fifo full; 37: cycles counter for sao input data valid; 38: cycles counter for busifd hold back sao write data; 39: cycles counter for sao output data valid; 40: counter for dec_ctrl read cmd num

rkvdec_swreg69_performance_cnt0
Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_cnt0 Field0000 Abstract Field0000 Description

rkvdec_swreg70_performance_cnt1
Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_cnt1

rkvdec_swreg71_performance_cnt2
Address: Operational Base + offset (0x011c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_cnt2 Field0000 Abstract Field0000 Description

rkvdec_swreg72_h264_refer30_poc
Address: Operational Base + offset (0x0120)
the poc of reference picture index 30

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer30_poc the poc of reference picture index 30 the poc of reference picture index 30

rkvdec_swreg73_h264_refer31_poc
Address: Operational Base + offset (0x0124)
the poc of reference picture index 31

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer31_poc the poc of reference picture index 31 the poc of reference picture index 31

rkvdec_swreg74_h264_cur_poc1
Address: Operational Base + offset (0x0128)
h264 cur poc for bottom filed

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_h264_cur_poc1 h264 cur poc for bottom field h264 cur poc for bottom field

rkvdec_swreg75_h264_errorinfo_base
Address: Operational Base + offset (0x012c)

h264 error info base addr

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	sw_errorinfo_base error info base addr error info base addr every slice contains 256 bits error info
2:0	RO	0x0	reserved

rkvdec_swreg76_h264_errorinfo_num
Address: Operational Base + offset (0x0130)
h264 error info num

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_error_packet_num error packet number error packet number
15	RW	0x0	sw_strmd_detect_error_flag strmd error detect flag streamd detect error flag
14	RO	0x0	reserved
13:0	RW	0x0000	sw_slicedec_num slice dec num h264 decoded num, the max slice num for H264 is 4096

rkvdec_swreg77_h264_error_e
Address: Operational Base + offset (0x0134)
h264 error enable high bits

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	sw_h264_error_en_highbits h264 error enable high bits h264 error enable bits

VDPU_SWREG0
Address: Operational Base + offset (0x0000)
axi control

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x01	sw_axi_id_wr AXI Write ID if you config 0,will modify as 1 by hw
15:8	RW	0x01	sw_axi_id_rd AXI Read ID if you config 0,will modify as 1 by hw
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5	RW	0x0	sw_scmd_off on-off for AXI Single Command Multiple Data on-off for AXI Single Command Multiple Data 0:on 1:off
4:0	RW	0x00	sw_max_burst_len the max burst length can be used by axi bus range : 1-16

VDPU_SWREG1
Address: Operational Base + offset (0x0004)
color coeff register

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	sw_coe_2st used in red color components calculate,used together with cr pix used for red color components calculate,used together with cr pix
19:10	RW	0x000	sw_coe_1st_1 used in all color components calculate,used together with y pix used for all color components calculate,used together with y pix
9:0	RW	0x000	sw_coe_1st_0 used for all color components calculate,used together with y pix

VDPU_SWREG2
Address: Operational Base + offset (0x0008)
color coeff register

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	sw_coe_5st used for blue components calculate,used together with cb pix
19:10	RW	0x000	sw_coe_4st used for green color components calculate,used together with cb pix
9:0	RW	0x000	sw_coe_3st used for green color components calculate,used together with cr pix

VDPU_SWREG3
Address: Operational Base + offset (0x000c)
color coeff register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	sw_coe_6st used for burightness adjust,used together with y pix

VDPU_SWREG4
Address: Operational Base + offset (0x0010)
scl ctrl register

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:22	RW	0x0	sw_scl_mode_vrt 0 = no scl 1 = up scl 2 = down scl
21:20	RW	0x0	sw_scl_mode_hrz to sellect scaling mode for Horizontal 0 = no scl 1 = up scl 2 = down scl
19:18	RO	0x0	reserved
17:0	RW	0x00000	sw_scl_fct_w scaling factor of width value = (output_width-1)/(input_width-1)

VDPU_SWREG5
Address: Operational Base + offset (0x0014)
scl ctrl register

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17:0	RW	0x00000	sw_scl_fct_h scaling factor of height value = (output_width-1)/(input_width-1)

VDPU_SWREG6
Address: Operational Base + offset (0x0018)
scl ctrl register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_scl_fct_h_inv scaling factor of height and cv value =(inputw-1) / (outputw-1)
15:0	RW	0x0000	sw_scl_fct_w_inv scaling factor of width and ch value =(inputw-1) / (outputw-1)

VDPU_SWREG7
Address: Operational Base + offset (0x001c)
Amount of pixels beyond border

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved

Bit	Attr	Reset Value	Description
26:16	RW	0x000	sw_pixnum_down_byd the Amount of vertical pixels beyond the down border Range : 0-dst_height
15:11	RO	0x0	reserved
10:0	RW	0x000	sw_pixnum_up_byd the Amount of vertical pixels beyond the up border Range : 0-dst_height

VDPU_SWREG8
Address: Operational Base + offset (0x0020)
Amount of pixels beyond border

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x000	sw_pixnum_right_byd the Amount of vertical pixels beyond the right border Range : 0~dst_width
15:11	RO	0x0	reserved
10:0	RW	0x000	sw_pixnum_left_byd the Amount of vertical pixels beyond the left border Range : 0~dst_width

VDPU_SWREG9
Address: Operational Base + offset (0x0024)
Rmask register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_mask_r color R/(alpha channnel) component 's bit mask

VDPU_SWREG10
Address: Operational Base + offset (0x0028)
Gmask register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_mask_g color G/(alpha channnel) component 's bit mask

VDPU_SWREG11
Address: Operational Base + offset (0x002c)
Bmask register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_mask_b color B/(alpha channnel) component 's bit mask

VDPU_SWREG12
Address: Operational Base + offset (0x0030)
PP input picture base address for Y bottom field

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_botfld_y_st_adr input bottom field pp start address for y component input bottom field pp start address for y component
1:0	RO	0x0	reserved

VDPU_SWREG13
Address: Operational Base + offset (0x0034)
PP input picture base for Ch bottom field

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_botfld_c_st_adr input bottom field pp start address for c component
1:0	RO	0x0	reserved

VDPU_SWREG14
Address: Operational Base + offset (0x0038)
coordinate used in macroblock crop

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	sw_mrmb_8pix_flag the most right unrotated MB of input picture just 8 lines pix data 829PP input picture width is not 16 pixels multiple. Only 8 pixels of the most right MB of the unrotated input picture is used for PP input.
28	RW	0x0	sw_mdmb_8pix_flag the most down unrotated MB of input picture just 8 rows pix data
27	RO	0x0	reserved
26:24	RW	0x0	sw_mbcrop_crdty_ext in order to support jpeg to extend coordinate y bits
23:16	RW	0x00	sw_mbcrop_crdty coordinate y used in macroblock crop
15:12	RO	0x0	reserved
11:9	RW	0x0	sw_mbcrop_crdtx_ext in order to support jpeg to extend bits
8:0	RW	0x000	sw_mbcrop_crdtx coordinate x used in macroblock crop

VDPU_SWREG15
Address: Operational Base + offset (0x003c)
range map register

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:8	RW	0x00	sw_rangemap_coef_c the value of chrominance component range map VC- 1:c range map value +9

Bit	Attr	Reset Value	Description
7:6	RO	0x0	reserved
5	RW	0x0	sw_yuv_conv_range to declaration the range of YCbCr when RGB conversion Y: 0:16~235 1:0~255 C: 0:16~240 1:0~255
4:0	RW	0x00	sw_rangemap_y the value of Y component range map VC- 1:y range map value +9

VDPU_SWREG16
Address: Operational Base + offset (0x0040)
total num of padded for RGB

Bit	Attr	Reset Value	Description
31:21	RO	0x0	reserved
20:16	RW	0x00	sw_padd_b the total num of padded in front of B componet
15:13	RO	0x0	reserved
12:8	RW	0x00	sw_padd_g the total num of padded in front of G componet the total num of padded in front of G componet
7:5	RO	0x0	reserved
4:0	RW	0x00	sw_padd_r the total num of padded in front of R componet

VDPU_SWREG17
Address: Operational Base + offset (0x0044)
hw support informan,read only

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	pp_deinterl_en on-off for pp deinterlance 0: off 1 : on
29	RO	0x0	pp_abled_en on-off for pp Alpha Blending 0: off 1 : on
28	RO	0x0	pp_work_en pp work allow flag 0 : off 1: on

Bit	Attr	Reset Value	Description
27:4	RO	0x0	reserved
3	RO	0x0	pp_outw_1920_en on-off for pp output width up to 1920 1st priority used
2	RO	0x0	pp_outw_1280_en on-off for pp output width up to 1280 2st priority used
1	RO	0x0	pp_outw_720_en on-off for pp output width up to 720 3st priority used
0	RO	0x0	pp_outw_352_en on-off for pp output width up to 352 4st priority used

VDPU_SWREG18
Address: Operational Base + offset (0x0048)
base address for reading post-processing input picture uminan

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_y_in_st_adr input y component start address The start address of topfield of the picture when data come from fields.extemal mode support only
1:0	RO	0x0	reserved

VDPU_SWREG19
Address: Operational Base + offset (0x004c)
Base address for reading post-processing input picture Cb/Ch

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_cb_in_st_adr input cb component start address The start address of topfield of the picture when data come from fields,extemal mode support only
1:0	RO	0x0	reserved

VDPU_SWREG20
Address: Operational Base + offset (0x0050)
input cr component address

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_cr_in_st_adr input cr component start address The start address of topfield of the picture when data come from fields,extemal mode support only
1:0	RO	0x0	reserved

VDPU_SWREG21
Address: Operational Base + offset (0x0054)
Base address for writing post-processed picture luminance/RGB

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_y_out_st_adr output y component start address also the start address of YUYV and RGB

VDPU_SWREG22
Address: Operational Base + offset (0x0058)
Base address for writing post-processed picture Ch

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_c_out_st_adr output chrominace component start address format is uvuvuv....

VDPU_SWREG23
Address: Operational Base + offset (0x005c)
Display width and PP input size extension register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_abled_st_adr_1st 1st alpha blending start address 1.valid when mask1 is used in alpha blending mode 2.Format of data the same as in PP input. 3.Amount of data is related to mask 1 size or ablend1_scanline informed with mask 1 size or with ablend1_scanline if ablend when crop flag valid

VDPU_SWREG24
Address: Operational Base + offset (0x0060)
alpha blending base address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_abled_st_adr_2st 2st alpha blending start address 1.valid when mask2 is used in alpha blending mode 2.Format of data the same as in PP input. 3.Amount of data is related to mask 2 size or ablend1_scanline informed with mask 1 size or with ablend1_scanline if ablend when crop flag valid

VDPU_SWREG25
Address: Operational Base + offset (0x0064)
ablend of pixels scanline

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

Bit	Attr	Reset Value	Description
28:16	RW	0x0000	sw_scanl_abld2 ablend 2 of pixels scanline corresponding function should be enabled
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_scanl_abld1 ablend 1 of pixels scanline corresponding function should be enabled

VDPU_SWREG26

Address: Operational Base + offset (0x0068)

x-coordinate of mask area 1 for Horizontal start pixel

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:12	RW	0x000	sw_end_coordx_ma1 the end x-coordinate of mask area 1 of Horizontal start pixel range:sw_st_coordx_ma1-dst width
11	RO	0x0	reserved
10:0	RW	0x000	sw_st_coordx_ma1 the start x-coordinate of mask area 1 of Horizontal start pixel

VDPU_SWREG27

Address: Operational Base + offset (0x006c)

y-coordinate of mask area 1 for Horizontal start pixel

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:12	RW	0x000	sw_end_coordy_ma1 the start y-coordinate of mask area 1 of Vertical start pixel range:sw_st_coordy_ma1~dst width
11	RO	0x0	reserved
10:0	RW	0x000	sw_st_coordy_ma1 the start y-coordinate of mask area 1 of Vertical start pixel

VDPU_SWREG28

Address: Operational Base + offset (0x0070)

x-coordinate of mask area 2 for Horizontal start pixel

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21:11	RW	0x000	sw_end_coordx_ma2 the end x-coordinate of mask area 2 of Horizontal start pixel range:sw_st_coordx_ma2~dst width
10:0	RW	0x000	sw_st_coordx_ma2 the start x-coordinate of mask area 2 of Horizontal start pixel

VDPU_SWREG29

Address: Operational Base + offset (0x0074)
y-coordinate of mask area 2 for Horizontal start pixel

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21:11	RW	0x000	sw_end_coordy_ma2 the start y-coordinate of mask area 2 of Vertical start pixel range:sw_st_coordy_ma2-dst width
10:0	RW	0x000	sw_st_coordy_ma2 the start y-coordinate of mask area 2 of Vertical start pixel

VDPU_SWREG30
Address: Operational Base + offset (0x0078)
register for deinterlace ctrl

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0000	sw_deinterl_edge the edge detect value of deinterlacing Edge detect value used for deinterlacing
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_deinterl_thr the threshold value of deinterlace

VDPU_SWREG31
Address: Operational Base + offset (0x007c)
contrast adjust threshold

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:8	RW	0x00	sw_cont_thr1 the threshold value 1 for contrast adjust
7:0	RW	0x00	sw_cont_thr0 the threshold value 0 for contrast adjust

VDPU_SWREG32
Address: Operational Base + offset (0x0080)
contrast adjust offset

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x000	sw_cont_offset1 the offset value 1 for contrast adjust
15:10	RO	0x0	reserved
9:0	RW	0x000	sw_cont_offset0 the offset value 0 for contrast adjust

VDPU_SWREG33
Address: Operational Base + offset (0x0084)
Synthesis configuration register post-processor (read only)

Bit	Attr	Reset Value	Description
31	RO	0x1	abld_crop_flag 0: unsupport crop,the exact image of the area being alpha blended should exist in the external memory 1: supprot crop,one picture in external memory which come from blended area can be cropped
30	RO	0x1	accut_out_exist_flag Pixel Accurate PP output mode exists flag PIP: 0 : use 8 pixels (width) or 2 pixels (height) steps to adjust Scaling and masks 1 : use 1 pixel for RGB and 2 pixels for subsampled chroma formats to adjust Scaling and masks
29	RO	0x1	tile_exist_flag the output of yuv422 tiled exist flag 0 : no exist 1 : exist
28	RO	0x1	dither_exist_flag Dithering exists flag 0 : no exist 1 : exist
27:26	RO	0x3	scl_perf_sel scaling perfomance sel 0 : without scaling 1 : low perfomance scaling 2 : high perfomance scaling 3 : high and fast perfomance scaling
25	RO	0x0	deinterl_exist_flag Deinterlacing exits flag 0 : no exist 1 : exist
24	RO	0x0	abld_exist_flag alpha blending exists flag 0 : no exist 1 : exist
23	RO	0x1	pp_in_buf_sel PP input buffering select 0 : output buffering is 1 MB 1 : output buffering is 4 MB
22:19	RO	0x0	reserved
18	RO	0x1	pp_endian_mode PP output endian mode select 0 : Endian mode supported except RGB 1 : Endian mode supported for all format

Bit	Attr	Reset Value	Description
17	RO	0x1	pp_out_buf_sel PP output buffering select 0 : output buffering is 1 unit 1 : output buffering is 4 unit
16	RO	0x1	ppd_exist_flag PPD exists flag 0 : no exist 1 : exist
15:14	RO	0x1	pp_tile_in_mode PD input tiled mode 0 : unsupport 1 : 8x4 tile be used
13:11	RO	0x0	reserved
10:0	RO	0x780	ppd_max_outw the max pixels width allow for pp output

VDPU_SWREG34
Address: Operational Base + offset (0x0088)
PP input pic size register

Bit	Attr	Reset Value	Description
31:29	RW	0x0	sw_pp_inh_ext PP input extended height in order to support jpeg
28:21	RW	0x00	sw_pp_inh the picture height of PP input with in macro blocks which can be cropped from a bigger picture when in the condtion of external mode
20:12	RW	0x000	sw_org_inw_ext the orginal width of pp input pic in MBS
11:9	RW	0x0	sw_pp_inw_ext PP input extended width in order to support jpeg
8:0	RW	0x000	sw_pp_inw the picture width of PP input with in macro blocks which can be cropped from a bigger picture when in the condtion of external mode

VDPU_SWREG35
Address: Operational Base + offset (0x008c)
PP output pic size register

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	sw_pp_outh_ext the extension height of pp output

Bit	Attr	Reset Value	Description
26:16	RW	0x000	sw_pp_outh (output width = 2*n (n=1,2,.....) || output width =(configurationed Pixel Accurate PP output configuration)*n) && (pp output width < 1920 || pp output width< 3*(sw_pp_inh-8))
15:12	RO	0x0	reserved
11	RW	0x0	sw_pp_outw_ext the extension width of pp output
10:0	RW	0x000	sw_pp_outw the pp output width (output width = 8*n (n=1,2,.....) || output width =(configurationed Pixel Accurate PP output configuration)*n) && (pp output width < 1920 || pp output width< 3*(sw_pp_inw-8))

VDPU_SWREG36
Address: Operational Base + offset (0x0090)
the dither mode for RGB

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:4	RW	0x0	sw_dither_mode_b the dither mode for B-component 0 : no use dithering 1 : 4-bits dither matrix be used 2 : 5-bits dither matrix be used 3 : 6-bits dither matrix be used
3:2	RW	0x0	sw_dither_mode_g the dither mode for G-component 0 : no use dithering 1 : 4-bits dither matrix be used 2 : 5-bits dither matrix be used 3 : 6-bits dither matrix be used
1:0	RW	0x0	sw_dither_mode_r the dither mode for R-component 0 : no use dithering 1 : 4-bits dither matrix be used 2 : 5-bits dither matrix be used 3 : 6-bits dither matrix be used

VDPU_SWREG37
Address: Operational Base + offset (0x0094)
PP input/output data format

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved

Bit	Attr	Reset Value	Description
26:24	RW	0x0	sw_pp_in_data_strc the data structure of pp input picture 0 : Top field 1 : Bottom field 2 : Interlaced field 3 : Interlaced frame 4 : Ripped top field 5 : Ripped bottom field if value=0/1/2,then should read every line from the base address,if value=3/4/5,then should read every second line from the base address
23:20	RO	0x0	reserved
19	RW	0x0	sw_pp_out_crbf_en output yuv422 or yuv420,cr before cb 0 : Y0CbY0Cr / CbY0CrY0 1 : Y0CrY0Cb / CrY0CbY0
18	RW	0x0	sw_pp_in_crbf_en in yuv422 or yuv420,cr before cb yuv422: 0 : Y0CbY0Cr / CbY0CrY0 1 : Y0CrY0Cb / CrY0CbY0 yuv420 semiplanar chrominance: 0 : CbCrCbCr 1:CrCbCrCb
17	RW	0x0	sw_pp_out_yuv_order the output yuv order 0 : Y0CbY0Cr / Y0CrY0Cb 1 : CbY0CrY0 / CrY0CbY0
16	RW	0x0	sw_pp_in_yuv_order the input yuv order 0 : Y0CbY0Cr / Y0CrY0Cb 1 : CbY0CrY0 / CrY0CbY0
15:12	RO	0x0	reserved
11	RW	0x0	sw_pp_out_wordsp the 32bit data swap for pp output data, it will be used in 64 bit environment 0 : no swapping 1 : swapping high and low 32bit data
10	RW	0x0	sw_pp_out_hfwordsp the half word swap inside of word 0:no swap 1:swap also be used as change pixel orders for 16 bit RGB,support all output format require pp_endian_mode=1

Bit	Attr	Reset Value	Description
9	RW	0x0	sw_pp_abld1_in_wordsp the 32bit data swap for the input 32bit data swap of Alpha blend for Alpha blend source 1 0 : no swapping 1 : swapping high and low 32bit data
8	RW	0x0	sw_pp_in_wordsp the 32bit data swap for pp input data, it will be used in 64 bit environment 0 : no swapping 1 : swapping high and low 32bit data
7:5	RO	0x0	reserved
4	RW	0x0	sw_rgb_pix_bits rga bits used sel 0: every word have only one rga pixel 1:every word have two rga pixel
3	RW	0x0	sw_pp_out_endian the endian mode of pp output for all yuv output endian mode or any data when pp_endian_mode=1 0 : big endian 1 : little endian if pp_endian_mode=0: 16 bit RGB: this bit used as pixel swapping bit 32 bit RGB: no used
2	RW	0x0	sw_pp_abld2_in_endian the endian select for input data of Alpha blend source 2 0: same with sw_pp_in_endian 1: same with sw_pp_abld1_in_endian '0' = Use PP in endian/swap definitions (sw_pp_in_endian, sw_pp_in_swap) '1' = Use Ablend source 1 endian/swap definitions
1	RW	0x0	sw_pp_abld1_in_endian the endian mode of input data for Alpha blend source 1 0 : big endian (0-1-2-3) 1 : little endian (3-2-1-0)
0	RW	0x0	sw_pp_in_endian the endian mode of pp input picture when PP in standalone mode this bit will no to be used when PP is running pipelined with the decoder 0 : big endian (0-1-2-3) 1 : little endian (3-2-1-0)

VDPU_SWREG38
Address: Operational Base + offset (0x0098)
PP input/output data format

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21:20	RW	0x0	sw_pp_in_tilmod the tiled mode of pp input data only support yuv420 input data,can be as pipeline or external mode 0 : Tiled mode not be actived 1 : 8x4 sized tiles be used 2,3 : reserved
19	RO	0x0	reserved
18:16	RW	0x0	sw_pp_in_fmt_ecp Escape PP in format be actived when sw_pp_in_fmt = 3'b111 0 : YCbCr 4:4:4 1 : YCbCr 4:1:1
15:14	RO	0x0	reserved
13:11	RW	0x0	sw_pp_out_fmt 0 : RGB 1 : YCbCr 4:2:0 ; planar (Not supported) 2 : YCbCr 4:2:2 ; planar (Not supported) 3 : YUYV 4:2:2 ; interleaved 4 : YCbCr 4:4:4 ; planar (Not supported) 5 : YCh 4:2:0 ; chrominance interleaved 6 : YCh 4:2:2 ; (Not supported) 7 : YCh 4:4:4 (Not supported)
10:8	RW	0x0	sw_pp_in_fmt the input format of pp input data 0 : YUYV 4:2:2 ; interleaved and it only supported in external mode 1 : YCbCr 4:2:0 ; the format of Semi-planar in linear raster-scan 2 : YCbCr 4:2:0 ; planar and it only supported in external mode 3 : YCbCr 4:0:0 ; it only supported in pipelined mode 4 : YCbCr 4:2:2 ; Semi-planar and it only supported only in pipelined mode 5 : YCbCr 4:2:0 ; Semi-planar in tiled format and it only supported in external mode 6 : YCbCr 4:4:0 ; Semi-planar and it only supported for jpeg in pipelined mode 7 : same as sw_pp_in_fmt_ecp
7:3	RO	0x0	reserved

Bit	Attr	Reset Value	Description
2:0	RW	0x0	sw_rot_mode Rotation mode 0 : rotation disabled 1 : rotate + 90 2 : rotate –90 3 : horizontal flip (mirror) 4 : vertical flip 5 : rotate 180

VDPU_SWREG39
Address: Operational Base + offset (0x009c)
Register0000 Abstract

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	sw_display_w the display width Max support 1920

VDPU_SWREG40
Address: Operational Base + offset (0x00a0)
pp int register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	sw_pp_bus_sts the Interrupt status bit for tell sw bus have some error
2	RW	0x0	sw_pp_rdy_sts the Interrupt status bit for tell sw processed a picture
1	RW	0x0	sw_pp_irq_dis the pp finish interrupt request diable flag 1 : use polling to see the interrupt 0 : use sw_pp_irq
0	RW	0x0	sw_pp_irq the pp finish interrupt request after sw query this interrupt,shoud write 0 to reset. this bit will no used in pipeline mode

VDPU_SWREG41
Address: Operational Base + offset (0x00a4)
enable ctrl flag

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	sw_pp_ahb_hlock_en the enable flag for AHB master HLOCK the service is locked to pp as long as it needs the bus

Bit	Attr	Reset Value	Description
27	RW	0x0	sw_rightwd_cross_en the enable flag for Right side overcross 0 : disable, 1 : enable
26	RW	0x0	sw_leftsd_cross_en the enable flag for Left side overcross 0 : disable, 1 : enable
25	RW	0x0	sw_downwd_cross_en the enable flag for Downward overcross 0 : disable, 1 : enable
24	RW	0x0	sw_upwd_cross_en the enable flag for Upward overcross 0 : disable, 1 : enable
23	RW	0x0	sw_mask2_abld_en the enable flag for Mask 2 alpha blending alpha blending for the output picture , only be supported when data format is RGB/YUYV422 Alpha blending read data from alpha blend 2 base address
22	RW	0x0	sw_mask1_abld_en the enable flag for Mask 1 alpha blending alpha blending for the output picture , only be supported when data format is RGB/YUYV422 Alpha blending read data from alpha blend 1 base address
21	RW	0x0	sw_mask2_en the enable flag for mask 2 0 : disable, 1 : enable
20	RW	0x0	sw_mask1_en the enable flag for mask 1 0 : disable, 1 : enable
19:17	RO	0x0	reserved
16	RW	0x0	sw_pp_discd_en the enable flag for PP data discard the burst length will be fix after sw_pp_discd_en=1,and extra read data will auto be discarded by HW
15:12	RO	0x0	reserved
11	RW	0x0	sw_pp_out_tiled_en the enable flag for pp output tiled mode only used in YCbYCr format . Tile size : 4x4 pixels.

Bit	Attr	Reset Value	Description
10	RW	0x0	sw_pp_fdscl_en the enable flag for fast downscaling 0 : disable 1 : enabled. it will inprove the performance but will decrease the quality of the pic
9	RW	0x0	sw_rangemap_c_en the enable flag for C component Range map
8	RW	0x0	sw_rangemap_y_en the enable flag for Y component Range map
7:5	RO	0x0	reserved
4	RW	0x0	sw_pp_pipl_en pp pipeline width Decoder enable 0 : disable, external mode 1 : enable, pipeline mode,Post-processing pipeline with decoder
3	RW	0x1	sw_pp_clkgate_en pp auto clock gating: default is 1 0 : don't auto gating 1 : audo gating PP dynamic clock gating enable: 1 = Clock is gated from PP structures that are not used 0 = Clock is running for all PP structures Note: Clock gating value can be changed only when PP is not enabled
2	RW	0x0	sw_deint_en Deinterlace enable flag the input data should be interlaced format
1	RW	0x0	sw_deint_bld_en on-off Blend for deinterlacing
0	RW	0x0	sw_pp_dec_st post-processing start flag after config other register,write 1 to start post-processing operation,and hw will reset to 0 after it decodered a picture should be under External mode.

VDPU_SWREG50
Address: Operational Base + offset (0x00c8)
video decoder ctrl register

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	sw_refbuf_pid the pic id for reference buffer The used reference picture ID for reference buffer usage

Bit	Attr	Reset Value	Description
24:13	RW	0x000	sw_refbuf_thrd Reference buffer threshold value Used shut down buffer
12	RW	0x0	sw_dec_tiled_lsb the enable for lsb tiled mode 0 : Tiled mode disable 1 : Tiled mode enabled for 8x4 tile size
11	RW	0x0	sw_adv_pref_dis disable for Advanced PREFETCH mode
10	RW	0x0	sw_dec_ascmd0_dis the disable for AXI Single Command Multiple Data0
9	RW	0x0	sw_skip_sel AVS format: 0 : skip mbs use special MB type 1 : avs skip mbs have the same skip run syntax element as h264
8	RW	0x0	sw_dblk_flt_dis the disable for current pic deblock filtering 1: disable 0: enable
7	RW	0x0	sw_dec_fixed_quant h.264: this bit is for the enable of multi view coding other format 0: it can be different inside pic for Quantization parameter 1: it is fixed for Quantization parameter
6:1	RW	0x00	sw_adtion_latency the additional latency for decoder master interface Can be used to slow down 8*sw_dec_latency cycles of IDLE between services,so if sw_dec_latency =0,that is no latency
0	RW	0x0	sw_dec_tiled_msb the enable for msb tiled mode 0 : Tiled mode disable 1 : Tiled mode enabled for 8x4 tile size

VDPU_SWREG51

Address: Operational Base + offset (0x00cc)

the stream length

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:25	RW	0x00	sw_qp_init_val the qp(quantization parameter)'s Initial value
24	RW	0x0	sw_strm_len_ext The extension bit of sw_strm_len

Bit	Attr	Reset Value	Description
23:0	RW	0x000000	sw_strm_len the stream data bytes number in input buffer. if the buffer size be given small than it required,hw will give an interrupt,and then you should config again,and the stream start address should be config also. VP6: one picture/slice of the picture's should be included in the input buffer H264/H263/MPEG*: one slice of the picture's should be included in the input buffer JPEG: 256bytes or onepicture should be included in the input buffer

VDPU_SWREG52
Address: Operational Base + offset (0x00d0)
error concealment case related

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:17	RW	0x0000	sw_adv_pref_thrd the threshold value for advanced prefetch when current MB num > this threshold value,then advanced mode will be closed
16:8	RW	0x000	sw_xdim_mbst the X dimension value for Start MB from SW it may be used in error concealment case
7:0	RW	0x00	sw_ydim_mbst the Y dimension value for Start MB from SW it may be used in error concealment case

VDPU_SWREG53
Address: Operational Base + offset (0x00d4)
decoder format

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x0	sw_dec_fmt_sel the dec format select 0 : H.264, 1 : MPEG-4, 2 : H.263, 3 : JPEG, 4 : reserved 5 : MPEG-2, 6 : MPEG-1, 7 : VP6, 8 : RV, 9 : VP7, 10 : reserved 11 : AVS, others : reserved

VDPU_SWREG54
Address: Operational Base + offset (0x00d8)
endian for input/output data

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x0	sw_dec_strendian_e the endian mode of stream data 0 : Big endian (0-1-2-3 order) 1 : Little endian (3-2-1-0 order)
4	RW	0x0	sw_dec_strm_wordsp the 32bit data swap for stream data it will be used in 64 bit environment 0 : no swapping 1 : swapping high and low 32bit data
3	RW	0x0	sw_dec_out_wordsp the 32bit data swap for dec output data, it will be used in 64 bit environment 0 : no swapping 1 : swapping high and low 32bit data
2	RW	0x0	sw_dec_in_wordsp the 32bit data swap for dec input data, it will be used in 64 bit environment 0 : no swapping 1 : swapping high and low 32bit data note : it no used for stream data

Bit	Attr	Reset Value	Description
1	RW	0x0	sw_dec_out_endian the endian mode of dec output Decoder output endian mode: 0 : Big endian (0-1-2-3 order) 1 : Little endian (3-2-1-0 order)
0	RW	0x0	sw_dec_in_endian the endian mode of dec input 0 : Big endian (0-1-2-3 order) 1 : Little endian (3-2-1-0 order) note : it no used for stream data

VDPU_SWREG55
Address: Operational Base + offset (0x00dc)
decoder int register

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13	RW	0x0	sw_timeout_det_sts the Interrupt status bit for tell us timeout detected AXI in IDLE status too long
12	RW	0x0	sw_error_det_sts the Interrupt status bit for tell us error detected Interrupt status bit input stream error. When high, an error is found in input data stream decoding. HW will self reset. (1,2,3,6,48,55,57)
11	RO	0x0	reserved
10	RW	0x0	sw_bslice_det_sts the Interrupt status bit for tell us B slice be detected
9	RW	0x0	sw_slice_det_sts the Interrupt status bit for tell us slice be decoded
8	RW	0x0	sw_aso_det_sts the Interrupt status bit for tell us ASO detectet ASO:Arbitrary Slice Ordering
7	RO	0x0	reserved
6	RW	0x0	sw_buf_emt_sts the Interrupt status bit for tell input buffer empty
5	RW	0x0	sw_pp_bus_sts the Interrupt status bit for tell sw bus have some error
4	RW	0x0	sw_dec_rdy_sts the Interrupt status bit for tell sw processed a picture
3:2	RO	0x0	reserved
1	RW	0x0	sw_dec_irq_dis the decoder finish interrupt request diable flag 1 : use polling to see the interrupt 0 : use sw_pp_irq

Bit	Attr	Reset Value	Description
0	RW	0x0	sw_dec_irq the decoder finish interrupt request after sw query this interrupt,shoud write 0 to reset.

VDPU_SWREG56
Address: Operational Base + offset (0x00e0)
axi ctrl for decoder

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23	RW	0x0	sw_axi_sel axi signals selected for encoder or decoder 0: auto sel for encoder or decoder 1: sel decoder (only used in the middle decoder frame to set bus_dec_en to 0)
22	RW	0x0	sw_dec_data_discd_en enable for Data discard the fixed burst length will be used ,and the more read datas will be auto discarded by hw
21	RW	0x1	sw_bus_pos_sel the parallel or serial mode for axi read and write 0:serial 1:parallel
20:16	RW	0x00	sw_dec_max_burlen the max burst length can be used by axi bus range : 1-16
15:8	RW	0x01	sw_dec_axi_id_wr AXI Write ID if you config 0,will modify as 1 by hw
7:0	RW	0x01	sw_dec_axi_id_rd AXI Read ID if you config 0/5,will modify as 1 by hw

VDPU_SWREG57
Address: Operational Base + offset (0x00e4)
enable flag for decoder

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_dec_timeout_mode dec timeout mode selset when 1'b0 , timeout cycle is 181'b1 when 1'b1, timeout cycle is 221'b1
30	RO	0x0	reserved

Bit	Attr	Reset Value	Description
29	RW	0x0	sw_cache_en cache enable 1'b1: cache enable 1'b0: cache disable when sw_cache_en is 1'b1, sw_pref_sigchan should also be 1'b1
28	RW	0x0	sw_pref_sigchan prefetch single channel enable 1'b1: prefetch single channel enable
27	RW	0x0	sw_intra_dbl3t In chroma dc intra prediction, when this bit is enable, there will 3 cycle enhance for every block
26	RW	0x0	sw_intra_dblspeed intra double speed enable Intra double speed enable
25	RW	0x0	sw_inter_dblspeed inter double speed enable Inter double speed enable
24:23	RO	0x0	reserved
22	RW	0x0	sw_st_code_exist existence flag for stream start code 0 : not exist 1 : exist
21	RW	0x0	sw_addit_ch_fmt_wen Enable for additional chrominance data format writing tiled mode should be disable,when this bit be used decoder writes chrominance: group of 8 pixels of Cb then corresponding 8 pixels of Cr Data is written to sw_dec_ch8pix_st_adr.
20	RW	0x0	sw_rlc_mode_en enable for RLC mode 0:decoder data come from bit stream(VLC mode),side information 1:decoder data come from RLC input data,only h.264 and MPEG4 sp be valid
19	RW	0x0	reserved
18	RW	0x0	sw_prog_jpeg_en enable flag for Progressive JPEG 0 : baseline JPEG 1 : progressive JPEG
17	RW	0x0	sw_curpic_code_sel the current picture coding mode select 0 : progressive 1 : interlaced

Bit	Attr	Reset Value	Description
16	RW	0x0	sw_curpic_stru_sel the current picture Structure selected 0 : frame structure, (that isMBAFF structured picture is interlaced) 1 : field structure
15	RW	0x0	sw_pic_type_sel1 pic type sel1 flag 0:desided by sw_pic_type_sel0 1: picture type is BI/D/B note: D is for mpeg1 B is for h264
14	RW	0x0	sw_pic_type_sel0 pic type sel0 flag should need sw_pic_type_sel1=0 0: Intra type (I) 1:Inter type (P)
13	RW	0x0	sw_pic_decfield_sel select which field will be decodered 0 : bottom field 1 : top field
12	RW	0x0	sw_fwd_refpic_mode_sel progressive and interlaced for coding mode used for forward reference picture: 0 : progressive 1 : interlaced the backward reference picture is the same as current picture
11	RW	0x0	sw_sorspa_en enable flag for Sorenson Sparc valid when sw_dec_fmt_sel= MPEG- 4 0 = disabled 1 = enable if enable,will use Sorenson escape coding to compatible stream for h.263
10	RW	0x0	sw_dmmv_wr_en enable flag for Direct mode motion vector write current picture 0:disable 1:enable this bit used in MPEG2 or VP6 is for the purpose error concealment case. this bit used in h264 is for the purpose write DPB case with the corresponding reference picture. this bit used in other decoder format is for the purpose writing to external memory starting from mv start address

Bit	Attr	Reset Value	Description
9	RW	0x0	sw_reftop_en enable flag for reference top field 0 = bottom field 1 = top field
8	RW	0x0	sw_first_reftop_en enable flag for FWD reference top field have been decoded first 0 : FWD reference bottom field 1 : FWD reference top field
7	RW	0x0	sw_sequ_mbaff_en the enable flag for Sequence includes MBAFF coded pictures 0:disable 1:enable
6	RW	0x0	sw_rd_cnt_tab_en the enable flag for reading Picture order count table read data from memory used 0:disable 1:enable (hw will read pic order counts)
5	RW	0x0	sw_timeout_sts_en the enable flag for Timeout interrupt 0:disable 1:enable (if hw can be working status too long,you will get an timeout interrupt)
4	RW	0x1	sw_dec_clkgate_en the enable flag for Decoder auto clock gating default hw will reset to 1 0:disable 1:enable
3	RO	0x0	reserved
2	RW	0x0	sw_dec_wr_extmem_dis disable flag for wiriting decoder output data to external memory 0 : enable 1:disable(no write to external memory)
1	RW	0x0	sw_refpic_buf2_en enable flag for Refer picture buffer 2 0:disable 1:enable (should : pic size > QVGA)
0	RW	0x0	sw_dec_st_work enable flag for decoder to start working hw will auto reset this be after a frame be decodered no matter it right or have some error

VDPU_SWREG58
Address: Operational Base + offset (0x00e8)
soft reset register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	W1C	0x0	sw_soft_rst the soft reset for decoder or pp or encoder write 1 to reset,and it will auto reset to 0 after one cycle

VDPU_SWREG59
Address: Operational Base + offset (0x00ec)
H264, MPEG4, VP6 Prediction filter tap

Bit	Attr	Reset Value	Description
31:22	RW	0x000	sw_pflt_set0_tap0 Prediction filter 0, tap 0
21:12	RW	0x000	sw_pflt_set0_tap1 Prediction filter set 0, tap 1
11:2	RW	0x000	sw_pflt_set0_tap2 Prediction filter set 0, tap 2
1:0	RO	0x0	reserved

VDPU_SWREG60
Address: Operational Base + offset (0x00f0)
additional chrominance address

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_addit_ch_st_adr the start address for additional chrominance data format The usage is enabled by sw_addit_ch_fmt_wen
1:0	RO	0x0	reserved

VDPU_SWREG61
Address: Operational Base + offset (0x00f4)
standard dependent tables start address

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_qtable_st_adr standard dependent tables start address JPEG : AC,DC, QP tables MPEG4/2 : QP table H.264 :various tables VP6/7/8 : stream decoding tables
1:0	RO	0x0	reserved

VDPU_SWREG62
Address: Operational Base + offset (0x00f8)
Direct mode motion vector write/read start address

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_dmmv_st_adr Direct mode motion vector write/read start address H264: Direct mode motion vector write/read start address Progressive JPEG: the start address for ACDC coefficient read/write If current round is for DC components : this start address is pointing to luminance AC component rounds: this start address is used for current type
1:0	RO	0x0	reserved

VDPU_SWREG63
Address: Operational Base + offset (0x00fc)
write decoder output picture or field start address

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_dec_out_st_adr write decoder output picture or field start address video: write decoder output picture or field start address JPEG snapshot: wirete decoder output luminance picture start address
1:0	RO	0x0	reserved

VDPU_SWREG64
Address: Operational Base + offset (0x0100)
rlc or vlc mode input data start addr

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_rlc_vlc_st_adr rlc or vlc mode input data start addr RLC mode: RLC data start address VLC mode: Stream start address HW return value of last_byte_address by this register to tell where stream has been read when you get some abnormality interrupt,may be used for debug VP7: DCT stream for MB rows 0,2n start address
1:0	RO	0x0	reserved

VDPU_SWREG65
Address: Operational Base + offset (0x0104)
refbufferd related

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_refbu_e 0 : disable 1 : enable
30:19	RW	0x000	sw_refbu_thr_level Reference buffer disable threshold value (cache miss amount). Used to buffer shut down (if more misses than allowed)
18:14	RW	0x00	sw_refbuf_picid the picture id for refference buffer
13	RW	0x0	sw_refbuf_idcal_e Enable for HW internal reference ID calculation If given threshold level is reached by any picture_id after first MB row, that picture_id is used for reference buffer fill for rest of the picture
12	RW	0x0	sw_refbuf_fildpar_mod_e the mode enable for Field parity mode enable. 0 : the result field of the evaluation be used 1 : the parity mode field be used
11:9	RO	0x0	reserved
8:0	RW	0x000	sw_refbuf_y_ofset the y offset for refbufferd if hw should compensate the global motion of the video for better buffer hit rate will use this coordinate

VDPU_SWREG66
Address: Operational Base + offset (0x0108)
ID register

Bit	Attr	Reset Value	Description
31:16	RO	0x6731	prod_id product number
15:12	RO	0x2	major_num
11:4	RO	0x68	minor_num
3	RO	0x1	ascii_id_en enable for ASCII product ID
2:0	RO	0x0	build_ver

VDPU_SWREG67
Address: Operational Base + offset (0x010c)
Synthesis configuration register decoder 1(read only)

Bit	Attr	Reset Value	Description
31	RO	0x1	jpeg_allow_flag JPEG sampling support 16Mpixel~67Mpixel be sampled and supported by 411 and 444

Bit	Attr	Reset Value	Description
30	RO	0x1	refbuf_allow_flag ref buffer support 0:no support 1:support
29	RO	0x0	reserved
28	RO	0x0	refbuf2_allow_flag refbuffer2 support
27:26	RO	0x1	rv_allow_flag
25	RO	0x0	rom_imp_type rom implementation type 0: from actual ROM units 1: from RTL
24	RO	0x1	vp7_allow_flag vp7 support
23	RO	0x1	reserved
22	RO	0x1	reserved
21:20	RO	0x1	mvc_allow_flag mvc support
19	RO	0x1	reserved
18:17	RO	0x1	tile_mode_sel tile mode support 0:no support 1: 8x4 support 2,3: no used
16:0	RO	0x0	reserved

VDPU_SWREG68
Address: Operational Base + offset (0x0110)
sum of partitions(read only)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	sw_refbuf_sum_top sum of the top partitions
15:0	RO	0x0000	sw_refbuf_sum_bot sum of the bottom partitions

VDPU_SWREG69
Address: Operational Base + offset (0x0114)
sum information (read only)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	sw_refbuf_sum_hit sum of the refbufferd hits of the picture
15:0	RO	0x0000	sw_luma_sum_intra sum of the luminance 8x8 intra partitons of the picture.

VDPU_SWREG70
Address: Operational Base + offset (0x0118)
sum of the decoded motion vector y-components(read only)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21:0	RO	0x000000	sw_ycomp_mv_sum sum of the decoded motion vector y-components

VDPU_SWREG71
Address: Operational Base + offset (0x011c)
information for read only register

Bit	Attr	Reset Value	Description
31	RO	0x1	dec_mpeg2_allow Decoding format support, for MPEG-2 / MPEG-1 0:no support 1:support
30:29	RO	0x0	reserved
28	RO	0x1	dec_jpeg_allow Decoding format support for JPEG 0:no support 1:support
27:26	RO	0x2	dec_mpeg4_allow Decoding format support for MPEG-4 / H.263 0 :not supported 1 :simple profile be supported 2 :advanced simple profile be supported
25:24	RO	0x3	dec_h264_allow h264 be support 0:no support 1:baseline profile be supported 2:high profile be supported
23	RO	0x1	dec_vp6_allow Decoding format support for VP6 0:no support 1:support
22	RO	0x0	dec_prog_jpeg_allow support for progressive jpeg 0:no support 1:support
21	RO	0x1	outbuf_sel output buffer selected 0 : 1MB buffer be used 1 : 4MB buffer be used
20	RO	0x1	refbuf_exist reference buffer support 0 : not supported 1 : support

Bit	Attr	Reset Value	Description
19:16	RO	0x5	dec_std_bus 0 : error 1 : AHB master, AHB slave 2 : OCP master, OCP slave 3 : AXI master, AXI slave 4 : AXI master, APB slave 5 : AXI master, AHB slave
15:14	RO	0x1	rtl_lan_sel 0: no used 1:vhdl 2:verilog
13:12	RO	0x2	bus_w 0 : error 1 : word bus 2 : double word bus 3 : quadruple word bus
11	RO	0x1	dec_srson_allow Decoding format support for Sorenson 0:no support 1:support
10:0	RO	0x780	sw_dec_max_allow_w the max width can be decoder

VDPU_SWREG72
Address: Operational Base + offset (0x0120)
debug0

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RO	0x00	debug_service debug_service signals this value[6:0]=service_wr[2:0], service_rd[3:0]
23:0	RO	0x0	reserved

VDPU_SWREG73
Address: Operational Base + offset (0x0124)
debug registers

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	debug_mv_req mvst_mv_req signal value
29	RO	0x0	debug_rlc_req prtr_res_y_req signal value
28	RO	0x0	debug_res_y_req prtr_res_y_req signal value
27	RO	0x0	debug_res_c_req

Bit	Attr	Reset Value	Description
26	RO	0x0	debug_strm_da_e
25	RO	0x0	debug_frm_rdy
24	RO	0x0	debug_flt_req
23	RO	0x0	debug_ref0_req
22	RO	0x0	debug_ref1_req
21	RO	0x0	reserved
20:0	RO	0x000000	debug_mb_cnt

VDPU_SWREG74
Address: Operational Base + offset (0x0128)
MV address for h264

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	h264_diff_mv_st_adr the Differential motion vector start address Differential motion vector base address used for h264 only it also reuse used as: [29:25] : 9st forward picid of inital reference pic list [24:20] : 8st forward picid of inital reference pic list [19:15] : 7st forward picid of inital reference pic list [14:10] : 6st forward picid of inital reference pic list [9:5] : 5st forward picid of inital reference pic list [4:0] : 4st forward picid of inital reference pic list
1:0	RO	0x0	reserved

VDPU_SWREG75
Address: Operational Base + offset (0x012c)
H.264 Intra prediction 4x4 mode start address

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	h264_pred4x4_st_adr H.264 Intra prediction 4x4 mode start address also be used as: [29:25] : 15st forward picid of inital reference pic list [24:20] : 14st forward picid of inital reference pic list [19:15] : 13st forward picid of inital reference pic list [14:10] : 12st forward picid of inital reference pic list [9:5] : 11st forward picid of inital reference pic list [4:0] : 10st forward picid of inital reference pic list
1:0	RO	0x0	reserved

VDPU_SWREG76
Address: Operational Base + offset (0x0130)
the number of referance pic

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	h264_num_ref_idx1 the number of referance pic index0
15:0	RW	0x0000	h264_num_ref_idx0 the number of referance pic index0

VDPU_SWREG77
Address: Operational Base + offset (0x0134)
the number of referance pic

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	h264_num_ref_idx3 the number of referance pic index3
15:0	RW	0x0000	h264_num_ref_idx2 the number of referance pic index2

VDPU_SWREG78
Address: Operational Base + offset (0x0138)
the number of referance pic

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	h264_num_ref_idx5 the number of referance pic index5
15:0	RW	0x0000	h264_num_ref_idx4 the number of referance pic index4

VDPU_SWREG79
Address: Operational Base + offset (0x013c)
the number of referance pic

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	h264_num_ref_idx7 the number of referance pic index7
15:0	RW	0x0000	h264_num_ref_idx6 the number of referance pic index6

VDPU_SWREG80
Address: Operational Base + offset (0x0140)
the number of referance pic

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	h264_num_ref_idx9 the number of referance pic index9
15:0	RW	0x0000	h264_num_ref_idx8 the number of referance pic index8

VDPU_SWREG81
Address: Operational Base + offset (0x0144)
the number of referance pic

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	h264_num_ref_idx11 the number of referance pic index11
15:0	RW	0x0000	h264_num_ref_idx10 the number of referance pic index10

VDPU_SWREG82
Address: Operational Base + offset (0x0148)
the number of referance pic

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	h264_num_ref_idx13 the number of referance pic index13
15:0	RW	0x0000	h264_num_ref_idx12 the number of referance pic index12

VDPU_SWREG83
Address: Operational Base + offset (0x014c)
the number of referance pic

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	h264_num_ref_idx15 the number of referance pic index15
15:0	RW	0x0000	h264_num_ref_idx14 the number of referance pic index14

VDPU_SWREG84
Address: Operational Base + offset (0x0150)
referance frame0 address for h264

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	h264_ref0_st_addr the start address of referance frame0
1	RW	0x0	h264_ref0_field_en the type Refer picture consist of 0 : frame 1 : field
0	RW	0x0	h264_ref0_closer_sel Which field is more closer to current picture 0 : bottom field be selected 1 : top field be selected

VDPU_SWREG85
Address: Operational Base + offset (0x0154)
referance frame1 address for h264

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	h264_ref1_st_addr the start address of referance frame1

Bit	Attr	Reset Value	Description
1	RW	0x0	h264_ref1_field_en the type Refer picture consist of 0 : frame 1 : field
0	RW	0x0	h264_ref1_closer_sel Which field is more closer to current picture 0 : bottom field be selected 1 : top field be selected

VDPU_SWREG86
Address: Operational Base + offset (0x0158)
referance frame2 address for h264

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	h264_ref2_st_addr the start address of referance frame2
1	RW	0x0	h264_ref2_field_en the type Refer picture consist of 0 : frame 1 : field
0	RW	0x0	h264_ref2_closer_sel Which field is more closer to current picture 0 : bottom field be selected 1 : top field be selected

VDPU_SWREG87
Address: Operational Base + offset (0x015c)
referance frame3 address for h264

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	h264_ref3_st_addr the start address of referance frame3
1	RW	0x0	h264_ref3_field_en the type Refer picture consist of 0 : frame 1 : field
0	RW	0x0	h264_ref3_closer_sel Which field is more closer to current picture 0 : bottom field be selected 1 : top field be selected

VDPU_SWREG88
Address: Operational Base + offset (0x0160)
referance frame4 address for h264

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	h264_ref4_st_addr the start address of referance frame4

Bit	Attr	Reset Value	Description
1	RW	0x0	h264_ref4_field_en the type Refer picture consist of 0 : frame 1 : field
0	RW	0x0	h264_ref4_closer_sel Which field is more closer to current picture 0 : bottom field be selected 1 : top field be selected

VDPU_SWREG89
Address: Operational Base + offset (0x0164)
referance frame5 address for h264

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	h264_ref5_st_addr the start address of referance frame5
1	RW	0x0	h264_ref5_field_en the type Refer picture consist of 0 : frame 1 : field
0	RW	0x0	h264_ref5_closer_sel Which field is more closer to current picture 0 : bottom field be selected 1 : top field be selected

VDPU_SWREG90
Address: Operational Base + offset (0x0168)
referance frame6 address for h264

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	h264_ref6_st_addr the start address of referance frame6
1	RW	0x0	h264_ref6_field_en the type Refer picture consist of 0 : frame 1 : field
0	RW	0x0	h264_ref6_closer_sel Which field is more closer to current picture 0 : bottom field be selected 1 : top field be selected

VDPU_SWREG91
Address: Operational Base + offset (0x016c)
referance frame7 address for h264

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	h264_ref7_st_addr the start address of referance frame7

Bit	Attr	Reset Value	Description
1	RW	0x0	h264_ref7_field_en the type Refer picture consist of 0 : frame 1 : field
0	RW	0x0	h264_ref7_closer_sel Which field is more closer to current picture 0 : bottom field be selected 1 : top field be selected

VDPU_SWREG92
Address: Operational Base + offset (0x0170)
referance frame8 address for h264

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	h264_ref8_st_addr the start address of referance frame8
1	RW	0x0	h264_ref8_field_en the type Refer picture consist of 0 : frame 1 : field
0	RW	0x0	h264_ref8_closer_sel Which field is more closer to current picture 0 : bottom field be selected 1 : top field be selected

VDPU_SWREG93
Address: Operational Base + offset (0x0174)
referance frame9 address for h264

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	h264_ref9_st_addr the start address of referance frame9
1	RW	0x0	h264_ref9_field_en the type Refer picture consist of 0 : frame 1 : field
0	RW	0x0	h264_ref9_closer_sel Which field is more closer to current picture 0 : bottom field be selected 1 : top field be selected

VDPU_SWREG94
Address: Operational Base + offset (0x0178)
referance frame10 address for h264

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	h264_ref10_st_addr the start address of referance frame10

Bit	Attr	Reset Value	Description
1	RW	0x0	h264_ref10_field_en the type Refer picture consist of 0 : frame 1 : field
0	RW	0x0	h264_ref10_closer_sel Which field is more closer to current picture 0 : bottom field be selected 1 : top field be selected

VDPU_SWREG95
Address: Operational Base + offset (0x017c)
referance frame11 address for h264

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	h264_ref11_st_addr the start address of referance frame11
1	RW	0x0	h264_ref11_field_en the type Refer picture consist of 0 : frame 1 : field
0	RW	0x0	h264_ref11_closer_sel Which field is more closer to current picture 0 : bottom field be selected 1 : top field be selected

VDPU_SWREG96
Address: Operational Base + offset (0x0180)
referance frame12 address for h264

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	h264_ref12_st_addr the start address of referance frame12
1	RW	0x0	h264_ref12_field_en the type Refer picture consist of 0 : frame 1 : field
0	RW	0x0	h264_ref12_closer_sel Which field is more closer to current picture 0 : bottom field be selected 1 : top field be selected

VDPU_SWREG97
Address: Operational Base + offset (0x0184)
referance frame13 address for h264

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	h264_ref13_st_addr the start address of referance frame13

Bit	Attr	Reset Value	Description
1	RW	0x0	h264_ref13_field_en the type Refer picture consist of 0 : frame 1 : field
0	RW	0x0	h264_ref13_closer_sel Which field is more closer to current picture 0 : bottom field be selected 1 : top field be selected

VDPU_SWREG98
Address: Operational Base + offset (0x0188)
referance frame14 address for h264

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	h264_ref14_st_addr the start address of referance frame14
1	RW	0x0	h264_ref14_field_en the type Refer picture consist of 0 : frame 1 : field
0	RW	0x0	h264_ref14_closer_sel Which field is more closer to current picture 0 : bottom field be selected 1 : top field be selected

VDPU_SWREG99
Address: Operational Base + offset (0x018c)
referance frame15 address for h264

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	h264_ref15_st_addr the start address of referance frame15
1	RW	0x0	h264_ref15_field_en the type Refer picture consist of 0 : frame 1 : field
0	RW	0x0	h264_ref15_closer_sel Which field is more closer to current picture 0 : bottom field be selected 1 : top field be selected

VDPU_SWREG100
Address: Operational Base + offset (0x0190)
initial reference picture list related

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

Bit	Attr	Reset Value	Description
29:25	RW	0x00	h264_init_reflist_df5 5st initial reference picture list for direct forward picid used for h264
24:20	RW	0x00	h264_init_reflist_df4 4st initial reference picture list for direct forward picid used for h264
19:15	RW	0x00	h264_init_reflist_df3 3st initial reference picture list for direct forward picid used for h264
14:10	RW	0x00	h264_init_reflist_df2 2st initial reference picture list for direct forward picid used for h264
9:5	RW	0x00	h264_init_reflist_df1 1st initial reference picture list for direct forward picid used for h264
4:0	RW	0x00	h264_init_reflist_df0 0st initial reference picture list for direct forward picid used for h264

VDPU_SWREG101
Address: Operational Base + offset (0x0194)
initial reference picture list related

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	h264_init_reflist_df11 11st initial reference picture list for direct forward picid used for h264
24:20	RW	0x00	h264_init_reflist_df10 10st initial reference picture list for direct forward picid used for h264
19:15	RW	0x00	h264_init_reflist_df9 9st initial reference picture list for direct forward picid used for h264
14:10	RW	0x00	h264_init_reflist_df8 8st initial reference picture list for direct forward picid used for h264
9:5	RW	0x00	h264_init_reflist_df7 7st initial reference picture list for direct forward picid used for h264
4:0	RW	0x00	h264_init_reflist_df6 6st initial reference picture list for direct forward picid used for h264

VDPU_SWREG102
Address: Operational Base + offset (0x0198)

initial reference picture list related

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:15	RW	0x00	h264_init_reflist_df15 15st initial reference picture list for direct forward picid used for h264
14:10	RW	0x00	h264_init_reflist_df14 14st initial reference picture list for direct forward picid used for h264
9:5	RW	0x00	h264_init_reflist_df13 13st initial reference picture list for direct forward picid used for h264
4:0	RW	0x00	h264_init_reflist_df12 12st initial reference picture list for direct forward picid used for h264

VDPU_SWREG103

Address: Operational Base + offset (0x019c)

initial reference picture list related

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	h264_init_reflist_db5 5st initial reference picture list for direct backward picid used for h264
24:20	RW	0x00	h264_init_reflist_db4 4st initial reference picture list for direct backward picid used for h264
19:15	RW	0x00	h264_init_reflist_db3 3st initial reference picture list for direct backward picid used for h264
14:10	RW	0x00	h264_init_reflist_db2 2st initial reference picture list for direct backward picid used for h264
9:5	RW	0x00	h264_init_reflist_db1 1st initial reference picture list for direct backward picid used for h264
4:0	RW	0x00	h264_init_reflist_db0 0st initial reference picture list for direct backward picid used for h264

VDPU_SWREG104

Address: Operational Base + offset (0x01a0)

initial reference picture list related

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

Bit	Attr	Reset Value	Description
29:25	RW	0x00	h264_init_reflist_db11 11st initial reference picture list for direct backward picid used for h264
24:20	RW	0x00	h264_init_reflist_db10 10st initial reference picture list for direct backward picid used for h264
19:15	RW	0x00	h264_init_reflist_db9 9st initial reference picture list for direct backward picid used for h264
14:10	RW	0x00	h264_init_reflist_db8 8st initial reference picture list for direct backward picid used for h264
9:5	RW	0x00	h264_init_reflist_db7 7st initial reference picture list for direct backward picid used for h264
4:0	RW	0x00	h264_init_reflist_db6 6st initial reference picture list for direct backward picid used for h264

VDPU_SWREG105
Address: Operational Base + offset (0x01a4)
initial reference picture list related

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:15	RW	0x00	h264_init_reflist_db15 15st initial reference picture list for direct backward picid used for h264
14:10	RW	0x00	h264_init_reflist_db14 14st initial reference picture list for direct backward picid used for h264
9:5	RW	0x00	h264_init_reflist_db13 13st initial reference picture list for direct backward picid used for h264
4:0	RW	0x00	h264_init_reflist_db12 12st initial reference picture list for direct backward picid used for h264

VDPU_SWREG106
Address: Operational Base + offset (0x01a8)
initial reference picture list related

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:15	RW	0x00	h264_init_reflist_pf3 3st initial reference picture list for P forward picid Initial reference picture list for P forward picid 3

Bit	Attr	Reset Value	Description
14:10	RW	0x00	h264_init_reflist_pf2 2st initial reference picture list for P forward picid Initial reference picture list for P forward picid 2
9:5	RW	0x00	h264_init_reflist_pf1 1st initial reference picture list for P forward picid Initial reference picture list for P forward picid 1
4:0	RW	0x00	h264_init_reflist_pf0 0st initial reference picture list for P forward picid used in 264

VDPU_SWREG107
Address: Operational Base + offset (0x01ac)
long term flag for reference pictuure index

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	h264_refpic_term_flag long term flag for reference pictuure index

VDPU_SWREG108
Address: Operational Base + offset (0x01b0)
valid flag for reference picture index

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	h264_refpic_valid_flag valid flag for reference picture index

VDPU_SWREG109
Address: Operational Base + offset (0x01b4)
the stream start word for decoder

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x00	h264_strm_start_bit the stream start word for decoder assosiates with sw_rlc_vlc_st_adr

VDPU_SWREG110
Address: Operational Base + offset (0x01b8)
h264 pic mb size

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:22	RW	0x00	h264_flt_offset_cr_qp filter offset of cr qp
21:17	RW	0x00	h264_flt_offset_cb_qp filter offset of cb qp

Bit	Attr	Reset Value	Description
16:9	RW	0x00	h264_pic_mb_h Picture height in macroblocks value =((pixel height+15)/16). used for frame or single field size being decoded
8:0	RW	0x000	h264_pic_mb_w Picture width in macroblocks value = ((pixel width + 15) /16)

VDPU_SWREG111
Address: Operational Base + offset (0x01bc)
h264 ctrl related

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17:16	RW	0x0	h264_wp_bslice_sel wp(weighted prediction) specification for B slice 0 : default wp be used 1 : explicit wp be used 2 : implicit wp be used
15:5	RO	0x0	reserved
4:0	RW	0x00	h264_max_refnum short and long term reference frames's maximum number this value is for decoded picture buffer

VDPU_SWREG112
Address: Operational Base + offset (0x01c0)
current frame related

Bit	Attr	Reset Value	Description
31	RW	0x0	h264_dblk_ctrl_flag the control present flag of deblocking filter to indicates if the slice header will have the deblocking filter's extra variables controlling characteristics
30	RW	0x0	h264_rpcp_flag redundant picture count present flag to specifies whether redundant picture count syntax elements
29:21	RO	0x0	reserved
20:16	RW	0x00	h264_curfrm_len the bit length of input data stream's frame num H.264: Bit length of frame_num in data stream
15:0	RW	0x0000	h264_curfrm_num the current frame number for h264 it may be use for reference picture reordering and identify short-term reference frames

VDPU_SWREG113
Address: Operational Base + offset (0x01c4)

reference picture related

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x000	h264_mk_len the length of marking bits use for decoded reference picture
15:0	RW	0x0000	h264_idrp_id instantaneous decoding refresh picture id

VDPU_SWREG114

Address: Operational Base + offset (0x01c8)

maximum reference

Bit	Attr	Reset Value	Description
31:24	RW	0x00	h264_pps_id the id for picture parameter set it identifies the slice header will have the id of picture parameter set
23:19	RW	0x00	h264_max_refidx1 the maximum reference index 1 it will be used in decoding inter predicted macro blocks
18:14	RW	0x00	h264_max_refidx0 the maximum reference index 0 it will be used in decoding inter predicted macro blocks
13:8	RO	0x0	reserved
7:0	RW	0x00	h264_pocf_len the length of picture order count field in stream

VDPU_SWREG115

Address: Operational Base + offset (0x01cc)

enable flag

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8	RW	0x0	h264_idr_pic_flag instantaneous decoding refresh picture flag
7	RW	0x0	h264_dlmv_method_en the method to use to derive luma motion vectors with B_skip, B_Direct_16x16 and B_direct_8x8_inference_flag
6	RW	0x0	h264_monochr_en monochromatic enable sampling format , 0 : 4:2:0 1 : 4:0:0
5	RW	0x0	h264_cabac_en enable for cabac
4	RW	0x0	h264_pslice_wp_en enable flag of Weighted prediction for P slices

Bit	Attr	Reset Value	Description
3	RW	0x0	h264_nimb_intra_en if intra prediction uses only neighbouring intra macroblocks 0 : neighbouring inter macroblocks are used in intra prediction process 1 : neighbouring intra macroblocks are used
2	RW	0x0	h264_tranf_flag_en_8x8 8x8 transform flag enable for stream decoding
1	RW	0x0	h264_scl_matrix_en scaling matrix enable 0 : normal transform 1 : use scaling matrix for transform
0	RW	0x0	h264_fieldpic_flag_exist Flag for streamd that field_pic_flag exists in stream Flag for streamd that field_pic_flag exists in stream

VDPU_SWREG120
Address: Operational Base + offset (0x01e0)
multi format reuse register0

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg0 multi format reuse register0 except h264 MPEG4/JPEG/MPEG2/VP6/RV/VP7/VP: [31:2] RLC mode: Base address for RLC data VLC mode: Stream start address VP7: [31:2] This base address is used as sw_dct_strm0_base including DCT stream for MB rows 0,2n

VDPU_SWREG121
Address: Operational Base + offset (0x01e4)
multi format reuse register1

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg1 multi format reuse register1 except h264 RV: [20:16] : frame size length JPEG: [26:0] : progressive JPEG MPEG2 : [12] : enable for bilinear motion compensation VP7: [31:26] : DCT stream partition index 1 of start bit [25:20] : DCT stream partition index 2 of start bit [13] : rominance motion vector resolution for VP7/8 [12] : enable for bilinear motion compensation [11:9] : 0st count for DC prediction mach [8:6] : 1st count for DC prediction mach

VDPU_SWREG122
Address: Operational Base + offset (0x01e8)
multi format reuse register2

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg2 multi format reuse register2 except h264 MPEG4: [31:26] : Exact bit of stream start word [25] : enable for sync markers [24] : enable for Type 1 quantization [23:19] : the offset of Qp filter [18:14] : the offset of Qp filter for cr [0] : filed_pic_flag exists in stream JPEG : [31:26] : Exact bit of stream start word [25] : enable for sync markers [12:11] : total of Quantization tables [10:8] : the sampling format for input pic [7] : JPEG width [6] : weather current strem buffer contain the end of a JPEG image [5:0] : vlc table vp6: [23:18] : start bit for ctrl stream (vp7) [17] : enable for huffman decoding [16] : enable for muti stream (vp7) [15:8] : boolean dec init value(vp7) [7:0] : boolean dec init range

VDPU_SWREG123
Address: Operational Base + offset (0x01ec)
multi format reuse register3

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg3 multi format reuse register3 except h264 JPEG: [15:0] : start marker frequency. vp6: [17:14] : loop filter limit value [13] : enable for variance test [12:10] : filter MV size threshold [9:0] : filter variance threshold VP7/VP : [31:16] : value 0 for inital dc predictor [15:0] : value 1 for inital dc predictor

VDPU_SWREG124
Address: Operational Base + offset (0x01f0)
multi format reuse register4

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg4 multi format reuse register4 except h264 MPEG4: [31:2] : MB ctrl start address VP6: [23:0] : total of CTRL stream data VP7/VP : [27:24] : coeffient partitions number [23:0] : total of CTRL stream data

VDPU_SWREG125
Address: Operational Base + offset (0x01f4)
multi format reuse register5

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg5 multi format reuse register5 except h264 JPEG: [31:2] : Cb ACDC coeff start address VP6/VP7/vp: [31:22] : prediction filter with set 5 and tap 1 [21:12] : prediction filter with set 5 and tap 2 [11:2] : prediction filter with set 5 and tap 3

VDPU_SWREG126
Address: Operational Base + offset (0x01f8)
multi format reuse register6

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg6 multi format reuse register6 except h264 JPEG: [31:2] : Cr ACDC coeff start address VP6/VP7/vp: [31:22] : prediction filter with set 6 and tap 0 [21:12] : prediction filter with set 6 and tap 1 [11:2] : prediction filter with set 6 and tap 2

VDPU_SWREG127
Address: Operational Base + offset (0x01fc)
multi format reuse register7

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg7 multi format reuse register7 except h264 VP6/VP7/vp: [31:22] : prediction filter with set 6 and tap 3 [21:12] : prediction filter with set 7 and tap 0 [11:2] : prediction filter with set 7 and tap 1

VDPU_SWREG128
Address: Operational Base + offset (0x0200)
multi format reuse register8

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg8 multi format reuse register8 except h264 VP6: [31:22] : prediction filter with set 7 and tap 2 [21:12] : prediction filter with set 7 and tap 3 VP7/VP: [31:22] : prediction filter with set 7 and tap 2 [21:12] : prediction filter with set 7 and tap 3 [11:10] : extra prediction filter with set 2 and tap -1 [9:8] : extra prediction filter with set 2 and tap 4 [7:6] : extra prediction filter with set 4 and tap -1 [5:4] : extra prediction filter with set 4 and tap 4 [3:2] : extra prediction filter with set 6 and tap -1 [1:0] : extra prediction filter with set 6 and tap 4

VDPU_SWREG129
Address: Operational Base + offset (0x0204)
multi format reuse register9

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg9 multi format reuse register9 except h264 VP6: [29:24] : 56st coef of scan read index [23:18] : 57st coef of scan read index [17:12] : 58st coef of scan read index [11:6] : 59st coef of scan read index [5:0] : 60st coef of scan read index

VDPU_SWREG130
Address: Operational Base + offset (0x0208)
multi format reuse register10

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg10 multi format reuse register10 except h264 VP6: [29:24] : 61st coef of scan read index [23:18] : 62st coef of scan read index [17:12] : 63st coef of scan read index VP7: [21:11] : QP0 for VP7 and quantisizer value [10:0] : QP1 for VP7 and quantisizer value

VDPU_SWREG131
Address: Operational Base + offset (0x020c)
multi format reuse register11

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg11 multi format reuse register11 except h264 MPEG4/H263/vp6 /VP7: [31:2] : reference pic0 start address JPEG: [31:2] : the ch decoder output start address

VDPU_SWREG132
Address: Operational Base + offset (0x0210)
multi format reuse register12

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg12 multi format reuse register12 except h264 VP7: [31] : type of loop filter [30:28] : sharpness of loop filter [27:21] : MB type0 adjustment of filter level [20:14] : MB type1 adjustment of filter level [13:7] : MB type2 adjustment of filter level [6:0] : MB type3 adjustment of filter level

VDPU_SWREG133
Address: Operational Base + offset (0x0214)
multi format reuse register13

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg13 multi format reuse register13 except h264 VP6: [29:24] : 51st coef of scan read index [23:18] : 52st coef of scan read index [17:12] : 53st coef of scan read index [11:6] : 54st coef of scan read index [5:0] : 55st coef of scan read index VP7: [27:21] : reference frame type0 adjustment of filter level [20:14] : reference frame type1 adjustment of filter level [13:7] : reference frame type2 adjustment of filter level [6:0] : reference frame type3 adjustment of filter level

VDPU_SWREG134
Address: Operational Base + offset (0x0218)
multi format reuse register14

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg14 multi format reuse register14 except h264 MPEG4/MEPG2: [31:2] : reference pic2 start address JPEG: [30:24] : code words of length 6 [21:16] : code words of length 5 [15:11] : code words of length 4 [10:7] : code words of length 3 [5:3] : code words of length 2 [1:0] : code words of length 1

VDPU_SWREG135

Address: Operational Base + offset (0x021c)
multi format reuse register15

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg15 multi format reuse register15 except h264 MPEG4/MEPG2: [31:2] : reference pic3 start address JPEG: [30:24] : code words of length 10 [23:16] : code words of length 9 [15:8] : code words of length 8 [7:0] : code words of length 7

VDPU_SWREG136
Address: Operational Base + offset (0x0220)
multi format reuse register16

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg16 multi format reuse register16 except h264 VP6/VP7 [31:2] : golden reference pic start address(PIC_ID 4) [0] : golden reference pic siggn bias(VP7) MPEG4/MPEG2: [19] : alternalte scan flag [18:15] : HRZ AXI's bit amount for representing FWD MV [14:11] : VRZ AXI's bit amount for representing FWD MV [10:7] : HRZ AXI's bit amount for representing BWD MV [6:3] : VRZ AXI's bit amount for representing BWD MV [2] : FWD MV Y resolution [1] : the ctrl bit for rounding(MPEG4),BWD MV Y resolution(MPEG2) [0] : pic type of previous anchor(MPEG4) JPEG: [30:24] : code words of length 14 [23:16] : code words of length 13 [15:8] : code words of length 12 [7:0] : code words of length 11

VDPU_SWREG137
Address: Operational Base + offset (0x0224)
multi format reuse register17

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg17 multi format reuse register17 except h264 MPEG4: [26:0] : reference distance syntax for delta value0 be used JPEG: [31:27] : tab2:code words of length 4 [26:23] : tab2:code words of length 3 [21:19] : tab2:code words of length 2 [17:16] : tab2:code words of length 1 [15:8] : tab1:code words of length 16 [7:0] : tab1:code words of length 15

VDPU_SWREG138
Address: Operational Base + offset (0x0228)
multi format reuse register18

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg18 multi format reuse register18 except h264 MPEG4: [26:0] : reference distance syntax for delta value -1 be used JPEG: [31:24] : tab2:code words of length 8 [23:16] : tab2:code words of length 7 [14:8] : tab2:code words of length 6 [5:0] : tab2:code words of length 5 VP6/VP7: [29:24] : 6st coef of scan read index [23:18] : 7st coef of scan read index [17:12] : 8st coef of scan read index [11:6] : 9st coef of scan read index [5:0] : 10st coef of scan read index

VDPU_SWREG139
Address: Operational Base + offset (0x022c)
multi format reuse register19

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg19 multi format reuse register19 except h264 MPEG4: [26:0] : reference distance syntax for delta value1 be used JPEG: [31:24] : tab2:code words of length 12 [23:16] : tab2:code words of length 11 [15:8] : tab2:code words of length 10 [7:0] : tab2:code words of length 9 VP6/VP7: [29:24] : 11st coef of scan read index [23:18] : 12st coef of scan read index [17:12] : 13st coef of scan read index [11:6] : 14st coef of scan read index [5:0] : 15st coef of scan read index

VDPU_SWREG140
Address: Operational Base + offset (0x0230)
multi format reuse register20

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg20 multi format reuse register20 except h264 JPEG: [31:24] : tab2:code words of length 16 [23:16] : tab2:code words of length 15 [15:8] : tab2:code words of length 14 [7:0] : tab2:code words of length 13 VP6: [29:24] : 16st coef of scan read index [23:18] : 17st coef of scan read index [17:12] : 18st coef of scan read index [11:6] : 19st coef of scan read index [5:0] : 20st coef of scan read index VP7: [31:2] : DCT stream MB row 2,2n+1 start address

VDPU_SWREG141
Address: Operational Base + offset (0x0234)
multi format reuse register21

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg21 multi format reuse register21 except h264 JPEG: [31:28] : tab1:code words of length 8 [27:24] : tab1:code words of length 7 [23:20] : tab1:code words of length 6 [19:16] : tab1:code words of length 5 [15:12] : tab1:code words of length 4 [11:8] : tab1:code words of length 3 [6:4] : tab1:code words of length 2 [1:0] : tab1:code words of length 1 VP6: [29:24] : 21st coef of scan read index [23:18] : 22st coef of scan read index [17:12] : 23st coef of scan read index [11:6] : 24st coef of scan read index [5:0] : 25st coef of scan read index VP7 [31:2] : DCT stream MB row 2,2n+2 start address

VDPU_SWREG142

Address: Operational Base + offset (0x0238)

multi format reuse register22

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg22 multi format reuse register22 except h264 JPEG: [31:28] : tab1:code words of length 16 [27:24] : tab1:code words of length 15 [23:20] : tab1:code words of length 14 [19:16] : tab1:code words of length 13 [15:12] : tab1:code words of length 12 [11:8] : tab1:code words of length 11 [6:4] : tab1:code words of length 10 [1:0] : tab1:code words of length 9 VP6: [29:24] : 26st coef of scan read index [23:18] : 27st coef of scan read index [17:12] : 28st coef of scan read index [11:6] : 29st coef of scan read index [5:0] : 30st coef of scan read index VP7 [31:2] : DCT stream MB row 2,2n+3 start address

VDPU_SWREG143

Address: Operational Base + offset (0x023c)
multi format reuse register23

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg23 multi format reuse register23 except h264 JPEG: [31:28] : tab2:code words of length 8 [27:24] : tab2:code words of length 7 [23:20] : tab2:code words of length 6 [19:16] : tab2:code words of length 5 [15:12] : tab2:code words of length 4 [11:8] : tab2:code words of length 3 [6:4] : tab2:code words of length 2 [1:0] : tab2:code words of length 1 VP6: [29:24] : 31st coef of scan read index [23:18] : 32st coef of scan read index [17:12] : 33st coef of scan read index [11:6] : 34st coef of scan read index [5:0] : 35st coef of scan read index VP7 [31:2] : DCT stream MB row 2,2n+4 start address

VDPU_SWREG144
Address: Operational Base + offset (0x0240)
multi format reuse register24

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg24 multi format reuse register24 except h264 JPEG: [31:28] : tab2:code words of length 16 [27:24] : tab2:code words of length 15 [23:20] : tab2:code words of length 14 [19:16] : tab2:code words of length 13 [15:12] : tab2:code words of length 12 [11:8] : tab2:code words of length 11 [6:4] : tab2:code words of length 10 [1:0] : tab2:code words of length 9 VP6: [29:24] : 36st coef of scan read index [23:18] : 37st coef of scan read index [17:12] : 38st coef of scan read index [11:6] : 39st coef of scan read index [5:0] : 40st coef of scan read index VP7 [31:2] : DCT stream MB row 2,2n+5 start address

VDPU_SWREG145
Address: Operational Base + offset (0x0244)
multi format reuse register25

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg25 multi format reuse register25 except h264 JPEG: [31:28] : tab3:code words of length 8 [27:24] : tab3:code words of length 7 [23:20] : tab3:code words of length 6 [19:16] : tab3:code words of length 5 [15:12] : tab3:code words of length 4 [11:8] : tab3:code words of length 3 [6:4] : tab2:code words of length 2 [1:0] : tab3:code words of length 1 VP6/VP7: [31:2] : ctrl data stream start address

VDPU_SWREG146
Address: Operational Base + offset (0x0248)
multi format reuse register26

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg26 multi format reuse register26 except h264 JPEG: [31:28] : tab3:code words of length 16 [27:24] : tab3:code words of length 15 [23:20] : tab3:code words of length 14 [19:16] : tab3:code words of length 13 [15:12] : tab3:code words of length 12 [11:8] : tab3:code words of length 11 [6:4] : tab3:code words of length 10 [1:0] : tab3:code words of length 9 VP6: [29:24] : 41st coef of scan read index [23:18] : 42st coef of scan read index [17:12] : 43st coef of scan read index [11:6] : 44st coef of scan read index [5:0] : 45st coef of scan read index VP7 [31:2] : DCT stream MB row 2,2n+6 start address

VDPU_SWREG147
Address: Operational Base + offset (0x024c)
multi format reuse register27

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg27 multi format reuse register27 except h264 VP6: [29:24] : 46st coef of scan read index [23:18] : 47st coef of scan read index [17:12] : 48st coef of scan read index [11:6] : 49st coef of scan read index [5:0] : 50st coef of scan read index VP7 [31:2] : DCT stream MB row 2,2n+7 start address

VDPU_SWREG148
Address: Operational Base + offset (0x0250)
multi format reuse register28

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg28 multi format reuse register28 except h264 MPEG4/MPEG2/VP7: [31:2] : ref pic index 1 start address JPEG: [7:0] : snapshot

VDPU_SWREG149
Address: Operational Base + offset (0x0254)
multi format reuse register29

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg29 multi format reuse register29 except h264 VP7: [31:2] : the segmentation map value start address [1] : enable for segmentation map update [0] : enable for segmentation

VDPU_SWREG150
Address: Operational Base + offset (0x0258)
multi format reuse register30

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg30 multi format reuse register30 except h264 VP7: [29:24] : DCT stream partition index 3 of start bit [23:18] : DCT stream partition index 4 of start bit [17:12] : DCT stream partition index 5 of start bit [11:6] : DCT stream partition index 6 of start bit [5:0] : DCT stream partition index 7 of start bit

VDPU_SWREG151
Address: Operational Base + offset (0x025c)
multi format reuse register31

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg31 multi format reuse register31 except h264 VP7: [21:11] : QP2 for VP7 and quantisizer value [10:0] : QP3 for VP7 and quantisizer value

VDPU_SWREG152
Address: Operational Base + offset (0x0260)
multi format reuse register32

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg32 multi format reuse register32 except h264 VP7: [21:11] : QP4 for VP7 and quantisizer value [10:0] : QP5 for VP7 and quantisizer value

VDPU_SWREG153
Address: Operational Base + offset (0x0264)
multi format reuse register33

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg33 multi format reuse register33 except h264 VP6/VP7: [31:22] : prediction filter with set 0,tap3 (also for mpeg4) [21:12] : prediction filter with set 1,tap0 [11:2] : prediction filter with set 1,tap1

VDPU_SWREG154
Address: Operational Base + offset (0x0268)
multi format reuse register34

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg34 multi format reuse register34 except h264 VP6/VP7: [31:22] : prediction filter with set 1,tap2 [21:12] : prediction filter with set 1,tap3 [11:2] : prediction filter with set 2,tap0

VDPU_SWREG155
Address: Operational Base + offset (0x026c)
multi format reuse register35

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg35 multi format reuse register35 except h264 VP6/VP7: [31:22] : prediction filter with set 2,tap1 [21:12] : prediction filter with set 2,tap2 [11:2] : prediction filter with set 2,tap3

VDPU_SWREG156
Address: Operational Base + offset (0x0270)
multi format reuse register36

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg36 multi format reuse register36 except h264 VP6/VP7: [31:22] : prediction filter with set 3,tap0 [21:12] : prediction filter with set 3,tap1 [11:2] : prediction filter with set 3,tap2

VDPU_SWREG157
Address: Operational Base + offset (0x0274)
multi format reuse register37

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg37 multi format reuse register37 except h264 VP6/VP7: [31:22] : prediction filter with set 3,tap3 [21:12] : prediction filter with set 4,tap0 [11:2] : prediction filter with set 4,tap1

VDPU_SWREG158
Address: Operational Base + offset (0x0278)
multi format reuse register38

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg38 multi format reuse register38 except h264 VP6/VP7: [31:22] : prediction filter with set 4,tap2 [21:12] : prediction filter with set 4,tap3 [11:2] : prediction filter with set 5,tap0

VDPU_SWREG164_PERF_LATENCY_CTRL0
Address: Operational Base + offset (0x0290)
Axi performance latency module contrl register0

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved

Bit	Attr	Reset Value	Description
19:8	RW	0x000	sw_rd_latency_thr sw_rd_latency_thr
7:4	RW	0x0	sw_rd_latency_id sw_rd_latency_id
3	RW	0x0	sw_axi_cnt_type sw_axi_cnt_type sw_axi_cnt_type
2	RW	0x0	sw_axi_perf_frm_type sw_axi_perf_frm_type 1'b0: clear by frame end 1'b1: clear by software configuration
1	W1C	0x0	sw_axi_perf_clr_e sw_axi_perf_clr_e 1'b0: software clear disable 1'b1: software clear enalbe
0	RW	0x0	sw_axi_perf_work_e sw_axi_perf_work_e 1'b0: disable 1'b1: enable

VDPU_SWREG165_PERF_LATENCY_CTRL1
Address: Operational Base + offset (0x0294)
PERF_LATENCY_CTRL1

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:8	RW	0x0	sw_aw_count_id sw_aw_count_id sw_aw_count_id
7:4	RW	0x0	sw_ar_count_id sw_ar_count_id sw_ar_count_id
3	RW	0x0	sw_aw_cnt_id_type sw_aw_cnt_id_type sw_aw_cnt_id_type
2	RW	0x0	sw_ar_cnt_id_type sw_ar_cnt_id_type sw_ar_cnt_id_type
1:0	RW	0x0	sw_addr_align_type sw_addr_align_type sw_addr_align_type

VDPU_SWREG166_PERF_RD_MAX_LATENCY_NUM0
Address: Operational Base + offset (0x0298)
Read max latency number

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RO	0x0000	rd_max_latency_num_ch0 read max latency value of channel 0

VDPU_SWREG167_PERF_RD_LATENCY_SAMP_NUM
Address: Operational Base + offset (0x029c)
The number of bigger than configed threshold value

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rd_latency_thr_num_ch0 read latency thr number channel 0

VDPU_SWREG168_PERF_RD_LATENCY_ACC_SUM
Address: Operational Base + offset (0x02a0)
Total sample number

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rd_latency_acc_sum

VDPU_SWREG169_PERF_RD_AXI_TOTAL_BYTE
Address: Operational Base + offset (0x02a4)
perf_rd_axi_total_byte

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_rd_axi_total_byte perf_rd_axi_total_byte perf_rd_axi_total_byte

VDPU_SWREG170_PERF_WR_AXI_TOTAL_BYTE
Address: Operational Base + offset (0x02a8)
perf_wr_axi_total_byte

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_wr_axi_total_byte perf_wr_axi_total_byte perf_wr_axi_total_byte

VDPU_SWREG171_PERF_WORKING_CNT
Address: Operational Base + offset (0x02ac)
perf_working_cnt

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_working_cnt perf_working_cnt perf_working_cnt

5.5.4 VEPU Registers Summary

Name	Offset	Size	Reset Value	Description
VEPU_swreg_0	0x0000	W	0x00000000	1st quantization for jpeg lumin table
VEPU_swreg_1	0x0004	W	0x00000000	2st quantization for jpeg lumin table
VEPU_swreg_2	0x0008	W	0x00000000	3st quantization for jpeg lumin table
VEPU_swreg_3	0x000c	W	0x00000000	4st quantization for jpeg lumin table
VEPU_swreg_4	0x0010	W	0x00000000	5st quantization for jpeg lumin table
VEPU_swreg_5	0x0014	W	0x00000000	6st quantization for jpeg lumin table/part 1 for qp round
VEPU_swreg_6	0x0018	W	0x00000000	7st quantization for jpeg lumin table
VEPU_swreg_7	0x001c	W	0x00000000	8st quantization for jpeg lumin table
VEPU_swreg_8	0x0020	W	0x00000000	9st quantization for jpeg lumin table
VEPU_swreg_9	0x0024	W	0x00000000	10st quantization for jpeg lumin table
VEPU_swreg_10	0x0028	W	0x00000000	11st quantization for jpeg lumin table
VEPU_swreg_11	0x002c	W	0x00000000	12st quantization for jpeg lumin table
VEPU_swreg_12	0x0030	W	0x00000000	13st quantization for jpeg lumin table
VEPU_swreg_13	0x0034	W	0x00000000	14st quantization for jpeg lumin table
VEPU_swreg_14	0x0038	W	0x00000000	15st quantization for jpeg lumin table
VEPU_swreg_15	0x003c	W	0x00000000	16st quantization for jpeg lumin table
VEPU_swreg_16	0x0040	W	0x00000000	1st quantization for jpeg chroma table
VEPU_swreg_17	0x0044	W	0x00000000	2st quantization for jpeg chroma table
VEPU_swreg_18	0x0048	W	0x00000000	3st quantization for jpeg chroma table
VEPU_swreg_19	0x004c	W	0x00000000	4st quantization for jpeg chroma table
VEPU_swreg_20	0x0050	W	0x00000000	5st quantization for jpeg chroma table

Name	Offset	Size	Reset Value	Description
VEPU_swreg_21	0x0054	W	0x00000000	6st quantization for jpeg chroma table
VEPU_swreg_22	0x0058	W	0x00000000	7st quantization for jpeg chroma table
VEPU_swreg_23	0x005c	W	0x00000000	8st quantization for jpeg chroma table/part 3 for qp round
VEPU_swreg_24	0x0060	W	0x00000000	9st quantization for jpeg chroma table
VEPU_swreg_25	0x0064	W	0x00000000	10st quantization for jpeg chroma table
VEPU_swreg_26	0x0068	W	0x00000000	11st quantization for jpeg chroma table
VEPU_swreg_27	0x006c	W	0x00000000	12st quantization for jpeg chroma
VEPU_swreg_28	0x0070	W	0x00000000	13st quantization for jpeg chroma
VEPU_swreg_29	0x0074	W	0x00000000	14st quantization for jpeg chroma
VEPU_swreg_30	0x0078	W	0x00000000	15st quantization for jpeg chroma
VEPU_swreg_31	0x007c	W	0x00000000	16st quantization for jpeg chroma
VEPU_swreg_44	0x00b0	W	0x00000000	Intra slice bitmap
VEPU_swreg_45	0x00b4	W	0x00000000	Intra slice bitmap
VEPU_swreg_46	0x00b8	W	0x00000000	intra macro block sellect register
VEPU_swreg_47	0x00bc	W	0x00000000	CIR intra control register
VEPU_swreg_48	0x00c0	W	0x00000000	input luma start address
VEPU_swreg_49	0x00c4	W	0x00000000	input cb start address
VEPU_swreg_50	0x00c8	W	0x00000000	input cr start address
VEPU_swreg_51	0x00cc	W	0x00000000	stream header bits left register
VEPU_swreg_52	0x00d0	W	0x00000000	stream header bits left register
VEPU_swreg_53	0x00d4	W	0x00000000	stream buffer register
VEPU_swreg_54	0x00d8	W	0x01010000	axi control register
VEPU_swreg_55	0x00dc	W	0x00000000	qp related
VEPU_swreg_56	0x00e0	W	0x00000000	the luma reference frame start address
VEPU_swreg_57	0x00e4	W	0x00000000	the chroma reference frame start address
VEPU_swreg_58	0x00e8	W	0x00000000	the result of qp sum div2
VEPU_swreg_59	0x00ec	W	0x00000000	Register0000 Abstract
VEPU_swreg_60	0x00f0	W	0x00000000	Register0001 Abstract
VEPU_swreg_61	0x00f4	W	0x00000000	input luminance information
VEPU_swreg_62	0x00f8	W	0x00000000	rlc_sum

Name	Offset	Size	Reset Value	Description
VEPU_swreg_63	0x00fc	W	0x00000000	the reconstructed luma start address
VEPU_swreg_64	0x0100	W	0x00000000	the reconstructed chroma start address
VEPU_swreg_65_reuse	0x0104	W	0x00000000	checkpoint 1 and 2
VEPU_swreg_66_reuse	0x0108	W	0x00000000	checkpoint 3 and 4
VEPU_swreg_67_reuse	0x010c	W	0x00000000	checkpoint 5 and 6
VEPU_swreg_68_reuse	0x0110	W	0x00000000	checkpoint 7 and 8
VEPU_swreg_69_reuse	0x0114	W	0x00000000	checkpoint 9 and 10
VEPU_swreg_70_reuse	0x0118	W	0x00000000	checkpoint word error 1 and 2
VEPU_swreg_71_reuse	0x011c	W	0x00000000	checkpoint word error 1 and 2
VEPU_swreg_72_reuse	0x0120	W	0x00000000	checkpoint word error 1 and 2
VEPU_swreg_73_reuse	0x0124	W	0x00000000	checkpoint delta QP register
VEPU_swreg_74	0x0128	W	0x00000000	input image format
VEPU_swreg_75	0x012c	W	0x00000000	intra/inter mode
VEPU_swreg_76_reuse	0x0130	W	0x00000000	encoder control regsiter 0
VEPU_swreg_77	0x0134	W	0x00000000	output stream start address
VEPU_swreg_78	0x0138	W	0x00000000	output control start address
VEPU_swreg_79	0x013c	W	0x00000000	next picture luminance start address
VEPU_swreg_80	0x0140	W	0x00000000	Base address for MV output
VEPU_swreg_81	0x0144	W	0x00000000	the cabac table start address
VEPU_swreg_82	0x0148	W	0x00000000	the first of ROI area register
VEPU_swreg_83	0x014c	W	0x00000000	the second of ROI area register
VEPU_swreg_84	0x0150	W	0x00000000	Stabilization matrix
VEPU_swreg_85	0x0154	W	0x00000000	Stabilization matrix
VEPU_swreg_86	0x0158	W	0x00000000	Stabilization matrix
VEPU_swreg_87	0x015c	W	0x00000000	Stabilization matrix
VEPU_swreg_88	0x0160	W	0x00000000	Stabilization matrix
VEPU_swreg_89	0x0164	W	0x00000000	Stabilization matrix
VEPU_swreg_90	0x0168	W	0x00000000	Stabilization matrix
VEPU_swreg_91	0x016c	W	0x00000000	Stabilization matrix
VEPU_swreg_92	0x0170	W	0x00000000	Stabilization matrix
VEPU_swreg_93	0x0174	W	0x00000000	the output of Stabilization motion sum
VEPU_swreg_94	0x0178	W	0x00000000	output of Stabilization
VEPU_swreg_95	0x017c	W	0x00000000	RGB to YUV conversion coefficient register
VEPU_swreg_96	0x0180	W	0x00000000	RGB to YUV conversion coefficient register
VEPU_swreg_97	0x0184	W	0x00000000	RGB to YUV conversion coefficient register
VEPU_swreg_98	0x0188	W	0x00000000	RGA MASK
VEPU_swreg_99	0x018c	W	0x00000000	mv related

Name	Offset	Size	Reset Value	Description
VEPU_swreg_100_reuse	0x0190	W	0x00000000	QP register
VEPU_swreg_101_read	0x0194	W	0x1f522780	hw config reg
VEPU_swreg_102	0x0198	W	0x00000000	mvc related
VEPU_swreg_103	0x019c	W	0x00000000	encoder start
VEPU_swreg_104	0x01a0	W	0x00000000	mb control register
VEPU_swreg_105	0x01a4	W	0x00000000	SWAP
VEPU_swreg_106_reuse	0x01a8	W	0x00000000	encoder control register 1
VEPU_swreg_107_reuse	0x01ac	W	0x00000000	JPEG control regsiter
VEPU_swreg_108_reuse	0x01b0	W	0x00000000	intra_slice_bmp2
VEPU_swreg_109	0x01b4	W	0x00001000	encoder status
VEPU_swreg_110_read	0x01b8	W	0x48311220	product ID
VEPU_swreg_120_183	0x01e0	W	0x00000000	DMV_4p_1p_penalty

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

5.5.5 VEPU Detail Register Description

VEPU_swreg_0
Address: Operational Base + offset (0x0000)
1st quantization for jpeg lumin table

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_jpeg_luma_quant1 jpeg luma quantiztion 1 jpeg luma quantization 1

VEPU_swreg_1
Address: Operational Base + offset (0x0004)
2st quantization for jpeg lumin table

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_jpeg_luma_quant2 jpeg luma quantization 2 jpeg luma quantization 2

VEPU_swreg_2
Address: Operational Base + offset (0x0008)
3st quantization for jpeg lumin table

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_jpeg_luma_quant3 jpeg luma quantization 3 jpeg luma quantization 3

VEPU_swreg_3
Address: Operational Base + offset (0x000c)
4st quantization for jpeg lumin table

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_jpeg_luma_quant4 jpeg luma quantization 4 jpeg luma quantization 4

VEPU_swreg_4
Address: Operational Base + offset (0x0010)
5st quantization for jpeg lumin table

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_jpeg_luma_quant5 jpeg luma quantization 5 jpeg luma quantization 5

VEPU_swreg_5
Address: Operational Base + offset (0x0014)
6st quantization for jpeg lumin table/part 1 for qp round

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_jpeg_luma_quant6 jpeg luma quantization 6 jpeg luma quantization 6

VEPU_swreg_6
Address: Operational Base + offset (0x0018)
7st quantization for jpeg lumin table

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_jpeg_luma_quant7 jpeg luma quantization 7 jpeg luma quantization 7

VEPU_swreg_7
Address: Operational Base + offset (0x001c)
8st quantization for jpeg lumin table

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_jpeg_luma_quant8 jpeg luma quantization 8 jpeg luma quantization 8

VEPU_swreg_8
Address: Operational Base + offset (0x0020)
9st quantization for jpeg lumin table

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_jpeg_luma_quant9 jpeg luma quantization 9 jpeg luma quantization 9

VEPU_swreg_9
Address: Operational Base + offset (0x0024)
10st quantization for jpeg lumin table

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_jpeg_luma_quant10 jpeg luma quantization 10 jpeg luma quantization 10

VEPU_swreg_10
Address: Operational Base + offset (0x0028)
11st quantization for jpeg lumin table

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_jpeg_luma_quant11 jpeg luma quantization 11 jpeg luma quantization 11

VEPU_swreg_11
Address: Operational Base + offset (0x002c)
12st quantization for jpeg lumin table

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_jpeg_luma_quant12 jpeg luma quantization 12 jpeg luma quantization 12

VEPU_swreg_12
Address: Operational Base + offset (0x0030)
13st quantization for jpeg lumin table

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_jpeg_luma_quant13 jpeg luma quantization 13 jpeg luma quantization 13

VEPU_swreg_13
Address: Operational Base + offset (0x0034)
14st quantization for jpeg lumin table

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_jpeg_luma_quant14 jpeg luma quantization 14 jpeg luma quantization 14

VEPU_swreg_14
Address: Operational Base + offset (0x0038)
15st quantization for jpeg lumin table

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_jpeg_luma_quant15 jpeg luma quantization 15 jpeg luma quantization 15

VEPU_swreg_15
Address: Operational Base + offset (0x003c)
16st quantization for jpeg lumin table

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	sw_jpeg_luma_quant16 jpeg luma quantization 16 jpeg luma quantization 16

VEPU_swreg_16
Address: Operational Base + offset (0x0040)
1st quantization for jpeg chroma table

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_jpeg_chroma_quant1 jpeg chroma quantization 1 jpeg chroma quantization 1

VEPU_swreg_17
Address: Operational Base + offset (0x0044)
2st quantization for jpeg chroma table

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_jpeg_chroma_quant2 jpeg chroma quantization 2 jpeg chroma quantization 2

VEPU_swreg_18
Address: Operational Base + offset (0x0048)
3st quantization for jpeg chroma table

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_jpeg_chroma_quant3 jpeg chroma quantization 3 jpeg chroma quantization 3

VEPU_swreg_19
Address: Operational Base + offset (0x004c)
4st quantization for jpeg chroma table

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_jpeg_chroma_quant4 jpeg chroma quantization 4 jpeg chroma quantization 4

VEPU_swreg_20
Address: Operational Base + offset (0x0050)
5st quantization for jpeg chroma table

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_jpeg_chroma_quant5 jpeg chroma quantization 5 jpeg chroma quantization 5

VEPU_swreg_21
Address: Operational Base + offset (0x0054)
6st quantization for jpeg chroma table

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_jpeg_chroma_quant6 jpeg chroma quantization 6 jpeg chroma quantization 6

VEPU_swreg_22
Address: Operational Base + offset (0x0058)
7st quantization for jpeg chroma table

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_jpeg_chroma_quant7 jpeg chroma quantization 7 jpeg chroma quantization 7

VEPU_swreg_23
Address: Operational Base + offset (0x005c)
8st quantization for jpeg chroma table/part 3 for qp round

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_jpeg_chroma_quant8 jpeg chroma quantization 8 jpeg chroma quantization 8

VEPU_swreg_24
Address: Operational Base + offset (0x0060)
9st quantization for jpeg chroma table

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_jpeg_chroma_quant9 jpeg chroma quantization 9 jpeg chroma quantization 9

VEPU_swreg_25
Address: Operational Base + offset (0x0064)
10st quantization for jpeg chroma table

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_jpeg_chroma_quant10 jpeg chroma quantization 10 jpeg chroma quantization 10

VEPU_swreg_26
Address: Operational Base + offset (0x0068)
11st quantization for jpeg chroma table

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:0	RW	0x000	sw_jpeg_chroma_quant11 jpeg chroma quantization 11 jpeg chroma quantization 11

VEPU_swreg_27
Address: Operational Base + offset (0x006c)
12st quantization for jpeg chroma

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_jpeg_chroma_quant11 jpeg chroma quantization 11 jpeg chroma quantization 11

VEPU_swreg_28
Address: Operational Base + offset (0x0070)
13st quantization for jpeg chroma

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	sw_jpeg_chroma_quant13 jpeg chroma quantization 13 jpeg chroma quantization 13

VEPU_swreg_29
Address: Operational Base + offset (0x0074)
14st quantization for jpeg chroma

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_jpeg_chroma_quant14 jpeg chroma quantization 14 jpeg chroma quantization 14

VEPU_swreg_30
Address: Operational Base + offset (0x0078)
15st quantization for jpeg chroma

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:0	RW	0x000	sw_jpeg_chroma_quant15 jpeg chroma quantization 15 jpeg chroma quantization 15

VEPU_swreg_31
Address: Operational Base + offset (0x007c)
16st quantization for jpeg chroma

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_jpeg_chroma_quant16 jpeg chroma quantization 16 jpeg chroma quantization 16

VEPU_swreg_44
Address: Operational Base + offset (0x00b0)
Intra slice bitmap

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	intra_slice_bmp0 Intra slice bitmap for slices0 to slices31 bit0 : slices0 bit1 : slices1 bit2 : slices2 ..... bit31 : slices31

VEPU_swreg_45
Address: Operational Base + offset (0x00b4)
Intra slice bitmap

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	intra_slice_bmp1 Intra slice bitmap for slices32 to slices63 bit0 : slices32 bit1 : slices33 bit2 : slices34 ..... bit31 : slices63

VEPU_swreg_46
Address: Operational Base + offset (0x00b8)
intra macro block sellect register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	intra_up_mb_area The up intra macro block's area used in row The top intra macro block's area used in row

Bit	Attr	Reset Value	Description
23:16	RW	0x00	intra_down_mb_area The down intra macro block's area used in row The bottom intra macro block's area used in row
15:8	RW	0x00	intra_left_mb_area The left intra macro block's area used in column The left intra macro block's area used in column
7:0	RW	0x00	intra_right_mb_area The right intra macro block's area used in column The right intra macro block's area used in column

VEPU_swreg_47
Address: Operational Base + offset (0x00bc)
CIR intra control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	cir_first_intra the first macro block sellected for cir 0:disable other:enable and be set
15:0	RW	0x0000	cir_intra_mb_itvl the interval for cir intra macro block 0: disable other: enable and be set

VEPU_swreg_48
Address: Operational Base + offset (0x00c0)
input luma start address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	luma_in_st_adr input luma start address input luma start address

VEPU_swreg_49
Address: Operational Base + offset (0x00c4)
input cb start address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cb_in_st_adr input cb start address input cb start address

VEPU_swreg_50
Address: Operational Base + offset (0x00c8)
input cr start address

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cr_in_st_adr input cr start address input cr start address

VEPU_swreg_51
Address: Operational Base + offset (0x00cc)
stream header bits left register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	strm_header_left_hbits the high 32 bit of stram header be left the high 32 bit of stram header be left

VEPU_swreg_52
Address: Operational Base + offset (0x00d0)
stream header bits left register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	strm_header_left_lbits the low 32 bit of stram header be left the low 32 bit of stram header be left

VEPU_swreg_53
Address: Operational Base + offset (0x00d4)
stream buffer register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	strm_bufsize_lmt the limit size of steam buffer the limit size of steam buffer

VEPU_swreg_54
Address: Operational Base + offset (0x00d8)
axi control register

Bit	Attr	Reset Value	Description
31:24	RW	0x01	axi_rd_id axi read id if config 0,it will be modify as 1 by HW auto
23:16	RW	0x01	axi_wr_id axi write id if config 0,it will be modify as 1 by HW auto
15:14	RO	0x0	reserved
13:8	RW	0x00	burst_len burst length burst length
7:3	RO	0x0	reserved

Bit	Attr	Reset Value	Description
2	RW	0x0	burst_incr_mod_sel burst increment mode select 0: single burst selected 1: incr burst selected
1	RW	0x0	burst_discard on-off burst data dicard 0:disable ,off 1:enable,on
0	RW	0x0	burst_disable disable burst mode for AXI 0: enable 1:disable

VEPU_swreg_55
Address: Operational Base + offset (0x00dc)
qp related

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:12	RW	0x0	roi_dlt_qp1 1st for delta qp for roi 1st for delta qp for roi
11:8	RW	0x0	roi_dlt_qp2 2st for delta qp for roi 2st for delta qp for roi
7:4	RO	0x0	reserved
3:0	RW	0x0	qp_adjst QP adjustment for mad signed register; range from -8 to 7

VEPU_swreg_56
Address: Operational Base + offset (0x00e0)
the luma reference frame start address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	luma_ref_st_adr the luma reference frame start address the luma reference frame start address

VEPU_swreg_57
Address: Operational Base + offset (0x00e4)
the chroma reference frame start address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chroma_ref_st_adr the chroma reference frame start address the chroma reference frame start address

VEPU_swreg_58
Address: Operational Base + offset (0x00e8)
the result of qp sum div2

Bit	Attr	Reset Value	Description
31:11	RW	0x000000	qp_sum_div2 the result of (qp sum)/2 the result of (qp sum)/2
10:0	RO	0x0	reserved

VEPU_swreg_59
Address: Operational Base + offset (0x00ec)
Register0000 Abstract

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	h264_qurt_pixmv_dis disable the function of quarter pixel MVs used in h264 1:disable 0:default,enable
27:26	RO	0x0	reserved
25:24	RW	0x0	dblking_flt_mode deblocking filter mode select 0 : enabled 1 : disabled 2 : disabled on slice
23	RO	0x0	reserved
22:21	RW	0x0	h264_cabac_idc the initial idc for cabac used in h264 0,1,2: used 3:no use
20	RW	0x0	entry_code_fmt the format of stream entropy coding h.264: 0: cavlc 1: cabac
19:18	RO	0x0	reserved
17	RW	0x0	h264_trfmod_8x8 on-off for 8x8 transform used in h264 on-off for 8x8 transform used in h264
16	RW	0x0	h264_res_intermod_4x4 the restriction inter mode selected in 4x4 block the restriction inter mode selected in 4x4 block
15	RW	0x0	h264_strm_mod_sel used to select stream mode 0 : NAL unit ; 1 : BYTE

Bit	Attr	Reset Value	Description
14:8	RW	0x00	h264_slice_num the h264 slice numeber in on picture 0=one slice in currect picture 1=two slice in currect picture .....
7:0	RO	0x0	reserved

VEPU_swreg_60
Address: Operational Base + offset (0x00f0)
Register0001 Abstract

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21:16	RW	0x00	strm_st_offset the start offset for stream
15:8	RW	0x00	skip_mb_mode H.264:SKIP macroblock mode
7:6	RO	0x0	reserved
5:4	RW	0x0	right_spill the right edge of image for spill pixels div4 value range:0~3
3:0	RW	0x0	bot_spill the bottom edge of image for spill pixels the bottom edge of image for spill pixels

VEPU_swreg_61
Address: Operational Base + offset (0x00f4)
input luminance information

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:20	RW	0x0	offset_in_chroma then offset of input chroma byte unit
19	RO	0x0	reserved
18:16	RW	0x0	offset_in_luma then offset of input luminance byte unit
15:14	RO	0x0	reserved
13:0	RW	0x0000	row_len_in_luma the row length of input luminance

VEPU_swreg_62
Address: Operational Base + offset (0x00f8)
rlc_sum

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21:0	RW	0x000000	rlc_sum rlc_sum rlc_sum

VEPU_swreg_63
Address: Operational Base + offset (0x00fc)
the reconstructed luma start address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	recon_luma_st_adr the reconstructed luma start address the reconstructed luma start address

VEPU_swreg_64
Address: Operational Base + offset (0x0100)
the reconstructed chroma start address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	recon_chroma_st_adr the reconstructed chroma start address the reconstructed chroma start address

VEPU_swreg_65_reuse
Address: Operational Base + offset (0x0104)
checkpoint 1 and 2

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	h264_chkpt_1 1st word used for check point used in h.264 1st word used for check point used in h.264
15:0	RW	0x0000	h264_chkpt_2 2st word used for check point used in h.264 2st word used for check point used in h.264

VEPU_swreg_66_reuse
Address: Operational Base + offset (0x0108)
checkpoint 3 and 4

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	h264_chkpt_3 3st word used for check point used in h.264 3st word used for check point used in h.264
15:0	RW	0x0000	h264_chkpt_4 4st word used for check point used in h.264 4st word used for check point used in h.264

VEPU_swreg_67_reuse

Address: Operational Base + offset (0x010c)
checkpoint 5 and 6

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	h264_chkpt_5 5st word used for check point used in h.264 5st word used for check point used in h.264
15:0	RW	0x0000	h264_chkpt_6 6st word used for check point used in h.264 6st word used for check point used in h.264

VEPU_swreg_68_reuse
Address: Operational Base + offset (0x0110)
checkpoint 7 and 8

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	h264_chkpt_7 7st word used for check point used in h.264 7st word used for check point used in h.264
15:0	RW	0x0000	h264_chkpt_8 8st word used for check point used in h.264 8st word used for check point used in h.264

VEPU_swreg_69_reuse
Address: Operational Base + offset (0x0114)
checkpoint 9 and 10

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	h264_chkpt_9 9st word used for check point used in h.264 9st word used for check point used in h.264
15:0	RW	0x0000	h264_chkpt_10 10st word used for check point used in h.264 10st word used for check point used in h.264

VEPU_swreg_70_reuse
Address: Operational Base + offset (0x0118)
checkpoint word error 1 and 2

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	h264_errchkpt_1 1st word error check point used in h.264 1st word error check point used in h.264
15:0	RW	0x0000	h264_errchkpt_2 2st word error check point used in h.264 2st word error check point used in h.264

VEPU_swreg_71_reuse
Address: Operational Base + offset (0x011c)
checkpoint word error 1 and 2

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	h264_errchkpt_3 3st word error check point used in h.264 3st word error check point used in h.264
15:0	RW	0x0000	h264_errchkpt_4 4st word error check point used in h.264 4st word error check point used in h.264

VEPU_swreg_72_reuse
Address: Operational Base + offset (0x0120)
checkpoint word error 1 and 2

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	h264_errchkpt_5 5st word error check point used in h.264 5st word error check point used in h.264
15:0	RW	0x0000	h264_errchkpt_6 6st word error check point used in h.264 6st word error check point used in h.264

VEPU_swreg_73_reuse
Address: Operational Base + offset (0x0124)
checkpoint delta QP register

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	chkqp_1 1st for delta qp check point 1st for delta qp check point
23:20	RW	0x0	chkqp_2 2st for delta qp check point 2st for delta qp check point
19:16	RW	0x0	chkqp_3 3st for delta qp check point 3st for delta qp check point
15:12	RW	0x0	chkqp_4 4st for delta qp check point 4st for delta qp check point
11:8	RW	0x0	chkqp_5 5st for delta qp check point 5st for delta qp check point
7:4	RW	0x0	chkqp_6 6st for delta qp check point 6st for delta qp check point
3:0	RW	0x0	chkqp_7 7st for delta qp check point 7st for delta qp check point

VEPU_swreg_74
Address: Operational Base + offset (0x0128)
input image format

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	mad_thsld MAD threshold value = (MAD threshold)/256
23:16	RW	0x00	encodered_slices the number of encoder slices which used in h.264 the number of encoder slices which used in h.264
15:8	RO	0x0	reserved
7:4	RW	0x0	img_fmt_in input image format. YUV420P YUV420SP YUV422 UYVY422 RGB565 RGB444 RGB888 RGB101010
3:2	RW	0x0	img_in_rot the input image rotation 0 : no rotation 1 : rotate right 90 degress 2 : rotate left 90 degress
1	RO	0x0	reserved
0	RW	0x0	nal_mode the output of NAL size to base control the output of NAL size to base control

VEPU_swreg_75
Address: Operational Base + offset (0x012c)
intra/inter mode

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	intramod_16x16 the Intra prediction for 16x16 mode favor
15:0	RW	0x0000	intermod the intra/inter selection for inter macro block mode favor the intra/inter selection for inter macro block mode favor

VEPU_swreg_76_reuse
Address: Operational Base + offset (0x0130)
encoder control regsiter 0

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:26	RW	0x00	pps_init_qp pps init qp in picture used in h264 pps init qp in picture used in h264 range : 0~51
25:22	RW	0x0	slice_flt_alpha the offset of slice filter alpha c0 used in h264 offset div2 range : -6~6
21:18	RW	0x0	slice_flt_beta the filter beta offset for h264 slice config value = (real value)/2 signed register range : -6 ~6
17:13	RW	0x00	qp_offset_ch the qp index offset for chroma qp used in h264 signed register range : -12~12
12:9	RO	0x0	reserved
8	RW	0x0	sw_qpass jpeg enc quant bypass
7:5	RO	0x0	reserved
4:1	RW	0x0	idr_picid IDR pic ID IDR pic ID
0	RW	0x0	constr_intra_pred constrained intra prediction constrained intra prediction

VEPU_swreg_77
Address: Operational Base + offset (0x0134)
output stream start address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	output_strm_st_adr output stream start address output stream start address

VEPU_swreg_78
Address: Operational Base + offset (0x0138)
output control start address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	output_ctrl_st_adr output control start address output control start address

VEPU_swreg_79
Address: Operational Base + offset (0x013c)
next picture luminance start address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	next_luma_st_adr next picture luminance start address next picture luminance start address

VEPU_swreg_80
Address: Operational Base + offset (0x0140)
Base address for MV output

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mv_out_st_adr MV wr start address

VEPU_swreg_81
Address: Operational Base + offset (0x0144)
the cabac table start address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cabac_table_st_adr the cabac table start address H264: cabac table

VEPU_swreg_82
Address: Operational Base + offset (0x0148)
the first of ROI area register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	first_roi_tmb the top mb column for first roi area (inside area)
23:16	RW	0x00	first_roi_bmb the bottom mb column for first roi area (outside area)
15:8	RW	0x00	first_roi_lmb the left mb column for first roi area qp=qp + roi1_Delta_Qp (inside area)
7:0	RW	0x00	first_roi_rmb the right mb column for first roi area qp=qp - roi1_Delta_Qp (outside area)

VEPU_swreg_83
Address: Operational Base + offset (0x014c)
the second of ROI area register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:24	RW	0x00	second_roi_rmb (inside area)
23:16	RW	0x00	second_roi_bmb (outside area)
15:8	RW	0x00	second_roi_lmb qp=qp + roi1_Delta_Qp (inside area)
7:0	RW	0x00	second_roi_tmb qp=qp - roi1_Delta_Qp (outside area)

VEPU_swreg_84
Address: Operational Base + offset (0x0150)
Stabilization matrix

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:0	RW	0x000000	stab_matrix1 the 1st output of Stabilization matrix (position@ up-left)

VEPU_swreg_85
Address: Operational Base + offset (0x0154)
Stabilization matrix

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:0	RW	0x000000	stab_matrix2 the 2st output of Stabilization matrix (position @ up)

VEPU_swreg_86
Address: Operational Base + offset (0x0158)
Stabilization matrix

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:0	RW	0x000000	stab_matrix3 the 3st output of Stabilization matrix (position @up-right)

VEPU_swreg_87
Address: Operational Base + offset (0x015c)
Stabilization matrix

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0x000000	stab_matrix4 the 4st output of Stabilization matrix (position @ left)

VEPU_swreg_88
Address: Operational Base + offset (0x0160)
Stabilization matrix

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:0	RW	0x000000	stab_matrix5 the 5st output of Stabilization matrix (position @GMV)

VEPU_swreg_89
Address: Operational Base + offset (0x0164)
Stabilization matrix

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:0	RW	0x000000	stab_matrix6 the 6st output of Stabilization matrix (position@right)

VEPU_swreg_90
Address: Operational Base + offset (0x0168)
Stabilization matrix

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:0	RW	0x000000	stab_matrix7 the 7st output of Stabilization matrix (position@down-left)

VEPU_swreg_91
Address: Operational Base + offset (0x016c)
Stabilization matrix

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:0	RW	0x000000	stab_matrix8 the 8st output of Stabilization matrix (position@down)

VEPU_swreg_92
Address: Operational Base + offset (0x0170)
Stabilization matrix

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:26	RW	0x00	stab_gmv_vrtl the output of Stabilization GMV vertical signed register range : -16~16
25:24	RO	0x0	reserved
23:0	RW	0x000000	stab_matrix9 the 9st output of Stabilization matrix (position@down- right)

VEPU_swreg_93
Address: Operational Base + offset (0x0174)
the output of Stabilization motion sum

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	stab_motion_sum the output of Stabilization motion sum read value = (real value)/8 range : 0~1089*253*255*53/8

VEPU_swreg_94
Address: Operational Base + offset (0x0178)
output of Stabilization

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	stab_min_value the minimum value output of Stabilization range : 0~255*253*253
7:6	RW	0x0	stab_mod_sel the mode select of Stabilization 0 : disabled 1 : stab only 2 : stab+encode
5:0	RW	0x00	stab_hor_gmv the horizontal output of Stabilization GMV signed register range : -16~16

VEPU_swreg_95
Address: Operational Base + offset (0x017c)
RGB to YUV conversion coefficient register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	rgb2yuv_coe2 the 2st conversion coefficien for RGB to YUV the 2st conversion coefficien for RGB to YUV
15:0	RW	0x0000	rgb2yuv_coe1 the 1st conversion coefficien for RGB to YUV the 1st conversion coefficien for RGB to YUV

VEPU_swreg_96
Address: Operational Base + offset (0x0180)
RGB to YUV conversion coefficient register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	rgb2yuv_coe5 the 5st conversion coefficien for RGB to YUV the 5st conversion coefficien for RGB to YUV
15:0	RW	0x0000	rgb2yuv_coe3 the 3st conversion coefficien for RGB to YUV the 3st conversion coefficien for RGB to YUV

VEPU_swreg_97
Address: Operational Base + offset (0x0184)
RGB to YUV conversion coefficient register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	rgb2yuv_coe6 the 6st conversion coefficien for RGB to YUV the 6st conversion coefficien for RGB to YUV

VEPU_swreg_98
Address: Operational Base + offset (0x0188)
RGA MASK

Bit	Attr	Reset Value	Description
31:21	RO	0x0	reserved
20:16	RW	0x00	bcmpt_mask_postition the mask msb bit position of rgb B-component range : 0~31
15:13	RO	0x0	reserved
12:8	RW	0x00	gcmpt_mask_postition the mask msb bit position of rgb G-component range : 0~31
7:5	RO	0x0	reserved
4:0	RW	0x00	rcmpt_mask_postition the mask msb bit position of rgb R-component range : 0~31

VEPU_swreg_99
Address: Operational Base + offset (0x018c)
mv related

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:21	RW	0x000	mv_1p_ply 1p of differential MV penalty differential MV penalty for 1p

Bit	Attr	Reset Value	Description
20:11	RW	0x000	mv_1p_4p_ply 1p or 4p of differential MV penalty ME. DMVPenaltyQp
10:1	RW	0x000	mv_4p_ply 4p of differential MV penalty
0	RW	0x0	mutimv_en on-off flag for using exceed one mv every mb on-off flag for using exceed one mv every mb

VEPU_swreg_100_reuse
Address: Operational Base + offset (0x0190)
QP register

Bit	Attr	Reset Value	Description
31:26	RW	0x00	h264_init_luma_qp Initial luma qp used in h264 range: 0~51
25:20	RW	0x00	h264_max_qp H.264 Minimum QP range : 0~51
19:14	RW	0x00	h264_min_qp Minimum QP range:0~51
13	RO	0x0	reserved
12:0	RW	0x0000	h264_chkpt_distance checkpoint distance for macro block checkpoint distance for macro block

VEPU_swreg_101_read
Address: Operational Base + offset (0x0194)
hw config reg

Bit	Attr	Reset Value	Description
31:12	RO	0x1f522	HW_CONFIG Field0000 Description
11:0	RO	0x780	MAX_VID_WIDTH Field0000 Description

VEPU_swreg_102
Address: Operational Base + offset (0x0198)
mvc related

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:20	RW	0x0	mv_favor_16x16 Zero 16x16 MV favor value = (real value)/2.

Bit	Attr	Reset Value	Description
19:11	RW	0x000	mv_ply_4x4 4x4 Mv Penalty
10:8	RW	0x0	mvc_view_id MVC view_id
7	RW	0x0	mvc_anchor_pic_flag to specifie picture is one part of anchor access unit
6:4	RW	0x0	mvc_priority_id MVC priority_id
3:1	RW	0x0	mvc_temporal_id MVC temporal_id
0	RW	0x0	mvc_inter_view_flag the inter-view prediction of picture MVC inter_view_flag.

VEPU_swreg_103
Address: Operational Base + offset (0x019c)
encoder start

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:20	RW	0x000	enc_height encoderd height lum height (macroblock unit) H264: [6..255] JPEG: [6..511]
19:17	RO	0x0	reserved
16:8	RW	0x000	enc_width the encoder width lum width (macroblock unit) H264: range : 9~255 JPEG: range : 6~511
7:6	RW	0x0	enc_frame_type frame type selected for current frame 0: INTER 1: INTRA(IDR) 2: MVC-INTER
5:4	RW	0x0	enc_fmt encoding format selected 2 : JPEG 3 : H264
3:1	RO	0x0	reserved
0	RW	0x0	enc_en encoder enable flag encoder enable

VEPU_swreg_104
Address: Operational Base + offset (0x01a0)
mb control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mb_count_out mb_count_out mb_count_out
15:0	RW	0x0000	mb_cnt macroblock_count macroblock_count

VEPU_swreg_105
Address: Operational Base + offset (0x01a4)
SWAP

Bit	Attr	Reset Value	Description
31	RW	0x0	swap8_in input swap 8-bits or not flag 0: no swap 1: swap 8bit
30	RW	0x0	swap16_in input swap 16-bits or not flag 0: no swap 1: swap 16bit
29	RW	0x0	swap32_in input swap 32-bits or not flag 0: no swap 1: swap 32bit
28	RW	0x0	swap8_out output swap 8-bits or not flag 0: no swap 1: swap 8bit
27	RW	0x0	swap16_out output swap 16-bits or not flag 0: no swap 1: swap 16bit
26	RW	0x0	swap32_out output swap 32-bits or not flag 0: no swap 1: swap 32bit
25	RO	0x0	reserved
24	RW	0x0	test_irq test irq
23:20	RW	0x0	test_counter test counter test counter

Bit	Attr	Reset Value	Description
19	RW	0x0	coher_test_reg test register coherency test register coherency
18	RW	0x0	coher_test_mem test memory coherency test memory coherency
17:0	RW	0x00000	test_len test data length

VEPU_swreg_106_reuse
Address: Operational Base + offset (0x01a8)
encoder control register 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	pic_para_id H.264 picture parameter id set
23:16	RW	0x00	intra_pred_mode intra prediction previous fpr 4x4 mode favor used in h264 H.264 intra prediction previous 4x4 mode favor
15:0	RW	0x0000	frame_num H.264 frame number

VEPU_swreg_107_reuse
Address: Operational Base + offset (0x01ac)
JPEG control regsiter

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	mv_ply_16x8_8x16 Penalty for using 16x8 or 8x16 MV. Penalty for using 16x8 or 8x16 MV
19:10	RW	0x000	mv_ply_8x8 Penalty for using 8x8 MV Penalty for using 8x8 MV
9:0	RW	0x000	mv_ply_8x4_4x8 Penalty for using 8x4 or 4x8 MV. Penalty for using 8x4 or 4x8 MV.

VEPU_swreg_108_reuse
Address: Operational Base + offset (0x01b0)
intra_slice_bmp2

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	intra_slice_bmp2 Field0000 Abstract bit0 : slices64 bit1 : slices65 bit2 : slices66 ..... bit31 : slices95

VEPU_swreg_109
Address: Operational Base + offset (0x01b4)
encoder status

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	int_non Field0000 Abstract Field0000 Description
27:25	RO	0x0	reserved
24	RW	0x0	mv_sad_wren the each MB MV and SAD be writed to mv_wr_st_adr enable
23:21	RO	0x0	reserved
20	RW	0x0	rocon_write_dis write reconstructed image disable flag
19:17	RO	0x0	reserved
16	RW	0x0	slice_rdyint_en enable slice ready interruupt enable slice ready interruupt
15:13	RO	0x0	reserved
12	RW	0x1	clk_gating_en clock gating enable flag default clk_gating_en =1'b1
11	RO	0x0	reserved
10	RW	0x0	int_timeout_en enable interrupt for timeout
9	RW	0x0	irq_clr irq clear
8	RW	0x0	irq_dis irq disable
7	RO	0x0	reserved
6	RW	0x0	irq_timeout HW wait timeout flag
5	RW	0x0	irq_buffer_full buffer full flag
4	RW	0x0	irq_bus_error bus error irq

Bit	Attr	Reset Value	Description
3	RW	0x0	fuse_int Field0000 Abstract Field0000 Description
2	RW	0x0	irq_slice_ready slice ready flag
1	RW	0x0	irq_frame_rdy one frame encoder sucess flag
0	RW	0x0	enc_irq enc interrupt

VEPU_swreg_110_read
Address: Operational Base + offset (0x01b8)
product ID

Bit	Attr	Reset Value	Description
31:16	RO	0x4831	prod_id Product ID
15:12	RO	0x1	major_num Major number
11:4	RO	0x22	minor_num Minor number
3:0	RO	0x0	synthesis

VEPU_swreg_120_183
Address: Operational Base + offset (0x01e0)
DMV_4p_1p_penalty

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	dmv_ply_table DMV 4p/1p penalty table values addr range : 0x01e0~0x02dc swreg120: DMV 4p/1p penalty table values swreg121: DMV 4p/1p penalty table values swreg122: DMV 4p/1p penalty table values swreg123: DMV 4p/1p penalty table values ..... swreg183: DMV 4p/1p penalty table values

5.5.6 MMU Registers Summary

Name	Offset	Size	Reset Value	Description
mmu_DTE_ADDR	0x0000	W	0x00000000	MMU current page Table address
mmu_STATUS	0x0004	W	0x00000018	MMU status register
mmu_COMMAND	0x0008	W	0x00000000	MMU command register
mmu_PAGE_FAULT_ADDR	0x000c	W	0x00000000	MMU logical address of last page fault
mmu_ZAP_ONE_LINE	0x0010	W	0x00000000	MMU Zap cache line register

Name	Offset	Size	Reset Value	Description
mmu_INT_RAWSTAT	0x0014	W	0x00000000	MMU raw interrupt status register
mmu_INT_CLEAR	0x0018	W	0x00000000	MMU raw interrupt status register
mmu_INT_MASK	0x001c	W	0x00000000	MMU raw interrupt status register
mmu_INT_STATUS	0x0020	W	0x00000000	MMU raw interrupt status register
mmu_AUTO_GATING	0x0024	W	0x00000001	mmu auto gating

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

5.5.7 MMU Detail Register Description

mmu_DTE_ADDR
Address: Operational Base + offset (0x0000)
MMU current page Table address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MMU_DTE_ADDR mmu dte base addr mmu dte base addr , the address must be 4kb aligned

mmu_STATUS
Address: Operational Base + offset (0x0004)
MMU status register

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:6	RO	0x00	PAGE_FAULT_BUS_ID page fault bus id Index of master reponsible for last page fault
5	RO	0x0	PAGE_FAULT_IS_WRITE page fault acess The direction of access for last page fault: 0 = Read 1 = Write
4	RO	0x1	REPLAY_BUFFER_EMPTY replay buffer empty status 1'b1:The MMU replay buffer is empty
3	RO	0x1	MMU_IDLE mmu idle status The MMU is idle when accesses are being translated and there are no unfinished translated accesses. 1'b1: MMU is idle
2	RO	0x0	STAIL_ACTIVE stall active status MMU stall mode currently enabled. The mode is enabled by command 1'b1: MMU is in stall active status

Bit	Attr	Reset Value	Description
1	RO	0x0	PAGE_FAULT_ACTIVE page fault active status MMU page fault mode currently enabled . The mode is enabled by command. 1'b1: page fault is active
0	RO	0x0	PAGING_ENABLED Paging enabled status 1'b0: paging is disabled 1'b1: Paging is enabled

mmu_COMMAND
Address: Operational Base + offset (0x0008)
MMU command register

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2:0	WO	0x0	MMU_CMD Field0000 Abstract MMU_CMD. This can be: 0: MMU_ENABLE_PAGING 1: MMU_DISABLE_PAGING 2: MMU_ENABLE_STALL 3: MMU_DISABLE_STALL 4: MMU_ZAP_CACHE 5: MMU_PAGE_FAULT_DONE 6: MMU_FORCE_RESET

mmu_PAGE_FAULT_ADDR
Address: Operational Base + offset (0x000c)
MMU logical address of last page fault

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	PAGE_FAULT_ADDR Field0000 Abstract address of last page fault

mmu_ZAP_ONE_LINE
Address: Operational Base + offset (0x0010)
MMU Zap cache line register

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	MMU_ZAP_ONE_LINE Field0000 Abstract address to be invalidated from the page table cache

mmu_INT_RAWSTAT
Address: Operational Base + offset (0x0014)
MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	READ_BUS_ERROR Field0000 Abstract read bus error
0	RW	0x0	PAGE_FAULT Field0000 Abstract page fault

mmu_INT_CLEAR
Address: Operational Base + offset (0x0018)
MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	WO	0x0	READ_BUS_ERROR Field0000 Abstract read bus error
0	WO	0x0	PAGE_FAULT Field0000 Abstract page fault

mmu_INT_MASK
Address: Operational Base + offset (0x001c)
MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	READ_BUS_ERROR Field0000 Abstract read bus error enable an interrupt source if the corresponding mask bit is set to 1
0	RW	0x0	PAGE_FAULT Field0000 Abstract page fault enable an interrupt source if the corresponding mask bit is set to 1

mmu_INT_STATUS
Address: Operational Base + offset (0x0020)
MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RO	0x0	READ_BUS_ERROR Field0000 Abstract read bus error
0	RO	0x0	PAGE_FAULT Field0000 Abstract page fault

mmu_AUTO_GATING
Address: Operational Base + offset (0x0024)
mmu auto gating

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x1	mmu_auto_gating mmu auto gating when it is 1'b1, the mmu will auto gating it self

5.5.8 PREF CACHE Registers Summary

Name	Offset	Size	Reset Value	Description
pref_cache_VERSION	0x0000	W	0xcac20101	VERSION register
pref_cache_SIZE	0x0004	W	0x07110206	L2 cache SIZE
pref_cache_STATUS	0x0008	W	0x00000000	Status register
pref_cache_COMMAND	0x0010	W	0x00000000	Command setting register
pref_cache_CLEAR_PAGE	0x0014	W	0x00000000	clear page register
pref_cache_MAX_READS	0x0018	W	0x0000001c	maximum read register
pref_cache_ENABLE	0x001c	W	0x00000003	enables cacheable accesses and cache read allocation
pref_cache_PERFCNT_SRC0	0x0020	W	0x00000000	performance counter 0 source register
pref_cache_PERFCNT_VAL0	0x0024	W	0x00000000	performance counter 0 value register
pref_cache_PERFCNT_SRC1	0x0028	W	0x00000000	performance counter 0 source register
pref_cache_PERFCNT_VAL1	0x002c	W	0x00000000	performance counter 1 value register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

5.5.9 PREF CACHE Detail Register Description

pref_cache_VERSION
Address: Operational Base + offset (0x0000)
VERSION register

Bit	Attr	Reset Value	Description
31:16	RO	0xcac2	PRODUCT_ID
15:8	RO	0x01	VERSION_MAJOR
7:0	RO	0x01	VERSION_MINOR

pref_cache_SIZE
Address: Operational Base + offset (0x0004)
L2 cache SIZE

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:24	RO	0x07	External_bus_width Log2 external bus width in bits
23:16	RO	0x11	CACHE_SIZE Log2 cache size in bytes
15:8	RO	0x02	ASSOCIATIVITY Log2 associativity
7:0	RO	0x06	LINE_SIZE Log2 line size in bytes

pref_cache_STATUS
Address: Operational Base + offset (0x0008)
Status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	DATA_BUSY set when the cache is busy handling data
0	RW	0x0	CMD_BUSY set when the cache is busy handling commands

pref_cache_COMMAND
Address: Operational Base + offset (0x0010)
Command setting register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x0	COMMAND The possible command is 1 = Clear entire cache

pref_cache_CLEAR_PAGE
Address: Operational Base + offset (0x0014)
clear page register

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	CLEAR_PAGE writing an address, invlidates all lines in that page from the cache

pref_cache_MAX_READS
Address: Operational Base + offset (0x0018)
maximum read register

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x1c	MAX_READS Limit the number of outstanding read transactions to this amount

pref_cache_ENABLE

Address: Operational Base + offset (0x001c)
enables cacheable accesses and cache read allocation

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	sw_cache_clk_disgate cache clk disgate cache clk disgate when it is 1'b0, enable cache clk auto clkgating when it is 1'b1, disable cache clk auto clkgating
2	RW	0x0	sw_readbuffer_counter_reject_en counter reject enable default is 1'b0, for enhance cacheable read performnace in readbuffer. 1'b1: normal origin counter reject
1	RW	0x1	permit_cache_read_allocate cache read allocate 1'b1: permit cache read allocate
0	RW	0x1	permit_cacheable_access cacheable access 1'b1: permit cacheable access

pref_cache_PERFCNT_SRC0
Address: Operational Base + offset (0x0020)
performance counter 0 source register

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6:0	RW	0x00	PERFCNT_SRC0 This register holds all the possible source values for Performance Counter 0 0: disabled 1: total clock cycles 2: active clock cycles 3: read transactions, master 4: word reads, master 5: read transactions, slave 6: word reads, slave 7: read hit, slave 8: read misses, slave 9: read invalidates, slave 10: cacheable read transactions, slave 11: bad hit nmber, slave

pref_cache_PERFCNT_VAL0
Address: Operational Base + offset (0x0024)
performance counter 0 value register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PERFCNT_VAL0 Performance counter 0 value

pref_cache_PERFCNT_SRC1
Address: Operational Base + offset (0x0028)
performance counter 0 source register

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6:0	RW	0x00	PERFCNT_SRC1 This register holds all the possible source values for Performance Counter 1 0: disabled 1: total clock cycles 2: active clock cycles 3: read transactions, master 4: word reads, master 5: read transactions, slave 6: word reads, slave 7: read hit, slave 8: read misses, slave 9: read invalidates, slave 10: cacheable read transactions, slave 11: bad hit nmber, slave

pref_cache_PERFCNT_VAL1
Address: Operational Base + offset (0x002c)
performance counter 1 value register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PERFCNT_VAL1 Performance counter 1 value

5.6 Interface Description

5.7 Application Notes

5.7.1 HEVC Configuration Flow

1. Prepare the data in the DDR.
2. Set the HEVC general system configuration in RKVDEC.swreg2, such as working mode, in/out endian.
3. Set the picture parameters with RKVDEC.swreg3.
4. Set the input and output data base address and HEVC reference configuration with RKVDEC.swreg4~RKVDEC.swreg43.
5. If CABAC error detection is desired, set the RKVDEC.swreg44 to enable the corresponding error detection.
6. Set the interrupt configuration and start the HEVC with HEVC.swreg1.
7. Wait for the frame interrupt, and then get the processed results in the target DDR
8. Clear all the interrupts, and repeat Process2~Process8 to start a new frame decoding if the decoding is not finished yet.

5.7.2 H264 Configuration Flow

1. Prepare the data in the DDR, for normal mode, we should prepare bitstream, tbl, pps and rps.
2. Set the h264 general system configuration in RKVDEC.swreg2, such as working mode, in/out endian.
3. Set the picture parameters with RKVDEC.swreg3.
4. Set the input and output data base address and H264 reference configuration with RKVDEC.swreg4~RKVDEC.swreg43.
5. If stream error detection is desired, set the swreg77_h264_error_e and swreg44_strmd_error_en to enable the corresponding error detection.
6. If prefech function is desired, set the prefetch common registers and clear its TLB. Pay attention, there contains two caches, which are for Y channel and UV channel.
7. If MMU function is desires, set the MMU common registers and clear its TLB. Pay attention, there contains two MMUs, which are for read channel and write channel.
8. Set the interrupt configuration and start the decoder with RKVDEC.swreg1.
9. Wait for the frame interrupt, and then get the processed results in the target DDR. There may be decoded frame, error_info, cur frame colmv output.
When the stream mode is not frame by frame mode,we also wait buf empty,and then send the next pack,repeat it until sw_dec_rdy_sta.
10. Clear all the interrupts, and repeat Process2~Process9 to start a new frame decoding if the decoding is not finished yet.

5.7.3 VP9 Configuration Flow

1. Prepare the data in the DDR, for normal mode, we should prepare bitstream, prob, and segid from last decoded frame.
2. Set the VP9 general system configuration in RKVDEC.swreg2, such as working mode, in/out endian.
3. Set the picture parameters with RKVDEC.swreg3.
4. Set the input and output data base address and HEVC reference configuration with RKVDEC.swreg4~RKVDEC.swreg43.
5. If stream error detection is desired, set the RKVDEC.swreg44 to enable the corresponding error detection.
6. If prefech function is desired, set the prefetch common registers and clear its TLB. Pay attention, there contains two caches, which are for Y channel and UV channel.
7. If MMU function is desires, set the MMU common registers and clear its TLB. Pay attention, there contains two MMUs, which are for read channel and write channel.
8. Set the interrupt configuration and start the decoder with RKVDEC.swreg1.
9. Wait for the frame interrupt, and then get the processed results in the target DDR. There may be decoded frame, cur frame segid, cur frame count, cur frame colmv output.
10. Clear all the interrupts, and repeat Process2~Process9 to start a new frame decoding if the decoding is not finished yet.

5.7.4 Other formats and encoder Configuration flow

1. Prepare the decoder data in the DDR memory, and in decoder other than JPEG decoder, the input stream buffer should at least contain a slice or a frame data, otherwise the decoder will produce an interrupt and show error and then reset itself.
2. Config all the registers will be used. and please notice that which be list as follows:
In encoder----- We can configure the registers to control the input picture data format (such as endian and swap), but some input data format are fixed, such as cabac_table data. And the register VEPU_SWREG0~31 are JPEG quantization registers. They are write only registers. When you want to write these registers, you should first set VEPU_SWREG103[0] to 1'b0 and VEPU_SWREG103[5:4] to 2'b10(select JPEG mode).
In decoder---- The decoder can support ref buffer mode or cacheable mode, but they can't be both enabled. We can config the swreg57[28],swreg57[29] to enable cache and config the swreg65 to control the ref buffer.
4. You should config VDPU_SWREG57[0] as 1'b1 to enable video decoder. And config

VDPU_SWREG41[0] as 1’b1 to enable pp. If pp performed in pipeline with decoder, you should config VDPU_SWREG41[4] as 1’b1 and then config VDPU_SWREG57[0] as 1’b1 to enable decoder and pp. VEPU_SWREG103[0] set to 1’b1 to enable encoder.
5. Wait for the frame interrupt,and then check if the frame decoder ready interrupt is right or not, after that,you can get the processed results in the target DDR
6. Clear all the interrupts,repeat step 2~5 to start a new frame decoder or encoder.

Chapter 6 Image Signal Processing (ISP)

6.1 Overview

The Image Signal Processing (ISP) represents a complete video and still picture input unit. It contains image processing and scaling functions. The integrated image processing unit supports simple CMOS sensors delivering RGB Bayer pattern without any integrated image processing and also image sensors with integrated YCbCr processing.
Scaling is used for downsizing the sensor data for either displaying them on the LCD, or for generating data stream for MPEG-4 compression. Scaling also can be used for digital zoom effects, because the scalers are capable of up-scaling as well.
An image effects block is present which can create images with sepia, black & white, color selection, negative, emboss and sketch effects.
The camera interface provides SMIA and/or MIPI support, so that ISP can be connected to PHY devices or IP blocks directly.
All data is transmitted via the memory interface to a BVCI/AXI bus system using a bus master interface.
Programming is done by register read/write transactions using an PVCI slave interface.
ISP supports the following features:

- Generic Sensor Interface with programmable polarity for synchronization signals
- ITU-R BT 601/656 compliant video interface supporting YCbCr or RGB Bayer data
- 12 bit camera interface
- 12 bit resolution per color component internally
- YCbCr 4:2:2 processing
- Flash light control
- Mechanical shutter support
- Windowing and frame synchronization
- Frame skip support for video (e.g. MPEG-4) encoding
- Macro block line, frame end, capture error, data loss interrupts and sync. (h_start, v_start) interrupts
- Luminance/chrominance and chrominance blue/red swapping for YUV input signals
- Continuous resize support
- Buffer in system memory organized as ring-buffer
- Buffer overflow protection for raw data
- Asynchronous reset input, software reset for the entire IP and separate software resets for all sub-modules
- Interconnect test support
- Semi planar storage format
- Color processing (contrast, saturation, brightness, hue, offset, range)
- Power management by software controlled clock disabling of currently not needed sub-modules
- Read port provided to read back a picture from system memory
- Black level compensation
- Four channel Lens shade correction (Vignetting)
- Auto focus measurement
- White balancing and black level measurement
- Auto exposure support by brightness measurement in 5x5 sub windows
- Defect pixel cluster correction unit (DPCC) supports on the fly and table based pixel correction
- De-noising pre filter (DPF)
- Enhanced color interpolation (RGB Bayer demosaicing)
- Chromatic aberration correction
- Combined edge sensitive Sharpening / Blurring filter (Noise filter)
- Color correction matrix (cross talk matrix)
- Global Tone Mapping with wide dynamic range unit (WDR)
- Image Stabilization support and Video Stabilization Measurement
- Flexible Histogram calculation

- Digital image effects (Emboss, Sketch, Sepia, B/W (Grayscale), Color Selection, Negative image, sharpening)
- Solarize effect through gamma correction
- AXI 64 bit interface 32Bit Address range (two DMA-write ports and one DMA-read port)
- Up to 16 Beat Bursts depending on configured FIFO size
- 32 bit AHB programming interface
- Maximum input resolution of 4416x3312 pixels
- Main scaler with pixel-accurate up- and down-scaling to any resolution between 4416x3312 and 32x16 pixel in processing mode
- Self scaler with pixel-accurate up- and down-scaling to any resolution between 1920x1080 and 32x16 pixel in processing mode
- Support of semiplanar NV21 color storage format
- Support of image cropping

6.2 Block Diagram

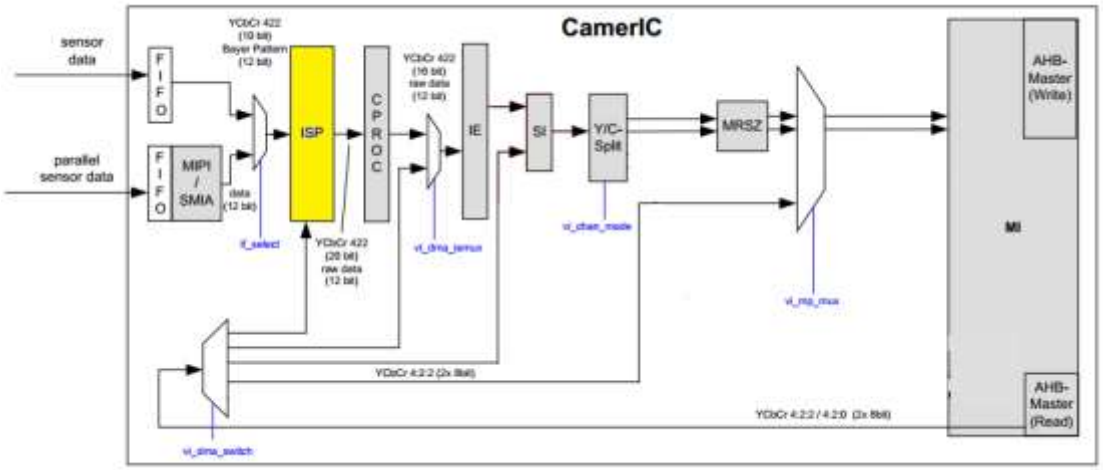


Fig. 6-1 ISP Block Diagram

ISP comprises with:

- MIPI serial camera interface
- Image Signal Processing (ISP)
- Color Processing (CPROC)
- Image Effects (IE)
- Superimpose (SI)
- Luminance /Chrominance Splitter (Y/C Split)
- Crop
- Main Resize (MRSZ)
- MPMUX for selection of main path data flow
- Control Unit

6.3 Function Description

6.3.1 MIPI

The MIPI interface is the second optional serial camera interface of ISP Controller. The interface is implemented according to the CSI2 specification defined by the MIPI Alliance, connecting a PPI data interface to a MIPI_D-PHY physical layer with a 12bits ALOMICs interface.

Features and Standard Compliance

Compliant to MIPI Alliance Standard for Camera Serial Interface 2 (CSI2)

- PPI Interface according to D-PHY specification, Annex A
- Supports up to 4 data lanes (extendable by request)
- Number of lanes is programmable and hardware configurable

- Provides lane merging, error detection and correction, virtual channel detection, programmable data extraction and embedded data separation
- Supported data types are:
  - Generic 8bit data
  - Non-legacy YUV 4:2:0 8bit / 10bit with cosited chroma sampling
  - Non-legacy YUV 4:2:0 8bit / 10bit with non-cosited chroma sampling
  - Legacy YUV 4:2:0 8bit
  - YUV 4:2:2 8bit / 10bit
  - RGB 444 / 555 / 565 / 666 / 888 image data
  - RAW 6-bit / 7-bit / 8-bit / 10-bit / 12-bit image data
  - User-defined 8-bit data
- PVCI similar output interface
- PVCI control interface

RAW 14-bit image data types are not supported. The MIPI D-PHY-Layer features Escape Modus and Low Power Data Transfer are not needed for the Protocol Receiver. According to the CSI2 specification only unidirectional high-speed data transfer is mandatory for the camera interface.

6.3.2 ISP Block

The ISP block includes the interface to the attached parallel sensor device and the MIPI interfaces. It accepts either ITU-R BT 601 YCbCr, well as raw Bayer data or ITU-R BT 656 YCbCr data. The order of Y and Cx as well as Cb and Cr is programmable. It contains the interpolation filter for the raw Bayer to plain RGB conversion.
An input acquisition window is programmable supporting detection of smaller than programmed input images. An error IRQ is generated in case of input error conditions.
The ISP allows programming of a continuous image sampling mode, or a mode where the number of images to be sampled subsequently can be programmed (1…1023).
Additionally it incorporates image quality improvements (gamma correction, black level subtraction, white balancing, etc.).
The ISP block supports also auto exposure capabilities by providing image color statistics information to the system processor for correct sensor device programming.
The input part of the ISP block is fully programmable in terms of signal polarities, active video data positions, and luminance/chrominance order.
The ISP block always delivers YCbCr 4:2:2 data at its output port. Data provided by the RGB channel are downsampled to YCbCr 4:2:2, supporting both co-sited and non co-sited calculation. Luminance and chrominance data are provided in parallel using line and frame end signals. In raw data mode (unprocessed data) these data are transferred via the Y port. Handshaking is used for data qualification. As the sensor device cannot be stopped delivering data the backward handshake (acknowledge) is only used for pixel drop detection which is signaled using an IRQ. To prevent pixel dropping a latency FIFO is implemented. The FIFO depth can be option of customization.
The ISP block also contains its own programming registers to be accessed by a 32 bit PVCI compliant interface supporting single transfers only.
The incoming hsync and vsync control signals from the camera are connected to interrupt logic. It is possible to trigger on these signals for an event triggered configuration during processing.

1. DPCC

The ISP core is designed to operate with high-end, mid-range and low-end image sensors, which mainly differ in the number of pixels and module cost. While high-end sensors aim at a high number of pixels with sufficiently large pixel area, low-cost modules often have a large number of defects. Additionally, for low cost sensors in the manufacturing process no time is available for determining the defect pixels locations.
Another problem is that hot pixels get visible at long integration times and can get a high density up to 5%. This means 250000 defect pixels for a 5 Megapixel sensor.
An improved algorithm has been developed, named Defect Pixel Cluster Correction (DPCC). This is an on-the-fly detection and replacement processing as well as a table based replacement method

Defect Pixel Detection

For each pixel threshold values are calculated by several methods, using the correlation of neighbor pixel of the same color (red, green or blue) with exception of the peak gradient estimation for red and blue that also uses the green pixel values in the 5x5 neighborhood of the raw Bayer image. These methods use statistical properties and linear prediction to determine if a pixel needs to be marked as defect. A 3x3 sorting algorithm with rank estimation including the calculation of median values of some pixel groups is a central unit. Output of the detection unit is a marker signal for the following correction stage to indicate, if the current pixel is defect. The detection can be controlled by programmable threshold values, factors and options which methods should be used. The correct setting of the thresholds is important for a good separation between defects and keeping high resolution and detail features in the image.

Defect Pixel Table control

A defect pixel table is implemented as SRAM of user defined size containing entries with defect pixel coordinates. The table control generates a replace flag independently from the on-the-fly detection, so that table correction and on-the-fly correction can be operated in parallel.

Defect Pixel Replacement

Basic algorithm is a switching median filter, which performs sorting and rank ordering. The replacement unit takes the information of the Defect Pixel Detection as input. It uses a statistical sorting filter (median filter) separately for each color to determine the nearest neighbor value for replacement. The filter size is 4 (upper, lower, left and right neighbor for red/blue or diagonal neighbors for green) optionally 5, including the center pixel. The condition for successful replacement is that NOT more than 4 of 9 pixels are defect. So correction of single and small cluster defects of 1x3 (3x1) and 2x2 pixels is possible (please note these clusters belong to a single color in the bayer pattern).

2. Auto Focus Measurement

An auto-focus measurement block is implemented to support auto-focus control. A substantial part of auto-focus control will be done software supported: The search algorithm which looks for maximum sharpness in the image is implemented using software and the movement of the lens is controlled by software. The auto-focus module which is implemented using hardware delivers measurement values of image sharpness via a register interface.

The module measures the sharpness in 3 windows of selectable size via register settings. The auto-focus measurement block uses the line buffer of the emosaicing block. The data in the buffer are stored in Bayer format and read 3-line-wise (top, middle, bottom).

3. Filter (Noise Reduction, Sharpness, Blurring)

As mentioned above, high-end, mid-range and low-end image sensors mainly differ in the number of pixels and module cost. While high end sensors aim at a high number of pixels with sufficiently large pixel area, low-cost modules have small pixels and lens with small diameter. This combination of small lens diameter and small pixels results in higher pixel noise at a given level of illumination than in high end sensors.

To improve the visual image quality, noise and artifacts of the Bayer Matrix should be eliminated and sharpness should be increased. These are requirements which cannot be easily combined.

Noise and the artifacts of the Bayer pattern must be eliminated by averaging or blurring filters. Sharpness could be improved by a high pass or Laplace filter.

Texture detection allows detecting planes or edges, high or low density of details.

With this texture information an adaptive filter is controlled which reduces noise in planes and improves sharpness in detailed regions. If there are less details below or near the noise level two-dimensional blurring is applied. With a higher detail level, the blurring is done along detected edges or lines. If improvement of sharpness is required, the sharpness will be enhanced orthogonally to the direction of the blurring operation.

For example if a horizontal edge is detected, blurring will be done in horizontal direction and sharpness will be improved in vertical direction. In regions with highest contrast and details the filter can be bypassed or if sharpness improvement is required, a two dimensional sharpness filter is realized.

Additionally if no noise reduction is required a fixed blurring or sharpness filter can be selected. The sharpness can be improved by a fixed sharpness filter or edge depending as described beyond.

The noise reduction level can be adapted by the filter coefficients which determine the weightiness of averaging, and by the threshold values which are compared with the texture detection results.
For an optimal noise reduction it is important to know the effective noise level. If the noise level is too high, the noise cannot be eliminated at the best possible rate. If the noise level is low and the noise reduction level is too high, too much details of the image will be lost unnecessarily.
If the light conditions are known, the noise level can be estimated using a table from the exposure settings of the image sensor. If the noise level must be calculated e.g. from the variance of the image RGB data, it is difficult to decide if the variance is caused by the noise or by image patterns.
In addition the hardware effort for separate filters is high because of the necessary line buffers. Therefore the filter algorithm is combined with demosaicing, so that the same line buffer can be used for demosaicing, noise filtering and blurring/sharpening.
The combined demosaicing filter module is designed to operate with linear RGB white balanced Bayer Data. So for best results of interpolation for demosaicing and of texture detection the RGB data should be optimal white balanced.

4. Video Stabilization

The ISP Controller Video Stabilization consists of the following components

- Video Stabilization Measurement
- Video Stabilization Software
- ISP Image Stabilizer

The Video Stabilization Measurement is done in hardware. It calculates per image the horizontal and vertical displacement vector for global motion in comparison to the previous image.
The Video Stabilization Software reads these measurements values, applies some smoothing algorithms and provides the respective cropping window to the ISP Image Stabilization.
The ISP Image Stabilization crops the image with respect to the given cropping window.
The cropping of an image has to be done after the video stabilization measurement for the image has been completed. This involves the usage of at least 1 frame buffer in system memory.
The Image Stabilizer unit delivers YUV data (either unmodified YUV data received as ITU-R BT.601 or ITU-R BT.656 data or color-processed image data) to the following ISP Controller environment.
The Video Stabilization process is currently limited to input line sizes of 2048 pixels and output line sizes of 1280 pixels.

5. Mechanical Shutter Control

With increasing sensor resolution the expectation of high quality pictures also rises. Therefore the exposure control must be decoupled from the frame rate and data read-out. This can be achieved by a mechanical shutter. The mechanical shutter control supports shutter speeds from 1/4000 sec to 10.7 sec by 48-100MHz.

6. Flash Light Control

The sensor interface supports triggering of a LED or tube flash light. The flash light output and the prelight output can be used to control a flash light device. Both the flash light and the prelight are activated by a trigger event. This event may either be a positive or negative edge from the camera or a positive edge from any other trigger source at the input port 'vds_vsync'.
Signal polarity, flash delay time and flash light time are determined by programming respective configuration register.

7. Histogram Calculation

A histogram function is implemented which counts the number of pixels with the same value. In general this histogram is a graphical representation of the pattern of variation that exists in the intensity values of the color or luminance planes.
Usually it is displayed by vertical bars drawn to indicate frequency levels of data collected within specific ranges. This measurement block can be used for different purposes. The most obvious application is an informative display for the end user. It is used for improving the exposure control, which is done by a software control loop.

Histogram Calculation is done independently for 5x5 windows which is important for advanced and fast auto exposure algorithms with complex scene detection.

8. Lens Shading Correction

The lens shading correction deals with the problems of vignetting and lens shading. It is done during input data processing: If the lens shading correction is enabled, each pixel is processed and corrected according to the stored settings. The lens shading correction is done by multiplying each input pixel with its respective correction value.

Only the correction factors at predefined sector corners as well as the sector positions are stored. The pixel position specific correction values are calculated using bilinear interpolation. The correction factors at the sector corners are calculated during a calibration process which uses one or more reference frames which have to be captured under dedicated light conditions and at a dedicated position of the sensor. The captured frames are evaluated by software and the calculated parameters for lens shading correction are stored in multiple illumination specific tables e.g. in external memory or on a flash device. The software controls the lens shading process by loading or updating the correct tables into the hardware module.

It is also possible to use different lens shading correction parameters for different environment conditions, e.g. lightness, light direction or sensor position.

9. Wide Dynamic Range (WDR)

ISP contains a global tone and color mapping unit for Wide Dynamic Range (WDR) compression. Compared with a standard camera, the dynamic range of input intensities appears to be widened, since more structure becomes visible out of the dark and bright image regions.

The dynamic range of real-word scenes is much higher than the available dynamic range of low cost CMOS image sensors. The image sensor thus captures a small range of the real word's scene radiance and maps it to the available output range of the sensor. Radiance levels above or below the sensor's value range are clipped to black or white in the sensor.

The auto-exposure control (AEC) controls which portion of the scene radiance is mapped to the sensor value range. The AEC uses a model-driven scene evaluation to determine the best exposure value.

Nevertheless, there is a chance that portions in the scene are mapped to the dark grey tones or near white tones. This is the case especially in high contrast scenes, when there is anyhow not the chance to perfectly reproduce the full scene radiance range.

Global tone mapping can be used to reduce this effect. It aims at shifting textures in dark grey or near white tones into the mid tone range and thus allows to optimize the perceptual reproduction of the scene. Compared with a standard camera, the dynamic range of input intensities appears to be widened, since more structure becomes visible out of the dark and bright image regions.

This step is being performed directly before the Gamma-Correction. Basically by applying a scene dependent tone curve the required intensity shift is being performed.

During this step the following constraints have to be considered:

- Shifting of textures from dark grey into mid tones increases noise. Thus this step should only be performed for images with a sufficiently low noise level in dark grey tones.
- Changing the intensity level of a pixel also effects the color saturation. In order to avoid color clipping a correction of the color saturation is to be performed. This ensures that after tone mapping the colors have the same hue as before.

The tone and color clipping correction unit for wide dynamic range applications (WDR) performs scene dependent correction such as brightening of dark texture tones. Suitably, the denoising pre-filter is being used for edge-preserving noise reduction especially in dark textures. Additionally, color clipping compensation is being performed with tone mapping.

6.3.3 Color Processing

The Color Processing block is responsible for color processing functions, i.e. hue, contrast, brightness, and saturation adjustment. It operates at YCbCr 4:2:2 data.

6.3.4 Image Effects (IE)

The Image Effects block modifies an image by pixel modifications. A set of different modifications can be applied: grayscale-, sepia-, color selection-, negative-, emboss-, sketch and sharpening effects

In addition a solarize effect can be created by using the gamma block of ISP Controller (for more information an application note is available).
The Image Effects module gets YCbCr 4:2:2 data via a 16 bit ([15:8]: Y, [7:0]: Cb/Cr) data interface.

IE Feature

- Data input- and output handshake interface
- Supports YCbCr 4:2:2 format
- 3x3 Laplace Filter (for picture edge extraction used for emboss, sketch and sharpening effects)
- ITU-R BT.601 compliant YCbCr to RGB conversion (used for the color selection effect to compare red green blue components of a pixel with defined threshold values)

6.3.5 Super Impose (SI)

The Super Impose module overlays an image with a bitmap from the main memory

- Color of the transparent area in superimpose bitmap is configurable. So the camera picture interfuses through the transparent area (A).
- Furthermore the Superimpose block is able to position a bitmap with the appropriate coordinates over the camera image range (B).

The Super Impose module gets picture data in YCbCr 4:2:2 formats via a 16 bit data interface from the Image Effects module. The Memory Interface module delivers the Y, Cb and Cr pixel components of the superimpose bitmap through three independent handshake data interfaces. Within the common area of the two pictures, output pixel data is determined by the bitmap from main memory or by the image from the Image Effects module.

6.3.6 Luminance/Chrominance Splitter (YC_Split)

The Luminance / Chrominance Splitter is responsible for providing component separated YCbCr 4:2:2 pixel data for further processing. Therefore it has to split the data path for chrominance and luminance values.

6.3.7 Resize

The Resize Modules get pictures in YCbCr 4:2:2 format, and scale them by an arbitrary factor up or down to a new format. See following Figure for a module overview:

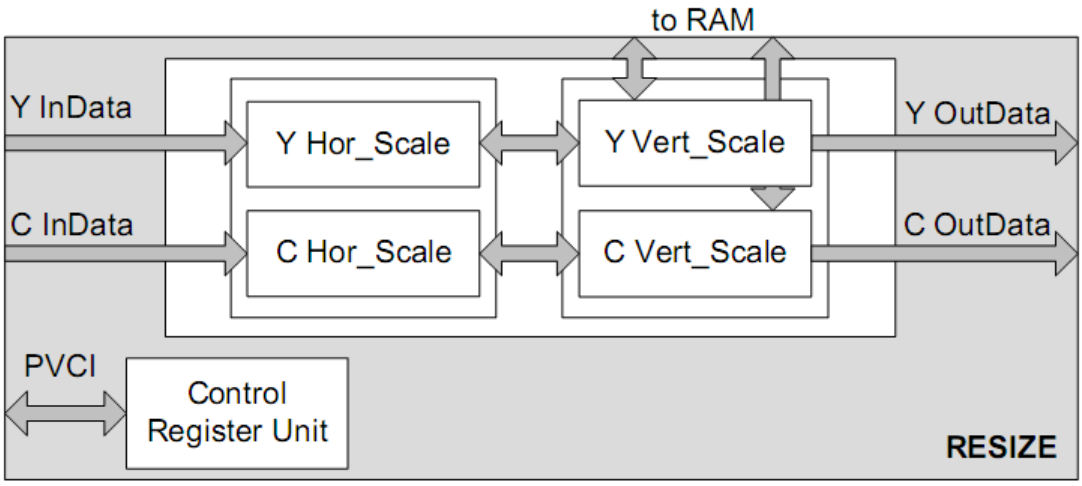


Fig. 6-2 Block Diagram of the Resize Module

Feature and Standard Compliance

PVCI compliant control port

- Data input and output handshake interfaces
- Supports 4:2:2 YCbYCr input format
- Different output formats (4:2:2, 4:2:0, 4:1:1, 4:1:0) possible by choosing from different scaling factors for luminance and chrominance components
- Support of cosited and non-cosited output formats via programmable phase offsets
- Discrete bypassing of each submodule is possible
- Output frame size for Main Picture Scaler (MRSZ) is up to 64 Mpixels.

The Resize module is configurable for horizontal and vertical up- or down-scaling.

Discrete values for the scaling factors of the luminance and the two chrominance components allow conversion between YUV4:2:2 and YUV4:2:0 color format and support of uneven line width.
Phase shift registers are provided to shift the output pixel positions with respect to the input pixel positions. This allows for e.g. format conversion between cosited and non-cosited color schemes.
In sensor mode the MRSZ block supports only down-scaling. This is because the sensor cannot be stopped from delivering data during one frame.
The Resize module is able to process luminance and chrominance data independently, i.e. there are separate pipelines for luminance and chrominance processing using dedicated scale factors and phase offsets. This allows format conversion to be done by the Resize block (YCbCr 4:2:2 to 4:2:0, 4:1:1, 4:1:0).

6.3.8 Memory Interface (MI)

The Memory Interface block provides three data bus master ports to the system memory, two write ports and one read port.
Write Port
The Memory Interface is responsible for collecting the internal data streams and writing them into system memory. Therefore it is attached to data bus master wrappers to access (write) the system bus.
The following types of data streams are supported:
- Raw 8 or 12 bit data
- 2x 8 bit Y, Cb/Cr main image data

The following modes of operation must be supported:
- Raw data only
- Main image data only
- Semi-planar mode

The image data has to be split into Y, Cb and Cr data to be separately written into system memory. So the Memory Interface (write port) consists of six FIFOs for the data.
The FIFOs are necessary for the component separated data streams of main path. Some of the FIFOs have to be re-used for the raw data. See Fig.32-3 for the definition of memory buffers and Fig.32-4 for the storage scheme in planar and semi-planar mode.

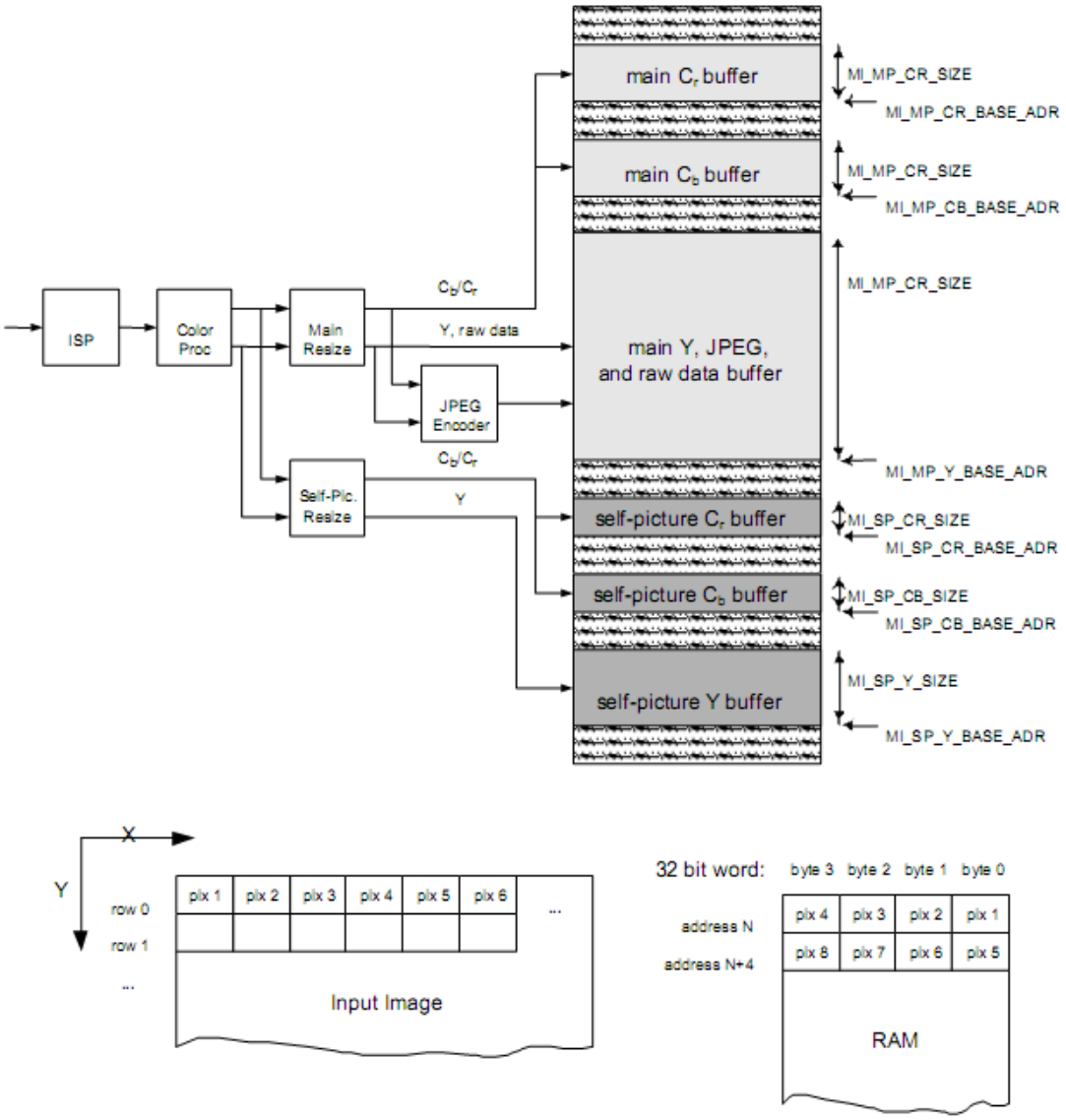


Fig. 6-3 Definition of Memory Buffers

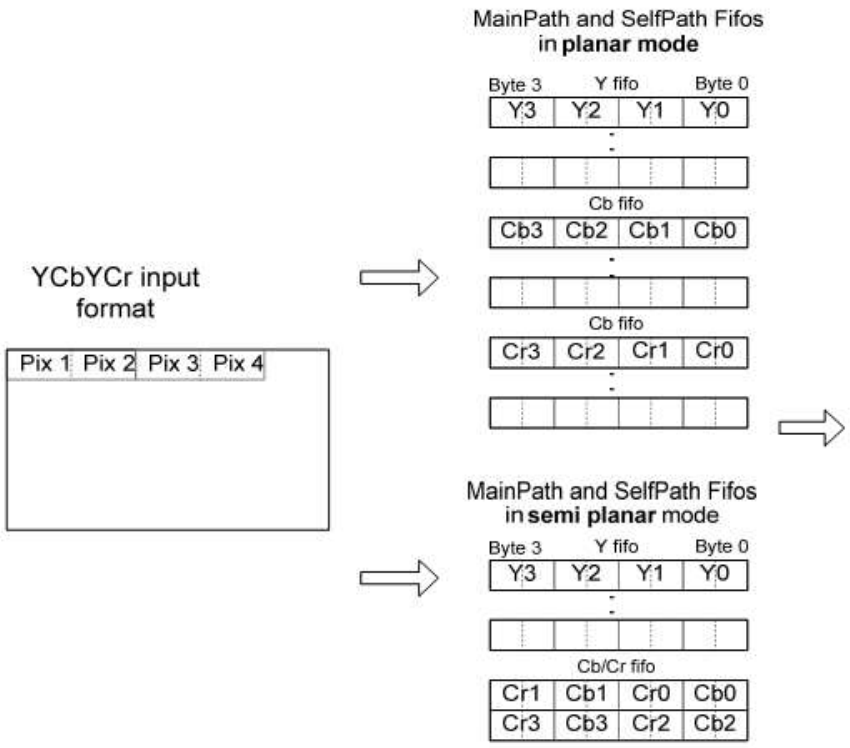


Fig. 6-4 Storage Scheme in Planar and Semi-plannar Mode

Read port (DMA)

The Memory Interface also supports reading back picture data from the system memory. Therefore it is attached to a second data bus master wrapper to access (read) the system data bus.

Three independent read channels are provided to accommodate the three color components of a picture. The picture has to be stored component separated (planar) in system memory. If one or two components are not used they can be turned off by programming the respective component size to zero. So it's also possible to read back raw data through one single channel.

The Memory Interface (read port) consists of three FIFOs, one FIFO per channel. Each FIFO features a PVCI interface at the output, so data can be easily halted by de-asserting the acknowledge line.

6.3.9 Control Unit

The Control Unit serves two purposes:

1. Interface o the local configuration register blocks of the other modules
2. Clock and reset control registers for ISP Controller core

The Control Unit has one 32 bit PVCI input interface and multiple 32 bit PVCI output interfaces. All transfers from the PVCI input interface are 32 bit wide.

Each block inside the ISP Controller IP core uses a dedicated clock signal that can be controlled by a programming register inside the Control Unit.

Existing software resets in the ISP Controller blocks can also be controlled by a programming register inside the Control Unit. An asynchronous reset for the processing clock domain has to be generated from the system reset. A soft reset for all registers in the IP core is provided. It works like an asynchronous reset.

All sub module processing clocks can be switched on and off. All sub module configuration clocks are enabled only when the dedicated address is active.

6.4 Register Description

The ISP uses a distributed configuration register scheme. So there is no central unit containing all programming registers, but all sub-modules contain their own programming registers. An address space is reserved for each sub-module inside the total ISP Controller

6.4.1 Registers Summary

Table 6-1 ISP module base address

Module	Description	Base Name	Offset Address
main_control	ISP Main Control Registers	ISP_BASE	0x0000
image_effects	Image Effects	ISP_IMGEFF_BASE	0x0200
superimpose	Superimpose	ISP_SI_BASE	0x0300
misp	ISP main registers	ISP_MISP_BASE	0x0400
isp_flash	FLASH_LIGHT registers	ISP_FLASH_BASE	0x0660
isp_shutter	SHUTTER registers	ISP_SHUT_BASE	0x0680
cproc	COLOR PROCESSING registers	ISP_CPROC_BASE	0x0800
dual_crop	Dual Cropping registers	ISP_DUAL_CROP_BASE	0x0880
main_resize	MAIN RESIZE registers	ISP_MRSZ_BASE	0x0C00
self_resize	SELF RESIZE registers	ISP_SRSZ_BASE	0x1000
mi	MEMORY Interface registers	ISP_MI_BASE	0x1400
mipi	MIPI Interface Registers	ISP_MIPI_BASE	0x1C00
isp_afm	ISP Auto Focus Measurement	ISP_AFM_BASE	0x2000
isp_bp	ISP Bad Pixel	ISP_BP_BASE	0x2100
isp_lsc	ISP Lens Shade Correction	ISP_LSC_BASE	0x2200
isp_is	ISP Image Stabilization	ISP_IS_BASE	0x2300
isp_hist	ISP Histogram	ISP_HIST_BASE	0x2400
isp_filter	ISP Filter	ISP_FILT_BASE	0x2500
isp_cac	ISP Chromatic Aberration Correction	ISP_CAC_BASE	0x2580
isp_exposure	ISP Auto Exposure Measurement	ISP_AE_BASE	0x2600
isp_bls	ISP Black Level Subtraction	ISP_BLS_BASE	0x2700
isp_dpf	ISP De-noising Pre-filter	ISP_DPF_BASE	0x2800
isp_dpcc	ISP Defect Pixel Cluster Correction	ISP_DPCC_BASE	0x2900
isp_wdr	ISP Wide Dynamic Range	ISP_WDR_BASE	0x2A00
vsm	video stabilization measurement	ISP_VSM_BASE	0x2F00

Table 6-2 Summary of available registers

Name	Address	Mode	Description
VI_CCL	ISP_BASE + 0000H	rw	Clock control register
VI_ID	ISP_BASE + 0008H	r	Revision identification register
VI_ICCL	ISP_BASE + 0010H	rw	Internal clock control register
VI_IRCL	ISP_BASE + 0014H	rw	Internal reset control register
VI_DPCL	ISP_BASE + 0018H	rw	Data path control register

Name	Address	Mode	Description
IMG_EFF_CTRL	ISP_IMGEFF_BASE + 0000H	rw	Global control register
IMG_EFF_COLOR_SEL	ISP_IMGEFF_BASE + 0004H	rw	Color selection register (for color selection effect)
IMG_EFF_MAT_1	ISP_IMGEFF_BASE + 0008H	rw	3x3 matrix coefficients for emboss effect (1)
IMG_EFF_MAT_2	ISP_IMGEFF_BASE + 000CH	rw	3x3 matrix coefficients for emboss effect (2)
IMG_EFF_MAT_3	ISP_IMGEFF_BASE + 0010H	rw	3x3 matrix coefficients for emboss(3) effect / sketch/sharpen(1) effect
IMG_EFF_MAT_4	ISP_IMGEFF_BASE + 0014H	rw	3x3 matrix coefficients for sketch/sharpen effect (2)
IMG_EFF_MAT_5	ISP_IMGEFF_BASE + 0018H	rw	3x3 matrix coefficients for sketch/sharpen effect (3)
IMG_EFF_TINT	ISP_IMGEFF_BASE + 001CH	rw	Chrominance increment values of a tint (used for sepia effect)
IMG_EFF_CTRL_SHD	ISP_IMGEFF_BASE + 0020H	r	Shadow register for control register
IMG_EFF_SHARPEN	ISP_IMGEFF_BASE + 0024H	rw	Factor and threshold for sharpen effect

Name	Address	Mode	Description
SUPER_IMP_CTRL	ISP_SI_BASE + 0000H	rw	Global control register
SUPER_IMP_OFFSET_X	ISP_SI_BASE + 0004H	rw	Offset x register
SUPER_IMP_OFFSET_Y	ISP_SI_BASE + 0008H	rw	Offset y register
SUPER_IMP_COLOR_Y	ISP_SI_BASE + 000CH	rw	Y component of transparent key color
SUPER_IMP_COLOR_CB	ISP_SI_BASE + 0010H	rw	Cb component of transparent key color
SUPER_IMP_COLOR_CR	ISP_SI_BASE + 0014H	rw	Cr component of transparent key color

Name	Address	M	Description
ISP_CTRL	ISP_MISP_BASE +	rw	global control register
ISP_ACQ_PROP	ISP_MISP_BASE +	rw	ISP acquisition properties
ISP_ACQ_H_OFFS	ISP_MISP_BASE +	rw	horizontal input offset
ISP_ACQ_V_OFFS	ISP_MISP_BASE +	rw	vertical input offset
ISP_ACQ_H_SIZE	ISP_MISP_BASE +	rw	horizontal input size
ISP_ACQ_V_SIZE	ISP_MISP_BASE +	rw	vertical input size
ISP_ACQ_NR_FRAMES	ISP_MISP_BASE +	rw	Number of frames to be
ISP_GAMMA_DX_LO	ISP_MISP_BASE + 001CH	rw	De-Gamma Curve definition lower x increments
ISP_GAMMA_DX_HI	ISP_MISP_BASE + 0020H	rw	De-Gamma Curve definition higher x increments (sampling
BLOCK ISP_GAMMA_R_Y	ISP_MISP_B ASE + 4n, 0x00 24+	rw	De-Gamma Curve definition y red
BLOCK ISP_GAMMA_G_Y	ISP_MISP_B ASE + 4n, 0x00 68+	rw	De-Gamma Curve definition y green
BLOCK ISP_GAMMA_B_Y	ISP_MISP_B ASE + 4n, 0x00 AC+	rw	De-Gamma Curve definition y blue

Name	Address	M	Description
ISP_AWB_PROP	ISP_MISP_BASE +	rw	Auto white balance
ISP_AWB_H_OFFS	ISP_MISP_BASE + 0114H	rw	Auto white balance horizontal offset of
ISP_AWB_V_OFFS	ISP_MISP_BASE + 0118H	rw	Auto white balance vertical offset of measure
ISP_AWB_H_SIZE	ISP_MISP_BASE + 011CH	rw	Auto white balance horizontal window size
ISP_AWB_V_SIZE	ISP_MISP_BASE + 0120H	rw	Auto white balance vertical window size
ISP_AWB_FRAMES	ISP_MISP_BASE + 0124H	rw	Auto white balance mean value over multiple
ISP_AWB_REF	ISP_MISP_BASE + 0128H	rw	Auto white balance reference Cb/Cr values
ISP_AWB_THRESH	ISP_MISP_BASE + 012CH	rw	Auto white balance threshold values
ISP_AWB_GAIN_G	ISP_MISP_BASE +	rw	Auto white balance gain
ISP_AWB_GAIN_RB	ISP_MISP_BASE + 013CH	rw	Auto white balance gain red and blue
ISP_AWB_WHITE_CNT	ISP_MISP_BASE + 0140H	r	Auto white balance white pixel count
ISP_AWB_MEAN	ISP_MISP_BASE + 0144H	r	Auto white balance measured mean value
ISP_CC_COEFF_0	ISP_MISP_BASE +	rw	Color conversion coefficient
ISP_CC_COEFF_1	ISP_MISP_BASE +	rw	Color conversion coefficient

Name	Address	M	Description
ISP_CC_COEFF_2	ISP_MISP_BASE +	rw	Color conversion coefficient
ISP_CC_COEFF_3	ISP_MISP_BASE +	rw	Color conversion coefficient
ISP_CC_COEFF_4	ISP_MISP_BASE +	rw	Color conversion coefficient
ISP_CC_COEFF_5	ISP_MISP_BASE +	rw	Color conversion coefficient
ISP_CC_COEFF_6	ISP_MISP_BASE +	rw	Color conversion coefficient
ISP_CC_COEFF_7	ISP_MISP_BASE +	rw	Color conversion coefficient
ISP_CC_COEFF_8	ISP_MISP_BASE +	rw	Color conversion coefficient
ISP_OUT_H_OFFS	ISP_MISP_BASE +	rw	Horizontal offset of output
ISP_OUT_V_OFFS	ISP_MISP_BASE +	rw	Vertical offset of output
ISP_OUT_H_SIZE	ISP_MISP_BASE +	rw	Output horizontal picture

Name	Address	M	Description
ISP_OUT_V_SIZE	ISP_MISP_BASE +	rw	Output vertical picture size
ISP_DEMOSAIC	ISP_MISP_BASE +	rw	Demosaic parameters
ISP_FLAGS_SHD	ISP_MISP_BASE + 01A8H	r	Flags (current status) of certain signals and Shadow regs for enable signals
ISP_OUT_H_OFFS_SHD	ISP_MISP_BASE + 01ACH	r	current horizontal offset of output window (shadow register)
ISP_OUT_V_OFFS_SHD	ISP_MISP_BASE + 01B0H	r	current vertical offset of output window (shadow register)
ISP_OUT_H_SIZE_SHD	ISP_MISP_BASE + 01B4H	r	current output horizontal picture size (shadow register)
ISP_OUT_V_SIZE_SHD	ISP_MISP_BASE + 01B8H	r	current output vertical picture size (shadow register)
ISP_IMSC	ISP_MISP_BASE +	rw	Interrupt mask
ISP_RIS	ISP_MISP_BASE +	r	Raw interrupt status
ISP_MIS	ISP_MISP_BASE +	r	Masked interrupt status
ISP_ICR	ISP_MISP_BASE +	w	Interrupt clear register
ISP_ISR	ISP_MISP_BASE +	w	Interrupt set register
BLOCK ISP_CT_COEFF 0...8	ISP_MISP_BASE + 0x01D0+ 4n, n=0...8	rw	cross-talk configuration register (color correction matrix)
ISP_GAMMA_OUT_MODE	ISP_MISP_BASE + 01F4H	rw	gamma segmentation mode
BLOCK ISP_GAMMA_OUT_Y	ISP_MISP_BASE + 0x01F8+ 4n, n=0...16	rw	Gamma Out Curve definition y_
ISP_ERR	ISP_MISP_BASE +	r	ISP error register
ISP_ERR_CLR	ISP_MISP_BASE +	w	ISP error clear register
ISP_FRAME_COUNT	ISP_MISP_BASE +	r	Frame counter
ISP_CT_OFFSET_R	ISP_MISP_BASE +	rw	cross-talk offset red

Name	Address	M	Description
ISP_CT_OFFSET_G	ISP_MISP_BASE +	rw	cross-talk offset green
ISP_CT_OFFSET_B	ISP_MISP_BASE +	rw	cross-talk offset blue

Name	Address	M	Description
ISP_FLASH_CM	ISP_FLASH_BASE +	w	Flash command
ISP_FLASH_CO	ISP_FLASH_BASE +	rw	Flash config
ISP_FLASH_PRE	ISP_FLASH_BASE +	rw	Flash Counter Pre-Divider
ISP_FLASH_DEL	ISP_FLASH_BASE +	rw	Flash Delay
ISP_FLASH_TIM	ISP_FLASH_BASE +	rw	Flash time
ISP_FLASH_MAX	ISP_FLASH_BASE +	rw	Maximum value for flash or

Name	Address	M	Description
ISP_SH_CTR	ISP_SHUT_BASE +	rw	mechanical shutter control
ISP_SH_PRE	ISP_SHUT_BASE +	rw	Mech. Shutter Counter Pre-Divider
ISP_SH_DEL	ISP_SHUT_BASE +	rw	Delay register
ISP_SH_TIM	ISP_SHUT_BASE +	rw	Time register

Name	Address	M	Description
CPROC_CTRL	ISP_CPROC_BASE +	rw	Global control register
CPROC_CONTRAS	ISP_CPROC_BASE +	rw	Color Processing contrast
CPROC_BRIGHTN	ISP_CPROC_BASE +	rw	Color Processing brightness
CPROC_SATURATI	ISP_CPROC_BASE +	rw	Color Processing saturation
CPROC_HUE	ISP_CPROC_BASE +	rw	Color Processing hue register

Name	Address	M	Description
MRSZ_CTRL	ISP_MRSZ_BASE +	rw	global control register
MRSZ_SCALE_HY	ISP_MRSZ_BASE + 0004H	rw	horizontal luminance scale factor register
MRSZ_SCALE_HCB	ISP_MRSZ_BASE +	rw	horizontal Cb scale factor register
MRSZ_SCALE_HCR	ISP_MRSZ_BASE +	rw	horizontal Cr scale factor register
MRSZ_SCALE_VY	ISP_MRSZ_BASE + 0010H	rw	vertical luminance scale factor register
MRSZ_SCALE_VC	ISP_MRSZ_BASE + 0014H	rw	vertical chrominance scale factor register
MRSZ_PHASE_HY	ISP_MRSZ_BASE + 0018H	rw	horizontal luminance phase register
MRSZ_PHASE_HC	ISP_MRSZ_BASE + 001CH	rw	horizontal chrominance phase register
MRSZ_PHASE_VY	ISP_MRSZ_BASE +	rw	vertical luminance phase register
MRSZ_PHASE_VC	ISP_MRSZ_BASE + 0024H	rw	vertical chrominance phase register

Name	Address	M	Description
MRSZ_SCALE_LUT_ADDR	ISP_MRSZ_BASE + 0028H	rw	Address pointer of up-scaling look up table
MRSZ_SCALE_LUT	ISP_MRSZ_BASE +	rw	Entry of up-scaling look up table
MRSZ_CTRL_SHD	ISP_MRSZ_BASE +	r	global control shadow register
MRSZ_SCALE_HY_SHD	ISP_MRSZ_BASE + 0034H	r	horizontal luminance scale factor shadow register
MRSZ_SCALE_HCB_SHD	ISP_MRSZ_BASE + 0038H	r	horizontal Cb scale factor shadow register
MRSZ_SCALE_HCR_SHD	ISP_MRSZ_BASE + 003CH	r	horizontal Cr scale factor shadow register
MRSZ_SCALE_VY_SHD	ISP_MRSZ_BASE + 0040H	r	vertical luminance scale factor shadow register
MRSZ_SCALE_VC_SHD	ISP_MRSZ_BASE + 0044H	r	vertical chrominance scale factor shadow register
MRSZ_PHASE_HY_SHD	ISP_MRSZ_BASE + 0048H	r	horizontal luminance phase shadow register
MRSZ_PHASE_HC_SHD	ISP_MRSZ_BASE + 004CH	r	horizontal chrominance phase shadow register
MRSZ_PHASE_VY_SHD	ISP_MRSZ_BASE + 0050H	r	vertical luminance phase shadow register
MRSZ_PHASE_VC_SHD	ISP_MRSZ_BASE + 0054H	r	vertical chrominance phase shadow register

Name	Address	M	Description
SRSZ_CTRL	ISP_SRSZ_BASE +	rw	global control register
SRSZ_SCALE_HY	ISP_SRSZ_BASE + 0004H	rw	horizontal luminance scale factor register
SRSZ_SCALE_HCB	ISP_SRSZ_BASE + 0008H	rw	horizontal chrominance scale factor register
SRSZ_SCALE_HCR	ISP_SRSZ_BASE + 000CH	rw	horizontal chrominance scale factor register
SRSZ_SCALE_VY	ISP_SRSZ_BASE + 0010H	rw	vertical luminance scale factor register
SRSZ_SCALE_VC	ISP_SRSZ_BASE + 0014H	rw	vertical chrominance scale factor register
SRSZ_PHASE_HY	ISP_SRSZ_BASE +	rw	horizontal luminance phase register
SRSZ_PHASE_HC	ISP_SRSZ_BASE + 001CH	rw	horizontal chrominance phase register
SRSZ_PHASE_VY	ISP_SRSZ_BASE +	rw	vertical luminance phase register
SRSZ_PHASE_VC	ISP_SRSZ_BASE +	rw	vertical chrominance phase register
SRSZ_SCALE_LUT_ADDR	ISP_SRSZ_BASE + 0028H	rw	Address pointer of up-scaling look up table
SRSZ_SCALE_LUT	ISP_SRSZ_BASE +	rw	Entry of up-scaling look up table
SRSZ_CTRL_SHD	ISP_SRSZ_BASE +	r	global control shadow register
SRSZ_SCALE_HY_SHD	ISP_SRSZ_BASE + 0034H	r	horizontal luminance scale factor shadow register
SRSZ_SCALE_HCB_SHD	ISP_SRSZ_BASE + 0038H	r	horizontal Cb scale factor shadow register
SRSZ_SCALE_HCR_SHD	ISP_SRSZ_BASE + 003CH	r	horizontal Cr scale factor shadow register
SRSZ_SCALE_VY_SHD	ISP_SRSZ_BASE + 0040H	r	vertical luminance scale factor shadow register
SRSZ_SCALE_VC_SHD	ISP_SRSZ_BASE + 0044H	r	vertical chrominance scale factor shadow register
SRSZ_PHASE_HY_SHD	ISP_SRSZ_BASE + 0048H	r	horizontal luminance phase shadow register
SRSZ_PHASE_HC_SHD	ISP_SRSZ_BASE + 004CH	r	horizontal chrominance phase shadow register
SRSZ_PHASE_VY_SHD	ISP_SRSZ_BASE + 0050H	r	vertical luminance phase shadow register
SRSZ_PHASE_VC_SHD	ISP_SRSZ_BASE + 0054H	r	vertical chrominance phase shadow register

Name	Address	M	Description
MI_CTRL	ISP_MI_BASE + 0000H	rw	Global control register
MI_INIT	ISP_MI_BASE + 0004H	w	Control register for address init and skip function
MI_MP_Y_BASE_AD_INIT	ISP_MI_BASE + 0008H	rw	Base address for main picture Y component, JPEG or raw data
MI_MP_Y_SIZE_INIT	ISP_MI_BASE + 000CH	rw	Size of main picture Y component, JPEG or raw data
MI_MP_Y_OFFS_CNT_INIT	ISP_MI_BASE + 0010H	rw	Offset counter init value for main picture Y, JPEG or raw data
MI_MP_Y_OFFS_CNT_START	ISP_MI_BASE + 0014H	r	Offset counter start value for main picture Y, JPEG or raw data
MI_MP_Y_IRQ_OFFS_INIT	ISP_MI_BASE + 0018H	rw	Fill level interrupt offset value for main picture Y, JPEG or raw data
MI_MP_CB_BASE_AD_INIT	ISP_MI_BASE + 001CH	rw	Base address for main picture Cb component ring buffer
MI_MP_CB_SIZE_INIT	ISP_MI_BASE + 0020H	rw	Size of main picture Cb component ring buffer
MI_MP_CB_OFFS_CNT_INIT	ISP_MI_BASE + 0024H	rw	Offset counter init value for main picture Cb component ring buffer
MI_MP_CB_OFFS_CNT_START	ISP_MI_BASE + 0028H	r	Offset counter start value for main picture Cb component ring buffer
MI_MP_CR_BASE_AD_INIT	ISP_MI_BASE + 002CH	rw	Base address for main picture Cr component ring buffer
MI_MP_CR_SIZE_INIT	ISP_MI_BASE + 0030H	rw	Size of main picture Cr component ring buffer
MI_MP_CR_OFFS_CNT_INIT	ISP_MI_BASE + 0034H	rw	Offset counter init value for main picture Cr component ring buffer
MI_MP_CR_OFFS_CNT_START	ISP_MI_BASE + 0038H	r	Offset counter start value for main picture Cr component ring buffer
MI_SP_Y_BASE_AD_INIT	ISP_MI_BASE + 003CH	rw	Base address for self picture Y component ring buffer
MI_SP_Y_SIZE_INIT	ISP_MI_BASE + 0040H	rw	Size of self picture Y component ring buffer
MI_SP_Y_OFFS_CNT_INIT	ISP_MI_BASE + 0044H	rw	Offset counter init value for self picture Y component ring buffer
MI_SP_Y_OFFS_CNT_START	ISP_MI_BASE + 0048H	r	Offset counter start value for self picture Y component ring buffer

Name	Address	M	Description
MI_SP_Y_LLENGTH	ISP_MI_BASE + 004CH	rw	Line length of self picture Y component
MI_SP_CB_BASE_AD_INIT	ISP_MI_BASE + 0050H	rw	Base address for self picture Cb component ring
MI_SP_CB_SIZE_INIT	ISP_MI_BASE + 0054H	rw	Size of self picture Cb component ring buffer
MI_SP_CB_OFFS_CNT_INIT	ISP_MI_BASE + 0058H	rw	Offset counter init value for self picture Cb component

Name	Address	M	Description
MI_SP_CB_OFFS_CNT_START	ISP_MI_BASE + 005CH	r	Offset counter start value for self picture Cb component
MI_SP_CR_BASE_AD_INIT	ISP_MI_BASE + 0060H	rw	Base address for self picture Cr component ring
MI_SP_CR_SIZE_INIT	ISP_MI_BASE + 0064H	rw	Size of self picture Cr component ring buffer
MI_SP_CR_OFFS_CNT_INIT	ISP_MI_BASE + 0068H	rw	Offset counter init value for self picture Cr component
MI_SP_CR_OFFS_CNT_START	ISP_MI_BASE + 006CH	r	Offset counter start value for self picture Cr component
MI_BYTE_CNT	ISP_MI_BASE + 0070H	r	Counter value of JPEG or RAW data bytes
MI_CTRL_SHD	ISP_MI_BASE + 0074H	r	global control internal shadow register
MI_MP_Y_BASE_AD_SHD	ISP_MI_BASE + 0078H	r	Base address shadow register for main picture Y component, JPEG or raw data
MI_MP_Y_SIZE_SHD	ISP_MI_BASE + 007CH	r	Size shadow register of main picture Y component, JPEG or raw data
MI_MP_Y_OFFS_CNT_SHD	ISP_MI_BASE + 0080H	r	Current offset counter of main picture Y component, JPEG or raw
MI_MP_Y_IRQ_OFFS_SHD	ISP_MI_BASE + 0084H	r	Shadow register of fill level interrupt offset value for main picture Y
MI_MP_CB_BASE_AD_SHD	ISP_MI_BASE + 0088H	r	Base address shadow register for main picture Cb component ring buffer

Name	Address	M	Description
MI_MP_CB_SIZE_SHD	ISP_MI_BASE + 008CH	r	Size shadow register of main picture Cb component ring buffer
MI_MP_CB_OFFS_CNT_SHD	ISP_MI_BASE + 0090H	r	Current offset counter of main picture Cb component ring buffer
MI_MP_CR_BASE_AD_SHD	ISP_MI_BASE + 0094H	r	Base address shadow register for main picture Cr component ring buffer
MI_MP_CR_SIZE_SHD	ISP_MI_BASE + 0098H	r	Size shadow register of main picture Cr component ring buffer
MI_MP_CR_OFFS_CNT_SHD	ISP_MI_BASE + 009CH	r	Current offset counter of main picture Cr component ring buffer
MI_SP_Y_BASE_AD_SHD	ISP_MI_BASE + 00A0H	r	Base address shadow register for self picture Y component ring buffer
MI_SP_Y_SIZE_SHD	ISP_MI_BASE + 00A4H	r	Size shadow register of self picture Y component ring buffer

Name	Address	M	Description
MI_SP_Y_OFFS_CNT_SHD	ISP_MI_BASE + 00A8H	r	Current offset counter of self picture Y component ring buffer
MI_SP_CB_BASE_AD_SHD	ISP_MI_BASE + 00B0H	r	Base address shadow register for self picture Cb component ring buffer
MI_SP_CB_SIZE_SHD	ISP_MI_BASE + 00B4H	r	Size shadow register of self picture Cb component ring buffer
MI_SP_CB_OFFS_CNT_SHD	ISP_MI_BASE + 00B8H	r	Current offset counter of self picture Cb component ring buffer
MI_SP_CR_BASE_AD_SHD	ISP_MI_BASE + 00BCH	r	Base address shadow register for self picture Cr component ring buffer
MI_SP_CR_SIZE_SHD	ISP_MI_BASE + 00C0H	r	Size shadow register of self picture Cr component ring buffer
MI_SP_CR_OFFS_CNT_SHD	ISP_MI_BASE + 00C4H	r	Current offset counter of self picture Cr component ring buffer
MI_DMA_Y_PIC_START	ISP_MI_BASE	r	Y component image start address
MI_DMA_Y_PIC_WIDTH	ISP_MI_BASE	r	Y component image width
MI_DMA_Y_LLENGTH	ISP_MI_BASE	r	Y component original line length
MI_DMA_Y_PIC_SIZE	ISP_MI_BASE	r	Y component image size

Name	Address	M	Description
MI_DMA_CB_PIC_START_AD	ISP_MI_BASE + 00D8H	rw	Cb component image start address
MI_DMA_CR_PIC_START_	ISP_MI_BASE +	rw	Cr component image start
MI_IMSC	ISP_MI_BASE + 00F8H	rw	Interrupt Mask („1“: interrupt active, „0“:
MI_RIS	ISP_MI_BASE +	r	Raw Interrupt Status
MI_MIS	ISP_MI_BASE +	r	Masked Interrupt Status
MI_ICR	ISP_MI_BASE +	w	Interrupt Clear Register
MI_ISR	ISP_MI_BASE +	w	Interrupt Set Register
MI_STATUS	ISP_MI_BASE +	r	MI Status Register
MI_STATUS_CLR	ISP_MI_BASE +	w	MI Status Clear Register
MI_SP_Y_PIC_WIDTH	ISP_MI_BASE +	rw	Y component image width
MI_SP_Y_PIC_HEIGHT	ISP_MI_BASE +	rw	Y component image height
MI_SP_Y_PIC_SIZE	ISP_MI_BASE +	rw	Y component image size
MI_DMA_CTRL	ISP_MI_BASE +	rw	DMA control register
MI_DMA_START	ISP_MI_BASE + 0124H	w	DMA start register
MI_DMA_STATUS	ISP_MI_BASE + 0128H	r	DMA status register
MI_PIXEL_CNT	ISP_MI_BASE + 012CH	r	Counter value for defect pixel list
MI_MP_Y_BASE_AD_INIT2	ISP_MI_BASE + 0130H	rw	Base address 2 (ping pong) for main picture Y component, JPEG or raw data

Name	Address	M	Description
MI_MP_CB_BASE_AD_INIT2	ISP_MI_BASE + 0134H	rw	Base address 2 (pingpong) for main picture Cb component
MI_MP_CR_BASE_AD_INIT2	ISP_MI_BASE + 0138H	rw	Base address 2 (pingpong) for main picture Cr component ring buffer
MI_SP_Y_BASE_AD_INIT2	ISP_MI_BASE + 013CH	rw	Base address 2 (ping pong) for self picture Y component
MI_SP_CB_BASE_AD_INIT2	ISP_MI_BASE + 0140H	rw	Base address 2 (pingpong) for self picture Cb component
MI_SP_CR_BASE_AD_INIT2	ISP_MI_BASE + 0144H	rw	Base address 2 (pingpong) for self picture Cr component ring buffer
MI_XTD_FORMAT_CTRL	ISP_MI_BASE + 0148H	rw	Extended Storage Format Control for main, self and dma read path

Name	Address	M	Description
MIPI_CTRL	ISP_MIPI_BASE +	rw	global control register
MIPI_STATUS	ISP_MIPI_BASE +	r	global status register
MIPI_IMSC	ISP_MIPI_BASE +	rw	Interrupt mask
MIPI_RIS	ISP_MIPI_BASE +	r	Raw interrupt status
MIPI_MIS	ISP_MIPI_BASE +	r	Masked interrupt status
MIPI_ICR	ISP_MIPI_BASE +	w	Interrupt clear register
MIPI_ISR	ISP_MIPI_BASE +	w	Interrupt set register
MIPI_CUR_DATA_ID	ISP_MIPI_BASE +	r	Current Data Identifier
MIPI_IMG_DATA_SEL	ISP_MIPI_BASE +	rw	Image Data Selector
MIPI_ADD_DATA_SEL_1	ISP_MIPI_BASE +	rw	Additional Data Selector 1
MIPI_ADD_DATA_SEL_2	ISP_MIPI_BASE +	rw	Additional Data Selector 2
MIPI_ADD_DATA_SEL_3	ISP_MIPI_BASE +	rw	Additional Data Selector 3
MIPI_ADD_DATA_SEL_4	ISP_MIPI_BASE +	rw	Additional Data Selector 4
MIPI_ADD_DATA_FIFO	ISP_MIPI_BASE +	r	Additional Data Fifo
MIPI_ADD_DATA_FILL_L	ISP_MIPI_BASE +	rw	Additional Data FIFO Fill Level
MIPI_COMPRESSED_MODE	ISP_MIPI_BASE + 003CH	rw	controls processing of compressed raw data types
MIPI_FRAME	ISP_MIPI_BASE + 0040H	r	frame number from frame start and frame end short packets
MIPI_GEN_SHORT_DT	ISP_MIPI_BASE + 0044H	r	data type flags for received generic short packets
MIPI_GEN_SHORT_8_9	ISP_MIPI_BASE + 0048H	r	data field for generic short packets of data type 0x8 and 0x9
MIPI_GEN_SHORT_A_B	ISP_MIPI_BASE + 004CH	r	data field for generic short packets of data type 0xA and 0xB
MIPI_GEN_SHORT_C_D	ISP_MIPI_BASE + 0050H	r	data field for generic short packets of data type 0xC and 0xD

MIPI_GEN_SHORT_E_F	ISP_MIPI_BASE + 0054H	r	data field for generic short packets of data type 0xE and 0xF

Name	Address	Mode	Description
ISP_AFM_CTRL	ISP_AFM_BASE + 0000H	rw	This is the control register for AF measurement unit
ISP_AFM_LT_A	ISP_AFM_BASE + 0004H	rw	Top Left corner of measure window A
ISP_AFM_RB_A	ISP_AFM_BASE + 0008H	rw	Bottom right corner of measure window A
ISP_AFM_LT_B	ISP_AFM_BASE + 000CH	rw	Top left corner of measure window B
ISP_AFM_RB_B	ISP_AFM_BASE + 0010H	rw	Bottom right corner of measure window B
ISP_AFM_LT_C	ISP_AFM_BASE + 0014H	rw	Top left corner of measure window C
ISP_AFM_RB_C	ISP_AFM_BASE + 0018H	rw	Bottom right corner of measure window C
ISP_AFM_THRES	ISP_AFM_BASE + 001CH	rw	Threshold register
ISP_AFM_VAR_SHIFT	ISP_AFM_BASE + 0020H	rw	Variable shift register
ISP_AFM_SUM_A	ISP_AFM_BASE + 0024H	r	Sharpness Value Status Register of Window A
ISP_AFM_SUM_B	ISP_AFM_BASE + 0028H	r	Sharpness Value Status Register of Window B
ISP_AFM_SUM_C	ISP_AFM_BASE + 002CH	r	Sharpness Value Status Register of Window C
ISP_AFM_LUM_A	ISP_AFM_BASE + 0030H	r	Luminance Value Status Register of Window A
ISP_AFM_LUM_B	ISP_AFM_BASE + 0034H	r	Luminance Value Status Register of Window B
ISP_AFM_LUM_C	ISP_AFM_BASE + 0038H	r	Luminance Value Status Register of Window C

Name	Address	Mode	Description
ISP_LSC_CTRL	ISP_LSC_BASE + 0000H	rw	Lens shade control
ISP_LSC_R_TABLE_ADDR	ISP_LSC_BASE + 0004H	rwh	Table RAM Address for red component
ISP_LSC_GR_TABLE_ADDR	ISP_LSC_BASE + 0008H	rwh	Table RAM Address for green (red) component
ISP_LSC_B_TABLE_ADDR	ISP_LSC_BASE + 000CH	rwh	Table RAM Address for blue component
ISP_LSC_GB_TABLE_ADDR	ISP_LSC_BASE + 0010H	rwh	Table RAM Address for green (blue) component
ISP_LSC_R_TABLE_DATA	ISP_LSC_BASE + 0014H	rw	Sample table red
ISP_LSC_GR_TABLE_DATA	ISP_LSC_BASE + 0018H	rw	Sample table green (red)
ISP_LSC_B_TABLE_DATA	ISP_LSC_BASE + 001CH	rw	Sample table blue
ISP_LSC_GB_TABLE_DATA	ISP_LSC_BASE + 0020H	rw	Sample table green (blue)
ISP_LSC_XGRAD_01	ISP_LSC_BASE + 0024H	rw	Gradient table x

Name	Address	Mode	Description
ISP_LSC_XGRAD_23	ISP_LSC_BASE + 0028H	rw	Gradient table x
ISP_LSC_XGRAD_45	ISP_LSC_BASE + 002CH	rw	Gradient table x
ISP_LSC_XGRAD_67	ISP_LSC_BASE + 0030H	rw	Gradient table x
ISP_LSC_YGRAD_01	ISP_LSC_BASE + 0034H	rw	Gradient table y
ISP_LSC_YGRAD_23	ISP_LSC_BASE + 0038H	rw	Gradient table y
ISP_LSC_YGRAD_45	ISP_LSC_BASE + 003CH	rw	Gradient table y
ISP_LSC_YGRAD_67	ISP_LSC_BASE + 0040H	rw	Gradient table y
ISP_LSC_XSIZE_01	ISP_LSC_BASE + 0044H	rw	Size table
ISP_LSC_XSIZE_23	ISP_LSC_BASE + 0048H	rw	Size table
ISP_LSC_XSIZE_45	ISP_LSC_BASE + 004CH	rw	Size table
ISP_LSC_XSIZE_67	ISP_LSC_BASE + 0050H	rw	Size table
ISP_LSC_YSIZE_01	ISP_LSC_BASE + 0054H	rw	Size table
ISP_LSC_YSIZE_23	ISP_LSC_BASE + 0058H	rw	Size table
ISP_LSC_YSIZE_45	ISP_LSC_BASE + 005CH	rw	Size table
ISP_LSC_YSIZE_67	ISP_LSC_BASE + 0060H	rw	Size table
ISP_LSC_TABLE_SEL	ISP_LSC_BASE + 0064H	rw	Lens shade table set selection
ISP_LSC_STATUS	ISP_LSC_BASE + 0068H	r	Lens shade status

Name	Address	Mode	Description
ISP_IS_CTRL	ISP_IS_BASE + 0000H	rw	Image Stabilization Control Register
ISP_IS_RECENTER	ISP_IS_BASE + 0004H	rw	Recenter register
ISP_IS_H_OFFS	ISP_IS_BASE + 0008H	rw	Horizontal offset of output window
ISP_IS_V_OFFS	ISP_IS_BASE + 000CH	rw	Vertical offset of output window
ISP_IS_H_SIZE	ISP_IS_BASE + 0010H	rw	Output horizontal picture size
ISP_IS_V_SIZE	ISP_IS_BASE + 0014H	rw	Output vertical picture size
ISP_IS_MAX_DX	ISP_IS_BASE + 0018H	rw	Maximum Horizontal Displacement
ISP_IS_MAX_DY	ISP_IS_BASE + 001CH	rw	Maximum Vertical Displacement
ISP_IS_DISPLACE	ISP_IS_BASE + 0020H	rw	Camera displacement
ISP_IS_H_OFFS_SHD	ISP_IS_BASE + 0024H	r	current horizontal offset of output window (shadow register)
ISP_IS_V_OFFS_SHD	ISP_IS_BASE + 0028H	r	current vertical offset of output window (shadow register)
ISP_IS_H_SIZE_SHD	ISP_IS_BASE + 002CH	r	current output horizontal picture size (shadow register)
ISP_IS_V_SIZE_SHD	ISP_IS_BASE + 0030H	r	current output vertical picture size (shadow register)

Name	Address	Mode	Description
ISP_HIST_PROP	ISP_HIST_BASE + 0000H	rw	Histogram properties
ISP_HIST_H_OFFS	ISP_HIST_BASE + 0004H	rw	Histogram window horizontal offset for first window of 25 sub-windows
ISP_HIST_V_OFFS	ISP_HIST_BASE + 0008H	rw	Histogram window vertical offset for first window of 25 sub-windows
ISP_HIST_H_SIZE	ISP_HIST_BASE + 000CH	rw	Horizontal (sub-)window size
ISP_HIST_V_SIZE	ISP_HIST_BASE + 0010H	rw	Vertical (sub-)window size
BLOCK ISP_HIST_BIN 0...15	ISP_HIST_BASE + 0x014+ 4n, n=0...15	r	histogram measurement result bin

Name	Address	Mode	Description
ISP_HIST_WEIGHT_00TO20	ISP_HIST_BASE + 0054H	rw	Weighting factor for sub-windows
ISP_HIST_WEIGHT_40TO21	ISP_HIST_BASE + 0058H	rw	Weighting factor for sub-windows
ISP_HIST_WEIGHT_31TO12	ISP_HIST_BASE + 005CH	rw	Weighting factor for sub-windows
ISP_HIST_WEIGHT_22TO03	ISP_HIST_BASE + 0060H	rw	Weighting factor for sub-windows
ISP_HIST_WEIGHT_13TO43	ISP_HIST_BASE + 0064H	rw	Weighting factor for sub-windows
ISP_HIST_WEIGHT_04TO24	ISP_HIST_BASE + 0068H	rw	Weighting factor for sub-windows
ISP_HIST_WEIGHT_44	ISP_HIST_BASE + 006CH	rw	Weighting factor for sub-windows

Name	Address	Mode	Description
ISP_FILT_MODE	ISP_FILT_BASE + 0000H	rw	mode control register for the filter block
ISP_FILT_THRESH_BL0	ISP_FILT_BASE + 0028H	rw	Blurring threshold 0
ISP_FILT_THRESH_BL1	ISP_FILT_BASE + 002CH	rw	Blurring threshold 1
ISP_FILT_THRESH_SH0	ISP_FILT_BASE + 0030H	rw	Sharpening threshold 0
ISP_FILT_THRESH_SH1	ISP_FILT_BASE + 0034H	rw	Sharpening threshold 1
ISP_FILT_LUM_WEIGHT	ISP_FILT_BASE + 0038H	rw	Parameters for luminance weight function
ISP_FILT_FAC_SH1	ISP_FILT_BASE + 003CH	rw	filter factor sharp1
ISP_FILT_FAC_SH0	ISP_FILT_BASE + 0040H	rw	filter factor sharp0
ISP_FILT_FAC_MID	ISP_FILT_BASE + 0044H	rw	filter factor middle
ISP_FILT_FAC_BL0	ISP_FILT_BASE + 0048H	rw	Parameter for blur 0 filter
ISP_FILT_FAC_BL1	ISP_FILT_BASE + 004CH	rw	Parameter for blur 1 filter

Name	Address	Mode	Description
ISP_CAC_CTRL	ISP_CAC_BASE + 0000H	rw	Control register for chromatic aberration correction
ISP_CAC_COUNT_START	ISP_CAC_BASE + 0004H	rw	Preload values for CAC pixel and line counter
ISP_CAC_A	ISP_CAC_BASE + 0008H	rw	Linear Parameters for radial shift calculation
ISP_CAC_B	ISP_CAC_BASE + 000CH	rw	Square Parameters for radial shift calculation
ISP_CAC_C	ISP_CAC_BASE + 0010H	rw	Cubical Parameters for radial shift calculation
ISP_CAC_X_NORM	ISP_CAC_BASE + 0014H	rw	Normalization parameters for calculation of image coordinate x_d relative to optical center
ISP_CAC_Y_NORM	ISP_CAC_BASE + 0018H	rw	Normalization parameters for calculation of image coordinate y_d relative to optical center

Name	Address	Mode	Description
ISP_EXP_CTRL	ISP_AE_BASE + 0000H	rw	Exposure control
ISP_EXP_H_OFFSET	ISP_AE_BASE + 0004H	rw	Horizontal offset for first block
ISP_EXP_V_OFFSET	ISP_AE_BASE + 0008H	rw	Vertical offset for first block
ISP_EXP_H_SIZE	ISP_AE_BASE + 000CH	rw	Horizontal size of one block
ISP_EXP_V_SIZE	ISP_AE_BASE + 0010H	rw	Vertical size of one block
ISP_EXP_MEAN_00	ISP_AE_BASE + 0014H	r	Mean luminance value of block 00
ISP_EXP_MEAN_10	ISP_AE_BASE + 0018H	r	Mean luminance value of block 10
ISP_EXP_MEAN_20	ISP_AE_BASE + 001CH	r	Mean luminance value of block 20
ISP_EXP_MEAN_30	ISP_AE_BASE + 0020H	r	Mean luminance value of block 30
ISP_EXP_MEAN_40	ISP_AE_BASE + 0024H	r	Mean luminance value of block 40
ISP_EXP_MEAN_01	ISP_AE_BASE + 0028H	r	Mean luminance value of block 01
ISP_EXP_MEAN_11	ISP_AE_BASE + 002CH	r	Mean luminance value of block 11
ISP_EXP_MEAN_21	ISP_AE_BASE + 0030H	r	Mean luminance value of block 21
ISP_EXP_MEAN_31	ISP_AE_BASE + 0034H	r	Mean luminance value of block 31
ISP_EXP_MEAN_41	ISP_AE_BASE + 0038H	r	Mean luminance value of block 41
ISP_EXP_MEAN_02	ISP_AE_BASE + 003CH	r	Mean luminance value of block 02
ISP_EXP_MEAN_12	ISP_AE_BASE + 0040H	r	Mean luminance value of block 12
ISP_EXP_MEAN_22	ISP_AE_BASE + 0044H	r	Mean luminance value of block 22
ISP_EXP_MEAN_32	ISP_AE_BASE + 0048H	r	Mean luminance value of block 32

Name	Address	Mode	Description
ISP_EXP_MEAN_42	ISP_AE_BASE + 004CH	r	Mean luminance value of block 42
ISP_EXP_MEAN_03	ISP_AE_BASE + 0050H	r	Mean luminance value of block 03
ISP_EXP_MEAN_13	ISP_AE_BASE + 0054H	r	Mean luminance value of block 13
ISP_EXP_MEAN_23	ISP_AE_BASE + 0058H	r	Mean luminance value of block 23
ISP_EXP_MEAN_33	ISP_AE_BASE + 005CH	r	Mean luminance value of block 33
ISP_EXP_MEAN_43	ISP_AE_BASE + 0060H	r	Mean luminance value of block 43
ISP_EXP_MEAN_04	ISP_AE_BASE + 0064H	r	Mean luminance value of block 04
ISP_EXP_MEAN_14	ISP_AE_BASE + 0068H	r	Mean luminance value of block 14
ISP_EXP_MEAN_24	ISP_AE_BASE + 006CH	r	Mean luminance value of block 24
ISP_EXP_MEAN_34	ISP_AE_BASE + 0070H	r	Mean luminance value of block 34
ISP_EXP_MEAN_44	ISP_AE_BASE + 0074H	r	Mean luminance value of block 44

Name	Address	Mode	Description
ISP_BLS_CTRL	ISP_BLS_BASE + 0000H	rw	global control register
ISP_BLS_SAMPLES	ISP_BLS_BASE + 0004H	rw	samples register
ISP_BLS_H1_START	ISP_BLS_BASE + 0008H	rw	window 1 horizontal start
ISP_BLS_H1_STOP	ISP_BLS_BASE + 000CH	rw	window 1 horizontal stop
ISP_BLS_V1_START	ISP_BLS_BASE + 0010H	rw	window 1 vertical start
ISP_BLS_V1_STOP	ISP_BLS_BASE + 0014H	rw	window 1 vertical stop
ISP_BLS_H2_START	ISP_BLS_BASE + 0018H	rw	window 2 horizontal start
ISP_BLS_H2_STOP	ISP_BLS_BASE + 001CH	rw	window 2 horizontal stop
ISP_BLS_V2_START	ISP_BLS_BASE + 0020H	rw	window 2 vertical start
ISP_BLS_V2_STOP	ISP_BLS_BASE + 0024H	rw	window 2 vertical stop
ISP_BLS_A_FIXED	ISP_BLS_BASE + 0028H	rw	fixed black level A
ISP_BLS_B_FIXED	ISP_BLS_BASE + 002CH	rw	fixed black level B
ISP_BLS_C_FIXED	ISP_BLS_BASE + 0030H	rw	fixed black level C
ISP_BLS_D_FIXED	ISP_BLS_BASE + 0034H	rw	fixed black level D
ISP_BLS_A_MEASURED	ISP_BLS_BASE + 0038H	r	measured black level A
ISP_BLS_B_MEASURED	ISP_BLS_BASE + 003CH	r	measured black level B
ISP_BLS_C_MEASURED	ISP_BLS_BASE + 0040H	r	measured black level C
ISP_BLS_D_MEASURED	ISP_BLS_BASE + 0044H	r	measured black level D

Name	Address	Mode	Description
ISP_DPF_MODE	ISP_DPF_BASE + 0000H	rw	Mode control for Denoising Pre- Filter block
ISP_DPF_STRENGTH_R	ISP_DPF_BASE + 0004H	rw	filter strength of the RED filter
ISP_DPF_STRENGTH_G	ISP_DPF_BASE + 0008H	rw	filter strength of the GREEN filter
ISP_DPF_STRENGTH_B	ISP_DPF_BASE + 000CH	rw	filter strength of the BLUE filter
ISP_DPF_S_WEIGHT_G_1_4	ISP_DPF_BASE + 0010H	rw	Spatial Weights green channel 1 2 3 4
ISP_DPF_S_WEIGHT_G_5_6	ISP_DPF_BASE + 0014H	rw	Spatial Weights green channel 5 6
ISP_DPF_S_WEIGHT_RB_1_4	ISP_DPF_BASE + 0018H	rw	Spatial Weights red/blue channels 1 2 3 4
ISP_DPF_S_WEIGHT_RB_5_6	ISP_DPF_BASE + 001CH	rw	Spatial Weights red/blue channels 5 6
BLOCK ISP_DPF_NLL_COEFF 0...16	ISP_DPF_BASE + 0x0020+ 4n, n=0...16	rw	Noise Level Lookup Coefficient
ISP_DPF_NF_GAIN_R	ISP_DPF_BASE + 0064H	rw	noise function gain for red pixels
ISP_DPF_NF_GAIN_GR	ISP_DPF_BASE + 0068H	rw	noise function gain for green in red pixels
ISP_DPF_NF_GAIN_GB	ISP_DPF_BASE + 006CH	rw	noise function gain for green in blue pixels
ISP_DPF_NF_GAIN_B	ISP_DPF_BASE + 0070H	rw	noise function gain for blue pixels

Name	Address	Mode	Description
ISP_DPCC_MODE	ISP_DPCC_BASE + 0000H	rw	Mode control for DPCC detection unit
ISP_DPCC_OUTPUT_MODE	ISP_DPCC_BASE + 0004H	rw	Interpolation mode for correction unit
ISP_DPCC_SET_USE	ISP_DPCC_BASE + 0008H	rw	DPCC methods set usage for detection
ISP_DPCC_METHODS_SET_1	ISP_DPCC_BASE + 000CH	rw	Methods enable bits for SET_1
ISP_DPCC_METHODS_SET_2	ISP_DPCC_BASE + 0010H	rw	Methods enable bits for SET_2
ISP_DPCC_METHODS_SET_3	ISP_DPCC_BASE + 0014H	rw	Methods enable bits for SET_3
ISP_DPCC_LINE_THRESH_1	ISP_DPCC_BASE + 0018H	rw	Line threshold SET_1
ISP_DPCC_LINE_MAD_FAC_1	ISP_DPCC_BASE + 001CH	rw	Mean Absolute Difference (MAD) factor for Line check set 1
ISP_DPCC_PG_FAC_1	ISP_DPCC_BASE + 0020H	rw	Peak gradient factor for set 1

Name	Address	Mode	Description
ISP_DPCC_RND_THRESH_1	ISP_DPCC_BASE + 0024H	rw	Rank Neighbor Difference threshold for set 1
ISP_DPCC_RG_FAC_1	ISP_DPCC_BASE + 0028H	rw	Rank gradient factor for set 1
ISP_DPCC_LINE_THRESH_2	ISP_DPCC_BASE + 002CH	rw	Line threshold set 2
ISP_DPCC_LINE_MAD_FAC_2	ISP_DPCC_BASE + 0030H	rw	Mean Absolute Difference (MAD) factor for Line check set 2
ISP_DPCC_PG_FAC_2	ISP_DPCC_BASE + 0034H	rw	Peak gradient factor for set 2
ISP_DPCC_RND_THRESH_2	ISP_DPCC_BASE + 0038H	rw	Rank Neighbor Difference threshold for set 2
ISP_DPCC_RG_FAC_2	ISP_DPCC_BASE + 003CH	rw	Rank gradient factor for set 2
ISP_DPCC_LINE_THRESH_3	ISP_DPCC_BASE + 0040H	rw	Line threshold set 3
ISP_DPCC_LINE_MAD_FAC_3	ISP_DPCC_BASE + 0044H	rw	Mean Absolute Difference (MAD) factor for Line check set 3
ISP_DPCC_PG_FAC_3	ISP_DPCC_BASE + 0048H	rw	Peak gradient factor for set 3
ISP_DPCC_RND_THRESH_3	ISP_DPCC_BASE + 004CH	rw	Rank Neighbor Difference threshold for set 3
ISP_DPCC_RG_FAC_3	ISP_DPCC_BASE + 0050H	rw	Rank gradient factor for set 3
ISP_DPCC_RO_LIMITS	ISP_DPCC_BASE + 0054H	rw	Rank Order Limits

Name	Address	Mode	Description
ISP_DPCC_RND_OFFS	ISP_DPCC_BASE + 0058H	rw	Differential Rank Offsets for Rank Neighbor Difference
ISP_DPCC_BPT_CTRL	ISP_DPCC_BASE + 005CH	rw	bad pixel table settings
ISP_DPCC_BPT_NUMBER	ISP_DPCC_BASE + 0060H	rw	Number of entries for bad pixel table (table based correction)
ISP_DPCC_BPT_ADDR	ISP_DPCC_BASE + 0064H	rwh	TABLE Start Address for table- based correction algorithm
ISP_DPCC_BPT_DATA	ISP_DPCC_BASE + 0068H	rwh	TABLE DATA register for read and write access of table RAM

Name	Address	Mode	Description
ISP_WDR_CTRL	ISP_WDR_BASE + 0000H	rw	Control Bits for Wide Dynamic Range Unit
ISP_WDR_TONECURVE_1	ISP_WDR_BASE + 0004H	rw	Tone Curve sample points dYn definition (part 1)

Name	Address	Mode	Description
ISP_WDR_TONECURVE_2	ISP_WDR_BASE + 0008H	rw	Tone Curve sample points dYn definition (part 2)
ISP_WDR_TONECURVE_3	ISP_WDR_BASE + 000CH	rw	Tone Curve sample points dYn definition (part 3)
ISP_WDR_TONECURVE_4	ISP_WDR_BASE + 0010H	rw	Tone Curve sample points dYn definition (part 4)
BLOCK ISP_WDR_TONECURVE_YM 0...32	ISP_WDR_BASE + 0x0014+ 4n, n=0...32	rw	Tonemapping curve coefficient Ym_

Name	Address	Mode	Description
ISP_WDR_OFFSET	ISP_WDR_BASE + 0098H	rw	Offset values for RGB path
ISP_WDR_DELTAMIN	ISP_WDR_BASE + 009CH	rw	DeltaMin Threshold and Strength factor
ISP_WDR_TONECURVE_1_SHD	ISP_WDR_BASE + 00A0H	r	Tone Curve sample points dYn definition shadow register (part 1)
ISP_WDR_TONECURVE_2_SHD	ISP_WDR_BASE + 00A4H	r	Tone Curve sample points dYn definition shadow register (part 2)
ISP_WDR_TONECURVE_3_SHD	ISP_WDR_BASE + 00A8H	r	Tone Curve sample points dYn definition shadow register (part 3)
ISP_WDR_TONECURVE_4_SHD	ISP_WDR_BASE + 00ACH	r	Tone Curve sample points dYn definition shadow register(part 4)
BLOCK ISP_WDR_TONECURVE_YM_SHD 0...32	ISP_WDR_BASE + 0x00B0+ 4n, n=0...32	r	Tonemapping curve coefficient shadow register

Name	Address	Mode	Description
ISP_VSM_MODE	ISP_VSM_BASE + 0000H	rw	VS Measure Mode
ISP_VSM_H_OFFS	ISP_VSM_BASE + 0004H	rw	VSM window horizontal offset
ISP_VSM_V_OFFS	ISP_VSM_BASE + 0008H	rw	VSM window vertical offset

Name	Address	Mode	Description
ISP_VSM_H_SIZE	ISP_VSM_BASE + 000CH	rw	Horizontal measure window size
ISP_VSM_V_SIZE	ISP_VSM_BASE + 0010H	rw	Vertical measure window size
ISP_VSM_H_SEGMENTS	ISP_VSM_BASE + 0014H	rw	Iteration 1 horizontal segments
ISP_VSM_V_SEGMENTS	ISP_VSM_BASE + 0018H	rw	Iteration 1 vertical segments
ISP_VSM_DELTA_H	ISP_VSM_BASE + 001CH	r	estimated horizontal displacement
ISP_VSM_DELTA_V	ISP_VSM_BASE + 0020H	r	estimated vertical displacement

6.4.2 ISP Detailed Register Description

Register: VI_CCL

Clock control register Reset value: 0000'0000H

Address: ISP_BASE + 0000H		Mode : rw
Bits	**Name**	**Description**
31:3	---	unused
2	vi_ccl_dis	Clock Control Logic disable 0: processing/cfg-clocks for all ISP sub modules enabled 1: processing/cfg-clocks for all ISP sub modules disabled w/o access to ID and VI_CCL register
1	vi_ccl_dis_status	Status of vi_ccl[2] bit (copy of vi_ccl[2])
0	---	unused

Register: VI_ICCL

Internal clock control register Reset value: 0000'1F7BH

Address: ISP_BASE + 0010H		Mode : rw
Bits	**Name**	**Description**
31:13	---	unused
12	reserved	reserved

Internal clock control register Reset value: 0000'1F7BH

Address: ISP_BASE + 0010H		Mode : rw
Bits	**Name**	**Description**
11	vi_mipi_clk_enable	MIPI interface clock enable 1: processing mode 0: power safe

Address: ISP_BASE + 0010H		Mode : rw
Bits	**Name**	**Description**
10	vi_smia_clk_enable	SMIA interface clock enable 1: processing mode 0: power safe
9	vi_simp_clk_enable	Superimpose clock enable 1: processing mode 0: power safe
8	vi_ie_clk_enable	Image effect clock enable 1: processing mode 0: power safe
7	---	unused
6	vi_mi_clk_enable	memory interface clock enable 1: processing mode 0: power safe
5	vi_jpeg_clk_enable	JPEG encoder clock enable 1: processing mode 0: power safe
4	vi_srsz_clk_enable	self picture resize clock enable 1: processing mode 0: power safe
3	vi_mrsz_clk_enable	main picture resize clock enable 1: processing mode 0: power safe
2	---	unused
1	vi_cp_clk_enable	color processing clock enable 1: processing mode 0: power safe
0	vi_isp_clk_enable	isp processing clock enable 1: processing mode 0: power safe

Register: VI_IRCL

Internal reset control register Reset value: 0000'0000H

Address: ISP_BASE + 0014H		Mode : rw
Bits	**Name**	**Description**
31:12	---	unused
12	reserved	reserved
11	vi_mipi_soft_rst	MIPI Interface software reset 0: processing mode 1: reset state

Address: ISP_BASE + 0014H		Mode : rw
Bits	**Name**	**Description**
10	vi_smia_soft_rst	SMIA Interface software reset 0: processing mode 1: reset state
9	vi_simp_soft_rst	Superimpose software reset 0: processing mode 1: reset state
8	vi_ie_soft_rst	Image effect software reset 0: processing mode 1: reset state
7	vi_ISP_rst	hardware reset of entire ISP 0: processing mode 1: reset state
6	vi_mi_soft_rst	memory interface software reset 0: processing mode 1: reset state
5	vi_jpeg_soft_rst	JPEG encoder software reset 0: processing mode 1: reset state
4	vi_srsz_soft_rst	Self-picture resize software reset 0: processing mode 1: reset state
3	vi_mrsz_soft_rst	Main-picture resize software reset 0: processing mode 1: reset state
2	vi_ycs_soft_rst	y/c splitter software reset 0: processing mode 1: reset state
1	vi_cp_soft_rst	color processing software reset 0: processing mode 1: reset state

Internal reset control register Reset value: 0000'0000H

Address: ISP_BASE + 0014H		Mode : rw
Bits	**Name**	**Description**
0	vi_isp_soft_rst	isp software reset 0: processing mode 1: reset state

Register: VI_DPCL

Data path control register Reset value: 0000'0000H

Address: ISP_BASE + 0018H		Mode : rw
Bits	**Name**	**Description**
31:12	---	unused
11	vi_dma_spmux	0: data from camera interface to self resize 1: data from DMA read port to self resize
10	vi_dma_iemux	0: data from camera interface to image effects 1: data from DMA read port to image effects
9:8	if_select	selects input interface 0: parallel interface 1: SMIA-interface 2: MIPI1-interface 3: reserved
7	---	unused
6:4	vi_dma_switch	DMA read data path selector 0: path to SPMUX 1: path to Superimpose 2: path to Image Effects 3: path to JPEG encoder 4: path to ISP Bayer RGB 5..7: reserved
3:2	vi_chan_mode	Y/C splitter channel mode 0: disabled 1: main path and raw data mode 2: self path mode 3: main and self path mode

Data path control register Reset value: 0000'0000H

Address: ISP_BASE + 0018H		Mode : rw
Bits	**Name**	**Description**
1:0	vi_mp_mux	data path selector for main path 00: data from DMA read port to JPEG encoder 01: data from main resize to MI, uncompressed

Register: IMG_EFF_CTRL

Global control register Reset value: 0000'0000H

Address: ISP_IMGEFF_BASE + 0000H		Mode : rw
Bits	**Name**	**Description**
31:6	---	unused
5	full_range	'0': pixel value range according to BT.601 '1': YCbCr full range 0...255

Address: ISP_IMGEFF_BASE + 0000H		Mode : rw
Bits	**Name**	**Description**
4	cfg_upd	write '0': nothing happens write '1': update shadow registers read: always '0'
3:1	effect_mode	effect mode 000: black & white effect (grayscale) 001: negative 010: sepia effect 011: color selection effect 100: emboss effect 101: sketch effect 110: sharpen effect 111: reserved
0	bypass_mode	bypass mode 1: processing is activated 0: processing is deactivated, bypass mode is selected
Note: full_range for image effects is supported in ISP M5_v6, M5_v7 only		

Register: IMG_EFF_COLOR_SEL

Color selection register (for color selection effect) Reset value: 0000'0000H

Address: ISP_IMGEFF_BASE + 0004H		Mode : rw
Bits	**Name**	**Description**
31:16	---	unused
15:8	color_threshold	Threshold value of the RGB colors for the color selection effect.
7:3	---	unused
2:0	color_selection	Defining the maintained color: 000: red green and blue 001: blue 010: green 011: green and blue 100: red 101: red and blue 110: red and green 111: red green and blue

Register: IMG_EFF_MAT_1

3x3 matrix coefficients for emboss effect (1) Reset value: 0000'8089H

Address: ISP_IMGEFF_BASE + 0008H		Mode : rw
Bits	Name	Description
31:16	---	unused
15	emb_coef_21_en	0: entry not used (coefficient is zero) 1: entry used
14:12	emb_coef_21	second line, left entry of 3x3 emboss effect matrix, 2 bit for coefficient, one sign bit.
11	emb_coef_13_en	0: entry not used (coefficient is zero) 1: entry used

Address: ISP_IMGEFF_BASE + 0008H		**Mode : rw**
Bits	Name	Description
10:8	emb_coef_13	first line, right entry of 3x3 emboss effect matrix, 2 bit for coefficient, one sign bit.
7	emb_coef_12_en	0: entry not used (coefficient is zero) 1: entry used
6:4	emb_coef_12	first line, middle entry of 3x3 emboss effect matrix, 2 bit for coefficient, one sign bit.
3	emb_coef_11_en	0: entry not used (coefficient is zero) 1: entry used

3x3 matrix coefficients for emboss effect (1) Reset value: 0000'8089H

Address: ISP_IMGEFF_BASE + 0008H		**Mode : rw**
Bits	**Name**	**Description**
2:0	emb_coef_11	first line, left entry of 3x3 emboss effect matrix, 2 bit for coefficient, one sign bit.
Note: possible values for coefficients: 000 (1), 001 (2), 010 (4), 011 (8),100 (-1), 101 (-2), 110 (-4), 111 (-8)		

Register: IMG_EFF_MAT_2

3x3 matrix coefficients for emboss effect (2) Reset value: 0000'C0C0H

Address: ISP_IMGEFF_BASE + 000CH		**Mode : rw**
Bits	**Name**	**Description**
31:16	---	unused
15	emb_coef_32_en	0: entry not used (coefficient is zero) 1: entry used
14:12	emb_coef_32	third line, middle entry of 3x3 emboss effect matrix, 2 bit for coefficient, one sign bit.
11	emb_coef_31_en	0: entry not used (coefficient is zero) 1: entry used
10:8	emb_coef_31	third line, left entry of 3x3 emboss effect matrix, 2 bit for coefficient, one sign bit.
7	emb_coef_23_en	0: entry not used (coefficient is zero) 1: entry used
6:4	emb_coef_23	second line, right entry of 3x3 emboss effect matrix, 2 bit for coefficient, one sign bit.
3	emb_coef_22_en	0: entry not used (coefficient is zero) 1: entry used
2:0	emb_coef_22	second line, middle entry of 3x3 emboss effect matrix, 2 bit for coefficient, one sign bit.

Register: IMG_EFF_MAT_3

3x3 matrix coefficients for emboss(3) effect / sketch/sharpen(1) effect **Reset value: 0000'CCCDH**

Address: ISP_IMGEFF_BASE + 0010H		**Mode : rw**
Bits	**Name**	**Description**
31:16	---	unused
15	sket_coef_13_en	0: entry not used (coefficient is zero) 1: entry used
14:12	sket_coef_13	first line, right entry of 3x3 sketch effect matrix, 2 bit for coefficient, one sign bit.
11	sket_coef_12_en	0: entry not used (coefficient is zero) 1: entry used
10:8	sket_coef_12	first line, middle entry of 3x3 sketch effect matrix, 2 bit for coefficient, one sign bit.
7	sket_coef_11_en	0: entry not used (coefficient is zero) 1: entry used
6:4	sket_coef_11	first line, left entry of 3x3 sketch effect matrix, 2 bit for coefficient, one sign bit.
3	emb_coef_33_en	0: entry not used (coefficient is zero) 1: entry used
2:0	emb_coef_33	third line, right entry of 3x3 emboss effect matrix, 2 bit for coefficient, one sign bit.
Note: possible values for coefficients: 000 (1), 001 (2), 010 (4), 011 (8), 100 (-1), 101 (-2), 110 (-4), 111 (-8)		

Register: IMG_EFF_MAT_4

3x3 matrix coefficients for sketch/sharpen effect (2) **Reset value: 0000'CCBCH**

Address: ISP_IMGEFF_BASE + 0014H		**Mode : rw**
Bits	**Name**	**Description**
31:16	---	unused
15	sket_coef_31_en	0: entry not used (coefficient is zero) 1: entry used
14:12	sket_coef_31	third line, left entry of 3x3 sketch effect matrix, 2 bit for coefficient, one sign bit.

Address: ISP_IMGEFF_BASE + 0014H		Mode : rw
Bits	Name	Description
11	sket_coef_23_en	0: entry not used (coefficient is zero) 1: entry used
10:8	sket_coef_23	second line, right entry of 3x3 sketch effect matrix, 2 bit for coefficient, one sign bit.
7	sket_coef_22_en	0: entry not used (coefficient is zero) 1: entry used
6:4	sket_coef_22	second line, middle entry of 3x3 sketch effect matrix, 2 bit for coefficient, one sign bit.
3	sket_coef_21_en	0: entry not used (coefficient is zero) 1: entry used
2:0	sket_coef_21	second line, left entry of 3x3 sketch effect matrix, 2 bit for coefficient, one sign bit.
Note: possible values for coefficients: 000 (1), 001 (2), 010 (4), 011 (8), 100 (-1), 101 (-2), 110 (-4), 111 (-8)		

Register: IMG_EFF_MAT_5

3x3 matrix coefficients for sketch/sharpen effect (3) **Reset value: 0000'00CCH**

Address: ISP_IMGEFF_BASE + 0018H		**Mode : rw**
Bits	**Name**	**Description**
31:8	---	unused
7	sket_coef_33_en	0: entry not used (coefficient is zero) 1: entry used
6:4	sket_coef_33	third line, right entry of 3x3 sketch effect matrix, 2 bit for coefficient, one sign bit.
3	sket_coef_32_en	0: entry not used (coefficient is zero) 1: entry used
2:0	sket_coef_32	third line, middle entry of 3x3 sketch effect matrix, 2 bit for coefficient, one sign bit.
Note: possible values for coefficients: 000 (1), 001 (2), 010 (4), 011 (8), 100 (-1), 101 (-2), 110 (-4), 111 (-8)		

Register: IMG_EFF_TINT

Chrominance increment values of a tint (used for sepia effect) Reset value: 0000'880CH

Address: ISP_IMGEFF_BASE + 001CH		**Mode : rw**
Bits	**Name**	**Description**
31:16	---	unused
15:8	incr_cr	Cr increment value of a tint. 7 bits for value, 1 sign bit. Default tint is R=162 G=138 B=101, which is used for the sepia effect. See below for the calculation of the
7:0	incr_cb	Cb increment value of a tint. 7 bits for value, 1 sign bit. Default tint is R=162 G=138 B=101, which is used for the sepia effect. See below for the calculation of the
Note: Calculation process of incr_cr and incr_cb: tint values given in RGB format: R G B converted to Cb and Cr: Cb = -0.148*R - 0.291*G + 0.439*B + 128 Cr = 0.439*R - 0.368*G - 0.071*B + 128 calculating of the increments inc_Cb = (128 – Cb)/110 inc_Cr = (128 – Cr)/110 register entry of the increments with an accuracy of 1/64 incr_cb = inc_Cb * 64 incr_cr = inc_Cr * 64		

Register: IMG_EFF_CTRL_SHD

Shadow register for control register Reset value: 0000'0000H

Address: ISP_IMGEFF_BASE + 0020H		**Mode : r**
Bits	**Name**	**Description**
31:4	---	unused
3:1	effect_mode_shd	effect mode 000: black & white effect (grayscale) 001: negative 010: sepia effect 011: color selection effect 100: emboss effect 101: sketch effect 110: sharpen effect 111: reserved
0	---	unused

Register: IMG_EFF_SHARPEN

Factor and threshold for sharpen effect Reset value: 0000'0000H

Address: ISP_IMGEFF_BASE + 0024H		**Mode : rw**
Bits	**Name**	**Description**
31:14	---	unused
13:8	sharp_factor	6Bit Factor for sharpening function. Value range is from 0x0 to 0x3F. High value means strong sharpening. The resulting factors are for example: 0x00 = 0 (no sharpen effect like bypass) 0x01 = 0.25 0x02 = 0.5 0x03 = 0.75 0x04 = 1.0 0x05 = 1.25 0x06 = 1.5 0x08 = 2.0 0x0A = 2.5 0x0C = 3.0 0x10 = 4.0 0x18 = 6.0 0x20 = 8.0 0x30 = 12.0 0x3F = 15.75
7:0	coring_thr	Threshold for coring function. This value is used to avoid amplifying noise too much by suppressing sharpening for small gradients. Higher value means less sharpening for smooth edges. Threshold zero means no coring, so all gradients are treated the same. Threshold 255 means nearly no sharpening. An absolute value for the highpass signal is defined here. The highpass signal is truncated at the defined level.
Note: For the sharpening effect the convolution mask must be set to the values [-1 -1 -1; -1 8 -1; -1 -1 -1]. The convolution mask for sharpening is defined by the values sket_coef_xx in registers IMG_EFF_MAT_3 through IMG_EFF_MAT_5. Sketch effect and sharpening effect share the same mask registers.		

Register: SUPER_IMP_CTRL
Global control register Reset value: 0000'0000H

Address: ISP_SI_BASE + 0000H		**Mode : rw**
Bits	**Name**	**Description**
31:2	---	unused

Global control register Reset value: 0000'0000H

Address: ISP_SI_BASE + 0000H		Mode : rw
Bits	**Name**	**Description**
2	transparency_mode	transparency mode 1: transparency mode disabled 0: transparency mode enabled
1	ref_image	Define the reference image 1: superimpose bitmap from main memory 0: image from the Image Effect module Note: the reference image defines the size of the
0	bypass_mode	Bypass mode 0: bypass mode 1: normal operation Note: in the bypass mode the data stream from Image Effect is transmitted to MUX module without overlaying

Register: SUPER_IMP_OFFSET_X
Offset x register Reset value: 0000'0000H

Address: ISP_SI_BASE + 0004H		Mode : rw
Bits	**Name**	**Description**
31:14	---	unused
13:1	offset_x	Offset X Note: the bit 0 is don“t care (write 1 doesn“t have any effect, the read access always gives „0“) Note: the offset_x is positive and refers to the reference image
0	---	unused

Register: SUPER_IMP_OFFSET_Y

Offset y register Reset value: 0000'0000H

Address: ISP_SI_BASE + 0008H		Mode : rw
Bits	**Name**	**Description**
31:14	---	unused
13:0	offset_y	Offset Y Note: the offset_y is positive and refers to the reference image

Register: SUPER_IMP_COLOR_Y

Y component of transparent key color Reset value: 0000'0000H

Address: ISP_SI_BASE + 000CH		Mode : rw
Bits	**Name**	**Description**
31:8	---	unused
7:0	y_comp	Y component of transparent key color

Register: SUPER_IMP_COLOR_CB

Cb component of transparent key color Reset value: 0000'0000H

Address: ISP_SI_BASE + 0010H		Mode : rw
Bits	**Name**	**Description**
31:8	---	unused
7:0	cb_comp	Cb component of transparent key color

Register: SUPER_IMP_COLOR_CR

Cr component of transparent key color Reset value: 0000'0000H

Address: ISP_SI_BASE + 0014H		Mode : rw
Bits	**Name**	**Description**
31:8	---	unused
7:0	cr_comp	Cr component of transparent key color

Register: ISP_CTRL

global control register Reset value: 0000'0000H

Address: ISP_MISP_BASE + 0000H		Mode : rw
Bits	**Name**	**Description**
31:17	---	unused
16	CTRL_RESERVED_1	reserved
15	CTRL_RESERVED_2	reserved

global control register Reset value: 0000'0000H

Address: ISP_MISP_BASE + 0000H		**Mode : rw**
its	Name	Description
4	ISP_CSM_C_RANGE	Color Space Matrix chrominance clipping range for ISP output 0: CbCr range 64..960 (16..240) according to ITU-R BT.601 standard 1: full UV range 0..1023 (0..255) Numbers in brackets are for 8 bit resolution. This bit also configures the YCbCr sequence align block accordingly
3	ISP_CSM_Y_RANGE	Color Space Matrix luminance clipping range for ISP output 0: Y range 64..940 (16..235) according to ITU-R BT.601 standard 1: full Y range 0..1023 (0..255) Numbers in brackets are for 8 bit resolution. This bit also configures the YCbCr sequence align block
2	ISP_FLASH_MODE	0: sensor interface works independently from flash control unit 1: one frame is captured when signaled by flash control
1	ISP_GAMMA_OUT_ENABLE	gamma ON/OFF
0	ISP_GEN_CFG_UPD	1: generate frame synchronous configuration signal at the output of ISP for shadow registers of the following processing modules, write only
	ISP_CFG_UPD	1: immediately configure (update) shadow registers, write only
	ISP_CFG_UPD_PERMANENT	1: permanent configure (update) shadow registers on frame end.
	ISP_AWB_ENABLE	auto white balance ON/OFF
	ISP_GAMMA_IN_ENABLE	Sensor De-gamma ON/OFF
	---	unused
	ISP_INFORM_ENABLE	1: input formatter enabled 0: input formatter disabled The ISP input formatter is enabled or disabled by this bit immediately, but always starts or stops acquisition frame synchronously.

Address: ISP_MISP_BASE + 0000H		Mode : rw
Bits	**Name**	**Description**
3:1	ISP_MODE	000 - RAW picture with BT.601 sync (ISP bypass) 001 - ITU-R BT.656 (YUV with embedded sync) 010 - ITU-R BT.601 (YUV input with H and Vsync signals) 011 - Bayer RGB processing with H and Vsync signals - data mode (ISP bypass, sync signals interpreted as data enable) - Bayer RGB processing with BT.656 synchronization 110 - RAW picture with ITU-R BT.656 synchronization (ISP bypass) 111 - reserved Side effect: If RAW, BT.601, BT.656, or data mode is selected, the clock of the ISP SRAMs (ISP line buffer, Lens Shading, Bad Pixel) is switched off. Only in Bayer RGB mode the clock to the SRAMs is enabled. This further reduces power consumption
0	ISP_ENABLE	1: ISP data output enabled 0: ISP data output disabled Controls output formatter frame synchronously, if isp_gen_cfg_upd is used to activate this bit. For immediate update isp_cfg_upd must be used
Note: partly write-only		

Register: ISP_ACQ_PROP

ISP acquisition properties Reset value: 0000'0000H

Address: ISP_MISP_BASE + 0004H		Mode : rw
Bits	**Name**	**Description**
31:17	---	unused
16	DMA_YUV_SELECTION	0: use align or conversion data for isp_is input. 1: use dma yuv read data for isp_is input
15	DMA_RGB_SELECTION	0: use input formatter data for latency fifo. 1: use dma rgb read data for latency fifo

ISP acquisition properties Reset value: 0000'0000H

Address: ISP_MISP_BASE + 0004H		**Mode : rw**
Bits	**Name**	**Description**
14:12	INPUT_SELECTION	000 000- 12Bit external Interface 001- 10Bit Interface, append 2 zeroes as LSBs 010- 10Bit Interface, append 2 MSBs as LSBs 011- 8Bit Interface, append 4 zeroes as LSBs 100- 8Bit Interface, append 4 MSBs as LSBs 101...111 reserved
11	FIELD_INV	1: swap odd and even fields 0: do not swap fields
10:9	FIELD_SELECTION	00- sample all fields (don"t care about fields) 01- sample only even fields 10- sample only odd fields 11- reserved
8:7	CCIR_SEQ	00- YCbYCr 01- YCrYCb 10- CbYCrY 11- CrYCbY
6:5	CONV_422	co-sited color subsampling Y0Cb0Cr0 – Y1 interleaved color subsampling Y0Cb0 – Y1Cr1 (not recommended) 10- non-cosited color subsampling Y0Cb(0+1)/2 – Y1Cr(0+1)/2 11- reserved
4:3	BAYER_PAT	color components from sensor, starting with top left position in sampled frame (reprogram with ISP_ACQ_H_OFFS, ISP_ACQ_V_OFFS) 00- first line: RGRG..., second line: GBGB..., etc. 01- first line: GRGR..., second line: BGBG..., etc. 10- first line: GBGB..., second line: RGRG..., etc. 11- first line: BGBG..., second line: GRGR..., etc. This configuration applies for the black level area after cropping by the input formatter.
2	VSYNC_POL	vertical sync polarity 0: high active 1: low active
1	HSYNC_POL	horizontal sync polarity 0: high active 1: low active
0	SAMPLE_EDGE	0- negative edge sampling 1- positive edge sampling

Register: ISP_ACQ_H_OFFS

horizontal input offset Reset value: 0000'0000H

Address: ISP_MISP_BASE + 0008H			Mode : rw
Bits	Name	Description	
31:15	---	unused	
14:0	ACQ_H_OFFS	horizontal sample offset in 8-bit samples (yuv: 4 samples=2pix)	

Register: ISP_ACQ_V_OFFS

vertical input offset Reset value: 0000'0000H

Address: ISP_MISP_BASE + 000CH			Mode : rw
Bits	Name	Description	
31:14	---	unused	
13:0	ACQ_V_OFFS	vertical sample offset in lines	

Register: ISP_ACQ_H_SIZE

horizontal input size Reset value: 0000'1000H

Address: ISP_MISP_BASE + 0010H			Mode : rw
Bits	Name	Description	
31:15	---	unused	
14:0	ACQ_H_SIZE	horizontal sample size in 12-bit samples YUV input: 2 samples = 1 pixel, else 1 sample = 1 pixel; So in YUV mode ACQ_H_SIZE must be twice as large as horizontal image size horizontal image size must always be even exept in raw picture mode; if an odd size is programmed the value will be truncated to even size	

Register: ISP_ACQ_V_SIZE

vertical input size Reset value: 0000'0C00H

Address: ISP_MISP_BASE + 0014H			Mode : rw
Bits	Name	Description	
31:14	---	unused	

vertical input size Reset value: 0000'0C00H

Address: ISP_MISP_BASE + 0014H		Mode : rw
Bits	**Name**	**Description**
13:0	ACQ_V_SIZE	vertical sample size in lines

Register: ISP_ACQ_NR_FRAMES

Number of frames to be captured Reset value: 0000'0000H

Address: ISP_MISP_BASE + 0018H		Mode : rw
Bits	**Name**	**Description**
31:10	---	unused
9:0	ACQ_NR_FRAMES	number of input frames to be sampled (0 = continuous)

Register: ISP_GAMMA_DX_LO

De-Gamma Curve definition lower x increments (sampling points) Reset value: 4444'4444H

Address: ISP_MISP_BASE + 001CH		Mode : rw
Bits	**Name**	**Description**
31	---	unused
30:28	GAMMA_DX_8	gamma curve sample point definition x-axis (input)
27	---	unused
26:24	GAMMA_DX_7	gamma curve sample point definition x-axis (input)
23	---	unused
22:20	GAMMA_DX_6	gamma curve sample point definition x-axis (input)
19	---	unused
18:16	GAMMA_DX_5	gamma curve sample point definition x-axis (input)
15	---	unused
14:12	GAMMA_DX_4	gamma curve sample point definition x-axis (input)
11	---	unused
10:8	GAMMA_DX_3	gamma curve sample point definition x-axis (input)
7	---	unused
6:4	GAMMA_DX_2	gamma curve sample point definition x-axis (input)

De-Gamma Curve definition lower x increments (sampling points) Reset value: 4444'4444H

Address: ISP_MISP_BASE + 001CH		Mode : rw
Bits	**Name**	**Description**
3	---	unused
2:0	GAMMA_DX_1	gamma curve sample point definition x-axis (input)

Register: ISP_GAMMA_DX_HI

De-Gamma Curve definition higher x increments (sampling points) Reset value: 4444'4444H

Address: ISP_MISP_BASE + 0020H		Mode : rw
Bits	**Name**	**Description**
31	---	unused
30:28	GAMMA_DX_16	gamma curve sample point definition x-axis (input)
27	---	unused
26:24	GAMMA_DX_15	gamma curve sample point definition x-axis (input)
23	---	unused
22:20	GAMMA_DX_14	gamma curve sample point definition x-axis (input)
19	---	unused
18:16	GAMMA_DX_13	gamma curve sample point definition x-axis (input)
15	---	unused
14:12	GAMMA_DX_12	gamma curve sample point definition x-axis (input)
11	---	unused
10:8	GAMMA_DX_11	gamma curve sample point definition x-axis (input)
7	---	unused
6:4	GAMMA_DX_10	gamma curve sample point definition x-axis (input)
3	---	unused
2:0	GAMMA_DX_9	gamma curve sample point definition x-axis (input)

Register: ISP_GAMMA_R_Y

De-Gamma Curve definition y red n (n=0..16) Reset value: 0H

Address: ISP_MISP_BASE + 0024H + (4H * n)		Mode : rw
Bits	**Name**	**Description**
31:12	---	unused
11:0	GAMMA_R_Y	gamma curve point definition y-axis (output) for red RESTRICTION: each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is
Note: The reset values define a linear curve which has the same effect as bypass. Reset values are: Y_00 = 0x0000, Y_01 = 0x0100, Y_02 = 0x0200, Y_03 = 0x0300, Y_04 = 0x0400,Y_05 = 0x0500, Y_06 = 0x0600, Y_07 = 0x0700, Y_08 = 0x0800, Y_09 = 0x0900, Y_10 = 0x0A00, Y_11 = 0x0B00, Y_12 = 0x0C00, Y_13 = 0x0D00, Y_14 = 0x0E00, Y_15 = 0x0F00, Y_16 = 0x0FFF		

Register: ISP_GAMMA_G_Y

De-Gamma Curve definition y green n (n=0..16) Reset value: 0H

Address: ISP_MISP_BASE + 0068H + (4H * n)		Mode : rw
Bits	**Name**	**Description**
31:12	---	unused
11:0	GAMMA_G_Y	gamma curve point definition y-axis (output) for green RESTRICTION: each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed !)
Note: The reset values define a linear curve which has the same effect as bypass. Reset values are: Y_00 = 0x0000, Y_01 = 0x0100, Y_02 = 0x0200, Y_03 = 0x0300, Y_04 = 0x0400,Y_05 = 0x0500, Y_06 = 0x0600, Y_07 = 0x0700, Y_08 = 0x0800, Y_09 = 0x0900, Y_10 = 0x0A00, Y_11 = 0x0B00, Y_12 = 0x0C00, Y_13 = 0x0D00, Y_14 = 0x0E00, Y_15 = 0x0F00, Y_16 = 0x0FFF		

Register: ISP_GAMMA_B_Y

De-Gamma Curve definition y blue n (n=0..16) Reset value: 0H

Address: ISP_MISP_BASE + 00ACH + (4H * n)		Mode : rw
Bits	**Name**	**Description**
31:12	---	unused

De-Gamma Curve definition y blue n (n=0..16) Reset value: 0H

Address: ISP_MISP_BASE + 00ACH + (4H * n)		Mode : rw
Bits	**Name**	**Description**
11:0	GAMMA_B_Y	gamma curve point definition y-axis (output) for blue RESTRICTION: each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed !)
Note: The reset values define a linear curve which has the same effect as bypass. Reset values are: Y_00 = 0x0000, Y_01 = 0x0100, Y_02 = 0x0200, Y_03 = 0x0300, Y_04 = 0x0400, Y_05 = 0x0500, Y_06 = 0x0600, Y_07 = 0x0700, Y_08 = 0x0800, Y_09 = 0x0900, Y_10 = 0x0A00, Y_11 = 0x0B00, Y_12 = 0x0C00, Y_13 =		

Register: ISP_AWB_PROP

Auto white balance properties Reset value: 0000'0000H

Address: ISP_MISP_BASE + 0110H		Mode : rw
Bits	**Name**	**Description**
31	AWB_MEAS_MODE	1: RGB based measurement mode 0: near white discrimination mode using YCbCr color space
30:2	---	unused
2	AWB_MAX_EN	1: enable Y_MAX compare 0: disable Y_MAX compare
1:0	AWB_MODE	AWB_MODE(1:0): 11: reserved 10: measurement of YCbCr means (AWB_MEAS_MODE = 0) or RGB means (AWB_MEAS_MODE = 1) 01: reserved
Note: The following conversion matrix is used for calculating the YCbCr values: Y = 16 + 0.2500 R + 0.5000 G + 0.1094 B Cb = 128 - 0.1406 R - 0.2969 G + 0.4375 B Cr = 128 + 0.4375 R - 0.3750 G - 0.0625 B		

Register: ISP_AWB_H_OFFS

Auto white balance horizontal offset of measure window Reset value: 0000'0000H

Address: ISP_MISP_BASE + 0114H			Mode : rw
Bits	Name	Description	
31:13	---	unused	
12:0	AWB_H_OFFS	horizontal window offset in pixel	

Register: ISP_AWB_V_OFFS

Auto white balance vertical offset of measure window Reset value: 0000'0000H

Address: ISP_MISP_BASE + 0118H			Mode : rw
Bits	Name	Description	
31:13	---	unused	
12:0	AWB_V_OFFS	vertical window offset in lines	

Register: ISP_AWB_H_SIZE

Auto white balance horizontal window size Reset value: 0000'0000H

Address: ISP_MISP_BASE + 011CH			Mode : rw
Bits	Name	Description	
31:14	---	unused	
13:0	AWB_H_SIZE	horizontal measurement window size in pixel	

Register: ISP_AWB_V_SIZE

Auto white balance vertical window size Reset value: 0000'0000H

Address: ISP_MISP_BASE + 0120H			Mode : rw
Bits	Name	Description	
31:14	---	unused	
13:0	AWB_V_SIZE	vertical measurement window size in lines	

Register: ISP_AWB_FRAMES

Auto white balance mean value over multiple frames Reset value: 0000'0000H

Address: ISP_MISP_BASE + 0124H		Mode : rw
Bits	**Name**	**Description**
31:3	---	unused
2:0	AWB_FRAMES	number of frames-1 used for mean value calculation (value of 0 means 1 frame, value of 7 means 8 frames)

Register: ISP_AWB_REF
Auto white balance reference Cb/Cr values Reset value: 0000'8080H

Address: ISP_MISP_BASE + 0128H		Mode : rw
Bits	**Name**	**Description**
31:16	---	unused
15:8	AWB_REF_CR MAX_R	reference Cr value for AWB regulation, target for AWB maximum red value, if RGB measurement mode is selected
7:0	AWB_REF_CB MAX_B	reference Cb value for AWB regulation, target for AWB maximum blue value, if RGB measurement mode is selected

Register: ISP_AWB_THRESH

Auto white balance threshold values Reset value: E9C0'1010H

Address: ISP_MISP_BASE + 012CH		Mode : rw
Bits	**Name**	**Description**
31:24	AWB_MAX_Y	Luminance maximum value, only consider pixels with luminance smaller than threshold for the WB measurement (must be enabled by register AWB_MODE bit AWB_MAX_EN). Not valid for RGB measurement mode.
23:16	AWB_MIN_Y MAX_G	Luminance minimum value, only consider pixels with luminance greater than threshold for the WB measurement maximum green value, if RGB measurement mode is
15:8	AWB_MAX_CSUM	Chrominance sum maximum value, only consider pixels with Cb+Cr smaller than threshold for WB measurements
7:0	AWB_MIN_C	Chrominance minimum value, only consider pixels with Cb/Cr each greater than threshold value for WB measurements

Register: ISP_AWB_GAIN_G

Auto white balance gain green Reset value: 0100'0100H

Address: ISP_MISP_BASE + 0138H		Mode : rw
Bits	**Name**	**Description**
31:26	---	unused
25:16	AWB_GAIN_GR	gain value for green component in red line 100h = 1, unsigned integer value, range 0 to 4 with 8 bit fractional part
15:10	---	unused
9:0	AWB_GAIN_GB	gain value for green component in blue line 100h = 1, unsigned integer value, range 0 to 4 with 8 bit fractional part

Register: ISP_AWB_GAIN_RB

Auto white balance gain red and blue Reset value: 0100'0100H

Address: ISP_MISP_BASE + 013CH		Mode : rw
Bits	**Name**	**Description**
31:26	---	unused
25:16	AWB_GAIN_R	gain value for red component 100h = 1, unsigned integer value, range 0 to 4 with 8 bit fractional part
15:10	---	unused
9:0	AWB_GAIN_B	gain value for blue component 100h = 1, unsigned integer value, range 0 to 4 with 8 bit fractional part

Register: ISP_AWB_WHITE_CNT

Auto white balance white pixel count Reset value: 0000'0000H

Address: ISP_MISP_BASE + 0140H		Mode : r
Bits	**Name**	**Description**
31:26	---	unused
25:0	AWB_WHITE_CNT	White pixel count, number of "white pixels" found during last measurement, i.e. pixels included in mean value calculation

Register: ISP_AWB_MEAN

Auto white balance measured mean value Reset value: 0000'0000H

Address: ISP_MISP_BASE + 0144H		**Mode : r**
Bits	**Name**	**Description**
31:24	---	unused
23:16	AWB_MEAN_Y G	mean value of Y within window and frames mean value of green, if RGB measurement mode is selected
15:8	AWB_MEAN_CB B	mean value of Cb within window and frames mean value of blue, if RGB measurement mode is selected
7:0	AWB_MEAN_CR R	mean value of Cr within window and frames mean value of red, if RGB measurement mode is selected

Register: ISP_CC_COEFF_0
Color conversion coefficient 0 Reset value: 0021H

Address: ISP_MISP_BASE + 0170H		**Mode : rw**
Bits	**Name**	**Description**
31:9	---	unused
8:0	cc_coeff_0	coefficient 0 for color space conversion
Note: all color conversion coefficients are signed integer values with 7 bit fractional part, range -2 to 1.992		

Register: ISP_CC_COEFF_1

Color conversion coefficient 1 Reset value: 0040H

Address: ISP_MISP_BASE + 0174H		**Mode : rw**
Bits	**Name**	**Description**
31:9	---	unused
8:0	cc_coeff_1	coefficient 1 for color space conversion

Register: ISP_CC_COEFF_2

Color conversion coefficient 2 Reset value: 000DH

Address: ISP_MISP_BASE + 0178H		Mode : rw
Bits	**Name**	**Description**
31:9	---	unused
8:0	cc_coeff_2	coefficient 2 for color space conversion

Register: ISP_CC_COEFF_3

Color conversion coefficient 3 Reset value: 01EDH

Address: ISP_MISP_BASE + 017CH		Mode : rw
Bits	**Name**	**Description**
31:9	---	unused
8:0	cc_coeff_3	coefficient 3 for color space conversion

Register: ISP_CC_COEFF_4

Color conversion coefficient 4 Reset value: 01DBH

Address: ISP_MISP_BASE + 0180H		Mode : rw
Bits	**Name**	**Description**
31:9	---	unused
8:0	cc_coeff_4	coefficient 4 for color space conversion

Register: ISP_CC_COEFF_5

Color conversion coefficient 5 Reset value: 0038H

Address: ISP_MISP_BASE + 0184H		Mode : rw
Bits	**Name**	**Description**
31:9	---	unused
8:0	cc_coeff_5	coefficient 5 for color space conversion

Register: ISP_CC_COEFF_6

Color conversion coefficient 6 Reset value: 0038H

Address: ISP_MISP_BASE + 0188H			Mode : rw
Bits	**Name**	**Description**	
31:9	---	unused	
8:0	cc_coeff_6	coefficient 6 for color space conversion	

Register: ISP_CC_COEFF_7

Color conversion coefficient 7 Reset value: 0'01D1H

Address: ISP_MISP_BASE + 018CH			Mode : rw
Bits	**Name**	**Description**	
31:9	---	unused	
8:0	cc_coeff_7	coefficient 7 for color space conversion	

Register: ISP_CC_COEFF_8

Color conversion coefficient 8 Reset value: 01F7H

Address: ISP_MISP_BASE + 0190H			Mode : rw
Bits	**Name**	**Description**	
31:9	---	unused	
8:0	cc_coeff_8	coefficient 8 for color space conversion	

Register: ISP_OUT_H_OFFS

Horizontal offset of output window Reset value: 0000'0000H

Address: ISP_MISP_BASE + 0194H			Mode : rw
Bits	**Name**	**Description**	
31:14	---	unused	
13:0	ISP_OUT_H_OFFS	vertical pic offset in lines	

Register: ISP_OUT_V_OFFS

Vertical offset of output window Reset value: 0000'0000H

Address: ISP_MISP_BASE + 0198H			Mode : rw
Bits	**Name**	**Description**	
31:14	---	unused	
13:0	ISP_OUT_V_OFFS	vertical pic offset in lines	

Register: ISP_OUT_H_SIZE

Output horizontal picture size Reset value: 0000'1000H

Address: ISP_MISP_BASE + 019CH			Mode : rw
Bits	**Name**	**Description**	
31:15	---	unused	
14:0	ISP_OUT_H_SIZE	horizontal picture size in pixel if ISP_MODE is set to 001-(ITU-R BT.656 YUV), 010-(ITU-R BT.601 YUV), 011-(ITU-R BT.601 Bayer RGB), 101-(ITU-R BT.656 Bayer RGB) only even numbers are accepted, because complete quadruples of YUYV(YCbYCr) are needed for the 422 output. (if an odd size is programmed the value will be truncated to even size)	

Register: ISP_OUT_V_SIZE

Output vertical picture size Reset value: 0000'0C00H

Address: ISP_MISP_BASE + 01A0H			Mode : rw
Bits	**Name**	**Description**	
31:14	---	unused	
13:0	ISP_OUT_V_SIZE	vertical pic size in lines	

Register: ISP_DEMOSAIC

Demosaic parameters Reset value: 0000'0004H

Address: ISP_MISP_BASE + 01A4H		**Mode : rw**
Bits	**Name**	**Description**
31:11	---	unused
10	DEMOSAIC_BYPASS	0: normal operation for RGB Bayer Pattern input 1: demosaicing bypass for Black&White input data
9:8	---	unused
7:0	DEMOSAIC_TH	Threshold for Bayer demosaicing texture detection. This value shifted left 4bit is compared with the difference of the vertical and horizontal 12Bit wide texture indicators, to decide if the vertical or horizontal texture flag must be set. 0xFF: no texture detection 0x00: maximum edge

Register: ISP_FLAGS_SHD

Flags (current status) of certain signals and Shadow regs for enable signals Reset value: 0000'0000H

Address: ISP_MISP_BASE + 01A8H		**Mode : r**
Bits	**Name**	**Description**
31	S_HSYNC	state of ISP input port s_hsync, for test purposes
30	S_VSYNC	state of ISP input port s_vsync, for test purposes
29:28	---	unused
27:16	S_DATA	state of ISP input port s_data, for test purposes
15:3	---	unused
2	INFORM_FIELD	current field information (0=odd, 1=even)
1	ISP_INFORM_ENABLE_SHD	Input formatter enable shadow register
0	ISP_ENABLE_SHD	ISP enable shadow register shows, if ISP currently outputs data (1) or not (0)

Register: ISP_OUT_H_OFFS_SHD

current horizontal offset of output window (shadow register) **Reset value: 0000'0000H**

Address: ISP_MISP_BASE + 01ACH			Mode : r
Bits	**Name**	**Description**	
31:14	---	unused	
13:0	ISP_OUT_H_OFFS_SHD	current vertical pic offset in lines	

Register: ISP_OUT_V_OFFS_SHD

current vertical offset of output window (shadow register) **Reset value: 0000'0000H**

Address: ISP_MISP_BASE + 01B0H			Mode : r
Bits	**Name**	**Description**	
31:14	---	unused	
13:0	ISP_OUT_V_OFFS_SHD	current vertical pic offset in lines	

Register: ISP_OUT_H_SIZE_SHD

current output horizontal picture size (shadow register) **Reset value: 0000'0000H**

Address: ISP_MISP_BASE + 01B4H			Mode : r
Bits	**Name**	**Description**	
31:15	---	unused	
14:0	ISP_OUT_H_SIZE_SHD	current horizontal pic size in pixel	

Register: ISP_OUT_V_SIZE_SHD

current output vertical picture size (shadow register) **Reset value: 0000'0000H**

Address: ISP_MISP_BASE + 01B8H			Mode : r
Bits	**Name**	**Description**	
31:14	---	unused	
13:0	ISP_OUT_V_SIZE_SHD	vertical pic size in lines	

Register: ISP_IMSC

Interrupt mask Reset value: 0000'0000H

Address: ISP_MISP_BASE + 01BCH		**Mode : rw**
Bits	**Name**	**Description**
31:20	---	unused
19	IMSC_VSM_END	enable interrupt (1) or mask out (0)
18	IMSC_EXP_END	enable interrupt (1) or mask out (0)
17	IMSC_FLASH_CAP	enable interrupt (1) or mask out (0)
16	IMSC_RESERVED_1	enable interrupt (1) or mask out (0)
15	IMSC_HIST_MEASURE_RDY	enable interrupt (1) or mask out (0)
14	IMSC_AFM_FIN	enable interrupt (1) or mask out (0)
13	IMSC_AFM_LUM_OF	enable interrupt (1) or mask out (0)
12	IMSC_AFM_SUM_OF	enable interrupt (1) or mask out (0)
11	IMSC_SHUTTER_OFF	enable interrupt (1) or mask out (0)
10	IMSC_SHUTTER_ON	enable interrupt (1) or mask out (0)
9	IMSC_FLASH_OFF	enable interrupt (1) or mask out (0)
8	IMSC_FLASH_ON	enable interrupt (1) or mask out (0)
7	IMSC_H_START	enable interrupt (1) or mask out (0)
6	IMSC_V_START	enable interrupt (1) or mask out (0)
5	IMSC_FRAME_IN	enable interrupt (1) or mask out (0)
4	IMSC_AWB_DONE	enable interrupt (1) or mask out (0)
3	IMSC_PIC_SIZE_ERR	enable interrupt (1) or mask out (0)
2	IMSC_DATA_LOSS	enable interrupt (1) or mask out (0)
1	IMSC_FRAME	enable interrupt (1) or mask out (0)
0	IMSC_ISP_OFF	enable interrupt (1) or mask out (0)

Register: ISP_RIS

Raw interrupt status Reset value: 0000'0000H

Address: ISP_MISP_BASE + 01C0H		**Mode : r**
Bits	**Name**	**Description**
31:20	---	unused
19	RIS_VSM_END	VSM measurement complete
18	RIS_EXP_END	Exposure measurement complete
17	RIS_FLASH_CAP	Signaling captured frame
16	RIS_RESERVED_1	reserved
15	RIS_HIST_MEASURE_RDY	Histogram measurement ready. (old or new histogram measurement)
14	RIS_AFM_FIN	AF measurement finished: this interrupt is set when the first complete frame is calculated after enabling the AF measurement
13	RIS_AFM_LUM_OF	Auto focus luminance overflow
12	RIS_AFM_SUM_OF	Auto focus sum overflow
11	RIS_SHUTTER_OFF	Mechanical shutter is switched off
10	RIS_SHUTTER_ON	Mechanical shutter is switched on
9	RIS_FLASH_OFF	Flash light is switched off
8	RIS_FLASH_ON	Flash light is switched on
7	RIS_H_START	Start edge of h_sync
6	RIS_V_START	Start edge of v_sync
5	RIS_FRAME_IN	sampled input frame is complete
4	RIS_AWB_DONE	White balancing measurement cycle is complete, results can be read out
3	RIS_PIC_SIZE_ERR	pic size violation occurred, programming seems wrong
2	RIS_DATA_LOSS	loss of data occurred within a line, processing failure
1	RIS_FRAME	frame was completely put out
0	RIS_ISP_OFF	isp output was disabled (vsynced) due to f_cnt reached or manual

Register: ISP_MIS

Masked interrupt status Reset value: 0000'0000H

Address: ISP_MISP_BASE + 01C4H		**Mode : r**
Bits	**Name**	**Description**
31:20	---	unused
19	MIS_VSM_END	VSM measurement complete
18	MIS_EXP_END	Exposure measurement complete
17	MIS_FLASH_CAP	Captured is frame is detected
16	MIS_RESERVED_1	reserved
15	MIS_HIST_MEASURE_RDY	Histogram measurement ready. (old or new histogram measurement)
14	MIS_AFM_FIN	AF measurement finished: this interrupt is set when the first complete frame is calculated after enabling the AF measurement
13	MIS_AFM_LUM_OF	Luminance overflow
12	MIS_AFM_SUM_OF	Sum overflow
11	MIS_SHUTTER_OFF	Mechanical shutter is switched off
10	MIS_SHUTTER_ON	Mechanical shutter is switched on
9	MIS_FLASH_OFF	Flash light is switched off
8	MIS_FLASH_ON	Flash light is switched on
7	MIS_H_START	Start edge of h_sync
6	MIS_V_START	Start edge of v_sync
5	MIS_FRAME_IN	sampled input frame is complete
4	MIS_AWB_DONE	White balancing measurement cycle is complete, results can be read out
3	MIS_PIC_SIZE_ERR	pic size violation occurred, programming seems wrong
2	MIS_DATA_LOSS	loss of data occurred within a line, processing failure
1	MIS_FRAME	frame was completely put out
0	MIS_ISP_OFF	isp was turned off (vsynced) due to f_cnt reached or manual

Register: ISP_ICR

Interrupt clear register Reset value: 0000'0000H

Address: ISP_MISP_BASE + 01C8H		**Mode : w**
Bits	**Name**	**Description**
31:20	---	unused
19	ICR_VSM_END	clear interrupt
18	ICR_EXP_END	clear interrupt
17	ICR_FLASH_CAP	clear interrupt
16	ICR_RESERVED_1	clear interrupt
15	ICR_HIST_MEASURE_RDY	clear interrupt
14	ICR_AFM_FIN	clear interrupt
13	ICR_AFM_LUM_OF	clear interrupt
12	ICR_AFM_SUM_OF	clear interrupt
11	ICR_SHUTTER_OFF	clear interrupt
10	ICR_SHUTTER_ON	clear interrupt
9	ICR_FLASH_OFF	clear interrupt
8	ICR_FLASH_ON	clear interrupt
7	ICR_H_START	clear interrupt
6	ICR_V_START	clear interrupt
5	ICR_FRAME_IN	clear interrupt
4	ICR_AWB_DONE	clear interrupt
3	ICR_PIC_SIZE_ERR	clear interrupt
2	ICR_DATA_LOSS	clear interrupt
1	ICR_FRAME	clear interrupt
0	ICR_ISP_OFF	clear interrupt

Register: ISP_ISR

Interrupt set register Reset value: 0000'0000H

Address: ISP_MISP_BASE + 01CCH		**Mode : w**
Bits	**Name**	**Description**
31:20	---	unused
19	ISR_VSM_END	set interrupt
18	ISR_EXP_END	set interrupt
17	ISR_FLASH_CAP	set interrupt
16	ISR_RESERVED_1	set interrupt
15	ISR_HIST_MEASURE_RDY	set interrupt
14	ISR_AFM_FIN	set interrupt
13	ISR_AFM_LUM_OF	set interrupt
12	ISR_AFM_SUM_OF	set interrupt
11	ISR_SHUTTER_OFF	set interrupt
10	ISR_SHUTTER_ON	set interrupt
9	ISR_FLASH_OFF	set interrupt
8	ISR_FLASH_ON	set interrupt
7	ISR_H_START	set interrupt
6	ISR_V_START	set interrupt
5	ISR_FRAME_IN	set interrupt
4	ISR_AWB_DONE	set interrupt
3	ISR_PIC_SIZE_ERR	set interrupt
2	ISR_DATA_LOSS	set interrupt
1	ISR_FRAME	set interrupt
0	ISR_ISP_OFF	set interrupt

Register: ISP_CT_COEFF

cross-talk configuration register (color correction matrix) n (n=0..8) Reset value: 0H

Address: ISP_MISP_BASE + 01D0H + (4H * n)		Mode : rw
Bits	**Name**	**Description**
31:11	---	unused
10:0	ct_coeff	Coefficient n for cross talk matrix. Values are 11-bit signed fixed-point numbers with 4 bit integer and 7 bit fractional part, ranging from -8 (0x400) to +7.992 (0x3FF). 0 is reprsented by 0x000 and a coefficient value of 1 as 0x080.
Note: Reset values generate a matrix which does not modify the pixel values. Reset values are: coeff_0 = 0x80, coeff_1 = 0x00, coeff_2 = 0x00, coeff_3 = 0x00, coeff_4 = 0x80, coeff_5 = 0x00, coeff_6 = 0x00, coeff_7 = 0x00, coeff_8 = 0x80		

Register: ISP_GAMMA_OUT_MODE

gamma segmentation mode register for output gamma Reset value: 0000'0000H

Address: ISP_MISP_BASE + 01F4H		Mode : rw
Bits	**Name**	**Description**
31:1	---	unused
0	equ_segm	0: logarithmic like segmentation of gamma curve (default after reset) segmentation from 0 to 4095: 64 64 64 64 128 128 128 128 256 256 256 512 512 512 512 512 1: equidistant segmentation (all 16 segments are

Register: ISP_GAMMA_OUT_Y

Gamma Out Curve definition y_ n (n=0..16) Reset value: 0H

Address: ISP_MISP_BASE + 01F8H + (4H * n)		Mode : rw
Bits	**Name**	**Description**
31:10	---	unused

Gamma Out Curve definition y_ n (n=0..16) Reset value: 0H

Address: ISP_MISP_BASE + 01F8H + (4H * n)		Mode : rw
Bits	**Name**	**Description**
9:0	isp_gamma_out_y	Gamma_out curve point definition y-axis (output) for all color components (red,green,blue) RESTRICTION: The difference between two Y_n (dy = Y_n - Y_n-1) is restricted to +511/-512 (10 bit signed)!
Note: Reset values generate a standard gamma of 2.2. Reset values are: y_00 = 0x000, y_01 = 0x049, y_02 = 0x089, y_03 = 0x0B7, y_04 = 0x0DF, y_05 = 0x11F, y_06 = 0x154, y_07 = 0x183, y_08 = 0x1AD, y_09 = 0x1F6, y_10 = 0x235, y_11 = 0x26F, y_12 = 0x2D3, y_13 = 0x32A, y_14 = 0x378, y_15 = 0x3BF, y_16 = 0x3FF		

Register: ISP_ERR

ISP error register Reset value: 0000'0000H

Address: ISP_MISP_BASE + 023CH		Mode : r
Bits	**Name**	**Description**
31:3	---	unused
2	outform_size_err	size error is generated in outmux submodule
1	is_size_err	size error is generated in image stabilization submodule
0	inform_size_err	size error is generated in inform submodule
Note: For debug purposes the ISP_ERR und ISP_ERR_CLR are implemented. For the case when a PIC_SIZE_ERR interrupt is signaled the SW is able to see in which submodule this error is generated. Writing to the ISP_ERR_CLR register clears this bit.		

Register: ISP_ERR_CLR

ISP error clear register Reset value: 0000'0000H

Address: ISP_MISP_BASE + 0240H		Mode : w
Bits	**Name**	**Description**
31:3	---	unused
2	outform_size_err_clr	size error is cleared
1	is_size_err_clr	size error is cleared
0	inform_size_err_clr	size error is cleared

Register: ISP_FRAME_COUNT

Frame counter Reset value: 0000'0000H

Address: ISP_MISP_BASE + 0244H		Mode : r
Bits	**Name**	**Description**
31:10	---	unused
9:0	frame_counter	Current frame count of processing
Note: In the ISP_FRAME_COUNT register the number of processed frames are displayed. For example: If a 8 is programmed into the ISP_ACQ_NR_FRAMES register, a read access to the ISP_FRAME_COUNT register during processing of the first picture shows a 7. After the entire frames are processed the ISP_OFF interrupt is generated and the ISP_FRAME_COUNT has the count zero. In case a "0" is programmed into the ISP_ACQ_NR_FRAMES register (continues mode) the ISP_FRAME_COUNT register keeps the value "0".		

Register: ISP_CT_OFFSET_R

cross-talk offset red Reset value: 0000'0000H

Address: ISP_MISP_BASE + 0248H		Mode : rw
Bits	**Name**	**Description**
31:12	---	unused
11:0	ct_offset_r	Offset red for cross talk matrix. Two's complement integer number ranging from -2048 (0x800) to 2047 (0x7FF). 0 is represented as 0x000.

Register: ISP_CT_OFFSET_G

cross-talk offset green Reset value: 0000'0000H

Address: ISP_MISP_BASE + 024CH		Mode : rw
Bits	**Name**	**Description**
31:12	---	unused
11:0	ct_offset_g	Offset green for cross talk matrix. Two's complement integer number ranging from -2048 (0x800) to 2047 (0x7FF). 0 is represented as 0x000.

Register: ISP_CT_OFFSET_B

cross-talk offset blue Reset value: 0000'0000H

Address: ISP_MISP_BASE + 0250H		Mode : rw
Bits	**Name**	**Description**
31:12	---	unused
11:0	ct_offset_b	Offset blue for cross talk matrix. Two's complement integer number ranging from -2048 (0x800) to 2047 (0x7FF). 0 is represented as 0x000.

Register: ISP_FLASH_CMD

Flash command Reset value: 0000'0000H

Address: ISP_FLASH_BASE + 0000H		Mode : w
Bits	**Name**	**Description**
31:3	---	unused
2	preflash_on	preflash on 0: no effect 1: flash delay counter is started at next trigger event No capture event is signaled to the sensor interface
1	flash_on	flash on 0: no effect 1: flash delay counter is started at next trigger event A capture event is signaled to the sensor interface
0	prelight_on	prelight on 0: prelight is switched off at next trigger event 1: prelight is switched on at next trigger event
Note: This is the command register for flash light and prelight activation. If the "rw" bits (e.g. "fl_cap_del") are re-programmed during operation, the following scheme shall be applied: prelight is active (prelight_on = 1 has been set before): Every write access to this register shall use prelight_on = 1 (to prevent undesired switch off of the prelight). prelight is off: Every write access to this register shall use prelight_on = 0 (to prevent		

Register: ISP_FLASH_CONFIG

Flash config Reset value: 0000'0000H

Address: ISP_FLASH_BASE + 0004H		Mode : rw
Bits	**Name**	**Description**
31:8	---	unused
7:4	fl_cap_del	capture delay frame number (0 to 15) to be captured after trigger event
3	fl_trig_src	trigger source for flash and prelight 0: use "vds_vsync" for trigger event (with evaluation of vs_in_edge) 1: use "fl_trig" for trigger event (positive edge)
2	fl_pol	polarity of flash related signals 0: flash_trig, prelight_trig are high active 1: flash_trig, prelight_trig are low active
1	vs_in_edge	VSYNC edge 0: use negative edge of "vds_vsync" if generating a trigger event 1: use positive edge of "vds_vsync" if generating a
0	prelight_mode	prelight mode 0: prelight is switched off at begin of flash 1: prelight is switched off at end of flash

Register: ISP_FLASH_PREDIV
Flash Counter Pre-Divider Reset value: 0000'0000H

Address: ISP_FLASH_BASE + 0008H		Mode : rw
Bits	**Name**	**Description**
31:10	---	unused
9:0	fl_pre_div	pre-divider for flush/preflash counter

Register: ISP_FLASH_DELAY

Flash Delay Reset value: 0000'0000H

Address: ISP_FLASH_BASE + 000CH		Mode : rw
Bits	**Name**	**Description**
31:18	---	unused

Flash Delay Reset value: 0000'0000H

Address: ISP_FLASH_BASE + 000CH		Mode : rw
Bits	**Name**	**Description**
17:0	fl_delay	counter value for flash/preflash delay open_delay = (fl_delay + 1) * (fl_pre_div+1) / clk_isp fl_delay = (open_delay * clk_isp) / (fl_pre_div+1) - 1
Note: Example: fl_delay = (10s * 100MHz) / (1023 + 1) – 1 = 976561		

Register: ISP_FLASH_TIME

Flash time Reset value: 0000'0000H

Address: ISP_FLASH_BASE + 0010H		Mode : rw
Bits	**Name**	**Description**
31:18	---	unused
17:0	fl_time	counter value for flash/preflash time open_time = (fl_time + 1) * (fl_pre_div+1) / clk_isp fl_time = (open_time * clk_isp) / (fl_pre_div+1) - 1
Note: Example: fl_time = (500ms * 100MHz) / (700 + 1) – 1 = 71530		

Register: ISP_FLASH_MAXP

Maximum value for flash or preflash Reset value: 0000'0000H

Address: ISP_FLASH_BASE + 0014H		Mode : rw
Bits	**Name**	**Description**
31:16	---	unused
15:0	fl_maxp	maximum period value for flash or preflash max. flash/preflash period = 214 * (fl_maxp + 1) / clk_isp fl_maxp = (max_period * clk_isp) / 214 - 1
Note: Example: fl_maxp = (10s * 100MHz) / (16384) – 1 = 61034		

Register: ISP_SH_CTRL

mechanical shutter control Reset value: 0000'0000H

Address: ISP_SHUT_BASE + 0000H		Mode : rw
Bits	**Name**	**Description**
31:5	---	unused
4	sh_open_pol	shutter_open polarity 0: shutter_open is high active 1: shutter_open is low active
3	sh_trig_en	mechanical shutter trigger edge 0: use negative edge of trigger signal 1: use positive edge of trigger signal
2	sh_trig_src	mechanical shutter trigger source 0: use "vds_vsync" for trigger event 1: use "shutter_trig" for trigger event
1	sh_rep_en	mechanical shutter repetition enable 0: shutter is opened only once 1: shutter is opened with the repetition rate of the trigger signal
0	sh_en	mechanical shutter enable 0: mechanical shutter function is disabled 1: mechanical shutter function is enabled

Register: ISP_SH_PREDIV

Mech. Shutter Counter Pre-Divider Reset value: 0000'0000H

Address: ISP_SHUT_BASE + 0004H		Mode : rw
Bits	**Name**	**Description**
31:10	---	unused
9:0	sh_pre_div	pre-divider for mechanical shutter open_delay and open_time counter

Register: ISP_SH_DELAY

Delay register Reset value: 0000'0000H

Address: ISP_SHUT_BASE + 0008H		Mode : rw
Bits	**Name**	**Description**
31:20	---	unused

Delay register Reset value: 0000'0000H

Address: ISP_SHUT_BASE + 0008H		Mode : rw
Bits	**Name**	**Description**
19:0	sh_delay	counter value for delay open_delay = (sh_delay + 1) * (fl_pre_div+1) / clk_isp sh_delay = (open_delay * clk_isp) / (sh_pre_div+1) – 1
Note: Example: sh_delay = (250us * 100MHz) / (50 + 1) – 1 = 489		

Register: ISP_SH_TIME

Time register Reset value: 0000'0000H

Address: ISP_SHUT_BASE + 000CH		Mode : rw
Bits	**Name**	**Description**
31:20	---	unused
19:0	sh_time	counter value for time open_time = (sh_time + 1) * (fl_pre_div+1) / clk_isp sh_time = (open_time * clk_isp) / (sh_pre_div+1) - 1
Note: Example: sh_time = (10s * 100MHz) / (1023 + 1) – 1 = 976561		

Register: CPROC_CTRL

Global control register Reset value: 0000'0000H

Address: ISP_CPROC_BASE + 0000H		Mode : rw
Bits	**Name**	**Description**
31:4	---	unused
3	cproc_c_out_range	Color processing chrominance pixel clipping range at output 0: CbCr_out clipping range 16..240 according to ITU-R BT.601 standard 1: full UV_out clipping range 0..255
2	cproc_y_in_range	Color processing luminance input range (offset processing) 0: Y_in range 64..940 according to ITU-R BT.601 standard; offset of 64 will be subtracted from Y_in 1: Y_in full range 0..1023; no offset will be subtracted from Y_in

Global control register Reset value: 0000'0000H

Address: ISP_CPROC_BASE + 0000H		Mode : rw
Bits	**Name**	**Description**
1	cproc_y_out_range	Color processing luminance output clipping range 0: Y_out clipping range 16..235; offset of 16 is added to Y_out according to ITU-R BT.601 standard 1: Y_out clipping range 0..255; no offset is added to Y_out
0	cproc_enable	color processing enable 0: color processing is bypassed 2 * 10 Bit input data are truncated to 2 * 8Bit output data 1: color processing is active output data are rounded to 2 * 8Bit and clipping is activ

Register: CPROC_CONTRAST

Color Processing contrast register Reset value: 0000'0080H

Address: ISP_CPROC_BASE + 0004H		Mode : rw
Bits	**Name**	**Description**
31:8	---	unused
7:0	cproc_contrast	contrast adjustment value 00H equals x 0.0 … 80H equals x 1.0 … FFH equals x 1.992

Register: CPROC_BRIGHTNESS
Color Processing brightness register Reset value: 0000'0000H

Address: ISP_CPROC_BASE + 0008H		Mode : rw
Bits	**Name**	**Description**
31:8	---	unused
7:0	cproc_brightness	brightness adjustment value 80H equals -128 … 00H equals +0 … 7FH equals +127

Register: CPROC_SATURATION

Color Processing saturation register Reset value: 0000'0080H

Address: ISP_CPROC_BASE + 000CH			Mode : rw
Bits	**Name**	**Description**	
31:8	---	unused	
7:0	cproc_saturation	saturation adjustment value 00H equals x 0.0 … 80H equals x 1.0 … FFH equals x 1.992	

Register: CPROC_HUE

Color Processing hue register Reset value: 0000'0000H

Address: ISP_CPROC_BASE + 0010H			Mode : rw
Bits	**Name**	**Description**	
31:8	---	unused	
7:0	cproc_hue	hue adjustment value 80H equals -90 deg … 00H equals 0 deg … 7FH equals +87.188 deg	

Register: MRSZ_CTRL

global control register Reset value: 0000'0000H

Address: ISP_MRSZ_BASE + 0000H			Mode : rw
Bits	**Name**	**Description**	
31:10	---	unused	
9	auto_upd	1: automatic register update at frame end enabled. 0: automatic register update at frame end disabled.	
8	cfg_upd	write 0: nothing happens write 1: update shadow registers read: always 0	

global control register Reset value: 0000'0000H

Address: ISP_MRSZ_BASE + 0000H		Mode : rw
Bits	**Name**	**Description**
7	scale_vc_up	1: vertical chrominance upscaling selected 0: vertical chrominance downscaling selected
6	scale_vy_up	1: vertical luminance upscaling selected 0: vertical luminance downscaling selected
5	scale_hc_up	1: horizontal chrominance upscaling selected 0: horizontal chrominance downscaling selected
4	scale_hy_up	1: horizontal luminance upscaling selected 0: horizontal luminance downscaling selected
3	scale_vc_enable	0: bypass vertical chrominance scaling unit 1: enable vertical chrominance scaling unit
2	scale_vy_enable	0: bypass vertical luminance scaling unit 1: enable vertical luminance scaling unit
1	scale_hc_enable	0: bypass horizontal chrominance scaling unit 1: enable horizontal chrominance scaling unit
0	scale_hy_enable	0: bypass horizontal luminance scaling unit 1: enable horizontal luminance scaling unit

Register: MRSZ_SCALE_HY
horizontal luminance scale factor register Reset value: 0000'0000H

Address: ISP_MRSZ_BASE + 0004H		Mode : rw
Bits	**Name**	**Description**
31:16	---	unused

horizontal luminance scale factor register Reset value: 0000'0000H

Address: ISP_MRSZ_BASE + 0004H		Mode : rw
Bits	**Name**	**Description**
15:0	scale_hy	This register is set to the horizontal luminance downscale factor or to the reciprocal of the horizontal luminance upscale factor

Note: The size of the output picture is calculated as follows:

upscaling: (size_in - 1) / (size_out - 1)) = scale downscaling: (size_out - 1) / (size_in - 1)) = scale,

where size_in/out is the width or height of the in/output picture. The value of the respective MRSZ_SCALE register then has to be
int(scale x 2^14) for upscaling and
int(scale x 2^14)+1 for downscaling.
For downscaling this formula has no restriction. In upscaling processes the limit is factor 5. The output is at max. 5 MegaPixel.
If a format conversion is performed, the scale factors have to be different for the luminance and the chrominance component, respectively. For example, for a format conversion from 4:2:2 to 4:2:0 the scale register value for the vertical
chrominance component should be half of the vertical luminance scale register value.

Register: MRSZ_SCALE_HCB

horizontal Cb scale factor register Reset value: 0000'0000H

Address: ISP_MRSZ_BASE + 0008H		**Mode : rw**
Bits	**Name**	**Description**
31:16	---	unused
15:0	scale_hcb	This register is set to the horizontal Cb downscale factor or to the reciprocal of the horizontal Cb upscale factor

Register: MRSZ_SCALE_HCR

horizontal Cr scale factor register Reset value: 0000'0000H

Address: ISP_MRSZ_BASE + 000CH		**Mode : rw**
Bits	**Name**	**Description**
31:16	---	unused
15:0	scale_hcr	This register is set to the horizontal Cr downscale factor or to the reciprocal of the horizontal Cr upscale factor

Register: MRSZ_SCALE_VY
vertical luminance scale factor register Reset value: 0000'0000H

Address: ISP_MRSZ_BASE + 0010H		**Mode : rw**
Bits	**Name**	**Description**
31:16	---	unused
15:0	scale_vy	This register is set to the vertical luminance downscale factor or to the reciprocal of the vertical luminance upscale factor

Register: MRSZ_SCALE_VC

vertical chrominance scale factor register Reset value: 0000'0000H

Address: ISP_MRSZ_BASE + 0014H			Mode : rw
Bits	Name	Description	
31:16	---	unused	
15:0	scale_vc	This register is set to the vertical chrominance downscale factor or to the reciprocal of the vertical	
Note: The size of the output picture is calculated as follows: (size_out - 1) / (size_in - 1)) = scale, where size_in/out is the width or heigth of the in/output picture. The values of the MRSZ_SCALE registers then have to be int(scale x 2^14)+1			

Register: MRSZ_PHASE_HY

horizontal luminance phase register Reset value: 0000'0000H

Address: ISP_MRSZ_BASE + 0018H			Mode : rw
Bits	Name	Description	
31:16	---	unused	
15:0	phase_hy	This register is set to the horizontal luminance phase	

Register: MRSZ_PHASE_HC

horizontal chrominance phase register Reset value: 0000'0000H

Address: ISP_MRSZ_BASE + 001CH			Mode : rw
Bits	Name	Description	
31:16	---	unused	
15:0	phase_hc	This register is set to the horizontal chrominance phase offset	

Register: MRSZ_PHASE_VY

vertical luminance phase register Reset value: 0000'0000H

Address: ISP_MRSZ_BASE + 0020H			Mode : rw
Bits	Name	Description	
31:16	---	unused	
15:0	phase_vy	This register is set to the vertical luminance phase	

Register: MRSZ_PHASE_VC

vertical chrominance phase register Reset value: 0000'0000H

Address: ISP_MRSZ_BASE + 0024H		Mode : rw
Bits	**Name**	**Description**
31:16	---	unused
15:0	phase_vc	This register is set to the vertical chrominance phase offset

Register: MRSZ_SCALE_LUT_ADDR

Address pointer of up-scaling look up table Reset value: 0000'0000H

Address: ISP_MRSZ_BASE + 0028H		Mode : rw
Bits	**Name**	**Description**
31:6	---	unused
5:0	scale_lut_addr	Pointer to entry of lookup table

Register: MRSZ_SCALE_LUT

Entry of up-scaling look up table Reset value: 0000'0000H

Address: ISP_MRSZ_BASE + 002CH		Mode : rw
Bits	**Name**	**Description**
31:6	---	unused
5:0	scale_lut	Entry of lookup table at position scale_lut_addr. The lookup table must be filled with appropriate values before the up- scaling functionality can be used.

Register: MRSZ_CTRL_SHD

global control shadow register Reset value: 0000'0000H

Address: ISP_MRSZ_BASE + 0030H		Mode : r
Bits	**Name**	**Description**
31:8	---	unused
7	scale_vc_up_shd	1: vertical chrominance upscaling selected 0: vertical chrominance downscaling selected
6	scale_vy_up_shd	1: vertical luminance upscaling selected 0: vertical luminance downscaling selected
5	scale_hc_up_shd	1: horizontal chrominance upscaling selected 0: horizontal chrominance downscaling selected
4	scale_hy_up_shd	1: horizontal luminance upscaling selected 0: horizontal luminance downscaling selected
3	scale_vc_enable_shd	0: bypass vertical chrominance scaling unit 1: enable vertical chrominance scaling unit

Address: ISP_MRSZ_BASE + 0030H			Mode : r
Bits	**Name**	**Description**	
2	scale_vy_enable_shd	0: bypass vertical luminance scaling unit 1: enable vertical luminance scaling unit	

global control shadow register Reset value: 0000'0000H

Address: ISP_MRSZ_BASE + 0030H			Mode : r
Bits	**Name**	**Description**	
1	scale_hc_enable_shd	0: bypass horizontal chrominance scaling unit 1: enable horizontal chrominance scaling unit	
0	scale_hy_enable_shd	0: bypass horizontal luminance scaling unit 1: enable horizontal luminance scaling unit	

Register: MRSZ_SCALE_HY_SHD
horizontal luminance scale factor shadow register Reset value: 0000'0000H

Address: ISP_MRSZ_BASE + 0034H			Mode : r
Bits	**Name**	**Description**	
31:16	---	unused	
15:0	scale_hy_shd	This register is set to the horizontal luminance downscale factor or to the reciprocal of the horizontal	

Register: MRSZ_SCALE_HCB_SHD

horizontal Cb scale factor shadow register Reset value: 0000'0000H

Address: ISP_MRSZ_BASE + 0038H			Mode : r
Bits	**Name**	**Description**	
31:16	---	unused	
15:0	scale_hcb_shd	This register is set to the horizontal Cb downscale factor or to the reciprocal of the horizontal Cb upscale	

Register: MRSZ_SCALE_HCR_SHD
horizontal Cr scale factor shadow register Reset value: 0000'0000H

Address: ISP_MRSZ_BASE + 003CH			Mode : r
Bits	**Name**	**Description**	
31:16	---	unused	
15:0	scale_hcr_shd	This register is set to the horizontal Cr downscale factor or to the reciprocal of the horizontal Cr upscale	

Register: MRSZ_SCALE_VY_SHD

vertical luminance scale factor shadow register Reset value: 0000'0000H

Address: ISP_MRSZ_BASE + 0040H		Mode : r
Bits	**Name**	**Description**
31:16	---	unused
15:0	scale_vy_shd	This register is set to the vertical luminance downscale factor or to the reciprocal of the vertical

Register: MRSZ_SCALE_VC_SHD

vertical chrominance scale factor shadow register Reset value: 0000'0000H

Address: ISP_MRSZ_BASE + 0044H		Mode : r
Bits	**Name**	**Description**
31:16	---	unused
15:0	scale_vc_shd	This register is set to the vertical chrominance downscale factor or to the reciprocal of the vertical

Register: MRSZ_PHASE_HY_SHD

horizontal luminance phase shadow register Reset value: 0000'0000H

Address: ISP_MRSZ_BASE + 0048H		Mode : r
Bits	**Name**	**Description**
31:16	---	unused
15:0	phase_hy_shd	This register is set to the horizontal luminance phase

Register: MRSZ_PHASE_HC_SHD

horizontal chrominance phase shadow register Reset value: 0000'0000H

Address: ISP_MRSZ_BASE + 004CH		Mode : r
Bits	**Name**	**Description**
31:16	---	unused
15:0	phase_hc_shd	This register is set to the horizontal chrominance phase offset

Register: MRSZ_PHASE_VY_SHD

vertical luminance phase shadow register Reset value: 0000'0000H

Address: ISP_MRSZ_BASE + 0050H			Mode : r
Bits	**Name**	**Description**	
31:16	---	unused	
15:0	phase_vy_shd	This register is set to the vertical luminance phase offset	

Register: MRSZ_PHASE_VC_SHD

vertical chrominance phase shadow register Reset value: 0000'0000H

Address: ISP_MRSZ_BASE + 0054H			Mode : r
Bits	**Name**	**Description**	
31:16	---	unused	
15:0	phase_vc_shd	This register is set to the vertical chrominance phase offset	

Register: SRSZ_CTRL

global control register Reset value: 0000'0000H

Address: ISP_SRSZ_BASE + 0000H			Mode : rw
Bits	**Name**	**Description**	
31:10	---	unused	
9	auto_upd	1: automatic register update at frame end enabled. 0: automatic register update at frame end disabled.	
8	cfg_upd	write 0: nothing happens write 1: update shadow registers read: always 0	
7	scale_vc_up	1: vertical chrominance upscaling selected 0: vertical chrominance downscaling selected	
6	scale_vy_up	1: vertical luminance upscaling selected 0: vertical luminance downscaling selected	
5	scale_hc_up	1: horizontal chrominance upscaling selected 0: horizontal chrominance downscaling selected	
4	scale_hy_up	1: horizontal luminance upscaling selected 0: horizontal luminance downscaling selected	

global control register Reset value: 0000'0000H

Address: ISP_SRSZ_BASE + 0000H		Mode : rw
Bits	**Name**	**Description**
3	scale_vc_enable	0: bypass vertical chrominance scaling unit 1: enable vertical chrominance scaling unit
2	scale_vy_enable	0: bypass vertical luminance scaling unit 1: enable vertical luminance scaling unit
1	scale_hc_enable	0: bypass horizontal chrominance scaling unit 1: enable horizontal chrominance scaling unit
0	scale_hy_enable	0: bypass horizontal luminance scaling unit 1: enable horizontal luminance scaling unit

Register: SRSZ_SCALE_HY
horizontal luminance scale factor register Reset value: 0000'0000H

Address: ISP_SRSZ_BASE + 0004H		Mode : rw
Bits	**Name**	**Description**
31:16	---	unused
15:0	scale_hy	This register is set to the horizontal luminance downscale factor or to the reciprocal of the horizontal luminance upscale factor
Note: The size of the output picture is calculated as follows: upscaling: (size_in - 1) / (size_out - 1)) = scale downscaling: (size_out - 1) / (size_in - 1)) = scale, where size_in/out is the width or height of the in/output picture. The value of the respective SRSZ_SCALE register then has to be int(scale x 2^14) for upscaling and int(scale x 2^14)+1 for downscaling. For downscaling this formula has no restriction. In upscaling processes the limit is factor 5. If a format conversion is performed, the scale factors have to be different for the luminance and the chrominance component, respectively. For example, for a format conversion from 4:2:2 to 4:2:0 the scale register value for the vertical chrominance component should be half of the vertical luminance scale register value.		

Register: SRSZ_SCALE_HCB

horizontal chrominance scale factor register Reset value: 0000'0000H

Address: ISP_SRSZ_BASE + 0008H			Mode : rw
Bits	Name	Description	
31:16	---	unused	
15:0	scale_hcb	This register is set to the horizontal Cb downscale factor or to the reciprocal of the horizontal Cb upscale factor	

Register: SRSZ_SCALE_HCR
horizontal chrominance scale factor register Reset value: 0000'0000H

Address: ISP_SRSZ_BASE + 000CH			Mode : rw
Bits	Name	Description	
31:16	---	unused	
15:0	scale_hcr	This register is set to the horizontal Cr downscale factor or to the reciprocal of the horizontal Cr upscale factor	

Register: SRSZ_SCALE_VY

vertical luminance scale factor register Reset value: 0000'0000H

Address: ISP_SRSZ_BASE + 0010H			Mode : rw
Bits	Name	Description	
31:16	---	unused	
15:0	scale_vy	This register is set to the vertical luminance downscale factor or to the reciprocal of the vertical luminance upscale factor	

Register: SRSZ_SCALE_VC
vertical chrominance scale factor register Reset value: 0000'0000H

Address: ISP_SRSZ_BASE + 0014H			Mode : rw
Bits	Name	Description	
31:16	---	unused	
15:0	scale_vc	This register is set to the vertical chrominance downscale factor or to the reciprocal of the vertical chrominance upscale factor	

Register: SRSZ_PHASE_HY

horizontal luminance phase register Reset value: 0000'0000H

Address: ISP_SRSZ_BASE + 0018H			Mode : rw
Bits	**Name**	**Description**	
31:16	---	unused	
15:0	phase_hy	This register is set to the horizontal luminance phase offset	

Register: SRSZ_PHASE_HC

horizontal chrominance phase register Reset value: 0000'0000H

Address: ISP_SRSZ_BASE + 001CH			Mode : rw
Bits	**Name**	**Description**	
31:16	---	unused	
15:0	phase_hc	This register is set to the horizontal chrominance phase offset	

Register: SRSZ_PHASE_VY

vertical luminance phase register Reset value: 0000'0000H

Address: ISP_SRSZ_BASE + 0020H			Mode : rw
Bits	**Name**	**Description**	
31:16	---	unused	
15:0	phase_vy	This register is set to the vertical luminance phase offset	

Register: SRSZ_PHASE_VC

vertical chrominance phase register Reset value: 0000'0000H

Address: ISP_SRSZ_BASE + 0024H			Mode : rw
Bits	**Name**	**Description**	
31:16	---	unused	
15:0	phase_vc	This register is set to the vertical chrominance phase offset	

Register: SRSZ_SCALE_LUT_ADDR

Address pointer of up-scaling look up table Reset value: 0000'0000H

Address: ISP_SRSZ_BASE + 0028H		Mode : rw
Bits	**Name**	**Description**
31:6	---	unused
5:0	scale_lut_addr	Pointer to entry of lookup table

Register: SRSZ_SCALE_LUT

Entry of up-scaling look up table Reset value: 0000'0000H

Address: ISP_SRSZ_BASE + 002CH		Mode : rw
Bits	**Name**	**Description**
31:6	---	unused
5:0	scale_lut	Entry of lookup table at position scale_lut_addr. The lookup table must be filled with appropriate values before the up- scaling functionality can be

Register: SRSZ_CTRL_SHD

global control shadow register Reset value: 0000'0000H

Address: ISP_SRSZ_BASE + 0030H		Mode : r
Bits	**Name**	**Description**
31:8	---	unused
7	scale_vc_up_shd	1: vertical chrominance upscaling selected 0: vertical chrominance downscaling selected
6	scale_vy_up_shd	1: vertical luminance upscaling selected 0: vertical luminance downscaling selected
5	scale_hc_up_shd	1: horizontal chrominance upscaling selected 0: horizontal chrominance downscaling selected
4	scale_hy_up_shd	1: horizontal luminance upscaling selected 0: horizontal luminance downscaling selected
3	scale_vc_enable_shd	0: bypass vertical chrominance scaling unit 1: enable vertical chrominance scaling unit
2	scale_vy_enable_shd	0: bypass vertical luminance scaling unit 1: enable vertical luminance scaling unit

Address: ISP_SRSZ_BASE + 0030H		Mode : r
Bits	**Name**	**Description**
1	scale_hc_enable_shd	0: bypass horizontal chrominance scaling unit 1: enable horizontal chrominance scaling unit
0	scale_hy_enable_shd	0: bypass horizontal luminance scaling unit 1: enable horizontal luminance scaling unit

Register: SRSZ_SCALE_HY_SHD
horizontal luminance scale factor shadow register Reset value: 0000'0000H

Address: ISP_SRSZ_BASE + 0034H		Mode : r
Bits	**Name**	**Description**
31:16	---	unused
15:0	scale_hy_shd	This register is set to the horizontal luminance downscale factor or to the reciprocal of the horizontal luminance upscale factor

Register: SRSZ_SCALE_HCB_SHD

horizontal Cb scale factor shadow register Reset value: 0000'0000H

Address: ISP_SRSZ_BASE + 0038H		Mode : r
Bits	**Name**	**Description**
31:16	---	unused
15:0	scale_hcb_shd	This register is set to the horizontal Cb downscale factor or to the reciprocal of the horizontal Cb upscale factor

Register: SRSZ_SCALE_HCR_SHD
horizontal Cr scale factor shadow register Reset value: 0000'0000H

Address: ISP_SRSZ_BASE + 003CH		Mode : r
Bits	**Name**	**Description**
31:16	---	unused
15:0	scale_hcr_shd	This register is set to the horizontal r downscale factor or to the reciprocal of the horizontal r upscale factor

Register: SRSZ_SCALE_VY_SHD

vertical luminance scale factor shadow register Reset value: 0000'0000H

Address: ISP_SRSZ_BASE + 0040H			Mode : r
Bits	**Name**	**Description**	
31:16	---	unused	
15:0	scale_vy_shd	This register is set to the vertical luminance downscale factor or to the reciprocal of the vertical luminance upscale factor	

Register: SRSZ_SCALE_VC_SHD
vertical chrominance scale factor shadow register Reset value: 0000'0000H

Address: ISP_SRSZ_BASE + 0044H			Mode : r
Bits	**Name**	**Description**	
31:16	---	unused	
15:0	scale_vc_shd	This register is set to the vertical chrominance downscale factor or to the reciprocal of the vertical chrominance upscale factor	

Register: SRSZ_PHASE_HY_SHD

horizontal luminance phase shadow register Reset value: 0000'0000H

Address: ISP_SRSZ_BASE + 0048H			Mode : r
Bits	**Name**	**Description**	
31:16	---	unused	
15:0	phase_hy_shd	This register is set to the horizontal luminance phase offset	

Register: SRSZ_PHASE_HC_SHD

horizontal chrominance phase shadow register Reset value: 0000'0000H

Address: ISP_SRSZ_BASE + 004CH			Mode : r
Bits	**Name**	**Description**	
31:16	---	unused	
15:0	phase_hc_shd	This register is set to the horizontal chrominance phase offset	

Register: SRSZ_PHASE_VY_SHD

vertical luminance phase shadow register Reset value: 0000'0000H

Address: ISP_SRSZ_BASE + 0050H		Mode : r
Bits	**Name**	**Description**
31:16	---	unused
15:0	phase_vy_shd	This register is set to the vertical luminance phase offset.

Register: SRSZ_PHASE_VC_SHD

vertical chrominance phase shadow register Reset value: 0000'0000H

Address: ISP_SRSZ_BASE + 0054H		Mode : r
Bits	**Name**	**Description**
31:16	---	unused
15:0	phase_vc_shd	This register is set to the vertical chrominance phase offset.

Register: MI_CTRL

Global control register Reset value: 0000'0000H

Address: ISP_MI_BASE + 0000H		Mode : rw
Bits	**Name**	**Description**
31	---	unused
30:28	sp_output_format	Selects output format of self picture. For possible restrictions see sub-chapter "Picture Orientation" in chapter "Self Path Output Programming". 111: reserved 110: RGB 888 101: RGB 666 100: RGB 565 011: YCbCr 4:4:4 010: YCbCr 4:2:2 001: YCbCr 4:2:0 000: YCbCr 4:0:0 Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path. for RGB output format the SP input format must be YCbCr 4:2:2

Address: ISP_MI_BASE + 0000H		Mode : rw
Bits	**Name**	**Description**
27:26	sp_input_format	Selects input format of self picture. For possible restrictions see sub-chapter "Picture Orientation" in chapter "Self Path Output Programming". 11: YCbCr 4:4:4 10: YCbCr 4:2:2 01: YCbCr 4:2:0 00: YCbCr 4:0:0 Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path.
25:24	sp_write_format	Defines how YCbCr self picture data is written to memory. Must be set to 00 if RGB conversion is active. Note that with RGB conversion active the output format is always interleaved. 00: planar 01: semi planar, for YCbCr 4:2:x 10: interleaved (combined), for YCbCr 4:2:2 only 11: reserved Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path.
23:22	mp_write_format	Defines how YCbCr main picture data is written to memory. Ignored if JPEG data is chosen. In YCbCr mode the following meaning is applicable 00: planar 01: semi planar, for YCbCr 4:2:x 10: interleaved (combined), for YCbCr 4:2:2 only 11: reserved In RAW data mode the following meaning is applicable 00: RAW 8 bit 01: reserved 10: RAW 12 bit 11: reserved Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the main path.

Address: ISP_MI_BASE + 0000H		Mode : rw
Bits	**Name**	**Description**
21	init_offset_en	Enables updating of the offset counters shadow registers for main and self picture to the programmed register init values. MI_MP/SP_Y/CB/CR_OFFS_CNT_INIT -> MI_MP/SP_Y/CB/CR_OFFS_CNT_SHD The update will be executed either when a forced software update occurs (in register MI_INIT bit cfg_upd = 1) or when an automatic config update signal arrives at the MI input port. The latter is split into main and self picture. So only the corresponding main/self shadow registers are affected. After a picture skip has been performed init_offset_en selects between skip restart and skip init mode (see bit skip in register MI_INIT).
20	init_base_en	Enables updating of the base address and buffer size shadow registers for main and self picture to the programmed register init values. MI_MP/SP_Y/CB/CR_BASE_AD_INIT -> MI_MP/SP_Y/CB/CR_BASE_AD_SHD MI_MP/SP_Y/CB/CR_SIZE_INIT -> MI_MP/SP_Y/CB/CR_SIZE_SHD The update will be executed either when a forced software update occurs (in register MI_INIT bit cfg_upd = 1) or when an automatic config update signal arrives at the MI input port. The latter is split into main and self picture. So only the corresponding main/self shadow registers are affected.
19:18	burst_len_chrom	Burst length for Cb or Cr data affecting write port. 00: 4-beat bursts 01: 8-beat bursts 10: 16-beat bursts 11: reserved Ignored if 8- or 16-beat bursts are not supported. If rotation is active, then only 4-beat bursts will be generated in self path, regardless of the setting here. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the main and self path.
17:16	burst_len_lum	Burst length for Y, JPEG, or raw data affecting write port. 00: 4-beat bursts 01: 8-beat bursts 10: 16-beat bursts 11: reserved Ignored if 8- or 16-beat bursts are not supported. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the main and self path.

Address: ISP_MI_BASE + 0000H		Mode : rw
Bits	**Name**	**Description**
15	last_pixel_sig_en	enables the last pixel signalization 1: enabled 0: disabled
14	sp_auto_update	automatic update of configuration registers for self path at frame end. 1: enabled 0: disabled
13	mp_auto_update	automatic update of configuration registers for main path at frame end. 1: enabled 0: disabled
12	sp_pingpong_enable	pingpong mode of configuration registers for self path at frame end. 1: enabled 0: disabled
11	mp_pingpong_enable	pingpong mode of configuration registers for main path at frame end. 1: enabled 0: disabled
10	422noncosited	Enables self path YCbCr422non-co-sited -> YCbCr444 interpolation 1: YCbCr422 data are non_co-sited (Cb and Cr samples are centered between Y samples) so modified interpolation is activated 0: YCbCr422 data are co-sited (Y0 Cb0 and Cr0 are sampled at the same position) Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path.
9	cbcr_full_range	Enables CbCr full range for self path YCbCr -> RGB conversion 1: CbCr have full range (0..255) 0: CbCr have compressed range range (16..240) Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path.
8	y_full_range	Enables Y full range for self path YCbCr -> RGB conversion 1: Y has full range (0..255) 0: Y has compressed range (16..235) Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path.

Address: ISP_MI_BASE + 0000H		Mode : rw
Bits	**Name**	**Description**
7	byte_swap	Enables change of byte order of the 32 bit output word at write port 1: byte order is mirrored but the bit order within one byte doesn“t change 0: no byte mirroring Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the main and self path.
6	rot	Rotation 90 degree counter clockwise of self picture, only in RGB mode. For picture orientation and operation modes see sub-chapter "Picture Orientation" in chapter "Self Path Output Programming". For RGB 565 format the line length must be a multiple of 2. There are no restrictions for RGB 888/666. 1: enabled 0: disabled Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path. In rotation mode only 4-beat bursts are supported for self- path.
5	v_flip	Vertical flipping of self picture. For picture orientation and operation modes see sub-chapter "Picture Orientation" in chapter "Self Path Output Programming". For Y component the line length in 4:2:x planar mode must be a multiple of 8, for all other component modes a multiple of 4 and for RGB 565 a multiple of 2. There are no restrictions for RGB 888/666. 1: enabled 0: disabled Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path.
4	h_flip	Horizontal flipping of self picture. For picture orientation and operation modes see sub-chapter "Picture Orientation" in chapter "Self Path Output Programming". For Y component the line length in 4:2:x planar mode must be a multiple of 8, for all other component modes a multiple of 4 and for RGB 565 a multiple of 2. There are no restrictions for RGB 888/666. 1: enabled 0: disabled Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path.

Address: ISP_MI_BASE + 0000H		Mode : rw
Bits	**Name**	**Description**
3:0	path_enable	Enables data pathes of MI according to the following table: 0000: disabled, no data is transferred 0001: YUV data output, mainpath only (mp_enable only) 0010: self-path only, output data format depending on other settings (sp_enable only) 0011: YUV data output in mainpath and self-path image data active 0100: JPEG data output, mainpath only (jpeg_enable only) 0101: not allowed 0110: JPEG data output in mainpath and self-path image data active 0111: not allowed 1000: RAW data output, mainpath only (raw_enable only) 1001: defect pixel data on self-path, image data on mainpath 1010: defect pixel data on mainpath, image data on self-path 1011: not allowed 1100: defect pixel data on self-path, JPEG data on mainpath 1101: defect pixel data on mainpath only 1110: defect pixel data on self-path only 1111: defect pixel data on self-path, RAW data on mainpath Programmed value becomes effective (visible in shadow register) after a soft reset, a forced software update or an automatic config update. Affects MI_IN and MI_OUT module

Register: MI_INIT

Control register for address init and skip function Reset value: 0000'0000H

Address: ISP_MI_BASE + 0004H		Mode : w
Bits	**Name**	**Description**
31:5	---	unused
4	mi_cfg_upd	Forced configuration update. Leads to an immediate update of the shadow registers. Depending on the two init enable bits in the MI_CTRL register (init_offset_en and init_base_en) the offset counter, base address and buffer size shadow registers
3	---	unused

Control register for address init and skip function Reset value: 0000'0000H

Address: ISP_MI_BASE + 0004H		Mode : w
Bits	**Name**	**Description**
2	mi_skip	Skip of current or next starting main picture: Aborts writing of main picture image data of the current frame to RAM (after the current burst transmission has been completed). Further main picture data up to the end of the current frame are discarded. No further makroblock line interrupt (mblk_line), no wrap around interrupt for main picture (wrap_mp_y/cb/cr) and no fill level interrupt (fill_mp_y) are generated. Skip does not affect the generation of the main path frame end interrupt (mp_frame_end). Skip does not affect the processing of self picture and its corresponding interrupts namely the self path frame end interrupt (sp_frame_end). The byte counter (register MI_BYTE_CNT) is not affected. It produces the correct number of JPEG or RAW data bytes at the end of the current (skipped) frame. After a skip has been performed the offset counter for the main picture at the start of the following frame are set depending on the bit init_offset_en in register MI_CTRL: Skip restart mode (init_offset_en = 0) The offset counters of the main picture are restarted at the old start values of the previous skipped frame. Skip init mode (init_offset_en = 1) The offset counters of the main picture are initialized with the register contents of the offset counter init registers without any additional forced software update or automatic config update.
1:0	---	unused

Register: MI_MP_Y_BASE_AD_INIT

Base address for main picture Y component, JPEG or raw data Reset value: 0000'0000H

Address: ISP_MI_BASE + 0008H		Mode : rw
Bits	**Name**	**Description**
31:3	mp_y_base_ad_init	Base address of main picture Y component ring buffer, JPEG ring buffer or raw data ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update.
2:0	---	unused

Note: This register protects from non-aligned access. The bits 0 to 2 are hard wired to "000". As a consequence any byte address that is written to the register will automatically be re-mapped to the next lower 64 bit aligned address: write(MI_MP_Y_BASE_AD_INIT, address_value) is equivalent to write(MI_Y_BASE_AD_INIT, address_value & 0xFFFFFFF8). Anyhow, in order to avoid confusion it is NOT recommended to use non-aligned address values for access. It is also NOT recommended to actively consider the register slice for register access in order to avoid unneccessary mask and shift operations. In addition, if ISP provides AXI interfaces the programmed base address shall be burst aligned with respect to the burst length configured in MI_CTRL . Set control bit init_base_en before updating so that a forced or automatic update can take

Register: MI_MP_Y_SIZE_INIT

Size of main picture Y component, JPEG or raw data Reset value: 0000'0000H

Address: ISP_MI_BASE + 000CH		**Mode : rw**
Bits	**Name**	**Description**
31:30	---	unused
28:3	mp_y_size_init	Size of main picture Y component ring buffer, JPEG ring buffer or raw data ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update.
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details. Set control bit init_base_en before updating so that a forced or automatic update can take effect.		

Register: MI_MP_Y_OFFS_CNT_INIT

Offset counter init value for main picture Y, JPEG or raw data Reset value: 0000'0000H

Address: ISP_MI_BASE + 0010H		**Mode : rw**
Bits	**Name**	**Description**
31:30	---	unused
28:3	mp_y_offs_cnt_init	Offset counter init value of main picture Y component ring buffer, JPEG ring buffer or raw data ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update.
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details. Set control bit init_base_en before updating so that a forced or automatic update can take effect. Check exceptional handling in skip modes.		

Register: MI_MP_Y_OFFS_CNT_START

Offset counter start value for main picture Y, JPEG or raw data Reset value: 0000'0000H

Address: ISP_MI_BASE + 0014H		**Mode : r**
Bits	**Name**	**Description**
31:30	---	unused
28:3	mp_y_offs_cnt_start	Offset counter value which points to the start address of the previously processed picture (main picture Y component, JPEG or raw data). Updated at frame end. Note: A soft reset resets the contents to the reset
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.		

Register: MI_MP_Y_IRQ_OFFS_INIT

Fill level interrupt offset value for main picture Y, JPEG or raw data Reset value: 0000'0000H

Address: ISP_MI_BASE + 0018H		**Mode : rw**
Bits	**Name**	**Description**
31:30	---	unused

Address: ISP_MI_BASE + 0018H		Mode : rw
Bits	**Name**	**Description**
28:3	mp_y_irq_offs_init	Reaching this programmed value by the current offset counter for addressing main picture Y component, JPEG or raw data leads to generation of fill level interrupt fill_mp_y. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update.
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.		

Register: MI_MP_CB_BASE_AD_INIT

Base address for main picture Cb component ring buffer Reset value: 0000'0000H

Address: ISP_MI_BASE + 001CH		Mode : rw
Bits	**Name**	**Description**
31:3	mp_cb_base_ad_init	Base address of main picture Cb component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details. Refer also to MI_MP_Y_BASE_AD_INIT with respect to the burst alignment restriction for AXI.		

Register: MI_MP_CB_SIZE_INIT

Size of main picture Cb component ring buffer Reset value: 0000'0000H

Address: ISP_MI_BASE + 0020H		Mode : rw
Bits	**Name**	**Description**
31:28	---	unused

Size of main picture Cb component ring buffer Reset value: 0000'0000H

Address: ISP_MI_BASE + 0020H		Mode : rw
Bits	**Name**	**Description**
27:3	mp_cb_size_init	Size of main picture Cb component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect.
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.		

Register: MI_MP_CB_OFFS_CNT_INIT

Offset counter init value for main picture Cb component ring buffer Reset value: 0000'0000H

Address: ISP_MI_BASE + 0024H		Mode : rw
Bits	**Name**	**Description**
31:28	---	unused
27:3	mp_cb_offs_cnt_init	Offset counter init value of main picture Cb component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. Check exceptional handling in skip modes.
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.		

Register: MI_MP_CB_OFFS_CNT_START

Offset counter start value for main picture Cb component ring buffer Reset value: 0000'0000H

Address: ISP_MI_BASE + 0028H		Mode : r
Bits	**Name**	**Description**
31:28	---	unused

Offset counter start value for main picture Cb component ring buffer Reset value: 0000'0000H

Address: ISP_MI_BASE + 0028H		Mode : r
Bits	**Name**	**Description**
27:3	mp_cb_offs_cnt_start	Offset counter value which points to the start address of the previously processed picture (main picture Cb component). Updated at frame end.
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.		

Register: MI_MP_CR_BASE_AD_INIT
Base address for main picture Cr component ring buffer Reset value: 0000'0000H

Address: ISP_MI_BASE + 002CH		Mode : rw
Bits	**Name**	**Description**
31:3	mp_cr_base_ad_init	Base address of main picture Cr component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect.
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details. Refer also to MI_MP_Y_BASE_AD_INIT with respect to the burst alignment restriction for AXI.		

Register: MI_MP_CR_SIZE_INIT

Size of main picture Cr component ring buffer Reset value: 0000'0000H

Address: ISP_MI_BASE + 0030H		Mode : rw
Bits	**Name**	**Description**
31:28	---	unused
27:3	mp_cr_size_init	Size of main picture Cr component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect.

Size of main picture Cr component ring buffer Reset value: 0000'0000H

Address: ISP_MI_BASE + 0030H		Mode : rw
Bits	**Name**	**Description**
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.		

Register: MI_MP_CR_OFFS_CNT_INIT

Offset counter init value for main picture Cr component ring buffer Reset value: 0000'0000H

Address: ISP_MI_BASE + 0034H		Mode : rw
Bits	**Name**	**Description**
31:28	---	unused
27:3	mp_cr_offs_cnt_init	Offset counter init value of main picture Cr component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. Check exceptional handling in skip modes.
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.		

Register: MI_MP_CR_OFFS_CNT_START

Offset counter start value for main picture Cr component ring buffer Reset value: 0000'0000H

Address: ISP_MI_BASE + 0038H		Mode : r
Bits	**Name**	**Description**
31:28	---	unused
27:3	mp_cr_offs_cnt_start	Offset counter value which points to the start address of the previously processed picture (main picture Cr component). Updated at frame end. Note: Soft reset will reset the contents to reset value.

Offset counter start value for main picture Cr component ring buffer Reset value: 0000'0000H

Address: ISP_MI_BASE + 0038H		Mode : r
Bits	**Name**	**Description**
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.		

Register: MI_SP_Y_BASE_AD_INIT

Base address for self picture Y component ring buffer Reset value: 0000'0000H

Address: ISP_MI_BASE + 003CH		Mode : rw
Bits	**Name**	**Description**
31:3	sp_y_base_ad_init	Base address of self picture Y component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details. Refer also to MI_MP_Y_BASE_AD_INIT with respect to the burst alignment restriction for AXI.		

Register: MI_SP_Y_SIZE_INIT

Size of self picture Y component ring buffer Reset value: 0000'0000H

Address: ISP_MI_BASE + 0040H		Mode : rw
Bits	**Name**	**Description**
31:29	---	unused
28:3	sp_y_size_init	Size of self picture Y component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect.

Size of self picture Y component ring buffer Reset value: 0000'0000H

Address: ISP_MI_BASE + 0040H		Mode : rw
Bits	**Name**	**Description**
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.		

Register: MI_SP_Y_OFFS_CNT_INIT

Offset counter init value for self picture Y component ring buffer Reset value: 0000'0000H

Address: ISP_MI_BASE + 0044H		Mode : rw
Bits	**Name**	**Description**
31:30	---	unused
28:3	sp_y_offs_cnt_init	Offset counter init value of self picture Y component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect.
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.		

Register: MI_SP_Y_OFFS_CNT_START

Offset counter start value for self picture Y component ring buffer Reset value: 0000'0000H

Address: ISP_MI_BASE + 0048H		Mode : r
Bits	**Name**	**Description**
31:30	---	unused
28:3	sp_y_offs_cnt_start	Offset counter value which points to the start address of the previously processed picture (self picture Y component). Updated at frame end. Note: Soft reset will reset the contents to reset value.

Address: ISP_MI_BASE + 0048H		Mode : r
Bits	**Name**	**Description**
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.		

Register: MI_SP_Y_LLENGTH

Line length of self picture Y component Reset value: 0000'0000H

Address: ISP_MI_BASE + 004CH		Mode : rw
Bits	**Name**	**Description**
31:15	---	unused
14:0	sp_y_llength	Line length of self picture Y component or RGB picture in pixel, also known as line stride. If no line stride is used, line length must match image width. For Y component the line length in 4:2:x planar mode must be a multiple of 8, for all other component modes a multiple of 4 and for RGB 565 a multiple of 2. There are no restrictions for RGB 888/666. In planar mode the line length of the Cb and Cr component is assumed according to the YCbCr format, i.e. half for 4:2:x and the same size for 4:4:4. In semi planar 4:2:x mode the line length of the Cb and Cr component is assumed the same size. Note: Line length always refers to the line length of the output image. This is particularly important when rotating. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path.

Register: MI_SP_CB_BASE_AD_INIT

Base address for self picture Cb component ring buffer Reset value: 0000'0000H

Address: ISP_MI_BASE + 0050H		Mode : rw
Bits	**Name**	**Description**
31:3	sp_cb_base_ad_init	Base address of self picture Cb component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect.
2:0	---	unused

Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details. Refer also to MI_MP_Y_BASE_AD_INIT with respect to the burst alignment restriction for AXI.

Register: MI_SP_CB_SIZE_INIT

Size of self picture Cb component ring buffer Reset value: 0000'0000H

Address: ISP_MI_BASE + 0054H		**Mode : rw**
Bits	**Name**	**Description**
31:28	---	unused
27:3	sp_cb_size_init	Size of self picture Cb component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect.
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.		

Register: MI_SP_CB_OFFS_CNT_INIT

Offset counter init value for self picture Cb component ring buffer Reset value: 0000'0000H

Address: ISP_MI_BASE + 0058H		**Mode : rw**
Bits	**Name**	**Description**
31:28	---	unused
27:3	sp_cb_offs_cnt_init	Offset counter init value of self picture Cb component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect.
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.		

Register: MI_SP_CB_OFFS_CNT_START

Offset counter start value for self picture Cb component ring buffer Reset value: 0000'0000H

Address: ISP_MI_BASE + 005CH	**Mode : r**

Bits	Name	Description
31:28	---	unused
27:3	sp_cb_offs_cnt_start	Offset counter value which points to the start address of the previously processed picture (self picture Cb component). Updated at frame end. Note: Soft reset will reset the contents to reset value.
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.		

Register: MI_SP_CR_BASE_AD_INIT

Base address for self picture Cr component ring buffer Reset value: 0000'0000H

Address: ISP_MI_BASE + 0060H		Mode : rw
Bits	**Name**	**Description**
31:3	sp_cr_base_ad_init	Base address of self picture Cr component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect.
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details. Refer also to MI_MP_Y_BASE_AD_INIT with respect to the burst alignment restriction for AXI.		

Register: MI_SP_CR_SIZE_INIT

Size of self picture Cr component ring buffer Reset value: 0000'0000H

Address: ISP_MI_BASE + 0064H		Mode : rw
Bits	**Name**	**Description**
31:28	---	unused
27:3	sp_cr_size_init	Size of self picture Cr component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect.
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.		

Register: MI_SP_CR_OFFS_CNT_INIT

Offset counter init value for self picture Cr component ring buffer Reset value: 0000'0000H

Address: ISP_MI_BASE + 0068H		Mode : rw
Bits	**Name**	**Description**
31:28	---	unused

Offset counter init value for self picture Cr component ring buffer Reset value: 0000'0000H

Address: ISP_MI_BASE + 0068H		Mode : rw
Bits	**Name**	**Description**
27:3	sp_cr_offs_cnt_init	Offset counter init value of self picture Cr component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect.
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.		

Register: MI_SP_CR_OFFS_CNT_START

Offset counter start value for self picture Cr component ring buffer Reset value: 0000'0000H

Address: ISP_MI_BASE + 006CH		Mode : r
Bits	**Name**	**Description**
31:28	---	unused
27:3	sp_cr_offs_cnt_start	Offset counter value which points to the start address of the previously processed picture (self picture Cr component).
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.		

Register: MI_BYTE_CNT
Counter value of JPEG or RAW data bytes Reset value: 0000'0000H

Address: ISP_MI_BASE + 0070H		Mode : r
Bits	**Name**	**Description**
31:28	---	unused

27:0	byte_cnt	Counter value specifies the number of JPEG or RAW data bytes of the last transmitted frame. Updated at frame end. A soft reset will set the byte counter to zero.

Register: MI_CTRL_SHD

global control internal shadow register Reset value: 0000'0000H

Address: ISP_MI_BASE + 0074H		**Mode : r**
Bits	**Name**	**Description**
31:20	---	unused
19:16	path_enable_out	path_enable shadow register for module MI_OUT (former raw_enable_out, jpeg_enable_out, sp_enable_out, mp_enable_out)
15:4	---	unused
3:0	path_enable_in	path_enable shadow register for module MI_IN (former raw_enable_in, jpeg_enable_in, sp_enable_in, mp_enable_in)

Register: MI_MP_Y_BASE_AD_SHD

Base address shadow register for main picture Y component, JPEG or raw data ring buffer Reset value: 0000'0000H

Address: ISP_MI_BASE + 0078H		**Mode : r**
Bits	**Name**	**Description**
31:3	mp_y_base_ad	Base address of main picture Y component ring buffer, JPEG ring buffer or raw data ring buffer.
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.		

Register: MI_MP_Y_SIZE_SHD

Size shadow register of main picture Y component, JPEG or raw data Reset value: 0000'0000H

Address: ISP_MI_BASE + 007CH		**Mode : r**
Bits	**Name**	**Description**
31:28	---	unused
27:3	mp_y_size	Size of main picture Y component ring buffer, JPEG ring buffer or raw data ring buffer.

Size shadow register of main picture Y component, JPEG or raw data **Reset value: 0000'0000H**

Address: ISP_MI_BASE + 007CH		Mode : r
Bits	**Name**	**Description**
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.		

Register: MI_MP_Y_OFFS_CNT_SHD

Current offset counter of main picture Y component, JPEG or raw data ring buffer **Reset value: 0000'0000H**

Address: ISP_MI_BASE + 0080H		Mode : r
Bits	**Name**	**Description**
31:30	---	unused
28:3	mp_y_offs_cnt	Current offset counter of main picture Y component, JPEG or raw data ring buffer for address generation Note: Soft reset will reset the contents to reset value.
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.		

Register: MI_MP_Y_IRQ_OFFS_SHD

Shadow register of fill level interrupt offset value for main picture Y component, JPEG or raw data **Reset value: 0000'0000H**

Address: ISP_MI_BASE + 0084H		Mode : r
Bits	**Name**	**Description**
31:30	---	unused
28:3	mp_y_irq_offs	Reaching this offset value by the current offset counter for addressing main picture Y component, JPEG or raw data leads to generation of fill level interrupt
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.		

Register: MI_MP_CB_BASE_AD_SHD

Base address shadow register for main picture Cb component ring buffer **Reset value: 0000'0000H**

Address: ISP_MI_BASE + 0088H		**Mode : r**
Bits	**Name**	**Description**
31:3	mp_cb_base_ad	Base address of main picture Cb component ring buffer
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.		

Register: MI_MP_CB_SIZE_SHD
Size shadow register of main picture Cb component ring buffer **Reset value: 0000'0000H**

Address: ISP_MI_BASE + 008CH		**Mode : r**
Bits	**Name**	**Description**
31:28	---	unused
27:3	mp_cb_size	Size of main picture Cb component ring buffer.
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.		

Register: MI_MP_CB_OFFS_CNT_SHD

Current offset counter of main picture Cb component ring buffer **Reset value: 0000'0000H**

Address: ISP_MI_BASE + 0090H		**Mode : r**
Bits	**Name**	**Description**
31:28	---	unused
27:3	mp_cb_offs_cnt	Current offset counter of main picture Cb component ring buffer for address generation Note: Soft reset will reset the contents to reset value.
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.		

Register: MI_MP_CR_BASE_AD_SHD

Base address shadow register for main picture Cr component ring buffer **Reset value: 0000'0000H**

Address: ISP_MI_BASE + 0094H		**Mode : r**
Bits	**Name**	**Description**
31:3	mp_cr_base_ad	Base address of main picture Cr component ring buffer
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.		

Register: MI_MP_CR_SIZE_SHD
Size shadow register of main picture Cr component ring buffer **Reset value: 0000'0000H**

Address: ISP_MI_BASE + 0098H		**Mode : r**
Bits	**Name**	**Description**
31:28	---	unused
27:3	mp_cr_size	Size of main picture Cr component ring buffer.
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.		

Register: MI_MP_CR_OFFS_CNT_SHD

Current offset counter of main picture Cr component ring buffer **Reset value: 0000'0000H**

Address: ISP_MI_BASE + 009CH		**Mode : r**
Bits	**Name**	**Description**
31:28	---	unused
27:3	mp_cr_offs_cnt	Current offset counter of main picture Cr component ring buffer for address generation Note: Soft reset will reset the contents to reset value.
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.		

Register: MI_SP_Y_BASE_AD_SHD

Base address shadow register for self picture Y component ring buffer **Reset value: 0000'0000H**

Address: ISP_MI_BASE + 00A0H		**Mode : r**
Bits	**Name**	**Description**
31:3	sp_y_base_ad	Base address of self picture Y component ring buffer.
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.		

Register: MI_SP_Y_SIZE_SHD
Size shadow register of self picture Y component ring buffer **Reset value: 0000'0000H**

Address: ISP_MI_BASE + 00A4H		**Mode : r**
Bits	**Name**	**Description**
31:29	---	unused
28:3	sp_y_size	Size of self picture Y component ring buffer.
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.		

Register: MI_SP_Y_OFFS_CNT_SHD

Current offset counter of self picture Y component ring buffer **Reset value: 0000'0000H**

Address: ISP_MI_BASE + 00A8H		**Mode : r**
Bits	**Name**	**Description**
31:29	---	unused
28:3	sp_y_offs_cnt	Current offset counter of self picture Y component ring buffer for address generation Note: Soft reset will reset the contents to reset value.
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.		

Register: MI_SP_CB_BASE_AD_SHD

Base address shadow register for self picture Cb component ring buffer **Reset value: 0000'0000H**

Address: ISP_MI_BASE + 00B0H		**Mode : r**
Bits	**Name**	**Description**
31:3	sp_cb_base_ad	Base address of self picture Cb component ring buffer.
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.		

Register: MI_SP_CB_SIZE_SHD
Size shadow register of self picture Cb component ring buffer **Reset value: 0000'0000H**

Address: ISP_MI_BASE + 00B4H		**Mode : r**
Bits	**Name**	**Description**
31:28	---	unused
27:3	sp_cb_size	Size of self picture Cb component ring buffer.
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.		

Register: MI_SP_CB_OFFS_CNT_SHD

Current offset counter of self picture Cb component ring buffer **Reset value: 0000'0000H**

Address: ISP_MI_BASE + 00B8H		**Mode : r**
Bits	**Name**	**Description**
31:28	---	unused
27:3	sp_cb_offs_cnt	Current offset counter of self picture Cb component ring buffer for address generation Note: Soft reset will reset the contents to reset value.
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.		

Register: MI_SP_CR_BASE_AD_SHD

Base address shadow register for self picture Cr component ring buffer **Reset value: 0000'0000H**

Address: ISP_MI_BASE + 00BCH		**Mode : r**
Bits	**Name**	**Description**
31:3	sp_cr_base_ad	Base address of self picture Cr component ring buffer.
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.		

Register: MI_SP_CR_SIZE_SHD
Size shadow register of self picture Cr component ring buffer **Reset value: 0000'0000H**

Address: ISP_MI_BASE + 00C0H		**Mode : r**
Bits	**Name**	**Description**
31:28	---	unused
27:3	sp_cr_size	Size of self picture Cr component ring buffer.
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.		

Register: MI_SP_CR_OFFS_CNT_SHD

Current offset counter of self picture Cr component ring buffer **Reset value: 0000'0000H**

Address: ISP_MI_BASE + 00C4H		**Mode : r**
Bits	**Name**	**Description**
31:28	---	unused
27:3	sp_cr_offs_cnt	Current offset counter of self picture Cr component ring buffer for address generation Note: Soft reset will reset the contents to reset value.
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.		

Register: MI_DMA_Y_PIC_START_AD

Y component image start address Reset value: 0000'0000H

Address: ISP_MI_BASE + 00C8H		Mode : rw
Bits	**Name**	**Description**
31:0	dma_y_pic_start_ad	Image start address of the y component Note: Must be multiple of 4 in interleaved mode.

Register: MI_DMA_Y_PIC_WIDTH

Y component image width Reset value: 0000'0000H

Address: ISP_MI_BASE + 00CCH		Mode : rw
Bits	**Name**	**Description**
31:1F	---	unused
14:0	dma_y_pic_width	Image width of the Y component in pixel. For YCbCr 4:2:x the image width must be a multiple of 2. In planar mode the image width of the Cb and Cr component is assumed according to the YCbCr format, i.e. half for 4:2:x and the same size for 4:4:4. In semi planar 4:2:x mode the image width of the Cb component (which includes Cr) is assumed the same size. In interleave mode no Cb/Cr image width is used.

Register: MI_DMA_Y_LLENGTH

Y component original line length Reset value: 0000'0000H

Address: ISP_MI_BASE + 00D0H		Mode : rw
Bits	**Name**	**Description**
31:1F	---	unused
14:0	dma_y_llength	Line length of the Y component of the original image in memory For an uncropped image, where lines follow each other without offset (no line stride), line length must match image width. For Y component the line length in 4:2:x planar mode must be a multiple of 8, for all other component modes a multiple of 4. In planar mode the line length of the Cb and Cr component is assumed according to the YCbCr format, i.e. half for 4:2:x and the same size for 4:4:4. In semi planar 4:2:x mode the line length of the Cb component (which includes Cr) is assumed the same size. In interleave mode no Cb/Cr line length is used.

Register: MI_DMA_Y_PIC_SIZE

Y component image size Reset value: 0000'0000H

Address: ISP_MI_BASE + 00D4H		Mode : rw
Bits	**Name**	**Description**
31:28	---	unused
27:0	dma_y_pic_size	Image size of the Y component in pixel which has to be the Y line length multiplied by the Y image height (dma_y_llength * dma_y_pic_height). In planar mode the image size of the Cb and Cr component is assumed according to the YCbCr format, i.e. a quarter for 4:2:0, half for 4:2:2 and the same for 4:4:4. In semi planar mode the image size of the Cb component (which includes Cr) is assumed half for 4:2:0 and the same size for 4:2:2. In interleave mode no Cb/Cr image size is used.

Register: MI_DMA_CB_PIC_START_AD

Cb component image start address Reset value: 0000'0000H

Address: ISP_MI_BASE + 00D8H		Mode : rw
Bits	**Name**	**Description**
31:0	dma_cb_pic_start_ad	Image start address of the Cb component Note: Must be multiple of 2 in semi-planar mode.

Register: MI_DMA_CR_PIC_START_AD

Cr component image start address Reset value: 0000'0000H

Address: ISP_MI_BASE + 00E8H		Mode : rw
Bits	**Name**	**Description**
31:0	dma_cr_pic_start_ad	Image start address of the Cr component

Register: MI_IMSC

Interrupt Mask („1“: interrupt active, „0“: interrupt masked) Reset value: 0000'0000H

Address: ISP_MI_BASE + 00F8H		Mode : rw
Bits	**Name**	**Description**
31:12	---	unused

Interrupt Mask („1“: interrupt active, „0“: interrupt masked) Reset value: 0000'0000H

Address: ISP_MI_BASE + 00F8H		Mode : rw
Bits	**Name**	**Description**
11	dma_ready	Mask bit for dma ready interrupt
10	---	unused
9	wrap_sp_cr	Mask bit for self picture Cr address wrap interrupt
8	wrap_sp_cb	Mask bit for self picture Cb address wrap interrupt
7	wrap_sp_y	Mask bit for self picture Y address wrap interrupt
6	wrap_mp_cr	Mask bit for main picture Cr address wrap interrupt
5	wrap_mp_cb	Mask bit for main picture Cb address wrap interrupt
4	wrap_mp_y	Mask bit for main picture Y address wrap interrupt
3	fill_mp_y	Mask bit for fill level interrupt of main picture Y, JPEG or raw data
2	mblk_line	Mask bit for makroblock line interrupt of main picture (16 lines of Y, 8 lines of Cb and 8 lines of Cr are written into RAM)
1	sp_frame_end	Mask self picture end of frame interrupt
0	mp_frame_end	Mask main picture end of frame interrupt

Register: MI_RIS

Raw Interrupt Status Reset value: 0000'0000H

Address: ISP_MI_BASE + 00FCH		Mode : r
Bits	**Name**	**Description**
31:12	---	unused
11	dma_ready	Raw status of dma ready interrupt
10	---	unused
9	wrap_sp_cr	Raw status of self picture Cr address wrap interrupt
8	wrap_sp_cb	Raw status of self picture Cb address wrap interrupt
7	wrap_sp_y	Raw status of self picture Y address wrap interrupt
6	wrap_mp_cr	Raw status of main picture Cr address wrap interrupt
5	wrap_mp_cb	Raw status of main picture Cb address wrap interrupt
4	wrap_mp_y	Raw status of main picture Y address wrap interrupt

Raw Interrupt Status Reset value: 0000'0000H

Address: ISP_MI_BASE + 00FCH		Mode : r
Bits	**Name**	**Description**
3	fill_mp_y	Raw status of fill level interrupt of main picture Y, JPEG or raw data
2	mblk_line	Raw status of makroblock line interrupt of main picture (16 lines of Y, 8 lines of Cb and 8 lines of Cr are written into RAM, valid only for planar and semi-planar
1	sp_frame_end	Raw status of self picture end of frame interrupt
0	mp_frame_end	Raw status of main picture end of frame interrupt

Register: MI_MIS

Masked Interrupt Status Reset value: 0000'0000H

Address: ISP_MI_BASE + 0100H		Mode : r
Bits	**Name**	**Description**
31:12	---	unused
11	dma_ready	Masked status of dma ready interrupt
10	---	unused
9	wrap_sp_cr	Masked status of self picture Cr address wrap interrupt
8	wrap_sp_cb	Masked status of self picture Cb address wrap interrupt
7	wrap_sp_y	Masked status of self picture Y address wrap interrupt
6	wrap_mp_cr	Masked status of main picture Cr address wrap interrupt
5	wrap_mp_cb	Masked status of main picture Cb address wrap interrupt
4	wrap_mp_y	Masked status of main picture Y address wrap interrupt
3	fill_mp_y	Masked status of fill level interrupt of main picture Y, JPEG or raw data
2	mblk_line	Masked status of makroblock line interrupt of main picture (16 lines of Y, 8 lines of Cb and 8 lines of Cr are written into RAM, valid only for planar and semi-planar
1	sp_frame_end	Masked status of self picture end of frame interrupt
0	mp_frame_end	Masked status of main picture end of frame interrupt

Register: MI_ICR

Interrupt Clear Register Reset value: 0000'0000H

Address: ISP_MI_BASE + 0104H		**Mode : w**
Bits	**Name**	**Description**
31:12	---	unused
11	dma_ready	Clear dma ready interrupt
10	---	unused
9	wrap_sp_cr	Clear self picture Cr address wrap interrupt
8	wrap_sp_cb	Clear self picture Cb address wrap interrupt
7	wrap_sp_y	Clear self picture Y address wrap interrupt
6	wrap_mp_cr	Clear main picture Cr address wrap interrupt
5	wrap_mp_cb	Clear main picture Cb address wrap interrupt
4	wrap_mp_y	Clear main picture Y address wrap interrupt
3	fill_mp_y	Clear fill level interrupt
2	mblk_line	Clear makroblock line interrupt
1	sp_frame_end	Clear self picture end of frame interrupt
0	mp_frame_end	Clear main picture end of frame interrupt

Register: MI_ISR
Interrupt Set Register Reset value: 0000'0000H

Address: ISP_MI_BASE + 0108H		**Mode : w**
Bits	**Name**	**Description**
31:12	---	unused
11	dma_ready	Set dma ready interrupt
10	---	unused
9	wrap_sp_cr	Set self picture Cr address wrap interrupt
8	wrap_sp_cb	Set self picture Cb address wrap interrupt
7	wrap_sp_y	Set self picture Y address wrap interrupt
6	wrap_mp_cr	Set main picture Cr address wrap interrupt
5	wrap_mp_cb	Set main picture Cb address wrap interrupt

Interrupt Set Register Reset value: 0000'0000H

Address: ISP_MI_BASE + 0108H		Mode : w
Bits	**Name**	**Description**
4	wrap_mp_y	Set main picture Y address wrap interrupt
3	fill_mp_y	Set fill level interrupt
2	mblk_line	Set makroblock line interrupt
1	sp_frame_end	Set self picture end of frame interrupt
0	mp_frame_end	Set main picture end of frame interrupt

Register: MI_STATUS

MI Status Register Reset value: 0000'0000H

Address: ISP_MI_BASE + 010CH		Mode : r
Bits	**Name**	**Description**
31:7	---	unused
6	sp_cr_fifo_full	FIFO full flag of Cr FIFO in self path asserted since last clear
5	sp_cb_fifo_full	FIFO full flag of Cb FIFO in self path asserted since last clear
4	sp_y_fifo_full	FIFO full flag of Y FIFO in self path asserted since last clear
3	---	unused
2	mp_cr_fifo_full	FIFO full flag of Cr FIFO in main path asserted since last clear
1	mp_cb_fifo_full	FIFO full flag of Cb FIFO in main path asserted since last clear
0	mp_y_fifo_full	FIFO full flag of Y FIFO in main path asserted since last clear

Register: MI_STATUS_CLR

MI Status Clear Register Reset value: 0000'0000H

Address: ISP_MI_BASE + 0110H		Mode : w
Bits	**Name**	**Description**
31:7	---	unused
6	sp_cr_fifo_full	Clear status of Cr FIFO full flag in self path
5	sp_cb_fifo_full	Clear status of Cb FIFO full flag in self path
4	sp_y_fifo_full	Clear status of Y FIFO full flag in self path

MI Status Clear Register Reset value: 0000'0000H

Address: ISP_MI_BASE + 0110H		Mode : w
Bits	**Name**	**Description**
3	---	unused
2	mp_cr_fifo_full	Clear status of Cr FIFO full flag in main path
1	mp_cb_fifo_full	Clear status of Cb FIFO full flag in main path
0	mp_y_fifo_full	Clear status of Y FIFO full flag in main path

Register: MI_SP_Y_PIC_WIDTH

Y component image width Reset value: 0000'0000H

Address: ISP_MI_BASE + 0114H		Mode : rw
Bits	**Name**	**Description**
31:15	---	unused
14:0	sp_y_pic_width	Image width of the self picture Y component or RGB picture in pixel. For YCbCr 4:2:x and RGB 565 the image width must be a multiple of 2. If no line stride is used but flipping required, the image width must be a multiple of 8 for 4:2:x planar or 4 for 4:4:4 planar/4:2:x semi planar. There are no restrictions for RGB 888/666. In planar mode the image width of the Cb and Cr component is assumed according to the YCbCr format, i.e. half for 4:2:x and the same size for 4:4:4. In semi planar 4:2:x mode the image width of the Cb component (which includes Cr) is assumed the same size. In interleave mode no Cb/Cr image width is used. Note: Image width always refers to the picture width of the output image. This is particularly important when rotating. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path.

Register: MI_SP_Y_PIC_HEIGHT

Y component image height Reset value: 0000'0000H

Address: ISP_MI_BASE + 0118H		Mode : rw
Bits	**Name**	**Description**
31:15	---	unused

Y component image height Reset value: 0000'0000H

Address: ISP_MI_BASE + 0118H		Mode : rw
Bits	**Name**	**Description**
14:0	sp_y_pic_height	Image height of the y component or RGB picture in pixel. In planar and semi planar mode the image width of the cb and cr component is assumed according to the YCbCr format, i.e. half for 4:2:0 and the same for 4:2:2 and 4:4:4. Note: Image height always refers to the picture height of the output image. This is particularly important when rotating.

Register: MI_SP_Y_PIC_SIZE

Y component image size Reset value: 0000'0000H

Address: ISP_MI_BASE + 011CH		Mode : rw
Bits	**Name**	**Description**
31:25	---	unused
24:0	sp_y_pic_size	Image size of the Y component or RGB picture in pixel which has to be the Y line length multiplied by the Y image height (sp_y_llength * sp_y_pic_height). In planar mode the image size of the Cb and Cr component is assumed according to the YCbCr format, i.e. a quarter for 4:2:0, half for 4:2:2 and the same for 4:4:4. In semi planar mode the image size of the Cb and Cr component is assumed half for 4:2:0 and the same size for 4:2:2. Note: Programmed value becomes effective immediately. So write to the register only if no picture

Register: MI_DMA_CTRL

DMA control register Reset value: 0000'0000H

Address: ISP_MI_BASE + 0120H		Mode : rw
Bits	**Name**	**Description**
31:14	---	unused

DMA control register Reset value: 0000'0000H

Address: ISP_MI_BASE + 0120H		**Mode : rw**
Bits	**Name**	**Description**
13:12	dma_rgb_format	Selects RGB Bayer data of read DMA picture 00: no DMA RGB Bayer data 01: 8 bit RGB Bayer data 10: 16 bit RGB Bayer data (12 bit used) bytes are organized MSB first and 4 lower bits of LSB remain unused: byte_even -> bayer[11:4], byte_odd[7:4] -> bayer[3:0] 11: reserved.
11	---	unused
10	dma_frame_end_disable	Suppresses v_end so that no frame end can be detected by following instances. Note: The dma_ready interrupt is raised as usual, but the dma_frame_end interrupt will not be generated until v_end has been
9	dma_continuous_en	Enables continuous mode. If set the same frame is read back over and over. A start pulse on dma_start is needed only for the first time. To stop continuous mode reset this bit (takes effect after the next frame end) or execute a soft reset. This bit is intended to be used in conjunction with the Superimpose feature.
8	dma_byte_swap	Enables change of DMA byte order of the 32 bit input word at read port 1: byte order is mirrored but the bit order within one byte doesn"t change 0: no byte mirroring
7:6	dma_inout_format	Selects input/output format of DMA picture. 11: YCbCr 4:4:4 10: YCbCr 4:2:2 01: YCbCr 4:2:0 00: YCbCr 4:0:0
5:4	dma_read_format	Defines how YCbCr picture data is read from memory. 00: planar 01: semi planar, for YCbCr 4:2:x 10: interleaved (combined), for YCbCr 4:2:2 and RGB only 11: reserved
3:2	dma_burst_len_chrom	Burst length for Cb or Cr data affecting DMA read port. 00: 4-beat bursts 01: 8-beat bursts 10: 16-beat bursts 11: reserved Ignored if 8- or 16-beat bursts are not supported.

DMA control register Reset value: 0000'0000H

Address: ISP_MI_BASE + 0120H		Mode : rw
Bits	**Name**	**Description**
1:0	dma_burst_len_lum	Burst length for Y data affecting DMA read port. 00: 4-beat bursts 01: 8-beat bursts 10: 16-beat bursts 11: reserved Ignored if 8- or 16-beat bursts are not supported.

Register: MI_DMA_START

DMA start register Reset value: 0000'0000H

Address: ISP_MI_BASE + 0124H		Mode : w
Bits	**Name**	**Description**
31:1	---	unused
0	dma_start	Enables DMA access. Additionally main or self path has to be enabled separately.

Register: MI_DMA_STATUS

DMA status register Reset value: 0000'0000H

Address: ISP_MI_BASE + 0128H		Mode : r
Bits	**Name**	**Description**
31:1	---	unused
0	dma_active	If set DMA access is active.

Register: MI_PIXEL_CNT

Counter value for defect pixel list Reset value: 0000'0000H

Address: ISP_MI_BASE + 012CH		Mode : r
Bits	**Name**	**Description**
31:28	---	unused

Counter value for defect pixel list Reset value: 0000'0000H

Address: ISP_MI_BASE + 012CH		Mode : r
Bits	**Name**	**Description**
27:0	pix_cnt	Counter value specifies the number of pixels of the defect pixel list generated by DPCC of the last transmitted frame. Updated at frame end. A soft reset will set the counter to zero.

Register: MI_MP_Y_BASE_AD_INIT2

Base address 2 (ping pong) for main picture Y component, JPEG or raw data Reset value: 0000'0000H

Address: ISP_MI_BASE + 0130H		Mode : rw
Bits	**Name**	**Description**
31:3	mp_y_base_ad_init2	2nd ping pong base address of main picture Y component buffer, JPEG buffer or raw data buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect.
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details. Refer also to MI_MP_Y_BASE_AD_INIT with respect to the burst alignment restriction for AXI.		

Register: MI_MP_CB_BASE_AD_INIT2
Base address 2 (pingpong) for main picture Cb component Reset value: 0000'0000H

Address: ISP_MI_BASE + 0134H		Mode : rw
Bits	**Name**	**Description**
31:3	mp_cb_base_ad_init2	2nd ping pong base address of main picture Cb component buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect.

Base address 2 (pingpong) for main picture Cb component Reset value: 0000'0000H

Address: ISP_MI_BASE + 0134H		Mode : rw
Bits	**Name**	**Description**
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details. Refer also to MI_MP_Y_BASE_AD_INIT with respect to the burst alignment restriction for AXI.		

Register: MI_MP_CR_BASE_AD_INIT2
Base address 2 (pingpong) for main picture Cr component ring buffer
Reset value: 0000'0000H

Address: ISP_MI_BASE + 0138H		Mode : rw
Bits	**Name**	**Description**
31:3	mp_cr_base_ad_init2	2nd ping pong Base address of main picture Cr component buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect.
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details. Refer also to MI_MP_Y_BASE_AD_INIT with respect to the burst alignment restriction for AXI.		

Register: MI_SP_Y_BASE_AD_INIT2

Base address 2 (ping pong) for self picture Y component Reset value: 0000'0000H

Address: ISP_MI_BASE + 013CH		Mode : rw
Bits	**Name**	**Description**
31:3	sp_y_base_ad_init2	2nd ping pong base address of self picture Y component buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details. Refer also to MI_MP_Y_BASE_AD_INIT with respect to the burst alignment restriction for AXI.		

Register: MI_SP_CB_BASE_AD_INIT2
Base address 2 (pingpong) for self picture Cb component Reset value: 0000'0000H

Address: ISP_MI_BASE + 0140H		Mode : rw
Bits	**Name**	**Description**
31:3	sp_cb_base_ad_init2	2nd ping pong base address of self picture Cb component buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details. Refer also to MI_MP_Y_BASE_AD_INIT with respect to the burst alignment restriction for AXI		

Register: MI_SP_CR_BASE_AD_INIT2

Base address 2 (pingpong) for self picture Cr component ring buffer Reset value: 0000'0000H

Address: ISP_MI_BASE + 0144H		Mode : rw
Bits	**Name**	**Description**
31:3	sp_cr_base_ad_init2	2nd ping pong Base address of self picture Cr component buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic config update. Note: Set control bit init_base_en before updating so that a forced or automatic update can
2:0	---	unused
Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details. Refer also to MI_MP_Y_BASE_AD_INIT with respect to the burst alignment restriction for AXI		

Register: MI_XTD_FORMAT_CTRL
Extended Storage Format Control for main, self and dma read path Reset value: 0000'0000H

Address: ISP_MI_BASE + 0148H		Mode : rw
Bits	**Name**	**Description**
31:2	---	unused
2	nv21_dma_read	0: dma read path: use NV12 storage format for semi-planar YCbCr 4:2:x mode, Cb is located on even addresses. 1: dma read path: use NV21 storage format for
1	nv21_self	0: self path: use NV12 storage format for semi-planar YCbCr 4:2:x mode, Cb is located on even addresses. 1: self path: use NV21 storage format for semi-planar YCbCr 4:2:x mode, Cr is located on even addresses.

Address: ISP_MI_BASE + 0148H		Mode : rw
Bits	**Name**	**Description**
0	nv21_main	0: main path: use NV12 storage format for semi-planar YCbCr 4:2:x mode, Cb is located on even addresses. 1: main path: use NV21 storage format for

Register: MIPI_CTRL
global control register Reset value: 0006'0000H

Address: ISP_MIPI_BASE + 0000H		Mode : rw
Bits	**Name**	**Description**
31:10	---	unused
18	S_ENABLE_CLK	Sensor clock lane enable signal. This register is directly connected to the output port "s_enableclk". '1': enable sensor clock lane (DEFAULT) '0': disable sensor clock lane
17	ERR_SOT_SYNC_HS_SKIP	1: data within the current transmission is skipped if ErrSotSyncHS is detected (default) 0: ErrSotSyncHS does not affect transmission
16	ERR_SOT_HS_SKIP	1: data within the current transmission is skipped if ErrSotHS is detected 0: ErrSotHS does not affect transmission (default)
15:14	---	unused
13:12	NUM_LANES	00: Lane 1 is used 01: Lanes 1 and 2 are used 10: Lanes 1, 2 and 3 are used 11: Lanes 1, 2, 3 and 4 are used (default)
11:8	SHUTDOWN_LANE	Shutdown Lane Module. Content of this register is directly connected to the output signal shutdown[n-1:0] where n denotes the lane number 1..4
7:2	---	unused
1	FLUSH_FIFO	writing '1' resets the write- and read pointers of the additional data fifo, reading returns the status of the flush_fifo bit. This bit must be reset by software.
0	OUTPUT_ENA	1: output to add data fifo and to output interface is enabled 0: output is disabled

Register: MIPI_STATUS
global status register Reset value: 0000'0000H

Address: ISP_MIPI_BASE + 0004H		Mode : r
Bits	**Name**	**Description**
31:14	---	unused
13	S_ULP_ACTIVE_NOT_CLK	sensor clock lane is in ULP state. This register is directly connected to the synchronized input signal "s_ulpsactivenotclk"

12	S_STOPSTATE_CLK	sensor clock lane is in stopstate. This register is directly connected to the synchronized input signal "s_stopstateclk"
11:8	STOPSTATE	Data Lane is in stopstate. This register is directly connected to the synchronized input signal stopstate[n-1:0] where n denotes the lane number 1..4
7:1	---	unused
0	ADD_DATA_AVAIL	1: additional data fifo contains data 0: additional data fifo is empty

Register: MIPI_IMSC
Interrupt mask Reset value: 0000'0000H

Address: ISP_MIPI_BASE + 0008H		**Mode : rw**
Bits	**Name**	**Description**
31:28	---	unused
27	IMSC_GEN_SHORT_PACK	enable interrupt (1) or mask out (0)
26	IMSC_ADD_DATA_FILL_LEVEL	enable interrupt (1) or mask out (0)
25	IMSC_ADD_DATA_OVFLW	enable interrupt (1) or mask out (0)
24	IMSC_FRAME_END	enable interrupt (1) or mask out (0)
23	IMSC_ERR_CS	enable interrupt (1) or mask out (0)
22	IMSC_ERR_ECC1	enable interrupt (1) or mask out (0)
21	IMSC_ERR_ECC2	enable interrupt (1) or mask out (0)
20	IMSC_ERR_PROTOCOL	enable interrupt (1) or mask out (0)
19:16	IMSC_ERR_CONTROL	enable interrupt (1) or mask out (0)
15:12	IMSC_ERR_EOT_SYNC	enable interrupt (1) or mask out (0)
11:8	IMSC_ERR_SOT_SYNC	enable interrupt (1) or mask out (0)
7:4	IMSC_ERR_SOT	enable interrupt (1) or mask out (0)
3:0	IMSC_SYNC_FIFO_OVFLW	enable interrupt (1) or mask out (0)

Register: MIPI_RIS

Raw interrupt status Reset value: 0000'0000H

Address: ISP_MIPI_BASE + 000CH		**Mode : r**
Bits	**Name**	**Description**
31:28	---	unused
27	RIS_GEN_SHORT_PACK	generic short packet was received (only available in version 2 of MIPI interface) When this interrupt is cleared, all the bits of the MIPI_GEN_SHORT_DT status register are cleared as well; Setting of this interrupt via MIPI_ISR register will set all the bits of the MIPI_GEN_SHORT_DT register.
26	RIS_ADD_DATA_FILL_LEVEL	Programmed fill level was reached; will be raised as long as the fill level is greater than the programmed value
25	RIS_ADD_DATA_OVFLW	additional data fifo overflow occurred
24	RIS_FRAME_END	frame end send to output interface
23	RIS_ERR_CS	checksum error occurred
22	RIS_ERR_ECC1	1-bit ecc error occurred
21	RIS_ERR_ECC2	2-bit ecc error occurred
20	RIS_ERR_PROTOCOL	packet start detected within current packet
19:16	RIS_ERR_CONTROL	PPI interface control error occured, one bit for each lane
15:12	RIS_ERR_EOT_SYNC	PPI interface eot sync error occured, one bit for each lane
11:8	RIS_ERR_SOT_SYNC	PPI interface sot sync error occured, one bit for each lane
7:4	RIS_ERR_SOT	PPI interface sot error occured, one bit for each lane
3:0	RIS_SYNC_FIFO_OVFLW	synchronization fifo overflow occurred, one bit for each lane

Register: MIPI_MIS
Masked interrupt status Reset value: 0000'0000H

Address: ISP_MIPI_BASE + 0010H		**Mode : r**
Bits	**Name**	**Description**
31:28	---	unused
27	MIS_GEN_SHORT_PACK	generic short packet was received (only available in version 2 of MIPI interface)
26	MIS_ADD_DATA_FILL_LEVEL	Programmed fill level was reached; will be raised as long as the fill level is greater the programmed value
25	MIS_ADD_DATA_OVFLW	additional data fifo overflow
24	MIS_FRAME_END	frame end send to output interface
23	MIS_ERR_CS	checksum error occurred

Address: ISP_MIPI_BASE + 0010H			Mode : r
Bits	**Name**	**Description**	
22	MIS_ERR_ECC1	1-bit ecc error occurred	
21	MIS_ERR_ECC2	2-bit ecc error occurred	
20	MIS_ERR_PROTOCOL	packet start detected within current packet	
19:16	MIS_ERR_CONTROL	PPI interface control error occured, one bit for each lane	
15:12	MIS_ERR_EOT_SYNC	PPI interface eot sync error occured, one bit for each lane	
11:8	MIS_ERR_SOT_SYNC	PPI interface sot sync error occured, one bit for each lane	
7:4	MIS_ERR_SOT	PPI interface sot error occured, one bit for each lane	
3:0	MIS_SYNC_FIFO_OVFLW	synchronization fifo overflow occurred, one bit for each lane	

Register: MIPI_ICR

Interrupt clear register Reset value: 0000'0000H

Address: ISP_MIPI_BASE + 0014H			Mode : w
Bits	**Name**	**Description**	
31:28	---	unused	
27	ICR_GEN_SHORT_PACK	1: clear register; 0: nothing happens	
26	ICR_ADD_DATA_FILL_LEVEL	1: clear register; 0: nothing happens	
25	ICR_ADD_DATA_OVFLW	1: clear register; 0: nothing happens	
24	ICR_FRAME_END	1: clear register; 0: nothing happens	
23	ICR_ERR_CS	1: clear register; 0: nothing happens	
22	ICR_ERR_ECC1	1: clear register; 0: nothing happens	
21	ICR_ERR_ECC2	1: clear register; 0: nothing happens	
20	ICR_ERR_PROTOCOL	1: clear register; 0: nothing happens	
19:16	ICR_ERR_CONTROL	1: clear register; 0: nothing happens (one bit for each lane)	

Interrupt clear register Reset value: 0000'0000H

Address: ISP_MIPI_BASE + 0014H			Mode : w
Bits	**Name**	**Description**	
15:12	ICR_ERR_EOT_SYNC	1: clear register; 0: nothing happens (one bit for each lane)	
11:8	ICR_ERR_SOT_SYNC	1: clear register; 0: nothing happens (one bit for each lane)	
7:4	ICR_ERR_SOT	1: clear register; 0: nothing happens (one bit for each lane)	

Address: ISP_MIPI_BASE + 0014H		Mode : w
Bits	**Name**	**Description**
3:0	ICR_SYNC_FIFO_OVFLW	1: clear register; 0: nothing happens (one bit for each lane)
Note: clears corresponding bits in MIPI_RIS register		

Register: MIPI_ISR

Interrupt set register Reset value: 0000'0000H

Address: ISP_MIPI_BASE + 0018H		Mode : w
Bits	**Name**	**Description**
31:28	---	unused
27	ISR_GEN_SHORT_PACK	1: set register; 0: nothing happens
26	ISR_ADD_DATA_FILL_LEVEL	1: set register; 0: nothing happens
25	ISR_ADD_DATA_OVFLW	1: set register; 0: nothing happens
24	ISR_FRAME_END	1: set register; 0: nothing happens
23	ISR_ERR_CS	1: set register; 0: nothing happens
22	ISR_ERR_ECC1	1: set register; 0: nothing happens
21	ISR_ERR_ECC2	1: set register; 0: nothing happens
20	ISR_ERR_PROTOCOL	1: set register; 0: nothing happens
19:16	ISR_ERR_CONTROL	1: set register; 0: nothing happens (one bit for each lane)
15:12	ISR_ERR_EOT_SYNC	1: set register; 0: nothing happens (one bit for each lane)
11:8	ISR_ERR_SOT_SYNC	1: set register; 0: nothing happens (one bit for each lane)
7:4	ISR_ERR_SOT	1: set register; 0: nothing happens (one bit for each lane)
3:0	ISR_SYNC_FIFO_OVFLW	1: set register; 0: nothing happens (one bit for each lane)
Note: sets corresponding bits in MIPI_RIS register		

Register: MIPI_CUR_DATA_ID

Current Data Identifier Reset value: 0000'0000H

Address: ISP_MIPI_BASE + 001CH		Mode : r
Bits	**Name**	**Description**
31:8	---	unused
7:6	VIRTUAL_CHANNEL	virtual channel of currently received packet
5:0	DATA_TYPE	data type of currently received packet

Register: MIPI_IMG_DATA_SEL

Image Data Selector Reset value: 0000'0000H

Address: ISP_MIPI_BASE + 0020H		Mode : rw
Bits	**Name**	**Description**
31:8	---	unused
7:6	VIRTUAL_CHANNEL_SEL	virtual channel selector for image data output
5:0	DATA_TYPE_SEL	data type selector for image data output: 0x08...0x0F generic short packets 0x12 embedded 8-bit data 0x18 YUV 420 8-bit 0x19 YUV 420 10-bit 0x1A Legacy YUV 420 8-bit 0x1C YUV 420 8-bit (CSPS) 0x1D YUV 420 10-bit (CSPS) 0x1E YUV 422 8-bit 0x1F YUV 422 10-bit 0x20 RGB 444 0x21 RGB 555 0x22 RGB 565 0x23 RGB 666 0x24 RGB 888 0x28 RAW 6 0x29 RAW 7 0x2A RAW 8 0x2B RAW 10 0x2C RAW 12 0x30...0x37 User Defined Byte-based data

Register: MIPI_ADD_DATA_SEL_1

Additional Data Selector 1 Reset value: 0000'00FFH

Address: ISP_MIPI_BASE + 0024H		Mode : rw
Bits	**Name**	**Description**
31:8	---	unused
7:6	ADD_DATA_VC_1	virtual channel selector for additional data output
5:0	ADD_DATA_TYPE_1	data type selector for additional data output

Register: MIPI_ADD_DATA_SEL_2

Additional Data Selector 2 Reset value: 0000'00FFH

Address: ISP_MIPI_BASE + 0028H		Mode : rw
Bits	**Name**	**Description**
31:8	---	unused
7:6	ADD_DATA_VC_2	virtual channel selector for additional data output
5:0	ADD_DATA_TYPE_2	data type selector for additional data output

Register: MIPI_ADD_DATA_SEL_3

Additional Data Selector 3 Reset value: 0000'00FFH

Address: ISP_MIPI_BASE + 002CH		Mode : rw
Bits	**Name**	**Description**
31:8	---	unused
7:6	ADD_DATA_VC_3	virtual channel selector for additional data output
5:0	ADD_DATA_TYPE_3	data type selector for additional data output

Register: MIPI_ADD_DATA_SEL_4
Additional Data Selector 4 Reset value: 0000'00FFH

Address: ISP_MIPI_BASE + 0030H		Mode : rw
Bits	**Name**	**Description**
31:8	---	unused
7:6	ADD_DATA_VC_4	virtual channel selector for additional data output

Additional Data Selector 4 Reset value: 0000'00FFH

Address: ISP_MIPI_BASE + 0030H		Mode : rw
Bits	**Name**	**Description**
5:0	ADD_DATA_TYPE_4	data type selector for additional data output

Register: MIPI_ADD_DATA_FIFO

Additional Data Fifo Reset value: 0000'0000H

Address: ISP_MIPI_BASE + 0034H		Mode : r
Bits	**Name**	**Description**
31:0	ADD_DATA_FIFO	lowest 4 bytes in additional data fifo; reading increments fifo read pointer. First embedded data byte will be written to bits 7:0 of 32-bit data word, second data byte written to 15:8 etc.

Register: MIPI_ADD_DATA_FILL_LEVEL

Additional Data FIFO Fill Level Reset value: 0000'0000H

Address: ISP_MIPI_BASE + 0038H		Mode : rw
Bits	**Name**	**Description**
31:13	---	unused

12:0	ADD_DATA_FILL_LEVEL	FIFO level in dwords for triggering the FILL_LEVEL interrupt, must be 32-bit aligned (bit 0 and bit 1 are hard wired to "00")

Register: MIPI_COMPRESSED_MODE

controls processing of compressed raw data types **Reset value: 0000'0000H**

Address: ISP_MIPI_BASE + 003CH		**Mode : rw**
Bits	**Name**	**Description**
31:9	---	unused
8	predictor_sel	predictor to be used: 0: predictor 1 1: predictor 2
7	---	unused

controls processing of compressed raw data types **Reset value: 0000'0000H**

Address: ISP_MIPI_BASE + 003CH		**Mode : rw**
Bits	**Name**	**Description**
6:4	comp_scheme	data compression scheme: 0: 12–8–12 1: 12–7–12 2: 12–6–12 3: 10–8–10 4: 10–7–10 5: 10–6–10 6..7: reserved
3:1	---	unused
0	compress_en	1: enable compressed mode processing 0: disable compressed mode
Note: This register is only available in MIPI interface version 2 of ISP		

Register: MIPI_FRAME

frame number from frame start and frame end short packets **Reset value: 0000'0000H**

Address: ISP_MIPI_BASE + 0040H		**Mode : r**
Bits	**Name**	**Description**
31:16	frame_number_fe	16 bit frame number from Frame End (FE) short packet
15:0	frame_number_fs	16 bit frame number from Frame Start (FS) short packet
Note: This register is only available in MIPI interface version 2 of ISP		

Register: MIPI_GEN_SHORT_DT

data type flags for received generic short packets **Reset value: 0000'0000H**

Address: ISP_MIPI_BASE + 0044H		Mode : r
Bits	**Name**	**Description**
31:0	---	unused
7	GEN_SHORT_DT_0xF	1: generic short packet of data type 0xF received 0: data type 0xF not received
6	GEN_SHORT_DT_0xE	1: generic short packet of data type 0xE received 0: data type 0xE not received
5	GEN_SHORT_DT_0xD	1: generic short packet of data type 0xD received 0: data type 0xD not received
4	GEN_SHORT_DT_0xC	1: generic short packet of data type 0xC received 0: data type 0xC not received
3	GEN_SHORT_DT_0xB	1: generic short packet of data type 0xB received 0: data type 0xB not received
2	GEN_SHORT_DT_0xA	1: generic short packet of data type 0xA received 0: data type 0xA not received
1	GEN_SHORT_DT_0x9	1: generic short packet of data type 0x9 received 0: data type 0x9 not received
0	GEN_SHORT_DT_0x8	1: generic short packet of data type 0x8 received 0: data type 0x8 not received
Note: This register is only available in MIPI interface version 2 of ISP		

Register: MIPI_GEN_SHORT_8_9

data field for generic short packets of data type 0x8 and 0x9 Reset value: 0000'0000H

Address: ISP_MIPI_BASE + 0048H		Mode : r
Bits	**Name**	**Description**
31:16	data_field_9	16 bit user defined data field from last generic short packet of data type 0x9
15:0	data_field_8	16 bit user defined data field from last generic short packet of data type 0x8
Note: This register is only available in MIPI interface version 2 of ISP		

Register: MIPI_GEN_SHORT_A_B

data field for generic short packets of data type 0xA and 0xB Reset value: 0000'0000H

Address: ISP_MIPI_BASE + 004CH		Mode : r
Bits	**Name**	**Description**
31:16	data_field_B	16 bit user defined data field from last generic short packet of data type 0xB

15:0	data_field_A	16 bit user defined data field from last generic short packet of data type 0xA
Note: This register is only available in MIPI interface version 2 of ISP		

Register: MIPI_GEN_SHORT_C_D

data field for generic short packets of data type 0xC and 0xD Reset value: 0000'0000H

Address: ISP_MIPI_BASE + 0050H		**Mode : r**
Bits	**Name**	**Description**
31:16	data_field_D	16 bit user defined data field from last generic short packet of data type 0xD
15:0	data_field_C	16 bit user defined data field from last generic short packet of data type 0xC
Note: This register is only available in MIPI interface version 2 of ISP		

Register: MIPI_GEN_SHORT_E_F

data field for generic short packets of data type 0xE and 0xF Reset value: 0000'0000H

Address: ISP_MIPI_BASE + 0054H		**Mode : r**
Bits	**Name**	**Description**
31:16	data_field_F	16 bit user defined data field from last generic short packet of data type 0xF
15:0	data_field_E	16 bit user defined data field from last generic short packet of data type 0xE
Note: This register is only available in MIPI interface version 2 of ISP		

This is the control register for AF measurement unit Reset value: 0000'0000H

Address: ISP_AFM_BASE + 0000H		**Mode : rw**
Bits	**Name**	**Description**
31:1	---	unused

0	afm_en	AF measurement enable 0: AF measurement is disabled 1: AF measurement is enabled Writing a 1 to this register starts a new measurement and resets the afm_fin (measurement finished) interrupt to 0.

Register: ISP_AFM_LT_A

Top Left corner of measure window A Reset value: 0000'0000H

Address: ISP_AFM_BASE + 0004H		**Mode : rw**
Bits	**Name**	**Description**
31:29	---	unused
28:16	a_h_l	first pixel of window A (horizontal left row), value must be greater or equal 5
15:13	---	unused
12:0	a_v_t	first line of window A (vertical top line), value must be greater or equal 2

Register: ISP_AFM_RB_A

Bottom right corner of measure window A Reset value: 0000'0000H

Address: ISP_AFM_BASE + 0008H		**Mode : rw**
Bits	**Name**	**Description**
31:29	---	unused
28:16	a_h_r	last pixel of window A (horizontal right row)
15:13	---	unused
12:0	a_v_b	last line of window A (vertical bottom line), value must be lower than (number of lines – 2)

Register: ISP_AFM_LT_B

Top left corner of measure window B Reset value: 0000'0000H

Address: ISP_AFM_BASE + 000CH			Mode : rw
Bits	**Name**	**Description**	
31:30	---	unused	
28:16	b_h_l	first pixel of window B (horizontal left row), value must be greater or equal 5	
15:13	---	unused	
12:0	b_v_t	first line of window B (vertical top line), value must be greater or equal 2	

Register: ISP_AFM_RB_B

Bottom right corner of measure window B Reset value: 0000'0000H

Address: ISP_AFM_BASE + 0010H			Mode : rw
Bits	**Name**	**Description**	
31:30	---	unused	
28:16	b_h_r	last pixel of window B (horizontal right row)	
15:13	---	unused	
12:0	b_v_b	last line of window B (vertical bottom line), value must be lower than (number of lines – 2)	

Register: ISP_AFM_LT_C
Top left corner of measure window C Reset value: 0000'0000H

Address: ISP_AFM_BASE + 0014H			Mode : rw
Bits	**Name**	**Description**	
31:30	---	unused	
28:16	c_h_l	first pixel of window C (horizontal left row), value must be greater or equal 5	
15:13	---	unused	
12:0	c_v_t	first line of window C (vertical top line), value must be greater or equal 2	

Register: ISP_AFM_RB_C

Bottom right corner of measure window C Reset value: 0000'0000H

Address: ISP_AFM_BASE + 0018H		Mode : rw
Bits	**Name**	**Description**
31:29	---	unused
28:16	c_h_r	last pixel of window C (horizontal right row)
15:13	---	unused
12:0	c_v_b	last line of window C (vertical bottom line), value must be lower than (number of lines – 2)

Register: ISP_AFM_THRES

Threshold register Reset value: 0000'0000H

Address: ISP_AFM_BASE + 001CH		Mode : rw
Bits	**Name**	**Description**
31:16	---	unused
15:0	afm_thres	AF measurement threshold This register defines a threshold which can be used for minimizing the influence of noise in the

Register: ISP_AFM_VAR_SHIFT

Variable shift register Reset value: 0000'0000H

Address: ISP_AFM_BASE + 0020H		Mode : rw
Bits	**Name**	**Description**
31:19	---	unused
18:16	lum_var_shift	variable shift for luminance summation The lum_var_shift defines the number of bits for the shift operation of the value of the current pixel before summation. The shift operation is used to avoid a luminance sum overflow.
15:3	---	unused
2:0	afm_var_shift	variable shift for AF measurement The afm_var_shift defines the number of bits for the shift operation at the end of the calculation chain. The shift operation is used to avoid an AF measurement sum overflow.

Register: ISP_AFM_SUM_A

Sharpness Value Status Register of Window A Reset value: 0000'0000H

Address: ISP_AFM_BASE + 0024H			Mode : r
Bits	Name	Description	
31:0	afm_sum_a	sharpness value of window A	

Register: ISP_AFM_SUM_B
Sharpness Value Status Register of Window B Reset value: 0000'0000H

Address: ISP_AFM_BASE + 0028H			Mode : r
Bits	Name	Description	
31:0	afm_sum_b	sharpness value of window B	

Register: ISP_AFM_SUM_C

Sharpness Value Status Register of Window C Reset value: 0000'0000H

Address: ISP_AFM_BASE + 002CH			Mode : r
Bits	Name	Description	
31:0	afm_sum_c	sharpness value of window C	

Register: ISP_AFM_LUM_A
Luminance Value Status Register of Window A Reset value: 0000'0000H

Address: ISP_AFM_BASE + 0030H			Mode : r
Bits	Name	Description	
31:24	---	unused	
23:0	afm_lum_a	luminance value of window A	

Register: ISP_AFM_LUM_B

Luminance Value Status Register of Window B Reset value: 0000'0000H

Address: ISP_AFM_BASE + 0034H			Mode : r
Bits	Name	Description	
31:24	---	unused	
23:0	afm_lum_b	luminance value of window B	

Register: ISP_AFM_LUM_C

Luminance Value Status Register of Window C Reset value: 0000'0000H

Address: ISP_AFM_BASE + 0038H			Mode : r
Bits	Name	Description	
31:24	---	unused	
23:0	afm_lum_c	luminance value of window C	

Register: ISP_LSC_CTRL

Lens shade control Reset value: 0000'0000H

Address: ISP_LSC_BASE + 0000H			Mode : rw
Bits	Name	Description	
31:1	---	unused	
0	lsc_en	0: activation request for lens shading correction 1: deactivation reqeust for lens shading correction Activation/Deactivation is object of a shadowing mechnism. The current status is visible at ISP_LSC_STATUS::lsc_enable_status	

Register: ISP_LSC_R_TABLE_ADDR

Table RAM Address for red component Reset value: 0000'0000H

Address: ISP_LSC_BASE + 0004H			Mode : rwh
Bits	Name	Description	
31:0	---	unused	

Table RAM Address for red component Reset value: 0000'0000H

Address: ISP_LSC_BASE + 0004H			Mode : rwh
Bits	Name	Description	
8:0	r_ram_addr	table address in RAM for samples of the R color component. Will be automatically incremented by each read or write access to the table. Valid addresses are in the range 0 to 152.	
Note: The table values are written into an internal RAM. The RAM Address is generated per auto- increment. The tables values will be read back by a continuous read access to the corresponding register. The read address is auto-incremented for each read access to that register and is reset to a specific value by a write access to the ISP_LSC_TABLE_ADDR register. Table set 0 access by SW at table address 0...152. Table set 1 access at table address 153...305.			

Register: ISP_LSC_GR_TABLE_ADDR

Table RAM Address for green (red) component Reset value: 0000'0000H

Address: ISP_LSC_BASE + 0008H		Mode : rwh
Bits	**Name**	**Description**
31:0	---	unused
8:0	gr_ram_addr	table address in RAM for samples of the G_R color component. Will be automatically incremented by each read or write access to the table.
Note: MKOE tbc: Orignial register mode was rwh which is no longer supported with new version of SIG-> rwhh Table set 0 access by SW at table address 0...153. Table set 1 access at table address 154...307.		

Register: ISP_LSC_B_TABLE_ADDR

Table RAM Address for blue component Reset value: 0000'0000H

Address: ISP_LSC_BASE + 000CH		Mode : rwh
Bits	**Name**	**Description**
31:0	---	unused

Table RAM Address for blue component Reset value: 0000'0000H

Address: ISP_LSC_BASE + 000CH		Mode : rwh
Bits	**Name**	**Description**
8:0	b_ram_addr	table address in RAM for samples of the B color component. Will be automatically incremented by each read or write access to the table.
Note: MKOE tbc: Orignial register mode was rwh which is no longer supported with new version of SIG-> rwhh Table set 0 access by SW at table address 0...153. Table set 1 access at table address 154...307.		

Register: ISP_LSC_GB_TABLE_ADDR

Table RAM Address for green (blue) component Reset value: 0000'0000H

Address: ISP_LSC_BASE + 0010H		Mode : rwh
Bits	**Name**	**Description**
31:0	---	unused
8:0	gb_ram_addr	table address in RAM for samples of the G_B color component. Will be automatically incremented by each read or write access to the table.
Note: MKOE tbc: Orignial register mode was rwh which is no longer supported with new version of SIG-> rwhh Table set 0 access by SW at table address 0...153. Table set 1 access at table address 154...307.		

Register: ISP_LSC_R_TABLE_DATA

Sample table red Reset value: 0000'0000H

Address: ISP_LSC_BASE + 0014H		Mode : rw
Bits	**Name**	**Description**
31:24	---	unused
23:12	r_sample_1	correction factor at sample point (fixed point number: 2 bits integer with 10-bit fractional part, range 1..3.999)

Sample table red Reset value: 0000'0000H

Address: ISP_LSC_BASE + 0014H		Mode : rw
Bits	**Name**	**Description**
11:0	r_sample_0	correction factor at sample point (fixed point number: 2 bits integer with 10-bit fractional part, range 1..3.999)
Note: The programmed sample value is immediately written into the RAM. The RAM address is generated per auto-increment. The parameter RAMs for Lens Shade Correction and Bad Pixel Correction can only be programmed, if the RGB Bayer path is switched on via ISP_CTRL register (ISP_MODE bits). Table set 0 access by SW at table address 0...153. Table set 1 access at table address		

Register: ISP_LSC_GR_TABLE_DATA

Sample table green (red) Reset value: 0000'0000H

Address: ISP_LSC_BASE + 0018H		Mode : rw
Bits	**Name**	**Description**
31:24	---	unused
23:12	gr_sample_1	correction factor at sample point (fixed point number: 2 bits integer with 10-bit fractional part, range 1..3.999)
11:0	gr_sample_0	correction factor at sample point (fixed point number: 2 bits integer with 10-bit fractional part, range 1..3.999)
Note: The programmed sample value is immediately written into the RAM. The RAM address is generated per auto-increment. The parameter RAMs for Lens Shade Correction and Bad Pixel Correction can only be programmed, if the RGB Bayer path is switched on via ISP_CTRL register (ISP_MODE bits). Table set 0 access by SW at table address 0...153. Table set 1 access at table address		

Register: ISP_LSC_B_TABLE_DATA

Sample table blue Reset value: 0000'0000H

Address: ISP_LSC_BASE + 001CH		Mode : rw
Bits	**Name**	**Description**
31:24	---	unused

23:12	b_sample_1	correction factor at sample point (fixed point number: 2 bits integer with 10-bit fractional part, range 1..3.999)
11:0	b_sample_0	correction factor at sample point (fixed point number: 2 bits integer with 10-bit fractional part, range 1..3.999)
Note: The programmed sample value is immediately written into the RAM. The RAM address is generated per auto-increment. The parameter RAMs for Lens Shade Correction and Bad Pixel Correction can only be programmed, if the RGB Bayer path is switched on via ISP_CTRL register (ISP_MODE bits). Table set 0 access by SW at table address 0...153. Table set 1 access at table address		

Register: ISP_LSC_GB_TABLE_DATA

Sample table green (blue) Reset value: 0000'0000H

Address: ISP_LSC_BASE + 0020H		**Mode : rw**
Bits	**Name**	**Description**
31:24	---	unused
23:12	gb_sample_1	correction factor at sample point (fixed point number: 2 bits integer with 10-bit fractional part, range 1..3.999)
11:0	gb_sample_0	correction factor at sample point (fixed point number: 2 bits integer with 10-bit fractional part, range 1..3.999)
Note: The programmed sample value is immediately written into the RAM. The RAM address is generated per auto-increment. The parameter RAMs for Lens Shade Correction and Bad Pixel Correction can only be programmed, if the RGB Bayer path is switched on via ISP_CTRL register (ISP_MODE bits).Table set 0 access by SW at table address 0...153. Table set 1 access at table address 154...307.		

Register: ISP_LSC_XGRAD_01

Gradient table x Reset value: 0000'0000H

Address: ISP_LSC_BASE + 0024H		**Mode : rw**
Bits	**Name**	**Description**
31:28	---	unused
27:16	xgrad_1	factor for x-gradient calculation of sector 1
15:12	---	unused

Gradient table x Reset value: 0000'0000H

Address: ISP_LSC_BASE + 0024H		**Mode : rw**
Bits	**Name**	**Description**
11:0	xgrad_0	factor for x-gradient calculation of sector 0

Register: ISP_LSC_XGRAD_23

Gradient table x Reset value: 0000'0000H

Address: ISP_LSC_BASE + 0028H			Mode : rw
Bits	Name	Description	
31:28	---	unused	
27:16	xgrad_3	factor for x-gradient calculation of sector 3	
15:12	---	unused	
11:0	xgrad_2	factor for x-gradient calculation of sector 2	

Register: ISP_LSC_XGRAD_45

Gradient table x Reset value: 0000'0000H

Address: ISP_LSC_BASE + 002CH			Mode : rw
Bits	Name	Description	
31:28	---	unused	
27:16	xgrad_5	factor for x-gradient calculation of sector 5	
15:12	---	unused	
11:0	xgrad_4	factor for x-gradient calculation of sector 4	

Register: ISP_LSC_XGRAD_67

Gradient table x Reset value: 0000'0000H

Address: ISP_LSC_BASE + 0030H			Mode : rw
Bits	Name	Description	
31:28	---	unused	
27:16	xgrad_7	factor for x-gradient calculation of sector 7	
15:12	---	unused	
11:0	xgrad_6	factor for x-gradient calculation of sector 6	

Register: ISP_LSC_YGRAD_01

Gradient table y Reset value: 0000'0000H

Address: ISP_LSC_BASE + 0034H			Mode : rw
Bits	Name	Description	
31:28	---	unused	
27:16	ygrad_1	factor for y-gradient calculation of sector 1	
15:12	---	unused	
11:0	ygrad_0	factor for y-gradient calculation of sector 0	

Register: ISP_LSC_YGRAD_23

Gradient table y Reset value: 0000'0000H

Address: ISP_LSC_BASE + 0038H			Mode : rw
Bits	**Name**	**Description**	
31:28	---	unused	
27:16	ygrad_3	factor for y-gradient calculation of sector 3	
15:12	---	unused	
11:0	ygrad_2	factor for y-gradient calculation of sector 2	

Register: ISP_LSC_YGRAD_45

Gradient table y Reset value: 0000'0000H

Address: ISP_LSC_BASE + 003CH			Mode : rw
Bits	**Name**	**Description**	
31:28	---	unused	
27:16	ygrad_5	factor for y-gradient calculation of sector 5	
15:12	---	unused	

Gradient table y Reset value: 0000'0000H

Address: ISP_LSC_BASE + 003CH		Mode : rw
Bits	**Name**	**Description**
11:0	ygrad_4	factor for y-gradient calculation of sector 4

Register: ISP_LSC_YGRAD_67

Gradient table y Reset value: 0000'0000H

Address: ISP_LSC_BASE + 0040H		Mode : rw
Bits	**Name**	**Description**
31:28	---	unused
27:16	ygrad_7	factor for y-gradient calculation of sector 7
15:12	---	unused
11:0	ygrad_6	factor for y-gradient calculation of sector 6

Register: ISP_LSC_XSIZE_01

Size table Reset value: 0000'0000H

Address: ISP_LSC_BASE + 0044H		Mode : rw
Bits	**Name**	**Description**
31:26	---	unused
25:16	x_sect_size_1	sector size 1 in x-direction
15:10	---	unused
9:0	x_sect_size_0	sector size 0 in x-direction
Note: The sector size in x-direction must be greater than 12 pixels. The sum of the sector sizes in x- direction must be "picture width / 2". The sum of the sector sizes in y-direction must be "picture height / 2". No interrupt is generated if above requirements are not fulfilled and the behaviour of the hardware cannot be predicted. The sector size in x-direction was defined to be 9 bits for preliminary ISP versions.		

Register: ISP_LSC_XSIZE_23

Size table **Reset value: 0000'0000H**

Address: ISP_LSC_BASE + 0048H		**Mode : rw**
Bits	**Name**	**Description**
31:26	---	unused
25:16	x_sect_size_3	sector size 3 in x-direction
15:10	---	unused
9:0	x_sect_size_2	sector size 2 in x-direction
Note: minimum sector size is 10 in x direction		

Register: ISP_LSC_XSIZE_45

Size table **Reset value: 0000'0000H**

Address: ISP_LSC_BASE + 004CH		**Mode : rw**
Bits	**Name**	**Description**
31:26	---	unused
25:16	x_sect_size_5	sector size 5 in x-direction
15:10	---	unused
9:0	x_sect_size_4	sector size 4in x-direction
Note: minimum sector size is 10 in x direction		

Register: ISP_LSC_XSIZE_67

Size table **Reset value: 0000'0000H**

Address: ISP_LSC_BASE + 0050H		**Mode : rw**
Bits	**Name**	**Description**
31:26	---	unused
25:16	x_sect_size_7	sector size 7 in x-direction
15:10	---	unused
9:0	x_sect_size_6	sector size 6 in x-direction
Note: minimum sector size is 10 in x direction		

Register: ISP_LSC_YSIZE_01

Size table **Reset value: 0000'0000H**

Address: ISP_LSC_BASE + 0054H		**Mode : rw**
Bits	**Name**	**Description**
31:26	---	unused
25:16	y_sect_size_1	sector size 1 in y-direction
15:10	---	unused
9:0	y_sect_size_0	sector size 0 in y-direction
Note: minimum sector size is 8 in y direction. The sector size in y-direction was defined to be 9 bits for preliminary ISP versions.		

Register: ISP_LSC_YSIZE_23

Size table **Reset value: 0000'0000H**

Address: ISP_LSC_BASE + 0058H		**Mode : rw**
Bits	**Name**	**Description**
31:26	---	unused
25:16	y_sect_size_3	sector size 3 in y-direction
15:10	---	unused
9:0	y_sect_size_2	sector size 2 in y-direction
Note: minimum sector size is 8 in y direction		

Register: ISP_LSC_YSIZE_45

Size table **Reset value: 0000'0000H**

Address: ISP_LSC_BASE + 005CH		**Mode : rw**
Bits	**Name**	**Description**
31:26	---	unused
25:16	y_sect_size_5	sector size 5 in y-direction
15:10	---	unused
9:0	y_sect_size_4	sector size 4 in y-direction
Note: minimum sector size is 8 in y direction		

Register: ISP_LSC_YSIZE_67

Size table Reset value: 0000'0000H

Address: ISP_LSC_BASE + 0060H		**Mode : rw**
Bits	**Name**	**Description**
31:26	---	unused
25:16	y_sect_size_7	sector size 7 in y-direction
15:10	---	unused
9:0	y_sect_size_6	sector size 6 in y-direction
Note: minimum sector size is 8 in y direction		

Register: ISP_LSC_TABLE_SEL

Lens shade table set selection Reset value: 0000'0000H

Address: ISP_LSC_BASE + 0064H		**Mode : rw**
Bits	**Name**	**Description**
31:1	---	unused
0	table_sel	0: next active tables set is table set 0. 1: next active tables set is table set 1. Table selection is object of a shadowing mechnism.
Note: Table set 0 access by SW at table address 0...153. Table set 1 access at table address 154...307. For LSC4_MSZ the table set 1 is physically not available: ISP_LSC_TABLE_SEL shall always be 0 for this HW configuration.		

Register: ISP_LSC_STATUS

Lens shade status Reset value: 0000'0000H

Address: ISP_LSC_BASE + 0068H		**Mode : r**
Bits	**Name**	**Description**
31:2	---	unused
1	active_table	0: currently active tables set is table set 0 1: currently active tables
0	lsc_en_status	0: lens shading correction is currently off 1: lens shading

Register: ISP_IS_CTRL

Image Stabilization Control Register Reset value: 0000'0000H

Address: ISP_IS_BASE + 0000H			Mode : rw
Bits	**Name**	**Description**	
31:1	---	unused	
0	is_en	1: image stabilization switched on 0: image stabilization switched off	

Register: ISP_IS_RECENTER
Recenter register Reset value: 0000'0000H

Address: ISP_IS_BASE + 0004H			Mode : rw
Bits	**Name**	**Description**	
31:3	---	unused	
2:0	is_recenter	000: recenter feature switched off 1..7: recentering by (new_h/v_offs-H/V_OFFS)/2^RECENTER	

Register: ISP_IS_H_OFFS

Horizontal offset of output window Reset value: 0000'0000H

Address: ISP_IS_BASE + 0008H			Mode : rw
Bits	**Name**	**Description**	
31:14	---	unused	
13:0	is_h_offs	horizontal picture offset in pixel	

Register: ISP_IS_V_OFFS

Vertical offset of output window Reset value: 0000'0000H

Address: ISP_IS_BASE + 000CH			Mode : rw
Bits	**Name**	**Description**	
31:14	---	unused	
13:0	is_v_offs	vertical picture offset in lines	

Register: ISP_IS_H_SIZE

Output horizontal picture size Reset value: 0000'1000H

Address: ISP_IS_BASE + 0010H			Mode : rw
Bits	Name	Description	
31:14	---	unused	
13:0	is_h_size	horizontal picture size in pixel if ISP_MODE is set to 001-(ITU-R BT.656 YUV), 010-(ITU-R BT.601 YUV), 011-(ITU-R BT.601 Bayer RGB), 101-(ITU-R BT.656 Bayer RGB) only even numbers are accepted, because complete quadruples of YUYV(YCbYCr) are needed for the following modules. If an odd size is programmed the value will be truncated to even size.	

Register: ISP_IS_V_SIZE

Output vertical picture size Reset value: 0000'0C00H

Address: ISP_IS_BASE + 0014H			Mode : rw
Bits	Name	Description	
31:14	---	unused	
13:0	is_v_size	vertical picture size in lines	

Register: ISP_IS_MAX_DX

Maximum Horizontal Displacement Reset value: 0000'0000H

Address: ISP_IS_BASE + 0018H			Mode : rw
Bits	Name	Description	
31:12	---	unused	
12:0	is_max_dx	maximum allowed accumulated horizontal displacement in pixels	

Register: ISP_IS_MAX_DY

Maximum Vertical Displacement Reset value: 0000'0000H

Address: ISP_IS_BASE + 001CH			Mode : rw
Bits	Name	Description	
31:12	---	unused	
12:0	is_max_dy	maximum allowed accumulated vertical displacement in lines	

Register: ISP_IS_DISPLACE

Camera displacement Reset value: 0000'0000H

Address: ISP_IS_BASE + 0020H		Mode : rw
Bits	**Name**	**Description**
31:30	---	unused
28:16	dy	ISP_IS will compensate for vertical camera displacement of DY lines in the next frame
15:13	---	unused
12:0	dx	ISP_IS will compensate for horizontal camera displacement of DX pixels in the next frame

Register: ISP_IS_H_OFFS_SHD

current horizontal offset of output window (shadow register) Reset value: 0000'0000H

Address: ISP_IS_BASE + 0024H		Mode : r
Bits	**Name**	**Description**
31:14	---	unused
13:0	is_h_offs_shd	current horizonatl picture offset in lines

Register: ISP_IS_V_OFFS_SHD

current vertical offset of output window (shadow register) Reset value: 0000'0000H

Address: ISP_IS_BASE + 0028H		Mode : r
Bits	**Name**	**Description**
31:14	---	unused
13:0	is_v_offs_shd	current vertical picture offset in lines

Register: ISP_IS_H_SIZE_SHD

current output horizontal picture size (shadow register) Reset value: 0000'0000H

Address: ISP_IS_BASE + 002CH		Mode : r
Bits	**Name**	**Description**
31:14	---	unused
13:0	isp_h_size_shd	current horizontal picture size in pixel

Register: ISP_IS_V_SIZE_SHD

current output vertical picture size (shadow register) Reset value: 0000'0000H

Address: ISP_IS_BASE + 0030H		Mode : r
Bits	**Name**	**Description**
31:14	---	unused
13:0	isp_v_size_shd	vertical picture size in lines

Register: ISP_HIST_PROP

Histogram properties **Reset value: 0000'0000H**

Address: ISP_HIST_BASE + 0000H		Mode : rw
Bits	**Name**	**Description**
31:10	---	unused
9:3	stepsize	histogram predivider, process every (stepsize)th pixel, all other pixels are skipped 0,1,2: not allowed 3: process every third input pixel 4: process every fourth input pixel ... 7FH: process every 127th pixel
2:0	hist_mode	histogram mode, luminance is taken at ISP output before output formatter, RGB is taken at xtalk output 7, 6: must not be used 5: Y (luminance) histogram 4: B histogram 3: G histogram 2: R histogram 1: RGB combined histogram 0: disable, no measurements
Note: If RGB combined mode is used, then the 3 color components are sampled one after the other. The software has to assure that all 3 color components are inside the selected window.		

Register: ISP_HIST_H_OFFS

Histogram window horizontal offset for first window of 25 sub- windows **Reset value: 0000'0000H**

Address: ISP_HIST_BASE + 0004H		Mode : rw
Bits	**Name**	**Description**
31:13	---	unused
12:0	hist_h_offset	Horizontal offset of first window in pixels.
Note: histogram measurement is done in 25 sub-windows like the exposure measurement, if histogram version 3 is implemented. All earlier versions use just one window.		

Register: ISP_HIST_V_OFFS

Histogram window vertical offset for first window of 25 sub-windows Reset value: 0000'0000H

Address: ISP_HIST_BASE + 0008H		Mode : rw
Bits	**Name**	**Description**
31:13	---	unused
12:0	hist_v_offset	Vertical offset of first window in pixels.
Note: histogram measurement is done in 25 sub-windows like the exposure measurement, if histogram version 3 is implemented. All earlier versions use just one window.		

Register: ISP_HIST_H_SIZE

Horizontal (sub-)window size Reset value: 0000'0000H

Address: ISP_HIST_BASE + 000CH		Mode : rw
Bits	**Name**	**Description**
31:11	---	unused
10:0	hist_h_size	Horizontal size in pixels of one sub-window, if histogram version 3 is implemented.
Note: hist_h_offset + hist_h_size x 5 should be less than or equal to the horizontal size of the picture, if histogram version 3 is implemented. Otherwise hist_h_size is the horizontal size of the measurement window in pixels.		

Register: ISP_HIST_V_SIZE

Vertical (sub-)window size Reset value: 0000'0000H

Address: ISP_HIST_BASE + 0010H		Mode : rw
Bits	**Name**	**Description**
31:11	---	unused
10:0	hist_v_size	Vertical size in lines of one sub-window, if histogram version 3 is implemented.

Note: hist_v_offset + hist_v_size x 5 should be less than or equal to the vertical size of the picture, if histogram version 3 is implemented. Otherwise hist_v_size is the vertical size of the measurement window in lines.

Register: ISP_HIST_BIN

histogram measurement result bin n (n=0..15) **Reset value: 0000'0000H**

Address: ISP_HIST_BASE + 014H + (4H * n)		**Mode : r**
Bits	**Name**	**Description**
31:20	---	unused
19:0	hist_bin_n	measured bin count as 16-bit unsigned integer value plus 4 bit fractional part
Note: MKOE tbc: Orignial register mode was rh which is no longer supported with new version of SIG -> r		

Register: ISP_HIST_WEIGHT_00TO30

Weighting factor for sub-windows **Reset value: 1010'1010H**

Address: ISP_HIST_BASE + 0054H		**Mode : rw**
Bits	**Name**	**Description**
31:29	---	unused
28:24	hist_weight_30	weighting factor for sub-window 30
23:21	---	unused
20:16	hist_weight_20	weighting factor for sub-window 20
15:13	---	unused
12:8	hist_weight_10	weighting factor for sub-window 10
7:5	---	unused
4:0	hist_weight_00	weighting factor for sub-window 00
Note: Allowed value range for weight factor is 0 to 16. The resulting weight is register_value / 16. The host software has to limit the register value for each factor to 16. Weight registers are available, if histogram version 3 is implemented.		

Register: ISP_HIST_WEIGHT_40TO21
Weighting factor for sub-windows **Reset value: 1010'1010H**

Address: ISP_HIST_BASE + 0058H		**Mode : rw**
Bits	**Name**	**Description**
31:29	---	unused
28:24	hist_weight_21	weighting factor for sub-window 21

Address: ISP_HIST_BASE + 0058H		Mode : rw
Bits	**Name**	**Description**
23:21	---	unused
20:16	hist_weight_11	weighting factor for sub-window 11
15:13	---	unused
12:8	hist_weight_01	weighting factor for sub-window 01
7:5	---	unused
4:0	hist_weight_40	weighting factor for sub-window 40
Note: Allowed value range for weight factor is 0 to 16. The resulting weight is register_value / 16. The host software has to limit the register value for each factor to 16. Weight registers are available, if histogram version 3 is implemented.		

Register: ISP_HIST_WEIGHT_31TO12

Weighting factor for sub-windows Reset value: 1010'1010H

Address: ISP_HIST_BASE + 005CH		Mode : rw
Bits	**Name**	**Description**
31:30	---	unused
28:24	hist_weight_12	weighting factor for sub-window 12
23:21	---	unused
20:16	hist_weight_02	weighting factor for sub-window 02
15:13	---	unused
12:8	hist_weight_41	weighting factor for sub-window 41
7:5	---	unused
4:0	hist_weight_31	weighting factor for sub-window 31
Note: Allowed value range for weight factor is 0 to 16. The resulting weight is register_value / 16. The host software has to limit the register value for each factor to 16. Weight registers are available, if histogram version 3 is implemented.		

Register: ISP_HIST_WEIGHT_22TO03
Weighting factor for sub-windows Reset value: 1010'1010H

Address: ISP_HIST_BASE + 0060H		Mode : rw
Bits	**Name**	**Description**
31:30	---	unused
28:24	hist_weight_03	weighting factor for sub-window 03
23:21	---	unused
20:16	hist_weight_42	weighting factor for sub-window 42

Address: ISP_HIST_BASE + 0060H		Mode : rw
Bits	**Name**	**Description**
15:13	---	unused
12:8	hist_weight_32	weighting factor for sub-window 32
7:5	---	unused
4:0	hist_weight_22	weighting factor for sub-window 22
Note: Allowed value range for weight factor is 0 to 16. The resulting weight is register_value / 16. The host software has to limit the register value for each factor to 16. Weight registers are available, if histogram version 3 is implemented.		

Register: ISP_HIST_WEIGHT_13TO43

Weighting factor for sub-windows Reset value: 1010'1010H

Address: ISP_HIST_BASE + 0064H		Mode : rw
Bits	**Name**	**Description**
31:29	---	unused
28:24	hist_weight_43	weighting factor for sub-window 43
23:21	---	unused
20:16	hist_weight_33	weighting factor for sub-window 33
15:13	---	unused
12:8	hist_weight_23	weighting factor for sub-window 23
7:5	---	unused
4:0	hist_weight_13	weighting factor for sub-window 13
Note: Allowed value range for weight factor is 0 to 16. The resulting weight is register_value / 16. The host software has to limit the register value for each factor to 16. Weight registers are available, if histogram version 3 is implemented.		

Register: ISP_HIST_WEIGHT_04TO34
Weighting factor for sub-windows Reset value: 1010'1010H

Address: ISP_HIST_BASE + 0068H		Mode : rw
Bits	**Name**	**Description**
31:29	---	unused
28:24	hist_weight_34	weighting factor for sub-window 34
23:21	---	unused
20:16	hist_weight_24	weighting factor for sub-window 24
15:13	---	unused
12:8	hist_weight_14	weighting factor for sub-window 14

Address: ISP_HIST_BASE + 0068H		Mode : rw
Bits	**Name**	**Description**
7:5	---	unused
4:0	hist_weight_04	weighting factor for sub-window 04
Note: Allowed value range for weight factor is 0 to 16. The resulting weight is register_value / 16. The host software has to limit the register value for each factor to 16. Weight registers are available, if histogram version 3 is implemented.		

Register: ISP_HIST_WEIGHT_44

Weighting factor for sub-windows Reset value: 0000'0010H

Address: ISP_HIST_BASE + 006CH		Mode : rw
Bits	**Name**	**Description**
31:5	---	unused
4:0	hist_weight_44	weighting factor for sub-window 44
Note: Allowed value range for weight factor is 0 to 16. The resulting weight is register_value / 16. The host software has to limit the register value for each factor to 16. Weight registers are available, if histogram version 3 is implemented.		

Register: ISP_FILT_MODE
mode control register for the filter block Reset value: 0000'04F2H

Address: ISP_FILT_BASE + 0000H		Mode : rw
Bits	**Name**	**Description**
31:12	---	unused
11:8	stage1_select	Green filter stage 1 select (range 0x0...0x8) 0x0 maximum blurring 0x4 Default 0x7 minimum blurring 0x8 filter stage1 bypass For a detailed description refer to chapter "ISP Filter Programming" of user manual
7:6	filt_chr_h_mode	Chroma filter horizontal mode 00 horizontal chroma filter bypass 01 horizontal chroma filter 1 static mask = [10 12 10] 10 horizontal chroma filter 2 (dynamic blur1) 11 horizontal chroma filter 3 (dynamic blur2) Default
5:4	filt_chr_v_mode	Chroma filter vertical mode vertical chroma filter bypass vertical chroma filter 1 static [8 16 8] vertical chroma filter 2 static [10 12 10] vertical chroma filter 3 static [12 8 12] Default
3:2	---	unused
1	filt_mode	0 green filter static mode (active filter factor = FILT_FAC_MID) 1 dynamic noise reduction/sharpen Default

Address: ISP_FILT_BASE + 0000H		Mode : rw
Bits	**Name**	**Description**
0	filt_enable	1 enable filter 0 bypass filter Default

Register: ISP_FILT_THRESH_BL0

Blurring threshold 0 Reset value: 0000'000DH

Address: ISP_FILT_BASE + 0028H		Mode : rw
Bits	**Name**	**Description**
31:10	---	unused
9:0	filt_thresh_bl0	If filt_thresh_bl1 < sum_grad < filt_thresh_bl0 then filt_fac_bl0 is selected
Note: sum_grad is calculated by the texture detection unit as the sum of horizontal and vertical gradients		

Register: ISP_FILT_THRESH_BL1
Blurring threshold 1 Reset value: 0000'0005H

Address: ISP_FILT_BASE + 002CH		Mode : rw
Bits	**Name**	**Description**
31:10	---	unused
9:0	filt_thresh_bl1	If sum_grad < filt_thresh_bl1 then filt_fac_bl1 is selected
Note: sum_grad is calculated by the texture detection unit as the sum of horizontal and vertical gradients		

Register: ISP_FILT_THRESH_SH0

Sharpening threshold 0 Reset value: 0000'001AH

Address: ISP_FILT_BASE + 0030H		Mode : rw
Bits	**Name**	**Description**
31:10	---	unused
9:0	filt_thresh_sh0	If filt_thresh_sh0 < sum_grad < filt_thresh_sh1 then filt_thresh_sh0 is selected
Note: sum_grad is calculated by the texture detection unit as the sum of horizontal and vertical gradients		

Register: ISP_FILT_THRESH_SH1

Sharpening threshold 1 Reset value: 0000'002CH

Address: ISP_FILT_BASE + 0034H		Mode : rw
Bits	**Name**	**Description**
31:10	---	unused

9:0	filt_thresh_sh1	If filt_thresh_sh1 < sum_grad then filt_thresh_sh1 is selected
Note: sum_grad is calculated by the texture detection unit as the sum of horizontal and vertical gradients		

Register: ISP_FILT_LUM_WEIGHT

Parameters for luminance weight function Reset value: 0002'2040H

Address: ISP_FILT_BASE + 0038H		**Mode : rw**
Bits	**Name**	**Description**
31:19	---	unused
18:16	lum_weight_gain	Gain select of luminance weight function
15:8	lum_weight_kink	Kink position of luminance weight function
7:0	lum_weight_min	Minimum value of luminance weight function

Register: ISP_FILT_FAC_SH1

filter factor sharp1 Reset value: 0000'0010H

Address: ISP_FILT_BASE + 003CH		**Mode : rw**
Bits	**Name**	**Description**
31:6	---	unused
5:0	filt_fac_sh1	Filter factor for sharp1 level

Register: ISP_FILT_FAC_SH0

filter factor sharp0 Reset value: 0000'000CH

Address: ISP_FILT_BASE + 0040H		**Mode : rw**
Bits	**Name**	**Description**
31:6	---	unused

filter factor sharp0 Reset value: 0000'000CH

Address: ISP_FILT_BASE + 0040H		Mode : rw
Bits	**Name**	**Description**
5:0	filt_fac_sh0	Filter factor for sharp0 level

Register: ISP_FILT_FAC_MID

filter factor middle Reset value: 0000'000AH

Address: ISP_FILT_BASE + 0044H		Mode : rw
Bits	**Name**	**Description**
31:6	---	unused
5:0	filt_fac_mid	Filter factor for mid level and for static filter mode

Register: ISP_FILT_FAC_BL0

Parameter for blur 0 filter Reset value: 0000'0006H

Address: ISP_FILT_BASE + 0048H		Mode : rw
Bits	**Name**	**Description**
31:6	---	unused
5:0	filt_fac_bl0	Filter factor for blur 0 level

Register: ISP_FILT_FAC_BL1

Parameter for blur 1 filter Reset value: 0000'0002H

Address: ISP_FILT_BASE + 004CH		Mode : rw
Bits	**Name**	**Description**
31:6	---	unused
5:0	filt_fac_bl1	Filter factor for blur 1 level (max blur)

Register: ISP_CAC_CTRL

Control register for chromatic aberration correction Reset value: 0000'0000H

Address: ISP_CAC_BASE + 0000H		**Mode : rw**
Bits	**Name**	**Description**
31:4	---	unused
3	h_clip_mode	Defines the maximum red/blue pixel shift in horizontal direction At pixel positions, that require a larger displacement, the maximum shift value is used instead (vector clipping) 0: Set horizontal vector clipping to +/-4 pixel displacement (Default) 1: Set horizontal vector clipping to +/-4 or +/-5 pixel displacement depending on pixel position inside the Bayer
2:1	v_clip_mode	Defines the maximum red/blue pixel shift in vertical direction 00: Set vertical vector clipping to +/-2 pixel ; fix filter_enable (Default) 01: Set vertical vector clipping to +/-3 pixel; dynamic filter_enable for chroma low pass filter 10: Set vertical vector clipping +/-3 or +/-4 pixel displacement depending on pixel position inside the Bayer raster (dynamic switching between +/-3 and +/-4) 11: reserved
0	cac_en	0: chromatic aberration correction off 1: chromatic aberration correction on
Note: Clipping behavior can be controlled by clip_mode bits. If no clipping occurs, because displacement is below the maximum correctable displacement, then it does not matter which mode is selected.		

Register: ISP_CAC_COUNT_START

Preload values for CAC pixel and line counter Reset value: 1000'1000H

Address: ISP_CAC_BASE + 0004H		**Mode : rw**
Bits	**Name**	**Description**
31:29	---	unused

Address: ISP_CAC_BASE + 0004H		Mode : rw
Bits	**Name**	**Description**
28:16	v_count_start	13 bit v_count preload value (range 8191 ... 1) of the vertical CAC line counter. Before frame start v_count has to be preloaded with (v_size/2 + v_center_offset), with v_size the image height and v_center_offset the vertical distance between image center and optical center. After frame start the v_count decrements with every line until a value of zero is reached for the line in the optical center. Than the v_sign bit toggles and the v_counter decrements with every line until end of frame.
15:13	---	unused
12:0	h_count_start	13 bit h_count preload value (range 8191 .. 1) of the horizontal CAC pixel counter. Before line start h_count has to be preloaded with (h_size/2 + h_center_offset), with h_size the image width and h_center_offset the horizontal distance between image center and optical center. After line start the h_count decrements with every pixel until a value of zero is reached for the column in the optical center. Than the h_sign bit toggles and the h_counter increments with every pixel until end of line.
Note: Reset value is valid for 8192 x 8192 image resolution with centered chromatic aberration (no offset from image center).		

Register: ISP_CAC_A

Linear Parameters for radial shift calculation **Reset value: 0000'0000H**

Address: ISP_CAC_BASE + 0008H		Mode : rw
Bits	**Name**	**Description**
31:25	---	unused
24:16	A_Blue	Parameter A_Blue for radial blue shift calculation, according to (A_Blue * r + B_Blue * r^2 + C_Blue * r^3). It is a 9 bit twos complement integer with 4 fractional digits value and value range from -16 up to 15.9375.
15:9	---	unused

Linear Parameters for radial shift calculation Reset value: 0000'0000H

Address: ISP_CAC_BASE + 0008H		Mode : rw
Bits	**Name**	**Description**
8:0	A_Red	Parameter A_Red for radial red shift calculation, according to (A_Red * r + B_Red * r^2 + C_Red * r^3). It is a 9 bit twos complement integer with 4 fractional digits value and value range from -16 up to 15.9375.

Register: ISP_CAC_B

Square Parameters for radial shift calculation Reset value: 0000'0000H

Address: ISP_CAC_BASE + 000CH		Mode : rw
Bits	**Name**	**Description**
31:25	---	unused
24:16	B_Blue	Parameter B_Blue for radial blue shift calculation, according to (A_Blue * r + B_Blue * r^2 + C_Blue * r^3). It is a 9 bit twos complement integer with 4 fractional digits value and value range from -16 up to 15.9375.
15:9	---	unused
8:0	B_Red	Parameter B_Red for radial red shift calculation, according to (A_Red * r + B_Red * r^2 + C_Red * r^3). It is a 9 bit twos complement integer with 4 fractional digits value and value range from -16 up to 15.9375.

Register: ISP_CAC_C

Cubical Parameters for radial shift calculation Reset value: 0000'0000H

Address: ISP_CAC_BASE + 0010H		Mode : rw
Bits	**Name**	**Description**
31:25	---	unused
24:16	C_Blue	Parameter C_Blue for radial blue shift calculation, according to (A_Blue * r + B_Blue * r^2 + C_Blue * r^3). It is a 9 bit twos complement integer with 4 fractional digits value and value range from -16 up to 15.9375.
15:9	---	unused

Cubical Parameters for radial shift calculation **Reset value: 0000'0000H**

Address: ISP_CAC_BASE + 0010H		**Mode : rw**
Bits	**Name**	**Description**
8:0	C_Red	Parameter C_Red for radial red shift calculation, according to (A_Red * r + B_Red * r^2 + C_Red * r^3). It is a 9 bit twos complement integer with 4 fractional digits value and value range from -16 up to 15.9375.

Register: ISP_CAC_X_NORM

Normalization parameters for calculation of image coordinate x_d relative to optical center **Reset value: 0008'0010H**

Address: ISP_CAC_BASE + 0014H		**Mode : rw**
Bits	**Name**	**Description**
31:20	---	unused
19:16	x_ns	Horizontal normalization shift parameter x_ns (4 bit unsigned integer) in equation x_d[7:0] = (((h_count << 4) >> x_ns) * x_nf) >> 5
15:5	---	unused
4:0	x_nf	Horizontal scaling or normalization factor x_nf (5 bit unsigned integer) range 0 .. 31 in equation x_d[7:0] = (((h_count << 4) >> x_ns) * x_nf) >> 5
Note: These values need to be programmed according to the image resolution and the center offset of the chromatic aberration. The parameters are necessary to avoid high gate count of the CAC hardware block. The reset value is valid for an image resolution of 2600 x 1950 and center offset 0.		

Register: ISP_CAC_Y_NORM

Normalization parameters for calculation of image coordinate y_d relative to optical center **Reset value: 0008'0010H**

Address: ISP_CAC_BASE + 0018H		**Mode : rw**
Bits	**Name**	**Description**
31:20	---	unused
19:16	y_ns	Vertical normalization shift parameter y_ns (4 bit unsigned integer) in equation y_d[7:0] = (((v_count << 4) >> y_ns) * y_nf) >> 5

Normalization parameters for calculation of image coordinate y_d relative to optical center **Reset value: 0008'0010H**

Address: ISP_CAC_BASE + 0018H		Mode : rw
Bits	**Name**	**Description**
15:5	---	unused
4:0	y_nf	Vertical scaling or normalization factor y_nf (5 bit unsigned integer) range 0 .. 31 in equation y_d[7:0] = (((v_count << 4) >> y_ns) * y_nf) >> 5
Note: These values need to be programmed according to the image resolution and the center offset of the chromatic aberration. The parameters are necessary to avoid high gate count of the CAC hardware block. The reset value is valid for an image resolution of 2600 x 1950 and center offset 0.		

Register: ISP_EXP_CTRL

Exposure control **Reset value: 0000'0000H**

Address: ISP_AE_BASE + 0000H		Mode : rw
Bits	**Name**	**Description**
31	exp_meas_mode	'1' luminance calculation according to Y=(R+G+B) x 0.332 (85/256) '0' luminance calculation according to Y=16+0.25R+0.5G+0.1094B
30:2	---	unused
1	autostop	'1' stop measuring after a complete frame '0' continous measurement
0	exp_start	'1' start measuring a frame. The exp block will reset this bit and halt after completing one frame, if bit "autostop" is set to '1'.

Register: ISP_EXP_H_OFFSET

Horizontal offset for first block **Reset value: 0000'0000H**

Address: ISP_AE_BASE + 0004H		Mode : rw
Bits	**Name**	**Description**
31:13	---	unused
12:0	isp_exp_h_offset	Horizontal offset of first block in pixels. 0 <= value <= 2424

Register: ISP_EXP_V_OFFSET

Vertical offset for first block Reset value: 0000'0000H

Address: ISP_AE_BASE + 0008H			**Mode : rw**
Bits	**Name**	**Description**	
31:12	---	unused	
12:0	isp_exp_v_offset	Vertical offset of first block in pixels. 0 <= value <= 1806	

Register: ISP_EXP_H_SIZE
Horizontal size of one block Reset value: 0000'0000H

Address: ISP_AE_BASE + 000CH			**Mode : rw**
Bits	**Name**	**Description**	
31:11	---	unused	
10:0	isp_exp_h_size	Horizontal size in pixels of one block. 35 <= value <= 516	
Note: exp_h_size x 5 must be less (not equal) than the horizontal size of the picture			

Register: ISP_EXP_V_SIZE

Vertical size of one block Reset value: 0000'0000H

Address: ISP_AE_BASE + 0010H			**Mode : rw**
Bits	**Name**	**Description**	
31:11	---	unused	
10:0	isp_exp_v_size	Vertical size in pixels of one block. 28 <= value <= 390	
Note: The vertical size must be set in a way that after the last measurement window at least two lines of the image will follow. In addition only even values for vertical size are allowed (vertical size must be a multiple of 2).			

Register: ISP_EXP_MEAN_00

Mean luminance value of block 00 Reset value: 0000'0000H

Address: ISP_AE_BASE + 0014H			Mode : r
Bits	**Name**	**Description**	
31:8	---	unused	
7:0	isp_exp_mean_00	Mean luminance value of block 00 (x,y)	

Register: ISP_EXP_MEAN_10

Mean luminance value of block 10 Reset value: 0000'0000H

Address: ISP_AE_BASE + 0018H			Mode : r
Bits	**Name**	**Description**	
31:8	---	unused	
7:0	isp_exp_mean_10	Mean luminance value of block 10 (x,y)	

Register: ISP_EXP_MEAN_20

Mean luminance value of block 20 Reset value: 0000'0000H

Address: ISP_AE_BASE + 001CH			Mode : r
Bits	**Name**	**Description**	
31:8	---	unused	
7:0	isp_exp_mean_20	Mean luminance value of block 20 (x,y)	

Register: ISP_EXP_MEAN_30

Mean luminance value of block 30 Reset value: 0000'0000H

Address: ISP_AE_BASE + 0020H			Mode : r
Bits	**Name**	**Description**	
31:8	---	unused	
7:0	isp_exp_mean_30	Mean luminance value of block 30 (x,y)	

Register: ISP_EXP_MEAN_40

Mean luminance value of block 40 Reset value: 0000'0000H

Address: ISP_AE_BASE + 0024H			Mode : r
Bits	**Name**	**Description**	
31:8	---	unused	
7:0	isp_exp_mean_40	Mean luminance value of block 40 (x,y)	

Register: ISP_EXP_MEAN_01

Mean luminance value of block 01 Reset value: 0000'0000H

Address: ISP_AE_BASE + 0028H			Mode : r
Bits	**Name**	**Description**	
31:8	---	unused	
7:0	isp_exp_mean_01	Mean luminance value of block 01 (x,y)	

Register: ISP_EXP_MEAN_11

Mean luminance value of block 11 Reset value: 0000'0000H

Address: ISP_AE_BASE + 002CH			Mode : r
Bits	**Name**	**Description**	
31:8	---	unused	
7:0	isp_exp_mean_11	Mean luminance value of block 11 (x,y)	

Register: ISP_EXP_MEAN_21

Mean luminance value of block 21 Reset value: 0000'0000H

Address: ISP_AE_BASE + 0030H			Mode : r
Bits	**Name**	**Description**	
31:8	---	unused	
7:0	isp_exp_mean_21	Mean luminance value of block 21 (x,y)	

Register: ISP_EXP_MEAN_31

Mean luminance value of block 31 Reset value: 0000'0000H

Address: ISP_AE_BASE + 0034H			Mode : r
Bits	**Name**	**Description**	
31:8	---	unused	
7:0	isp_exp_mean_31	Mean luminance value of block 31 (x,y)	

Register: ISP_EXP_MEAN_41

Mean luminance value of block 41 Reset value: 0000'0000H

Address: ISP_AE_BASE + 0038H			Mode : r
Bits	**Name**	**Description**	
31:8	---	unused	
7:0	isp_exp_mean_41	Mean luminance value of block 41 (x,y)	

Register: ISP_EXP_MEAN_02

Mean luminance value of block 02 Reset value: 0000'0000H

Address: ISP_AE_BASE + 003CH			Mode : r
Bits	**Name**	**Description**	
31:8	---	unused	
7:0	isp_exp_mean_02	Mean luminance value of block 02 (x,y)	

Register: ISP_EXP_MEAN_12

Mean luminance value of block 12 Reset value: 0000'0000H

Address: ISP_AE_BASE + 0040H			Mode : r
Bits	**Name**	**Description**	
31:8	---	unused	
7:0	isp_exp_mean_12	Mean luminance value of block 12 (x,y)	

Register: ISP_EXP_MEAN_22

Mean luminance value of block 22 Reset value: 0000'0000H

Address: ISP_AE_BASE + 0044H		Mode : r
Bits	**Name**	**Description**
31:8	---	unused
7:0	isp_exp_mean_22	Mean luminance value of block 22 (x,y)

Register: ISP_EXP_MEAN_32

Mean luminance value of block 32 Reset value: 0000'0000H

Address: ISP_AE_BASE + 0048H		Mode : r
Bits	**Name**	**Description**
31:8	---	unused
7:0	isp_exp_mean_32	Mean luminance value of block 32 (x,y)

Register: ISP_EXP_MEAN_42

Mean luminance value of block 42 Reset value: 0000'0000H

Address: ISP_AE_BASE + 004CH		Mode : r
Bits	**Name**	**Description**
31:8	---	unused
7:0	isp_exp_mean_42	Mean luminance value of block 42 (x,y)

Register: ISP_EXP_MEAN_03

Mean luminance value of block 03 Reset value: 0000'0000H

Address: ISP_AE_BASE + 0050H		Mode : r
Bits	**Name**	**Description**
31:8	---	unused
7:0	isp_exp_mean_03	Mean luminance value of block 03 (x,y)

Register: ISP_EXP_MEAN_13

Mean luminance value of block 13 Reset value: 0000'0000H

Address: ISP_AE_BASE + 0054H		Mode : r
Bits	**Name**	**Description**
31:8	---	unused
7:0	isp_exp_mean_13	Mean luminance value of block 13 (x,y)

Register: ISP_EXP_MEAN_23

Mean luminance value of block 23 Reset value: 0000'0000H

Address: ISP_AE_BASE + 0058H		Mode : r
Bits	**Name**	**Description**
31:8	---	unused
7:0	isp_exp_mean_23	Mean luminance value of block 23 (x,y)

Register: ISP_EXP_MEAN_33

Mean luminance value of block 33 Reset value: 0000'0000H

Address: ISP_AE_BASE + 005CH		Mode : r
Bits	**Name**	**Description**
31:8	---	unused
7:0	isp_exp_mean_33	Mean luminance value of block 33 (x,y)

Register: ISP_EXP_MEAN_43

Mean luminance value of block 43 Reset value: 0000'0000H

Address: ISP_AE_BASE + 0060H		Mode : r
Bits	**Name**	**Description**
31:8	---	unused
7:0	isp_exp_mean_43	Mean luminance value of block 43 (x,y)

Register: ISP_EXP_MEAN_04

Mean luminance value of block 04 Reset value: 0000'0000H

Address: ISP_AE_BASE + 0064H			Mode : r
Bits	**Name**	**Description**	
31:8	---	unused	
7:0	isp_exp_mean_04	Mean luminance value of block 04 (x,y)	

Register: ISP_EXP_MEAN_14

Mean luminance value of block 14 Reset value: 0000'0000H

Address: ISP_AE_BASE + 0068H			Mode : r
Bits	**Name**	**Description**	
31:8	---	unused	
7:0	isp_exp_mean_14	Mean luminance value of block 14 (x,y)	

Register: ISP_EXP_MEAN_24

Mean luminance value of block 24 Reset value: 0000'0000H

Address: ISP_AE_BASE + 006CH			Mode : r
Bits	**Name**	**Description**	
31:8	---	unused	
7:0	isp_exp_mean_24	Mean luminance value of block 24 (x,y)	

Register: ISP_EXP_MEAN_34

Mean luminance value of block 34 Reset value: 0000'0000H

Address: ISP_AE_BASE + 0070H			Mode : r
Bits	**Name**	**Description**	
31:8	---	unused	
7:0	isp_exp_mean_34	Mean luminance value of block 34 (x,y)	

Register: ISP_EXP_MEAN_44

Mean luminance value of block 44 Reset value: 0000'0000H

Address: ISP_AE_BASE + 0074H			Mode : r
Bits	**Name**	**Description**	
31:8	---	unused	
7:0	isp_exp_mean_44	Mean luminance value of block 44 (x,y)	

Register: ISP_BLS_CTRL

global control register Reset value: 0000'0000H

Address: ISP_BLS_BASE + 0000H			Mode : rw
Bits	**Name**	**Description**	
31:4	---	unused	
3:2	WINDOW_ENABLE	0: no measuring is performed 1: only window 1 is measured 2: only window 2 is	
1	BLS_MODE	1: subtract measured values 0: subtract fixed	
0	BLS_ENABLE	1: black level subtraction is enabled 0: bypass the black	

Register: ISP_BLS_SAMPLES

samples register Reset value: 0000'0000H

Address: ISP_BLS_BASE + 0004H			Mode : rw
Bits	**Name**	**Description**	
31:5	---	unused	

samples register Reset value: 0000'0000H

Address: ISP_BLS_BASE + 0004H		Mode : rw
Bits	**Name**	**Description**
4:0	BLS_SAMPLES	This number to the power of two gives the number of measure samples for each Bayer position. Range 0x00: 2^0=1 to 0x12: 2^18=262144. This number is also the divider for the accumulator for each Bayer position. The accumulation will be stopped, if the number of measured pixels for the current Bayer position is equal to the number of samples. The measure windows must be positioned that way that the number of included pixels of each Bayer position included by both windows is equal or greater than the number of measure samples calculated by 2^BLS_SAMPLES ! NOTE: The number of pixels of one Bayer position is 1/4 of the number of all Pixels included by the measure windows

Register: ISP_BLS_H1_START

window 1 horizontal start Reset value: 0000'0000H

Address: ISP_BLS_BASE + 0008H		Mode : rw
Bits	**Name**	**Description**
31:14	---	unused
13:0	BLS_H1_START	Black pixel window 1 horizontal start position

Register: ISP_BLS_H1_STOP

window 1 horizontal stop Reset value: 0000'0000H

Address: ISP_BLS_BASE + 000CH		Mode : rw
Bits	**Name**	**Description**
31:14	---	unused
13:0	BLS_H1_STOP	Black pixel window 1 horizontal stop position

Register: ISP_BLS_V1_START

window 1 vertical start Reset value: 0000'0000H

Address: ISP_BLS_BASE + 0010H			Mode : rw
Bits	Name	Description	
31:14	---	unused	
13:0	BLS_V1_START	Black pixel window 1 vertical start position	

Register: ISP_BLS_V1_STOP

window 1 vertical stop Reset value: 0000'0000H

Address: ISP_BLS_BASE + 0014H			Mode : rw
Bits	Name	Description	
31:14	---	unused	
13:0	BLS_V1_STOP	Black pixel window 1 vertical stop position	

Register: ISP_BLS_H2_START

window 2 horizontal start Reset value: 0000'0000H

Address: ISP_BLS_BASE + 0018H			Mode : rw
Bits	Name	Description	
31:14	---	unused	
13:0	BLS_H2_START	Black pixel window 2 horizontal start position	

Register: ISP_BLS_H2_STOP

window 2 horizontal stop Reset value: 0000'0000H

Address: ISP_BLS_BASE + 001CH			Mode : rw
Bits	Name	Description	
31:14	---	unused	
13:0	BLS_H2_STOP	Black pixel window 2 horizontal stop position	

Register: ISP_BLS_V2_START

window 2 vertical start Reset value: 0000'0000H

Address: ISP_BLS_BASE + 0020H			Mode : rw
Bits	**Name**	**Description**	
31:14	---	unused	
13:0	BLS_V2_START	Black pixel window 2 vertical start position	

Register: ISP_BLS_V2_STOP

window 2 vertical stop Reset value: 0000'0000H

Address: ISP_BLS_BASE + 0024H			Mode : rw
Bits	**Name**	**Description**	
31:14	---	unused	
13:0	BLS_V2_STOP	Black pixel window 2 vertical stop position	

Register: ISP_BLS_A_FIXED

fixed black level A Reset value: 0000'0000H

Address: ISP_BLS_BASE + 0028H			Mode : rw
Bits	**Name**	**Description**	
31:12	---	unused	
12:0	BLS_A_FIXED	Fixed black level for A pixels – signed two's complement, value range from -4096 to +4095, a positive value will be subtracted from the pixel	

Register: ISP_BLS_B_FIXED

fixed black level B Reset value: 0000'0000H

Address: ISP_BLS_BASE + 002CH			Mode : rw
Bits	**Name**	**Description**	
31:12	---	unused	
12:0	BLS_B_FIXED	Fixed black level for B pixels – signed two's complement, value range from -4096 to +4095	

Register: ISP_BLS_C_FIXED

fixed black level C Reset value: 0000'0000H

Address: ISP_BLS_BASE + 0030H			Mode : rw
Bits	Name	Description	
31:13	---	unused	
12:0	BLS_C_FIXED	Fixed black level for C pixels – signed two's complement, value range from -4096 to +4095	

Register: ISP_BLS_D_FIXED
fixed black level D Reset value: 0000'0000H

Address: ISP_BLS_BASE + 0034H			Mode : rw
Bits	Name	Description	
31:13	---	unused	
12:0	BLS_D_FIXED	Fixed black level for D pixels - signed two's complement, value range from -4096 to +4095	

Register: ISP_BLS_A_MEASURED

measured black level A Reset value: 0000'0000H

Address: ISP_BLS_BASE + 0038H			Mode : r
Bits	Name	Description	
31:12	---	unused	
11:0	BLS_A_MEASURED	Measured black level for A pixels	

Register: ISP_BLS_B_MEASURED

measured black level B Reset value: 0000'0000H

Address: ISP_BLS_BASE + 003CH			Mode : r
Bits	Name	Description	
31:12	---	unused	
11:0	BLS_B_MEASURED	Measured black level for B pixels	

Register: ISP_BLS_C_MEASURED

measured black level C Reset value: 0000'0000H

Address: ISP_BLS_BASE + 0040H		Mode : r
Bits	**Name**	**Description**
31:12	---	unused
11:0	BLS_C_MEASURED	Measured black level for C pixels

Register: ISP_BLS_D_MEASURED

measured black level D Reset value: 0000'0000H

Address: ISP_BLS_BASE + 0044H		Mode : r
Bits	**Name**	**Description**
31:12	---	unused
11:0	BLS_D_MEASURED	Measured black level for D pixels

Register: ISP_DPF_MODE

Mode control for Denoising Pre-Filter block Reset value: 0000'0000H

Address: ISP_DPF_BASE + 0000H		Mode : rw
Bits	**Name**	**Description**
31:10	---	unused
9	USE_NF_GAIN	1: DPF_NF_GAINs will be used. 0: DPF_NF_GAINs will not be used. *Default*
8	LSC_GAIN_COMP	1: LSC gain will be processed 0: LSC gain will not be processed. Use LSC gain factor of 1. *Default*
7	AWB_GAIN_COMP	Only relevant when use_nf_gain == 0 && ISP_CTRL::ISP_AWB_ENABLE ==1 1: ISP_AWB gains will be processed 0: ISP_AWB gains will not be processed. Use AWB gain factor of 1. *Default*
6	NLL_SEGMENTATION	1: optimized logarithmic like segmentation for Noise Level Lookup (NLL) 0: equidistant segmentation for NLL *Default*

Mode control for Denoising Pre-Filter block Reset value: 0000'0000H

Address: ISP_DPF_BASE + 0000H		Mode : rw
Bits	**Name**	**Description**
5	RB_FILTER_SIZE	1: Red and Blue filter kernel size of 9x9 (5x5 active) pixels 0: Wide Red and Blue filter kernel size of 13x9 (7x5 active) pixels *Default*
4	R_FILTER_OFF	1: disable filter processing for red pixels (R) 0: filter R pixels *Default*
3	GR_FILTER_OFF	1: disable filter processing for green pixels in green/red lines (GR) 0: filter GR pixels *Default*
2	GB_FILTER_OFF	1: disable filter processing for green pixels in green/blue lines (GB) 0: filter GB pixels *Default*
1	B_FILTER_OFF	1: disable filter processing for blue pixels (B) 0: filter B pixels *Default*
0	DPF_ENABLE	1: enable dpf 0: bypass dpf *Default*

Register: ISP_DPF_STRENGTH_R

filter strength of the RED filter Reset value: 0000'0040H

Address: ISP_DPF_BASE + 0004H		Mode : rw
Bits	**Name**	**Description**
31:8	---	unused
7:0	INV_WEIGHT_R	Filter strength of the filter is determined by weight. Default is a weight of 1. A higher weight increases the filter strength. In this register the unsigned 8 bit value 64/weight is stored. The following values show examples: weight=0.251 -> 255, weight=0.5 -> 128, weight=1 -> 64 *default* weight=1.25 -> 51, weight=1.5 -> 42, weight=1.75 -> 37, weight=2 -> 32

Register: ISP_DPF_STRENGTH_G

filter strength of the GREEN filter Reset value: 0000'0040H

Address: ISP_DPF_BASE + 0008H		Mode : rw
Bits	**Name**	**Description**
31:8	---	unused
7:0	INV_WEIGHT_G	Filter strength of the filter is determined by weight. Default is a weight of 1. A higher weight increases the filter strength. In this register the unsigned 8 bit value 64/weight is stored. The following values show examples: weight=0.251 -> 255, weight=0.5 -> 128, weight=1 -> 64 *default* weight=1.25 -> 51, weight=1.5 -> 42, weight=1.75 -> 37, weight=2 -> 32

Register: ISP_DPF_STRENGTH_B

filter strength of the BLUE filter Reset value: 0000'0040H

Address: ISP_DPF_BASE + 000CH		Mode : rw
Bits	**Name**	**Description**
31:8	---	unused
7:0	INV_WEIGHT_B	Filter strength of the filter is determined by weight. Default is a weight of 1. A higher weight increases the filter strength. In this register the unsigned 8 bit value 64/weight is stored. The following values show examples: weight=0.251 -> 255, weight=0.5 -> 128, weight=1 -> 64 *default* weight=1.25 -> 51, weight=1.5 -> 42, weight=1.75 -> 37, weight=2 -> 32

Register: ISP_DPF_S_WEIGHT_G_1_4

Spatial Weights green channel 1 2 3 4 Reset value: 1010'1010H

Address: ISP_DPF_BASE + 0010H		Mode : rw
Bits	**Name**	**Description**
31:30	---	unused

Spatial Weights green channel 1 2 3 4 Reset value: 1010'1010H

Address: ISP_DPF_BASE + 0010H		Mode : rw
Bits	**Name**	**Description**
28:24	S_WEIGHT_G4	Filter Coefficient green channel S_WEIGHT_G4 5 bit unsigned, value range 1/16 to 16/16 Default value is 16/16 (*Default*)
23:21	---	unused
20:16	S_WEIGHT_G3	Filter Coefficient green channel S_WEIGHT_G3 5 bit unsigned, value range 1/16 to 16/16 Default value is 16/16 (*Default*)
15:13	---	unused
12:8	S_WEIGHT_G2	Filter Coefficient green channel S_WEIGHT_G2 5 bit unsigned, value range 1/16 to 16/16 Default value is 16/16 (*Default*)
7:5	---	unused
4:0	S_WEIGHT_G1	Filter Coefficient green channel S_WEIGHT_G1 5 bit unsigned, value range 1/16 to 16/16 Default value is 16/16 (*Default*)
Note: The value zero (0/16) disables the filter tap		

Register: ISP_DPF_S_WEIGHT_G_5_6
Spatial Weights green channel 5 6 Reset value: 0000'1010H

Address: ISP_DPF_BASE + 0014H		Mode : rw
Bits	**Name**	**Description**
31:13	---	unused
12:8	S_WEIGHT_G6	Filter Coefficient green channel S_WEIGHT_G6 5 bit unsigned, value range 1/16 to 16/16 Default value is 16/16 (*Default*)
7:5	---	unused
4:0	S_WEIGHT_G5	Filter Coefficient green channel S_WEIGHT_G5 5 bit unsigned, value range 1/16 to 16/16 Default value is 16/16 (*Default*)
Note: The value zero (0/16) disables the filter tap.		

Register: ISP_DPF_S_WEIGHT_RB_1_4

Spatial Weights red/blue channels 1 2 3 4 Reset value: 1010'1010H

Address: ISP_DPF_BASE + 0018H			Mode : rw
Bits	Name	Description	
31:30	---	unused	
28:24	S_WEIGHT_RB4	Filter Coefficient red/blue channels S_WEIGHT_RB4 5 bit unsigned, value range 1/16 to 16/16 Default value is 16/16 (*Default*)	
23:21	---	unused	
20:16	S_WEIGHT_RB3	Filter Coefficient red/blue channels S_WEIGHT_RB3 5 bit unsigned, value range 1/16 to 16/16 Default value is 16/16 (*Default*)	
15:13	---	unused	
12:8	S_WEIGHT_RB2	Filter Coefficient red/blue channels S_WEIGHT_RB2 5 bit unsigned, value range 1/16 to 16/16 Default value is 16/16 (*Default*)	
7:5	---	unused	
4:0	S_WEIGHT_RB1	Filter Coefficient red/blue channels S_WEIGHT_RB1 5 bit unsigned, value range 1/16 to 16/16 Default value is 16/16 (*Default*)	
Note: The value zero (0/16) disables the filter tap.			

Register: ISP_DPF_S_WEIGHT_RB_5_6
Spatial Weights red/blue channels 5 6 Reset value: 0000'1010H

Address: ISP_DPF_BASE + 001CH			Mode : rw
Bits	Name	Description	
31:13	---	unused	
12:8	S_WEIGHT_RB6	Filter Coefficient red/blue channels S_WEIGHT_RB6 5 bit unsigned, value range 1/16 to 16/16 Default value is 16/16 (*Default*)	
7:5	---	unused	
4:0	S_WEIGHT_RB5	Filter Coefficient red/blue channels S_WEIGHT_RB5 5 bit unsigned, value range 1/16 to 16/16 Default value is 16/16 (*Default*)	
Note: The value zero (0/16) disables the filter tap.			

Register: ISP_DPF_NLL_COEFF
Noise Level Lookup Coefficient n (n=0..16) Reset value: 0000'03FFH

Address: ISP_DPF_BASE + 0020H + (4H * n)			Mode : rw
Bits	Name	Description	

31:10	---	unused
9:0	nll_coeff_n	Noise Level Lookup Table Coefficient nll_coeff_n 10 bit unsigned, value range 1/1024 to 1023/1024 (*Default*)

Register: ISP_DPF_NF_GAIN_R

noise function gain for red pixels Reset value: 0000'0100H

Address: ISP_DPF_BASE + 0064H		**Mode : rw**
Bits	**Name**	**Description**
31:12	---	unused
11:0	DPF_NF_GAIN_R	Noise Function (NF) Gain that replaces the AWB gain for red pixels. 12 bit unsigned integer format: gain=1 -> 0x100

Register: ISP_DPF_NF_GAIN_GR

noise function gain for green in red pixels Reset value: 0000'0100H

Address: ISP_DPF_BASE + 0068H		**Mode : rw**
Bits	**Name**	**Description**
31:12	---	unused
11:0	DPF_NF_GAIN_GR	Noise Function (NF) Gain that replaces the AWB gain for green pixels in a red line. 12 bit unsigned integer format: gain=1 -> 0x100

Register: ISP_DPF_NF_GAIN_GB

noise function gain for green in blue pixels Reset value: 0000'0100H

Address: ISP_DPF_BASE + 006CH		**Mode : rw**
Bits	**Name**	**Description**
31:12	---	unused
11:0	DPF_NF_GAIN_GB	Noise Function (NF) Gain that replaces the AWB gain for green pixels in a blue line. 12 bit unsigned integer format: gain=1 -> 0x100

Register: ISP_DPF_NF_GAIN_B

noise function gain for blue pixels Reset value: 0000'0100H

Address: ISP_DPF_BASE + 0070H		**Mode : rw**
Bits	**Name**	**Description**
31:12	---	unused

11:0	DPF_NF_GAIN_B	Noise Function (NF) Gain that replaces the AWB gain for blue pixels. 12 bit unsigned integer format: gain=1 -> 0x100

Register: ISP_DPCC_MODE

Mode control for DPCC detection unit Reset value: 0000'0004H

Address: ISP_DPCC_BASE + 0000H		**Mode : rw**
Bits	**Name**	**Description**
31:3	---	unused
2	STAGE1_ENABLE	1: enable stage1 *Default* 0: bypass stage1
1	GRAYSCALE_MODE	1: enable gray scale data input from black and white sensors (without color filter array) 0: BAYER DATA INPUT *Default*
0	ISP_DPCC_enable	1: enable DPCC 0: bypass DPCC *Default*

Register: ISP_DPCC_OUTPUT_MODE

Interpolation mode for correction unit Reset value: 0000'0000H

Address: ISP_DPCC_BASE + 0004H		**Mode : rw**
Bits	**Name**	**Description**
31:4	---	unused
3	STAGE1_RB_3x3	1: stage1 red/blue 9 pixel (3x3) output median 0: stage1 red/blue 4 or 5 pixel output median *Default*
2	STAGE1_G_3x3	1: stage1 green 9 pixel (3x3) output median 0: stage1 green 4 or 5 pixel output median *Default*
1	STAGE1_INCL_RB_CENTER	1: stage1 include center pixel for red/blue output median 2x2+1 *Default* 0: stage1 do not include center pixel for red/blue output median 2x2
0	STAGE1_INCL_GREEN_CENTER	1: stage1 include center pixel for green output median 2x2+1 *Default* 0: stage1 do not include center pixel for green output median 2x2

Register: ISP_DPCC_SET_USE

DPCC methods set usage for detection Reset value: 0000'0001H

Address: ISP_DPCC_BASE + 0008H		**Mode : rw**
Bits	**Name**	**Description**
31:4	---	unused

3	STAGE1_USE_FIX_SET	1: stage1 use hard coded methods set *Default* 0: stage1 do not use hard coded methods set

DPCC methods set usage for detection Reset value: 0000'0001H

Address: ISP_DPCC_BASE + 0008H		Mode : rw
Bits	**Name**	**Description**
2	STAGE1_USE_SET_3	1: stage1 use methods set 3 0: stage1 do not use methods set 3 *Default*
1	STAGE1_USE_SET_2	1: stage1 use methods set 2 0: stage1 do not use methods set 2 *Default*
0	STAGE1_USE_SET_1	1: stage1 use methods set 1 *Default* 0: stage1 do not use methods set 1
Note: methods sets can be used in parallel for each stage and the result is the logical OR of all selected sets		

Register: ISP_DPCC_METHODS_SET_1
Methods enable bits for SET_1 Reset value: 0000'1D1DH

Address: ISP_DPCC_BASE + 000CH		Mode : rw
Bits	**Name**	**Description**
31:13	---	unused
12	RG_RED_BLUE1_ENABLE	1: enable Rank Gradient check for red_blue *Default* 0: bypass Rank Gradient check for red_blue
11	RND_RED_BLUE1_ENABLE	1: enable Rank Neighbor Difference check for red_blue *Default* 0: bypass Rank Neighbor Difference check for red_blue
10	RO_RED_BLUE1_ENABLE	1: enable Rank Order check for red_blue *Default* 0: bypass Rank Order check for red_blue
9	LC_RED_BLUE1_ENABLE	1: enable Line check for red_blue *Default* 0: bypass Line check for red_blue
8	PG_RED_BLUE1_ENABLE	1: enable Peak Gradient check for red_blue *Default* 0: bypass Peak Gradient check for red_blue
7:5	---	unused
4	RG_GREEN1_ENABLE	1: enable Rank Gradient check for green *Default* 0: bypass Rank Gradient check for green
3	RND_GREEN1_ENABLE	1: enable Rank Neighbor Difference check for green *Default* 0: bypass Rank Neighbor Difference check for green
2	RO_GREEN1_ENABLE	1: enable Rank Order check for green *Default* 0: bypass Rank Order check for green
1	LC_GREEN1_ENABLE	1: enable Line check for green *Default* 0: bypass Line check for green
0	PG_GREEN1_ENABLE	1: enable Peak Gradient check for green *Default* 0: bypass Peak Gradient check for green

Note: different methods can be used in parallel, the result is the logical AND of all selected methods

Register: ISP_DPCC_METHODS_SET_2

Methods enable bits for SET_2 Reset value: 0000'0000H

Address: ISP_DPCC_BASE + 0010H		**Mode : rw**
Bits	**Name**	**Description**
31:12	---	unused
12	RG_RED_BLUE2_ENABLE	1: enable Rank Gradient check for red_blue *Default* 0: bypass Rank Gradient check for red_blue
11	RND_RED_BLUE2_ENABLE	1: enable Rank Neighbor Difference check for red_blue *Default* 0: bypass Rank Neighbor Difference check for red_blue
10	RO_RED_BLUE2_ENABLE	1: enable Rank Order check for red_blue *Default* 0: bypass Rank Order check for red_blue
9	LC_RED_BLUE2_ENABLE	1: enable Line check for red_blue 0: bypass Line check for red_blue *Default*
8	PG_RED_BLUE2_ENABLE	1: enable Peak Gradient check for red_blue *Default* 0: bypass Peak Gradient check for red_blue
7:5	---	unused
4	RG_GREEN2_ENABLE	1: enable Rank Gradient check for green *Default* 0: bypass Rank Gradient check for green
3	RND_GREEN2_ENABLE	1: enable Rank Neighbor Difference check for green *Default* 0: bypass Rank Neighbor Difference check for green
2	RO_GREEN2_ENABLE	1: enable Rank Order check for green *Default* 0: bypass Rank Order check for green
1	LC_GREEN2_ENABLE	1: enable Line check for green 0: bypass Line check for green *Default*

Methods enable bits for SET_2 Reset value: 0000'0000H

Address: ISP_DPCC_BASE + 0010H		Mode : rw
Bits	**Name**	**Description**
0	PG_GREEN2_ENABLE	1: enable Peak Gradient check for green *Default* 0: bypass Peak Gradient check for green
Note: different methods can be used in parallel, the result is the logical AND of all selected methods		

Register: ISP_DPCC_METHODS_SET_3

Methods enable bits for SET_3 Reset value: 0000'0000H

Address: ISP_DPCC_BASE + 0014H		Mode : rw
Bits	**Name**	**Description**
31:13	---	unused
12	RG_RED_BLUE3_ENABLE	1: enable Rank Gradient check for red_blue 0: bypass Rank Gradient check for red_blue *Default*
11	RND_RED_BLUE3_ENABLE	1: enable Rank Neighbor Difference check for red_blue 0: bypass Rank Neighbor Difference check for red_blue
10	RO_RED_BLUE3_ENABLE	1: enable Rank Order check for red_blue *Default* 0: bypass Rank Order check for red_blue
9	LC_RED_BLUE3_ENABLE	1: enable Line check for red_blue *Default* 0: bypass Line check for red_blue
8	PG_RED_BLUE3_ENABLE	1: enable Peak Gradient check for red_blue *Default* 0: bypass Peak Gradient check for red_blue
7:5	---	unused
4	RG_GREEN3_ENABLE	1: enable Rank Gradient check for green 0: bypass Rank Gradient check for green *Default*
3	RND_GREEN3_ENABLE	1: enable Rank Neighbor Difference check for green 0: bypass Rank Neighbor Difference check for green *Default*
2	RO_GREEN3_ENABLE	1: enable Rank Order check for green *Default* 0: bypass Rank Order check for green
1	LC_GREEN3_ENABLE	1: enable Line check for green *Default* 0: bypass Line check for green

Methods enable bits for SET_3 Reset value: 0000'0000H

Address: ISP_DPCC_BASE + 0014H		Mode : rw
Bits	**Name**	**Description**
0	PG_GREEN3_ENABLE	1: enable Peak Gradient check for green *Default* 0: bypass Peak Gradient check for green
Note: different methods can be used in parallel, the result is the logical AND of all selected methods		

Register: ISP_DPCC_LINE_THRESH_1

Line threshold SET_1 Reset value: 0000'0000H

Address: ISP_DPCC_BASE + 0018H		Mode : rw
Bits	**Name**	**Description**
31:16	---	unused
15:8	LINE_THR_1_RB	line threshold for set 1 red/blue
7:0	LINE_THR_1_G	line threshold for set 1 green
Note: all values are unsigned integer		

Register: ISP_DPCC_LINE_MAD_FAC_1

Mean Absolute Difference (MAD) factor for Line check set 1 Reset value: 0000'0000H

Address: ISP_DPCC_BASE + 001CH		Mode : rw
Bits	**Name**	**Description**
31:14	---	unused
13:8	LINE_MAD_FAC_1_RB	line MAD factor for set 1 red/blue
7:6	---	unused
5:0	LINE_MAD_FAC_1_G	line MAD factor for set 1 green
Note: all values are unsigned integer		

Register: ISP_DPCC_PG_FAC_1

Peak gradient factor for set 1 Reset value: 0000'0000H

Address: ISP_DPCC_BASE + 0020H		**Mode : rw**
Bits	**Name**	**Description**
31:14	---	unused
13:8	PG_FAC_1_RB	Peak gradient factor for set 1 red/blue
7:6	---	unused
5:0	PG_FAC_1_G	Peak gradient factor for set 1 green
Note: all values are unsigned integer		

Register: ISP_DPCC_RND_THRESH_1

Rank Neighbor Difference threshold for set 1 Reset value: 0000'0000H

Address: ISP_DPCC_BASE + 0024H		**Mode : rw**
Bits	**Name**	**Description**
31:16	---	unused
15:8	RND_THR_1_RB	Rank Neighbor Difference threshold for set 1 red/blue
7:0	RND_THR_1_G	Rank Neighbor Difference threshold for set 1 green
Note: all values are unsigned integer		

Register: ISP_DPCC_RG_FAC_1

Rank gradient factor for set 1 Reset value: 0000'0000H

Address: ISP_DPCC_BASE + 0028H		**Mode : rw**
Bits	**Name**	**Description**
31:14	---	unused
13:8	RG_FAC_1_RB	Rank gradient factor for set 1 red/blue
7:6	---	unused
5:0	RG_FAC_1_G	Rank gradient factor for set 1 green
Note: all values are unsigned integer		

Register: ISP_DPCC_LINE_THRESH_2

Line threshold set 2 Reset value: 0000'0000H

Address: ISP_DPCC_BASE + 002CH		**Mode : rw**
Bits	**Name**	**Description**
31:16	---	unused
15:8	LINE_THR_2_RB	line threshold for set 2 red/blue
7:0	LINE_THR_2_G	line threshold for set 2 green
Note: all values are unsigned integer		

Register: ISP_DPCC_LINE_MAD_FAC_2

Mean Absolute Difference (MAD) factor for Line check set 2 Reset value: 0000'0000H

Address: ISP_DPCC_BASE + 0030H		**Mode : rw**
Bits	**Name**	**Description**
31:14	---	unused
13:8	LINE_MAD_FAC_2_RB	line MAD factor for set 2 red/blue
7:6	---	unused
5:0	LINE_MAD_FAC_2_G	line MAD factor for set 2 green
Note: all values are unsigned integer		

Register: ISP_DPCC_PG_FAC_2

Peak gradient factor for set 2 Reset value: 0000'0000H

Address: ISP_DPCC_BASE + 0034H		**Mode : rw**
Bits	**Name**	**Description**
31:14	---	unused
13:8	PG_FAC_2_RB	Peak gradient factor for set 2 red/blue
7:6	---	unused
5:0	PG_FAC_2_G	Peak gradient factor for set 2 green
Note: all values are unsigned integer		

Register: ISP_DPCC_RND_THRESH_2

Rank Neighbor Difference threshold for set 2 Reset value: 0000'0000H

Address: ISP_DPCC_BASE + 0038H		Mode : rw
Bits	**Name**	**Description**
31:16	---	unused
15:8	RND_THR_2_RB	Rank Neighbor Difference threshold for set 2 red/blue
7:0	RND_THR_2_G	Rank Neighbor Difference threshold for set 2 green
Note: all values are unsigned integer		

Register: ISP_DPCC_RG_FAC_2

Rank gradient factor for set 2 Reset value: 0000'0000H

Address: ISP_DPCC_BASE + 003CH		Mode : rw
Bits	**Name**	**Description**
31:14	---	unused
13:8	RG_FAC_2_RB	Rank gradient factor for set 2 red/blue
7:6	---	unused
5:0	RG_FAC_2_G	Rank gradient factor for set 2 green
Note: all values are unsigned integer		

Register: ISP_DPCC_LINE_THRESH_3

Line threshold set 3 Reset value: 0000'0000H

Address: ISP_DPCC_BASE + 0040H		Mode : rw
Bits	**Name**	**Description**
31:16	---	unused
15:8	LINE_THR_3_RB	line threshold for set 3 red/blue
7:0	LINE_THR_3_G	line threshold for set 3 green
Note: all values are unsigned integer		

Register: ISP_DPCC_LINE_MAD_FAC_3

Mean Absolute Difference (MAD) factor for Line check set 3 Reset value: 0000'0000H

Address: ISP_DPCC_BASE + 0044H		**Mode : rw**
Bits	**Name**	**Description**
31:14	---	unused
13:8	LINE_MAD_FAC_3_RB	line MAD factor for set 3 red/blue
7:6	---	unused
5:0	LINE_MAD_FAC_3_G	line MAD factor for set 3 green
Note: all values are unsigned integer		

Register: ISP_DPCC_PG_FAC_3

Peak gradient factor for set 3 Reset value: 0000'0000H

Address: ISP_DPCC_BASE + 0048H		**Mode : rw**
Bits	**Name**	**Description**
31:14	---	unused
13:8	PG_FAC_3_RB	Peak gradient factor for set 3 red/blue
7:6	---	unused
5:0	PG_FAC_3_G	Peak gradient factor for set 3 green
Note: all values are unsigned integer		

Register: ISP_DPCC_RND_THRESH_3

Rank Neighbor Difference threshold for set 3 Reset value: 0000'0000H

Address: ISP_DPCC_BASE + 004CH		**Mode : rw**
Bits	**Name**	**Description**
31:16	---	unused
15:8	RND_THR_3_RB	Rank Neighbor Difference threshold for set 3 red/blue
7:0	RND_THR_3_G	Rank Neighbor Difference threshold for set 3 green
Note: all values are unsigned integer		

Register: ISP_DPCC_RG_FAC_3

Rank gradient factor for set 3 Reset value: 0000'0000H

Address: ISP_DPCC_BASE + 0050H		Mode : rw
Bits	**Name**	**Description**
31:14	---	unused
13:8	RG_FAC_3_RB	Rank gradient factor for set 3 red/blue
7:6	---	unused
5:0	RG_FAC_3_G	Rank gradient factor for set 3 green
Note: all values are unsigned integer		

Register: ISP_DPCC_RO_LIMITS

Rank Order Limits Reset value: 0000'0000H

Address: ISP_DPCC_BASE + 0054H		Mode : rw
Bits	**Name**	**Description**
31:12	---	unused
11:10	RO_LIM_3_RB	Rank order limit for set 3 red/blue
9:8	RO_LIM_3_G	Rank order limit for set 3 green
7:6	RO_LIM_2_RB	Rank order limit for set 2 red/blue
5:4	RO_LIM_2_G	Rank order limit for set 2 green
3:2	RO_LIM_1_RB	Rank order limit for set 1 red/blue
1:0	RO_LIM_1_G	Rank order limit for set 1 green
Note: all values are unsigned integer		

Register: ISP_DPCC_RND_OFFS

Differential Rank Offsets for Rank Neighbor Difference Reset value: 0000'0000H

Address: ISP_DPCC_BASE + 0058H		Mode : rw
Bits	**Name**	**Description**
31:12	---	unused
11:10	RND_OFFS_3_RB	Rank Offset to Neighbor for set 3 red/blue
9:8	RND_OFFS_3_G	Rank Offset to Neighbor for set 3 green

Differential Rank Offsets for Rank Neighbor Difference Reset value: 0000'0000H

Address: ISP_DPCC_BASE + 0058H		Mode : rw
Bits	**Name**	**Description**
7:6	RND_OFFS_2_RB	Rank Offset to Neighbor for set 2 red/blue
5:4	RND_OFFS_2_G	Rank Offset to Neighbor for set 2 green
3:2	RND_OFFS_1_RB	Rank Offset to Neighbor for set 1 red/blue
1:0	RND_OFFS_1_G	Rank Offset to Neighbor for set 1 green
Note: all values are unsigned integer		

Register: ISP_DPCC_BPT_CTRL

bad pixel table settings Reset value: 0000'0000H

Address: ISP_DPCC_BASE + 005CH		Mode : rw
Bits	**Name**	**Description**
31:12	---	unused
11	BPT_RB_3x3	1: if BPT active red/blue 9 pixel (3x3) output median 0: if BPT active red/blue 4 or 5 pixel output median *Default*
10	BPT_G_3x3	1: if BPT active green 9 pixel (3x3) output median 0: if BPT active green 4 or 5 pixel output median *Default*
9	BPT_INCL_RB_CENTER	1: if BPT active include center pixel for red/blue output median 2x2+1 0: if BPT active do not include center pixel for red/blue output median 2x2 *Default*
8	BPT_INCL_GREEN_CENTER	1: if BPT active include center pixel for green output median 2x2+1 0: if BPT active do not include center pixel for green output median 2x2 *Default*
7	BPT_USE_FIX_SET	1: for BPT write use hard coded methods set 0: for BPT write do not use hard coded methods set *Default*
6	BPT_USE_SET_3	1: for BPT write use methods set 3 0: for BPT write do not use methods set 3 *Default*
5	BPT_USE_SET_2	1: for BPT write use methods set 2 0: for BPT write do not use methods set 2 *Default*
4	BPT_USE_SET_1	1: for BPT write use methods set 1 0: for BPT write do not use methods set 1 *Default*
3:2	---	unused

bad pixel table settings Reset value: 0000'0000H

Address: ISP_DPCC_BASE + 005CH		Mode : rw
Bits	**Name**	**Description**
1	bpt_cor_en	table based correction enable 1: table based correction is enabled 0: table based correction is disabled
0	bpt_det_en	Bad pixel detection write enable 1: bad pixel detection write to memory is enabled 0: bad pixel detection write to memory is disabled
Note: This register controls the behaviour of the table based bad pixel correction module. It can be switched on and off independently of the DPCC detection and correction block. Different correction algorithms for the table based correction are available and are defined by this register. The default setting after reset enables a correction algorithm with most accurate correlation to surrounding pixels. Detection for the table based correction can be configured independently from the on-the-fly DPCC detection scheme.		

Register: ISP_DPCC_BPT_NUMBER
Number of entries for bad pixel table (table based correction) Reset value: 0000'0000H

Address: ISP_DPCC_BASE + 0060H		Mode : rw
Bits	**Name**	**Description**
31:12	---	unused
11:0	bp_number	Number of current Bad Pixel entries in bad pixel table (BPT)
Note: bit width of bp_number depends on size of BP RAM which is defined during chip synthesis		

Register: ISP_DPCC_BPT_ADDR

TABLE Start Address for table-based correction algorithm Reset value: 0000'0000H

Address: ISP_DPCC_BASE + 0064H		Mode : rwh
Bits	**Name**	**Description**
31:11	---	unused
10:0	bp_table_addr	Table RAM start address for read or write operations. The address counter is incremented at each read or write access to the data register (auto-increment
Note: MKOE tbc: Orignial register mode was rwh which is no longer supported with new version of SIG		

Register: ISP_DPCC_BPT_DATA

TABLE DATA register for read and write access of table RAM Reset value: 0000'0000H

Address: ISP_DPCC_BASE + 0068H		Mode : rwh
Bits	**Name**	**Description**
31:28	---	unused
27:16	bpt_v_addr	Bad Pixel vertical address (pixel position)
15:13	---	unused
12:0	bpt_h_addr	Bad Pixel horizontal address (pixel position)
Note: MKOE tbc: Orignial register mode was rwh which is no longer supported with new version of SIG -> rwhh The programmed table value is immediately written into the RAM. The RAM address is generated per auto-increment. The parameter RAMs for Lens Shade Correction and Bad		

Register: ISP_WDR_CTRL
Control Bits for Wide Dynamic Range Unit Reset value: 0000'0000H

Address: ISP_WDR_BASE + 0000H		Mode : rw
Bits	**Name**	**Description**
31:12	---	unused
11:8	WDR_RGB_FACTOR	rgb_factor defines how much influence the RGBmax approach has in comparison to Y. The illumination reference Iref is calculated according to the following formula: Iref = (WDR_RGB_FACTOR * RGBYmax_tr + (8 - WDR_RGB_FACTOR) * Y) / 8 So, rgb_factor = 0 means that the standard approach is used. Use of this factor requires that Iref has been selected, see WDR_USE_IREF.
7	---	unused
6	WDR_DISABLE_TRANSIENT	1: disable transient between Y and RGBY_max 0: calculate transient between Y and RGBY_max (for noise reduction) *Default* Use of this bit requires that Iref has been selected, see WDR_USE_IREF.
5	WDR_USE_RGB7_8	1: decrease RGBmax by 7/8 (for noise reduction) 0: do not modify RGBmax *Default* Use of this bit requires that Iref has been selected, see WDR_USE_IREF.

Control Bits for Wide Dynamic Range Unit Reset value: 0000'0000H

Address: ISP_WDR_BASE + 0000H		Mode : rw
Bits	**Name**	**Description**
4	WDR_USE_Y9_8	1: use R G B and Y*9/8 for maximum value calculation (for noise reduction) 0: only use R G B for maximum value calculation (RGBYmax approach) *Default* Use of this bit requires that Iref has been selected, see WDR_USE_IREF.
3	WDR_USE_IREF	1: use Iref (Illumination reference) instead of Y for ToneMapping and Gain calculation 0: use Y for ToneMapping and Gain calculation *Default* Iref is calculated according to the following formula: Iref = (WDR_RGB_FACTOR * RGBmax_tr + (8 -
2	WDR_CR_MAPPING_DISABLE	1: disable (bypass) Chrominance Mapping 0: enable Chrominance Mapping *Default* requires that Luminance/chrominance color space has been selected
1	WDR_COLOR_SPACE_SELECT	1: R, G, B color space 0: Luminance/Chrominance color space *Default*
0	WDR_ENABLE	1: enable WDR 0: bypass WDR *Default*

Register: ISP_WDR_TONECURVE_1

Tone Curve sample points dYn definition (part 1) Reset value: 4444'4444H

Address: ISP_WDR_BASE + 0004H		Mode : rw
Bits	**Name**	**Description**
31	---	unused
30:28	WDR_dY8	Tone curve sample point definition dY8 on the horizontal axis (input)
27	---	unused
26:24	WDR_dY7	Tone curve sample point definition dY7 on the horizontal axis (input)
23	---	unused
22:20	WDR_dY6	Tone curve sample point definition dY6 on the horizontal axis (input)

Tone Curve sample points dYn definition (part 1) **Reset value: 4444'4444H**

Address: ISP_WDR_BASE + 0004H		**Mode : rw**
Bits	**Name**	**Description**
19	---	unused
18:16	WDR_dY5	Tone curve sample point definition dY5 on the horizontal axis (input)
15	---	unused
14:12	WDR_dY4	Tone curve sample point definition dY4 on the horizontal axis (input)
11	---	unused
10:8	WDR_dY3	Tone curve sample point definition dY3 on the horizontal axis (input)
7	---	unused
6:4	WDR_dY2	Tone curve sample point definition dY2 on the horizontal axis (input)
3	---	unused
2:0	WDR_dY1	Tone curve sample point definition dY1 on the horizontal axis (input)
Note: The interval widths dYn are to be defined in a 2^(value+3) notation, where "value" has to be written to the register. So the steps would be dYn=0 -> 8 (2^3), dYn=1 -> 16 (2^4), dYn=2 -> 32 (2^5),... dYn=6 -> 512 (2^9), dYn=7 ->		

Register: ISP_WDR_TONECURVE_2

Tone Curve sample points dYn definition (part 2) **Reset value: 4444'4444H**

Address: ISP_WDR_BASE + 0008H		**Mode : rw**
Bits	**Name**	**Description**
31	---	unused
30:28	WDR_dY16	Tone curve sample point definition dY16 on the horizontal axis (input)
27	---	unused
26:24	WDR_dY15	Tone curve sample point definition dY15 on the horizontal axis (input)
23	---	unused

Tone Curve sample points dYn definition (part 2) **Reset value: 4444'4444H**

Address: ISP_WDR_BASE + 0008H		**Mode : rw**
Bits	**Name**	**Description**
22:20	WDR_dY14	Tone curve sample point definition dY14 on the horizontal axis (input)
19	---	unused
18:16	WDR_dY13	Tone curve sample point definition dY13 on the horizontal axis (input)
15	---	unused
14:12	WDR_dY12	Tone curve sample point definition dY12 on the horizontal axis (input)
11	---	unused
10:8	WDR_dY11	Tone curve sample point definition dY11 on the horizontal axis (input)
7	---	unused
6:4	WDR_dY10	Tone curve sample point definition dY10 on the horizontal axis (input)
3	---	unused
2:0	WDR_dY9	Tone curve sample point definition dY9 on the horizontal axis (input)
Note: The interval widths dYn are to be defined in a 2^(value+3) notation, where "value" has to be written to the register. So the steps would be dYn=0 -> 8 (2^3), dYn=1 -> 16 (2^4), dYn=2 -> 32 (2^5),... dYn=6 -> 512 (2^9), dYn=7 ->		

Register: ISP_WDR_TONECURVE_3

Tone Curve sample points dYn definition (part 3) **Reset value: 4444'4444H**

Address: ISP_WDR_BASE + 000CH		**Mode : rw**
Bits	**Name**	**Description**
31	---	unused
30:28	WDR_dY24	Tone curve sample point definition dY24 on the horizontal axis (input)
27	---	unused
26:24	WDR_dY23	Tone curve sample point definition dY23 on the horizontal axis (input)

Tone Curve sample points dYn definition (part 3) **Reset value: 4444'4444H**

Address: ISP_WDR_BASE + 000CH		**Mode : rw**
Bits	**Name**	**Description**
23	---	unused
22:20	WDR_dY22	Tone curve sample point definition dY22 on the horizontal axis (input)
19	---	unused
18:16	WDR_dY21	Tone curve sample point definition dY21 on the horizontal axis (input)
15	---	unused
14:12	WDR_dY20	Tone curve sample point definition dY20 on the horizontal axis (input)
11	---	unused
10:8	WDR_dY19	Tone curve sample point definition dY19 on the horizontal axis (input)
7	---	unused
6:4	WDR_dY18	Tone curve sample point definition dY18 on the horizontal axis (input)
3	---	unused
2:0	WDR_dY17	Tone curve sample point definition dY17 on the horizontal axis (input)
Note: The interval widths dYn are to be defined in a 2^(value+3) notation, where "value" has to be written to the register. So the steps would be dYn=0 -> 8 (2^3), dYn=1 -> 16 (2^4), dYn=2 -> 32 (2^5),... dYn=6 -> 512 (2^9), dYn=7 ->		

Register: ISP_WDR_TONECURVE_4

Tone Curve sample points dYn definition (part 4) **Reset value: 4444'4444H**

Address: ISP_WDR_BASE + 0010H		**Mode : rw**
Bits	**Name**	**Description**
31	---	unused
30:28	WDR_dY32	Tone curve sample point definition dY32 on the horizontal axis (input)
27	---	unused

Tone Curve sample points dYn definition (part 4) **Reset value: 4444'4444H**

Address: ISP_WDR_BASE + 0010H		**Mode : rw**
Bits	**Name**	**Description**
26:24	WDR_dY31	Tone curve sample point definition dY31 on the horizontal axis (input)
23	---	unused
22:20	WDR_dY30	Tone curve sample point definition dY30 on the horizontal axis (input)
19	---	unused
18:16	WDR_dY29	Tone curve sample point definition dY29 on the horizontal axis (input)
15	---	unused
14:12	WDR_dY28	Tone curve sample point definition dY28 on the horizontal axis (input)
11	---	unused
10:8	WDR_dY27	Tone curve sample point definition dY27 on the horizontal axis (input)
7	---	unused
6:4	WDR_dY26	Tone curve sample point definition dY26 on the horizontal axis (input)
3	---	unused
2:0	WDR_dY25	Tone curve sample point definition dY25 on the horizontal axis (input)
Note: The interval widths dYn are to be defined in a 2^(value+3) notation, where "value" has to be written to the register. So the steps would be dYn=0 -> 8 (2^3), dYn=1 -> 16 (2^4), dYn=2 -> 32 (2^5),... dYn=6 -> 512 (2^9), dYn=7 -> 1024 (2^10).		

Register: ISP_WDR_TONECURVE_YM

Tonemapping curve coefficient Ym_ n (n=0..32) **Reset value: 0000'0000H**

Address: ISP_WDR_BASE + 0014H + (4H * n)		**Mode : rw**
Bits	**Name**	**Description**
31:13	---	unused

Tonemapping curve coefficient Ym_ n (n=0..32) Reset value: 0000'0000H

Address: ISP_WDR_BASE + 0014H + (4H * n)		Mode : rw
Bits	**Name**	**Description**
12:0	tonecurve_ym_n	Tone curve value definition y-axis (output) of WDR unit

Note: The reset values define a linear curve which has the same effect as bypass. Reset values are: Ym_00 = 0x0000, Ym_01 = 0x0080, Ym_02 = 0x0100, Ym_03 = 0x0180, Ym_04 = 0x0200,
Ym_05 = 0x0280, Ym_06 = 0x0300, Ym_07 = 0x0380, Ym_08 = 0x0400, Ym_09 = 0x0480, Ym_10 = 0x0500, Ym_11 = 0x0580, Ym_12 = 0x0600, Ym_13 = 0x0680, Ym_14 = 0x0700, Ym_15 = 0x0780, Ym_16 = 0x0800, Ym_17 = 0x0880, Ym_18 = 0x0900, Ym_19 = 0x0980, Ym_20 = 0x0A00, Ym_21 = 0x0A80, Ym_22 = 0x0B00, Ym_23 = 0x0B80, Ym_24 = 0x0C00, Ym_25 = 0x0C80, Ym_26 = 0x0D00, Ym_27 = 0x0D80, Ym_28 = 0x0E00, Ym_29 = 0x0E80, Ym_30 = 0x0F00, Ym_31 = 0x0F80, Ym_32 = 0x1000

Data format: 13 bit unsigned

RESTRICTION: each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed !)

Register: ISP_WDR_OFFSET

Offset values for RGB path Reset value: 0000'0000H

Address: ISP_WDR_BASE + 0098H		Mode : rw
Bits	**Name**	**Description**
31:28	---	unused
27:16	LUM_OFFSET	Luminance Offset value (a) for RGB operation mode unsigned 12 bit value
15:12	---	unused
11:0	RGB_OFFSET	RGB Offset value (b) for RGB operation mode unsigned 12 bit value

Register: ISP_WDR_DELTAMIN
DeltaMin Threshold and Strength factor Reset value: 0010'0000H

Address: ISP_WDR_BASE + 009CH		Mode : rw
Bits	**Name**	**Description**
31:21	---	unused
20:16	DMIN_STRENGTH	strength factor for DMIN unsigned 5 bit value, range 0x00...0x10

DeltaMin Threshold and Strength factor Reset value: 0010'0000H

Address: ISP_WDR_BASE + 009CH			Mode : rw
Bits	Name	Description	
15:12	---	unused	
11:0	DMIN_THRESH	Lower threshold for deltaMin value unsigned 12 bit value	

Register: ISP_WDR_TONECURVE_1_SHD

Tone Curve sample points dYn definition shadow register (part 1) Reset value: 4444'4444H

Address: ISP_WDR_BASE + 00A0H			Mode : r
Bits	Name	Description	
31	---	unused	
30:28	WDR_dY8	Tone curve sample point definition dY8 on the horizontal axis (input)	
27	---	unused	
26:24	WDR_dY7	Tone curve sample point definition dY7 on the horizontal axis (input)	
23	---	unused	
22:20	WDR_dY6	Tone curve sample point definition dY6 on the horizontal axis (input)	
19	---	unused	
18:16	WDR_dY5	Tone curve sample point definition dY5 on the horizontal axis (input)	
15	---	unused	
14:12	WDR_dY4	Tone curve sample point definition dY4 on the horizontal axis (input)	
11	---	unused	
10:8	WDR_dY3	Tone curve sample point definition dY3 on the horizontal axis (input)	
7	---	unused	
6:4	WDR_dY2	Tone curve sample point definition dY2 on the horizontal axis (input)	
3	---	unused	

Tone Curve sample points dYn definition shadow register (part 1) Reset value: 4444'4444H

Address: ISP_WDR_BASE + 00A0H		Mode : r
Bits	**Name**	**Description**
2:0	WDR_dY1	Tone curve sample point definition dY1 on the horizontal axis (input)
Note: see register ISP_WDR_TONECURVE_1.		

Register: ISP_WDR_TONECURVE_2_SHD

Tone Curve sample points dYn definition shadow register (part 2) Reset value: 4444'4444H

Address: ISP_WDR_BASE + 00A4H		Mode : r
Bits	**Name**	**Description**
31	---	unused
30:28	WDR_dY16	Tone curve sample point definition dY16 on the horizontal axis (input)
27	---	unused
26:24	WDR_dY15	Tone curve sample point definition dY15 on the horizontal axis (input)
23	---	unused
22:20	WDR_dY14	Tone curve sample point definition dY14 on the horizontal axis (input)
19	---	unused
18:16	WDR_dY13	Tone curve sample point definition dY13 on the horizontal axis (input)
15	---	unused
14:12	WDR_dY12	Tone curve sample point definition dY12 on the horizontal axis (input)
11	---	unused
10:8	WDR_dY11	Tone curve sample point definition dY11 on the horizontal axis (input)
7	---	unused
6:4	WDR_dY10	Tone curve sample point definition dY10 on the horizontal axis (input)
3	---	unused

Tone Curve sample points dYn definition shadow register (part 2) Reset value: 4444'4444H

Address: ISP_WDR_BASE + 00A4H		Mode : r
Bits	**Name**	**Description**
2:0	WDR_dY9	Tone curve sample point definition dY9 on the horizontal axis (input)
Note: see register ISP_WDR_TONECURVE_2.		

Register: ISP_WDR_TONECURVE_3_SHD

Tone Curve sample points dYn definition shadow register (part 3) Reset value: 4444'4444H

Address: ISP_WDR_BASE + 00A8H		Mode : r
Bits	**Name**	**Description**
31	---	unused
30:28	WDR_dY24	Tone curve sample point definition dY24 on the horizontal axis (input)
27	---	unused
26:24	WDR_dY23	Tone curve sample point definition dY23 on the horizontal axis (input)
23	---	unused
22:20	WDR_dY22	Tone curve sample point definition dY22 on the horizontal axis (input)
19	---	unused
18:16	WDR_dY21	Tone curve sample point definition dY21 on the horizontal axis (input)
15	---	unused
14:12	WDR_dY20	Tone curve sample point definition dY20 on the horizontal axis (input)
11	---	unused
10:8	WDR_dY19	Tone curve sample point definition dY19 on the horizontal axis (input)
7	---	unused
6:4	WDR_dY18	Tone curve sample point definition dY18 on the horizontal axis (input)
3	---	unused

Tone Curve sample points dYn definition shadow register (part 3) Reset value: 4444'4444H

Address: ISP_WDR_BASE + 00A8H		Mode : r
Bits	**Name**	**Description**
2:0	WDR_dY17	Tone curve sample point definition dY17 on the horizontal axis (input)
Note: see register ISP_WDR_TONECURVE_3.		

Register: ISP_WDR_TONECURVE_4_SHD

Tone Curve sample points dYn definition shadow register(part 4) Reset value: 4444'4444H

Address: ISP_WDR_BASE + 00ACH		Mode : r
Bits	**Name**	**Description**
31	---	unused
30:28	WDR_dY32	Tone curve sample point definition dY32 on the horizontal axis (input)
27	---	unused
26:24	WDR_dY31	Tone curve sample point definition dY31 on the horizontal axis (input)
23	---	unused
22:20	WDR_dY30	Tone curve sample point definition dY30 on the horizontal axis (input)
19	---	unused
18:16	WDR_dY29	Tone curve sample point definition dY29 on the horizontal axis (input)
15	---	unused
14:12	WDR_dY28	Tone curve sample point definition dY28 on the horizontal axis (input)
11	---	unused
10:8	WDR_dY27	Tone curve sample point definition dY27 on the horizontal axis (input)
7	---	unused
6:4	WDR_dY26	Tone curve sample point definition dY26 on the horizontal axis (input)
3	---	unused

Tone Curve sample points dYn definition shadow register(part 4) Reset value: 4444'4444H

Address: ISP_WDR_BASE + 00ACH		Mode : r
Bits	**Name**	**Description**
2:0	WDR_dY25	Tone curve sample point definition dY25 on the horizontal axis (input)
Note: see register ISP_WDR_TONECURVE_4.		

Register: ISP_WDR_TONECURVE_YM_SHD

Tonemapping curve coefficient shadow register n (n=0..32) Reset value: 0000'0000H

Address: ISP_WDR_BASE + 00B0H + (4H * n)		Mode : r
Bits	**Name**	**Description**
31:12	---	unused
12:0	tonecurve_ym_n_shd	Tone curve value definition y-axis (output) of WDR unit shadow register.

Note: The reset values define a linear curve which has the same effect as bypass. Reset values are: Ym_00 = 0x0000, Ym_01 = 0x0080, Ym_02 = 0x0100, Ym_03 = 0x0180, Ym_04 = 0x0200,

Ym_05 = 0x0280, Ym_06 = 0x0300, Ym_07 = 0x0380, Ym_08 = 0x0400, Ym_09 = 0x0480, Ym_10 = 0x0500, Ym_11 = 0x0580, Ym_12 = 0x0600, Ym_13 = 0x0680, Ym_14 = 0x0700, Ym_15 = 0x0780, Ym_16 = 0x0800, Ym_17 = 0x0880, Ym_18 = 0x0900, Ym_19 = 0x0980, Ym_20 = 0x0A00, Ym_21 = 0x0A80, Ym_22 = 0x0B00, Ym_23 = 0x0B80, Ym_24 = 0x0C00, Ym_25 = 0x0C80, Ym_26 = 0x0D00, Ym_27 = 0x0D80, Ym_28 = 0x0E00, Ym_29 = 0x0E80, Ym_30 = 0x0F00, Ym_31 = 0x0F80, Ym_32 = 0x1000

Data format: 13 bit unsigned

RESTRICTION: each Y must be in the +2047/-2048 range compared to its predecessor (so that the difference between successive Y values is 12-bit signed !)

Register: ISP_VSM_MODE

VS Measure Mode Reset value: 0000'0000H

Address: ISP_VSM_BASE + 0000H		Mode : rw
Bits	**Name**	**Description**
31:2	---	unused
1	vsm_meas_irq_enable	1: VS measure done IRQ enable.
0	vsm_meas_en	1: enable measure.

Register: ISP_VSM_H_OFFS

VSM window horizontal offset Reset value: 0000'0000H

Address: ISP_VSM_BASE + 0004H		Mode : rw
Bit	**Name**	**Description**
31:	---	unused
12:	vsm_h_offset	Horizontal offset in pixels.

Register: ISP_VSM_V_OFFS

VSM window vertical offset Reset value: 0000'0000H

Address: ISP_VSM_BASE + 0008H		Mode : rw
Bit	**Name**	**Description**
31:	---	unused
12:	vsm_v_offset	Vertical offset in pixels.

Register: ISP_VSM_H_SIZE

Horizontal measure window size Reset value: 0000'0000H

Address: ISP_VSM_BASE + 000CH		Mode : rw
Bit	**Name**	**Description**
31:	---	unused
10:	vsm_h_size	Horizontal size in pixels. Range 64..1920
0	---	unused
Note: only even values are allowed: vsm_h_size[0] not writable and read returns 0.		

Register: ISP_VSM_V_SIZE

Vertical measure window size Reset value: 0000'0000H

Address: ISP_VSM_BASE + 0010H		Mode : rw
Bit	**Name**	**Description**
31:	---	unused
10:	vsm_v_size	Vertical size. Range 64..1088
0	---	unused
Note: only even values are allowed: vsm_v_size[0] not writable and read returns 0.		

Register: ISP_VSM_H_SEGMENTS

Iteration 1 horizontal segments Reset value: 0000'0000H

Address: ISP_VSM_BASE + 0014H		Mode : rw
Bit	**Name**	**Description**

31:	---	unused
7:0	vsm_h_segments	number of 16 point wide segments enclosed by the first iteration sample points in horizontal direction. Range: 1 ... 117
Note: number of 1st iteration sample points = vsm_h_segments + 1		

Register: ISP_VSM_V_SEGMENTS

Iteration 1 vertical segments Reset value: 0000'0000H

Address: ISP_VSM_BASE + 0018H		**Mode : rw**
Bit	**Name**	**Description**
31:	---	unused
7:0	vsm_v_segments	number of 16 point wide segments enclosed by the first iteration sample points in vertical direction. Range: 1 ... 65
Note: number of 1st iteration sample points = vsm_v_segments + 1		

Register: ISP_VSM_DELTA_H

estimated horizontal displacement Reset value: 0000'0000H

Address: ISP_VSM_BASE + 001CH		**Mode : r**
Bit	**Name**	**Description**
31:	---	unused
11:0	delta_h	estimated horizontal displacement 12Bit two's complement. positive values indicate a displacement of the image from right to left (camera turns right)

Register: ISP_VSM_DELTA_V

estimated vertical displacement Reset value: 0000'0000H

Address: ISP_VSM_BASE + 0020H		**Mode : r**
Bit	**Name**	**Description**
31:	---	unused
11:0	delta_v	estimated vertical displacement 12Bit two's complement. positive values indicate a displacement of the image from bottom to top (camera turns down)

6.5 Interface Description

Table 6-3 ISP0 Interface Description

Module Pin	IO	Pad Name	IOMUX Setting
isp0_fl_trig	I	IO_ISP0flashtrigin_ISP1flashtrigin_TCPDcc1vconn_PMU1830gpio1a2	PMUGRF_GPIO1A_IOMUX[5:4]==2'b01
isp0_flash_trig	O	IO_ISP0flashtrigout_ISP1flashtrigout_PMU1830gpio1a3	PMUGRF_GPIO1A_IOMUX[7:6]==2'b01

Module Pin	IO	Pad Name	IOMUX Setting
isp0_perlight_tig	O	IO_ISP0prelighttrig_ISP1prelighttrig_PMU1830gpio1a4	PMUGRF_GPIO1A_IOMUX[9:8]==2'b01
isp0_shutter_trig	I	IO_ISP0shuttertrig_ISP1shuttertrig_TCPDcc0vconn_PMU1830gpio1a1	PMUGRF_GPIO1A_IOMUX[3:2]==2'b01
isp0_shutter_open	O	IO_ISP0shutteren_ISP1shutteren_TCPDvbussink_PMU1830gpio1a0	PMUGRF_GPIO1A_IOMUX[1:0]==2'b01

Notes: I=input, O=output, I/O=input/output, bidirectional

Table 6-4 ISP1 Interface Description1

Module Pin	IO	Pad Name	IOMUX Setting
isp1_fl_trig	I	IO_ISP0flashtrigin_ISP1flashtrigin_TCPDcc1vconn_PMU1830gpio1a2	PMUGRF_GPIO1A_IOMUX[5:4]==2'b10
isp1_flash_trig	O	IO_ISP0flashtrigout_ISP1flashtrigout_PMU1830gpio1a3	PMUGRF_GPIO1A_IOMUX[7:6]==2'b10
isp1_perlight_tig	O	IO_ISP0prelighttrig_ISP1prelighttrig_PMU1830gpio1a4	PMUGRF_GPIO1A_IOMUX[9:8]==2'b10
isp1_shutter_trig	I	IO_ISP0shuttertrig_ISP1shuttertrig_TCPDcc0vconn_PMU1830gpio1a1	PMUGRF_GPIO1A_IOMUX[3:2]==2'b10
isp1_shutter_open	O	IO_ISP0shutteren_ISP1shutteren_TCPDvbussink_PMU1830gpio1a0	PMUGRF_GPIO1A_IOMUX[1:0]==2'b10

Notes: I=input, O=output, I/O=input/output, bidirectional

Table 6-5 ISP1 Interface Description2

Module Pin	IO	Pad Name	IOMUX Setting
isp_clkin	I	IO_SPI2TPMtxd_I2C6TPMscl_CIFclkin_BT656gpio2b2	GRF_GPIO2B_MUX[5:4]==2'b11
isp_href	I	IO_SPI2TPMrxd_I2C6TPMsda_CIFhref_BT656gpio2b1	GRF_GPIO2B_MUX[3:2]==2'b11
isp_vsync	I	IO_VOPdclk_I2C7NFCscl_CIFvsync_BT656gpio2b0	GRF_GPIO2B_MUX[1:0]==2'b11
isp_data0	I	IO_VOPdata0_I2C2TPsda_CIFdata0_BT656gpio2a0	GRF_GPIO2A_MUX[1:0]==2'b11
isp_data1	I	IO_VOPdata1_I2C2TPscl_CIFdata1_BT656gpio2a1	GRF_GPIO2A_MUX[3:2]==2'b11
isp_data2	I	IO_VOPdata2_UPHYJTAGtrstn_CIFdata2_BT656gpio2a2	GRF_GPIO2A_MUX[5:4]==2'b11
isp_data3	I	IO_VOPdata3_UPHYJTAGtdi_CIFdata3_BT656gpio2a3	GRF_GPIO2A_MUX[7:6]==2'b11
isp_data4	I	IO_VOPdata4_UPHYJTAGtdo_CIFdata4_BT656gpio2a4	GRF_GPIO2A_MUX[9:8]==2'b11
isp_data5	I	IO_VOPdata5_UPHYJTAGtck_CIFdata5_BT656gpio2a5	GRF_GPIO2A_MUX[11:10]==2'b11
isp_data6	I	IO_VOPdata6_UPHYJTAGtms_CIFdata6_BT656gpio2a6	GRF_GPIO2A_MUX[13:12]==2'b11
isp_data7	I	IO_VOPdata7_I2C7NFCsda_CIFdata7_BT656gpio2a7	GRF_GPIO2A_MUX[15:14]==2'b11

Notes: I=input, O=output, I/O=input/output, bidirectional

Table 6-6 ISP to Camera Clk Interface

Module Pin	I	Pad Name	IOMUX Setting

	O		
cif_clkouta	O	IO_SPI2TPMclk_VOPden_CIFclkouta_BT656gpio2b3	GRF_ GPIO2B_IOMUX [7:6]==2'b11
cif_clkoutb	O	IO_MACcrs_UART3GPSsout_CIFclkoutb_GMACgpio3b7	GRF_ GPIO3B_IOMUX [15:14]==2'b11

Notes: I=input, O=output, I/O=input/output, bidirectional

6.6 Application Notes

In 3399, we have 2 ISP (ISP0&ISP1)here. Only ISP1 has the parallel data interface. What's more, ISP1 only support 8bit parallel data which means that the lower 4 bits of parallel data in will be connected to 0.

Chapter 7 HDCP22 Controller

7.1 Overview

The HDCP22 controller is an Embedded Security Module (ESM). This module is a self-contained module that can be integrated with HDMI cores to ensure DCP robustness rules for HDCP.

The ESM has a small MCU inside. It reads ESM Image for operation through the AXI interface.

The HDCP22 Controller supports following features:

- Supports HDCP Revision 2.2
- Bus Interface Features:
  - An AXI port for instruction fetch and shared R/W memory
  - An Identity Interface for secret keys used to secure the ESM
  - An Entropy Interface to a true random number generator
  - A Host Port Interface for an external host processor to send commands and get status from the ESM.
    (APB Interface)
- The Tx ports contain interfaces to a HDMI controller, where each port is factory configurable for HDMI support. The HDMI portion of the port contains the following interfaces:
  - HDMI video data and associated control
  - I2C interface for access to the remote end of the HDCP link
  - A GPIO interface for direct hardware signaling between the ESM and the controller
- MMU:
  - 4k/64k page size
  - TLB pre-fetch

7.2 Block Diagram

The following figure illustrates the HDMI controller connections with external interfaces. The ESM executes firmware from system memory external to the ESM which must be processed with the supplied tools as the firmware image is encrypted to the keys you created to present on the ID Interface. A host library (supplied in source code) is compiled with your application software running on the host processor to send commands to the ESM and monitor its status for results.

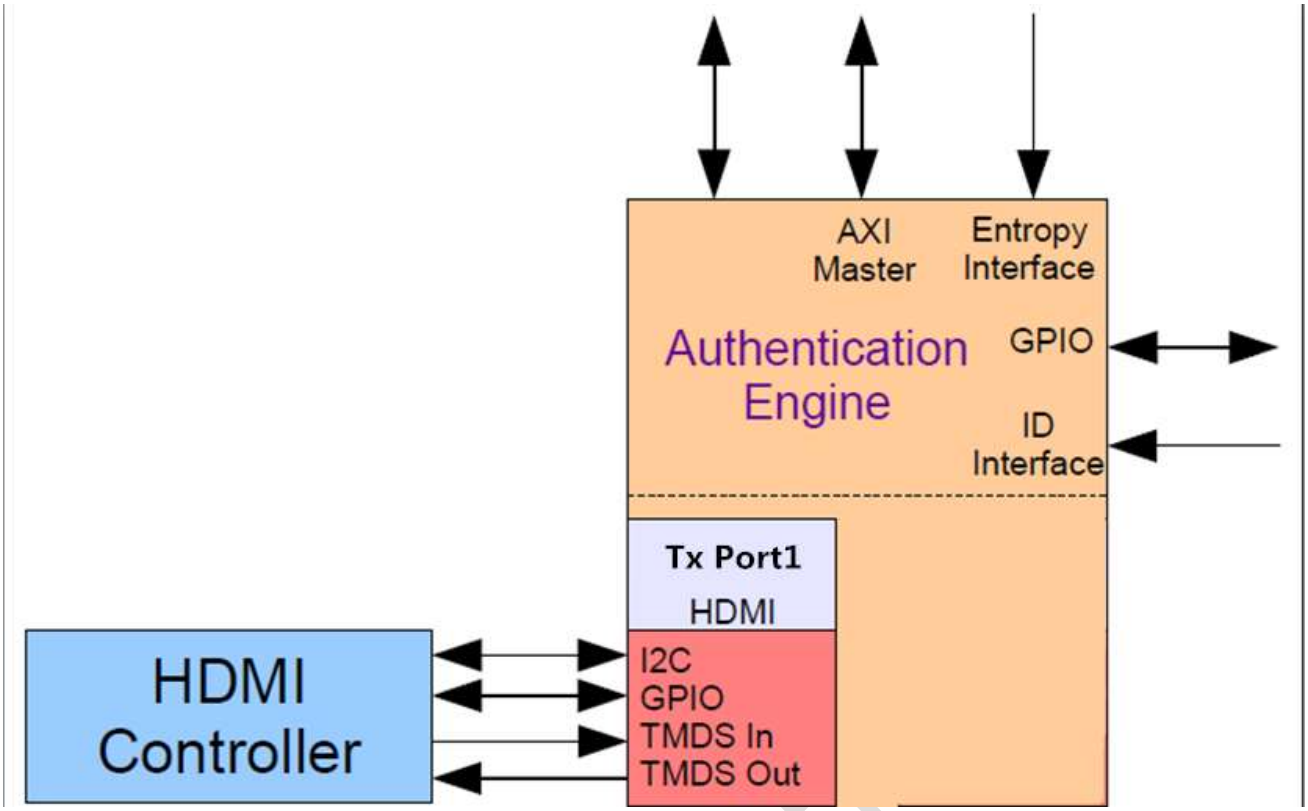


Fig. 7-1 hdcp22 Controller Block Diagram

The embedded security module is composed of two parts:

- The Authentication Engine (AE) contains a controller that runs the HDCP authentication process.
- The Content Encryption Engine (CEE) is an ESM component that encrypts data for the HDCP transmitter.

The following figure represents how the ESM is typically integrated in a SoC.

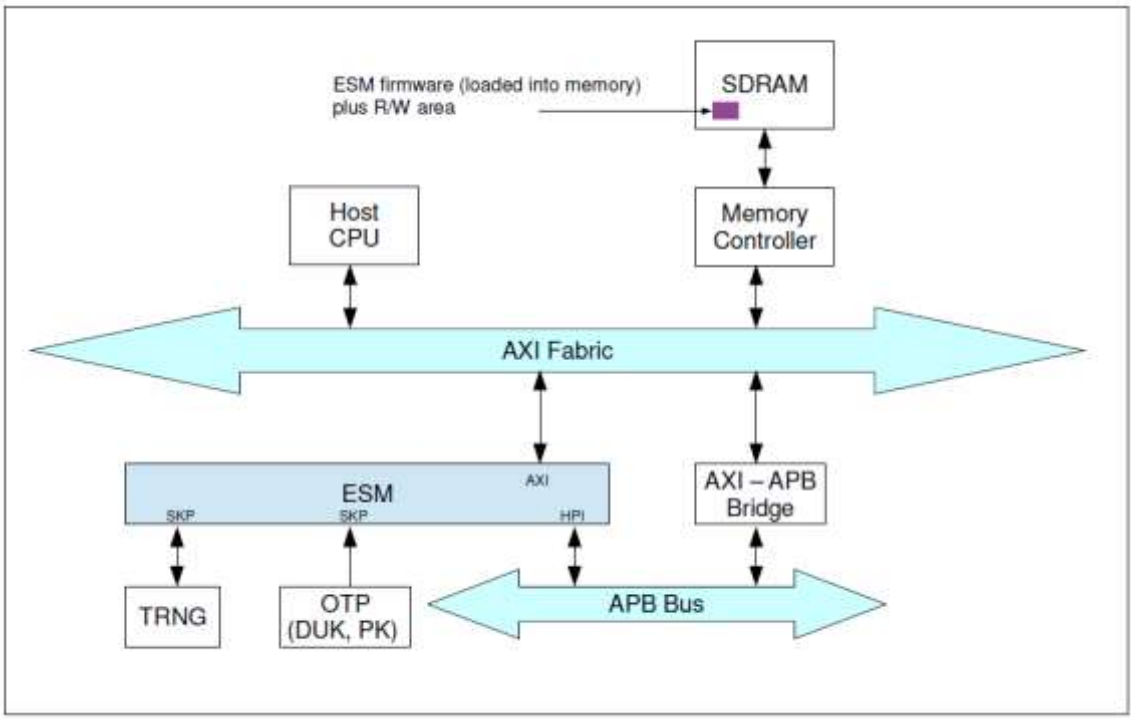


Fig. 7-2 Typical ESM Integration in a SoC

7.3 Function Description

7.3.1 AXI interface

The ESM requires continuous access to its firmware for operation, which is accessed through the AXI interface and usually placed a reserved portion of SDRAM. It also uses this interface for communicating messages with the external host processor to pass content such as SRM data, pairing information, and debug/logging information.
The ESM requires access to relatively fast and low latency external memory as it randomly accesses its firmware periodically to perform operations. For AXI transactions the average initial access latency may be up to 1000ns.
Note: *The ESM still functions in higher latency systems; however, the ESM may experience intermittent errors, such as failing to authenticate, as there are fixed timeout requirements during the authentication process which must be met. A system with persistent high latency memory accesses may prevent the ESM from fetching its firmware in a timely fashion resulting in protocol timeouts.Following Table summarizes the various requirements the ESM places on the RK3399's memory, assuming an AXI interface clock of 261 MHz and an average latency of 1000 ns.*

Table 7-1 ESM average memory bandwidth usage

Phase	Duration (ms)	Appropriate Bandwidth (Mbytes/sec)	Description
Bootup	100 (maximum)	5.0	Initial startup of ESM to Idle state.
Tx Authentication	525ms	1.5	ESM transmitter authentication phase including capability check.
Rx Authentication	525 ms	1.0	ESM receiver authentication phase.
Idle, authenticated	n/a	< 1.0, 4.0	ESM is either in the Idle state waiting to start authentication or in the authenticated state. The second number is when the ESM has debug logging enabled.

The external host memory required by the ESM must be physically contiguous and allocated before the ESM can be started. The ESM Image and R/W memory buffer addresses must be 4K aligned otherwise the ESM cannot properly access the memory. Following table describes the requirements.

Table 7-2 ESM average memory bandwidth usage

Size (bytes)	ESM Access	Purpose
~256K	Read Only	Contains the ESM firmware. This size varies depending on the particular configuration of the ESM you are using.
16K + p*n*256 (Tx) (p is the number of transmitters and n is the number of paired devices supported)	Read / Write	Bidirectional communication buffer to exchange data with the Host. Messages such as SRM updates, pairing data, and logging information are placed in this area by the host and the ESM. The number of pairs supported by this parameter is defined in the configuration file.

In RK3399 the provided ESM host application library allocates a small amount of the processor's memory space, which is accessible by the ESM. Communication with this interface is provided by the ESM host application library.

7.3.2 HPI Interface

The external host issues commands to the ESM through the HPI which supports a limited set of commands such as:

- Enabling and disabling of security on the link
- Enabling debugging/logging
- Retrieving pairing information
- Updating the SRM
- ESM status

Communication with this interface is provided by the ESM host application library.

7.3.3 APB interface (HPI)

The external host issues commands to the ESM through the HPI. The ESM supports a limited set of commands such as:

- Enabling and disabling of security on the link
- Enabling debugging/logging
- Retrieving pairing information
- Updating the SRM
- ESM status

The external host must issue a SRM list to the ESM when one is available, according to the requirements of DCP LLC.

Communication with this interface is provided by the ESM host application library.

7.3.4 Identity Interface

This interface contains the secret keys the ESM requires to implement its security. The KPf and DUK signals on this interface must be secure from tampering and external user observation as it is used by the ESM to create session keys and other cryptographic secrets required for operation.

When integrating the ESM into your design, you must take to ensure that these requirements are met otherwise the operation of the ESM can be compromised.

Table 7-3 Secure Key for ESM

Description	Purpose
Platform Key (PKf)	A customer created secret random key used to decrypt the ESM firmware. The KPf is intended to be common across a deployed model of a product.
Device Unique Key (DUK)	A customer created secret random key used to decrypt the DCP key data and to encrypt and decrypt content unique to the ESM such as the pairing message content. It is strongly recommended this value should be unique for every unit.
Device Number (Devnum)	This is a non-secret device number and is currently not used.

Note: *The PKf and DUK must be kept confidential as exposing either one compromises the security of the ESM.*

7.3.5 Entropy Interface

This interface connects to a True Random Number Generator (TRNG). The nonce data on this interface must be secure from tampering and external user observation as it is used by the ESM to create session keys and other cryptographic secrets required for operation.

Table 7-4 Entropy Interface

Description	Purpose
Entropy Valid	This is the nonce data from the TRNG. The value is used to seed the ESM's PRNG which is used to generate keys for the authentication process and session keys. The value must be truly random and not generated by another PRNG, as per the HDCP for HDMI specification, Section 2.13 (Random Number Generation).

7.3.6 GPIO Interface

This interface contains a number of general purpose inputs and outputs which can be used by the host to monitor the status of the ESM.

7.3.7 HDMI Interface

The HDMI interface contains logic to apply content protection to the Data and Video Islands as the TMDS data passes through the ESM.

Table 7-5 Entropy Interface

Description	Purpose
I2C	A standard I2C serial interface for HDCP protocol communication with the remote device, mapped by the controller onto the DDC interface.
GPIO	Direct signals between the controller and the ESM to indicate the status of the ESM to the controller, and to signal the ESM
TMDS In	TMDS data output from the controller. For a Tx this is the unencrypted data, for the Rx this is the encrypted data.
TMDS Out	TMDS data input to the controller. For a Tx this is the encrypted data, for the Rx this is the decrypted data.

7.3.8 HDCP22 Controller Behavior

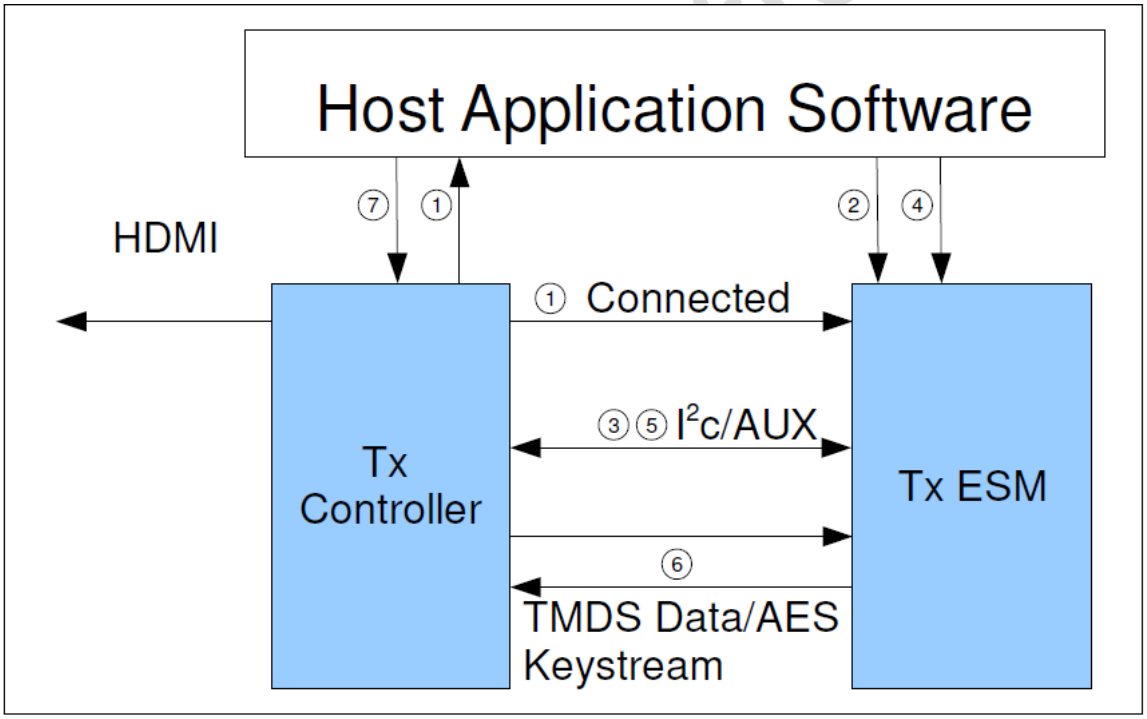


Fig. 7-3 Transmitter Authentication

Hdcp22 controller in RK3399 is a transmitter, it works as following steps:

1. The controller asserts the Connected signal to the ESM. The application software1 receives the notification from the controller. For HDMI operation the ESM outputs a fixed pattern (the BSOD value) on the TMDS data output.
2. The application software issues the HLC_HDCPTX_SetCapability() command which causes the ESM to perform a capability check with the receiver. Before this point in time the ESM does not know the capability of the Rx so the port's capable GPIO output signal is not asserted.
3. The ESM queries the receiver. If the receiver does not support HDCP 2.2 then the port's not_capable GPIO output is asserted. The application software should then check if the receiver supports HDCP 1.4 (or no link protection) and take appropriate action; the ESM is no

longer required. If the receiver supports HDCP 2.2 then the capable GPIO output is asserted and the ESM transitions to a pre-authorized state. For HDMI operation this means unencrypted low value content is permitted on the video path (TMDS interface).
4. If the receiver supports HDCP 2.2 the application software issues the HLC_HDCP_Authenticate() command to the ESM. As a security feature the ESM enforces a timeout (set in the configuration file) after the receiver indicates it is HDCP 2.2 capable to the time the HLC_HDCP_Authenticate() command must be issued. If you exceed this timeout you must repeat the process from step #2. (When the port is configured for HDMI it will switch its TMDS output back to the fixed pattern output).
5. The ESM initiates authentication with the receiver and successfully completes authentication (or not). The application software and the HDMI controller are appropriately notified (authenticated and authentication_failed outputs asserted accordingly).
6. If authentication is successful the ESM starts to encrypt the TMDS data (HDMI).
7. The application software can now send high value content securely on the link.
Following successful authentication the ESM periodically checks the status of the connected receiver. If a response is not received, or the receiver requests re-authentication the ESM immediately outputs a fixed pattern on the TMDS output (HDMI), asserts the outputs authentication_failed along with a reath_req, and returns to the Idle state. To re-authenticate you must call HLC_HDCP_Authenticate() to drop authentication and then call the function again to start authentication.

7.3.9 HDCP22 Software Initialization

An external host controller (ARM Core or MCU) allocates memory, initializes the ESM, and enables the ESM controller. The general reset and startup sequence is:

a. Configure clocks for hdcp controller.
b. Load PKF & DUK from effuse to gasket.
c. The ESM reset is de-asserted and the ESM enters a reset state.
d. The host allocates contiguous memory for the firmware and R/W areas. The buffers are 4K aligned.
e. The host configures the ESM's HPI interface, defining the physical memory pointer for the ESM firmware.
f. The host copies the ESM firmware from persistent storage to the firmware memory location.
g. The host enables the ESM controller, putting it in a running state. At this point the ESM initiates transactions on the AXI bus to fetch its firmware.
h. ESM asserts a GPIO to indicate it is booted to indicate it can accept commands. The status can also be monitored from the HPI interface.

The ESM host application library provides the startup sequence from steps d through h.

7.3.10 Autostart

The autostart feature is an option which permits a transmitter or receiver port (configurable per port) on the ESM to autonomously take over the detection of a connection and run through the authentication process without intervention from the external host. In the event of an error the port automatically retries up to a specified number of attempts (configuration based) before idling requiring intervention from the host.
For a transmitter this feature automates the capability checking and authentication along with any reauthentication which may be required due to link errors. For a receiver this feature enables the port to immediately respond to authentication requests without host intervention.

7.3.11 Key Usage

There are two secret, 128 bit keys you are responsible for creating for use by the ESM.
The Platform Key (KPf) is used by the ESM to decrypt its firmware. It is recommended this key

be common for all ESMs deployed for a particular product as it permits a common (encrypted) firmware image to be deployed.

The Device Unique Key (DUK) is used by the ESM to protect secrets unique to the device such as HDCP receiver keys and locally generated data such as pairing information. Although it is not required, it is strongly recommended this key be unique for every different unit deployed in a product so that if the kPf is and DUK are compromised, device specific secrets for only that unit are exposed. Using a common DUK for all devices could permit device specific secrets for all devices to be exposed.

As shipped from the factory, the firmware cannot be used as-is and must be processed with tools that are provided with the ESM software package. Figure 1-3 illustrates the tools and the flow that are required to produce encrypted ESM firmware. You edit the firmware.aic file supplied with the firmware image and replace the factory test/simulation values with your secret KPf and DUK keys.

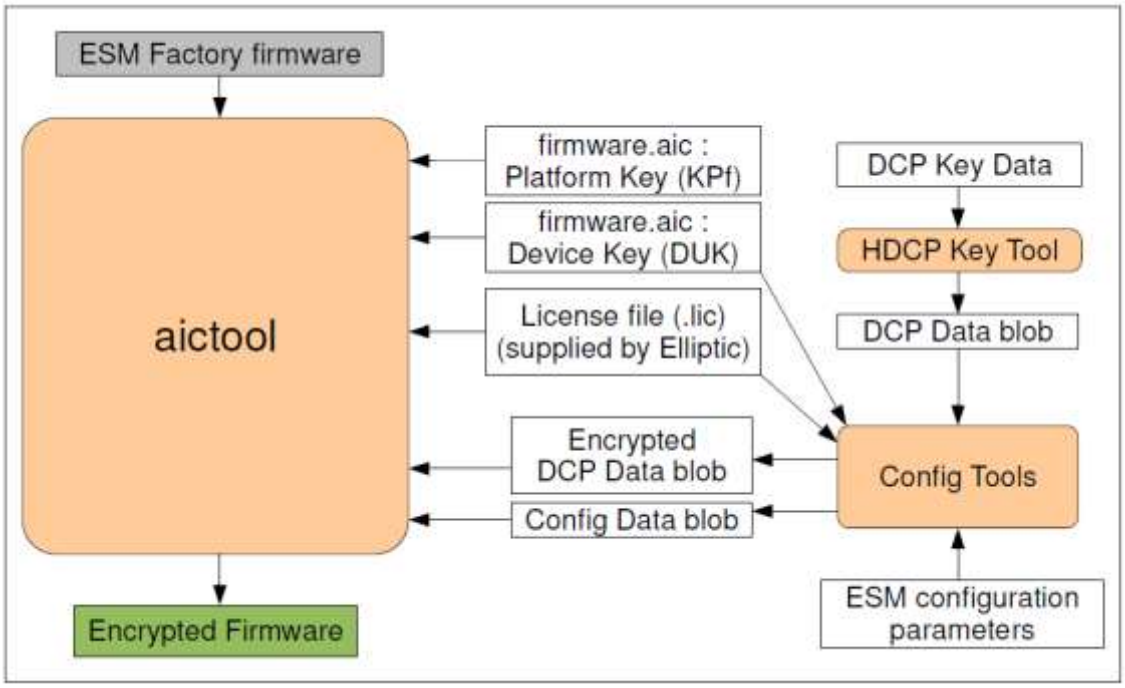


Fig. 7-4 ESM Image tool flow

The DCP Tx key data is common for all transmitter ports whereas the DCP Rx key data is unique for each receiver port.

To facilitate manufacturing it is highly desirable to build and deploy a common software image for all units. If your ESM only contains transmitter ports then it is possible to do this, however if you also have receiver ports you are required by DCP to have a unique receiver key for each receiver in your design.

7.4 Application Notes

7.4.1 Host Application Software

The ESM package contains a series of tools and a run-time library as bellow:

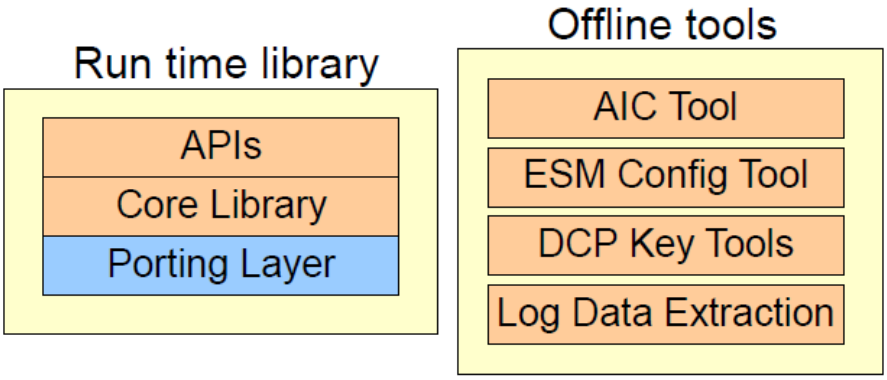


Fig. 7-5 ESM software

7.4.2 Run Time Library

This library is provided as source code and is used by the host application processor to control the ESM.
Setting the configurable options of the ESM is not provided through APIs for security reasons. It is instead embedded into the ESM's Image as part of the process of building a deployable image.
The APIs provide a minimal interface to the ESM, which include the following:

- Load/Initialize firmware image
- Start authentication to secure a link
- Terminate an authenticated link
- Collect logging data
- Get/Set pairing information
- Update SRM data
- Status updates

Sample code is provided and demonstrates how to use the various APIs. In addition, a software API reference guide is included and provides details on the API calls and their parameters.

7.4.3 Offline Tools

There are three separate offline tools that are required to build a deployable image for the ESM as shown in Figure ESM Image tool flow and one tool for logging information. All of these tools are developed to run on a 32 bit Linux system.

7.4.4 Configuration Tool

The troot_base_config_interface tool is used to convert the various configuration files into a data blob to be used by the aictool which creates the encrypted ESM firmware. There are a number of different configuration files which the tools reads, with each configuration file containing a mix of factory configured parameters, and user-adjustable parameters.
This tool also requires the firmware.aic file in order to generate the data blob.

User Parameters for Configuration Files

The following table indicates which parameters in the configuration files are user-adjustable and other non-described parameters should not be changed. A basic description of the parameter is included below, see the configuration file's comments for a more complete description.

Table 7-6 Configuration files

File Name	Parameter	Description
troot_base_config.cfg	[LOGGING_MODE]	Logging on/off
	[LOGGING_LEVEL]	Sets the verbosity of the output log messages.
	[RESEED_TIMEOUT]	Specifies the time the ESM will wait for the TRNG to supply a new nonce before reporting an error

File Name	Parameter	Description
	[RESEED_AUTO_INTERVAL]	By default the ESM will periodically query the TRNG for a new nonce at the period specified.
	[CPU_FREQ]	Sets the frequency of the esm_clk input. Mandatory to change.
troot_hdcpmgr_tx.cfg	[SRM_VERSION]	Denotes whether the SRM is to be checked or not and the minimum version number permitted.
troot_hdcptx.cfg	[I2C_FREQ]	(HDMI) Sets the default I2C frequency. Can be changed via an API.
	[I2C_USE_SHORT_READ]	(HDMI) Sets whether the interface uses short reads for status requests. Can be changed via an API.
	[CEE_BSOD]	(HDMI) Sets the 24 bit fixed pattern value output by the ESM. See the description following this table for more details.
	[AUTO_START]	Sets the default startup state of the Autostart feature
	[HDCP_TIMEOUTS]	Sets whether the ESM enforces the HDCP timeout periods. Should be enabled only for testing and/or debugging.
	[CEE_FRAME_CNT_DEBUG]	(HDMI) The ESM emits periodic log messages once authenticated, based on the number of VSYNC pulses counted by this parameter.
	[PAIRING_ENABLED]	Sets whether pairing will be enabled or not
	[MAX_PAIRING_DEVICES]	Sets the maximum number of paired devices supported per port. Note the external R/W memory requirements increase based on this setting, and the number of Tx ports in your design.
	[MEM_PAIRING_SIZE]	Sets the amount of R/W memory the pairing data will occupy.
	[CAPABLE_BYPASS_TIME]	(HDMI) Sets the maximum amount of time the ESM will enable low value content after a capability check before switching back to a fixed pattern output. See HLC_HDCPTX_SetCapability in the API guide.
	[LVC_TIMEOUT]	(HDMI) Sets the maximum amount

File Name	Parameter	Description
		of time the ESM will enable low value content without a capability check. See HLC_HDCPTX_EnableLowValueContent in the API guide.
	[LVC_EXPIRED_CNT]	(HDMI) Sets the maximum number of LVC timeouts permitted.

The [CEE_BSOD] is a 32 bit decimal value which parameter represents fixed data output on the TMDS data bus if the ESM encounters an authentication issue or detects attempts have been made to tamper with it. The value is only relevant for ports configured for HDMI. This 32 bit value is output as follows:

Table 7-7 ESM BSOD Output Mapping

BSOD Bit Positions	HDMI Controller TMDS Data Channel
7..0	O_tmds_ch0 [7..0]
15..8	O_tmds_ch1 [7..0]
23..16	O_tmds_ch2 [7..0]
32..24	Not used

7.4.5 HDCP Key Tools

This tool (hdcpkeys) is used to create a DCP key data file, which is required to build the encrypted DCP data blob needed for creating the encrypted ESM firmware. The tool reads a configuration file that contains the Rx or Tx key information from DCP in clear text and outputs a structured data file for the configuration interface tool to encrypt with the appropriate secret keys.

The tools can also accept the DCP published key files themselves.

7.4.6 AIC Tool

The aictool tool is used to create the encrypted ESM firmware. To build the encrypted firmware, you must first create the data files for the DCP keys and the configuration. These files, along with an input configuration file for this tool are used to build an image that can be used by the ESM. In addition to specifying the Platform and Device Unique Keys in the configuration file, there are additional keys that also must be specified as noted below.

Content Randomization

There are two separate values in the firmware.aic file, IK and IVc (128 bits and 96 bits respectively), which you must randomly generate to create a new encrypted ESM firmware image. Failure to do this puts secret data in the ESM firmware at risk of being compromised.

7.4.7 Log Data Extraction

The logging information from the ESM is output in a proprietary format. This tool is used to produce readable output of captured logging data content.

The Host Library contains a core library component which includes all the functions necessary to use the ESM. The library is built using portable C code and uses various abstraction functions to allow for migration to different platforms. Before using the ESM in your system you must properly implement the abstraction components specific to your platform.

There are two distinct abstraction components used by the Host Library, the System Abstraction Layer and the Host Library Driver (HLD) component. The System Abstraction Layer (or Common Component) defines system level functions used by the Host Library, such as malloc, memcpy, etc.

These functions are linked into the Host Library when it is built.

The Host Library Driver (HLD) component establishes a communication between the library and the physical ESM hardware, including managing the memory required for the ESM Image and the read/write area. This is a run-time plug-in module that is defined in your application and specified as a parameter to the ESM initialization function.

The figure below illustrates the abstraction components used by the Host Library package. This figure demonstrates one example where there are three separate ESMs in the system, requiring (typically) three separate HLD instantiations. Consult the ESM Host Library API guide for more details on the HLD implementation.

7.4.8 Host Library

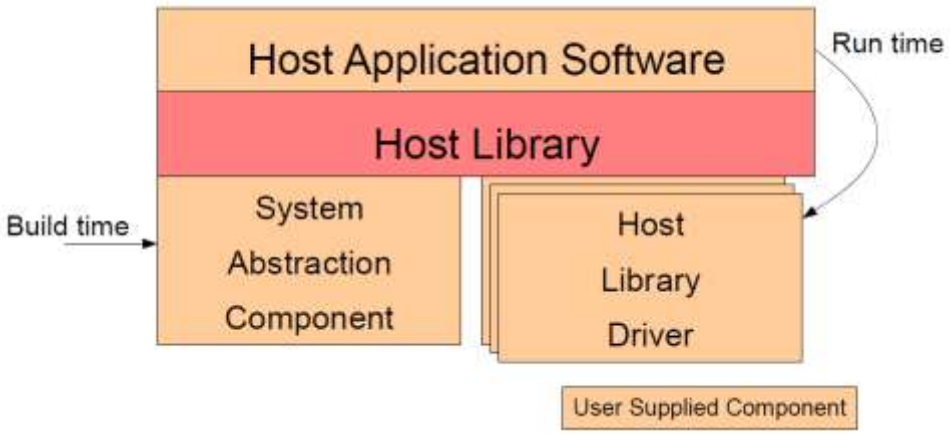


Fig. 7-6 Host Library Layers

The Host Library provides a number of sample applications using the ESM with the library. The applications demonstrate using the library in a User Space Linux application:

- Repeater/Converter (Linux) [Planned in later releases – not currently available]
- Transmitter (Linux)

All the sample applications demonstrate API usage, loading the ESM firmware, and running a specific ESM application.

The sample applications provided as a Linux User Space application communicate to the ESM hardware through a Linux Kernel driver which is implemented as a Host Library Driver (HLD) plug-in.

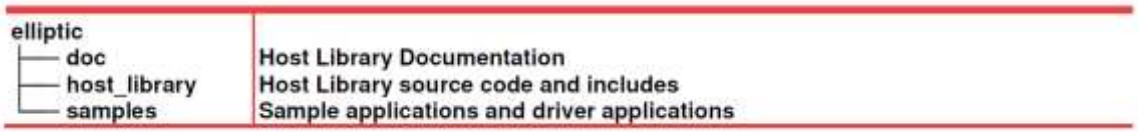


Fig. 7-7 Development Tree Overview

Transmitter

There is a sample transmitter applications provided in the samples folder:
hdcp_tx.c is a Linux based example and utilizes file IO and threads.

Linux OS

Sample applications are targeted for a Linux User Space application environment. In order to use them a custom kernel driver is used and the HLD plug-in for the host library was made to call IOCTLs which mapped to the appropriate interfaces in the kernel driver module to access the ESM.

To build for this platform run the makefile from the esm_host_lib folder:

make samples

The implementation of the platform specific APIs (for the Linux example) are in the following files:

./host_library/cal/system/sample_platform/elliptic_common.c

./host_library/cal/system/sample_platform/elliptic_log.c
./host_library/include/elliptic_platform_specific_system_type.h
./host_library/include/elliptic_platform_specific_system.h
You can change these implementations as needed for your specific platform.

Debugging Suggestions

The host library driver interface is relatively straightforward to implement as the host library itself takes care of the required protocols to communicate with the ESM. The detailed HPI interface and command protocols are considered proprietary information, however, the information presented below can be followed if you are having difficulty getting the ESM operating in your environment.

Chapter 8 DP Controller

8.1 Overview

DisplayPort controller (DPTX) is a digital display interface. It supports up to 5.4Gpbs bandwidth and High-Bandwidth Digital Content Protection.
It supports the following features:

- Standards Specification
  - DP1.3 standards
  - CEA-861-F
  - IEC–60958
  - IEC-61937
  - HDCP22

8.2 Block Diagram

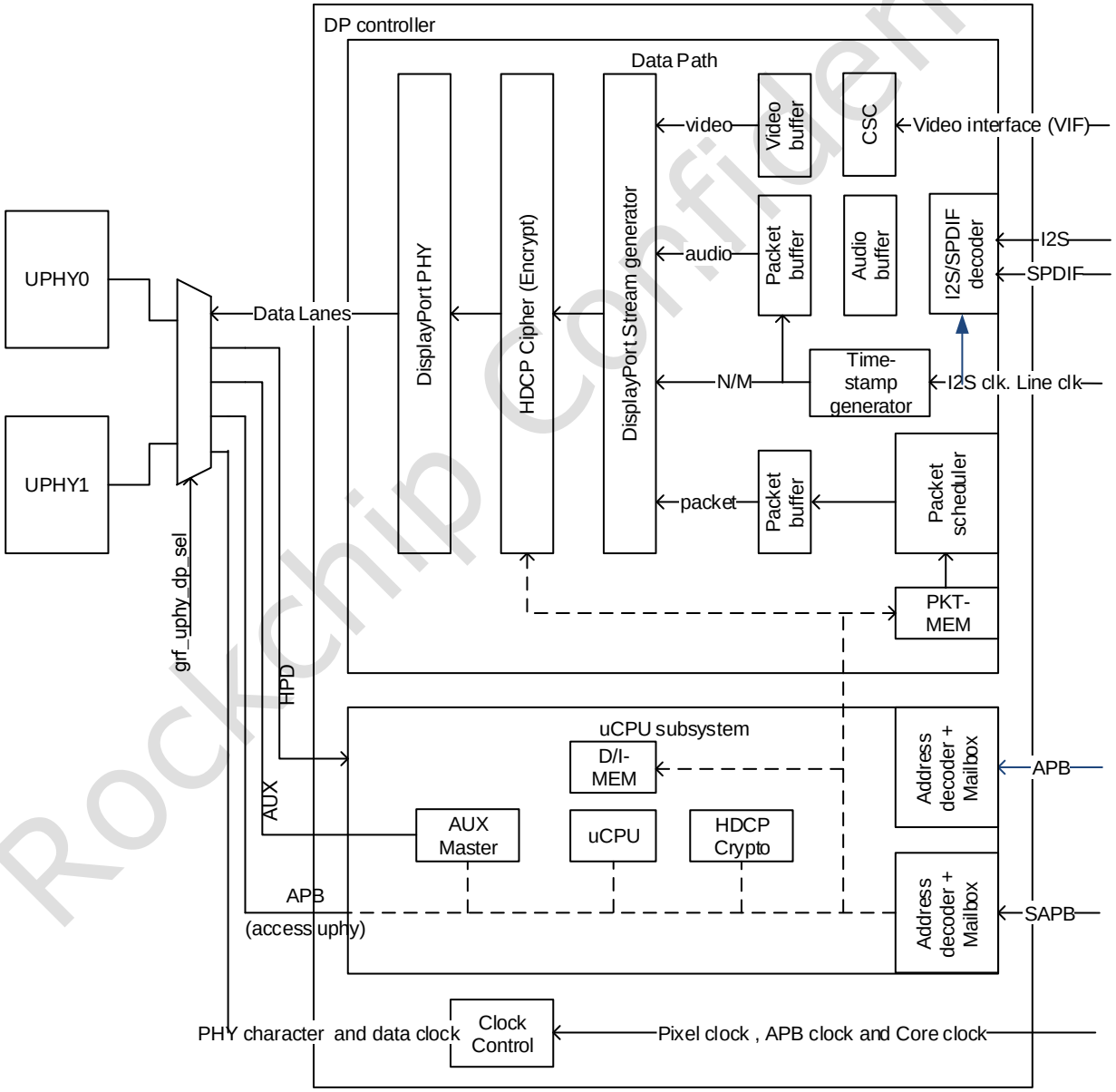


Fig. 8-1 DP controller Block Diagram

8.3 Function Description

8.3.1 APB Interface

The HD Display TX controller has the following APB slave ports that are controlled by the host processor:

1) APB Slave port (APB)
   a) used as the main control interface between the host processor and the HD Display TX controller.
   b) used in different methods during boot
   c) used for directly loading the FW into the memories
   d) used for directly access several HW modules and for communicating the internal uCPU over the mailbox channel.
2) SAPB Slave port (SAPB) – used for secure connection, that is, HDCP key loading between the host processor and the uCPU through mailbox and pre-defined commands.

The uCPU controls different modules over an internal APB bus. This bus could be controlled (for debug purpose) during boot time. The internal APB bus has an output APB master port which is used to manage the PHY.

Mailxbox channel (APB) generates an interrupt-level signal when its received FIFO is not empty or when its transmitted FIFO is full. The interrupt is cleared when the MAILBOX_INT_STATUS register is read.

8.3.2 Video Interface

The video timing of the video-interface bus (VIF) follows the specification in CEA-861-F Annex L.

Table 8-1Pixel Mapping

Video Bus	RGB / YCbCr 4:4:4				4:2:0 / 4:2:2				Y Only
Bit Width	8	10	12	16	8	10	12	16	16/12/10/8
Channel 2	R/Cr				Cb/Cr				
[47:40]	Cr[15:8]	Cr[15:6]	Cr[15:8]	Cb[15:0]	C[15:8]	C[15:6]	C[15:4]	C[15:0]	
[39:38]									
[37:36]									
[35:32]									
Channel 1	G/Y				Y				
[31:24]	Y[15:8]	Y[15:6]	Y[15:4]	Y[15:0]	Y[15:8]	Y[15:6]	Y[15:8]	Y[15:0]	Y[15:0] Y[15:4] Y[15:6] Y[15:8]
[23:22]									
[21:20]									
[19:16]									
Channel 0	B/Cb								
[15:12]	Cb[15:8]	Cb[15:6]	Cb[15:4]	Cb[15:0]					
[11:8]									
[7:6]									
[5:4]									
[3:0]									

The HD Display TX controller expect the interlaced timing format to comply with the specification defined in CEA-861-F Figure 14. The field information will be extracted from the

input signal (hsync,vsync and de) and will be propagated toward the framer (i.e VB-ID field bit in DisplayPort).

8.3.3 Color Space Conversion Module

An add-on Color Space Conversion (CSC) module is optionally provided. It supports the video-timing defined in CEA-861-F.
The following conversion operations are supported:
1) Color space conversion from RGB to YCbCr
2) Color space conversion from YCbCr to RGB
3) YCbCr up-sampling from 4:2:2 to 4:4:4
4) YCbCr down-sampling from 4:4:4 to 4:2:2

The CSC module is configurable over APB slave port.

8.3.4 Audio Interface

Audio samples are input to the HD Display TX controller over SPDIF or I2S interface. Only single stream is supported.
The following sequence is supported:
1) Samples are decoded
2) Converted into a SPDIF format (if needed)
3) buffered (compensating for the video active period)
4) mapped into an audio info-frame packet.

The I2S interface could be configured to support multiple physical channels, i2s_data[n], (n=1, 2, 4) where channels could be configured with variable TDM time slots (m = 2 or 8).The time slot size is 32, 24 or 16 bits, supporting variable word length (28, 24, 20, 16) configured as left or right justified.

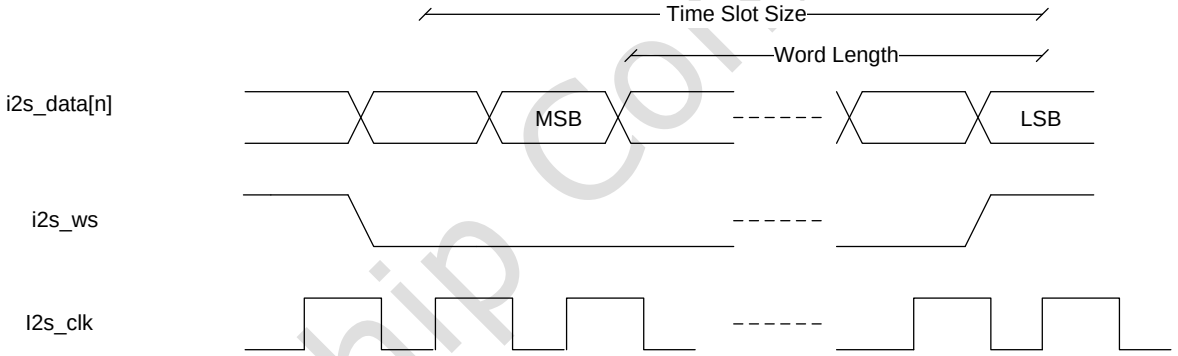


Fig. 8-2 I2S bit allocation (right justification)

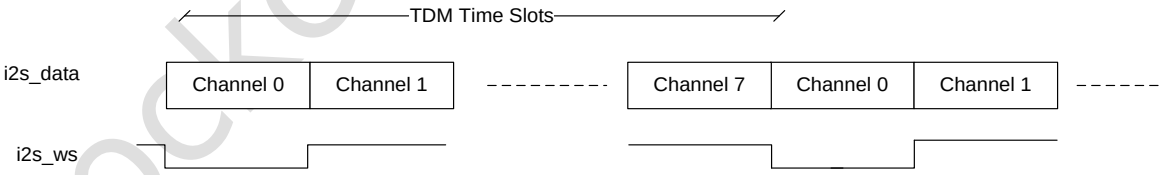


Fig. 8-3 I2S TDM time slot allocation (M=8)

The I2S interface can carry audio samples in one of the following formats:
LPCM audio samples capture 16 up to 24 bits, as shown in the following figure (left justified, right justification is also supported), where other bits are padded to zero.

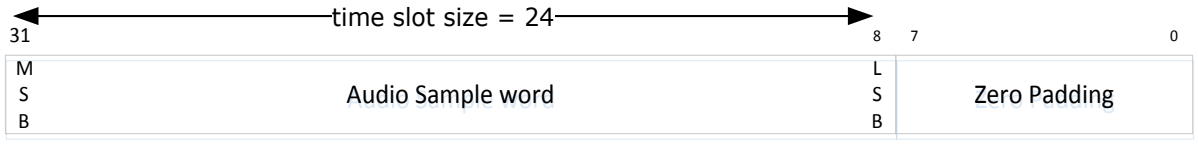


Fig. 8-4 Audio L-PCM sample format

"SPDIF" audio samples format as defined in IEC–60958 and IEC-61937 – could carry L-PCM or compressed audio format

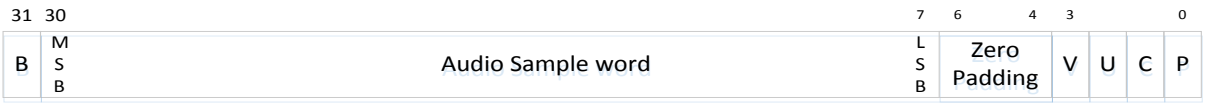


Fig. 8-5 Audio SPDIF sample format

The SPDIF interface comply with S/PDIF specification, S/PDIF data is decoded.
For proper decoding, a source_ref_clk_in must be provided with frequency greater than 10 times of the bit-time frequency.

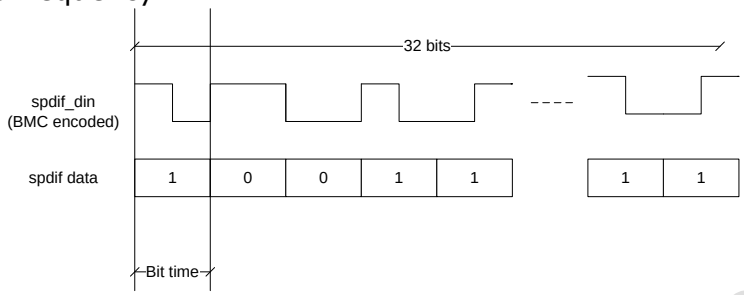


Fig. 8-6 SPDIF input interface

The following block diagram shows the audio path from I2S/SPDIF interface to creation of audio info-frame.

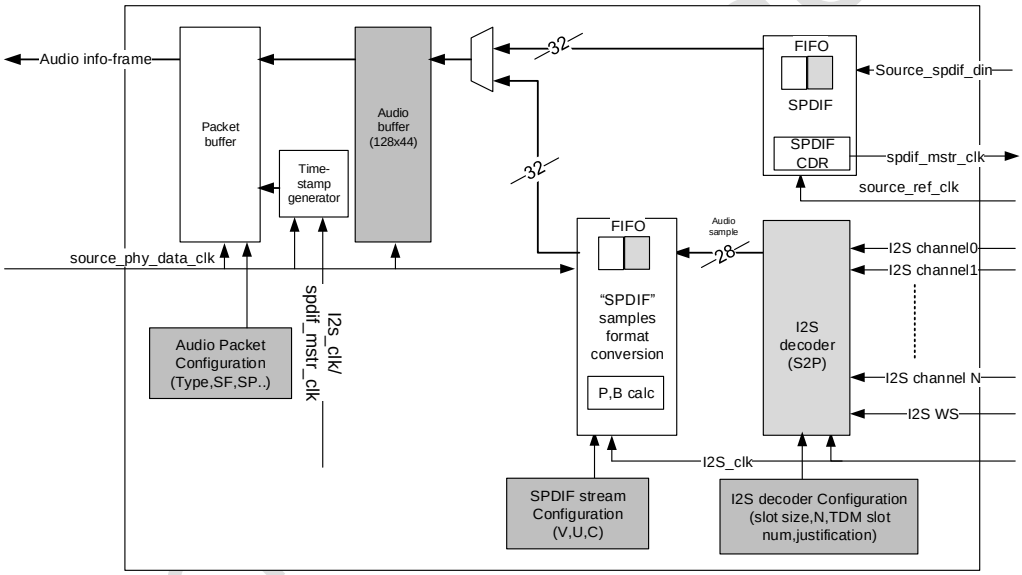


Fig. 8-7 Audio data path

8.3.5 Info-frame processing

Info-frames are encoded over the video stream vertical blanking period.
Audio and video meta-data are written into the PKT-MEM by the host processor (directly accessed over the APB bus) only when changed, to be then read and encoded by the HD Display TX controller packet-scheduler over the stream once per frame. Parity bytes (in DisplayPort) are generated by the DP controller. Up to 16 info-frames are supported. When writing info-frames into the PKT-MEM the host must update the packet allocation table.

8.3.6 DP controller Data Path

1) DPTX Stream generator block
The DPTX Stream Generator controls the insertion of Video stream data over the main stream, and Audio and DP info-frames over the Secondary stream.
This module inserts all the control symbols (BS, BE, SS, SE…) and additional data, such as VB-ID, MSA, MVID and MAUD as defined in the standard.
2) DPTX PHY block
The DPTX PHY block integrated in the HD Display TX controller comply with DisplayPort PHY logical sub-block as defined in the DP 1.3 standard.
It implements the following functionalities:

- Scrambler
- Encoder
- Inter lane skew insertion
- Training pattern generation – TPS1,2,34, PRBS7 and 80-bit custom training pattern generation bypassing the scrambler and encoder.

The DPTX PHY block is controlled by the uCPU during link training.

3) DPTX AUX Master

The dp_aux block implements the physical (Manchester-II coding) and the link layers of the Auxiliary Channel, and messages are created and parsed by the uCPU.

The Protocol layer, that is, HDCP and EDID is managed by the FW.

8.4 Register Description

8.4.1 Internal Address Mapping

Please refer to HTML format register list.

8.5 Interface Description

There are two UPHY in RK3399, DPTX can communicate with only one at the same time. This is selected by grf_uphy_dp_sel. When grf_uphy_dp_sel set to 1, DPTX is connected to UPHY1. HPD input of DPTX controller is controlled by grf_dptx_hpd_sel (GRF_SOC_CON26[13:12]), as in following picture.

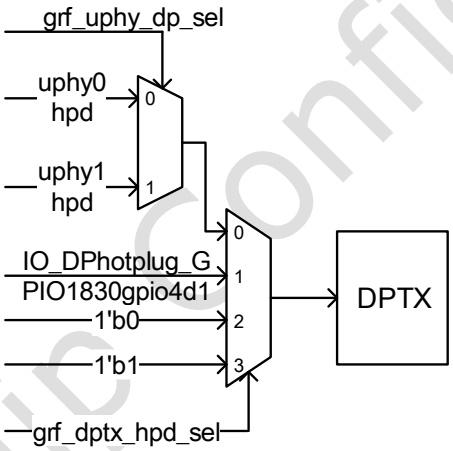


Fig. 8-8 DPTX hpd selection

grf_con_dp_lcdc_sel is the selection signal for choosing DPTX vif source, from VOPB or VOPL.

8.6 Application Notes

8.6.1 Introduction

The following document describes the programming interface between host processor and the DPTX which has an integrated Xtensa processor executed the embedded firmware (FW).

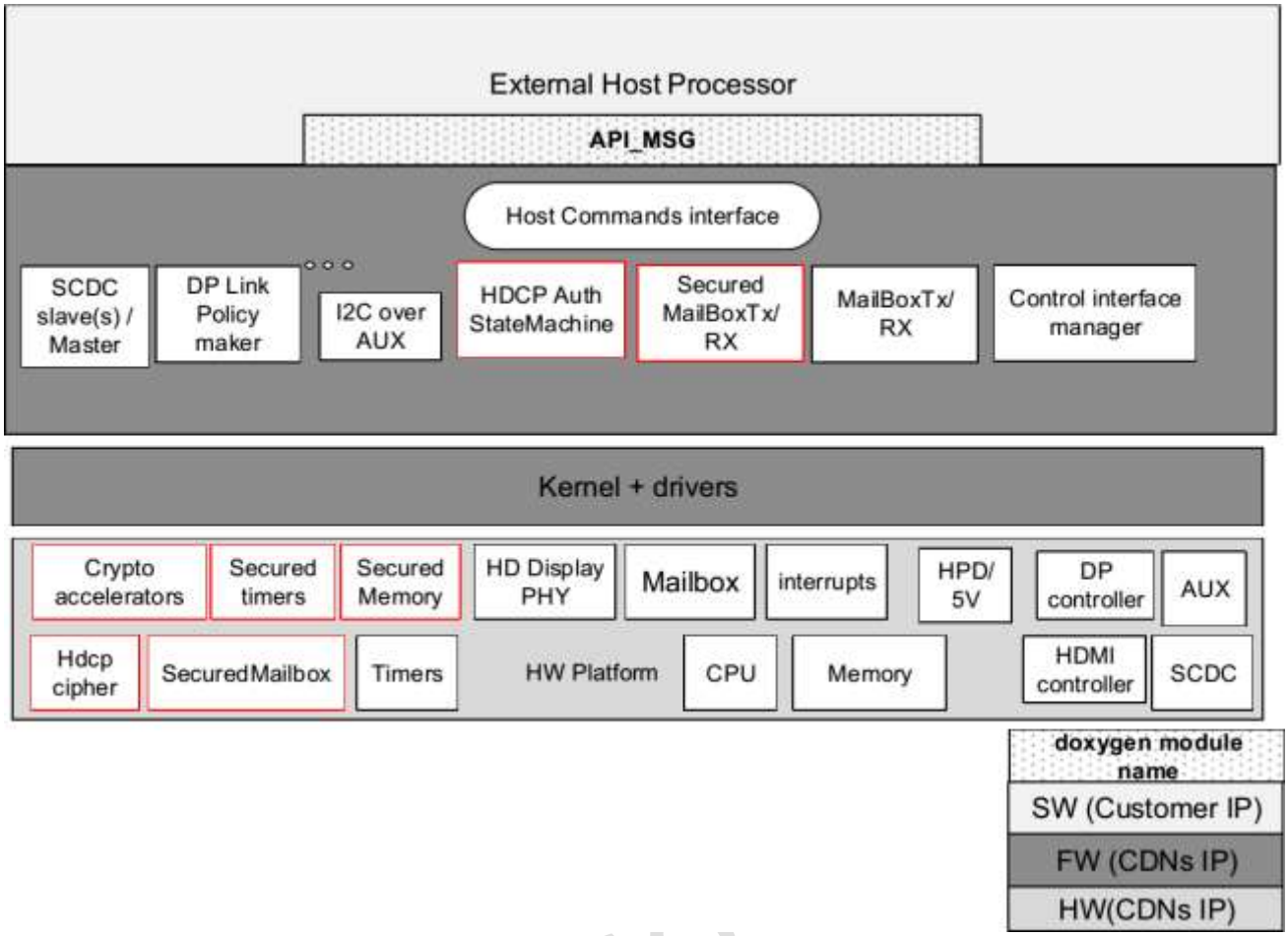


Fig. 8-9 DPTX SW architecture

8.6.2 DP Link Policy Maker

This block is responsible for performing the link training and link maintaining during normal operation. The external host needs to support it with the capabilities including:

- Max link rate
- Lanes count
- Max voltage swing
- Max pre-emphasis
- Test patterns supported

The link training is started automatically after obtaining the information mentioned above and HPD signal detection. After the training is finished, the host may get (if not disabled) the message containing training results.

After the training is finished, DP TX Link module is responsible for keeping the link synchronized. Is informs the host about any changes in the Sink device, like disconnection from the port.

8.6.3 DP TX Link

DP TX Link is the lowest firmware layer responsible for handling read or write request via AUX and I2C-over-AUX transactions. It processes the requests from DP Link Policy Maker and sent by the host to read EDID or access the DPCD memory space.

DP TX Link needs read/write requests from higher firmware layers. It translates them into AUX or I2C-over-AUX transactions between Source and Sink devices. After processing the request the requesting module is asynchronously informed about the request result: reply command from the Sink, number of data written or read and the data itself if needed. This module is able to process only one request at a time.

8.6.4 DP TX Mail Handler

This block handles the commands sent from external host to DP TX controller and generated the requests for DP TX Link. It also formats the response messages for the host.

After a message is found in the mailbox, the mail handler releases the memory buffers, so it doesn't block communication with other modules. Then if it is necessary, it sends a request to lower layer to communicate with Sink device. After the response is processed, the mail handler waits for the mailbox to be available and sends the reply. This module is able to handle only one message at a time, so next message directed to the DP module will block the mailbox until the previous one is processed.

Access	Registers Space	Block	Address Base [19:0]	Size
APB	CSC	CSC	0x40000	
	PIF	PIF	0x30800	
	AIF	AIF	0x30000	
	Debug Source+Internal		0x00000	
SAPB	DMEM (Opt APB)		0x20000	upto 64KB
	IMEM (Opt APB)		0x10000	upto 64KB
	Debug Source+Internal		0x00000	
Xtensa CPU		Source CAR	0x00900	
		Source Clock Meters	0x00A00	
		SCDC	0x01800	
	DP-TX	DPTX-PHY	0x02000	16x4B
		DPTX-HPD	0x02100	16x4B
		DPTX-FRMR	0x02200	16x4B
		DPTX-STREAM	0x02200+41*N	16x4B
		DPTX-GLBL	0x02300	16x4B
		DPTX-AUX	0x02800	16x4B
	CEC	CEC	0x03800	
	AFE	AFE	0x04800	
	CRYPTO	HDCP Crypto	0x05800	
	CIPHER	HDCP CIPHER	0x60000	

Fig. 8-10 DPTX APB slave port memory map

8.6.5 Boot Sequence

After Reset the Xtensa processor is disabled. The full controller address space is accessible for the external host as well as the I-MEM and D-MEM .
External host processor should load the FW into the I-MEM and D-MEM and then enable the Xtensa processor.
The FW is composed from two files – imem.hex and dmem.hex.
The imem.hex contains the instruction memory and the dmem.hex contains the variables initialization.
In order to load the I-MEM and the D-MEM the host processor should assign the APB bus to directly access the memories by writing the value of 0x07 to the APB_CTRL register.
Afterwards, write to memories is enabled and the I-MEM address is mapped to 0x80000, the D-MEM address is 0x40000. After loading the memories, the host should select the Xtensa processor to be the master of the I-MEM, D-MEM memories (by writing the value of 0x00 to the APB_CTRL register) and enable the Xtensa processor. After completing the boot sequence, user can read the following registers to verify the FW has been loaded as expected:

Register 6 (h6) – KEEP_ALIVE – When the FW is running, this register will be changed

on every kernel loop (<2ms), host should read it twice to see if the CPU is running.

Register 7 (h7) – VER_L and Register 8 (h8) – VER_H – These two registers represent the firmware version, automatically from our SVN server. On any release supplied by us there will be a unique number.

8.6.6 HDCP (Embedded HDCP Crypto)

In this mode the HDCP functionality is fully supported by the controller. where the AKE phase (and the corresponding cryptographic operations) are handled by the FW .following the AKE phase, the FW initialize the stream cipher with the session key.

The external host communicate with the controller for configuring the capabilities, loading the HDCP keys (or certificate) and monitoring authentication status. The SAPB is used to carry secured commands over mailbox (commands which carry secret information or need to be protected from tampering).

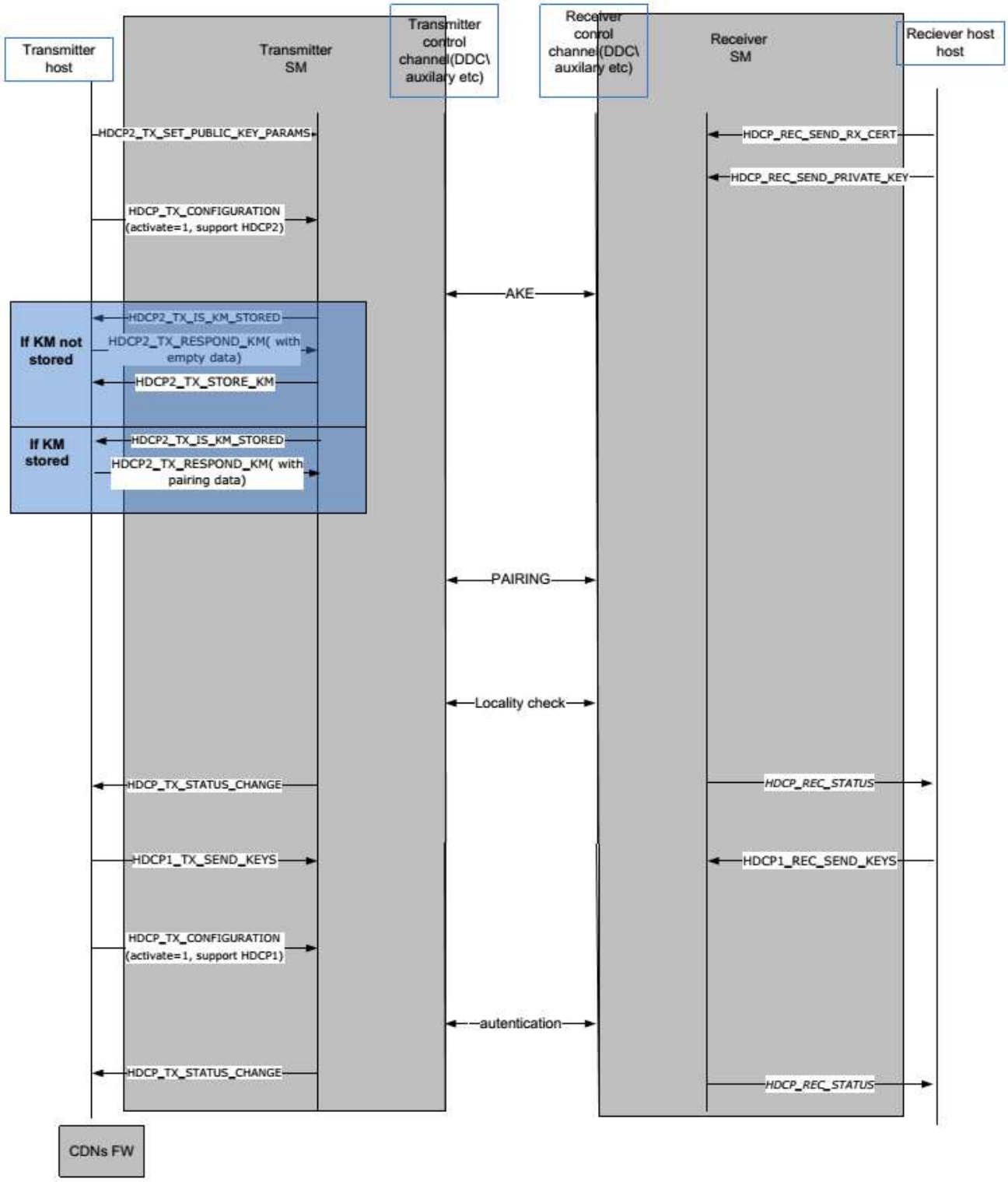


Fig. 8-11 Operation sequence HDCP2.2

8.6.7 Info-Frame Handling

Info frames are directly accessed from the host processor. The controller does not handle the info-frames, which should be managed by the external host using API's. For this purpose the host should use PKT-MEM register bank for directly writing or reading the info-frames.

8.6.8 Protocol over Auxiliary

The firmware provides an interface for the AUX and I2C-over-AUX data transactions. The external host may use it for direct DPCD (including the HDCP address range) access.

8.6.9 I2S (Audio) Control

Audio Interface I2S and SPDIF configurations are directly accessed from the host processor. The controller does not handle AIF, which should be managed by the external host using API's. For this purpose the host should use AIF register bank for directly writing or reading.

8.6.10 CSC (Color Space Conversion) Control

CSC Interface configurations are directly accessed from the host processor. The controller does not handle CSC, which should be managed by the external host using API's. For this purpose the host should use CSC register bank for directly writing or reading.

8.6.11 Mail-Box Channel

After boot, entire communication between the processor and the host is conducted through the mail-box.
There are two mail boxes (RX and TX), for communication between host and the controller, with each mail box being independent and working in parallel. The communication is used to set the configuration, and status updates.
The mailbox is implemented by a HW FIFO managed by the embedded FW, where the FIFO depth is 8 words.
In the case of register mailbox_full when the host wants to write data to processor, it can do so while the mailbox_full bit is 0. When mailbox_empty is 1, there are waiting data to read (at least 1).
Following Table shows the mailbox message data structure. All of the commands sent and receive in the following order: less significant byte first in little endian convention.

Table 8-2 Mailbox Message Data Structure

Name	Number of Bytes	Description
Opcode	1	Command OpCode
Module-id	1	Module type code (Must be DPTX 0x01 or HDCP 0x07)
size	2	Size of the message (not including header), max of 1019
message	0-1019	The message to transfer

DP TX commands (From host cpu to DPTX)

Command 0x00, DPTX_SET_POWER_MNG – set power mode for sink

Byte 0
Power mode: 0x00 normal operation 0x01 Power down 0x02 Power down, active AUX

Command 0x01, DPTX_SET_HOST_CAPABILITIES – set host capabilities for training

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Max link rate	Lanes count	Max voltage swing	Max pre emphasis	Test patterns supported	Reserved	Reserved	Reserved

Command 0x02, DPTX_GET_ EDID – no extra parameters needed

Command 0x03, DPTX_Read_DPCD - read DPCD from from Sink

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
Number of bytes to read (MSB)	Number of bytes to read (LSB)	Address (MSB)	Address	Address (LSB)

Command 0x04, DPTX_WRITE_DPCD – write DPCD registers on sink
Sending this command will result in writing directly to the DPCD bank in the Sink device

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Bytes 5-1019
Number of bytes to write (MSB)	Number of bytes to write (LSB)	Address (MSB)	Address	Address (LSB)	Bytes to write

Command 0x05, DPTX_ENABLE_EVENT enables or disables messages types, 1 for enable, 0 for disable

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
Bit 0 -HPD Bit1 – training	Reserved	Reserved	Reserved	Reserved

Command 0x06, DPTX_WRITE_REGISTER

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5
Bank id(see bank id table)	Register address	Msb data	data	data	Lsb data

Command 0x07, DPTX_READ_REGISTER

Byte 0	Byte 1
Bank id(see bank id table)	Register address

Command 0x08, DPTX_WRITE_FIELD – write field (start bit and number of bits)

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Bank id(see bank id table)	Register address	Start bit (include)	Number of bits	Msb data	data	data	Lsb data

Bank id table

Bank name	Bank id
DPTX_STREAM	3
Reserved	
Reserved	

Command 0x09, DPTX_CONTROL

Byte 0
Set working mode: 0 – not active 1 – run (if already run, nothing will happen) 2 – restart (if already run, will restart the link

DP TX commands (From DPTX to host cpu)
Command 0x02, DPTX_EDID_RESP - response

Byte 0	Byte 1	Byte 2 - 129
EDID length(up to 128) (MSB)	EDID block (LSB)	EDID

Command 0x03, DPTX_DPCD_READ_RESP – response

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5 – (5+N-1)
Number of bytes (N)(MSB)	Number of bytes (N)(LSB)	Address (MSB)	Address	Address (LSB)	Values

Command 0x04, DPTX_DPCD_WRITE_RESP– response

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
Number of written bytes (MSB)	Number of written bytes (LSB)	Address (MSB)	Address	Address (LSB)

Command 0x05, DPTX_EVENT (see section Message types and codes)

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
Event id (see list of events)	Code/ Value	Reserved	Reserved	Reserved

The following events are supported

Event ID	Codes/Values
0 HPD events	0 HPD changed to high 1 HPD changed to low 2 HPD pulse
1 Training	0 Training started 1 Training complete 2 Training failed (clock recovery) 3 Training failed (channel equalization)

Command 0x07, DPTX_READ_REGISTER_RESP

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5
Bank id(see bank id table)	Register address	Msb data	data	data	Lsb data

Special Debug command to check CPU and mailbox interface are working:
Command 0xFD, DPTX_CHECK_MAIL_BOX

Byte 0	Byte 1	Byte 2
AA	BB	CC

HDCP Transmitter Device Commands (From host cpu to DPTX)

Command 0, HDCP_TX_CONFIGURATION

HDCP_TX_CONFIGURATION– use this command to set HDCP transmitter type and wake it up (or stop it)	Bit 1 – 0 - 0 – support only HDCP 2.2 1 – support only HDCP 1.4 2 – support both HDCP - It will always try the first the 2.2 and if the receiver doesn't support 2.2, will go to the the 1.4
	Bit 2 –to activate set to 1, to stop set to 0
	Bit 3 – Content Stream type in case receiver is repeater: 0 - Type 0 Content Stream. May be transmitted by The HDCP Repeater to all HDCP Devices. 1 - Type 1 Content Stream. Must not be transmitted by the HDCP Repeater to HDCP 1.x-compliant Devices and HDCP 2.0-compliant Repeaters

Command 1, HDCP2_TX_SET_PUBLIC_KEY_PARAMS

HDCP2_TX_SET_PUBLIC_KEY_PARAMS use it to set public key for the HDCP2.x transmitter (HDCP2.x)	Modulus n – 384 bytes	E – 3 bytes

Command 2, HDCP2_TX_SET_DEBUG_RANDOM_NUMBERS

HDCP2_TX_SET_DEBUG_RANDOM_NUMBERS– use this command to enforce the random parameters (for debug only!), instead of the random data generated by the embedded RNG. Use this command after HDCP_TX_SET_PUBLIC_KEY_PARAMS command. Relevant to (HDCP2.x)	KM 16 bytes	RN 8 bytes	KS 16 bytes	RIV 8 bytes	RTX 8 bytes

Command 3, HDCP2_TX_RESPOND_KM

HDCP2_TX_RESPOND_KM If km is stored, return all parameters, else there is no extra data (HDCP2.x)	Receiver ID (5 bytes)	m (16 bytes)	Km (16 bytes)	Ekh (Km) (16 bytes)

Command 4, HDCP1_TX_SEND_KEYS

HDCP1_TX_SEND_KEYS Set HDCP1 keys (HDCP1.x)	transmitter ID (5 bytes)	ksv (280 bytes)

Command 5, HDCP1_TX_SEND_RANDOM_AN

HDCP1_TX_SEND_RANDOM_AN Set HDCP1 a random number, use for debug only! (HDCP1.x)	An (8 bytes)

Command 10, HDCP_TX_RESPOND_RECEIVER_ID_VALID

HDCP_TX_RESPOND_RECEIVER_ID_VALID respond to command HDCP_TX_IS_RECEIVER_ID_VALID – if all receivers are not in revocation list return 1, if one of the receivers in the revocation list, return 0	1 All receivers are not in revocation list 0 at least one of the receivers is not valid (1 byte)

HDCP Transmitter Device Commands (From DPTX to host cpu)

Command 6, HDCP_TX_STATUS_CHANGE

HDCP_TX_STATUS_CHANGE Will be called in port status change	Status for the port: (bytes 1-0) Bit 0 – AUTHENTICATED (1 – link is authenticated) Bit 1 – receiver is REPEATER (1 for repeater, 0 not) Bit 3-2 – rx type - 1 for HDCP1, 2 for HDCP2 Bit 4 – 1 for AuthStreamId success, 0 if not Bit 8-5 - last error, see the error code table Bit 9 – work with ENABLE_1.1_FEATURES
	Byte 2 (for hdmi 1.4) bcaps
	Byte 4-3 (for hdmi 1.4) bstatus (3 msb, 4 lsb)
Error ID	Error description
0x0	No specific
0x1	HPD is down
0x2	SRM failure
0x3	signature verification error
0x4	h tag != h
0x5	V tag diff v
0x6	locality check
0x7	DDC error
0x8	REAUTH_REQ
0x9	topology error MAX_CASCADE_EXCEEDED or MAX_DEVS_EXCEEDED or CurSeqNumV != seq_num_V)
0xa	Verify receiver id list failed
0xb	HDCP_RSVD1 was not 0,0,0
0xc	HDMI capability or HDMI mode (bcaps and bstatus are available) -> restart autentication
0xd	RI result was different than expected
0xe	watchDog expired
0xf	REAPEATER INTEGRITY failed

Command 7, HDCP2_TX_IS_KM_STORED

HDCP2_TX_IS_KM_STORED controller check if KM is stored by host(HDCP2.x)	Receiver ID (5 bytes)

Command 8, HDCP2_TX_STORE_KM

HDCP2_TX_STORE_KM controller ask host to store KM, host may store it on non-volatile memory for faster authentication (HDCP2.x)	Receiver ID (5 bytes)	m (16 bytes)	Km(16 bytes)	Ekh(Km) (16 bytes)

Command 9, HDCP_TX_IS_RECEIVER_ID_VALID

HDCP_TX_IS_RECEIVER_ID_VALID controller ask host to check the receivers revocation list	Number of receivers (1 in regular case, more can be in repeater) (1 byte)	Receiver ID (5 bytes * Number of receivers)

HDCP Management Commands (From host cpu to DPTX)

Command 0, HDCP_GENERAL_2_SET_LC

HDCP_GENERAL_2_SET_LC - set the LC128	16 byte lc128

Command 1, HDCP_ GENERAL_SET_SEED

HDCP_SET_SEED – set random seed, Customer might use 3rd party TRNG for generating a true number seed number, it is expected that the seed number will meet high entropy level. if customer is not using this command, the embedded TRNG will generate the seed	32 bytes of seed

8.6.12 APIs

As part of the controller release, APIs written in c code will be supplied. User may use these APIs.
User need to supply functions for APB_WRITE and APB_READ.
Our API need to run on task in order to check the mailbox, when new msg arrived, we will call customer callback function for customer use.
For example, to read EDID, customer will use function to read EDID and will supply callback function, our APS will call the callback with EDID data when it be ready.
We will supply function that the customer need to run on task, and the callbacks will be called from this task (and function)
Api assumptions:

API functions are not thread-safe

Only one response can be expected at a time

If response opcode differs form expected opcode, callback receives CDN_BAD_OPCODE status

If no response is expected, but is received, it is ignored

If task is waiting for response it cannot process another request

Processing request/response by task and issuing request by api functions must be synchronized, therefore customer must provide void cdn_enter_critical(), void cdn_exit_critical(), and int cdn_try_enter_critical() (returning 1 if successfully enetered critical section). These can be noop if task does not run in parallel to api calls.

Chapter 9 MIPI DSI HOST Controller

9.1 Overview

The Display Serial Interface (DSI) is part of a group of communication protocols defined by the MIPI Alliance. The MIPI DSI HOST Controller is a digital core that implements all protocol functions defined in the MIPI DSI Specification. The MIPI DSI HOST Controller provides an interface between the system and the MIPI D-PHY, allowing the communication with a DSI-compliant display. The MIPI DSI HOST Controller supports one to four lanes for data transmission with MIPI D-PHY.

The MIPI DSI HOST Controller supports the following features:

- Compliant with MIPI Alliance standards
- Support the DPI interface color coding mappings into 24-bit Interface
  - 16 bits per pixel, configurations 1,2,and 3
  - 18 bits per pixel, configurations 1 and 2
  - 24 bits per pixel
- Programmable polarity of all DPI interface signals
- Extended resolutions beyond the DPI standard maximum resolution of 800x480 pixels:
  - Up to 2047 vertical active lines
  - Up to 63 vertical back porch lines
  - Up to 63 vertical front porch lines
  - Maximum resolution is limited by available DSI Physical link bandwidth which depends on the number of lanes and maximum speed per lane
- Interface with MIPI D-PHY following PHY Protocol Interface (PPI), as defined in MIPI Alliance Specification for D-PHY
- Up to four D-PHY Data Lanes
- Bidirectional communication and escape mode support through data lane 0
- Transmission of all generic commands
- ECC and Checksum capabilities
- End of Transmission Packet(EOTp)
- Ultra Low-Power mode
- Fault recovery schemes

9.2 Block Diagram

The following diagram shows the MIPI DSI HOST Controller architecture.

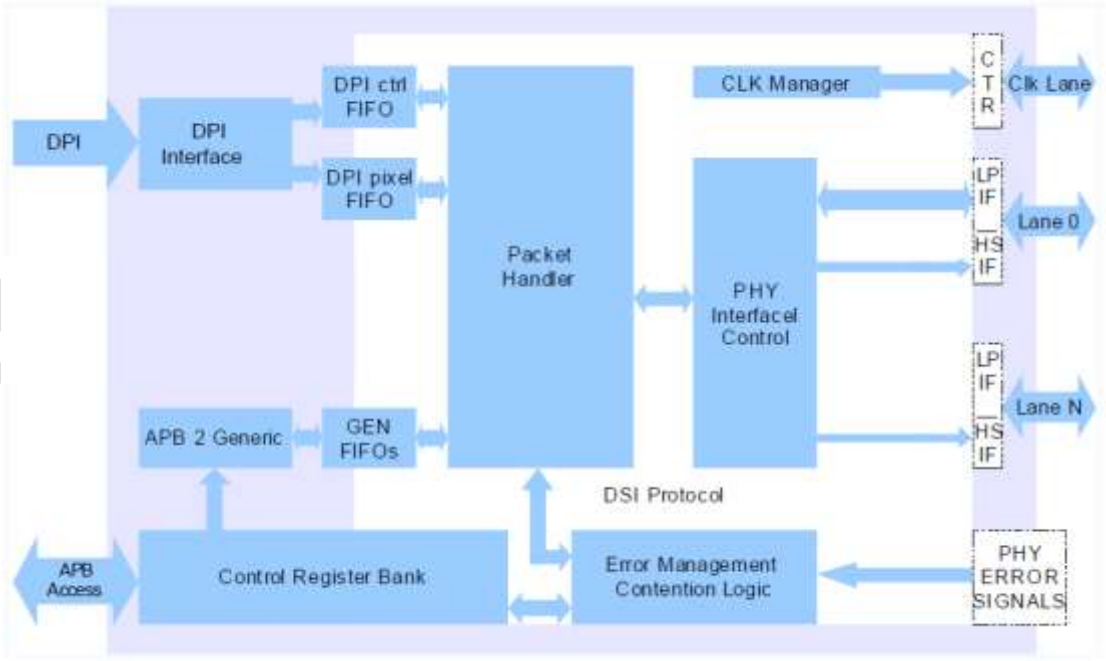


Fig. 9-1 MIPI DSI HOST Controller architecture

The DPI interface captures the data and control signals and conveys them to a FIFO for video

control signals and another one for pixel data. This data is then used to build Video packets, hen in Video mode.
The Register Bank is accessible through a standard AMBA-APB slave interface, providing access to the MIPI DSI HOST Controller registers for configuration and control. There is also a fully programmable interrupt generator to inform the system about certain events.
The PHY Interface Control is responsible for managing the D-PHY PPI interface. It acknowledges the current operation and enables low-power transmission/reception or a high-speed transmission. It also performs data splitting between available D-PHY lanes for high-speed transmission.
The Packet Handler schedules the activities inside the link. It performs several functions based on the interfaces that are currently DPI and the video transmission mode that is used (burst mode or non-burst mode with sync pulse or sync events). It builds long or short packet generating correspondent ECC and CRC codes. This block also performs the following functions: Packet reception, Validation of packet header by checking the ECC, Header correction and notification for single-bit errors, Termination of reception, Multiple header error notification.
The APB-to-Generic block bridges the APB operations into FIFOs holding the Generic commands. The block interfaces with the following FIFOS: Command FIFO, Write payload FIFO, Read payload FIFO.
The Error Management notifies and monitors the error conditions on the DSI link. It controls the timers used to determine if a timeout condition occurred, performing an internal soft reset and triggering an interruption notification.

9.3 Function Description

9.3.1 DPI interface function

The DPI interface follows the MIPI DPI specification with pixel data bus width up to 24 bits. It is used to transmit the information in Video mode in which the transfers from the host processor to the peripheral take the form of a real-time pixel stream. This interface allows sending ShutDown (SD) and ColorMode (CM) commands, which are triggered directly by writing to the register of CFG_MISC_CON[2:1]. To transfer additional commands(for example, to initialize the display), use another interface such as APB Slave Generic Interface to complement the DPI interface.
The DPI interface captures the data and control signals and conveys them to the FIFO interfaces that transmit them to the DSI link. Two different streams of data are presented at the interface; video control signals and pixel data. Depending on the interface color coding, the pixel data is disposed differently throughout the dpipixdata bus. The following table shows the Interface pixel color coding.

Table 9-1 Color table

Signal Line	16-bit			18-bit		24-bit
	Config1	Config2	Config3	Config1	Config2	
dpipixdata23	Not used	Not used	Not used	Not used	Not used	R7
dpipixdata22	Not used	Not used	Not used	Not used	Not used	R6
dpipixdata21	Not used	Not used	R4	Not used	R5	R5
dpipixdata20	Not used	R4	R3	Not used	R4	R4
dpipixdata19	Not used	R3	R2	Not used	R3	R3
dpipixdata18	Not used	R2	R1	Not used	R2	R2
dpipixdata17	Not used	R1	R0	R5	R1	R1
dpipixdata16	Not used	R0	Not used	R4	R0	R0
dpipixdata15	R4	Not used	Not used	R3	Not used	G7
dpipixdata14	R3	Not used	Not used	R2	Not used	G6
dpipixdata13	R2	G5	G5	R1	G5	G5
dpipixdata12	R1	G4	G4	R0	G4	G4
dpipixdata11	R0	G3	G3	G5	G3	G3
dpipixdata10	G5	G2	G2	G4	G2	G2
dpipixdata9	G4	G1	G1	G3	G1	G1
dpipixdata8	G3	G0	G0	G2	G0	G0
dpipixdata7	G2	Not used	Not used	G1	Not used	B7
dpipixdata6	G1	Not used	Not used	G0	Not used	B6
dpipixdata5	G0	Not used	B5	B5	B5	B5
dpipixdata4	B4	B4	B4	B4	B4	B4
dpipixdata3	B3	B3	B3	B3	B3	B3
dpipixdata2	B2	B2	B2	B2	B2	B2
dpipixdata1	B1	B1	B1	B1	B1	B1
dpipixdata0	B0	B0	Not used	B0	B0	B0

The DPI interface can be configured to increase flexibility and promote correct usage of this interface for several systems. These configuration options are as follows:Polarity control: All the control signals are programmable to change the polarity depending on system requirements.

After the MIPI DSI HOST Controller reset, DPI waits for the first VSYNC active transition to start signal sampling, including pixel data, and preventing image transmission in the middle of a frame.

If interface pixel color coding is 18 bits and the 18-bit loosely packed stream is disabled, the number of lines programmed in the pixels per lines configuration is a multiple of four. This means that in this mode, the two LSBs in the configuration are always inferred as zero. The specification states that in this mode, the pixel line size should be a multiple of four.

9.3.2 APB Slave Generic Interface

The APB Slave interface allows the transmission of generic information in Command mode, and follows the proprietary register interface. Commands sent through this interface are not constrained to comply with the DCS specification, and can include generic commands described in the DSI specification as manufacturer-specific.

The MIPI DSI HOST Controller supports the transmission or write and read command mode packets as described in the DSI specification. These packets are built using the APB register access. The GEN_PLD_DATA register has two distinct functions based on the operation. Writing to this register sends the data as payload when sending a Command mode packet. Reading this register returns the payload of a read back operation. The GEN_HDR register contains the Command mode packet header type and header data. Writing to this register triggers the transmission of the packet implying that for a long Command mode packet, the packet's payload needs to be written in advance in the GEN_PLD_DATA register.

The valid packets available to be transmitted through the Generic interface are as follows:

- Generic Write Short Packet 0 Parameters

- Generic Write Short Packet 1 Parameters
- Generic Write Short Packet 2 Parameter
- Generic Write Short Packet 0 Parameter
- Generic Write Short Packet 1 Parameters
- Generic Write Short Packet 2 Parameter
- Maximum Read Packet Configuration
- Generic Long Write Packet
- DCS Write Short Packet 0 Parameter
- DCS Write Short Packet 1 Parameter
- DCS Write Short Packet 0 Parameter
- DCS Write Long Packet

A set of bits in the CMD_PKT_STATUS register report the status of the FIFOs associated with APB interface support.

Generic interface packets are always transported using one of the DSI transmission modes; Video mode or Command mode. If neither of these mode are selected, the packets are not transmitted through the link and the released FIFOs eventually get overflowed.

The transfer of packets through the APB bus is based on the following conditions:

The APB protocol defines that the write and read procedure takes two clock cycles each to be executed. This means that the maximum input data rate through the APB interfaces is always half the speed of the APB clock.

The data input bus has a maximum width of 32 bits. This allows for a relation to be defined between the input APB clock frequency and maximum bi rate achievable by the APB interface.

The DSI link bit rate when using solely APB is equal to (APB clock frequency) *16 Mbps.

The bandwidth is dependent on the APB clock frequency; the available bandwidth increases with the clock frequency.

To drive the APB interface to achieve high bandwidth Command mode traffic transported by the DSI link, the MIPI DSI HOST Controller should operate in the Command mode only and the APB interface should be the only data source that is currently in use. Thus, the APB interface has the entire bandwidth of the DSI link and does not share it with any another input interface source.

The memory write commands require maximum throughout from the APB interface, because they contain the most amount of data conveyed by the DSI link. While writing the packet information, first write the payload of a given packet into the payload FIFO using the GEN_PLD_DATA register. When the payload data is for the command parameters, place the first byte to be transmitted in the least sgnificant byte position of the APB data bus.

After writing the payload, write the packet header into the command FIFO. For more information and it should follow the pixel to byte conversion organization referred in the Annexure A of the DCS specification. The follow figures show how the pixel data should be orgavized in the APB data write bus. The memory write commands are conveyed in DCS long packets. DCS long packets are encapsulated in a DSI packet. The DSI included in the diagrams.In the follow figures, the Write Memory Command can be replaced by the DCS command Write Memory Start and Write Memory Continue.

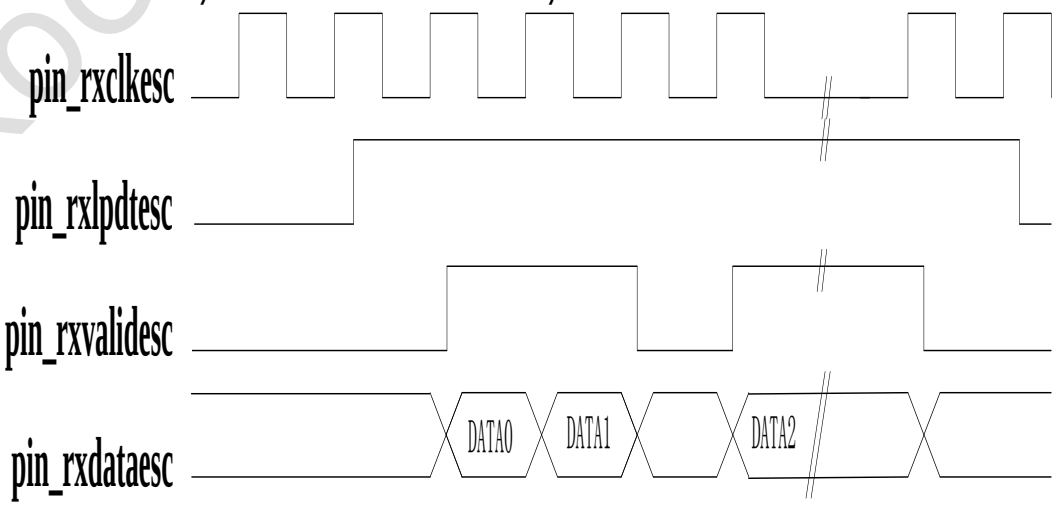


Fig. 9-2 24bpp APB Pixel to Byte Organization

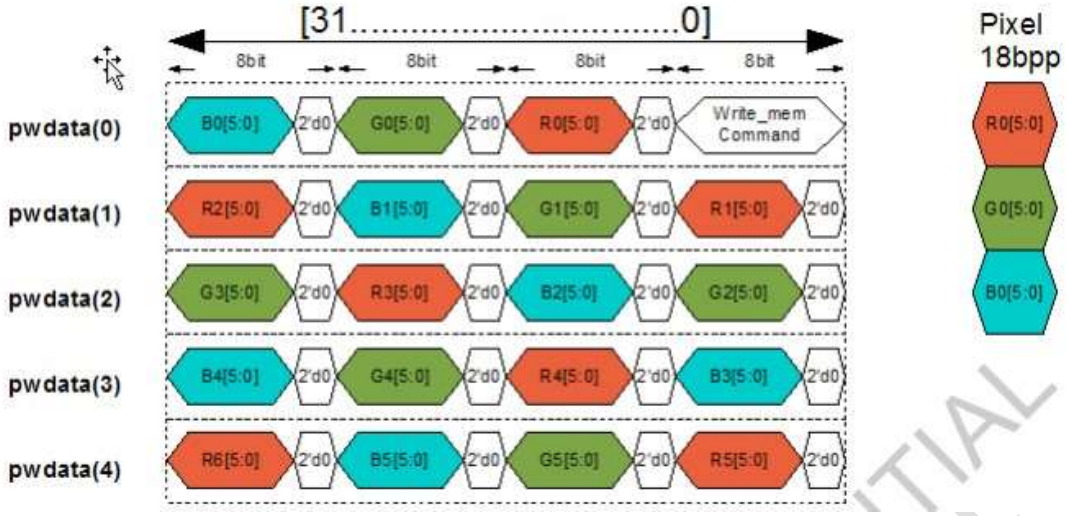


Fig. 9-3 18 bpp APB Pixel to Byte Organization

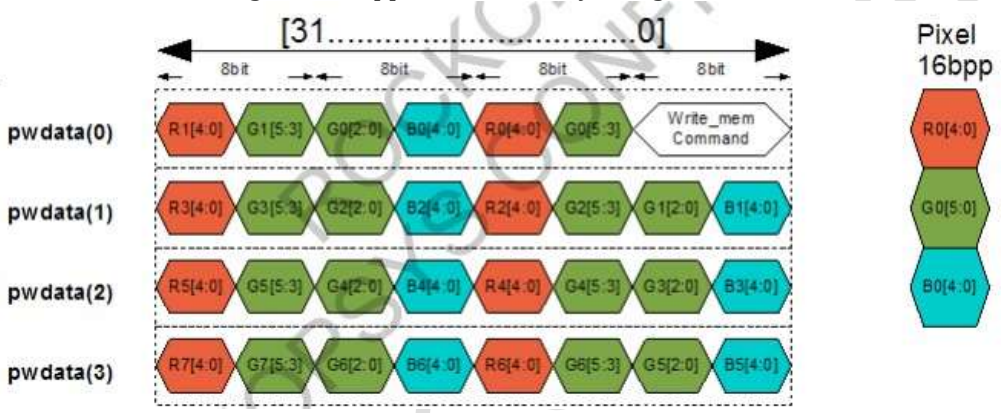


Fig. 9-4 16 bpp APB Pixel to Byte Organization

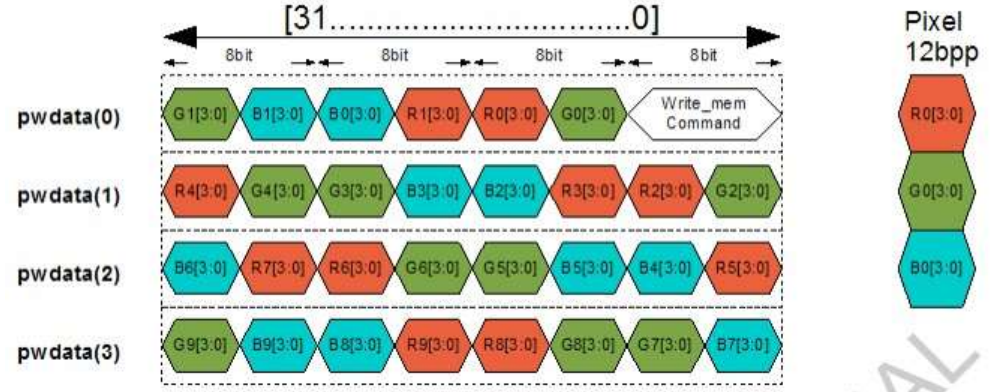


Fig. 9-5 12 bpp APB Pixel to Byte Organization

Fig. 9-6 8bpp APB Pixel to Byte Organization

9.3.3 Transmission of Commands in Video Mode

The MIPI DSI HOST Controller supports the transmission of commands, both in high-speed and low-power, while in Video mode. The DSI controller uses Blanking or Low-Power(BLLP) periods to transmit commands inserted through the APB Generic interface. Those periods correspond to the shaded areas of the following figure.

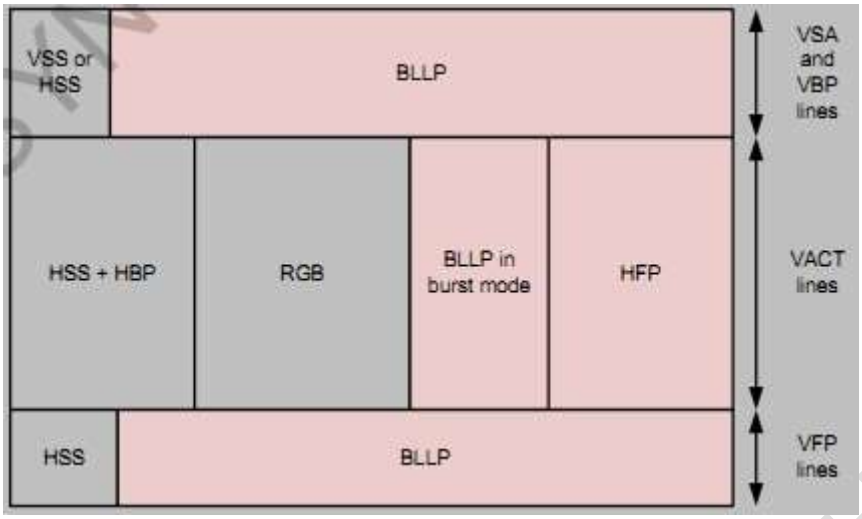


Fig. 9-7 Command Transmission Periods within the Image Area

Commands are transmitted in the blanking periods after the following packet/states:

- Bertical Sync Start (VSS) packets, if the Video Sync pulses are not enabled
- Horizontal Sync End (HSE) packets, in the VSA, VBP, and VFP regions
- Horizontal Sync Start (HSS) packets, if the Video Sync pulses are not enabled in the VSA, VBP, and VFP regions
- Horizontal Active (HACT) state

Only one command is transmitted per line, even in the case of the last line of a frame but one command is possible for each line.

The MIPI DSI HOST Controller avoids sending commands in the last line because it is possible that the last line is shorter than the other ones. For instance, the line time (tL) could be half a cycle longer than the tL on the DPI interface, that is, each line in the frame taking half a cycle from time for the last line. This results in the last line being (1/2 cycle) * (number of lines -1) shorter than tL.

The dpicolorm and dpishutdn input signals are also able to trigger the sending of command packets. The commands are DSI data types Color Mode On, Color Mode Off, Shut Down Peripheral, and Turn on Peripheral. These commands are not sent in the VACT region. If the lpcmden bit of the VID_MODE_CFG register is 1, these commands are sent in LP mode. In LP mode, the ouvact_lpcmd_time field of the LP_CMD_TIM register is used to determine if these commands can be transmitted. It is assumed that outvact_lpcmd_time is greater than or equal to 4 bytes (number of bytes in a short packet), because the DSI HOST does not transmit these commands on the last line.

If the frame_BTA_ack field is set in the VID_MODE_CFG register, a BTA is generated by DSI HOST after the last line of a frame. This may coincide with a write command or a read command. In either case, the edpihalt signal is held asserted until an acknowledge has been received (control of the DSI bus is returned to the host).

If the lpcmden bit of the VID_MODE_CFG register is set to 1, the commands are sent in low-power in Video mode. In this case, it is necessary to calculate the time available, in bytes, to transmit a command in LP mode for Horizontal Front Porch (HFP), Vertical Sync Active (VSA), Vertical Back Porch (VBP), and Vertical Front Porch(VFP) regions.

The outvact_lpcmd_time field of the LP_CMD_TIM register indicates the time available (in bytes) to transmit a command in LP mode, based on the escape clock, on a line during the VSA, VBP, and the VFP

Outvact_lpcmd_time=(tL-(Time to transmit HSS and HSE frames +tHSA+Time to enter and leave LP mode+Time to send the D-PHY LPDT command)) / escape clock period / 8 / 2

Where,

tL=Line time

tHSA=Time to send a short packet (for sync events) or time of the HAS pulse (for sync pulses)

In the above equation, division by eight is done to convert the time available to bytes and division by two is done because one bit is transmitted once in every two escape clock cycles. The outvact_lpcmd_time filed can be compared directly with the size of the command to be transmitted to determine if there is enough time to transmit the command. The maximum size

of a command that can be transmitted in LP mode is limited to 255 bytes by this field. This register must be programmed to a value greater than or equal to 4 bytes for the transmission of the DCTRL commands such as shutdown and colorm in LP mode.
Consider an example with 12.6 μs per line and assume an escape clock frequency of 15 MHz. In this case, 189 escape clock cycles are available to enter and exit LP mode and transmit command. The following are assumed:
Sync pulses are not being transmitted
Two lane byte clock ticks are required to transmit a short packet
phy_lp2hs_time=16
phy_lp2p_time=20
In this example, a 11-byte command can be transmitted as follows:
outvact_lpcmd_time=(12.6μs-(2*10 ns)-(16*10 ns)-(20*10 ns)-(8*66 ns)) / 66 ns / 8 / 2 = 11 bytes
The invact_lpcmd_time field of the LP_CMD_TIM register indicates the time available (in bytes) to transmite a command in LP mode (based on the escape clock) in the Vertical Active (VACT) region. This time is calculated as follows:
Invact_lpcmd_time=((tHFP-Time to enter and leave low-power mode + Blanking period before the HFP when in Burst mode- Time to send the D-PHY LPDT command) / escape clock period) / 8
Where,
tHFP=line time-tHSA-tHBP-tHACT
tHACT=vid_pkt_size*bits_per_pixel*lane_byte_clock_period / num_lanes
The invact_lpcmd_time field can be compared directly with the size of the command to be transmitted to determined if there is time to transmit the command.
Consider an example where the refresh rate is 60 Hz. The number of lines is 1320 (typical). The tL in this case is 12.6μs. With a lane byte clock of 100 MHz, 1260 clock ticks are availabel to transmit a single frame. If 800 ticks are used for pixel data then 460 ticks (4.6μs) are available for Horizontal Sync Start (HSS), HFP, and HBP. Assuming that 2.3μs is available for HFP and the escape clock is 15MHz, only 34 LP clock ticks are available to enter LP, transmit a command, and return from LP mode. Approximately 12 escape clock ticks are required to enter and leave LP mode. Therefore, only 1 byte could be transmitted in this period.
A short packet (for example, generic short write) requires a minimum of 4 bytes. Therefore, in this exampled, commands are not sent in the VACT region. If Burst mode is enabled, more time is available to transmit commands in the VACT region. The following are assumed:
The controller is not in Burst mode
phy_lp2hs_time=16
phy_lp2hs_time=16
In this examplem invact_lpcmd_time is calculated as follows:
Invact_lpcmd_time = (2.3μs –(16*10 ns)-(20*10 ns)-(8*66 ns)) /66 ns / 8 = 2 bytes
The outvact_lpcmd_time and invact_lpcmd_time fields allow a simple comparision to determine if a command can be transmitted in any of the BLLP periods.
Following figure illustrates the meaning of invact_lpcmd_time and outvact_lpcmd_time, matching them with the shaded areas and the VACT region.

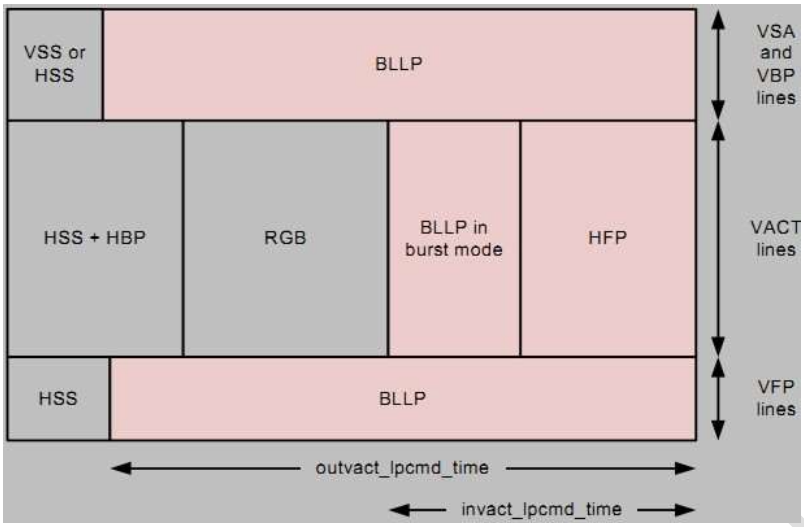


Fig. 9-8 Location in the Image Area

If the lpcmden bit of the VID_MODE_CFG register is 0, the commands are sent in high_speed in Video Mode. In this case, the DSI HOST automatically determines the area where each command can be sent and no programming or calculation is requied.

On read command Transmission, the max_rd_time field of the PHY_TMR_CFG register configures the maximum amount of time required to perform a read command in lane byte clock cycles.

The maximum time required to perform a read command in Lane byte clock cycles (max_rd_time) =Time to transmit the read command in LP mode + Time to enter and leave LP mode + Time to return the read data packet from the peripheral device.

The time to return the read data packet from the pripheral depends on the number of bytes read and the escape clock frequency of the peripheal; not the escape clock of the host. The max_rd_time field is used in both HS and LP mode to determine if there is time to complete a read command in a BLLP period.

In high-speed mode (lpcmden=0), max_rd_time is calculated as follows:

max_rd_time = phy_hs2lp_time + Time to return the read data packet from the peripheral device + phy_hs2hs_time

In low-power mode (lpcmden = 1), max_rd_time is calculated as follows:

max_rd_time = phy_hs2lp_time +LPDT command time + Read command time in LP mode + Time to return the data read from the peripheral device + phy_lp2hs_time

Where,

LPDT command time = (8*Host escape clock period) / Lane byte clock period

Read command time in LP mode = (32 * host escape clock period) / lane byte clock period

It is recommended to keep the maximum number of bytes read from the peripheral to a minimum to have sufficient time available to issue the read commands on a line. Ensure that max_rd_time* Lane byte clock period is less than outvact_lpcmd_time *8*Escape clock period of the host.

Otherwise, the read commands are serviced on the last line of a frame and the edpihalt signal may be asserted. If it is necessary to read a large number of parameters (＞16), increase the max_rd_time while the read command is being executed. When the read has completed, decrease the max_rd_time to a lower value.

9.3.4 Dual DSI Controllers system

There are 2 DSI Controllers. dsi0 is connected to dphy0. dsi1 is connected to dphy1. This is implemented by RTL design and cannot be changed by Software.

There are 2 VOPs, vop lit and vop big. Software can set the connection between VOP and SDI Controller.

GRF_SOC_CON20[0]:Set source of DSI0, 1:select VOPL; 0:select VOPB

GRF_SOC_CON20[4]:Set source of DSI1, 1:select VOPL; 0:select VOPB

9.4 Register Description

9.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

9.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
MIPI_DSI_HOST_VERSION	0x0000	W	0x3133302a	VERSION
MIPI_DSI_HOST_PWR_UP	0x0004	W	0x00000000	PWR_UP
MIPI_DSI_HOST_CLKMGR_CFG	0x0008	W	0x00000000	Internal Clock Dividers Configuration Register
MIPI_DSI_HOST_DPI_VCID	0x000c	W	0x00000000	DPI Virtual Channel ID Register
MIPI_DSI_HOST_DPI_COLOR_CODING	0x0010	W	0x00000000	DPI Color Coding Register
MIPI_DSI_HOST_DPI_CFG_POL	0x0014	W	0x00000000	DPI Polarity Configuration Register
MIPI_DSI_HOST_DPI_LP_CMD_TIM	0x0018	W	0x00000000	Low-Power Command Timing Configuration Register
MIPI_DSI_HOST_PCKHDL_CFG	0x002c	W	0x00000000	Packet Handler Configuration Register
MIPI_DSI_HOST_GEN_VCID	0x0030	W	0x00000000	Generic Interface Virtual Channel Id Register
MIPI_DSI_HOST_MODE_CFG	0x0034	W	0x00000001	Register0000 Abstract
MIPI_DSI_HOST_VID_MODE_CFG	0x0038	W	0x00000000	Video Mode Configuration Register
MIPI_DSI_HOST_VID_PKT_SIZE	0x003c	W	0x00000000	Video Packet Size Register
MIPI_DSI_HOST_VID_NUM_CHUNKS	0x0040	W	0x00000000	Number Of Chunks Register
MIPI_DSI_HOST_VID_NULL_SIZE	0x0044	W	0x00000000	Null Packet Size Register
MIPI_DSI_HOST_VID_HSA_TIME	0x0048	W	0x00000000	Horizontal Sync Active Time Register
MIPI_DSI_HOST_VID_HBP_TIME	0x004c	W	0x00000000	Register0005 Abstract
MIPI_DSI_HOST_VID_HLINE_TIME	0x0050	W	0x00000000	Line Time Register
MIPI_DSI_HOST_VID_VSA_LINES	0x0054	W	0x00000000	VID_VSA_LINES
MIPI_DSI_HOST_VID_VBP_LINES	0x0058	W	0x00000000	Vertical Back Porch Period Register
MIPI_DSI_HOST_VID_VFP_LINES	0x005c	W	0x00000000	Vertical Front Porch Period Register
MIPI_DSI_HOST_VID_VACTIVE_LINES	0x0060	W	0x00000000	Vertical Resolution Register
MIPI_DSI_HOST_EDPI_CMD_SIZE	0x0064	W	0x00000000	eDPI Packet Size Register
MIPI_DSI_HOST_CMD_MODE_CFG	0x0068	W	0x00000000	Command Mode Configuration Register
MIPI_DSI_HOST_GEN_HDR	0x006c	W	0x00000000	Generic Packet Header Configuration Register

Name	Offset	Size	Reset Value	Description
MIPI_DSI_HOST_GEN_PLD_DATA	0x0070	W	0x00000000	Generic Payload Data In And Out Register
MIPI_DSI_HOST_CMD_PKT_STATUS	0x0074	W	0x00000000	Command Packet Status Register
MIPI_DSI_HOST_TO_CNT_CFG	0x0078	W	0x00000000	Timeout Timers Configuration Register
MIPI_DSI_HOST_HS_RD_TO_CNT	0x007c	W	0x00000000	Peripheral Response Timeout Definition after Hi
MIPI_DSI_HOST_LP_RD_TO_CNT	0x0080	W	0x00000000	Peripheral Response Timeout Definition after Lo
MIPI_DSI_HOST_HS_WR_TO_CNT	0x0084	W	0x00000000	Peripheral Response Timeout Definition after Hi
MIPI_DSI_HOST_LP_WR_TO_CNT	0x0088	W	0x00000000	Peripheral Response Timeout Definition after Lo
MIPI_DSI_HOST_BTA_TO_CNT	0x008c	W	0x00000000	Peripheral Response Timeout Definition after B
MIPI_DSI_HOST_LPCLK_CTRL	0x0094	W	0x00000000	Low-power in Clock Lane Register
MIPI_DSI_HOST_PHY_TMR_LPCLK_CFG	0x0098	W	0x00000000	D-PHY Timing Configuration for the Clock Lane
MIPI_DSI_HOST_PHY_TMR_CFG	0x009c	W	0x00000000	D-PHY Data Lanes Timing Configuration Registe
MIPI_DSI_HOST_PHY_RSTZ	0x00a0	W	0x00000000	D-PHY Reset Control Register
MIPI_DSI_HOST_PHY_IF_CFG	0x00a4	W	0x00000003	D-PHY Interface Configuration Register
MIPI_DSI_HOST_PHY_ULPS_CTRL	0x00a8	W	0x00000000	D-PHY Ultra Low-Power Control Register
MIPI_DSI_HOST_PHY_TX_TRIGGERS	0x00ac	W	0x00000000	D-PHY Transmit Triggers Register
MIPI_DSI_HOST_PHY_STATUS	0x00b0	W	0x00000000	Register0010 Abstract
MIPI_DSI_HOST_PHY_TST_CTRL0	0x00b4	W	0x00000000	D-PHY Test Interface Control 0 Register
MIPI_DSI_HOST_PHY_TST_CTRL1	0x00b8	W	0x00000000	D-PHY Test Interface Control 1 Register
MIPI_DSI_HOST_INT_ST0	0x00bc	W	0x00000000	Interrupt Status Register 0
MIPI_DSI_HOST_INT_ST1	0x00c0	W	0x00000000	Interrupt Status Register 1
MIPI_DSI_HOST_INT_MSK0	0x00c4	W	0x00000000	Masks the Interrupt Generation Triggered by the
MIPI_DSI_HOST_INT_MSK1	0x00c8	W	0x00000000	Masks the Interrupt Generation Triggered by the
MIPI_DSI_HOST_INT_FORCE0	0x00d8	W	0x00000000	Force Interrupt Configuration Register
MIPI_DSI_HOST_INT_FORCE1	0x00dc	W	0x00000000	Force Interrupt Configuration Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

9.4.3 Detail Register Description

MIPI_DSI_HOST_VERSION

Address: Operational Base + offset (0x0000)

VERSION

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x3133302a	VERSION VERSION VERSION

MIPI_DSI_HOST_PWR_UP
Address: Operational Base + offset (0x0004)
PWR_UP

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	shutdownz Field0000 Abstract This bit configures the core either to power up or to reset. shutdownz is the soft reset register. Its default value is 0. After the core configuration, to enable the DSI HOST, set this register to 1.

MIPI_DSI_HOST_CLKMGR_CFG
Address: Operational Base + offset (0x0008)
Internal Clock Dividers Configuration Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:8	RW	0x00	to_clk_division to_clk_division This field indicates the division factor for the Time Out clock used as the timing unit in the configuration of HS to LP and LP to HS transition error.
7:0	RW	0x00	tx_esc_clk_division tx_esc_clk_division This field indicates the division factor for the TX Escape clock source (lanebyteclk). The values 0 and 1 stop the TX_ESC clock generation.

MIPI_DSI_HOST_DPI_VCID
Address: Operational Base + offset (0x000c)
DPI Virtual Channel ID Register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1:0	RW	0x0	dpi_vcid dpi_vcid This field configures the DPI virtual channel id that is indexed to the Video mode packets.

MIPI_DSI_HOST_DPI_COLOR_CODING
Address: Operational Base + offset (0x0010)
DPI Color Coding Register

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved

8	RW	0x0	loosely18_en Field0001 Abstract When set to 1, this bit activates loosely packed variant to 18-bit configurations.
7:4	RO	0x0	reserved
3:0	RW	0x0	dpi_color_coding dpi_color_coding This field configures the DPI color coding as follows: ■0000: 16-bit configuration 1 ■0001: 16-bit configuration 2 ■0010: 16-bit configuration 3 ■0011: 18-bit configuration 1 ■0100: 18-bit configuration 2 ■0101: 24-bit ■0110: 20-bit YCbCr 4:2:2 loosely packed ■0111: 24-bit YCbCr 4:2:2 ■1000: 16-bit YCbCr 4:2:2 ■1001: 30-bit ■1010: 36-bit ■1011-1111: 12-bit YCbCr 4:2:0

MIPI_DSI_HOST_DPI_CFG_POL

Address: Operational Base + offset (0x0014)

DPI Polarity Configuration Register

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x0	colorm_active_low Field0001 Abstract When set to 1, this bit configures the color mode pin (dpicolorm) as active low.
3	RW	0x0	shutd_active_low Field0001 Abstract When set to 1, this bit configures the shutdown pin (dpishutdn) as active low.
2	RW	0x0	hsync_active_low Field0001 Abstract When set to 1, this bit configures the horizontal synchronism pin (dpihsync) as active low.
1	RW	0x0	vsync_active_low Field0001 Abstract When set to 1, this bit configures the vertical synchronism pin (dpivsync) as active low.
0	RW	0x0	dataen_active_low Field0000 Abstract When set to 1, this bit configures the data enable pin (dpidataen) as active low.

MIPI_DSI_HOST_DPI_LP_CMD_TIM

Address: Operational Base + offset (0x0018)

Low-Power Command Timing Configuration Register

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved

23:16	RW	0x00	outvact_lpcmd_time outvact_lpcmd_time This field is used for the transmission of commands in low-power mode. It defines the size, in bytes, of the largest packet that can fit in a line during the VSA, VBP, and VFP regions.
15:8	RO	0x0	reserved
7:0	RW	0x00	invact_lpcmd_time invact_lpcmd_time This field is used for the transmission of commands in low-power mode. It defines the size, in bytes, of the largest packet that can fit in a line during the VACT region.

MIPI_DSI_HOST_PCKHDL_CFG

Address: Operational Base + offset (0x002c)

Packet Handler Configuration Register

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x0	crc_rx_en crc_rx_en When set to 1, this bit enables the CRC reception and error reporting
3	RW	0x0	ecc_rx_en ecc_rx_en When set to 1, this bit enables the ECC reception, error correction, and reporting.
2	RW	0x0	bta_en Field0000 Abstract When set to 1, this bit enables the Bus Turn-Around (BTA) request.
1	RW	0x0	eotp_rx_en eotp_rx_en When set to 1, this bit enables the EoTp reception.
0	RW	0x0	eotp_tx_en eotp_tx_en When set to 1, this bit enables the EoTp transmission. (When transfer video to UNIPRO, this bit must be set to 0).

MIPI_DSI_HOST_GEN_VCID

Address: Operational Base + offset (0x0030)

Generic Interface Virtual Channel Id Register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1:0	RW	0x0	gen_vcid_rx gen_vcid_rx This field indicates the Generic interface read-back virtual channel identification.

MIPI_DSI_HOST_MODE_CFG

Address: Operational Base + offset (0x0034)

Register0000 Abstract

Bit	Attr	Reset Value	Description

31:1	RO	0x0	reserved
0	RW	0x1	cmd_video_mode Field0000 Abstract This bit configures the operation mode: ■0: Video mode ■1: Command mode

MIPI_DSI_HOST_VID_MODE_CFG

Address: Operational Base + offset (0x0038)

Video Mode Configuration Register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	vpg_orientation vpg_orientation This field indicates the color bar orientation as follows: 0: Vertical mode 1: Horizontal mode
23:21	RO	0x0	reserved
20	RW	0x0	vpg_mode vpg_mode This field is to select the pattern: 0: Color bar (horizontal or vertical) 1: BER pattern (vertical only)
19:17	RO	0x0	reserved
16	RW	0x0	vpg_en vpg_en When set to 1, this bit enables the video mode pattern generator.
15	RW	0x0	lp_cmd_en lp_cmd_en When set to 1, this bit enables the command transmission only in lowpower mode.
14	RW	0x0	frame_bta_ack_en frame_bta_ack_en When set to 1, this bit enables the request for an acknowledge response at the end of a frame.
13	RW	0x0	lp_hfp_en lp_hfp_en When set to 1, this bit enables the return to low-power inside the Horizontal Front Porch (HFP) period when timing allows.
12	RW	0x0	lp_hbp_en lp_hbp_en When set to 1, this bit enables the return to low-power inside the Horizontal Back Porch (HBP) period when timing allows.
11	RW	0x0	lp_vact_en lp_vact_en When set to 1, this bit enables the return to low-power inside the Vertical Active (VACT) period when timing allows.
10	RW	0x0	lp_vfp_en lp_vfp_en When set to 1, this bit enables the return to low-power inside the Vertical Front Porch (VFP) period when timing allows.

Bit	Attr	Reset Value	Description
9	RW	0x0	lp_vbp_en lp_vbp_en When set to 1, this bit enables the return to low-power inside the Vertical Back Porch (VBP) period when timing allows.
8	RW	0x0	lp_vsa_en lp_vsa_en When set to 1, this bit enables the return to low-power inside the Vertical Sync Time (VSA) period when timing allows.
7:1	RO	0x0	reserved
0	RW	0x0	vid_mode_type vid_mode_type This field indicates the video mode transmission type as follows: ■00: Non-burst with sync pulses ■01: Non-burst with sync events ■10 and 11: Burst mode

MIPI_DSI_HOST_VID_PKT_SIZE
Address: Operational Base + offset (0x003c)
Video Packet Size Register

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:0	RW	0x0000	vid_pkt_size vid_pkt_size This field configures the number of pixels in a single video packet. For 18-bit not loosely packed data types, this number must be a multiple of 4. For YCbCr data types, it must be a multiple of 2, as described in the DSI specification.

MIPI_DSI_HOST_VID_NUM_CHUNKS
Address: Operational Base + offset (0x0040)
Number Of Chunks Register

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	vid_num_chunks vid_num_chunks This register configures the number of chunks to be transmitted during a Line period (a chunk consists of a video packet and a null packet). If set to 0 or 1, the video line is transmitted in a single packet. If set to 1, the packet is part of a chunk, so a null packet follows it if vid_null_size > 0. Otherwise, multiple chunks are used to transmit each video line.

MIPI_DSI_HOST_VID_NULL_SIZE
Address: Operational Base + offset (0x0044)
Null Packet Size Register

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	vid_null_size vid_null_size This register configures the number of bytes inside a null packet. Setting it to 0 disables the null packets.

MIPI_DSI_HOST_VID_HSA_TIME
Address: Operational Base + offset (0x0048)
Horizontal Sync Active Time Register

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	vid_hsa_time vid_hsa_time This field configures the Horizontal Synchronism Active period in lane byte clock cycles.

MIPI_DSI_HOST_VID_HBP_TIME
Address: Operational Base + offset (0x004c)
Register0005 Abstract

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	vid_hbp_time vid_hbp_time This field configures the Horizontal Back Porch period in lane byte clock cycles.

MIPI_DSI_HOST_VID_HLINE_TIME
Address: Operational Base + offset (0x0050)
Line Time Register

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14:0	RW	0x0000	vid_hline_time vid_hline_time This field configures the size of the total line time (HSA+HBP+HACT+HFP) counted in lane byte clock cycles.

MIPI_DSI_HOST_VID_VSA_LINES
Address: Operational Base + offset (0x0054)
VID_VSA_LINES

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x000	vsa_lines Field0000 Abstract This field configures the Vertical Synchronism Active period measured in number of horizontal lines.

MIPI_DSI_HOST_VID_VBP_LINES
Address: Operational Base + offset (0x0058)
Vertical Back Porch Period Register

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x000	vbp_lines vbp_lines This field configures the Vertical Back Porch period measured in number of horizontal lines.

MIPI_DSI_HOST_VID_VFP_LINES
Address: Operational Base + offset (0x005c)
Vertical Front Porch Period Register

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x000	vfp_lines vfp_lines This field configures the Vertical Front Porch period measured in number of horizontal lines.

MIPI_DSI_HOST_VID_VACTIVE_LINES
Address: Operational Base + offset (0x0060)
Vertical Resolution Register

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:0	RW	0x0000	v_active_lines v_active_lines This field configures the Vertical Active period measured in number of horizontal lines.

MIPI_DSI_HOST_EDPI_CMD_SIZE
Address: Operational Base + offset (0x0064)
eDPI Packet Size Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	edpi_allowed_cmd_size edpi_allowed_cmd_size This field configures the maximum allowed size for an eDPI write memory command, measured in pixels. Automatic partitioning of data obtained from eDPI is permanently enabled.

MIPI_DSI_HOST_CMD_MODE_CFG
Address: Operational Base + offset (0x0068)
Command Mode Configuration Register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	max_rd_pkt_size max_rd_pkt_size This bit configures the maximum read packet size command transmission type: ■0: High-speed ■1: Low-power
23:20	RO	0x0	reserved

Bit	Attr	Reset Value	Description
19	RW	0x0	dcs_lw_tx dcs_lw_tx This bit configures the DCS long write packet command transmission type: ■0: High-speed ■1: Low-power
18	RW	0x0	dcs_sr_0p_tx dcs_sr_0p_tx This bit configures the DCS short read packet with zero parameter command transmission type: ■0: High-speed ■1: Low-power
17	RW	0x0	dcs_sw_1p_tx dcs_sw_1p_tx This bit configures the DCS short write packet with one parameter command transmission type: ■0: High-speed ■1: Low-power
16	RW	0x0	dcs_sw_0p_tx dcs_sw_0p_tx This bit configures the DCS short write packet with zero parameter command transmission type: ■0: High-speed ■1: Low-power
15	RO	0x0	reserved
14	RW	0x0	gen_lw_tx gen_lw_tx This bit configures the Generic long write packet command transmission type: ■0: High-speed ■1: Low-power
13	RW	0x0	gen_sr_2p_tx gen_sr_2p_tx This bit configures the Generic short read packet with two parameters command transmission type: ■0: High-speed ■1: Low-power
12	RW	0x0	gen_sr_1p_tx gen_sr_1p_tx This bit configures the Generic short read packet with one parameter command transmission type: ■0: High-speed ■1: Low-power
11	RW	0x0	gen_sr_0p_tx gen_sr_0p_tx This bit configures the Generic short read packet with zero parameter command transmission type: ■0: High-speed ■1: Low-power

Bit	Attr	Reset Value	Description
10	RW	0x0	gen_sw_2p_tx gen_sw_2p_tx This bit configures the Generic short write packet with two parameters command transmission type: ■0: High-speed ■1: Low-power
9	RW	0x0	gen_sw_1p_tx gen_sw_1p_tx This bit configures the Generic short write packet with one parameter command transmission type: ■0: High-speed ■1: Low-power
8	RW	0x0	gen_sw_0p_tx gen_sw_0p_tx This bit configures the Generic short write packet with zero parameter command transmission type: ■0: High-speed ■1: Low-power
7:2	RO	0x0	reserved
1	RW	0x0	ack_rqst_en ack_rqst_en When set to 1, this bit enables the acknowledge request after each packet transmission.
0	RW	0x0	tear_fx_en tear_fx_en When set to 1, this bit enables the tearing effect acknowledge request.

MIPI_DSI_HOST_GEN_HDR
Address: Operational Base + offset (0x006c)
Generic Packet Header Configuration Register

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	gen_wc_msbyte gen_wc_msbyte gen_wc_msbyte
15:8	RW	0x00	gen_wc_lsbyte gen_wc_lsbyte This field configures the least significant byte of the header packet's Word count for long packets or data 0 for short packets
7:6	RW	0x0	gen_vc gen_vc This field configures the virtual channel id of the header packet.
5:0	RW	0x00	gen_dt gen_dt This field configures the packet data type of the header packet.

MIPI_DSI_HOST_GEN_PLD_DATA
Address: Operational Base + offset (0x0070)
Generic Payload Data In And Out Register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	gen_pld_b4 gen_pld_b4 This field indicates byte 4 of the packet payload.
23:16	RW	0x00	gen_pld_b3 gen_pld_b3 This field indicates byte 3 of the packet payload.
15:8	RW	0x00	gen_pld_b2 gen_pld_b2 This field indicates byte 2 of the packet payload.
7:0	RW	0x00	gen_pld_b1 gen_pld_b1 This field indicates byte 1 of the packet payload.

MIPI_DSI_HOST_CMD_PKT_STATUS
Address: Operational Base + offset (0x0074)
Command Packet Status Register

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RO	0x0	gen_rd_cmd_busy gen_rd_cmd_busy This bit is set when a read command is issued and cleared when the entire response is stored in the FIFO.
5	RO	0x0	gen_pld_r_full gen_pld_r_full This bit indicates the full status of the generic read payload FIFO.
4	RO	0x0	gen_pld_r_empty gen_pld_r_empty This bit indicates the empty status of the generic read payload FIFO.
3	RO	0x0	gen_pld_w_full gen_pld_w_full This bit indicates the full status of the generic write payload FIFO.
2	RO	0x0	gen_pld_w_empty gen_pld_w_empty This bit indicates the empty status of the generic write payload FIFO.
1	RO	0x0	gen_cmd_full gen_cmd_full This bit indicates the full status of the generic command FIFO.
0	RO	0x0	gen_cmd_empty gen_cmd_empty This bit indicates the empty status of the generic command FIFO.

MIPI_DSI_HOST_TO_CNT_CFG
Address: Operational Base + offset (0x0078)
Timeout Timers Configuration Register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	hstx_to_cnt hstx_to_cnt This field configures the timeout counter that triggers a high-speed transmission timeout contention detection (measured in TO_CLK_DIVISION cycles). If using the non-burst mode and there is no sufficient time to switch from HS to LP and back in the period which is from one line data finishing to the next line sync start, the DSI link returns the LP state once per frame, then you should configure the TO_CLK_DIVISION and hstx_to_cnt to be in accordance with: hstx_to_cnt * lanebyteclkperiod * TO_CLK_DIVISION >= the time of one FRAME data transmission * (1 + 10%) In burst mode, RGB pixel packets are time-compressed, leaving more time during a scan line. Therefore, if in burst mode and there is sufficient time to switch from HS to LP and back in the period of time from one line data finishing to the next line sync start, the DSI link can return LP mode and back in this time interval to save power. For this, configure the TO_CLK_DIVISION and hstx_to_cnt to be in accordance with: hstx_to_cnt * lanebyteclkperiod * TO_CLK_DIVISION >= the time of one LINE data transmission * (1 + 10%)
15:0	RW	0x0000	lprx_to_cnt lprx_to_cnt This field configures the timeout counter that triggers a low-power reception timeout contention detection (measured in TO_CLK_DIVISION cycles).

MIPI_DSI_HOST_HS_RD_TO_CNT
Address: Operational Base + offset (0x007c)
Peripheral Response Timeout Definition after Hi

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	hs_rd_to_cnt hs_rd_to_cnt This field sets a period for which the DWC_mipi_dsi_host keeps the link still, after sending a high-speed read operation. This period is measured in cycles of lanebyteclk. The counting starts when the D-PHY enters the Stop state and causes no interrupts.

MIPI_DSI_HOST_LP_RD_TO_CNT
Address: Operational Base + offset (0x0080)
Peripheral Response Timeout Definition after Lo

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	lp_rd_to_cnt lp_rd_to_cnt This field sets a period for which the DSI HOST keeps the link still, after sending a low-power read operation. This period is measured in cycles of lanebyteclk. The counting starts when theD-PHY enters the Stop state and causes no interrupts.

MIPI_DSI_HOST_HS_WR_TO_CNT
Address: Operational Base + offset (0x0084)

Peripheral Response Timeout Definition after Hi

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	presp_to_mode presp_to_mode When set to 1, this bit ensures that the peripheral response timeout caused by hs_wr_to_cnt is used only once per eDPI frame, when both the following conditions are met: ■dpivsync_edpiwms has risen and fallen. ■Packets originated from eDPI have been transmitted and its FIFO is empty again. In this scenario no non-eDPI requests are sent to the D-PHY, even if there is traffic from generic, making it return to stop state. When it does so, PRESP_TO counter is activated and only when it finishes does the controller send any other traffic that is ready.
23:16	RO	0x0	reserved
15:0	RW	0x0000	hs_wr_to_cnt hs_wr_to_cnt This field sets a period for which the DSI HOST keeps the link inactive after sending a high-speed write operation. This period is measured in cycles of lanebyteclk. The counting starts when the D-PHY enters the Stop state and causes no interrupts.

MIPI_DSI_HOST_LP_WR_TO_CNT

Address: Operational Base + offset (0x0088)

Peripheral Response Timeout Definition after Lo

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	lp_wr_to_cnt lp_wr_to_cnt This field sets a period for which the DSI HOST keeps the link still, after sending a low-power write operation. This period is measured in cycles of lanebyteclk. The counting starts when the D-PHY enters the Stop state and causes no interrupts.

MIPI_DSI_HOST_BTA_TO_CNT

Address: Operational Base + offset (0x008c)

Peripheral Response Timeout Definition after B

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	bta_to_cnt bta_to_cnt This field sets a period for which the DWC_mipi_dsi_host keeps the link still, after completing a Bus Turn-Around. This period is measured in cycles of lanebyteclk. The counting starts when the D-PHY enters the Stop state and causes no interrupts.

MIPI_DSI_HOST_LPCLK_CTRL

Address: Operational Base + offset (0x0094)

Low-power in Clock Lane Register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1	RW	0x0	auto_clklane_ctrl auto_clklane_ctrl This bit enables the automatic mechanism to stop providing clock in the clock lane when time allows.
0	RW	0x0	phy_txrequestclkhs phy_txrequestclkhs This bit controls the D-PHY PPI txrequestclkhs signal.

MIPI_DSI_HOST_PHY_TMR_LPCLK_CFG
Address: Operational Base + offset (0x0098)
D-PHY Timing Configuration for the Clock Lane

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x000	phy_clkhs2lp_time phy_clkhs2lp_time This field configures the maximum time that the D-PHY clock lane takes to go from high-speed to low-power transmission measured in lane byte clock cycles.
15:10	RO	0x0	reserved
9:0	RW	0x000	phy_clklp2hs_time phy_clklp2hs_time This field configures the maximum time that the D-PHY clock lane takes to go from low-power to high-speed transmission measured in lane byte clock cycles.

MIPI_DSI_HOST_PHY_TMR_CFG
Address: Operational Base + offset (0x009c)
D-PHY Data Lanes Timing Configuration Registe

Bit	Attr	Reset Value	Description
31:24	RW	0x00	phy_hs2lp_time phy_hs2lp_time This field configures the maximum time that the D-PHY data lanes take to go from high-speed to low-power transmission measured in lane byte clock cycles.
23:16	RW	0x00	phy_lp2hs_time phy_lp2hs_time This field configures the maximum time that the D-PHY data lanes take to go from low-power to high-speed transmission measured in lane byte clock cycles.
15	RO	0x0	reserved
14:0	RW	0x0000	max_rd_time max_rd_time This field configures the maximum time required to perform a read command in lane byte clock cycles. This register can only be modified when no read command is in progress.

MIPI_DSI_HOST_PHY_RSTZ
Address: Operational Base + offset (0x00a0)
D-PHY Reset Control Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3	RW	0x0	phy_forcepll phy_forcepll When the D-PHY is in ULPS, this bit enables the D-PHY PLL. Dependency: DSI_HOST_FPGA = 0. Otherwise, this bit is reserved.
2	RW	0x0	phy_enableclk phy_enableclk When set to1, this bit enables the D-PHY Clock Lane module.
1	RW	0x0	phy_rstz phy_rstz When set to 0, this bit places the digital section of the D-PHY in the reset state.
0	RW	0x0	phy_shutdownz phy_shutdownz When set to 0, this bit places the D-PHY macro in power-down state.

MIPI_DSI_HOST_PHY_IF_CFG
Address: Operational Base + offset (0x00a4)
D-PHY Interface Configuration Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:8	RW	0x00	phy_stop_wait_time phy_stop_wait_time This field configures the minimum wait period to request a high-speed transmission after the Stop state.
7:2	RO	0x0	reserved
1:0	RW	0x3	n_lanes n_lanes This field configures the number of active data lanes: ■00: One data lane (lane 0) ■01: Two data lanes (lanes 0 and 1) ■10: Three data lanes (lanes 0, 1, and 2) ■11: Four data lanes (lanes 0, 1, 2, and 3)

MIPI_DSI_HOST_PHY_ULPS_CTRL
Address: Operational Base + offset (0x00a8)
D-PHY Ultra Low-Power Control Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	phy_txexitulpslan phy_txexitulpslan ULPS mode Exit on all active data lanes.
2	RW	0x0	phy_txrequlpslan phy_txrequlpslan ULPS mode Request on all active data lanes.
1	RW	0x0	phy_txexitulpsclk phy_txexitulpsclk ULPS mode Exit on clock lane.
0	RW	0x0	phy_txrequlpsclk phy_txrequlpsclk ULPS mode Request on clock lane.

MIPI_DSI_HOST_PHY_TX_TRIGGERS
Address: Operational Base + offset (0x00ac)
D-PHY Transmit Triggers Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x0	phy_tx_triggers phy_tx_triggers This field controls the trigger transmissions.

MIPI_DSI_HOST_PHY_STATUS
Address: Operational Base + offset (0x00b0)
Register0010 Abstract

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RO	0x0	phy_rxulpsesc0lane phy_rxulpsesc0lane This bit indicates the status of rxulpsesc0lane D-PHY signal.
5	RO	0x0	phy_ulpsactivenot0lane phy_ulpsactivenot0lane This bit indicates the status of ulpsactivenot0lane D-PHY signal.
4	RO	0x0	phy_stopstate0lane phy_stopstate0lane This bit indicates the status of phystopstate0lane D-PHY signal.
3	RO	0x0	phy_ulpsactivenotclk phy_ulpsactivenotclk This bit indicates the status of phyulpsactivenotclk D-PHY signal.
2	RO	0x0	phy_stopstateclklane phy_stopstateclklane phy_stopstateclklane
1	RO	0x0	phy_direction phy_direction This bit indicates the status of phydirection D-PHY signal.
0	RO	0x0	phy_lock phy_lock This bit indicates the status of phylock D-PHY signal.

MIPI_DSI_HOST_PHY_TST_CTRL0
Address: Operational Base + offset (0x00b4)
D-PHY Test Interface Control 0 Register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	phy_testclk phy_testclk This bit is used to clock the TESTDIN bus into the D-PHY.
0	RW	0x0	phy_testclr phy_testclr PHY test interface clear (active high).

MIPI_DSI_HOST_PHY_TST_CTRL1
Address: Operational Base + offset (0x00b8)
D-PHY Test Interface Control 1 Register

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved

Bit	Attr	Reset Value	Description
16	RW	0x0	phy_testen phy_testen PHY test interface operation selector: ■1: The address write operation is set on the falling edge of the testclk signal. ■0: The data write operation is set on the rising edge of the testclk signal.
15:8	RO	0x00	pht_testdout pht_testdout PHY output 8-bit data bus for read-back and internal probing functionalities.
7:0	RW	0x00	phy_testdin phy_testdin PHY test interface input 8-bit data bus for internal register programming and test functionalities access.

MIPI_DSI_HOST_INT_ST0

Address: Operational Base + offset (0x00bc)

Interrupt Status Register 0

Bit	Attr	Reset Value	Description
31:21	RO	0x0	reserved
20	RO	0x0	dphy_errors_4 dphy_errors_4 This bit indicates the LP1 contention error ErrContentionLP1 from Lane 0.
19	RO	0x0	dphy_errors_3 dphy_errors_3 This bit indicates the LP0 contention error ErrContentionLP0 from Lane 0.
18	RO	0x0	dphy_errors_2 dphy_errors_2 This bit indicates the ErrControl error from Lane 0.
17	RO	0x0	dphy_errors_1 dphy_errors_1 This bit indicates ErrSyncEsc low-power data transmission synchronization error from Lane 0.
16	RO	0x0	dphy_errors_0 dphy_errors_0 This bit indicates ErrEsc escape entry error from Lane 0.
15	RO	0x0	ack_with_err_15 ack_with_err_15 This bit retrieves the DSI protocol violation from the Acknowledge error report.
14	RO	0x0	ack_with_err_14 ack_with_err_14 This bit retrieves the reserved (specific to device) from the Acknowledge error report.
13	RO	0x0	ack_with_err_13 ack_with_err_13 This bit retrieves the invalid transmission length from the Acknowledge error report.

Bit	Attr	Reset Value	Description
12	RO	0x0	ack_with_err_12 ack_with_err_12 This bit retrieves the DSI VC ID Invalid from the Acknowledge error report.
11	RO	0x0	ack_with_err_11 ack_with_err_11 This bit retrieves the not recognized DSI data type from the Acknowledge error report.
10	RO	0x0	ack_with_err_10 ack_with_err_10 This bit retrieves the checksum error (long packet only) from the Acknowledge error report.
9	RO	0x0	ack_with_err_9 ack_with_err_9 This bit retrieves the ECC error, multi-bit (detected, not corrected) from the Acknowledge error report.
8	RO	0x0	ack_with_err_8 ack_with_err_8 This bit retrieves the ECC error, single-bit (detected and corrected) from the Acknowledge error report.
7	RO	0x0	ack_with_err_7 ack_with_err_7 This bit retrieves the reserved (specific to device) from the Acknowledge error report.
6	RO	0x0	ack_with_err_6 ack_with_err_6 This bit retrieves the False Control error from the Acknowledge error report.
5	RO	0x0	ack_with_err_5 ack_with_err_5 This bit retrieves the Peripheral Timeout error from the Acknowledge Error report.
4	RO	0x0	ack_with_err_4 ack_with_err_4 This bit retrieves the LP Transmit Sync error from the Acknowledge error report.
3	RO	0x0	ack_with_err_3 ack_with_err_3 This bit retrieves the Escape Mode Entry Command error from the Acknowledge error report.
2	RO	0x0	ack_with_err_2 ack_with_err_2 This bit retrieves the EoT Sync error from the Acknowledge error report.
1	RO	0x0	ack_with_err_1 ack_with_err_1 This bit retrieves the SoT Sync error from the Acknowledge error report.
0	RO	0x0	ack_with_err_0 ack_with_err_0 This bit retrieves the SoT error from the Acknowledge error report.

MIPI_DSI_HOST_INT_ST1
Address: Operational Base + offset (0x00c0)
Interrupt Status Register 1

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12	RO	0x0	gen_pld_recev_err gen_pld_recev_err This bit indicates that during a generic interface packet read back, the payload FIFO becomes full and the received data is corrupted.
11	RO	0x0	gen_pld_rd_err gen_pld_rd_err This bit indicates that during a DCS read data, the payload FIFO becomes empty and the data sent to the interface is corrupted.
10	RO	0x0	gen_pld_send_err gen_pld_send_err This bit indicates that during a Generic interface packet build, the payload FIFO becomes empty and corrupt data is sent.
9	RO	0x0	gen_pld_wr_err gen_pld_wr_err This bit indicates that the system tried to write a payload data through the Generic interface and the FIFO is full. Therefore, the payload is not written.
8	RO	0x0	gen_cmd_wr_err gen_cmd_wr_err This bit indicates that the system tried to write a command through the Generic interface and the FIFO is full. Therefore, the command is not written.
7	RO	0x0	dpi_pld_wr_err dpi_pld_wr_err This bit indicates that during a DPI pixel line storage, the payload FIFO becomes full and the data stored is corrupted.
6	RO	0x0	eopt_err eopt_err This bit indicates that the EoTp packet is not received at the end of the incoming peripheral transmission.
5	RO	0x0	pkt_size_err pkt_size_err This bit indicates that the packet size error is detected during the packet reception
4	RO	0x0	crc_err crc_err This bit indicates that the CRC error is detected in the received packet payload.
3	RO	0x0	ecc_multi_err ecc_multi_err This bit indicates that the ECC multiple error is detected in a received error.
2	RO	0x0	ecc_single_err ecc_single_err This bit indicates that the ECC single error is detected and corrected in a received packet.
1	RO	0x0	to_lp_rx to_lp_rx This bit indicates that the low-power reception timeout counter reached the end and contention is detected.
0	RO	0x0	to_hs_tx to_hs_tx This bit indicates that the high-speed transmission timeout counter reached the end and contention is detected.

MIPI_DSI_HOST_INT_MSK0
Address: Operational Base + offset (0x00c4)
Masks the Interrupt Generation Triggered by the

Bit	Attr	Reset Value	Description
31:21	RO	0x0	reserved
20	RO	0x0	dphy_errors_4 dphy_errors_4 This bit indicates the LP1 contention error ErrContentionLP1 from Lane 0.
19	RO	0x0	dphy_errors_3 dphy_errors_3 This bit indicates the LP0 contention error ErrContentionLP0 from Lane 0.
18	RO	0x0	dphy_errors_2 dphy_errors_2 This bit indicates the ErrControl error from Lane 0.
17	RO	0x0	dphy_errors_1 dphy_errors_1 This bit indicates ErrSyncEsc low-power data transmission synchronization error from Lane 0.
16	RO	0x0	dphy_errors_0 dphy_errors_0 This bit indicates ErrEsc escape entry error from Lane 0.
15	RO	0x0	ack_with_err_15 ack_with_err_15 This bit retrieves the DSI protocol violation from the Acknowledge error report.
14	RO	0x0	ack_with_err_14 ack_with_err_14 This bit retrieves the reserved (specific to device) from the Acknowledge error report.
13	RO	0x0	ack_with_err_13 ack_with_err_13 This bit retrieves the invalid transmission length from the Acknowledge error report.
12	RO	0x0	ack_with_err_12 ack_with_err_12 This bit retrieves the DSI VC ID Invalid from the Acknowledge error report.
11	RO	0x0	ack_with_err_11 ack_with_err_11 This bit retrieves the not recognized DSI data type from the Acknowledge error report.
10	RO	0x0	ack_with_err_10 ack_with_err_10 This bit retrieves the checksum error (long packet only) from the Acknowledge error report.
9	RO	0x0	ack_with_err_9 ack_with_err_9 This bit retrieves the ECC error, multi-bit (detected, not corrected) from the Acknowledge error report.
8	RO	0x0	ack_with_err_8 ack_with_err_8 This bit retrieves the ECC error, single-bit (detected and corrected) from the Acknowledge error report.

Bit	Attr	Reset Value	Description
7	RO	0x0	ack_with_err_7 ack_with_err_7 This bit retrieves the reserved (specific to device) from the Acknowledge error report.
6	RO	0x0	ack_with_err_6 ack_with_err_6 This bit retrieves the False Control error from the Acknowledge error report.
5	RO	0x0	ack_with_err_5 ack_with_err_5 This bit retrieves the Peripheral Timeout error from the Acknowledge Error report.
4	RO	0x0	ack_with_err_4 ack_with_err_4 This bit retrieves the LP Transmit Sync error from the Acknowledge error report.
3	RO	0x0	ack_with_err_3 ack_with_err_3 This bit retrieves the Escape Mode Entry Command error from the Acknowledge error report.
2	RO	0x0	ack_with_err_2 ack_with_err_2 This bit retrieves the EoT Sync error from the Acknowledge error report.
1	RO	0x0	ack_with_err_1 ack_with_err_1 This bit retrieves the SoT Sync error from the Acknowledge error report.
0	RO	0x0	ack_with_err_0 ack_with_err_0 This bit retrieves the SoT error from the Acknowledge error report.

MIPI_DSI_HOST_INT_MSK1

Address: Operational Base + offset (0x00c8)

Masks the Interrupt Generation Triggered by the

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12	RO	0x0	gen_pld_recev_err gen_pld_recev_err This bit indicates that during a generic interface packet read back, the payload FIFO becomes full and the received data is corrupted.
11	RO	0x0	gen_pld_rd_err gen_pld_rd_err This bit indicates that during a DCS read data, the payload FIFO becomes empty and the data sent to the interface is corrupted.
10	RO	0x0	gen_pld_send_err gen_pld_send_err This bit indicates that during a Generic interface packet build, the payload FIFO becomes empty and corrupt data is sent.
9	RO	0x0	gen_pld_wr_err gen_pld_wr_err This bit indicates that the system tried to write a payload data through the Generic interface and the FIFO is full. Therefore, the payload is not written.

Bit	Attr	Reset Value	Description
8	RO	0x0	gen_cmd_wr_err gen_cmd_wr_err This bit indicates that the system tried to write a command through the Generic interface and the FIFO is full. Therefore, the command is not written.
7	RO	0x0	dpi_pld_wr_err dpi_pld_wr_err This bit indicates that during a DPI pixel line storage, the payload FIFO becomes full and the data stored is corrupted.
6	RO	0x0	eopt_err eopt_err This bit indicates that the EoTp packet is not received at the end of the incoming peripheral transmission.
5	RO	0x0	pkt_size_err pkt_size_err This bit indicates that the packet size error is detected during the packet reception
4	RO	0x0	crc_err crc_err This bit indicates that the CRC error is detected in the received packet payload.
3	RO	0x0	ecc_multi_err ecc_multi_err This bit indicates that the ECC multiple error is detected in a received error.
2	RO	0x0	ecc_single_err ecc_single_err This bit indicates that the ECC single error is detected and corrected in a received packet.
1	RO	0x0	to_lp_rx to_lp_rx This bit indicates that the low-power reception timeout counter reached the end and contention is detected.
0	RO	0x0	to_hs_tx to_hs_tx This bit indicates that the high-speed transmission timeout counter reached the end and contention is detected.

MIPI_DSI_HOST_INT_FORCE0

Address: Operational Base + offset (0x00d8)

Force Interrupt Configuration Register

Bit	Attr	Reset Value	Description
31:21	RO	0x0	reserved
20	WO	0x0	dphy_errors_4 dphy_errors_4 This bit indicates the LP1 contention error ErrContentionLP1 from Lane 0.
19	WO	0x0	dphy_errors_3 dphy_errors_3 This bit indicates the LP0 contention error ErrContentionLP0 from Lane 0.
18	WO	0x0	dphy_errors_2 dphy_errors_2 This bit indicates the ErrControl error from Lane 0.

Bit	Attr	Reset Value	Description
17	WO	0x0	dphy_errors_1 dphy_errors_1 This bit indicates ErrSyncEsc low-power data transmission synchronization error from Lane 0.
16	WO	0x0	dphy_errors_0 dphy_errors_0 This bit indicates ErrEsc escape entry error from Lane 0.
15	WO	0x0	ack_with_err_15 ack_with_err_15 This bit retrieves the DSI protocol violation from the Acknowledge error report.
14	WO	0x0	ack_with_err_14 ack_with_err_14 This bit retrieves the reserved (specific to device) from the Acknowledge error report.
13	WO	0x0	ack_with_err_13 ack_with_err_13 This bit retrieves the invalid transmission length from the Acknowledge error report.
12	WO	0x0	ack_with_err_12 ack_with_err_12 This bit retrieves the DSI VC ID Invalid from the Acknowledge error report.
11	WO	0x0	ack_with_err_11 ack_with_err_11 This bit retrieves the not recognized DSI data type from the Acknowledge error report.
10	WO	0x0	ack_with_err_10 ack_with_err_10 This bit retrieves the checksum error (long packet only) from the Acknowledge error report.
9	WO	0x0	ack_with_err_9 ack_with_err_9 This bit retrieves the ECC error, multi-bit (detected, not corrected) from the Acknowledge error report.
8	WO	0x0	ack_with_err_8 ack_with_err_8 This bit retrieves the ECC error, single-bit (detected and corrected) from the Acknowledge error report.
7	WO	0x0	ack_with_err_7 ack_with_err_7 This bit retrieves the reserved (specific to device) from the Acknowledge error report.
6	WO	0x0	ack_with_err_6 ack_with_err_6 This bit retrieves the False Control error from the Acknowledge error report.
5	WO	0x0	ack_with_err_5 ack_with_err_5 This bit retrieves the Peripheral Timeout error from the Acknowledge Error report.
4	WO	0x0	ack_with_err_4 ack_with_err_4 This bit retrieves the LP Transmit Sync error from the Acknowledge error report.

Bit	Attr	Reset Value	Description
3	WO	0x0	ack_with_err_3 ack_with_err_3 This bit retrieves the Escape Mode Entry Command error from the Acknowledge error report.
2	WO	0x0	ack_with_err_2 ack_with_err_2 This bit retrieves the EoT Sync error from the Acknowledge error report.
1	WO	0x0	ack_with_err_1 ack_with_err_1 This bit retrieves the SoT Sync error from the Acknowledge error report.
0	WO	0x0	ack_with_err_0 ack_with_err_0 This bit retrieves the SoT error from the Acknowledge error report.

MIPI_DSI_HOST_INT_FORCE1

Address: Operational Base + offset (0x00dc)

Force Interrupt Configuration Register

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12	WO	0x0	gen_pld_recev_err gen_pld_recev_err This bit indicates that during a generic interface packet read back, the payload FIFO becomes full and the received data is corrupted.
11	WO	0x0	gen_pld_rd_err gen_pld_rd_err This bit indicates that during a DCS read data, the payload FIFO becomes empty and the data sent to the interface is corrupted.
10	WO	0x0	gen_pld_send_err gen_pld_send_err This bit indicates that during a Generic interface packet build, the payload FIFO becomes empty and corrupt data is sent.
9	WO	0x0	gen_pld_wr_err gen_pld_wr_err This bit indicates that the system tried to write a payload data through the Generic interface and the FIFO is full. Therefore, the payload is not written.
8	WO	0x0	gen_cmd_wr_err gen_cmd_wr_err This bit indicates that the system tried to write a command through the Generic interface and the FIFO is full. Therefore, the command is not written.
7	WO	0x0	dpi_pld_wr_err dpi_pld_wr_err This bit indicates that during a DPI pixel line storage, the payload FIFO becomes full and the data stored is corrupted.
6	WO	0x0	eopt_err eopt_err This bit indicates that the EoTp packet is not received at the end of the incoming peripheral transmission.

Bit	Attr	Reset Value	Description
5	WO	0x0	pkt_size_err pkt_size_err This bit indicates that the packet size error is detected during the packet reception
4	WO	0x0	crc_err crc_err This bit indicates that the CRC error is detected in the received packet payload.
3	WO	0x0	ecc_multi_err ecc_multi_err This bit indicates that the ECC multiple error is detected in a received error.
2	WO	0x0	ecc_single_err ecc_single_err This bit indicates that the ECC single error is detected and corrected in a received packet.
1	WO	0x0	to_lp_rx to_lp_rx This bit indicates that the low-power reception timeout counter reached the end and contention is detected.
0	WO	0x0	to_hs_tx to_hs_tx This bit indicates that the high-speed transmission timeout counter reached the end and contention is detected.

9.5 Application Notes

9.5.1 COMMON CONFIGURATION (DEFAULT IN MIPI MODE)

Step1: Enable reference clock.
Step2: Wait a period after reference clock have been enabled.
Step3: Send 0xe4 to register MIPI_DSI_DPHY_CTRL_PWRCTL. Enable PLL and LDO.
Step4: Send 0x7d to register MIPI_DSI_DPHY_CTRL_LANE_ENABLE. Enable all lanes on analog part.
Step5: Send 0xe0 to register MIPI_DSI_DPHY_CTRL_PWRCTL. Reset analog.
Step6: Wait a period after analog has been reset.
Step7: Send 0x1e to register MIPI_DSI_DPHY_CTRL_DIG_RST. Reset digital.
Step8: Send 0x1f to register MIPI_DSI_DPHY_CTRL_DIG_RST. Reset digital.
Step9: Wait a period until pll locked. Run in MIPI mode.

9.5.2 LOW POWER MODE (FOR DSI ONLY)

Low Power Mode is a special feature for D-PHY. You can control this function by using proper registers from the Innosilicon D-PHY with few operations. The following is a step by step instruction for low power mode in and out.
Perform the following steps to configure the DPI packet transmission:
Step1:Global configuration:
Configure n_lanes (PHY_IF_CFG-[1:0]) to define the number of lanes in which the controller has to perform high-speed transmissions.
Step2:Configure the DPI Interface to define how the DPI interface interacts with the controller.
Configure dpi_vid (DPI_CFG-[1:0]): This field configures the virtual channel that the packet generated by the DPI interface is indexed to.
Configure dpi_color_coding (DPI_CFG-[4:2]): This field configures the bits per pixels that the interface transmits and also the variant configuration of each bpp. If you select 18 bpp, and the Enable_18_loosely_packed is not active, the number or pixels per line should be a multiple of four.
Configure dataen_active_low (DPI_CFG-[5]): This bit configures the polarity of the dpidataen

signal and enables if it is active low.
Configure vsync_active_low(DPI_CFG-[6]): This bit configures the polarity of the dpivsync signal and enables if it is active low.
Configure vsync_active_low(DPI_CFG-[7]): This bit configures the polarity of the dpivsync signal and enables if it is active low.
Configure vsync_active_low(DPI_CFG-[8]): This bit configures the polarity of the dpishutdn signal and enables if it is active low.
Configure vsync_active_low(DPI_CFG-[9]): This bit configures the polarity of the dpicolorm signal and enables if it is active low.
Configure en18_loosely(DPI_CFG-[10]): This bit configures if the pixel packing is done loosely or packed when dpi_color_coding is 18 bpp. This bit enables loosely packing.
Step3: Select the Video Transmission Mode to define how the processor requires the video line to be transported through the DSI link.
Configure low-power transitions (VID_MODE_CFG-[8:3]): This defines the video line to be transported through the DSI link.
Configure low-power transitions (VID_MODE_CFG-[8:3]): This defines the video periods which are permitted to go to low-power if there is available time to do so.
Configure frame_BTA_ack (VID_MODE_CFG-[11]): This specifies if the controller should request the peripheral acknowledge message at the end of frames.
Burst mode: In this mode, the entire active pixel line is buffered into a FIFO and transmitted in a single packed with no interruptions. This transmission mode requires that the DPI Pixel FIFO has the capacity to store a full line of active pixel data inside it. This mode is optimally used if the difference between pixel required bandwidth and DSI link bandwidth is very different. This enables the DWC_mipi_dsi_host to quickly dispatch the entire active video line in a single burst of data and then return to low-power mode.
Configure the register fiedl vid_mode_type (VID_MODE_CFG-[10]), num_chunks (VID_PKT_CFG-[20:11]), and null_pkt_size (VID_PKT_CFG-[30:21]) are automatically ignored by the DWC_mipi_dsi_host.
Non-Burst mode: In this mode, the processor uses the partitioning properties of the DWC_mipi_dsi_host to divide the video line transmission into several DSI packets. This is done to match th pixel required bandwidth with the DSI link bandwidth. With this mode, the controller configuration dose not require a full line of pixel data to be stored inside the DPI Pixel FIFO. It requires only the content of one video packet.
Configure the vid_mode_type field (VID_MODE_CFG-[2:1]) with 2’b0x.
Configure the vid_mode_type field (VID_MODE_CFG-[2:1]) with 2’b00x to enable the transmission of sync pulses.
Configure the vid_mode_type field (VID_MODE_CFG-[2:1]) with 2’b01to enable the transmission of sync events.
Configure the vid_mode_type field (VID_MODE_CFG-[10:0]) with the number of pixels to be transmitted in a single packet.
Configure the en_multi_pkt field (VID_MODE_CFG-[9]) to enable the division of the active video transmission into more than one packet.
Configure the num_chunks field (VID_MODE_CFG-[20:11]) with the number of video chunks that the active video transmission is divided into.
Configure the en_null_pkt field (VID_MODE_CFG-[10]) to enable the insertion of null packets between video packets.
The field is effective only when en_multi_pkt field is activated, otherwise the controller ignores it and does not sent the null packets.
Configure the null_pkt_size field (VID_MODE_CFG-[30:21]) with the actual size of the inserted null packet.
Step4:Define the DPI Horizontal timing configuration as follows:
Configure the hline_time field (TMR_LINE_CFG-[31:18]) with the time taken by a DPI video line accounted in Clock Lane bytes clock cycles (for a clock lane at 500 MHz the Lane byte clock period is 8 ns). When the DPI clock and Clock Lane clock are not multiples, the hline_time is a result of a round of a number. If the DWC_mipi_dsi_host is configured to go to low-power, it is possible that the error included in a line is incremented with the next one. At the end of several lines, the DWC_mipi_dsi_host can have a number of errors that can cause

a malfunction of the video transmission.
Configure the hsa_time field (TMR_LINE_CFG-[8:0]) with the time taken by a DPI Horizontal Sync Active period accounted in Clock Lane byte clock cycles (normally a period of 8ns).
Configure the hbp_time field (TMR_LINE_CFG-[17:9]) with the time taken by a DPI Horizontal Sync Active period accounted in Clock Lane byte clock cycles (normally a period of 8ns). Special attention should be given to the calculation of this parameter.
Step5:Define the Vertical line configuration:
Configure the vsa_lines field (VTIMING_CFG-[3:0]) with the number of lines existing in the DPI Vertical Sync Active period.
Configure the vbp_lines field (VTIMING_CFG-[9:4]) with the number of lines existing in the DPI Vertical Back Porch period.
Configure the vfp_lines field (VTIMING_CFG-[15:10]) with the number of lines existing in the DPI Vertical Front Porch period.
Configure the v_active_lines field (VTIMING_CFG-[26:16]) with the number of lines existing in the DPI Vertical Active period.

Chapter 10 Crypto

10.1 Overview

Crypto is a hardware accelerator of encrypting or decrypting. There are two Crypto blocks in RK3399: Crypto0 and Crypto1. Crypto0 supports the most commonly used algorithm: DES/3DES, AES, SHA1, SHA256, MD5 and RSA. Crypto1 supports these above algorithms except RSA.

The Crypto0 supports following features:

- Support AES 128/192/256 bits key mode, ECB/CBC/CTR/XTS chain mode, Slave/FIFO mode
- Support DES/3DES (ECB and CBC chain mode) , 3DES (EDE/ EEE key mode), Slave/FIFO mode
- Support SHA1/SHA256/MD5 (with hardware padding) HASH function, FIFO mode only
- Support 160 bit Pseudo Random Number Generator (PRNG)
- Support 256 bit True Random Number Generator (TRNG)
- Support PKA 512/1024/2048 bit Exp Modulator
- Support up to 200M clock frequency

10.2 Block Diagram

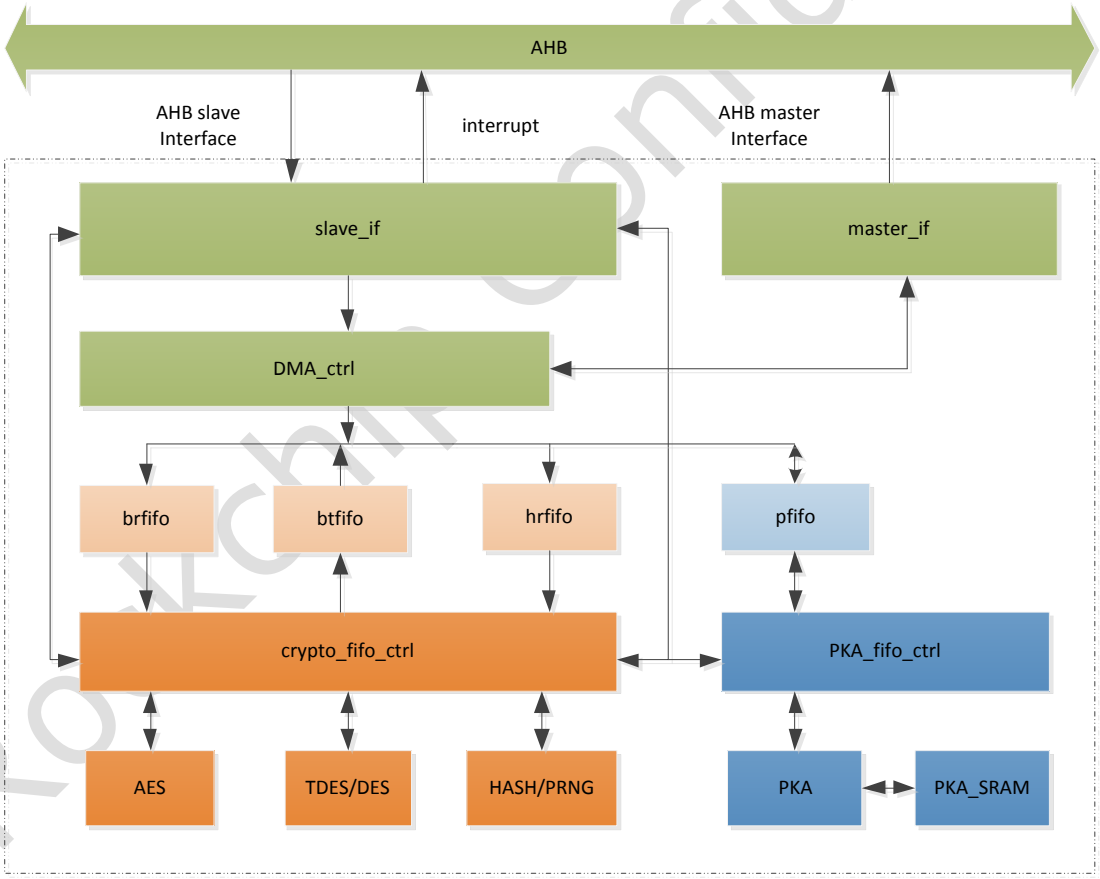


Fig. 10-1 Crypto Architecture

Figure above shows the architecture of Crypto.

10.3 Register description

10.3.1 Register Summary

Name	Offset	Size	Reset Value	Description

Name	Offset	Size	Reset Value	Description
Crypto_INTSTS	0x00000	W	0x00000000	Interrupt Status Register
Crypto_INTENA	0x00004	W	0x00000000	Interrupt Set Register
Crypto_CTRL	0x00008	W	0x00000000	Control Register
Crypto_CONF	0x0000c	W	0x00000000	Configure Register
Crypto_BRDMAS	0x00010	W	0x00000000	Block Receiving DMA Start Address Register
Crypto_BTDMAS	0x00014	W	0x00000000	Block Transmiting DMA Start Address Register
Crypto_BRDMAL	0x00018	W	0x00000000	Block Receiving DMA Length Register
Crypto_HRDMAS	0x0001c	W	0x00000000	Hash Receiving DMA Start Address Register
Crypto_HRDMAL	0x00020	W	0x00000000	Hash Receiving DMA Length Register
Crypto_AES_CTRL	0x00080	W	0x00000000	AES Control Register
Crypto_AES_STS	0x00084	W	0x00000000	Status Register
Crypto_AES_DIN_0	0x00088	W	0x00000000	AES Input Data 0 Register
Crypto_AES_DIN_1	0x0008c	W	0x00000000	AES Input Data 1 Register
Crypto_AES_DIN_2	0x00090	W	0x00000000	AES Input Data 2 Register
Crypto_AES_DIN_3	0x00094	W	0x00000000	AES Input Data 3 Register
Crypto_AES_DOUT_0	0x00098	W	0x00000000	AES Output Data 0 Register
Crypto_AES_DOUT_1	0x0009c	W	0x00000000	AES Output Data 1 Register
Crypto_AES_DOUT_2	0x000a0	W	0x00000000	AES Output Data 2 Register
Crypto_AES_DOUT_3	0x000a4	W	0x00000000	AES Output Data 3 Register
Crypto_AES_IV_0	0x000a8	W	0x00000000	AES IV data 0 Register
Crypto_AES_IV_1	0x000ac	W	0x00000000	AES IV data 1 Register
Crypto_AES_IV_2	0x000b0	W	0x00000000	AES IV data 2 Register
Crypto_AES_IV_3	0x000b4	W	0x00000000	AES IV data 3 Register
Crypto_AES_KEY_0	0x000b8	W	0x00000000	AES Key data 0 Register
Crypto_AES_KEY_1	0x000bc	W	0x00000000	AES Key data 1 Register
Crypto_AES_KEY_2	0x000c0	W	0x00000000	AES Key data 2 Register
Crypto_AES_KEY_3	0x000c4	W	0x00000000	AES Key data 3 Register
Crypto_AES_KEY_4	0x000c8	W	0x00000000	AES Key data 4 Register
Crypto_AES_KEY_5	0x000cc	W	0x00000000	AES Key data 5 Register
Crypto_AES_KEY_6	0x000d0	W	0x00000000	AES Key data 6 Register
Crypto_AES_KEY_7	0x000d4	W	0x00000000	AES Key data 7 Register
Crypto_AES_CNT_0	0x000d8	W	0x00000000	AES Input Counter 0 Register
Crypto_AES_CNT_1	0x000dc	W	0x00000000	AES Input Counter 1 Register
Crypto_AES_CNT_2	0x000e0	W	0x00000000	AES Input Counter 2 Register
Crypto_AES_CNT_3	0x000e4	W	0x00000000	AES Input Counter 3 Register
Crypto_TDES_CTRL	0x00100	W	0x00000000	TDES Control Register
Crypto_TDES_STS	0x00104	W	0x00000000	Status Register
Crypto_TDES_DIN_0	0x00108	W	0x00000000	TDES Input Data 0 Register
Crypto_TDES_DIN_1	0x0010c	W	0x00000000	TDES Input Data 1 Register

Name	Offset	Size	Reset Value	Description
Crypto_TDES_DOUT_0	0x00110	W	0x00000000	TDES Output Data 0 Register
Crypto_TDES_DOUT_1	0x00114	W	0x00000000	TDES Output Data 1 Register
Crypto_TDES_IV_0	0x00118	W	0x00000000	TDES IV data 0 Register
Crypto_TDES_IV_1	0x0011c	W	0x00000000	TDES IV data 1 Register
Crypto_TDES_KEY1_0	0x00120	W	0x00000000	TDES Key1 data 1 Register
Crypto_TDES_KEY1_1	0x00124	W	0x00000000	TDES Key1 data 1 Register
Crypto_TDES_KEY2_0	0x00128	W	0x00000000	TDES Key2 data 0 Register
Crypto_TDES_KEY2_1	0x0012c	W	0x00000000	TDES Key2 data 1 Register
Crypto_TDES_KEY3_0	0x00130	W	0x00000000	TDES Key3 data 0 Register
Crypto_TDES_KEY3_1	0x00134	W	0x00000000	TDES Key3 data 1 Register
Crypto_HASH_CTRL	0x00180	W	0x00000000	Hash Control Register
Crypto_HASH_STS	0x00184	W	0x00000000	Hash Status Register
Crypto_HASH_MSG_LEN	0x00188	W	0x00000000	Hash Message Len
Crypto_HASH_DOUT_0	0x0018c	W	0x00000000	Hash Result Register 0
Crypto_HASH_DOUT_1	0x00190	W	0x00000000	Hash Result Register 1
Crypto_HASH_DOUT_2	0x00194	W	0x00000000	Hash Result Register 2
Crypto_HASH_DOUT_3	0x00198	W	0x00000000	Hash Result Register 3
Crypto_HASH_DOUT_4	0x0019c	W	0x00000000	Hash Result Register 4
Crypto_HASH_DOUT_5	0x001a0	W	0x00000000	Hash Result Register 5
Crypto_HASH_DOUT_6	0x001a4	W	0x00000000	Hash Result Register 6
Crypto_HASH_DOUT_7	0x001a8	W	0x00000000	Hash Result Register 7
Crypto_HASH_SEED_0	0x001ac	W	0x00000000	PRNG Seed/HMAC Key Register 0
Crypto_HASH_SEED_1	0x001b0	W	0x00000000	PRNG Seed/HMAC Key Register 1
Crypto_HASH_SEED_2	0x001b4	W	0x00000000	PRNG Seed/HMAC Key Register 2
Crypto_HASH_SEED_3	0x001b8	W	0x00000000	PRNG Seed/HMAC Key Register 3
Crypto_HASH_SEED_4	0x001bc	W	0x00000000	PRNG Seed/HMAC Key Register 4
Crypto_TRNG_CTRL	0x00200	W	0x00000000	TRNG Control register
Crypto_TRNG_DOUT_0	0x00204	W	0x00000000	TRNG output register 0
Crypto_TRNG_DOUT_1	0x00208	W	0x00000000	TRNG output register 1
Crypto_TRNG_DOUT_2	0x0020c	W	0x00000000	TRNG output register 2
Crypto_TRNG_DOUT_3	0x00210	W	0x00000000	TRNG output register 3
Crypto_TRNG_DOUT_4	0x00214	W	0x00000000	TRNG output register 4
Crypto_TRNG_DOUT_5	0x00218	W	0x00000000	TRNG output register 5
Crypto_TRNG_DOUT_6	0x0021c	W	0x00000000	TRNG output register 6
Crypto_TRNG_DOUT_7	0x00220	W	0x00000000	TRNG output register 7
Crypto_PKA_CTRL	0x00280	W	0x00000000	PKA Control Register
Crypto_AES_TKEY_0	0x00300	W	0x00000000	AES Tweak Key data 0 Register
Crypto_AES_TKEY_1	0x00304	W	0x00000000	AES Tweak Key data 1 Register
Crypto_AES_TKEY_2	0x00308	W	0x00000000	AES Tweak Key data 2 Register
Crypto_AES_TKEY_3	0x0030c	W	0x00000000	AES Tweak Key data 3 Register
Crypto_AES_TKEY_4	0x00310	W	0x00000000	AES Tweak Key data 4 Register
Crypto_AES_TKEY_5	0x00314	W	0x00000000	AES Tweak Key data 5 Register
Crypto_AES_TKEY_6	0x00318	W	0x00000000	AES Tweak Key data 6 Register
Crypto_AES_TKEY_7	0x0031c	W	0x00000000	AES Tweak Key data 7 Register

Name	Offset	Size	Reset Value	Description
Crypto_AES_TWK_0	0x00320	W	0x00000000	AES Tweak data 0 Register
Crypto_AES_TWK_1	0x00324	W	0x00000000	AES Tweak data 1 Register
Crypto_AES_TWK_2	0x00328	W	0x00000000	AES Tweak data 2 Register
Crypto_AES_TWK_3	0x0032c	W	0x00000000	AES Tweak data 3 Register
Crypto_KEY_SECURE	0x00330	W	0x00000000	Key Secure Control Register
Crypto_CLK_GATE	0x00334	W	0x0000000f	Clock Gate Control Register
Crypto_CRYPTO_VER	0x003f0	W	0x00000300	Crypto Version register
Crypto_PKA_M	0x0400	W	0x00000000	PKA input/output data
Crypto_PKA_C	0x0500	W	0x00000000	PKA C value
Crypto_PKA_N	0x0600	W	0x00000000	PKA modular
Crypto_PKA_E	0x0700	W	0x00000000	PKA exponent

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

10.3.2 Detail Register Description

Crypto_INTSTS
Address: Operational Base + offset (0x0000)
Interrupt Status Register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x0	PKA_DONE_INT PKA Done Interrupt
4	W1C	0x0	HASH_DONE_INT Hash Done Interrupt
3	W1C	0x0	HRDMA_ERR_INT Specifies the interrupt of hash receiving DMA Error
2	W1C	0x0	HRDMA_DONE_INT Specifies the interrupt of hash receiving DMA Done
1	W1C	0x0	BCDMA_ERR_INT Specifies the interrupt of block cipher Error
0	W1C	0x0	BCDMA_DONE_INT Specifies the interrupt of block cipher Done

Crypto_INTENA
Address: Operational Base + offset (0x0004)
Interrupt Set Register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x0	PKA_DONE_ENA Set the interrupt Enable of PKA done 1'b1: enable 1'b0: disable

Bit	Attr	Reset Value	Description
4	RW	0x0	HASH_DONE_ENA Set the interrupt Enable of hash done 1'b1: enable 1'b0: disable
3	RW	0x0	HRDMA_ERR_ENA Set the interrupt Enable of hash receiving DMA Error 1'b1: enable 1'b0: disable
2	RW	0x0	HRDMA_DONE_ENA Set the interrupt Enable of hash receiving DMA DONE 1'b1: enable 1'b0: disable
1	RW	0x0	BCDMA_ERR_ENA Set the interrupt Enable of block cipher DMA Error 1'b1: enable 1'b0: disable
0	RW	0x0	BCDMA_DONE_ENA Set the interrupt Enable of block cipher DMA DONE 1'b1: enable 1'b0: disable

Crypto_CTRL
Address: Operational Base + offset (0x0008)
Control Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	Write_Mask
15:10	RO	0x0	reserved
9	RW	0x0	TRNG_FLUSH Flush TRNG Software write 1 to start. When finishes, the core will clear it.
8	R/WSC	0x0	TRNG_START Start TRNG Software write 1 to start. When finishes, the core will clear it.
7	R/WSC	0x0	PKA_FLUSH Software write 1 to start Flush Process.The process will clear BRFIFO, BTFIFO, and state machine. Then Software should write 0 to end FLUSH Process
6	RW	0x0	HASH_FLUSH Software write 1 to start Flush Process. The process will clear BRFIFO, BTFIFO, and state machine. Then Software should write 0 to end FLUSH Process

Bit	Attr	Reset Value	Description
5	RW	0x0	BLOCK_FLUSH Software write 1 to start Flush Process. The process will clear BRFIFO, BTFIFO, and state machine. Then Software should write 0 to end FLUSH Process. It must last for at least 20 cycles to clean registers and FSM
4	R/W SC	0x0	PKA_START Starts/initializes PKA Software write 1 to start. When finishes, the core will clear it.
3	R/W SC	0x0	HASH_START Starts/initializes HASH/PRNG/HMAC Software write 1 to start. When finishes, the core will clear it.
2	R/W SC	0x0	BLOCK_START Starts/initializes Block Cipher Software write 1 to start. When finishes, the core will clear it.
1	R/W SC	0x0	TDES_START Starts/initializes TDES Software write 1 to start. When finishes, the core will clear it.
0	R/W SC	0x0	AES_START Starts/initializes AES Software write 1 to start. When finishes, the core will clear it.

Crypto_CONF
Address: Operational Base + offset (0x000c)
Control Register

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8	RW	0x0	HR_ADDR_MODE Hash Receive DMA Address Mode 1'b1: fix 1'b0: increment
7	RW	0x0	BT_ADDR_MODE Block Transmit DMA Address Mode 1'b1: fix 1'b0: increment
6	RW	0x0	BR_ADDR_MODE Block Receive DMA Address Mode 1'b1: fix 1'b0: increment
5	RW	0x0	Byteswap_HRFIFO If this bit is high, then the data read from the bus is byte-swapped in a word boundary. If this bit is low (default), then the data is handed over to the FIFO without byte-swap. For little endian bus, this bit should be 1'b1.

Bit	Attr	Reset Value	Description
4	RW	0x0	Byteswap_BTFIFO If this bit is high, then the data read from the bus is byte-swapped in a word boundary. If this bit is low (default), then the data is handed over to the FIFO without byte-swap. For little endian bus, this bit should be 1'b1.
3	RW	0x0	Byteswap_BRFIFO If this bit is high, then the data read from the bus is byte-swapped in a word boundary. If this bit is low (default), then the data is handed over to the FIFO without byte-swap. For little endian bus, this bit should be 1'b1.
2	RW	0x0	DESSEL Specifies the Destination block cipher of FIFO. 1'b0:AES; 1'b1:DES.
1:0	RW	0x0	HASHINSEL Specifies the following 2'b00:Data from independent source; 2'b01:Data from block cipher input; 2'b10:Data from block cipher output; 2'b11:Reserved.

Crypto_BRDMAS
Address: Operational Base + offset (0x0010)
Block Receiving DMA Start Address Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	STARTADDR Specifies the Start Address of DMA The address should be aligned by 32-bit.

Crypto_BTDMAS
Address: Operational Base + offset (0x0014)
Block Transmiting DMA Start Address Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	STARTADDR Specifies the Start Address of DMA The address needs to be aligned by 32-bit.

Crypto_BRDMAL
Address: Operational Base + offset (0x0018)
Block Receiving DMA Length Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LENGTH Specifies the Block length of DMA. The length unit is WORD.

Crypto_HRDMAS
Address: Operational Base + offset (0x001c)
Hash Receiving DMA Start Address Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	STARTADDR Specifies the Start Address of DMA The address needs to be aligned by 32-bit.

Crypto_HRDMAL
Address: Operational Base + offset (0x0020)
Hash Receiving DMA Length Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LENGTH Specifies the Block length of DMA. The length unit is BYTE.

Crypto_AES_CTRL
Address: Operational Base + offset (0x0080)
AES Control Register

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13	RW	0x0	AES_ByteSwap_TWK Change the Big-endian and Little-endian by swapping the byte oder. 0 = Disables Tweak Value byte swap 1 = Enables Tweak Valuebyte swap
12	RW	0x0	AES_ByteSwap_Tkey Change the Big-endian and Little-endian by swapping the byte oder. 0 = Disables Tweak Key byte swap 1 = Enables Tweak Key byte swap
11	RW	0x0	AES_ByteSwap_CNT Change the Big-endian and Little-endian by swapping the byte oder. 0 = Disables Counter data byte swap 1 = Enables Counter data byte swap
10	RW	0x0	AES_ByteSwap_Key Change the Big-endian and Little-endian by swapping the byte oder. 0 = Disables Key byte swap 1 = Enables Key byte swap
9	RW	0x0	AES_ByteSwap_IV Change the Big-endian and Little-endian by swapping the byte oder. 0 = Disables Initial value byte swap 1 = Enables Initial value byte swap

Bit	Attr	Reset Value	Description
8	RW	0x0	AES_ByteSwap_DO Change the Big-endian and Little-endian by swapping the byte oder. 0 = Disables Output data byte swap 1 = Enables Output data byte swap
7	RW	0x0	AES_ByteSwap_DI Change the Big-endian and Little-endian by swapping the byte oder. 0 = Disables Input data byte swap 1 = Enables Input data byte swap
6	RW	0x0	AES_KeyChange Specifies the AES key change mode selection signal. When the bit is asserted, it will not do key-expansion function to calculate new sub-key. So it is a faster way, when several times of calculation use the same key. But if the keys are different, asserting this bit will have the wrong result. 0 = Key is not changed 1 = Key is changed
5:4	RW	0x0	AES_ChainMode Specifies AES chain mode selection 00 = ECB mode 01 = CBC mode 10 = CTR mode 11 = XTS mode
3:2	RW	0x0	AES_KeySize Specifies the AES key size selection signal 00 : 128-bit key 01 : 192-bit key 10 : 256-bit key
1	RW	0x0	AES_FifoMode Specify AES Fifo Mode 1'b0: Slave mode 1'b1: fifo mode
0	RW	0x0	AES_Enc Specifies the Encryption/ Decryption mode selection signal 0 : Encryption 1 : Decryption

Crypto_AES_STS
Address: Operational Base + offset (0x0084)
Status Register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	AES_DONE When AES finish, it will be HIGH, And it will not be LOW until it restart . 1: done 0: not done

Crypto_AES_DIN_0
Address: Operational Base + offset (0x0088)
AES Input Data 0 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_DIN_0 Specifies AES Input data [127:96].

Crypto_AES_DIN_1
Address: Operational Base + offset (0x008c)
AES Input Data 1 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_DIN_1 Specifies AES Input data [95:64].

Crypto_AES_DIN_2
Address: Operational Base + offset (0x0090)
AES Input Data 2 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_DIN_2 Specifies AES Input data [63:32]

Crypto_AES_DIN_3
Address: Operational Base + offset (0x0094)
AES Input Data 3 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_DIN_3 Specifies AES Input data [31:0]

Crypto_AES_DOUT_0
Address: Operational Base + offset (0x0098)
AES Output Data 0 Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	AES_DOUT_0 Specifies AES Output data [127:96].

Crypto_AES_DOUT_1
Address: Operational Base + offset (0x009c)
AES Output Data 1 Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	AES_DOUT_1 Specifies the Output data [95:64].

Crypto_AES_DOUT_2
Address: Operational Base + offset (0x00a0)
AES Output Data 2 Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	AES_DOUT_2 Specifies AES Output data [63:32].

Crypto_AES_DOUT_3
Address: Operational Base + offset (0x00a4)
AES Output Data 3 Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	AES_DOUT_3 Specifies AES Output data [31:0].

Crypto_AES_IV_0
Address: Operational Base + offset (0x00a8)
AES IV data 0 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_IV_0 Specifies AES Initialization vector [127:96]

Crypto_AES_IV_1
Address: Operational Base + offset (0x00 ac)
AES IV data 1 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_IV_1 Specifies AES Initialization vector [95:64]

Crypto_AES_IV_2
Address: Operational Base + offset (0x00b0)
AES IV data 2 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_IV_2 Specifies AES Initialization vector [63:32]

Crypto_AES_IV_3
Address: Operational Base + offset (0x00b4)
AES IV data 3 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_IV_3 Specifies AES Initialization vector [31:0]

Crypto_AES_KEY_0
Address: Operational Base + offset (0x00b8)
AES Key data 0 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_KEY_0 Specifies AES key data [255:224]

Crypto_AES_KEY_1
Address: Operational Base + offset (0x00bc)
AES Key data 1 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_KEY_1 Specifies AES key data [223:192]

Crypto_AES_KEY_2
Address: Operational Base + offset (0x00c0)
AES Key data 2 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_KEY_2 Specifies AES key data [191:160]

Crypto_AES_KEY_3
Address: Operational Base + offset (0x00c4)
AES Key data 3 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_KEY_3 Specifies AES key data [159:128]

Crypto_AES_KEY_4
Address: Operational Base + offset (0x00c8)
AES Key data 4 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_KEY_4 Specifies AES key data [127:96]

Crypto_AES_KEY_5
Address: Operational Base + offset (0x00cc)
AES Key data 5 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_KEY_5 Specifies the key data [95:64]

Crypto_AES_KEY_6
Address: Operational Base + offset (0x00d0)
AES Key data 6 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_KEY_6 Specifies AES key data [63:32]

Crypto_AES_KEY_7
Address: Operational Base + offset (0x00d4)
AES Key data 7 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_KEY_7 Specifies the key data [31:0]

Crypto_AES_CNT_0
Address: Operational Base + offset (0x00d8)
AES Input Counter 0 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_CNT_0 Specifies AES Input Counter [127:96].

Crypto_AES_CNT_1
Address: Operational Base + offset (0x00dc)
AES Input Counter 1 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_CNT_1 Specifies AES Input Counter [95:64].

Crypto_AES_CNT_2
Address: Operational Base + offset (0x00e0)
AES Input Counter 2 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_CNT_2 Specifies AES Input Counter[63:32]

Crypto_AES_CNT_3
Address: Operational Base + offset (0x00e4)
AES Input Counter 3 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_CNT_3 Specifies AES Input Counter [31:0]

Crypto_TDES_CTRL
Address: Operational Base + offset (0x00100)
TDES Control Register

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved

Bit	Attr	Reset Value	Description
8	RW	0x0	TDES_ByteSwap_Key 0 = Disables Key byte swap 1 = Enables Key byte swap
7	RW	0x0	TDES_ByteSwap_IV 0 = Disables Initial value byte swap 1 = Enables Initial value byte swap
6	RW	0x0	TDES_ByteSwap_DO 0 = Disables Output data byte swap 1 = Enables Output data byte swap
5	RW	0x0	TDES_ByteSwap_DI 0 = Disables Input data byte swap 1 = Enables Input data byte swap
4	RW	0x0	TDES_ChainMode Specifies TDES chain mode selection 0 : ECB mode 1 : CBC mode
3	RW	0x0	TDES_EEE Specifies the TDES key mode selection 1'b0 : EDE 1'b1 : EEE
2	RW	0x0	TDES_Select Specify DES or TDES cipher 1'b0 : DES 1'b1 : TDES
1	RW	0x0	TDES_FifoMode Specify TDES Fifo Mode 1'b0: Slave mode 1'b1: Fifo mode
0	RW	0x0	TDES_Enc Specifies the Encryption/ Decryption mode selection signal 0 : Encryption 1 : Decryption

Crypto_TDES_STS

Address: Operational Base + offset (0x00104)

Status Register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	TDES_DONE When DES/TDES finishes, it will be HIGH, And it will not be LOW until it restart . 1: done 0: not done

Crypto_TDES_DIN_0

Address: Operational Base + offset (0x00108)
TDES Input Data 0 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TDES_DIN_0 Specifies TDES Input data [63:32].

Crypto_TDES_DIN_1
Address: Operational Base + offset (0x0010c)
TDES Input Data 1 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TDES_DIN_1 Specifies TDES Input data [31:0].

Crypto_TDES_DOUT_0
Address: Operational Base + offset (0x00110)
TDES Output Data 0 Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TDES_DOUT_0 Specifies TDES Output data [63:32].

Crypto_TDES_DOUT_1
Address: Operational Base + offset (0x00114)
TDES Output Data 1 Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TDES_DOUT_1 Specifies TDES Output data [31:0].

Crypto_TDES_IV_0
Address: Operational Base + offset (0x00118)
TDES IV data 0 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TDES_IV_0 Specifies TDES Initialization vector [63:32]

Crypto_TDES_IV_1
Address: Operational Base + offset (0x0011c)
TDES IV data 1 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TDES_IV_1 Specifies TDES Initialization vector [31:0]

Crypto_TDES_KEY1_0
Address: Operational Base + offset (0x00120)
TDES Key1 data 1 Register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TDES_KEY1_0 Specifies TDES key1 data [63:32]

Crypto_TDES_KEY1_1
Address: Operational Base + offset (0x00124)
TDES Key1 data 1 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TDES_KEY1_1 Specifies TDES key1 data [31:0]

Crypto_TDES_KEY2_0
Address: Operational Base + offset (0x00128)
TDES Key2 data 0 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TDES_KEY2_0 Specifies TDES key2 data [63:32]

Crypto_TDES_KEY2_1
Address: Operational Base + offset (0x0012c)
TDES Key2 data 1 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TDES_KEY_1 Specifies TDES key data [31:0]

Crypto_TDES_KEY3_0
Address: Operational Base + offset (0x00130)
TDES Key3 data 0 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TDES_KEY3_0 Specifies TDES key3 data [63:32]

Crypto_TDES_KEY3_1
Address: Operational Base + offset (0x00134)
TDES Key3 data 1 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_KEY3_1 Specifies TDES key3 data [31:0]

Crypto_HASH_CTRL
Address: Operational Base + offset (0x00180)
Hash Control Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3	RW	0x0	HASH_SWAP_DO Specifies the Byte swap of data output (hash result) 0 = Does not swap (default) 1 = Swap
2	RW	0x0	reserved
1:0	RW	0x0	Engine_Selection 2'b00: SHA1_HASH 2'b01: MD5_HASH 2'b10: SHA256_HASH 2'b11: PRNG

Crypto_HASH_STS
Address: Operational Base + offset (0x00184)
Hash Status Register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	HASH_DONE Hash Done Signal When HASH finishes, it will be HIGH, And it will not be LOW until it restart 1'b1 : done 1'b0 : not done

Crypto_HASH_MSG_LEN
Address: Operational Base + offset (0x00188)
Hash Message Len

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Msg_size Hash total byte.

Crypto_HASH_DOUT_0
Address: Operational Base + offset (0x0018c)
Hash Result Register 0

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	HASH_RESULT_0 Specifies the HASH Result [159:128]

Crypto_HASH_DOUT_1
Address: Operational Base + offset (0x00190)
Hash Result Register 1

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	HASH_RESULT_1 Specifies the HASH Result [127:96]

Crypto_HASH_DOUT_2
Address: Operational Base + offset (0x00194)
Hash Result Register 2

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	HASH_RESULT_2 Specifies the HASH Result [95:64]

Crypto_HASH_DOUT_3
Address: Operational Base + offset (0x00198)
Hash Result Register 3

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	HASH_RESULT_3 Specifies the HASH Result [63:32]

Crypto_HASH_DOUT_4
Address: Operational Base + offset (0x0019c)
Hash Result Register 4

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	HASH_RESULT_4 Specifies the HASH Result [31:0]

Crypto_HASH_DOUT_5
Address: Operational Base + offset (0x001a0)
Hash Result Register 4

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	HASH_RESULT_5 Specifies the HASH Result [31:0]

Crypto_HASH_DOUT_6
Address: Operational Base + offset (0x001a4)
Hash Result Register 6

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	HASH_RESULT_6 Specifies the HASH Result [31:0]

Crypto_HASH_DOUT_7
Address: Operational Base + offset (0x001a8)
Hash Result Register 7

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	HASH_RESULT_7 Specifies the HASH Result [31:0]

Crypto_HASH_SEED_0
Address: Operational Base + offset (0x001ac)
PRNG Seed/HMAC Key Register 0

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HASH_SEED_0 Specifies PRNG Seed/HMAC Key buffer [159:128]

Crypto_HASH_SEED_1
Address: Operational Base + offset (0x001b0)
PRNG Seed/HMAC Key Register 1

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HASH_SEED_1 Specifies PRNG Seed/HMAC Key buffer [127:96]

Crypto_HASH_SEED_2
Address: Operational Base + offset (0x001b4)
PRNG Seed/HMAC Key Register 2

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HASH_SEED_2 Specifies PRNG Seed/HMAC Key buffer [95:64]

Crypto_HASH_SEED_3
Address: Operational Base + offset (0x001b8)
PRNG Seed/HMAC Key Register 3

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HASH_SEED_3 Specifies PRNG Seed/HMAC Key buffer [63:32]

Crypto_HASH_SEED_4
Address: Operational Base + offset (0x001bc)
PRNG Seed/HMAC Key Register 4

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HASH_SEED_4 Specifies PRNG Seed/HMAC Key buffer [31:0]

Crypto_TRNG_CTRL
Address: Operational Base + offset (0x00200)
crypto TRNG control

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	reserved
16	RW	0x0000	osc_enable osc_ring enable It controls the running of osc_ring. And it is independent of clock and flush signal. This mean that it can run even when clock is gating or flush is asserted as long as osc_enable is asserted. Before it is used to get TRNG result , please run osc_ring first to get enough entropy. 1'b1: Enable ; 1'b0: Disable ;

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	period sample period TRNG use clock_crypto to sample ring osc output, this parameter is specify how many cycles to generate 1 bit random data.

Crypto_TRNG_DOUT_0
Address: Operational Base + offset (0x00204)
TRNG output register0

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TRNG output

Crypto_TRNG_DOUT_1
Address: Operational Base + offset (0x00204)
TRNG output register1

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TRNG output

Crypto_TRNG_DOUT_2
Address: Operational Base + offset (0x00208)
TRNG output register2

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TRNG output

Crypto_TRNG_DOUT_3
Address: Operational Base + offset (0x00210)
TRNG output register3

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TRNG output

Crypto_TRNG_DOUT_4
Address: Operational Base + offset (0x00214)
TRNG output register4

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TRNG output

Crypto_TRNG_DOUT_5
Address: Operational Base + offset (0x00218)
TRNG output register5

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TRNG output

Crypto_TRNG_DOUT_6
Address: Operational Base + offset (0x0021c)
TRNG output register6

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TRNG output

Crypto_TRNG_DOUT_7
Address: Operational Base + offset (0x00220)
TRNG output register7

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TRNG output

Crypto_PKA_CTRL
Address: Operational Base + offset (0x00280)
PKA Control Register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1:0	RW	0x0	block_size PKA Size It specifies the bits of N in PKA calculation. 2'b00: 512 bit 2'b01: 1024 bit 2'b10: 2048 bit

Crypto_AES_TKEY_0
Address: Operational Base + offset (0x0300)
AES Tweak Key data 0 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_TKEY_0 Specifies AES-XTS tweak key data [255:224]

Crypto_AES_TKEY_1
Address: Operational Base + offset (0x0304)
AES Tweak Key data 1 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_TKEY_1 Specifies AES-XTS tweak key data [223:192]

Crypto_AES_TKEY_2
Address: Operational Base + offset (0x0308)
AES Tweak Key data 2 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_TKEY_2 Specifies AES-XTS tweak key data [191:160]

Crypto_AES_TKEY_3
Address: Operational Base + offset (0x030c)
AES Tweak Key data 3 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_TKEY_3 Specifies AES-XTS tweak key data [159:128]

Crypto_AES_TKEY_4
Address: Operational Base + offset (0x0310)
AES Tweak Key data 4 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_TKEY_4 Specifies AES-XTS tweak key data [127:96]

Crypto_AES_TKEY_5
Address: Operational Base + offset (0x0314)
AES Tweak Key data 5 Register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_TKEY_5 Specifies AES-XTS tweak key data [95:64]

Crypto_AES_TKEY_6
Address: Operational Base + offset (0x0318)
AES Tweak Key data 6 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_TKEY_6 Specifies AES-XTS tweak key data [63:32]

Crypto_AES_TKEY_7
Address: Operational Base + offset (0x031c)
AES Tweak Key data 7 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_TKEY_7 Specifies AES-XTS tweak key data [31:0]

Crypto_AES_TWK_0
Address: Operational Base + offset (0x0320)
AES Tweak data 0 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_TWK_0 Specifies AES-XTS tweak date[127:96]

Crypto_AES_TWK_1
Address: Operational Base + offset (0x0324)
AES Tweak data 1 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_TWK_1 Specifies AES-XTS tweak date[95:64]

Crypto_AES_TWK_2
Address: Operational Base + offset (0x0328)
AES Tweak data 2 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_TWK_2 Specifies AES-XTS tweak date[63:32]

Crypto_AES_TWK_3
Address: Operational Base + offset (0x032c)
AES Tweak data 3 Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	AES_TWK_3 Specifies AES-XTS tweak date[31:0]

Crypto_KEY_SECURE
Address: Operational Base + offset (0x0330)
Key secure register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	KEY_SECURE 0 = AES key ,tkey and DES key are non-secure 1 = AES key ,tkey and DES key are secure

Crypto_CLK_GATE
Address: Operational Base + offset (0x0334)
Clock Gate Control register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x1	AES_CLK_GATE 0= AES clock is gated 1= AES clock is not gated
2	RW	0x1	HASH_CLK_GATE 0= HASH clock is gated 1= HASH clock is not gated
1	RW	0x1	TDES_CLK_GATE 0= TDES clock is gated 1= TDES clock is not gated
0	RW	0x1	RSA_CLK_GATE 0= RSA clock is gated 1= RSA clock is not gated

Crypto_CRYPTO_VER
Address: Operational Base + offset (0x03f0)
Key secure register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000300	CRYPTO_VER Crypto version

Crypto_PKA_M
Address: Operational Base + offset (0x0400)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	m PKA input or output data. PKA result = (M ^ E) mod N. When it finishes, the result data is in M position. Start from PKA_M base address, and may contain 512/1024/2048 bits data.

Crypto_PKA_C
Address: Operational Base + offset (0x0500)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	c PKA pre-calculate data, C = 2 ^(2n+2) mod N

Crypto_PKA_N
Address: Operational Base + offset (0x0600)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	n PKA modular

Crypto_PKA_E
Address: Operational Base + offset (0x0700)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	e PKA exponent.

10.4 Application Note

10.4.1 Reset a port

CRU.resetn_crypto_req is used to do a soft reset to crypto . Please refer to "Chapter CRU" for more details.

10.4.2 Overall Performance

Use CRU.crypto_div_con to select crypto frequency: F_{crypto} = F_{aclk} / (div + 1).
Make sure F_{crypto}donot exceed 200M.
The performance of crypto FIFO mode is list below.

Table 10-1 Crypto Performance Description

algorithm	cycle	block size	frequency	throughput rate
DES	17	64 bit	200M	<=752 M bps
TDES	51	64 bit	200M	<=250 M bps
AES	11/13/15	128 bit	200M	<=2320/1968/1706Mbps
SHA-1	81	512 bit	200M	<=1264 Mbps
MD5	65	512 bit	200M	<=1574 Mbps

10.4.3 Usage

1. Symmetric algorithm
DES/3DES, AES are symmetric algorithms. There are two ways of using these algorithms: Slave mode and FIFO mode, AES_XTS only support FIFO mode.
In Slave mode, you can calculate 1 block size of data by starting the engine. Take AES-128 for example, you should

- Program Input 128 bit Data to AES_DIN_0~AES_DIN_3
- Program Input 128 bit Key to AES_KEY_0~AES_KEY_3
- Program control mode to AES_CTRL to run in different mode
- Program CTRL.AES_START to run
- wait AES_STS.DONE High
- Read AES_DOUT_0 ~ AES_DOUT_3 to get result.

In FIFO mode,

- Program the source address to BRDMAS, the destination address to BTDMAS, program the length in word unit to BRDMAL;
- Program Input 128 bit Key to AES_KEY_0~AES_KEY_3;
- Program control mode to AES_CTRL to run in different mode;

- Program INTENA to enable interrupt;
- Program CTRL.BLOCK_START to start;
- wait interrupt asserted;
- Program INTSTS to clear interrupt status;
- Read the destination address which BTDMA points to.

FIFO mode get much higher throughput rate.

2. HASH

HASH is used to get digest of data. Only support FIFO mode.
There are three source: (1) hr_fifo; (2) br_fifo; (3) bt_fifo.
Take hr_fifo for example
Program CTRL.HASH_FLUSH 1'b1 to clear, wait several cycle (>= 10 cycles) , and Program CTRL.HASH_FLUSH 1'b0
Program data source address to HRDMAS, program 1 time data length in word unit to HRDMAL, program total length in byte unit to HASH_MSG_LEN
Program HASH_CTRL to choose algorithm, for example SHA-256
Program INTENA to enable interrupt;
Program CTRL.HASH_START 1'b1 to start;
Wait interrupt asserted; Only if HRDMAL length meets can this interrupt be asserted
If you have another section of data to hash, then go to (2), HASH_MSG_LEN need not to be programmed;
else go to (8)
waitHASH_STS.done asserted. Only if Hash_MSG_LEN meet can this bit status register asserted.
Read HASH_DOUT_0 – HASH_DOUT_7 to get result.

3. Asymmetric Algorithm

Support 512/1024/2048 bit RSA calculation. It provide the big number calculation. Result = ME mod N
Program CTRL.PKA_FLUSH 1'b1 to flush RSA module;
Wait CTRL.PKA_FLUSH to be LOW. It is self-cleared;
Program input_data(M) to PKA_M; Program pre_caculated C to PKA_C; Program Key(N) to PKA_N; Program Key(E) to PKA_E. C = 2 (2n+2) mod N. n is the required bit of N. For example 2048 bit N, n = 2048;
Program PKA_CTRL to select RSA size: 512/1024/2048
Program INTENA to enable interrupt;
Program CTRL.PKA_START to start;
Wait interrupt asserted.
Read PKA_M to get results.