Rockchip
RK3562
Technical Reference Manual
(Part 1)

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Revision History

Date	Revision	Description
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Chapter 1 System Overview

1.1 Address Mapping

RK3562 boot from internal BootRom, which supports remap function by software programming. Remap is controlled by PMU_SGRF_SOC_CON1[7:6]. When remap is set to 2'b01, the BootRom is un-accessible and PMU_SRAM is mapped to address 0xFFFF0000. When remap is set to 2'b10, the BootRom is un-accessible and SYSTEM_SRAM is mapped to address 0xFFFF0000.

Table 1-1 Address Mapping

Module	Start Address	Size	Module	Start Address	Size
PCIe2x1_S	FC000000	32MB	CAN1	FF610000	64KB
PCIe2x1_DBI	FE000000	4MB	GPIO1	FF620000	64KB
NPU_CBUF(256K)	FE400000	512KB	GPIO2	FF630000	64KB
SYSTEM_SRAM(64K)	FE480000	64KB	SPI1	FF640000	64KB
PMU_MEM(8K)	FE490000	8KB	SPI2	FF650000	64KB
Reserved	FE492000	220KB	Reserved	FF660000	64KB
Reserved	FE4C9000	220KB	UART1	FF670000	64KB
USB30OTG	FE500000	4MB	UART2	FF680000	64KB
GIC400	FE900000	32KB	UART3	FF690000	64KB
Reserved	FE908000	3.96875MB	UART4	FF6A0000	64KB
USB20HOST	FED00000	512KB	UART5	FF6B0000	64KB
DAPLITE	FED80000	512KB	UART6	FF6C0000	64KB
Reserved	FEE00000	1MB	UART7	FF6D0000	64KB
FIREWALL_DDR	FEF00000	64KB	UART8	FF6E0000	64KB
Reserved	FEF10000	0.9375MB	UART9	FF6F0000	64KB
PMU_SGRF	FF000000	64KB	PWM1	FF700000	64KB
PMU_GRF	FF010000	64KB	PWM2	FF710000	64KB
SYS_SGRF	FF020000	64KB	PWM3	FF720000	64KB
SYS_GRF	FF030000	64KB	SARADC0	FF730000	64KB
PERI_GRF	FF040000	64KB	U2PHY	FF740000	64KB
DDR_GRF	FF050000	64KB	PIPEPHY	FF750000	64KB
GPIO1_IOC/GPIO2_IOC	FF060000	64KB	Reserved	FF760000	0.625MB
GPIO3_IOC/GPIO4_IOC	FF070000	64KB	SAI0	FF800000	64KB
GPIO0_IOC	FF080000	64KB	SAI1	FF810000	64KB
USBPHY_GRF	FF090000	32KB	SAI2	FF820000	64KB
PIPEPHY_GRF	FF098000	32KB	PDM	FF830000	64KB
Reserved	FF0A0000	384KB	SPDIF_8CH	FF840000	64KB
CRU	FF100000	64KB	RK_DSM	FF850000	64KB
PMU0CRU	FF110000	32KB	SFC	FF860000	64KB
PMU1CRU	FF118000	32KB	EMMC	FF870000	64KB
DDRCRU	FF120000	64KB	SDMMC0	FF880000	64KB
PERICRU	FF130000	64KB	SDMMC1	FF890000	64KB
Reserved	FF140000	0.75MB	CRYPTO_NS	FF8A0000	32KB
I2C0	FF200000	64KB	CRYPTO_S	FF8A8000	32KB
UART0	FF210000	64KB	KEY_LAD	FF8B0000	64KB
SPI0	FF220000	64KB	RK_RNG_S	FF8C0000	64KB
PWM0	FF230000	64KB	TRNG_S	FF8D0000	64KB

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Module	Start Address	Size	Module	Start Address	Size
PVTM_PMU	FF240000	64KB	RK_RNG_NS	FF8E0000	64KB
PMU	FF250000	64KB	TRNG_NS	FF8F0000	64KB
GPIO0	FF260000	64KB	WDT_S	FF900000	64KB
HPTIMER	FF270000	64KB	KEY_READER	FF910000	64KB
DDR_SCRAMBLE_KEY	FF280000	64KB	OTP_S	FF920000	64KB
MAILBOX_PMU	FF290000	64KB	OTP_NS	FF930000	64KB
WDT_PMU	FF2A0000	64KB	OTPPHY	FF940000	64KB
Reserved	FF2B0000	320KB	Reserved	FF950000	192KB
RKNN	FF300000	64KB	DMAC_S	FF980000	64KB
Reserved	FF310000	64KB	DMAC_NS	FF990000	64KB
MALIG52	FF320000	128KB	RKDMA	FF9A0000	64KB
RKVDEC	FF340000	128KB	Reserved	FF9B0000	192KB
RKVENC	FF360000	128KB	SPINLOCK	FF9E0000	64KB
CSI_RX_CTRL0	FF380000	64KB	RK_CACHE	FF9F0000	64KB
CSI_RX_CTRL1	FF390000	64KB	I2C1	FFA00000	64KB
CSI_RX_CTRL2	FF3A0000	64KB	I2C2	FFA10000	64KB
CSI_RX_CTRL3	FF3B0000	64KB	I2C3	FFA20000	64KB
CSI_RX_PHY0	FF3C0000	64KB	I2C4	FFA30000	64KB
CSI_RX_PHY1	FF3D0000	64KB	I2C5	FFA40000	64KB
VICAP	FF3E0000	64KB	TIMER_NS	FFA50000	64KB
ISP	FF3F0000	64KB	WDT_NS	FFA60000	64KB
VOP	FF400000	64KB	TSADC	FFA70000	64KB
Reserved	FF410000	192KB	GMAC	FFA80000	64KB
RGA	FF440000	64KB	STIMER	FFA90000	64KB
JPEG_DEC	FF450000	64KB	SARADC1	FFAA0000	64KB
Reserved	FF460000	384KB	HASH	FFAB0000	64KB
DFIMON	FF4C0000	32KB	GPIO3	FFAC0000	64KB
DMA2DDR	FF4C8000	32KB	GPIO4	FFAD0000	64KB
DFICTRL	FF4D0000	32KB	MAILBOX_SYS	FFAE0000	64KB
HWLP	FF4D8000	32KB	SYSMCU_INTC	FFAF0000	64KB
UPCTL2	FF4E0000	64KB	DCF	FFB00000	64KB
DDRPHY	FF4F0000	64KB	DSI_TX	FFB10000	64KB
PCIE20_SLV	FF500000	64KB	DSI_TX_PHY	FFB20000	64KB
Reserved	FF510000	0.9375MB	MAC100	FFB30000	64KB
CAN0	FF600000	64KB	PCIe2x1_S	300000000	1024MB

The following table shows the boot address when before remap and after remap.

Table 1-2 Address Remapping

remap[1:0]=2'b00		remap[1:0]=2'b01		remap[1:0]=2'b10	
		not accessible	BootRom(36KB)	not accessible	BootRom(36KB)
0xFFFF0000	BootRom(36KB)	0xFFFF0000	PMU_SRAM(8KB)	0xFFFF0000	SYSTEM_SRAM (64KB)
0XFE490000	PMU_SRAM(8KB)	0XFE490000	PMU_SRAM(8KB)	0XFE490000	PMU_SRAM(8KB)

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0XFE480000	SYSTEM_SRAM (64KB)	0XFE480000	SYSTEM_SRAM (64KB)	0XFE480000	SYSTEM_SRAM (64KB)

1.2 System Boot

RK3562 provides system boot from off-chip devices such as SDMMC card, eMMC memory, serial Nand or Norflash. When boot code is not ready in these devices, also provide system code download into them by USB OTG interface. All of the boot code will be stored in internal BootRom. The following is the whole boot procedure for boot code, which will be stored in BootRom in advance.

The following features are supported.

- Support system boot from the following device:
  - Serial Nor Flash, 1bit or 4bits data width(device layout in FSPI IO)
  - Serial Nand Flash, 1bit data width(device layout in FSPI IO)
  - eMMC Interface, 8bits data width
  - SDMMC Card, 4bits data width
- Support system code download by USB OTG

The following figure shows RK3562 boot procedure flow.

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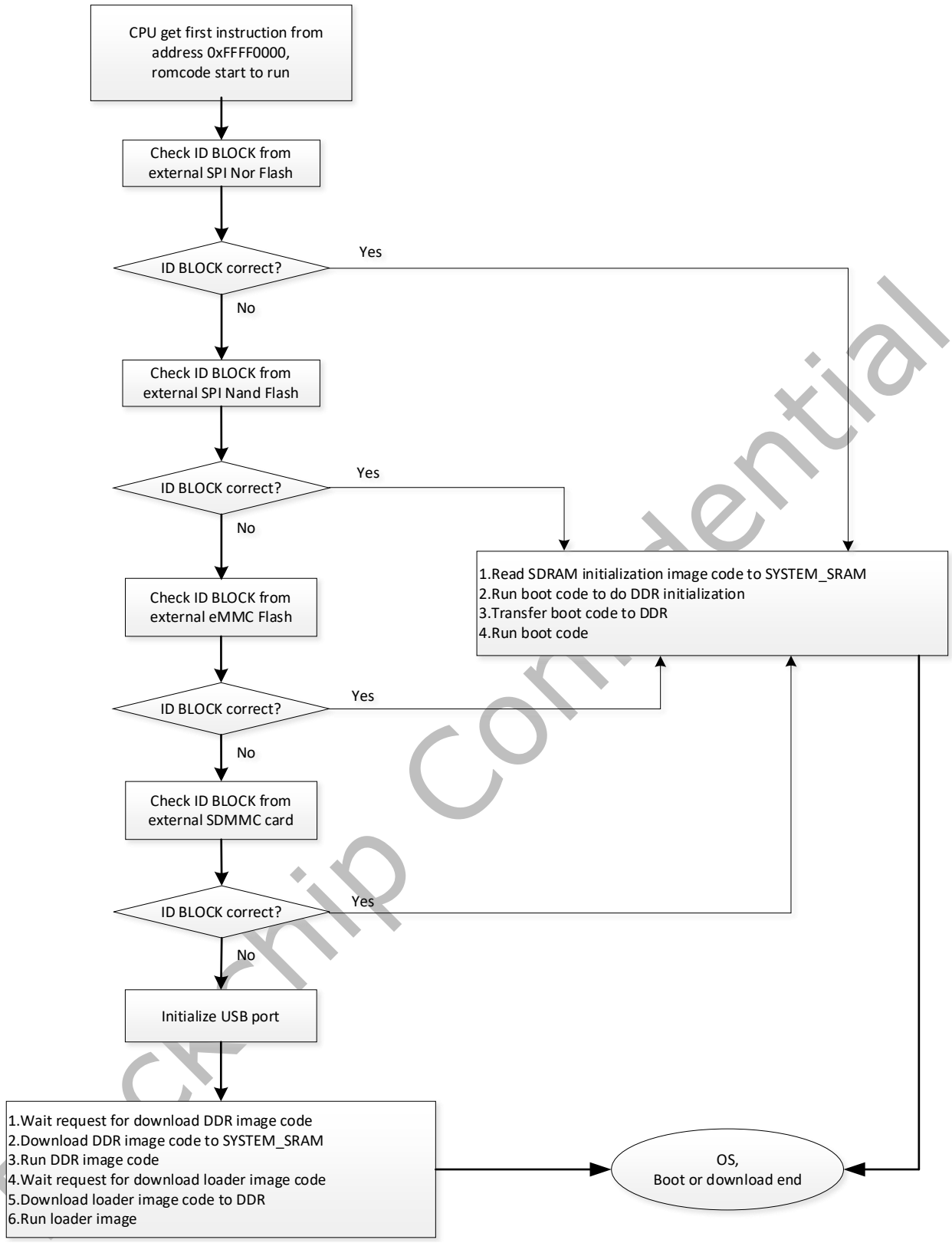


Fig.1-1 RK3562 Boot Procedure Flow

1.3 System Interrupt Connection

RK3562 provides an general interrupt controller (GIC) for CPU, which has 256 SPI (shared peripheral interrupts) interrupt sources and 3 PPI(Private peripheral interrupt) interrupt source and separately generates one nIRQ and one nFIQ to CPU. The triggered type for each interrupt is high level sensitive, not programmable. The detailed interrupt sources connection is in the following table.

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Table 1-3 RK3562 Interrupt Connection List

Number	Source	Polarity	Number	Source	Polarity
0-31 PPI		Low level	141	irq_derate_temp_limit_fault	High level
32	irq_gpio0_pmu	High level	142	irq_dmac0_abort	High level
33	irq_gpio0_exp_pmu	High level	143	|irq_dmac0	High level
34	irq_gpio1	High level	144	irq_rkdma	High level
35	irq_gpio1_exp	High level	145	|irq_rkdma_ch	High level
36	irq_gpio2	High level	146	|irq_mailbox_ap	High level
37	irq_gpio2_exp	High level	147	|irq_mailbox_bb	High level
38	irq_gpio3	High level	148	irq_crypto	High level
39	irq_gpio3_exp	High level	149	irq_klad	High level
40	irq_gpio4	High level	150	irq_dcf	High level
41	irq_gpio4_exp	High level	151	irq_rknn	High level
42	Reserved	High level	152	irq_jpeg_dec_mmu	High level
43	Reserved	High level	153	irq_jpeg_dec	High level
44	irq_i2c0_pmu	High level	154	irq_rkvdec_m_dec	High level
45	irq_i2c1	High level	155	irq_rkvdec_m_mmu	High level
46	irq_i2c2	High level	156	irq_saradc1	High level
47	irq_i2c3	High level	157	irq_tsadc	High level
48	irq_i2c4	High level	158	irq_rga	High level
49	irq_i2c5	High level	159	irq_spdif_8ch	High level
50	irq_mailbox_pmu1_ap	High level	160	irq_sfc	High level
51	irq_mailbox_pmu1_bb	High level	161	irq_pdm	High level
52	irq_pwm_pmu	High level	162	Reserved	High level
53	irq_pwr_pwm_pmu	High level	163	Reserved	High level
54	irq_pwm1	High level	164	irq_mipi_dsi	High level
55	irq_pwm1_pwr	High level	165	irq_vop_lb	High level
56	irq_pwm2	High level	166	irq_vop_ddr	High level
57	irq_pwm2_pwr	High level	167	irq_vop	High level
58	irq_pwm3	High level	168	irq_rkvenc	High level
59	irq_pwm3_pwr	High level	169	irq_rkvenc_mmu	High level
60	irq_csirx3_1	High level	170	Reserved	High level
61	irq_csirx3_2	High level	171	irq_key_reader	High level
62	irq_uart0_pmu	High level	172	irq_pvtm_pmu	High level
63	irq_uart1	High level	173	irq_pcie_err	High level
64	irq_uart2	High level	174	irq_pcie_msg_rx	High level
65	irq_uart3	High level	175	irq_pcie_legacy	High level
66	irq_uart4	High level	176	irq_pcie_sys	High level
67	irq_uart5	High level	177	irq_pcie_pmc	High level
68	irq_uart6	High level	178	irq_pcie_msi_ctrl	High level
69	irq_uart7	High level	179	Reserved	High level
70	irq_uart8	High level	180	irq_lfps_beacon	High level
71	irq_uart9	High level	181	irq_usb3otg	High level
72	irq_saradc0	High level	182	irq_usb2host_ehci	High level
73	irq_dma2ddr	High level	183	irq_usb2host_ohci	High level

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Number	Source	Polarity	Number	Source	Polarity
74	irq_pmu0hptimer	High level	184	irq_usb2host_arb	High level
75	irq_stimer0	High level	185	irq_usbphy_otg_bvalid	High level
76	irq_stimer1	High level	186	irq_usbphy_otg_id	High level
77	irq_timer0	High level	187	irq_usbphy_otg_linestate	High level
78	irq_timer1	High level	188	irq_usbphy_host_linestate	High level
79	irq_timer2	High level	189	irq_usbphy_host_disconnect	High level
80	irq_timer3	High level	190	irq_usbphy_otg_disconnect	High level
81	irq_timer4	High level	191	irq_pcie_msi_ctrl_vec[0]	High level
82	irq_timer5	High level	192	irq_pcie_msi_ctrl_vec[1]	High level
83	irq_wdtns_pmu	High level	193	irq_pcie_msi_ctrl_vec[2]	High level
84	irq_spi0	High level	194	irq_pcie_msi_ctrl_vec[3]	High level
85	irq_spi1	High level	195	irq_pcie_msi_ctrl_vec[4]	High level
86	irq_spi2	High level	196	irq_pcie_msi_ctrl_vec[5]	High level
87	irq_cache	High level	197	irq_pcie_msi_ctrl_vec[6]	High level
88	irq_sdmmc0	High level	198	irq_pcie_msi_ctrl_vec[7]	High level
89	irq_sdmmc1	High level	199	Reserved	High level
90	Reserved	High level	200	Reserved	High level
91	irq_sdmmc0_detectn_grf	High level	201	Reserved	High level
92	irq_sdmmc1_detectn_grf	High level	202	Reserved	High level
93	Reserved	High level	203	Reserved	High level
94	irq_sdmmc0_dectn_in_flt_grf	High level	204	Reserved	High level
95	irq_emmc	High level	205	Reserved	High level
96	irq_can0	High level	206	Reserved	High level
97	irq_can1	High level	207	Reserved	High level
98	Reserved	High level	208	Reserved	High level
99	irq_mac100	High level	209	Reserved	High level
100	irq_mac100_pmt	High level	210	Reserved	High level
101	irq_gmac_lpi	High level	211	Reserved	High level
102	irq_gmac_pmt	High level	212	Reserved	High level
103	irq_gmac_sbd_perch_rx	High level	213	Reserved	High level
104	irq_gmac_sbd_perch_tx	High level	214	Reserved	High level
105	irq_gmac_sbd	High level	215	Reserved	High level
106	irq_gpu_event	High level	216	Reserved	High level
107	irq_gpu_gpu	High level	217	Reserved	High level
108	irq_gpu_job	High level	218	Reserved	High level
109	irq_gpu_mmu	High level	219	Reserved	High level
110	irq_sai0_8ch	High level	220	Reserved	High level
111	irq_sai1_8ch	High level	221	Reserved	High level
112	irq_sai2_2ch	High level	222	Reserved	High level
113	irq_crypto_s	High level	223	Reserved	High level
114	irq_csirx0_1	High level	224	Reserved	High level
115	irq_csirx0_2	High level	225	Reserved	High level
116	irq_csirx1_1	High level	259:226	Reserved	High level

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Number	Source	Polarity	Number	Source	Polarity
117	irq_csirx1_2	High level	260	ca53_pmuirq[0]	High level
118	irq_csirx2_1	High level	261	ca53_pmuirq[1]	High level
119	irq_csirx2_2	High level	262	ca53_pmuirq[2]	High level
120	irq_isp_mipi	High level	263	ca53_pmuirq[3]	High level
121	irq_isp_mi	High level	264	nvcpumntirq[0]	High level
122	irq_isp	High level	265	nvcpumntirq[1]	High level
123	irq_isp_mmu0	High level	266	nvcpumntirq[2]	High level
124	irq_rk_rng_s	High level	267	nvcpumntirq[3]	High level
125	irq_rk_rng_ns	High level	268	ncommirq[0]	High level
126	irq_trng_s	High level	269	ncommirq[1]	High level
127	irq_trng_ns	High level	270	ncommirq[2]	High level
128	irq_otp_s	High level	271	ncommirq[3]	High level
129	irq_ot_ns	High level	272	nexterrirq	High level
130	irq_otp_mask	High level	273		High level
131	irq_vicap	High level	274		High level
132	irq_vicap_mmu	High level	275		High level
133	irq_wdt_s	High level	276		High level
134	irq_wdtns	High level	277		High level
135	irq_ddrmon	High level	278		High level
136	irq_msch_alarm	High level	279		High level
137	irq_upctl_alert_err	High level	280		High level
138	irq_upctl_arpoison	High level	281		High level
139	irq_upctl_awpoison	High level	282		High level
140	irq_derate_temp_limit	High level			

1.4 System DMA Hardware Request Connection

RK3562 provides two DMA controller (DMAC) inside the system, the following table is the DMA hardware request list.

Table 1-4 RK3562 DMAC Hardware Request Connection List

DMAC0			DMAC1		
Req Number	Source	Polarity	Req Number	Source	Polarity
0	Uart0 rx	High level	0	Uart0 rx	High level
1	Uart1 rx	High level	1	Uart1 rx	High level
2	Uart2 rx	High level	2	Uart2 rx	High level
3	Uart3 rx	High level	3	Uart3 rx	High level
4	Uart4 rx	High level	4	Uart4 rx	High level
5	Uart5 rx(can1_rx)	High level	5	Uart5 rx	High level
6	Uart6 rx	High level	6	Uart6 rx	High level
7	Uart7 rx	High level	7	Uart7 rx	High level
8	Uart8 rx	High level	8	Uart8 rx	High level
9	Uart9 rx	High level	9	Uart9 rx	High level
10	uart1 tx	High level	10	uart1 tx	High level
11	uart5 tx(can1_tx)	High level	11	uart5 tx	High level
12	spi0_rx	High level	12	spi0_rx	High level

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DMAC0			DMAC1		
Req Number	**Source**	**Polarity**	**Req Number**	**Source**	**Polarity**
13	spi0_tx	High level	13	spi0_tx	High level
14	spi1_rx	High level	14	spi1_rx	High level
15	spi1_tx	High level	15	spi1_tx	High level
16	spi2_rx	High level	16	spi2_rx	High level
17	spi2_tx	High level	17	spi2_tx	High level
18	SAI0_rx	High level	18	SAI0_rx	High level
19	SAI0_tx	High level	19	SAI0_tx	High level
20	SAI1_rx	High level	20	SAI1_rx	High level
21	SAI1_tx	High level	21	SAI1_tx	High level
22	SAI2_rx	High level	22	SAI2_rx	High level
23	SAI2_tx	High level	23	SAI2_tx	High level
24	can0_rx	High level	24	can0_rx	High level
25	can0_tx	High level	25	can0_tx	High level
26	pwm0	High level	26	pwm0	High level
27	pwm1	High level	27	pwm1	High level
28	pwm2	High level	28	pwm2	High level
29	pwm3	High level	29	pwm3	High level
30	spdif	High level	30	spdif	High level
31	pdm	High level	31	pdm	High level
			32	can1_rx	High level
			33	can1_tx	High level
			34	uart0_tx	High level
			35	uart2_tx	High level
			36	uart3_tx	High level
			37	uart4_tx	High level
			38	uart6_tx	High level
			39	uart7_tx	High level
			40	uart8_tx	High level
			41	uart9_tx	High level

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Chapter 2 Clock & Reset Unit (CRU)

2.1 Overview

The CRU is an APB slave module that is designed for generating all of the internal and system clocks, resets in the chip. CRU generates system clocks from PLL output clock or external clock source, and generates system reset from external power-on-reset, watchdog timer reset or software reset or temperature sensor.
The CRU is located at several addresses.

- TOPCRU, used for general system, with base address 0xFF100000
- PMU0CRU, used for always on system, with base address 0xFF110000
- PMU1CRU, used for always on system, with base address 0xFF118000
- DDRCRU, used for general ddr system, with base address 0xFF120000
- SUBDDRCRU, used for clk1x ddr system, with base address 0xFF128000
- PERICRU, used for peripheral system, with base address 0xFF130000

The CRU supports the following features:

- Compliance with AMBA APB interface
- Embedded with 5 fractional PLLs and 1 integer PLLs
- Flexible selection of clock source
- Support dividing clock separately
- Support gating clock separately
- Support software reset each module separately.

2.2 Block Diagram

The CRU is comprised of:

- PLL
- Register configuration unit
- Clock generate unit
- Reset generate unit

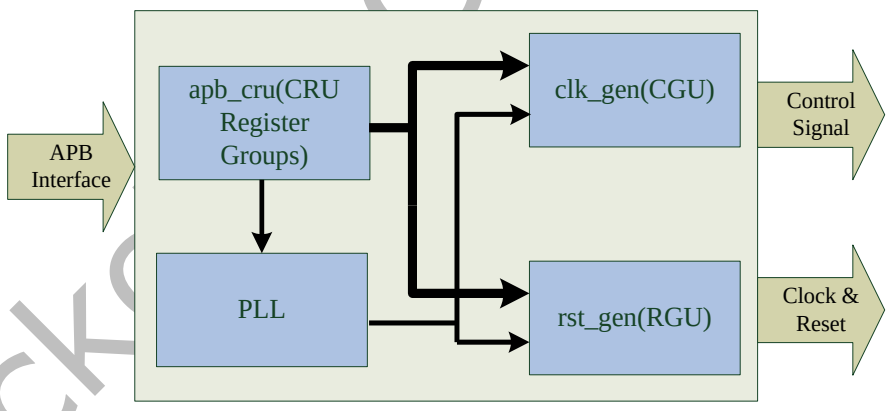


Fig.2-1 CRU Block Diagram

2.3 Function Description

2.3.1 System Clock Solution

There are 5 fractional PLLs in RK3562: CPLL, GPLL, HPLL, VPLL, DPLL. There are also 1 integer PLLs: APLL. Each PLL can only receive 24MHz oscillator as input reference clock and can be set to three work modes: normal mode, slow mode and deep slow mode. When power on or changing PLL setting, we must program PLL into slow mode or deep slow mode.
To maximize the flexibility, some of clocks can select divider source from multiple PLLs. To provide some specific frequency, another solution is integrated: fractional divider. Divfree50 divider are also provided for some modules. All clocks can be gated by software.
The basic units for clock generation are:

- Gating

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- MUX(multiplexer)
- Divfree(Glitch free divider)
  - clk_out_freq=clk_in_freq/divisor
  - When divisor is even, the clock duty cycle of clk_out is 50%
  - When divisor is odd, the clock duty cycle of clk_out is not 50%
- Fracdiv(Fractional divider)
  - clk_out_freq=clk_in_freq*numerator/denominator, both numerator and denominator are 16 bits
- Divfree50(Glitch free divider for duty cycle 50%)
  - clk_out_freq=clk_in_freq/divisor
  - When divisor is even or odd, the clock duty cycle of clk_out is 50%

The settings of all basic units are controlled by CRU registers

2.3.2 System Reset Solution

Almost all modules have these reset source as the following figure shows. The 'xxx' in the figure is the module name.

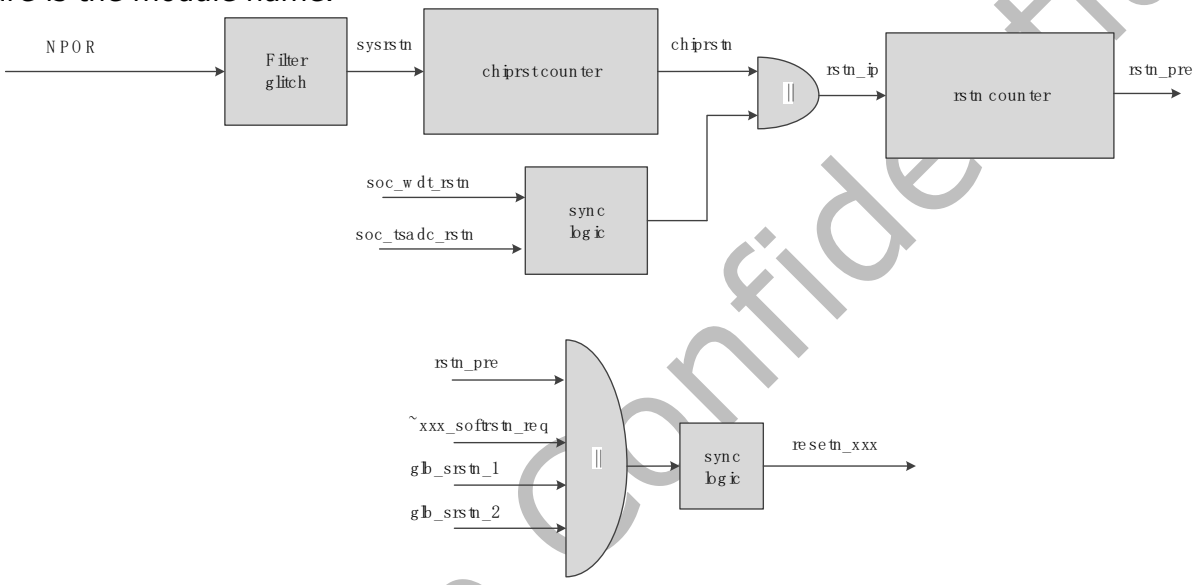


Fig.2-2 Reset Architecture Diagram

Reset source of each reset signal includes:

- NPOR: External power on reset
- soc_wdt_rstn: Reset from WDT module
- soc_tsadc_rstn:Reset from TSADCmodule
- softrstn_req:Software resetrequest by programming CRU_SOFTRST_CON
- glb_srstn_1: First global softwarereset by programming CRU_GLB_SRST_FST as 0xfdb9
- glb_srstn_2: Second global software reset by programming CRU_GLB_SRST_SND as 0xeca8

2.3.3 Fractional PLL Introduction

The fractional PLLs inside RK3562 output clock's frequency up to 3.8GHz. The PLL is a general purpose, high-performance PLL-based clock generator. The PLL is a multi-function, general purpose frequency synthesizer. Ultra-wide input and output ranges along with best-in-class jitter performance allow the PLL to be used for almost any clocking application. With excellent supply noise immunity, the PLL is ideal for use in noisy mixed signal SoC environments.

The PLL supports the following features:

- Input frequency range:1MHz to 1200MHz for integer mode and 10 MHz to 1200 MHz for fractional mode
- PFD minimum reference frequency range: 1MHz for integer mode and 10MHz for fractional mode
- Output frequency range: 19 MHz to 3.8GHz
- VCO output frequency range: 950MHz to 3.8GHz
- 24bit fractional accuracy, and fractional mode jitter performance to nearly match integer mode performance.

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- 4:1 VCO frequency range allows PLL to be optimized for minimum jitter or minimum power.
- Isolated analog supply(1.8V) allows for excellent supply rejection in noisy SoC applications
- Lock detect signal indicates when frequency lock has been achieved

PLL block diagram is shown below.

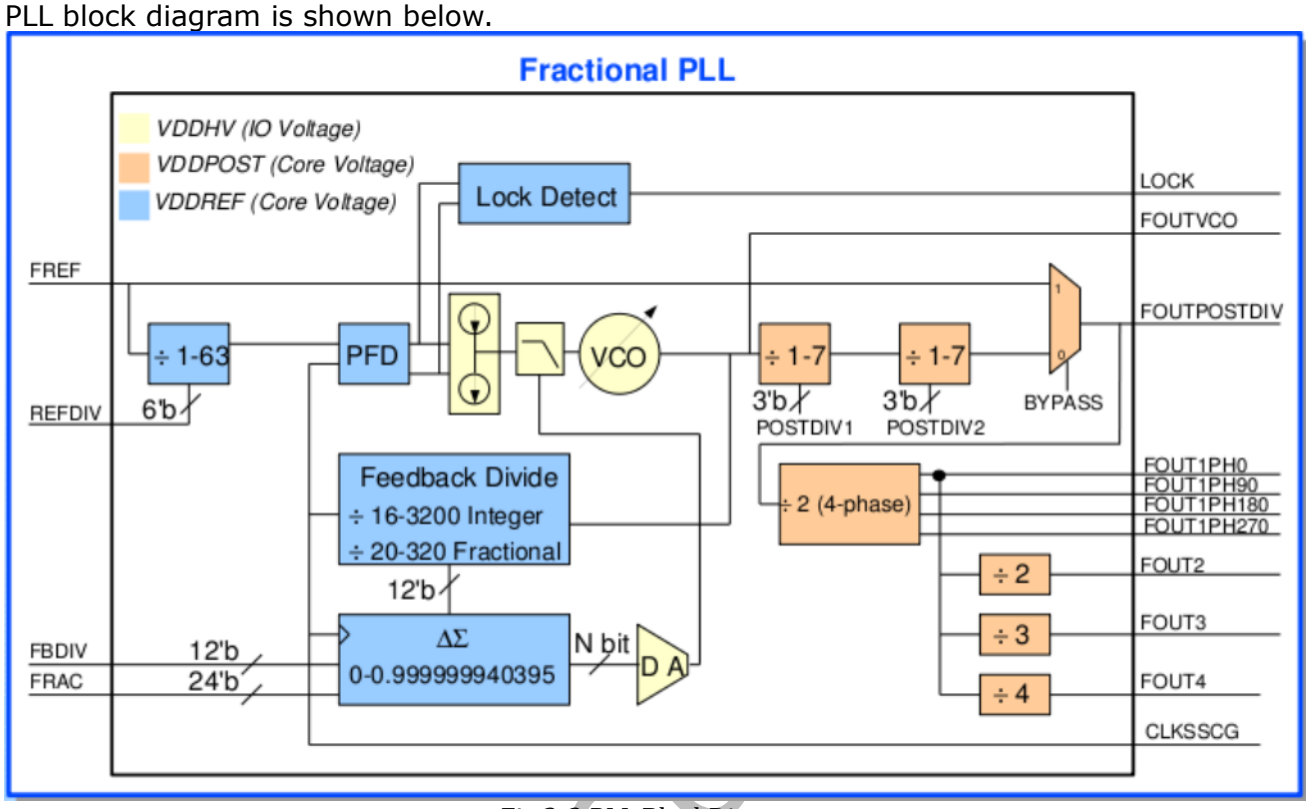


Fig.2-3 PLL BlockDiagram

2.3.4 Integer PLL Introduction

The integer PLLs inside RK3562 output clock's frequency up to 1.9GHz. The PLL is a multi-function, general purpose frequency synthesizer optimized for low power digital clocking. Wide input and output ranges along with best-in-class jitter performance allow the PLL to be used for a variety of different application. With excellent supply noise immunity, the PLL is ideal for use in noisy SoC environments.

The PLL supports the following features:

- Input frequency range:10MHz to 800MHz
- PFD minimum reference frequency range: 10MHz
- Output frequency range:9 MHz to 1.9GHz
- VCO output frequency range:475 MHz to1.9 GHz
- 4:1 VCO frequency range allows PLL to be optimized form inimum jitter or minimum power
- Low period jitter provides maximum timing margin in high frequency designs
- Lock detect signal indicates when frequency lock has been achieved

PLL block diagram is shown below.

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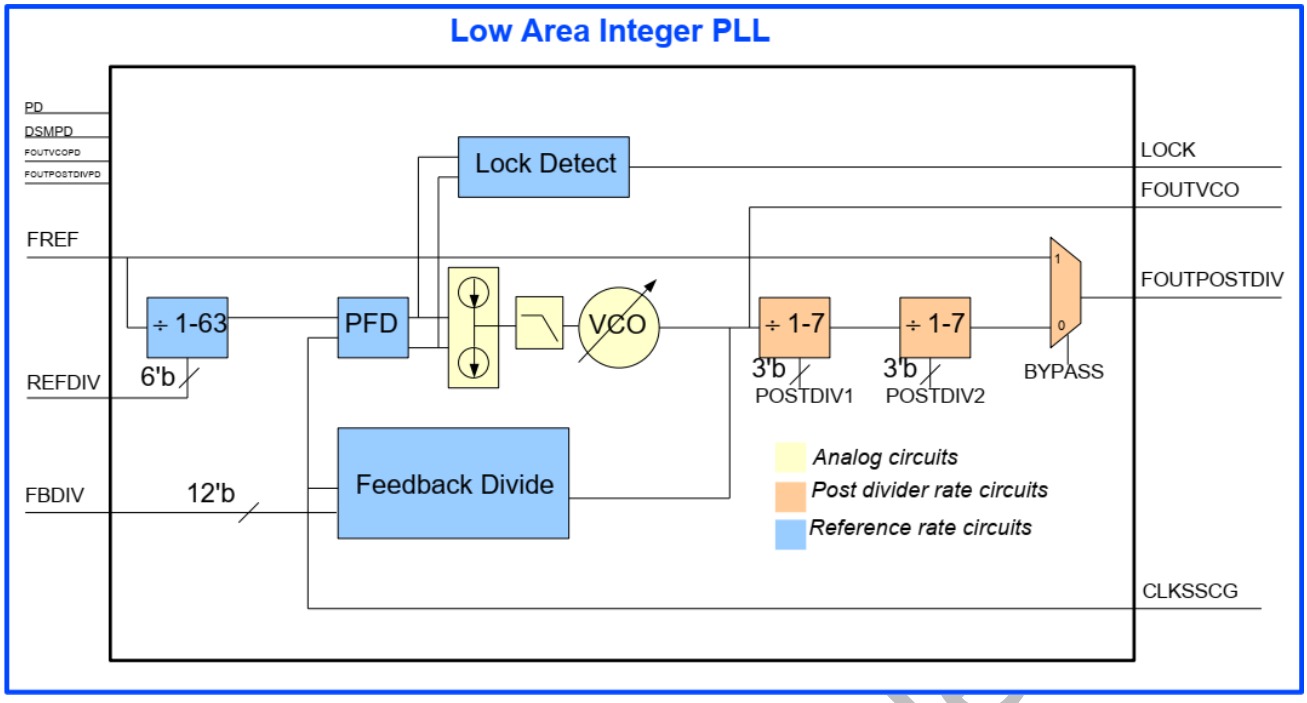


Fig.2-4 Integer PLL Block Diagram

2.4 TOPCRU Register Description

2.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
TOPCRU_APLL_CON0	0x0000	W	0x00001064	APLL configuration register0
TOPCRU_APLL_CON1	0x0004	W	0x00001042	APLL configuration register1
TOPCRU_APLL_CON2	0x0008	W	0x00000000	APLL configuration register2
TOPCRU_GPLL_CON0	0x0060	W	0x00002063	GPLL configuration register0
TOPCRU_GPLL_CON1	0x0064	W	0x00001041	GPLL configuration register1
TOPCRU_GPLL_CON2	0x0068	W	0x00000000	GPLL configuration register2
TOPCRU_GPLL_CON3	0x006C	W	0x00000007	GPLL configuration register3
TOPCRU_GPLL_CON4	0x0070	W	0x00007F00	GPLL configuration register4
TOPCRU_VPLL_CON0	0x0080	W	0x0000307D	VPLL configuration register0
TOPCRU_VPLL_CON1	0x0084	W	0x00001041	VPLL configuration register1
TOPCRU_VPLL_CON2	0x0088	W	0x00000000	VPLL configuration register2
TOPCRU_VPLL_CON3	0x008C	W	0x00000007	VPLL configuration register3
TOPCRU_VPLL_CON4	0x0090	W	0x00007F00	VPLL configuration register4
TOPCRU_HPLL_CON0	0x00A0	W	0x0000107D	HPLL configuration register0
TOPCRU_HPLL_CON1	0x00A4	W	0x00001043	HPLL configuration register1
TOPCRU_HPLL_CON2	0x00A8	W	0x00000000	HPLL configuration register2
TOPCRU_HPLL_CON3	0x00AC	W	0x00000007	HPLL configuration register3
TOPCRU_HPLL_CON4	0x00B0	W	0x00007F00	HPLL configuration register4
TOPCRU_CLKSEL_CON00	0x0100	W	0x00008993	Internal clock select and division register 0
TOPCRU_CLKSEL_CON01	0x0104	W	0x00000087	Internal clock select and division register 1
TOPCRU_CLKSEL_CON02	0x0108	W	0x00000005	Internal clock select and division register 2
TOPCRU_CLKSEL_CON03	0x010C	W	0x00000003	Internal clock select and division register 3
TOPCRU_CLKSEL_CON04	0x0110	W	0x0000000F	Internal clock select and division register 4

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Name	Offset	Size	Reset Value	Description
TOPCRU_CLKSEL_CON05	0x0114	W	0x00000101	Internal clock select and division register 5
TOPCRU_CLKSEL_CON06	0x0118	W	0x00000128	Internal clock select and division register 6
TOPCRU_CLKSEL_CON08	0x0120	W	0x00008080	Internal clock select and division register 8
TOPCRU_CLKSEL_CON09	0x0124	W	0x00008080	Internal clock select and division register 9
TOPCRU_CLKSEL_CON10	0x0128	W	0x00000000	Internal clock select and division register 10
TOPCRU_CLKSEL_CON11	0x012C	W	0x00000101	Internal clock select and division register 11
TOPCRU_CLKSEL_CON12	0x0130	W	0x00000707	Internal clock select and division register 12
TOPCRU_CLKSEL_CON13	0x0134	W	0x00000005	Internal clock select and division register 13
TOPCRU_CLKSEL_CON14	0x0138	W	0x00000000	Internal clock select and division register 14
TOPCRU_CLKSEL_CON15	0x013C	W	0x00000001	Internal clock select and division register 15
TOPCRU_CLKSEL_CON16	0x0140	W	0x00000003	Internal clock select and division register 16
TOPCRU_CLKSEL_CON17	0x0144	W	0x00000000	Internal clock select and division register 17
TOPCRU_CLKSEL_CON18	0x0148	W	0x00000081	Internal clock select and division register 18
TOPCRU_CLKSEL_CON19	0x014C	W	0x00000000	Internal clock select and division register 19
TOPCRU_CLKSEL_CON20	0x0150	W	0x00000303	Internal clock select and division register 20
TOPCRU_CLKSEL_CON21	0x0154	W	0x00000001	Internal clock select and division register 21
TOPCRU_CLKSEL_CON22	0x0158	W	0x00000005	Internal clock select and division register 22
TOPCRU_CLKSEL_CON23	0x015C	W	0x00000200	Internal clock select and division register 23
TOPCRU_CLKSEL_CON24	0x0160	W	0x00000001	Internal clock select and division register 24
TOPCRU_CLKSEL_CON25	0x0164	W	0x00000041	Internal clock select and division register 25
TOPCRU_CLKSEL_CON26	0x0168	W	0x00000401	Internal clock select and division register 26
TOPCRU_CLKSEL_CON27	0x016C	W	0x00004241	Internal clock select and division register 27
TOPCRU_CLKSEL_CON28	0x0170	W	0x00000002	Internal clock select and division register 28
TOPCRU_CLKSEL_CON29	0x0174	W	0x00000001	Internal clock select and division register 29
TOPCRU_CLKSEL_CON30	0x0178	W	0x00008003	Internal clock select and division register 30
TOPCRU_CLKSEL_CON31	0x017C	W	0x00008003	Internal clock select and division register 31
TOPCRU_CLKSEL_CON32	0x0180	W	0x00000102	Internal clock select and division register 32

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Name	Offset	Size	Reset Value	Description
TOPCRU_CLKSEL_CON33	0x0184	W	0x00000002	Internal clock select and division register 33
TOPCRU_CLKSEL_CON36	0x0190	W	0x00000203	Internal clock select and division register 36
TOPCRU_CLKSEL_CON37	0x0194	W	0x00000000	Internal clock select and division register 37
TOPCRU_CLKSEL_CON40	0x01A0	W	0x00000505	Internal clock select and division register 40
TOPCRU_CLKSEL_CON41	0x01A4	W	0x0000000B	Internal clock select and division register 41
TOPCRU_CLKSEL_CON43	0x01AC	W	0x0000081F	Internal clock select and division register 43
TOPCRU_CLKSEL_CON44	0x01B0	W	0x00000001	Internal clock select and division register 44
TOPCRU_CLKSEL_CON45	0x01B4	W	0x00000000	Internal clock select and division register 45
TOPCRU_CLKSEL_CON46	0x01B8	W	0x000000A7	Internal clock select and division register 46
TOPCRU_CLKSEL_CON47	0x01BC	W	0x00000000	Internal clock select and division register 47
TOPCRU_GATE_CON00	0x0300	W	0x00008000	Internal clock gate and division register 0
TOPCRU_GATE_CON01	0x0304	W	0x00000000	Internal clock gate and division register 1
TOPCRU_GATE_CON04	0x0310	W	0x00004000	Internal clock gate and division register 4
TOPCRU_GATE_CON05	0x0314	W	0x00000000	Internal clock gate and division register 5
TOPCRU_GATE_CON06	0x0318	W	0x00000080	Internal clock gate and division register 6
TOPCRU_GATE_CON08	0x0320	W	0x00000040	Internal clock gate and division register 8
TOPCRU_GATE_CON09	0x0324	W	0x00000080	Internal clock gate and division register 9
TOPCRU_GATE_CON10	0x0328	W	0x00000200	Internal clock gate and division register 10
TOPCRU_GATE_CON11	0x032C	W	0x00000000	Internal clock gate and division register 11
TOPCRU_GATE_CON12	0x0330	W	0x00008000	Internal clock gate and division register 12
TOPCRU_GATE_CON13	0x0334	W	0x00008000	Internal clock gate and division register 13
TOPCRU_GATE_CON14	0x0338	W	0x00008000	Internal clock gate and division register 14
TOPCRU_GATE_CON16	0x0340	W	0x00000000	Internal clock gate and division register 16
TOPCRU_GATE_CON17	0x0344	W	0x00008000	Internal clock gate and division register 17
TOPCRU_GATE_CON18	0x0348	W	0x00000000	Internal clock gate and division register 18
TOPCRU_GATE_CON19	0x034C	W	0x00000000	Internal clock gate and division register 19
TOPCRU_GATE_CON20	0x0350	W	0x00000000	Internal clock gate and division register 20

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Name	Offset	Size	Reset Value	Description
TOPCRU_GATE_CON21	0x0354	W	0x00000000	Internal clock gate and division register 21
TOPCRU_GATE_CON22	0x0358	W	0x00000000	Internal clock gate and division register 22
TOPCRU_GATE_CON23	0x035C	W	0x00000000	Internal clock gate and division register 23
TOPCRU_GATE_CON24	0x0360	W	0x00000000	Internal clock gate and division register 24
TOPCRU_GATE_CON25	0x0364	W	0x00004000	Internal clock gate and division register 25
TOPCRU_GATE_CON26	0x0368	W	0x00000000	Internal clock gate and division register 26
TOPCRU_GATE_CON27	0x036C	W	0x00000000	Internal clock gate and division register 27
TOPCRU_SOFTRST_CON01	0x0404	W	0x00000000	Internal clock reset register 1
TOPCRU_SOFTRST_CON03	0x040C	W	0x00000000	Internal clock reset register 3
TOPCRU_SOFTRST_CON04	0x0410	W	0x00000000	Internal clock reset register 4
TOPCRU_SOFTRST_CON05	0x0414	W	0x00000000	Internal clock reset register 5
TOPCRU_SOFTRST_CON06	0x0418	W	0x00000000	Internal clock reset register 6
TOPCRU_SOFTRST_CON08	0x0420	W	0x00000000	Internal clock reset register 8
TOPCRU_SOFTRST_CON09	0x0424	W	0x00000000	Internal clock reset register 9
TOPCRU_SOFTRST_CON10	0x0428	W	0x00000000	Internal clock reset register 10
TOPCRU_SOFTRST_CON11	0x042C	W	0x00000000	Internal clock reset register 11
TOPCRU_SOFTRST_CON12	0x0430	W	0x00000000	Internal clock reset register 12
TOPCRU_SOFTRST_CON13	0x0434	W	0x00000000	Internal clock reset register 13
TOPCRU_SOFTRST_CON14	0x0438	W	0x00000000	Internal clock reset register 14
TOPCRU_SOFTRST_CON16	0x0440	W	0x00000100	Internal clock reset register 16
TOPCRU_SOFTRST_CON17	0x0444	W	0x00000000	Internal clock reset register 17
TOPCRU_SOFTRST_CON18	0x0448	W	0x00000000	Internal clock reset register 18
TOPCRU_SOFTRST_CON19	0x044C	W	0x00000000	Internal clock reset register 19
TOPCRU_SOFTRST_CON20	0x0450	W	0x00000000	Internal clock reset register 20
TOPCRU_SOFTRST_CON21	0x0454	W	0x00000000	Internal clock reset register 21
TOPCRU_SOFTRST_CON22	0x0458	W	0x00000000	Internal clock reset register 22
TOPCRU_SOFTRST_CON23	0x045C	W	0x00000008	Internal clock reset register 23

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Name	Offset	Size	Reset Value	Description
TOPCRU_SOFTRST_CON24	0x0460	W	0x00000000	Internal clock reset register 24
TOPCRU_SOFTRST_CON25	0x0464	W	0x00000000	Internal clock reset register 25
TOPCRU_SOFTRST_CON26	0x0468	W	0x00000000	Internal clock reset register 26
TOPCRU_SOFTRST_CON27	0x046C	W	0x00000000	Internal clock reset register 27
TOPCRU_SSGTBL0_3	0x0500	W	0x00000000	External wave table register0
TOPCRU_SSGTBL4_7	0x0504	W	0x00000000	External wave table register1
TOPCRU_SSGTBL8_11	0x0508	W	0x00000000	External wave table register2
TOPCRU_SSGTBL12_15	0x050C	W	0x00000000	External wave table register3
TOPCRU_SSGTBL16_19	0x0510	W	0x00000000	External wave table register4
TOPCRU_SSGTBL20_23	0x0514	W	0x00000000	External wave table register5
TOPCRU_SSGTBL24_27	0x0518	W	0x00000000	External wave table register6
TOPCRU_SSGTBL28_31	0x051C	W	0x00000000	External wave table register7
TOPCRU_SSGTBL32_35	0x0520	W	0x00000000	External wave table register8
TOPCRU_SSGTBL36_39	0x0524	W	0x00000000	External wave table register9
TOPCRU_SSGTBL40_43	0x0528	W	0x00000000	External wave table register10
TOPCRU_SSGTBL44_47	0x052C	W	0x00000000	External wave table register11
TOPCRU_SSGTBL48_51	0x0530	W	0x00000000	External wave table register12
TOPCRU_SSGTBL52_55	0x0534	W	0x00000000	External wave table register13
TOPCRU_SSGTBL56_59	0x0538	W	0x00000000	External wave table register14
TOPCRU_SSGTBL60_63	0x053C	W	0x00000000	External wave table register15
TOPCRU_SSGTBL64_67	0x0540	W	0x00000000	External wave table register16
TOPCRU_SSGTBL68_71	0x0544	W	0x00000000	External wave table register17
TOPCRU_SSGTBL72_75	0x0548	W	0x00000000	External wave table register18
TOPCRU_SSGTBL76_79	0x054C	W	0x00000000	External wave table register19
TOPCRU_SSGTBL80_83	0x0550	W	0x00000000	External wave table register20
TOPCRU_SSGTBL84_87	0x0554	W	0x00000000	External wave table register21
TOPCRU_SSGTBL88_91	0x0558	W	0x00000000	External wave table register22
TOPCRU_SSGTBL92_95	0x055C	W	0x00000000	External wave table register23
TOPCRU_SSGTBL96_99	0x0560	W	0x00000000	External wave table register24
TOPCRU_SSGTBL100_103	0x0564	W	0x00000000	External wave table register25
TOPCRU_SSGTBL104_107	0x0568	W	0x00000000	External wave table register26
TOPCRU_SSGTBL108_111	0x056C	W	0x00000000	External wave table register27
TOPCRU_SSGTBL112_115	0x0570	W	0x00000000	External wave table register28
TOPCRU_SSGTBL116_119	0x0574	W	0x00000000	External wave table register29
TOPCRU_SSGTBL120_123	0x0578	W	0x00000000	External wave table register30
TOPCRU_SSGTBL124_127	0x057C	W	0x00000000	External wave table register31
TOPCRU_MODE_CON00	0x0600	W	0x00000000	Internal clock select and division register 0
TOPCRU_GLB_CNT_TH	0x0610	W	0x00640064	GLB_CNT_TH
TOPCRU_GLB_SRST_FST	0x0614	W	0x00000000	GLB_SRST_FST
TOPCRU_GLB_SRST_SND	0x0618	W	0x00000000	GLB_SRST_SND
TOPCRU_GLB_RST_CON	0x061C	W	0x00000000	GLB_RST_CON
TOPCRU_GLB_RST_ST	0x0620	W	0x00000000	GLB_RST_ST
TOPCRU_SDMMC0_CON0	0x0624	W	0x00002004	SDMMC0 CRU Register
TOPCRU_SDMMC0_CON1	0x0628	W	0x00000000	SDMMC0 CRU Register
TOPCRU_SDMMC1_CON0	0x062C	W	0x00002004	SDMMC1 CRU Register
TOPCRU_SDMMC1_CON1	0x0630	W	0x00000000	SDMMC1 CRU Register
TOPCRU_EMMC_CON	0x063C	W	0x00000007	EMMC CRU Register
TOPCRU_CM0_GATEMASK	0x0680	W	0x00000007	CM0 CORE CRU Register

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Name	Offset	Size	Reset Value	Description
TOPCRU_MISC_CON0	0x0684	W	0x00000000	MISC CRU Register
TOPCRU_MISC_CON1	0x0688	W	0x00000000	MISC CRU Register
TOPCRU_MISC_CON2	0x068C	W	0x00000000	MISC CRU Register
TOPCRU_FREQ_CAL	0x0694	W	0x00000000	FREQ_CAL

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.4.2 Detail Registers Description

TOPCRU_APLL_CON0

Address: Operational Base(0xFF100000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	bypass PLL Bypass. FREF bypasses PLL to FOUTPOSTDIV 1'b0: No bypass 1'b1: Bypass
14:12	RW	0x1	postdiv1 First Post Divide Value, (1-7)
11:0	RW	0x064	fbdiv Feedback Divide Value, valid divider settings are: [16, 2500] in integer mode [20, 500] in fractional mode Tips: No plus one operation

TOPCRU_APLL_CON1

Address: Operational Base(0xFF100000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pllpdsel PLL global power down source selection If pllpdsel == 1, PLL can be power down only by pllpd1, otherwise pll is power down when any one of refdiv/fbdiv/fracdiv is changed or pllpd0 is asserted
14	RW	0x0	pllpd1 PLL global power down request 1'b0: No power down 1'b1: Power down
13	RW	0x0	pllpd0 PLL global power down request 1'b0: No power down 1'b1: Power down
12	RW	0x1	dsmpd PLL delta sigma modulator enable 1'b0: Modulator is enable 1'b1: Modulator is disabled
11	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
10	RW	0x0	pll_lock PLL lock status 1'b0: Unlock 1'b1: Lock
9	RO	0x0	reserved
8:6	RW	0x1	postdiv2 Second Post Divide Value, (1-7)
5:0	RW	0x02	refdiv Reference Clock Divide Value, (1-63)

TOPCRU_APLL_CON2

Address: Operational Base(0xFF100000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	fout4phasepd Power down 4-phase clocks and 2X, 3X, 4X clocks 1'b0: No power down 1'b1: Power down
26	RW	0x0	foutvcopd Power down buffered VCO clock 1'b0: No power down 1'b1: Power down
25	RW	0x0	foutpostdivpd Power down all outputs except for buffered VCO clock 1'b0: No power down 1'b1: Power down
24:0	RO	0x0000000	reserved

TOPCRU_GPLL_CON0

Address: Operational Base(0xFF100000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	bypass PLL Bypass. FREF bypasses PLL to FOUTPOSTDIV 1'b0: No bypass 1'b1: Bypass
14:12	RW	0x2	postdiv1 First Post Divide Value, (1-7)
11:0	RW	0x063	fbdiv Feedback Divide Value, valid divider settings are: [16, 2500] in integer mode [20, 500] in fractional mode Tips: No plus one operation

TOPCRU_GPLL_CON1

Address: Operational Base(0xFF100000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15	RW	0x0	pllpdsel PLL global power down source selection If pllpdsel == 1, PLL can be power down only by pllpd1, otherwise pll is power down when any one of refdiv/fbdiv/fracdiv is changed or pllpd0 is asserted
14	RW	0x0	pllpd1 PLL global power down request 1'b0: No power down 1'b1: Power down
13	RW	0x0	pllpd0 PLL global power down request 1'b0: No power down 1'b1: Power down
12	RW	0x1	dsmpd PLL delta sigma modulator enable 1'b0: Modulator is enable 1'b1: Modulator is disabled
11	RO	0x0	reserved
10	RW	0x0	pll_lock PLL lock status 1'b0: Unlock 1'b1: Lock
9	RO	0x0	reserved
8:6	RW	0x1	postdiv2 Second Post Divide Value, (1-7)
5:0	RW	0x01	refdiv Reference Clock Divide Value, (1-63)

TOPCRU_GPLL_CON2

Address: Operational Base(0xFF100000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	fout4phasepd Power down 4-phase clocks and 2X, 3X, 4X clocks 1'b0: No power down 1'b1: Power down
26	RW	0x0	foutvcopd Power down buffered VCO clock 1'b0: No power down 1'b1: Power down
25	RW	0x0	foutpostdivpd Power down all outputs except for buffered VCO clock 1'b0: No power down 1'b1: Power down
24	RW	0x0	dacpd Power down quantization noise cancellation DAC 1'b0: No power down 1'b1: Power down
23:0	RW	0x000000	fracdiv Fractional part of feedback divide (fraction = FRAC/2^24)

TOPCRU_GPLL_CON3

Address: Operational Base(0xFF100000) + offset (0x006C)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x00	ssmod_spread spread amplitude % = 0.1 * SPREAD[4: 0]
7:4	RW	0x0	ssmod_divval Divider required to set the modulation frequency
3	RW	0x0	ssmod_downspread Selects center spread or downs pread 1'b0: Down spread 1'b1: Center spread
2	RW	0x1	ssmod_reset Reset modulator state 1'b0: No reset 1'b1: Reset
1	RW	0x1	ssmod_disable_sscg Bypass SSMOD by module 1'b0: No bypass 1'b1: Bypass
0	RW	0x1	ssmod_bp Bypass SSMOD by integration 1'b0: No bypass 1'b1: Bypass

TOPCRU_GPLL_CON4

Address: Operational Base(0xFF100000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x7f	ssmod_ext_maxaddr External wave table data inputs (0-255)
7:1	RO	0x00	reserved
0	RW	0x0	ssmod_sel_ext_wave select external wave 1'b0: No select ext_wave 1'b1: Select ext_wave

TOPCRU_VPLL_CON0

Address: Operational Base(0xFF100000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	bypass PLL Bypass. FREF bypasses PLL to FOUTPOSTDIV 1'b0: No bypass 1'b1: Bypass

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Bit	Attr	Reset Value	Description
14:12	RW	0x3	postdiv1 First Post Divide Value, (1-7)
11:0	RW	0x07d	fbdiv Feedback Divide Value, valid divider settings are: [16, 2500] in integer mode [20, 500] in fractional mode Tips: No plus one operation

TOPCRU_VPLL_CON1

Address: Operational Base(0xFF100000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pllpdsel PLL global power down source selection If pllpdsel == 1, PLL can be power down only by pllpd1, otherwise pll is power down when any one of refdiv/fbdiv/fracdiv is changed or pllpd0 is asserted
14	RW	0x0	pllpd1 PLL global power down request 1'b0: No power down 1'b1: Power down
13	RW	0x0	pllpd0 PLL global power down request 1'b0: No power down 1'b1: Power down
12	RW	0x1	dsmpd PLL delta sigma modulator enable 1'b0: Modulator is enable 1'b1: Modulator is disabled
11	RO	0x0	reserved
10	RW	0x0	pll_lock PLL lock status 1'b0: Unlock 1'b1: Lock
9	RO	0x0	reserved
8:6	RW	0x1	postdiv2 Second Post Divide Value, (1-7)
5:0	RW	0x01	refdiv Reference Clock Divide Value, (1-63)

TOPCRU_VPLL_CON2

Address: Operational Base(0xFF100000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	fout4phasepd Power down 4-phase clocks and 2X, 3X, 4X clocks 1'b0: No power down 1'b1: Power down
26	RW	0x0	foutvcopd Power down buffered VCO clock 1'b0: No power down 1'b1: Power down

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Bit	Attr	Reset Value	Description
25	RW	0x0	foutpostdivpd Power down all outputs except for buffered VCO clock 1'b0: No power down 1'b1: Power down
24	RW	0x0	dacpd Power down quantization noise cancellation DAC 1'b0: No power down 1'b1: Power down
23:0	RW	0x000000	fracdiv Fractional part of feedback divide (fraction = FRAC/2^24)

TOPCRU_VPLL_CON3

Address: Operational Base(0xFF100000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x00	ssmod_spread spread amplitude % = 0.1 * SPREAD[4: 0]
7:4	RW	0x0	ssmod_divval Divider required to set the modulation frequency
3	RW	0x0	ssmod_downspread Selects center spread or downs pread 1'b0: Down spread 1'b1: Center spread
2	RW	0x1	ssmod_reset Reset modulator state 1'b0: No reset 1'b1: Reset
1	RW	0x1	ssmod_disable_sscg Bypass SSMOD by module 1'b0: No bypass 1'b1: Bypass
0	RW	0x1	ssmod_bp Bypass SSMOD by integration 1'b0: No bypass 1'b1: Bypass

TOPCRU_VPLL_CON4

Address: Operational Base(0xFF100000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x7f	ssmod_ext_maxaddr External wave table data inputs (0-255)
7:1	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	ssmod_sel_ext_wave select external wave 1'b0: No select ext_wave 1'b1: Select ext_wave

TOPCRU_HPLL_CON0

Address: Operational Base(0xFF100000) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	bypass PLL Bypass. FREF bypasses PLL to FOUTPOSTDIV 1'b0: No bypass 1'b1: Bypass
14:12	RW	0x1	postdiv1 First Post Divide Value, (1-7)
11:0	RW	0x07d	fbdiv Feedback Divide Value, valid divider settings are: [16, 2500] in integer mode [20, 500] in fractional mode Tips: No plus one operation

TOPCRU_HPLL_CON1

Address: Operational Base(0xFF100000) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pllpdsel PLL global power down source selection If pllpdsel == 1, PLL can be power down only by pllpd1, otherwise pll is power down when any one of refdiv/fbdiv/fracdiv is changed or pllpd0 is asserted
14	RW	0x0	pllpd1 PLL global power down request 1'b0: No power down 1'b1: Power down
13	RW	0x0	pllpd0 PLL global power down request 1'b0: No power down 1'b1: Power down
12	RW	0x1	dsmpd PLL delta sigma modulator enable 1'b0: Modulator is enable 1'b1: Modulator is disabled
11	RO	0x0	reserved
10	RW	0x0	pll_lock PLL lock status 1'b0: Unlock 1'b1: Lock
9	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
8:6	RW	0x1	postdiv2 Second Post Divide Value, (1-7)
5:0	RW	0x03	refdiv Reference Clock Divide Value, (1-63)

TOPCRU_HPLL_CON2

Address: Operational Base(0xFF100000) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	fout4phasepd Power down 4-phase clocks and 2X, 3X, 4X clocks 1'b0: No power down 1'b1: Power down
26	RW	0x0	foutvcopd Power down buffered VCO clock 1'b0: No power down 1'b1: Power down
25	RW	0x0	foutpostdivpd Power down all outputs except for buffered VCO clock 1'b0: No power down 1'b1: Power down
24	RW	0x0	dacpd Power down quantization noise cancellation DAC 1'b0: No power down 1'b1: Power down
23:0	RW	0x000000	fracdiv Fractional part of feedback divide (fraction = FRAC/2^24)

TOPCRU_HPLL_CON3

Address: Operational Base(0xFF100000) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x00	ssmod_spread spread amplitude % = 0.1 * SPREAD[4: 0]
7:4	RW	0x0	ssmod_divval Divider required to set the modulation frequency
3	RW	0x0	ssmod_downspread Selects center spread or downs pread 1'b0: Down spread 1'b1: Center spread
2	RW	0x1	ssmod_reset Reset modulator state 1'b0: No reset 1'b1: Reset
1	RW	0x1	ssmod_disable_sscg Bypass SSMOD by module 1'b0: No bypass 1'b1: Bypass

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Bit	Attr	Reset Value	Description
0	RW	0x1	ssmod_bp Bypass SSMOD by integration 1'b0: No bypass 1'b1: Bypass

TOPCRU_HPLL_CON4

Address: Operational Base(0xFF100000) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x7f	ssmod_ext_maxaddr External wave table data inputs (0-255)
7:1	RO	0x00	reserved
0	RW	0x0	ssmod_sel_ext_wave select external wave 1'b0: No select ext_wave 1'b1: Select ext_wave

TOPCRU_CLKSEL_CON00

Address: Operational Base(0xFF100000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	clk_matrix_100m_src_sel clk_matrix_100m_src clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux_from_pmu1
14:12	RO	0x0	reserved
11:8	RW	0x9	clk_matrix_100m_src_div DT50 division register. Divide clk_matrix_100m_src by (div_con + 1).
7	RW	0x1	clk_matrix_50m_src_sel clk_matrix_50m_src clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux_from_pmu1
6:5	RO	0x0	reserved
4:0	RW	0x13	clk_matrix_50m_src_div DT50 division register. Divide clk_matrix_50m_src by (div_con + 1).

TOPCRU_CLKSEL_CON01

Address: Operational Base(0xFF100000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
7	RW	0x1	clk_matrix_125m_src_sel clk_matrix_125m_src clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux_from_pmu1
6:4	RO	0x0	reserved
3:0	RW	0x7	clk_matrix_125m_src_div DT50 division register. Divide clk_matrix_125m_src by (div_con + 1).

TOPCRU_CLKSEL_CON02

Address: Operational Base(0xFF100000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	clk_matrix_200m_src_sel clk_matrix_200m_src clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux_from_pmu1
6:4	RO	0x0	reserved
3:0	RW	0x5	clk_matrix_200m_src_div DT50 division register. Divide clk_matrix_200m_src by (div_con + 1).

TOPCRU_CLKSEL_CON03

Address: Operational Base(0xFF100000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	clk_matrix_300m_src_sel clk_matrix_300m_src clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux_from_pmu1
6:4	RO	0x0	reserved
3:0	RW	0x3	clk_matrix_300m_src_div DT50 division register. Divide clk_matrix_300m_src by (div_con + 1).

TOPCRU_CLKSEL_CON04

Address: Operational Base(0xFF100000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:8	RW	0x00	clk_testout_top_sel clk_testout_top clock mux. 5'b00000: xin_osc0_func 5'b00001: clk_testout_core 5'b00010: clk_testout_npu 5'b00011: clk_testout_gpu 5'b00100: clk_testout_vepu 5'b00101: clk_testout_vdpu 5'b00110: clk_testout_viphy 5'b00111: clk_testout_vo 5'b01000: clk_testout_rga 5'b01001: 1'b0 5'b01010: clk_testout_phpphy 5'b01011: clk_testout_bus 5'b01100: clk_testout_peri 5'b01101: clk_testout_subddr 5'b01110: clk_testout_pmu1 5'b01111: clk_apll 5'b10000: clk_gpll 5'b10001: clk_vpll 5'b10010: clk_hpll 5'b10011: test_clk_pvtpll_logic 5'b10100: clk_24m_sscsrc 5'b10101: clk_deepslow 5'b10110: 1'b0 5'b10111: 1'b0 5'b11000: 1'b0 5'b11001: 1'b0 5'b11010: 1'b0 5'b11011: 1'b0 5'b11100: 1'b0 5'b11101: 1'b0 5'b11110: 1'b0 5'b11111: 1'b0
7:0	RW	0x0f	clk_testout_top_div Divide clk_testout_top by (div_con + 1).

TOPCRU_CLKSEL_CON05

Address: Operational Base(0xFF100000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	aclk_top_vio_biu_sel aclk_top_vio_biu clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux_from_pmu1
14:12	RO	0x0	reserved
11:8	RW	0x1	aclk_top_vio_biu_div Divide aclk_top_vio_biu by (div_con + 1).
7	RW	0x0	aclk_top_biu_sel aclk_top_biu clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux_from_pmu1
6:4	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
3:0	RW	0x1	aclk_top_biu_div Divide aclk_top_biu by (div_con + 1).

TOPCRU_CLKSEL_CON06

Address: Operational Base(0xFF100000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x1	clk_pvtpll_logic_o_sel clk_pvtpll_logic_o clock mux. 1'b0: clk_pvtpll_logic 1'b1: xin_osc0_func
7:6	RW	0x0	clk_24m_sscsrc_sel clk_24m_sscsrc clock mux. 2'b00: clk_vpll_mux 2'b01: clk_hpll_mux 2'b10: clk_gpll_mux 2'b11: clk_cpll_mux_from_pmu1
5:0	RW	0x28	clk_24m_sscsrc_div DT50 division register. Divide clk_24m_sscsrc by (div_con + 1).

TOPCRU_CLKSEL_CON08

Address: Operational Base(0xFF100000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	clk_cam1_out2io_sel clk_cam1_out2io clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux_from_pmu1 2'b10: xin_osc0_func 2'b11: clk_apll_mux
13:8	RW	0x00	clk_cam1_out2io_div Divide clk_cam1_out2io by (div_con + 1).
7:6	RW	0x2	clk_cam0_out2io_sel clk_cam0_out2io clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux_from_pmu1 2'b10: xin_osc0_func 2'b11: clk_apll_mux
5:0	RW	0x00	clk_cam0_out2io_div Divide clk_cam0_out2io by (div_con + 1).

TOPCRU_CLKSEL_CON09

Address: Operational Base(0xFF100000) + offset (0x0124)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	clk_cam3_out2io_sel clk_cam3_out2io clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux_from_pmu1 2'b10: xin_osc0_func 2'b11: clk_apll_mux
13:8	RW	0x00	clk_cam3_out2io_div Divide clk_cam3_out2io by (div_con + 1).
7:6	RW	0x2	clk_cam2_out2io_sel clk_cam2_out2io clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux_from_pmu1 2'b10: xin_osc0_func 2'b11: clk_apll_mux
5:0	RW	0x00	clk_cam2_out2io_div Divide clk_cam2_out2io by (div_con + 1).

TOPCRU_CLKSEL_CON10

Address: Operational Base(0xFF100000) + offset (0x0128)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_core_i_sel clk_core_i clock mux. 1'b0: clk_core_pre 1'b1: clk_core_pvtpll_src
14	RW	0x0	clk_core_pre_ndft_sel clk_core_pre_ndft clock mux. 1'b0: i_clk_core_pre 1'b1: clk_apll_g(this is for high freq value)
13:9	RO	0x00	reserved
8	RW	0x0	clk_core_pvtpll_src_sel clk_core_pvtpll_src clock mux. 1'b0: clk_deepslow 1'b1: clk_core_pvtpll
7	RW	0x0	clk_core_lev1pre_sel clk_core_lev1pre clock mux. 1'b0: clk_apll_mux 1'b1: clk_gpll_mux
6:5	RO	0x0	reserved
4:0	RW	0x00	clk_core_lev1pre_div Divide clk_core_lev1pre by (div_con + 1).

TOPCRU_CLKSEL_CON11

Address: Operational Base(0xFF100000) + offset (0x012C)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:8	RW	0x1	clk_scanhs_aclkm_core_div Divide clk_scanhs_aclkm_core by (div_con + 1).
7:3	RO	0x00	reserved
2:0	RW	0x1	aclk_core_pre_div Divide aclk_core_pre by (div_con + 1).

TOPCRU_CLKSEL_CON12

Address: Operational Base(0xFF100000) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:8	RW	0x7	clk_scanhs_pclk_dbg_div Divide clk_scanhs_pclk_dbg by (div_con + 1).
7:4	RO	0x0	reserved
3:0	RW	0x7	pclk_dbg_pre_div Divide pclk_dbg_pre by (div_con + 1).

TOPCRU_CLKSEL_CON13

Address: Operational Base(0xFF100000) + offset (0x0134)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5:0	RW	0x05	hclk_core_biu_div Divide hclk_core_biu by (div_con + 1).

TOPCRU_CLKSEL_CON14

Address: Operational Base(0xFF100000) + offset (0x0138)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_testout_core_sel clk_testout_core clock mux. 1'b0: test_clk_pvtpll_core 1'b1: clk_core
14:11	RO	0x0	reserved
10:8	RW	0x0	clk_testout_core_div Divide clk_testout_core by (div_con + 1).
7:0	RO	0x00	reserved

TOPCRU_CLKSEL_CON15

Address: Operational Base(0xFF100000) + offset (0x013C)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_npu_i_sel clk_npu_i clock mux. 1'b0: clk_npu_pre 1'b1: clk_npu_pvtpll_src
14:9	RO	0x00	reserved
8	RW	0x0	clk_npu_pvtpll_src_sel clk_npu_pvtpll_src clock mux. 1'b0: clk_deepslow 1'b1: clk_npu_pvtpll
7	RW	0x0	clk_npu_pre_sel clk_npu_pre clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux_from_pmu1
6:4	RO	0x0	reserved
3:0	RW	0x1	clk_npu_pre_div Divide clk_npu_pre by (div_con + 1).

TOPCRU_CLKSEL_CON16

Address: Operational Base(0xFF100000) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3:0	RW	0x3	hclk_npu_pre_div Divide hclk_npu_pre by (div_con + 1).

TOPCRU_CLKSEL_CON17

Address: Operational Base(0xFF100000) + offset (0x0144)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	clk_testout_npu_sel clk_testout_npu clock mux. 1'b0: test_clk_pvtpll_npu 1'b1: clk_npu
6:3	RO	0x0	reserved
2:0	RW	0x0	clk_testout_npu_div Divide clk_testout_npu by (div_con + 1).

TOPCRU_CLKSEL_CON18

Address: Operational Base(0xFF100000) + offset (0x0148)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15	RW	0x0	clk_gpu_i_sel clk_gpu_i clock mux. 1'b0: clk_gpu_pre 1'b1: clk_gpu_pvtpll_src
14:9	RO	0x00	reserved
8	RW	0x0	clk_gpu_pvtpll_src_sel clk_gpu_pvtpll_src clock mux. 1'b0: clk_deepslow 1'b1: clk_gpu_pvtpll
7	RW	0x1	clk_gpu_lev1pre_sel clk_gpu_lev1pre clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux_from_pmu1
6:4	RO	0x0	reserved
3:0	RW	0x1	clk_gpu_lev1pre_div Divide clk_gpu_lev1pre by (div_con + 1).

TOPCRU_CLKSEL_CON19

Address: Operational Base(0xFF100000) + offset (0x014C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_gpu_brg_biu_sel clk_gpu_brg_biu clock mux. 1'b0: clk_matrix_200m_src 1'b1: clk_matrix_100m_src
14:8	RO	0x00	reserved
7	RW	0x0	clk_testout_gpu_sel clk_testout_gpu clock mux. 1'b0: test_clk_pvtpll_gpu 1'b1: clk_gpu
6:4	RW	0x0	clk_testout_gpu_div Divide clk_testout_gpu by (div_con + 1).
3:0	RW	0x0	aclk_gpu_pre_div Divide aclk_gpu_pre by (div_con + 1).

TOPCRU_CLKSEL_CON20

Address: Operational Base(0xFF100000) + offset (0x0150)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	aclk_vepu_pre_sel aclk_vepu_pre clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux_from_pmu1 2'b10: clk_pvtpll_logic_o 2'b11: clk_apll_mux
13	RO	0x0	reserved
12:8	RW	0x03	aclk_vepu_pre_div Divide aclk_vepu_pre by (div_con + 1).

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Bit	Attr	Reset Value	Description
7:6	RW	0x0	clk_rkvenc_core_sel clk_rkvenc_core clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux_from_pmu1 2'b10: clk_pvtpll_logic_o 2'b11: clk_apll_mux
5	RO	0x0	reserved
4:0	RW	0x03	clk_rkvenc_core_div Divide clk_rkvenc_core by (div_con + 1).

TOPCRU_CLKSEL_CON21

Address: Operational Base(0xFF100000) + offset (0x0154)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_testout_vepu_sel clk_testout_vepu clock mux. 1'b0: clk_rkvenc_core 1'b1: aclk_vepu_pre
14:4	RO	0x000	reserved
3:0	RW	0x1	hclk_vepu_pre_div Divide hclk_vepu_pre by (div_con + 1).

TOPCRU_CLKSEL_CON22

Address: Operational Base(0xFF100000) + offset (0x0158)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:6	RW	0x0	aclk_vdpu_pre_sel aclk_vdpu_pre clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux_from_pmu1 2'b10: clk_pvtpll_logic_o 2'b11: clk_apll_mux
5	RO	0x0	reserved
4:0	RW	0x05	aclk_vdpu_pre_div Divide aclk_vdpu_pre by (div_con + 1).

TOPCRU_CLKSEL_CON23

Address: Operational Base(0xFF100000) + offset (0x015C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:14	RW	0x0	clk_rkvdec_hevc_ca_sel clk_rkvdec_hevc_ca clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux_from_pmu1 2'b10: clk_pvtpll_logic_o 2'b11: clk_apll_mux
13	RO	0x0	reserved
12:8	RW	0x02	clk_rkvdec_hevc_ca_div Divide clk_rkvdec_hevc_ca by (div_con + 1).
7:0	RO	0x00	reserved

TOPCRU_CLKSEL_CON24

Address: Operational Base(0xFF100000) + offset (0x0160)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_testout_vdpu_sel clk_testout_vdpu clock mux. 1'b0: clk_rkvdec_hevc_ca 1'b1: aclk_vdpu_pre
14:4	RO	0x000	reserved
3:0	RW	0x1	hclk_vdpu_pre_div Divide hclk_vdpu_pre by (div_con + 1).

TOPCRU_CLKSEL_CON25

Address: Operational Base(0xFF100000) + offset (0x0164)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:6	RW	0x1	aclk_vi_sel aclk_vi clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux_from_pmu1 2'b10: clk_pvtpll_logic_o 2'b11: clk_apll_mux
5:4	RO	0x0	reserved
3:0	RW	0x1	aclk_vi_div Divide aclk_vi by (div_con + 1).

TOPCRU_CLKSEL_CON26

Address: Operational Base(0xFF100000) + offset (0x0168)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:12	RW	0x0	clk_testout_viphy_sel clk_testout_viphy clock mux. 4'b0000: clk_isp 4'b0001: dclk_vicap 4'b0010: csirx0_clk_data 4'b0011: csirx1_clk_data 4'b0100: csirx2_clk_data 4'b0101: csirx3_clk_data 4'b0110: csiphy0_lanebyrxclk0 4'b0111: csiphy0_lanebyrxclk1 4'b1000: csiphy1_lanebyrxclk0 4'b1001: csiphy1_lanebyrxclk1
11:8	RW	0x4	pclk_vi_div Divide pclk_vi by (div_con + 1).
7:4	RO	0x0	reserved
3:0	RW	0x1	hclk_vi_div Divide hclk_vi by (div_con + 1).

TOPCRU_CLKSEL_CON27

Address: Operational Base(0xFF100000) + offset (0x016C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	dclk_vicap_sel dclk_vicap clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux_from_pmu1 2'b10: clk_pvtpll_logic_o 2'b11: clk_apll_mux
13:12	RO	0x0	reserved
11:8	RW	0x2	dclk_vicap_div Divide dclk_vicap by (div_con + 1).
7:6	RW	0x1	clk_isp_sel clk_isp clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux_from_pmu1 2'b10: clk_pvtpll_logic_o 2'b11: clk_apll_mux
5:4	RO	0x0	reserved
3:0	RW	0x1	clk_isp_div Divide clk_isp by (div_con + 1).

TOPCRU_CLKSEL_CON28

Address: Operational Base(0xFF100000) + offset (0x0170)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
7:6	RW	0x0	aclk_vo_pre_sel aclk_vo_pre clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux_from_pmu1 2'b10: clk_vpll_mux 2'b11: clk_hpll_mux
5	RO	0x0	reserved
4:0	RW	0x02	aclk_vo_pre_div Divide aclk_vo_pre by (div_con + 1).

TOPCRU_CLKSEL_CON29

Address: Operational Base(0xFF100000) + offset (0x0174)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4:0	RW	0x01	hclk_vo_pre_div Divide hclk_vo_pre by (div_con + 1).

TOPCRU_CLKSEL_CON30

Address: Operational Base(0xFF100000) + offset (0x0178)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	dclk_vop_sel dclk_vop clock mux. 2'b00: clk_gpll_mux 2'b01: clk_hpll_mux 2'b10: clk_vpll_mux 2'b11: clk_apll_mux
13:8	RO	0x00	reserved
7:0	RW	0x03	dclk_vop_div Divide dclk_vop by (div_con + 1).

TOPCRU_CLKSEL_CON31

Address: Operational Base(0xFF100000) + offset (0x017C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	dclk_vop1_sel dclk_vop1 clock mux. 2'b00: clk_gpll_mux 2'b01: clk_hpll_mux 2'b10: clk_vpll_mux 2'b11: clk_apll_mux
13:10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9:8	RW	0x0	clk_testout_vo_sel clk_testout_vo clock mux. 2'b00: aclk_vo_pre 2'b01: dclk_vop 2'b10: dclk_vop1
7:0	RW	0x03	dclk_vop1_div Divide dclk_vop1 by (div_con + 1).

TOPCRU_CLKSEL_CON32

Address: Operational Base(0xFF100000) + offset (0x0180)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:8	RW	0x1	hclk_rga_pre_div Divide hclk_rga_pre by (div_con + 1).
7:6	RW	0x0	aclk_rga_pre_sel aclk_rga_pre clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux_from_pmu1 2'b10: clk_pvtpll_logic_o 2'b11: clk_apll_mux
5:4	RO	0x0	reserved
3:0	RW	0x2	aclk_rga_pre_div Divide aclk_rga_pre by (div_con + 1).

TOPCRU_CLKSEL_CON33

Address: Operational Base(0xFF100000) + offset (0x0184)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_testout_rga_sel clk_testout_rga clock mux. 1'b0: aclk_rga_pre 1'b1: clk_rga_core
14:8	RO	0x00	reserved
7:6	RW	0x0	clk_rga_core_sel clk_rga_core clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux_from_pmu1 2'b10: clk_pvtpll_logic_o 2'b11: clk_apll_mux
5:4	RO	0x0	reserved
3:0	RW	0x2	clk_rga_core_div Divide clk_rga_core by (div_con + 1).

TOPCRU_CLKSEL_CON36

Address: Operational Base(0xFF100000) + offset (0x0190)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_usb3otg_suspend_sel clk_usb3otg_suspend clock mux. 1'b0: xin_osc0_func 1'b1: clk_deepslow
14:12	RO	0x0	reserved
11:8	RW	0x2	pclk_php_div Divide pclk_php by (div_con + 1).
7	RW	0x0	aclk_php_sel aclk_php clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux_from_pmu1
6:4	RO	0x0	reserved
3:0	RW	0x3	aclk_php_div Divide aclk_php by (div_con + 1).

TOPCRU_CLKSEL_CON37

Address: Operational Base(0xFF100000) + offset (0x0194)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:6	RW	0x0	clk_testout_phpphy_sel clk_testout_phpphy clock mux. 2'b00: aclk_php 2'b01: clk_pipephy_pipe 2'b10: clk_usbphy_usb3otg_utmi
5:0	RO	0x00	reserved

TOPCRU_CLKSEL_CON40

Address: Operational Base(0xFF100000) + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	hclk_bus_sel hclk_bus clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux_from_pmu1
14	RO	0x0	reserved
13:8	RW	0x05	hclk_bus_div Divide hclk_bus by (div_con + 1).
7	RW	0x0	aclk_bus_sel aclk_bus clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux_from_pmu1
6:5	RO	0x0	reserved
4:0	RW	0x05	aclk_bus_div Divide aclk_bus by (div_con + 1).

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TOPCRU_CLKSEL_CON41

Address: Operational Base(0xFF100000) + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	dclk_bus_gpio_sel dclk_bus_gpio clock mux. 1'b0: xin_osc0_func 1'b1: clk_deepslow
14:10	RO	0x00	reserved
9:8	RW	0x0	clk_i2c_sel clk_i2c clock mux. 2'b00: clk_matrix_200m_src 2'b01: clk_matrix_100m_src 2'b10: clk_matrix_50m_src 2'b11: xin_osc0_func
7	RW	0x0	pclk_bus_sel pclk_bus clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux_from_pmu1
6:5	RO	0x0	reserved
4:0	RW	0x0b	pclk_bus_div Divide pclk_bus by (div_con + 1).

TOPCRU_CLKSEL_CON43

Address: Operational Base(0xFF100000) + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RW	0x01	clk_tsadc_tsen_div Divide clk_tsadc_tsen by (div_con + 1).
10:0	RW	0x01f	clk_tsadc_div Divide clk_tsadc by (div_con + 1).

TOPCRU_CLKSEL_CON44

Address: Operational Base(0xFF100000) + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:0	RW	0x001	clk_saradc_to_vccio156_div Divide clk_saradc_to_vccio156 by (div_con + 1).

TOPCRU_CLKSEL_CON45

Address: Operational Base(0xFF100000) + offset (0x01B4)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	clk_gmac_125m_cru_i_sel clk_gmac_125m_cru_i clock mux. 1'b0: clk_matrix_125m_src 1'b1: xin_osc0_func
7	RW	0x0	clk_gmac_50m_cru_i_sel clk_gmac_50m_cru_i clock mux. 1'b0: clk_matrix_50m_src 1'b1: xin_osc0_func
6:0	RO	0x00	reserved

TOPCRU_CLKSEL_CON46

Address: Operational Base(0xFF100000) + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RW	0x0	clk_testout_bus_sel clk_testout_bus clock mux. 3'b000: aclk_bus 3'b001: 1'b0 3'b010: 1'b0 3'b011: 1'b0 3'b100: clk_dsiphy_txbytehs 3'b101: clk_dsiphy_rxesc 3'b110: 1'b0
12:8	RO	0x00	reserved
7	RW	0x1	clk_gmac_eth_out2io_sel clk_gmac_eth_out2io clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux_from_pmu1
6:0	RW	0x27	clk_gmac_eth_out2io_div Divide clk_gmac_eth_out2io by (div_con + 1).

TOPCRU_CLKSEL_CON47

Address: Operational Base(0xFF100000) + offset (0x01BC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	clk_mac100_50m_matrix_sel clk_mac100_50m_matrix clock mux. 1'b0: clk_matrix_50m_src 1'b1: xin_osc0_func
6:0	RO	0x00	reserved

TOPCRU_GATE_CON00

Address: Operational Base(0xFF100000) + offset (0x0300)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	clk_testout_top_en clk_testout_top clock gating control. When high, disable clock This is also the clk_apll_i_test, clk_hpll_i_test, clk_vpll_i_test Three of them 's gating control. You can gaing the clock when you don't want to test the clock for saving the power. The default value is 1 just for decrease power.
14:7	RO	0x00	reserved
6	RW	0x0	clk_matrix_300m_src_en clk_matrix_300m_src clock gating control. When high, disable clock
5	RO	0x0	reserved
4	RW	0x0	clk_matrix_200m_src_en clk_matrix_200m_src clock gating control. When high, disable clock
3	RO	0x0	reserved
2	RW	0x0	clk_matrix_125m_src_en clk_matrix_125m_src clock gating control. When high, disable clock
1	RW	0x0	clk_matrix_100m_src_en clk_matrix_100m_src clock gating control. When high, disable clock
0	RW	0x0	clk_matrix_50m_src_en clk_matrix_50m_src clock gating control. When high, disable clock

TOPCRU_GATE_CON01

Address: Operational Base(0xFF100000) + offset (0x0304)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_cam3_out2io_en clk_cam3_out2io clock gating control. When high, disable clock
14	RW	0x0	clk_cam2_out2io_en clk_cam2_out2io clock gating control. When high, disable clock
13	RW	0x0	clk_cam1_out2io_en clk_cam1_out2io clock gating control. When high, disable clock
12	RW	0x0	clk_cam0_out2io_en clk_cam0_out2io clock gating control. When high, disable clock
11:10	RO	0x0	reserved
9	RW	0x0	clk_24m_sscsrc_en clk_24m_sscsrc clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
8	RW	0x0	clk_hpll_mux_to_peri_en clk_hpll_mux_to_peri clock gating control. When high, disable clock
7	RW	0x0	clk_gpll_mux_to_peri_en clk_gpll_mux_to_peri clock gating control. When high, disable clock
6	RW	0x0	clk_gpll_mux_to_ddr_en clk_gpll_mux_to_ddr clock gating control. When high, disable clock This is also the clk_gpll_mux_to_core's clock gating control.
5:4	RO	0x0	reserved
3	RW	0x0	clk_pvtpll_logic_o_en clk_pvtpll_logic_o clock gating control. When high, disable clock
2	RW	0x0	clk_ref_pvtpll_logic_en clk_ref_pvtpll_logic clock gating control. When high, disable clock
1	RW	0x0	aclk_top_vio_biu_en aclk_top_vio_biu clock gating control. When high, disable clock
0	RW	0x0	aclk_top_biu_en aclk_top_biu clock gating control. When high, disable clock

TOPCRU_GATE_CON04

Address: Operational Base(0xFF100000) + offset (0x0310)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x1	clk_testout_core_en clk_testout_core clock gating control. When high, disable clock
13	RW	0x0	clk_ref_pvtpll_core_en clk_ref_pvtpll_core clock gating control. When high, disable clock
12:7	RO	0x00	reserved
6	RW	0x0	clk_scanhs_pclk_dbg_en clk_scanhs_pclk_dbg clock gating control. When high, disable clock
5	RW	0x0	pclk_dbg_pre_en pclk_dbg_pre clock gating control. When high, disable clock
4	RW	0x0	clk_scanhs_aclkm_core_en clk_scanhs_aclkm_core clock gating control. When high, disable clock
3	RW	0x0	aclk_core_pre_en aclk_core_pre clock gating control. When high, disable clock
2	RW	0x0	clk_core_pre_en clk_core_pre clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
1	RW	0x0	clk_core_lev1pre_en clk_core_lev1pre clock gating control. When high, disable clock
0	RW	0x0	clk_core_en clk_core clock gating control. When high, disable clock

TOPCRU_GATE_CON05

Address: Operational Base(0xFF100000) + offset (0x0314)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_apll_g_en clk_apll_g clock gating control. When high, disable clock
14	RW	0x0	clk_apll_i clk_apll_i clock gating control. When high, disable clock. Attention: When the core use the pvtpll, you can gate this clock for decrease the power.
13:3	RO	0x000	reserved
2	RW	0x0	hclk_core_biu_en hclk_core_biu clock gating control. When high, disable clock
1	RW	0x0	pclk_core_biu_en pclk_core_biu clock gating control. When high, disable clock
0	RW	0x0	aclk_core_biu_en aclk_core_biu clock gating control. When high, disable clock

TOPCRU_GATE_CON06

Address: Operational Base(0xFF100000) + offset (0x0318)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	clk_testout_npu_en clk_testout_npu clock gating control. When high, disable clock
6	RW	0x0	clk_ref_pvtpll_npu_en clk_ref_pvtpll_npu clock gating control. When high, disable clock
5	RW	0x0	hclk_rknn_en hclk_rknn clock gating control. When high, disable clock
4	RW	0x0	aclk_rknn_en aclk_rknn clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
3	RW	0x0	hclk_npu_biu_en hclk_npu_biu clock gating control. When high, disable clock
2	RW	0x0	aclk_npu_biu_en aclk_npu_biu clock gating control. When high, disable clock
1	RW	0x0	hclk_npu_pre_en hclk_npu_pre clock gating control. When high, disable clock
0	RW	0x0	clk_npu_pre_en clk_npu_pre clock gating control. When high, disable clock

TOPCRU_GATE_CON08

Address: Operational Base(0xFF100000) + offset (0x0320)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	clk_gpu_brg_biu_en clk_gpu_brg_biu clock gating control. When high, disable clock
7	RO	0x0	reserved
6	RW	0x1	clk_testout_gpu_en clk_testout_gpu clock gating control. When high, disable clock
5	RW	0x0	clk_ref_pvtpll_gpu_en clk_ref_pvtpll_gpu clock gating control. When high, disable clock
4	RW	0x0	clk_gpu_en clk_gpu clock gating control. When high, disable clock
3	RW	0x0	aclk_gpu_biu_en aclk_gpu_biu clock gating control. When high, disable clock
2	RW	0x0	aclk_gpu_pre_en aclk_gpu_pre clock gating control. When high, disable clock
1	RW	0x0	clk_gpu_pre_en clk_gpu_pre clock gating control. When high, disable clock
0	RW	0x0	clk_gpu_lev1pre_en clk_gpu_lev1pre clock gating control. When high, disable clock

TOPCRU_GATE_CON09

Address: Operational Base(0xFF100000) + offset (0x0324)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
7	RW	0x1	clk_testout_vepu_en clk_testout_vepu clock gating control. When high, disable clock
6	RW	0x0	hclk_rkvenc_en hclk_rkvenc clock gating control. When high, disable clock
5	RW	0x0	aclk_rkvenc_en aclk_rkvenc clock gating control. When high, disable clock
4	RW	0x0	hclk_vepu_biu_en hclk_vepu_biu clock gating control. When high, disable clock
3	RW	0x0	aclk_vepu_biu_en aclk_vepu_biu clock gating control. When high, disable clock
2	RW	0x0	hclk_vepu_pre_en hclk_vepu_pre clock gating control. When high, disable clock
1	RW	0x0	aclk_vepu_pre_en aclk_vepu_pre clock gating control. When high, disable clock
0	RW	0x0	clk_rkvenc_core_en clk_rkvenc_core clock gating control. When high, disable clock

TOPCRU_GATE_CON10

Address: Operational Base(0xFF100000) + offset (0x0328)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x1	clk_testout_vdpu_en clk_testout_vdpu clock gating control. When high, disable clock
8	RW	0x0	hclk_rkvdec_en hclk_rkvdec clock gating control. When high, disable clock
7	RW	0x0	aclk_rkvdec_en aclk_rkvdec clock gating control. When high, disable clock
6	RW	0x0	hclk_vdpu_biu_en hclk_vdpu_biu clock gating control. When high, disable clock
5	RW	0x0	aclk_vdpu_biu_en aclk_vdpu_biu clock gating control. When high, disable clock
4	RW	0x0	hclk_vdpu_pre_en hclk_vdpu_pre clock gating control. When high, disable clock
3	RW	0x0	clk_rkvdec_hevc_ca_en clk_rkvdec_hevc_ca clock gating control. When high, disable clock
2:1	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	aclk_vdpu_pre_en aclk_vdpu_pre clock gating control. When high, disable clock

TOPCRU_GATE_CON11

Address: Operational Base(0xFF100000) + offset (0x032C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	csirx3_clk_data_en csirx3_clk_data clock gating control. When high, disable clock
14	RW	0x0	csirx2_clk_data_en csirx2_clk_data clock gating control. When high, disable clock
13	RW	0x0	csirx1_clk_data_en csirx1_clk_data clock gating control. When high, disable clock
12	RW	0x0	csirx0_clk_data_en csirx0_clk_data clock gating control. When high, disable clock
11	RW	0x0	dclk_vicap_en dclk_vicap clock gating control. When high, disable clock
10	RW	0x0	hclk_vicap_en hclk_vicap clock gating control. When high, disable clock
9	RW	0x0	aclk_vicap_en aclk_vicap clock gating control. When high, disable clock
8	RW	0x0	clk_isp_en clk_isp clock gating control. When high, disable clock
7	RW	0x0	hclk_isp_en hclk_isp clock gating control. When high, disable clock
6	RW	0x0	aclk_isp_en aclk_isp clock gating control. When high, disable clock
5	RW	0x0	pclk_vi_biu_en pclk_vi_biu clock gating control. When high, disable clock
4	RW	0x0	hclk_vi_biu_en hclk_vi_biu clock gating control. When high, disable clock
3	RW	0x0	aclk_vi_biu_en aclk_vi_biu clock gating control. When high, disable clock
2	RW	0x0	pclk_vi_en pclk_vi clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
1	RW	0x0	hclk_vi_en hclk_vi clock gating control. When high, disable clock
0	RW	0x0	aclk_vi_en aclk_vi clock gating control. When high, disable clock

TOPCRU_GATE_CON12

Address: Operational Base(0xFF100000) + offset (0x0330)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	clk_testout_viphy_en clk_testout_viphy clock gating control. When high, disable clock
14:12	RO	0x0	reserved
11	RW	0x0	clk_rxbytehs_csihost3_dft_en clk_rxbytehs_csihost3_dft clock gating control. When high, disable clock
10	RW	0x0	clk_rxbytehs_csihost2_dft_en clk_rxbytehs_csihost2_dft clock gating control. When high, disable clock
9	RW	0x0	clk_rxbytehs_csihost1_dft_en clk_rxbytehs_csihost1_dft clock gating control. When high, disable clock
8	RW	0x0	clk_rxbytehs_csihost0_dft_en clk_rxbytehs_csihost0_dft clock gating control. When high, disable clock
7:6	RO	0x0	reserved
5	RW	0x0	pclk_csiphy1_en pclk_csiphy1 clock gating control. When high, disable clock
4	RW	0x0	pclk_csiphy0_en pclk_csiphy0 clock gating control. When high, disable clock
3	RW	0x0	pclk_csihost3_en pclk_csihost3 clock gating control. When high, disable clock
2	RW	0x0	pclk_csihost2_en pclk_csihost2 clock gating control. When high, disable clock
1	RW	0x0	pclk_csihost1_en pclk_csihost1 clock gating control. When high, disable clock
0	RW	0x0	pclk_csihost0_en pclk_csihost0 clock gating control. When high, disable clock

TOPCRU_GATE_CON13

Address: Operational Base(0xFF100000) + offset (0x0334)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	clk_testout_vo_en clk_testout_vo clock gating control. When high, disable clock
14:10	RO	0x00	reserved
9	RW	0x0	dclk_vop1_en dclk_vop1 clock gating control. When high, disable clock
8	RW	0x0	dclk_vop_en dclk_vop clock gating control. When high, disable clock
7	RW	0x0	hclk_vop_en hclk_vop clock gating control. When high, disable clock
6	RW	0x0	aclk_vop_en aclk_vop clock gating control. When high, disable clock
5	RO	0x0	reserved
4	RW	0x0	hclk_vo_biu_en hclk_vo_biu clock gating control. When high, disable clock
3	RW	0x0	aclk_vo_biu_en aclk_vo_biu clock gating control. When high, disable clock
2	RO	0x0	reserved
1	RW	0x0	hclk_vo_pre_en hclk_vo_pre clock gating control. When high, disable clock
0	RW	0x0	aclk_vo_pre_en aclk_vo_pre clock gating control. When high, disable clock

TOPCRU_GATE_CON14

Address: Operational Base(0xFF100000) + offset (0x0338)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	clk_testout_rga_en clk_testout_rga clock gating control. When high, disable clock
14:11	RO	0x0	reserved
10	RW	0x0	hclk_jdec_en hclk_jdec clock gating control. When high, disable clock
9	RW	0x0	aclk_jdec_en aclk_jdec clock gating control. When high, disable clock
8	RW	0x0	clk_rga_core_en clk_rga_core clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
7	RW	0x0	hclk_rga_en hclk_rga clock gating control. When high, disable clock
6	RW	0x0	aclk_rga_en aclk_rga clock gating control. When high, disable clock
5	RO	0x0	reserved
4	RW	0x0	hclk_rga_biu_en hclk_rga_biu clock gating control. When high, disable clock
3	RW	0x0	aclk_rga_biu_en aclk_rga_biu clock gating control. When high, disable clock
2	RO	0x0	reserved
1	RW	0x0	hclk_rga_pre_en hclk_rga_pre clock gating control. When high, disable clock
0	RW	0x0	aclk_rga_pre_en aclk_rga_pre clock gating control. When high, disable clock

TOPCRU_GATE_CON16

Address: Operational Base(0xFF100000) + offset (0x0340)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	clk_usb3otg_ref_en clk_usb3otg_ref clock gating control. When high, disable clock
11	RW	0x0	clk_usb3otg_suspend_en clk_usb3otg_suspend clock gating control. When high, disable clock
10	RW	0x0	aclk_usb3otg_en aclk_usb3otg clock gating control. When high, disable clock
9	RO	0x0	reserved
8	RW	0x0	clk_pcie20_aux_en clk_pcie20_aux clock gating control. When high, disable clock
7	RW	0x0	pclk_pcie20_en pclk_pcie20 clock gating control. When high, disable clock
6	RW	0x0	aclk_pcie20_dbi_en aclk_pcie20_dbi clock gating control. When high, disable clock
5	RW	0x0	aclk_pcie20_slv_en aclk_pcie20_slv clock gating control. When high, disable clock
4	RW	0x0	aclk_pcie20_mst_en aclk_pcie20_mst clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
3	RW	0x0	aclk_php_biu_en aclk_php_biu clock gating control. When high, disable clock
2	RW	0x0	pclk_php_biu_en pclk_php_biu clock gating control. When high, disable clock
1	RW	0x0	pclk_php_en pclk_php clock gating control. When high, disable clock
0	RW	0x0	aclk_php_en aclk_php clock gating control. When high, disable clock

TOPCRU_GATE_CON17

Address: Operational Base(0xFF100000) + offset (0x0344)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	clk_testout_phpphy_en clk_testout_phpphy clock gating control. When high, disable clock
14:4	RO	0x000	reserved
3	RW	0x0	clk_pipephy_ref_func_en clk_pipephy_ref_func clock gating control. When high, disable clock
2	RW	0x0	clk_usbphy_usb3otg_utmi_dft_en clk_usbphy_usb3otg_utmi_dft clock gating control. When high, disable clock
1	RW	0x0	clk_usb3otg_pipe_dft_en clk_usb3otg_pipe_dft clock gating control. When high, disable clock
0	RW	0x0	clk_pipephy_en clk_pipephy_pipe_g clock gating control. When high, disable clock

TOPCRU_GATE_CON18

Address: Operational Base(0xFF100000) + offset (0x0348)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	pclk_bus_biu_en pclk_bus_biu clock gating control. When high, disable clock
4	RW	0x0	hclk_bus_biu_en hclk_bus_biu clock gating control. When high, disable clock
3	RW	0x0	aclk_bus_biu_en aclk_bus_biu clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
2	RW	0x0	pclk_bus_en pclk_bus clock gating control. When high, disable clock
1	RW	0x0	hclk_bus_en hclk_bus clock gating control. When high, disable clock
0	RW	0x0	aclk_bus_en aclk_bus clock gating control. When high, disable clock

TOPCRU_GATE_CON19

Address: Operational Base(0xFF100000) + offset (0x034C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10	RW	0x0	clk_i2c5_en clk_i2c5 clock gating control. When high, disable clock
9	RW	0x0	clk_i2c4_en clk_i2c4 clock gating control. When high, disable clock
8	RW	0x0	clk_i2c3_en clk_i2c3 clock gating control. When high, disable clock
7	RW	0x0	clk_i2c2_en clk_i2c2 clock gating control. When high, disable clock
6	RW	0x0	clk_i2c1_en clk_i2c1 clock gating control. When high, disable clock
5	RW	0x0	clk_i2c_en clk_i2c clock gating control. When high, disable clock
4	RW	0x0	pclk_i2c5_en pclk_i2c5 clock gating control. When high, disable clock
3	RW	0x0	pclk_i2c4_en pclk_i2c4 clock gating control. When high, disable clock
2	RW	0x0	pclk_i2c3_en pclk_i2c3 clock gating control. When high, disable clock
1	RW	0x0	pclk_i2c2_en pclk_i2c2 clock gating control. When high, disable clock
0	RW	0x0	pclk_i2c1_en pclk_i2c1 clock gating control. When high, disable clock

TOPCRU_GATE_CON20

Address: Operational Base(0xFF100000) + offset (0x0350)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	dclk_bus_gpio4_en dclk_bus_gpio4 clock gating control. When high, disable clock
5	RW	0x0	dclk_bus_gpio3_en dclk_bus_gpio3 clock gating control. When high, disable clock
4	RW	0x0	dclk_bus_gpio_en dclk_bus_gpio clock gating control. When high, disable clock
3:0	RO	0x0	reserved

TOPCRU_GATE_CON21

Address: Operational Base(0xFF100000) + offset (0x0354)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	clk_stimer1_en clk_stimer1 clock gating control. When high, disable clock
8	RW	0x0	clk_stimer0_en clk_stimer0 clock gating control. When high, disable clock
7	RW	0x0	pclk_stimer_en pclk_stimer clock gating control. When high, disable clock
6	RW	0x0	clk_timer5_en clk_timer5 clock gating control. When high, disable clock
5	RW	0x0	clk_timer4_en clk_timer4 clock gating control. When high, disable clock
4	RW	0x0	clk_timer3_en clk_timer3 clock gating control. When high, disable clock
3	RW	0x0	clk_timer2_en clk_timer2 clock gating control. When high, disable clock
2	RW	0x0	clk_timer1_en clk_timer1 clock gating control. When high, disable clock
1	RW	0x0	clk_timer0_en clk_timer0 clock gating control. When high, disable clock
0	RW	0x0	pclk_timer_en pclk_timer clock gating control. When high, disable clock

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TOPCRU_GATE_CON22

Address: Operational Base(0xFF100000) + offset (0x0358)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	aclk_bus_gic400_en aclk_bus_gic400 clock gating control. When high, disable clock
5	RW	0x0	pclk_intc_en pclk_intc clock gating control. When high, disable clock
4	RW	0x0	pclk_mailbox_en pclk_mailbox clock gating control. When high, disable clock
3	RW	0x0	pclk_sgrf_en pclk_sgrf clock gating control. When high, disable clock
2	RW	0x0	pclk_grf_en pclk_grf clock gating control. When high, disable clock
1	RW	0x0	clk_wdtns_en clk_wdtns clock gating control. When high, disable clock
0	RW	0x0	pclk_wdtns_en pclk_wdtns clock gating control. When high, disable clock

TOPCRU_GATE_CON23

Address: Operational Base(0xFF100000) + offset (0x035C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	hclk_dcache_en hclk_dcache clock gating control. When high, disable clock
8	RW	0x0	hclk_icache_en hclk_icache clock gating control. When high, disable clock
7:5	RO	0x0	reserved
4	RW	0x0	clk_bus_cm0_rtc_en clk_bus_cm0_rtc clock gating control. When high, disable clock
3	RW	0x0	fclk_bus_cm0_core_en fclk_bus_cm0_core clock gating control. When high, disable clock
2	RW	0x0	pclk_dcf_en pclk_dcf clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
1	RW	0x0	aclk_dcf_en aclk_dcf clock gating control. When high, disable clock
0	RW	0x0	aclk_bus_spinlock_en aclk_bus_spinlock clock gating control. When high, disable clock

TOPCRU_GATE_CON24

Address: Operational Base(0xFF100000) + offset (0x0360)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	clk_saradc_vccio156_en clk_saradc_to_vccio156 clock gating control. When high, disable clock
8:5	RO	0x0	reserved
4	RW	0x0	pclk_dft2apb_en pclk_dft2apb clock gating control. When high, disable clock
3	RW	0x0	clk_tsadc_tsen_en clk_tsadc_tsen clock gating control. When high, disable clock
2	RO	0x0	reserved
1	RW	0x0	clk_tsadc_en clk_tsadc clock gating control. When high, disable clock
0	RW	0x0	pclk_tsadc_en pclk_tsadc clock gating control. When high, disable clock

TOPCRU_GATE_CON25

Address: Operational Base(0xFF100000) + offset (0x0364)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pclk_topcru_en pclk_topcru clock gating control. When high, disable clock
14	RW	0x1	clk_testout_bus_en clk_testout_bus clock gating control. When high, disable clock
13:12	RO	0x0	reserved
11	RW	0x0	pclk_hash_en pclk_hash clock gating control. When high, disable clock
10	RW	0x0	pclk_cpu_ema_det_en pclk_cpu_ema_det clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
9	RW	0x0	pclk_dsitx_en pclk_dsitx clock gating control. When high, disable clock
8	RW	0x0	pclk_dsiphy_en pclk_dsiphy clock gating control. When high, disable clock
7	RO	0x0	reserved
6	RW	0x0	pclk_to_vccio156_en pclk_to_vccio156 clock gating control. When high, disable clock
5	RW	0x0	pclk_apb2asb_vccio156_en pclk_apb2asb_vccio156 clock gating control. When high, disable clock
4	RW	0x0	clk_gmac_eth_out2io_en clk_gmac_eth_out2io clock gating control. When high, disable clock
3	RW	0x0	clk_gmac_50m_cru_en clk_gmac_50m_cru_i clock gating control. When high, disable clock
2	RW	0x0	clk_gmac_125m_cru_en clk_gmac_125m_cru_i clock gating control. When high, disable clock
1	RW	0x0	aclk_gmac_en aclk_gmac clock gating control. When high, disable clock
0	RW	0x0	pclk_gmac_en pclk_gmac clock gating control. When high, disable clock

TOPCRU_GATE_CON26

Address: Operational Base(0xFF100000) + offset (0x0368)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x0	pclk_saradc_vccio156_en pclk_saradc_vccio156 clock gating control. When high, disable clock
3	RW	0x0	pclk_gpio4_vccio156_en pclk_gpio4_vccio156 clock gating control. When high, disable clock
2	RW	0x0	pclk_gpio3_vccio156_en pclk_gpio3_vccio156 clock gating control. When high, disable clock
1	RW	0x0	pclk_ioc_vccio156_en pclk_ioc_vccio156 clock gating control. When high, disable clock
0	RW	0x0	pclk_asb2apb_vccio156_en pclk_asb2apb_vccio156 clock gating control. When high, disable clock

TOPCRU_GATE_CON27

Address: Operational Base(0xFF100000) + offset (0x036C)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2	RW	0x0	clk_mac100_50m_cru_en clk_mac100_50m_matrix clock gating control. When high, disable clock
1	RW	0x0	aclk_mac100_en aclk_mac100 clock gating control. When high, disable clock
0	RW	0x0	pclk_mac100_en pclk_mac100 clock gating control. When high, disable clock

TOPCRU_SOFTRST_CON01

Address: Operational Base(0xFF100000) + offset (0x0404)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2	RW	0x0	resetn_ref_pvtpll_logic When high, reset relative logic
1	RW	0x0	aresetn_top_vio_biu When high, reset relative logic
0	RW	0x0	aresetn_top_biu When high, reset relative logic

TOPCRU_SOFTRST_CON03

Address: Operational Base(0xFF100000) + offset (0x040C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	nl2reset When high, reset relative logic
7	RW	0x0	ncoreset3 When high, reset relative logic
6	RW	0x0	ncoreset2 When high, reset relative logic
5	RW	0x0	ncoreset1 When high, reset relative logic
4	RW	0x0	ncoreset0 When high, reset relative logic
3	RW	0x0	ncoreporeset3 When high, reset relative logic
2	RW	0x0	ncoreporeset2 When high, reset relative logic
1	RW	0x0	ncoreporeset1 When high, reset relative logic

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Bit	Attr	Reset Value	Description
0	RW	0x0	ncoreporeset0 When high, reset relative logic

TOPCRU_SOFTRST_CON04

Address: Operational Base(0xFF100000) + offset (0x0410)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	resetn_ref_pvtpll_core When high, reset relative logic
12:11	RO	0x0	reserved
10	RW	0x0	presetn_dbg_daplite When high, reset relative logic
9	RW	0x0	resetn_dap When high, reset relative logic
8:0	RO	0x000	reserved

TOPCRU_SOFTRST_CON05

Address: Operational Base(0xFF100000) + offset (0x0414)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2	RW	0x0	hresetn_core_biu When high, reset relative logic
1	RW	0x0	presetn_core_biu When high, reset relative logic
0	RW	0x0	aresetn_core_biu When high, reset relative logic

TOPCRU_SOFTRST_CON06

Address: Operational Base(0xFF100000) + offset (0x0418)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	resetn_ref_pvtpll_npu When high, reset relative logic
5	RW	0x0	hresetn_rknn When high, reset relative logic
4	RW	0x0	aresetn_rknn When high, reset relative logic
3	RW	0x0	hresetn_npu_biu When high, reset relative logic
2	RW	0x0	aresetn_npu_biu When high, reset relative logic
1:0	RO	0x0	reserved

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TOPCRU_SOFTRST_CON08

Address: Operational Base(0xFF100000) + offset (0x0420)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	resetn_gpu_brg_biu When high, reset relative logic
7:6	RO	0x0	reserved
5	RW	0x0	resetn_ref_pvtpll_gpu When high, reset relative logic
4	RW	0x0	resetn_gpu When high, reset relative logic
3	RW	0x0	aresetn_gpu_biu When high, reset relative logic
2:0	RO	0x0	reserved

TOPCRU_SOFTRST_CON09

Address: Operational Base(0xFF100000) + offset (0x0424)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	hresetn_rkvenc When high, reset relative logic
5	RW	0x0	aresetn_rkvenc When high, reset relative logic
4	RW	0x0	hresetn_vepu_biu When high, reset relative logic
3	RW	0x0	aresetn_vepu_biu When high, reset relative logic
2:1	RO	0x0	reserved
0	RW	0x0	resetn_rkvenc_core When high, reset relative logic

TOPCRU_SOFTRST_CON10

Address: Operational Base(0xFF100000) + offset (0x0428)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	hresetn_rkvdec When high, reset relative logic
7	RW	0x0	aresetn_rkvdec When high, reset relative logic
6	RW	0x0	hresetn_vdpu_biu When high, reset relative logic
5	RW	0x0	aresetn_vdpu_biu When high, reset relative logic
4:3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2	RW	0x0	resetn_rkvdec_hevc_ca When high, reset relative logic
1:0	RO	0x0	reserved

TOPCRU_SOFTRST_CON11

Address: Operational Base(0xFF100000) + offset (0x042C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	i3resetn_vicap When high, reset relative logic
14	RW	0x0	i2resetn_vicap When high, reset relative logic
13	RW	0x0	i1resetn_vicap When high, reset relative logic
12	RW	0x0	i0resetn_vicap When high, reset relative logic
11	RW	0x0	dresetn_vicap When high, reset relative logic
10	RW	0x0	hresetn_vicap When high, reset relative logic
9	RW	0x0	aresetn_vicap When high, reset relative logic
8	RW	0x0	resetn_isp When high, reset relative logic
7:6	RO	0x0	reserved
5	RW	0x0	presetn_vi_biu When high, reset relative logic
4	RW	0x0	hresetn_vi_biu When high, reset relative logic
3	RW	0x0	aresetn_vi_biu When high, reset relative logic
2:0	RO	0x0	reserved

TOPCRU_SOFTRST_CON12

Address: Operational Base(0xFF100000) + offset (0x0430)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	presetn_csiphy1 When high, reset relative logic
4	RW	0x0	presetn_csiphy0 When high, reset relative logic
3	RW	0x0	presetn_csihost3 When high, reset relative logic
2	RW	0x0	presetn_csihost2 When high, reset relative logic
1	RW	0x0	presetn_csihost1 When high, reset relative logic

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Bit	Attr	Reset Value	Description
0	RW	0x0	presetn_csihost0 When high, reset relative logic

TOPCRU_SOFTRST_CON13

Address: Operational Base(0xFF100000) + offset (0x0434)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	dresetn_vop1 When high, reset relative logic
8	RW	0x0	dresetn_vop When high, reset relative logic
7	RW	0x0	hresetn_vop When high, reset relative logic
6	RW	0x0	aresetn_vop When high, reset relative logic
5	RO	0x0	reserved
4	RW	0x0	hresetn_vo_biu When high, reset relative logic
3	RW	0x0	aresetn_vo_biu When high, reset relative logic
2:0	RO	0x0	reserved

TOPCRU_SOFTRST_CON14

Address: Operational Base(0xFF100000) + offset (0x0438)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10	RW	0x0	hresetn_jdec When high, reset relative logic
9	RW	0x0	aresetn_jdec When high, reset relative logic
8	RW	0x0	resetn_rga_core When high, reset relative logic
7	RW	0x0	hresetn_rga When high, reset relative logic
6	RW	0x0	aresetn_rga When high, reset relative logic
5	RO	0x0	reserved
4	RW	0x0	hresetn_rga_biu When high, reset relative logic
3	RW	0x0	aresetn_rga_biu When high, reset relative logic
2:0	RO	0x0	reserved

TOPCRU_SOFTRST_CON16

Address: Operational Base(0xFF100000) + offset (0x0440)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10	RW	0x0	resetn_usb3otg When high, reset relative logic
9	RO	0x0	reserved
8	RW	0x1	resetn_pcie20_powerup When high, reset relative logic
7	RW	0x0	presetn_pcie20 When high, reset relative logic
6:4	RO	0x0	reserved
3	RW	0x0	aresetn_php_biu When high, reset relative logic
2	RW	0x0	presetn_php_biu When high, reset relative logic
1:0	RO	0x0	reserved

TOPCRU_SOFTRST_CON17

Address: Operational Base(0xFF100000) + offset (0x0444)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	resetn_pipephy When high, reset relative logic
2:0	RO	0x0	reserved

TOPCRU_SOFTRST_CON18

Address: Operational Base(0xFF100000) + offset (0x0448)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	presetn_bus_biu When high, reset relative logic
4	RW	0x0	hresetn_bus_biu When high, reset relative logic
3	RW	0x0	aresetn_bus_biu When high, reset relative logic
2:0	RO	0x0	reserved

TOPCRU_SOFTRST_CON19

Address: Operational Base(0xFF100000) + offset (0x044C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
10	RW	0x0	resetn_i2c5 When high, reset relative logic
9	RW	0x0	resetn_i2c4 When high, reset relative logic
8	RW	0x0	resetn_i2c3 When high, reset relative logic
7	RW	0x0	resetn_i2c2 When high, reset relative logic
6	RW	0x0	resetn_i2c1 When high, reset relative logic
5	RO	0x0	reserved
4	RW	0x0	presetn_i2c5 When high, reset relative logic
3	RW	0x0	presetn_i2c4 When high, reset relative logic
2	RW	0x0	presetn_i2c3 When high, reset relative logic
1	RW	0x0	presetn_i2c2 When high, reset relative logic
0	RW	0x0	presetn_i2c1 When high, reset relative logic

TOPCRU_SOFTRST_CON20

Address: Operational Base(0xFF100000) + offset (0x0450)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	resetn_bus_gpio4 When high, reset relative logic
5	RW	0x0	resetn_bus_gpio3 When high, reset relative logic
4:0	RO	0x00	reserved

TOPCRU_SOFTRST_CON21

Address: Operational Base(0xFF100000) + offset (0x0454)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	resetn_stimer1 When high, reset relative logic
8	RW	0x0	resetn_stimer0 When high, reset relative logic
7	RW	0x0	presetn_stimer When high, reset relative logic
6	RW	0x0	resetn_timer5 When high, reset relative logic
5	RW	0x0	resetn_timer4 When high, reset relative logic

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Bit	Attr	Reset Value	Description
4	RW	0x0	resetn_timer3 When high, reset relative logic
3	RW	0x0	resetn_timer2 When high, reset relative logic
2	RW	0x0	resetn_timer1 When high, reset relative logic
1	RW	0x0	resetn_timer0 When high, reset relative logic
0	RW	0x0	presetn_timer When high, reset relative logic

TOPCRU_SOFTRST_CON22

Address: Operational Base(0xFF100000) + offset (0x0458)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	aresetn_bus_gic400_debug When high, reset relative logic
6	RW	0x0	aresetn_bus_gic400 When high, reset relative logic
5	RW	0x0	presetn_intc When high, reset relative logic
4	RW	0x0	presetn_mailbox When high, reset relative logic
3	RW	0x0	presetn_sgrf When high, reset relative logic
2	RW	0x0	presetn_grf When high, reset relative logic
1	RW	0x0	resetn_wdtns When high, reset relative logic
0	RW	0x0	presetn_wdtns When high, reset relative logic

TOPCRU_SOFTRST_CON23

Address: Operational Base(0xFF100000) + offset (0x045C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	hresetn_dcache When high, reset relative logic
8	RW	0x0	hresetn_icache When high, reset relative logic
7:6	RO	0x0	reserved
5	RW	0x0	tresetn_bus_cm0_jtag When high, reset relative logic
4	RO	0x0	reserved
3	RW	0x1	fresetn_bus_cm0_core When high, reset relative logic

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Bit	Attr	Reset Value	Description
2	RW	0x0	presetn_dcf When high, reset relative logic
1	RW	0x0	aresetn_dcf When high, reset relative logic
0	RW	0x0	aresetn_bus_spinlock When high, reset relative logic

TOPCRU_SOFTRST_CON24

Address: Operational Base(0xFF100000) + offset (0x0460)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x0	presetn_dft2apb When high, reset relative logic
3	RO	0x0	reserved
2	RW	0x0	resetn_tsadcphy When high, reset relative logic
1	RW	0x0	resetn_tsadc When high, reset relative logic
0	RW	0x0	presetn_tsadc When high, reset relative logic

TOPCRU_SOFTRST_CON25

Address: Operational Base(0xFF100000) + offset (0x0464)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	presetn_topcru When high, reset relative logic
14:12	RO	0x0	reserved
11	RW	0x0	presetn_hash When high, reset relative logic
10	RW	0x0	presetn_cpu_ema_det When high, reset relative logic
9	RW	0x0	presetn_dsitx When high, reset relative logic
8	RW	0x0	presetn_dsiphy When high, reset relative logic
7:6	RO	0x0	reserved
5	RW	0x0	presetn_apb2asb_vccio156 When high, reset relative logic
4:2	RO	0x0	reserved
1	RW	0x0	aresetn_gmac When high, reset relative logic
0	RO	0x0	reserved

TOPCRU_SOFTRST_CON26

Address: Operational Base(0xFF100000) + offset (0x0468)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	resetn_saradc_vccio156_phy When high, reset relative logic
5	RW	0x0	resetn_saradc_vccio156 When high, reset relative logic
4	RW	0x0	presetn_saradc_vccio156 When high, reset relative logic
3	RW	0x0	presetn_gpio4_vccio156 When high, reset relative logic
2	RW	0x0	presetn_gpio3_vccio156 When high, reset relative logic
1	RW	0x0	presetn_ioc_vccio156 When high, reset relative logic
0	RW	0x0	presetn_asb2apb_vccio156 When high, reset relative logic

TOPCRU_SOFTRST_CON27

Address: Operational Base(0xFF100000) + offset (0x046C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	aresetn_mac100 When high, reset relative logic
0	RO	0x0	reserved

TOPCRU_SSGTBL0_3

Address: Operational Base(0xFF100000) + offset (0x0500)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl0_3 Extern wave table 0-3 7-0: table0 15-8: table1 23-16: table2 31-24: table3

TOPCRU_SSGTBL4_7

Address: Operational Base(0xFF100000) + offset (0x0504)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl4_7 Extern wave table 4-7 7-0: table4 15-8: table5 23-16: table6 31-24: table7

TOPCRU_SSGTBL8_11

Address: Operational Base(0xFF100000) + offset (0x0508)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl8_11 Extern wave table 8-11 7-0: table8 15-8: table9 23-16: table10 31-24: table11

TOPCRU_SSGTBL12_15

Address: Operational Base(0xFF100000) + offset (0x050C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl12_15 Extern wave table 12-15 7-0: table12 15-8: table13 23-16: table14 31-24: table15

TOPCRU_SSGTBL16_19

Address: Operational Base(0xFF100000) + offset (0x0510)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl16_19 Extern wave table 16-19 7-0: table16 15-8: table17 23-16: table18 31-24: table19

TOPCRU_SSGTBL20_23

Address: Operational Base(0xFF100000) + offset (0x0514)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl20_23 Extern wave table 20-23 7-0: table20 15-8: table21 23-16: table22 31-24: table23

TOPCRU_SSGTBL24_27

Address: Operational Base(0xFF100000) + offset (0x0518)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl24_27 Extern wave table 24-27 7-0: table24 15-8: table25 23-16: table26 31-24: table27

TOPCRU_SSGTBL28_31

Address: Operational Base(0xFF100000) + offset (0x051C)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl28_31 Extern wave table 28-31 7-0: table28 15-8: table29 23-16: table30 31-24: table31

TOPCRU_SSGTBL32_35

Address: Operational Base(0xFF100000) + offset (0x0520)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl32_35 Extern wave table 32-35 7-0: table32 15-8: table33 23-16: table34 31-24: table35

TOPCRU_SSGTBL36_39

Address: Operational Base(0xFF100000) + offset (0x0524)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl36_39 Extern wave table 36-39 7-0: table36 15-8: table37 23-16: table38 31-24: table39

TOPCRU_SSGTBL40_43

Address: Operational Base(0xFF100000) + offset (0x0528)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl40_43 Extern wave table 40-43 7-0: table40 15-8: table41 23-16: table42 31-24: table43

TOPCRU_SSGTBL44_47

Address: Operational Base(0xFF100000) + offset (0x052C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl44_47 Extern wave table 44-47 7-0: table44 15-8: table45 23-16: table46 31-24: table47

TOPCRU_SSGTBL48_51

Address: Operational Base(0xFF100000) + offset (0x0530)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl48_51 Extern wave table 48-51 7-0: table48 15-8: table49 23-16: table50 31-24: table51

TOPCRU_SSGTBL52_55

Address: Operational Base(0xFF100000) + offset (0x0534)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl52_55 Extern wave table 52-55 7-0: table52 15-8: table53 23-16: table54 31-24: table55

TOPCRU_SSGTBL56_59

Address: Operational Base(0xFF100000) + offset (0x0538)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl56_59 Extern wave table 56-59 7-0: table56 15-8: table57 23-16: table58 31-24: table59

TOPCRU_SSGTBL60_63

Address: Operational Base(0xFF100000) + offset (0x053C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl60_63 Extern wave table 60-63 7-0: table60 15-8: table61 23-16: table62 31-24: table63

TOPCRU_SSGTBL64_67

Address: Operational Base(0xFF100000) + offset (0x0540)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl64_67 Extern wave table 64-67 7-0: table64 15-8: table65 23-16: table66 31-24: table67

TOPCRU_SSGTBL68_71

Address: Operational Base(0xFF100000) + offset (0x0544)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl68_71 Extern wave table 68-71 7-0: table68 15-8: table69 23-16: table70 31-24: table71

TOPCRU_SSGTBL72_75

Address: Operational Base(0xFF100000) + offset (0x0548)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl72_75 Extern wave table 72-75 7-0: table72 15-8: table73 23-16: table74 31-24: table75

TOPCRU_SSGTBL76_79

Address: Operational Base(0xFF100000) + offset (0x054C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl76_79 Extern wave table 76-79 7-0: table76 15-8: table77 23-16: table78 31-24: table79

TOPCRU_SSGTBL80_83

Address: Operational Base(0xFF100000) + offset (0x0550)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl80_83 Extern wave table 76-79 7-0: table80 15-8: table81 23-16: table82 31-24: table83

TOPCRU_SSGTBL84_87

Address: Operational Base(0xFF100000) + offset (0x0554)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl84_87 Extern wave table 84-87 7-0: table84 15-8: table85 23-16: table86 31-24: table87

TOPCRU_SSGTBL88_91

Address: Operational Base(0xFF100000) + offset (0x0558)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl88_91 Extern wave table 88-91 7-0: table88 15-8: table89 23-16: table90 31-24: table91

TOPCRU_SSGTBL92_95

Address: Operational Base(0xFF100000) + offset (0x055C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl92_95 Extern wave table 92-95 7-0: table92 15-8: table93 23-16: table94 31-24: table95

TOPCRU_SSGTBL96_99

Address: Operational Base(0xFF100000) + offset (0x0560)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl96_99 Extern wave table 96-99 7-0: table96 15-8: table97 23-16: table98 31-24: table99

TOPCRU_SSGTBL100_103

Address: Operational Base(0xFF100000) + offset (0x0564)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl100_103 Extern wave table 100-103 7-0: table100 15-8: table101 23-16: table102 31-24: table103

TOPCRU_SSGTBL104_107

Address: Operational Base(0xFF100000) + offset (0x0568)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl104_107 Extern wave table 104-107 7-0: table104 15-8: table105 23-16: table106 31-24: table107

TOPCRU_SSGTBL108_111

Address: Operational Base(0xFF100000) + offset (0x056C)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl108_111 Extern wave table 108-111 7-0: table108 15-8: table109 23-16: table110 31-24: table111

TOPCRU_SSGTBL112_115

Address: Operational Base(0xFF100000) + offset (0x0570)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl112_115 Extern wave table 112-115 7-0: table112 15-8: table113 23-16: table114 31-24: table115

TOPCRU_SSGTBL116_119

Address: Operational Base(0xFF100000) + offset (0x0574)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl116_119 Extern wave table 116-119 7-0: table116 15-8: table117 23-16: table118 31-24: table119

TOPCRU_SSGTBL120_123

Address: Operational Base(0xFF100000) + offset (0x0578)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl120_123 Extern wave table 120-123 7-0: table120 15-8: table121 23-16: table122 31-24: table123

TOPCRU_SSGTBL124_127

Address: Operational Base(0xFF100000) + offset (0x057C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl124_127 Extern wave table 124-127 7-0: table124 15-8: table125 23-16: table126 31-24: table127

TOPCRU_MODE_CON00

Address: Operational Base(0xFF100000) + offset (0x0600)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:8	RW	0x0	clk_hpll_mode clk_hpll_mux clock mux. 2'b00: xin_osc0_func 2'b01: clk_hpll 2'b10: clk_deepslow
7:6	RW	0x0	clk_vpll_mode clk_vpll_mux clock mux. 2'b00: xin_osc0_func 2'b01: clk_vpll 2'b10: clk_deepslow
5:4	RO	0x0	reserved
3:2	RW	0x0	clk_gpll_mode clk_gpll_mux clock mux. 2'b00: xin_osc0_func 2'b01: clk_gpll 2'b10: clk_deepslow
1:0	RW	0x0	clk_apll_mode clk_apll_mux clock mux. 2'b00: xin_osc0_func 2'b01: clk_apll 2'b10: clk_deepslow

TOPCRU_GLB_CNT_TH

Address: Operational Base(0xFF100000) + offset (0x0610)

Bit	Attr	Reset Value	Description
31:16	RW	0x0064	Reserved
15:0	RW	0x0064	global_reset_counter_threshold Global soft reset, wdt reset or tsadc_shut reset asserted time counter threshold. Measured in OSC clock cycles

TOPCRU_GLB_SRST_FST

Address: Operational Base(0xFF100000) + offset (0x0614)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	GLB_SRST_FST The first global software reset config value

TOPCRU_GLB_SRST_SND

Address: Operational Base(0xFF100000) + offset (0x0618)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	GLB_SRST_SND The second global software reset config value

TOPCRU_GLB_RST_CON

Address: Operational Base(0xFF100000) + offset (0x061C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	pmusgrf_crc_chk_glb_srst_ctrl 1'b0: Pmusgrf crc chk trigger second global reset 1'b1: Pmusgrf crc chk trigger first global reset effective when glb_rst_con[11] enable
14:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11	RW	0x0	pmusgrf_crc_chk_glb_srst_ctrl_enable 1'b0: Pmusgrf crc chk dont trigger global reset 1'b1: Pmusgrf crc chk trigger global reset
10:8	RO	0x0	reserved
7	RW	0x0	wdt_reset_ext_en 1: Enable wdt reset extend, reset extend time depend on bit15~0 of GLB_CNT_TH 0: Disable wdt reset extend
6	RW	0x0	tsadc_shut_reset_ext_en 1: Enable tsadc_shut reset extend, reset extend time depend on bit15~0 of GLB_CNT_TH 0: Disable tsadc_shut reset extend
5	RO	0x0	reserved
4	RW	0x0	pmu_srst_wdt_en 0: Enable Wdt reset as pmu reset source 1: Disable Wdt reset as pmu reset source
3	RW	0x0	pmu_srst_glb_en 1'b0: global reset trigger pmu reset 1'b1: global reset dont trigger pmu reset
2	RW	0x0	pmu_srst_glb_ctrl 0: Enable first global reset as pmu reset source 1: Enable second global reset as pmu reset source effective when glb_rst_con[3] enable
1	RW	0x0	wdt_glb_srst_ctrl 1'b0: Wdt trigger second global reset 1'b1: Wdt trigger first global reset
0	RW	0x0	tsadc_glb_srst_ctrl 1'b0: tsadc trigger second global reset 1'b1: tsadc trigger first global reset

TOPCRU_GLB_RST_ST

Address: Operational Base(0xFF100000) + offset (0x0620)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	glb_pmusgrf_crc_rst_st global PMUSGRF CRC CHK triggered reset flag 1'b0: Last hot reset is not global PMUSGRF CRC CHK triggered reset 1'b1: Last hot reset is global PMUSGRF CRC CHK triggered reset
8:6	RO	0x0	reserved
5	RW	0x0	snd_glb_wdt_rst_st sencond global WDT triggered reset flag 1'b0: Last hot reset is not sencond global WDT triggered reset 1'b1: Last hot reset is sencond global WDT triggered reset
4	RW	0x0	fst_glb_wdt_rst_st first global WDT triggered reset flag 1'b0: Last hot reset is not first global WDT triggered reset 1'b1: Last hot reset is first global WDT triggered reset
3	RW	0x0	snd_glb_tsadc_rst_st sencond global TSADC triggered reset flag 1'b0: Last hot reset is not sencond global TSADC triggered reset 1'b1: Last hot reset is sencond global TSADC triggered reset

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Bit	Attr	Reset Value	Description
2	RW	0x0	fst_glb_tsadc_rst_st first global TSADC triggered reset flag 1'b0: Last hot reset is not first global TSADC triggered reset 1'b1: Last hot reset is first global TSADC triggered reset
1	RW	0x0	snd_glb_rst_st second global rst flag 1'b0: Last hot reset is not sencond global reset 1'b1: Last hot reset is sencond global reset
0	RW	0x0	fst_glb_rst_st first global rst flag 1'b0: Last hot reset is not first global reset 1'b1: Last hot reset is first global reset

TOPCRU_SDMMC0_CON0

Address: Operational Base(0xFF100000) + offset (0x0624)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x1	ram_clkgat_disable
12	RW	0x0	test_clkout_0_sel
11	RW	0x0	drv_sel
10:3	RW	0x00	drv_delaynum delay num value.
2:1	RW	0x2	drv_degree
0	RO	0x0	init_state

TOPCRU_SDMMC0_CON1

Address: Operational Base(0xFF100000) + offset (0x0628)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	test_clkout_1_sel
11	RW	0x0	sample_sel
10:3	RW	0x00	sample_delaynum delay num value.
2:1	RW	0x0	sample_degree
0	RO	0x0	reserved

TOPCRU_SDMMC1_CON0

Address: Operational Base(0xFF100000) + offset (0x062C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x1	ram_clkgat_disable
12	RW	0x0	test_clkout_0_sel
11	RW	0x0	drv_sel

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Bit	Attr	Reset Value	Description
10:3	RW	0x00	drv_delaynum delay num value.
2:1	RW	0x2	drv_degree
0	RO	0x0	init_state

TOPCRU_SDMMC1_CON1

Address: Operational Base(0xFF100000) + offset (0x0630)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	test_clkout_1_sel
11	RW	0x0	sample_sel
10:3	RW	0x00	sample_delaynum delay num value.
2:1	RW	0x0	sample_degree
0	RO	0x0	reserved

TOPCRU_EMMC_CON

Address: Operational Base(0xFF100000) + offset (0x063C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2	RW	0x1	ram_clkgat_disable
1	RW	0x1	clkbypass
0	RW	0x1	clkstable

TOPCRU_CM0_GATEMASK

Address: Operational Base(0xFF100000) + offset (0x0680)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2	RW	0x1	sgrf_con_mcu_sclk_cm0s_en =0: not gated the clk, but if the ip gated the clk, so the clk can also be gated. =1: gated the clk. the clk we talk about is the "sclk".
1	RW	0x1	sgrf_con_mcu_hclk_cm0s_en =0: not gated the clk, but if the ip gated the clk, so the clk can also be gated. =1: gated the clk. the clk we talk about is the "hclk".
0	RW	0x1	sgrf_con_muc_dclk_cm0s_en =0: not gated the clk, but if the ip gated the clk, so the clk can also be gated. =1: gated the clk. the clk we talk about is the "dclk".

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TOPCRU_MISC_CON0

Address: Operational Base(0xFF100000) + offset (0x0684)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	enable_rga_idle_clk_core
2	RO	0x0	reserved
1	RW	0x0	enable_pd_bus_clk_src_gating
0	RW	0x0	enable_cluseter_clk_src_gating

TOPCRU_MISC_CON1

Address: Operational Base(0xFF100000) + offset (0x0688)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	corepo3_srstn_en "corepo3_srstn_en" is the core3 power resetn enable. =1: enable it. =0: disable it.
12	RW	0x0	corepo2_srstn_en "corepo2_srstn_en" is the core2 power resetn enable. =1: enable it. =0: disable it.
11	RW	0x0	corepo1_srstn_en "corepo1_srstn_en" is the core1 power resetn enable. =1: enable it. =0: disable it.
10	RW	0x0	core3_srstn_en "core3_srstn_en" is the core3 software rst enable. =1: enable it. =0: disable it.
9	RW	0x0	core2_srstn_en "core2_srstn_en" is the core2 software rst enable. =1: enable it. =0: disable it.
8	RW	0x0	core1_srstn_en "core1_srstn_en" is the core1 software rst enable. =1: enable it. =0: disable it.
7:5	RO	0x0	reserved
4	RW	0x0	corepo_wrst_wfien "corepo_wrst_wfien" is the core power warm resetn wifen. It is the same as "core power dbg resetn wifen. =1: enable it. =0: disable it.
3	RW	0x0	corepo_srst_wfien "corepo_srst_wfien" is the core power software resetn wifen. =1: enable it. =0: disable it.

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Bit	Attr	Reset Value	Description
2	RW	0x0	core_wrst_wfien "core_wrstn_wfien" is the core warm resetn wifen. It is the same as "core_dbgrst_wifen". =1: enable it. =0: disable it.
1	RW	0x0	core_srstn_wfien "core_srstn_wfien" is the core software resetn wifen . =1: enable it. =0: disable it.
0	RO	0x0	warmrstn_en

TOPCRU_MISC_CON2

Address: Operational Base(0xFF100000) + offset (0x068C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	enable_ref_clk_testout_clk
14:13	RO	0x0	reserved
12	RW	0x0	enable_pd_vo_dwn_clk_en
11	RW	0x0	enable_pd_vi_dwn_clk_en
10	RW	0x0	enable_pd_vepu_dwn_clk_en
9	RW	0x0	enable_pd_vdpu_dwn_clk_en
8	RW	0x0	enable_pd_rga_dwn_clk_en
7	RW	0x0	enable_pd_php_dwn_clk_en
6	RW	0x0	enable_pd_npu_dwn_clk_en
5	RW	0x0	enable_pd_gpu_dwn_clk_en
4	RW	0x0	enable_pd_core_dwn_clk_en
3:0	RO	0x0	enable_pd_a53_dwn_clk_en bit0=0: enable pd_a53_dwn_clk_en[0] it is normal state. =1: disable it. bit1=0: enable pd_a53_dwn_clk_en[1] it is normal state. =1: disable it. bit2=0: enable pd_a53_dwn_clk_en[2] it is normal state. =1: disable it. bit3=0: enable pd_a53_dwn_clk_en[3] it is normal state. =1: disable it.

TOPCRU_FREQ_CAL

Address: Operational Base(0xFF100000) + offset (0x0694)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	freq_cal return the test_clkout pin's frequency value. the real freq is the value x 1000 Hz. For example: If the return val = 32. so the real frequency is 32K Hz.

2.5 PMU0CRU Register Description

2.5.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PMU0CRU_PMU0CLKSEL_CON00	0x0100	W	0x0040B71B	Internal clock select and division register 0

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Name	Offset	Size	Reset Value	Description
PMU0CRU_PMU0CLKSEL_CON01	0x0104	W	0x00000008	Internal clock select and division register 1
PMU0CRU_PMU0CLKSEL_CON02	0x0108	W	0x00000009	Internal clock select and division register 2
PMU0CRU_PMU0CLKSEL_CON03	0x010C	W	0x00000000	Internal clock select and division register 3
PMU0CRU_PMU0GATE_CON00	0x0180	W	0x00000000	Internal clock gate and division register 0
PMU0CRU_PMU0GATE_CON01	0x0184	W	0x00000000	Internal clock gate and division register 1
PMU0CRU_PMU0GATE_CON02	0x0188	W	0x00000000	Internal clock gate and division register 2
PMU0CRU_PMU0SOFTRST_CON00	0x0200	W	0x00000000	Internal clock reset register 0
PMU0CRU_PMU0SOFTRST_CON01	0x0204	W	0x00000000	Internal clock reset register 1
PMU0CRU_PMU0SOFTRST_CON02	0x0208	W	0x00000000	Internal clock reset register 2
PMU0CRU_MISC_CON0	0x0290	W	0x0000000A	MISC CRU Register
PMU0CRU_GRF_FREQ	0x0294	W	0x00000000	FREQ Register
PMU0CRU_IO32K_EXIST	0x0298	W	0x00000000	IO32K EXIST REGISTER

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.5.2 Detail Registers Description

PMU0CRU_PMU0CLKSEL_CON00

Address: Operational Base(0xFF110000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:0	RW	0x0040b71b	xin_osc0_div_div xin_osc0_div fraction division register. High 16-bit for numerator Low 16-bit for denominator

PMU0CRU_PMU0CLKSEL_CON01

Address: Operational Base(0xFF110000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4:3	RW	0x1	clk_pdpmu_200m_div_div Divide clk_pdpmu_200m_div by (div_con + 1).
2	RO	0x0	reserved
1:0	RW	0x0	clk_deepslow_sel clk_deepslow clock mux. 2'b00: xin_osc0_div 2'b01: xin_osc1_32k 2'b10: clk_pvtm_32k

PMU0CRU_PMU0CLKSEL_CON02

Address: Operational Base(0xFF110000) + offset (0x0108)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_mipidsiphy_ref_sel clk_mipidsiphy_ref clock mux. 1'b0: xin_osc0_mipidsiphy_g 1'b1: clk_24m_sscsrc
14:9	RO	0x00	reserved
8	RW	0x0	clk_usb2phy_ref_sel clk_usb2phy_ref clock mux. 1'b0: xin_osc0_usb2phy_g 1'b1: clk_24m_sscsrc
7	RW	0x0	clk_pipephy_ref_sel clk_pipephy_ref clock mux. 1'b0: clk_pipephy_div 1'b1: xin_osc0_pipephy_g
6	RO	0x0	reserved
5:0	RW	0x09	clk_pipephy_div_div DT50 division register. Divide clk_pipephy_div by (div_con + 1).

PMU0CRU_PMU0CLKSEL_CON03

Address: Operational Base(0xFF110000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clk_pmu0_i2c0_sel clk_pmu0_i2c0 clock mux. 2'b00: clk_200m_pmu 2'b01: xin_osc0_func 2'b10: clk_deepslow
13	RO	0x0	reserved
12:8	RW	0x00	clk_pmu0_i2c0_div Divide clk_pmu0_i2c0 by (div_con + 1).
7:0	RO	0x00	reserved

PMU0CRU_PMU0GATE_CON00

Address: Operational Base(0xFF110000) + offset (0x0180)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	xin_osc0_div_en xin_osc0_div clock gating control. When high, disable clock
14	RW	0x0	clk_pdpmu_200m_div_en clk_pdpmu_200m_div clock gating control. When high, disable clock
13	RW	0x0	busclk_pdpmu0_en busclk_pdpmu0 clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
12	RW	0x0	pclk_pmu0_sgrf_en pclk_pmu0_sgrf clock gating control. When high, disable clock
11	RW	0x0	pclk_pmu0_grf_en pclk_pmu0_grf clock gating control. When high, disable clock
10	RW	0x0	dbclk_pmu0_gpio0_en dbclk_pmu0_gpio0 clock gating control. When high, disable clock
9	RW	0x0	pclk_pmu0_gpio0_en pclk_pmu0_gpio0 clock gating control. When high, disable clock
8	RW	0x0	pclk_ioc_pmuio_en pclk_ioc_pmuio clock gating control. When high, disable clock
7	RW	0x0	clk_pmu0_pvtm_en clk_pmu0_pvtm clock gating control. When high, disable clock
6	RW	0x0	pclk_pmu0_pvtm_en pclk_pmu0_pvtm clock gating control. When high, disable clock
5	RW	0x0	clk_pmu0_32k_hp_timer_en clk_pmu0_32k_hp_timer clock gating control. When high, disable clock
4	RW	0x0	clk_pmu0_hp_timer_en clk_pmu0_hp_timer clock gating control. When high, disable clock
3	RW	0x0	pclk_pmu0_hp_timer_en pclk_pmu0_hp_timer clock gating control. When high, disable clock
2	RW	0x0	clk_pmu0_pmu_en clk_pmu0_pmu clock gating control. When high, disable clock
1	RW	0x0	pclk_pmu0_pmu_en pclk_pmu0_pmu clock gating control. When high, disable clock
0	RW	0x0	pclk_pmu0_cru_en pclk_pmu0_cru clock gating control. When high, disable clock

PMU0CRU_PMU0GATE_CON01

Address: Operational Base(0xFF110000) + offset (0x0184)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	pclk_pmu0_scrkeygen_en pclk_pmu0_scrkeygen clock gating control. When high, disable clock
0	RW	0x0	clk_ddr_fail_safe_en clk_ddr_fail_safe clock gating control. When high, disable clock

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PMU0CRU_PMU0GATE_CON02

Address: Operational Base(0xFF110000) + offset (0x0188)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	clk_pmu0_i2c0_en clk_pmu0_i2c0 clock gating control. When high, disable clock
8	RW	0x0	pclk_pmu0_i2c0_en pclk_pmu0_i2c0 clock gating control. When high, disable clock
7	RW	0x0	clk_mipidsiphy_ref_en clk_mipidsiphy_ref clock gating control. When high, disable clock
6	RW	0x0	xin_osc0_mipidsiphy_g_en xin_osc0_mipidsiphy_g clock gating control. When high, disable clock
5	RW	0x0	clk_usb2phy_ref_en clk_usb2phy_ref clock gating control. When high, disable clock
4	RW	0x0	xin_osc0_usb2phy_g_en xin_osc0_usb2phy_g clock gating control. When high, disable clock
3	RO	0x0	reserved
2	RW	0x0	clk_pipephy_ref_en clk_pipephy_ref clock gating control. When high, disable clock
1	RW	0x0	xin_osc0_pipephy_g_en xin_osc0_pipephy_g clock gating control. When high, disable clock
0	RW	0x0	clk_pipephy_div_en clk_pipephy_div clock gating control. When high, disable clock

PMU0CRU_PMU0SOFTRST_CON00

Address: Operational Base(0xFF110000) + offset (0x0200)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	presetn_pmu0_sgrf When high, reset relative logic
11	RW	0x0	presetn_pmu0_grf When high, reset relative logic
10	RW	0x0	dbresetn_pmu0_gpio0 When high, reset relative logic
9	RW	0x0	presetn_pmu0_gpio0 When high, reset relative logic
8	RW	0x0	presetn_ioc_pmuio When high, reset relative logic

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Bit	Attr	Reset Value	Description
7	RW	0x0	resetn_pmu0_pvtm When high, reset relative logic
6	RW	0x0	presetn_pmu0_pvtm When high, reset relative logic
5	RW	0x0	resetn_pmu0_32k_hp_timer When high, reset relative logic
4	RW	0x0	resetn_pmu0_hp_timer When high, reset relative logic
3	RW	0x0	presetn_pmu0_hp_timer When high, reset relative logic
2	RW	0x0	resetn_pmu0_pmu When high, reset relative logic
1	RW	0x0	presetn_pmu0_pmu When high, reset relative logic
0	RW	0x0	presetn_pmu0_cru When high, reset relative logic

PMU0CRU_PMU0SOFTRST_CON01

Address: Operational Base(0xFF110000) + offset (0x0204)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	presetn_pmu0_scrkeygen When high, reset relative logic
0	RW	0x0	resetn_ddr_fail_safe When high, reset relative logic

PMU0CRU_PMU0SOFTRST_CON02

Address: Operational Base(0xFF110000) + offset (0x0208)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	resetn_pmu0_i2c0 When high, reset relative logic
8	RW	0x0	presetn_pmu0_i2c0 When high, reset relative logic
7:0	RO	0x00	reserved

PMU0CRU_MISC_CON0

Address: Operational Base(0xFF110000) + offset (0x0290)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9	RW	0x0	grf_rst_the_32k_detect =1: means reset active , when reset active ,the exit value =0 , this means the 32k clk lost. If we want to test the 32k io is exit or lost. The frist step we should set this bit to 1 and then set it to 0. =0: means release reset.
8	RW	0x0	grf_xin_osc0_gate =1: means the ref clk for the 32k test is open. If we want to test the 32k we should open it. =0: means close the ref clk.
7:0	RW	0x0a	grf_32k_deviation the 32k clk detect deviation value, default =10. For example, if the vale = 10, so if we test the clk's freq value is from (32-10)K to (32+10) K, we think it is exist. if not the range. we think it is lost.

PMU0CRU_GRF_FREQ

Address: Operational Base(0xFF110000) + offset (0x0294)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	grf_freq_value return the 32k io test freq value . For example if the io freq is 32k. then the return value is 32.

PMU0CRU_IO32K_EXIST

Address: Operational Base(0xFF110000) + offset (0x0298)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	grf_exist =1: means the 32k io freq is exist. =0: means lost.

2.6 PMU1CRU Register Description

2.6.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PMU1CRU_CPLL_CON0	0x0040	W	0x0000307D	CPLL configuration register0
PMU1CRU_CPLL_CON1	0x0044	W	0x00001041	CPLL configuration register1
PMU1CRU_CPLL_CON2	0x0048	W	0x00000000	CPLL configuration register2
PMU1CRU_CPLL_CON3	0x004C	W	0x00000007	CPLL configuration register3
PMU1CRU_CPLL_CON4	0x0050	W	0x00007F00	CPLL configuration register4
PMU1CRU_PMU1CLKSEL_CON00	0x0100	W	0x00000004	Internal clock select and division register 0
PMU1CRU_PMU1CLKSEL_CON02	0x0108	W	0x00000080	Internal clock select and division register 2
PMU1CRU_PMU1CLKSEL_CON03	0x010C	W	0x0008007D	Internal clock select and division register 3
PMU1CRU_PMU1CLKSEL_CON04	0x0110	W	0x00000100	Internal clock select and division register 4
PMU1CRU_PMU1CLKSEL_CON06	0x0118	W	0x00000000	Internal clock select and division register 6
PMU1CRU_PMU1GATE_CON00	0x0180	W	0x00000000	Internal clock gate and division register 0

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Name	Offset	Size	Reset Value	Description
PMU1CRU_PMU1GATE_CON01	0x0184	W	0x00000000	Internal clock gate and division register 1
PMU1CRU_PMU1GATE_CON02	0x0188	W	0x00000000	Internal clock gate and division register 2
PMU1CRU_PMU1GATE_CON03	0x018C	W	0x00008000	Internal clock gate and division register 3
PMU1CRU_PMU1SOFTRST_CON00	0x0200	W	0x00000000	Internal clock reset register 0
PMU1CRU_PMU1SOFTRST_CON01	0x0204	W	0x00000000	Internal clock reset register 1
PMU1CRU_PMU1SOFTRST_CON02	0x0208	W	0x00000001	Internal clock reset register 2
PMU1CRU_SSGTBL0_3	0x0280	W	0x00000000	External wave table register0
PMU1CRU_SSGTBL4_7	0x0284	W	0x00000000	External wave table register1
PMU1CRU_SSGTBL8_11	0x0288	W	0x00000000	External wave table register2
PMU1CRU_SSGTBL12_15	0x028C	W	0x00000000	External wave table register3
PMU1CRU_SSGTBL16_19	0x0290	W	0x00000000	External wave table register4
PMU1CRU_SSGTBL20_23	0x0294	W	0x00000000	External wave table register5
PMU1CRU_SSGTBL24_27	0x0298	W	0x00000000	External wave table register6
PMU1CRU_SSGTBL28_31	0x029C	W	0x00000000	External wave table register7
PMU1CRU_SSGTBL32_35	0x02A0	W	0x00000000	External wave table register8
PMU1CRU_SSGTBL36_39	0x02A4	W	0x00000000	External wave table register9
PMU1CRU_SSGTBL40_43	0x02A8	W	0x00000000	External wave table register10
PMU1CRU_SSGTBL44_47	0x02AC	W	0x00000000	External wave table register11
PMU1CRU_SSGTBL48_51	0x02B0	W	0x00000000	External wave table register12
PMU1CRU_SSGTBL52_55	0x02B4	W	0x00000000	External wave table register13
PMU1CRU_SSGTBL56_59	0x02B8	W	0x00000000	External wave table register14
PMU1CRU_SSGTBL60_63	0x02BC	W	0x00000000	External wave table register15
PMU1CRU_SSGTBL64_67	0x02C0	W	0x00000000	External wave table register16
PMU1CRU_SSGTBL68_71	0x02C4	W	0x00000000	External wave table register17
PMU1CRU_SSGTBL72_75	0x02C8	W	0x00000000	External wave table register18
PMU1CRU_SSGTBL76_79	0x02CC	W	0x00000000	External wave table register19
PMU1CRU_SSGTBL80_83	0x02D0	W	0x00000000	External wave table register20
PMU1CRU_SSGTBL84_87	0x02D4	W	0x00000000	External wave table register21
PMU1CRU_SSGTBL88_91	0x02D8	W	0x00000000	External wave table register22
PMU1CRU_SSGTBL92_95	0x02DC	W	0x00000000	External wave table register23
PMU1CRU_SSGTBL96_99	0x02E0	W	0x00000000	External wave table register24
PMU1CRU_SSGTBL100_103	0x02E4	W	0x00000000	External wave table register25
PMU1CRU_SSGTBL104_107	0x02E8	W	0x00000000	External wave table register26
PMU1CRU_SSGTBL108_111	0x02EC	W	0x00000000	External wave table register27
PMU1CRU_SSGTBL112_115	0x02F0	W	0x00000000	External wave table register28
PMU1CRU_SSGTBL116_119	0x02F4	W	0x00000000	External wave table register29
PMU1CRU_SSGTBL120_123	0x02F8	W	0x00000000	External wave table register30
PMU1CRU_SSGTBL124_127	0x02FC	W	0x00000000	External wave table register31
PMU1CRU_PMU1MODE_CON00	0x0380	W	0x00000000	Internal clock select and division register 0

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Name	Offset	Size	Reset Value	Description
PMU1CRU_CM0_GATMASK_CON	0x0420	W	0x00000000	CM0 CORE GATEMASK CON
PMU1CRU_MISC_CON00	0x0684	W	0x00000000	MISC CRU CON00

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.6.2 Detail Registers Description

PMU1CRU_CPLL_CON0

Address: Operational Base(0xFF118000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	bypass PLL Bypass. FREF bypasses PLL to FOUTPOSTDIV 1'b0: No bypass 1'b1: Bypass
14:12	RW	0x3	postdiv1 First Post Divide Value, (1-7)
11:0	RW	0x07d	fbdiv Feedback Divide Value, valid divider settings are: [16, 2500] in integer mode [20, 500] in fractional mode Tips: No plus one operation

PMU1CRU_CPLL_CON1

Address: Operational Base(0xFF118000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pllpdsel PLL global power down source selection If pllpdsel == 1, PLL can be power down only by pllpd1, otherwise pll is power down when any one of refdiv/fbdiv/fracdiv is changed or pllpd0 is asserted
14	RW	0x0	pllpd1 PLL global power down request 1'b0: No power down 1'b1: Power down
13	RW	0x0	pllpd0 PLL global power down request 1'b0: No power down 1'b1: Power down
12	RW	0x1	dsmpd PLL delta sigma modulator enable 1'b0: Modulator is enable 1'b1: Modulator is disabled
11	RO	0x0	reserved
10	RW	0x0	pll_lock PLL lock status 1'b0: Unlock 1'b1: Lock

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Bit	Attr	Reset Value	Description
9	RO	0x0	reserved
8:6	RW	0x1	postdiv2 Second Post Divide Value, (1-7)
5:0	RW	0x01	refdiv Reference Clock Divide Value, (1-63)

PMU1CRU_CPLL_CON2

Address: Operational Base(0xFF118000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	fout4phasepd Power down 4-phase clocks and 2X, 3X, 4X clocks 1'b0: No power down 1'b1: Power down
26	RW	0x0	foutvcopd Power down buffered VCO clock 1'b0: No power down 1'b1: Power down
25	RW	0x0	foutpostdivpd Power down all outputs except for buffered VCO clock 1'b0: No power down 1'b1: Power down
24	RW	0x0	dacpd Power down quantization noise cancellation DAC 1'b0: No power down 1'b1: Power down
23:0	RW	0x000000	fracdiv Fractional part of feedback divide (fraction = FRAC/2^24)

PMU1CRU_CPLL_CON3

Address: Operational Base(0xFF118000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x00	ssmod_spread spread amplitude % = 0.1 * SPREAD[4: 0]
7:4	RW	0x0	ssmod_divval Divider required to set the modulation frequency
3	RW	0x0	ssmod_downspread Selects center spread or downs pread 1'b0: Down spread 1'b1: Center spread
2	RW	0x1	ssmod_reset Reset modulator state 1'b0: No reset 1'b1: Reset
1	RW	0x1	ssmod_disable_sscg Bypass SSMOD by module 1'b0: No bypass 1'b1: Bypass

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Bit	Attr	Reset Value	Description
0	RW	0x1	ssmod_bp Bypass SSMOD by integration 1'b0: No bypass 1'b1: Bypass

PMU1CRU_CPLL_CON4

Address: Operational Base(0xFF118000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x7f	ssmod_ext_maxaddr External wave table data inputs (0-255)
7:1	RO	0x00	reserved
0	RW	0x0	ssmod_sel_ext_wave select external wave 1'b0: No select ext_wave 1'b1: Select ext_wave

PMU1CRU_PMU1CLKSEL_CON00

Address: Operational Base(0xFF118000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4:0	RW	0x04	clk_200m_pmu_div Divide clk_200m_pmu by (div_con + 1).

PMU1CRU_PMU1CLKSEL_CON02

Address: Operational Base(0xFF118000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:6	RW	0x2	sclk_pmu1_uart0_sel sclk_pmu1_uart0 clock mux. 2'b00: clk_pmu1_uart0_src 2'b01: clk_pmu1_uart0_frac 2'b10: xin_osc0_func
5:4	RO	0x0	reserved
3:0	RW	0x0	clk_pmu1_uart0_src_div Divide clk_pmu1_uart0_src by (div_con + 1).

PMU1CRU_PMU1CLKSEL_CON03

Address: Operational Base(0xFF118000) + offset (0x010C)

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Bit	Attr	Reset Value	Description
31:0	RW	0x0008007d	clk_pmu1_uart0_frac_div clk_pmu1_uart0_frac fraction division register. High 16-bit for numerator Low 16-bit for denominator

PMU1CRU_PMU1CLKSEL_CON04

Address: Operational Base(0xFF118000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clk_pmu1_pwm0_sel clk_pmu1_pwm0 clock mux. 2'b00: clk_200m_pmu 2'b01: xin_osc0_func 2'b10: clk_deepslow
13:10	RO	0x0	reserved
9:8	RW	0x1	clk_pmu1_pwm0_div Divide clk_pmu1_pwm0 by (div_con + 1).
7:6	RW	0x0	clk_pmu1_spi0_sel clk_pmu1_spi0 clock mux. 2'b00: clk_200m_pmu 2'b01: xin_osc0_func 2'b10: clk_deepslow
5:2	RO	0x0	reserved
1:0	RW	0x0	clk_pmu1_spi0_div Divide clk_pmu1_spi0 by (div_con + 1).

PMU1CRU_PMU1CLKSEL_CON06

Address: Operational Base(0xFF118000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RW	0x0	clk_testout_pmu1_sel clk_testout_pmu1 clock mux. 3'b000: clk_deepslow 3'b001: 1'b0 3'b010: clk_cpll_mux_from_pmu1 3'b011: 1'b0 3'b100: busclk_pdpmu0 3'b101: 1'b0 3'b110: 1'b0 3'b111: 1'b0
12:11	RO	0x0	reserved
10:8	RW	0x0	clk_testout_pmu1_div Divide clk_testout_pmu1 by (div_con + 1).
7:0	RO	0x00	reserved

PMU1CRU_PMU1GATE_CON00

Address: Operational Base(0xFF118000) + offset (0x0180)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pclk_pdpmu1_to_peri_en pclk_pdpmu1_to_peri clock gating control. When high, disable clock
14:11	RO	0x0	reserved
10	RW	0x0	sclk_pmu1_uart0_en sclk_pmu1_uart0 clock gating control. When high, disable clock
9	RW	0x0	clk_pmu1_uart0_frac_en clk_pmu1_uart0_frac clock gating control. When high, disable clock
8	RW	0x0	clk_pmu1_uart0_en clk_pmu1_uart0_src clock gating control. When high, disable clock
7	RW	0x0	pclk_pmu1_uart0_en pclk_pmu1_uart0 clock gating control. When high, disable clock
6:5	RO	0x0	reserved
4	RW	0x0	pclk_pmu1_biu_en pclk_pmu1_biu clock gating control. When high, disable clock
3	RW	0x0	hclk_pmu1_biu_en hclk_pmu1_biu clock gating control. When high, disable clock
2	RW	0x0	hclk_pmu1_mem_en hclk_pmu1_mem clock gating control. When high, disable clock
1	RW	0x0	clk_200m_pmu_en clk_200m_pmu clock gating control. When high, disable clock
0	RW	0x0	pclk_pmu1_cru_en pclk_pmu1_cru clock gating control. When high, disable clock

PMU1CRU_PMU1GATE_CON01

Address: Operational Base(0xFF118000) + offset (0x0184)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	clk_pmu1_wfi_en clk_pmu1_wifi clock gating control. When high, disable clock
5	RW	0x0	clk_capture_pmu1_pwm0_en clk_capture_pmu1_pwm0 clock gating control. When high, disable clock
4	RW	0x0	clk_pmu1_pwm0_en clk_pmu1_pwm0 clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
3	RW	0x0	pclk_pmu1_pwm0_en pclk_pmu1_pwm0 clock gating control. When high, disable clock
2	RW	0x0	sclk_in_pmu1_spi0_en sclk_in_pmu1_spi0 clock gating control. When high, disable clock
1	RW	0x0	clk_pmu1_spi0_en clk_pmu1_spi0 clock gating control. When high, disable clock
0	RW	0x0	pclk_pmu1_spi0_en pclk_pmu1_spi0 clock gating control. When high, disable clock

PMU1CRU_PMU1GATE_CON02

Address: Operational Base(0xFF118000) + offset (0x0188)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x0	clk_pmu1_wdtns_en clk_pmu1_wdtns clock gating control. When high, disable clock
3	RW	0x0	pclk_pmu1_wdtns_en pclk_pmu1_wdtns clock gating control. When high, disable clock
2	RO	0x0	reserved
1	RW	0x0	clk_pmu1_cm0_rtc_en clk_pmu1_cm0_rtc clock gating control. When high, disable clock
0	RW	0x0	fclk_pmu1_cm0_core_en fclk_pmu1_cm0_core clock gating control. When high, disable clock

PMU1CRU_PMU1GATE_CON03

Address: Operational Base(0xFF118000) + offset (0x018C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	clk_testout_pmu1_en clk_testout_pmu1 clock gating control. When high, disable clock
14:9	RO	0x00	reserved
8	RW	0x0	pclk_pmu1_mailbox_en pclk_pmu1_mailbox clock gating control. When high, disable clock
7:0	RO	0x00	reserved

PMU1CRU_PMU1SOFTRST_CON00

Address: Operational Base(0xFF118000) + offset (0x0200)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10	RW	0x0	sresetn_pmu1_uart0 When high, reset relative logic
9:8	RO	0x0	reserved
7	RW	0x0	presetn_pmu1_uart0 When high, reset relative logic
6:5	RO	0x0	reserved
4	RW	0x0	presetn_pmu1_biu When high, reset relative logic
3	RW	0x0	hresetn_pmu1_biu When high, reset relative logic
2	RW	0x0	hresetn_pmu1_mem When high, reset relative logic
1	RO	0x0	reserved
0	RW	0x0	presetn_pmu1_cru When high, reset relative logic

PMU1CRU_PMU1SOFTRST_CON01

Address: Operational Base(0xFF118000) + offset (0x0204)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x0	resetn_pmu1_pwm0 When high, reset relative logic
3	RW	0x0	presetn_pmu1_pwm0 When high, reset relative logic
2	RO	0x0	reserved
1	RW	0x0	resetn_pmu1_spi0 When high, reset relative logic
0	RW	0x0	presetn_pmu1_spi0 When high, reset relative logic

PMU1CRU_PMU1SOFTRST_CON02

Address: Operational Base(0xFF118000) + offset (0x0208)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	presetn_pmu1_mailbox When high, reset relative logic
7:5	RO	0x0	reserved
4	RW	0x0	resetn_pmu1_wdtns When high, reset relative logic
3	RW	0x0	presetn_pmu1_wdtns When high, reset relative logic

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Bit	Attr	Reset Value	Description
2	RW	0x0	tresetn_pmu1_cm0_jtag When high, reset relative logic
1	RO	0x0	reserved
0	RW	0x1	fresetn_pmu1_cm0_core When high, reset relative logic

PMU1CRU_SSGTBL0_3

Address: Operational Base(0xFF118000) + offset (0x0280)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl0_3 Extern wave table 0-3 7-0: table0 15-8: table1 23-16: table2 31-24: table3

PMU1CRU_SSGTBL4_7

Address: Operational Base(0xFF118000) + offset (0x0284)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl4_7 Extern wave table 4-7 7-0: table4 15-8: table5 23-16: table6 31-24: table7

PMU1CRU_SSGTBL8_11

Address: Operational Base(0xFF118000) + offset (0x0288)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl8_11 Extern wave table 8-11 7-0: table8 15-8: table9 23-16: table10 31-24: table11

PMU1CRU_SSGTBL12_15

Address: Operational Base(0xFF118000) + offset (0x028C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl12_15 Extern wave table 12-15 7-0: table12 15-8: table13 23-16: table14 31-24: table15

PMU1CRU_SSGTBL16_19

Address: Operational Base(0xFF118000) + offset (0x0290)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl16_19 Extern wave table 16-19 7-0: table16 15-8: table17 23-16: table18 31-24: table19

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PMU1CRU_SSGTBL20_23

Address: Operational Base(0xFF118000) + offset (0x0294)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl20_23 Extern wave table 20-23 7-0: table20 15-8: table21 23-16: table22 31-24: table23

PMU1CRU_SSGTBL24_27

Address: Operational Base(0xFF118000) + offset (0x0298)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl24_27 Extern wave table 24-27 7-0: table24 15-8: table25 23-16: table26 31-24: table27

PMU1CRU_SSGTBL28_31

Address: Operational Base(0xFF118000) + offset (0x029C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl28_31 Extern wave table 28-31 7-0: table28 15-8: table29 23-16: table30 31-24: table31

PMU1CRU_SSGTBL32_35

Address: Operational Base(0xFF118000) + offset (0x02A0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl32_35 Extern wave table 32-35 7-0: table32 15-8: table33 23-16: table34 31-24: table35

PMU1CRU_SSGTBL36_39

Address: Operational Base(0xFF118000) + offset (0x02A4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl36_39 Extern wave table 36-39 7-0: table36 15-8: table37 23-16: table38 31-24: table39

PMU1CRU_SSGTBL40_43

Address: Operational Base(0xFF118000) + offset (0x02A8)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl40_43 Extern wave table 40-43 7-0: table40 15-8: table41 23-16: table42 31-24: table43

PMU1CRU_SSGTBL44_47

Address: Operational Base(0xFF118000) + offset (0x02AC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl44_47 Extern wave table 44-47 7-0: table44 15-8: table45 23-16: table46 31-24: table47

PMU1CRU_SSGTBL48_51

Address: Operational Base(0xFF118000) + offset (0x02B0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl48_51 Extern wave table 48-51 7-0: table48 15-8: table49 23-16: table50 31-24: table51

PMU1CRU_SSGTBL52_55

Address: Operational Base(0xFF118000) + offset (0x02B4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl52_55 Extern wave table 52-55 7-0: table52 15-8: table53 23-16: table54 31-24: table55

PMU1CRU_SSGTBL56_59

Address: Operational Base(0xFF118000) + offset (0x02B8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl56_59 Extern wave table 56-59 7-0: table56 15-8: table57 23-16: table58 31-24: table59

PMU1CRU_SSGTBL60_63

Address: Operational Base(0xFF118000) + offset (0x02BC)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl60_63 Extern wave table 60-63 7-0: table60 15-8: table61 23-16: table62 31-24: table63

PMU1CRU_SSGTBL64_67

Address: Operational Base(0xFF118000) + offset (0x02C0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl64_67 Extern wave table 64-67 7-0: table64 15-8: table65 23-16: table66 31-24: table67

PMU1CRU_SSGTBL68_71

Address: Operational Base(0xFF118000) + offset (0x02C4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl68_71 Extern wave table 68-71 7-0: table68 15-8: table69 23-16: table70 31-24: table71

PMU1CRU_SSGTBL72_75

Address: Operational Base(0xFF118000) + offset (0x02C8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl72_75 Extern wave table 72-75 7-0: table72 15-8: table73 23-16: table74 31-24: table75

PMU1CRU_SSGTBL76_79

Address: Operational Base(0xFF118000) + offset (0x02CC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl76_79 Extern wave table 76-79 7-0: table76 15-8: table77 23-16: table78 31-24: table79

PMU1CRU_SSGTBL80_83

Address: Operational Base(0xFF118000) + offset (0x02D0)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl80_83 Extern wave table 76-79 7-0: table80 15-8: table81 23-16: table82 31-24: table83

PMU1CRU_SSGTBL84_87

Address: Operational Base(0xFF118000) + offset (0x02D4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl84_87 Extern wave table 84-87 7-0: table84 15-8: table85 23-16: table86 31-24: table87

PMU1CRU_SSGTBL88_91

Address: Operational Base(0xFF118000) + offset (0x02D8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl88_91 Extern wave table 88-91 7-0: table88 15-8: table89 23-16: table90 31-24: table91

PMU1CRU_SSGTBL92_95

Address: Operational Base(0xFF118000) + offset (0x02DC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl92_95 Extern wave table 92-95 7-0: table92 15-8: table93 23-16: table94 31-24: table95

PMU1CRU_SSGTBL96_99

Address: Operational Base(0xFF118000) + offset (0x02E0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl96_99 Extern wave table 96-99 7-0: table96 15-8: table97 23-16: table98 31-24: table99

PMU1CRU_SSGTBL100_103

Address: Operational Base(0xFF118000) + offset (0x02E4)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl100_103 Extern wave table 100-103 7-0: table100 15-8: table101 23-16: table102 31-24: table103

PMU1CRU_SSGTBL104_107

Address: Operational Base(0xFF118000) + offset (0x02E8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl104_107 Extern wave table 104-107 7-0: table104 15-8: table105 23-16: table106 31-24: table107

PMU1CRU_SSGTBL108_111

Address: Operational Base(0xFF118000) + offset (0x02EC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl108_111 Extern wave table 108-111 7-0: table108 15-8: table109 23-16: table110 31-24: table111

PMU1CRU_SSGTBL112_115

Address: Operational Base(0xFF118000) + offset (0x02F0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl112_115 Extern wave table 112-115 7-0: table112 15-8: table113 23-16: table114 31-24: table115

PMU1CRU_SSGTBL116_119

Address: Operational Base(0xFF118000) + offset (0x02F4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl116_119 Extern wave table 116-119 7-0: table116 15-8: table117 23-16: table118 31-24: table119

PMU1CRU_SSGTBL120_123

Address: Operational Base(0xFF118000) + offset (0x02F8)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl120_123 Extern wave table 120-123 7-0: table120 15-8: table121 23-16: table122 31-24: table123

PMU1CRU_SSGTBL124_127

Address: Operational Base(0xFF118000) + offset (0x02FC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl124_127 Extern wave table 124-127 7-0: table124 15-8: table125 23-16: table126 31-24: table127

PMU1CRU_PMU1MODE_CON00

Address: Operational Base(0xFF118000) + offset (0x0380)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1:0	RW	0x0	clk_cpll_mode clk_cpll_mux_from_pmu1 clock mux. 2'b00: xin_osc0_func 2'b01: clk_cpll 2'b10: clk_deepslow

PMU1CRU_CM0_GATMASK_CON

Address: Operational Base(0xFF118000) + offset (0x0420)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	sgrf_con_mcu_sclk_cm0s_en =0: disable the output clk gating,but if the ip dclk_en is 1 the output clk can also be gating. =1: force the output clk gating. the output clk is "sclk".
2	RW	0x0	sgrf_con_mcu_hclk_cm0s_en =0: disable the output clk gating,but if the ip dclk_en is 1 the output clk can also be gating. =1: force the output clk gating. the output clk is "hclk".
1:0	RW	0x0	sgrf_con_mcu_dclk_cm0s_en =0: disable the output clk gating,but if the ip dclk_en is 1 the output clk can also be gating. =1: force the output clk gating. the output clk is "dclk".

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PMU1CRU_MISC_CON00

Address: Operational Base(0xFF118000) + offset (0x0684)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	enable_pd_pmu1_clk_en =0: disable the pd_pmu1_dwn_clk_en , it means the i_pd_pmu1_dwn_clk_en keep 0. =1: enable it.

2.7 DDRCRU Register Description

2.7.1 Registers Summary

Name	Offset	Size	Reset Value	Description
DDRCRU_DDRCLKSEL_CON01	0x0104	W	0x00000B05	Internal clock select and division register 1
DDRCRU_DDRGATE_CON00	0x0180	W	0x00000000	Internal clock gate and division register 0
DDRCRU_DDRGATE_CON01	0x0184	W	0x00000000	Internal clock gate and division register 1
DDRCRU_DDRSOFTRST_CON00	0x0200	W	0x00000000	Internal clock reset register 0
DDRCRU_DDRSOFTRST_CON01	0x0204	W	0x00000000	Internal clock reset register 1
DDRCRU_MISC_CON0	0x0684	W	0x00000000	MISC CRU Register

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.7.2 Detail Registers Description

DDRCRU_DDRCLKSEL_CON01

Address: Operational Base(0xFF120000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x0b	pclk_ddr_div Divide pclk_ddr by (div_con + 1).
7:4	RO	0x0	reserved
3:0	RW	0x5	clk_msch_brg_biu_div Divide clk_msch_brg_biu by (div_con + 1).

DDRCRU_DDRGATE_CON00

Address: Operational Base(0xFF120000) + offset (0x0180)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10	RW	0x0	pclk_ddr_dma2ddr_en pclk_ddr_dma2ddr clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
9	RW	0x0	pclk_ddr_dfictl_en pclk_ddr_dfictl clock gating control. When high, disable clock
8	RW	0x0	pclk_ddr_phy_en pclk_ddr_phy clock gating control. When high, disable clock
7	RO	0x0	reserved
6	RW	0x0	pclk_ddr_hwlp_en pclk_ddr_hwlp clock gating control. When high, disable clock
5	RW	0x0	pclk_msch_biu_en pclk_msch_biu clock gating control. When high, disable clock
4	RW	0x0	clk_msch_brg_biu_en clk_msch_brg_biu clock gating control. When high, disable clock
3	RW	0x0	pclk_ddr_en pclk_ddr clock gating control. When high, disable clock
2	RW	0x0	clk_deepslow_to_subddr_en clk_deepslow_to_subddr clock gating control. When high, disable clock
1	RW	0x0	xin_osc0_func_to_subddr_en xin_osc0_func_to_subddr clock gating control. When high, disable clock
0	RW	0x0	clk_gpll_mux_to_subddr_en clk_gpll_mux_to_subddr clock gating control. When high, disable clock

DDRCRU_DDRGATE_CON01

Address: Operational Base(0xFF120000) + offset (0x0184)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x0	pclk_subddr_cru_en pclk_subddr_cru clock gating control. When high, disable clock
3	RW	0x0	pclk_ddr_cru_en pclk_ddr_cru clock gating control. When high, disable clock
2	RW	0x0	pclk_ddr_grf_en pclk_ddr_grf clock gating control. When high, disable clock
1	RW	0x0	tmclk_ddr_mon_en tmclk_ddr_mon clock gating control. When high, disable clock
0	RW	0x0	pclk_ddr_mon_en pclk_ddr_mon clock gating control. When high, disable clock

DDRCRU_DDRSOFTRST_CON00

Address: Operational Base(0xFF120000) + offset (0x0200)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10	RW	0x0	presetn_ddr_dma2ddr When high, reset relative logic
9	RW	0x0	presetn_ddr_dfictl When high, reset relative logic
8	RW	0x0	presetn_ddr_phy When high, reset relative logic
7	RO	0x0	reserved
6	RW	0x0	presetn_ddr_hwlp When high, reset relative logic
5	RW	0x0	presetn_msch_biu When high, reset relative logic
4	RW	0x0	resetn_msch_brg_biu When high, reset relative logic
3:0	RO	0x0	reserved

DDRCRU_DDRSOFTRST_CON01

Address: Operational Base(0xFF120000) + offset (0x0204)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x0	presetn_subddr_cru When high, reset relative logic
3	RW	0x0	presetn_ddr_cru When high, reset relative logic
2	RW	0x0	presetn_ddr_grf When high, reset relative logic
1	RW	0x0	tmresetn_ddr_mon When high, reset relative logic
0	RW	0x0	presetn_ddr_mon When high, reset relative logic

DDRCRU_MISC_CON0

Address: Operational Base(0xFF120000) + offset (0x0684)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	enable_pd_ddr_clk_en =0: enable the pd_ddr_clk_en signal when power active. =1: disable the pd_ddr_clk_en signal.

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2.8 SUBDDRCRU Register Description

2.8.1 Registers Summary

Name	Offset	Size	Reset Value	Description
SUBDDRCRU_DPLL_CON0	0x0020	W	0x00003064	DPLL configuration register0
SUBDDRCRU_DPLL_CON1	0x0024	W	0x00001081	DPLL configuration register1
SUBDDRCRU_DPLL_CON2	0x0028	W	0x00000000	DPLL configuration register2
SUBDDRCRU_DPLL_CON3	0x002C	W	0x00000007	DPLL configuration register3
SUBDDRCRU_DPLL_CON4	0x0030	W	0x00007F00	DPLL configuration register4
SUBDDRCRU_SUBDDRCLKSEL_CON00	0x0100	W	0x00000000	Internal clock select and division register 0
SUBDDRCRU_SUBDDRGATE_CON00	0x0180	W	0x00008000	Internal clock gate and division register 0
SUBDDRCRU_SUBDDRSOFTRST_CON00	0x0200	W	0x00000000	Internal clock reset register 0
SUBDDRCRU_SSGTBL0_3	0x0280	W	0x00000000	External wave table register0
SUBDDRCRU_SSGTBL4_7	0x0284	W	0x00000000	External wave table register1
SUBDDRCRU_SSGTBL8_11	0x0288	W	0x00000000	External wave table register2
SUBDDRCRU_SSGTBL12_15	0x028C	W	0x00000000	External wave table register3
SUBDDRCRU_SSGTBL16_19	0x0290	W	0x00000000	External wave table register4
SUBDDRCRU_SSGTBL20_23	0x0294	W	0x00000000	External wave table register5
SUBDDRCRU_SSGTBL24_27	0x0298	W	0x00000000	External wave table register6
SUBDDRCRU_SSGTBL28_31	0x029C	W	0x00000000	External wave table register7
SUBDDRCRU_SSGTBL32_35	0x02A0	W	0x00000000	External wave table register8
SUBDDRCRU_SSGTBL36_39	0x02A4	W	0x00000000	External wave table register9
SUBDDRCRU_SSGTBL40_43	0x02A8	W	0x00000000	External wave table register10
SUBDDRCRU_SSGTBL44_47	0x02AC	W	0x00000000	External wave table register11
SUBDDRCRU_SSGTBL48_51	0x02B0	W	0x00000000	External wave table register12
SUBDDRCRU_SSGTBL52_55	0x02B4	W	0x00000000	External wave table register13
SUBDDRCRU_SSGTBL56_59	0x02B8	W	0x00000000	External wave table register14
SUBDDRCRU_SSGTBL60_63	0x02BC	W	0x00000000	External wave table register15
SUBDDRCRU_SSGTBL64_67	0x02C0	W	0x00000000	External wave table register16
SUBDDRCRU_SSGTBL68_71	0x02C4	W	0x00000000	External wave table register17
SUBDDRCRU_SSGTBL72_75	0x02C8	W	0x00000000	External wave table register18
SUBDDRCRU_SSGTBL76_79	0x02CC	W	0x00000000	External wave table register19

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Name	Offset	Size	Reset Value	Description
SUBDDRCRU_SSGTBL80_83	0x02D0	W	0x00000000	External wave table register20
SUBDDRCRU_SSGTBL84_87	0x02D4	W	0x00000000	External wave table register21
SUBDDRCRU_SSGTBL88_91	0x02D8	W	0x00000000	External wave table register22
SUBDDRCRU_SSGTBL92_95	0x02DC	W	0x00000000	External wave table register23
SUBDDRCRU_SSGTBL96_99	0x02E0	W	0x00000000	External wave table register24
SUBDDRCRU_SSGTBL100_103	0x02E4	W	0x00000000	External wave table register25
SUBDDRCRU_SSGTBL104_107	0x02E8	W	0x00000000	External wave table register26
SUBDDRCRU_SSGTBL108_111	0x02EC	W	0x00000000	External wave table register27
SUBDDRCRU_SSGTBL112_115	0x02F0	W	0x00000000	External wave table register28
SUBDDRCRU_SSGTBL116_119	0x02F4	W	0x00000000	External wave table register29
SUBDDRCRU_SSGTBL120_123	0x02F8	W	0x00000000	External wave table register30
SUBDDRCRU_SSGTBL124_127	0x02FC	W	0x00000000	External wave table register31
SUBDDRCRU_SUBDDRMODE_CON00	0x0380	W	0x00000000	Internal clock select and division register 0

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.8.2 Detail Registers Description

SUBDDRCRU_DPLL_CON0

Address: Operational Base(0xFF128000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	bypass PLL Bypass. FREF bypasses PLL to FOUTPOSTDIV 1'b0: No bypass 1'b1: Bypass
14:12	RW	0x3	postdiv1 First Post Divide Value, (1-7)
11:0	RW	0x064	fbdiv Feedback Divide Value, valid divider settings are: [16, 2500] in integer mode [20, 500] in fractional mode Tips: No plus one operation

SUBDDRCRU_DPLL_CON1

Address: Operational Base(0xFF128000) + offset (0x0024)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pllpdsel PLL global power down source selection If pllpdsel == 1, PLL can be power down only by pllpd1, otherwise pll is power down when any one of refdiv/fbdiv/fracdiv is changed or pllpd0 is asserted
14	RW	0x0	pllpd1 PLL global power down request 1'b0: No power down 1'b1: Power down
13	RW	0x0	pllpd0 PLL global power down request 1'b0: No power down 1'b1: Power down
12	RW	0x1	dsmpd PLL delta sigma modulator enable 1'b0: Modulator is enable 1'b1: Modulator is disabled
11	RO	0x0	reserved
10	RW	0x0	pll_lock PLL lock status 1'b0: Unlock 1'b1: Lock
9	RO	0x0	reserved
8:6	RW	0x2	postdiv2 Second Post Divide Value, (1-7)
5:0	RW	0x01	refdiv Reference Clock Divide Value, (1-63)

SUBDDRCRU_DPLL_CON2

Address: Operational Base(0xFF128000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	fout4phasepd Power down 4-phase clocks and 2X, 3X, 4X clocks 1'b0: No power down 1'b1: Power down
26	RW	0x0	foutvcopd Power down buffered VCO clock 1'b0: No power down 1'b1: Power down
25	RW	0x0	foutpostdivpd Power down all outputs except for buffered VCO clock 1'b0: No power down 1'b1: Power down
24	RW	0x0	dacpd Power down quantization noise cancellation DAC 1'b0: No power down 1'b1: Power down
23:0	RW	0x000000	fracdiv Fractional part of feedback divide (fraction = FRAC/2^24)

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SUBDDRCRU_DPLL_CON3

Address: Operational Base(0xFF128000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x00	ssmod_spread spread amplitude % = 0.1 * SPREAD[4: 0]
7:4	RW	0x0	ssmod_divval Divider required to set the modulation frequency
3	RW	0x0	ssmod_downspread Selects center spread or downs pread 1'b0: Down spread 1'b1: Center spread
2	RW	0x1	ssmod_reset Reset modulator state 1'b0: No reset 1'b1: Reset
1	RW	0x1	ssmod_disable_sscg Bypass SSMOD by module 1'b0: No bypass 1'b1: Bypass
0	RW	0x1	ssmod_bp Bypass SSMOD by integration 1'b0: No bypass 1'b1: Bypass

SUBDDRCRU_DPLL_CON4

Address: Operational Base(0xFF128000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x7f	ssmod_ext_maxaddr External wave table data inputs (0-255)
7:1	RO	0x00	reserved
0	RW	0x0	ssmod_sel_ext_wave select external wave 1'b0: No select ext_wave 1'b1: Select ext_wave

SUBDDRCRU_SUBDDRCLKSEL_CON00

Address: Operational Base(0xFF128000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15	RW	0x0	clk_testout_subddr_sel clk_testout_subddr clock mux. 1'b0: clk_ddr 1'b1: pclk_ddr
14:10	RO	0x00	reserved
9:8	RW	0x0	clk_testout_subddr_div Divide clk_testout_subddr by (div_con + 1).
7	RW	0x0	clk_ddr_sel clk_ddr clock mux. 1'b0: clk_dpll_mux 1'b1: clk_gpll_mux_to_subddr
6:0	RO	0x00	reserved

SUBDDRCRU_SUBDDRGATE_CON00

Address: Operational Base(0xFF128000) + offset (0x0180)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	clk_testout_subddr_en clk_testout_subddr clock gating control. When high, disable clock
14:10	RO	0x00	reserved
9	RW	0x0	aclk_ddr_dma2ddr_en aclk_ddr_dma2ddr clock gating control. When high, disable clock
8	RW	0x0	aclk_ddr_split_en aclk_ddr_split clock gating control. When high, disable clock
7	RW	0x0	clk_ddr_mon_en clk_ddr_mon clock gating control. When high, disable clock
6	RW	0x0	clk_ddr_scramble_en clk_ddr_scramble clock gating control. When high, disable clock
5	RW	0x0	clk_ddr_dfictl_en clk_ddr_dfictl clock gating control. When high, disable clock
4	RW	0x0	clk1x_ddr_phy_en clk1x_ddr_phy clock gating control. When high, disable clock
3:2	RO	0x0	reserved
1	RW	0x0	clk_msch_biu_en clk_msch_biu clock gating control. When high, disable clock
0	RW	0x0	clk_ddr_en clk_ddr clock gating control. When high, disable clock

SUBDDRCRU_SUBDDRSOFTRST_CON00

Address: Operational Base(0xFF128000) + offset (0x0200)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	aresetn_ddr_dma2ddr When high, reset relative logic
8	RW	0x0	aresetn_ddr_split When high, reset relative logic
7	RW	0x0	resetn_ddr_mon When high, reset relative logic
6	RW	0x0	resetn_ddr_scramble When high, reset relative logic
5	RW	0x0	resetn_ddr_dfictl When high, reset relative logic
4	RW	0x0	resetn_ddr_phy When high, reset relative logic
3:2	RO	0x0	reserved
1	RW	0x0	resetn_msch_biu When high, reset relative logic
0	RO	0x0	reserved

SUBDDRCRU_SSGTBL0_3

Address: Operational Base(0xFF128000) + offset (0x0280)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl0_3 Extern wave table 0-3 7-0: table0 15-8: table1 23-16: table2 31-24: table3

SUBDDRCRU_SSGTBL4_7

Address: Operational Base(0xFF128000) + offset (0x0284)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl4_7 Extern wave table 4-7 7-0: table4 15-8: table5 23-16: table6 31-24: table7

SUBDDRCRU_SSGTBL8_11

Address: Operational Base(0xFF128000) + offset (0x0288)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl8_11 Extern wave table 8-11 7-0: table8 15-8: table9 23-16: table10 31-24: table11

SUBDDRCRU_SSGTBL12_15

Address: Operational Base(0xFF128000) + offset (0x028C)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl12_15 Extern wave table 12-15 7-0: table12 15-8: table13 23-16: table14 31-24: table15

SUBDDRCRU_SSGTBL16_19

Address: Operational Base(0xFF128000) + offset (0x0290)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl16_19 Extern wave table 16-19 7-0: table16 15-8: table17 23-16: table18 31-24: table19

SUBDDRCRU_SSGTBL20_23

Address: Operational Base(0xFF128000) + offset (0x0294)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl20_23 Extern wave table 20-23 7-0: table20 15-8: table21 23-16: table22 31-24: table23

SUBDDRCRU_SSGTBL24_27

Address: Operational Base(0xFF128000) + offset (0x0298)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl24_27 Extern wave table 24-27 7-0: table24 15-8: table25 23-16: table26 31-24: table27

SUBDDRCRU_SSGTBL28_31

Address: Operational Base(0xFF128000) + offset (0x029C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl28_31 Extern wave table 28-31 7-0: table28 15-8: table29 23-16: table30 31-24: table31

SUBDDRCRU_SSGTBL32_35

Address: Operational Base(0xFF128000) + offset (0x02A0)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl32_35 Extern wave table 32-35 7-0: table32 15-8: table33 23-16: table34 31-24: table35

SUBDDRCRU_SSGTBL36_39

Address: Operational Base(0xFF128000) + offset (0x02A4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl36_39 Extern wave table 36-39 7-0: table36 15-8: table37 23-16: table38 31-24: table39

SUBDDRCRU_SSGTBL40_43

Address: Operational Base(0xFF128000) + offset (0x02A8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl40_43 Extern wave table 40-43 7-0: table40 15-8: table41 23-16: table42 31-24: table43

SUBDDRCRU_SSGTBL44_47

Address: Operational Base(0xFF128000) + offset (0x02AC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl44_47 Extern wave table 44-47 7-0: table44 15-8: table45 23-16: table46 31-24: table47

SUBDDRCRU_SSGTBL48_51

Address: Operational Base(0xFF128000) + offset (0x02B0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl48_51 Extern wave table 48-51 7-0: table48 15-8: table49 23-16: table50 31-24: table51

SUBDDRCRU_SSGTBL52_55

Address: Operational Base(0xFF128000) + offset (0x02B4)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl52_55 Extern wave table 52-55 7-0: table52 15-8: table53 23-16: table54 31-24: table55

SUBDDRCRU_SSGTBL56_59

Address: Operational Base(0xFF128000) + offset (0x02B8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl56_59 Extern wave table 56-59 7-0: table56 15-8: table57 23-16: table58 31-24: table59

SUBDDRCRU_SSGTBL60_63

Address: Operational Base(0xFF128000) + offset (0x02BC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl60_63 Extern wave table 60-63 7-0: table60 15-8: table61 23-16: table62 31-24: table63

SUBDDRCRU_SSGTBL64_67

Address: Operational Base(0xFF128000) + offset (0x02C0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl64_67 Extern wave table 64-67 7-0: table64 15-8: table65 23-16: table66 31-24: table67

SUBDDRCRU_SSGTBL68_71

Address: Operational Base(0xFF128000) + offset (0x02C4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl68_71 Extern wave table 68-71 7-0: table68 15-8: table69 23-16: table70 31-24: table71

SUBDDRCRU_SSGTBL72_75

Address: Operational Base(0xFF128000) + offset (0x02C8)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl72_75 Extern wave table 72-75 7-0: table72 15-8: table73 23-16: table74 31-24: table75

SUBDDRCRU_SSGTBL76_79

Address: Operational Base(0xFF128000) + offset (0x02CC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl76_79 Extern wave table 76-79 7-0: table76 15-8: table77 23-16: table78 31-24: table79

SUBDDRCRU_SSGTBL80_83

Address: Operational Base(0xFF128000) + offset (0x02D0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl80_83 Extern wave table 76-79 7-0: table80 15-8: table81 23-16: table82 31-24: table83

SUBDDRCRU_SSGTBL84_87

Address: Operational Base(0xFF128000) + offset (0x02D4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl84_87 Extern wave table 84-87 7-0: table84 15-8: table85 23-16: table86 31-24: table87

SUBDDRCRU_SSGTBL88_91

Address: Operational Base(0xFF128000) + offset (0x02D8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl88_91 Extern wave table 88-91 7-0: table88 15-8: table89 23-16: table90 31-24: table91

SUBDDRCRU_SSGTBL92_95

Address: Operational Base(0xFF128000) + offset (0x02DC)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl92_95 Extern wave table 92-95 7-0: table92 15-8: table93 23-16: table94 31-24: table95

SUBDDRCRU_SSGTBL96_99

Address: Operational Base(0xFF128000) + offset (0x02E0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl96_99 Extern wave table 96-99 7-0: table96 15-8: table97 23-16: table98 31-24: table99

SUBDDRCRU_SSGTBL100_103

Address: Operational Base(0xFF128000) + offset (0x02E4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl100_103 Extern wave table 100-103 7-0: table100 15-8: table101 23-16: table102 31-24: table103

SUBDDRCRU_SSGTBL104_107

Address: Operational Base(0xFF128000) + offset (0x02E8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl104_107 Extern wave table 104-107 7-0: table104 15-8: table105 23-16: table106 31-24: table107

SUBDDRCRU_SSGTBL108_111

Address: Operational Base(0xFF128000) + offset (0x02EC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl108_111 Extern wave table 108-111 7-0: table108 15-8: table109 23-16: table110 31-24: table111

SUBDDRCRU_SSGTBL112_115

Address: Operational Base(0xFF128000) + offset (0x02F0)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl112_115 Extern wave table 112-115 7-0: table112 15-8: table113 23-16: table114 31-24: table115

SUBDDRCRU_SSGTBL116_119

Address: Operational Base(0xFF128000) + offset (0x02F4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl116_119 Extern wave table 116-119 7-0: table116 15-8: table117 23-16: table118 31-24: table119

SUBDDRCRU_SSGTBL120_123

Address: Operational Base(0xFF128000) + offset (0x02F8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl120_123 Extern wave table 120-123 7-0: table120 15-8: table121 23-16: table122 31-24: table123

SUBDDRCRU_SSGTBL124_127

Address: Operational Base(0xFF128000) + offset (0x02FC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ssgtbl124_127 Extern wave table 124-127 7-0: table124 15-8: table125 23-16: table126 31-24: table127

SUBDDRCRU_SUBDDRMODE_CON00

Address: Operational Base(0xFF128000) + offset (0x0380)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1:0	RW	0x0	clk_dpll_mode clk_dpll_mux clock mux. 2'b00: xin_osc0_func_to_subddr 2'b01: clk_dpll 2'b10: clk_deepslow_to_subddr

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2.9 PERICRU Register Description

2.9.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PERICRU_PERICLKSEL_CON00	0x0100	W	0x00000705	Internal clock select and division register 0
PERICRU_PERICLKSEL_CON01	0x0104	W	0x0000170B	Internal clock select and division register 1
PERICRU_PERICLKSEL_CON02	0x0108	W	0x03000C35	Internal clock select and division register 2
PERICRU_PERICLKSEL_CON03	0x010C	W	0x00001700	Internal clock select and division register 3
PERICRU_PERICLKSEL_CON04	0x0110	W	0x03000C35	Internal clock select and division register 4
PERICRU_PERICLKSEL_CON05	0x0114	W	0x00000000	Internal clock select and division register 5
PERICRU_PERICLKSEL_CON06	0x0118	W	0x00001700	Internal clock select and division register 6
PERICRU_PERICLKSEL_CON07	0x011C	W	0x03000C35	Internal clock select and division register 7
PERICRU_PERICLKSEL_CON08	0x0120	W	0x00000000	Internal clock select and division register 8
PERICRU_PERICLKSEL_CON12	0x0130	W	0x00000003	Internal clock select and division register 12
PERICRU_PERICLKSEL_CON13	0x0134	W	0x00001700	Internal clock select and division register 13
PERICRU_PERICLKSEL_CON14	0x0138	W	0x03000C35	Internal clock select and division register 14
PERICRU_PERICLKSEL_CON15	0x013C	W	0x00000000	Internal clock select and division register 15
PERICRU_PERICLKSEL_CON16	0x0140	W	0x00000002	Internal clock select and division register 16
PERICRU_PERICLKSEL_CON17	0x0144	W	0x00000002	Internal clock select and division register 17
PERICRU_PERICLKSEL_CON18	0x0148	W	0x00000005	Internal clock select and division register 18
PERICRU_PERICLKSEL_CON19	0x014C	W	0x00000500	Internal clock select and division register 19
PERICRU_PERICLKSEL_CON20	0x0150	W	0x00000005	Internal clock select and division register 20
PERICRU_PERICLKSEL_CON21	0x0154	W	0x00008001	Internal clock select and division register 21
PERICRU_PERICLKSEL_CON22	0x0158	W	0x0008004B	Internal clock select and division register 22
PERICRU_PERICLKSEL_CON23	0x015C	W	0x00008001	Internal clock select and division register 23
PERICRU_PERICLKSEL_CON24	0x0160	W	0x0008004B	Internal clock select and division register 24
PERICRU_PERICLKSEL_CON25	0x0164	W	0x00008001	Internal clock select and division register 25
PERICRU_PERICLKSEL_CON26	0x0168	W	0x0008004B	Internal clock select and division register 26
PERICRU_PERICLKSEL_CON27	0x016C	W	0x00008001	Internal clock select and division register 27

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Name	Offset	Size	Reset Value	Description
PERICRU_PERICLKSEL_CON28	0x0170	W	0x0008004B	Internal clock select and division register 28
PERICRU_PERICLKSEL_CON29	0x0174	W	0x00008001	Internal clock select and division register 29
PERICRU_PERICLKSEL_CON30	0x0178	W	0x0008004B	Internal clock select and division register 30
PERICRU_PERICLKSEL_CON31	0x017C	W	0x00008001	Internal clock select and division register 31
PERICRU_PERICLKSEL_CON32	0x0180	W	0x0008004B	Internal clock select and division register 32
PERICRU_PERICLKSEL_CON33	0x0184	W	0x00008001	Internal clock select and division register 33
PERICRU_PERICLKSEL_CON34	0x0188	W	0x0008004B	Internal clock select and division register 34
PERICRU_PERICLKSEL_CON35	0x018C	W	0x00008001	Internal clock select and division register 35
PERICRU_PERICLKSEL_CON36	0x0190	W	0x0008004B	Internal clock select and division register 36
PERICRU_PERICLKSEL_CON37	0x0194	W	0x00008001	Internal clock select and division register 37
PERICRU_PERICLKSEL_CON38	0x0198	W	0x0008004B	Internal clock select and division register 38
PERICRU_PERICLKSEL_CON40	0x01A0	W	0x00000000	Internal clock select and division register 40
PERICRU_PERICLKSEL_CON43	0x01AC	W	0x00000000	Internal clock select and division register 43
PERICRU_PERICLKSEL_CON44	0x01B0	W	0x00000101	Internal clock select and division register 44
PERICRU_PERICLKSEL_CON46	0x01B8	W	0x00000001	Internal clock select and division register 46
PERICRU_PERICLKSEL_CON47	0x01BC	W	0x00000000	Internal clock select and division register 47
PERICRU_PERIGATE_CON01	0x0304	W	0x00000000	Internal clock gate and division register 1
PERICRU_PERIGATE_CON02	0x0308	W	0x00000000	Internal clock gate and division register 2
PERICRU_PERIGATE_CON03	0x030C	W	0x00000000	Internal clock gate and division register 3
PERICRU_PERIGATE_CON04	0x0310	W	0x00000000	Internal clock gate and division register 4
PERICRU_PERIGATE_CON05	0x0314	W	0x00000000	Internal clock gate and division register 5
PERICRU_PERIGATE_CON06	0x0318	W	0x00000000	Internal clock gate and division register 6
PERICRU_PERIGATE_CON07	0x031C	W	0x00000000	Internal clock gate and division register 7
PERICRU_PERIGATE_CON08	0x0320	W	0x00000000	Internal clock gate and division register 8
PERICRU_PERIGATE_CON09	0x0324	W	0x00000000	Internal clock gate and division register 9
PERICRU_PERIGATE_CON10	0x0328	W	0x00000000	Internal clock gate and division register 10
PERICRU_PERIGATE_CON12	0x0330	W	0x00000000	Internal clock gate and division register 12

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Name	Offset	Size	Reset Value	Description
PERICRU_PERIGATE_CON13	0x0334	W	0x00000000	Internal clock gate and division register 13
PERICRU_PERIGATE_CON14	0x0338	W	0x00000000	Internal clock gate and division register 14
PERICRU_PERIGATE_CON15	0x033C	W	0x00000000	Internal clock gate and division register 15
PERICRU_PERIGATE_CON16	0x0340	W	0x00000000	Internal clock gate and division register 16
PERICRU_PERIGATE_CON17	0x0344	W	0x00008000	Internal clock gate and division register 17
PERICRU_PERISOFTRST_CON01	0x0404	W	0x00000000	Internal clock reset register 1
PERICRU_PERISOFTRST_CON02	0x0408	W	0x00000000	Internal clock reset register 2
PERICRU_PERISOFTRST_CON03	0x040C	W	0x00000000	Internal clock reset register 3
PERICRU_PERISOFTRST_CON04	0x0410	W	0x00000000	Internal clock reset register 4
PERICRU_PERISOFTRST_CON05	0x0414	W	0x00000000	Internal clock reset register 5
PERICRU_PERISOFTRST_CON06	0x0418	W	0x00000000	Internal clock reset register 6
PERICRU_PERISOFTRST_CON07	0x041C	W	0x00000000	Internal clock reset register 7
PERICRU_PERISOFTRST_CON08	0x0420	W	0x00000000	Internal clock reset register 8
PERICRU_PERISOFTRST_CON09	0x0424	W	0x00000000	Internal clock reset register 9
PERICRU_PERISOFTRST_CON10	0x0428	W	0x00000000	Internal clock reset register 10
PERICRU_PERISOFTRST_CON12	0x0430	W	0x00000000	Internal clock reset register 12
PERICRU_PERISOFTRST_CON13	0x0434	W	0x00000000	Internal clock reset register 13
PERICRU_PERISOFTRST_CON14	0x0438	W	0x00000000	Internal clock reset register 14
PERICRU_PERISOFTRST_CON15	0x043C	W	0x00000000	Internal clock reset register 15
PERICRU_PERISOFTRST_CON16	0x0440	W	0x00000000	Internal clock reset register 16
PERICRU_PERISOFTRST_CON17	0x0444	W	0x00000000	Internal clock reset register 17
PERICRU_MISC_CON0	0x0684	W	0x00000001	MISC CRU Register

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

2.9.2 Detail Registers Description

PERICRU_PERICLKSEL_CON00

Address: Operational Base(0xFF130000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15	RW	0x0	hclk_peri_sel hclk_peri clock mux. 1'b0: clk_gpll_mux_to_peri 1'b1: clk_cpll_mux_from_pmu1
14	RO	0x0	reserved
13:8	RW	0x07	hclk_peri_div Divide hclk_peri by (div_con + 1).
7	RW	0x0	aclk_peri_sel aclk_peri clock mux. 1'b0: clk_gpll_mux_to_peri 1'b1: clk_cpll_mux_from_pmu1
6:5	RO	0x0	reserved
4:0	RW	0x05	aclk_peri_div Divide aclk_peri by (div_con + 1).

PERICRU_PERICLKSEL_CON01

Address: Operational Base(0xFF130000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clk_sai0_src_sel clk_sai0_src clock mux. 2'b00: clk_gpll_mux_to_peri 2'b01: clk_cpll_mux_from_pmu1 2'b10: clk_hpll_mux_to_peri
13:8	RW	0x17	clk_sai0_src_div Divide clk_sai0_src by (div_con + 1).
7	RW	0x0	pclk_peri_sel pclk_peri clock mux. 1'b0: clk_gpll_mux_to_peri 1'b1: clk_cpll_mux_from_pmu1
6:5	RO	0x0	reserved
4:0	RW	0x0b	pclk_peri_div Divide pclk_peri by (div_con + 1).

PERICRU_PERICLKSEL_CON02

Address: Operational Base(0xFF130000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:0	RW	0x03000c35	clk_sai0_frac_div clk_sai0_frac fraction division register. High 16-bit for numerator Low 16-bit for denominator

PERICRU_PERICLKSEL_CON03

Address: Operational Base(0xFF130000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:14	RW	0x0	clk_sai1_src_sel clk_sai1_src clock mux. 2'b00: clk_gpll_mux_to_peri 2'b01: clk_cpll_mux_from_pmu1 2'b10: clk_hpll_mux_to_peri
13:8	RW	0x17	clk_sai1_src_div Divide clk_sai1_src by (div_con + 1).
7:6	RW	0x0	mclk_sai0_sel mclk_sai0 clock mux. 2'b00: clk_sai0_src 2'b01: clk_sai0_frac 2'b10: xin_osc0_half 2'b11: mclk_sai0_from_io
5	RW	0x0	mclk_sai0_out2io_sel mclk_sai0_out2io clock mux. 1'b0: mclk_sai0 1'b1: xin_osc0_half
4:0	RO	0x00	reserved

PERICRU_PERICLKSEL_CON04

Address: Operational Base(0xFF130000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:0	RW	0x03000c35	clk_sai1_frac_div clk_sai1_frac fraction division register. High 16-bit for numerator Low 16-bit for denominator

PERICRU_PERICLKSEL_CON05

Address: Operational Base(0xFF130000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:6	RW	0x0	mclk_sai1_sel mclk_sai1 clock mux. 2'b00: clk_sai1_src 2'b01: clk_sai1_frac 2'b10: xin_osc0_half 2'b11: mclk_sai1_from_io
5	RW	0x0	mclk_sai1_out2io_sel mclk_sai1_out2io clock mux. 1'b0: mclk_sai1 1'b1: xin_osc0_half
4:0	RO	0x00	reserved

PERICRU_PERICLKSEL_CON06

Address: Operational Base(0xFF130000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:14	RW	0x0	clk_sai2_src_sel clk_sai2_src clock mux. 2'b00: clk_gpll_mux_to_peri 2'b01: clk_cpll_mux_from_pmu1 2'b10: clk_hpll_mux_to_peri
13:8	RW	0x17	clk_sai2_src_div Divide clk_sai2_src by (div_con + 1).
7:0	RO	0x00	reserved

PERICRU_PERICLKSEL_CON07

Address: Operational Base(0xFF130000) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:0	RW	0x03000c35	clk_sai2_frac_div clk_sai2_frac fraction division register. High 16-bit for numerator Low 16-bit for denominator

PERICRU_PERICLKSEL_CON08

Address: Operational Base(0xFF130000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:6	RW	0x0	mclk_sai2_sel mclk_sai2 clock mux. 2'b00: clk_sai2_src 2'b01: clk_sai2_frac 2'b10: xin_osc0_half 2'b11: mclk_sai2_from_io
5	RW	0x0	mclk_sai2_out2io_sel mclk_sai2_out2io clock mux. 1'b0: mclk_sai2 1'b1: xin_osc0_half
4:0	RO	0x00	reserved

PERICRU_PERICLKSEL_CON12

Address: Operational Base(0xFF130000) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:6	RW	0x0	mclk_pdm_sel mclk_pdm clock mux. 2'b00: clk_gpll_mux_to_peri 2'b01: clk_cpll_mux_from_pmu1 2'b10: clk_hpll_mux_to_peri 2'b11: xin_osc0_func
5	RO	0x0	reserved
4:0	RW	0x03	mclk_pdm_div Divide mclk_pdm by (div_con + 1).

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PERICRU_PERICLKSEL_CON13

Address: Operational Base(0xFF130000) + offset (0x0134)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clk_spdif_src_sel clk_spdif_src clock mux. 2'b00: clk_gpll_mux_to_peri 2'b01: clk_cpll_mux_from_pmu1 2'b10: clk_hpll_mux_to_peri
13:8	RW	0x17	clk_spdif_src_div Divide clk_spdif_src by (div_con + 1).
7:0	RO	0x00	reserved

PERICRU_PERICLKSEL_CON14

Address: Operational Base(0xFF130000) + offset (0x0138)

Bit	Attr	Reset Value	Description
31:0	RW	0x03000c35	clk_spdif_frac_div clk_spdif_frac fraction division register. High 16-bit for numerator Low 16-bit for denominator

PERICRU_PERICLKSEL_CON15

Address: Operational Base(0xFF130000) + offset (0x013C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:6	RW	0x0	mclk_spdif_sel mclk_spdif clock mux. 2'b00: clk_spdif_src 2'b01: clk_spdif_frac 2'b10: xin_osc0_half
5:0	RO	0x00	reserved

PERICRU_PERICLKSEL_CON16

Address: Operational Base(0xFF130000) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	cclk_sdmmc0_sel cclk_sdmmc0 clock mux. 2'b00: clk_gpll_mux_to_peri 2'b01: clk_cpll_mux_from_pmu1 2'b10: xin_osc0_func 2'b11: clk_hpll_mux_to_peri
13:8	RO	0x00	reserved
7:0	RW	0x02	cclk_sdmmc0_div DT50 division register. Divide cclk_sdmmc0 by (div_con + 1).

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PERICRU_PERICLKSEL_CON17

Address: Operational Base(0xFF130000) + offset (0x0144)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	cclk_sdmmc1_sel cclk_sdmmc1 clock mux. 2'b00: clk_gpll_mux_to_peri 2'b01: clk_cpll_mux_from_pmu1 2'b10: xin_osc0_func 2'b11: clk_hpll_mux_to_peri
13:8	RO	0x00	reserved
7:0	RW	0x02	cclk_sdmmc1_div DT50 division register. Divide cclk_sdmmc1 by (div_con + 1).

PERICRU_PERICLKSEL_CON18

Address: Operational Base(0xFF130000) + offset (0x0148)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	cclk_emmc_sel cclk_emmc clock mux. 2'b00: clk_gpll_mux_to_peri 2'b01: clk_cpll_mux_from_pmu1 2'b10: xin_osc0_func 2'b11: clk_hpll_mux_to_peri
13:8	RO	0x00	reserved
7:0	RW	0x05	cclk_emmc_div DT50 division register. Divide cclk_emmc by (div_con + 1).

PERICRU_PERICLKSEL_CON19

Address: Operational Base(0xFF130000) + offset (0x014C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	bclk_emmc_sel bclk_emmc clock mux. 1'b0: clk_gpll_mux_to_peri 1'b1: clk_cpll_mux_from_pmu1
14:8	RW	0x05	bclk_emmc_div Divide bclk_emmc by (div_con + 1).
7:0	RO	0x00	reserved

PERICRU_PERICLKSEL_CON20

Address: Operational Base(0xFF130000) + offset (0x0150)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clk_spi2_sel clk_spi2 clock mux. 2'b00: clk_matrix_200m_src 2'b01: clk_matrix_100m_src 2'b10: clk_matrix_50m_src 2'b11: xin_osc0_func
13:12	RW	0x0	clk_spi1_sel clk_spi1 clock mux. 2'b00: clk_matrix_200m_src 2'b01: clk_matrix_100m_src 2'b10: clk_matrix_50m_src 2'b11: xin_osc0_func
11:10	RO	0x0	reserved
9:8	RW	0x0	sclk_sfc_sel sclk_sfc clock mux. 2'b00: clk_gpll_mux_to_peri 2'b01: clk_cpll_mux_from_pmu1 2'b10: xin_osc0_func
7:0	RW	0x05	sclk_sfc_div DT50 division register. Divide sclk_sfc by (div_con + 1).

PERICRU_PERICLKSEL_CON21

Address: Operational Base(0xFF130000) + offset (0x0154)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	sclk_uart1_sel sclk_uart1 clock mux. 2'b00: clk_uart1_src 2'b01: clk_uart1_frac 2'b10: xin_osc0_func
13:9	RO	0x00	reserved
8	RW	0x0	clk_uart1_src_sel clk_uart1_src clock mux. 1'b0: clk_gpll_mux_to_peri 1'b1: clk_cpll_mux_from_pmu1
7	RO	0x0	reserved
6:0	RW	0x01	clk_uart1_src_div Divide clk_uart1_src by (div_con + 1).

PERICRU_PERICLKSEL_CON22

Address: Operational Base(0xFF130000) + offset (0x0158)

Bit	Attr	Reset Value	Description
31:0	RW	0x0008004b	clk_uart1_frac_div clk_uart1_frac fraction division register. High 16-bit for numerator Low 16-bit for denominator

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PERICRU_PERICLKSEL_CON23

Address: Operational Base(0xFF130000) + offset (0x015C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	sclk_uart2_sel sclk_uart2 clock mux. 2'b00: clk_uart2_src 2'b01: clk_uart2_frac 2'b10: xin_osc0_func
13:9	RO	0x00	reserved
8	RW	0x0	clk_uart2_src_sel clk_uart2_src clock mux. 1'b0: clk_gpll_mux_to_peri 1'b1: clk_cpll_mux_from_pmu1
7	RO	0x0	reserved
6:0	RW	0x01	clk_uart2_src_div Divide clk_uart2_src by (div_con + 1).

PERICRU_PERICLKSEL_CON24

Address: Operational Base(0xFF130000) + offset (0x0160)

Bit	Attr	Reset Value	Description
31:0	RW	0x0008004b	clk_uart2_frac_div clk_uart2_frac fraction division register. High 16-bit for numerator Low 16-bit for denominator

PERICRU_PERICLKSEL_CON25

Address: Operational Base(0xFF130000) + offset (0x0164)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	sclk_uart3_sel sclk_uart3 clock mux. 2'b00: clk_uart3_src 2'b01: clk_uart3_frac 2'b10: xin_osc0_func
13:9	RO	0x00	reserved
8	RW	0x0	clk_uart3_src_sel clk_uart3_src clock mux. 1'b0: clk_gpll_mux_to_peri 1'b1: clk_cpll_mux_from_pmu1
7	RO	0x0	reserved
6:0	RW	0x01	clk_uart3_src_div Divide clk_uart3_src by (div_con + 1).

PERICRU_PERICLKSEL_CON26

Address: Operational Base(0xFF130000) + offset (0x0168)

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Bit	Attr	Reset Value	Description
31:0	RW	0x0008004b	clk_uart3_frac_div clk_uart3_frac fraction division register. High 16-bit for numerator Low 16-bit for denominator

PERICRU_PERICLKSEL_CON27

Address: Operational Base(0xFF130000) + offset (0x016C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	sclk_uart4_sel sclk_uart4 clock mux. 2'b00: clk_uart4_src 2'b01: clk_uart4_frac 2'b10: xin_osc0_func
13:9	RO	0x00	reserved
8	RW	0x0	clk_uart4_src_sel clk_uart4_src clock mux. 1'b0: clk_gpll_mux_to_peri 1'b1: clk_cpll_mux_from_pmu1
7	RO	0x0	reserved
6:0	RW	0x01	clk_uart4_src_div Divide clk_uart4_src by (div_con + 1).

PERICRU_PERICLKSEL_CON28

Address: Operational Base(0xFF130000) + offset (0x0170)

Bit	Attr	Reset Value	Description
31:0	RW	0x0008004b	clk_uart4_frac_div clk_uart4_frac fraction division register. High 16-bit for numerator Low 16-bit for denominator

PERICRU_PERICLKSEL_CON29

Address: Operational Base(0xFF130000) + offset (0x0174)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	sclk_uart5_sel sclk_uart5 clock mux. 2'b00: clk_uart5_src 2'b01: clk_uart5_frac 2'b10: xin_osc0_func
13:9	RO	0x00	reserved
8	RW	0x0	clk_uart5_src_sel clk_uart5_src clock mux. 1'b0: clk_gpll_mux_to_peri 1'b1: clk_cpll_mux_from_pmu1
7	RO	0x0	reserved
6:0	RW	0x01	clk_uart5_src_div Divide clk_uart5_src by (div_con + 1).

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PERICRU_PERICLKSEL_CON30

Address: Operational Base(0xFF130000) + offset (0x0178)

Bit	Attr	Reset Value	Description
31:0	RW	0x0008004b	clk_uart5_frac_div clk_uart5_frac fraction division register. High 16-bit for numerator Low 16-bit for denominator

PERICRU_PERICLKSEL_CON31

Address: Operational Base(0xFF130000) + offset (0x017C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	sclk_uart6_sel sclk_uart6 clock mux. 2'b00: clk_uart6_src 2'b01: clk_uart6_frac 2'b10: xin_osc0_func
13:9	RO	0x00	reserved
8	RW	0x0	clk_uart6_src_sel clk_uart6_src clock mux. 1'b0: clk_gpll_mux_to_peri 1'b1: clk_cpll_mux_from_pmu1
7	RO	0x0	reserved
6:0	RW	0x01	clk_uart6_src_div Divide clk_uart6_src by (div_con + 1).

PERICRU_PERICLKSEL_CON32

Address: Operational Base(0xFF130000) + offset (0x0180)

Bit	Attr	Reset Value	Description
31:0	RW	0x0008004b	clk_uart6_frac_div clk_uart6_frac fraction division register. High 16-bit for numerator Low 16-bit for denominator

PERICRU_PERICLKSEL_CON33

Address: Operational Base(0xFF130000) + offset (0x0184)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	sclk_uart7_sel sclk_uart7 clock mux. 2'b00: clk_uart7_src 2'b01: clk_uart7_frac 2'b10: xin_osc0_func
13:9	RO	0x00	reserved
8	RW	0x0	clk_uart7_src_sel clk_uart7_src clock mux. 1'b0: clk_gpll_mux_to_peri 1'b1: clk_cpll_mux_from_pmu1
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:0	RW	0x01	clk_uart7_src_div Divide clk_uart7_src by (div_con + 1).

PERICRU_PERICLKSEL_CON34

Address: Operational Base(0xFF130000) + offset (0x0188)

Bit	Attr	Reset Value	Description
31:0	RW	0x0008004b	clk_uart7_frac_div clk_uart7_frac fraction division register. High 16-bit for numerator Low 16-bit for denominator

PERICRU_PERICLKSEL_CON35

Address: Operational Base(0xFF130000) + offset (0x018C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	sclk_uart8_sel sclk_uart8 clock mux. 2'b00: clk_uart8_src 2'b01: clk_uart8_frac 2'b10: xin_osc0_func
13:9	RO	0x00	reserved
8	RW	0x0	clk_uart8_src_sel clk_uart8_src clock mux. 1'b0: clk_gpll_mux_to_peri 1'b1: clk_cpll_mux_from_pmu1
7	RO	0x0	reserved
6:0	RW	0x01	clk_uart8_src_div Divide clk_uart8_src by (div_con + 1).

PERICRU_PERICLKSEL_CON36

Address: Operational Base(0xFF130000) + offset (0x0190)

Bit	Attr	Reset Value	Description
31:0	RW	0x0008004b	clk_uart8_frac_div clk_uart8_frac fraction division register. High 16-bit for numerator Low 16-bit for denominator

PERICRU_PERICLKSEL_CON37

Address: Operational Base(0xFF130000) + offset (0x0194)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	sclk_uart9_sel sclk_uart9 clock mux. 2'b00: clk_uart9_src 2'b01: clk_uart9_frac 2'b10: xin_osc0_func
13:9	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
8	RW	0x0	clk_uart9_src_sel clk_uart9_src clock mux. 1'b0: clk_gpll_mux_to_peri 1'b1: clk_cpll_mux_from_pmu1
7	RO	0x0	reserved
6:0	RW	0x01	clk_uart9_src_div Divide clk_uart9_src by (div_con + 1).

PERICRU_PERICLKSEL_CON38

Address: Operational Base(0xFF130000) + offset (0x0198)

Bit	Attr	Reset Value	Description
31:0	RW	0x0008004b	clk_uart9_frac_div clk_uart9_frac fraction division register. High 16-bit for numerator Low 16-bit for denominator

PERICRU_PERICLKSEL_CON40

Address: Operational Base(0xFF130000) + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9:8	RW	0x0	clk_pwm3_peri_sel clk_pwm3_peri clock mux. 2'b00: clk_matrix_100m_src 2'b01: clk_matrix_50m_src 2'b10: xin_osc0_func
7:6	RW	0x0	clk_pwm2_peri_sel clk_pwm2_peri clock mux. 2'b00: clk_matrix_100m_src 2'b01: clk_matrix_50m_src 2'b10: xin_osc0_func
5:2	RO	0x0	reserved
1:0	RW	0x0	clk_pwm1_peri_sel clk_pwm1_peri clock mux. 2'b00: clk_matrix_100m_src 2'b01: clk_matrix_50m_src 2'b10: xin_osc0_func

PERICRU_PERICLKSEL_CON43

Address: Operational Base(0xFF130000) + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	tclk_peri_wdt_sel tclk_peri_wdt clock mux. 1'b0: xin_osc0_func 1'b1: clk_deepslow
14:8	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
7:6	RW	0x0	clk_pka_crypto_sel clk_pka_crypto clock mux. 2'b00: clk_matrix_300m_src 2'b01: clk_matrix_200m_src 2'b10: clk_matrix_100m_src 2'b11: xin_osc0_func
5:2	RO	0x0	reserved
1:0	RW	0x0	clk_core_crypto_sel clk_core_crypto clock mux. 2'b00: clk_matrix_200m_src 2'b01: clk_matrix_100m_src 2'b10: xin_osc0_func

PERICRU_PERICLKSEL_CON44

Address: Operational Base(0xFF130000) + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x01	clk_user_otpc_s_div Divide clk_user_otpc_s by (div_con + 1).
7:0	RW	0x01	clk_user_otpc_ns_div Divide clk_user_otpc_ns by (div_con + 1).

PERICRU_PERICLKSEL_CON46

Address: Operational Base(0xFF130000) + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:0	RW	0x001	clk_saradc_div Divide clk_saradc by (div_con + 1).

PERICRU_PERICLKSEL_CON47

Address: Operational Base(0xFF130000) + offset (0x01BC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:11	RW	0x00	clk_testout_peri_sel clk_testout_peri clock mux. 5'b00000: aclk_peri 5'b00001: hclk_peri 5'b00010: pclk_peri 5'b00011: cclk_emmc 5'b00100: bclk_emmc 5'b00101: sclk_sfc 5'b00110: clk_usbphy_usb2host_utmi 5'b00111: clk_usbphy_usb2host_ohci 5'b01000: clk_spi1 5'b01001: clk_spi2 5'b01010: sclk_uart1 5'b01011: sclk_uart2 5'b01100: sclk_uart3 5'b01101: sclk_uart4 5'b01110: sclk_uart5 5'b01111: sclk_uart6 5'b10000: sclk_uart7 5'b10001: sclk_uart8 5'b10010: sclk_uart9 5'b10011: reserved 5'b10100: reserved 5'b10101: clk_core_crypto 5'b10110: clk_pka_crypto 5'b10111: rk_rng_dbg_work_clk_io 5'b11000: rk_rng_dbg_cro_str_dout_io 5'b11001: sdmmc0_test_clkout_0 5'b11010: sdmmc0_test_clkout_1 5'b11011: sdmmc1_test_clkout_0 5'b11100: sdmmc1_test_clkout_1 5'b11101: otp_ips_osc_out 5'b11110: 1'b0 5'b11111: 1'b0
10:9	RO	0x0	reserved
8	RW	0x0	dclk_peri_gpio_sel dclk_peri_gpio clock mux. 1'b0: xin_osc0_func 1'b1: clk_deepslow
7:0	RO	0x00	reserved

PERICRU_PERIGATE_CON01

Address: Operational Base(0xFF130000) + offset (0x0304)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	pclk_pericru_en pclk_pericru clock gating control. When high, disable clock
5	RW	0x0	pclk_peri_biu_en pclk_peri_biu clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
4	RW	0x0	hclk_peri_biu_en hclk_peri_biu clock gating control. When high, disable clock
3	RW	0x0	aclk_peri_biu_en aclk_peri_biu clock gating control. When high, disable clock
2	RW	0x0	pclk_peri_en pclk_peri clock gating control. When high, disable clock
1	RW	0x0	hclk_peri_en hclk_peri clock gating control. When high, disable clock
0	RW	0x0	aclk_peri_en aclk_peri clock gating control. When high, disable clock

PERICRU_PERIGATE_CON02

Address: Operational Base(0xFF130000) + offset (0x0308)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	mclk_sai2_out2io_en mclk_sai2_out2io clock gating control. When high, disable clock
13	RW	0x0	mclk_sai2_en mclk_sai2 clock gating control. When high, disable clock
12	RW	0x0	clk_sai2_frac_en clk_sai2_frac clock gating control. When high, disable clock
11	RW	0x0	clk_sai2_en clk_sai2_src clock gating control. When high, disable clock
10	RW	0x0	hclk_sai2_en hclk_sai2 clock gating control. When high, disable clock
9	RW	0x0	mclk_sai1_out2io_en mclk_sai1_out2io clock gating control. When high, disable clock
8	RW	0x0	mclk_sai1_en mclk_sai1 clock gating control. When high, disable clock
7	RW	0x0	clk_sai1_frac_en clk_sai1_frac clock gating control. When high, disable clock
6	RW	0x0	clk_sai1_en clk_sai1_src clock gating control. When high, disable clock
5	RW	0x0	hclk_sai1_en hclk_sai1 clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
4	RW	0x0	mclk_sai0_out2io_en mclk_sai0_out2io clock gating control. When high, disable clock
3	RW	0x0	mclk_sai0_en mclk_sai0 clock gating control. When high, disable clock
2	RW	0x0	clk_sai0_frac_en clk_sai0_frac clock gating control. When high, disable clock
1	RW	0x0	clk_sai0_en clk_sai0_src clock gating control. When high, disable clock
0	RW	0x0	hclk_sai0_en hclk_sai0 clock gating control. When high, disable clock

PERICRU_PERIGATE_CON03

Address: Operational Base(0xFF130000) + offset (0x030C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	mclk_spdif_en mclk_spdif clock gating control. When high, disable clock
10	RW	0x0	clk_spdif_frac_en clk_spdif_frac clock gating control. When high, disable clock
9	RW	0x0	clk_spdif_en clk_spdif_src clock gating control. When high, disable clock
8	RW	0x0	hclk_spdif_en hclk_spdif clock gating control. When high, disable clock
7:6	RO	0x0	reserved
5	RW	0x0	mclk_pdm_en mclk_pdm clock gating control. When high, disable clock
4	RW	0x0	hclk_pdm_en hclk_pdm clock gating control. When high, disable clock
3	RO	0x0	reserved
2	RW	0x0	clk_dsm_en clk_dsm clock gating control. When high, disable clock
1	RW	0x0	hclk_dsm_en hclk_dsm clock gating control. When high, disable clock
0	RO	0x0	reserved

PERICRU_PERIGATE_CON04

Address: Operational Base(0xFF130000) + offset (0x0310)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	hclk_sfc_en hclk_sfc clock gating control. When high, disable clock
13	RW	0x0	sclk_sfc_en sclk_sfc clock gating control. When high, disable clock
12	RW	0x0	tmclk_emmc_en tmclk_emmc clock gating control. When high, disable clock
11	RW	0x0	bclk_emmc_en bclk_emmc clock gating control. When high, disable clock
10	RW	0x0	cclk_emmc_en cclk_emmc clock gating control. When high, disable clock
9	RW	0x0	aclk_emmc_en aclk_emmc clock gating control. When high, disable clock
8	RW	0x0	hclk_emmc_en hclk_emmc clock gating control. When high, disable clock
7:4	RO	0x0	reserved
3	RW	0x0	cclk_sdmmc1_en cclk_sdmmc1 clock gating control. When high, disable clock
2	RW	0x0	hclk_sdmmc1_en hclk_sdmmc1 clock gating control. When high, disable clock
1	RW	0x0	cclk_sdmmc0_en cclk_sdmmc0 clock gating control. When high, disable clock
0	RW	0x0	hclk_sdmmc0_en hclk_sdmmc0 clock gating control. When high, disable clock

PERICRU_PERIGATE_CON05

Address: Operational Base(0xFF130000) + offset (0x0314)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	hclk_usb2host_arb_en hclk_usb2host_arb clock gating control. When high, disable clock
0	RW	0x0	hclk_usb2host_en hclk_usb2host clock gating control. When high, disable clock

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PERICRU_PERIGATE_CON06

Address: Operational Base(0xFF130000) + offset (0x0318)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	sclk_in_spi2_en sclk_in_spi2 clock gating control. When high, disable clock
4	RW	0x0	clk_spi2_en clk_spi2 clock gating control. When high, disable clock
3	RW	0x0	pclk_spi2_en pclk_spi2 clock gating control. When high, disable clock
2	RW	0x0	sclk_in_spi1_en sclk_in_spi1 clock gating control. When high, disable clock
1	RW	0x0	clk_spi1_en clk_spi1 clock gating control. When high, disable clock
0	RW	0x0	pclk_spi1_en pclk_spi1 clock gating control. When high, disable clock

PERICRU_PERIGATE_CON07

Address: Operational Base(0xFF130000) + offset (0x031C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_uart3_en clk_uart3_src clock gating control. When high, disable clock
14	RW	0x0	sclk_uart2_en sclk_uart2 clock gating control. When high, disable clock
13	RW	0x0	clk_uart2_frac_en clk_uart2_frac clock gating control. When high, disable clock
12	RW	0x0	clk_uart2_en clk_uart2_src clock gating control. When high, disable clock
11	RW	0x0	sclk_uart1_en sclk_uart1 clock gating control. When high, disable clock
10	RW	0x0	clk_uart1_frac_en clk_uart1_frac clock gating control. When high, disable clock
9	RW	0x0	clk_uart1_en clk_uart1_src clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
8	RW	0x0	pclk_uart9_en pclk_uart9 clock gating control. When high, disable clock
7	RW	0x0	pclk_uart8_en pclk_uart8 clock gating control. When high, disable clock
6	RW	0x0	pclk_uart7_en pclk_uart7 clock gating control. When high, disable clock
5	RW	0x0	pclk_uart6_en pclk_uart6 clock gating control. When high, disable clock
4	RW	0x0	pclk_uart5_en pclk_uart5 clock gating control. When high, disable clock
3	RW	0x0	pclk_uart4_en pclk_uart4 clock gating control. When high, disable clock
2	RW	0x0	pclk_uart3_en pclk_uart3 clock gating control. When high, disable clock
1	RW	0x0	pclk_uart2_en pclk_uart2 clock gating control. When high, disable clock
0	RW	0x0	pclk_uart1_en pclk_uart1 clock gating control. When high, disable clock

PERICRU_PERIGATE_CON08

Address: Operational Base(0xFF130000) + offset (0x0320)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_uart8_frac_en clk_uart8_frac clock gating control. When high, disable clock
14	RW	0x0	clk_uart8_en clk_uart8_src clock gating control. When high, disable clock
13	RW	0x0	sclk_uart7_en sclk_uart7 clock gating control. When high, disable clock
12	RW	0x0	clk_uart7_frac_en clk_uart7_frac clock gating control. When high, disable clock
11	RW	0x0	clk_uart7_en clk_uart7_src clock gating control. When high, disable clock
10	RW	0x0	sclk_uart6_en sclk_uart6 clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
9	RW	0x0	clk_uart6_frac_en clk_uart6_frac clock gating control. When high, disable clock
8	RW	0x0	clk_uart6_en clk_uart6_src clock gating control. When high, disable clock
7	RW	0x0	sclk_uart5_en sclk_uart5 clock gating control. When high, disable clock
6	RW	0x0	clk_uart5_frac_en clk_uart5_frac clock gating control. When high, disable clock
5	RW	0x0	clk_uart5_en clk_uart5_src clock gating control. When high, disable clock
4	RW	0x0	sclk_uart4_en sclk_uart4 clock gating control. When high, disable clock
3	RW	0x0	clk_uart4_frac_en clk_uart4_frac clock gating control. When high, disable clock
2	RW	0x0	clk_uart4_en clk_uart4_src clock gating control. When high, disable clock
1	RW	0x0	sclk_uart3_en sclk_uart3 clock gating control. When high, disable clock
0	RW	0x0	clk_uart3_frac_en clk_uart3_frac clock gating control. When high, disable clock

PERICRU_PERIGATE_CON09

Address: Operational Base(0xFF130000) + offset (0x0324)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	sclk_uart9_en sclk_uart9 clock gating control. When high, disable clock
2	RW	0x0	clk_uart9_frac_en clk_uart9_frac clock gating control. When high, disable clock
1	RW	0x0	clk_uart9_en clk_uart9_src clock gating control. When high, disable clock
0	RW	0x0	sclk_uart8_en sclk_uart8 clock gating control. When high, disable clock

PERICRU_PERIGATE_CON10

Address: Operational Base(0xFF130000) + offset (0x0328)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	clk_capture_pwm3_peri_en clk_capture_pwm3_peri clock gating control. When high, disable clock
7	RW	0x0	clk_pwm3_peri_en clk_pwm3_peri clock gating control. When high, disable clock
6	RW	0x0	pclk_pwm3_peri_en pclk_pwm3_peri clock gating control. When high, disable clock
5	RW	0x0	clk_capture_pwm2_peri_en clk_capture_pwm2_peri clock gating control. When high, disable clock
4	RW	0x0	clk_pwm2_peri_en clk_pwm2_peri clock gating control. When high, disable clock
3	RW	0x0	pclk_pwm2_peri_en pclk_pwm2_peri clock gating control. When high, disable clock
2	RW	0x0	clk_capture_pwm1_peri_en clk_capture_pwm1_peri clock gating control. When high, disable clock
1	RW	0x0	clk_pwm1_peri_en clk_pwm1_peri clock gating control. When high, disable clock
0	RW	0x0	pclk_pwm1_peri_en pclk_pwm1_peri clock gating control. When high, disable clock

PERICRU_PERIGATE_CON12

Address: Operational Base(0xFF130000) + offset (0x0330)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	hclk_crypto_s_en hclk_crypto_s clock gating control. When high, disable clock
10	RW	0x0	hclk_trng_s_en hclk_trng_s clock gating control. When high, disable clock
9	RW	0x0	hclk_trng_ns_en hclk_trng_ns clock gating control. When high, disable clock
8	RW	0x0	hclk_rk_rng_s_en hclk_rk_rng_s clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
7	RW	0x0	hclk_rk_rng_ns_en hclk_rk_rng_ns clock gating control. When high, disable clock
6	RW	0x0	pclk_key_reader_en pclk_key_reader clock gating control. When high, disable clock
5	RW	0x0	hclk_klad_en hclk_klad clock gating control. When high, disable clock
4	RW	0x0	clk_pka_crypto_en clk_pka_crypto clock gating control. When high, disable clock
3	RW	0x0	clk_core_crypto_en clk_core_crypto clock gating control. When high, disable clock
2	RW	0x0	pclk_crypto_en pclk_crypto clock gating control. When high, disable clock
1	RW	0x0	hclk_crypto_en hclk_crypto clock gating control. When high, disable clock
0	RW	0x0	aclk_crypto_en aclk_crypto clock gating control. When high, disable clock

PERICRU_PERIGATE_CON13

Address: Operational Base(0xFF130000) + offset (0x0334)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	aclk_rkdmac_en aclk_rkdmac clock gating control. When high, disable clock
5	RW	0x0	aclk_dmac_en aclk_dmac clock gating control. When high, disable clock
4	RW	0x0	pclk_peri_grf_en pclk_peri_grf clock gating control. When high, disable clock
3	RW	0x0	hclk_bootrom_en hclk_bootrom clock gating control. When high, disable clock
2	RW	0x0	aclk_sysmem_en aclk_sysmem clock gating control. When high, disable clock
1	RW	0x0	tclk_peri_wdt_en tclk_peri_wdt clock gating control. When high, disable clock
0	RW	0x0	pclk_peri_wdt_en pclk_peri_wdt clock gating control. When high, disable clock

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PERICRU_PERIGATE_CON14

Address: Operational Base(0xFF130000) + offset (0x0338)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	pclk_otpphy_en pclk_otpphy clock gating control. When high, disable clock
6	RW	0x0	clk_otpc_arb_en clk_otpc_arb clock gating control. When high, disable clock
5	RW	0x0	clk_user_otpc_s_en clk_user_otpc_s clock gating control. When high, disable clock
4	RW	0x0	clk_sbpi_otpc_s_en clk_sbpi_otpc_s clock gating control. When high, disable clock
3	RW	0x0	pclk_otpc_s_en pclk_otpc_s clock gating control. When high, disable clock
2	RW	0x0	clk_user_otpc_ns_en clk_user_otpc_ns clock gating control. When high, disable clock
1	RW	0x0	clk_sbpi_otpc_ns_en clk_sbpi_otpc_ns clock gating control. When high, disable clock
0	RW	0x0	pclk_otpc_ns_en pclk_otpc_ns clock gating control. When high, disable clock

PERICRU_PERIGATE_CON15

Address: Operational Base(0xFF130000) + offset (0x033C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	pclk_pipephy_en pclk_pipephy clock gating control. When high, disable clock
6:1	RO	0x00	reserved
0	RW	0x0	pclk_usb2phy_en pclk_usb2phy clock gating control. When high, disable clock

PERICRU_PERIGATE_CON16

Address: Operational Base(0xFF130000) + offset (0x0340)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12	RW	0x0	pclk_ioc_vccio234_en pclk_ioc_vccio234 clock gating control. When high, disable clock
11:6	RO	0x00	reserved
5	RW	0x0	clk_saradc_en clk_saradc clock gating control. When high, disable clock
4	RW	0x0	pclk_saradc_en pclk_saradc clock gating control. When high, disable clock
3:0	RO	0x0	reserved

PERICRU_PERIGATE_CON17

Address: Operational Base(0xFF130000) + offset (0x0344)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	clk_testout_peri_en clk_testout_peri clock gating control. When high, disable clock
14:5	RO	0x000	reserved
4	RW	0x0	dclk_peri_gpio_en dclk_peri_gpio clock gating control. When high, disable clock
3	RW	0x0	dclk_peri_gpio2_en dclk_peri_gpio2 clock gating control. When high, disable clock
2	RW	0x0	dclk_peri_gpio1_en dclk_peri_gpio1 clock gating control. When high, disable clock
1	RW	0x0	pclk_peri_gpio2_en pclk_peri_gpio2 clock gating control. When high, disable clock
0	RW	0x0	pclk_peri_gpio1_en pclk_peri_gpio1 clock gating control. When high, disable clock

PERICRU_PERISOFTRST_CON01

Address: Operational Base(0xFF130000) + offset (0x0404)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	presetn_pericru When high, reset relative logic
5	RW	0x0	presetn_peri_biu When high, reset relative logic
4	RW	0x0	hresetn_peri_biu When high, reset relative logic

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Bit	Attr	Reset Value	Description
3	RW	0x0	aresetn_peri_biu When high, reset relative logic
2:0	RO	0x0	reserved

PERICRU_PERISOFTRST_CON02

Address: Operational Base(0xFF130000) + offset (0x0408)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	mresetn_sai2 When high, reset relative logic
12:11	RO	0x0	reserved
10	RW	0x0	hresetn_sai2 When high, reset relative logic
9	RO	0x0	reserved
8	RW	0x0	mresetn_sai1 When high, reset relative logic
7:6	RO	0x0	reserved
5	RW	0x0	hresetn_sai1 When high, reset relative logic
4	RO	0x0	reserved
3	RW	0x0	mresetn_sai0 When high, reset relative logic
2:1	RO	0x0	reserved
0	RW	0x0	hresetn_sai0 When high, reset relative logic

PERICRU_PERISOFTRST_CON03

Address: Operational Base(0xFF130000) + offset (0x040C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	mresetn_spdif When high, reset relative logic
10:9	RO	0x0	reserved
8	RW	0x0	hresetn_spdif When high, reset relative logic
7:6	RO	0x0	reserved
5	RW	0x0	mresetn_pdm When high, reset relative logic
4	RW	0x0	hresetn_pdm When high, reset relative logic
3	RO	0x0	reserved
2	RW	0x0	resetn_dsm When high, reset relative logic
1	RW	0x0	hresetn_dsm When high, reset relative logic
0	RO	0x0	reserved

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PERICRU_PERISOFTRST_CON04

Address: Operational Base(0xFF130000) + offset (0x0410)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	hresetn_sfc When high, reset relative logic
13	RW	0x0	sresetn_sfc When high, reset relative logic
12	RW	0x0	tresetn_emmc When high, reset relative logic
11	RW	0x0	bresetn_emmc When high, reset relative logic
10	RW	0x0	cresetn_emmc When high, reset relative logic
9	RW	0x0	aresetn_emmc When high, reset relative logic
8	RW	0x0	hresetn_emmc When high, reset relative logic
7:3	RO	0x00	reserved
2	RW	0x0	hresetn_sdmmc1 When high, reset relative logic
1	RO	0x0	reserved
0	RW	0x0	hresetn_sdmmc0 When high, reset relative logic

PERICRU_PERISOFTRST_CON05

Address: Operational Base(0xFF130000) + offset (0x0414)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2	RW	0x0	resetn_usb2host_utmi When high, reset relative logic
1	RW	0x0	hresetn_usb2host_arb When high, reset relative logic
0	RW	0x0	hresetn_usb2host When high, reset relative logic

PERICRU_PERISOFTRST_CON06

Address: Operational Base(0xFF130000) + offset (0x0418)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x0	resetn_spi2 When high, reset relative logic
3	RW	0x0	presetn_spi2 When high, reset relative logic

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Bit	Attr	Reset Value	Description
2	RO	0x0	reserved
1	RW	0x0	resetn_spi1 When high, reset relative logic
0	RW	0x0	presetn_spi1 When high, reset relative logic

PERICRU_PERISOFTRST_CON07

Address: Operational Base(0xFF130000) + offset (0x041C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	sresetn_uart2 When high, reset relative logic
13:12	RO	0x0	reserved
11	RW	0x0	sresetn_uart1 When high, reset relative logic
10:9	RO	0x0	reserved
8	RW	0x0	presetn_uart9 When high, reset relative logic
7	RW	0x0	presetn_uart8 When high, reset relative logic
6	RW	0x0	presetn_uart7 When high, reset relative logic
5	RW	0x0	presetn_uart6 When high, reset relative logic
4	RW	0x0	presetn_uart5 When high, reset relative logic
3	RW	0x0	presetn_uart4 When high, reset relative logic
2	RW	0x0	presetn_uart3 When high, reset relative logic
1	RW	0x0	presetn_uart2 When high, reset relative logic
0	RW	0x0	presetn_uart1 When high, reset relative logic

PERICRU_PERISOFTRST_CON08

Address: Operational Base(0xFF130000) + offset (0x0420)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	sresetn_uart7 When high, reset relative logic
12:11	RO	0x0	reserved
10	RW	0x0	sresetn_uart6 When high, reset relative logic
9:8	RO	0x0	reserved
7	RW	0x0	sresetn_uart5 When high, reset relative logic

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Bit	Attr	Reset Value	Description
6:5	RO	0x0	reserved
4	RW	0x0	sresetn_uart4 When high, reset relative logic
3:2	RO	0x0	reserved
1	RW	0x0	sresetn_uart3 When high, reset relative logic
0	RO	0x0	reserved

PERICRU_PERISOFTRST_CON09

Address: Operational Base(0xFF130000) + offset (0x0424)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	sresetn_uart9 When high, reset relative logic
2:1	RO	0x0	reserved
0	RW	0x0	sresetn_uart8 When high, reset relative logic

PERICRU_PERISOFTRST_CON10

Address: Operational Base(0xFF130000) + offset (0x0428)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	resetn_pwm3_peri When high, reset relative logic
6	RW	0x0	presetn_pwm3_peri When high, reset relative logic
5	RO	0x0	reserved
4	RW	0x0	resetn_pwm2_peri When high, reset relative logic
3	RW	0x0	presetn_pwm2_peri When high, reset relative logic
2	RO	0x0	reserved
1	RW	0x0	resetn_pwm1_peri When high, reset relative logic
0	RW	0x0	presetn_pwm1_peri When high, reset relative logic

PERICRU_PERISOFTRST_CON12

Address: Operational Base(0xFF130000) + offset (0x0430)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	hresetn_crypto_s When high, reset relative logic

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Bit	Attr	Reset Value	Description
10	RW	0x0	hresetn_trng_s When high, reset relative logic
9	RW	0x0	hresetn_trng_ns When high, reset relative logic
8	RW	0x0	hresetn_rk_rng_s When high, reset relative logic
7	RW	0x0	hresetn_rk_rng_ns When high, reset relative logic
6	RW	0x0	presetn_key_reader When high, reset relative logic
5	RW	0x0	hresetn_klad When high, reset relative logic
4	RW	0x0	resetn_pka_crypto When high, reset relative logic
3	RW	0x0	resetn_core_crypto When high, reset relative logic
2	RW	0x0	presetn_crypto When high, reset relative logic
1	RW	0x0	hresetn_crypto When high, reset relative logic
0	RW	0x0	aresetn_crypto When high, reset relative logic

PERICRU_PERISOFTRST_CON13

Address: Operational Base(0xFF130000) + offset (0x0434)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	aresetn_rkdmac When high, reset relative logic
5	RW	0x0	aresetn_dmac When high, reset relative logic
4	RW	0x0	presetn_peri_grf When high, reset relative logic
3	RW	0x0	hresetn_bootrom When high, reset relative logic
2	RW	0x0	aresetn_sysmem When high, reset relative logic
1	RW	0x0	tresetn_peri_wdt When high, reset relative logic
0	RW	0x0	presetn_peri_wdt When high, reset relative logic

PERICRU_PERISOFTRST_CON14

Address: Operational Base(0xFF130000) + offset (0x0438)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
8	RW	0x0	resetn_otp_npor When high, reset relative logic
7	RW	0x0	presetn_otpphy When high, reset relative logic
6	RW	0x0	resetn_otpc_arb When high, reset relative logic
5	RW	0x0	resetn_user_otpc_s When high, reset relative logic
4	RW	0x0	resetn_sbpi_otpc_s When high, reset relative logic
3	RW	0x0	presetn_otpc_s When high, reset relative logic
2	RW	0x0	resetn_user_otpc_ns When high, reset relative logic
1	RW	0x0	resetn_sbpi_otpc_ns When high, reset relative logic
0	RW	0x0	presetn_otpc_ns When high, reset relative logic

PERICRU_PERISOFTRST_CON15

Address: Operational Base(0xFF130000) + offset (0x043C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	presetn_pipephy When high, reset relative logic
6	RW	0x0	resetn_usb2phy_host When high, reset relative logic
5	RW	0x0	resetn_usb2phy_otg When high, reset relative logic
4	RW	0x0	resetn_usb2phy_por When high, reset relative logic
3:1	RO	0x0	reserved
0	RW	0x0	presetn_usb2phy When high, reset relative logic

PERICRU_PERISOFTRST_CON16

Address: Operational Base(0xFF130000) + offset (0x0440)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	presetn_ioc_vccio234 When high, reset relative logic
11:7	RO	0x00	reserved
6	RW	0x0	resetn_saradc_phy When high, reset relative logic
5	RW	0x0	resetn_saradc When high, reset relative logic

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Bit	Attr	Reset Value	Description
4	RW	0x0	presetn_saradc When high, reset relative logic
3:0	RO	0x0	reserved

PERICRU_PERISOFTRST_CON17

Address: Operational Base(0xFF130000) + offset (0x0444)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	resetn_peri_gpio2 When high, reset relative logic
2	RW	0x0	resetn_peri_gpio1 When high, reset relative logic
1	RW	0x0	presetn_peri_gpio2 When high, reset relative logic
0	RW	0x0	presetn_peri_gpio1 When high, reset relative logic

PERICRU_MISC_CON0

Address: Operational Base(0xFF130000) + offset (0x0684)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	enable_pd_peri_clk_src_gating =1: enable pd_peri_clk_src_gating =0: disable it . it is default value.
14:2	RO	0x0000	reserved
1	RW	0x0	enable_usb3otg_usb2phy_reset =1: enable usb3otg_usb2phy_reset =0: disable it, default disable it.
0	RW	0x1	enable_resetn_phy2host_src =1: disable the resetn_phy2host_src. default is 1. =0: enable it.

2.10 Application Notes

2.10.1 Fractional PLL Usage

2.10.1.1 PLL Frequency Configuration

FBDIV, POSTDIV1, BYPASS can be configured by programming CRU_xPLL_CON0.
DSMPD, REFDIV, POSTDIV2 can be configured by programming CRU_xPLL_CON1.
FRAC can be configured by programming CRU_xPLL_CON2.(x=A,D,C,P,H,G)
If DSMPD = 1 (DSM is disabled, "integer mode")
FOUTVCO = (FREF / REFDIV) * FBDIV
FOUTPOSTDIV = FOUTVCO / (POSTDIV1*POSTDIV2)
When FREF is 24MHz, and if 700MHz FOUTPOSTDIV is needed. The configuration can be:

DSMPD = 1
REFDIV = 6
FBDIV = 175
POSTDIV1=1

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POSTDIV2=1
And then
FOUTVCO = (FREF / REFDIV) * FBDIV = 24/6*175=700
FOUTPOSTDIV = FOUTVCO / (POSTDIV1*POSTDIV2)=700/1/1=700
If DSMPD = 0 (DSM is enabled, "fractional mode")
FOUTVCO = (FREF / REFDIV) * (FBDIV + FRAC / (2^24))
FOUTPOSTDIV = FOUTVCO / (POSTDIV1*POSTDIV2)
When FREF is 24MHz, and if 491.52MHz FOUTPOSTDIV is needed. The configuration can be:

DSMPD = 0
REFDIV = 1
FBDIV = 40
FRAC = 24'hf5c28f
POSTDIV1=2
POSTDIV2=1

And then
FOUTVCO = (FREF / REFDIV) * (FBDIV + FRAC / (2^24)) = 983.04
FOUTPOSTDIV = FOUTVCO / (POSTDIV1*POSTDIV2)=983.04/(2*1)=491.52
POSTDIV1=0, POSTDIV2=0 are unused. We should make sure that POSTDIV1>=POSTDIV2.

2.10.1.2 PLL Setting Consideration

- If the POSTDIV value is changed during operation, a short pulse (glitch) may occur on FOUTPOSTDIV. The minimum width of the short pulse will be equal to twice the period of the VCO. Therefore, if the circuitry clocked by the PLL is sensitive to short pulses, the new divide value should be re-timed so that it is synchronous with the rising edge of the output clock (FOUTPOSTDIV). Glitches cannot occur on any of the other outputs.
- For lowest power operation, the minimum VCO and FREF frequencies should be used. For minimum jitter operation, the highest VCO and FREF frequencies should be used. The normal operating range for the VCO is described above in.
- The supply rejection will be worse at the low end of the VCO range so care should be taken to keep the supply clean for low power applications.
- The feedback divider is not capable of dividing by all possible settings due to the use of a power-saving architecture. The following settings are valid for FBDIV:
  - DSMPD=1 (Integer Mode)
  - DSMPD=0 (Fractional Mode)
- The PD input places the PLL into the lowest power mode. In this case, all analog circuits are turned off and FREF will be "ignored". The FOUTPOSTDIV and FOUTVCO pins are forced to logic low (0V).
- The BYPASS pin controls FREF to be passed to the FOUTPOSTDIV when active high. However, the PLL continues to run as it normally would if bypass were low. This is a useful feature for PLL testing since the clock path can be verified without the PLL being required to work. Also, the effect that the PLL induced supply noise has on the output buffering can be evaluated. It is not recommended to switch between BYPASS mode and normal mode for regular chip operation since this may result in a glitch. Also, FOUTPOSTDIVPD should be set low if the PLL is to be used in BYPASS mode.

2.10.1.3 PLL Frequency Change and Lock Check

PLL lock state can be checked in CRU_xPLL_CON1[10] (x=A,D,C,P,H,G) register. The lock state is high when both original hardware PLL lock and PLL counter lock are high.
The max delay time is 500*REFDIV/FREF.
PLL locking consists of three phases.

- Phase 1 is control voltage slewing. During this phase one of the clocks (reference or divide) is much faster than the other, and the PLL frequency adjusts almost continuously. When locking from power down, the divide clock is initially very slow and steadily increases frequency. It will take slightly longer for faster VCO settings when locking from power down, since the PLL must slew further.
- Phase 2 is small signal phase acquisition. During this phase, the internal up/down signals alternate semi-chaotically as the phase slowly adjusts until the two signals are

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aligned. The duration of this phase depends on the loop bandwidth and is faster with higher bandwidth. Bandwidth can be estimated as FREF / REFDIV / 20 for integer mode and FREF /REFDIV / 40 for fractional mode. The duration of small signal locking is about 1/Bandwidth.

- Phase 3 is the digital cycle count. After the last cycle slip is detected, an internal counter waits 128 FREF / REFDIV cycles before the lock signal goes high. This is frequently the dominant factor in lock time – especially for slower reference clock signals or large reference divide settings. This time can be calculated as 128*REFDIV/FREF.

2.10.2 Integer PLL Usage

2.10.2.1 PLL Frequency Configuration

FBDIV, POSTDIV1, BYPASS can be configured by programming CRU_xPLL_CON0.
DSMPD, REFDIV, POSTDIV2 can be configured by programming CRU_xPLL_CON1(x=M,N,V).
DSMPD should always be set to 1 (CLKSSCG is power down), and REFDIV can only be 1 or 2.
FOUTVCO = (FREF / REFDIV) * FBDIV
FOUTPOSTDIV = FOUTVCO / (POSTDIV1*POSTDIV2)
POSTDIV1=0, POSTDIV2=0 are unused. We should make sure that POSTDIV1>=POSTDIV2.

2.10.2.2 PLL Frequency Change and Lock Check

The PLL programming supports changed on-the-fly and the PLL will simply slew to the new frequency.
PLL lock state can be checked in CRU_xPLL_CON1[10] (x=M,N,V) register. The lock state is high when both original hardware PLL lock and PLL counter lock are high.
The max delay time is 1500*REFDIV/FREF.

2.10.3 Divider Usage

2.10.3.1 Fractional Divider Usage

To get specific frequency, clocks of 32k source UART and SAI can be generated by fractional divider. Generally you should set that denominator 20 times larger than numerator to generate precise clock frequency. So the fractional divider applies only to generate low frequency clock. For implementation issue, the input source clocks of fractional divider should limit to less than 1200MHz.

2.10.3.2 Divfree50 Divider Usage

Some modules like PDM, EMMC, SDMMC, FSPI GMAC need clock of 50% duty cycle, divfree50 can generate clock of 50% duty cycle even in odd value divisor.

2.10.4 Global Software Reset

Two global software resets are designed in RK3562, you can program CRU_GLB_SRST_FST_VALUE[15:0] as 0xfdb9 to assert the first global software reset glb_srstn_1 and program CRU_GLB_SRST_SND_VALUE[15:0] as 0xeca8 to assert the second global software reset glb_srstn_2. These two software resets are self-de-asserted by hardware. Resetting hold timing of global software reset (glb_srstn_1, glb_srstn_2, wdt_rstn, tsadc_rstn) can be programed up to 1ms.
glb_srstn_1 resets almost all logic except some registers just supporting hardware reset.
glb_srstn_2 resets almost all logic except GRFs and GPIOs.
Reset for IP in PD_PMU can be hold if its reset_hold_enable in PMUGRF_PMU_SOC_CON1 or PMUGRF_PMU_SOC_CON2 is high even if glb_srstn_1 or glb_srstn_2 active.

2.10.5 SSCG Usage

There are some scenes where SSCG should be enabled. One scene is in communication where a fixed frequency is required. Another scene is a system requiring a clock with low long-term jitter. When SSCG is used, the PLL should be configured to fractional mode firstly for spread spectrum capability.

2.10.5.1 SSCG Use Internal Point Table

Attention： XPLL means CPLL or GPLL or HPLL or VPLL or DPLL.
User can use SSCG with internal point table as following steps:

- Setting ssmod_spread(CRU_XPLL_CON3[12:8])

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andssmod_downspread(CRU_XPLL_CON3[3])

The modulation amplitude is controlled by the value of ssmod_spread. A ssmod_spread value of5'd0 turns off the modulation. A ssmod_spread value of 5'd31 (5'b11111) gives maximummodulation while a value of 5'd1gives minimum modulation.

The modulation amplitude can be calculated from the value of modulation by:

Modulation Amplitude = ±5'd(ssmod_spread)*0.1%

The modulation direction is determined by thessmod_downspread bit.

- ssmod_downspread=1'b1, down spread mode is used. If ssmod_spread = 5'd29, the maximum PLL frequency is the nominallyprogrammed value F_{NOM}, and the minimumvalue is given by F_{NOM}* (1–0.029).
- ssmod_downspread=1'b0,center spread modeis used. If ssmod_spread = 5'd29, the maximum PLL frequency would be determined by F_{NOM}*(1+0.029) and theminimum frequency by F_{NOM}* (1–0.029).

Setting the style of modulation (center versus down) and the modulation amplitude depend on the amount of EMI reduction desired and the timing margin for circuits running on the spread clock domain. The larger the spread value, the greater the reduction in EMI amplitude. However, the larger the spread value, the more timing margin needed for correct circuit operation.

- Setting ssmod_sel_ext_wave (CRU_XPLL_CON4[0])=1'b0

When use internal point table, the frequency will change as following during 128 point:

- Change from minimum value to maximum value uniformly within 64 points
- Change from maximum value to minimum value uniformly within 64 points

Spread spectrum modulator is implemented by repeating as above.

- Setting ssmod_divval(CRU_XPLL_CON3[7:4])

The frequency of modulation FMOD= FREF / (Point number*REFDIV*ssmod_divval). The FMOD is typically set above 32KHz and below the maximum frequency for modulation fidelity, which isdetermined by the PLL bandwidth. The maximum modulation frequency is conservativelyset at FREF/(200*REFDIV).

When FREF=24MHz and REFDIV= 1, the value of ssmod_divval can be 5, then the FMOD is 37.5KHz.

- Setting ssmod_bp(CRU_XPLL_CON3[0])=1'b0
- Setting ssmod_disable_sscg(CRU_XPLL_CON3[1])=1'b0
- Setting ssmod_reset(CRU_XPLL_CON3[2])=1'b0

2.10.5.2 SSCG Use External Point Table

In addition to the internal shape table, an external shape table can be used.

This enables customization tables in both shape and the number of sample points for theenvelope wave formup to 128 data points. The external table of 128 data points can be configured from CRU_SSCGTBL_CON0~CRU_SSCGTBL_CON31.

User can use SSMOD with external point table as following steps:

- Setting ssmod_spread(CRU_XPLL_CON3[12:8]) andssmod_downspread(CRU_XPLL_CON3[3]), same with internal point table usage.
- Setting ssmod_sel_ext_wave (CRU_XPLL_CON4[0])=1'b1
- Setting ssmod_ext_maxaddr(CRU_XPLL_CON4[15:8]) and table0~table127(CRU_SSCGTBL_CON0~CRU_SSCGTBL_CON31)

ssmod_ext_maxaddr is the maximum table address. For example, if the number of points describing the envelope shape is 128, the ssmod_ext_maxaddr should be configured to 127. The table address circulates over the range 0 to 127.

The table0~table127 must be 8 bit numbers in the form of sign and magnitude.

- 1.00 is represented by 8'b01111111, it is corresponded to maximum frequency.
- -1.00 is represented in the table by8'b11111111, it is corresponded to minimum frequency.
- 0.5 is represented in the table by 8'b00111111.
- -0.5is represented in the table by 8'b10111111.

The frequency will change base table0~table127 within 128 points, and then repeat.

- Setting ssmod_divval(CRU_XPLL_CON3[7:4])

The frequency of modulation FMOD= FREF/(Point number*REFDIV*ssmod_divval). The point number equals to ssmod_ext_maxaddr+1.

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- Setting ssmod_bp(CRU_XPLL_CON3[0])=1'b0
- Setting ssmod_disable_sscg(CRU_XPLL_CON3[1])=1'b0
- Setting ssmod_reset(CRU_XPLL_CON3[2])=1'b0.

Attention： XPLL means CPLL or GPLL or HPLL or VPLL or DPLL.

2.10.6 BIU Clock gating reliance

When these clocks are in use, another BIU clock must be opened, and cannot be gated. These clocks and the special clock on which they are relied are as following:

Table 2-1 BIU Clocks dependency

Clocks which have dependency	The clock which can not be gated
hclk_bus_biu pclk_bus_biu	aclk_bus_biu aclk_top_biu
hclk_peri_biu pclk_peri_biu	aclk_peri_biu
aclk_vo	aclk_top_vio_biu
pclk_core_biu	aclk_core_biu
hclk_npu_biu	aclk_npu_biu
hclk_vdpu_biu	aclk_vdpu_biu
hclk_vi_biu Pclk_vi_biu	aclk_vi_biu
pclk_vi hclk_vepu	hclk_vi
aclk_vepu_biu	aclk_vi_biu(PD_VI must be powered up)
hclk_vepu_biu	aclk_vepu_biu
hclk_vepu	hclk_vi
aclk_vdpu aclk_vi	aclk_top_vio
hclk_vo_biu	aclk_vo_biu
aclk_rga_biu	aclk_vo_biu(PD VO must be powered up)
hclk_rga_biu	aclk_rga_biu
pclk_php_biu	aclk_php_biu
pclk_ddr_biu clk_msch_brg_biu	clk_gpll_mux_to_bufddr

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Chapter 3 Power Management Unit (PMU)

3.1 Overview

In order to meet low power requirements, a power management unit (PMU) is designed for controlling power resources in RK3562. The RK3562 PMU is dedicated for managing the power of the whole chip.

PMU supports the following features:

- Support multi voltage domains: VD_PMU, VD_CORE, VD_GPU, VD_NPU, VD_LOGIC
- Support multi power domains in VD_CORE: PD_CPU_0, PD_CPU_1, PD_CPU_2, PD_CPU_3
- Support multi power domains in VD_PMU: PD_PMU1
- Support multi power domains in VD_LOGIC: PD_VI, PD_VO, PD_VEPU, PD_VDPU, PD_RGA, PD_PHP, PD_DDR
- Support PD_NPU act as power domain or voltage domain
- Support BIU idle operations: BIU_MCSH, BIU_CORE, BIU_GPU, BIU_NPU, BIU_VI, BIU_VO, BIU_RGA, BIU_VEPU, BIU_VDPU, BIU_PHP, BIU_PERI, BIU_BUS, BIU_TOP, BIU_DDRC
- Support power down power domains in default: VD_GPU, VD_NPU, PD_VI, PD_VO, PD_VEPU, PD_VDPU, PD_RGA
- Support a particular order of power on: PD_RGA should be powered off before PD_VO, PD_VEPU should be powered off before PD_VI
- Support a particular order of power off: PD_RGA should be powered on after PD_VO, PD_VEPU should be powered on after PD_VI
- Support CPU auto power down and SCU auto power down
- Support power down/up all power domains by software or hardware
- Support power down/up all voltage domains by software or hardware
- Support clock gating maskable for each domain
- Support auto clock gating domain: BUS/PERI/CORE
- Support to send idle request to BIU
- Support global interrupt disable in low power mode
- Support low frequency clock source from IO or PVTM
- Support PMU clock switch to low frequency clock in low power mode
- Support PLLs power down/up by hardware in low power mode
- Support OSC enable/disable request in low power mode
- Support to clamp all VD_PMU input before power off VD_LOGIC in low power mode
- Support wakeup reset control in power off mode
- Support DDR self-refresh in low power mode
- Support DDR controller clock auto gating in low power mode
- Support varies configurable wakeup source for low power mode
- Support sending PMU debug information to IO
- Support sending PMU sleep signals to IO
- Support PWM auto switch to GPIO during power down
- Support configurable counters: PLL lock/SCU stable/OSC stable/PWM switch/PMU sleep counter, etc.

3.2 Block Diagram

The following figure is the PMU block diagram. The PMU includes the 3 following sections:

- APB Interface and Register: Provide AMBA APB interface for register read and write
- System Power State Control: Provide power management for various low power modes
- Power Gating Control: Provide power gating control for power domains

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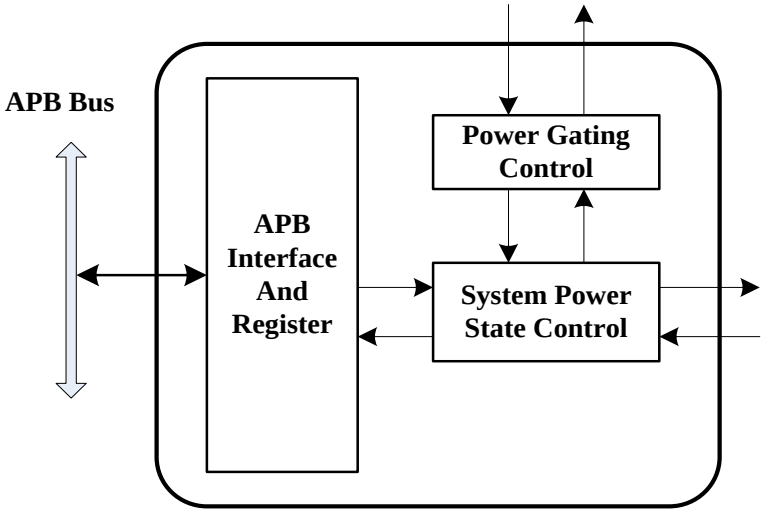


Fig.3-1 PMU Bock Diagram

3.3 Function Description

3.3.1 Domain Partition

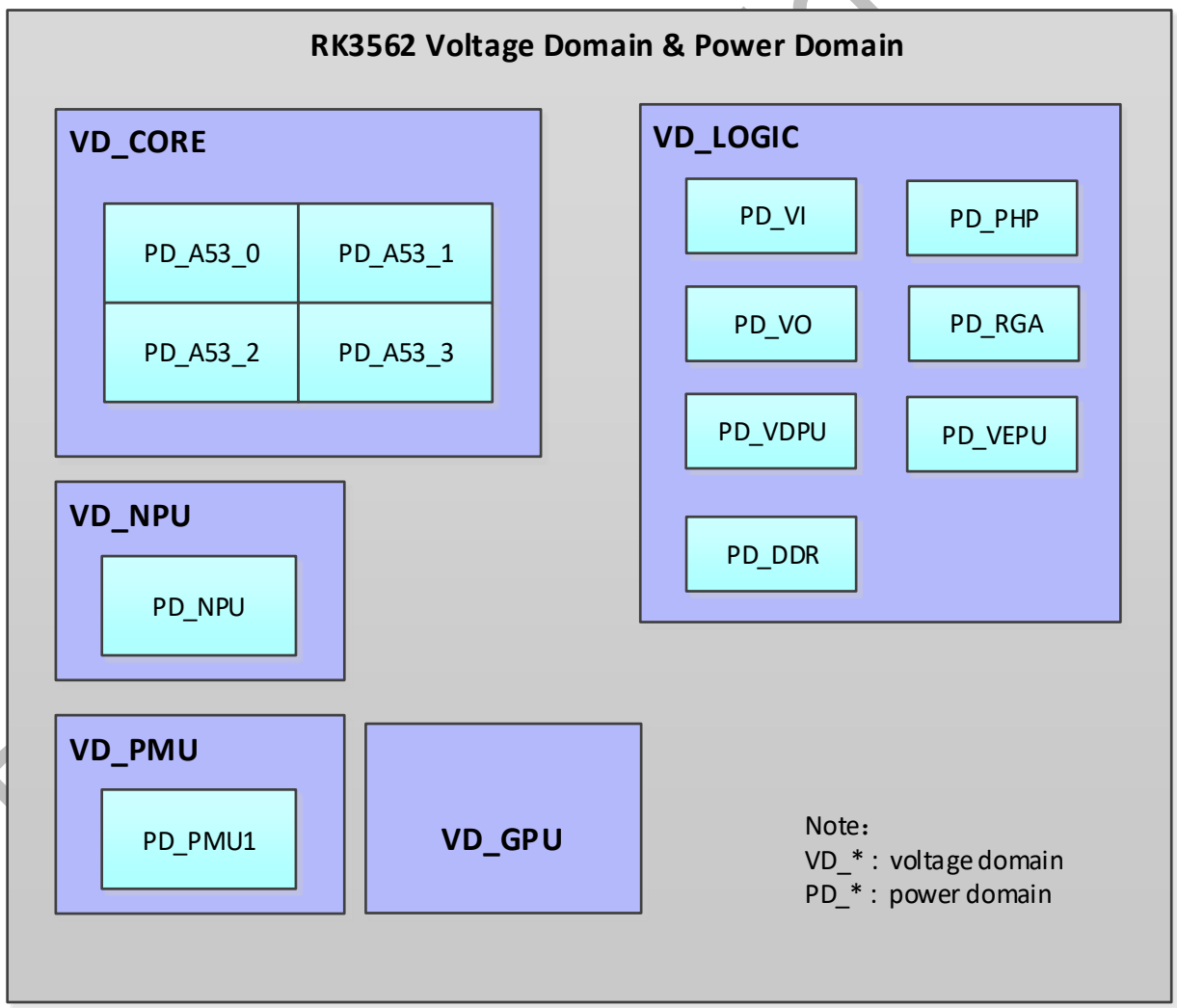


Fig.3-2 RK3562 Voltage Domain and Power Domain Partition

The above diagram describes the power domain and voltage domain partition, and the following table lists IPs in every power domain.

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Table 3-1 RK3562 Voltage Domain and Power Domain Summary

Voltage Domain	Power Domain	Description
VD_CORE	PD_CPU_0	CPU CORE 0
	PD_CPU_1	CPU CORE 1
	PD_CPU_2	CPU CORE 2
	PD_CPU_3	CPU CORE 3
	ALIVE	BIU_CPU L2 DAPLITE PVTPLL_CORE
VP_PMU	PD_PMU1	BIU_PMU PMU1_CRU PMU_SRAM CORTEXM0_PMU WDT_PMU SPI0 I2C0 UART0 PWM0 PMU1_PADRING PMU1_IOMUX
	ALIVE	PMU PMU0_CRU FRAC_CPLL I2C0 DDR_FAIL_SAFE SCRAMBLE_KEYGEN GPIO0 HPTIMER PVTM_PMU PMU_GRF/SGRF/IOC XIN24M_OSC PMU0_PADRING PMU0_IOMUX
VD_NPU	PD_NPU	BIU_NPU RKNN PVTPLL
VD_GPU	PD_GPU	BIU_GPU MALI-G57 MP6 PVTPLL
VD_LOGIC	PD_VI	BIU_VI VICAP CSIHOST INNO_CSIPHY0_WRAPPER ISP
	PD_VO	BIU_VO VOP
	PD_RGA	BIU_RGA RGA RKDJPEG
	PD_VDPU	BIU_VDPU RKVDEC
	PD_VEPU	BIU_VEPU RKVENC

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Voltage Domain	Power Domain	Description
	PD_PHP	BIU_PHP USB3OTG PCIE PIPE_PHY_WRAPPER
	PD_DDR	BIU_MSCH MSCH FRAC_DPLL AXI_SPLIT UMCTL2 DFICTRL DFI MONITOR HW_LP_CTRL DDR_LPCKCTL DDR_DQ_SWAP DDR_SCRAMBLE DDR_GRF
	ALIVE	[PD_BUS] BIU_BUS CORTEXM0_TOP SPINLOCK GIC400 DECOM DCF GMAC SYS_GRF/SGRF TIMER_NS WDT_NS TSADC SARADC I2C1~5 MAILBOX DFT2APB APB2ASB

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Voltage Domain	Power Domain	Description
		[PD_PERI] BIU_PERI DMAC_0 RKDMA DSIHOST_WRAPPER SCRYPTO RK_RNG SEC_TRNG_S/NS KEY_READER OTPC_S/NS OTPC_LOCK_ARB INT_MEM AHB_ROM SAI0~2 RK_DSM PDM SPDIF_8CH SDMMC0~1 EMMC SFC_TOP USB2HOST SPI1~2 UART1~9 PWM1~3 WDT_S PERI_GRF CAN0~1 GPIO1~2 APB_SARADC SARADC_WRAPPER OTP_WRAPPER USBPHY_COMB_WRAPPER INNO_DSIPHY_WRAPPER
		[TOP] BIU_TOP CRU APB2ASB GPIO3~4 SARADCPHY0~1 TSADCPHY OTPPHY PIPEPHY USB2PHY DSIPHY CSIPHY0~1 TM_DECODER DDR_PHY PVTPLL_CRU PLLs

3.3.2 Operation Mode

First of all, we define two operation modes of PMU, normal mode and low power mode.

When operating at normal mode, that means software can manage power sources directly by accessing PMU registers. For example, CPU or MCU_PMU can write PMU2_PWR_GATE_CON0 register to determine that power off/on which power domain independently.

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When operating at low power mode, software manages power sources indirectly through FSM (Finite States Machine) in PMU and those settings always not take effect immediately. That means software also can configure PMU registers to power down/up some power resources, but these setting will not be executed immediately after configuration. They will be delayed to execute after FSM running in particular phase.
To enter low power mode, after setting some power configurations, the PMU1_PWR_CON1[0] bit must be set 1 to enable PMU FSM. Then CPU needs to execute a WFI command to perform ready signal. After PMU detects all CPUs in WFI status, the FSM will be fetched. And the specific power sources will be controlled during specific status in FSM. So, the low power mode is a "delay affect" way to handle power sources inside the RK3562 chip.

3.3.3 Low Power Mode

There are 2 low power modes defined for RK3562: Power mode 0, Power mode 1.
Power mode 0: Ultra low power mode. In this power mode, all logic except ALIVE in VD_PMU can be power off or power down. Chip can be waked up by GPIO interrupt triggered by IO in PMUIO0 domain.
Power mode 1: Low power mode. In this power mode, all logic except ALIVE and PD_PMU1 in VD_PMU can be power off or power down. Chip can be waked up by GPIO interrupt triggered by IO in PMUIO0 and PMUIO1 domain or other wake up source from PD_PMU1 when in hardware power mode, or wake up by MCU_PMU when in hardware power mode.

3.4 Register Description

RK3562 PMU registers are divided into 3 parts for flexible applications:
- Offset = 0x0000~0x3FFF: registers defined in PMU0;
- Offset = 0x4000~0x7FFF: registers defined in PMU1;
- Offset = 0x8000~0xBFFF: registers defined in PMU2.

3.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PMU0_PWR_CON0	0x0000	W	0x00000000	PMU power control 0 register
PMU0_WAKEUP_INT_ST	0x000C	W	0x00000000	PMU wake up interrupt status register for power mode 0
PMU0_INFO_TX_CON	0x0030	W	0x00000000	PMU debug information transmit control register
PMU1_VERSION	0x4000	W	0x00003562	PMU version register
PMU1_PWR_CON1	0x4004	W	0x00000000	PMU power control 1 register
PMU1_GLB_POWER_STS	0x4008	W	0x00000000	PMU global power status register
PMU1_INT_MASK_CON	0x400C	W	0x00000000	PMU interrupt mask control register
PMU1_WAKEUP_INT_CON	0x4010	W	0x00000000	PMU wake up interrupt control register
PMU1_WAKEUP_INT_STS	0x4014	W	0x00000000	PMU wake up interrupt status register
PMU1_WAKEUP_EDGE_CON	0x4018	W	0x00000000	PMU wake up edge control register
PMU1_WAKEUP_EDGE_ST	0x401C	W	0x00000000	PMU wake up edge status register
PMU1_DDR_CH0_PWR_CON	0x4020	W	0x00000000	DDR channel 0 hardware power control register
PMU1_DDR_CH0_PWR_SFTCON	0x4030	W	0x00000000	DDR channel 0 software power control register
PMU1_DDR_POWER_STS	0x4040	W	0x00000000	DDR power state register
PMU1_DDR_STS	0x4044	W	0x00000000	DDR state register
PMU1_CRU_PWR_CON	0x4050	W	0x00000000	Clock and reset hardware power control register
PMU1_CRU_PWR_SFTCON	0x4054	W	0x00000000	Clock and reset software power control register

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Name	Offset	Size	Reset Value	Description
PMU1_CRU_POWER_STS	0x4058	W	0x00000000	Clock and reset power state register
PMU1_PLLPD_CON0	0x4060	W	0x00000000	PLL hardware power control register 0
PMU1_PLLPD_SFTCON0	0x4068	W	0x00000000	PLL software power control register 0
PMU1_PMIC_STABLE_CNT	0x4080	W	0x000FFFFF	PMIC stable count register
PMU1_OSC_STABLE_CNT	0x4084	W	0x000FFFFF	Oscillator stable count register
PMU1_WAKEUP_RST_CLR_CNT	0x4088	W	0x000FFFFF	Wake up reset clear count register
PMU1_PLL_LOCK_CNT	0x408C	W	0x000FFFFF	PLL lock count register
PMU1_WAKEUP_TIMEOUT_CNT	0x4094	W	0x00005DC0	PMU wake up timeout count register
PMU1_PWM_SWITCH_CNT	0x4098	W	0x000FFFFF	PWM switch stable count register
PMU1_SLEEP_CNT	0x409C	W	0x00000000	PMU sleep count register
PMU2_SCU_PWR_CON0	0x8000	W	0x00000000	SCU power control register
PMU2_SCU_PWR_SFTCON	0x8004	W	0x00000000	SCU power control software register
PMU2_SCU_AUTO_PWR_CON	0x8008	W	0x00000000	SCU auto power control register
PMU2_SCU_PWR_STATE	0x800C	W	0x00000000	SCU power status register
PMU2_CPU_AUTO_PWR_CON	0x8010	W	0x00000000	CPU auto power control register
PMU2_CPU_PWR_SFTCON	0x8014	W	0x00000000	CPU power control software register
PMU2_DBG_PWR_CON	0x8018	W	0x00000000	CPU debug power control register
PMU2_CLUSTER_PWR_ST	0x801C	W	0x00000000	CLUSTER status register
PMU2_CLUSTER_IDLE_CON	0x8020	W	0x00000000	ClUSTER idle control register
PMU2_CLUSTER_IDLE_SFTCON	0x8024	W	0x00000000	ClUSTER idle control software register
PMU2_SCU_STABLE_CNT	0x8030	W	0x000FFFFF	SCU power stable counter
PMU2_SCU_PWRUP_CNT	0x8034	W	0x00005DC0	SCU power up stable counter
PMU2_SCU_PWRDN_CNT	0x8038	W	0x00005DC0	SCU power down stable counter
PMU2_SCU_VOLUP_CNT	0x803C	W	0x00005DC0	SCU voltage up stable counter
PMU2_SCU_VOLDN_CNT	0x8040	W	0x00005DC0	SCU voltage down stable counter
PMU2_BIU_IDLE_CON0	0x8100	W	0x00000000	BIU idle request hardware control register 0
PMU2_BIU_IDLE_SFTCON0	0x8110	W	0x00000000	BIU idle request software control register 0
PMU2_BIU_IDLE_ACK_STS0	0x8120	W	0x00000000	BIU idle acknowledge status register 0
PMU2_BIU_IDLE_STS0	0x8128	W	0x00000000	BIU idle status register 0
PMU2_BIU_AUTO_CON0	0x8130	W	0x00000000	BIU automatic clock gating control register 0
PMU2_BIU_AUTO_SFTCON0	0x8140	W	0x00000000	BIU software clock gating control register 0
PMU2_PWR_GATE_CON0	0x8200	W	0x00000000	Power domain hardware power control register 0
PMU2_PWR_GATE_SFTCON0	0x8210	W	0x0000007F	Power domain software power control register 0
PMU2_VOL_GATE_CON0	0x8220	W	0x00000003	Voltage domain power control register 0

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Name	Offset	Size	Reset Value	Description
PMU2_PWR_GATE_STS0	0x8230	W	0x000000FF	Power domain power status register 0
PMU2_PWR_GATE_POWER_STS	0x8238	W	0x00000000	Power gating status register
PMU2_MEM_SD_SFTCON0	0x8300	W	0x0000FFFF	memory sd control register 0
PMU2_MEM_SD_SFTCON1	0x8304	W	0x000000FF	memory sd control register 1

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

3.4.2 Detail Registers Description

PMU0_PWR_CON0

Address: Operational Base(0xFF250000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	biu_auto_pmu1 When perform idle operation, BIU_PMU1 corresponding clock can be opened or gated automatically. 1'b0: Disable 1'b1: Enable
12	RW	0x0	pmu1_bus_idle_sftena Enable sending idle request to BIU_PMU1 by software. 1'b0: Disable 1'b1: Enable
11	RW	0x0	pmu1_bus_idle_ena Enable sending idle request to BIU_PMU1 by hardware. 1'b0: Disable 1'b1: Enable
10	RO	0x0	reserved
9	RW	0x0	pmu1_pwr_gate_sftena Enable power down PD_PMU1 by software. 1'b0: Disable 1'b1: Enable
8	RW	0x0	pmu1_pwr_gate_ena Enable power down PD_PMU1 by hardware. 1'b0: Disable 1'b1: Enable
7:3	RO	0x00	reserved
2	RW	0x0	pmu1_bus_bypass Bypass BIU_PMU1 idle flow in power mode 0 procedure. 1'b0: Disable 1'b1: Enable
1	RW	0x0	pmu1_pwr_bypass Bypass PD_PMU1 power gating flow in power mode 0 procedure. If asserted, PD_PMU1 is not power down or power up during power mode 0 procedure. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
0	R/WSC	0x0	powermode0_en Power mode 0 (minimal power status) enable. When controller enters power mode 0 procedure, this bit is automatically cleared. 1'b0: Disable 1'b1: Enable

PMU0_WAKEUP_INT_ST

Address: Operational Base(0xFF250000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	wakeup_int_st Power mode 0 wake up source status. 1'b0: Inactive 1'b1: Active

PMU0_INFO_TX_CON

Address: Operational Base(0xFF250000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	info_tx_en Enable PMU debug information transition. 1'b0: Disable 1'b1: Enable
7:0	RW	0x00	info_tx_intv_time The interval time between the bytes of PMU debug information.

PMU1_VERSION

Address: Operational Base(0xFF254000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RO	0x00003562	version PMU version

PMU1_PWR_CON1

Address: Operational Base(0xFF254000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	sleep_cnt_en Enable sleep_cnt in power mode 1 procedure when PMU is in ST_SLEEP. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
12	RW	0x0	wfi_bypass Bypass WFI in power mode 1 procedure. If asserted, PMU FSM does not need to wait for CPU standbywfi state before entering low power flow. 1'b0: Disable 1'b1: Enable
11:10	RO	0x0	reserved
9	RW	0x0	pdpmu1_bypass Bypass pd_pmu1 low power flow in power mode 1 procedure. 1'b0: Disable 1'b1: Enable
8	RW	0x0	qch_bypass Bypass power Q-Channel low power flow in power mode 1 procedure. If asserted, PMU_QCHANNEL_PWR_CON cannot take effect for power Q-Channel low power flow. If you want to execute power Q-Channel low power flow, you can program PMU_QCHANNEL_PWR_SFTCON through software flow. 1'b0: Disable 1'b1: Enable
7	RW	0x0	cru_bypass Bypass clock and reset low power flow in power mode 1 procedure. If asserted, PMU_CRU_PWR_CON cannot take effect for clock and reset low power flow. If you want to execute clock and reset low power flow, you can program PMU_CRU_PWR_SFTCON through software flow. 1'b0: Disable 1'b1: Enable
6	RW	0x0	pwrgate_bypass Bypass power gating flow in power mode 1 procedure. If asserted, PMU_PWR_GATE_CON0/1/2 cannot take effect for power gating flow. If you want to execute power gating flow, you can program PMU_PWR_GATE_SFTCON0/1/2 through software flow. 1'b0: Disable 1'b1: Enable
5	RW	0x0	ddr_bypass Bypass DDR low power flow in power mode 1 procedure. If asserted, PMU_DDR_CH0/1/2/3_PWR_CON cannot take effect for DDR low power flow. If you want to execute DDR low power flow, you can program PMU_DDR_CH0/1/2/3_PWR_SFTCON through software flow. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
4	RW	0x0	bus_bypass Bypass BIU idle request in power mode 1 procedure. If asserted, PMU_BIU_IDLE_CON0/1/2 cannot take effect for BIU idle request. If you want to execute BIU idle request, you can program PMU_BIU_IDLE_SFTCON0/1/2 through software flow. 1'b0: Disable 1'b1: Enable
3:2	RO	0x0	reserved
1	RW	0x0	scu_bypass Bypass SCU low power flow in power mode 1 procedure. 1'b0: Disable 1'b1: Enable
0	R/WSC	0x0	powermode1_en Power mode 1 enable. When controller enters power mode 1 procedure. It is automatically cleared after PMU enters power mode 1 procedure. 1'b0: Disable 1'b1: Enable

PMU1_GLB_POWER_STS

Address: Operational Base(0xFF254000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RO	0x0	power_state PMU1 global power state. 4'h0: Normal state 4'h1: Core low power state 4'h2: Cluster low power state 4'h3: Q-Channel low power state 4'h4: Bus low power state 4'h5: DDR low power state 4'h6: Power gating low power state 4'h7: Clock and reset low power state 4'h8: Sleep state 4'h9: Clock and reset active state 4'ha: Power gating active state 4'hb: DDR active state 4'hc: Bus active state 4'hd: Q-Channel active state 4'hd: Cluster active state 4'hf: Core active state

PMU1_INT_MASK_CON

Address: Operational Base(0xFF254000) + offset (0x000C)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	R/WSC	0x0	glb_int_mask Global interrupt mask during SCU sleep state. Cleared when SCU is active. 1'b0: Interrupt is not mask 1'b1: Interrupt is mask

PMU1_WAKEUP_INT_CON

Address: Operational Base(0xFF254000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	wakeup_timeout_en Enable PMU wake up timeout as wake up source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
16	RW	0x0	wakeup_sys_int_en Enable system interrupt as wake up source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
15	RW	0x0	wakeup_hptimer_int_en Enable PMU_HPTIMER interrupt as wake up source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
14	RW	0x0	wakeup_timer_int_en Enable TIMER0 interrupt as wake up source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
13	RW	0x0	wakeup_pwm0_pwr_int_en Enable PWM0_pwr interrupt as wake up source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
12	RW	0x0	wakeup_pwm0_int_en Enable PWM0 interrupt as wake up source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
11	RW	0x0	wakeup_uart0_int_en Enable UART0 interrupt as wake up source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
10	RW	0x0	wakeup_usb_int_en Enable USB detect interrupt as wake up source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
9	RW	0x0	wakeup_sdio_int_en Enable SDIO interrupt as wake up source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
8	RW	0x0	wakeup_pcie_int_en Enable PCIE interrupt as wake up source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
7	RW	0x0	wakeup_sdmmc1_int_en Enable SDMMC1 detect interrupt as wake up source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
6	RW	0x0	wakeup_sdmmc0_int_en Enable SDMMC0 detect interrupt as wake up source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
5	RW	0x0	wakeup_gpio0_int_exp_en Enable GPIO0 exp interrupt as wake up source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
4	RW	0x0	wakeup_gpio0_int_en Enable GPIO0 interrupt as wake up source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
3	RW	0x0	wakeup_cpu3_int_en Enable CPU3 interrupt as wake up source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
2	RW	0x0	wakeup_cpu2_int_en Enable CPU2 interrupt as wake up source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
1	RW	0x0	wakeup_cpu1_int_en Enable CPU1 interrupt as wake up source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
0	RW	0x0	wakeup_cpu0_int_en Enable CPU0 interrupt as wake up source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable

PMU1_WAKEUP_INT_STS

Address: Operational Base(0xFF254000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RO	0x0	wakeup_timeout_st Wake up timeout as wake up source status. 1'b0: Inactive 1'b1: Active
16	RO	0x0	wakeup_sys_int_st System interrupt as wake up source status. 1'b0: Inactive 1'b1: Active
15	RO	0x0	wakeup_hptimer_int_st PMU_HPTIMER interrupt as wake up source status. 1'b0: Inactive 1'b1: Active
14	RO	0x0	wakeup_timer_int_st TIMER0 interrupt as wake up source status. 1'b0: Inactive 1'b1: Active
13	RO	0x0	wakeup_pwm0_pwr_int_st PWM0_pwr interrupt as wake up source status. 1'b0: Inactive 1'b1: Active
12	RO	0x0	wakeup_pwm0_int_st PWM0 interrupt as wake up source status. 1'b0: Inactive 1'b1: Active

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Bit	Attr	Reset Value	Description
11	RO	0x0	wakeup_uart0_int_st UART0 interrupt as wake up source status. 1'b0: Inactive 1'b1: Active
10	RO	0x0	wakeup_usb_int_st USB interrupt as wake up source status. 1'b0: Inactive 1'b1: Active
9	RO	0x0	wakeup_sdio_int_st SDIO interrupt as wake up source status. 1'b0: Inactive 1'b1: Active
8	RW	0x0	wakeup_pcie_int_st PCIE interrupt as wake up source status. 1'b0: Inactive 1'b1: Active
7	RO	0x0	wakeup_sdmmc1_int_st SDMMC1 interrupt as wake up source status. 1'b0: Inactive 1'b1: Active
6	RO	0x0	wakeup_sdmmc0_int_st SDMMC0 interrupt as wake up source status. 1'b0: Inactive 1'b1: Active
5	RO	0x0	wakeup_gpio0_exp_int_st GPIO0_exp interrupt as wake up source status. 1'b0: Inactive 1'b1: Active
4	RO	0x0	wakeup_gpio0_int_st GPIO0 interrupt as wake up source status. 1'b0: Inactive 1'b1: Active
3	RO	0x0	wakeup_cpu3_int_st CPU3 interrupt as wake up source status. 1'b0: Inactive 1'b1: Active
2	RO	0x0	wakeup_cpu2_int_st CPU2 interrupt as wake up source status. 1'b0: Inactive 1'b1: Active
1	RO	0x0	wakeup_cpu1_int_st CPU1 interrupt as wake up source status. 1'b0: Inactive 1'b1: Active

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Bit	Attr	Reset Value	Description
0	RO	0x0	wakeup_cpu0_int_st CPU0 interrupt as wake up source status. 1'b0: Inactive 1'b1: Active

PMU1_WAKEUP_EDGE_CON

Address: Operational Base(0xFF254000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	edge_wakeup_en Enable both posedge and negedge of GPIO0 pins as wakeup source. Each pin has independent control bit. 1'b0: Disable 1'b1: Enable

PMU1_WAKEUP_EDGE_ST

Address: Operational Base(0xFF254000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	edge_status Edge interrupt wakeup status. Each pin has independent control bit. 1'b0: Inactive 1'b1: Active

PMU1_DDR_CH0_PWR_CON

Address: Operational Base(0xFF254000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10	RW	0x0	ddrphy_auto_gating_ena Enable DDRPHY auto clock gating. DDRPHY's clock can be gated when in sleep mode. 1'b0: Disable 1'b1: Enable
9	RW	0x0	ddrctl_c_auto_gating_ena Enable DDRCTRL's core-clock auto clock gating. Core-clock can be gated when in self-refresh mode. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
8	RW	0x0	ddrctl_a_auto_gating_ena Enable DDRCTRL's AXI-clock auto clock gating. AXI-clock can be gated when in self-refresh mode. 1'b0: Disable 1'b1: Enable
7	RW	0x0	ddrio_rstiov_exit_ena Enable DDR exits retention mode through RST_IOV by hardware. 1'b0: Disable 1'b1: Enable
6	RW	0x0	ddrio_rstiov_enter_ena Enable DDR enters retention mode through RST_IOV by hardware. 1'b0: Disable 1'b1: Enable
5	RW	0x0	ddrio_reton_exit_ena Enable DDR exits retention mode through RETON/RETOFF by hardware. 1'b0: Disable 1'b1: Enable
4:3	RO	0x0	reserved
2	RW	0x0	ddrio_reton_enter_ena Enable DDR enters retention mode through RETON/RETOFF by hardware. 1'b0: Disable 1'b1: Enable
1	RW	0x0	ddr_sref_a_ena Enable DDR self-refresh mode for AXI-clock domain by hardware. 1'b0: Disable 1'b1: Enable
0	RW	0x0	ddr_sref_c_ena Enable DDR self-refresh mode for core-clock domain by hardware. 1'b0: Disable 1'b1: Enable

PMU1_DDR_CH0_PWR_SFTCON

Address: Operational Base(0xFF254000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11	RW	0x0	ddrctl_c_active_wait_enter 1'b0: Not need to wait for ddrctl_c_active low before FSM enter self-refresh state 1'b1: Need to wait for ddrctl_c_active low before FSM enter self-refresh state
10	RW	0x0	ddrctl_a_active_wait_exit 1'b0: Not need to wait for ddrctl_a_active high before FSM exit self-refresh state 1'b1: Need to wait for ddrctl_a_active high before FSM exit self-refresh state
9	RW	0x0	ddrctl_c_active_wait_exit 1'b0: Not need to wait for ddrctl_c_active high before FSM exit self-refresh state 1'b1: Need to wait for ddrctl_c_active high before FSM exit self-refresh state
8	RW	0x0	ddrctl_a_active_wait_enter 1'b0: Not need to wait for ddrctl_a_active low before FSM enter self-refresh state 1'b1: Need to wait for ddrctl_a_active low before FSM enter self-refresh state
7	R/W SC	0x0	ddrio_rstiov_exit_sftena Enable DDR exits retention mode through RST_IOV by software. It is auto cleared after DDR exits retention mode. 1'b0: Disable 1'b1: Enable
6	RW	0x0	ddrio_rstiov_enter_sftena Enable DDR enters retention mode through RST_IOV by software. 1'b0: Disable 1'b1: Enable
5	R/W SC	0x0	ddrio_reton_exit_sftena Enable DDR exits retention mode through RETON/RETOFF by software. It is auto cleared after DDR exits retention mode. 1'b0: Disable 1'b1: Enable
4:3	RO	0x0	reserved
2	RW	0x0	ddrio_reton_enter_sftena Enable DDR enters retention mode through RETON/RETOFF by software. 1'b0: Disable 1'b1: Enable
1	RW	0x0	ddr_sref_a_sftena Enable DDR self-refresh mode for AXI-clock domain by software. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
0	RW	0x0	ddr_sref_c_sftena Enable DDR self-refresh mode for core-clock domain by software. 1'b0: Disable 1'b1: Enable

PMU1_DDR_POWER_STS

Address: Operational Base(0xFF254000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RO	0x0	ddr_power_state DDR power state. 4'h0: Normal state 4'h1: Enter self-refresh mode for AXI-clock state 4'h2: Enter self-refresh mode core-clock state 4'h3: Enter retention mode through RETON/RETOFF state 4'h4: Enter retention mode through RST_IOV state 4'h5: Sleep state 4'h6: Exit retention mode through RST_IOV state 4'h7: Exit retention mode through RETON/RETOFF state 4'h8: Exit self-refresh mode for core-clock state 4'h9: Exit self-refresh mode for AXI-clock state Others: Reserved

PMU1_DDR_STS

Address: Operational Base(0xFF254000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RO	0x0	ddr_ch0_io_rstiov DDR RST_IOV state for channel 0. 1'b0: Inactive 1'b1: Active
4	RO	0x0	ddrctrl_ch0_a_sysactive DDRC AXI clock active for channel 0. 1'b0: Active 1'b1: Inactive
3	RO	0x0	ddrctrl_ch0_a_sysack DDRC AXI hardware low-power request acknowledge for channel 0. 1'b0: Active 1'b1: Inactive
2	RO	0x0	ddr_ch0_io_reton DDR RETON/RETOFF state for channel 0. 1'b0: Inactive 1'b1: Active

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Bit	Attr	Reset Value	Description
1	RO	0x0	ddrctrl_ch0_c_sysactive DDRC hardware low-power clock active for channel 0. 1'b0: Active 1'b1: Inactive
0	RO	0x0	ddrctrl_ch0_c_sysack DDRC hardware low-power request acknowledge for channel 0. 1'b0: Active 1'b1: Inactive

PMU1_CRU_PWR_CON

Address: Operational Base(0xFF254000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	pd_peri_clk_src_gate_ena Gating BIU_PERI's clock source during clock low power mode. 1'b0: Disable 1'b1: Enable
10	RW	0x0	pd_bus_clk_src_gate_ena Gating BIU_BUS's clock source during clock low power mode. 1'b0: Disable 1'b1: Enable
9	RW	0x0	power_off_io_ena Enable VCCIO enter low power mode by hardware. 1'b0: Disable 1'b1: Enable
8	RW	0x0	pwm_switch_iout PWM output. 1'b0: Disable 1'b1: Enable It is set 0 for RK3588.
7	RW	0x0	pwm_gpio_ioe_ena PWM output enable. 1'b0: Disable 1'b1: Enable It is set 0 for RK3588.
6	RW	0x0	pwm_switch_ena PWM switch enable. 1'b0: Disable 1'b1: Enable It is set 0 for RK3588.

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Bit	Attr	Reset Value	Description
5	RW	0x0	power_off_ena Enable chip power off by hardware. 1'b0: Disable 1'b1: Enable
4	RW	0x0	alive_osc_ena Enable clk_pmu/hclk_pmu/pclk_pmu switch to oscillator by hardware. When alive_32k_ena is asserted, this bit is ignored. 1'b0: Disable 1'b1: Enable
3	RW	0x0	input_clamp_ena Enable VD_PMU input clamped by hardware. 1'b0: Disable 1'b1: Enable
2	RW	0x0	wakeup_rst_ena Enable wake up reset by hardware. If asserted, all registers without reset hold will be reset after chip wake up. 1'b0: Disable 1'b1: Enable
1	RW	0x0	osc_dis_ena Disable oscillator by hardware. 1'b0: Enable 1'b1: Disable
0	RW	0x0	alive_32k_ena Enable pclk_pmu and clk_pmu switch to 32KHz clock by hardware. 1'b0: Disable 1'b1: Enable

PMU1_CRU_PWR_SFTCON

Address: Operational Base(0xFF254000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	power_off_io_sftena Enable VCCIO enter low power mode by software. 1'b0: Disable 1'b1: Enable
5	RW	0x0	power_off_sftena Enable chip power off by software. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
4	RW	0x0	alive_osc_sftena Enable clk_pmu/hclk_pmu/pclk_pmu switch to oscillator by software. When alive_32k_ena is asserted, this bit is ignored. 1'b0: Disable 1'b1: Enable
3	RW	0x0	input_clamp_sftena Enable VD_PMU input clamp by software. 1'b0: Disable 1'b1: Enable
2	RW	0x0	wakeup_rst_sftena Enable wake up reset by software. If asserted, all digital except IP with reset hold will be reset. 1'b0: Disable 1'b1: Enable
1	RW	0x0	osc_dis_sftena Disable oscillator by software. 1'b0: Enable 1'b1: Disable
0	RW	0x0	alive_32k_sftena Enable pclk_pmu and clk_pmu switch to 32KHz clock by software. 1'b0: Disable 1'b1: Enable

PMU1_CRU_POWER_STS

Address: Operational Base(0xFF254000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RO	0x0	cru_power_state Clock and reset power state. 4'h0: Normal state 4'h1: Clock low frequency state 4'h2: PLL power down state 4'h3: Input clamp state 4'h4: Oscillator disable state 4'h5: Sleep state 4'h6: Wake up state 4'h7: Input clamp release state 4'h8: Oscillator enable state 4'h9: Clock high frequency state 4'ha: Wake up reset clear state 4'hc: PLL power up state Others: Reserved

PMU1_PLLPD_CON0

Address: Operational Base(0xFF254000) + offset (0x0060)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	vpll_pd_ena Enable power down VPLL by hardware. 1'b0: Disable 1'b1: Enable
4	RW	0x0	hpll_pd_ena Enable power down HPLL by hardware. 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpll_pd_ena Enable power down GPLL by hardware. 1'b0: Disable 1'b1: Enable
2	RW	0x0	cpll_pd_ena Enable power down CPLL by hardware. 1'b0: Disable 1'b1: Enable
1	RW	0x0	dpll_pd_ena Enable power down DPLL by hardware. 1'b0: Disable 1'b1: Enable
0	RW	0x0	apll_pd_ena Enable power down APLL by hardware. 1'b0: Disable 1'b1: Enable

PMU1_PLLPD_SFTCON0

Address: Operational Base(0xFF254000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	vpll_pd_sftena Enable power down VPLL by software. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
4	RW	0x0	hpll_pd_sftena Enable power down HPLL by software. 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpll_pd_sftena Enable power down GPLL by software. 1'b0: Disable 1'b1: Enable
2	RW	0x0	cpll_pd_sftena Enable power down CPLL by software. 1'b0: Disable 1'b1: Enable
1	RW	0x0	dpll_pd_sftena Enable power down DPLL by software. 1'b0: Disable 1'b1: Enable
0	RW	0x0	apll_pd_sftena Enable power down APLL by software. 1'b0: Disable 1'b1: Enable

PMU1_PMIC_STABLE_CNT

Address: Operational Base(0xFF254000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	pmic_stable_cnt PMIC stable count for mode 1 procedure. Number of clk_pmu used by counter logic.

PMU1_OSC_STABLE_CNT

Address: Operational Base(0xFF254000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	osc_stable_cnt Oscillator stable count for mode 1 procedure. Number of clk_pmu used by counter logic.

PMU1_WAKEUP_RST_CLR_CNT

Address: Operational Base(0xFF254000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	wakeup_rst_clr_cnt Wake up reset clear count for mode 1 procedure. Number of clk_pmu used by counter logic.

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PMU1_PLL_LOCK_CNT

Address: Operational Base(0xFF254000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	pll_lock_cnt Count for PLL from power up to lock. Number of clk_pmu used by counter logic.

PMU1_WAKEUP_TIMEOUT_CNT

Address: Operational Base(0xFF254000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:0	RW	0x00005dc0	wakeup_timeout_cnt Wake up timeout count. Number of clk_pmu used by counter logic.

PMU1_PWM_SWITCH_CNT

Address: Operational Base(0xFF254000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	pwm_switch_cnt PWM switch count. Number of clk_pmu used by counter logic.

PMU1_SLEEP_CNT

Address: Operational Base(0xFF254000) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sleep_cnt_thresh PMU sleep counter thresh. Number of clk_pmu used by counter logic. The counter start counting when PMU is in ST_SLEEP and sleep_cnt_en is enable. After counter equal to counter thresh, PMU can be waked up by wakeup_source.

PMU2_SCU_PWR_CON0

Address: Operational Base(0xFF258000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	cluster_clk_src_gate_ena Enable Cluster clock gate by hardware. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
6	RW	0x0	scu_vol_gate_ena Enable SCU voltage gate by hardware. 1'b0: Disable 1'b1: Enable
5	RW	0x0	cluster_cpu_pwrdn_ena Enable all cpu power down by hardware. 1'b0: Disable 1'b1: Enable
4	RO	0x0	reserved
3	RW	0x0	scu_pwroff_ena Enable SCU power off by hardware. Indicate the PMIC to cut off the scu power. 1'b0: Disable 1'b1: Enable
2	RW	0x0	scu_pwrdn_ena Enable SCU power down by hardware. 1'b0: Disable 1'b1: Enable
1	RW	0x0	l2_idle_ena Enable sending l2 idle request by hardware. 1'b0: Disable 1'b1: Enable
0	RW	0x0	l2_flush_ena Enable sending l2 flush request by hardware. 1'b0: Disable 1'b1: Enable

PMU2_SCU_PWR_SFTCON

Address: Operational Base(0xFF258000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	scu_pwroff_cfg Enable SCU power off by software. 1'b0: Disable 1'b1: Enable
2	RW	0x0	scu_pwrdn_req_cfg Enable SCU power down by software. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
1	RW	0x0	acinactm_cluster_cfg Enable sending l2 idle request by software. 1'b0: Disable 1'b1: Enable
0	RW	0x0	l2flushreq_cluster_cfg Enable sending l2 flush request by software. 1'b0: Disable 1'b1: Enable

PMU2_SCU_AUTO_PWR_CON

Address: Operational Base(0xFF258000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	scu_sft_wakeup_cluster_ena SCU software wakeup enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	scu_int_mask_ena SCU interrupt mask enable. 1'b0: Disable 1'b1: Enable
1	RW	0x0	scu_int_wakeup_cluster_ena SCU interrupt wakeup enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	scu_lp_en Enable SCU low-power procedure by hardware. Start when all core enter WFI, Cleared when SCU wakeup. 1'b0: Disable 1'b1: Enable

PMU2_SCU_PWR_STATE

Address: Operational Base(0xFF258000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
3:0	RO	0x0	scu_power_state SCU power state. 4'h0: SCU normal state 4'h1: CPU power down state 4'h4: Cluster transfer idle state 4'h5: SCU power down state 4'h6: SCU sleep state 4'h7: SCU wakeup state 4'h8: SCU power up state 4'h9: Cluster transfer resume state 4'ha: CPU power up state Others: Reserved

PMU2_CPU_AUTO_PWR_CON

Address: Operational Base(0xFF258000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	cpu3_sft_wakeup_cluster_ena CPU3 software wakeup enable. 1'b0: Disable 1'b1: Enable
14	RW	0x0	cpu3_int_mask_ena CPU3 interrupt mask enable. 1'b0: Disable 1'b1: Enable
13	RW	0x0	cpu3_int_wakeup_ena CPU3 interrupt wakeup enable. 1'b0: Disable 1'b1: Enable
12	RW	0x0	cpu3_auto_pwrdn_ena CPU3 auto power down enable. 1'b0: Disable 1'b1: Enable
11	RW	0x0	cpu2_sft_wakeup_cluster_ena CPU2 software wakeup enable. 1'b0: Disable 1'b1: Enable
10	RW	0x0	cpu2_int_mask_ena CPU2 interrupt mask enable. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
9	RW	0x0	cpu2_int_wakeup_ena CPU2 interrupt wakeup enable. 1'b0: Disable 1'b1: Enable
8	RW	0x0	cpu2_auto_pwrdn_ena CPU2 auto power down enable. 1'b0: Disable 1'b1: Enable
7	RW	0x0	cpu1_sft_wakeup_cluster_ena CPU1 software wakeup enable. 1'b0: Disable 1'b1: Enable
6	RW	0x0	cpu1_int_mask_ena CPU1 interrupt mask enable. 1'b0: Disable 1'b1: Enable
5	RW	0x0	cpu1_int_wakeup_ena CPU1 interrupt wakeup enable. 1'b0: Disable 1'b1: Enable
4	RW	0x0	cpu1_auto_pwrdn_ena CPU1 auto power down enable. 1'b0: Disable 1'b1: Enable
3	RW	0x0	cpu0_sft_wakeup_cluster_ena CPU0 software wakeup enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	cpu0_int_mask_ena CPU0 interrupt mask enable. 1'b0: Disable 1'b1: Enable
1	RW	0x0	cpu0_int_wakeup_ena CPU0 interrupt wakeup enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	cpu0_auto_pwrdn_ena CPU0 auto power down enable. 1'b0: Disable 1'b1: Enable

PMU2_CPU_PWR_SFTCON

Address: Operational Base(0xFF258000) + offset (0x0014)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	cpu3_sft_pwrdn_ena CPU3 software power down enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	cpu2_sft_pwrdn_ena CPU2 software power down enable. 1'b0: Disable 1'b1: Enable
1	RW	0x0	cpu1_sft_pwrdn_ena CPU1 software power down enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	cpu0_sft_pwrdn_ena CPU0 software power down enable. 1'b0: Disable 1'b1: Enable

PMU2_DBG_PWR_CON

Address: Operational Base(0xFF258000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	cpu3_dbgnopwrdwn_ena CPU3 dbgnopwrdwn check enable. 1'b0: Disable 1'b1: Enable
6	RW	0x0	cpu2_dbgnopwrdwn_ena CPU2 dbgnopwrdwn check enable. 1'b0: Disable 1'b1: Enable
5	RW	0x0	cpu1_dbgnopwrdwn_ena CPU1 dbgnopwrdwn check enable. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
4	RW	0x0	cpu0_dbgnopwrdwn_ena CPU0 dbgnopwrdwn check enable. 1'b0: Disable 1'b1: Enable
3	RW	0x0	cpu3_dbgpwrupreq_ena CPU3 dbgpwrupreq check enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	cpu2_dbgpwrupreq_ena CPU2 dbgpwrupreq check enable. 1'b0: Disable 1'b1: Enable
1	RW	0x0	cpu1_dbgpwrupreq_ena CPU1 dbgpwrupreq check enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	cpu0_dbgpwrupreq_ena CPU0 dbgpwrupreq check enable. 1'b0: Disable 1'b1: Enable

PMU2_CLUSTER_PWR_ST

Address: Operational Base(0xFF258000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RO	0x0	cpu3_standbywfi CPU3 STANDBYWFI state. 1'b0: Inactive 1'b1: Active
10	RO	0x0	cpu2_standbywfi CPU2 STANDBYWFI state. 1'b0: Inactive 1'b1: Active
9	RO	0x0	cpu1_standbywfi CPU1 STANDBYWFI state. 1'b0: Inactive 1'b1: Active
8	RO	0x0	cpu0_standbywfi CPU0 STANDBYWFI state. 1'b0: Inactive 1'b1: Active
7	RO	0x0	cpu3_dwn_state CPU3 power down state. 1'b0: Inactive 1'b1: Active

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Bit	Attr	Reset Value	Description
6	RO	0x0	cpu2_dwn_state CPU2 power down state. 1'b0: Inactive 1'b1: Active
5	RO	0x0	cpu1_dwn_state CPU1 power down state. 1'b0: Inactive 1'b1: Active
4	RO	0x0	cpu0_dwn_state CPU0 power down state. 1'b0: Inactive 1'b1: Active
3	RO	0x0	reserved
2	RO	0x0	scu_dwn_state SCU power down state. 1'b0: Inactive 1'b1: Active
1	RO	0x0	standbywfil2 L2 STANDBYWFI state. 1'b0: Inactive 1'b1: Active
0	RO	0x0	l2flushdone L2 flushdone state. 1'b0: Inactive 1'b1: Active

PMU2_CLUSTER_IDLE_CON

Address: Operational Base(0xFF258000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2	RW	0x0	gic2core_pwrq_req Enable sending gic2core power q-channel request by PMU. 1'b0: Disable 1'b1: Enable
1	RW	0x0	core2gic_pwrq_req Enable sending core2gic power q-channel request by PMU. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
0	RW	0x0	idle_req_cpu Enable sending bus idle request to BIU_CPU by PMU. 1'b0: Disable 1'b1: Enable

PMU2_CLUSTER_IDLE_SFTCON

Address: Operational Base(0xFF258000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2	RW	0x0	gic2core_pwrq_req Enable sending gic2core power q-channel request by software. 1'b0: Disable 1'b1: Enable
1	RW	0x0	core2gic_pwrq_req Enable sending core2gic power q-channel request by software. 1'b0: Disable 1'b1: Enable
0	RW	0x0	idle_req_cpu Enable sending bus idle request to BIU_CPU by software. 1'b0: Disable 1'b1: Enable

PMU2_SCU_STABLE_CNT

Address: Operational Base(0xFF258000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	stable_cnt SCU power stable counter for SCU from power off to wakeup.

PMU2_SCU_PWRUP_CNT

Address: Operational Base(0xFF258000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x05dc0	stable_cnt SCU power up stable counter, reflect on the falling time of pd_scu_dwn_ack.

PMU2_SCU_PWRDN_CNT

Address: Operational Base(0xFF258000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
19:0	RW	0x05dc0	stable_cnt SCU power down stable counter, reflect on the rising time of pd_scu_dwn_ack.

PMU2_SCU_VOLUP_CNT

Address: Operational Base(0xFF258000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x05dc0	stable_cnt SCU voltage up stable counter, reflect on the falling time of pd_scu_dwn_en.

PMU2_SCU_VOLDN_CNT

Address: Operational Base(0xFF258000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x05dc0	stable_cnt SCU voltage up stable counter, reflect on the rising time of pd_scu_dwn_en.

PMU2_BIU_IDLE_CON0

Address: Operational Base(0xFF258000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	idle_req_ddrc_ena Enable sending idle request to BIU_DDRC by hardware. 1'b0: Disable 1'b1: Enable
11	RW	0x0	idle_req_top_ena Enable sending idle request to BIU_TOP by hardware. 1'b0: Disable 1'b1: Enable
10	RW	0x0	idle_req_bus_ena Enable sending idle request to BIU_BUS by hardware. 1'b0: Disable 1'b1: Enable
9	RW	0x0	idle_req_peri_ena Enable sending idle request to BIU_PERI by hardware. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
8	RW	0x0	idle_req_php_ena Enable sending idle request to BIU_PHP by hardware. 1'b0: Disable 1'b1: Enable
7	RW	0x0	idle_req_vepu_ena Enable sending idle request to BIU_VEPU by hardware. 1'b0: Disable 1'b1: Enable
6	RW	0x0	idle_req_vdpu_ena Enable sending idle request to BIU_VDPU by hardware. 1'b0: Disable 1'b1: Enable
5	RW	0x0	idle_req_rga_ena Enable sending idle request to BIU_RGA by hardware. 1'b0: Disable 1'b1: Enable
4	RW	0x0	idle_req_vo_ena Enable sending idle request to BIU_VO by hardware. 1'b0: Disable 1'b1: Enable
3	RW	0x0	idle_req_vi_ena Enable sending idle request to BIU_VI by hardware. 1'b0: Disable 1'b1: Enable
2	RW	0x0	idle_req_npu_ena Enable sending idle request to BIU_NPU by hardware. 1'b0: Disable 1'b1: Enable
1	RW	0x0	idle_req_gpu_ena Enable sending idle request to BIU_GPU by hardware. 1'b0: Disable 1'b1: Enable
0	RW	0x0	idle_req_msch_ena Enable sending idle request to BIU_MSCH by hardware. 1'b0: Disable 1'b1: Enable

PMU2_BIU_IDLE_SFTCON0

Address: Operational Base(0xFF258000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12	RW	0x0	idle_req_ddrc_sftena Enable sending idle request to BIU_DDRC by software. 1'b0: Disable 1'b1: Enable
11	RW	0x0	idle_req_top_sftena Enable sending idle request to BIU_TOP by software. 1'b0: Disable 1'b1: Enable
10	RW	0x0	idle_req_bus_sftena Enable sending idle request to BIU_BUS by software. 1'b0: Disable 1'b1: Enable
9	RW	0x0	idle_req_peri_sftena Enable sending idle request to BIU_PERI by software. 1'b0: Disable 1'b1: Enable
8	RW	0x0	idle_req_php_sftena Enable sending idle request to BIU_PHP by software. 1'b0: Disable 1'b1: Enable
7	RW	0x0	idle_req_vepu_sftena Enable sending idle request to BIU_VEPU by software. 1'b0: Disable 1'b1: Enable
6	RW	0x0	idle_req_vdpu_sftena Enable sending idle request to BIU_VDPU by software. 1'b0: Disable 1'b1: Enable
5	RW	0x0	idle_req_rga_sftena Enable sending idle request to BIU_RGA by software. 1'b0: Disable 1'b1: Enable
4	RW	0x0	idle_req_vo_sftena Enable sending idle request to BIU_VO by software. 1'b0: Disable 1'b1: Enable
3	RW	0x0	idle_req_vi_sftena Enable sending idle request to BIU_VI by software. 1'b0: Disable 1'b1: Enable
2	RW	0x0	idle_req_npu_sftena Enable sending idle request to BIU_NPU by software. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
1	RW	0x0	idle_req_gpu_sftena Enable sending idle request to BIU_GPU by software. 1'b0: Disable 1'b1: Enable
0	RW	0x0	idle_req_msch_sftena Enable sending idle request to BIU_MSCH by software. 1'b0: Disable 1'b1: Enable

PMU2_BIU_IDLE_ACK_STS0

Address: Operational Base(0xFF258000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RO	0x0	idle_ack_ddrc BIU_DDRC idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
11	RO	0x0	idle_ack_top BIU_TOP idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
10	RO	0x0	idle_ack_bus BIU_BUS idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
9	RO	0x0	idle_ack_peri BIU_PERI idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
8	RO	0x0	idle_ack_php BIU_PHP idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
7	RO	0x0	idle_ack_vepu BIU_VEPU idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
6	RO	0x0	idle_ack_vdpu BIU_VDPU idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
5	RO	0x0	idle_ack_rga BIU_RGA idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge

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Bit	Attr	Reset Value	Description
4	RO	0x0	idle_ack_vo BIU_VO idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
3	RO	0x0	idle_ack_vi BIU_VI idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
2	RO	0x0	idle_ack_npu BIU_NPU idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
1	RO	0x0	idle_ack_gpu BIU_GPU idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
0	RO	0x0	idle_ack_msch BIU_MSCH idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge

PMU2_BIU_IDLE_STS0

Address: Operational Base(0xFF258000) + offset (0x0128)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RO	0x0	idle_ddrc BIU_DDRC idle state. 1'b0: Not idle 1'b1: Idle
11	RO	0x0	idle_top BIU_TOP idle state. 1'b0: Not idle 1'b1: Idle
10	RO	0x0	idle_bus BIU_BUS idle state. 1'b0: Not idle 1'b1: Idle
9	RO	0x0	idle_peri BIU_PERI idle state. 1'b0: Not idle 1'b1: Idle
8	RO	0x0	idle_php BIU_PHP idle state. 1'b0: Not idle 1'b1: Idle

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Bit	Attr	Reset Value	Description
7	RO	0x0	idle_vepu BIU_VEPU idle state. 1'b0: Not idle 1'b1: Idle
6	RO	0x0	idle_vdpu BIU_VDPU idle state. 1'b0: Not idle 1'b1: Idle
5	RO	0x0	idle_rga BIU_RGA idle state. 1'b0: Not idle 1'b1: Idle
4	RO	0x0	idle_vo BIU_VO idle state. 1'b0: Not idle 1'b1: Idle
3	RO	0x0	idle_vi BIU_VI idle state. 1'b0: Not idle 1'b1: Idle
2	RO	0x0	idle_npu BIU_NPU idle state. 1'b0: Not idle 1'b1: Idle
1	RO	0x0	idle_gpu BIU_GPU idle state. 1'b0: Not idle 1'b1: Idle
0	RO	0x0	idle_msch BIU_MSCH idle state. 1'b0: Not idle 1'b1: Idle

PMU2_BIU_AUTO_CON0

Address: Operational Base(0xFF258000) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14	RW	0x0	biu_auto_scu_ena If enable, BIU_SCU corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
13	RO	0x0	reserved
12	RW	0x0	biu_auto_ddrc_ena If enable, BIU_DDRC corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
11	RW	0x0	biu_auto_top_ena If enable, BIU_TOP corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
10	RW	0x0	biu_auto_bus_ena If enable, BIU_BUS corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
9	RW	0x0	biu_auto_peri_ena If enable, BIU_PERI corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
8	RW	0x0	biu_auto_php_ena If enable, BIU_PHP corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
7	RW	0x0	biu_auto_vepu_ena If enable, BIU_VEPU corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
6	RW	0x0	biu_auto_vdpu_ena If enable, BIU_VDPU corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
5	RW	0x0	biu_auto_rga_ena If enable, BIU_RGA corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
4	RW	0x0	biu_auto_vo_ena If enable, BIU_VO corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
3	RW	0x0	biu_auto_vi_ena If enable, BIU_VI corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
2	RW	0x0	biu_auto_npu_ena If enable, BIU_NPU corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
1	RW	0x0	biu_auto_gpu_ena If enable, BIU_GPU corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
0	RW	0x0	biu_auto_msch_ena If enable, BIU_MSCH corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable

PMU2_BIU_AUTO_SFTCON0

Address: Operational Base(0xFF258000) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	biu_ddrc_sftena If enable, BIU_DDRC corresponding clock can not be gated. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
11	RW	0x0	biu_top_sftena If enable, BIU_TOP corresponding clock can not be gated. 1'b0: Disable 1'b1: Enable
10	RW	0x0	biu_bus_sftena If enable, BIU_BUS corresponding clock can not be gated. 1'b0: Disable 1'b1: Enable
9	RW	0x0	biu_peri_sftena If enable, BIU_PERI corresponding clock can not be gated. 1'b0: Disable 1'b1: Enable
8	RW	0x0	biu_php_sftena If enable, BIU_PHP corresponding clock can not be gated. 1'b0: Disable 1'b1: Enable
7	RW	0x0	biu_vepu_sftena If enable, BIU_VEPU corresponding clock can not be gated. 1'b0: Disable 1'b1: Enable
6	RW	0x0	biu_vdpu_sftena If enable, BIU_VDPU corresponding clock can not be gated. 1'b0: Disable 1'b1: Enable
5	RW	0x0	biu_rga_sftena If enable, BIU_RGA corresponding clock can not be gated. 1'b0: Disable 1'b1: Enable
4	RW	0x0	biu_vo_sftena If enable, BIU_VO corresponding clock can not be gated. 1'b0: Disable 1'b1: Enable
3	RW	0x0	biu_vi_sftena If enable, BIU_VI corresponding clock can not be gated. 1'b0: Disable 1'b1: Enable
2	RW	0x0	biu_npu_sftena If enable, BIU_NPU corresponding clock can not be gated. 1'b0: Disable 1'b1: Enable
1	RW	0x0	biu_gpu_sftena If enable, BIU_GPU corresponding clock can not be gated. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
0	RW	0x0	biu_msch_sftena If enable, BIU_MSCH corresponding clock can not be gated. 1'b0: Disable 1'b1: Enable

PMU2_PWR_GATE_CON0

Address: Operational Base(0xFF258000) + offset (0x0200)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	pd_php_dwn_ena Enable power down PD_PHP by hardware. 1'b0: Disable 1'b1: Enable
6	RW	0x0	pd_vo_dwn_ena Enable power down PD_VO by hardware. 1'b0: Disable 1'b1: Enable
5	RW	0x0	pd_vi_dwn_ena Enable power down PD_VI by hardware. 1'b0: Disable 1'b1: Enable
4	RW	0x0	pd_rga_dwn_ena Enable power down PD_RGA by hardware. 1'b0: Disable 1'b1: Enable
3	RW	0x0	pd_vepu_dwn_ena Enable power down PD_VEPU by hardware. 1'b0: Disable 1'b1: Enable
2	RW	0x0	pd_vdpu_dwn_ena Enable power down PD_VDPU by hardware. 1'b0: Disable 1'b1: Enable
1	RW	0x0	pd_npu_dwn_ena Enable power down VD_NPU by hardware. 1'b0: Disable 1'b1: Enable
0	RW	0x0	pd_gpu_dwn_ena Enable power down VD_GPU by hardware. 1'b0: Disable 1'b1: Enable

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PMU2_PWR_GATE_SFTCON0

Address: Operational Base(0xFF258000) + offset (0x0210)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	pd_php_dwn_sftena Enable power down PD_PHP by software. 1'b0: Disable 1'b1: Enable
6	RW	0x1	pd_vo_dwn_sftena Enable power down PD_VO by software. 1'b0: Disable 1'b1: Enable
5	RW	0x1	pd_vi_dwn_sftena Enable power down PD_VI by software. 1'b0: Disable 1'b1: Enable
4	RW	0x1	pd_rga_dwn_sftena Enable power down PD_RGA by software. 1'b0: Disable 1'b1: Enable
3	RW	0x1	pd_vepu_dwn_sftena Enable power down PD_VEPU by software. 1'b0: Disable 1'b1: Enable
2	RW	0x1	pd_vdpu_dwn_sftena Enable power down PD_VDPU by software. 1'b0: Disable 1'b1: Enable
1	RW	0x1	pd_npu_dwn_sftena Enable power down VD_NPU by software. 1'b0: Disable 1'b1: Enable
0	RW	0x1	pd_gpu_dwn_sftena Enable power down VD_GPU by software. 1'b0: Disable 1'b1: Enable

PMU2_VOL_GATE_CON0

Address: Operational Base(0xFF258000) + offset (0x0220)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x1	vd_npu_off_ena Enable power off VD_NPU. 1'b0: Disable 1'b1: Enable
0	RW	0x1	vd_gpu_off_ena Enable power off VD_GPU. 1'b0: Disable 1'b1: Enable

PMU2_PWR_GATE_STS0

Address: Operational Base(0xFF258000) + offset (0x0230)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x1	pd_php_dwn_stat The power state of PD_PHP. 1'b0: Power up 1'b1: Power down
6	RO	0x1	pd_vo_dwn_stat The power state of PD_VO. 1'b0: Power up 1'b1: Power down
5	RO	0x1	pd_vi_dwn_stat The power state of PD_VI. 1'b0: Power up 1'b1: Power down
4	RO	0x1	pd_rga_dwn_stat The power state of PD_RGA. 1'b0: Power up 1'b1: Power down
3	RO	0x1	pd_vepu_dwn_stat The power state of PD_VEPU. 1'b0: Power up 1'b1: Power down
2	RO	0x1	pd_vdpu_dwn_stat The power state of VD_VDPU. 1'b0: Power up 1'b1: Power down

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Bit	Attr	Reset Value	Description
1	RO	0x1	pd_npu_dwn_stat The power state of VD_NPU. 1'b0: Power up 1'b1: Power down
0	RO	0x1	pd_gpu_dwn_stat The power state of VD_GPU. 1'b0: Power up 1'b1: Power down

PMU2_PWR_GATE_POWER_STS

Address: Operational Base(0xFF258000) + offset (0x0238)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RO	0x0	power_gate_state Power gating state. 3'h0: Normal state 3'h1: Power down start state 3'h2: Power down running state 3'h3: Wait for power up state 3'h4: Power up start state 3'h5: Power up running state Others: Reserved

PMU2_MEM_SD_SFTCON0

Address: Operational Base(0xFF258000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0xffff	vop_mem_sd_con Enable shut down VOP memory. 1'b0: Disable 1'b1: Enable

PMU2_MEM_SD_SFTCON1

Address: Operational Base(0xFF258000) + offset (0x0304)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0xff	ddr_mem_sd_con Enable shut down DDR memory. 1'b0: Disable 1'b1: Enable

3.5 Timing Diagram

3.5.1 Each Domain Power Switch Timing

The following figure shows the timing for each domain power down and power up.

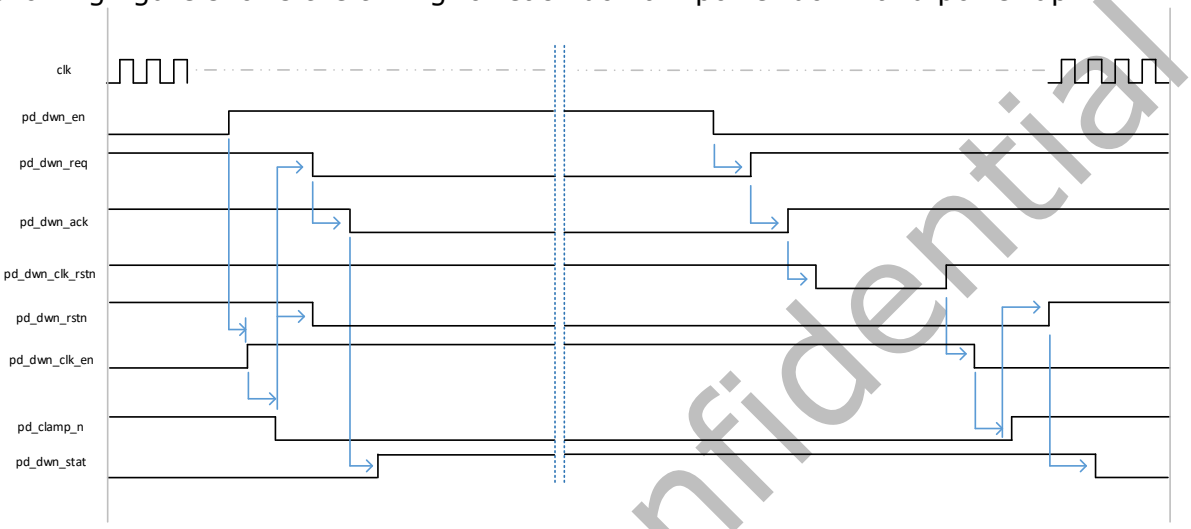


Fig.3-3 Each Domain Power Switch Timing

3.5.2 External Wakeup PAD Timing

The PMU supports a lot of external wakeup sources, such as SDMMC, USBDEV, SDIO, GPIO0 wakeup source and so on. All these external wakeup sources must meet the timing requirement (at least 200us) when the wakeup event is asserted. The following figure gives the timing information.

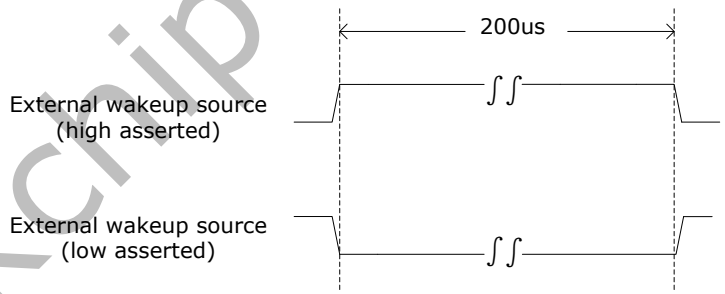


Fig.3-4 External Wakeup Source PAD Timing

3.6 Application Notes

3.6.1 Low Power Mode

PMU can work in the power mode 1 by setting bit[0] of PMU1_PWR_CON1 register. After setting this bit and all CPUs enter standby states, PMU low power FSM will start to run. In this low power mode, PMU will manage power resources by hardware or software, such as send idle request or resume transfer to specified BIU interface, power down or power up the specified power domain, DDR enters or exits retention mode, shut down or power up PLL, disable or enable oscillator, and so on. All of above are configurable by setting corresponding registers.

PMU can work in power mode 0 by setting bit[0] in PMU0_PWR_CON0 register. After setting this bit and PMU enters power mode 1, PMU power mode 0 FSM will start to run. In this low power mode, PMU will manage PD_PMU1 power resource. All of above are configurable by setting corresponding registers.

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3.6.2 Nested Power Domain

There are some particular orders of power on and off in RK3562. PD_RGA should be powered off before PD_VO and PD_VEPU should be powered off before PD_VI. PD_RGA should be powered on after PD_VO and PD_VEPU should be powered on after PD_VI.

3.6.3 Power Management IO Usage

There are independent power supplies for different voltage domain. You can communicate with external PMIC (Power Management Integrated Circuits) through I2C interface, or through IO interface.

There are 4 IOs designed for purpose, corresponding Module Pin names are pwr_sleep_0~ pwr_sleep_3. The IO interface configuration is as below.

Table 3-2 Power Management IO Interface

Module Pin	Direction	Pin Name	IOMUX Setting
pwr_sleep_0	O	PWR_CTRL0/TSADC_SHUT_M1/ GPIO0_A2_d	PMU_IOC_GPIO0A_IOMUX_SEL_L[11:8]=1
pwr_sleep_1	O	PWR_CTRL1/GPIO0_A3_u	PMU_IOC_GPIO0A_IOMUX_SEL_L[15:12]=1
pwr_sleep_2	O	PCIE20_CLKREQN_M0/GPIO0_A6_d	PMU_IOC_GPIO0A_IOMUX_SEL_H[11:8]=0 & PMUGRF_SOC_CON13[0]=1
pwr_sleep_3	O	PWM3_M0/GPIO0_A7_d	PMU_IOC_GPIO0A_IOMUX_SEL_H[15:12]=0 & PMUGRF_SOC_CON13[1]=1

Each pwr_sleep_i (i=0~3) has multi power off requests and you can only choose one at a time. Detail refers to PMUGRF_SOC_CON0.

3.6.4 Debug IO

ALL FSM power states could be monitored through IO. RK3562 also provide PMU Debug IO for FSM observation in UART signal mode.

Table 3-3 Debug IO for PMU FSM state

Module Pin	Direction	Pin Name	IOMUX Setting
pmu_state[0]	O	SDMMC0_DETN/I2C4_SDA_M1/ GPIO0_A4_u	PMU_IOC_GPIO0A_IOMUX_SEL_H[3:0]=5
pmu_state[1]	O	SDMMC0_PWREN/I2C4_SCL_M1 /PMU_DEBUG/GPIO0_A5_d	PMU_IOC_GPIO0A_IOMUX_SEL_H[7:4]=5
pmu_state[2]	O	PCIE20_CLKREQN_M0/GPIO0_A6_d	PMU_IOC_GPIO0A_IOMUX_SEL_H[11:8]=5
pmu_state[3]	O	PWM3_M0/GPIO0_A7_d	PMU_IOC_GPIO0A_IOMUX_SEL_H[15:12]=5
pmu_debug_tx	O	SDMMC0_PWREN/I2C4_SCL_M1 /PMU_DEBUG/GPIO0_A5_d	PMU_IOC_GPIO0A_IOMUX_SEL_H[7:4]=3

3.6.5 Configuration Constraint

In order to shut down the power domains which are managed by software correctly, the software must obey the rules bellow:

- Send BIU request to the BIU in power domain that you want to shut down by configure PMU2_BIU_IDLE_SFTCON0 register.
- Querying PMU2_BIU_IDLE_STS0 register to get the information until the pacific BIU is in idle state.
- Send power request to the power domain through PMU2_PWR_GATE_SFTCON0 register.
- Querying PMU2_PWR_GATE_STS0 register to make sure the pacific power domain is power down.

3.6.6 Configuration of memory shut down

The memory in DDR and VOP should be shut down before the corresponding power domain power off. Each bit in register PMU2_MEM_SD_SFTCON0/1 should be configured in sequence. By the way, both ascending and descending order should be fine.

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Chapter 4 System Debug

4.1 Overview

The chip uses the DAPLITE Technology to support real-time debug.

4.1.1 Features

- Invasive debug with core halted
- SW-DP

4.1.2 Debug Components Address Map

The following table shows the debug components address in memory map:

Module	Base Address
DAP_ROM	0xFED80000

4.2 Block Diagram

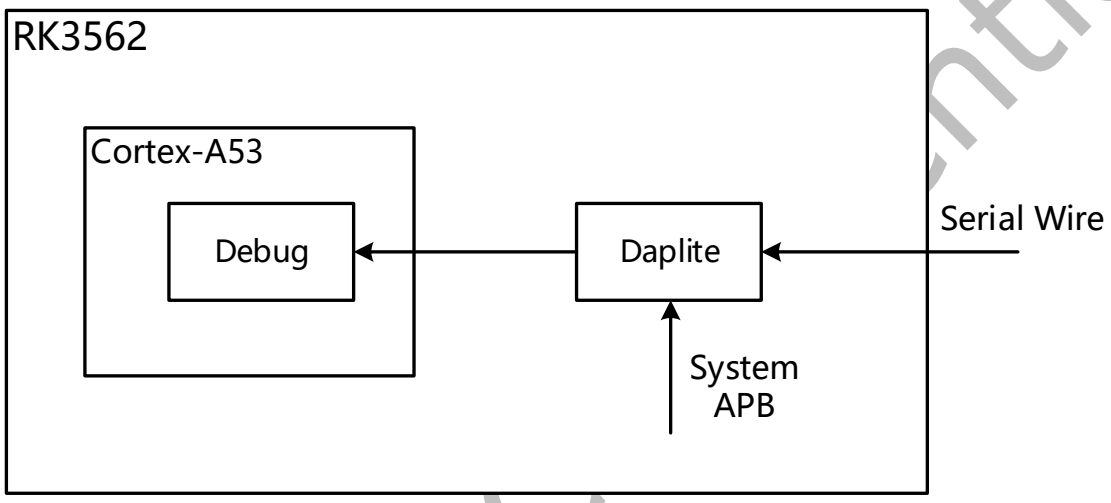


Fig.4-1 Debug System Structure

4.3 Function Description

4.3.1 DAP

The DAP has following components:

- Serial Wire JTAG Debug Port(SWJ-DP)
- APB Access Port(APB-AP)
- ROM table

The debug port is the host tools interface to access the DAP-Lite. This interface controls any access ports provided within the DAP-Lite. The DAP-Lite supports a combined debug port which includes both JTAG and Serial Wire Debug(SWD), with a mechanism that supports switching between them.

The APB-AP acts as a bridge between SWJ-DP and APB bus which translate the Debug request to APB bus.

The DAP provides an internal ROM table connected to the master Debug APB port of the APB-Mux. The Debug ROM table is loaded at address 0x00000000 and 0x80000000 of this bus and is accessible from both APB-AP and the system APB input. Bit[31] of the address bus is not connected to the ROM Table, ensuring that both views read the same value. The ROM table stores the locations of the components on the Debug APB.

More information please refer to the document CoreSight_DAPLite_TRM.pdf for the debug detail description.

4.4 Register Description

Please refer to the document CoreSight_DAPLite_TRM.pdf for the debug detail description.

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4.5 Interface Description

4.5.1 DAP SWJ-DP Interface

The following figure is the DAP SWJ-DP interface, the SWJ-DP is a combined JTAG-DP and SW-DP that enable you connect either a Serial Wire Debug(SWJ) to JTAG probe to a target.

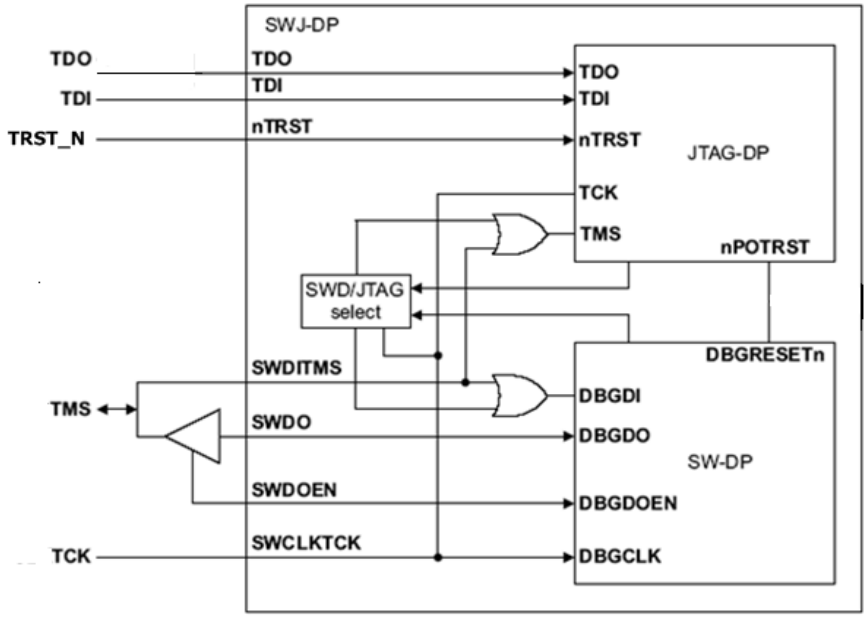


Fig.4-2 DAP SWJ Interface

4.5.2 DAP SW-DP Interface

This implementation is taken from ADIv5.1 and operates with a synchronous serial interface. This uses a single bidirectional data signal, and a clock signal.

The figure below describes the interaction between the timing of transactions on the serial wire interface, and the DAP internal bus transfers. It shows when the target responds with a WAIT acknowledgement.

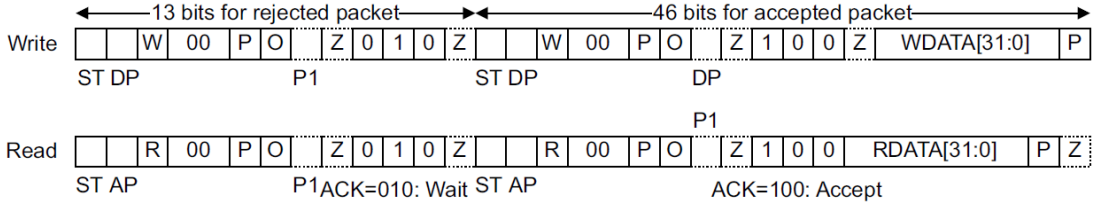


Fig.4-3 SW-DP Acknowledgement Timing

Table 4-1 DAP-Lite Interface Description

Module pin	Dir	Pad name	IOMUX
jtag_tckm0	I	UART0_TX_M0/JTAG_CPU_MCU_TCK_M0/GPIO0_D1_u	PMU_IOC_GPIO0D_IOMUX_SEL_L[7:4]=2
jtag_tmsm0	I/O	UART0_RX_M0/JTAG_CPU_MCU_TMS_M0/GPIO0_D0_u	PMU_IOC_GPIO0D_IOMUX_SEL_L[3:0]=2
jtag_tckm1	I	SDMMC0_D2/JTAG_CPU_MCU_TCK_M1/UART5_CTSN_M0/SPI1_CSN1_M1/PWM10_M0/DSM_AUD_RP/GPIO1_B5_u	GPIO1_IOC_GPIO1B_IOMUX_SEL_H[7:4]=2
jtag_tmsm1	I/O	SDMMC0_D3/JTAG_CPU_MCU_TMS_M1/UART5_RTSN_M0/SPI1_CSN0_M1/PWM11_M0/DSM_AUD_RN/GPIO1_B6_u	GPIO1_IOC_GPIO1B_IOMUX_SEL_H[11:8]=2

In addition, the SGRF_SOC_CON1[4] should be set for enable DEVICEEN. By default, jtag_tckm1 and jtag_tmsm1 are forced to connect to corresponding io pad, we don't need to set IOMUX again.

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Chapter 5 General Register Files (GRF)

5.1 Overview

The general register file will be used to do static setting by software, which is composed of many registers for system control. The GRF is located at several addresses.

5.2 Function Description

The function of general register file is：

- GPIO IOMUX control
- GPIO PAD pull down and pull up control
- Common system control
- Record the system state

Table 5-1 GRF Adress Mapping Table

Name	Address Base
PMU_GRF	0XFF010000
SYS_GRF	0XFF030000
PERI_GRF	0XFF040000
DDR_GRF	0XFF050000
GPIO1_IOC	0XFF060000
GPIO2_IOC	0XFF060000
GPIO3_IOC	0XFF070000
GPIO4_IOC	0XFF070000
GPIO0_IOC	0XFF080000
USBPHY_GRF	0XFF090000
PIPEPHY_GRF	0XFF098000

5.3 PMU_GRF Register Description

5.3.1 Registers Summary

Name	Offset	Size	Reset Value	Description
GRF_PMU_SOC_CON0	0x0100	W	0x00000080	System control register 0
GRF_PMU_SOC_CON1	0x0104	W	0x0000241C	System control register 1
GRF_PMU_SOC_CON2	0x0108	W	0x00000000	System control register 2
GRF_PMU_SOC_CON3	0x010C	W	0x00000000	System control register 3
GRF_PMU_SOC_CON4	0x0110	W	0x00000000	System control register 4
GRF_PMU_SOC_CON5	0x0114	W	0x0000081B	System control register 5
GRF_PMU_SOC_CON6	0x0118	W	0x00000000	System control register 6
GRF_PMU_SOC_CON7	0x011C	W	0x00000000	System control register 7
GRF_PMU_SOC_CON8	0x0120	W	0x00000000	System control register 8
GRF_PMU_SOC_CON9	0x0124	W	0x00000000	System control register 9
GRF_PMU_SOC_CON10	0x0128	W	0x00000000	System control register 10
GRF_PMU_SOC_CON11	0x012C	W	0x00000000	System control register 11
GRF_PMU_SOC_CON12	0x0130	W	0x00000000	System control register 12
GRF_PMU_SOC_CON13	0x0134	W	0x00000000	System control register 13
GRF_PMU_SOC_STATUS0	0x0138	W	0x00000000	System status register 0
GRF_PMU_PVTM_CON0	0x0180	W	0x00000003	PVTM control register 0
GRF_PMU_OS_REG0	0x0200	W	0x00000000	PMU GRF OS register0
GRF_PMU_OS_REG1	0x0204	W	0x00000000	PMU GRF OS register1
GRF_PMU_OS_REG2	0x0208	W	0x00000000	PMU GRF OS register2
GRF_PMU_OS_REG3	0x020C	W	0x00000000	PMU GRF OS register3
GRF_PMU_OS_REG4	0x0210	W	0x00000000	PMU GRF OS register4
GRF_PMU_OS_REG5	0x0214	W	0x00000000	PMU GRF OS register5
GRF_PMU_OS_REG6	0x0218	W	0x00000000	PMU GRF OS register6
GRF_PMU_OS_REG7	0x021C	W	0x00000000	PMU GRF OS register7

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Name	Offset	Size	Reset Value	Description
GRF_PMU_OS_REG8	0x0220	W	0x00000000	PMU GRF OS register8
GRF_PMU_OS_REG9	0x0224	W	0x00000000	PMU GRF OS register9
GRF_PMU_OS_REG10	0x0228	W	0x00000000	PMU GRF OS register10
GRF_PMU_OS_REG11	0x022C	W	0x00000000	PMU GRF OS register11
GRF_PMU_RESET_FUNCTION_STATUS	0x0230	W	0x00000000	system reset status register
GRF_PMU_RESET_FUNCTION_CLR	0x0234	W	0x00000000	system reset status clear register
GRF_PMU_SIG_DETECT_CON	0x0380	W	0x00000000	sdmmc detect control reg
GRF_PMU_SIG_DETECT_STATUS	0x0390	W	0x00000000	sdmmc detect status reg
GRF_PMU_SIG_DETECT_STATUS_CLEAR	0x03A0	W	0x00000000	sdmmc irq clear reg
GRF_PMU_SDMMC_DET_COUNTER	0x03B0	W	0x000003E8	sdmmc detect counter reg

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.3.2 Detail Registers Description

GRF_PMU_SOC_CON0

Address: Operational Base(0xFF010000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	grf_con_pwr3_sleep_pol Polarity selection of pwr3 sleep. 1'b0: Low active 1'b1: High active
14:12	RW	0x0	grf_con_pwr3_sleep_src_sel IO_PWRctrl3(GPIO0a7) function selection 3'b000: From pmu block, indicate the VDD_LOGIC power off state 3'b001: From reset pulse generator, can reset external PMIC 3'b010: From pmu block, indicate the VDD_CORE power off state 3'b011: From pmu block, indicate the VDD_GPU power off state 3'b100: From pmu block, indicate the VDD_NPU power off state 3'b101: From pmu block, indicate the VDD_PD_PMU1 power off state 3'b110: From pmu block, indicate the CPLL power off state
11	RW	0x0	grf_con_pwr2_sleep_pol Polarity selection of pwr2 sleep. 1'b0: Low active 1'b1: High active
10:8	RW	0x0	grf_con_pwr2_sleep_src_sel IO_PWRctrl2(GPIO0a6) function selection 3'b000: From pmu block, indicate the VDD_LOGIC power off state 3'b001: From reset pulse generator, can reset external PMIC 3'b010: From pmu block, indicate the VDD_CORE power off state 3'b011: From pmu block, indicate the VDD_GPU power off state 3'b100: From pmu block, indicate the VDD_NPU power off state 3'b101: From pmu block, indicate the VDD_PD_PMU1 power off state 3'b110: From pmu block, indicate the CPLL power off state

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Bit	Attr	Reset Value	Description
7	RW	0x1	grf_con_pwr1_sleep_pol Polarity selection of pwr1 sleep. 1'b0: Low active 1'b1: High active
6:4	RW	0x0	grf_con_pwr1_sleep_src_sel IO_PWRctrl1 function selection 3'b000: From pmu block, indicate the VDD_LOGIC power off state 3'b001: From reset pulse generator, can reset external PMIC 3'b010: From pmu block, indicate the VDD_CORE power off state 3'b011: From pmu block, indicate the VDD_GPU power off state 3'b100: From pmu block, indicate the VDD_NPU power off state 3'b101: From pmu block, indicate the VDD_PD_PMU1 power off state 3'b110: From pmu block, indicate the CPLL power off state
3	RW	0x0	grf_con_pwr0_sleep_pol Polarity selection of pwr0 sleep. 1'b0: Low active 1'b1: High active
2:0	RW	0x0	grf_con_pwr0_sleep_src_sel IO_PWRctrl0 function selection 3'b000: From pmu block, indicate the VDD_LOGIC power off state 3'b001: From reset pulse generator, can reset external PMIC 3'b010: From pmu block, indicate the VDD_CORE power off state 3'b011: From pmu block, indicate the VDD_GPU power off state 3'b100: From pmu block, indicate the VDD_NPU power off state 3'b101: From pmu block, indicate the VDD_PD_PMU1 power off state 3'b110: From pmu block, indicate the CPLL power off state

GRF_PMU_SOC_CON1

Address: Operational Base(0xFF010000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	grf_con_wdt_ns_pmu_pause_en Enable pause of WDT_PMU. 1'b0: Disable 1'b1: Enable
13	RW	0x1	grf_con_dma_rx_single_bypass Enable dma rx single bypass of UART0. 1'b0: Disable 1'b1: Enable
12	RW	0x0	grf_con_ddrphy_hwlp_en 1'b0: Enable hwlp_ddrphy_io_ret 1'b1: Disable hwlp_ddrphy_io_ret
11	RW	0x0	grf_con_ddrphy_bufferen_core 1'b0: Enable ddrphy io retention 1'b1: Disable ddrphy io retention
10	RW	0x1	grf_con_ddrphy_bufferen_sel 1'b0: Ddrphy_bufferen from pmu and ddr_fail_safe 1'b1: Ddrphy_bufferen from grf_con_ddrphy_bufferen_core. Default value is 1'b1, so ddr_io_ret is enable.

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Bit	Attr	Reset Value	Description
9	RW	0x0	hold_the_ddrfailsafe hold ddrfailsafe reset
8	RW	0x0	upctl_c_sysreq_cfg 1'b0: After ddr failsafe module enters self-refresh status, then request DDR controller to enter low power state 1'b1: Always enable requesting DDR controller to enter low power state, when ddr failsafe module is working
7	RW	0x0	ddr_io_ret_oen_cfg ddr_io_ret_oen_cfg bit control 1'b0: Ddr_io_ret output enable 1'b1: Ddr_io_ret_output disable
6	RW	0x0	ddr_io_ret_cfg 1'b0: Ddr io retention managed by hardware automatically 1'b1: Enable ddr io retention manually
5	RW	0x0	ddr_io_ret_de_req Request to enter retention, during system failure 1'b0: Disable 1'b1: Enable
4	RW	0x1	ddrc_gating_en 1'b0: Disable ddr clock gating during system failure 1'b1: Enable ddr clock gating during system failure
3	RW	0x1	sref_enter_en 1'b0: Disable ddr self-refresh enter when system is failed 1'b1: Enable ddr self-refresh enter when system is failed
2	RW	0x1	ddrio_ret_en 1'b0: Remain ddr io status when system is failed 1'b1: Enable ddr io retension when system is failed
1	RW	0x0	wdt_shut_reset_trigger_en Enable failsafe wdt input 1'b0: Disable 1'b1: Enable
0	RW	0x0	tsadc_shut_reset_trigger_en Enable failsafe tsadc input 1'b0: Disable 1'b1: Enable

GRF_PMU_SOC_CON2

Address: Operational Base(0xFF010000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	pd_pmu0_srst_con_hold[15:0] Please refer to cru_pd_pmu0_srst_con. Each bit has a hold.

GRF_PMU_SOC_CON3

Address: Operational Base(0xFF010000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	pd_pmu0_rstn_hold0[19:16] Please refer to cru_pd_pmu0_srst_con. Each bit has a hold.

GRF_PMU_SOC_CON4

Address: Operational Base(0xFF010000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	pd_pmu1_rstn_hold0 pd_pmu1_rstn_hold0[14:0]: Please refer to cru_pd_pmu1_srst_con[14:0]. Each bit has a hold. pd_pmu1_rstn_hold0[15]: Reset hold for chiprstn_pd_pmu1.

GRF_PMU_SOC_CON5

Address: Operational Base(0xFF010000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:0	RW	0x081b	npor_out2chip_pulse_width Pulse width of triggered NPOR output. Multiplied with XIN_OSC clock period.

GRF_PMU_SOC_CON6

Address: Operational Base(0xFF010000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:0	RW	0x00	mcu_irqlatency The processor supports zero jitter interrupt latency for zero wait-state memory. IRQLATENCY specifies the minimum number of cycles between an interrupt that becomes pended in the NVIC, and the vector fetch for that interrupt being issued on the AHB-Lite interface.

GRF_PMU_SOC_CON7

Address: Operational Base(0xFF010000) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:0	RW	0x0000000	mcu_stcalib Systick timer counter. Stcalib[25]: Indicates that no alternative reference clock source has been integrated. Stcalib[24]: Tie this LOW if the system timer clock, the external reference clock, or SCLK as indicated by STCALIB[25], can guarantee an exact multiple of 10ms. Stcalib[23:0]: Indicates the processor is idle, waiting for an interrupt on either the IRQ, NMI, or internal SysTick, or HIGH level on RXEV.

GRF_PMU_SOC_CON8

Address: Operational Base(0xFF010000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	mcu_rxev A HIGH level on this input causes the architecture defined Event Register to be set in the NPU MCU processor. This causes a WFE instruction to complete. It also awakens the processor if it is sleeping as the result of encountering a WFE instruction when the Event Register is clear.
2	RW	0x0	mcu_nmi MCU Non-maskable interrupt
1	RW	0x0	mcu_edbgrq MCU external debug request.
0	RW	0x0	mcu_pmu_enable MCU internal PMU enable 0: Disable 1: Enable

GRF_PMU_SOC_CON9

Address: Operational Base(0xFF010000) + offset (0x0124)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	mcu_code_start_addr MCU code start address.

GRF_PMU_SOC_CON10

Address: Operational Base(0xFF010000) + offset (0x0128)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	mcu_experi_start_addr MCU experi start address.

GRF_PMU_SOC_CON11

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Address: Operational Base(0xFF010000) + offset (0x012C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	mcu_exsram_start_addr MCU exsram start address.

GRF_PMU_SOC_CON12

Address: Operational Base(0xFF010000) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	mcu_sram_start_addr MCU experi start address.

GRF_PMU_SOC_CON13

Address: Operational Base(0xFF010000) + offset (0x0134)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	grf_con_pwr3_sleep_gpio0a7_sel GPIO0a7 source selection. 1'b0: From GPIO controller 1'b1: From pwr3_sleep
0	RW	0x0	grf_con_pwr2_sleep_gpio0a6_sel GPIO0a6 source selection. 1'b0: From GPIO controller 1'b1: From pwr2_sleep

GRF_PMU_SOC_STATUS0

Address: Operational Base(0xFF010000) + offset (0x0138)

Bit	Attr	Reset Value	Description
31	RO	0x0	irq_gpio0 Interrupt status. 1'b0: No active 1'b1: Active
30	RO	0x0	irq_gpio0_exp Interrupt status. 1'b0: No active 1'b1: Active
29	RO	0x0	irq_sdmmc1_dect Interrupt status. 1'b0: No active 1'b1: Active
28	RO	0x0	irq_sdmmc0_dect Interrupt status. 1'b0: No active 1'b1: Active

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Bit	Attr	Reset Value	Description
27	RO	0x0	irq_pwm_pmu Interrupt status. 1'b0: No active 1'b1: Active
26	RO	0x0	irq_pwr_pwm_pmu Interrupt status. 1'b0: No active 1'b1: Active
25	RO	0x0	irq_i2c0_pmu Interrupt status. 1'b0: No active 1'b1: Active
24	RO	0x0	irq_spi0 Interrupt status. 1'b0: No active 1'b1: Active
23:21	RO	0x0	reserved
20	RW	0x0	pmu0_hptimer_en_status Hptimer status.
19:18	RO	0x0	reserved
17	RO	0x0	mcu_deepsleep Active only when SLEEPING is HIGH. Indicates that the SLEEPDEEP bit in the NVIC is set to 1.
16	RO	0x0	mcu_sleeping Indicates the processor is idle, waiting for an interrupt on either the IRQ, NMI, or internal SysTick, or HIGH level on RXEV.
15	RO	0x0	mcu_lockup Indicates that the processor is in the architect lock-up state, as the result of an unrecoverable exception.
14	RO	0x0	mcu_halted Indicates that the processor is in debug state. HALTED remains asserted for as long as the processor remains in debug state.
13	RO	0x0	reserved
12	RO	0x0	grf_st_pmumcu_txev A single SCLK cycle HIGH level is generated on this output every time an SEV instruction is executed on the MCU processor.
11:9	RO	0x0	reserved
8	RO	0x0	core_standbywfil2 L2WFI status of CPU. 1'b0: Not WFI 1'b1: WFI
7	RO	0x0	core_standbywfe_core3 WFE status of core3. 1'b0: Not WFE 1'b1: WFE
6	RO	0x0	core_standbywfe_core2 WFE status of core2. 1'b0: Not WFE 1'b1: WFE
5	RO	0x0	core_standbywfe_core1 WFE status of core1. 1'b0: Not WFE 1'b1: WFE

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Bit	Attr	Reset Value	Description
4	RO	0x0	core_standbywfe_core0 WFE status of core0. 1'b0: Not WFE 1'b1: WFE
3	RO	0x0	core_standbywfi_core3 WFI status of core3. 1'b0: Not WFI 1'b1: WFI
2	RO	0x0	core_standbywfi_core2 WFI status of core2. 1'b0: Not WFI 1'b1: WFI
1	RO	0x0	core_standbywfi_core1 WFI status of core1. 1'b0: Not WFI 1'b1: WFI
0	RO	0x0	core_standbywfi_core0 WFI status of core0. 1'b0: Not WFI 1'b1: WFI

GRF_PMU_PVTM_CON0

Address: Operational Base(0xFF010000) + offset (0x0180)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:0	RW	0x003	pvtm_clkout_div pvtm_clkout_div Frequence is pvtm_clkout_div*4+1

GRF_PMU_OS_REG0

Address: Operational Base(0xFF010000) + offset (0x0200)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_os_reg0 OS register

GRF_PMU_OS_REG1

Address: Operational Base(0xFF010000) + offset (0x0204)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_os_reg1 OS register

GRF_PMU_OS_REG2

Address: Operational Base(0xFF010000) + offset (0x0208)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_os_reg2 OS register

GRF_PMU_OS_REG3

Address: Operational Base(0xFF010000) + offset (0x020C)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_os_reg3 OS register

GRF_PMU_OS_REG4

Address: Operational Base(0xFF010000) + offset (0x0210)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_os_reg4 OS register

GRF_PMU_OS_REG5

Address: Operational Base(0xFF010000) + offset (0x0214)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_os_reg5 OS register

GRF_PMU_OS_REG6

Address: Operational Base(0xFF010000) + offset (0x0218)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_os_reg6 OS register

GRF_PMU_OS_REG7

Address: Operational Base(0xFF010000) + offset (0x021C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_os_reg7 OS register

GRF_PMU_OS_REG8

Address: Operational Base(0xFF010000) + offset (0x0220)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_os_reg8 OS register, once this reg is wrotten, it can't be reset

GRF_PMU_OS_REG9

Address: Operational Base(0xFF010000) + offset (0x0224)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_os_reg9 OS register, once this reg is wrotten, it can't be reset

GRF_PMU_OS_REG10

Address: Operational Base(0xFF010000) + offset (0x0228)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_os_reg10 OS register, once this reg is wrotten, it can't be reset

GRF_PMU_OS_REG11

Address: Operational Base(0xFF010000) + offset (0x022C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_os_reg11 OS register, once this reg is wrotten, it can't be reset

GRF_PMU_RESET_FUNCTION_STATUS

Address: Operational Base(0xFF010000) + offset (0x0230)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
3	RO	0x0	ddr_fail_safe_src ddr_fail_safe is active
2	RO	0x0	tsadc_shut_reset_src Reset by tsadc shut trigger
1	RO	0x0	wdt_reset_src Reset by wdt trigger
0	RO	0x0	first_reset_src Reset by first reset trigger

GRF_PMU_RESET_FUNCTION_CLR

Address: Operational Base(0xFF010000) + offset (0x0234)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	WO	0x0	ddr_fail_safe_src_clr Clear bit for ddr_fail_safe is active 1'b1: Clear enable 1'b0: Clear disable
2	WO	0x0	tsadc_shut_reset_src_clr Clear bit for reset by tsadc shut trigger 1'b1: Clear enable 1'b0: Clear disable
1	WO	0x0	wdt_reset_src_clr Clear bit for reset by wdt trigger 1'b1: Clear enable 1'b0: Clear disable
0	WO	0x0	first_reset_src_clr Clear bit for reset by first reset trigger 1'b1: Clear enable 1'b0: Clear disable

GRF_PMU_SIG_DETECT_CON

Address: Operational Base(0xFF010000) + offset (0x0380)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	sdmmc1_detectn_neg_irq_msk Enable sdmmc1 detectn negedge irq 1'b0: Disable 1'b1: Enable
2	RW	0x0	sdmmc1_detectn_pos_irq_msk Enable sdmmc1 detectn posedge irq 1'b0: Disable 1'b1: Enable
1	RW	0x0	sdmmc0_detectn_neg_irq_msk Enable sdmmc0 detectn negedge irq 1'b0: Disable 1'b1: Enable
0	RW	0x0	sdmmc0_detectn_pos_irq_msk Enable sdmmc0 detectn posedge irq 1'b0: Disable 1'b1: Enable

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GRF_PMU_SIG_DETECT_STATUS

Address: Operational Base(0xFF010000) + offset (0x0390)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RO	0x0	sdmmc1_detectn_neg_irq 1'b1: Irq asserted; 1'b0: No irq
2	RO	0x0	sdmmc1_detectn_pos_irq 1'b1: Irq asserted; 1'b0: No irq
1	RO	0x0	sdmmc0_detectn_neg_irq 1'b1: Irq asserted; 1'b0: No irq
0	RO	0x0	sdmmc0_detectn_pos_irq 1'b1: Irq asserted; 1'b0: No irq

GRF_PMU_SIG_DETECT_STATUS_CLEAR

Address: Operational Base(0xFF010000) + offset (0x03A0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	WO	0x0	sdmmc1_detectn_neg_irq_clr 1'b1: Clear irq
2	WO	0x0	sdmmc1_detectn_pos_irq_clr 1'b1: Clear irq
1	WO	0x0	sdmmc0_detectn_neg_irq_clr 1'b1: Clear irq
0	WO	0x0	sdmmc0_detectn_pos_irq_clr 1'b1: Clear irq

GRF_PMU_SDMMC_DET_COUNTER

Address: Operational Base(0xFF010000) + offset (0x03B0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x003e8	sdmmc_detectn_count sdmmc_detectn_count bit register

5.4 SYS_GRF Register Description

5.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
GRF_SYS_SOC_CON0	0x0400	W	0x00000000	SOC control register0
GRF_SYS_SOC_CON1	0x0404	W	0x00000800	SOC control register1
GRF_SYS_SOC_CON2	0x0408	W	0x00000000	SOC control register2
GRF_SYS_SOC_CON3	0x040C	W	0x00000000	SOC control register3
GRF_SYS_SOC_CON4	0x0410	W	0x00000000	SOC control register4
GRF_SYS_SOC_CON5	0x0414	W	0xFC000000	SOC control register5
GRF_SYS_SOC_CON6	0x0418	W	0xFFFF0000	SOC control register6
GRF_SYS_SOC_STATUS0	0x0430	W	0x0001FE3F	SOC status register0
GRF_SYS_SOC_STATUS1	0x0434	W	0x00000040	SOC status register1
GRF_SYS_SOC_STATUS2	0x0438	W	0x3F7FFFEF	SOC status register2
GRF_SYS_BIU_CON0	0x0440	W	0x00000000	NOC control register0
GRF_SYS_BIU_CON1	0x0444	W	0x00000000	NOC control register1

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Name	Offset	Size	Reset Value	Description
GRF_SYS_RAM_CON	0x0460	W	0x00005402	SRAM control register0
GRF_SYS_CORE_RAM_CON	0x0464	W	0x00000000	CORE SRAM control register
GRF_SYS_CPU_CON0	0x0500	W	0x00008000	SOC control register0
GRF_SYS_CPU_CON1	0x0504	W	0x00003FFC	SOC control register1
GRF_SYS_CPU_STATUS0	0x0510	W	0x00000000	CPU status register0
GRF_SYS_CPU_STATUS1	0x0514	W	0x00000003	CPU status register1
GRF_SYS_VI_CON0	0x0520	W	0x00000000	video input block register0
GRF_SYS_VI_CON1	0x0524	W	0x00000000	video input block register1
GRF_SYS_VI_STATUS0	0x0530	W	0x181F181F	video input block status register
GRF_SYS_GPU_CON0	0x0570	W	0x00000000	GPU control register0
GRF_SYS_GPU_CON1	0x0574	W	0xFFFFFFFF	GPU control register1
GRF_SYS_TSADC_CON	0x0580	W	0x00000000	TSADC Control Regesters
GRF_SYS_VO_CON0	0x05D0	W	0x00000000	video output disphy control register
GRF_SYS_VO_CON1	0x05D4	W	0x00000000	video output disphy control register
GRF_SYS_TOP_PVTPLL_CON0	0x0600	W	0x00000000	TOP PVTPLL control register0
GRF_SYS_TOP_PVTPLL_CON1	0x0604	W	0x00000000	TOP PVTPLL control register1
GRF_SYS_TOP_PVTPLL_CON2	0x0608	W	0x00000000	TOP PVTPLL control register2
GRF_SYS_TOP_PVTPLL_CON3	0x060C	W	0x00000000	TOP PVTPLL control register3
GRF_SYS_CPU_PVTPLL_CON0	0x0620	W	0x00000000	CPU PVTPLL control register0
GRF_SYS_CPU_PVTPLL_CON1	0x0624	W	0x00000000	CPU PVTPLL control register1
GRF_SYS_CPU_PVTPLL_CON2	0x0628	W	0x00000000	CPU PVTPLL control register2
GRF_SYS_CPU_PVTPLL_CON3	0x062C	W	0x00000000	CPU PVTPLL control register3
GRF_SYS_GPU_PVTPLL_CON0	0x0640	W	0x00000000	GPU PVTPLL control register0
GRF_SYS_GPU_PVTPLL_CON1	0x0644	W	0x00000000	GPU PVTPLL control register1
GRF_SYS_GPU_PVTPLL_CON2	0x0648	W	0x00000000	GPU PVTPLL control register2
GRF_SYS_GPU_PVTPLL_CON3	0x064C	W	0x00000000	GPU PVTPLL control register3
GRF_SYS_NPU_PVTPLL_CON0	0x0660	W	0x00000000	NPU PVTPLL control register0
GRF_SYS_NPU_PVTPLL_CON1	0x0664	W	0x00000000	NPU PVTPLL control register1
GRF_SYS_NPU_PVTPLL_CON2	0x0668	W	0x00000000	NPU PVTPLL control register2
GRF_SYS_NPU_PVTPLL_CON3	0x066C	W	0x00000000	NPU PVTPLL control register3
GRF_SYS_CHIP_ID	0x0800	W	0x00000DEA	CHIP ID

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.4.2 Detail Registers Description

GRF_SYS_SOC_CON0

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Address: Operational Base(0xFF030000) + offset (0x0400)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pmu_pwr_idle_req BIU_PMU idle request. 1'b0: Disable 1'b1: Enable
14	RO	0x0	reserved
13	RW	0x0	gic_cfgsdisable gic cfgsdisable
12	RW	0x0	cpu_ema_detect_en cpu_ema_detect_en
11	RW	0x0	mac100_speed Mac Speed indication/status. 1'b0: 10Mbps (MII) 1'b1: 100Mbps (MII)
10	RW	0x0	mac100_flowctrl MAC100 transmit flow control. When set high, instructs the MAC100 to transmit PAUSE Control frame in Full-duplex mode. In Half-duplex mode, the MAC100 enables the Back-pressure function until this signal is made low again
9:5	RW	0x00	gmac_clk_con Gmac clock configuration. bit0: rmii_mode 1'b0: rgmii 1'b1: rmii bit1: clk_mac_ref_gating_en 1'b1: gate rmii reference clock bit[3:2]: mii_txclk_sel_gmac When rmii_mode = 1: 2'd0: rmii 10Mbps 2'd1: rmii 100Mbps When rmii_mode = 0: 2'd2: rgmii 10Mbps 2'd3: rgmii 100Mbps other: rgmii 1Gbps bit4: 1'b0: clk source from cru 1'b1: clk source from io
4	RW	0x0	gmac_flowctrl GMAC transmit flow control. When set high, instructs the GMAC to transmit PAUSE Control frame in Full-duplex mode. In Half-duplex mode, the GMAC enables the Back-pressure function until this signal is made low again

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Bit	Attr	Reset Value	Description
3	RW	0x0	wdt_ns_pause_en Non-Secure wdt pause enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	pmu_wdtns_glb_reset_en non-secure watch dog reset enable 1'b0: Disable reset system 1'b1: Enable reset system
1	RW	0x0	npu_nsp_mem_soft_gate Enable RKNN NSP memory clock gating. 1'b0: Disable 1'b1: Enable
0	RW	0x0	npu_mem_ckg_enable Enable BIU_NPU memory clock gating. 1'b0: Disable 1'b1: Enable

GRF_SYS_SOC_CON1

Address: Operational Base(0xFF030000) + offset (0x0404)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RW	0x01	mac100_clk_con Gmac clock configuration. bit0: 1'b1 bit1: clk_mac_ref_gating_en 1'b1: gate rmii reference clock bit[3:2]: mii_txclk_sel_gmac 2'd0: rmii 10Mbps 2'd1: rmii 100Mbps bit4: 1'b0: clk source from cru 1'b1: clk source from io
10:9	RW	0x0	cache_slv_memattr Transaction memory attribute When support mpu mode, the cache controller will cache the request if both the hprot[3] and memattr[0] is high on AHB slave bus, or will bypass the request.
8	RW	0x0	mcu_cache_flush_req BUS mcu cache memory flush request.
7:0	RW	0x00	mcu_irqlatency The processor supports zero jitter interrupt latency for zero wait-state memory. IRQLATENCY specifies the minimum number of cycles between an interrupt that becomes pended in the NVIC, and the vector fetch for that interrupt being issued on the AHB-Lite interface.

GRF_SYS_SOC_CON2

Address: Operational Base(0xFF030000) + offset (0x0408)

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Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:0	RW	0x0000000	mcu_stcalib Systick timer counter. Stcalib[25]: Indicates that no alternative reference clock source has been integrated. Stcalib[24]: Tie this LOW if the system timer clock, the external reference clock, or SCLK as indicated by STCALIB[25], can guarantee an exact multiple of 10ms. Stcalib[23:0]: Indicates the processor is idle, waiting for an interrupt on either the IRQ, NMI, or internal SysTick, or HIGH level on RXEV.

GRF_SYS_SOC_CON3

Address: Operational Base(0xFF030000) + offset (0x040C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cache_ram_test_addr_start BUS MCU cache ram test start address.

GRF_SYS_SOC_CON4

Address: Operational Base(0xFF030000) + offset (0x0410)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cache_ram_test_addr_end BUS MCU cache ram test end address.

GRF_SYS_SOC_CON5

Address: Operational Base(0xFF030000) + offset (0x0414)

Bit	Attr	Reset Value	Description
31:0	RW	0xfc000000	cache_periphral_addr_start BUS MCU cache peripheral start address.

GRF_SYS_SOC_CON6

Address: Operational Base(0xFF030000) + offset (0x0418)

Bit	Attr	Reset Value	Description
31:0	RW	0xffff0000	cache_periphral_addr_end BUS MCU cache peripheral end address.

GRF_SYS_SOC_STATUS0

Address: Operational Base(0xFF030000) + offset (0x0430)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RW	0x0	gmac_sdb_tx_clk_gating_ctrl LPI Tx Clock Gating Control. This signal is high after the MAC enters the Tx LPI (low power idle) mode. You can use this signal to control the Tx clock gating.
24:23	RW	0x0	gmac_speed Mac Speed indication/status. 2'b00:1000Mbps (GMII) 2'b01: 2500Mbps (GMII) 2'b10: 10Mbps (MII) 2'b11: 100Mbps (MII)
22	RO	0x0	reserved
21	RO	0x0	vop_standby vop_standby status
20	RO	0x0	rknn_work_on rknn_work_on status

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Bit	Attr	Reset Value	Description
19	RO	0x0	vop_dma_finish voprawb_dma_finish status
18	RO	0x0	isp_shutter_open isp_shutter_open status
17	RO	0x0	scramble_shift_ready ddr_scramble seed shift ready status
16	RO	0x1	timer_en_status5 timer5_en status
15	RO	0x1	timer_en_status4 timer4_en status
14	RO	0x1	timer_en_status3 timer3_en status
13	RO	0x1	timer_en_status2 timer2_en status
12	RO	0x1	timer_en_status1 timer1_en status
11	RO	0x1	timer_en_status0 timer0_en status
10	RO	0x1	stimer_en_status1 stimer1_en status
9	RO	0x1	stimer_en_status0 stimer0_en status
8:6	RO	0x0	reserved
5	RO	0x1	hpll_lock HPLL lock status
4	RO	0x1	vpll_lock VPLL lock status
3	RO	0x1	gpll_lock GPLL lock status
2	RO	0x1	cpll_lock CPLL lock status
1	RO	0x1	dpll_lock DPLL lock status
0	RO	0x1	apll_lock APLL lock status

GRF_SYS_SOC_STATUS1

Address: Operational Base(0xFF030000) + offset (0x0434)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RO	0x1	cache_top_idle BUS MCU cache top idle acknowledge.
5	RO	0x0	mcu_deepsleep Active only when SLEEPING is HIGH. Indicates that the SLEEPDEEP bit in the NVIC is set to 1.
4	RO	0x0	mcu_sleeping Indicates the processor is idle, waiting for an interrupt on either the IRQ, NMI, or internal SysTick, or HIGH level on RXEV.
3	RO	0x0	mcu_lockup Indicates that the processor is in the architect lock-up state, as the result of an unrecoverable exception.
2	RO	0x0	mcu_halted Indicates that the processor is in debug state. HALTED remains asserted for as long as the processor remains in debug state.

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Bit	Attr	Reset Value	Description
1	RO	0x0	mcu_cache_flush_ack BUS MCU cache memory flush acknowledge.
0	RO	0x0	mcu_txev A single SCLK cycle HIGH level is generated on this output every time an SEV instruction is executed on the MCU processor.

GRF_SYS_SOC_STATUS2

Address: Operational Base(0xFF030000) + offset (0x0438)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x1	dma2ddr_m_I_mainNoPendingTrans BIU no pending trans status. 1'b0: Pending 1'b1: Idle
28	RO	0x1	rkvdec_m_I_mainNoPendingTrans BIU no pending trans status. 1'b0: Pending 1'b1: Idle
27	RO	0x1	vepu_m_I_mainNoPendingTrans BIU no pending trans status. 1'b0: Pending 1'b1: Idle
26	RO	0x1	vicap_m_I_mainNoPendingTrans BIU no pending trans status. 1'b0: Pending 1'b1: Idle
25	RO	0x1	isp_m_I_mainNoPendingTrans BIU no pending trans status. 1'b0: Pending 1'b1: Idle
24	RO	0x1	vop_m_I_mainNoPendingTrans BIU no pending trans status. 1'b0: Pending 1'b1: Idle
23	RO	0x0	reserved
22	RW	0x1	npu_m_I_mainNoPendingTrans BIU no pending trans status. 1'b0: Pending 1'b1: Idle
21	RW	0x1	mac100_m_I_mainNoPendingTrans BIU no pending trans status. 1'b0: Pending 1'b1: Idle
20	RO	0x1	rga_wr_m_I_mainNoPendingTrans BIU no pending trans status. 1'b0: Pending 1'b1: Idle
19	RO	0x1	rga_rd_m_I_mainNoPendingTrans BIU no pending trans status. 1'b0: Pending 1'b1: Idle
18	RO	0x1	jpeg_m_I_mainNoPendingTrans BIU no pending trans status. 1'b0: Pending 1'b1: Idle

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Bit	Attr	Reset Value	Description
17	RO	0x1	usb3_otg_m_I_mainNoPendingTrans BIU no pending trans status. 1'b0: Pending 1'b1: Idle
16	RO	0x1	pcie2x1_m_I_mainNoPendingTrans BIU no pending trans status. 1'b0: Pending 1'b1: Idle
15	RO	0x1	usb2_host_m_I_mainNoPendingTrans BIU no pending trans status. 1'b0: Pending 1'b1: Idle
14	RO	0x1	sfc_m_I_mainNoPendingTrans BIU no pending trans status. 1'b0: Pending 1'b1: Idle
13	RO	0x1	emmc_m_I_mainNoPendingTrans BIU no pending trans status. 1'b0: Pending 1'b1: Idle
12	RO	0x1	sdmmc1_m_I_mainNoPendingTrans BIU no pending trans status. 1'b0: Pending 1'b1: Idle
11	RO	0x1	sdmmc0_m_I_mainNoPendingTrans BIU no pending trans status. 1'b0: Pending 1'b1: Idle
10	RO	0x1	rkdmac_m_I_mainNoPendingTrans BIU no pending trans status. 1'b0: Pending 1'b1: Idle
9	RO	0x1	dmac_m_I_mainNoPendingTrans BIU no pending trans status. 1'b0: Pending 1'b1: Idle
8	RO	0x1	crypto_m_I_mainNoPendingTrans BIU no pending trans status. 1'b0: Pending 1'b1: Idle
7	RO	0x1	crypto_apb_m_I_mainNoPendingTrans BIU no pending trans status. 1'b0: Pending 1'b1: Idle
6	RO	0x1	gpu_m_I_mainNoPendingTrans BIU no pending trans status. 1'b0: Pending 1'b1: Idle
5	RO	0x1	daplite_apb_m_I_mainNoPendingTrans BIU no pending trans status. 1'b0: Pending 1'b1: Idle
4	RO	0x0	cpu_m_I_mainNoPendingTrans BIU no pending trans status. 1'b0: Pending 1'b1: Idle

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Bit	Attr	Reset Value	Description
3	RO	0x1	mcu_m_I_mainNoPendingTrans BIU no pending trans status. 1'b0: Pending 1'b1: Idle
2	RO	0x1	gmac_m_I_mainNoPendingTrans BIU no pending trans status. 1'b0: Pending 1'b1: Idle
1	RO	0x1	dft_apb_m_I_mainNoPendingTrans BIU no pending trans status. 1'b0: Pending 1'b1: Idle
0	RO	0x1	dcf_m_I_mainNopendingTrans BIU no pending trans status. 1'b0: Pending 1'b1: Idle

GRF_SYS_BIU_CON0

Address: Operational Base(0xFF030000) + offset (0x0440)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	npu_fwd_msch_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
14	RW	0x0	gpu_fwd_msch_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
13	RW	0x0	cpu_fwd_npu_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
12	RW	0x0	cpu_fwd_msch_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
11	RW	0x0	cpu_fwd_bus_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
10	RO	0x0	reserved
9	RW	0x0	bus_fwd_vdpu_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
8	RW	0x0	bus_fwd_top_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus

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Bit	Attr	Reset Value	Description
7	RW	0x0	bus_fwd_vo_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
6	RW	0x0	bus_fwd_pmu_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
5	RW	0x0	bus_fwd_vi_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
4	RW	0x0	bus_fwd_peri_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
3	RW	0x0	bus_fwd_gpu_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
2	RW	0x0	bus_fwd_msch_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
1	RW	0x0	bus_fwd_ddrc_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
0	RW	0x0	bus_fwd_rga_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus

GRF_SYS_BIU_CON1

Address: Operational Base(0xFF030000) + offset (0x0444)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	topmv_fwd_msch_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
12	RW	0x0	topmb_fwd_msch_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
11	RW	0x0	vdpu_fwd_top_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus

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Bit	Attr	Reset Value	Description
10	RW	0x0	vepu_fwd_vi_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
9	RW	0x0	vi_fwd_vepu_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
8	RW	0x0	vi_fwd_top_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
7	RW	0x0	vo_fwd_top_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
6:5	RO	0x0	reserved
4	RW	0x0	rga_fwd_vo_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
3	RW	0x0	php_fwd_peri_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
2	RW	0x0	peri_fwd_top_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
1	RW	0x0	peri_fwd_php_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus
0	RW	0x0	peri_fwd_bus_stall Response type when bus is force to idle state 1'b0: bus return error response 1'b1: bus return ok response and hold the bus

GRF_SYS_RAM_CON

Address: Operational Base(0xFF030000) + offset (0x0460)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	rom_trb ROM memory timing adjustment setting for debug purpose
13:12	RW	0x1	rom_rtsel ROM memory timing adjustment setting for debug purpose
11:10	RW	0x1	rom_ptsel ROM memory timing adjustment setting for debug purpose

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Bit	Attr	Reset Value	Description
9:8	RW	0x0	dpra_wtsel DPRA memory timing adjustment setting for debug purpose 2'b00:Recommended setting with the optimized write margin 2'b01:Relaxed write margin setting, used for debugging purpose. 2'b10:More relaxed write margin setting, used for debugging purpose. 2'b11:Most relaxed write margin setting, used for debugging purpose.
7:6	RW	0x0	dpra_rtsel DPRA memory timing adjustment setting for debug purpose 2'b00: Recommended setting with the optimized read margin. 2'b01: Relaxed read margin setting, used for debugging purpose. 2'b10: More relaxed read margin setting, used for debugging purpose. 2'b11: Most relaxed read margin setting, used for debugging purpose.
5:4	RW	0x0	dpra_ptsel DPRA memory timing adjustment setting for debug purpose 2'b00: Recommended setting for internal clock skew of port A/B with the optimized design margin and timing 2'b01: Relaxed setting for internal clock skew of port A/B used for debugging purpose 2'b10: More relaxed setting for internal clock skew of port A/B used for debugging purpose 2'b11: Most relaxed setting for internal clock skew of port A/B used for debugging purpose
3:2	RW	0x0	spra_wtsel SPRA mux1/2 memory timing adjustment setting for debug purpose
1:0	RW	0x2	spra_rtsel SPRA mux1/2 memory timing adjustment setting for debug purpose

GRF_SYS_CORE_RAM_CON

Address: Operational Base(0xFF030000) + offset (0x0464)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:6	RW	0x0	spra_mux4_wtsel SPRA mux4 memory timing adjustment setting for debug purpose
5:4	RW	0x0	spra_mux4_rtsel SPRA mux4 memory timing adjustment setting for debug purpose
3:2	RW	0x0	wtsel_cpu CPU SPRA memory timing adjustment setting for debug purpose.
1:0	RW	0x0	rtsel_cpu CPU SPRA memory timing adjustment setting for debug purpose.

GRF_SYS_CPU_CON0

Address: Operational Base(0xFF030000) + offset (0x0500)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	sysbardisable Disable broadcasting of barriers onto the system bus. 1'b0: Barriers are broadcast onto the system bus. This requires an AMBA 4 ACE or AMBA 5 CHI interconnect 1'b1: Barriers are not broadcast onto the system bus. This is compatible with an AXI3 interconnect, and most AMBA 4 interconnects
14	RW	0x0	broadcastouter Enable broadcasting of outer shareable transactions. 1'b0: Outer Shareable transactions are not broadcast externally 1'b1: Outer Shareable transactions are broadcast externally
13	RW	0x0	broadcastinner Enable broadcasting of Inner Shareable transactions. 1'b0: Inner Shareable transactions are not broadcast externally 1'b1: Inner Shareable transactions are broadcast externally
12	RW	0x0	broadcastcachemaint Enable broadcasting of cache maintenance operations to downstream caches. 1'b0: Cache maintenance operations are not broadcast to downstream caches 1'b1: Cache maintenance operations are broadcast to downstream caches
11	RW	0x0	evenctireq Event input for processor wake-up from WFE state. This pin must be asserted for at least one CLKIN clock cycles. When this signal is asserted, it acts as WFE wake-up event to all the cores in the cluster
10	RW	0x0	eventoack Set this bit to clear the evento rising edge state
9	RW	0x0	clrexmonreq Request to clear the external global exclusive monitor. This sends a WFE wake-up event to all cores in the cluster.
8	RW	0x0	l2_rstdisable Disable automatic L2 cache invalidate at reset. Only change this signal when the processor is in the reset state. 1'b0: Enable L2 cache invalidate at reset 1'b1: Disable L2 cache invalidate at reset
7:4	RW	0x0	cfgte Enable T32 exception. It sets the initial value of the TE bit in the SCTLR and HSCTLR register. Each bit is defined below. 1'b0: TE bit is low 1'b1: TE bit is high These bits are sampled only during reset of the core. Tie low for the ARM instruction set for exception handling. Tie high for the Thumb instruction set for exception handling. Only change it when the core is in the reset state

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	cfgend Endianness configuration at reset. It sets the initial value of the EE bits in the SCTLR, HSCTLR, SCTLR_EL1, SCTLR_EL2, and SCTLR_EL3 registers. Each bit is defined below. 1'b0: EE bit is low 1'b1: EE bit is high These bits are sampled only during reset of the core. Tie high for big-endian data during exception handling. Tie it low for little-endian data during exception handling. Only change it when the cores are in the state

GRF_SYS_CPU_CON1

Address: Operational Base(0xFF030000) + offset (0x0504)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	dbgl1rstdisable Disable L1 data cache automatic invalidate on reset functionality. 1'b0: Enable automatic invalidation of L1 data cache on reset 1'b1: Disable automatic invalidation of L1 data cache on reset
13:0	RW	0x3ffc	periphbase Specifies the base address for the GIC registers. This value is sampled into the CP15 Configuration Base Address Register (CBAR) at reset.

GRF_SYS_CPU_STATUS0

Address: Operational Base(0xFF030000) + offset (0x0510)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	wrmemattr Request memory write attributes.
23:16	RO	0x00	rdmemattr Request memory read attributes.
15:12	RO	0x0	smpen Indicates whether a core is taking part in coherency.
11	RO	0x0	eventiack Event input request acknowledge
10	RO	0x0	eventoreq Event output request for wake-up, triggered by SEV instruction
9	RO	0x0	clrexmonack Clearing of the external global exclusive monitor acknowledge.
8	RO	0x0	core_standbywfil2 Indicates that CPU is in a L2-WFI state.
7:4	RO	0x0	core_standbywfe Indicates that a core is in a WFE state.
3:0	RO	0x0	core_standbywfi Indicates that a core is in a WFI state.

GRF_SYS_CPU_STATUS1

Address: Operational Base(0xFF030000) + offset (0x0514)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
1	RO	0x1	jtagtop SWJ-DP Status. JTAG Active. Output is driven HIGH when the Debug Port is operating using the JTAG protocol.
0	RO	0x1	jtagnsw SWJ-DP Status. Serial Wire Active. Output is driven HIGH when the Debug Port is operating using the Serial Wire protocol.

GRF_SYS_VI_CON0

Address: Operational Base(0xFF030000) + offset (0x0520)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	csiphy1_lane_sel 1'b0: Full mode(one dphy with 4 lanes) ; 1'b1: Split mode(two dphy each with 2 lanes).
12	RW	0x0	csiphy0_lane_sel 1'b0: Full mode(one dphy with 4 lanes) ; 1'b1: Split mode(two dphy each with 2 lanes).
11	RW	0x0	csiphy0_clk1_inv_selection 1'b0: Disable clock inverter for clock lane1 1'b1: Enable clock inverter for clock lane1
10	RW	0x0	csiphy0_clklane1_en 1'b0: Disable clock1 lane 1'b1: Enable clock1 lane
9	RW	0x0	csiphy0_clk0_inv_selection 1'b0: Disable clock inverter for clock lane0 1'b1: Enable clock inverter for clock lane0
8	RW	0x0	csiphy0_clklane0_en 1'b0: Disable clock0 lane 1'b1: Enable clock0 lane
7	RW	0x0	csiphy0_datalane_en_3 1'b1: Enable csiphy lane3 1'b0: Disable csiphy_lane3
6	RW	0x0	csiphy0_datalane_en_2 1'b1: Enable csiphy lane2 1'b0: Disable csiphy_lane2
5	RW	0x0	csiphy0_datalane_en_1 1'b1: Enable csiphy lane1 1'b0: Disable csiphy_lane1
4	RW	0x0	csiphy0_datalane_en_0 1'b1: Enable csiphy lane0 1'b0: Disable csiphy_lane0
3	RW	0x0	csiphy0_forcerxmode_3 1'b1: Force to rx mode of lane3; 1'b0: Disable force control
2	RW	0x0	csiphy0_forcerxmode_2 1'b1: Force to rx mode of lane2; 1'b0: Disable force control

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Bit	Attr	Reset Value	Description
1	RW	0x0	csiphy0_forcerxmode_1 1'b1: Force to rx mode of lane1; 1'b0: Disable force control
0	RW	0x0	csiphy0_forcerxmode_0 1'b1: Force to rx mode od lane0; 1'b0: Disable force control

GRF_SYS_VI_CON1

Address: Operational Base(0xFF030000) + offset (0x0524)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	isp_width ISP interface isp_width control
13	RW	0x0	isp_shutter_trig ISP interface shutter_trig control
12	RO	0x0	reserved
11	RW	0x0	csiphy1_clk1_inv_selection 1'b0: Disable clock inverter for clock lane1 1'b1: Enable clock inverter for clock lane1
10	RW	0x0	csiphy1_clklane1_en 1'b0: Disable clock1 lane 1'b1: Enable clock1 lane
9	RW	0x0	csiphy1_clk0_inv_selection 1'b0: Disable clock inverter for clock lane0 1'b1: Enable clock inverter for clock lane0
8	RW	0x0	csiphy1_clklane0_en 1'b0: Disable clock0 lane 1'b1: Enable clock0 lane
7	RW	0x0	csiphy1_datalane_en_3 1'b1: Enable csiphy lane0 1'b0: Disable csiphy_lane0
6	RW	0x0	csiphy1_datalane_en_2 1'b1: Enable csiphy lane0 1'b0: Disable csiphy_lane0
5	RW	0x0	csiphy1_datalane_en_1 1'b1: Enable csiphy lane0 1'b0: Disable csiphy_lane0
4	RW	0x0	csiphy1_datalane_en_0 1'b1: Enable csiphy lane0 1'b0: Disable csiphy_lane0
3	RW	0x0	csiphy1_forcerxmode_3 1'b1: Force to rx mode of lane3; 1'b0: Disable force control
2	RW	0x0	csiphy1_forcerxmode_2 1'b1: Force to rx mode of lane2; 1'b0: Disable force control
1	RW	0x0	csiphy1_forcerxmode_1 1'b1: Force to rx mode of lane1; 1'b0: Disable force control
0	RW	0x0	csiphy1_forcerxmode_0 1'b1: Force to rx mode od lane0; 1'b0: Disable force control

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GRF_SYS_VI_STATUS0

Address: Operational Base(0xFF030000) + offset (0x0530)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RO	0x1	csiphy1_ulpsactivenotclk_1_raw ULP State (not) Active 1 status This active low signal is asserted to indicate that the Lane is in ULP state.
27	RO	0x1	csiphy1_ulpsactivenotclk_raw ULP State (not) Active status This active low signal is asserted to indicate that the Lane is in ULP state.
26	RO	0x0	csiphy1_errcontentionlp1_0 LP1 Contention error status
25	RO	0x0	csiphy1_errcontentionlp0_0 LP0 Contention error status
24	RO	0x0	csiphy1_rxskewcalhs_3 Lane3 high-speed receive skew calibration status
23	RO	0x0	csiphy1_rxskewcalhs_2 Lane2 high-speed receive skew calibration status
22	RO	0x0	csiphy1_rxskewcalhs_1 Lane1 high-speed receive skew calibration status
21	RO	0x0	csiphy1_rxskewcalhs_0 Lane0 high-speed receive skew calibration status
20	RO	0x1	csiphy1_direction Transmit/Receive direction. 1'b0: transmit mode 1'b1: receive mode
19	RO	0x1	csiphy1_ulpsactivenot_3 Lane3 ULP active status This active low signal is asserted to indicate that the Lane is in ULP state
18	RO	0x1	csiphy1_ulpsactivenot_2 Lane2 ULP active status This active low signal is asserted to indicate that the Lane is in ULP state
17	RO	0x1	csiphy1_ulpsactivenot_1 Lane1 ULP active status This active low signal is asserted to indicate that the Lane is in ULP state
16	RO	0x1	csiphy1_ulpsactivenot_0 Lane0 ULP active status This active low signal is asserted to indicate that the Lane is in ULP state
15:13	RO	0x0	reserved
12	RO	0x1	csiphy0_ulpsactivenotclk_1_raw ULP State (not) Active 1 status This active low signal is asserted to indicate that the Lane is in ULP state.
11	RO	0x1	csiphy0_ulpsactivenotclk_raw ULP State (not) Active status This active low signal is asserted to indicate that the Lane is in ULP state.
10	RO	0x0	csiphy0_errcontentionlp1_0 LP1 Contention error status

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Bit	Attr	Reset Value	Description
9	RO	0x0	csiphy0_errcontentionlp0_0 LP0 Contention error status
8	RO	0x0	csiphy0_rxskewcalhs_3 Lane3 high-speed receive skew calibration status
7	RO	0x0	csiphy0_rxskewcalhs_2 Lane2 high-speed receive skew calibration status
6	RO	0x0	csiphy0_rxskewcalhs_1 Lane1 high-speed receive skew calibration status
5	RO	0x0	csiphy0_rxskewcalhs_0 Lane0 high-speed receive skew calibration status
4	RO	0x1	csiphy0_direction Transmit/Receive direction. 1'b0: transmit mode 1'b1: receive mode
3	RO	0x1	csiphy0_ulpsactivenot_3 Lane3 ULP active status This active low signal is asserted to indicate that the Lane is in ULP state
2	RO	0x1	csiphy0_ulpsactivenot_2 Lane2 ULP active status This active low signal is asserted to indicate that the Lane is in ULP state
1	RO	0x1	csiphy0_ulpsactivenot_1 Lane1 ULP active status This active low signal is asserted to indicate that the Lane is in ULP state
0	RO	0x1	csiphy0_ulpsactivenot_0 Lane0 ULP active status This active low signal is asserted to indicate that the Lane is in ULP state

GRF_SYS_GPU_CON0

Address: Operational Base(0xFF030000) + offset (0x0570)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4:2	RW	0x0	stripping_granule Controls memory striping in level two cache. Memory accesses are striped across the cache slices. For each memory transaction, its Physical Address(PA) is used to select the Level 2 Cache (L2C) slice and the external ACE port 3'b000: 4KB 3'b001: 128KB 3'b010: 256KB 3'b011: 512KB 3'b100: 1KB 3'b101: 2KB
1	RW	0x0	niden gpu niden port control 1'b0: Noninvasive debug disable 1'b1: Noninvasive debug enable

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Bit	Attr	Reset Value	Description
0	RW	0x0	dbgen gpu dbgen port control 1'b0: Debug disable 1'b1: Debug enable

GRF_SYS_GPU_CON1

Address: Operational Base(0xFF030000) + offset (0x0574)

Bit	Attr	Reset Value	Description
31:0	RW	0xffffffff	gpu_texfmtenable Compressed texture format support control.

GRF_SYS_TSADC_CON

Address: Operational Base(0xFF030000) + offset (0x0580)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	tsadc_tsen tsadc_tsen
7	RO	0x0	reserved
6	RW	0x0	tsadc_ana_reg6 External voltage buffer control 0: disable voltage buffer 1: enable voltage buffer
5	RW	0x0	tsadc_ana_reg5 Temperature-related voltage filter bypass control 0: select filter 1: bypass filter
4	RW	0x0	tsadc_ana_reg4 Temperature-related voltage buffer control 0: disable voltage buffer 1: enable voltage buffer
3	RW	0x0	tsadc_ana_reg3 Temperature-related voltage control 0: select voltage 1 1: select voltage 2
2	RW	0x0	tsadc_ana_reg2 Bandgap voltage filter bypass control 0: select filter 1: bypass filter
1	RW	0x0	tsadc_ana_reg1 Bandgap voltage buffer control 0: disable voltage buffer and select AVDD as reference 1: enable voltage buffer and select bandgap voltage as reference
0	RW	0x0	tsadc_ana_reg0 Bandgap chopper enable control 0: disable chopper 1: enable chopper

GRF_SYS_VO_CON0

Address: Operational Base(0xFF030000) + offset (0x05D0)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5:4	RW	0x0	lvdsformat_lvds0_select 2'b00: VESA 24bit 2'b01: JEIDA 24bit 2'b10: JEIDA 18bit 2'b11: VESA 18bit
3	RW	0x0	lvdsformat_lvds0_msbsel 1'b0: LSB 1'b1:MSB
2	RW	0x0	dsi0_dpiupdatecfg DSI0 controller dpiupdatecfg control
1	RW	0x0	dsi0_dpicolorm DSI0 Controller dpicolorm configuration 1'b0: normal color modle 1'b1: reduced color mode
0	RW	0x0	dsi0_dpishutdn DSI0 Controller dpishutdn configuration 1'b0: enable display 1'b1: shutdown the disaplay

GRF_SYS_VO_CON1

Address: Operational Base(0xFF030000) + offset (0x05D4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	dsiphy0_txskewcalhs_3 Request to transmit skew calibration on lane3. 1'b1: Request; 1'b0: Idle
14	RW	0x0	dsiphy0_txskewcalhs_2 Request to transmit skew calibration on lane2. 1'b1: Request; 1'b0: Idle
13	RW	0x0	dsiphy0_txskewcalhs_1 Request to transmit skew calibration on lane1. 1'b1: Request; 1'b0: Idle
12	RW	0x0	dsiphy0_txskewcalhs_0 Request to transmit skew calibration on lane0. 1'b1: Request; 1'b0: Idle
11	RW	0x0	dsiphy0_txskewcalhs_ck Request to transmit skew calibration on clock lane. 1'b1: Request; 1'b4: Idle
10	RO	0x0	reserved
9	RW	0x0	lvds0_dclk_inv_sel 1'b0: Normal clock 1'b1: Inverted clock

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Bit	Attr	Reset Value	Description
8	RW	0x0	lvds0_dclk_div2_sel lvds dclk divided by 2 selection 1'b0: clock bypass 1'b1: clock divided by 2
7	RW	0x0	dsiphy0_lane3_frctxstpm Force DSI TX PHY lane3 into transmit mode and generate stop state 1'b0: Disable 1'b1: Enable
6	RW	0x0	dsiphy0_lane2_frctxstpm Force DSI TX PHY lane3 into transmit mode and generate stop state 1'b0: Disable 1'b1: Enable
5	RW	0x0	dsiphy0_lane1_frctxstpm Force DSI TX PHY lane3 into transmit mode and generate stop state 1'b0: Disable 1'b1: Enable
4	RW	0x0	dsiphy0_lane0_frctxstpm Force DSI TX PHY lane0 into transmit mode and generate stop state 1'b0: Disable 1'b1: Enable
3	RO	0x0	reserved
2	RW	0x0	dsiphy0_lane0_turndisable Disable Turn-around. This signal is used to prevent Lane from going into transmit mode, even if it observes a turn-around request on the Lane interconnect
1	RW	0x0	dsiphy0_lvds_mode DSI/LVDS combo PHY0 mode control 1'b0: dsi mode 1'b1: lvds mode
0	RW	0x0	dsiphy0_forcerxmode Force DSI TX PHY0 lane module into Receive mode, wait for stop state 1'b0: Disable 1'b1: Enable

GRF_SYS_TOP_PVTPLL_CON0

Address: Operational Base(0xFF030000) + offset (0x0600)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:23	RW	0x0	pvtpll_clk_div_cnt PVTPLL clock out divided nuber
22:16	RW	0x00	pvtpll_ring_length_sel PVTPLL delay cell element number control 7'b000: 10 7'b001: 20 7'b010: 30 7'b011: 40 ...
15	RW	0x0	pvtpll_bypass Bypass enable

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Bit	Attr	Reset Value	Description
14:13	RW	0x0	clk_div_osc PVTPLL osc_clock divided nuber
12:11	RW	0x0	clk_div_ref PVTPLL ref_clock divided nuber
10:8	RW	0x0	pvtpll_osc_sel osc_ring selection. 3'b000: osc_ring 0 3'b001: osc_ring 1 3'b010: osc_ring 2 3'b011: osc_ring 3 3'b100: osc_ring 4
7:3	RO	0x00	reserved
2	RW	0x0	pvtpll_out_polar PVTPLL output polarity
1	RW	0x0	pvtpll_osc_en Set high to enable the osc_ring in the PVTPLL
0	RW	0x0	pvtpll_start Set high to start PVTPLL

GRF_SYS_TOP_PVTPLL_CON1

Address: Operational Base(0xFF030000) + offset (0x0604)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtpll_cal_cnt PVTPLL calculation counter

GRF_SYS_TOP_PVTPLL_CON2

Address: Operational Base(0xFF030000) + offset (0x0608)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	ckg_val PVTPLL control for ckg_val
15:0	RW	0x0000	pvtpll_threshold Threshold control for voltage adjustment

GRF_SYS_TOP_PVTPLL_CON3

Address: Operational Base(0xFF030000) + offset (0x060C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtpll_ref_cnt PVTPLL reference counter

GRF_SYS_CPU_PVTPLL_CON0

Address: Operational Base(0xFF030000) + offset (0x0620)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:23	RW	0x0	pvtpll_clk_div_cnt PVTPLL clock out divided nuber
22:16	RW	0x00	pvtpll_ring_length_sel PVTPLL delay cell element number control 7'b000: 10 7'b001: 20 7'b010: 30 7'b011: 40 ...
15	RW	0x0	pvtpll_bypass Bypass enable

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Bit	Attr	Reset Value	Description
14:13	RW	0x0	clk_div_osc PVTPLL osc_clock divided nuber
12:11	RW	0x0	clk_div_ref PVTPLL ref_clock divided nuber
10:8	RW	0x0	pvtpll_osc_sel osc_ring selection. 3'b000: osc_ring 0 3'b001: osc_ring 1 3'b010: osc_ring 2 3'b011: osc_ring 3 3'b100: osc_ring 4
7:3	RO	0x00	reserved
2	RW	0x0	pvtpll_out_polar PVTPLL output polarity
1	RW	0x0	pvtpll_osc_en Set high to enable the osc_ring in the PVTPLL
0	RW	0x0	pvtpll_start Set high to start PVTPLL

GRF_SYS_CPU_PVTPLL_CON1

Address: Operational Base(0xFF030000) + offset (0x0624)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtpll_cal_cnt PVTPLL calculation counter

GRF_SYS_CPU_PVTPLL_CON2

Address: Operational Base(0xFF030000) + offset (0x0628)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	ckg_val PVTPLL control for ckg_val
15:0	RW	0x0000	pvtpll_threshold Threshold control for voltage adjustment

GRF_SYS_CPU_PVTPLL_CON3

Address: Operational Base(0xFF030000) + offset (0x062C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtpll_ref_cnt PVTPLL reference counter

GRF_SYS_GPU_PVTPLL_CON0

Address: Operational Base(0xFF030000) + offset (0x0640)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:23	RW	0x0	pvtpll_clk_div_cnt PVTPLL clock out divided nuber
22:16	RW	0x00	pvtpll_ring_length_sel PVTPLL delay cell element number control 7'b000: 10 7'b001: 20 7'b010: 30 7'b011: 40 ...
15	RW	0x0	pvtpll_bypass Bypass enable

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Bit	Attr	Reset Value	Description
14:13	RW	0x0	clk_div_osc PVTPLL osc_clock divided nuber
12:11	RW	0x0	clk_div_ref PVTPLL ref_clock divided nuber
10:8	RW	0x0	pvtpll_osc_sel osc_ring selection. 3'b000: osc_ring 0 3'b001: osc_ring 1 3'b010: osc_ring 2 3'b011: osc_ring 3 3'b100: osc_ring 4
7:3	RO	0x00	reserved
2	RW	0x0	pvtpll_out_polar PVTPLL output polarity
1	RW	0x0	pvtpll_osc_en Set high to enable the osc_ring in the PVTPLL
0	RW	0x0	pvtpll_start Set high to start PVTPLL

GRF_SYS_GPU_PVTPLL_CON1

Address: Operational Base(0xFF030000) + offset (0x0644)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtpll_cal_cnt PVTPLL calculation counter

GRF_SYS_GPU_PVTPLL_CON2

Address: Operational Base(0xFF030000) + offset (0x0648)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	ckg_val PVTPLL control for ckg_val
15:0	RW	0x0000	pvtpll_threshold Threshold control for voltage adjustment

GRF_SYS_GPU_PVTPLL_CON3

Address: Operational Base(0xFF030000) + offset (0x064C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtpll_ref_cnt PVTPLL reference counter

GRF_SYS_NPU_PVTPLL_CON0

Address: Operational Base(0xFF030000) + offset (0x0660)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:23	RW	0x0	pvtpll_clk_div_cnt PVTPLL clock out divided nuber
22:16	RW	0x00	pvtpll_ring_length_sel PVTPLL delay cell element number control 7'b000: 10 7'b001: 20 7'b010: 30 7'b011: 40 ...
15	RW	0x0	pvtpll_bypass Bypass enable

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Bit	Attr	Reset Value	Description
14:13	RW	0x0	clk_div_osc PVTPLL osc_clock divided nuber
12:11	RW	0x0	clk_div_ref PVTPLL ref_clock divided nuber
10:8	RW	0x0	pvtpll_osc_sel osc_ring selection. 3'b000: osc_ring 0 3'b001: osc_ring 1 3'b010: osc_ring 2 3'b011: osc_ring 3 3'b100: osc_ring 4
7:3	RO	0x00	reserved
2	RW	0x0	pvtpll_out_polar PVTPLL output polarity
1	RW	0x0	pvtpll_osc_en Set high to enable the osc_ring in the PVTPLL
0	RW	0x0	pvtpll_start Set high to start PVTPLL

GRF_SYS_NPU_PVTPLL_CON1

Address: Operational Base(0xFF030000) + offset (0x0664)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtpll_cal_cnt PVTPLL calculation counter

GRF_SYS_NPU_PVTPLL_CON2

Address: Operational Base(0xFF030000) + offset (0x0668)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	ckg_val PVTPLL control for ckg_val
15:0	RW	0x0000	pvtpll_threshold Threshold control for voltage adjustment

GRF_SYS_NPU_PVTPLL_CON3

Address: Operational Base(0xFF030000) + offset (0x066C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtpll_ref_cnt PVTPLL reference counter

GRF_SYS_CHIP_ID

Address: Operational Base(0xFF030000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000dea	chip_id

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5.5 PERI_GRF Register Description

5.5.1 Registers Summary

Name	Offset	Size	Reset Value	Description
GRF_PERI_PERI_CON0	0x0000	W	0x00000000	PERI control register0
GRF_PERI_PERI_CON1	0x0004	W	0x000007FC	PERI control register1
GRF_PERI_PERI_CON2	0x0008	W	0x00000000	PERI control register2

Name	Offset	Size	Reset Value	Description
GRF_PERI_PERI_CON3	0x000C	W	0x00000000	PERI control register3
GRF_PERI_PERI_CON4	0x0010	W	0x00000000	PERI control register4
GRF_PERI_DMAC0_CON0	0x0020	W	0x0000FFFF	dma control register0
GRF_PERI_DMAC0_CON1	0x0024	W	0x0000FFFF	dma control register1
GRF_PERI_DMAC0_CON2	0x0028	W	0x0000FFFF	dma control register2
GRF_PERI_DMAC0_CON3	0x002C	W	0x00000001	dma control register3
GRF_PERI_DMAC0_CON4	0x0030	W	0x00005555	dma control register4
GRF_PERI_DMAC0_CON5	0x0034	W	0x00005555	dma control register5
GRF_PERI_DMAC0_CON6	0x0038	W	0x00005555	dma control register6
GRF_PERI_DMAC0_CON7	0x003C	W	0x00005555	dma control register7
GRF_PERI_DMAC0_CON8	0x0040	W	0x00000000	dma control register8
GRF_PERI_DMAC0_CON9	0x0044	W	0x00000000	dma control register9
GRF_PERI_SECURE_CON	0x0050	W	0x00000004	secure control register
GRF_PERI_SECURE_STATUS	0x0060	W	0x00000101	secure status
GRF_PERI_AUDIO_CON	0x0070	W	0x00000000	AUDIO control register
GRF_PERI_HOST_CON0	0x0080	W	0x00000820	USB host control register0
GRF_PERI_HOS0_CON1	0x0084	W	0x000004BC	USB host control register1
GRF_PERI_HOST_STATUS	0x008C	W	0x00000000	USB host status register
GRF_PERI_USB3OTG_CON0	0x0090	W	0x00002000	usb3otg control register0
GRF_PERI_USB3OTG_CON1	0x0094	W	0x00001100	usb3otg control register1
GRF_PERI_USB3OTG_CON2	0x0098	W	0x00000000	usb3otg control register2
GRF_PERI_USB3OTG_STATUS_LAT0	0x00A0	W	0x00000000	usb3otg status_lat0 register
GRF_PERI_USB3OTG_STATUS_LAT1	0x00A4	W	0x00000000	usb3otg status_lat1 register
GRF_PERI_USB3OTG_STATUS_CB	0x00A8	W	0x000007E8	usb3otg status_cb register
GRF_PERI_USB3OTG_STATUS	0x00AC	W	0x00000000	usb3otg status register
GRF_PERI_SARADC0_CON	0x00B0	W	0x00000007	SARADC0 Contronl Registers

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.5.2 Detail Registers Description

GRF_PERI_PERI_CON0

Address: Operational Base(0xFF040000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	uart8_rts_inv uart8_rts polarity selection 1'b0: Low asserted 1'b1: High asserted
14	RW	0x0	uart8_cts_inv uart8_cts polarity selection 1'b0: Low asserted 1'b1: High asserted

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Bit	Attr	Reset Value	Description
13	RW	0x0	uart7_rts_inv uart7_rts polarity selection 1'b0: Low asserted 1'b1: High asserted
12	RW	0x0	uart7_cts_inv uart7_cts polarity selection 1'b0: Low asserted 1'b1: High asserted
11	RW	0x0	uart6_rts_inv uart6_rts polarity selection 1'b0: Low asserted 1'b1: High asserted
10	RW	0x0	uart6_cts_inv uart6_cts polarity selection 1'b0: Low asserted 1'b1: High asserted
9	RW	0x0	uart5_rts_inv uart5_rts polarity selection 1'b0: Low asserted 1'b1: High asserted
8	RW	0x0	uart5_cts_inv uart5_cts polarity selection 1'b0: Low asserted 1'b1: High asserted
7	RW	0x0	uart4_rts_inv uart4_rts polarity selection 1'b0: Low asserted 1'b1: High asserted
6	RW	0x0	uart4_cts_inv uart4_cts polarity selection 1'b0: Low asserted 1'b1: High asserted
5	RW	0x0	uart3_rts_inv uart3_rts polarity selection 1'b0: Low asserted 1'b1: High asserted
4	RW	0x0	uart3_cts_inv uart3_cts polarity selection 1'b0: Low asserted 1'b1: High asserted
3	RW	0x0	uart2_rts_inv uart2_rts polarity selection 1'b0: Low asserted 1'b1: High asserted
2	RW	0x0	uart2_cts_inv uart2_cts polarity selection 1'b0: Low asserted 1'b1: High asserted
1	RW	0x0	uart1_rts_inv uart1_rts polarity selection 1'b0: Low asserted 1'b1: High asserted
0	RW	0x0	uart1_cts_inv uart1_cts polarity selection 1'b0: Low asserted 1'b1: High asserted

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GRF_PERI_PERI_CON1

Address: Operational Base(0xFF040000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pcie20_link_rst_grt PCIe20 link rest grant control
14:12	RO	0x0	reserved
11	RW	0x0	can1_use_uart5_dma can1 and uart5 dma function select 1'b0: uart5 dma fucntion effective 1'b1: can1 dma function effective
10	RW	0x1	uart8_dma_rx_single_bypass uart_dma_rx_single_bypass 1'b0: no bypass 1'b1: bypass
9	RW	0x1	uart9_dma_rx_single_bypass uart_dma_rx_single_bypass 1'b0: no bypass 1'b1: bypass
8	RW	0x1	uart7_dma_rx_single_bypass uart_dma_rx_single_bypass 1'b0: no bypass 1'b1: bypass
7	RW	0x1	uart6_dma_rx_single_bypass uart_dma_rx_single_bypass 1'b0: no bypass 1'b1: bypass
6	RW	0x1	uart5_dma_rx_single_bypass uart_dma_rx_single_bypass 1'b0: no bypass 1'b1: bypass
5	RW	0x1	uart4_dma_rx_single_bypass uart_dma_rx_single_bypass 1'b0: no bypass 1'b1: bypass
4	RW	0x1	uart3_dma_rx_single_bypass uart_dma_rx_single_bypass 1'b0: no bypass 1'b1: bypass
3	RW	0x1	uart2_dma_rx_single_bypass uart_dma_rx_single_bypass 1'b0: no bypass 1'b1: bypass
2	RW	0x1	uart1_dma_rx_single_bypass uart1_dma_rx_single_bypass 1'b0: no bypass 1'b1: bypass
1	RW	0x0	uart9_rts_inv uart9_rts polarity selection 1'b0: Low asserted 1'b1: High asserted

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Bit	Attr	Reset Value	Description
0	RW	0x0	uart9_cts_inv uart9_cts polarity selection 1'b0: Low asserted 1'b1: High asserted

GRF_PERI_PERI_CON2

Address: Operational Base(0xFF040000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	spi1_tx_dma_sel 1'b0: use dma_bus 1'b1: use rkdma
14	RW	0x0	spi1_rx_dma_sel 1'b0: use dma_bus 1'b1: use rkdma
13	RW	0x0	spi0_tx_dma_sel 1'b0: use dma_bus 1'b1: use rkdma
12	RW	0x0	spi0_rx_dma_sel 1'b0: use dma_bus 1'b1: use rkdma
11	RW	0x0	uart5_tx_dma_sel 1'b0: use dma_bus 1'b1: use rkdma
10	RW	0x0	uart5_rx_dma_sel 1'b0: use dma_bus 1'b1: use rkdma
9	RW	0x0	uart4_tx_dma_sel 1'b0: use dma_bus 1'b1: use rkdma
8	RW	0x0	uart4_rx_dma_sel 1'b0: use dma_bus 1'b1: use rkdma
7	RW	0x0	uart3_tx_dma_sel 1'b0: use dma_bus 1'b1: use rkdma
6	RW	0x0	uart3_rx_dma_sel 1'b0: use dma_bus 1'b1: use rkdma
5	RW	0x0	uart2_tx_dma_sel 1'b0: use dma_bus 1'b1: use rkdma
4	RW	0x0	uart2_rx_dma_sel 1'b0: use dma_bus 1'b1: use rkdma
3	RW	0x0	uart1_tx_dma_sel 1'b0: use dma_bus 1'b1: use rkdma
2	RW	0x0	uart1_rx_dma_sel 1'b0: use dma_bus 1'b1: use rkdma

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Bit	Attr	Reset Value	Description
1	RW	0x0	uart6_tx_dma_sel 1'b0: use dma_bus 1'b1: use rkdma
0	RW	0x0	uart6_rx_dma_sel 1'b0: use dma_bus 1'b1: use rkdma

GRF_PERI_PERI_CON3

Address: Operational Base(0xFF040000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pdm_dma_sel 1'b0: use dma_bus 1'b1: use rkdma
14	RW	0x0	spdif_dma_sel 1'b0: use dma_bus 1'b1: use rkdma
13	RW	0x0	pwm3_dma_sel 1'b0: use dma_bus 1'b1: use rkdma
12	RW	0x0	pwm2_dma_sel 1'b0: use dma_bus 1'b1: use rkdma
11	RW	0x0	pwm1_dma_sel 1'b0: use dma_bus 1'b1: use rkdma
10	RW	0x0	pwm0_dma_sel 1'b0: use dma_bus 1'b1: use rkdma
9	RW	0x0	can0_tx_dma_sel 1'b0: use dma_bus 1'b1: use rkdma
8	RW	0x0	can0_rx_dma_sel 1'b0: use dma_bus 1'b1: use rkdma
7	RW	0x0	sai2_2ch_tx_dma_sel 1'b0: use dma_bus 1'b1: use rkdma
6	RW	0x0	sai2_2ch_rx_dma_sel 1'b0: use dma_bus 1'b1: use rkdma
5	RW	0x0	sai1_8ch_tx_dma_sel 1'b0: use dma_bus 1'b1: use rkdma
4	RW	0x0	sai1_8ch_rx_dma_sel 1'b0: use dma_bus 1'b1: use rkdma
3	RW	0x0	sai0_8ch_tx_dma_sel 1'b0: use dma_bus 1'b1: use rkdma

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Bit	Attr	Reset Value	Description
2	RW	0x0	sai0_8ch_rx_dma_sel 1'b0: use dma_bus 1'b1: use rkdma
1	RW	0x0	spi2_tx_dma_sel 1'b0: use dma_bus 1'b1: use rkdma
0	RW	0x0	spi2_rx_dma_sel 1'b0: use dma_bus 1'b1: use rkdma

GRF_PERI_PERI_CON4

Address: Operational Base(0xFF040000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	uart9_tx_dma_sel 1'b0: dma function disabled 1'b1: use rkdma
8	RW	0x0	uart9_rx_dma_sel 1'b0: dma function disabled 1'b1: use rkdma
7	RW	0x0	uart8_tx_dma_sel 1'b0: dma function disabled 1'b1: use rkdma
6	RW	0x0	uart8_rx_dma_sel 1'b0: dma function disabled 1'b1: use rkdma
5	RW	0x0	uart7_tx_dma_sel 1'b0: dma function disabled 1'b1: use rkdma
4	RW	0x0	uart7_rx_dma_sel 1'b0: dma function disabled 1'b1: use rkdma
3	RW	0x0	uart0_tx_dma_sel 1'b0: dma function disabled 1'b1: use rkdma
2	RW	0x0	uart0_rx_dma_sel 1'b0: dma function disabled 1'b1: use rkdma
1	RW	0x0	can1_tx_dma_sel 1'b0: use dma_bus when grf_can1_use_uart5_dma effective 1'b1: use rkdma
0	RW	0x0	can1_rx_dma_sel 1'b0: use dma_bus when grf_can1_use_uart5_dma effective 1'b1: use rkdma

GRF_PERI_DMAC0_CON0

Address: Operational Base(0xFF040000) + offset (0x0020)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0xffff	dma0_irq_boot_nonsec 1'b0: Secure 1'b1: Non-sercure

GRF_PERI_DMAC0_CON1

Address: Operational Base(0xFF040000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0xffff	dma0_peri_ch_nonsec_15_0 1'b0 : Secure 1'b1 : Non-sercure

GRF_PERI_DMAC0_CON2

Address: Operational Base(0xFF040000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0xffff	dma0_peri_ch_nonsec_31_16 1'b0: Secure 1'b1: Non-sercure

GRF_PERI_DMAC0_CON3

Address: Operational Base(0xFF040000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x1	dma0_manager_boot_nonsec 1'b0: Secure 1'b1: Non-sercure

GRF_PERI_DMAC0_CON4

Address: Operational Base(0xFF040000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	grf_type_uart_3_rx DMAC type of acknowledgement or request for UART_3 rx signals
13:12	RW	0x1	grf_type_uart_3_tx DMAC type of acknowledgement or request for UART_3 tx signals
11:10	RW	0x1	grf_type_uart_2_rx DMAC type of acknowledgement or request for UART_2 rx signals

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Bit	Attr	Reset Value	Description
9:8	RW	0x1	grf_type_uart_2_tx DMAC type of acknowledgement or request for UART_2 tx signals
7:6	RW	0x1	grf_type_uart_1_rx DMAC type of acknowledgement or request for UART_1 rx signals
5:4	RW	0x1	grf_type_uart_1_tx DMAC type of acknowledgement or request for UART_1 tx signals
3:2	RW	0x1	grf_type_uart_6_rx DMAC type of acknowledgement or request for UART_6 rx signals
1:0	RW	0x1	grf_type_uart_6_tx DMAC type of acknowledgement or request for UART_6 tx signals

GRF_PERI_DMAC0_CON5

Address: Operational Base(0xFF040000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	grf_type_spi1_rx DMAC type of acknowledgement or request for SPI1 rx signals
13:12	RW	0x1	grf_type_spi1_tx DMAC type of acknowledgement or request for spi1 tx signals
11:10	RW	0x1	grf_type_spi0_rx DMAC type of acknowledgement or request for SPI0 rx signals
9:8	RW	0x1	grf_type_spi0_tx DMAC type of acknowledgement or request for SPI0 tx signals
7:6	RW	0x1	grf_type_uart_5_rx DMAC type of acknowledgement or request for UART_5 rx signals
5:4	RW	0x1	grf_type_uart_5_tx DMAC type of acknowledgement or request for UART_5 tx signals
3:2	RW	0x1	grf_type_uart_4_rx DMAC type of acknowledgement or request for UART_4 rx signals
1:0	RW	0x1	grf_type_uart_4_tx DMAC type of acknowledgement or request for UART_4 tx signals

GRF_PERI_DMAC0_CON6

Address: Operational Base(0xFF040000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	grf_type_sai2_rx DMAC type of acknowledgement or request for SAI2 rx signals
13:12	RW	0x1	grf_type_sai2_tx DMAC type of acknowledgement or request for SAI2 tx signals
11:10	RW	0x1	grf_type_sai1_rx DMAC type of acknowledgement or request for SAI1 rx signals
9:8	RW	0x1	grf_type_sai1_tx DMAC type of acknowledgement or request for SAI1 tx signals
7:6	RW	0x1	grf_type_sai0_rx DMAC type of acknowledgement or request for SAI0 rx signals
5:4	RW	0x1	grf_type_sai0_tx DMAC type of acknowledgement or request for SAI0 tx signals

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Bit	Attr	Reset Value	Description
3:2	RW	0x1	grf_type_spi2_rx DMAC type of acknowledgement or request for SPI2 rx signals
1:0	RW	0x1	grf_type_spi2_tx DMAC type of acknowledgement or request for SPI2 tx signals

GRF_PERI_DMAC0_CON7

Address: Operational Base(0xFF040000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	grf_type_pdm_tx DMAC type of acknowledgement or request for PDM tx signals
13:12	RW	0x1	grf_type_spdif_tx DMAC type of acknowledgement or request for SPDIF tx signals
11:10	RW	0x1	grf_type_pwm3_tx DMAC type of acknowledgement or request for PWM3 tx signals
9:8	RW	0x1	grf_type_pwm2_tx DMAC type of acknowledgement or request for PWM2 tx signals
7:6	RW	0x1	grf_type_pwm1_tx DMAC type of acknowledgement or request for PWM1 tx signals
5:4	RW	0x1	grf_type_pwm0_tx DMAC type of acknowledgement or request for PWM0 tx signals
3:2	RW	0x1	grf_type_can0_rx DMAC type of acknowledgement or request for CAN0 rx signals
1:0	RW	0x1	grf_type_can0_tx DMAC type of acknowledgement or request for CAN0 tx signals

GRF_PERI_DMAC0_CON8

Address: Operational Base(0xFF040000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	grf_dma0_req_modify_dis dma0 peri channel request mode. bit0-15 correspond to ch0-15 1'b0: Request valid only when last ack is finish 1'b1: Request directly from peri device

GRF_PERI_DMAC0_CON9

Address: Operational Base(0xFF040000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	grf_dma0_req_modify_dis dma0 peri channel request mode. bit0-15 correspond to ch16-31 1'b0: Request valid only when last ack is finish 1'b1: Request directly from peri device

GRF_PERI_SECURE_CON

Address: Operational Base(0xFF040000) + offset (0x0050)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	optcns_lock otpc-non-secure lock signal
6	RW	0x0	otpcs_lock otpc-secure lock signal
5:3	RO	0x0	reserved
2	RW	0x1	trng_ns_rst_sync_bypass trng_ns_rst_sync_bypass
1	RW	0x0	trng_ns_ctrl_reseed trng_ns_ctrl_reseed
0	RW	0x0	trng_ns_ctrl_zeroize trng_ns_ctrl_zeroize

GRF_PERI_SECURE_STATUS

Address: Operational Base(0xFF040000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	otps_user_busy Secure OTPC status user interface busy
14	RO	0x0	otps_sbpi_busy Secure OTPC status sbpi interface busy
13	RO	0x0	trng_s_ctrl_rand_vld Secure TRNG status Serial random bit valid output, high valid
12	RO	0x0	trng_s_ctrl_rand_bit Secure TRNG status Serial random bit output
11	RO	0x0	trng_s_ctrl_seeded Secure TRNG status (Re)Seeding completion output, high valid
10	RO	0x0	trng_s_ctrl_reseeding Secure TRNG status Reseeding activity output, high valid
9	RO	0x0	trng_s_ctrl_reminder Secure TRNG status Reseed reminder output, high pulse valid
8	RO	0x1	trng_s_ctrl_secure Secure TRNG status secure mode output, high valid
7	RO	0x0	otpns_user_busy Non-Secure OTPC status user interface busy
6	RO	0x0	otpns_sbpi_busy Non-Secure OTPC status sbpi interface busy
5	RO	0x0	trng_ns_ctrl_rand_vld Non-Secure TRNG status Serial random bit valid output, high valid

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Bit	Attr	Reset Value	Description
4	RO	0x0	trng_ns_ctrl_rand_bit Non-Secure TRNG status Serial random bit output
3	RO	0x0	trng_ns_ctrl_seeded Non-Secure TRNG status (Re)Seeding completion output, high valid
2	RO	0x0	trng_ns_ctrl_reseeding Non-Secure TRNG status Reseeding activity output, high valid
1	RO	0x0	trng_ns_ctrl_reminder Non-Secure TRNG status Reseed reminder output, high pulse valid
0	RO	0x1	trng_ns_ctrl_secure Non-Secure TRNG status secure mode output, high valid

GRF_PERI_AUDIO_CON

Address: Operational Base(0xFF040000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	rkdsm_sai_active sai1 usage selection 1'b0: Used as IO with external SAI bus device 1'b1: Used to comunucatied with dsm IP
13:12	RO	0x0	reserved
11	RW	0x0	sai2_mclk_oe sai2 mclk source selection 1'b0: from external chip 1'b1: from cru
10	RO	0x0	reserved
9	RW	0x0	sai1_mclk_oe sai1 mclk source selection 1'b0: from external chip 1'b1: from cru
8:5	RO	0x0	reserved
4	RW	0x0	sai0_mclk_oe sai0 mclk source selection 1'b0: from external chip 1'b1: from cru
3:0	RO	0x0	reserved

GRF_PERI_HOST_CON0

Address: Operational Base(0xFF040000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:6	RW	0x20	host0_fladj_val_common USB HOST0 fladj_val_common bit control

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Bit	Attr	Reset Value	Description
5:0	RW	0x20	host0_fladj_val USB HOST0 fladj bit control

GRF_PERI_HOS0_CON1

Address: Operational Base(0xFF040000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	host0_arb_pause host0 ehci/ohci arbiter pause control
12	RW	0x0	host0_ohci_susp_lgcy USB HOST0 ohci_susp_lgcy bit control
11	RW	0x0	host0_ohci_cntsel USB HOST0 ohci_cntsel bit control
10	RW	0x1	host0_ohci_clkcktrst USB HOST0 ohci_clkcktrst bit control
9	RW	0x0	host0_app_prt_ovrcur USB HOST0 app_prt_ovrcur bit control
8	RW	0x0	host0_autoppd_on_overcur_en USB HOST0 autoppd_on_overcur_en bit control
7	RW	0x1	host0_word_if USB HOST0 word_if bit control
6	RW	0x0	host0_sim_mode USB HOST0 sim_mode bit control 1'b0: Disable 1'b1: Enable
5	RW	0x1	host0_incrx_en USB HOST0 incrx_en bit control 1'b0: Disable 1'b1: Enable
4	RW	0x1	host0_incr8_en USB HOST0 incr8_en bit control 1'b0: Disable 1'b1: Enable
3	RW	0x1	host0_incr4_en USB HOST0 incr4_en bit control 1'b0: Disable 1'b1: Enable
2	RW	0x1	host0_incr16_en USB HOST0 incr16_en bit control 1'b0: Disable 1'b1: Enable
1	RW	0x0	host0_hubsetup_min USB HOST0 bubsetup_min bit control
0	RW	0x0	host0_app_start_clk USB HOST0 app_start_clk bit control

GRF_PERI_HOST_STATUS

Address: Operational Base(0xFF040000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
30	RO	0x0	host0_ehci_power_state_ack host0_ehci_power_state_ack bit status
29	RO	0x0	host0_ehci_pme_status host0_ehci_pme_status bit status
28	RO	0x0	host0_ehci_bufacc host0_ehci_bufacc bit status
27	RO	0x0	host0_ehci_xfer_prdc host0_ehci_xfer_prdc bit status
26	RO	0x0	host0_ohci_ccs host0_ohci_ccs bit status
25	RO	0x0	host0_ohci_rwe host0_ohci_rwe bit status
24	RO	0x0	host0_ohci_drwe host0_ohci_drwe bit status
23	RO	0x0	host0_ohci_globalsuspend host0_ohci_globalsuspend bit status
22	RO	0x0	host0_ohci_bufacc host0_ohci_bufacc bit status
21	RO	0x0	host0_ohci_rmtwkp host0_ohci_rmtwkp bit status
20:17	RO	0x0	host0_ehci_lpsmc_state host0_ehci_lpsmc_state bit status
16:11	RO	0x00	host0_ehci_usbsts host0_ehci_usbsts bit status
10:0	RW	0x000	host0_ehci_xfer_cnt host0_ehci_xfer_cnt bit status

GRF_PERI_USB3OTG_CON0

Address: Operational Base(0xFF040000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	usb3otg0_host_u2_port_disable USB2.0 Port Disable control. 1'b0: Port Enabled 1'b1: Port Disabled When 1, this signal stops reporting connect/disconnect events the port and keeps the port in disabled state
14	RW	0x0	usb3otg0_host_port_power_control_present This indicates whether the host controller implementation includes port power control. 1'b0: Indicates that the port does not have port power switches. 1'b1: Indicates that the port has port power switches
13:8	RW	0x20	usb3otg0_fladj_30mhz_reg usb3otg_fladj_30mhz_reg bit control
7:6	RW	0x0	usb3otg0_hub_port_perm_attach Indicates if the device attached to a downstream port is permanently attached or not. 1'b0: Not permanently attached 1'b1: Permanently attached Bit0 is for USB2.0 port and bit1 are for USB 3.0 SS port

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Bit	Attr	Reset Value	Description
5:4	RW	0x0	usb3otg0_hub_port_overcurrent This is the per port Overcurrent indication of the root-hub ports: 1'b0: No Overcurrent 1'b1: Overcurrent Bit0 is for USB 2.0 port and bit1 are for USB 3.0 SS port
3:0	RW	0x0	usb3otg0_bus_filter_bypass It is expected that this signal is set or reset at power-on reset and is not changed during the normal operation of the core. The function of each bit is: bus_filter_bypass[3]: Bypass the filter for utmiotg_iddig bus_filter_bypass[2]: Bypass the filters for utmisrp_bvalid and utmisrp_sessend bus_filter_bypass[1]: Bypass the filter for pipe3_PowerPresent all U3 ports bus_filter_bypass[0]: Bypass the filter for utmiotg_vbusvalid all U2 ports In non-OTG Host-only mode, internal bus filters are not needed. Values: 1'b0: Bus filter(s) enabled 1'b1: Bus filter(s) disabled (bypassed)

GRF_PERI_USB3OTG_CON1

Address: Operational Base(0xFF040000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x1	usb3otg0_host_num_u3_port xHCI usb3 port number, default as 1
11:8	RW	0x1	usb3otg0_host_num_u2_port xHCI host USB2 Port number, default as 1
7	RW	0x0	usb3otg0_pipe_clk_sel usb3otg0_pipe3_rx_pclk/tx_pclk input source clk select 1'b0: select clk_usb3otg0_pipe for source clk 1'b0: select clk_usb3otg0_utmi for source clk
6	RO	0x0	reserved
5	RW	0x0	usb3otg0_host_legacy_smi_bar Use this register to support SMI on BAR defined in xHCI spec. SW must set this register, then clear this register to indicate Base Address Register written
4	RW	0x0	usb3otg0_host_legacy_smi_pci_cmd Use this register to support SMI on PCI Command defined in xHCI spec. SW must set this register, then clear this register to indicate PCI command register written
3:2	RW	0x0	usb3otg0_pipe_rate 2'b00: Use 5.0GT/s signaling rate 2'b01: Not allowed 2'b10: Not allowed 2'b11: Not allowed
1	RW	0x0	usb3otg0_pme_en Enable signal for the pme_generation. Enable the core to assert pme_generation

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Bit	Attr	Reset Value	Description
0	RW	0x0	usb3otg0_host_u3_port_disable USB 3.0 SS Port Disable control. 1'b0: Port Enabled 1'b1: Port Disabled

GRF_PERI_USB3OTG_CON2

Address: Operational Base(0xFF040000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	usb3otg0_pme_generation_irq_en usb3otg0_pme_generation_irq_en 1'b0: irq disable 1'b1: irq enableable
0	RW	0x0	usb3otg0_host_sys_err_irq_en usb3otg0_host_sys_err_irq_en 1'b0: irq disable 1'b1: irq enableable

GRF_PERI_USB3OTG_STATUS_LAT0

Address: Operational Base(0xFF040000) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	usb3otg_logic_analyzer_trace0 usb3otg_logic_analyzer_trace[31:0] bit status

GRF_PERI_USB3OTG_STATUS_LAT1

Address: Operational Base(0xFF040000) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	usb3otg_logic_analyzer_trace1 usb3otg_logic_analyzer_trace[63:32] bit status

GRF_PERI_USB3OTG_STATUS_CB

Address: Operational Base(0xFF040000) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x7e8	usb3otg_host_current_belt[11:0] usb3otg_host_current_belt[11:0] bit status

GRF_PERI_USB3OTG_STATUS

Address: Operational Base(0xFF040000) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	usb3otg0_pme_generation Used to generate the pme.
0	RO	0x0	usb3otg0_host_sys_err usb3otg0 host system error status

GRF_PERI_SARADC0_CON

Address: Operational Base(0xFF040000) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15:0	RW	0x0007	saradc_ana_reg Reserved

5.6 DDR_GRF Register Description

5.6.1 Registers Summary

Name	Offset	Size	Reset Value	Description
GRF_DDR_GRF_DDR_CON0	0x0000	W	0x00000000	DDR Control Register0
GRF_DDR_GRF_DDR_CON1	0x0004	W	0x00000600	DDR Control Register1
GRF_DDR_GRF_DDR_CON2	0x0008	W	0x00000000	DDR Control Register2
GRF_DDR_GRF_DDR_CON3	0x000C	W	0x0000E400	DDR Control Register3
GRF_DDR_SPLIT_CON	0x0010	W	0x00000110	DDR AXI SPLIT Control Register
GRF_DDR_PROB_CTRL	0x0014	W	0x00000000	
GRF_DDR_LP_CON	0x0020	W	0x00001101	DDR PHY Lower Power Control Register
GRF_DDR_STATUS0	0x0100	W	0x00000000	DDR Status Register0
GRF_DDR_STATUS1	0x0104	W	0x00000000	DDR Status Register1
GRF_DDR_STATUS2	0x0108	W	0x00000000	DDR Status Register2
GRF_DDR_STATUS3	0x010C	W	0x00000000	DDR Status Register3
GRF_DDR_STATUS4	0x0110	W	0x00000000	DDR Status Register4
GRF_DDR_STATUS5	0x0114	W	0x00000000	DDR Status Register5
GRF_DDR_STATUS6	0x0118	W	0x00000000	DDR Status Register6
GRF_DDR_STATUS7	0x011C	W	0x00000000	DDR Status Register7
GRF_DDR_STATUS8	0x0120	W	0x00000000	DDR Status Register8
GRF_DDR_STATUS9	0x0124	W	0x00000000	DDR Status Register9
GRF_DDR_STATUS10	0x0128	W	0x00000000	DDR Status Register10
GRF_DDR_STATUS11	0x012C	W	0x00000000	DDR Status Register11
GRF_DDR_STATUS12	0x0130	W	0x00000000	DDR Status Register12
GRF_DDR_STATUS13	0x0134	W	0x00000000	DDR Status Register13
GRF_DDR_STATUS14	0x0138	W	0x00000000	DDR Status Register14
GRF_DDR_STATUS15	0x013C	W	0x00000000	DDR Status Register15
GRF_DDR_STATUS16	0x0140	W	0x00000000	DDR Status Register16
GRF_DDR_STATUS17	0x0144	W	0x00000000	DDR Status Register17
GRF_DDR_STATUS18	0x0148	W	0x00000000	DDR Status Register18
GRF_DDR_SCRAMBLE_STATUS	0x0150	W	0x00000000	DDR Scramble Status Register

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.6.2 Detail Registers Description

GRF_DDR_GRF_DDR_CON0

Address: Operational Base(0xFF050000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14	RW	0x0	awpoison AXI write poison control
13	RW	0x0	awurgen AXI write urgent control
12	RW	0x0	arpoison AXI read poison control
11	RW	0x0	arurgent AXI bus read urgent control
10	RW	0x0	pa_wmask When asserted(active high), it will prevent the corresponding write to PA
9:8	RW	0x0	pa_rmask When asserted(active high), it will prevent the corresponding read to PA
7	RW	0x0	axisplit_4g_sel axi split only support one rank, and address space max=4G. 1'b0: ddr low 4g space; 1'b1: ddr high 4g space.
6	RW	0x0	msch_cgen msch mem clock gating enable 1'b0: clock auto gating valid; 1'b1: clock always exist.
5	RW	0x0	csysreq_upctl_hwlp csysreq from hwlp mask bit. 1'b0: hwlp csysreq invalid; 1'b1: hwlp csysreq valid.
4	RW	0x0	csysreq_upctl_pmu csysreq from pmu mask bit. 1'b0: pmu csysreq invalid; 1'b1: pmu csysreq valid.
3	RW	0x0	csysreq_aclk when hwlp_cysreq_0_en(grf_ddr_reg08[4])=1'b0, this bit map to upctl_csysreq_0. 1'b0: request upctl aclk enter low power 1'b1: request upctl aclk exit low power
2	RW	0x0	dfi_init_start grf_ddr_dfi_init_start, when dfi_init_start_sel(grf_ddr_reg00[1])=1'b1, this bit map to the ddrphy input dfi_init_start. 1'b0: ddrphy into low power mode(when dfi_init_start_sel=1'b1); 1'b1: ddrphy initial start or ddrphy exit low powe mode(when dfi_init_start_sel=1'b1).
1	RW	0x0	dfi_init_start_sel dfi initial start select. 1'b0: dfi init start from dfi_ctrl or upctl or hwlp; 1'b1: dfi init start from grf_ddr_reg00[2].
0	RW	0x0	upctl_slverr_enable upctl apb interface slave error response enable. 1'b0: disable; 1'b1: enable

GRF_DDR_GRF_DDR_CON1

Address: Operational Base(0xFF050000) + offset (0x0004)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:8	RW	0x6	auto_sr_dly The delay of auto gated ddrc_core_clk. It should be to be 0x6
7	RW	0x0	arautopre axi read auto precharge control
6	RW	0x0	awautopre axi write auto precharge control
5	RO	0x0	reserved
4	RW	0x0	upctl2_syscreq_cg_en 1'b0: Disable force ddrc_core_clk ungating when external ddrc_csysreq asserted 1'b1: Enable force ddrc_core ungating when external ddrc_csysreq asserted
3	RW	0x0	selfref_type2_en 1'b0: Disable ddrc_core_clk auto gating in type2 selfrefresh 1'b1: Enable ddrc_core_clk auto gating in type2 selfrefresh
2	RW	0x0	upctl_core_cg_en 1'b0: Disable ddrc_core_clk auto gating 1'b1: Enable ddrc_core_clk auto gating
1	RW	0x0	upctl_apb_cg_en 1'b0: Disable function of force aclk/ddrc_core_clk ungated when apb access is going 1'b1: Enable function of force aclk/ddrc_core_clk ungated when apb access is going
0	RW	0x0	upctl_axi_cg_en 1'b0: Disable aclk auto gating 1'b1: Enable aclk auto gating

GRF_DDR_GRF_DDR_CON2

Address: Operational Base(0xFF050000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9:0	RW	0x000	ddr_clk_gate each bit is dedicated for a subblock auto gating function inside ddr control 1'b0 enable auto gating 1'b1 disable auto gating

GRF_DDR_GRF_DDR_CON3

Address: Operational Base(0xFF050000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:14	RW	0x3	dq_swap_sel3 select which dfi dq byte is used for dq byte 0 in IO 2'b00 dfi dq byte 0 is used for byte3 2'b01 dfi dq byte 1 is used for byte3 2'b10 dfi dq byte 2 is used for byte3 2'b11 dfi dq byte 3 is used for byte3
13:12	RW	0x2	dq_swap_sel2 select which dfi dq byte is used for dq byte 0 in IO 2'b00 dfi dq byte 0 is used for byte2 2'b01 dfi dq byte 1 is used for byte2 2'b10 dfi dq byte 2 is used for byte2 2'b11 dfi dq byte 3 is used for byte2
11:10	RW	0x1	dq_swap_sel1 select which dfi dq byte is used for dq byte 0 in IO 2'b00 dfi dq byte 0 is used for byte1 2'b01 dfi dq byte 1 is used for byte1 2'b10 dfi dq byte 2 is used for byte1 2'b11 dfi dq byte 3 is used for byte1
9:8	RW	0x0	dq_swap_sel0 select which dfi dq byte is used for dq byte 0 in IO 2'b00 dfi dq byte 0 is used for byte0 2'b01 dfi dq byte 1 is used for byte0 2'b10 dfi dq byte 2 is used for byte0 2'b11 dfi dq byte 3 is used for byte0
7	RW	0x0	dq_swap_en ddr dfi dq swap enable 1'b1 enable 1'b0 disalbe
6	RW	0x0	dfi_init_complete grf dfi_init_complet. 1'b0: ddrphy not ready; 1'b1: ddrphy ready.
5	RW	0x0	dfi_init_complete_sel 1'b0: ddrphy controls upctl dfi_init_complete; 1'b1: grf dfi_init_complet controls upctl dfi_init_complete.
4	RW	0x0	hwlp_csysreq_0_en 1'b0: grf csysreq_aclk(grf_ddr_reg00[3]) controls upctl_csysreq_0; 1'b1: csysreq_0_hwlp controls upctl_csysreq_0
3:0	RO	0x0	reserved

GRF_DDR_SPLIT_CON

Address: Operational Base(0xFF050000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
10:9	RW	0x0	split_mode Split mode select. 2'b00:DDR controller and phy works at 32 bits mode. Low 16 bits are valid if access address is above split address. 2'b01:DDR controller and phy works at 32 bits mode. High 16 bits are valid if access address is above split address. 2'b10:DDR controller and phy works at 16 bits mode. Low 8 bits are valid if access address is above split address. 2'b11:DDR controller and phy works at 16 bits mode. High 8 bits are valid if access address is above split address
8	RW	0x1	bypass 1'b0: Enable axi split 1'b1: Bypass axi split
7:0	RW	0x10	spaddr Split address high 8 bits of 32bit address. For example, if SPADDR=0x10, then the split address is 0x10000000. The axi_split module will be bypassed if reading or writing DDR below split address, otherwise axi burst will be split.

GRF_DDR_PROB_CTRL

Address: Operational Base(0xFF050000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	vio_port_probe_stat_suspend suspend ctrl 1'b0: no suspend 1'b1: ctrl by ddrmon
3	RW	0x0	npu_port_probe_stat_suspend suspend ctrl 1'b0: no suspend 1'b1: ctrl by ddrmon
2	RW	0x0	gpu_port_probe_stat_suspend suspend ctrl 1'b0: no suspend 1'b1: ctrl by ddrmon
1	RW	0x0	cpu_port_probe_stat_suspend suspend ctrl 1'b0: no suspend 1'b1: ctrl by ddrmon
0	RW	0x0	bus_port_probe_stat_suspend suspend ctrl 1'b0: no suspend 1'b1: ctrl by ddrmon

GRF_DDR_LP_CON

Address: Operational Base(0xFF050000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	sr_ctl_en 1'b0: Disable sr exit/enter reload/inverse lpckdis_ini 1'b1: Enable sr exit/eneter reload/inverse lpckdis_ini

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Bit	Attr	Reset Value	Description
12	RW	0x1	pd_ctl_en 1'b0: Disable pd exit/enter reload/inverse lpckdis_ini 1'b1: Enable pd exit/eneter reload/inverse lpckdis_ini
11:10	RO	0x0	reserved
9	RW	0x0	lpckdis_en 1'b0: Disable ddr phy low power fuction 1'b1: Enable ddr phy low power function
8	RW	0x1	lpckdis_ini lpckdis intial value
7:3	RO	0x00	reserved
2	RW	0x0	lp23_mode 1'b0: Disable LPDDR2/LPDDR3 mode 1'b1: Enable LPDDR2/LPDDR3 mode
1	RW	0x0	ddr4_mode 1'b0: Disable DDR4 mode 1'b1: Enable DDR4 mode
0	RW	0x1	ddr23_mode 1'b0: Disable DDR2/DDR3 mode 1'b1: Enable DDR2/DDR3 mode

GRF_DDR_STATUS0

Address: Operational Base(0xFF050000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mrr_data0[31:0] DDR_STATUS0~DDR_STATUS7 are Mode Register Read Data. mrr_data0[31:0] data status.

GRF_DDR_STATUS1

Address: Operational Base(0xFF050000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mrr_data0[63:32] mrr_data0[63:32] data status. See DDR_STATUS0

GRF_DDR_STATUS2

Address: Operational Base(0xFF050000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mrr_data0[95:64] mrr_data0[95:64] data status. See DDR_STATUS0

GRF_DDR_STATUS3

Address: Operational Base(0xFF050000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mrr_data0[127:96] mrr_data0[127:96] data status. See DDR_STATUS0

GRF_DDR_STATUS4

Address: Operational Base(0xFF050000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mrr_data1[31:0] mrr_data1[31:0] data status. See DDR_STATUS0

GRF_DDR_STATUS5

Address: Operational Base(0xFF050000) + offset (0x0114)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mrr_data1[63:32] mrr_data1[63:32] data status. See DDR_STATUS0

GRF_DDR_STATUS6

Address: Operational Base(0xFF050000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mrr_data1[95:64] mrr_data1[95:64] data status. See DDR_STATUS0

GRF_DDR_STATUS7

Address: Operational Base(0xFF050000) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mrr_data1[127:96] mrr_data1[127:96] data status. See DDR_STATUS0

GRF_DDR_STATUS8

Address: Operational Base(0xFF050000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RO	0x0	link_msch_fifo_empty link msch obsrv main Fifo empty.
25	RO	0x0	link_msch_fifo_full link msch obsrv main Fifo full.
24:22	RO	0x0	reserved
21	RO	0x0	cpu_mainStatAlarm cpu port probe main stat alarm.
20	RO	0x0	cpu_mainTraceAlarm cpu port probe main trace alarm.
19	RO	0x0	bus_mainStatAlarm bus port probe main stat alarm.
18	RO	0x0	npu_mainStatAlarm npu port probe main stat alarm.
17	RO	0x0	npu_mainTraceAlarm npu port probe main trace alarm.
16	RO	0x0	bus_mainTraceAlarm gpu port probe main trace alarm.
15	RO	0x0	gpu_mainStatAlarm gpu port probe main stat alarm.
14	RO	0x0	gpu_mainTraceAlarm gpu port probe main trace alarm.
13	RO	0x0	vio_mainStatAlarm vio port probe main stat alarm.
12	RO	0x0	vio_mainTraceAlarm vio port probe main trace alarm.
11	RO	0x0	ddr_apb_pwr_idleack ddr apb pwr idle ack.
10	RO	0x0	ddr_apb_pwr_idle ddr apb pwr idle status.
9	RO	0x0	msch_pwr_idleack msch pwr idle ack.
8	RO	0x0	msch_pwr_idle msch pwr idle status.
7:6	RO	0x0	ddrc_reg_selfref_type The status of ddrc_reg_selfref_type

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Bit	Attr	Reset Value	Description
5	RO	0x0	cactive_aclk The status of cactive_aclk
4	RO	0x0	csysack_aclk The status of csysack_aclk
3	RO	0x0	con_csysreq_aclk The status of csysreq_aclk
2	RO	0x0	cactive_ddrc The status of external cactive_ddrc
1	RO	0x0	csysack_ddrc The status of external csysack_ddrc
0	RO	0x0	csysreq_ddrc The status of external csysreq_ddrc

GRF_DDR_STATUS9

Address: Operational Base(0xFF050000) + offset (0x0124)

Bit	Attr	Reset Value	Description
31	RO	0x0	dfi_lp_ck_disable The status of low power of ddr phy
30	RO	0x0	ddr_cmd_plllock ddr phy pll lock
29:23	RO	0x00	reserved
22:16	RO	0x00	wr_credit_cnt Indicates the number of available write CAM slots (free positions). Each slots holds a DRAM burst. Value is decremented/incremented as the commands flow in out of the write CAM.
15	RO	0x0	reserved
14:8	RO	0x00	hpr_credit_cnt Indicates the number of available High priority read CAM slots (free positions). Each slots holds a DRAM burst (Channel 1). Value is decremented/incremented as the commands flow in out of the read CAM (HPR store).
7	RO	0x0	reserved
6:0	RO	0x00	lpr_credit_cnt Indicates the number of available Low priority read CAM slots (free positions). Each slots holds a DRAM burst (Channel 1). Value is decremented/incremented as the commands flow in out of the read CAM (LPR store).

GRF_DDR_STATUS10

Address: Operational Base(0xFF050000) + offset (0x0128)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mrr_data2[31:0] mrr_data2[31:0] data status. See DDR_STATUS0

GRF_DDR_STATUS11

Address: Operational Base(0xFF050000) + offset (0x012C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mrr_data2[63:32] mrr_data2[63:32] data status. See DDR_STATUS0

GRF_DDR_STATUS12

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Address: Operational Base(0xFF050000) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mrr_data2[95:64] mrr_data2[95:64] data status. See DDR_STATUS0

GRF_DDR_STATUS13

Address: Operational Base(0xFF050000) + offset (0x0134)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mrr_data2[127:96] mrr_data2[127:96] data status. See DDR_STATUS0

GRF_DDR_STATUS14

Address: Operational Base(0xFF050000) + offset (0x0138)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mrr_data3[31:0] mrr_data3[31:0] data status. See DDR_STATUS0

GRF_DDR_STATUS15

Address: Operational Base(0xFF050000) + offset (0x013C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mrr_data3[63:32] mrr_data3[63:32] data status. See DDR_STATUS0

GRF_DDR_STATUS16

Address: Operational Base(0xFF050000) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mrr_data3[95:64] mrr_data3[95:64] data status. See DDR_STATUS0

GRF_DDR_STATUS17

Address: Operational Base(0xFF050000) + offset (0x0144)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mrr_data3[127:96] mrr_data3[127:96] data status. See DDR_STATUS0

GRF_DDR_STATUS18

Address: Operational Base(0xFF050000) + offset (0x0148)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	hit_refresh_req_bank hif refresh req bank status.
19:0	RO	0x00000	reserved

GRF_DDR_SCRAMBLE_STATUS

Address: Operational Base(0xFF050000) + offset (0x0150)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	scramble_idle 1'b0: scrambe busy; 1'b1: scrambe idle.

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5.7 GPIO1_IOC Register Description

5.7.1 Registers Summary

Name	Offset	Size	Reset Value	Description
GPIO1_IOC_GPIO1A_IOMUX_SEL_L	0x0000	W	0x00000000	GPIO1A IOMUX control low bits
GPIO1_IOC_GPIO1A_IOMUX_SEL_H	0x0004	W	0x00000000	GPIO1A IOMUX control high bits
GPIO1_IOC_GPIO1B_IOMUX_SEL_L	0x0008	W	0x00000000	GPIO1B IOMUX control low bits
GPIO1_IOC_GPIO1B_IOMUX_SEL_H	0x000C	W	0x00000220	GPIO1B IOMUX control high bits
GPIO1_IOC_GPIO1C_IOMUX_SEL_L	0x0010	W	0x00000000	GPIO1C IOMUX control low bits
GPIO1_IOC_GPIO1C_IOMUX_SEL_H	0x0014	W	0x00000000	GPIO1C IOMUX control high bits
GPIO1_IOC_GPIO1D_IOMUX_SEL_L	0x0018	W	0x00000000	GPIO1D IOMUX control low bits
GPIO1_IOC_GPIO1D_IOMUX_SEL_H	0x001C	W	0x00000000	GPIO1D IOMUX control high bits
GPIO1_IOC_GPIO1A_P	0x0080	W	0x00005555	GPIO1A PU/PD control
GPIO1_IOC_GPIO1B_P	0x0084	W	0x00005569	GPIO1B PU/PD control
GPIO1_IOC_GPIO1C_P	0x0088	W	0x0000AAAA	GPIO1C PU/PD control
GPIO1_IOC_GPIO1D_P	0x008C	W	0x0000AAAA	GPIO1D PU/PD control
GPIO1_IOC_GPIO1A_IE	0x00C0	W	0x00005555	GPIO1A PAD input enable control
GPIO1_IOC_GPIO1B_IE	0x00C4	W	0x00005555	GPIO1B PAD input enable control
GPIO1_IOC_GPIO1C_IE	0x00C8	W	0x00005555	GPIO1C PAD input enable control
GPIO1_IOC_GPIO1D_IE	0x00CC	W	0x00005555	GPIO1D PAD input enable control
GPIO1_IOC_GPIO1A_OD	0x0100	W	0x00000000	GPIO1A PAD open drain functionality enable
GPIO1_IOC_GPIO1B_OD	0x0104	W	0x00000000	GPIO1B PAD open drain functionality enable
GPIO1_IOC_GPIO1C_OD	0x0108	W	0x00000000	GPIO1C PAD open drain functionality enable
GPIO1_IOC_GPIO1D_OD	0x010C	W	0x00000000	GPIO1D PAD open drain functionality enable
GPIO1_IOC_GPIO1A_SUS	0x0140	W	0x00000000	GPIO1A PAD weak Pull Keeper enable
GPIO1_IOC_GPIO1B_SUS	0x0144	W	0x00000000	GPIO1B PAD weak Pull Keeper enable
GPIO1_IOC_GPIO1C_SUS	0x0148	W	0x00000000	GPIO1C PAD weak Pull Keeper enable
GPIO1_IOC_GPIO1D_SUS	0x014C	W	0x00000000	GPIO1D PAD weak Pull Keeper enable
GPIO1_IOC_GPIO1A_SL	0x0180	W	0x0000FFFF	Slew Rate Control for the driver secton while driving PAD.
GPIO1_IOC_GPIO1B_SL	0x0184	W	0x0000FFFF	Slew Rate Control for the driver secton while driving PAD.
GPIO1_IOC_GPIO1C_SL	0x0188	W	0x0000FFFF	Slew Rate Control for the driver secton while driving PAD.
GPIO1_IOC_GPIO1D_SL	0x018C	W	0x0000FFFF	Slew Rate Control for the driver secton while driving PAD.
GPIO1_IOC_GPIO1A_DS0	0x0200	W	0x00000707	GPIO1A driver strength control
GPIO1_IOC_GPIO1A_DS1	0x0204	W	0x00000707	GPIO1A driver strength control

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Name	Offset	Size	Reset Value	Description
GPIO1_IOC_GPIO1A_DS2	0x0208	W	0x00000707	GPIO1A driver strength control
GPIO1_IOC_GPIO1A_DS3	0x020C	W	0x00000707	GPIO1A driver strength control
GPIO1_IOC_GPIO1B_DS0	0x0210	W	0x00000F07	GPIO1B driver strength control
GPIO1_IOC_GPIO1B_DS1	0x0214	W	0x00000707	GPIO1B driver strength control
GPIO1_IOC_GPIO1B_DS2	0x0218	W	0x00000707	GPIO1B driver strength control
GPIO1_IOC_GPIO1B_DS3	0x021C	W	0x00000707	GPIO1B driver strength control
GPIO1_IOC_GPIO1C_DS0	0x0220	W	0x0000070F	GPIO1C driver strength control
GPIO1_IOC_GPIO1C_DS1	0x0224	W	0x00000707	GPIO1C driver strength control
GPIO1_IOC_GPIO1C_DS2	0x0228	W	0x00000707	GPIO1C driver strength control
GPIO1_IOC_GPIO1C_DS3	0x022C	W	0x0000070F	GPIO1C driver strength control
GPIO1_IOC_GPIO1D_DS0	0x0230	W	0x00000707	GPIO1D driver strength control
GPIO1_IOC_GPIO1D_DS1	0x0234	W	0x00000707	GPIO1D driver strength control
GPIO1_IOC_GPIO1D_DS2	0x0238	W	0x00000707	GPIO1D driver strength control
GPIO1_IOC_GPIO1D_DS3	0x023C	W	0x00000707	GPIO1D driver strength control

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.7.2 Detail Registers Description

GPIO1_IOC_GPIO1A_IOMUX_SEL_L

Address: Operational Base(0xFF060000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio1a3_sel 3'h0: GPIO1_A3 3'h1: EMMC_D3 3'h2: FSPI_D3
11	RO	0x0	reserved
10:8	RW	0x0	gpio1a2_sel 3'h0: GPIO1_A2 3'h1: EMMC_D2 3'h2: FSPI_D2
7	RO	0x0	reserved
6:4	RW	0x0	gpio1a1_sel 3'h0: GPIO1_A1 3'h1: EMMC_D1 3'h2: FSPI_D1
3	RO	0x0	reserved
2:0	RW	0x0	gpio1a0_sel 3'h0: GPIO1_A0 3'h1: EMMC_D0 3'h2: FSPI_D0

GPIO1_IOC_GPIO1A_IOMUX_SEL_H

Address: Operational Base(0xFF060000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14:12	RW	0x0	gpio1a7_sel 3'h0: GPIO1_A7 3'h1: EMMC_D7
11	RO	0x0	reserved
10:8	RW	0x0	gpio1a6_sel 3'h0: GPIO1_A6 3'h1: EMMC_D6
7	RO	0x0	reserved
6:4	RW	0x0	gpio1a5_sel 3'h0: GPIO1_A5 3'h1: EMMC_D5
3	RO	0x0	reserved
2:0	RW	0x0	gpio1a4_sel 3'h0: GPIO1_A4 3'h1: EMMC_D4

GPIO1_IOC_GPIO1B_IOMUX_SEL_L

Address: Operational Base(0xFF060000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio1b3_sel 3'h0: GPIO1_B3 3'h1: SDMMC0_D0 3'h2: UART0_RX_M1 3'h3: UART7_RX_M1 3'h4: SPI1_MOSI_M1 3'h5: DSM_AUD_LP
11	RO	0x0	reserved
10:8	RW	0x0	gpio1b2_sel 3'h0: GPIO1_B2 3'h1: EMMC_STRB 3'h2: FSPI_CSN1
7	RO	0x0	reserved
6:4	RW	0x0	gpio1b1_sel 3'h0: GPIO1_B1 3'h1: EMMC_CLK 3'h2: FSPI_CLK
3	RO	0x0	reserved
2:0	RW	0x0	gpio1b0_sel 3'h0: GPIO1_B0 3'h1: EMMC_CMD 3'h2: FSPI_CSN0

GPIO1_IOC_GPIO1B_IOMUX_SEL_H

Address: Operational Base(0xFF060000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14:12	RW	0x0	gpio1b7_sel 3'h0: GPIO1_B7 3'h1: SDMMC0_CMD 3'h2: SPDIF_TX_M2 3'h3: UART5_RX_M0 3'h4: CAN1_RX_M0
11	RO	0x0	reserved
10:8	RW	0x2	gpio1b6_sel 3'h0: GPIO1_B6 3'h1: SDMMC0_D3 3'h2: JTAG_CPU_MCU_TMS_M1 3'h3: UART5_RTSN_M0 3'h4: SPI1_CSN0_M1 3'h5: PWM11_M0 3'h6: DSM_AUD_RN
7	RO	0x0	reserved
6:4	RW	0x2	gpio1b5_sel 3'h0: GPIO1_B5 3'h1: SDMMC0_D2 3'h2: JTAG_CPU_MCU_TCK_M1 3'h3: UART5_CTSN_M0 3'h4: SPI1_CSN1_M1 3'h5: PWM10_M0 3'h6: DSM_AUD_RP
3	RO	0x0	reserved
2:0	RW	0x0	gpio1b4_sel 3'h0: GPIO1_B4 3'h1: SDMMC0_D1 3'h2: UART0_TX_M1 3'h3: UART7_TX_M1 3'h4: SPI1_MISO_M1 3'h5: DSM_AUD_LN

GPIO1_IOC_GPIO1C_IOMUX_SEL_L

Address: Operational Base(0xFF060000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio1c3_sel 3'h0: GPIO1_C3 3'h1: SDMMC1_D2 3'h2: RGMII_TXCLK_M1 3'h3: I2S0_SDO0_M1 3'h4: PWM10_M1
11	RO	0x0	reserved
10:8	RW	0x0	gpio1c2_sel 3'h0: GPIO1_C2 3'h1: SDMMC1_D1 3'h2: RGMII_TXD3_M1 3'h3: I2S0_SDI1_M1 3'h4: PWM9_M1
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:4	RW	0x0	gpio1c1_sel 3'h0: GPIO1_C1 3'h1: SDMMC1_D0 3'h2: RGMII_TXD2_M1 3'h3: I2S0_SDI0_M1 3'h4: PWM8_M1
3	RO	0x0	reserved
2:0	RW	0x0	gpio1c0_sel 3'h0: GPIO1_C0 3'h1: SDMMC0_CLK 3'h2: TEST_CLK_OUT 3'h3: UART5_TX_M0 3'h4: SPI1_CLK_M1 3'h5: CAN1_TX_M0

GPIO1_IOC_GPIO1C_IOMUX_SEL_H

Address: Operational Base(0xFF060000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio1c7_sel 3'h0: GPIO1_C7 3'h1: SDMMC1_PWREN 3'h2: RGMII_MDC_M1 3'h3: PWM2_M1 3'h4: I2C5_SCL_M1 3'h5: RMII_MDC
11	RO	0x0	reserved
10:8	RW	0x0	gpio1c6_sel 3'h0: GPIO1_C6 3'h1: SDMMC1_CLK 3'h2: RGMII_RXCLK_M1 3'h3: I2S0_MCLK_M1 3'h4: PWM1_M1
7	RO	0x0	reserved
6:4	RW	0x0	gpio1c5_sel 3'h0: GPIO1_C5 3'h1: SDMMC1_CMD 3'h2: RGMII_RXD3_M1 3'h3: I2S0_SCLK_M1 3'h4: PWM0_M1
3	RO	0x0	reserved
2:0	RW	0x0	gpio1c4_sel 3'h0: GPIO1_C4 3'h1: SDMMC1_D3 3'h2: RGMII_RXD2_M1 3'h3: I2S0_LRCK_M1 3'h4: PWM11_M1

GPIO1_IOC_GPIO1D_IOMUX_SEL_L

Address: Operational Base(0xFF060000) + offset (0x0018)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio1d3_sel 3'h0: GPIO1_D3 3'h1: UART1_RTSN_M0 3'h2: RGMII_TXEN_M1 3'h3: I2S0_SDI2_M1 3'h4: PWM6_M1 3'h5: RMII_TXEN
11	RO	0x0	reserved
10:8	RW	0x0	gpio1d2_sel 3'h0: GPIO1_D2 3'h1: UART1_TX_M0 3'h2: RGMII_TXD1_M1 3'h3: I2S0_SDO2_M1 3'h4: PWM5_M1 3'h5: RMII_TXD1
7	RO	0x0	reserved
6:4	RW	0x0	gpio1d1_sel 3'h0: GPIO1_D1 3'h1: UART1_RX_M0 3'h2: RGMII_TXD0_M1 3'h3: I2S0_SDO1_M1 3'h4: PWM4_M1 3'h5: RMII_TXD0
3	RO	0x0	reserved
2:0	RW	0x0	gpio1d0_sel 3'h0: GPIO1_D0 3'h1: SDMMC1_DETN 3'h2: RGMII_MDIO_M1 3'h3: PWM3_M1 3'h4: I2C5_SDA_M1 3'h5: RMII_MDIO

GPIO1_IOC_GPIO1D_IOMUX_SEL_H

Address: Operational Base(0xFF060000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio1d7_sel 3'h0: GPIO1_D7 3'h1: I2S2_SDO_M0 3'h2: RGMII_RXD1_M1 3'h3: UART4_RTSN_M1 3'h4: SPI2_MOSI_M1 3'h5: PWM14_M1 3'h6: RMII_RXD1
11	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
10:8	RW	0x0	gpio1d6_sel 3'h0: GPIO1_D6 3'h1: I2S2_LRCK_M0 3'h2: RGMII_RXDV_M1 3'h3: UART4_TX_M1 3'h4: SPI2_CSN0_M1 3'h5: RMII_RXDV_CRS
7	RO	0x0	reserved
6:4	RW	0x0	gpio1d5_sel 3'h0: GPIO1_D5 3'h1: I2S2_SCLK_M0 3'h2: RGMII_CLK_M1 3'h3: UART4_RX_M1 3'h4: SPI2_CSN1_M1 3'h5: RMII_CLK
3	RO	0x0	reserved
2:0	RW	0x0	gpio1d4_sel 3'h0: GPIO1_D4 3'h1: UART1_CTSN_M0 3'h2: RGMII_RXD0_M1 3'h3: I2S0_SDI3_M1 3'h4: PWM7_M1 3'h5: RMII_RXD0

GPIO1_IOC_GPIO1A_P

Address: Operational Base(0xFF060000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	gpio1a7_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
13:12	RW	0x1	gpio1a6_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
11:10	RW	0x1	gpio1a5_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
9:8	RW	0x1	gpio1a4_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
7:6	RW	0x1	gpio1a3_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

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Bit	Attr	Reset Value	Description
5:4	RW	0x1	gpio1a2_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
3:2	RW	0x1	gpio1a1_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
1:0	RW	0x1	gpio1a0_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

GPIO1_IOC_GPIO1B_P

Address: Operational Base(0xFF060000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	gpio1b7_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
13:12	RW	0x1	gpio1b6_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
11:10	RW	0x1	gpio1b5_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
9:8	RW	0x1	gpio1b4_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
7:6	RW	0x1	gpio1b3_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
5:4	RW	0x2	gpio1b2_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

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Bit	Attr	Reset Value	Description
3:2	RW	0x2	gpio1b1_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
1:0	RW	0x1	gpio1b0_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

GPIO1_IOC_GPIO1C_P

Address: Operational Base(0xFF060000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	gpio1c7_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
13:12	RW	0x2	gpio1c6_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
11:10	RW	0x2	gpio1c5_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
9:8	RW	0x2	gpio1c4_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
7:6	RW	0x2	gpio1c3_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
5:4	RW	0x2	gpio1c2_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
3:2	RW	0x2	gpio1c1_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

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Bit	Attr	Reset Value	Description
1:0	RW	0x2	gpio1c0_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

GPIO1_IOC_GPIO1D_P

Address: Operational Base(0xFF060000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	gpio1d7_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
13:12	RW	0x2	gpio1d6_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
11:10	RW	0x2	gpio1d5_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
9:8	RW	0x2	gpio1d4_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
7:6	RW	0x2	gpio1d3_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
5:4	RW	0x2	gpio1d2_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
3:2	RW	0x2	gpio1d1_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
1:0	RW	0x2	gpio1d0_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

GPIO1_IOC_GPIO1A_IE

Address: Operational Base(0xFF060000) + offset (0x00C0)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	gpio1a7_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
13:12	RW	0x1	gpio1a6_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
11:10	RW	0x1	gpio1a5_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
9:8	RW	0x1	gpio1a4_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
7:6	RW	0x1	gpio1a3_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
5:4	RW	0x1	gpio1a2_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
3:2	RW	0x1	gpio1a1_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
1:0	RW	0x1	gpio1a0_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

GPIO1_IOC_GPIO1B_IE

Address: Operational Base(0xFF060000) + offset (0x00C4)

Rockchip Confidential

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	gpio1b7_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
13:12	RW	0x1	gpio1b6_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
11:10	RW	0x1	gpio1b5_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
9:8	RW	0x1	gpio1b4_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
7:6	RW	0x1	gpio1b3_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
5:4	RW	0x1	gpio1b2_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
3:2	RW	0x1	gpio1b1_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
1:0	RW	0x1	gpio1b0_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

GPIO1_IOC_GPIO1C_IE

Address: Operational Base(0xFF060000) + offset (0x00C8)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	gpio1c7_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
13:12	RW	0x1	gpio1c6_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
11:10	RW	0x1	gpio1c5_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
9:8	RW	0x1	gpio1c4_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
7:6	RW	0x1	gpio1c3_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
5:4	RW	0x1	gpio1c2_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
3:2	RW	0x1	gpio1c1_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
1:0	RW	0x1	gpio1c0_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

GPIO1_IOC_GPIO1D_IE

Address: Operational Base(0xFF060000) + offset (0x00CC)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	gpio1d7_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
13:12	RW	0x1	gpio1d6_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
11:10	RW	0x1	gpio1d5_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
9:8	RW	0x1	gpio1d4_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
7:6	RW	0x1	gpio1d3_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
5:4	RW	0x1	gpio1d2_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
3:2	RW	0x1	gpio1d1_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
1:0	RW	0x1	gpio1d0_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

GPIO1_IOC_GPIO1A_OD

Address: Operational Base(0xFF060000) + offset (0x0100)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio1a7_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio1a6_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio1a5_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio1a4_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio1a3_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio1a2_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio1a1_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio1a0_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

GPIO1_IOC_GPIO1B_OD

Address: Operational Base(0xFF060000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio1b7_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio1b6_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
5	RW	0x0	gpio1b5_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio1b4_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio1b3_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio1b2_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio1b1_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio1b0_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

GPIO1_IOC_GPIO1C_OD

Address: Operational Base(0xFF060000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio1c7_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio1c6_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio1c5_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio1c4_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio1c3_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
2	RW	0x0	gpio1c2_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio1c1_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio1c0_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

GPIO1_IOC_GPIO1D_OD

Address: Operational Base(0xFF060000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio1d7_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio1d6_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio1d5_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio1d4_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio1d3_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio1d2_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio1d1_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio1d0_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

GPIO1_IOC_GPIO1A_SUS

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Address: Operational Base(0xFF060000) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio1a7_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio1a6_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio1a5_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio1a4_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio1a3_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio1a2_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio1a1_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio1a0_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

GPIO1_IOC_GPIO1B_SUS

Address: Operational Base(0xFF060000) + offset (0x0144)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio1b7_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio1b6_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
5	RW	0x0	gpio1b5_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio1b4_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio1b3_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio1b2_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio1b1_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio1b0_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

GPIO1_IOC_GPIO1C_SUS

Address: Operational Base(0xFF060000) + offset (0x0148)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio1c7_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio1c6_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio1c5_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio1c4_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio1c3_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
2	RW	0x0	gpio1c2_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio1c1_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio1c0_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

GPIO1_IOC_GPIO1D_SUS

Address: Operational Base(0xFF060000) + offset (0x014C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio1d7_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio1d6_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio1d5_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio1d4_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio1d3_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio1d2_sus GPIO weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio1d1_sus GPIO weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio1d0_sus GPIO weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

GPIO1_IOC_GPIO1A_SL

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Address: Operational Base(0xFF060000) + offset (0x0180)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x3	gpio1a7_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
13:12	RW	0x3	gpio1a6_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
11:10	RW	0x3	gpio1a5_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
9:8	RW	0x3	gpio1a4_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
7:6	RW	0x3	gpio1a3_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
5:4	RW	0x3	gpio1a2_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
3:2	RW	0x3	gpio1a1_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
1:0	RW	0x3	gpio1a0_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

GPIO1_IOC_GPIO1B_SL

Address: Operational Base(0xFF060000) + offset (0x0184)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x3	gpio1b7_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
13:12	RW	0x3	gpio1b6_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
11:10	RW	0x3	gpio1b5_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
9:8	RW	0x3	gpio1b4_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
7:6	RW	0x3	gpio1b3_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
5:4	RW	0x3	gpio1b2_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
3:2	RW	0x3	gpio1b1_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
1:0	RW	0x3	gpio1b0_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

GPIO1_IOC_GPIO1C_SL

Address: Operational Base(0xFF060000) + offset (0x0188)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x3	gpio1c7_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
13:12	RW	0x3	gpio1c6_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
11:10	RW	0x3	gpio1c5_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
9:8	RW	0x3	gpio1c4_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
7:6	RW	0x3	gpio1c3_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
5:4	RW	0x3	gpio1c2_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
3:2	RW	0x3	gpio1c1_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
1:0	RW	0x3	gpio1c0_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

GPIO1_IOC_GPIO1D_SL

Address: Operational Base(0xFF060000) + offset (0x018C)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x3	gpio1d7_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
13:12	RW	0x3	gpio1d6_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
11:10	RW	0x3	gpio1d5_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
9:8	RW	0x3	gpio1d4_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
7:6	RW	0x3	gpio1d3_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
5:4	RW	0x3	gpio1d2_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
3:2	RW	0x3	gpio1d1_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
1:0	RW	0x3	gpio1d0_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

GPIO1_IOC_GPIO1A_DS0

Address: Operational Base(0xFF060000) + offset (0x0200)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio1a1_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio1a0_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO1_IOC_GPIO1A_DS1

Address: Operational Base(0xFF060000) + offset (0x0204)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio1a3_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio1a2_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

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GPIO1_IOC_GPIO1A_DS2

Address: Operational Base(0xFF060000) + offset (0x0208)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio1a5_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio1a4_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO1_IOC_GPIO1A_DS3

Address: Operational Base(0xFF060000) + offset (0x020C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio1a7_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x07	gpio1a6_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO1_IOC_GPIO1B_DS0

Address: Operational Base(0xFF060000) + offset (0x0210)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio1b1_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio1b0_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO1_IOC_GPIO1B_DS1

Address: Operational Base(0xFF060000) + offset (0x0214)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x07	gpio1b3_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio1b2_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO1_IOC_GPIO1B_DS2

Address: Operational Base(0xFF060000) + offset (0x0218)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio1b5_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio1b4_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO1_IOC_GPIO1B_DS3

Address: Operational Base(0xFF060000) + offset (0x021C)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio1b7_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio1b6_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO1_IOC_GPIO1C_DS0

Address: Operational Base(0xFF060000) + offset (0x0220)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio1c1_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio1c0_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

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GPIO1_IOC_GPIO1C_DS1

Address: Operational Base(0xFF060000) + offset (0x0224)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio1c3_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio1c2_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO1_IOC_GPIO1C_DS2

Address: Operational Base(0xFF060000) + offset (0x0228)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio1c5_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x07	gpio1c4_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO1_IOC_GPIO1C_DS3

Address: Operational Base(0xFF060000) + offset (0x022C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio1c7_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio1c6_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO1_IOC_GPIO1D_DS0

Address: Operational Base(0xFF060000) + offset (0x0230)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x07	gpio1d1_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio1d0_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO1_IOC_GPIO1D_DS1

Address: Operational Base(0xFF060000) + offset (0x0234)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio1d3_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio1d2_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO1_IOC_GPIO1D_DS2

Address: Operational Base(0xFF060000) + offset (0x0238)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio1d5_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio1d4_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO1_IOC_GPIO1D_DS3

Address: Operational Base(0xFF060000) + offset (0x023C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio1d7_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio1d6_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

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5.8 GPIO2_IOC Register Description

5.8.1 Registers Summary

Name	Offset	Size	Reset Value	Description
GPIO2_IOC_GPIO2A_IOMUX_SEL_L	0x0020	W	0x00000000	GPIO2A IOMUX control low bits
GPIO2_IOC_GPIO2A_P	0x0090	W	0x0000000A	GPIO2A PU/PD control
GPIO2_IOC_GPIO2A_IE	0x00D0	W	0x00000005	GPIO2A PAD input enable control
GPIO2_IOC_GPIO2A_OD	0x0110	W	0x00000000	GPIO2A PAD open drain functionality enable
GPIO2_IOC_GPIO2A_SUS	0x0150	W	0x00000000	GPIO2A PAD weak Pull Keeper enable
GPIO2_IOC_GPIO2A_SL	0x0190	W	0x0000000F	Slew Rate Control for the driver secton while driving PAD.
GPIO2_IOC_GPIO2A_DS0	0x0240	W	0x00000707	GPIO2A driver strength control
GPIO2_IOC_IO_VSEL0	0x0300	W	0x00000070	IO voltage seletion register0
GPIO2_IOC_GMAC0_IOFUNC1_CON0	0x0400	W	0x00000000	RGMII M1 IO control register1
GPIO2_IOC_GMAC0_IOFUNC1_CON1	0x0404	W	0x00000000	RGMII M1 IO control register1
GPIO2_IOC_SDCARD0_IO_CON	0x0500	W	0x0003A980	saradc0 IO control register
GPIO2_IOC_JTAG_M1_CON	0x0504	W	0x00000001	JTAG m1 control register0

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.8.2 Detail Registers Description

GPIO2_IOC_GPIO2A_IOMUX_SEL_L

Address: Operational Base(0xFF060000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6:4	RW	0x0	gpio2a1_sel 3'h0: GPIO2_A1 3'h1: I2S2_MCLK_M0 3'h2: ETH_CLK_25M_OUT_M1 3'h3: CLK1_32K_OUT 3'h4: SPI2_CLK_M1 3'h5: I2S0_SDO3_M1
3	RO	0x0	reserved
2:0	RW	0x0	gpio2a0_sel 3'h0: GPIO2_A0 3'h1: I2S2_SDI_M0 3'h2: RGMII_RXER_M1 3'h3: UART4_CTSN_M1 3'h4: SPI2_MISO_M1 3'h5: PWM15_M1 3'h6: RMII_RXER

GPIO2_IOC_GPIO2A_P

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Address: Operational Base(0xFF060000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3:2	RW	0x2	gpio2a1_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
1:0	RW	0x2	gpio2a0_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

GPIO2_IOC_GPIO2A_IE

Address: Operational Base(0xFF060000) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3:2	RW	0x1	gpio2a1_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
1:0	RW	0x1	gpio2a0_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

GPIO2_IOC_GPIO2A_OD

Address: Operational Base(0xFF060000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	gpio2a1_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio2a0_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

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GPIO2_IOC_GPIO2A_SUS

Address: Operational Base(0xFF060000) + offset (0x0150)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	gpio2a1_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio2a0_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

GPIO2_IOC_GPIO2A_SL

Address: Operational Base(0xFF060000) + offset (0x0190)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3:2	RW	0x3	gpio2a1_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
1:0	RW	0x3	gpio2a0_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

GPIO2_IOC_GPIO2A_DS0

Address: Operational Base(0xFF060000) + offset (0x0240)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio2a1_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

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Bit	Attr	Reset Value	Description
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio2a0_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO2_IOC_IO_VSEL0

Address: Operational Base(0xFF060000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RO	0x0	poc_vccio4_vd VCCIO4 hardware voltage status 1'b0: 1.8V 1'b1: 3.3V
13	RO	0x0	poc_vccio3_vd VCCIO3 hardware voltage status 1'b0: 1.8V 1'b1: 3.3V
12	RO	0x0	poc_vccio2_vd VCCIO2 hardware voltage status 1'b0: 1.8V 1'b1: 3.3V
11:10	RO	0x0	reserved
9	RW	0x0	poc_vccio4_iddq VCCIO4 iddq control 1'b0: Disable 1'b1: Enable
8	RW	0x0	poc_vccio3_iddq VCCIO3 iddq control 1'b0: Disable 1'b1: Enable
7	RW	0x0	poc_vccio2_iddq VCCIO2 iddq control 1'b0: Disable 1'b1: Enable
6	RW	0x1	poc_vccio4_sel33 VCCIO4 3.3V control 1'b0: Disable 1'b1: Enable
5	RW	0x1	poc_vccio3_sel33 VCCIO3 3.3V control 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
4	RW	0x1	poc_vccio2_sel33 VCCIO2 3.3V control 1'b0: Disable 1'b1: Enable
3	RW	0x0	poc_vccio4_sel18 VCCIO4 1.8V control 1'b0: Disable 1'b1: Enable
2	RW	0x0	poc_vccio3_sel18 VCCIO3 1.8V control 1'b0: Disable 1'b1: Enable
1	RW	0x0	poc_vccio2_sel18 VCCIO2 1.8V control 1'b0: Disable 1'b1: Enable
0	RW	0x0	poc_vccio234_sel VCCIO voltage source select control 1'b0: From hardware 1'b1: From ioc_grf

GPIO2_IOC_GMAC0_IOFUNC1_CON0

Address: Operational Base(0xFF060000) + offset (0x0400)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x00	gmac0_iofunc1_clk_rx_dl_cfg EQOS GMAC0 M1 RX clock delayline enable 1'b1: Enable 1'b0: Disable
7:0	RW	0x00	gmac0_iofunc1_clk_tx_dl_cfg EQOS GMAC0 M1 TX clock delayline enable 1'b1: Enable 1'b0: Disable

GPIO2_IOC_GMAC0_IOFUNC1_CON1

Address: Operational Base(0xFF060000) + offset (0x0404)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	gmac1_extclk_sel RMII ONLY GMAC1 external clock select, need config simultaneously with GRF_SYS_SOC_CON1[15] 1'b1: from external 1'b0: from CRU
2	RW	0x0	gmac0_iofunc1_extclk_sel EQOS GMAC0 M1 external clock select , need config simultaneously with GRF_SYS_SOC_CON0[9] 1'b1: from external 1'b0: from CRU

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Bit	Attr	Reset Value	Description
1	RW	0x0	gmac0_iofunc1_rxclk_dly_ena EQOS GMAC0 M1 RX clock delayline enable 1'b1: Enable 1'b0: Disable
0	RW	0x0	gmac0_iofunc1_txclk_dly_ena EQOS GMAC0 M1 TX clock delayline enable 1'b1: Enable 1'b0: Disable

GPIO2_IOC_SDCARD0_IO_CON

Address: Operational Base(0xFF060000) + offset (0x0500)

Bit	Attr	Reset Value	Description
31:0	RW	0x0003a980	sdcard_dectn_dly Delay counter setting after sdcard plug out. Count by 24M clock

GPIO2_IOC_JTAG_M1_CON

Address: Operational Base(0xFF060000) + offset (0x0504)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2:1	RW	0x0	jtag_sel_m1 Switch source when GPIO1b5 and GPIO1b6 switch to JTAG function. 2'b00: connect to CPU 2'b01: connect to BUSMCU 2'b10: connect to PMUMCU 2'b11: Reserved
0	RW	0x1	force_jtag Force SDMMC IO to JTAG function enable When force_jtag is high , gpio1_b5_sel is 0x1 , gpio1_b6_sel is 0x1, and SDMMC_DETECTN is inactive, switch the SDMMC IO to CPU JTAG function.

5.9 GPIO3_IOC Register Description

5.9.1 Registers Summary

Name	Offset	Size	Reset Value	Description
GPIO3_IOC_GPIO3A_IOMUX_SEL_L	0x0040	W	0x00000000	GPIO3A IOMUX control low bits
GPIO3_IOC_GPIO3A_IOMUX_SEL_H	0x0044	W	0x00000000	GPIO3A IOMUX control high bits
GPIO3_IOC_GPIO3B_IOMUX_SEL_L	0x0048	W	0x00000000	GPIO3B IOMUX control low bits
GPIO3_IOC_GPIO3B_IOMUX_SEL_H	0x004C	W	0x00000000	GPIO3B IOMUX control high bits
GPIO3_IOC_GPIO3C_IOMUX_SEL_L	0x0050	W	0x00000000	GPIO3C IOMUX control low bits
GPIO3_IOC_GPIO3C_IOMUX_SEL_H	0x0054	W	0x00000000	GPIO3C IOMUX control high bits

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Name	Offset	Size	Reset Value	Description
GPIO3_IOC_GPIO3D_IOMUX_SEL_L	0x0058	W	0x00000000	GPIO3D IOMUX control low bits
GPIO3_IOC_GPIO3D_IOMUX_SEL_H	0x005C	W	0x00000000	GPIO3D IOMUX control high bits
GPIO3_IOC_GPIO3A_P	0x00A0	W	0x0000AAAA	GPIO3A PU/PD control
GPIO3_IOC_GPIO3B_P	0x00A4	W	0x0000AAAA	GPIO3B PU/PD control
GPIO3_IOC_GPIO3C_P	0x00A8	W	0x0000AAAA	GPIO3C PU/PD control
GPIO3_IOC_GPIO3D_P	0x00AC	W	0x0000AAAA	GPIO3D PU/PD control
GPIO3_IOC_GPIO3A_IE	0x00E0	W	0x00005555	GPIO3A PAD input enable control
GPIO3_IOC_GPIO3B_IE	0x00E4	W	0x00005555	GPIO3B PAD input enable control
GPIO3_IOC_GPIO3C_IE	0x00E8	W	0x00005555	GPIO3C PAD input enable control
GPIO3_IOC_GPIO3D_IE	0x00EC	W	0x00005555	GPIO3D PAD input enable control
GPIO3_IOC_GPIO3A_OD	0x0120	W	0x00000000	GPIO3A PAD open drain functionality enable
GPIO3_IOC_GPIO3B_OD	0x0124	W	0x00000000	GPIO3B PAD open drain functionality enable
GPIO3_IOC_GPIO3C_OD	0x0128	W	0x00000000	GPIO3C PAD open drain functionality enable
GPIO3_IOC_GPIO3D_OD	0x012C	W	0x00000000	GPIO3D PAD open drain functionality enable
GPIO3_IOC_GPIO3A_SUS	0x0160	W	0x00000000	GPIO3A PAD weak Pull Keeper enable
GPIO3_IOC_GPIO3B_SUS	0x0164	W	0x00000000	GPIO3B PAD weak Pull Keeper enable
GPIO3_IOC_GPIO3C_SUS	0x0168	W	0x00000000	GPIO3C PAD weak Pull Keeper enable
GPIO3_IOC_GPIO3D_SUS	0x016C	W	0x00000000	GPIO3D PAD weak Pull Keeper enable
GPIO3_IOC_GPIO3A_SL	0x01A0	W	0x0000FFFF	Slew Rate Control for the driver secton while driving PAD.
GPIO3_IOC_GPIO3B_SL	0x01A4	W	0x0000FFFF	Slew Rate Control for the driver secton while driving PAD.
GPIO3_IOC_GPIO3C_SL	0x01A8	W	0x0000FFFF	Slew Rate Control for the driver secton while driving PAD.
GPIO3_IOC_GPIO3D_SL	0x01AC	W	0x0000FFFF	Slew Rate Control for the driver secton while driving PAD.
GPIO3_IOC_GPIO3A_DS0	0x0280	W	0x00000707	GPIO3A driver strength control
GPIO3_IOC_GPIO3A_DS1	0x0284	W	0x00000707	GPIO3A driver strength control
GPIO3_IOC_GPIO3A_DS2	0x0288	W	0x00000707	GPIO3A driver strength control
GPIO3_IOC_GPIO3A_DS3	0x028C	W	0x00000707	GPIO3A driver strength control
GPIO3_IOC_GPIO3B_DS0	0x0290	W	0x00000707	GPIO3B driver strength control
GPIO3_IOC_GPIO3B_DS1	0x0294	W	0x00000707	GPIO3B driver strength control
GPIO3_IOC_GPIO3B_DS2	0x0298	W	0x00000707	GPIO3B driver strength control
GPIO3_IOC_GPIO3B_DS3	0x029C	W	0x00000707	GPIO3B driver strength control
GPIO3_IOC_GPIO3C_DS0	0x02A0	W	0x00000707	GPIO3C driver strength control
GPIO3_IOC_GPIO3C_DS1	0x02A4	W	0x00000707	GPIO3C driver strength control
GPIO3_IOC_GPIO3C_DS2	0x02A8	W	0x00000707	GPIO3C driver strength control
GPIO3_IOC_GPIO3C_DS3	0x02AC	W	0x00000707	GPIO3C driver strength control
GPIO3_IOC_GPIO3D_DS0	0x02B0	W	0x00000707	GPIO3D driver strength control
GPIO3_IOC_GPIO3D_DS1	0x02B4	W	0x00000707	GPIO3D driver strength control
GPIO3_IOC_GPIO3D_DS2	0x02B8	W	0x00000707	GPIO3D driver strength control
GPIO3_IOC_GPIO3D_DS3	0x02BC	W	0x0000070F	GPIO3D driver strength control

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-*

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Double WORD (64 bits) access

5.9.2 Detail Registers Description

GPIO3_IOC_GPIO3A_IOMUX_SEL_L

Address: Operational Base(0xFF070000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio3a3_sel 3'h0: GPIO3_A3 3'h1: I2S0_SCLK_M0 3'h2: UART2_RTSN_M1
11	RO	0x0	reserved
10:8	RW	0x0	gpio3a2_sel 3'h0: GPIO3_A2 3'h1: I2S0_MCLK_M0 3'h2: UART2_CTSN_M1 3'h3: PDM_CLK1_M0
7	RO	0x0	reserved
6:4	RW	0x0	gpio3a1_sel 3'h0: GPIO3_A1 3'h1: I2C3_SDA_M0 3'h2: UART2_RX_M1 3'h3: SPDIF_TX_M0 3'h4: CAN0_RX_M0 3'h5: UART5_RTSN_M1
3	RO	0x0	reserved
2:0	RW	0x0	gpio3a0_sel 3'h0: GPIO3_A0 3'h1: I2C3_SCL_M0 3'h2: UART2_TX_M1 3'h3: PDM_SDI3_M0 3'h4: CAN0_TX_M0 3'h5: UART5_CTSN_M1

GPIO3_IOC_GPIO3A_IOMUX_SEL_H

Address: Operational Base(0xFF070000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio3a7_sel 3'h0: GPIO3_A7 3'h1: I2S0_SDO2_M0 3'h2: I2S0_SDI2_M0 3'h3: PDM_SDI2_M0 3'h4: PCIE20_WAKEN_M1 3'h5: UART5_RX_M1
11	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
10:8	RW	0x0	gpio3a6_sel 3'h0: GPIO3_A6 3'h1: I2S0_SDO1_M0 3'h2: I2S0_SDI3_M0 3'h3: PDM_CLK0_M0 3'h4: PCIE20_CLKREQN_M1 3'h5: UART5_TX_M1
7	RO	0x0	reserved
6:4	RW	0x0	gpio3a5_sel 3'h0: GPIO3_A5 3'h1: I2S0_SDO0_M0 3'h2: PWM9_M0
3	RO	0x0	reserved
2:0	RW	0x0	gpio3a4_sel 3'h0: GPIO3_A4 3'h1: I2S0_LRCK_M0 3'h2: PWM8_M0

GPIO3_IOC_GPIO3B_IOMUX_SEL_L

Address: Operational Base(0xFF070000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio3b3_sel 3'h0: GPIO3_B3 3'h1: I2S1_SCLK_M1 3'h2: CAM_CLK1_OUT_M0 3'h3: UART8_RX_M0
11	RO	0x0	reserved
10:8	RW	0x0	gpio3b2_sel 3'h0: GPIO3_B2 3'h1: I2S1_MCLK_M1 3'h2: CAM_CLK0_OUT_M0 3'h3: UART8_TX_M0
7	RO	0x0	reserved
6:4	RW	0x0	gpio3b1_sel 3'h0: GPIO3_B1 3'h1: I2S0_SDI0_M0 3'h2: PDM_SDI0_M0
3	RO	0x0	reserved
2:0	RW	0x0	gpio3b0_sel 3'h0: GPIO3_B0 3'h1: I2S0_SDO3_M0 3'h2: I2S0_SDI1_M0 3'h3: PDM_SDI1_M0 3'h4: PCIE20_PERSTN_M1

GPIO3_IOC_GPIO3B_IOMUX_SEL_H

Address: Operational Base(0xFF070000) + offset (0x004C)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio3b7_sel 3'h0: GPIO3_B7 3'h1: I2S1_SDO2_M1 3'h2: I2S1_SDI2_M1 3'h3: UART3_TX_M1 3'h4: SPI0_CSN0_M1 3'h5: I2C4_SDA_M0 3'h6: CAN0_RX_M1
11	RO	0x0	reserved
10:8	RW	0x0	gpio3b6_sel 3'h0: GPIO3_B6 3'h1: I2S1_SDO1_M1 3'h2: I2S1_SDI3_M1 3'h3: UART3_CTSN_M1 3'h4: SPI0_CSN1_M1 3'h5: I2C4_SCL_M0 3'h6: CAN0_TX_M1
7	RO	0x0	reserved
6:4	RW	0x0	gpio3b5_sel 3'h0: GPIO3_B5 3'h1: I2S1_SDO0_M1 3'h2: CAM_CLK3_OUT 3'h3: UART8_RTSN_M0 3'h4: SPI0_CLK_M1 3'h5: PWM13_M1
3	RO	0x0	reserved
2:0	RW	0x0	gpio3b4_sel 3'h0: GPIO3_B4 3'h1: I2S1_LRCK_M1 3'h2: CAM_CLK2_OUT 3'h3: UART8_CTSN_M0 3'h4: SPI0_MOSI_M1 3'h5: PWM12_M1

GPIO3_IOC_GPIO3C_IOMUX_SEL_L

Address: Operational Base(0xFF070000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio3c3_sel 3'h0: GPIO3_C3 3'h1: I2C5_SDA_M0 3'h2: ISP_FLASH_TRIGOUT 3'h3: UART9_RX_M1
11	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
10:8	RW	0x0	gpio3c2_sel 3'h0: GPIO3_C2 3'h1: I2C5_SCL_M0 3'h2: ISP_PRELIGHT_TRIGOUT 3'h3: UART9_TX_M1
7	RO	0x0	reserved
6:4	RW	0x0	gpio3c1_sel 3'h0: GPIO3_C1 3'h1: I2S1_SDI0_M1 3'h2: ISP_FLASH_TRIGIN 3'h3: UART3_RTSN_M1
3	RO	0x0	reserved
2:0	RW	0x0	gpio3c0_sel 3'h0: GPIO3_C0 3'h1: I2S1_SDO3_M1 3'h2: I2S1_SDI1_M1 3'h3: UART3_RX_M1 3'h4: SPI0_MISO_M1

GPIO3_IOC_GPIO3C_IOMUX_SEL_H

Address: Operational Base(0xFF070000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio3c7_sel 3'h0: GPIO3_C7 3'h1: VO_LCDC_D6 3'h2: I2S1_SDO0_M0 3'h3: UART7_RX_M0
11	RO	0x0	reserved
10:8	RW	0x0	gpio3c6_sel 3'h0: GPIO3_C6 3'h1: VO_LCDC_D5 3'h2: I2S1_LRCK_M0 3'h3: UART4_RTSN_M0 3'h4: PWM15_M0
7	RO	0x0	reserved
6:4	RW	0x0	gpio3c5_sel 3'h0: GPIO3_C5 3'h1: VO_LCDC_D4 3'h2: I2S1_SCLK_M0 3'h3: UART4_CTSN_M0 3'h4: PWM14_M0
3	RO	0x0	reserved
2:0	RW	0x0	gpio3c4_sel 3'h0: GPIO3_C4 3'h1: VO_LCDC_D3 3'h2: I2S1_MCLK_M0 3'h3: UART7_TX_M0

GPIO3_IOC_GPIO3D_IOMUX_SEL_L

Address: Operational Base(0xFF070000) + offset (0x0058)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio3d3_sel 3'h0: GPIO3_D3 3'h1: VO_LCDC_D12 3'h2: I2S1_SDI3_M0 3'h3: UART7_RTSN_M0 3'h4: SPI2_MOSI_M0 3'h5: I2C2_SDA_M1
11	RO	0x0	reserved
10:8	RW	0x0	gpio3d2_sel 3'h0: GPIO3_D2 3'h1: VO_LCDC_D11 3'h2: I2S1_SDI2_M0 3'h3: UART7_CTSN_M0 3'h4: SPI2_MISO_M0 3'h5: I2C2_SCL_M1
7	RO	0x0	reserved
6:4	RW	0x0	gpio3d1_sel 3'h0: GPIO3_D1 3'h1: VO_LCDC_D10 3'h2: I2S1_SDI1_M0 3'h3: UART4_RX_M0 3'h4: UART3_RTSN_M0
3	RO	0x0	reserved
2:0	RW	0x0	gpio3d0_sel 3'h0: GPIO3_D0 3'h1: VO_LCDC_D7 3'h2: I2S1_SDI0_M0 3'h3: UART4_TX_M0

GPIO3_IOC_GPIO3D_IOMUX_SEL_H

Address: Operational Base(0xFF070000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio3d7_sel 3'h0: GPIO3_D7 3'h1: VO_LCDC_D19 3'h2: RGMII_RXD2_M0 3'h3: UART8_CTSN_M1 3'h4: SPI1_CSN0_M0
11	RO	0x0	reserved
10:8	RW	0x0	gpio3d6_sel 3'h0: GPIO3_D6 3'h1: VO_LCDC_D15 3'h2: RGMII_TXCLK_M0 3'h3: I2S2_MCLK_M1 3'h4: SPI1_CLK_M0

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Bit	Attr	Reset Value	Description
7	RO	0x0	reserved
6:4	RW	0x0	gpio3d5_sel 3'h0: GPIO3_D5 3'h1: VO_LCDC_D14 3'h2: RGMII_TXD3_M0 3'h3: UART8_RX_M1 3'h4: I2S2_SDO_M1
3	RO	0x0	reserved
2:0	RW	0x0	gpio3d4_sel 3'h0: GPIO3_D4 3'h1: VO_LCDC_D13 3'h2: RGMII_TXD2_M0 3'h3: UART8_TX_M1 3'h4: I2S2_SDI_M1

GPIO3_IOC_GPIO3A_P

Address: Operational Base(0xFF070000) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	gpio3a7_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
13:12	RW	0x2	gpio3a6_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
11:10	RW	0x2	gpio3a5_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
9:8	RW	0x2	gpio3a4_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
7:6	RW	0x2	gpio3a3_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
5:4	RW	0x2	gpio3a2_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

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Bit	Attr	Reset Value	Description
3:2	RW	0x2	gpio3a1_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
1:0	RW	0x2	gpio3a0_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

GPIO3_IOC_GPIO3B_P

Address: Operational Base(0xFF070000) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	gpio3b7_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
13:12	RW	0x2	gpio3b6_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
11:10	RW	0x2	gpio3b5_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
9:8	RW	0x2	gpio3b4_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
7:6	RW	0x2	gpio3b3_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
5:4	RW	0x2	gpio3b2_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
3:2	RW	0x2	gpio3b1_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

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Bit	Attr	Reset Value	Description
1:0	RW	0x2	gpio3b0_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

GPIO3_IOC_GPIO3C_P

Address: Operational Base(0xFF070000) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	gpio3c7_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
13:12	RW	0x2	gpio3c6_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
11:10	RW	0x2	gpio3c5_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
9:8	RW	0x2	gpio3c4_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
7:6	RW	0x2	gpio3c3_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
5:4	RW	0x2	gpio3c2_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
3:2	RW	0x2	gpio3c1_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
1:0	RW	0x2	gpio3c0_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

GPIO3_IOC_GPIO3D_P

Address: Operational Base(0xFF070000) + offset (0x00AC)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	gpio3d7_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
13:12	RW	0x2	gpio3d6_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
11:10	RW	0x2	gpio3d5_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
9:8	RW	0x2	gpio3d4_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
7:6	RW	0x2	gpio3d3_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
5:4	RW	0x2	gpio3d2_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
3:2	RW	0x2	gpio3d1_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
1:0	RW	0x2	gpio3d0_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

GPIO3_IOC_GPIO3A_IE

Address: Operational Base(0xFF070000) + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:14	RW	0x1	gpio3a7_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
13:12	RW	0x1	gpio3a6_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
11:10	RW	0x1	gpio3a5_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
9:8	RW	0x1	gpio3a4_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
7:6	RW	0x1	gpio3a3_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
5:4	RW	0x1	gpio3a2_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
3:2	RW	0x1	gpio3a1_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
1:0	RW	0x1	gpio3a0_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

GPIO3_IOC_GPIO3B_IE

Address: Operational Base(0xFF070000) + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:14	RW	0x1	gpio3b7_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
13:12	RW	0x1	gpio3b6_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
11:10	RW	0x1	gpio3b5_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
9:8	RW	0x1	gpio3b4_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
7:6	RW	0x1	gpio3b3_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
5:4	RW	0x1	gpio3b2_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
3:2	RW	0x1	gpio3b1_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
1:0	RW	0x1	gpio3b0_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

GPIO3_IOC_GPIO3C_IE

Address: Operational Base(0xFF070000) + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:14	RW	0x1	gpio3c7_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
13:12	RW	0x1	gpio3c6_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
11:10	RW	0x1	gpio3c5_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
9:8	RW	0x1	gpio3c4_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
7:6	RW	0x1	gpio3c3_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
5:4	RW	0x1	gpio3c2_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
3:2	RW	0x1	gpio3c1_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
1:0	RW	0x1	gpio3c0_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

GPIO3_IOC_GPIO3D_IE

Address: Operational Base(0xFF070000) + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:14	RW	0x1	gpio3d7_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
13:12	RW	0x1	gpio3d6_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
11:10	RW	0x1	gpio3d5_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
9:8	RW	0x1	gpio3d4_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
7:6	RW	0x1	gpio3d3_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
5:4	RW	0x1	gpio3d2_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
3:2	RW	0x1	gpio3d1_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
1:0	RW	0x1	gpio3d0_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

GPIO3_IOC_GPIO3A_OD

Address: Operational Base(0xFF070000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:8	RO	0x00	reserved
7	RW	0x0	gpio3a7_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio3a6_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio3a5_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio3a4_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio3a3_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio3a2_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio3a1_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio3a0_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

GPIO3_IOC_GPIO3B_OD

Address: Operational Base(0xFF070000) + offset (0x0124)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio3b7_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio3b6_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio3b5_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
4	RW	0x0	gpio3b4_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio3b3_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio3b2_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio3b1_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio3b0_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

GPIO3_IOC_GPIO3C_OD

Address: Operational Base(0xFF070000) + offset (0x0128)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio3c7_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio3c6_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio3c5_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio3c4_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio3c3_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio3c2_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
1	RW	0x0	gpio3c1_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio3c0_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

GPIO3_IOC_GPIO3D_OD

Address: Operational Base(0xFF070000) + offset (0x012C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio3d7_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio3d6_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio3d5_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio3d4_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio3d3_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio3d2_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio3d1_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio3d0_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

GPIO3_IOC_GPIO3A_SUS

Address: Operational Base(0xFF070000) + offset (0x0160)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio3a7_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio3a6_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio3a5_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio3a4_sus GPIO PADweak Pull Keeper enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio3a3_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio3a2_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio3a1_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio3a0_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

GPIO3_IOC_GPIO3B_SUS

Address: Operational Base(0xFF070000) + offset (0x0164)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio3b7_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio3b6_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
5	RW	0x0	gpio3b5_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio3b4_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio3b3_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio3b2_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio3b1_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio3b0_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

GPIO3_IOC_GPIO3C_SUS

Address: Operational Base(0xFF070000) + offset (0x0168)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio3c7_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio3c6_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio3c5_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio3c4_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio3c3_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
2	RW	0x0	gpio3c2_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio3c1_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio3c0_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

GPIO3_IOC_GPIO3D_SUS

Address: Operational Base(0xFF070000) + offset (0x016C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio3d7_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio3d6_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio3d5_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio3d4_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio3d3_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio3d2_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio3d1_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio3d0_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

GPIO3_IOC_GPIO3A_SL

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Address: Operational Base(0xFF070000) + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x3	gpio3a7_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
13:12	RW	0x3	gpio3a6_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
11:10	RW	0x3	gpio3a5_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
9:8	RW	0x3	gpio3a4_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
7:6	RW	0x3	gpio3a3_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
5:4	RW	0x3	gpio3a2_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
3:2	RW	0x3	gpio3a1_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
1:0	RW	0x3	gpio3a0_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

GPIO3_IOC_GPIO3B_SL

Address: Operational Base(0xFF070000) + offset (0x01A4)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x3	gpio3b7_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
13:12	RW	0x3	gpio3b6_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
11:10	RW	0x3	gpio3b5_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
9:8	RW	0x3	gpio3b4_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
7:6	RW	0x3	gpio3b3_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
5:4	RW	0x3	gpio3b2_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
3:2	RW	0x3	gpio3b1_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
1:0	RW	0x3	gpio3b0_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

GPIO3_IOC_GPIO3C_SL

Address: Operational Base(0xFF070000) + offset (0x01A8)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x3	gpio3c7_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
13:12	RW	0x3	gpio3c6_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
11:10	RW	0x3	gpio3c5_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
9:8	RW	0x3	gpio3c4_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
7:6	RW	0x3	gpio3c3_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
5:4	RW	0x3	gpio3c2_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
3:2	RW	0x3	gpio3c1_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
1:0	RW	0x3	gpio3c0_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

GPIO3_IOC_GPIO3D_SL

Address: Operational Base(0xFF070000) + offset (0x01AC)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x3	gpio3d7_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
13:12	RW	0x3	gpio3d6_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
11:10	RW	0x3	gpio3d5_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
9:8	RW	0x3	gpio3d4_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
7:6	RW	0x3	gpio3d3_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
5:4	RW	0x3	gpio3d2_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
3:2	RW	0x3	gpio3d1_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
1:0	RW	0x3	gpio3d0_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

GPIO3_IOC_GPIO3A_DS0

Address: Operational Base(0xFF070000) + offset (0x0280)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio3a1_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio3a0_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO3_IOC_GPIO3A_DS1

Address: Operational Base(0xFF070000) + offset (0x0284)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio3a3_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio3a2_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

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GPIO3_IOC_GPIO3A_DS2

Address: Operational Base(0xFF070000) + offset (0x0288)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio3a5_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio3a4_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO3_IOC_GPIO3A_DS3

Address: Operational Base(0xFF070000) + offset (0x028C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio3a7_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x07	gpio3a6_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO3_IOC_GPIO3B_DS0

Address: Operational Base(0xFF070000) + offset (0x0290)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio3b1_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio3b0_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO3_IOC_GPIO3B_DS1

Address: Operational Base(0xFF070000) + offset (0x0294)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x07	gpio3b3_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio3b2_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO3_IOC_GPIO3B_DS2

Address: Operational Base(0xFF070000) + offset (0x0298)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio3b5_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio3b4_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO3_IOC_GPIO3B_DS3

Address: Operational Base(0xFF070000) + offset (0x029C)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio3b7_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio3b6_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO3_IOC_GPIO3C_DS0

Address: Operational Base(0xFF070000) + offset (0x02A0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio3c1_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio3c0_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

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GPIO3_IOC_GPIO3C_DS1

Address: Operational Base(0xFF070000) + offset (0x02A4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio3c3_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio3c2_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO3_IOC_GPIO3C_DS2

Address: Operational Base(0xFF070000) + offset (0x02A8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio3c5_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x07	gpio3c4_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO3_IOC_GPIO3C_DS3

Address: Operational Base(0xFF070000) + offset (0x02AC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio3c7_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio3c6_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO3_IOC_GPIO3D_DS0

Address: Operational Base(0xFF070000) + offset (0x02B0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x07	gpio3d1_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio3d0_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO3_IOC_GPIO3D_DS1

Address: Operational Base(0xFF070000) + offset (0x02B4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio3d3_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio3d2_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO3_IOC_GPIO3D_DS2

Address: Operational Base(0xFF070000) + offset (0x02B8)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio3d5_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio3d4_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO3_IOC_GPIO3D_DS3

Address: Operational Base(0xFF070000) + offset (0x02BC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio3d7_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio3d6_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

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5.10 GPIO4_IOC Register Description

5.10.1 Registers Summary

Name	Offset	Size	Reset Value	Description
GPIO4_IOC_GPIO4A_IOMUX_SEL_L	0x0060	W	0x00000000	GPIO4A IOMUX control low bits
GPIO4_IOC_GPIO4A_IOMUX_SEL_H	0x0064	W	0x00000000	GPIO4A IOMUX control high bits
GPIO4_IOC_GPIO4B_IOMUX_SEL_L	0x0068	W	0x00000000	GPIO4B IOMUX control low bits
GPIO4_IOC_GPIO4B_IOMUX_SEL_H	0x006C	W	0x00000000	GPIO4B IOMUX control high bits
GPIO4_IOC_GPIO4A_P	0x00B0	W	0x0000AAAA	GPIO4A PU/PD control
GPIO4_IOC_GPIO4B_P	0x00B4	W	0x0000AAAA	GPIO4B PU/PD control
GPIO4_IOC_GPIO4A_IE	0x00F0	W	0x00005555	GPIO4A PAD input enable control
GPIO4_IOC_GPIO4B_IE	0x00F4	W	0x00005555	GPIO4B PAD input enable control
GPIO4_IOC_GPIO4A_OD	0x0130	W	0x00000000	GPIO4A PAD open drain functionality enable
GPIO4_IOC_GPIO4B_OD	0x0134	W	0x00000000	GPIO4B PAD open drain functionality enable
GPIO4_IOC_GPIO4A_SUS	0x0170	W	0x00000000	GPIO4A PAD weak Pull Keeper enable
GPIO4_IOC_GPIO4B_SUS	0x0174	W	0x00000000	GPIO4B PAD weak Pull Keeper enable
GPIO4_IOC_GPIO4A_SL	0x01B0	W	0x0000FFFF	Slew Rate Control for the driver secton while driving PAD.
GPIO4_IOC_GPIO4B_SL	0x01B4	W	0x0000FFFF	Slew Rate Control for the driver secton while driving PAD.
GPIO4_IOC_GPIO4A_DS0	0x02C0	W	0x00000707	GPIO4A driver strength control
GPIO4_IOC_GPIO4A_DS1	0x02C4	W	0x00000707	GPIO4A driver strength control
GPIO4_IOC_GPIO4A_DS2	0x02C8	W	0x00000707	GPIO4A driver strength control
GPIO4_IOC_GPIO4A_DS3	0x02CC	W	0x00000707	GPIO4A driver strength control
GPIO4_IOC_GPIO4B_DS0	0x02D0	W	0x00000707	GPIO4B driver strength control
GPIO4_IOC_GPIO4B_DS1	0x02D4	W	0x00000707	GPIO4B driver strength control
GPIO4_IOC_GPIO4B_DS2	0x02D8	W	0x00000707	GPIO4B driver strength control
GPIO4_IOC_GPIO4B_DS3	0x02DC	W	0x00000F0F	GPIO4B driver strength control
GPIO4_IOC_IO_VSEL1	0x0300	W	0x00000070	IO voltage seletion register1
GPIO4_IOC_GMAC0_IOFUNC0_CON0	0x0400	W	0x00000000	RGMII M0 IO control register0
GPIO4_IOC_GMAC0_IOFUNC0_CON1	0x0404	W	0x00000000	RGMII M0 IO control register1
GPIO4_IOC_VO_IO_CON	0x0500	W	0x00000000	display io control register
GPIO4_IOC_SARADC1_CON	0x0590	W	0x00000007	saradc1 io control register

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.10.2 Detail Registers Description

GPIO4_IOC_GPIO4A_IOMUX_SEL_L

Address: Operational Base(0xFF070000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15	RO	0x0	reserved
14:12	RW	0x0	gpio4a3_sel 3'h0: GPIO4_A3 3'h1: VO_LCDC_D23 3'h2: RGMII_TXD1_M0 3'h3: UART6_RTSN_M1 3'h4: SPI1_MISO_M0
11	RO	0x0	reserved
10:8	RW	0x0	gpio4a2_sel 3'h0: GPIO4_A2 3'h1: VO_LCDC_D22 3'h2: RGMII_TXD0_M0 3'h3: UART6_CTSN_M1 3'h4: SPI1_MOSI_M0
7	RO	0x0	reserved
6:4	RW	0x0	gpio4a1_sel 3'h0: GPIO4_A1 3'h1: VO_LCDC_D21 3'h2: RGMII_RXCLK_M0 3'h3: I2S2_LRCK_M1 3'h4: PWM12_M0
3	RO	0x0	reserved
2:0	RW	0x0	gpio4a0_sel 3'h0: GPIO4_A0 3'h1: VO_LCDC_D20 3'h2: RGMII_RXD3_M0 3'h3: UART8_RTSN_M1 3'h4: SPI1_CSN1_M0

GPIO4_IOC_GPIO4A_IOMUX_SEL_H

Address: Operational Base(0xFF070000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio4a7_sel 3'h0: GPIO4_A7 3'h1: VO_LCDC_D9 3'h2: RGMII_RXDV_M0 3'h3: UART1_RTSN_M1 3'h4: PDM_SDI0_M1 3'h5: UART6_TX_M1
11	RO	0x0	reserved
10:8	RW	0x0	gpio4a6_sel 3'h0: GPIO4_A6 3'h1: VO_LCDC_D8 3'h2: RGMII_RXD1_M0 3'h3: UART1_RX_M1 3'h4: PDM_SDI3_M1 3'h5: I2C3_SDA_M1
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:4	RW	0x0	gpio4a5_sel 3'h0: GPIO4_A5 3'h1: VO_LCDC_D1 3'h2: RGMII_RXD0_M0 3'h3: UART1_TX_M1 3'h4: PDM_SDI2_M1 3'h5: I2C3_SCL_M1
3	RO	0x0	reserved
2:0	RW	0x0	gpio4a4_sel 3'h0: GPIO4_A4 3'h1: VO_LCDC_D0 3'h2: RGMII_TXEN_M0 3'h3: PWM13_M0

GPIO4_IOC_GPIO4B_IOMUX_SEL_L

Address: Operational Base(0xFF070000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio4b3_sel 3'h0: GPIO4_B3 3'h1: VO_LCDC_D18 3'h2: RGMII_MDIO_M0 3'h3: UART9_RX_M0
11	RO	0x0	reserved
10:8	RW	0x0	gpio4b2_sel 3'h0: GPIO4_B2 3'h1: VO_LCDC_D2 3'h2: RGMII_MDC_M0 3'h3: UART9_TX_M0
7	RO	0x0	reserved
6:4	RW	0x0	gpio4b1_sel 3'h0: GPIO4_B1 3'h1: VO_LCDC_D17 3'h2: ETH_CLK_25M_OUT_M0 3'h3: CAM_CLK0_OUT_M1 3'h4: I2S2_SCLK_M1 3'h5: PDM_CLK1_M1
3	RO	0x0	reserved
2:0	RW	0x0	gpio4b0_sel 3'h0: GPIO4_B0 3'h1: VO_LCDC_D16 3'h2: RGMII_RXER_M0 3'h3: UART1_CTSN_M1 3'h4: PDM_SDI1_M1 3'h5: UART6_RX_M1

GPIO4_IOC_GPIO4B_IOMUX_SEL_H

Address: Operational Base(0xFF070000) + offset (0x006C)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio4b7_sel 3'h0: GPIO4_B7 3'h1: VO_LCDC_CLK 3'h2: RGMII_CLK_M0 3'h3: CAM_CLK1_OUT_M1 3'h4: PDM_CLK0_M1
11	RO	0x0	reserved
10:8	RW	0x0	gpio4b6_sel 3'h0: GPIO4_B6 3'h1: VO_LCDC_DEN 3'h2: I2S1_SDO3_M0 3'h3: UART3_CTSN_M0 3'h4: SPI2_CLK_M0
7	RO	0x0	reserved
6:4	RW	0x0	gpio4b5_sel 3'h0: GPIO4_B5 3'h1: VO_LCDC_VSYNC 3'h2: I2S1_SDO2_M0 3'h3: UART9_RTSN_M0 3'h4: SPI2_CSN0_M0 3'h5: I2C1_SDA_M1 3'h6: UART3_RX_M0
3	RO	0x0	reserved
2:0	RW	0x0	gpio4b4_sel 3'h0: GPIO4_B4 3'h1: VO_LCDC_HSYNC 3'h2: I2S1_SDO1_M0 3'h3: UART9_CTSN_M0 3'h4: SPI2_CSN1_M0 3'h5: I2C1_SCL_M1 3'h6: UART3_TX_M0

GPIO4_IOC_GPIO4A_P

Address: Operational Base(0xFF070000) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	gpio4a7_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
13:12	RW	0x2	gpio4a6_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

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Bit	Attr	Reset Value	Description
11:10	RW	0x2	gpio4a5_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
9:8	RW	0x2	gpio4a4_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
7:6	RW	0x2	gpio4a3_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
5:4	RW	0x2	gpio4a2_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
3:2	RW	0x2	gpio4a1_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
1:0	RW	0x2	gpio4a0_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

GPIO4_IOC_GPIO4B_P

Address: Operational Base(0xFF070000) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	gpio4b7_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
13:12	RW	0x2	gpio4b6_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
11:10	RW	0x2	gpio4b5_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

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Bit	Attr	Reset Value	Description
9:8	RW	0x2	gpio4b4_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
7:6	RW	0x2	gpio4b3_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
5:4	RW	0x2	gpio4b2_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
3:2	RW	0x2	gpio4b1_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
1:0	RW	0x2	gpio4b0_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

GPIO4_IOC_GPIO4A_IE

Address: Operational Base(0xFF070000) + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	gpio4a7_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
13:12	RW	0x1	gpio4a6_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
11:10	RW	0x1	gpio4a5_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

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Bit	Attr	Reset Value	Description
9:8	RW	0x1	gpio4a4_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
7:6	RW	0x1	gpio4a3_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
5:4	RW	0x1	gpio4a2_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
3:2	RW	0x1	gpio4a1_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
1:0	RW	0x1	gpio4a0_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

GPIO4_IOC_GPIO4B_IE

Address: Operational Base(0xFF070000) + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	gpio4b7_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
13:12	RW	0x1	gpio4b6_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
11:10	RW	0x1	gpio4b5_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

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Bit	Attr	Reset Value	Description
9:8	RW	0x1	gpio4b4_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
7:6	RW	0x1	gpio4b3_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
5:4	RW	0x1	gpio4b2_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
3:2	RW	0x1	gpio4b1_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
1:0	RW	0x1	gpio4b0_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

GPIO4_IOC_GPIO4A_OD

Address: Operational Base(0xFF070000) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio4a7_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio4a6_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio4a5_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio4a4_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3	RW	0x0	gpio4a3_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio4a2_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio4a1_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio4a0_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

GPIO4_IOC_GPIO4B_OD

Address: Operational Base(0xFF070000) + offset (0x0134)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio4b7_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio4b6_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio4b5_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio4b4_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio4b3_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio4b2_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio4b1_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
0	RW	0x0	gpio4b0_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

GPIO4_IOC_GPIO4A_SUS

Address: Operational Base(0xFF070000) + offset (0x0170)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio4a7_sus GPIO PAD weak Pull Keeper enablee 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio4a6_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio4a5_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio4a4_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio4a3_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio4a2_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio4a1_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio4a0_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

GPIO4_IOC_GPIO4B_SUS

Address: Operational Base(0xFF070000) + offset (0x0174)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
7	RW	0x0	gpio4b7_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio4b6_sus GPIO weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio4b5_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio4b4_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio4b3_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio4b2_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio4b1_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio4b0_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

GPIO4_IOC_GPIO4A_SL

Address: Operational Base(0xFF070000) + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x3	gpio4a7_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
13:12	RW	0x3	gpio4a6_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

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Bit	Attr	Reset Value	Description
11:10	RW	0x3	gpio4a5_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
9:8	RW	0x3	gpio4a4_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
7:6	RW	0x3	gpio4a3_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
5:4	RW	0x3	gpio4a2_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
3:2	RW	0x3	gpio4a1_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
1:0	RW	0x3	gpio4a0_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

GPIO4_IOC_GPIO4B_SL

Address: Operational Base(0xFF070000) + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
15:14	RW	0x3	gpio4b7_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

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Bit	Attr	Reset Value	Description
13:12	RW	0x3	gpio4b6_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
11:10	RW	0x3	gpio4b5_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
9:8	RW	0x3	gpio4b4_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
7:6	RW	0x3	gpio4b3_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
5:4	RW	0x3	gpio4b2_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
3:2	RW	0x3	gpio4b1_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
1:0	RW	0x3	gpio4b0_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

GPIO4_IOC_GPIO4A_DS0

Address: Operational Base(0xFF070000) + offset (0x02C0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x07	gpio4a1_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio4a0_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO4_IOC_GPIO4A_DS1

Address: Operational Base(0xFF070000) + offset (0x02C4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio4a3_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio4a2_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO4_IOC_GPIO4A_DS2

Address: Operational Base(0xFF070000) + offset (0x02C8)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio4a5_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio4a4_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO4_IOC_GPIO4A_DS3

Address: Operational Base(0xFF070000) + offset (0x02CC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio4a7_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio4a6_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

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GPIO4_IOC_GPIO4B_DS0

Address: Operational Base(0xFF070000) + offset (0x02D0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio4b1_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio4b0_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO4_IOC_GPIO4B_DS1

Address: Operational Base(0xFF070000) + offset (0x02D4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio4b3_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x07	gpio4b2_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO4_IOC_GPIO4B_DS2

Address: Operational Base(0xFF070000) + offset (0x02D8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio4b5_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio4b4_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO4_IOC_GPIO4B_DS3

Address: Operational Base(0xFF070000) + offset (0x02DC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x0f	gpio4b7_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio4b6_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO4_IOC_IO_VSEL1

Address: Operational Base(0xFF070000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RO	0x0	poc_vccio6_vd VCCIO6 hardware voltage status 1'b0: 1.8V 1'b1: 3.3V
13	RO	0x0	poc_vccio5_vd VCCIO5 hardware voltage status 1'b0: 1.8V 1'b1: 3.3V
12	RO	0x0	poc_vccio1_vd VCCIO1 hardware voltage status 1'b0: 1.8V 1'b1: 3.3V
11:10	RO	0x0	reserved
9	RW	0x0	poc_vccio6_iddq VCCIO6 iddq control 1'b0: Disable 1'b1: Enable
8	RW	0x0	poc_vccio5_iddq VCCIO5 iddq control 1'b0: Disable 1'b1: Enable
7	RW	0x0	poc_vccio1_iddq VCCIO1 iddq control 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
6	RW	0x1	poc_vccio6_sel33 VCCIO6 3.3V control 1'b0: Disable 1'b1: Enable
5	RW	0x1	poc_vccio5_sel33 VCCIO5 3.3V control 1'b0: Disable 1'b1: Enable
4	RW	0x1	poc_vccio1_sel33 VCCIO1 3.3V control 1'b0: Disable 1'b1: Enable
3	RW	0x0	poc_vccio6_sel18 VCCIO6 1.8V control 1'b0: Disable 1'b1: Enable
2	RW	0x0	poc_vccio5_sel18 VCCIO5 1.8V control 1'b0: Disable 1'b1: Enable
1	RW	0x0	poc_vccio1_sel18 VCCIO1 1.8V control 1'b0: Disable 1'b1: Enable
0	RW	0x0	poc_vccio156_sel VCCIO voltage source select control 1'b0: From hardware 1'b1: From ioc_grf

GPIO4_IOC_GMAC0_IOFUNC0_CON0

Address: Operational Base(0xFF070000) + offset (0x0400)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x00	gmac0_iofunc0_clk_rx_dl_cfg EQOS GMAC0 M0 RX clock delayline enable 1'b1: Enable 1'b0: Disable
7:0	RW	0x00	gmac0_iofunc0_clk_tx_dl_cfg EQOS GMAC0 M0 TX clock delayline enable 1'b1: Enable 1'b0: Disable

GPIO4_IOC_GMAC0_IOFUNC0_CON1

Address: Operational Base(0xFF070000) + offset (0x0404)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
2	RW	0x0	gmac0_iofunc0_extclk_sel EQOS GMAC0 M0 external clock select , need config simultaneously with GRF_SYS_SOC_CON0[9] 1'b1: from external 1'b0: from CRU
1	RW	0x0	gmac0_iofunc0_rxclk_dly_ena EQOS GMAC0 M0 RX clock delayline enable 1'b1: Enable 1'b0: Disable
0	RW	0x0	gmac0_iofunc0_txclk_dly_ena EQOS GMAC0 M0 TX clock delayline enable 1'b1: Enable 1'b0: Disable

GPIO4_IOC_VO_IO_CON

Address: Operational Base(0xFF070000) + offset (0x0500)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x00	rgb_dclk_delay_num rgb dclk delayline control
7	RO	0x0	reserved
6	RW	0x0	rgb_bypass 1'b1: Bypass data sync 1'b0: Use data sync
5:4	RO	0x0	reserved
3	RW	0x0	RGB_dclk_inv_sel 1'b0: Normal clock. 1'b1: rbg_dclk is inverted
2:0	RO	0x0	reserved

GPIO4_IOC_SARADC1_CON

Address: Operational Base(0xFF070000) + offset (0x0590)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0007	saradc_ana_reg Reserved

5.11 GPIO0_IOC Register Description

5.11.1 Registers Summary

Name	Offset	Size	Reset Value	Description
GPIO0_IOC_GPIO0A_IOMUX_SEL_L	0x0000	W	0x00000010	GPIO0A IOMUX Select Low bits
GPIO0_IOC_GPIO0A_IOMUX_SEL_H	0x0004	W	0x00000001	GPIO0A IOMUX Select High bits
GPIO0_IOC_GPIO0B_IOMUX_SEL_L	0x0008	W	0x00000000	GPIO0B IOMUX Select Low bits

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Name	Offset	Size	Reset Value	Description
GPIO0_IOC_GPIO0B_IOMUX_SEL_H	0x000C	W	0x00000000	GPIO0B IOMUX Select High bits
GPIO0_IOC_GPIO0C_IOMUX_SEL_L	0x0010	W	0x00000000	GPIO0C IOMUX Select Low bits
GPIO0_IOC_GPIO0C_IOMUX_SEL_H	0x0014	W	0x00000000	GPIO0C IOMUX Select High bits
GPIO0_IOC_GPIO0D_IOMUX_SEL_L	0x0018	W	0x00000000	GPIO0D IOMUX Select Low bits
GPIO0_IOC_GPIO0A_P	0x0020	W	0x0000A962	GPIO0A Pull-up/down Control
GPIO0_IOC_GPIO0B_P	0x0024	W	0x0000AAAA	GPIO0B Pull-up/down Control
GPIO0_IOC_GPIO0C_P	0x0028	W	0x0000AAAA	GPIO0C Pull-up/down Control
GPIO0_IOC_GPIO0D_P	0x002C	W	0x00000005	GPIO0D Pull-up/down Control
GPIO0_IOC_GPIO0A_IE	0x0030	W	0x0000FFFF	GPIO0A PAD input enable control
GPIO0_IOC_GPIO0B_IE	0x0034	W	0x0000FFFF	GPIO0B PAD input enable control
GPIO0_IOC_GPIO0C_IE	0x0038	W	0x0000FFFF	GPIO0C PAD input enable control
GPIO0_IOC_GPIO0D_IE	0x003C	W	0x0000000F	GPIO0D PAD input enable control
GPIO0_IOC_GPIO0A_OD	0x0040	W	0x00000000	GPIO0A PAD open drain functionality enable
GPIO0_IOC_GPIO0B_OD	0x0044	W	0x00000000	GPIO0B PAD open drain functionality enable
GPIO0_IOC_GPIO0C_OD	0x0048	W	0x00000000	GPIO0C PAD open drain functionality enable
GPIO0_IOC_GPIO0D_OD	0x004C	W	0x00000000	GPIO0D PAD open drain functionality enable
GPIO0_IOC_GPIO0A_SUS	0x0050	W	0x00000000	GPIO0A PAD weak Pull Keeper enable
GPIO0_IOC_GPIO0B_SUS	0x0054	W	0x00000000	GPIO0B PAD weak Pull Keeper enable
GPIO0_IOC_GPIO0C_SUS	0x0058	W	0x00000000	GPIO0C PAD weak Pull Keeper enable
GPIO0_IOC_GPIO0D_SUS	0x005C	W	0x00000000	GPIO0D PAD weak Pull Keeper enable
GPIO0_IOC_GPIO0A_SL	0x0060	W	0x0000FFFF	Slew Rate Control for the driver secton while driving PAD.
GPIO0_IOC_GPIO0B_SL	0x0064	W	0x0000FFFF	Slew Rate Control for the driver secton while driving PAD.
GPIO0_IOC_GPIO0C_SL	0x0068	W	0x0000FFFF	Slew Rate Control for the driver secton while driving PAD.
GPIO0_IOC_GPIO0D_SL	0x006C	W	0x0000000F	Slew Rate Control for the driver secton while driving PAD.
GPIO0_IOC_GPIO0A_DS0	0x0070	W	0x00000707	GPIO0A driver strength control
GPIO0_IOC_GPIO0A_DS1	0x0074	W	0x00000707	GPIO0A driver strength control
GPIO0_IOC_GPIO0A_DS2	0x0078	W	0x00000707	GPIO0A driver strength control
GPIO0_IOC_GPIO0A_DS3	0x007C	W	0x00000707	GPIO0A driver strength control
GPIO0_IOC_GPIO0B_DS0	0x0080	W	0x00000707	GPIO0B driver strength control
GPIO0_IOC_GPIO0B_DS1	0x0084	W	0x00000707	GPIO0B driver strength control
GPIO0_IOC_GPIO0B_DS2	0x0088	W	0x00000707	GPIO0B driver strength control
GPIO0_IOC_GPIO0B_DS3	0x008C	W	0x00000707	GPIO0B driver strength control
GPIO0_IOC_GPIO0C_DS0	0x0090	W	0x00000707	GPIO0C driver strength control
GPIO0_IOC_GPIO0C_DS1	0x0094	W	0x00000707	GPIO0C driver strength control
GPIO0_IOC_GPIO0C_DS2	0x0098	W	0x00000707	GPIO0C driver strength control
GPIO0_IOC_GPIO0C_DS3	0x009C	W	0x00000707	GPIO0C driver strength control
GPIO0_IOC_GPIO0D_DS0	0x00A0	W	0x00000707	GPIO0D driver strength control

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Name	Offset	Size	Reset Value	Description
GPIO0_IOC_JTAG_M0_CON	0x0100	W	0x00000001	JTAG m0 control register0
GPIO0_IOC_UART_IO_CON	0x0104	W	0x00000000	JTAG m0 control register1
GPIO0_IOC_IO_VSEL2	0x0148	W	0x00000004	IO voltage seletion register2
GPIO0_IOC_XIN_CON	0x014C	W	0x0000000F	OSC Control register

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.11.2 Detail Registers Description

GPIO0_IOC_GPIO0A_IOMUX_SEL_L

Address: Operational Base(0xFF080000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio0a3_sel 3'h0: GPIO0_A3 3'h1: PWR_CTRL1
11	RO	0x0	reserved
10:8	RW	0x0	gpio0a2_sel 3'h0: GPIO0_A2 3'h1: PWR_CTRL0 3'h2: TSADC_SHUT_M1
7	RO	0x0	reserved
6:4	RW	0x1	gpio0a1_sel 3'h0: GPIO0_A1 3'h1: TSADC_SHUT_M0 3'h2: TSADC_SHUT_ORG
3	RO	0x0	reserved
2:0	RW	0x0	gpio0a0_sel 3'h0: GPIO0_A0 3'h1: REF_CLK_OUT

GPIO0_IOC_GPIO0A_IOMUX_SEL_H

Address: Operational Base(0xFF080000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio0a7_sel 3'h0: GPIO0_A7 3'h1: PWM3_M0
11	RO	0x0	reserved
10:8	RW	0x0	gpio0a6_sel 3'h0: GPIO0_A6 3'h1: PCIE20_CLKREQN_M0
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:4	RW	0x0	gpio0a5_sel 3'h0: GPIO0_A5 3'h1: SDMMC0_PWREN 3'h2: I2C4_SCL_M1 3'h3: PMU_DEBUG
3	RO	0x0	reserved
2:0	RW	0x1	gpio0a4_sel 3'h0: GPIO0_A4 3'h1: SDMMC0_DETN 3'h2: I2C4_SDA_M1

GPIO0_IOC_GPIO0B_IOMUX_SEL_L

Address: Operational Base(0xFF080000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio0b3_sel 3'h0: GPIO0_B3 3'h1: I2C1_SCL_M0
11	RO	0x0	reserved
10:8	RW	0x0	gpio0b2_sel 3'h0: GPIO0_B2 3'h1: I2C0_SDA
7	RO	0x0	reserved
6:4	RW	0x0	gpio0b1_sel 3'h0: GPIO0_B1 3'h1: I2C0_SCL
3	RO	0x0	reserved
2:0	RW	0x0	gpio0b0_sel 3'h0: GPIO0_B0 3'h1: CLK_32K_IN 3'h2: CLK0_32K_OUT 3'h3: PCIE20_BUTTONRSTN

GPIO0_IOC_GPIO0B_IOMUX_SEL_H

Address: Operational Base(0xFF080000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio0b7_sel 3'h0: GPIO0_B7 3'h1: SPI0_CSN1_M0 3'h2: PWM4_M0 3'h3: CPU_AVS 3'h4: SPDIF_TX_M1
11	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
10:8	RW	0x0	gpio0b6_sel 3'h0: GPIO0_B6 3'h1: I2C2_SDA_M0 3'h2: PCIE20_WAKEN_M0
7	RO	0x0	reserved
6:4	RW	0x0	gpio0b5_sel 3'h0: GPIO0_B5 3'h1: I2C2_SCL_M0 3'h2: PCIE20_PERSTN_M0
3	RO	0x0	reserved
2:0	RW	0x0	gpio0b4_sel 3'h0: GPIO0_B4 3'h1: I2C1_SDA_M0

GPIO0_IOC_GPIO0C_IOMUX_SEL_L

Address: Operational Base(0xFF080000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	gpio0c3_sel 3'h0: GPIO0_C3 3'h1: UART2_RTSN_M0 3'h2: PWM0_M0 3'h3: SPI0_CLK_M0
11	RO	0x0	reserved
10:8	RW	0x0	gpio0c2_sel 3'h0: GPIO0_C2 3'h1: UART2_CTSN_M0 3'h2: PWM5_M0 3'h3: SPI0_CSN0_M0
7	RO	0x0	reserved
6:4	RW	0x0	gpio0c1_sel 3'h0: GPIO0_C1 3'h1: UART2_RX_M0 3'h2: PWM6_M0 3'h3: NPU_AVS 3'h4: CAN1_RX_M1
3	RO	0x0	reserved
2:0	RW	0x0	gpio0c0_sel 3'h0: GPIO0_C0 3'h1: UART2_TX_M0 3'h2: PWM7_M0 3'h3: GPU_AVS 3'h4: CAN1_TX_M1

GPIO0_IOC_GPIO0C_IOMUX_SEL_H

Address: Operational Base(0xFF080000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15	RO	0x0	reserved
14:12	RW	0x0	gpio0c7_sel 3'h0: GPIO0_C7 3'h1: UART6_RX_M0 3'h2: CAN0_RX_M2
11	RO	0x0	reserved
10:8	RW	0x0	gpio0c6_sel 3'h0: GPIO0_C6 3'h1: UART6_TX_M0 3'h2: CAN0_TX_M2
7	RO	0x0	reserved
6:4	RW	0x0	gpio0c5_sel 3'h0: GPIO0_C5 3'h1: UART6_RTSN_M0 3'h2: PWM2_M0 3'h3: SPI0_MISO_M0
3	RO	0x0	reserved
2:0	RW	0x0	gpio0c4_sel 3'h0: GPIO0_C4 3'h1: UART6_CTSN_M0 3'h2: PWM1_M0 3'h3: SPI0_MOSI_M0

GPIO0_IOC_GPIO0D_IOMUX_SEL_L

Address: Operational Base(0xFF080000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6:4	RW	0x0	gpio0d1_sel 3'h0: GPIO0_D1 3'h1: UART0_TX_M0 3'h2: JTAG_CPU_MCU_TCK_M0
3	RO	0x0	reserved
2:0	RW	0x0	gpio0d0_sel 3'h0: GPIO0_D0 3'h1: UART0_RX_M0 3'h2: JTAG_CPU_MCU_TMS_M0

GPIO0_IOC_GPIO0A_P

Address: Operational Base(0xFF080000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	gpio0a7_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

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Bit	Attr	Reset Value	Description
13:12	RW	0x2	gpio0a6_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
11:10	RW	0x2	gpio0a5_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
9:8	RW	0x1	gpio0a4_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
7:6	RW	0x1	gpio0a3_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
5:4	RW	0x2	gpio0a2_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
3:2	RW	0x0	gpio0a1_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
1:0	RW	0x2	gpio0a0_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

GPIO0_IOC_GPIO0B_P

Address: Operational Base(0xFF080000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	gpio0b7_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
13:12	RW	0x2	gpio0b6_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

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Bit	Attr	Reset Value	Description
11:10	RW	0x2	gpio0b5_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
9:8	RW	0x2	gpio0b4_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
7:6	RW	0x2	gpio0b3_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
5:4	RW	0x2	gpio0b2_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
3:2	RW	0x2	gpio0b1_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
1:0	RW	0x2	gpio0b0_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

GPIO0_IOC_GPIO0C_P

Address: Operational Base(0xFF080000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	gpio0c7_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
13:12	RW	0x2	gpio0c6_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
11:10	RW	0x2	gpio0c5_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

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Bit	Attr	Reset Value	Description
9:8	RW	0x2	gpio0c4_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
7:6	RW	0x2	gpio0c3_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
5:4	RW	0x2	gpio0c2_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
3:2	RW	0x2	gpio0c1_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
1:0	RW	0x2	gpio0c0_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

GPIO0_IOC_GPIO0D_P

Address: Operational Base(0xFF080000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3:2	RW	0x1	gpio0d1_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;
1:0	RW	0x1	gpio0d0_p 2'b00: Z(Normal operation); 2'b01: Weak 1(pull-up); 2'b10: Weak 0(pull-down); 2'b11: Reserved;

GPIO0_IOC_GPIO0A_IE

Address: Operational Base(0xFF080000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:14	RW	0x3	gpio0a7_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
13:12	RW	0x3	gpio0a6_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
11:10	RW	0x3	gpio0a5_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
9:8	RW	0x3	gpio0a4_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
7:6	RW	0x3	gpio0a3_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
5:4	RW	0x3	gpio0a2_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
3:2	RW	0x3	gpio0a1_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
1:0	RW	0x3	gpio0a0_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

GPIO0_IOC_GPIO0B_IE

Address: Operational Base(0xFF080000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:14	RW	0x3	gpio0b7_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
13:12	RW	0x3	gpio0b6_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
11:10	RW	0x3	gpio0b5_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
9:8	RW	0x3	gpio0b4_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
7:6	RW	0x3	gpio0b3_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
5:4	RW	0x3	gpio0b2_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
3:2	RW	0x3	gpio0b1_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
1:0	RW	0x3	gpio0b0_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

GPIO0_IOC_GPIO0C_IE

Address: Operational Base(0xFF080000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:14	RW	0x3	gpio0c7_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
13:12	RW	0x3	gpio0c6_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
11:10	RW	0x3	gpio0c5_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
9:8	RW	0x3	gpio0c4_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
7:6	RW	0x3	gpio0c3_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
5:4	RW	0x3	gpio0c2_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
3:2	RW	0x3	gpio0c1_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
1:0	RW	0x3	gpio0c0_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

GPIO0_IOC_GPIO0D_IE

Address: Operational Base(0xFF080000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:4	RO	0x000	reserved
3:2	RW	0x3	gpio0d1_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved
1:0	RW	0x3	gpio0d0_ie GPIO PAD input enable 2'b00: Disable 2'b01: Non-Schmitt trigger input enable 2'b10: Schmitt trigger input enable 2'b11: Reserved

GPIO0_IOC_GPIO0A_OD

Address: Operational Base(0xFF080000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio0a7_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio0a6_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio0a5_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio0a4_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio0a3_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio0a2_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio0a1_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio0a0_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

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GPIO0_IOC_GPIO0B_OD

Address: Operational Base(0xFF080000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio0b7_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio0b6_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio0b5_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio0b4_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio0b3_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio0b2_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio0b1_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio0b0_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

GPIO0_IOC_GPIO0C_OD

Address: Operational Base(0xFF080000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio0c7_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
6	RW	0x0	gpio0c6_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio0c5_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio0c4_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio0c3_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio0c2_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio0c1_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio0c0_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

GPIO0_IOC_GPIO0D_OD

Address: Operational Base(0xFF080000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	gpio0d1_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio0d0_od GPIO PAD open drain functionality enable 1'b0: Disable 1'b1: Enable

GPIO0_IOC_GPIO0A_SUS

Address: Operational Base(0xFF080000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
7	RW	0x0	gpio0a7_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio0a6_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio0a5_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio0a4_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio0a3_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio0a2_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio0a1_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio0a0_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

GPIO0_IOC_GPIO0B_SUS

Address: Operational Base(0xFF080000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio0b7_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio0b6_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio0b5_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
4	RW	0x0	gpio0b4_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio0b3_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio0b2_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	gpio0b1_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio0b0_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

GPIO0_IOC_GPIO0C_SUS

Address: Operational Base(0xFF080000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio0c7_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
6	RW	0x0	gpio0c6_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	gpio0c5_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	gpio0c4_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	gpio0c3_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	gpio0c2_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
1	RW	0x0	gpio0c1_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio0c0_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

GPIO0_IOC_GPIO0D_SUS

Address: Operational Base(0xFF080000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	gpio0d1_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpio0d0_sus GPIO PAD weak Pull Keeper enable 1'b0: Disable 1'b1: Enable

GPIO0_IOC_GPIO0A_SL

Address: Operational Base(0xFF080000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x3	gpio0a7_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
13:12	RW	0x3	gpio0a6_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
11:10	RW	0x3	gpio0a5_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

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Bit	Attr	Reset Value	Description
9:8	RW	0x3	gpio0a4_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
7:6	RW	0x3	gpio0a3_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
5:4	RW	0x3	gpio0a2_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
3:2	RW	0x3	gpio0a1_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
1:0	RW	0x3	gpio0a0_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

GPIO0_IOC_GPIO0B_SL

Address: Operational Base(0xFF080000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x3	gpio0b7_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
13:12	RW	0x3	gpio0b6_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
11:10	RW	0x3	gpio0b5_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

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Bit	Attr	Reset Value	Description
9:8	RW	0x3	gpio0b4_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
7:6	RW	0x3	gpio0b3_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
5:4	RW	0x3	gpio0b2_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
3:2	RW	0x3	gpio0b1_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
1:0	RW	0x3	gpio0b0_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

GPIO0_IOC_GPIO0C_SL

Address: Operational Base(0xFF080000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x3	gpio0c7_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
13:12	RW	0x3	gpio0c6_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
11:10	RW	0x3	gpio0c5_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

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Bit	Attr	Reset Value	Description
9:8	RW	0x3	gpio0c4_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
7:6	RW	0x3	gpio0c3_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
5:4	RW	0x3	gpio0c2_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
3:2	RW	0x3	gpio0c1_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
1:0	RW	0x3	gpio0c0_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

GPIO0_IOC_GPIO0D_SL

Address: Operational Base(0xFF080000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3:2	RW	0x3	gpio0d1_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3
1:0	RW	0x3	gpio0d0_sl GPIO slew rate control, always set to 2'b11 in normal operation. 2'b00: Level 0 2'b01: Level 1 2'b10: Level 2 2'b11: Level 3

GPIO0_IOC_GPIO0A_DS0

Address: Operational Base(0xFF080000) + offset (0x0070)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio0a1_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio0a0_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO0_IOC_GPIO0A_DS1

Address: Operational Base(0xFF080000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio0a3_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio0a2_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

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GPIO0_IOC_GPIO0A_DS2

Address: Operational Base(0xFF080000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio0a5_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio0a4_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO0_IOC_GPIO0A_DS3

Address: Operational Base(0xFF080000) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio0a7_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x07	gpio0a6_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO0_IOC_GPIO0B_DS0

Address: Operational Base(0xFF080000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio0b1_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio0b0_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO0_IOC_GPIO0B_DS1

Address: Operational Base(0xFF080000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x07	gpio0b3_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio0b2_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO0_IOC_GPIO0B_DS2

Address: Operational Base(0xFF080000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio0b5_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio0b4_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO0_IOC_GPIO0B_DS3

Address: Operational Base(0xFF080000) + offset (0x008C)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio0b7_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio0b6_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO0_IOC_GPIO0C_DS0

Address: Operational Base(0xFF080000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio0c1_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio0c0_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

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GPIO0_IOC_GPIO0C_DS1

Address: Operational Base(0xFF080000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio0c3_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio0c2_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO0_IOC_GPIO0C_DS2

Address: Operational Base(0xFF080000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio0c5_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x07	gpio0c4_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO0_IOC_GPIO0C_DS3

Address: Operational Base(0xFF080000) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x07	gpio0c7_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio0c6_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO0_IOC_GPIO0D_DS0

Address: Operational Base(0xFF080000) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x07	gpio0d1_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved
7:6	RO	0x0	reserved
5:0	RW	0x07	gpio0d0_ds GPIO PAD Drive Strength control. 6'b000000: Disable 6'b000001: Level 0 6'b000011: Level 1 6'b000111: Level 2 6'b001111: Level 3 6'b011111: Level 4 6'b111111: Level 5 All other setting are reserved

GPIO0_IOC_JTAG_M0_CON

Address: Operational Base(0xFF080000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2:1	RW	0x0	jtag_sel_m0 Switch source when GPIO0d0 and GPIO0d1 switch to JTAG function. 2'b00: connect to CPU 2'b01: connect to BUSMCU 2'b10: connect to PMUMCU 2'b11: Reserved
0	RW	0x1	force_jtag_uart Enable GPIO0d0 and GPIO0d1 switch to JTAG function if uart0_rx low last for a specified period of time. 1'b0: Disable 1'b1: Enable

GPIO0_IOC_UART_IO_CON

Address: Operational Base(0xFF080000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	uart0rx_low_dly uart0_rx low count

GPIO0_IOC_IO_VSEL2

Address: Operational Base(0xFF080000) + offset (0x0148)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RO	0x0	poc_pmuio1_vd PMUIO1 hardware voltage status 1'b0: 1.8V 1'b1: 3.3V
11:5	RO	0x00	reserved
4	RW	0x0	poc_pmuio0_iddq PMUIO0 iddq control 1'b0: Disable 1'b1: Enable
3	RW	0x0	poc_pmuio1_iddq PMUIO1 iddq control 1'b0: Disable 1'b1: Enable
2	RW	0x1	poc_pmuio1_sel33 PMUIO1 3.3V control 1'b0: Disable 1'b1: Enable
1	RW	0x0	poc_pmuio1_sel18 PMUIO1 1.8V control 1'b0: Disable 1'b1: Enable
0	RW	0x0	poc_pmuio1_sel PMUIO1 voltage source select control 1'b0: From hardware 1'b1: From ioc_grf

GPIO0_IOC_XIN_CON

Address: Operational Base(0xFF080000) + offset (0x014C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x1	reserved
2:0	RW	0x7	osc_ds OSC drive strength control

5.12 USBPHY_GRF Register Description

5.12.1 Registers Summary

Name	Offset	Size	Reset Value	Description
GRF_USBPHY_CON0	0x0100	W	0x00000C52	USB PHY control register0
GRF_USBPHY_CON1	0x0104	W	0x000001D2	USB PHY control register1
GRF_USBPHY_CON2	0x0108	W	0x00000000	USB PHY control register2
GRF_USBPHY_CON3	0x010C	W	0x00000000	USB PHY control register3
GRF_USBPHY_INT_MASK	0x0110	W	0x00000000	USB PHY interrupt mask register

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Name	Offset	Size	Reset Value	Description
GRF_USBPHY_INT_STATUS	0x0114	W	0x00000000	USB PHY interrupt status register
GRF_USBPHY_INT_STATUS_CLR	0x0118	W	0x00000000	USB PHY interrupt status clear register
GRF_USBPHY_STATUS	0x0120	W	0x00000000	USB PHY status register
GRF_USBPHY_LS_CON	0x0130	W	0x00030100	USB PHY linestate control register
GRF_USBPHY_DIS_CON	0x0134	W	0x00030100	USB PHY disconnect control register
GRF_USBPHY_BVALID_CON	0x0138	W	0x00030100	USB PHY bvalid control register
GRF_USBPHY_ID_CON	0x013C	W	0x00030100	USB PHY id control register
GRF_USBPHY_CON4	0x0140	W	0x00000000	USB PHY control register4

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.12.2 Detail Registers Description

GRF_USBPHY_CON0

Address: Operational Base(0xFF090000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	usbotg_utmi_dischrgvbus usbotg_utmi_dischrgvbus
12	RW	0x0	usbotg_utmi_chrgvbus usbotg_utmi_chrgvbus
11	RW	0x1	usbotg_utmi_idpullup usbotg_utmi_idpullup
10	RW	0x1	usbotg_utmi_iddig GRF USB OTG Plug iddig Indicator
9	RW	0x0	usbotg_utmi_iddig_sel USB OTG plug indicator output selection 1'b0: Select phy iddig status to controller 1'b1: Select GRF plug iddig indicator to controller
8	RW	0x0	usbotg_utmi_dmpulldown GRF OTG DM pulldown resistor
7	RW	0x0	usbotg_utmi_dppulldown GRF OTG DP pulldown resistor
6	RW	0x1	usbotg_utmi_termselect GRF OTG termination select between FS/LS/HS speed
5:4	RW	0x1	usbotg_utmi_xcvrselect GRF OTG transceiver select between FS/LS/HS speed
3:2	RW	0x0	usbotg_utmi_opmode GRF OTG operational mode selection
1	RW	0x1	usbotg_utmi_suspend_n GRF OTG suspend mode 1'b0: Suspend 1'b1: Normal
0	RW	0x0	usbotg_utmi_sel 1'b0: Select OTG controller utmi interface to phy 1'b1: Select GRF utmi interface to phy

GRF_USBPHY_CON1

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Address: Operational Base(0xFF090000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x1	usbhost_utmi_dmpulldown GRF HOST DM pulldown resistor
7	RW	0x1	usbhost_utmi_dppulldown GRF HOST DP pulldown resistor
6	RW	0x1	usbhost_utmi_termselect GRF HOST termination select between FS/LS/HS speed
5:4	RW	0x1	usbhost_utmi_xcvrselect GRF HOST transceiver select between FS/LS/HS speed
3:2	RW	0x0	usbhost_utmi_opmode GRF HOST operational mode selection
1	RW	0x1	usbhost_utmi_suspend_n GRF HOST suspend mode 1'b0: Suspend 1'b1: Normal
0	RW	0x0	usbhost_utmi_sel 1'b0:Select HOST controller utmi interface to phy 1'b1:Select GRF utmi interface to phy

GRF_USBPHY_CON2

Address: Operational Base(0xFF090000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	bvalid_vbusvalid_sel 1'b0: Select bvalid and vbusvalid of usbphy as bvalid and vbusvalid of usb controller 1'b1: Select value of bvalid_vbusvalid_grf (bit14) as bvalid and vbusvalid of usb controller
14	RW	0x0	bvalid_vbusvalid_grf bvalid_vbusvalid value to usb controller
13	RO	0x0	reserved
12	RW	0x0	vdm_src_en_usbotg open dm voltage source
11	RW	0x0	vdp_src_en_usbotg open dp voltage source
10	RW	0x0	rdm_pdwn_en_usbotg open dm pull down resistor
9	RW	0x0	idp_src_en_usbotg open dm source current
8	RW	0x0	idm_sink_en_usbotg open dm sink current
7	RW	0x0	idp_sink_en_usbotg open dp sink current
6:5	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
4	RW	0x0	usbphy_commononn configure PLL clock output in suspend mode 1'b0:480MHz clock always on 1'b1:480MHz clock will turn off when both ports suspend asserted. If the supsend of any port deassert, it will wait 1ms to make 480MHz clock stable
3	RW	0x0	bypasssel_usbotg bypass select
2	RW	0x0	bypassdmen_usbotg bypass dm enable
1	RW	0x0	usbotg_disable_1 bypass OTG function
0	RW	0x0	usbotg_disable_0 bypass OTG function

GRF_USBPHY_CON3

Address: Operational Base(0xFF090000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	usbphy_hostport_wakeup_irq_en 1'b0:Disable wakeup irq 1'b1:Enable wakeup irq
14	RO	0x0	reserved
13	RW	0x0	usbotg_utmi_chrgvbus USB OTG GRF charge vbus
12	RO	0x0	reserved
11	RW	0x0	usbotg_utmi_drvvbus USB OTG GRF utmi_drvvbus
10	RW	0x0	usbotg_utmi_drvvbus_sel USB OTG utmi_drvvbus_sel bit control 1'b0: Select OTG controller drvvbus to phy 1'b1: Select OTG GRF utmidrvvbus to phy
9	RW	0x0	usbotg_utmi_fs_se0 USB OTG utmi_fs_se0 bit control
8	RW	0x0	usbotg_utmi_fs_data USB OTG utmi_fs_data bit control
7	RW	0x0	usbotg_utmi_fs_oe USB OTG utmi_fs_oe bit control
6	RW	0x0	usbotg_utmi_fs_xver_own USB OTG utmi_fs_xver_own bit control
5:0	RO	0x00	reserved

GRF_USBPHY_INT_MASK

Address: Operational Base(0xFF090000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:8	RW	0x0	host0_disconnect_irq_en host0_disconnect_irq edge status enable 2'bx1: Disconnect rising edge irq status enable 2'b1x: Disconnect falling edge irq status enable
7:6	RW	0x0	otg0_disconnect_irq_en otg0_disconnect_irq edge status enable 2'bx1: Disconnect rising edge irq status enable 2'b1x: Disconnect falling edge irq status enable
5:4	RW	0x0	otg0_id_irq_en otg0_id edge status enable 2'bx1: Id rising edge irq status enable 2'b1x: Id falling edge irq status enable
3:2	RW	0x0	otg0_bvalid_irq_en otg0_bvalid edge status irq enable 2'bx1: Bvalid rising edge irq status enable 2'b1x: Bvalid falling edge irq status enable
1	RW	0x0	host0_linestate_irq_en host0_linestate change status irq enable
0	RW	0x0	otg0_linestate_irq_en otg0_linestate change status irq enable

GRF_USBPHY_INT_STATUS

Address: Operational Base(0xFF090000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RO	0x0	host0_disconnect_irq host0_disconnect edge irq status 2'bx1: Disconnect rising edge irq status 2'b1x: Disconnect falling edge irq status
7:6	RO	0x0	otg0_disconnect_irq otg0_disconnect edge irq status 2'bx1: Disconnect rising edge irq status 2'b1x: Disconnect falling edge irq status
5:4	RO	0x0	otg0_id_irq otg0_id edge irq status 2'bx1: Id rising edge irq status 2'b1x: Id falling edge irq status
3:2	RO	0x0	otg0_bvalid_irq otg0_bvalid edge irq status 2'bx1: Bvalid rising edge irq status 2'b1x: Bvalid falling edge irq status
1	RO	0x0	host0_linestate_irq host0_linestate change irq status
0	RO	0x0	otg0_linestate_irq otg0_linestate change irq status

GRF_USBPHY_INT_STATUS_CLR

Address: Operational Base(0xFF090000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	WO	0x0	host0_disconnect_irq_clr host0_disconnect_irq_clr irq status clear 2'b01: Disconnect rising edge irq status clear 2'b10: Disconnect falling edge irq status clear

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Bit	Attr	Reset Value	Description
7:6	WO	0x0	otg0_disconnect_irq_clr otg0_disconnect_irq_clr irq status clear 2'b01: Disconnect rising edge irq status clear 2'b10: Disconnect falling edge irq status clear
5:4	WO	0x0	otg0_id_irq_clr otg0_id edge irq status clear 2'b01: Id rising edge irq status clear 2'b10: Id falling edge irq status clear
3:2	WO	0x0	otg0_bvalid_irq_clr otg0_bvalid edge irq status clear 2'b01: Bvalid rising edge irq status clear 2'b10: Bvalid falling edge irq status clear
1	WO	0x0	host0_linestate_irq_clr host0_linestate change irq status clear, write 1 to clear irq status
0	WO	0x0	otg0_linestate_irq_clr otg0_linestate change irq status clear, write 1 to clear irq status

GRF_USBPHY_STATUS

Address: Operational Base(0xFF090000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RO	0x0	usbphy_dp_detected usbphy_dp_detected bit status
24	RO	0x0	usbphy_cp_detected usbphy_cp_detected bit status
23	RW	0x0	usbphy_dcp_detected usbphy_dcp_detected bit status
22	RO	0x0	usbhost_phy_ls_fs_rcv host_phy_ls_fs_rcv status
21	RO	0x0	usbhost_utmi_avalid host_utmi_avalid status
20	RO	0x0	usbhost_utmi_bvalid host_utmi_bvalid status
19	RO	0x0	usbhost_utmi_hostdisconnect host_utmi_hostdisconnect status
18	RO	0x0	usbhost_utmi_iddig_o host_utmi_iddig status
17:16	RO	0x0	usbhost_utmi_linestate host_utmi_linestate status
15	RO	0x0	usbhost_utmi_sessend host_utmi_sessend status
14	RO	0x0	usbhost_utmi_vbusvalid host_utmi_vbusvalid status
13	RO	0x0	usbhost_utmi_vmi host_utmi_vmi status
12	RO	0x0	usbhost_utmi_vpi host_utmi_vpi status
11	RO	0x0	usbotg_phy_ls_fs_rcv utmi_phy_ls_fs_rcv_out status
10	RO	0x0	usbotg_utmi_avalid otg_utmi avalid bit status
9	RO	0x0	usbotg_utmi_bvalid otg_utmi bvalid bit status
8	RO	0x0	usbotg_utmi_fs_xver_own OTG utmi_fs_xver_own status

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Bit	Attr	Reset Value	Description
7	RO	0x0	usbotg_utmi_hostdisconnect otg_utmi_hostdisconnect status
6	RO	0x0	usbotg_utmi_iddig usbotg_utmi_iddig status
5:4	RO	0x0	usbotg_utmi_linestate otg_utmi_linestate status
3	RO	0x0	usbotg_utmi_sessend otg_utmi_sessend bit status
2	RO	0x0	usbotg_utmi_vbusvalid otg_utmi_vbusvalid bit status
1	RO	0x0	usbotg_utmi_vmi otg_utmi_vmi bit status
0	RO	0x0	usbotg_utmi_vpi otg_utmi_vpi bit status

GRF_USBPHY_LS_CON

Address: Operational Base(0xFF090000) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x30100	linestate_filter_con host/otg port linestate filter time control register. Unit:Pclk(up to 100MHz)

GRF_USBPHY_DIS_CON

Address: Operational Base(0xFF090000) + offset (0x0134)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x30100	disconnect_filter_con host/otg port hostdisconnect filter time control register. Unit:Pclk(up to 100MHz)

GRF_USBPHY_BVALID_CON

Address: Operational Base(0xFF090000) + offset (0x0138)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x30100	bvalid_filter_con otg port bvalid filter time control register. Unit:Pclk(up to 100MHz)

GRF_USBPHY_ID_CON

Address: Operational Base(0xFF090000) + offset (0x013C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0030100	id_filter_con otg ID port filter time control register. Unit:Pclk(up to 100MHz)

GRF_USBPHY_CON4

Address: Operational Base(0xFF090000) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	usbotg_utmi_suspend_n usbotg_utmi_suspend_n GRF value
5	RW	0x0	usbotg_utmi_suspend_sel1 1'b0:grf_usbphy_con4[6] 1'b1:Usbotg_utmi_suspend_n & usbotg_utmi_l1_suspend_n

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Bit	Attr	Reset Value	Description
4	RW	0x0	usbotg_utmi_suspend_sel0 1'b0:~usbotg_utmi_suspend_com_n & ~usbotg_utmi_l1_suspend_com_n 1'b1:grf_usbphy_con4[5]?(usbotg_utmi_suspend_n & sbotg_utmi_l1_suspend_n) :grf_usbphy_con4[6];
3:0	RO	0x0	reserved

5.13 PIPEPHY_GRF Register Description

5.13.1 Registers Summary

Name	Offset	Size	Reset Value	Description
GRF_PIPEPHY_PIPE_CON0	0x0000	W	0x00000110	PIPE Combo PHY Configuration Register 0
GRF_PIPEPHY_PIPE_CON1	0x0004	W	0x00000000	PIPE Combo PHY Configuration Register 1
GRF_PIPEPHY_PIPE_CON2	0x0008	W	0x00009401	PIPE Combo PHY Configuration Register 2
GRF_PIPEPHY_PIPE_CON3	0x000C	W	0x00000402	PIPE Combo PHY Configuration Register 3
GRF_PIPEPHY_PIPE_CON4	0x0010	W	0x00000000	PIPE Combo PHY Configuration Register 4
GRF_PIPEPHY_PIPE_STATUS1	0x0034	W	0x000000C0	PIPE Combo PHY Status Register1
GRF_PIPEPHY_LFPS_DET_CON	0x0080	W	0x00000009	PIPE Combo PHY LFPS Detect Control Register
GRF_PIPEPHY_PHY_INT_EN	0x00A0	W	0x00000000	PIPE Combo PHY Interrupt Signal Enable
GRF_PIPEPHY_PHY_INT_STATUS	0x00A4	W	0x00000000	PIPE Combo PHY Interrupt Status

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

5.13.2 Detail Registers Description

GRF_PIPEPHY_PIPE_CON0

Address: Operational Base(0xFF098000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14	RW	0x0	pipe_rxstandby SATA mode Controls whether the PHY RX is active when the PHY is in any power state with PCLK on. RX_STANDBY is ignored when the PHY is in any power state where the high-speed receiver is always off. 1'b0: Active 1'b1: Standby PCIe mode Controls whether the PHY RX is active when the PHY is in P0 or P0s. RX_STANDBY is ignored when the PHY is in P1 or P2. 1'b0: Active 1'b1: Standby Only used in SATA and PCIe mode. USB3.0 mode should be tied to 1'b0. The value when override enable is selected.
13	RW	0x0	pipe_rxelecidle_disable RX electrical idle detect disable. The value when override enable is selected. 1'b0: Idle detect enable 1'b1: Idle detect disable
12	RW	0x0	pipe_rxterm Control presence of receiver terminations. The value when override enable is selected. 1'b0: Termination removed 1'b1: Termination present Only used in USB3.0 mode, PCIe and SATA mode should be tied to 1'b1.
11	RW	0x0	pipe_bypass_codec PCIe mode, USB mode, and SATA mode. The value when override enable is selected. Controls whether the PHY performs 8b/10b encode and decode. 1'b0: 8b/10b encode/decode performed normally by the PHY 1'b1: 8b/10b encode/decode bypassed, 20bit 8b/10b encode/decode bypass mode works only when BUS_WIDTH=2'b01 It should be tie to 1'b1 in SATA low latency and SERDES mode.
10	RW	0x0	pipe_ebuffmode RX Elasticity Buffer operating mode selection. The value when override enable is selected. 1'b0: Nominal half-full buffer mode 1'b1: Nominal empty buffer mode In SATA and USB3.0 mode, when RX elastic buffer is operating at nominal empty buffer mode, RX_DATA_VALID is de-asserted which means elastic buffer is empty and no data is available. In PCIe mode, only nominal half-full Elasticity Buffer mode is supported.

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Bit	Attr	Reset Value	Description
9	RW	0x0	pipe_l1sub_entreq In PCIe mode L1 sub-state entry request signal in PCIe mode. When set to high, it instructs PHY to do power transition to L1 sub-state. In SATA Mode When set to high, it will be power down PLL. This signal could be connected to the L1 sub-state enable/request signal from controller Only used in PCIe and SATA mode, USB mode should be tied to 1'b0. The value when override enable is selected. Reserved for current chip.
8	RW	0x1	pipe_mac_pclkreq_n PCIe common clock request signal in PCIe mode. The signal shall be low and CKREF_SRC[1:0] is set to 2'b10 when CKREFP/N and PCI_100M_CLK output from PHY is used for PCIe system with common clock Note: Details refer to CKREFP/N and PCI_100M_CLK. Only used in PCIe mode, USB and SATA mode should be tied to 1'b1. This bit is a override bit for input CLKREQ for PHY when override selection enable.
7:6	RW	0x0	pipe_powerdown Power up or power down status control of Transceiver. If PIPE PHY support PIPE4.3, the powerdown is 4-bit, PIPE4.2 or below 2-bit. This filed is powerdown [1:0], powerdown[3:2] is controlled by pipe_powerdown_4p3. The value when override enable is selected. In PCIe mode 4'h0: P0, normal mode 4'h1: P0s, low recovery time latency, power saving state 4'h2: P1, longer recovery time latency, lower power saving 4'h3: P2, lowest power state 4'h4: P1.CPM 4'h5: P1.1 4'hc: P1.2 Others: Reserved In USB3.0 mode 4'h0: P0, normal mode 4'h1: P1, low recovery time latency, power saving state 4'h2: P2, longer recovery time latency, lower power saving 4'h3: P3, lowest power state Others: Reserved In SATA and Serdes mode 4'h0: POWER_STATE_0 operational state, PHY normal operation 4'h1: PCLK on, TX common mode on 4'h3: PCLK on, TX common mode off 4'h5: PCLK off, TX common mode on 4'h7: PCLK off, TX common mode off Others: Reserved

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Bit	Attr	Reset Value	Description
5:4	RW	0x1	pipe_rate Combo PHY link signaling rate. The value when override enable is selected. In PCIe mode 2'b00: 2.5GT/s 2'b01: 5.0GT/s Others: Reserved In USB3.0 mode 2'b00: 5GT/s Others: Reserved In SATA mode 2'b00: 1.5GT/s 2'b01: 3.0GT/s 2'b10: 6.0GT/s 2'b11: Reserved In SERDES(QSGMII/SGMII) mode 2'b00: 1.25Gbps 2'b01: Reserved 2'b10: 5.0Gbps 2'b11: Reserved
3:2	RW	0x0	pipe_phymode Combo PHY mode. 2'b00: PCIe 2'b01: USB3 2'b10: SATA 2'b11: Serdes
1:0	RW	0x0	pipe_databuswidth Combo PHY PIPE data bus width. The value when override enable is selected. 2'b00: 32-bit, PCIe and USB3 only support 32-bit 2'b01: Reserved 2'b10: Reserved 2'b11: Reserved

GRF_PIPEPHY_PIPE_CON1

Address: Operational Base(0xFF098000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:13	RW	0x0	phy_clk_sel Combo Phy PIPE reference clock frequency selection. 2'b00: 24M 2'b01: 25M 2'b10: 100M 2'b11: Reserved

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Bit	Attr	Reset Value	Description
12:11	RW	0x0	pipe_txpattern_sata Controls which pattern the PHY sends at the Gen 1 rate when sending OOB or initialization signaling. The PHY transmits this pattern at the Gen 1 rate regardless of what rate the PHY is configured at. Used in SATA mode only. The value when override enable is selected. 2'b00: C ALIGN 2'b01: C D24.3 2'b10: C D10.2 2'b11: C Reserved
10:8	RW	0x0	pipe_txmargin Transmit margin control, combined with txswing to control TX output amplitude. The value when override enable is selected.
7:6	RW	0x0	pipe_txdeemph Transmitter de-emphasis level configuration. The value when override enable is selected. 2'b00: -6dB 2'b01: -3.5dB 2'b10: No de-emphasis 2'b11: Reserved
5	RW	0x0	pipe_txswing Control transmitter voltage swing level. The value when override enable is selected. 1'b0: Full swing 1'b1: Low swing
4	RW	0x0	pipe_txcompliance Set the running disparity to negative. Only used in PCIe mode, USB and SATA mode should be tied to 1'b0. The value when override enable is selected.
3	RW	0x0	pipe_txcommonmode_disable TX Common mode Control. 1'b0: Enable 1'b1: Disable The value when override enable is selected.
2	RW	0x0	pipe_txoneszeros This signal is used in USB3.0 mode for transmitting compliance pattern CP7 and CP8. When set to high, it causes the transmitter to transmit an alternating sequence of 0s and 1s, regardless the states of TX_DATA. Only used in USB mode, PCIE and SATA mode should be tied to 1'b0. The value when override enable is selected.
1	RW	0x0	pipe_txelecidle Forces TX output to electrical idle when asserted except in loopback, refer to PIPE spec for details on control signal usage. When asserted with TX_COMPLIANCE high, the PHY is fully powered off. Shall be kept high when SATA mode that is not in P0. The value when override enable is selected.
0	RW	0x0	pipe_txdectrx_loopback Used to tell the PHY to begin a receiver detection operation or to begin loopback. Refer to s PIPE spec for detail description. This signal shall be set to low when SATA mode that is not in P0. The value when override enable is selected.

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GRF_PIPEPHY_PIPE_CON2

Address: Operational Base(0xFF098000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	sel_pipe_txcompliance pipe_txcompliance selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
14	RW	0x0	sel_pipe_txcommonmode_disable pipe_txcommonmode_disable selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
13	RW	0x0	sel_pipe_txoneszeros pipe_txoneszeros selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
12	RW	0x1	sel_pipe_txelecidle pipe_txelecidle selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
11	RW	0x0	sel_pipe_txdectrx_loopback pipe_txdectrx_loopback selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
10	RW	0x1	sel_pipe_rxstandby sel_pipe_rxstandby selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
9	RW	0x0	sel_pipe_rxelecidle_disable pipe_rxelecidle_disable selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
8	RW	0x0	sel_pipe_rxterm pipe_rxterm selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
7	RW	0x0	sel_pipe_bypass_codec pipe_bypass_codec selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF

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Bit	Attr	Reset Value	Description
6	RW	0x0	sel_pipe_ebuffmode pipe_ebuffmode selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
5	RW	0x0	sel_pipe_l1sub_entreq pipe_l1sub_entreq selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
4	RW	0x0	sel_pipe_powerdown pipe_powerdown selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
3	RW	0x0	sel_pipe_mac_pclkreq_n pipe_mac_pclkreq_n selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
2	RW	0x0	sel_pipe_rate pipe_rate selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
1	RW	0x0	sel_pipe_phymode pipe_phymode selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF Reserved
0	RW	0x1	sel_pipe_databuswidth pipe_databuswidth selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF

GRF_PIPEPHY_PIPE_CON3

Address: Operational Base(0xFF098000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	qsgm_mode QSGMII mode enable. 1'b0: Other mode 1'b1: QSGMII/SGMII mode Reserved in this chip
14:13	RW	0x0	pipe_sel For Combo PIPE PHY2 2'b00: Connect to PCIe 2.0 Controller 2'b01: Connect to USB 3.0 Controller Others: Reserved
12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11	RW	0x0	sel_clkreq CLKREQ for PIPE PHY source selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side(Controller/Constant/PD GRF/PHY GRF) 1'b1: From GPIO mux for CLKREQ_N Because the CLKREQ is valid when high, so the pipe_mac_pclkreq_n should set to "0" when sel_pipe_mac_pclkreq_n is set to "1".
10	RW	0x1	sel_rxelecidle Rxelecidle to controller source selection. Override value is selected for PIPE PHY interface. 1'b0: From PIPE PHY 1'b1: When rxelecidle_disable is high, rxelecidle return "1" to controller
9:8	RW	0x0	phy_clk_ref_src Combo PHY PIPE reference clock source selection. 2'b00: Use PLL_CKREF_INNER as reference clock source, CKREFP/N is not active, the PAD can be floating 2'b01: Use CKREFP/N as input reference clock source 2'b10: Use PLL_CKREF_INNER (From SoC CRU) as reference clock source, Use CKREFP/N as output clock to provide a differential 100M reference clock in PCIe mode while PIPE PHY CLKREQ is high. 2'b11: Not allowed
7:4	RO	0x0	reserved
3	RW	0x0	sel_pipe_txpattern_sata pipe_txpattern_sata selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
2	RW	0x0	sel_pipe_txmargin pipe_txmargin selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
1	RW	0x1	sel_pipe_txdeemph pipe_txdeemph selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
0	RW	0x0	sel_pipe_txswing pipe_txswing selection. Override value is selected select for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF

GRF_PIPEPHY_PIPE_CON4

Address: Operational Base(0xFF098000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	pipe_txdeemph_ext Extra direct control the txdeemph bit3.

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	bist_mode BIST mode test in normal operation. 4'h0: PHY Normal operation, default value of BIST_MODE 4'h8: PHY external BIST from TXP/TXN to RXP/RXN 4'h9: PHY internal BIST 4'ha: PHY send 1'b0 on TXP and 1'b1 on TXN (only for VOL test) 4'hc: PHY send 1'b1 on TXP and 1'b0 on TXN (only for VOH test) 4'he: PHY send D10.2 (only for Eye-Diagram test) Others: Reserved
3:0	RO	0x0	reserved

GRF_PIPEPHY_PIPE_STATUS1

Address: Operational Base(0xFF098000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RO	0x0	pipe_clkreq_n Indicates that the PHY is in corresponding state to L1-sub-state in PCIE mode, during which PHY reference clock could be turned off. This signal could connect to corresponding signal in controller IP, if applicable.
8	RO	0x0	pipe_power_presetn Reserved
7	RO	0x1	pipe_rxelecidle_o Indicates receiver detection of an electrical idle. When de-asserted with the PHY in P2 (PCIE Mode), indicates a detection of beacon, while indicate exit from electrical idle in other power states in PCIe mode. In USB3.0 mode, it indicates the detection of LFPS. In SATA mode, it indicates if there is no data/OOB received.
6	RO	0x1	pipe_phystatus_o Used to communicate completion of several PHY functions including power management state transitions, rate change and receiver detection.
5:3	RO	0x0	pipe_rxstatus_o PIPE PHY receiver status. Encode receiver status and error codes for the received data stream when receiving data. 3'b000: Received data OK 3'b001: PCIe mode, 1 SKP added; USB mode: 1 SKP added; SATA mode: 1 ALIGN added Asseted width first byte of Align that was added 3'b010: PCIe mode: 1 SKP Ordered set removed; 1 SKP Ordered Set removed; SATA mode: 1 or more ALIGNs 3'b011: PCIe and USB mode: Receiver detected 3'b100: 8B/10B decode error 3'b101: Elastic buffer overflow 3'b110: Elastic buffer under flow, this error code is not used if the elastic buffer is operating in the nominal buffer empty mode 3'b111: Receive disparity error, overwritten by decode error
2:0	RO	0x0	reserved

GRF_PIPEPHY_LFPS_DET_CON

Address: Operational Base(0xFF098000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x09	lfps_detect_con LFPS Detect Count Filter Control. This counter determines whether a rxelecidle (high pulse) is valid or not. The counter is based on Combo PIPE PHY APB PCLK.

GRF_PIPEPHY_PHY_INT_EN

Address: Operational Base(0xFF098000) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	rxelecidle_l0_fall_irq_en rxelecidle_l0_fall irq enable. 1'b0: IRQ disable 1'b1: IRQ enable

GRF_PIPEPHY_PHY_INT_STATUS

Address: Operational Base(0xFF098000) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1C	0x0	rxelecidle_l0_fall_irq_st rxelecidle_l0_fall irq status. 1'b0: Interrupt inactive 1'b1: Interrupt active

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Chapter 6 CPU (Cortex-A53)

6.1 Overview

The RK3562 has a quad-core Cortex-A53 cluster with 512K L2 memory. Cortex-A53 processor, which is a mid-range, low-power processor that implements the ARMv8-A architecture.
The Cortex-A53 processor includes following features:

- Full implementation of the ARMv8-A architecture instruction set
- Support for both AArch32 and AArch64 Execution status.
- Support for all exception levels, EL0, EL1, EL2, and EL3, in each execution states.
- Support A32 instruction set, previously called the ARM instruction set.
- Support T32 instruction set, previously called the Thumb instruction set.
- Support A64 instruction set.
- In-order pipeline with symmetric dual-issue of most instructions.
- Harvard Level 1(L1) memory system with a Memory Management Unit (MMU).
- Level 2(L2) memory system providing cluster memory coherency, with L2 cache.
- Support advanced SIMD and Floating-point Extension for integer and floating-point vector operations.
- Support ARMv8 Cryptography Extensions.
- Support AMBA 4 ACE bus architecture.

The configuration details of cluster are shown in following tables

Table 6-1 CPU Configuration

Number of CPU	4
L1 I cache size	32K
L1 D cache size	32K
L2 cache size	512K
L2 data RAM output latency	3 cycles
L2 data RAM input latency	3 cycles
CPU cache protection	No
SCU L2 cache protection	No
BUS master interface	ACE
NEON and floating point support	Yes
Cryptography extension	Yes

6.2 Block Diagram

The Cortex-A53 sub system is shown as below. As illustrated, dual-core Cortex-A53 connects to system bus through asynchronous bridges which can handle with CDC(clock domain crossing) issue.
The Cortex-A53 is connected with system counter, which can run under a constant frequency clock, for PPI interrupt generation.

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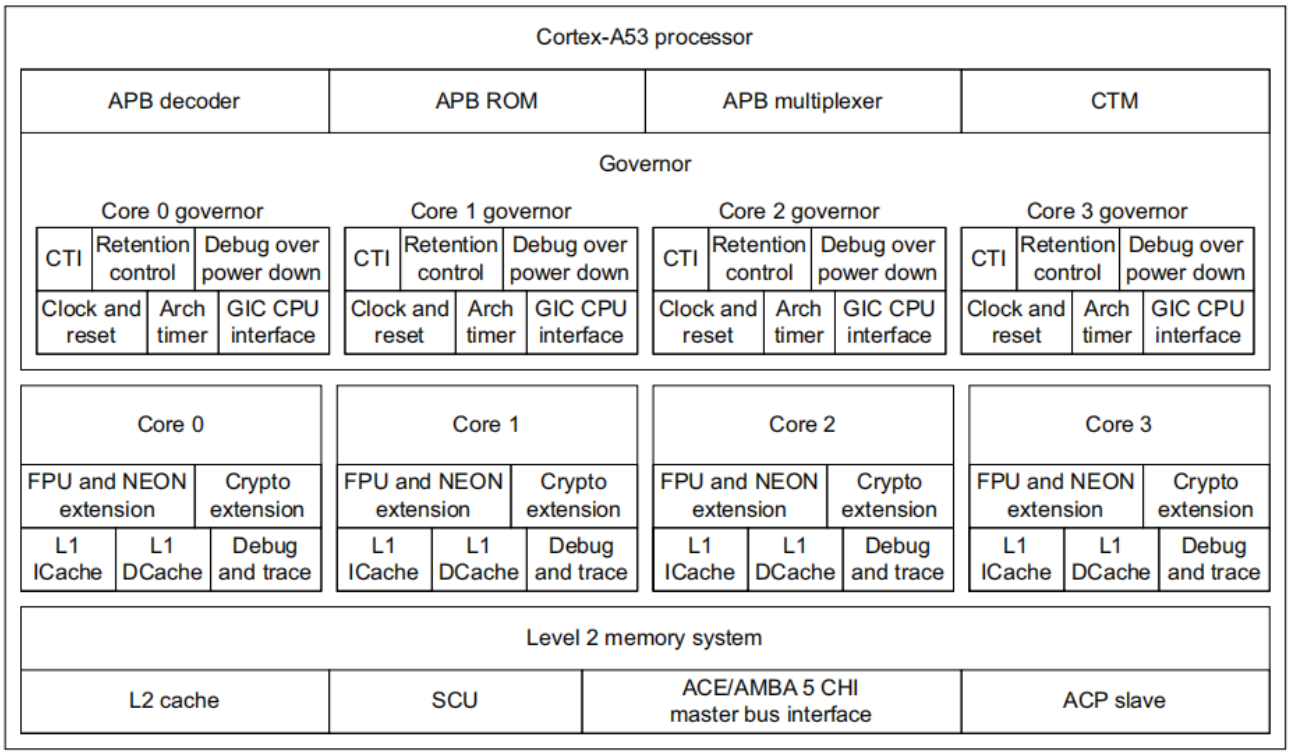


Fig.6-1 Block Diagram

6.3 Function Description

Please refer to the document cortex_a53_r0p4_trm.pdf for the detail function description.

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Chapter 7 Generic Interrupt Controller (GIC)

7.1 Overview

There is a generic interrupt controller (GIC400) in RK3562 which generates physical interrupts to Cortex-A53. It has two interfaces, the distributor interface connects to the interrupt source, and the CPU interface connects to Cortex-A53. The details of CPU interface connectivity are shown in the following table.

Table 7-1 CPU Interface Connectivity

CPU Interface Number	Connectivity
CPU interface 0	CPU0
CPU interface 1	CPU1
CPU interface 2	CPU2
CPU interface 3	CPU3

It supports the following features:

- Support 256 hardware interrupt inputs
- Support masking of any interrupts
- Support interrupts prioritization
- Support distribution of the interrupts to the target Cortex-A53 processor(s)
- Support generation of interrupts by software
- Support security extensions
- Support virtual extension

7.2 Block Diagram

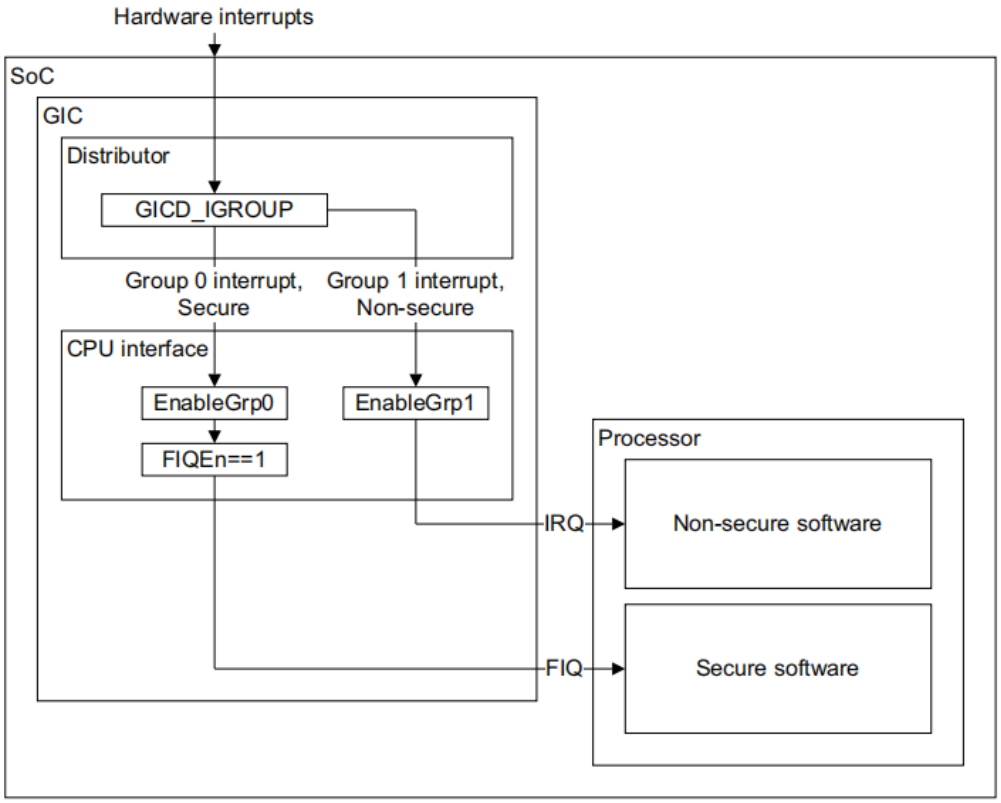


Fig.7-1 GIC Block Diagram

7.3 Function Description

Please refer to the document IHI0048B_gic_architecture_specification.pdf and GIC400_Technical_Reference_Manual.pdf for the detail function description.

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Chapter 8 Graphics Process Unit (GPU)

8.1 Overview

The Mali-Gondul GPU is a graphics acceleration platform that is based on open standards. It supports 2D graphics, 3D graphics, and General Purpose computing on GPU (GPGPU).
The GPU hardware and software support compute standards and graphics API standards.
The GPU supports these compute API standards:

- OpenCL 2.0 Full Profile.

The GPU supports these graphics API standards:

- OpenGLES 1.1, 2.0, and 3.2.
- Vulkan 1.0 and 1.1.

The Arm Mali-Gondul GPU has significant features and properties.

- Compressed texture formats.
- Arm Frame Buffer Compression (AFBC) 1.2
- 8-bit, 10-bit and 16-bit YUV input and output formats
- L2 cache:128KB
- Support one Shader core and two execution engines

8.2 Block Diagram

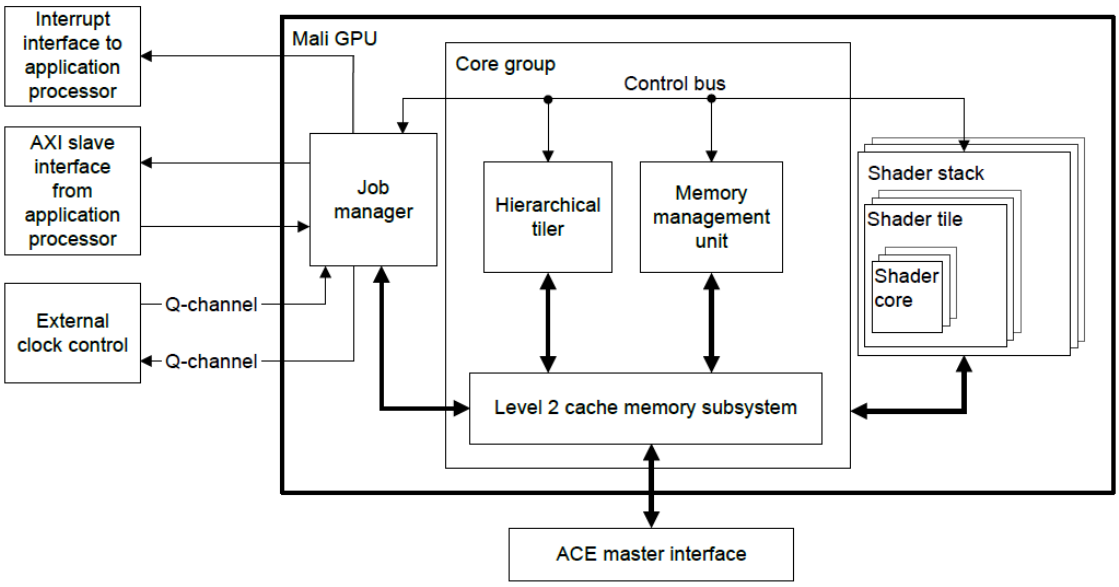


Fig.8-1 GPU Architecture

8.3 Function Description

Please refer to the document "ARM_Gondul_r1p0_00eac0_TechnicalReferenceManual.pdf" for the GPU detail description.

8.4 Register Description

Please refer to the document "ARM_Gondul_r1p0_00eac0_TechnicalReferenceManual.pdf" for the GPU detail description.

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Chapter 9 RKNN

9.1 Overview

The RKNN is a specialized hardware accelerator designed to accelerate AI (artificial intelligence) applications, including machine vision and natural language processing. Typical applications include algorithms for gesture and body tracking, image classification, video surveillance, automatic speech recognition (ASR) and advanced driver assistance systems (ADAS).

RKNN supports the following features:

- AHB interface used for register configuration, only supports single transaction
- AXI interface used to fetch data from memory
- NSP slave interface used to access internal buffer directly from bus
- Support integer 8bit, integer 16bit, float point 16bit, bfloat point 16bit and tensor float 32bit convolution operation
- Support integer 4bit, integer 8bit, integer 16bit, float point 16bit, bfloat point 16bit and tf32bit network model
- 256 integer 16bit MAC operations per cycle
- 256 float point 16bit MAC operations per cycle
- 256 bfloat point 16bit MAC operations per cycle
- 128 tf32bit MAC operations per cycle
- 512 integer 8 MAC operations per cycle
- 256KB internal buffer
- support creating simple custom operators
- Inference Engine: TensorFlow, Caffe, Tflite, Pytorch, Onnx NN, Android NN, etc.

9.2 Block Diagram

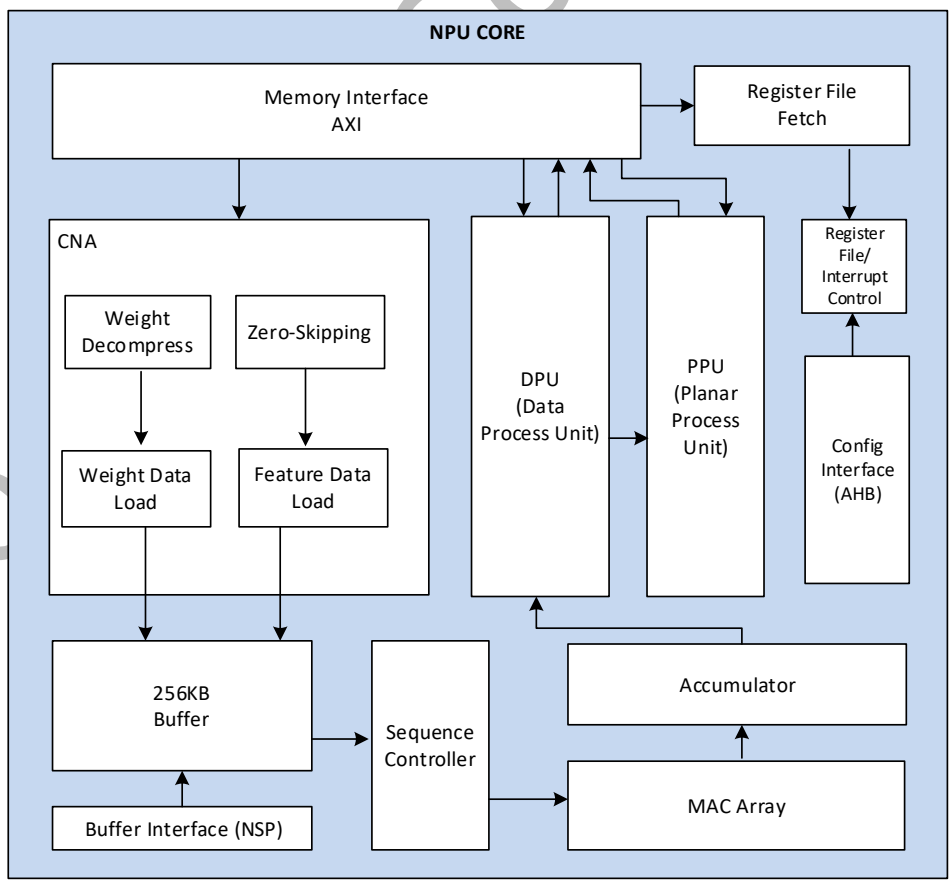


Fig.9-1 RKNN Block Diagram

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9.3 Function Description

9.3.1 AHB/AXI/NSP Interface

The AXI master interface is used to fetch data from memory that is attached to the Soc AXI interconnect.
The AHB slave interface is used to access registers for configuration, debug and test.
The NSP Interface makes it possible for other components on the chip to access CBUF directly.

9.3.2 Neural Network Accelerating Engine

As the unit's name, this engine is the main process unit for Neural Network arithmetic. This unit include convolution pre-process controller, internal buffer, mac array, accumulator. It provides parallel convolution MAC for recognition functions and int4, int8, int16, fp16, bfloat16 and tf32 are supported.

9.3.3 Data Processing Unit

Data Processing Unit mainly process single data calculation, such as leaky_relu, relu, relux, sigmoid, tanh…etc. It also provides function: softmax, transpose, data format conversion, …etc.

9.3.4 Planar Processing Unit

Planar Processing Unit mainly provides planar function to output data from Data Processing Unit. Average pooling, max pooling and min pooling functions are supported.

9.3.5 Register File Fetch Unit

Register File Fetch Unit fetch register configuration from external system memory through AXI interface.

9.4 Register Description

9.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Table 9-1 RKNN Address Mapping

Base Address[15:12]	Device	Address Length	Offset Address Range
4'h0	PC	4K BYTE	0x0000 ~ 0x0fff
4'h1	CNA	4K BYTE	0x1000 ~ 0x1fff
4'h3	CORE	4K BYTE	0x3000 ~ 0x3fff
4'h4	DPU	4K BYTE	0x4000 ~ 0x4fff
4'h5	DPU_RDMA	4K BYTE	0x5000 ~ 0x5fff
4'h6	PPU	4K BYTE	0x6000 ~ 0x6fff
4'h7	PPU_RDMA	4K BYTE	0x7000 ~ 0x7fff
4'h8	DDMA	4K BYTE	0x8000 ~ 0x8fff
4'h9	SDMA	4K BYTE	0x9000 ~ 0x9fff
4'hf	GLOBAL	4 BYTE	0xf000 ~ 0xf004

9.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
PC_pc_operation_enable	0x0008	W	0x00000000	Operation Enable
PC_pc_base_address	0x0010	W	0x00000000	PC address register
PC_pc_cmd_amounts	0x0014	W	0x00000000	Register amount for each task
PC_pc_interrupt_mask	0x0020	W	0x0001FFFF	Interrupt Mask
PC_pc_interrupt_clear	0x0024	W	0x00000000	Interrupt clear
PC_pc_interrupt_status	0x0028	W	0x00000000	Interrupt status

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Name	Offset	Size	Reset Value	Description
PC_pc_interrupt_raw_status	0x002C	W	0x00000000	Interrupt raw status
PC_pc_task_con	0x0030	W	0x00000000	Task control register
PC_pc_task_dma_0_base_addr	0x0034	W	0x00000000	Task Base address
PC_pc_task_dma_1_base_addr	0x0038	W	0x00000000	
PC_pc_task_dma_2_base_addr	0x003C	W	0x00000000	
PC_pc_task_dma_3_base_addr	0x0040	W	0x00000000	
PC_pc_task_dma_base_sel	0x0044	W	0x00000000	
PC_pc_task_status	0x0048	W	0x00000000	Task status register
CNA_cna_s_status	0x1000	W	0x00000000	Single register group status
CNA_cna_s_pointer	0x1004	W	0x00000000	Single register group pointer
CNA_cna_operation_enable	0x1008	W	0x00000000	Operation Enable
CNA_cna_conv_con1	0x100C	W	0x00000000	Convolution control register1
CNA_cna_conv_con2	0x1010	W	0x00000000	Convolution control register2
CNA_cna_conv_con3	0x1014	W	0x00000000	Convolution control register3
CNA_cna_conv_con4	0x1018	W	0x00000000	
CNA_cna_weight_size0	0x101C	W	0x00000000	Weight size control 0
CNA_cna_weight_size1	0x1020	W	0x00000000	Weight size control 1
CNA_cna_weight_size2	0x1024	W	0x00000000	Weight size control 2
CNA_cna_data_size1	0x1028	W	0x00000000	Feature data size control register1
CNA_cna_data_size0	0x102C	W	0x00000000	Feature data size control register0
CNA_cna_data_size2	0x1030	W	0x00000000	Feature data size control register2
CNA_cna_data_size3	0x1034	W	0x00000000	Feature data size control register3
CNA_cna_cbuf_con0	0x1038	W	0x00000000	CBUF control register 0
CNA_cna_cbuf_con1	0x103C	W	0x00000000	CBUF control register 1
CNA_cna_cbuf_con2	0x1040	W	0x00000000	
CNA_cna_cbuf_con3	0x1044	W	0x00000000	
CNA_cna_cvt_con0	0x1048	W	0x00000000	Input convert control register0
CNA_cna_cvt_con1	0x104C	W	0x00000000	Input convert control register1
CNA_cna_cvt_con2	0x1050	W	0x00000000	Input convert control register2
CNA_cna_cvt_con3	0x1054	W	0x00000000	Input convert control register3
CNA_cna_cvt_con4	0x1058	W	0x00000000	Input convert control register4
CNA_cna_cvt_con5	0x105C	W	0x00000000	Input convert control register5
CNA_cna_cvt_con6	0x1060	W	0x00000000	Input convert control register5
CNA_cna_cvt_con7	0x1064	W	0x00000000	Input convert control register5
CNA_cna_cvt_con8	0x1068	W	0x00000000	Input convert control register5
CNA_cna_fc_con0	0x106C	W	0x00000000	Full connected control register0
CNA_cna_fc_con1	0x1070	W	0x00000000	Full connected control register1
CNA_cna_fc_con2	0x1074	W	0x00000000	Full connected control register2
CNA_cna_fc_data_size0	0x1078	W	0x00000000	
CNA_cna_fc_data_size1	0x107C	W	0x00000000	
CNA_cna_pad_con0	0x1080	W	0x00000000	Pad control register0
CNA_cna_pad_con1	0x1084	W	0x00000000	Pad controller register1
CNA_cna_feature_data_addr	0x1088	W	0x00000000	Base address for input feature data
CNA_cna_dma_con0	0x108C	W	0x00000000	AXI control register 0
CNA_cna_dma_con1	0x1090	W	0x00000000	AXI control register 1

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Name	Offset	Size	Reset Value	Description
CNA_cna_dma_con2	0x1094	W	0x00000000	AXI control register 2
CNA_cna_dma_con3	0x1098	W	0x00000000	
CNA_cna_clk_gate	0x109C	W	0x00000000	Clock gating control register
CNA_cna_dcomp_ctrl	0x10A0	W	0x00000000	Weight decompress control register
CNA_cna_dcomp_regnum	0x10A4	W	0x00000000	Weight decompress register number
CNA_cna_dcomp_addr0	0x10A8	W	0x00000000	Base address of the weight
CNA_cna_dcomp_amount0	0x10AC	W	0x00000000	Amount of the weight decompress for the 0 decompress
CNA_cna_dcomp_amount1	0x10B0	W	0x00000000	Amount of the weight decompress for the 1 decompress
CNA_cna_rsp_amount	0x10B4	W	0x00000000	
CORE_core_s_status	0x3000	W	0x00000000	Single register group status
CORE_core_s_pointer	0x3004	W	0x00000000	Single register group pointer
CORE_core_operation_enable	0x3008	W	0x00000000	Operation Enable
CORE_core_misc_cfg	0x300C	W	0x00000000	Misc configuration register
CORE_core_dataout_size_0	0x3010	W	0x00000000	Feature size register 0 of output
CORE_core_dataout_size_1	0x3014	W	0x00000000	Feature size register 1 of output
CORE_core_clip_truncate	0x3018	W	0x00000000	Shift value register
DPU_dpu_s_status	0x4000	W	0x00000000	Single register group status
DPU_dpu_s_pointer	0x4004	W	0x00000000	Single register group pointer
DPU_dpu_operation_enable	0x4008	W	0x00000000	Operation Enable
DPU_dpu_feature_mode_cfg	0x400C	W	0x00000000	Configuration of the feature mode
DPU_dpu_data_format	0x4010	W	0x00000000	Configuration of the data format
DPU_dpu_offset_pend	0x4014	W	0x00000000	Value of the offset pend
DPU_dpu_dst_base_addr	0x4018	W	0x00000000	Destination base address
DPU_dpu_dst_surf_stride	0x401C	W	0x00000000	Destination surface size
DPU_dpu_data_cube_width	0x4020	W	0x00000000	Width of the input cube
DPU_dpu_data_cube_height	0x4024	W	0x00000000	Height of the input cube
DPU_dpu_data_cube_notch_addr	0x4028	W	0x00000000	Notch signal of the input cube
DPU_dpu_data_cube_channel	0x402C	W	0x00000000	Channel of the input cube
DPU_dpu_wdma_size_0	0x4030	W	0x00000000	Size 0 of the WDMA
DPU_dpu_wdma_size_1	0x4034	W	0x00000000	Size 1 of the WDMA
DPU_dpu_bs_cfg	0x4038	W	0x00000000	Configuration of the BS
DPU_dpu_bs_alu_cfg	0x403C	W	0x00000000	Configuration of the BS ALU
DPU_dpu_bs_alu1_cfg	0x4040	W	0x00000000	
DPU_dpu_bs_mul_cfg	0x4044	W	0x00000000	Configuration of the BS MUL
DPU_dpu_bs_rlu_cfg	0x4048	W	0x00000000	Value of the RELUX compare with
DPU_dpu_bs_rlu1_cfg	0x404C	W	0x00000000	
DPU_dpu_bs_ow_cfg	0x4050	W	0x00000000	Configuration of the BS OW
DPU_dpu_bs_ow_op	0x4054	W	0x00000000	Ow op of the BS OW
DPU_dpu_bs_relu_val_0	0x4058	W	0x00000000	
DPU_dpu_bs_relu_val_1	0x405C	W	0x00000000	

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Name	Offset	Size	Reset Value	Description
DPU_dpu_bn_cfg	0x4060	W	0x00000000	Configuration of BN
DPU_dpu_bn_alu_cfg	0x4064	W	0x00000000	
DPU_dpu_bn_mul_cfg	0x4068	W	0x00000000	Configuration of the BN MUL
DPU_dpu_bn_rlu_cfg	0x406C	W	0x00000000	Value of the RELUX compare with
DPU_dpu_bn_rlu1_cfg	0x4070	W	0x00000000	
DPU_dpu_bn_relu_val_0	0x4074	W	0x00000000	
DPU_dpu_bn_relu_val_1	0x4078	W	0x00000000	
DPU_dpu_ew_cfg	0x407C	W	0x00000000	Configuration of EW
DPU_dpu_ew_cvt_offset_value	0x4080	W	0x00000000	Offset of the EW input convert
DPU_dpu_ew_cvt_scale_value	0x4084	W	0x00000000	Scale of the EW input convert
DPU_dpu_ew_rlu_cfg	0x4088	W	0x00000000	Value of the RELUX compare with
DPU_dpu_ew_rlu1_cfg	0x408C	W	0x00000000	
DPU_dpu_ew_operand	0x4090	W	0x00000000	Configure operand0 of the EW
DPU_dpu_ew_con_value_a_l	0x4094	W	0x00000000	
DPU_dpu_ew_con_value_a_h	0x4098	W	0x00000000	
DPU_dpu_ew_con_value_b_l	0x409C	W	0x00000000	
DPU_dpu_ew_con_value_b_h	0x40A0	W	0x00000000	
DPU_dpu_ew_relu_val_0	0x40A4	W	0x00000000	
DPU_dpu_ew_relu_val_1	0x40A8	W	0x00000000	
DPU_dpu_out_cvt_offset	0x40AC	W	0x00000000	Offset of the output converter
DPU_dpu_out_cvt_scale	0x40B0	W	0x00000000	Scale of the output converter
DPU_dpu_out_cvt_shift	0x40B4	W	0x00000000	Shift of the output converter
DPU_dpu_surface_add	0x40B8	W	0x00000000	Value of the surface adder
DPU_dpu_perf_en	0x40BC	W	0x00000000	
DPU_dpu_misc_con	0x40C0	W	0x00000000	
DPU_dpu_surf_len	0x40C4	W	0x00000000	
DPU_dpu_misc_con1	0x40C8	W	0x00000000	
DPU_dpu_lut_access_cfg	0x40CC	W	0x00000000	LUT access address and type
DPU_dpu_lut_access_data	0x40D0	W	0x00000000	Configuration of LUT access data
DPU_dpu_lut_cfg	0x40D4	W	0x00000000	Configuration of the LUT
DPU_dpu_lut_info	0x40D8	W	0x00000000	LUT information register
DPU_dpu_lut_le_start	0x40DC	W	0x00000000	LE LUT start point
DPU_dpu_lut_le_end	0x40E0	W	0x00000000	LE LUT end point
DPU_dpu_lut_lo_start	0x40E4	W	0x00000000	LO LUT start point
DPU_dpu_lut_lo_end	0x40E8	W	0x00000000	LO LUT end point
DPU_dpu_lut_le_slope_scale	0x40EC	W	0x00000000	LE LUT slope scale
DPU_dpu_lut_le_slope_shift	0x40F0	W	0x00000000	LE LUT slope shift
DPU_dpu_lut_lo_slope_scale	0x40F4	W	0x00000000	LO LUT slope scale
DPU_dpu_lut_lo_slope_shift	0x40F8	W	0x00000000	LO LUT slope shift
DPU_RDMA_dpu_rdma_s_status	0x5000	W	0x00000000	Single register group status
DPU_RDMA_dpu_rdma_s_pointer	0x5004	W	0x00000000	Single register group pointer

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Name	Offset	Size	Reset Value	Description
DPU_RDMA_dpu_rdma_operation_enable	0x5008	W	0x00000000	Operation Enable
DPU_RDMA_dpu_rdma_data_cube_width	0x500C	W	0x00000000	Input cube width
DPU_RDMA_dpu_rdma_data_cube_height	0x5010	W	0x00000000	Input cube height
DPU_RDMA_dpu_rdma_data_cube_channel	0x5014	W	0x00000000	Input cube channel
DPU_RDMA_dpu_rdma_src_base_addr	0x5018	W	0x00000000	Base address of the input cube
DPU_RDMA_dpu_rdma_brdma_cfg	0x501C	W	0x00000000	Configurations of BRDMA
DPU_RDMA_dpu_rdma_bs_base_addr	0x5020	W	0x00000000	Source base address of BRDMA
DPU_RDMA_dpu_rdma_nrdma_cfg	0x5024	W	0x00000000	Configurations of NRDMA
DPU_RDMA_dpu_rdma_bn_base_addr	0x5028	W	0x00000000	Source base address of NRDMA
DPU_RDMA_dpu_rdma_erdma_cfg	0x502C	W	0x00000000	Configurations of ERDMA
DPU_RDMA_dpu_rdma_ew_base_addr	0x5030	W	0x00000000	Source base address of ERDMA
DPU_RDMA_dpu_rdma_ew_surf_stride	0x5034	W	0x00000000	Surface size of the cube that the ERDMA read
DPU_RDMA_dpu_rdma_feature_mode_cfg	0x5038	W	0x00000000	Configuration of the feature mode
DPU_RDMA_dpu_rdma_src_dma_cfg	0x503C	W	0x00000000	Configuration of the source read DMA
DPU_RDMA_dpu_rdma_surf_notch	0x5040	W	0x00000000	Surface notch
DPU_RDMA_dpu_rdma_pad_cfg	0x5044	W	0x00000000	Configuration of the pad
DPU_RDMA_dpu_rdma_ew_surf_notch	0x5048	W	0x00000000	Surface notch
DPU_RDMA_dpu_rdma_line_notch	0x504C	W	0x00000000	
DPU_RDMA_dpu_rdma_ew_line_notch	0x5050	W	0x00000000	
PPU_ppu_s_status	0x6000	W	0x00000000	Single register group status
PPU_ppu_s_pointer	0x6004	W	0x00000000	Single register group pointer
PPU_ppu_operation_enable	0x6008	W	0x00000000	Operation Enable
PPU_ppu_data_cube_in_width	0x600C	W	0x00000000	Width of the input cube
PPU_ppu_data_cube_in_height	0x6010	W	0x00000000	Height of the input cube
PPU_ppu_data_cube_in_channel	0x6014	W	0x00000000	Channel of the input cube
PPU_ppu_data_cube_out_width	0x6018	W	0x00000000	Width of the output cube
PPU_ppu_data_cube_out_height	0x601C	W	0x00000000	Height of the output cube
PPU_ppu_data_cube_out_channel	0x6020	W	0x00000000	Channel of the output cube

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Name	Offset	Size	Reset Value	Description
PPU_ppu_operation_mode_cfg	0x6024	W	0x00000000	Configuration of the operation mode
PPU_ppu_pooling_kernel_cfg	0x6028	W	0x00000000	Configuration of the pooling kernel size
PPU_ppu_recip_kernel_width	0x602C	W	0x00000000	The reciprocal of the kernel width
PPU_ppu_recip_kernel_height	0x6030	W	0x00000000	The reciprocal of the kernel height
PPU_ppu_pooling_padding_cfg	0x6034	W	0x00000000	Configuration of the pooling pad
PPU_ppu_padding_value_1_cfg	0x6038	W	0x00000000	Pad Value register0
PPU_ppu_padding_value_2_cfg	0x603C	W	0x00000000	Pad Value register1
PPU_ppu_padding_value_3_cfg	0x6040	W	0x00000000	
PPU_ppu_padding_value_4_cfg	0x6044	W	0x00000000	
PPU_ppu_padding_value_5_cfg	0x6048	W	0x00000000	
PPU_ppu_padding_value_6_cfg	0x604C	W	0x00000000	
PPU_ppu_padding_value_7_cfg	0x6050	W	0x00000000	
PPU_ppu_back_con_0	0x6054	W	0x00000000	
PPU_ppu_back_con_1	0x6058	W	0x00000000	
PPU_ppu_back_con_2	0x605C	W	0x00000000	
PPU_ppu_back_con_3	0x6060	W	0x00000000	
PPU_ppu_dst_base_addr	0x6064	W	0x00000000	Destination address of the output cube
PPU_ppu_dst_surf_stride	0x6068	W	0x00000000	Destination surface size
PPU_ppu_data_format	0x606C	W	0x00000000	Configuration of the data format
PPU_ppu_misc_ctrl	0x6070	W	0x00000000	Misc configuration
PPU_RDMA_ppu_rdma_s_status	0x7000	W	0x00000000	Single register group status
PPU_RDMA_ppu_rdma_s_pointer	0x7004	W	0x00000000	Single register group pointer
PPU_RDMA_ppu_rdma_operation_enable	0x7008	W	0x00000000	Operation Enable
PPU_RDMA_ppu_rdma_cube_in_width	0x700C	W	0x00000000	Input cube width
PPU_RDMA_ppu_rdma_cube_in_height	0x7010	W	0x00000000	Input cube height
PPU_RDMA_ppu_rdma_cube_in_channel	0x7014	W	0x00000000	Input cube channel
PPU_RDMA_ppu_rdma_src_base_addr	0x7018	W	0x00000000	Source base address for input feature
PPU_RDMA_ppu_rdma_src_line_stride	0x701C	W	0x00000000	Source line number including Virtual box
PPU_RDMA_ppu_rdma_src_surf_stride	0x7020	W	0x00000000	Source surface size including Virtual box
PPU_RDMA_ppu_rdma_data_format	0x7024	W	0x00000140	Data format for the input feature
DDMA_Register001	0x0000	W	0x0	

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Name	Offset	Size	Reset Value	Description
DDMA_ddma_cfg_outstanding	0x8000	W	0x00000000	Outstanding config register
DDMA_ddma_rd_weight_0	0x8004	W	0x00000000	Weight of read arbiter
DDMA_ddma_wr_weight_0	0x8008	W	0x00000000	Weight of write arbiter
DDMA_ddma_cfg_id_error	0x800C	W	0x00000000	Id where error happened
DDMA_ddma_rd_weight_1	0x8010	W	0x00000000	Weight of read arbiter register1
DDMA_ddma_cfg_dma_fifo_clr	0x8014	W	0x00000000	Clear DMA FIFO
DDMA_ddma_cfg_dma_arb	0x8018	W	0x00000000	DMA arbiter configuration register
DDMA_ddma_cfg_dma_rd_qos	0x801C	W	0x00000000	Read Qos for DMA
DDMA_ddma_cfg_dma_rd_cfg	0x8020	W	0x00000000	Read configuration for AXI signals
DDMA_ddma_cfg_dma_wr_cfg	0x8024	W	0x0000000C	Write configuration for AXI signals
DDMA_ddma_cfg_dma_wstrb	0x8028	W	0xFFFFFFFF	Write strobe signal for AXI
DDMA_ddma_cfg_status	0x802C	W	0x00000000	AXI status signal
DDMA_ddma_fd_write_bw	0x8030	W	0x00000000	
DDMA_ddma_fd_read_bw	0x8034	W	0x00000000	
DDMA_ddma_wt_read_bw	0x8038	W	0x00000000	
GLOBAL_global_op_en	0x0008	W	0x00000000	Combine Operation Enable

Double WORD (64 bits) access

9.4.3 Detail Registers Description

PC_pc_rknn_version

PC_pc_rknn_version

Address: Operational Base(0xFF300000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RO	0x46495245	rknn_version

PC_pc_operation_enable

Address: Operational Base(0xFF300000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	op_en PC operation enable. 1'd0: Disable PC module; 1'd1: Enable PC module to fetch register for each task.

PC_pc_base_address

Address: Operational Base(0xFF300000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	base_addr PC base address. This is the address of DMA instruction where it located.
3:1	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	pc_sel PC mode select. 1'd0: PC mode, use AXI DMA to fetch register config; 1'd1: Slave mode, use AHB to set register.

PC_pc_cmd_amounts

Address: Operational Base(0xFF300000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	data_amount Data amount. The register amount need to be fetched of each task. Each register takes 64 bits, it is combined as following: bit[63:48] indicates which block the register forward to. bit[47:16] the register's value bit[15: 0] the register's offset address in each block. bit[56]= 1 means this register is for pc block. bit[57]= 1 CNA bit[59]= 1 CORE bit[60]= 1 DPU bit[61]= 1 DPU_RDMA bit[62]= 1 PPU bit[63]= 1 PPU_RDMA bit[55]= 1 to set each block's op_en Eg. 64'h0081_0000_007f_0008 will set each block's op_en(CNA, CORE, ..., PPU_RDMA). Note: op_en is strongly recommended set at the end of register list. before op_en, 64'h0041_xxxx_xxxx_xxxx must be set.

PC_pc_interrupt_mask

Address: Operational Base(0xFF300000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31	RW	0x0	task_last
30:17	RO	0x0000	reserved
16:0	RW	0x1ffff	int_mask Interrupt mask. mask[0]: CNA feature group 0 interrupt mask. set 1 to enable interrupt; mask[1]: CNA feature group 1; mask[2]: CNA weight group 0; mask[3]: CNA weight group 1; mask[4]: CNA csc group 0; mask[5]: CNA csc group 1; mask[6]: CORE group 0; mask[7]: CORE group 1; mask[8]: DPU group 0; mask[9]: DPU group 1; mask[10]: PPU group 0; mask[11]: PPU group 1; mask[12]: DMA read error; mask[13]: DMA write error; Note: In pc mode, int mask set the last one task's interrupt masking.

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PC_pc_interrupt_clear

Address: Operational Base(0xFF300000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	W1C	0x00000	int_clr Interrupt clear. done_clr[0]: CNA feature group 0 interrupt clear; done_clr[1]: CNA feature group 1; done_clr[2]: CNA weight group 0; done_clr[3]: CNA weight group 1; done_clr[4]: CNA csc group 0; done_clr[5]: CNA csc group 1; done_clr[6]: CORE group 0; done_clr[7]: CORE group 1; done_clr[8]: DPU group 0; done_clr[9]: DPU group 1; done_clr[10]: PPU group 0; done_clr[11]: PPU group 1; done_clr[12]: DMA read error; done_clr[13]: DMA write error.

PC_pc_interrupt_status

Address: Operational Base(0xFF300000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	W1C	0x00000	int_st Interrupt status. int_st[0]: CNA feature group 0 interrupt status, which and with mask bit; int_st[1]: CNA feature group 1; int_st[2]: CNA weight group 0; int_st[3]: CNA weight group 1; int_st[4]: CNA csc group 0; int_st[5]: CNA csc group 1; int_st[6]: CORE group 0; int_st[7]: CORE group 1; int_st[8]: DPU group 0; int_st[9]: DPU group 1; int_st[10]: PPU group 0; int_st[11]: PPU group 1; int_st[12]: DMA read error; int_st[13]: DMA write error.

PC_pc_interrupt_raw_status

Address: Operational Base(0xFF300000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
16:0	W1C	0x00000	int_raw_st Interrupt raw status. int_st[0]: CNA feature group 0 interrupt raw status; int_st[1]: CNA feature group 1; int_st[2]: CNA weight group 0; int_st[3]: CNA weight group 1; int_st[4]: CNA csc group 0; int_st[5]: CNA csc group 1; int_st[6]: CORE group 0; int_st[7]: CORE group 1; int_st[8]: DPU group 0; int_st[9]: DPU group 1; int_st[10]: PPU group 0; int_st[11]: PPU group 1; int_st[12]: DMA read error; int_st[13]: DMA write error.

PC_pc_task_con

Address: Operational Base(0xFF300000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	W1C	0x0	task_last_layer_clear 1'b1: Clear the task last layer signal to 0. Before task started , it is suggestted to clear.
17	W1C	0x0	task_count_clear Task counter clear register. Clear the counter that counting current task. Before task started, it is suggested to clear.
16	RW	0x0	task_pp_en PC task ping-pong mode enable. 1'd0: Ping-pong mode off. The second group register setting is fetched after first group task operation is finished; 1'd1: Tasks' registers are fetched in ping-pong mode. The second group register setting is fetched immediately after first group's register fetching is finished.
15:0	RW	0x0000	task_number PC task number. Set the total task number to be executed.

PC_pc_task_dma_0_base_addr

Address: Operational Base(0xFF300000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	dma_0_base_addr Task base address. This is for each DMA's base address. For feature DMA, weight DMA, DPU DMA, PPU DMA, the address is set as offset address. Final address appear on AXI bus is base address + offset address.
3:0	RO	0x0	reserved

PC_pc_task_dma_1_base_addr

Address: Operational Base(0xFF300000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dma_1_base_addr

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PC_pc_task_dma_2_base_addr

Address: Operational Base(0xFF300000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dma_2_base_addr

PC_pc_task_dma_3_base_addr

Address: Operational Base(0xFF300000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dma_3_base_addr

PC_pc_task_dma_base_sel

Address: Operational Base(0xFF300000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RW	0x0	use_ppu_sel
13:12	RW	0x0	use_dpu_sel
11:10	RW	0x0	use_ew_sel
9:8	RW	0x0	use_bn_sel
7:6	RW	0x0	use_bs_sel
5:4	RW	0x0	use_wt_sel
3:2	RW	0x0	use_fd_sel
1:0	RW	0x0	use_pc_sel

PC_pc_task_status

Address: Operational Base(0xFF300000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	task_status Task status. [11:0]: Current task counter value; [12]: Indicate the first task is operating; [13]: Indicate the last task is operating; [12]: Indicate the first task's register is fetching; [13]: Indicate the last task's register is fetching.

CNA_cna_s_status

Address: Operational Base(0xFF301000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RO	0x0	status_1 Executer 1 status. 2'd0: Executer 1 is in idle state; 2'd1: Executer 1 is operating; 2'd2: Executer 1 is operating, executer 1 is waiting to operate; 2'd3: Reserved.
15:2	RO	0x0000	reserved
1:0	RO	0x0	status_0 Executer 0 status. 2'd0: Executer 0 is in idle state; 2'd1: Executer 0 is operating; 2'd2: Executer 0 is operating, executer 1 is waiting to operate; 2'd3: Reserved.

CNA_cna_s_pointer

Address: Operational Base(0xFF301000) + offset (0x0004)

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Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RO	0x0	executer Which register group to be used. 1'd0: Executer group 0; 1'd1: Executer group 1.
15:6	RO	0x000	reserved
5	W1C	0x0	executer_pp_clear Clear executer group pointer. Set this bit to 1 to clear pointer to 0.
4	W1C	0x0	pointer_pp_clear Clear register group pointer. Set this bit to 1 to clear pointer to 0.
3	RW	0x0	pointer_pp_mode Register group ping-pong mode. 1'd0: Pointer ping-pong by executer; eg. if current executer is 0, next pointer will toggle to 1; 1'd1: Pointer ping-pong by pointer; eg. if current pointer is 0, next pointer will toggle to 1.
2	RW	0x0	executer_pp_en Executer group ping-pong enable. 1'd0: Disable; 1'd1: Enable.
1	RW	0x0	pointer_pp_en Register group ping-pong enable. 1'd0: Disable; 1'd1: Enable.
0	RW	0x0	pointer Which register group ready to be set. 1'd0: Register group 0; 1'd1: Register group 1.

CNA_cna_operation_enable

Address: Operational Base(0xFF301000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	op_en Set this register will trigger CNA block operate. This register and after this are all shadowed for ping-pong operation. 1'd0: Disable; 1'd1: Enable.

CNA_cna_conv_con1

Address: Operational Base(0xFF301000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31	RW	0x0	addr_nonalign_proc If enable correct the non align address command to 0x40 aligned address command.
30	RW	0x0	fc_skip_backup
29	RW	0x0	group_line_off If group 4 lines for each series.
28	RW	0x0	soft_gen_dbuf_depth
27	RO	0x0	reserved
26	RW	0x0	soft_gen_entries
25:23	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
22:20	RW	0x0	wt_precision
19:18	RO	0x0	reserved
17:16	RW	0x0	fd_group_num How many groups in one tiling. 2'd0: One group; 2'd1: Two groups; 2'd2: Reserved; 2'd3: Four groups;
15	RW	0x0	argb_en If enable ARGB mode. 1'd0: Disable; 1'd1: Enable.
14	RW	0x0	group_en If enable group feature calculation. 1'd0: Disable; 1'd1: Enable.
13:12	RW	0x0	argb_in ARGB channels. 2'd0: 1 channel input mode; 2'd1: 2 channel input mode; 2'd2: 3 channel input mode; 2'd3: 4 channel input mode.
11:10	RO	0x0	reserved
9:7	RW	0x0	proc_precision Process precision. 3'd0: Input precision is int 8; 3'd1: Input data precision is int 16; 3'd2: Input data precision is float 16; 3'd3: Input data precision is bfloat 16; 3'd4: Reserved; 3'd5: Reserved; 3'd6: Input data precision is int4; 3'd7: Input data precision is tf32.
6:4	RW	0x0	in_precision Input precision. 3'd0: Input precision is int 8; 3'd1: Input data precision is int 16; 3'd2: Input data precision is float 16; 3'd3: Input data precision is bfloat 16; 3'd4: Reserved; 3'd5: Reserved; 3'd6: Input data precision is int4; 3'd7: Input data precision is tf32.
3	RW	0x0	special_wt_pipeline
2	RW	0x0	qd_cal_en Usefull in depthwise mode and argb mode. 1'd0: Per layer quantify, weight is original weight; 1'd1: Per channel quantify, you must add offset of weight behind each channel.
1:0	RW	0x0	conv_mode Convolution mode. 2'd0: Direct convolution; 2'd1: Depthwise convolution; 2'd2: Argb convolution; 2'd3: Reserved.

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CNA_cna_conv_con2

Address: Operational Base(0xFF301000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	wt_bank_grp_ker_num
15:14	RO	0x0	reserved
13:0	RW	0x0000	feature_grains Feature data rows needs to be buffered before convolution start. It's suggested to set this field as y_stride+weight_height+1.

CNA_cna_conv_con3

Address: Operational Base(0xFF301000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:21	RW	0x00	atrous_y_dilation Atrous x dilation. Pad numbers inserted in feature map column between 2 pixels.
20:16	RW	0x00	atrous_x_dilation Atrous x dilation. Pad numbers inserted in feature map row between 2 pixels. Set this register value >0 will enable atrous convolution.
15:14	RO	0x0	reserved
13:11	RW	0x0	deconv_y_stride Deconvolution y stride. Pad numbers inserted in feature map column between 2 pixels.
10:8	RW	0x0	deconv_x_stride Deconvolution x stride. Pad numbers inserted in feature map row between 2 pixels.
7:6	RO	0x0	reserved
5:3	RW	0x0	conv_y_stride Convolution y stride. Stride value in y direction.
2:0	RW	0x0	conv_x_stride Convolution x stride. Stride value in x direction.

CNA_cna_conv_con4

Address: Operational Base(0xFF301000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31	RW	0x0	data_wr_wrap_en
30:24	RO	0x00	reserved
23:16	RW	0x00	dbuf_depth
15:13	RO	0x0	reserved
12:8	RW	0x00	data_bank_used
7:5	RO	0x0	reserved
4:0	RW	0x00	data_bank_end

CNA_cna_weight_size0

Address: Operational Base(0xFF301000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	weight_bytes Weight bytes in total for this convolution.

CNA_cna_weight_size1

Address: Operational Base(0xFF301000) + offset (0x0020)

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Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	bank_used_depth
19	RO	0x0	reserved
18:0	RW	0x00000	weight_bytes_per_kernel Weight bytes for one kernel.

CNA_cna_weight_size2

Address: Operational Base(0xFF301000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	weight_width Kernel width.
23:21	RO	0x0	reserved
20:16	RW	0x00	weight_height Kernel height.
15:14	RO	0x0	reserved
13:0	RW	0x0000	weight_kernels Weight kernels.

CNA_cna_data_size1

Address: Operational Base(0xFF301000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	datain_channel Real channel number. If the input channel is not integer times of 8(int8) or 4(int 16/float 16), set the real channel number in this field.

CNA_cna_data_size0

Address: Operational Base(0xFF301000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	datain_width Input feature data width.
15:14	RO	0x0	reserved
13:0	RW	0x0000	datain_height Input feature data height.

CNA_cna_data_size2

Address: Operational Base(0xFF301000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	dataout_width Data width after convolution.

CNA_cna_data_size3

Address: Operational Base(0xFF301000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:22	RW	0x0	surf_mode Surface serial mode. 2'd0: 1surf series; 2'd1: 1surf series; 2'd2: 2 surf series; 2'd3: 4 surf series.

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Bit	Attr	Reset Value	Description
21:0	RW	0x000000	dataout_atomics Data atomics after convolution which is data out total pixels number.

CNA_cna_cbuf_con0

Address: Operational Base(0xFF301000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	use_config_wt Do not fetch weight, but use the weight_offset to fetch MAC.
14	RW	0x0	use_config_fd Do not fetch feature data, but use the data_offset to fetch MAC.
13	RW	0x0	weight_reuse Weight data reuse enable. 1'd0: Disable; 1'd1: Enable data reuse. fetching weight directly from internal buffer.
12	RW	0x0	data_reuse Feature data reuse enable. 1'd0: Disable; 1'd1: Enable data reuse. fetching data directly from internal buffer.
11:5	RO	0x00	reserved
4:0	RW	0x00	bank_used We have 16 banks in CBUF. But we can separate some banks for another use. This register means the banks for NPU.

CNA_cna_cbuf_con1

Address: Operational Base(0xFF301000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	data_entries Usefull when soft_gen_entries is enable;
15:14	RO	0x0	reserved
13:0	RW	0x0000	fc_bank_st Start address of fc feature in CBUF.

CNA_cna_cbuf_con2

Address: Operational Base(0xFF301000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	weight_bank_st Start address of weight in CBUF.
15:14	RO	0x0	reserved
13:0	RW	0x0000	data_bank_st Start address of feature in CBUF.

CNA_cna_cbuf_con3

Address: Operational Base(0xFF301000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	entries_pergroup
15:14	RO	0x0	reserved
13:0	RW	0x0000	entries_csc

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CNA_cna_cvt_con0

Address: Operational Base(0xFF301000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:22	RW	0x00	cvt_truncate_3 CVT truncate value 3.
21:16	RW	0x00	cvt_truncate_2 CVT truncate value 2.
15:10	RW	0x00	cvt_truncate_1 CVT truncate value 1.
9:4	RW	0x00	cvt_truncate_0 CVT truncate value 0.
3	RW	0x0	data_sign Feature data is signed or unsigned. 1'd0: Unsigned; 1'd1: Signed.
2	RW	0x0	round_type Rounding type of the input convert. 1'd0: Odd in, even not; 1'd1: Round-up 0.5 to 1.
1	RW	0x0	cvt_type
0	RW	0x0	cvt_bypass Bypass input convert. 1'd0: Enable CVT function; 1'd1: Disable CVT function.

CNA_cna_cvt_con1

Address: Operational Base(0xFF301000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	cvt_scale1 CVT scale 1. Multiplier operand for 1st channel.
15:0	RW	0x0000	cvt_scale0 CVT scale 0. Mul operand for 0st channel.

CNA_cna_cvt_con2

Address: Operational Base(0xFF301000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	cvt_scale3 CVT scale 3 Multiplier operand for 3rd channel.
15:0	RW	0x0000	cvt_scale2 CVT scale 2. Mul operand for 2nd channel.

CNA_cna_cvt_con3

Address: Operational Base(0xFF301000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cvt_offset0 CVT offset 0. Adder operand for 0st channel.

CNA_cna_cvt_con4

Address: Operational Base(0xFF301000) + offset (0x0058)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cvt_offset1 CVT offset 1. Adder operand for 1st channel.

CNA_cna_cvt_con5

Address: Operational Base(0xFF301000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cvt_offset2

CNA_cna_cvt_con6

Address: Operational Base(0xFF301000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cvt_offset3

CNA_cna_cvt_con7

Address: Operational Base(0xFF301000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	per_channel_cvt_en_l convert enable. Per channel enable CVT function. Int 4 has 32 channels in total for 128 bits. Int 8 16 channel...

CNA_cna_cvt_con8

Address: Operational Base(0xFF301000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	per_channel_cvt_en_h convert enable. Per channel enable CVT function. Int 4 has 32 channels in total for 128 bits. Int 8 16 channel...

CNA_cna_fc_con0

Address: Operational Base(0xFF301000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	fc_skip_data FC zero skipping data Skipped feature data value, normally set to 0.
15:6	RO	0x000	reserved
5:4	RW	0x0	zero_num_sft
3	RO	0x0	reserved
2	RW	0x0	addr_wrap
1	RW	0x0	skip_inv
0	RW	0x0	fc_skip_en FC zero skipping enable 1'd0: Disable; 1'd1: Enable skip some feature data value, normally skip zero. When one pixel feature data is 0, the corresponding weight data is not fetched from system memory.

CNA_cna_fc_con1

Address: Operational Base(0xFF301000) + offset (0x0070)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	data_offset FC zero skipping data offset. Feature data offset in fc skip mode.

CNA_cna_fc_con2

Address: Operational Base(0xFF301000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RW	0x00000	weight_offset Weight data address.

CNA_cna_fc_data_size0

Address: Operational Base(0xFF301000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	dma_width
15:14	RO	0x0	reserved
13:0	RW	0x0000	dma_height

CNA_cna_fc_data_size1

Address: Operational Base(0xFF301000) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	dma_channel

CNA_cna_pad_con0

Address: Operational Base(0xFF301000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	pad_right
23:22	RO	0x0	reserved
21:16	RW	0x00	pad_bottom
15:14	RO	0x0	reserved
13:8	RW	0x00	pad_left Pad left Pad numbers in left of the feature map.
7:6	RO	0x0	reserved
5:0	RW	0x00	pad_top PAD top Pad numbers in top of the feature map.

CNA_cna_pad_con1

Address: Operational Base(0xFF301000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pad_value Pad value.

CNA_cna_feature_data_addr

Address: Operational Base(0xFF301000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	feature_base_addr Feature data address.

CNA_cna_dma_con0

Address: Operational Base(0xFF301000) + offset (0x008C)

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Bit	Attr	Reset Value	Description
31	RW	0x0	ov4k_bypass Separate the burst command of over 4k to 2 independent burst commands. 1'd0: Enable this feature; 1'd1: Bypass this feature.
30:20	RO	0x000	reserved
19:16	RW	0x0	weight_burst_len AXI burst length for weight data DMA. 4'd3: Burst length is 4; 4'd7: Burst length is 8; 4'd15: Burst length is 16.
15	RO	0x0	reserved
14:12	RW	0x0	dat_read_size
11:4	RO	0x00	reserved
3:0	RW	0x0	data_burst_len AXI burst length for feature data DMA. 4'd3: Burst length is 4; 4'd7: Burst length is 8; 4'd15: Burst length is 16.

CNA_cna_dma_con1

Address: Operational Base(0xFF301000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	line_stride Line stride Feature width with Virtual box.

CNA_cna_dma_con2

Address: Operational Base(0xFF301000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	surf_stride Surface stride Feature map actual surface area.

CNA_cna_dma_con3

Address: Operational Base(0xFF301000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	surf_stride_backup

CNA_cna_clk_gate

Address: Operational Base(0xFF301000) + offset (0x009C)

Bit	Attr	Reset Value	Description
31	RW	0x0	mem_soft_gate
30:5	RO	0x0000000	reserved
4	RW	0x0	cbuf_cs_disable_clkgate Cache auto gating. 1'd0: Auto clock gate is enabled; 1'd1: Disable CBUF clock auto gate.
3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2	RW	0x0	csc_disable_clkgate Sequence scan auto gating. 1'd0: Auto clock gate is enabled; 1'd1: Disable csc block clock gate.
1	RW	0x0	cna_weight_disable_clkgate Weight fetch auto gating. 1'd0: Auto clock gate is enabled; 1'd1: Disable weight block clock gate.
0	RW	0x0	cna_feature_disable_clkgate Feature fetch auto gating. 1'd0: Auto clock gate is enabled; 1'd1: Disable feature block clock gate.

CNA_cna_dcomp_ctrl

Address: Operational Base(0xFF301000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	decomp_control Control register for weight decompress. 4'b0000: Do not use decompress; 4'b0101: Use two decompress module; 4'b1001: The first decompress module work on, and the second decompress module bypass; 4'b0110: The first decompress module bypass, while the second decompress work on; 4'b1010: Both the two decompress module bypass; Others: Illegal.

CNA_cna_dcomp_regnum

Address: Operational Base(0xFF301000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	dcomp_regnum Weight decompress register number.

CNA_cna_dcomp_addr0

Address: Operational Base(0xFF301000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	decompress_addr0 Base address of the weight.
3:0	RO	0x0	reserved

CNA_cna_dcomp_amount0

Address: Operational Base(0xFF301000) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dcomp_amount0 Amount of the weight decompress for the 0 decompress.

CNA_cna_dcomp_amount1

Address: Operational Base(0xFF301000) + offset (0x0144)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dcomp_amount1 Amount of the weight decompress for the 1 decompress.

CNA_cna_rsp_amount

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Address: Operational Base(0xFF301000) + offset (0x018C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	nonalign_rsp_amount

CORE_core_s_status

Address: Operational Base(0xFF303000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RO	0x0	status_1 Executer 1 status. 2'd0: Executer 1 is in idle state; 2'd1: Executer 1 is operating; 2'd2: Executer 1 is operating, executer 1 is waiting to operate; 2'd3: Reserved.
15:2	RO	0x0000	reserved
1:0	RO	0x0	status_0 Executer 0 status. 2'd0: Executer 0 is in idle state; 2'd1: Executer 0 is operating; 2'd2: Executer 0 is operating, executer 1 is waiting to operate; 2'd3: Reserved.

CORE_core_s_pointer

Address: Operational Base(0xFF303000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RO	0x0	executer Which register group to be used. 1'd0: Executer group 0; 1'd1: Executer group 1.
15:6	RO	0x000	reserved
5	W1C	0x0	executer_pp_clear Clear executer group pointer. Set this bit to 1 to clear pointer to 0.
4	W1C	0x0	pointer_pp_clear Clear register group pointer. Set this bit to 1 to clear pointer to 0.
3	RW	0x0	pointer_pp_mode Register group ping-pong mode. 1'd0: Pointer ping-pong by executer; eg. if current executer is 0, next pointer will toggle to 1; 1'd1: Pointer ping-pong by pointer; eg. if current pointer is 0, next pointer will toggle to 1.
2	RW	0x0	executer_pp_en Executer group ping-pong enable. 1'd0: Disable; 1'd1: Enable.
1	RW	0x0	pointer_pp_en Register group ping-pong enable. 1'd0: Disable; 1'd1: Enable.
0	RW	0x0	pointer Which register group ready to be set. 1'd0: Register group 0; 1'd1: Register group 1.

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CORE_core_operation_enable

Address: Operational Base(0xFF303000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	op_en Set this register will trigger core block operate. This register and after this are all shadowed for ping-pong operation. 1'd0: Disable; 1'd1: Enable.

CORE_core_misc_cfg

Address: Operational Base(0xFF303000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:8	RW	0x0	proc_precision Process precision 3'd0: Input precision is int 8; 3'd1: Input data precision is int 16; 3'd2: Input data precision is float 16; 3'd3: Input data precision is bfloat 16; 3'd4: Reserved; 3'd5: Reserved; 3'd6: Input data precision is int4; 3'd7: Input data precision is tf32.
7	RW	0x0	argb_en
6	RW	0x0	fc_skip
5:4	RW	0x0	group_num How many group in group convolution. 2'd0: One group; 2'd1: Two groups; 2'd2: Reserved; 2'd3: Four groups.
3	RW	0x0	sign_inv
2	RW	0x0	group_en If enable group convolution. 1'd0: Disable; 1'd1: Enable.
1	RW	0x0	dw_en Depthwise enable 1'd0: Disable; 1'd1: Depthwise mode enable.
0	RW	0x0	qd_cnt_en Quantify feature data calculate enable 1'd0: Disable; 1'd1: Enable.

CORE_core_dataout_size_0

Address: Operational Base(0xFF303000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	dataout_height Data out height Data height after activation.
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x0000	dataout_width Data out width. Data width after activation.

CORE_core_dataout_size_1

Address: Operational Base(0xFF303000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	dataout_channel Data out channel number Data channel number after activation.

CORE_core_clip_truncate

Address: Operational Base(0xFF303000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10	RW	0x0	round_type Rounding type 1'b0: Odd in, even not; 1'b1: Round-up 0.5 to 1.
9:5	RW	0x00	clip_qd Truncate bits number for qd cal out. Note: In ARGB MODE and DPU cal cpend, clip_qd must be clip_conv+1.
4:0	RW	0x00	clip_conv Truncate bits number for convolution out.

DPU_dpu_s_status

Address: Operational Base(0xFF304000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RO	0x0	status_1 Executer 1 status. 2'd0: Executer 1 is in idle state; 2'd1: Executer 1 is operating; 2'd2: Executer 1 is operating, executer 1 is waiting to operate; 2'd3: Reserved.
15:2	RO	0x0000	reserved
1:0	RO	0x0	status_0 Executer 0 status. 2'd0: Executer 0 is in idle state; 2'd1: Executer 0 is operating; 2'd2: Executer 0 is operating, executer 1 is waiting to operate; 2'd3: Reserved.

DPU_dpu_s_pointer

Address: Operational Base(0xFF304000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RO	0x0	executer Which register group to be used. 1'd0: Executer group 0; 1'd1: Executer group 1.
15:6	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
5	W1C	0x0	executer_pp_clear Clear executer group pointer. Set this bit to 1 to clear pointer to 0.
4	W1C	0x0	pointer_pp_clear Clear register group pointer. Set this bit to 1 to clear pointer to 0.
3	RW	0x0	pointer_pp_mode Register group ping-pong mode. 1'd0: Pointer ping-pong by executer; eg. if current executer is 0, next pointer will toggle to 1; 1'd1: Pointer ping-pong by pointer; eg. if current pointer is 0, next pointer will toggle to 1.
2	RW	0x0	executer_pp_en Executer group ping-pong enable. 1'd0: Disable; 1'd1: Enable.
1	RW	0x0	pointer_pp_en Register group ping-pong enable. 1'd0: Disable; 1'd1: Enable.
0	RW	0x0	pointer Which register group ready to be set. 1'd0: Register group 0; 1'd1: Register group 1.

DPU_dpu_operation_enable

Address: Operational Base(0xFF304000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	op_en Set this register will trigger DPU block operate. This register and after this are all shadowed for ping-pong operation. 1'd0: Disable; 1'd1: Enable.

DPU_dpu_feature_mode_cfg

Address: Operational Base(0xFF304000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	rgp_full_en If cut all pixel or the last pixel of each line. 1'd0: Last; 1'd1: All.

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Bit	Attr	Reset Value	Description
29:26	RW	0x0	rgp_type Regroup type. 4'd0: Cut all input (128bit); 4'd1: Cut 8bit; 4'd2: Cut 16bit; 4'd3: Cut 24bit; 4'd4: Cut 32bit; 4'd5: Cut 40bit; 4'd6: Cut 48bit; 4'd7: Cut 56bit; 4'd8: Cut 64bit; 4'd9: Cut 72bit; 4'd10: Cut 80bit; 4'd11: Cut 88bit; 4'd12: Cut 96bit; 4'd13: Cut 104bit; 4'd14: Cut 112bit; 4'd15: Cut 120bit.
25	RW	0x0	nonalign If non-align mode is enabled. If the output data flow is the same as the input data flow, this mode can be used.
24:9	RO	0x0000	reserved
8:5	RW	0x0	burst_len Burst length. 4'd3: Burst4; 4'd7: Burst8; 4'd15: Burst16.
4:3	RW	0x0	conv_mode Convolution mode. 2'd0: Normal convolution mode; 2'd1: Reserved; 2'd2: Reserved; 2'd3: Depthwise convolution mode.
2:1	RW	0x0	output_mode Where the DPU core output goes. 2'b00: Illegal; 2'b01: Output goes to PPU or WRITE BACK, it depends on if the PPU is enable; 2'b10: Output goes to outside; 2'b11: Output goes to PPU and outside.
0	RW	0x0	flying_mode Flying mode enable. 1'd0: DPU core main data is from convolution output; 1'd1: DPU core main data is from MRDMA;

DPU_dpu_data_format

Address: Operational Base(0xFF304000) + offset (0x0010)

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Bit	Attr	Reset Value	Description
31:29	RW	0x0	out_precision Output precision. 3'd0: Integer 8bit; 3'd1: Integer 16bit; 3'd2: Float point 16bit; 3'd3: Bfloat 16bit; 3'd4: Integer 32bit; 3'd5: Float point 32bit; 3'd6: Integer 4bit.
28:22	RO	0x00	reserved
21:16	RW	0x00	ew_truncate_neg Shift value in BN core for negative data.
15:10	RW	0x00	bn_mul_shift_value_neg
9:4	RW	0x00	bs_mul0_shift_value_neg Shift value in BS core for negative data.
3	RO	0x0	reserved
2:0	RW	0x0	proc_precision Proc precision. 3'd0: Integer 8bit; 3'd1: Integer 16bit; 3'd2: Float point 16bit; 3'd3: Bfloat 16bit; 3'd4: Integer 32bit; 3'd5: Float point 32bit; 3'd6: Integer 4bit.

DPU_dpu_offset_pend

Address: Operational Base(0xFF304000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	offset_pend What value the extra channel be set.

DPU_dpu_dst_base_addr

Address: Operational Base(0xFF304000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	dst_base_addr Destination base address.
3:0	RO	0x0	reserved

DPU_dpu_dst_surf_stride

Address: Operational Base(0xFF304000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dst_surf_stride Output shape surface stride.

DPU_dpu_data_cube_width

Address: Operational Base(0xFF304000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	width Width of the input cube.

DPU_dpu_data_cube_height

Address: Operational Base(0xFF304000) + offset (0x0024)

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Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:22	RW	0x0	minmax_ctl Configuration of the minmax op. [0]: Enable minmax op; [1]: Minmax type; [2]: Probability only.
21:13	RO	0x000	reserved
12:0	RW	0x0000	height Height of the input cube.

DPU_dpu_data_cube_notch_addr

Address: Operational Base(0xFF304000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	notch_addr_0 How many pixels from the end of width to the end of the shape line end.

DPU_dpu_data_cube_channel

Address: Operational Base(0xFF304000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	channel Cube channel.

DPU_dpu_wdma_size_0

Address: Operational Base(0xFF304000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	size_c_wdma channel for DPU_WDMA.
15:5	RO	0x000	reserved
4	RW	0x0	rgp_partial_wr cfg: 1, npu use configed rgp_left cfg: 0, npu use hardware generate rgp_left
3	RW	0x0	rgp_all_mask cfg: 1, all output value equals offset_pend
2:0	RW	0x0	rgp_left In normal situation, it equals to rgp_cnter. But if you want to mask extra surface and do not output it, you can set this register less than rgp_cnter.

DPU_dpu_wdma_size_1

Address: Operational Base(0xFF304000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	height_wdma Height for DPU_WDMA.
15:13	RO	0x0	reserved
12:0	RW	0x0000	width_wdma Width for DPU_WDMA.

DPU_dpu_bs_cfg

Address: Operational Base(0xFF304000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
21:19	RW	0x0	bs_alu1_algo BS core ALU op type. 3'd0: Reserved; 3'd1: Reserved; 3'd2: Add 3'd3: Reserved; 3'd4: Minus; Else: Reserved;
18:16	RW	0x0	bs_alu0_algo BS core ALU op type. 3'd0: Reserved; 3'd1: Reserved; 3'd2: Add 3'd3: Reserved; 3'd4: Minus; Else: Reserved;
15:14	RO	0x0	reserved
13:8	RW	0x00	bs_mul1_shift_value
7	RW	0x0	bs_alu1_src
6	RW	0x0	bs_alu1_bypass If bypass BS core ALU1 op. 1'd0: Do not bypass; 1'd1: Bypass.
5	RW	0x0	bs_mul0_prelu If enable MUL PRELU. 1'd0: Disable; 1'd1: Enable.
4	RW	0x0	bs_mul0_bypass If bypass BS core MUL op. 1'd0: Do not bypass; 1'd1: Bypass.
3:2	RO	0x0	reserved
1	RW	0x0	bs_alu0_bypass If bypass BS core ALU op. 1'd0: Do not bypass; 1'd1: Bypass.
0	RW	0x0	bs_bypass If bypass BS core. 1'd0: Do not bypass bs core; 1'd1: Bypass bs core.

DPU_dpu_bs_alu_cfg

Address: Operational Base(0xFF304000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	bs_alu0_operand Bs core ALU operand.

DPU_dpu_bs_alu1_cfg

Address: Operational Base(0xFF304000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	bs_alu1_operand

DPU_dpu_bs_mul_cfg

Address: Operational Base(0xFF304000) + offset (0x0044)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	bs_mul1_operand
15:8	RW	0x00	bs_mul0_shift_value Shift value in BS core for positive data.
7:3	RO	0x00	reserved
2	RW	0x0	bs_mul1_prelu
1	RW	0x0	bs_truncate_src Where the shift value from. 1'd0: From configure register; 1'd1: From outside.
0	RW	0x0	bs_mul0_src Where the MUL operand from. 1'd0: From configure register; 1'd1: From outside.

DPU_dpu_bs_rlu_cfg

Address: Operational Base(0xFF304000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	bs_relu_cmp_under Bottom value of the RELU compare with.

DPU_dpu_bs_rlu1_cfg

Address: Operational Base(0xFF304000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	bs_relu_cmp_over Top value of the threshold of relu.

DPU_dpu_bs_ow_cfg

Address: Operational Base(0xFF304000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:22	RW	0x0	tp_precision 3'd0: 8bit transpose. 3'd1: 16bit transpose. 3'd2: 32bit transpose. 3'd3: 64bit transpose. 3'd4: 128bit transpose.
21:20	RW	0x0	tp_mode 2'd0: Normal; 2'd1: Merge; 2'd2: Transpose. 2'd3: tp_en;
19:11	RO	0x000	reserved
10:8	RW	0x0	size_e_2 How many 8 channels in a row the last output line (minus 1).
7:5	RW	0x0	size_e_1 How many 8 channels in a row the middle output line (minus 1).
4:2	RW	0x0	size_e_0 How many 8 channels in a row the first output line (minus 1).
1	RW	0x0	bs_mul1_bypass If bypass CPEND. 1'd0: Do not bypass; 1'd1: Bypass.

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Bit	Attr	Reset Value	Description
0	RW	0x0	bs_mul1_src Where the CPEND operand from. 1'd0: From configure register; 1'd1: From outside.

DPU_dpu_bs_ow_op

Address: Operational Base(0xFF304000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31	RW	0x0	qd_cal_cpend_en
30:22	RO	0x000	reserved
21:16	RW	0x00	bs_mul1_shift_value_neg
15:0	RW	0x0000	bs_mul0_operand

DPU_dpu_bs_relu_val_0

Address: Operational Base(0xFF304000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	bs_relu_val_under

DPU_dpu_bs_relu_val_1

Address: Operational Base(0xFF304000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	bs_relu_val_over

DPU_dpu_bn_cfg

Address: Operational Base(0xFF304000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:16	RW	0x0	bn_alu_algo BS core ALU op type. 4'd0: Reserved; 4'd1: Reserved; 4'd2: Add 4'd3: Reserved; 4'd4: Minus; 4'd5: Reserved; 4'd6: Reserved; 4'd7: Reserved; 4'd8: Reserved.
15:9	RO	0x00	reserved
8	RW	0x0	bn_alu_src Where the ALU operand from 1'd0: From configure register; 1'd1: From outside.
7:6	RO	0x0	reserved
5	RW	0x0	bn_mul_prelu If enable MUL PRELU. 1'd0: Disable; 1'd1: Enable.
4	RW	0x0	bn_mul_bypass If bypass BN core MUL op. 1'd0: Do not bypass; 1'd1: Bypass.
3:2	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x0	bn_alu_bypass If bypass BN core ALU op. 1'd0: Do not bypass; 1'd1: Bypass.
0	RW	0x0	bn_bypass If bypass BN core. 1'd0: Do not bypass BN core; 1'd1: Bypass BN core.

DPU_dpu_bn_alu_cfg

Address: Operational Base(0xFF304000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	bn_alu_operand

DPU_dpu_bn_mul_cfg

Address: Operational Base(0xFF304000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	bn_mul_operand
15:14	RO	0x0	reserved
13:8	RW	0x00	bn_mul_shift_value
7:2	RO	0x00	reserved
1	RW	0x0	bn_truncate_src Where the shift value from 1'd0: From configure register; 1'd1: From outside.
0	RW	0x0	bn_mul_src Where the MUL operand from. 1'd0: From configure register; 1'd1: From outside.

DPU_dpu_bn_rlu_cfg

Address: Operational Base(0xFF304000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	bn_relu_cmp_under RELUX compare data in BN core.

DPU_dpu_bn_rlu1_cfg

Address: Operational Base(0xFF304000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	bn_relu_cmp_over Top value of the threshold relu.

DPU_dpu_bn_relu_val_0

Address: Operational Base(0xFF304000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	bn_relu_val_under

DPU_dpu_bn_relu_val_1

Address: Operational Base(0xFF304000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	bn_relu_val_over

DPU_dpu_ew_cfg

Address: Operational Base(0xFF304000) + offset (0x007C)

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Bit	Attr	Reset Value	Description
31	RW	0x0	ew_cvt_type Convert type of EW input convert when if 0.5 1'd0: Mul first; 1'd1: Add first.
30	RW	0x0	ew_cvt_round Rounding type of EW input convert when if 0.5 1'd0: If the integer is odd, carry 1; 1'd1: Carry 1 no matter what the integer is.
29:25	RO	0x00	reserved
24	RW	0x0	ew_alu_bypass
23	RW	0x0	ew_binary_en_neg
22	RW	0x0	edata_size Data size of the cube from ERDMA. 1'd0: Not 32bit; 1'd1: Is 32bit.
21	RW	0x0	ew_equal_en Min max equal enable. 1'd0: Disable; 1'd1: Enable.
20	RW	0x0	ew_binary_en_pos Min max binary enable. 1'd0: Disable; 1'd1: Enable.
19:16	RW	0x0	ew_alu_algo EW core ALU op type. 4'd0: Max; 4'd1: Min; 4'd2: Add; 4'd3: Div; 4'd4: Minus; 4'd5: Abs; 4'd6: Neg; 4'd7: Floor; 4'd8: Ceil.
15	RW	0x0	ew_alu_src If enable RELUX. 1'd0: Disable; 1'd1: Enable.
14	RW	0x0	ew_div_bypass If bypass EW core RELU op. 1'd0: Do not bypass; 1'd1: Bypass.
13	RW	0x0	ew_div_src
12:9	RO	0x0	reserved
8	RW	0x0	ew_op_cvt_bypass If bypass EW input converter. 1'd0: Do not bypass; 1'd1: Bypass.
7	RW	0x0	ew_lut_bypass If bypass LUT. 1'd0: Do not bypass; 1'd1: Bypass.
6	RW	0x0	ew_mul_bypass

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Bit	Attr	Reset Value	Description
5	RW	0x0	ew_mul_prelu If enable MUL PRELU. 1'd0: Disable; 1'd1: Enable.
4	RW	0x0	ew_mul_src
3:2	RW	0x0	ew_op_type Operator type. 2'd0: ALU; 2'd1: MUL. 2'd2: DIV;
1	RO	0x0	reserved
0	RW	0x0	ew_bypass If bypass EW core. 1'd0: Do not bypass EW core; 1'd1: Bypass EW core.

DPU_dpu_ew_cvt_offset_value

Address: Operational Base(0xFF304000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	ew_op_cvt_offset EW convert offset.

DPU_dpu_ew_cvt_scale_value

Address: Operational Base(0xFF304000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:22	RW	0x00	ew_truncate EW core shift value.
21:16	RW	0x00	ew_op_cvt_shift EW convert shift value.
15:0	RW	0x0000	ew_op_cvt_scale EW convert scale.

DPU_dpu_ew_rlu_cfg

Address: Operational Base(0xFF304000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ew_relu_cmp_under EW RELUX compare data.

DPU_dpu_ew_rlu1_cfg

Address: Operational Base(0xFF304000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ew_relu_cmp_over Top value of the threshold relu.

DPU_dpu_ew_operand

Address: Operational Base(0xFF304000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ew_operand The 1st EW operand for EW core op.

DPU_dpu_ew_con_value_a_l

Address: Operational Base(0xFF304000) + offset (0x0094)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ew_alu_value_a_l

DPU_dpu_ew_con_value_a_h

Address: Operational Base(0xFF304000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ew_alu1_value_a_h

DPU_dpu_ew_con_value_b_l

Address: Operational Base(0xFF304000) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ew_alu1_value_b_l

DPU_dpu_ew_con_value_b_h

Address: Operational Base(0xFF304000) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ew_alu1_value_b_h

DPU_dpu_ew_relu_val_0

Address: Operational Base(0xFF304000) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ew_relu_val_under

DPU_dpu_ew_relu_val_1

Address: Operational Base(0xFF304000) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ew_relu_val_over

DPU_dpu_out_cvt_offset

Address: Operational Base(0xFF304000) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	out_cvt_offset Offset of the output converter.

DPU_dpu_out_cvt_scale

Address: Operational Base(0xFF304000) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	fp32tofp16_en If enable output from fp32 to fp16. 1'd0: Disable; 1'd1: Enable.
15:0	RW	0x0000	out_cvt_scale Scale of the output converter.

DPU_dpu_out_cvt_shift

Address: Operational Base(0xFF304000) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31	RW	0x0	cvt_type Convert type of out convert when if 0.5. 1'd0: MUL first; 1'd1: ALU first.

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Bit	Attr	Reset Value	Description
30	RW	0x0	cvt_round Rounding type of out convert when if 0.5. 1'd0: If the integer is odd, carry 1; 1'd1: Carry 1 no matter what the integer is.
29:20	RO	0x000	reserved
19:12	RW	0x00	minus_exp
11:0	RW	0x000	out_cvt_shift Shift of the output converter.

DPU_dpu_surface_add

Address: Operational Base(0xFF304000) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	surf_add How many surfaces in a row.

DPU_dpu_perf_en

Address: Operational Base(0xFF304000) + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	bubble_except
15:11	RO	0x00	reserved
10	RW	0x0	nan_clr
9	RO	0x0	dp2reg_out_nan
8:0	RO	0x000	reserved

DPU_dpu_misc_con

Address: Operational Base(0xFF304000) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:24	RW	0x0	ew_relu_con
23	RO	0x0	reserved
22:20	RW	0x0	bn_relu_con
19	RO	0x0	reserved
18:16	RW	0x0	bs_relu_con
15:10	RO	0x00	reserved
9:4	RW	0x00	tp_align_byte
3:2	RO	0x0	reserved
1	RW	0x0	wr_ov4k_bypass
0	RO	0x0	reserved

DPU_dpu_surf_len

Address: Operational Base(0xFF304000) + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	surf_len

DPU_dpu_misc_con1

Address: Operational Base(0xFF304000) + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tp_byte_size

DPU_dpu_lut_access_cfg

Address: Operational Base(0xFF304000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
17	RW	0x0	lut_access_type Access type. 1'd0: Read; 1'd1: Write.
16	RW	0x0	lut_table_id Access Id. 1'd0: LE LUT; 1'd1: LO LUT.
15:10	RO	0x00	reserved
9:0	RW	0x000	lut_addr Access address.

DPU_dpu_lut_access_data

Address: Operational Base(0xFF304000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	lut_access_data Configuration of LUT access data.

DPU_dpu_lut_cfg

Address: Operational Base(0xFF304000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:7	RW	0x0	lut_lo_le_mux
6	RW	0x0	lut_hybrid_priority LUT hybrid flow priority. 1'd0: LE LUT; 1'd1: LO LUT.
5	RW	0x0	lut_oflow_priority Priority when over flow happened. 1'd0: LE LUT; 1'd1: LO LUT.
4	RW	0x0	lut_uflow_priority Priority when under flow happened. 1'd0: LE LUT; 1'd1: LO LUT.
3:1	RO	0x0	reserved
0	RW	0x0	lut_road_sel LUT road sel. 1'd0: 1st; 1'd1: 2nd.

DPU_dpu_lut_info

Address: Operational Base(0xFF304000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	lut_lo_index_select LUT LO index selected. Used in index generator, choose some bits to be the index.
15:8	RW	0x00	lut_le_index_select LUT LE index selected. Used in index generator, choose some bits to be the index.
7:0	RO	0x00	reserved

DPU_dpu_lut_le_start

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Address: Operational Base(0xFF304000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	lut_le_start LE LUT start point.

DPU_dpu_lut_le_end

Address: Operational Base(0xFF304000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	lut_le_end LE LUT end point.

DPU_dpu_lut_lo_start

Address: Operational Base(0xFF304000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	lut_lo_start LO LUT start point.

DPU_dpu_lut_lo_end

Address: Operational Base(0xFF304000) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	lut_lo_end LO LUT end point.

DPU_dpu_lut_le_slope_scale

Address: Operational Base(0xFF304000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	lut_le_slope_oflow_scale LE LUT slope scale if over flow.
15:0	RW	0x0000	lut_le_slope_uflow_scale LE LUT slope scale if under flow.

DPU_dpu_lut_le_slope_shift

Address: Operational Base(0xFF304000) + offset (0x0124)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:5	RW	0x00	lut_le_slope_oflow_shift LE LUT slope shift if over flow.
4:0	RW	0x00	lut_le_slope_uflow_shift LE LUT slope shift if under flow.

DPU_dpu_lut_lo_slope_scale

Address: Operational Base(0xFF304000) + offset (0x0128)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	lut_lo_slope_oflow_scale LO LUT slope scale if over flow.
15:0	RW	0x0000	lut_lo_slope_uflow_scale LO LUT slope scale if under flow.

DPU_dpu_lut_lo_slope_shift

Address: Operational Base(0xFF304000) + offset (0x012C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:5	RW	0x00	lut_lo_slope_oflow_shift LO LUT slope shift if over flow.
4:0	RW	0x00	lut_lo_slope_uflow_shift LO LUT slope shift if under flow.

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DPU_RDMA_dpu_rdma_s_status

Address: Operational Base(0xFF305000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RO	0x0	status_1 Executer 1 status. 2'd0: Executer 1 is in idle state; 2'd1: Executer 1 is operating; 2'd2: Executer 1 is operating, executer 1 is waiting to operate; 2'd3: Reserved.
15:2	RO	0x0000	reserved
1:0	RO	0x0	status_0 Executer 0 status. 2'd0: Executer 0 is in idle state; 2'd1: Executer 0 is operating; 2'd2: Executer 0 is operating, executer 1 is waiting to operate; 2'd3: Reserved.

DPU_RDMA_dpu_rdma_s_pointer

Address: Operational Base(0xFF305000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RO	0x0	executer Which register group to be used. 1'd0: Executer group 0; 1'd1: Executer group 1.
15:6	RO	0x000	reserved
5	W1C	0x0	executer_pp_clear Clear executer group pointer. Set this bit to 1 to clear pointer to 0.
4	W1C	0x0	pointer_pp_clear Clear register group pointer. Set this bit to 1 to clear pointer to 0.
3	RW	0x0	pointer_pp_mode Register group ping-pong mode. 1'd0: Pointer ping-pong by executer; eg. if current executer is 0, next pointer will toggle to 1; 1'd1: Pointer ping-pong by pointer; eg. if current pointer is 0, next pointer will toggle to 1.
2	RW	0x0	executer_pp_en Executer group ping-pong enable. 1'd0: Disable; 1'd1: Enable.
1	RW	0x0	pointer_pp_en Register group ping-pong enable. 1'd0: Disable; 1'd1: Enable.
0	RW	0x0	pointer Which register group ready to be set. 1'd0: Register group 0; 1'd1: Register group 1.

DPU_RDMA_dpu_rdma_operation_enable

Address: Operational Base(0xFF305000) + offset (0x0008)

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Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	op_en Set this register will trigger DPU_RDMA block operate. This register and after this are all shadowed for ping-pong operation. 1'd0: Disable; 1'd1: Enable.

DPU_RDMA_dpu_rdma_data_cube_width

Address: Operational Base(0xFF305000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	width Input feature width (need to minus 1).

DPU_RDMA_dpu_rdma_data_cube_height

Address: Operational Base(0xFF305000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	height Input feature height (need to minus 1).

DPU_RDMA_dpu_rdma_data_cube_channel

Address: Operational Base(0xFF305000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	channel Input feature channel (need to minus 1).

DPU_RDMA_dpu_rdma_src_base_addr

Address: Operational Base(0xFF305000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_base_addr Fly mode source address.

DPU_RDMA_dpu_rdma_brdma_cfg

Address: Operational Base(0xFF305000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	brdma_data_src
7:5	RO	0x0	reserved
4:1	RW	0x0	brdma_data_use How many data type need to be read. [0]: If read ALU operand, set 1 to enable; [1]: If read CPEND operand, set 1 to enable; [2]: If read MUL operand, set 1 to enable; [3]: If read TRT operand, set 1 to enable.
0	RO	0x0	reserved

DPU_RDMA_dpu_rdma_bs_base_addr

Address: Operational Base(0xFF305000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	bs_base_addr Base address to read BS ALU, BS CPEND, BS MUL operand.

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DPU_RDMA_dpu_rdma_nrdma_cfg

Address: Operational Base(0xFF305000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	nrdma_data_src
7:5	RO	0x0	Reserved
4:1	RW	0x0	nrdma_data_use How many data type need to be read. [0]: If read ALU operand, set 1 to enable; [1]: If read CPEND operand, set 1 to enable, (tie to 0, cause BN do not have CPEND); [2]: If read MUL operand, set 1 to enable; [3]: If read TRT operand, set 1 to enable.
0	RO	0x0	Reserved

DPU_RDMA_dpu_rdma_bn_base_addr

Address: Operational Base(0xFF305000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	bn_base_addr Base address to read BN ALU, BN MUL operand.

DPU_RDMA_dpu_rdma_erdma_cfg

Address: Operational Base(0xFF305000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	erdma_data_mode If the read data is per channel or per pixel 2'd0: Per channel; 2'd1: Per pixel; 2'd2: Per channel by pixel; 2'd3: Reserved.
29	RW	0x0	erdma_surf_mode Surface mode of the EW cube. 1'd0: 1 surface series; 1'd1: 2 surface series.
28	RW	0x0	erdma_nonalign If read the EW cube in non-align mode. 1'd0: Do not use non-align mode; 1'd1: Use non-align mode.
27:4	RO	0x000000	reserved
3:2	RW	0x0	erdma_data_size What the precision of the cube that the ERDMA read. 2'd0: 4bit; 2'd1: 8bit; 2'd2: 16bit; 2'd3: 32bit.
1	RW	0x0	ov4k_bypass Separate the burst command of over 4k to 2 independent burst commands. 1'd0: Enable this feature; 1'd1: Bypass this feature.
0	RW	0x0	erdma_disable If disable ERDMA. 1'd0: Do not disable ERDMA; 1'd1: Disable ERDMA.

DPU_RDMA_dpu_rdma_ew_base_addr

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Address: Operational Base(0xFF305000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ew_base_addr Base address to read EW operand.

DPU_RDMA_dpu_rdma_ew_surf_stride

Address: Operational Base(0xFF305000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ew_surf_stride The surface stride of the element wise feature map; If erdma_data_mode is per channel, it need set to be 1.

DPU_RDMA_dpu_rdma_feature_mode_cfg

Address: Operational Base(0xFF305000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RW	0x0	nrdma_fix_addr
20	RW	0x0	brdma_fix_addr
19:18	RO	0x0	reserved
17:15	RW	0x0	in_precision Input data precision. 3'd0: Integer 8bit; 3'd1: Integer 16bit; 3'd2: Gloat point 16bit; 3'd3: Bfloat 16bit; 3'd4: Integer 32bit; 3'd5: Float point 32bit; 3'd6: Integer 4bit.
14:11	RW	0x0	burst_len Burst length. 4'd3: Burst4; 4'd7: Burst8; 4'd15: Burst16.
10:8	RW	0x0	comb_use If enable combine use and where the response data goes. 3'b000: Disable combine read; 3'b011: Enable combine read and data goes to MRDMA; 3'b101: Enable combine read and data goes to ERDMA; Others: Reserved.
7:5	RW	0x0	proc_precision Process precision. 3'd0: Integer 8bit; 3'd1: Integer 16bit; 3'd2: Float point 16bit; 3'd3: Bfloat 16bit; 3'd4: Integer 32bit; 3'd5: Float point 32bit; 3'd6: Integer 4bit.
4	RW	0x0	mrdma_disable If disable MRDMA. 1'd0: Do not disable MRDMA; 1'd1: Disable MRDMA.

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Bit	Attr	Reset Value	Description
3	RW	0x0	mrdma_fp16tofp32_en If enable DPU input from fp16 to fp32 or if the integer data is signed. 1'd0: Do not change data from fp16 to fp32, or the integer data is unsigned; 2'd1: Do change froma fp16 to fp32, or the integer data is signed.
2:1	RW	0x0	conv_mode Convolution mode. 2'd0: Dc; 2'd1: Reserved; 2'd2: Reserved; 2'd3: Depthwise.
0	RW	0x0	flying_mode Flying mode enable. 1'd0: DPU core main data is from convolution output; 1'd1: DPU core main data is from MRDMA.

DPU_RDMA_dpu_rdma_src_dma_cfg

Address: Operational Base(0xFF305000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RW	0x0	pooling_method Pooling method 1'd0: Average pooling (up sampling can use this mode); 1'd1: Min or max pooling.
12	RW	0x0	unpooling_en If enable un-pooling.
11:9	RW	0x0	kernel_stride_height Un-pooling kernel stride height (minus 1).
8:6	RW	0x0	kernel_stride_width Un-pooling kernel stride width (minus 1).
5:3	RW	0x0	kernel_height Un-pooling kernel height (minus 1).
2:0	RW	0x0	kernel_width Un-pooling kernel width (minus 1).

DPU_RDMA_dpu_rdma_surf_notch

Address: Operational Base(0xFF305000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	surf_notch_addr How many pixels from the end of this process feature map to the end of the shape feature map.

DPU_RDMA_dpu_rdma_pad_cfg

Address: Operational Base(0xFF305000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	pad_value Pad value.
15:7	RO	0x000	reserved
6:4	RW	0x0	pad_top Un-pooling top pad.
3	RO	0x0	reserved
2:0	RW	0x0	pad_left Un-pooling left pad.

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DPU_RDMA_dpu_rdma_ew_surf_notch

Address: Operational Base(0xFF305000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ew_surf_notch Surface notch of EW.

DPU_RDMA_dpu_rdma_line_notch

Address: Operational Base(0xFF305000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	line_notch_addr

DPU_RDMA_dpu_rdma_ew_line_notch

Address: Operational Base(0xFF305000) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	ew_line_notch_addr

PPU_ppu_s_status

Address: Operational Base(0xFF306000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RO	0x0	status_1 Executer 1 status. 2'd0: Executer 1 is in idle state; 2'd1: Executer 1 is operating; 2'd2: Executer 1 is operating, executer 1 is waiting to operate; 2'd3: Reserved.
15:2	RO	0x0000	reserved
1:0	RO	0x0	status_0 Executer 0 status. 2'd0: Executer 0 is in idle state; 2'd1: Executer 0 is operating; 2'd2: Executer 0 is operating, executer 1 is waiting to operate; 2'd3: Reserved.

PPU_ppu_s_pointer

Address: Operational Base(0xFF306000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RO	0x0	executer Which register group to be used. 1'd0: Executer group 0; 1'd1: Executer group 1.
15:6	RO	0x000	reserved
5	W1C	0x0	executer_pp_clear Clear executer group pointer. Set this bit to 1 to clear pointer to 0.
4	W1C	0x0	pointer_pp_clear Clear register group pointer. Set this bit to 1 to clear pointer to 0.

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Bit	Attr	Reset Value	Description
3	RW	0x0	pointer_pp_mode Register group ping-pong mode. 1'd0: Pointer ping-pong by executer; eg. if current executer is 0, next pointer will toggle to 1; 1'd1: Pointer ping-pong by pointer; eg. if current pointer is 0, next pointer will toggle to 1.
2	RW	0x0	executer_pp_en Executer group ping-pong enable. 1'd0: Disable; 1'd1: Enable.
1	RW	0x0	pointer_pp_en Register group ping-pong enable. 1'd0: Disable; 1'd1: Enable.
0	RW	0x0	pointer Which register group ready to be set. 1'd0: Register group 0; 1'd1: Register group 1.

PPU_ppu_operation_enable

Address: Operational Base(0xFF306000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	op_en Set this register will trigger PPU block operate. This register and after this are all shadowed for ping-pong operation. 1'd0: Disable; 1'd1: Enable.

PPU_ppu_data_cube_in_width

Address: Operational Base(0xFF306000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	cube_in_width Pooling cube width (need to minus 1).

PPU_ppu_data_cube_in_height

Address: Operational Base(0xFF306000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	cube_in_height Pooling cube height (need to minus 1).

PPU_ppu_data_cube_in_channel

Address: Operational Base(0xFF306000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	cube_in_channel Pooling cube channel (need to minus 1).

PPU_ppu_data_cube_out_width

Address: Operational Base(0xFF306000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x0000	cube_out_width Pooling output cube width (need to minus 1).

PPU_ppu_data_cube_out_height

Address: Operational Base(0xFF306000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	cube_out_height Pooling output cube height (need to minus 1).

PPU_ppu_data_cube_out_channel

Address: Operational Base(0xFF306000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	cube_out_channel Pooling output cube channel (need to minus 1).

PPU_ppu_operation_mode_cfg

Address: Operational Base(0xFF306000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	index_en If enable output the position of each kernel. 1'd0: Disable; 1'd1: Enable.
29	RO	0x0	reserved
28:16	RW	0x0000	notch_addr How many pixels from the end of the width end to the shape line end.
15:8	RO	0x00	reserved
7:5	RW	0x0	use_cnt Use_cnt.
4	RW	0x0	flying_mode Where the pooling cube from. 1'd0: DPU; 1'd1: Outside.
3	RW	0x0	pad_exclude
2	RO	0x0	reserved
1:0	RW	0x0	pooling_method Pooling method. 2'd0: Average pooling; 2'd1: Max pooling; 2'd2: Min pooling; 2'd3: Reserved.

PPU_ppu_pooling_kernel_cfg

Address: Operational Base(0xFF306000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:20	RW	0x0	kernel_stride_height Pooling kernel stride height (need to minus 1).
19:16	RW	0x0	kernel_stride_width Pooling kernel stride width (need to minus 1).
15:11	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
10:8	RW	0x0	kernel_height Pooling kernel height (need to minus 1).
7:3	RO	0x00	reserved
2:0	RW	0x0	kernel_width Pooling kernel width (need to minus 1).

PPU_ppu_recip_kernel_width

Address: Operational Base(0xFF306000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RW	0x00000	recip_kernel_width The Reciprocal of the shape kernel width multiple 2^16.

PPU_ppu_recip_kernel_height

Address: Operational Base(0xFF306000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RW	0x00000	recip_kernel_height The Reciprocal of the shape kernel height multiple 2^16.

PPU_ppu_pooling_padding_cfg

Address: Operational Base(0xFF306000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:12	RW	0x0	pad_bottom Pooling bottom pad.
11	RO	0x0	reserved
10:8	RW	0x0	pad_right Pooling right pad.
7	RO	0x0	reserved
6:4	RW	0x0	pad_top Pooling top pad.
3	RO	0x0	reserved
2:0	RW	0x0	pad_left Pooling left pad.

PPU_ppu_padding_value_1_cfg

Address: Operational Base(0xFF306000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RW	0x00000	pad_value_1x Pad_value*1 [31:0].

PPU_ppu_padding_value_2_cfg

Address: Operational Base(0xFF306000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RW	0x00000	pad_value_2x Pad_value*1 [34:32].

PPU_ppu_padding_value_3_cfg

Address: Operational Base(0xFF306000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
18:0	RW	0x00000	pad_value_3x

PPU_ppu_padding_value_4_cfg

Address: Operational Base(0xFF306000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RW	0x00000	pad_value_4x

PPU_ppu_padding_value_5_cfg

Address: Operational Base(0xFF306000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RW	0x00000	pad_value_5x

PPU_ppu_padding_value_6_cfg

Address: Operational Base(0xFF306000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RW	0x00000	pad_value_6x

PPU_ppu_padding_value_7_cfg

Address: Operational Base(0xFF306000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RW	0x00000	pad_value_7x

PPU_ppu_back_con_0

Address: Operational Base(0xFF306000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	ppu_back_en
19:17	RO	0x0	reserved
16	RW	0x0	dpu_back_en
15:11	RO	0x00	reserved
10:8	RW	0x0	ppu_out_precision
7	RO	0x0	reserved
6:4	RW	0x0	ppu_proc_precision
3:2	RO	0x0	reserved
1:0	RW	0x0	ppu_conv_mode

PPU_ppu_back_con_1

Address: Operational Base(0xFF306000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	ppu_height
15:13	RO	0x0	reserved
12:0	RW	0x0000	ppu_width

PPU_ppu_back_con_2

Address: Operational Base(0xFF306000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	ppu_back_bank_st
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x0000	ppu_channel

PPU_ppu_back_con_3

Address: Operational Base(0xFF306000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	ppu_entries
15:14	RO	0x0	reserved
13:0	RW	0x0000	ppu_entries_pergroup

PPU_ppu_dst_base_addr

Address: Operational Base(0xFF306000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	dst_base_addr Base address the output cube goes.
3:0	RO	0x0	reserved

PPU_ppu_dst_surf_stride

Address: Operational Base(0xFF306000) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	dst_surf_stride Output shape area.
3:0	RO	0x0	reserved

PPU_ppu_data_format

Address: Operational Base(0xFF306000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	index_add If index_en enable, this register is dst_surface_stride x number of cube surface (every 8bytes per surface), else it equals to dst_surface_stride.
3	RW	0x0	dpu_flyin If the data from DPU, and DPU data is from outside, this bit set to be 1.
2:0	RW	0x0	proc_precision Process precision.

PPU_ppu_misc_ctrl

Address: Operational Base(0xFF306000) + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	surf_len Surface count length.
15:9	RO	0x00	reserved
8	RW	0x0	mc_surf_out If enable multiple surfaces out. 1'd0: Disable; 1'd1: Enable.
7	RW	0x0	nonalign If enable non-align mode. 1'd0: Disable; 1'd1: Enable.
6:4	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	burst_len Burst length 4'd3: Burst4; 4'd7: Burst8; 4'd15: Burst16.

PPU_RDMA_ppu_rdma_s_status

Address: Operational Base(0xFF307000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RO	0x0	status_1 Executer 1 status. 2'd0: Executer 1 is in idle state; 2'd1: Executer 1 is operating; 2'd2: Executer 1 is operating, executer 1 is waiting to operate; 2'd3: Reserved.
15:2	RO	0x0000	reserved
1:0	RO	0x0	status_0 Executer 0 status. 2'd0: Executer 0 is in idle state; 2'd1: Executer 0 is operating; 2'd2: Executer 0 is operating, executer 1 is waiting to operate; 2'd3: Reserved.

PPU_RDMA_ppu_rdma_s_pointer

Address: Operational Base(0xFF307000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RO	0x0	executer Which register group to be used. 1'd0: Executer group 0; 1'd1: Executer group 1.
15:6	RO	0x000	reserved
5	W1C	0x0	executer_pp_clear Clear executer group pointer. Set this bit to 1 to clear pointer to 0.
4	W1C	0x0	pointer_pp_clear Clear register group pointer. Set this bit to 1 to clear pointer to 0.
3	RW	0x0	pointer_pp_mode Register group ping-pong mode. 1'd0: Pointer ping-pong by executer; eg. if current executer is 0, next pointer will toggle to 1; 1'd1: Pointer ping-pong by pointer; eg. if current pointer is 0, next pointer will toggle to 1.
2	RW	0x0	executer_pp_en Executer group ping-pong enable. 1'd0: Disable; 1'd1: Enable.
1	RW	0x0	pointer_pp_en Register group ping-pong enable. 1'd0: Disable; 1'd1: Enable.

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Bit	Attr	Reset Value	Description
0	RW	0x0	pointer Which register group ready to be set. 1'd0: Register group 0; 1'd1: Register group 1.

PPU_RDMA_ppu_rdma_operation_enable

Address: Operational Base(0xFF307000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	op_en Set this register will trigger PPU_RDMA block operate. This register and after this are all shadowed for ping-pong operation. 1'd0: Disable; 1'd1: Enable.

PPU_RDMA_ppu_rdma_cube_in_width

Address: Operational Base(0xFF307000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	cube_in_width Pooling cube width (need to minus 1).

PPU_RDMA_ppu_rdma_cube_in_height

Address: Operational Base(0xFF307000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	cube_in_height Pooling cube height (need to minus 1).

PPU_RDMA_ppu_rdma_cube_in_channel

Address: Operational Base(0xFF307000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	cube_in_channel Pooling cube channel (need to minus 1).

PPU_RDMA_ppu_rdma_src_base_addr

Address: Operational Base(0xFF307000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	src_base_addr Base address of the pooling cube.

PPU_RDMA_ppu_rdma_src_line_stride

Address: Operational Base(0xFF307000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	src_line_stride Pooling cube shape width.
3:0	RO	0x0	reserved

PPU_RDMA_ppu_rdma_src_surf_stride

Address: Operational Base(0xFF307000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	src_surf_stride Pooling cube shape area.

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Bit	Attr	Reset Value	Description
3:0	RO	0x0	reserved

PPU_RDMA_ppu_rdma_data_format

Address: Operational Base(0xFF307000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x1	wstrb_clr Usefull in int4 data, recommended set to be 1.
7	RO	0x0	reserved
6:4	RW	0x4	read_size Default 4. When read int4 data, this regfile should be 3.
3	RO	0x0	reserved
2:0	RW	0x0	in_precision Input precision. 3'd0: Int8; 3'd6: Int4; Else: Reserved.

DDMA_ddma_cfg_outstanding

Address: Operational Base(0xFF308000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	rd_os_cnt Max numbers of read outstanding.

DDMA_ddma_rd_weight_0

Address: Operational Base(0xFF308000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	rd_weight_pdp Weight of PPU read burst.
23:16	RW	0x00	rd_weight_dpu Weight of DPU read burst.
15:8	RW	0x00	rd_weight_kernel Weight of read weight burst.
7:0	RW	0x00	rd_weight_feature Weight of read feature burst.

DDMA_ddma_wr_weight_0

Address: Operational Base(0xFF308000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	wr_weight_pdp Write_weight_ppu.
7:0	RW	0x00	wr_weight_dpu Write_weight_dpu.

DDMA_ddma_cfg_id_error

Address: Operational Base(0xFF308000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:6	RW	0x0	wr_resp_id Error write id.
5	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
4:0	RW	0x00	rd_resp_id Error read id.

DDMA_ddma_rd_weight_1

Address: Operational Base(0xFF308000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31	RW	0x0	monitor_clear Clear the monitor counter.
30:8	RO	0x000000	reserved
7:0	RW	0x00	rd_weight_pc Weight of PC read burst.

DDMA_ddma_cfg_dma_fifo_clr

Address: Operational Base(0xFF308000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	dma_fifo_clr Clear DMA FIFO.

DDMA_ddma_cfg_dma_arb

Address: Operational Base(0xFF308000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	wr_arbit_model Write_arbit_model.
8	RW	0x0	rd_arbit_model Read_arbit_model.
7	RO	0x0	reserved
6:4	RW	0x0	wr_fix_arb Write_fix_arb.
3	RO	0x0	reserved
2:0	RW	0x0	rd_fix_arb Read_fix_arb.

DDMA_ddma_cfg_dma_rd_qos

Address: Operational Base(0xFF308000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RW	0x0	rd_pc_qos Read_pc_qos.
7:6	RW	0x0	rd_ppu_qos Read_ppu_qos.
5:4	RW	0x0	rd_dpu_qos Read_dpu_qos.
3:2	RW	0x0	rd_kernel_qos Read_kernel_qos.
1:0	RW	0x0	rd_feature_qos Read feature_qos.

DDMA_ddma_cfg_dma_rd_cfg

Address: Operational Base(0xFF308000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	rd_arlock Read_arlock.

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Bit	Attr	Reset Value	Description
11:8	RW	0x0	rd_arcache Read_arcache.
7:5	RW	0x0	rd_arprot Read_arprot.
4:3	RW	0x0	rd_arburst Read_arburst.
2:0	RW	0x0	rd_arsize Read_arsize.

DDMA_ddma_cfg_dma_wr_cfg

Address: Operational Base(0xFF308000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	wr_wstrb_sft wr_wstrb shift.
15:13	RO	0x0	reserved
12	RW	0x0	wr_awlock Write_awlock. tied to 0x0.
11:8	RW	0x0	wr_awcache Write awcache. tied to 0x0.
7:5	RW	0x0	wr_awprot Write_awprot. tied to 0x0.
4:3	RW	0x1	wr_awburst Write_awburst. tied to 0x1.
2:0	RW	0x4	wr_awsize Write_awsize. 0:8bits, 1:16bits, 2:32bits, 3:64bits, 4:128bits

DDMA_ddma_cfg_dma_wstrb

Address: Operational Base(0xFF308000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	RW	0xffffffff	wr_wstrb Write_wstrb. lower 16bits works.

DDMA_ddma_cfg_status

Address: Operational Base(0xFF308000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	idel Idel.
7:0	RO	0x00	reserved

DDMA_ddma_fd_write_bw

Address: Operational Base(0xFF308000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	fd_write_bw

DDMA_ddma_fd_read_bw

Address: Operational Base(0xFF308000) + offset (0x0038)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	fd_read_bw

DDMA_ddma_wt_read_bw

Address: Operational Base(0xFF308000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wt_read_bw

GLOBAL_global_op_en

Address: Operational Base(0xFF30F000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	ppu_rdma_op_en PPU_RDMA operation enable signal.
5	RW	0x0	ppu_op_en PPU operation enable signal.
4	RW	0x0	dpu_rdma_op_en DPU_RDMA operation enable signal.
3	RW	0x0	dpu_op_en DPU operation enable signal.
2	RW	0x0	core_op_en CORE operation enable signal.
1	RO	0x0	reserved
0	RW	0x0	cna_op_en CNA operation enable signal.

9.5 Application Notes

9.5.1 Ping-pong registers

To reduce the time of fetching register lists, every Calculate Core and Control Core of RKNN has two group independent ping-pong registers. The ping-pong registers, group0 and group1, can be write alternatively while the corresponding group is in the workmode (e.g., group 0 registers can be configured while RKNN Cores are working with group 1 registers). As a result, the register-fetching time can be hidden. S_POINTER register should be written every block to enable this function.

9.5.2 Clock and Reset

9.5.2.1 Clock Domains

RKNN has two clock domains: AHB clock domain and AXI clock domain. AHB clock is the clock for AHB interface, while AXI clock is the clock for AXI interface. AXI clock is also used as core clock of all Calculate Core and Control Cores. Clock frequency can be controlled by CRU(can be referred in the relevant sections). Automatic localized clock gating is employed throughout the design to minimize dynamic power consumption. Almost all of the flip-flops are clock gated in the design. Besides, block level clock gating is also implemented. When the block and interface to the block are both idle, clock of the block will be gated automatically. This feature can be disabled by software.

9.5.2.2 NPU Reset

Corresponding to the two clock domain, there are two reset signals: Aresetn and Hresetn. Aresetn is the reset signal for AXI interface and all Calculate and Control Cores. Hresetn is AHB interface reset pin and which is synchronized to the AHB clock domain.
All the two signals must be asserted for a minimum of 32 core clock cycles, using the slowest of the two clocks. Then two signals must be release at the same time.

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9.5.3 NPU Interrupt Application

RKNN has 1 interrupt output signal and will remain asserted until the host processor clears the interrupt. Each bit of PC_INTERRUPT_STATUS represents one of the 17 possible events that the RKNN can signal to the host processor. By setting the bits of the interrupt enable register (PC_INTERRUPT_MASK) the programmer can control which of those events will generate an interrupt.

9.5.4 NPU operate flow

RKNN has two work modes: slave configured mode and pc work mode. In pc work mode, register information needs to be initialized in the system memory, and then the flowing flows should be followed.
The information of registers initialized in the system memory is the op you want to specify. And we describe the normal work flows by describe the slave configured mode.

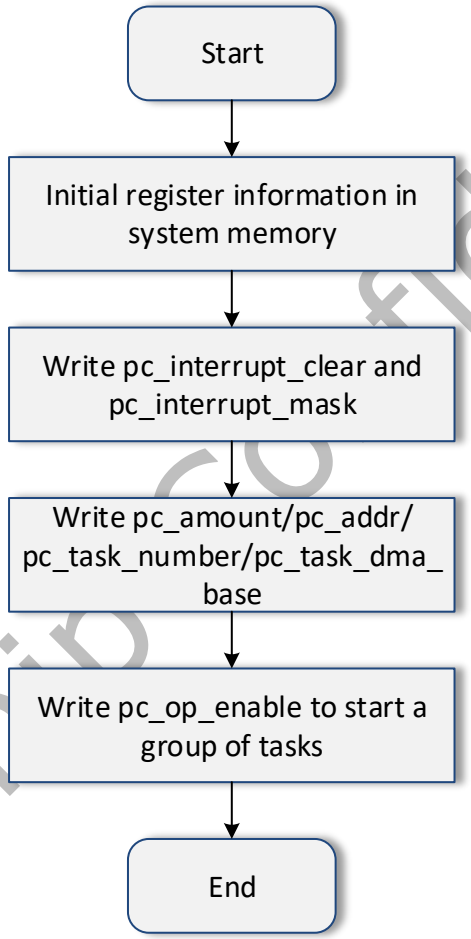


Fig.9-2 PC flow

9.5.5 Convolution flow

RKNN supports a variety of convolution and matrix multiplication. The following work flow should be obeyed when using the MAC array to do calculation,and if using DPU CORE, the work flow 2 should be obeyed.

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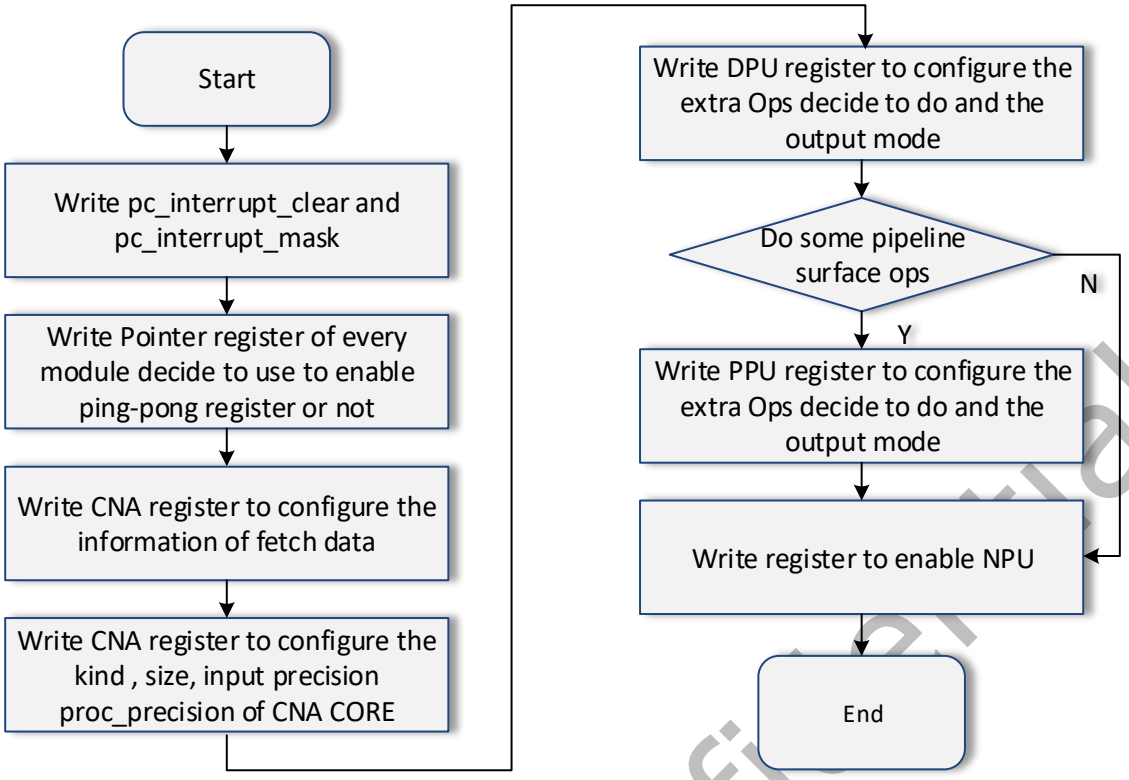


Fig.9-3 Convolution flow 1

In step 1, do not set PPU mask bit if PPU is not used.
In step 3, you need to configure the size of feature map, and the input precision, process precision, grains, entries and weight size, as well as weight height, weight width, kernels and weight bytes etc.
In step 4, you need to configure processing precision, conv_mode and auto gating registers of CMAC and CNA sequence controller.
In step 5, you should specify some operators to the outputs of convolution according to configure the DPU_CORE. DPU CORE has some fixed operators, you can also specify other programmed operators.
In step 6, extra operators can be done with the outputs of DPU, pooling for example.

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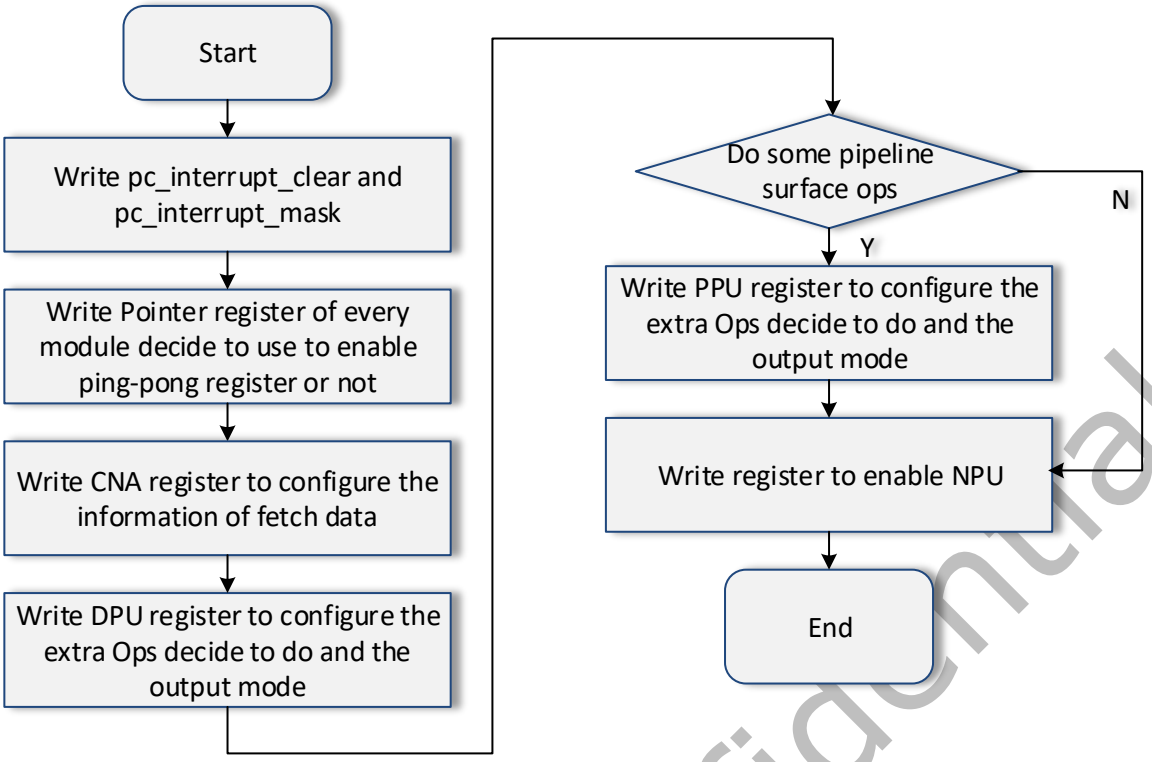


Fig.9-4 Convolution flow 2

In step 3, you need to configure the size of feature map, input precision, process precision, grains, entries, and weight size, as well as height, width, kernels and weight bytes etc. Here we supply zero skipping switch, if there's a lot of zero or some number else in the feature map, you can enable zero skipping by writing cna_fc_con0, cna_fc_con1 and cna_fc_con2, therefore correspond weights of the pixel in the feature map will not be read. In zero skipping mode, you can specify the feature map size for read different from the feature map size for calculate.

If enable zero skipping, the conv_mode of DPU must configure to be 3 and must bypass the BS_CORE. The alu_src must set to be 0, the mul_src must set to be 1, and the alu_algo must set be 3. We bypass BS_CORE, and use BN_CORE to calculate convolution, so the extra operators must achieve by EW_CORE. But we use NRDMA to read operands to EW_CORE when ew_src is 1.

9.5.6 Pooling flow

You can use PPU in two ways, pipeline with DPU, and flying mode independently. The first one is described above, we describe the second flow below.

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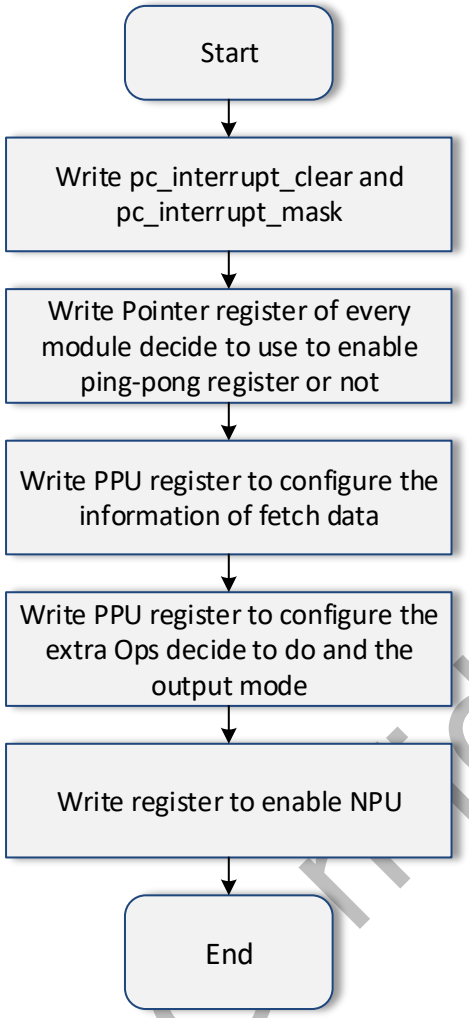


Fig.9-5 Pooling flow

In step 4, we supply two type of output mode, 8byte align per pixel and non-align mode. In some case with uncomfortable feature map size, you can enable non-align mode by writing ppu_misc_ctrl_nonalign and ppu_misc_ctrl_surf_len.

9.5.7 Separate op flow

As for the operators that RKNN do not fixed, you can combine DPU and PPU to achieve it. In the following section we describe the DPU flying mode flow.

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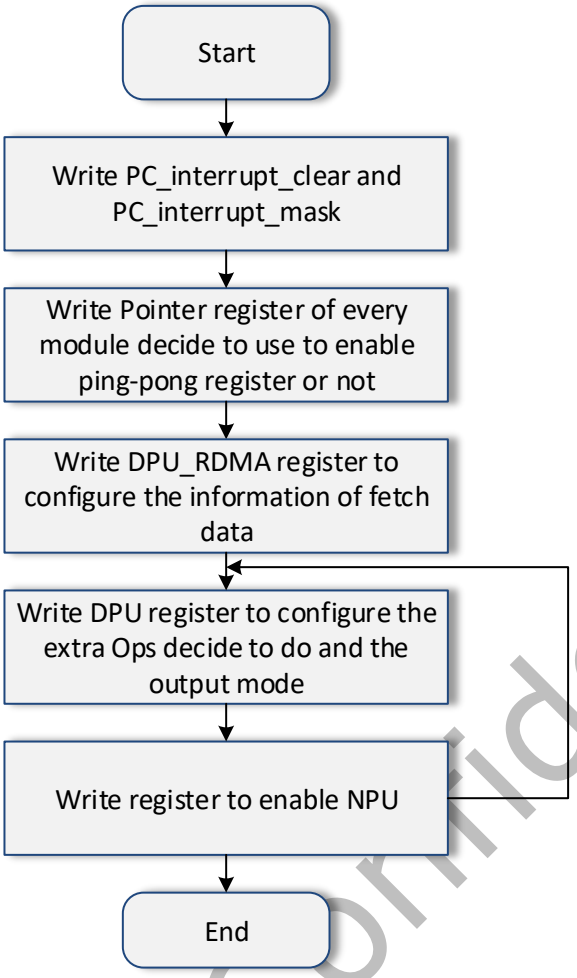


Fig.9-6 DPU flying mode flow

In step 3, you can enable MRDMA, BRDMA, NRDMA, ERDMA to fetch data. RKNN supports 6 types of data input precision.

In step 4, you can configure BS_ALU_BYPASS, BS_MUL_BYPASS, BS_RELU_BYPASS, BS_MUL_PRELU, BS_MUL_SHIFT, BS_RELUX_EN etc. to specify the operators you want to achieve.

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Chapter 10 VPU

10.1 Overview

VPU is composed by VDPU382, VDPU720 and VEPU540 to realize the high quality video decoding and encoding.
VDPU382 is a multi-format video decoder which supports H265, H264 and VP9, max solution is up 32Kx32K.
VDPU720 is JPEG decoder.
VEPU540 is H264 and JPEG video encoder.

10.1.1 Feature

The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

The features of VDPU382 decoder are listed as follows:

- MMU embedded with MMU interrupt support
- H.265 HEVC/MVC Main Profile yuv420@L5.0 up to 4096x2304@30fps, max solution up to 32Kx32K
- H.264 AVC/MVC Main Profile yuv400/yuv420/422@L5.0 up to 1920x1080@60fps, max solution up to 32Kx32K
- VP9 Profile0 yuv420@L5.0 up to 4096x2304@30fps, max solution up to 32Kx32K

The features of VDPU720 decoder are listed as follows:

- Supports JPEG decoding
  - 48x48 to 65536x65536(4295Mpixels), Step size 8 pixels
  - Baseline interleaved, and support DRI decode

The features of VEPU540 are listed as follows:

- H.264 High Profile, level 4.2
- Supports JPEG encoding
- Resolution upto 8192x8192
- Bitrate upto 200Mbps with CBR/VBR/FixQP/QPMAP bitrate control
- YUV420 and YUV400 format
- Slice split
- Area and Block Mapping ROI
- Link table configuration mode
- YUV/RGB video source with crop, rotation and mirror
- MMU Inside

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10.2 Block Diagram

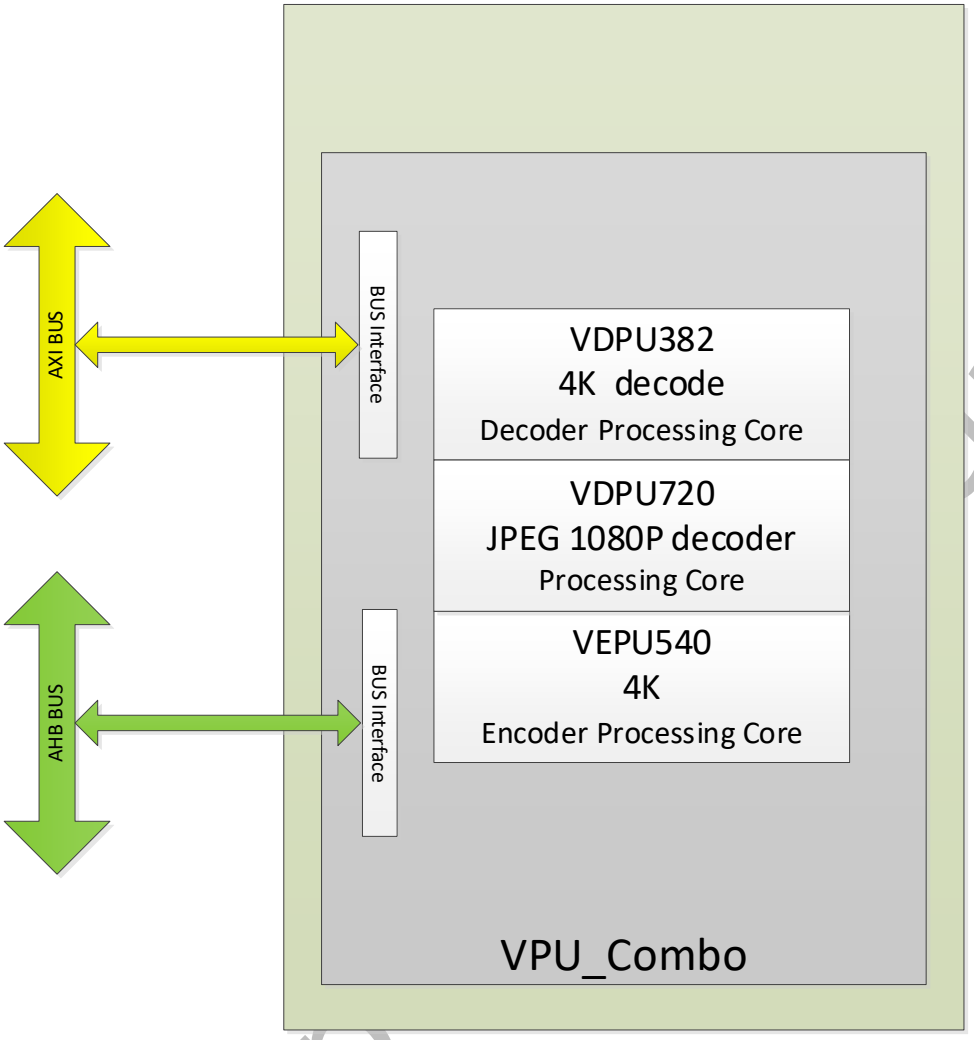


Fig.10-1 Combo Block Diagram

As shown in the figures above, CPU accesses to the decoder register bank through AHB bus. Bitstream and other necessary data are fed into processing core though AXI read channel, and after several steps of decoding process, decoded pictures and other information data are transferred to designated location in the DDR through AXI write channel.

VDPU382 decoder: can support h.265/vp9/h.264 video standard decoder, max solution is up 32Kx32K.

VDPU720 processing core support jpeg decoder.

VEPU540 encoder processing core can support H.264 and JPEG video encoder, max solution size is 8Kx8K

Please note that VDPU382 and VDPU720 and VEPU540 is different IP cores, so these processing core can be work together.

10.3 Video Frame Format

This chapter describes different input and output video frame formats supported by VCODEC. Each function module has its own supported video frame formats, and this chapter describes all the video frame formats.

10.3.1 YCbCr 4:2:0 Planar Format

In the planar format, each video sample component forms one memory plane. Within one plane, the data has to be stored linearly and contiguously in the memory as shown in fellows. The luminance samples are stored in raster-scan order (Y0Y1 Y2Y3 Y4….). The chrominance samples are stored in two planes also in raster scan order (Cb0Cb1 Cb2Cb3 Cb4…. and Cr0Cr1 Cr2Cr3 Cr4….). In this format each pixel takes 12 bits of memory.

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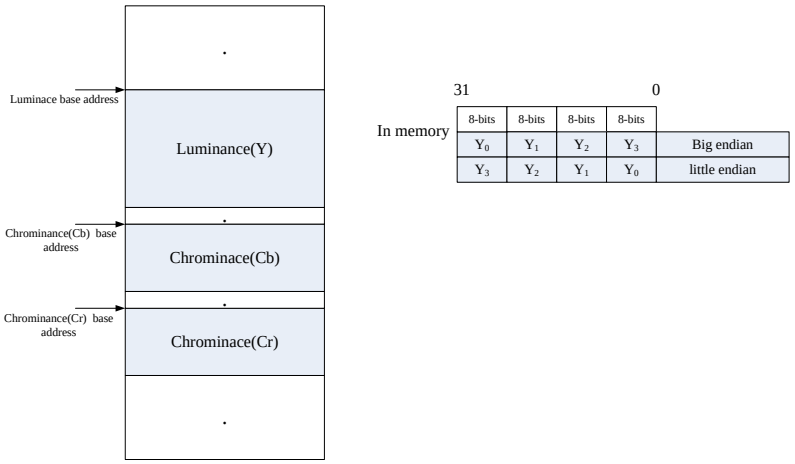


Fig.10-2 VCODEC YCbCr 4:2:0 planar format

10.3.2 YCbCr 4:2:0 Semi-Planar format

In semi-planar YcbCr4:2:0 format the luminance samples from one plane in memory, and chrominance samples from another. Within one plane, the data has to be stored linearly and contiguously in the memory. The luminance pixels are stored in raster-scan order (Y0Y1 Y2Y3 Y4….). The interleaved chrominance CbCr samples are stored in raster-scan order in memory as Cb0Cr0 Cb1Cr1 Cb2 Cr2 Cb3Cr3 Cb4 Cr4….

Semi-Planar format supports both progressive and interlaced format as presented in the following figure. The interlaced format may be alternative line or each line.

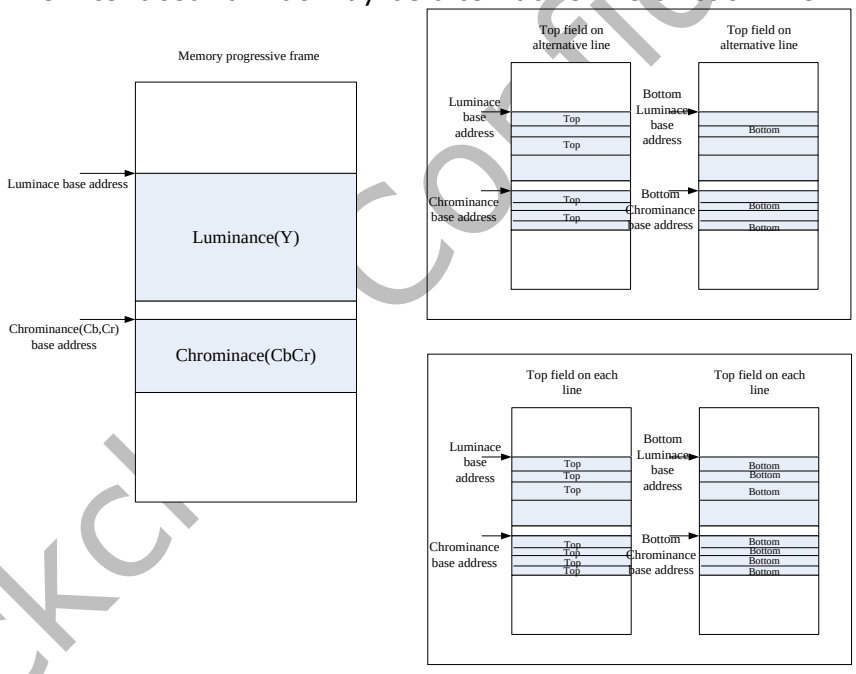


Fig.10-3 VCODEC YCbCr 4:2:0 Semi-planar format

10.3.3 YCbCr 4:2:2 Interleaved Format

In the interleaved YCbCr 4:2:2 format the pixel samples from a single plane in which the data has to be stored linearly and contiguously as shown in the following figure. The pixel data is in raster scan order and the chrominance samples are interleaved between the luminance samples as Y0Cb0 Y1Cr0 Y2 Cb1 Y3Cr1 Y4 Cb2…. YCrCb, CbYCrY and CrYCbY component orders are supported also. In this format, each pixel takes 16 bits in the memory.

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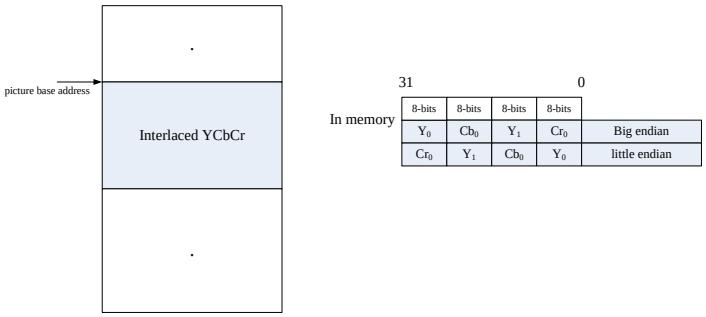


Fig.10-4 VCODEC YCbCr4:2:2 Interleaved format

10.3.4 YCbCr Tiled Semi-Planar Format

Like the YUV semi-planar format, the tiled semi-planar format is also organized in the memory on two separate planes. The difference between these formats is that in tiled format the pixel samples are not anymore in raster-scan order but are stored macroblock (16x16 pixels or 8x8 pixels) by macroblock. The samples of each macroblock are stored in consecutive addresses and the macroblocks are ordered from left to right and from top to down as the following figure shows. When this format used as input data format, it causes the lowest bus load to the system as there is minimal amount of non-sequential memory addressing required when reading the input data to the post-processor.

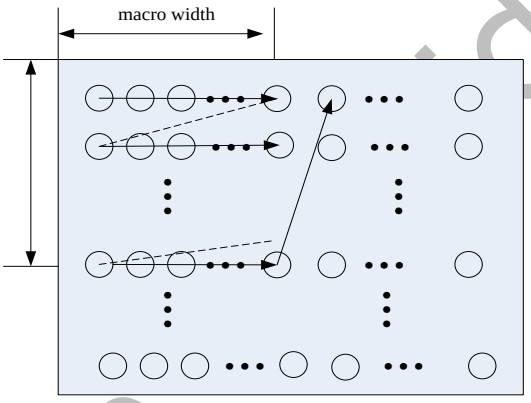


Fig.10-5 VCODEC Tile scan mode

10.3.5 RGB 16bpp Format

In this format each pixel is represented by 16 or less bits containing the red, blue and green samples. There are several 16bpp formats which use different number of bits for each sample. For example, the RGB 5-5-5 format uses 5 bits for each sample and 1 bit is left unused or can represent a transparency flag, where RGB 5-6-5 uses 6 bits for the G sample and 5 bits for R and B samples. Common for all 16bpp types is that two pixels fit into one 32-bit space.

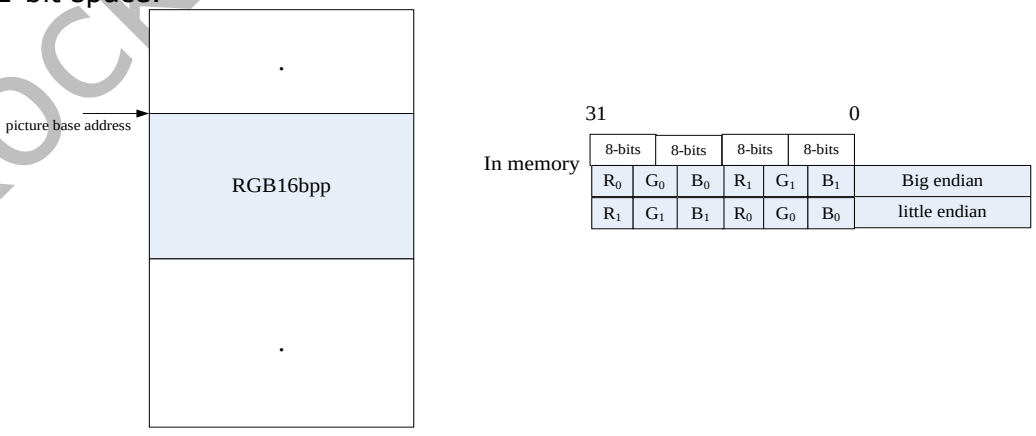


Fig.10-6 VCODEC RGB 16bpp format

10.3.6 RGB 32bpp Format

Any RGB format that has its pixels represented by more than 16bits each is considered to be of 32bpp type. Typically in this format each pixel is represented by three bytes containing a red, blue and green sample and a 4th byte which can be empty or hold an

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alpha blending value. Common for all 32bpp types is that only one pixel fit into one 32-bit space. The data has to be stored linearly and contiguously in the memory.

10.4 Function Description

10.4.1 MMU

The MMU divides memory into 4KB pages, where each page can be individually configured. For each page the following parameters are specified:

- Address translation of virtual memory, this enables the processor to work using address that differ from the physical address in the memory system.
- The permitted types of accesses to that page. Each page can permit read, write, both, or none.

The MMU use 2-level page table structure:

1. The first level, the page directory consists of 1024 directory table entries(DTEs), each pointing to a page table.
2. The second level, the page table consists of 1024 page table entries(PTEs), each pointing to a page in memory.

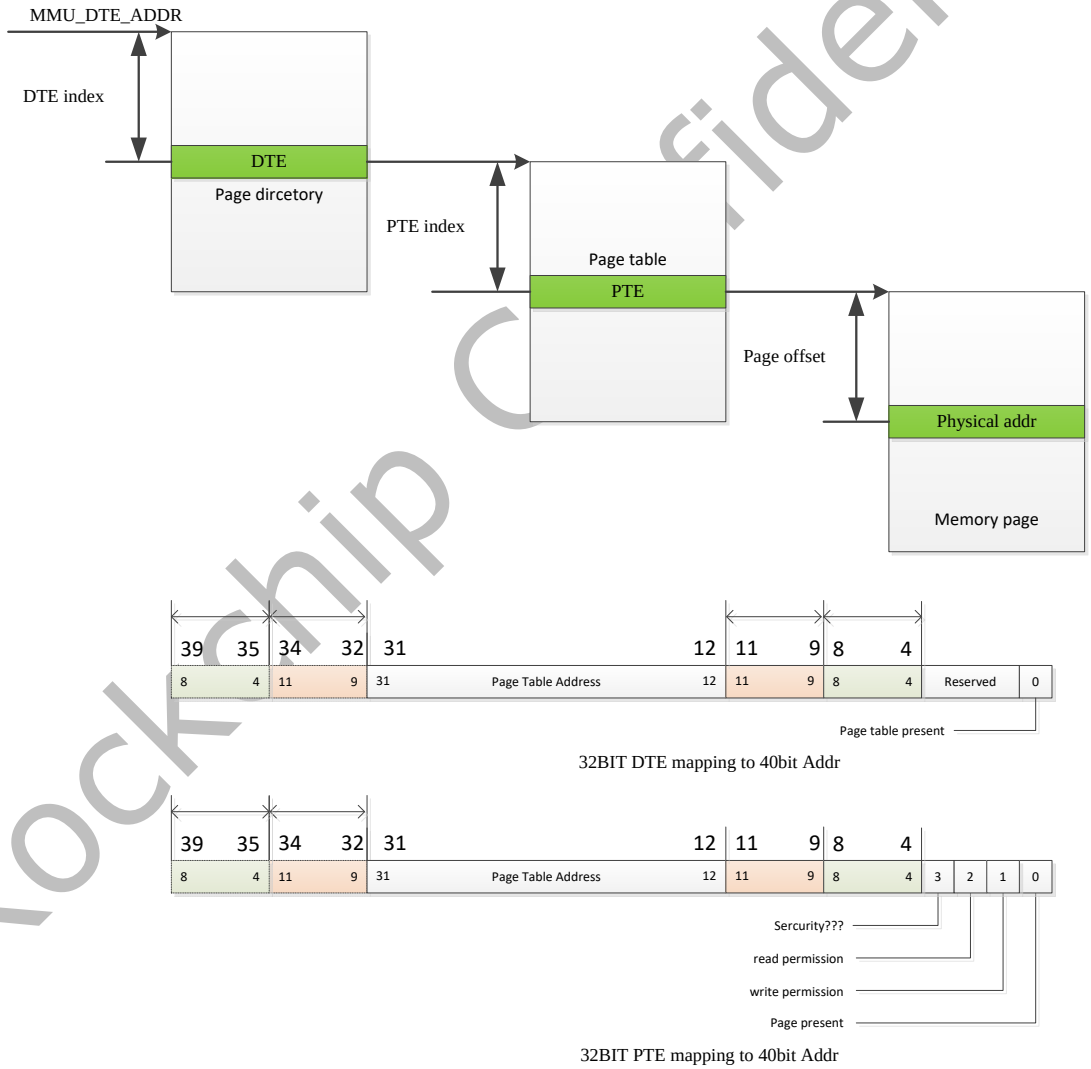


Fig.10-7 Structure of two-level page table

10.4.2 VDPU382 feature supported

1. H265/MVC

Table 10-1 Video H.265 decoder features

Feature	Decoder support
Input data format	H265 byte unit stream/MVC stream
Decoding scheme	Frame by frame

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Feature	Decoder support
Output data format	YCbCr 4:2:0 Semi-Planar YCbCr Tiled Semi-Planar(Scale Down work mode)
Supported image size	64x64 to 32kx32k step size 16pixels
Profile/level	Main level 5.0
Maximum frame rate	YCbCr 4:2:0 30fps @4096x2304
Maximum bit rate	400MBPS
Other feature	Error detection and concealment Linked List Pointer mode Scale Down work mode Qos mode W2DDR buffer performance statistics and analysis

2. H264/MVC

Table 10-2 Video H.264 decoder features

Feature	Decoder support
Input data format	H264byte or NAL unit stream/SVC stream/MVC stream
Decoding scheme	Frame by frame(or field by field) Slice by slice
Output data format	YCbCr 4:0:0 (monochrome) YCbCr 4:2:0 semi-planar raster-scan YCbCr 4:2:2 semi-planar raster-scan YCbCr Tiled Semi-Planar(Scale Down work mode)
Supported image size	16x16 to 32kx32k step size 16 pixels
Profile and Level	Main level 5.0
Maximum frame rate	60fps @1920x1080
Maximum bit rate	more than 250MBPS
Other feature	Error detection and concealment Linked List Pointer mode Scale Down work mode Qos mode W2DDR buffer performance statistics and analysis

3. VP9

Table 10-3 Video vp9 decoder features

Feature	Decoder support
Input data format	VP9 byte unit stream
Decoding scheme	Frame by frame
Output data format	YCbCr 4:2:0 Semi-Planar YCbCr Tiled Semi-Planar(Scale Down work mode)
Supported image size	64x64 to 4096x2304 step size 16pixels
Profile/level	Profile0 level 5.0
Maximum frame rate	30fps @4096x2304
Maximum bit rate	more than 250MBPS
Other feature	Linked List Pointer mode Scale Down work mode Qos mode W2DDR buffer performance statistics and analysis

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10.4.3 VDPU382 DDR buf size requirements

10.4.3.1 VDPU382 Input Buffer Size Requested

(1).H265 Unique input data

Table 10-4 Video H.265 decoder Unique input data

buffer name	buffer size
MMU_table	Determined according to whether the MMU is turned on and the actual space of the MMU table
PPS+SPS	7x128bit
RPS	32x128bit
Cabac table	11x128bit
Scanlist	84x128bit
Stream_in	According to the actual situation
dpb_frame	According to the reference frame size, max reference frame num is 16

1-2.H264 Unique input data

Table 10-5 Video H.264 decoder Unique input data

buffer name	buffer size
MMU_table	Determined according to whether the MMU is turned on and the actual space of the MMU table
PPS	3x128bit
RPS	8x128bit
Cabac table	58x128bit
Scanlist	13x128bit
Stream_in	According to the actual situation
dpb_frame	According to the reference frame size, max reference frame num is 16

1-3.VP9 Unique input data

Table 10-6 Video VP9 decoder Unique input data

buffer name	buffer size
MMU_table	Determined according to whether the MMU is turned on and the actual space of the MMU table
segid	((pic_widthxpic_height)/(8x8))x3bit
prob_intra	165x128bit
prob_inter	172x128bit
cabac_table	368Byte
stream_in	According to the actual situation
dbp_frame	According to the reference frame size, max reference frame num is 3

2. Config Register Linked List Pointer mode(LLP mode)

VDPU382 Video decoder support link table mode to improve decoder continuity and reduce CPU participate and interrupt response time. In this mode, the register which used for config will be prepare into DDR, after that user enable link table mode, and then our decoder will fetch the register config information through AXI bus frame by frame. On link table mode, the decoder will auto finish all the frame decoder which be prepared in DDR, and not need CPU participate.

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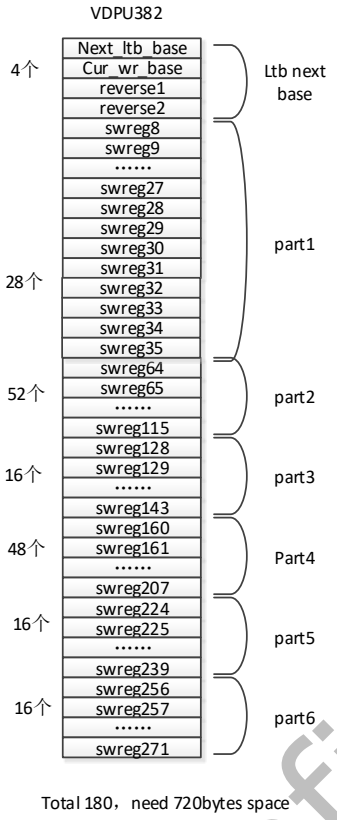


Fig.10-8 Link table register prepare in DDR format

As show in the above figure, Link table register prepare in DDR format, each frame config information need 720bytes in DDR. When Link table register work mode be actived, MMU should be config in first, and then parpare register to ddr, at last to config LLP ctrl register to start decoder.

For LLP work mode, LLP register buffer will be required. Every frame will require 512 byte DDR space. Then, buffer size calculate formula be defined as follows:

LLP_register_buffer_size = frame_num * 720 byte

After hardware decoder one frame, will write back some information to DDR where the write back base address is current config storage addr base. All the write back information is listed in the follows table.

Table 10-7 Link table write back register

offset	Description
0x0	swreg224_sta_int
0x4	swreg225_sta_err_info
0x8	swreg226_sta_cabac_error_status
0xc	swreg227_sta_colmv_error_ref_picidx
0x10	swreg228_sta_cabac_error_ctu_offset
0x14	swreg229_sta_saowr_ctu_offset
0x18	swreg230_sta_slice_dec_num
0x1c	swreg231_sta_frame_error_ctu_num
0x20	swreg232_sta_error_packet_num
0x24	swreg233_sta_err_ctu_num_in_ro
0x28	swreg258_debug_perf_rd_max_latency_num
0x2c	swreg259_perf_rd_latency_samp_num
0x30	swreg260_debug_perf_rd_latency_acc_sum
0x34	swreg261_debug_perf_rd_axi_total_byte
0x38	swreg262_debug_perf_wr_axi_total_byte
0x3c	swreg263_debug_perf_working_cnt
0x40	assign info_data0[31:0] = {8'h0,dec_sw_ctu_num[23:0]};

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offset	Description
0x44	assign info_data1[31:0] = inter_sw_reflst_idx_use[31:0];
0x48	assign info_data2[31:0] = {12'h0,inter_sw_pu_cnt_sum[19:0]};
0x4c	assign info_data3[31:0] = {inter_sw_mv_y_min_out[15:0],inter_sw_mv_x_min_out[15:0]};
0x50	assign info_data4[31:0] = {inter_sw_mv_y_max_out[15:0],inter_sw_mv_x_max_out[15:0]};
0x54	assign info_data5[31:0] = inter_sw_mv_x_out_sum[31:0];
0x58	assign info_data6[31:0] = inter_sw_mv_y_out_sum[31:0];
0x5c	assign info_data7[31:0] = inter_sw_mv_x_out_abs_sum[31:0];
0x60	assign info_data8[31:0] = inter_sw_mv_y_out_abs_sum[31:0];
0x64	assign info_data9[31:0] = {{(40-MV_BIT_WIDTH){1'b0}},inter_sw_mv_y_out_abs_sum[MV_BIT_WIDTH-1:32], {(40-MV_BIT_WIDTH){1'b0}},inter_sw_mv_x_out_abs_sum[MV_BIT_WIDTH-1:32], {(40-MV_BIT_WIDTH){inter_sw_mv_y_out_sum[MV_BIT_WIDTH-1]}},inter_sw_mv_y_out_sum[MV_BIT_WIDTH-1:32], {(40-MV_BIT_WIDTH){inter_sw_mv_x_out_sum[MV_BIT_WIDTH-1]}},inter_sw_mv_x_out_sum[MV_BIT_WIDTH-1:32]};
0x68	assign info_data10[31:0] = {16'h0,cu8x8_skip_num[15:0]};
0x6c	assign info_data11[31:0] = {{(32-TU_SKIP_SUM_WIDTH){1'b0}},tu_skip_sum[TU_SKIP_SUM_WIDTH-1:0]};
0x70	assign info_data12[31:0] = {8'b0,1'b0,cr_qp_max[6:0],1'b0,cb_qp_max[6:0],1'b0,luma_qp_max[6:0]};
0x74	assign info_data13[31:0] = {8'b0,1'b0,cr_qp_min[6:0],1'b0,cb_qp_min[6:0],1'b0,luma_qp_min[6:0]};
0x78	assign info_data14[31:0] = {{(32-QP_SUM_WIDTH){1'b0}},luma_qp_sum[QP_SUM_WIDTH-1:0]};
0x7c	assign info_data15[31:0] = {{(32-QP_SUM_WIDTH){1'b0}},cb_qp_sum[QP_SUM_WIDTH-1:0]};
0x80	assign info_data16[31:0] = {{(32-QP_SUM_WIDTH){1'b0}},cr_qp_sum[QP_SUM_WIDTH-1:0]};
0x84	assign info_data17[31:0] = {12'd0,inter_sw_mv_x_pu_cnt_sum[19:0]};
0x88	assign info_data18[31:0] = {12'd0,inter_sw_mv_y_pu_cnt_sum[19:0]};
0x8c	swreg274_sta_ pix_range_y
0x90	swreg275_sta_ pix_range_u
0x94	swreg276_sta_ pix_range_v

The base address of config link table mode is RKVDEC_BASE+0x100.

10.4.3.2 VDPU382 Output Buffer Size Requested

We define variables ceilM(N) as follows:

$$\text{ceil(M,N)}=ceilM(N)=((N+M-1)/M)*M$$

(1). Output frame decoder buffer size

If output select YCbCr 4:2:0 semi-planar raster-scan format, you can use follows formula to calculate the decoder frame buffer size.

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$$luma_frame_buffer_size = y_vir_hor_stride * pic_h * bit_depth_y / 8$$

$$chroma_frame_buffer_size = uv_vir_hor_stride * (pic_h / 2) * bit_depth_c / 8$$

$$frame_buffer_size = luma_frame_buffer_size + chroma_frame_buffer_size$$

There:

- y_vir_hor_stirde: The virtual stride of luma, it must should more bigger than picture width
- uv_vir_hor_stride: The virtual stride of chroma, it must should more big than picture width for YCbCr 4:2:0
- bit_depth_y/c: Main, its value will be 8
- pixel_byte_num: yuv400 and yuv444 is 3xbitdepth/8; yuv420 is 1.5xbitdepth/8; yuv422 is 2xbitdepth/8

(2). Output frame colmv buffer size

you can use follows formula to calculate the decoder frame buffer size.

Table 10-8 Colmv uncompress info

Format	Colmv_size	Colmv space(bytes unit)
h264	4x4	8
hevc	16x16	16
vp9	8x8	16

So, the colmv uncompress size is:

$$colmv_buffer_size0 = (ceil64(pic_w) * ceil64(pic_h) / (colmv_size * colmv_size)) * colmv_bytes$$

The buffer size unit is byte unit.

where:

- ctu_size: ctu size;
- colmv_size：the block size for each colmv
- colmv_bytes：each colmv space used

(3). Error info buffer size

If error infomation be enable write to DDR, the error info buffer size will be required, and we can use the follows formula to calculate the error info buffer size.

$$error_info_buffer_size = ceil2(slice_num) * 8$$

only h264 and h265 support error info output.

10.4.3.3 VDPU382 Decoder Temporary Buffer Size Requested

The temporary buffer only used when VDPU346 on working status. The data write to temporary buffer size is row and col buffer data, we suggest row buffer used internal sram buffer will enhance the decoder performance.

Row buffer and Col buffer size require are listed as fellows.

Table 10-9 Row or Col buffer size required

data type	required condtion	buffer size
STRMD Row	H.265/H.264/VP9	3*pic_width
Inter Row	H.265/H.264/VP9	6*pic_width
Inter Col	H.265/H.264/VP9	3*pic_height
Transd Row	H.265/H.264/VP9	0.4* pic_width
Transd col	H.265/H.264/VP9	0.1* pic_height
Recon Row	H.265/H.264/VP9	6*pic_width
Dblk Row	H.265/H.264/VP9	22*pic_width
Sao Row	H.265/H.264/VP9	6*pic_width
FBC Row	H.265/H.264/VP9	11*pic_width
Filterd Col	H.265/VP9, have col tile	67* pic_height

10.4.4 VDPU720 feature supported

1. JPEG Decoder

JPEG features supported by decoder are as shown in the following figure.

Table 10-10 JPEG features

Feature	Decoder support
Input data format	JFIF file format 1.02

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Feature	Decoder support
	YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar
Decoding scheme	frame by frame
Output data format	YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar
Supported image size	48x48 to 65536x65536(4295Mpixels) Step size 8 pixels
Maximum frame rate	Up to 560 million pixels per second
Thumbnail decoding	JPEG compressed thumbnails supported
Restart marker frequency decoding	Supported
MJPEG	Supported
Error detection	Supported

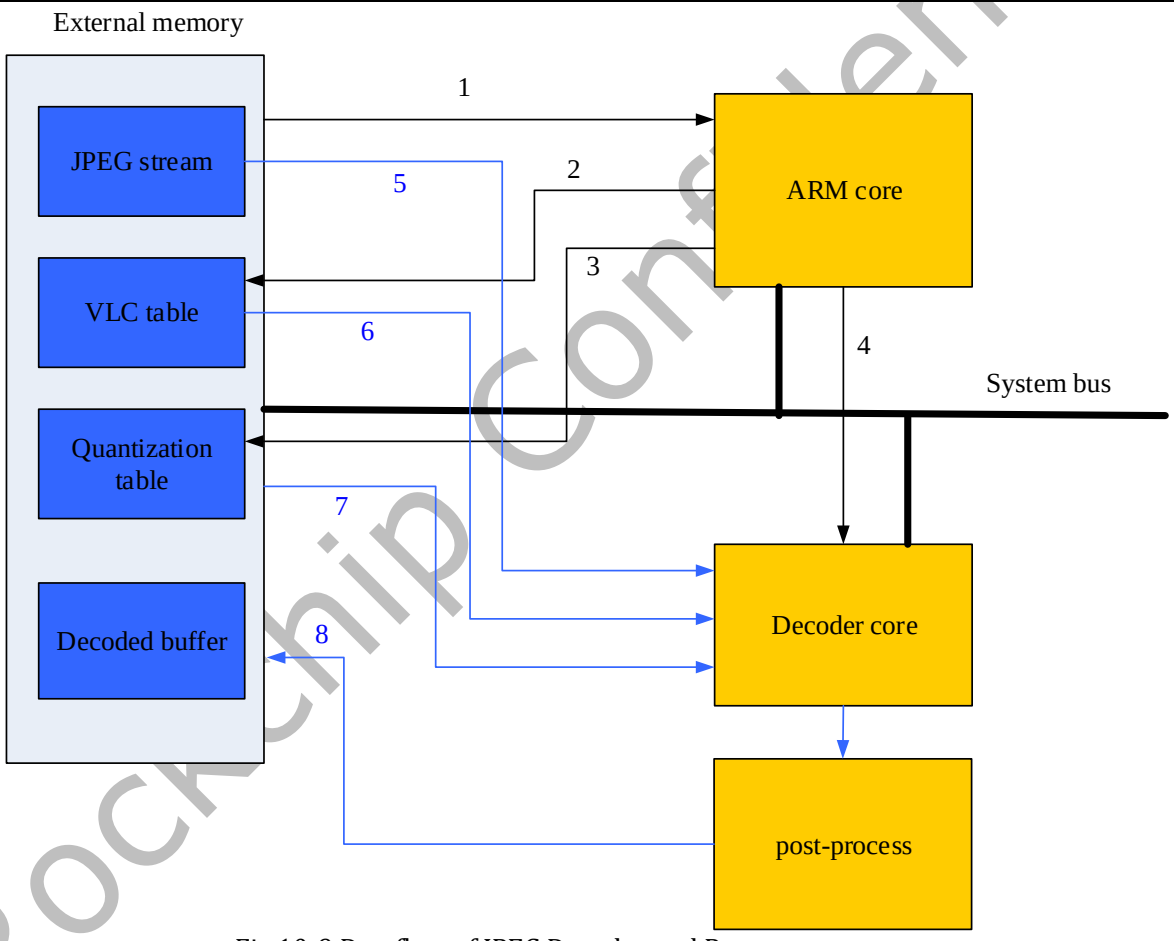


Fig.10-9 Dataflow of JPEG Decoder and Post-processor

The data flow of jpeg decoder is as shown in the preceding figure. The decoder software starts decoding the picture by parsing the stream headers (1) and then writes the following items to external memory:

VLC tables (2)

Quantization tables (3)

Last step for the software is to write the hardware control registers and to enable the hardware (4). After starting hardware, SW waits interrupt from HW.

Hardware decodes the picture by reading stream (5), VLC (6) and QP (7) tables. Hardware writes the decoded output picture memory one macroblock at a time (8). When the picture has been fully decoded, or the hardware has run out of stream data, it gives an interrupt with a proper status flag and provides stream end address for software to continue and returns to initial state.

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The follow image post-processor only supports combined mode.

2. Image Post-processor

The features supported by Post-processor are as show in the following table.

Table 10-11 Post-processor features

Feature	Post-processor support
Input data format	Any format generated by the decoder in combined mode YCbCr 4:2:0 semi-planar YCbCr 4:2:0 planar YCbYCr 4:2:2 YCrYCb 4:2:2 CbYCrY 4:2:2 CrYCbY 4:2:2
Post-processor scheme	Frame by frame. Post-processor handles the image macroblock by macroblock.
Input image source	Internal source
Output data format	YCbCr 4:2:0 semi-planar YCbCr 4:2:2 YCrYCb 4:2:2 CbYCrY 4:2:2 CrYCbY 4:2:2 Fully configurable RGB channel lengths and locations inside 24 bits, e.g. RGB 24-bit (8-8-8), RGB 16-bit(5-6-5).
Input image size	48x48 to 65536x65536 Step size 8 pixels
Output image size	16x16 to 65536x65536 Horizontal step size 1 Vertical step size 1
Image down-scaling	Proprietary averaging filter Arbitrary, integer scaling ratio separately for both dimensions 0/2/4/8 down-scaling ratio
YCbCr to RGB color conversion	BT.601 compliant BT.709 compliant User definable conversion coefficient
Dithering	2x2 ordered spatial dithering for 4, 5 and 6 bit RGB channel precision
Output picture	support raster or tile mode picture out luma 8x8 block tile

In pipe-line mode, the post-processor works together with the multi-format decoder. The PP will take its input directly from the decoder. The dataflow is as shown as follows.

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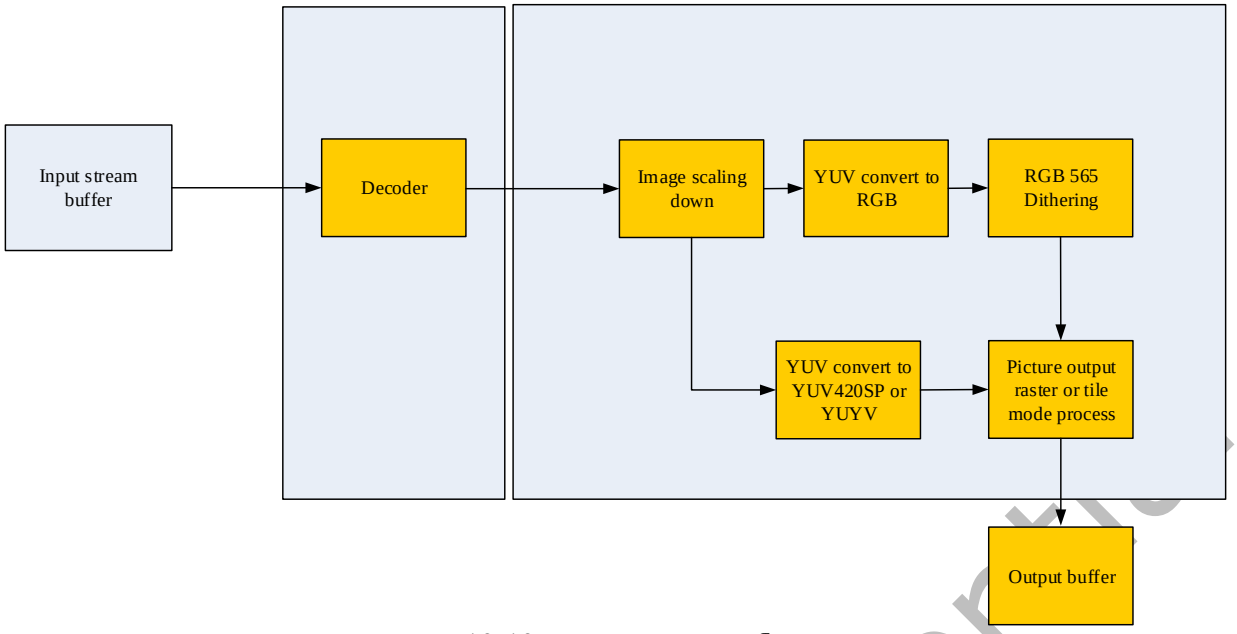


Fig.10-10 Post-process Dataflow

10.4.5 VEPU540 feature supported

Table 10-12 H.264 and JPEG encoder feature

Feature	Decoder support
Input data format	YCbCr formats: YCbCr 4:2:0 planar YCbCr 4:2:0 semi-planar YCbYCr 4:2:2 CbYCrY 4:2:2 Interleaved RGB formats: RGB888 ARGB8888
Encoding scheme	Frame by frame
Output data format	H.264 and JPEG Bit Stream
Supported image size	64x64 to 8192x8192
Maximum bit rate	200Mbps

10.5 Register Description

10.5.1 Internal Address Mapping

This section describes the control/status registers of the codec.
If VDPU382 decoder is chosen to work, the register base address is VDPU382_base.
If VDPU720 decoder is chosen to work, the register base address is VDPU720_base.
If VEPU540 encoder is chosen to work, the register base address is VEPU540_base.
All the register config base are listed as follows:

Table 10-13 Base address of config

Config Register	Base addr
VDPU382 link table config base	VDPU382_base+0x000
VDPU382 function config base	VDPU382_base+0x100
VDPU382 cache config base	VDPU382_base+0x600 for Y channel VDPU382_base+0x640 for C channel VDPU382_base+0x680 for head channel
VDPU382 mmu config base	VDPU382_base+0x800 for rd channel VDPU382_base+0x900 for wr channel
VDPU720 function config base	VDPU720_base

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Config Register	Base addr
VDPU720 mmu config base	VDPU720_base+0x480
VDPU720 link table config base	VDPU720_base+0x300
VEPU540 function config base	VEPU540_base

Base address value

Base addr	value
VDPU382_base	0xFF34_0000
VDPU720_base	0xFF45_0000
VEPU540_base	0xFF36_0000

10.5.2 VDPU382 Registers Summary

Name	Offset	Size	Reset Value	Description
RKVDEC_SWREG0_ID	0x0000	W	0x00000000	ID register (read only)
RKVDEC_SWREG8_IN_OUT	0x0020	W	0x00000000	Data input and output endian setting and sys ctrl
RKVDEC_SWREG9_DEC_MODE	0x0024	W	0x00000000	Dec mode
RKVDEC_SWREG10_DEC_E	0x0028	W	0x00000000	Decoder enable
RKVDEC_SWREG11_IMPORTANT_EN	0x002C	W	0x00000000	Interrupt and decoder enable register
RKVDEC_SWREG12_SENCODARY_EN	0x0030	W	0x00000000	Sys ctrl
RKVDEC_SWREG13_EN_MODE_SET	0x0034	W	0x00000000	Enable register
RKVDEC_SWREG14_FBC_PARAM_SET	0x0038	W	0x00000000	Fbc parem set
RKVDEC_SWREG15_STREAM_PARAM_SET	0x003C	W	0x00000000	Stream param set
RKVDEC_SWREG16_STREAM_LEN	0x0040	W	0x00000000	Amount of stream bytes in the input buffer or amount ot rlc bytes in the input buffer
RKVDEC_SWREG17_SLICE_NUMBER	0x0044	W	0x00000000	The current frame slice number
RKVDEC_SWREG18_Y_HOR_STRIDE	0x0048	W	0x00000000	Picture horizontal virtual stride
RKVDEC_SWREG19_UV_HOR_STRIDE	0x004C	W	0x00000000	Picture parametes
RKVDEC_SWREG20_FBC_PAYLOAD_OFFSET	0x0050	W	0x00000000	Register0004 Description
RKVDEC_SWREG20_Y_STRIDE	0x0050	W	0x00000000	The output picture y fac virtual stride.Suggest this register to config to even for advance ddr performance.
RKVDEC_SWREG21_ERROR_CTRL_SET	0x0054	W	0x00000000	Error sys ctrl
RKVDEC_SWREG22_ERR_ROI_CTU_OFFSET_START	0x0058	W	0x00000000	It will cal the error ctu num in the roi.It will include the st ctu and end ctu.
RKVDEC_SWREG23_ERR_ROI_CTU_OFFSET_END	0x005C	W	0x00000000	It will cal the error ctu num in the roi.It will include the st ctu and end ctu.
RKVDEC_SWREG24_CABAC_ERROR_EN_LOWBITS	0x0060	W	0x00000000	Cabac error enable config
RKVDEC_SWREG25_CABAC_ERROR_EN_HIGHBITS	0x0064	W	0x00000000	Cabac error enable high bits config

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Name	Offset	Size	Reset Value	Description
RKVDEC_SWREG26_BLOCK_GATING_EN	0x0068	W	0x00000000	Block gating enable ctrl flag
RKVDEC_SWREG27_CORE_SAFE_PIXELS	0x006C	W	0x00000000	colmv and recon report coord should be protect by safe pixels
RKVDEC_SWREG28_MULTIPLY_CORE_CTRL	0x0070	W	0x00000000	Multiply core work ctrl
RKVDEC_SWREG29_SCALE_DOWN_CTRL	0x0074	W	0x00000000	Scale down ctrl
RKVDEC_SWREG30_Y_SCALE_DOWN_TILE8X8_HOR_STRIDE	0x0078	W	0x00000000	Picture horizontal virtual stride
RKVDEC_SWREG31_UV_SCALE_DOWN_TILE8X8_HOR_STRIDE	0x007C	W	0x00000000	Picture parametes
RKVDEC_SWREG32_TIMEOUT_THRESHOLD	0x0080	W	0x00000000	Timeout threshold for timeout
RKVDEC_SWREG33_LINE_IRQ_CTRL	0x0084	W	0x00000000	Line_irq_ctrl
RKVDEC_SWREG34_SCALE_DOWN_ROI_OFFSET	0x0088	W	0x00000000	Scale down roi start offset
RKVDEC_SWREG35_SCALE_DOWN_ROI_OUT_SIZE	0x008C	W	0x00000000	Scale down roi output size
RKVDEC_SWREG64_H26X_SET	0x0100	W	0x00000000	For H26x use
RKVDEC_SWREG64_VP9_SET	0x0100	W	0x00000000	Vp9 compressed header offset.2014.11.19 del this register, because we can decode out sw_vp9_cprheader_offset from the stream.
RKVDEC_SWREG65_CUR_POC	0x0104	W	0x00000000	Hevc & h264 & avs2 :the poc of cur picture.add vp9.
RKVDEC_SWREG66_H264_CUR_POC1	0x0108	W	0x00000000	When cur is field, h264 cur poc for bottom field.
RKVDEC_SWREG67_REF0_POC	0x010C	W	0x00000000	Hevc & h264 & avs2: The poc of reference picture index 0.
RKVDEC_SWREG67_VP9_SEGID_GRP0	0x010C	W	0x00000000	Vp9 segid syntax grp0.When write it is for last frame.When read it is for cur frame.
RKVDEC_SWREG68_REF1_POC	0x0110	W	0x00000000	Hevc & h264 & avs2: The poc of reference picture index 1.
RKVDEC_SWREG68_VP9_SEGID_GRP1	0x0110	W	0x00000000	Vp9 segid syntax grp1.When write it is for last frame.When read it is for cur frame.
RKVDEC_SWREG69_REF2_POC	0x0114	W	0x00000000	Hevc & h264 & avs2: The poc of reference picture index 2.
RKVDEC_SWREG69_VP9_SEGID_GRP2	0x0114	W	0x00000000	Vp9 segid syntax grp2.When write it is for last frame.When read it is for cur frame.
RKVDEC_SWREG70_REF3_POC	0x0118	W	0x00000000	Hevc & h264 & avs2: The poc of reference picture index 3.
RKVDEC_SWREG70_VP9_SEGID_GRP3	0x0118	W	0x00000000	Vp9 segid syntax grp3.When write it is for last frame.When read it is for cur frame.
RKVDEC_SWREG71_REF4_POC	0x011C	W	0x00000000	Hevc & h264 & avs2: The poc of reference picture index 4.

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RKVDEC_SWREG71_VP9_SEGID_GRP4	0x011C	W	0x00000000	Vp9 segid syntax grp4.When write it is for last frame.When read it is for cur frame.
RKVDEC_SWREG72_REF5_POC	0x0120	W	0x00000000	Hevc & h264 & avs2: The poc of reference picture index 5.
RKVDEC_SWREG72_VP9_SEGID_GRP5	0x0120	W	0x00000000	Vp9 segid syntax grp5.When write it is for last frame.When read it is for cur frame.
RKVDEC_SWREG73_REF6_POC	0x0124	W	0x00000000	Hevc & h264 & avs2: The poc of reference picture index 6.
RKVDEC_SWREG73_VP9_SEGID_GRP6	0x0124	W	0x00000000	Vp9 segid syntax grp6.When write it is for last frame.When read it is for cur frame.
RKVDEC_SWREG74_REF7_POC	0x0128	W	0x00000000	Hevc & h264 & avs2: The poc of reference picture index 7.
RKVDEC_SWREG74_VP9_SEGID_GRP7	0x0128	W	0x00000000	Vp9 segid syntax grp7.When write it is for last frame.When read it is for cur frame.
RKVDEC_SWREG75_REF8_POC	0x012C	W	0x00000000	Hevc & h264: The poc of reference picture index 8.
RKVDEC_SWREG75_VP9_INFO_LASTFRAME	0x012C	W	0x00000000	Vp9 info for lastframe
RKVDEC_SWREG76_REF9_POC	0x0130	W	0x00000000	Hevc & h264: The poc of reference picture index 9.
RKVDEC_SWREG76_VP9_CPRHEADER_CONFIG	0x0130	W	0x00000000	Vp9 compressed header config info
RKVDEC_SWREG77_REF10_POC	0x0134	W	0x00000000	Hevc & h264: The poc of reference picture index 10.
RKVDEC_SWREG77_VP9_INTERCMD_NUM	0x0134	W	0x00000000	Vp9 intercmd num
RKVDEC_SWREG78_REF11_POC	0x0138	W	0x00000000	Hevc & h264: The poc of reference picture index 11.
RKVDEC_SWREG78_VP9_STREAM_SIZE	0x0138	W	0x00000000	Vp9 last tile size
RKVDEC_SWREG79_REF12_POC	0x013C	W	0x00000000	Hevc & h264: The poc of reference picture index 12.
RKVDEC_SWREG79_VP9_LASTF_Y_HOR_VIRSTRIDE	0x013C	W	0x00000000	Vp9 last frame y horizontal virstride
RKVDEC_SWREG80_REF13_POC	0x0140	W	0x00000000	Hevc & h264: The poc of reference picture index 13.
RKVDEC_SWREG80_VP9_LASTF_UV_HOR_VIRSTRIDE	0x0140	W	0x00000000	Vp9 last frame uv horizontal virstride
RKVDEC_SWREG81_REF14_POC	0x0144	W	0x00000000	Hevc & h264: The poc of reference picture index 14.
RKVDEC_SWREG81_VP9_GOLDENF_Y_HOR_VIRSTRIDE	0x0144	W	0x00000000	Vp9 golden frame y horizontal virstride
RKVDEC_SWREG82_REF15_POC	0x0148	W	0x00000000	H264: The poc of reference picture index 15.Hevc: Used for mvc.Vp9: Now is no use.
RKVDEC_SWREG82_VP9_GOLDEN_UV_HOR_VIRSTRIDE	0x0148	W	0x00000000	Vp9 golden uv horizontal virstirde

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Name	Offset	Size	Reset Value	Description
RKVDEC_SWREG83_REF16_POC	0x014C	W	0x00000000	H264: The poc of reference picture index 16.Hevc & vp9: Now is no use.
RKVDEC_SWREG83_VP9_ALTREFF_Y_HOR_VIRSTRIDE	0x014C	W	0x00000000	Vp9 altref frame y horizontal virstride
RKVDEC_SWREG84_REF17_POC	0x0150	W	0x00000000	H264: The poc of reference picture index 17.Hevc & vp9: Now is no use.
RKVDEC_SWREG84_VP9_ALTREFF_UV_HOR_VIRSTRIDE	0x0150	W	0x00000000	Vp9 altreff uv horizontal virstirde.2015.10.23, change from 9bits to 10bits.
RKVDEC_SWREG85_REF18_POC	0x0154	W	0x00000000	H264: The poc of reference picture index 18.Hevc & vp9: Now is no use.
RKVDEC_SWREG85_VP9_LASTF_Y_VIRSTRIDE	0x0154	W	0x00000000	Last ref ystride
RKVDEC_SWREG86_REF19_POC	0x0158	W	0x00000000	H264: The poc of reference picture index 19.Hevc & vp9: Now is no use.
RKVDEC_SWREG86_VP9_GOLDEN_Y_VIRSTRIDE	0x0158	W	0x00000000	Vp9 golden y stride
RKVDEC_SWREG87_REF20_POC	0x015C	W	0x00000000	H264: The poc of reference picture index 20.Hevc & vp9: Now is no use.
RKVDEC_SWREG87_VP9_ALTREF_Y_VIRSTRIDE	0x015C	W	0x00000000	Altref ref ystride
RKVDEC_SWREG88_REF21_POC	0x0160	W	0x00000000	H264: The poc of reference picture index 21.Hevc & vp9: Now is no use.
RKVDEC_SWREG88_VP9_LREF_HOR_SCALE	0x0160	W	0x00000000	Horizontal scaling factor for last reference picture
RKVDEC_SWREG89_REF22_POC	0x0164	W	0x00000000	H264: The poc of reference picture index 22.Hevc & vp9: Now is no use.
RKVDEC_SWREG89_VP9_LREF_VER_SCALE	0x0164	W	0x00000000	Vertical scaling factor for last reference picture
RKVDEC_SWREG90_REF23_POC	0x0168	W	0x00000000	H264: The poc of reference picture index 23.Hevc & vp9: Now is no use.
RKVDEC_SWREG90_VP9_GREF_HOR_SCALE	0x0168	W	0x00000000	Horizontal scaling factor for golden reference picture
RKVDEC_SWREG91_REF24_POC	0x016C	W	0x00000000	H264: The poc of reference picture index 24.Hevc & vp9: Now is no use.
RKVDEC_SWREG91_VP9_GREF_VER_SCALE	0x016C	W	0x00000000	Vertical scaling factor for golden reference picture
RKVDEC_SWREG92_REF25_POC	0x0170	W	0x00000000	H264: The poc of reference picture index 25.Hevc & vp9: Now is no use.
RKVDEC_SWREG92_VP9_AREF_HOR_SCALE	0x0170	W	0x00000000	Horizontal scaling factor for alfter reference picture
RKVDEC_SWREG93_REF26_POC	0x0174	W	0x00000000	H264: The poc of reference picture index 26.Hevc & vp9: Now is no use.

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Name	Offset	Size	Reset Value	Description
RKVDEC_SWREG93_VP9_AREF_VER_SCALE	0x0174	W	0x00000000	Vertical scaling factor for alfter reference picture
RKVDEC_SWREG94_REF27_POC	0x0178	W	0x00000000	H264: The poc of reference picture index 27.Hevc & vp9: Now is no use.
RKVDEC_SWREG94_VP9_REF_DELTAS_LASTFRAME	0x0178	W	0x00000000	Vp9 ref deltas
RKVDEC_SWREG95_REF28_POC	0x017C	W	0x00000000	H264: The poc of reference picture index 28.Hevc & vp9: Now is no use.
RKVDEC_SWREG95_VP9_LAST_POC	0x017C	W	0x00000000	VP9: The poc of last reference
RKVDEC_SWREG96_REF29_POC	0x0180	W	0x00000000	H264: The poc of reference picture index 29.Hevc & vp9: Now is no use.
RKVDEC_SWREG96_VP9_GOLDEN_POC	0x0180	W	0x00000000	VP9: The poc of golden reference
RKVDEC_SWREG97_REF30_POC	0x0184	W	0x00000000	H264: The poc of reference picture index 30.Hevc & vp9: Now is no use.
RKVDEC_SWREG97_VP9_ALTREF_POC	0x0184	W	0x00000000	VP9: The poc of altref reference
RKVDEC_SWREG98_REF31_POC	0x0188	W	0x00000000	H264: The poc of reference picture index 31.Hevc & vp9: Now is no use.
RKVDEC_SWREG98_VP9_COL_REF_POC	0x0188	W	0x00000000	VP9: The poc of colpic reference
RKVDEC_SWREG99_HEVC_REF_VALID	0x018C	W	0x00000000	Valid flag for picture index 0 ~14
RKVDEC_SWREG99_H264_REG0_3_INFO	0x018C	W	0x00000000	Rreference picture index 0~3
RKVDEC_SWREG99_AVS2_REG0_3_INFO	0x018C	W	0x00000000	Rreference picture index 0~3
RKVDEC_SWREG99_VP9_PROB_REF_POC	0x018C	W	0x00000000	VP9: The poc of reference prob
RKVDEC_SWREG100_AVS2_REG4_7_INFO	0x0190	W	0x00000000	Rreference picture index 4~7
RKVDEC_SWREG100_H264_REG4_7_INFO	0x0190	W	0x00000000	Rreference picture index 4~7
RKVDEC_SWREG100_VP9_SEGID_REF_POC	0x0190	W	0x00000000	VP9: The poc of reference segmentid
RKVDEC_SWREG101_H264_REG8_11_INFO	0x0194	W	0x00000000	Rreference picture index 8~11
RKVDEC_SWREG102_H264_REG12_15_INFO	0x0198	W	0x00000000	Rreference picture index 12~15
RKVDEC_SWREG103_HEVC_MVC0	0x019C	W	0x00000000	Hevc mvc config register
RKVDEC_SWREG103_AVS2_CTRL_EXTRA	0x019C	W	0x00000000	Avs2 ctrl register
RKVDEC_SWREG103_VP9_PROB_EN	0x019C	W	0x00000000	Vp9_prob_en config
RKVDEC_SWREG104_HEVC_MVC1	0x01A0	W	0x00000000	Hevc MVC ctrl register

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Name	Offset	Size	Reset Value	Description
RKVDEC_SWREG105_VP9CNT_UPD_EN_AVS2_HEADLEN	0x01A4	W	0x00000000	Avs2_head_len and Vp9 count update en
RKVDEC_SWREG106_VP9_FRAME_WIDTH_LAST	0x01A8	W	0x00000000	Last frame frame_size_width
RKVDEC_SWREG107_VP9_FRAME_HEIGHT_LAST	0x01AC	W	0x00000000	Last frame frame_size_height
RKVDEC_SWREG108_VP9_FRAME_WIDTH_GOLDEN	0x01B0	W	0x00000000	Golden frame_size_width
RKVDEC_SWREG109_VP9_FRAME_HEIGHT_GOLDEN	0x01B4	W	0x00000000	Golden frame_size_height
RKVDEC_SWREG110_VP9_FRAME_WIDTH_ALTREF	0x01B8	W	0x00000000	Alfter frame_size_width
RKVDEC_SWREG111_VP9_FRAME_HEIGHT_ALTREF	0x01BC	W	0x00000000	Alfter frame_size_height
RKVDEC_SWREG112_ERROR_REF_INFO	0x01C0	W	0x00000000	Refer error is top or bot field flag
RKVDEC_SWREG128_STRM_RLC_BASE	0x0200	W	0x00000000	The stream or rlc data base address
RKVDEC_SWREG129_RLCWRITE_BASE	0x0204	W	0x00000000	The base address of rlcwrite base address.When frame is ready, it is the address of the end of rlcwrite address.
RKVDEC_SWREG129_ERROR_INFO_BASE	0x0204	W	0x00000000	The base address of error info
RKVDEC_SWREG130_DECOUT_BASE	0x0208	W	0x00000000	Base address of decoder output picture.Suggest this register to config to even for advance ddr performance.
RKVDEC_SWREG131_COLMV_CUR_BASE	0x020C	W	0x00000000	Cur frame colmv output addr
RKVDEC_SWREG132_ERROR_REF_BASE	0x0210	W	0x00000000	Error reference frame base address
RKVDEC_SWREG133_RCB_INTRAR_OFFSET	0x0214	W	0x00000000	Rcb intra row base address, unit: 64byts align
RKVDEC_SWREG134_RCB_TRANSDR_OFFSET	0x0218	W	0x00000000	Rcb transd row base address, unit: 64byts align
RKVDEC_SWREG135_RCB_TRANSDC_OFFSET	0x021C	W	0x00000000	Rcb transd col base address, unit: 64byts align
RKVDEC_SWREG136_RCB_STRMDR_OFFSET	0x0220	W	0x00000000	Rcb stream row base address, unit: 64byts align
RKVDEC_SWREG137_RCB_INTERR_OFFSET	0x0224	W	0x00000000	Rcb inter row base address, unit: 64byts align
RKVDEC_SWREG138_RCB_INTERC_OFFSET	0x0228	W	0x00000000	Rcb inter col base address, unit: 64byts align
RKVDEC_SWREG139_RCB_DBLKR_OFFSET	0x022C	W	0x00000000	Rcb dblock row base address, unit: 64byts align
RKVDEC_SWREG140_RCB_SAOR_OFFSET	0x0230	W	0x00000000	Rcb sao row base address, unit: 64byts align
RKVDEC_SWREG141_RCB_FBCR_OFFSET	0x0234	W	0x00000000	Rcb fbc row base address, unit: 64byts align
RKVDEC_SWREG142_RCB_FILTC_COL_OFFSET	0x0238	W	0x00000000	Rcb filter col base address, unit: 64byts align
RKVDEC_SWREG143_RCB_BASE	0x023C	W	0x00000000	Rcb base address, unit: 64byts align

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Name	Offset	Size	Reset Value	Description
RKVDEC_SWREG160_VP9_DELTA_PROB_BASE	0x0280	W	0x00000000	The base address of prob
RKVDEC_SWREG161_PPS_BASE	0x0284	W	0x00000000	The base address of pps
RKVDEC_SWREG161_AVS2_HEAD_BASE	0x0284	W	0x00000000	The base address of avs2 head
RKVDEC_SWREG162_VP9_LAST_PROB_BASE	0x0288	W	0x00000000	It only used when hardware parse prob.This base addr is for last prob
RKVDEC_SWREG163_RPS_BASE	0x028C	W	0x00000000	The base address of rps
RKVDEC_SWREG164_REF0_BASE	0x0290	W	0x00000000	Base address for reference picture index0
RKVDEC_SWREG164_VP9_REFERLAST_BASE	0x0290	W	0x00000000	Base address for reference picture.Suggest this register to config to even for advance ddr performance
RKVDEC_SWREG165_REF1_BASE	0x0294	W	0x00000000	Base address for reference picture index1
RKVDEC_SWREG165_VP9_REFERGOLDEN_BASE	0x0294	W	0x00000000	Base address for golden picture.Suggest this register to config to even for advance ddr performance.
RKVDEC_SWREG166_REF2_BASE	0x0298	W	0x00000000	Base address for reference picture index2
RKVDEC_SWREG166_VP9_REFERALFTER_BASE	0x0298	W	0x00000000	Base address for alfter picture.Suggest this register to config to even for advance ddr performance.
RKVDEC_SWREG167_VP9COUNT_BASE	0x029C	W	0x00000000	Vp9 count base addr
RKVDEC_SWREG167_REF3_BASE	0x029C	W	0x00000000	Base address for reference picture index3
RKVDEC_SWREG168_VP9_SEGIDLAST_BASE	0x02A0	W	0x00000000	Base address for last frame segment id
RKVDEC_SWREG168_REF4_BASE	0x02A0	W	0x00000000	Base address for reference picture index4
RKVDEC_SWREG169_AVP9_SEGIDCUR_BASE	0x02A4	W	0x00000000	Base address for cur frame segment id
RKVDEC_SWREG169_REF5_BASE	0x02A4	W	0x00000000	Base address for reference picture index5
RKVDEC_SWREG170_VP9_REFCOLMV_BASE	0x02A8	W	0x00000000	Vp9 refcolmv base addr
RKVDEC_SWREG170_REF6_BASE	0x02A8	W	0x00000000	Base address for reference picture index6
RKVDEC_SWREG171_VP9_INTERCMD_BASE	0x02AC	W	0x00000000	Inter cmd base addr
RKVDEC_SWREG171_REF7_BASE	0x02AC	W	0x00000000	Base address for reference picture index7
RKVDEC_SWREG172_VP9_UPDATE_PROB_WR_BASE	0x02B0	W	0x00000000	Hardware parse prob: Used as vp9 prob write base
RKVDEC_SWREG172_H26X_REF8_BASE	0x02B0	W	0x00000000	Base address for reference picture index8
RKVDEC_SWREG173_H26X_REF9_BASE	0x02B4	W	0x00000000	Base address for reference picture index9

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Name	Offset	Size	Reset Value	Description
RKVDEC_SWREG174_H26X_REF10_BASE	0x02B8	W	0x00000000	Base address for reference picture index10
RKVDEC_SWREG175_H26X_REF11_BASE	0x02BC	W	0x00000000	Base address for reference picture index11
RKVDEC_SWREG176_H26X_REF12_BASE	0x02C0	W	0x00000000	Base address for reference picture index12
RKVDEC_SWREG177_H26X_REF13_BASE	0x02C4	W	0x00000000	Base address for reference picture index13
RKVDEC_SWREG178_H26X_REF14_BASE	0x02C8	W	0x00000000	Base address for reference picture index14
RKVDEC_SWREG179_H26X_REF15_BASE	0x02CC	W	0x00000000	Base address for reference picture index15
RKVDEC_SWREG180_SCANLIST_ADDR	0x02D0	W	0x00000000	The addr for scanlist table
RKVDEC_SWREG181_COLMV_REF0_BASE	0x02D4	W	0x00000000	Ref0 frame colmv base addr
RKVDEC_SWREG182_COLMV_REF1_BASE	0x02D8	W	0x00000000	Ref1 frame colmv base addr
RKVDEC_SWREG183_COLMV_REF2_BASE	0x02DC	W	0x00000000	Ref2 frame colmv base addr
RKVDEC_SWREG184_COLMV_REF3_BASE	0x02E0	W	0x00000000	Ref3 frame colmv base addr
RKVDEC_SWREG185_COLMV_REF4_BASE	0x02E4	W	0x00000000	Ref4 frame colmv base addr
RKVDEC_SWREG186_COLMV_REF5_BASE	0x02E8	W	0x00000000	Ref5 frame colmv base addr
RKVDEC_SWREG187_COLMV_REF6_BASE	0x02EC	W	0x00000000	Ref6 frame colmv base addr
RKVDEC_SWREG188_COLMV_REF7_BASE	0x02F0	W	0x00000000	Ref7 frame colmv base addr
RKVDEC_SWREG189_COLMV_REF8_BASE	0x02F4	W	0x00000000	Ref8 frame colmv base addr
RKVDEC_SWREG190_COLMV_REF9_BASE	0x02F8	W	0x00000000	Ref9 frame colmv base addr
RKVDEC_SWREG191_COLMV_REF10_BASE	0x02FC	W	0x00000000	Ref10 frame colmv base addr
RKVDEC_SWREG192_COLMV_REF11_BASE	0x0300	W	0x00000000	Ref11 frame colmv base addr
RKVDEC_SWREG193_COLMV_REF12_BASE	0x0304	W	0x00000000	Ref12 frame colmv base addr
RKVDEC_SWREG194_COLMV_REF13_BASE	0x0308	W	0x00000000	Ref13 frame colmv base addr
RKVDEC_SWREG195_COLMV_REF14_BASE	0x030C	W	0x00000000	Ref14 frame colmv base addr
RKVDEC_SWREG196_COLMV_REF15_BASE	0x0310	W	0x00000000	Ref15 frame colmv base addr
RKVDEC_SWREG197_CABACTBL_BASE	0x0314	W	0x00000000	Hevc & H264: The base address of cabac table.
RKVDEC_SWREG198_SCALE_DOWN_LUMA_BASE	0x0318	W	0x00000000	Hevc & H264: The base address of cabac table.
RKVDEC_SWREG199_SCALE_DOWN_CHRO_BASE	0x031C	W	0x00000000	The base address of scale down chro base

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Name	Offset	Size	Reset Value	Description
RKVDEC_SWREG200_REF_POC_HIGHBIT_P0	0x0320	W	0x00000000	Sw_ref_poc_highbituse for separate top/bot field or multi-view stream in multi-core casevp9 not used
RKVDEC_SWREG201_REF_POC_HIGHBIT_P1	0x0324	W	0x00000000	Sw_ref_poc_highbituse for separate top/bot field or multi-view stream in multi-core casevp9 not used
RKVDEC_SWREG202_REF_POC_HIGHBIT_P2	0x0328	W	0x00000000	Sw_ref_poc_highbituse for separate top/bot field or multi-view stream in multi-core casevp9 not used
RKVDEC_SWREG203_REF_POC_HIGHBIT_P3	0x032C	W	0x00000000	Sw_ref_poc_highbituse for separate top/bot field or multi-view stream in multi-core casevp9 not used
RKVDEC_SWREG204_CUR_POC_HIGHBIT	0x0330	W	0x00000000	Sw_cur_poc_highbituse for separate top/bot field or multi-view stream in multi-core casevp9 not used
RKVDEC_SWREG205_DEBUG_INFO	0x0334	W	0x00000000	Debug register info
RKVDEC_SWREG224_STA_INT	0x0380	W	0x00000000	Decoder status
RKVDEC_SWREG225_SLICE_BYTE_OFFSET_STA	0x0384	W	0x00000000	Slice byte status
RKVDEC_SWREG226_STA_CABAC_ERROR_STATUS	0x0388	W	0x00000000	Cabac error status
RKVDEC_SWREG227_STA_COLMV_ERROR_REF_PICIDX	0x038C	W	0x00000000	Colmv error ref picidx
RKVDEC_SWREG228_STA_CABAC_ERROR_CTU_OFFSET	0x0390	W	0x00000000	Cabac error ctu offset
RKVDEC_SWREG229_STA_AXI_WCH_FINISH_FLAG	0x0394	W	0x00000000	When there is any error, it is for the position of sao decode output to busifd.
RKVDEC_SWREG230_STA_SLICE_DEC_NUM	0x0398	W	0x00000000	Slice dec num
RKVDEC_SWREG231_STA_FRAME_ERROR_CTU_NUM	0x039C	W	0x00000000	H264 and hevc error ctu number
RKVDEC_SWREG232_STA_ERROR_PACKET_NUM	0x03A0	W	0x00000000	Error packet number
RKVDEC_SWREG233_STA_ERR_CTU_NUM_IN_ROI	0x03A4	W	0x00000000	The error ctu num in roi
RKVDEC_SWREG234_BUF_EMPTY_OFFSET	0x03A8	W	0x00000000	Coord_report (x,y) offset, crtl by sw_coord_realtime_report_en
RKVDEC_SWREG235_COORD_REPORT_OUTBUF_HEIGHT	0x03AC	W	0x00000000	Minus pixel height
RKVDEC_SWREG256_DEBUG_PERF_LATENCY_CTRL0	0x0400	W	0x00000000	Axi performance latency module contrl register
RKVDEC_SWREG257_DEBUG_PERF_LATENCY_CTRL1	0x0404	W	0x00000000	Debug perf latency ctrl

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Name	Offset	Size	Reset Value	Description
RKVDEC_SWREG258_DEBUG_PERF_RD_MAX_LATENCY_NUM	0x0408	W	0x00000000	Read max latency number
RKVDEC_SWREG259_PERF_RD_LATENCY_SAMP_NUM	0x040C	W	0x00000000	The number of bigger than configed threshold value
RKVDEC_SWREG260_DEBUG_PERF_RD_LATENCY_ACC_SUM	0x0410	W	0x00000000	Total sample number
RKVDEC_SWREG261_DEBUG_PERF_RD_AXI_TOTAL_BYTE	0x0414	W	0x00000000	The bandwidth of total read bytes
RKVDEC_SWREG262_DEBUG_PERF_WR_AXI_TOTAL_BYTE	0x0418	W	0x00000000	The bandwidth of total write bytes
RKVDEC_SWREG263_DEBUG_PERF_WORKING_CNT	0x041C	W	0x00000000	The total running cycle of current frame
RKVDEC_SWREG264_DEBUG_BUS_STATE	0x0420	W	0x00000000	Bus_state
RKVDEC_SWREG265_DEBUG_PERF_SEL	0x0424	W	0x00000000	Performance montor ctrl
RKVDEC_SWREG266_DEBUG_PERF_CNT0	0x0428	W	0x00000000	Performance count value0
RKVDEC_SWREG267_DEBUG_PERF_CNT1	0x042C	W	0x00000000	Performance count value1
RKVDEC_SWREG268_DEBUG_PERF_CNT2	0x0430	W	0x00000000	Performance count value2
RKVDEC_SWREG269_VP9_ERROR_INFO	0x0434	W	0x00000000	Performance count value2
RKVDEC_SWREG270_DEBUG_QOS_CTRL	0x0438	W	0x00000000	AXI bus hurry ctrl
RKVDEC_SWREG271_DEBUG_WAIT_CYCLE_QOS	0x043C	W	0x00000000	Hw find sw_wr_wait_cycle_qos cycle can't wr to ddr, it will give hurry.
RKVDEC_SWREG272_DEBUG_INT	0x0440	W	0x00000000	Debug info
RKVDEC_SWREG273_STAB_FRAME_FLAG	0x0444	W	0x00000000	Debug info
RKVDEC_SWREG274_PIX_RANGE_Y	0x0448	W	0x00000000	It will montior current frame max or min pix value.
RKVDEC_SWREG275_PIX_RANGE_U	0x044C	W	0x00000000	It will montior current frame max or min pix value.
RKVDEC_SWREG276_PIX_RANGE_V	0x0450	W	0x00000000	It will montior current frame max or min pix value.
RKVDEC_SWREG277_ERROR_SPREAD_NUM	0x0454	W	0x00000000	Error spread block numbers
RKVDEC_SWREG278_DEC_LINE_OFFSET_Y	0x0458	W	0x00000000	Decoder line offset y state from lpf report

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

10.5.3 VDPU382 Detail Register Description

RKVDEC_SWREG0_ID

Address: Operational Base(0xFF740100) + offset (0x0000)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	prod_num Prod code
15:8	RO	0x00	major_ver Major verision
7:0	RW	0x00	minor_ver Minor version

RKVDEC_SWREG8_IN_OUT

Address: Operational Base(0xFF740100) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	sw_out_swap64_e May be used for 64 or 128 bit environment. 1'b0: No swapping of 64 bit words 1'b1: 64 bit data words are swapped
8	RW	0x0	sw_out_cbcr_swap 1'b0: Cb(u) is in the lower address, cr(v) is in the higher address. 1'b1: Cb(u) is in the higher address,cr(v) is in the lower address. Sw_in_cbcr_swap is the same with sw_out_cbcr_swap.
7	RW	0x0	sw_out_swap32_e May be used for 64 or 128 bit environment. 1'b0: No swapping of 32 bit words 1'b1: 32 bit data words are swapped
6	RW	0x0	sw_out_endian 1'b0: Little endian 1'b1: Big endian For litter enadian, a data 0x12345678, 0x78 is stored in lower address, 0x12 is stored in higher address.
5	RW	0x0	sw_str_swap64_e May be used for 128 bit environment. 1'b0: No swapping of 64 bit words 1'b1: 64 bit data words are swapped
4	RW	0x0	sw_str_swap32_e May be used for 64 or 128 bit environment. 1'b0: No swapping of 32 bit words 1'b1: 32 bit data words are swapped
3	RW	0x0	sw_str_endian 1'b0: Little endian 1'b1: Big endian For litter enadian, a data 0x12345678, 0x78 is stored in lower address, 0x12 is stored in higher address.
2	RW	0x0	sw_in_swap64_e May be used for 128 bit environment. 1'b0: No swapping of 64 bit words 1'b1: 64 bit data words are swapped
1	RW	0x0	sw_in_swap32_e May be used for 64 or 128 bit environment. 1'b0: No swapping of 32 bit words 1'b1: 32 bit data words are swapped
0	RW	0x0	sw_in_endian 1'b0: Little endian 1'b1: Big endian For litter enadian, a data 0x12345678, 0x78 is stored in lower address, 0x12 is stored in higher address.

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RKVDEC_SWREG9_DEC_MODE

Address: Operational Base(0xFF740100) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	sw_dec_mode 10'h0: Hevc 10'h1: H264 10'h2: Vp9 10'h3: Avs2 Others: Reserved

RKVDEC_SWREG10_DEC_E

Address: Operational Base(0xFF740100) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	sw_dec_e Decoder enable. Setting this bit high will start the decoding operation. HW will reset this when the picture is decoded ready or bus error or time out interrupt is given for all decode format. HW will reset this when picture is processed stream error for vp9 & hevc & (h264 when sw_h264_error_mode is 1'b0).

RKVDEC_SWREG11_IMPORTANT_EN

Address: Operational Base(0xFF740100) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	sw_mmu_wlast_match_fail MMU integrity wlast match fail state.
28	RW	0x0	sw_wlast_match_fail Axi integrity wlast match fail state.
27:25	RO	0x0	reserved
24	RW	0x0	sw_pix_range_det_e 1'b0: Pix range detect disable 1'b1: Pix range detect enable
23	RW	0x0	sw_err_colmv_fill_e Dec error colmv fill enable. 1'b0: Disable 1'b1: Enable
22	RW	0x0	sw_err_head_fill_e Dec error head fill enable at afbc mode.
21	RO	0x0	reserved
20	RW	0x0	sw_softrst_en_p Softreset enable signal, write 1 to soft reset, write 0 invalid, puls register.
19:11	RO	0x000	reserved
10	RW	0x0	sw_dec_e_rewrite_valid Sw_dec_e rewrite valid signal, maybe for only when buffer empty, restart the decoder use.
9	RO	0x0	reserved
8	RW	0x0	sw_dec_line_irq_en 1'b0: Line irq proc disable 1'b1: Line irq proc enable
7	RO	0x0	reserved
6	RW	0x0	sw_buf_empty_en Buffer empty interrupt enable.

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Bit	Attr	Reset Value	Description
5	RW	0x0	sw_dec_line_irq_dis When hight, there are no line irq interrupts concerning decoder from HW. Polling must be used to see the interrupt status.
4	RW	0x0	sw_dec_irq_dis When hight, there are no interrupts concerning decoder from HW. Polling must be used to see the interrupt status.
3:2	RO	0x0	reserved
1	RW	0x0	sw_dec_clkgate_e 1'b0: Clock is running for all structures. 1'b1: Clock is gated for decoder structures that are not used.
0	RO	0x0	reserved

RKVDEC_SWREG12_SENCODARY_EN

Address: Operational Base(0xFF740100) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	sw_scale_down_en Scale down used rasater mode output. It support 1/2 scale down ratio for hor or vrz. 1'b0: Disable scale down function 1'b1: Enable scale down function
8	RO	0x0	sw_scanlist_addr_valid_en 1'b0: Scanlsit addr get from pps table 1'b1: Scanlist addr get from config Hardware fix 1'b1.
7	RO	0x0	reserved
6	RW	0x0	sw_collect_info_en 1'b0: Disable 1'b1: Enable
5	RW	0x0	sw_error_info_en 1'b0: Disable 1'b1: Enable
4	RO	0x0	reserved
3	RW	0x0	sw_tile_e 1'b0: Tile mode disable 1'b1: Tile mode enable
2	RW	0x0	sw_fbc_e 1'b0: Fbc disable 1'b1: Fbc enable
1	RW	0x0	sw_colmv_compress_en 1'b0: Disable 1'b1: Enable
0	RO	0x0	reserved

RKVDEC_SWREG13_EN_MODE_SET

Address: Operational Base(0xFF740100) + offset (0x0034)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_filter_outbuf_mode Active at sw_fbc_e=1. 1'b0: Fbchead write ddr with 64byte align 1'b1: Fbchead write ddr not almost 64byte align
30:25	RO	0x00	reserved
24	RW	0x0	sw_cur_pic_is_idr All frame is I frame flag.
23:19	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
18	RW	0x0	sw_error_mode For H264/hevc/avs2: 1'b0: When there is any error, the hardware will stop the decoder and reset itself. 1'b1: When there is any error, the hardware will start error proc and wait frame end. It is recommend that when vp9, it is configed to 1'b0.
17:14	RO	0x0	reserved
13	RW	0x0	sw_fbc_output_wr_disable 1'b0: Fbc output picture data will be write to ddr when sw_fbc_e=1. 1'b1: Fbc output picture data will not be write to ddr even if sw_fbc_e=1.
12	RW	0x0	sw_allow_not_wr_unref_bframe 1'b1: If dec not referance b frame, will not write to ddr. If wan't to set this bit to 1, should set sw_scl_down_en=1 also. It only used in hevc and unsupport tile mode.
11:9	RO	0x0	reserved
8	RW	0x0	sw_strmd_zero_rm_en Default value is 1. Remove extend zero byte, use only at h264 mode.
7	RO	0x0	reserved
6	RW	0x0	sw_stmerror_waitdecfifo_empty When it is 1'b0, the stream error process will no wait the ca2decfifo empty; When it is 1'b1, the stream error process will wait the ca2decfifo empty, when sw_dec_mode is HEVC and VP9. It always take effect. When sw_dec_mode is H264. It only take effect, when sw_h264_error_mode is 1'b0.
5:4	RO	0x0	reserved
3	RW	0x0	sw_dec_commonirq_mode 1'b0: In H264 and vp9 mode, the interrrupt will wait strmd end pulse. 1'b1: In H264 and vp9 mode, the interrupt will not wait strmd end plus.
2	RO	0x0	reserved
1	RW	0x0	sw_req_timeout_rst_sel Use for multicore pu/colmv offset req timeout reset enable select active when the counter is 16'hffff. 1'b0: Req timeout reset enable 1'b1: Req timeout reset disable
0	RO	0x0	reserved

RKVDEC_SWREG14_FBC_PARAM_SET

Address: Operational Base(0xFF740100) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	sw_fbc_h264_exten_4or8_flag It was h264 mbaff flag. 1'b0: Not mabff 1'b1: Mabff
5:4	RO	0x0	reserved
3	RW	0x0	sw_allow_16x8_cp_flag 1'b0: Not allow 1'b1: Allow The config value is depend on vop work mode.

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Bit	Attr	Reset Value	Description
2:1	RO	0x0	reserved
0	RW	0x0	sw_fbc_force_uncompress 1'b0: Allow fbce compress yuv block 1'b1: Force all yuv block use uncompress mode

RKVDEC_SWREG15_STREAM_PARAM_SET

Address: Operational Base(0xFF740100) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:5	RW	0x00	sw_strm_start_bit Exact bit of streamd start word where decoding can be started (asosiates with sw_str_rlc_base).
4:3	RO	0x0	reserved
2	RW	0x0	sw_strmd_ofifo_perf_opt_en Strmd output fifo performance option. 1'b0: Disable 1'b1: Enable
1	RW	0x0	sw_rlc_mode 1'b0: Hw decodes video from bit stream 1'b1: Hw decodes video from RLC input data
0	RW	0x0	sw_rlc_mode_direct_write Cabac decode output direct write enable. When this bit is enable, all the module other than cabac and busifd are not work.

RKVDEC_SWREG16_STREAM_LEN

Address: Operational Base(0xFF740100) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_stream_len Amount of stream 8bits in the input buffer, byte unitL. The max of sw_stream_len: min(65536x65536x1.5x1.5,4G) = 4G.

RKVDEC_SWREG17_SLICE_NUMBER

Address: Operational Base(0xFF740100) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:0	RW	0x0000000	sw_slice_num Hevc: Slice number in a frame (0~199, when it is 0, it real means 1 slice in a frame), just only used for rps read. The meaning from count from 1, so it will be in 1~200. H264: Slice number in a frame (0~4095, when it is 1, it real means 1 slice in a frame) Vp9: No use

RKVDEC_SWREG18_Y_HOR_STRIDE

Address: Operational Base(0xFF740100) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	sw_y_hor_virstride Picture horizontal virtual stride (the unit is 128bit). The max is (4096x1.5 + 128) /16 = 0x188. Suggest this register to config to even for advance ddr performance. Fbc mode: Used for head hor virstirde 2015.10.23, change from 9 bit to 10bit.

RKVDEC_SWREG19_UV_HOR_STRIDE

Address: Operational Base(0xFF740100) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_uv_hor_virstride Picture horizontal virtual stride (the unit is 128bit). The max is (4096x1.5 + 128) /16 = 0x188. Suggest this register to config to even for advance ddr performance.

RKVDEC_SWREG20_FBC_PAYLOAD_OFFSET

Address: Operational Base(0xFF740100) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_fbc_payload_base_addr The offset should be 128bit align. [Note]: The payload will be store in the base: sw_decout_base + sw_payload_st_offset.
3:0	RO	0x0	reserved

RKVDEC_SWREG20_Y_STRIDE

Address: Operational Base(0xFF740100) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_y_virstride The output picture y virtual stride (the unit is 128bit). The max:min((65536x1.5 +128) x 65536,4G) = 4G. We can know the sw_uvout_base = sw_decout_base + (sw_y_virstride <<4). 2015.10.23, change from 20bits to 21bits.

RKVDEC_SWREG21_ERROR_CTRL_SET

Address: Operational Base(0xFF740100) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	sw_roi_error_ctu_cal_en 1'b0: Disable 1'b1: Enable
23:13	RO	0x000	reserved
12	RW	0x0	sw_error_inter_pred_cross_slice 1'b0: Inter mv pred can't cross slice boundary. 1'b1: Inter mv pred will cross slice boundary. It only be used when sw_inter_error_prc_mode=0.
11:9	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
8	RW	0x0	sw_error_spread_e 1'b0: Error info spread disable 1'b1: Error info spread enable Error info spread unit is ctu size. H264/HEVC/AVS2 avaliable.
7:3	RW	0x00	sw_picidx_replace Hevc: [4:1]: Default pic idx [0]: Invalid H264: [4:1]: Default pic idx [0]: Field mode, 0 is top field
2	RW	0x0	sw_error_deb_en 1'b0: Disable 1'b1: Enable Only valid when sw_error_prc_intra_mode_sel = 1'b1.
1	RW	0x0	sw_error_intra_mode 1'b0: Use inter mode to proc error ctu 1'b1: Use intra mode to proc error ctu
0	RW	0x0	sw_inter_error_prc_mode 1'b0: Mv used pred 1'b1: Mv=0, and sw_error_ref_base will be used

RKVDEC_SWREG22_ERR_ROI_CTU_OFFSET_START

Address: Operational Base(0xFF740100) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_roi_y_ctu_offset_st The start offset of ctu_y when roi check.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_roi_x_ctu_offset_st The start offset of ctu_x when roi check.

RKVDEC_SWREG23_ERR_ROI_CTU_OFFSET_END

Address: Operational Base(0xFF740100) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_roi_y_ctu_offset_end The end offset of ctu_y when roi check.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_roi_x_ctu_offset_end The end offset of ctu_x when roi check.

RKVDEC_SWREG24_CABAC_ERROR_EN_LOWBITS

Address: Operational Base(0xFF740100) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_cabac_error_en_lowbits Cabac error enable config.

RKVDEC_SWREG25_CABAC_ERROR_EN_HIGHBITS

Address: Operational Base(0xFF740100) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	sw_cabac_error_en_highbits Cabac error enable high bits config.

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RKVDEC_SWREG26_BLOCK_GATING_EN

Address: Operational Base(0xFF740100) + offset (0x0068)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_reg_cfg_gating_en 1'b0: Disable 1'b1: Enable auto gating
30:20	RO	0x000	reserved
19	RW	0x0	sw_clk_gate_style_disable 1'b0: Enable 1'b1: Disable
18	RO	0x0	reserved
17	RW	0x0	sw_cru_auto_gating_e 1'b0: Disable 1'b1: Enable auto gating
16	RW	0x0	sw_sram_auto_gating_e 1'b0: Disable 1'b1: Enable auto gating
15:12	RO	0x0	reserved
11	RW	0x0	sw_transd_auto_gating_e 1'b0: Disable 1'b1: Enable auto gating
10	RW	0x0	sw_mc_auto_gating_e 1'b0: Disable 1'b1: Enable auto gating
9	RW	0x0	sw_intra_auto_gating_e 1'b0: Disable 1'b1: Enable auto gating
8	RW	0x0	sw_dec_ctrl_auto_gating_e 1'b0: Disable 1'b1: Enable auto gating
7:5	RO	0x0	reserved
4	RW	0x0	sw_strmd_pps_gating_e 1'b0: Disable 1'b1: Enable auto gating
3	RW	0x0	sw_mcp_auto_gating_e 1'b0: Disable 1'b1: Enable auto gating
2	RW	0x0	sw_strmd_auto_gating_e 1'b0: Disable 1'b1: Enable auto gating
1	RW	0x0	sw_filterd_auto_gating_e 1'b0: Disable 1'b1: Enable auto gating
0	RW	0x0	sw_inter_auto_gating_e 1'b0: Disable 1'b1: Enable auto gating

RKVDEC_SWREG27_CORE_SAFE_PIXELS

Address: Operational Base(0xFF740100) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_core_safe_y_pixles Colmv and recon report coord y safe pixels.
15:0	RW	0x0000	sw_core_safe_x_pixels Colmv and recon report coord x safe pixels.

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RKVDEC_SWREG28_MULTIPLY_CORE_CTRL

Address: Operational Base(0xFF740100) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	sw_colmv_req_mismatch_dis Inter colmv set req flag care refpoc mismatch flag is 1 or not. 1'b0: Inter colmv set req flag care mismatch flag. 1'b1: Inter colmv set req flag not care mismatch flag.
28	RW	0x0	sw_pu_req_mismatch_dis Inter pu set req flag care refpoc mismatch flag is 1 or not. 1'b0: Inter pu set req flag care mismatch flag. 1'b1: Inter pu set req flag not care mismatch flag.
27:26	RO	0x0	reserved
25:16	RW	0x000	sw_film_idx Film index is separe from difference decode sequences.
15:12	RO	0x0	reserved
11	RW	0x0	sw_poc_arb_flag Multiply core use poc arb flag, without common 32bits poc, but not include vp9 format. 1'b0: Use common 32bits base addr flag 1'b1: Use common 32bits poc or highbit poc flag
10	RW	0x0	sw_poc_only_highbit_flag Multiply core use only highbit poc flag, without common 32bits poc, but not include vp9 format. 1'b0: Use common 32bits poc and highbit poc flag 1'b1: Only use highbit poc flag
9	RW	0x0	sw_colmv_req_advance_flag Inter colmv data reqire with advance 1/4 picture right and height flag. 1'b0: Pixels offset not advance 1'b1: Pixels x and y offset both advance
8	RW	0x0	sw_ref_req_advance_flag Inter pu reference pred data reqire with advance 1/4 picture right and height flag. 1'b0: Pixels offset not advance 1'b1: Pixels x and y offset both advance
7	RO	0x0	reserved
6:4	RW	0x0	sw_vp9_rd_prob_idx Reference prob index only vp9 used.
3	RO	0x0	reserved
2:0	RW	0x0	sw_vp9_wr_prob_idx Current prob index only vp9 used.

RKVDEC_SWREG29_SCALE_DOWN_CTRL

Address: Operational Base(0xFF740100) + offset (0x0074)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_scale_down_tile_mode 1'b0: Scale down raster mode 1'b1: Scale down tile mode No used
30	RW	0x0	sw_scale_down_roi_mode Scale down roi mode enable.
29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28:24	RW	0x00	sw_scale_down_c_hratio Scale down chroma height ratio 5'h0: No support 5'h1: Orginal size 5'h2: 1/2 picture height size Others: No support
23:21	RO	0x0	reserved
20:16	RW	0x00	sw_scale_down_c_wratio Scale down chroma width ratio 5'h0: No support 5'h1: Orginal size 5'h2: 1/2 picture width size Others: No support
15:13	RO	0x0	reserved
12:8	RW	0x00	sw_scale_down_y_hratio Scale down luma height ratio 5'h0: No support 5'h1: Orginal size 5'h2: 1/2 picture height size Others: No support
7:5	RO	0x0	reserved
4:0	RW	0x00	sw_scale_down_y_wratio Scale down luma width ratio 5'h0: No support 5'h1: Orginal size 5'h2: 1/2 picture width size Others: No support

RKVDEC_SWREG30_Y_SCALE_DOWN_TILE8X8_HOR_STRIDE

Address: Operational Base(0xFF740100) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_y_scale_down_tile8x8_hor_stride Picture horizontal virtual stride (the unit is 128bit).

RKVDEC_SWREG31_UV_SCALE_DOWN_TILE8X8_HOR_STRIDE

Address: Operational Base(0xFF740100) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_uv_scale_down8x8_tile_hor_stride Picture horizontal virtual stride (the unit is 128bit).

RKVDEC_SWREG32_TIMEOUT_THRESHOLD

Address: Operational Base(0xFF740100) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_timeout_threshold Aclk cnt if equal to sw_timeout_threshold,it will give timeout.

RKVDEC_SWREG33_LINE_IRQ_CTRL

Address: Operational Base(0xFF740100) + offset (0x0084)

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_buf_empty_timeout_threshold Buffer empty filterd timeout threshold counter with 256cycle unit. eg. 8'h1: Filterd timeout threshold active at counter 1x256=256 cycles. 8'h8: Filterd timeout threshold active at counter 8x256=2048 cycles.
23:12	RW	0x000	sw_dec_line_offset_y_st Decoder line irq should above the config value of offset y y offset threshold with 16pixels. eg. 12'h1: Decoder line irq occur at line start or above with 1x16=16 value. 12'h8: Decoder line irq occur at line start or above with 8x16=128 value.
11:0	RW	0x000	sw_dec_line_irq_step Decoder line irq offset y steps with 16pixels. eg. Value 0 active dec line irq with lpf report each minimum lines offset y. Value 1 active dec line irq with lpf report each 16 lines offset y. Value 2 active dec line irq with lpf report each 32 lines offset y.

RKVDEC_SWREG34_SCALE_DOWN_ROI_OFFSET

Address: Operational Base(0xFF740100) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_scale_down_roi_st_offsety Scale down roi y start offset at pixels unit
15:0	RW	0x0000	sw_scale_down_roi_st_offsetx Scale down roi x start offset at pixels unit

RKVDEC_SWREG35_SCALE_DOWN_ROI_OUT_SIZE

Address: Operational Base(0xFF740100) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_scale_down_roi_out_height Scale down roi output height
15:0	RW	0x0000	sw_scale_down_roi_out_width Scale down roi output width

RKVDEC_SWREG64_H26X_SET

Address: Operational Base(0xFF740100) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	sw_h264_first_slice_flag 1'b1: First packet in the frame, for h264 decode to read rps/pps data, because the first_mb_in_slice may be wrong, so need this syntax.
3	RW	0x0	sw_h26x_stream_lastpacket When sw_h26x_stream_mode is 1'b1, sw_h26x_stream_lastpacket. 1'b0: This packet is not the last packet of frame. 1'b1: The packet is the last packet of frame.

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Bit	Attr	Reset Value	Description
2	RW	0x0	sw_h26x_stream_mode 1'b0: Stream packet is slice by slice or frame by frame, should use sw_h26x_frame_orslice. 1'b1: Stream packet is random, should use sw_h26x_stream_last.
1	RW	0x0	sw_h26x_rps_mode 1'b0: Hardware parse rps mode. 1'b1: Software parse rps mode.
0	RW	0x0	sw_h26x_frame_orslice For H26x use 1'b0: Frame 1'b1: Slice When sw_h26x_streamd_mode is 1'b0, this register is valid.

RKVDEC_SWREG64_VP9_SET

Address: Operational Base(0xFF740100) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_vp9_cprheader_offset Vp9 compressed header offset, at most 2000 probs, 10bit per prob, 20000 bit at most. Now is for no use, because it can read from the last syntax of the uncompressed header.

RKVDEC_SWREG65_CUR_POC

Address: Operational Base(0xFF740100) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_cur_poc The poc of the cur picture For H264, it may be cur frame poc or cur top field poc.

RKVDEC_SWREG66_H264_CUR_POC1

Address: Operational Base(0xFF740100) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_h264_cur_poc1 H264 cur poc for bottom field

RKVDEC_SWREG67_REF0_POC

Address: Operational Base(0xFF740100) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer0_poc Hevc & h264 & avs2: The poc of reference picture index 0

RKVDEC_SWREG67_VP9_SEGID_GRP0

Address: Operational Base(0xFF740100) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	RW	0x0	sw_vp9segid0_frame_skip_en Frame skip feature enable
21:20	RW	0x0	sw_vp9segid0_referinfo Specifies segment i's reference_info which is used to get ref_frame[0]
19	RW	0x0	sw_vp9segid0_referinfo_en Frame reference info enable

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Bit	Attr	Reset Value	Description
18:12	RW	0x00	sw_vp9segid0_frame_loopfilter_value Specifies segment i's loopfilter_delta value which is used to calculate filter level
11	RW	0x0	sw_vp9segid0_frame_loopfitler_value_en Frame_loopfilter_value feature enable
10:2	RW	0x000	sw_vp9segid0_frame_qp_delta Specifies segment i's qp_delta value which is used to calculate y_dequant and uv_dequant
1	RW	0x0	sw_vp9segid0_frame_qp_delta_en Frame_qp_delta feature enable
0	RW	0x0	sw_vp9segid_abs_delta Used to decide quant and loopfilter param

RKVDEC_SWREG68_REF1_POC

Address: Operational Base(0xFF740100) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer1_poc Hevc & h264 & avs2: The poc of reference picture index 1

RKVDEC_SWREG68_VP9_SEGID_GRP1

Address: Operational Base(0xFF740100) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	RW	0x0	sw_vp9segid1_frame_skip_en Frame skip feature enable
21:20	RW	0x0	sw_vp9segid1_referinfo Specifies segment i's reference_info which is used to get ref_frame[0]
19	RW	0x0	sw_vp9segid1_referinfo_en Frame reference info enable
18:12	RW	0x00	sw_vp9segid1_frame_loopfilter_value Specifies segment i's loopfilter_delta value which is used to calculate filter level
11	RW	0x0	sw_vp9segid1_frame_loopfitler_value_en Frame_loopfilter_value feature enable
10:2	RW	0x000	sw_vp9segid1_frame_qp_delta Specifies segment i's qp_delta value which is used to calculate y_dequant and uv_dequant
1	RW	0x0	sw_vp9segid1_frame_qp_delta_en Frame_qp_delta feature enable
0	RO	0x0	reserved

RKVDEC_SWREG69_REF2_POC

Address: Operational Base(0xFF740100) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer2_poc Hevc & h264 & avs2: The poc of reference picture index 2

RKVDEC_SWREG69_VP9_SEGID_GRP2

Address: Operational Base(0xFF740100) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	RW	0x0	sw_vp9segid2_frame_skip_en Frame skip feature enable

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Bit	Attr	Reset Value	Description
21:20	RW	0x0	sw_vp9segid2_referinfo Specifies segment i's reference_info which is used to get ref_frame[0]
19	RW	0x0	sw_vp9segid2_referinfo_en Frame reference info enable
18:12	RW	0x00	sw_vp9segid2_frame_loopfilter_value Specifies segment i's loopfilter_delta value which is used to calculate filter level
11	RW	0x0	sw_vp9segid2_frame_loopfitler_value_en Frame_loopfilter_value feature enable
10:2	RW	0x000	sw_vp9segid2_frame_qp_delta Specifies segment i's qp_delta value which is used to calculate y_dequant and uv_dequant
1	RW	0x0	sw_vp9segid2_frame_qp_delta_en Frame_qp_delta feature enable
0	RO	0x0	reserved

RKVDEC_SWREG70_REF3_POC

Address: Operational Base(0xFF740100) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer3_poc Hevc & h264 & avs2: The poc of reference picture index 3

RKVDEC_SWREG70_VP9_SEGID_GRP3

Address: Operational Base(0xFF740100) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	RW	0x0	sw_vp9segid3_frame_skip_en Frame skip feature enable
21:20	RW	0x0	sw_vp9segid3_referinfo Specifies segment i's reference_info which is used to get ref_frame[0]
19	RW	0x0	sw_vp9segid3_referinfo_en Frame reference info enable
18:12	RW	0x00	sw_vp9segid3_frame_loopfilter_value Specifies segment i's loopfilter_delta value which is used to calculate filter level
11	RW	0x0	sw_vp9segid3_frame_loopfitler_value_en Frame_loopfilter_value feature enable
10:2	RW	0x000	sw_vp9segid3_frame_qp_delta Specifies segment i's qp_delta value which is used to calculate y_dequant and uv_dequant
1	RW	0x0	sw_vp9segid3_frame_qp_delta_en Frame_qp_delta feature enable
0	RO	0x0	reserved

RKVDEC_SWREG71_REF4_POC

Address: Operational Base(0xFF740100) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer4_poc Hevc & h264 & avs2: The poc of reference picture index 4

RKVDEC_SWREG71_VP9_SEGID_GRP4

Address: Operational Base(0xFF740100) + offset (0x011C)

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Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	RW	0x0	sw_vp9segid4_frame_skip_en Frame skip feature enable
21:20	RW	0x0	sw_vp9segid4_referinfo Specifies segment i's reference_info which is used to get ref_frame[0]
19	RW	0x0	sw_vp9segid4_referinfo_en Frame reference info enable
18:12	RW	0x00	sw_vp9segid4_frame_loopfilter_value Specifies segment i's loopfilter_delta value which is used to calculate filter level
11	RW	0x0	sw_vp9segid4_frame_loopfitler_value_en Frame_loopfilter_value feature enable
10:2	RW	0x000	sw_vp9segid4_frame_qp_delta Specifies segment i's qp_delta value which is used to calculate y_dequant and uv_dequant
1	RW	0x0	sw_vp9segid4_frame_qp_delta_en Frame_qp_delta feature enable
0	RO	0x0	reserved

RKVDEC_SWREG72_REF5_POC

Address: Operational Base(0xFF740100) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer5_poc Hevc & h264 & avs2: The poc of reference picture index 5

RKVDEC_SWREG72_VP9_SEGID_GRP5

Address: Operational Base(0xFF740100) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	RW	0x0	sw_vp9segid5_frame_skip_en Frame skip feature enable
21:20	RW	0x0	sw_vp9segid5_referinfo Specifies segment i's reference_info which is used to get ref_frame[0]
19	RW	0x0	sw_vp9segid5_referinfo_en Frame reference info enable
18:12	RW	0x00	sw_vp9segid5_frame_loopfilter_value Specifies segment i's loopfilter_delta value which is used to calculate filter level
11	RW	0x0	sw_vp9segid5_frame_loopfitler_value_en Frame_loopfilter_value feature enable
10:2	RW	0x000	sw_vp9segid5_frame_qp_delta Specifies segment i's qp_delta value which is used to calculate y_dequant and uv_dequant
1	RW	0x0	sw_vp9segid5_frame_qp_delta_en Frame_qp_delta feature enable
0	RO	0x0	reserved

RKVDEC_SWREG73_REF6_POC

Address: Operational Base(0xFF740100) + offset (0x0124)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer6_poc Hevc & h264 & avs2: The poc of reference picture index 6

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RKVDEC_SWREG73_VP9_SEGID_GRP6

Address: Operational Base(0xFF740100) + offset (0x0124)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	RW	0x0	sw_vp9segid6_frame_skip_en Frame skip feature enable
21:20	RW	0x0	sw_vp9segid6_referinfo Specifies segment i's reference_info which is used to get ref_frame[0]
19	RW	0x0	sw_vp9segid6_referinfo_en Frame reference info enable
18:12	RW	0x00	sw_vp9segid6_frame_loopfilter_value Specifies segment i's loopfilter_delta value which is used to calculate filter level
11	RW	0x0	sw_vp9segid6_frame_loopfitler_value_en Frame_loopfilter_value feature enable
10:2	RW	0x000	sw_vp9segid6_frame_qp_delta Specifies segment i's qp_delta value which is used to calculate y_dequant and uv_dequant
1	RW	0x0	sw_vp9segid6_frame_qp_delta_en Frame_qp_delta feature enable
0	RO	0x0	reserved

RKVDEC_SWREG74_REF7_POC

Address: Operational Base(0xFF740100) + offset (0x0128)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer7_poc Hevc & h264 & avs2: The poc of reference picture index 7

RKVDEC_SWREG74_VP9_SEGID_GRP7

Address: Operational Base(0xFF740100) + offset (0x0128)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	RW	0x0	sw_vp9segid7_frame_skip_en Frame skip feature enable
21:20	RW	0x0	sw_vp9segid7_referinfo Specifies segment i's reference_info which is used to get ref_frame[0]
19	RW	0x0	sw_vp9segid7_referinfo_en Frame reference info enable
18:12	RW	0x00	sw_vp9segid7_frame_loopfilter_value Specifies segment i's loopfilter_delta value which is used to calculate filter level
11	RW	0x0	sw_vp9segid7_frame_loopfitler_value_en Frame_loopfilter_value feature enable
10:2	RW	0x000	sw_vp9segid7_frame_qp_delta Specifies segment i's qp_delta value which is used to calculate y_dequant and uv_dequant
1	RW	0x0	sw_vp9segid7_frame_qp_delta_en Frame_qp_delta feature enable
0	RO	0x0	reserved

RKVDEC_SWREG75_REF8_POC

Address: Operational Base(0xFF740100) + offset (0x012C)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer8_poc Hevc & h264: The poc of reference picture index 8

RKVDEC_SWREG75_VP9_INFO_LASTFRAME

Address: Operational Base(0xFF740100) + offset (0x012C)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RW	0x0	sw_vp9_color_space_lastkeyframe Vp9 last keyframe color_space
19	RW	0x0	sw_vp9_last_widhheight_eqcur Last width and height equal cur frame
18	RW	0x0	sw_vp9_last_intra_only Vp9 last frame intra only flag, to give inter command use It is for last_dec_frame.
17	RW	0x0	sw_vp9_last_showframe For cal the flag use_prev_in_find_mv_refs which is to inter cmd. It is for last_dec_frame.
16	RW	0x0	sw_segmentation_enable_lstframe 1'b1: sw_segmentation_enable for last frame It is for last_dec_frame.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_vp9_mode_deltas_lastframe Vp9 mode deltas It is for last dec frame.

RKVDEC_SWREG76_REF9_POC

Address: Operational Base(0xFF740100) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer9_poc Hevc & h264: The poc of reference picture index 9

RKVDEC_SWREG76_VP9_CPRHEADER_CONFIG

Address: Operational Base(0xFF740100) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:3	RW	0x0	sw_vp9_frame_reference_mode Frame_reference_mode specifies frame reference mode SINGLE_REFERENCE = 0, COMPOUND_REFERENCE = 1, REFERENCE_MODE_SELECT = 2, REFERENCE_MODES = 3, When frame_reference_mode_flag0 is not present ,it equal to 0 by default. When frame_reference_mode_flag1 is not present ,it equal to 0 by default. frame_reference_mode = frame_reference_mode_flag0 == 0 ? frame_reference_mode_flag1 == 0 ? REFERENCE_MODE_SELECT : COMPOUND_REFERENCE) : SINGLE_REFERENCE.

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Bit	Attr	Reset Value	Description

2:0	RW	0x0	sw_vp9_tx_mode
			Tx_mode specifies frame transform mode
			ONLY_4X4 = 0, // only 4x4 transform used.
			ALLOW_8X8 = 1, // allow block transform size up to 8x8.
			ALLOW_16X16 = 2, // allow block transform size up to 16x16.
			ALLOW_32X32 = 3, // allow block transform size up to 32x32.
			TX_MODE_SELECT = 4, // transform specified for each block.

RKVDEC_SWREG77_REF10_POC

Address: Operational Base(0xFF740100) + offset (0x0134)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer10_poc Hevc & h264: The poc of reference picture index 10

RKVDEC_SWREG77_VP9_INTERCMD_NUM

Address: Operational Base(0xFF740100) + offset (0x0134)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	sw_vp9_intercmd_num When rlc_mode is 1'b1, for sw_vp9_intercmd_num Its unit is 128bit. It count from 1.

RKVDEC_SWREG78_REF11_POC

Address: Operational Base(0xFF740100) + offset (0x0138)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer11_poc Hevc & h264: The poc of reference picture index 11.

RKVDEC_SWREG78_VP9_STREAM_SIZE

Address: Operational Base(0xFF740100) + offset (0x0138)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_vp9_stream_size The size of vp9 compressed header and compressed frame data Its unit is byte. The real meaning the current frame size.

RKVDEC_SWREG79_REF12_POC

Address: Operational Base(0xFF740100) + offset (0x013C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer12_poc Hevc & h264: The poc of reference picture index 12

RKVDEC_SWREG79_VP9_LASTF_Y_HOR_VIRSTRIDE

Address: Operational Base(0xFF740100) + offset (0x013C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_vp9_lastfy_hor_virstride Vp9 last frame y horizontal virstride 2015.10.23, change from 9bits to 10bits. For fbc mode: Vp9 head hor stride of last frame.

RKVDEC_SWREG80_REF13_POC

Address: Operational Base(0xFF740100) + offset (0x0140)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer13_poc Hevc & h264: The poc of reference picture index 13.

RKVDEC_SWREG80_VP9_LASTF_UV_HOR_VIRSTRIDE

Address: Operational Base(0xFF740100) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_vp9_lastfuv_hor_virstride Vp9 last frame uv horizontal virstride. 2015.10.23, change from 9bits to 10bits.

RKVDEC_SWREG81_REF14_POC

Address: Operational Base(0xFF740100) + offset (0x0144)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer14_poc Hevc & h264: The poc of reference picture index 14

RKVDEC_SWREG81_VP9_GOLDENF_Y_HOR_VIRSTRIDE

Address: Operational Base(0xFF740100) + offset (0x0144)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_vp9_goldenfy_hor_virstride Vp9 golden frame y horizontal virstride 2015.10.23, change from 9bits to 10bits. For fbc mode: Vp9 head hor stride of golden frame.

RKVDEC_SWREG82_REF15_POC

Address: Operational Base(0xFF740100) + offset (0x0148)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer15_poc The poc of reference picture index 15 Used to hevc for mvc

RKVDEC_SWREG82_VP9_GOLDEN_UV_HOR_VIRSTRIDE

Address: Operational Base(0xFF740100) + offset (0x0148)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_vp9_goldenuv_hor_virstride Vp9 golden uv horizontal virstirde 2015.10.23, change from 9bits to 10bits.

RKVDEC_SWREG83_REF16_POC

Address: Operational Base(0xFF740100) + offset (0x014C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer16_poc H264: The poc of reference picture index 16 Hevc & vp9: Now is no use

RKVDEC_SWREG83_VP9_ALTREFF_Y_HOR_VIRSTRIDE

Address: Operational Base(0xFF740100) + offset (0x014C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	sw_vp9_altreffy_hor_virstride Vp9 altref frame y horizontal virstride 2015.10.23, change from 9bits to 10bits. For fbc mode: Vp9 head hor stride of after frame.

RKVDEC_SWREG84_REF17_POC

Address: Operational Base(0xFF740100) + offset (0x0150)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer17_poc H264: The poc of reference picture index 17 Hevc & vp9: Now is no use.

RKVDEC_SWREG84_VP9_ALTREFF_UV_HOR_VIRSTRIDE

Address: Operational Base(0xFF740100) + offset (0x0150)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_vp9_altreffuv_hor_virstride Vp9 altreff uv horizontal virstirde 2015.10.23, change from 9bits to 10bits.

RKVDEC_SWREG85_REF18_POC

Address: Operational Base(0xFF740100) + offset (0x0154)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer18_poc H264: The poc of reference picture index 18 Hevc & vp9: Now is no use.

RKVDEC_SWREG85_VP9_LASTF_Y_VIRSTRIDE

Address: Operational Base(0xFF740100) + offset (0x0154)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_vp9_lastfy_virstride Vp9 last frame y stride 2015.10.23, change from 20bits to 21bits.

RKVDEC_SWREG86_REF19_POC

Address: Operational Base(0xFF740100) + offset (0x0158)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer19_poc H264: The poc of reference picture index 19 Hevc & vp9: Now is no use.

RKVDEC_SWREG86_VP9_GOLDEN_Y_VIRSTRIDE

Address: Operational Base(0xFF740100) + offset (0x0158)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_vp9_goldeny_virstride Vp9 golden frame y stride 2015.10.23, change from 20bits to 21bits.

RKVDEC_SWREG87_REF20_POC

Address: Operational Base(0xFF740100) + offset (0x015C)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer20_poc H264: The poc of reference picture index 20 Hevc & vp9: Now is no use.

RKVDEC_SWREG87_VP9_ALTREF_Y_VIRSTRIDE

Address: Operational Base(0xFF740100) + offset (0x015C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_vp9_altrefy_virstride Vp9 altref frame y stride Change from 20bits to 21bits.

RKVDEC_SWREG88_REF21_POC

Address: Operational Base(0xFF740100) + offset (0x0160)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer21_poc H264: The poc of reference picture index 21 Hevc & vp9: Now is no use.

RKVDEC_SWREG88_VP9_LREF_HOR_SCALE

Address: Operational Base(0xFF740100) + offset (0x0160)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_vp9_lref_hor_scale Horizontal scaling factor for last reference picture Sw_vp9_lref_hor_scale = (last_ref_width / cur_width) * 0x4000

RKVDEC_SWREG89_REF22_POC

Address: Operational Base(0xFF740100) + offset (0x0164)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer22_poc H264: The poc of reference picture index 22 Hevc & vp9: Now is no use.

RKVDEC_SWREG89_VP9_LREF_VER_SCALE

Address: Operational Base(0xFF740100) + offset (0x0164)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_vp9_lref_ver_scale Vertical scaling factor for last reference picture

RKVDEC_SWREG90_REF23_POC

Address: Operational Base(0xFF740100) + offset (0x0168)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer23_poc H264: The poc of reference picture index 23 Hevc & vp9: Now is no use.

RKVDEC_SWREG90_VP9_GREF_HOR_SCALE

Address: Operational Base(0xFF740100) + offset (0x0168)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	sw_vp9_gref_hor_scale Horizontal scaling factor for golden reference picture Sw_vp9_gref_hor_scale = (golden_ref_width / cur_width) * 0x4000.

RKVDEC_SWREG91_REF24_POC

Address: Operational Base(0xFF740100) + offset (0x016C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer24_poc H264: The poc of reference picture index 24 Hevc & vp9: Now is no use.

RKVDEC_SWREG91_VP9_GREF_VER_SCALE

Address: Operational Base(0xFF740100) + offset (0x016C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_vp9_gref_ver_scale Vertical scaling factor for golden reference picture

RKVDEC_SWREG92_REF25_POC

Address: Operational Base(0xFF740100) + offset (0x0170)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer25_poc H264: The poc of reference picture index 25 Hevc & vp9: Now is no use.

RKVDEC_SWREG92_VP9_AREF_HOR_SCALE

Address: Operational Base(0xFF740100) + offset (0x0170)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_vp9_aref_hor_scale Horizontal scaling factor for alfter reference picture Sw_vp9_gref_hor_scale = (alfter_ref_width / cur_width) * 0x4000

RKVDEC_SWREG93_REF26_POC

Address: Operational Base(0xFF740100) + offset (0x0174)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer26_poc H264: The poc of reference picture index 26 Hevc & vp9: Now is no use.

RKVDEC_SWREG93_VP9_AREF_VER_SCALE

Address: Operational Base(0xFF740100) + offset (0x0174)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_vp9_aref_ver_scale Vertical scaling factor for alfter reference picture

RKVDEC_SWREG94_REF27_POC

Address: Operational Base(0xFF740100) + offset (0x0178)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer27_poc H264: The poc of reference picture index 27 Hevc & vp9: Now is no use.

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RKVDEC_SWREG94_VP9_REF_DELTAS_LASTFRAME

Address: Operational Base(0xFF740100) + offset (0x0178)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_vp9_ref_deltas_lastframe Vp9 ref deltas of lastframe, for cal loopfilter filter type use

RKVDEC_SWREG95_REF28_POC

Address: Operational Base(0xFF740100) + offset (0x017C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer28_poc H264: The poc of reference picture index 28 Hevc & vp9: Now is no use.

RKVDEC_SWREG95_VP9_LAST_POC

Address: Operational Base(0xFF740100) + offset (0x017C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_vp9_last_poc VP9: The poc of last reference

RKVDEC_SWREG96_REF29_POC

Address: Operational Base(0xFF740100) + offset (0x0180)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer29_poc H264: The poc of reference picture index 29 Hevc & vp9: Now is no use.

RKVDEC_SWREG96_VP9_GOLDEN_POC

Address: Operational Base(0xFF740100) + offset (0x0180)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_vp9_golden_poc VP9: The poc of golden reference

RKVDEC_SWREG97_REF30_POC

Address: Operational Base(0xFF740100) + offset (0x0184)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer30_poc H264: The poc of reference picture index 30 Hevc & vp9: Now is no use.

RKVDEC_SWREG97_VP9_ALTREF_POC

Address: Operational Base(0xFF740100) + offset (0x0184)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_vp9_altref_poc VP9: The poc of altref reference

RKVDEC_SWREG98_REF31_POC

Address: Operational Base(0xFF740100) + offset (0x0188)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer31_poc H264: The poc of reference picture index 31 Hevc & vp9: Now is no use.

RKVDEC_SWREG98_VP9_COL_REF_POC

Address: Operational Base(0xFF740100) + offset (0x0188)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_vp9_col_ref_poc VP9: The poc of colpic reference

RKVDEC_SWREG99_HEVC_REF_VALID

Address: Operational Base(0xFF740100) + offset (0x018C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RW	0x0	sw_hevc_ref_valid_14 Valid flag for picture index 14
25	RW	0x0	sw_hevc_ref_valid_13 Valid flag for picture index 13
24	RW	0x0	sw_hevc_ref_valid_12 Valid flag for picture index 12
23:20	RO	0x0	reserved
19	RW	0x0	sw_hevc_ref_valid_11 Valid flag for picture index 11
18	RW	0x0	sw_hevc_ref_valid_10 Valid flag for picture index 10
17	RW	0x0	sw_hevc_ref_valid_9 Valid flag for picture index 9
16	RW	0x0	sw_hevc_ref_valid_8 Valid flag for picture index 8
15:12	RO	0x0	reserved
11	RW	0x0	sw_hevc_ref_valid_7 Valid flag for picture index 7
10	RW	0x0	sw_hevc_ref_valid_6 Valid flag for picture index 6
9	RW	0x0	sw_hevc_ref_valid_5 Valid flag for picture index 5
8	RW	0x0	sw_hevc_ref_valid_4 Valid flag for picture index 4
7:4	RO	0x0	reserved
3	RW	0x0	sw_hevc_ref_valid_3 Valid flag for picture index 3
2	RW	0x0	sw_hevc_ref_valid_2 Valid flag for picture index 2
1	RW	0x0	sw_hevc_ref_valid_1 Valid flag for picture index 1
0	RW	0x0	sw_hevc_ref_valid_0 Valid flag for picture index 0

RKVDEC_SWREG99_H264_REG0_3_INFO

Address: Operational Base(0xFF740100) + offset (0x018C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	sw_ref3_colmv_use_flag Ref3 colmv use flag
26	RW	0x0	sw_ref3_botfield_used Ref3 bottom field is used, the same meaning with ref_valid
25	RW	0x0	sw_ref3_topfield_used Ref3 top field is used, the same meaning with ref_valid
24	RW	0x0	sw_ref3_field 1'b0: Frame 1'b1: Field

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Bit	Attr	Reset Value	Description
23:20	RO	0x0	reserved
19	RW	0x0	sw_ref2_colmv_use_flag Ref2 colmv use flag
18	RW	0x0	sw_ref2_botfield_used Ref2 bottom field is used, the same meaning with ref_valid
17	RW	0x0	sw_ref2_topfield_used Ref2 top field is used, the same meaning with ref_valid
16	RW	0x0	sw_ref2_field 1'b0: Frame 1'b1: Field
15:12	RO	0x0	reserved
11	RW	0x0	sw_ref1_colmv_use_flag Ref1 colmv use flag
10	RW	0x0	sw_ref1_botfield_used Ref1 bottom field is used, the same meaning with ref_valid
9	RW	0x0	sw_ref1_topfield_used Ref1 top field is used, the same meaning with ref_valid
8	RW	0x0	sw_ref1_field 1'b0: Frame 1'b1: Field
7:4	RO	0x0	reserved
3	RW	0x0	sw_ref0_colmv_use_flag Ref0 colmv use flag
2	RW	0x0	sw_ref0_botfield_used Ref0 bottom field is used, the same meaning with ref_valid
1	RW	0x0	sw_ref0_topfield_used Ref0 top field is used, the same meaning with ref_valid
0	RW	0x0	sw_ref0_field 1'b0: Frame 1'b1: Field

RKVDEC_SWREG99_AVS2_REG0_3_INFO

Address: Operational Base(0xFF740100) + offset (0x018C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	sw_ref3_valid_flag Reference picture3 used flag 1'b0: Not be valid 1'b1: Be valid
26	RW	0x0	sw_ref3_botfield_used Refer3 is bottow field flag 1'b0: Top field flag 1'b1: Bottom field flag
25	RO	0x0	reserved
24	RW	0x0	sw_ref3_field 1'b0: Frame 1'b1: Field
23:20	RO	0x0	reserved
19	RW	0x0	sw_ref2_valid_flag Reference picture2 used flag 1'b0: Not be valid 1'b1: Be valid

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Bit	Attr	Reset Value	Description
18	RW	0x0	sw_ref2_botfield_used Refer2 is bottow field flag 1'b0: Top field flag 1'b1: Bottom field flag
17	RO	0x0	reserved
16	RW	0x0	sw_ref2_field 1'b0: Frame 1'b1: Field
15:12	RO	0x0	reserved
11	RW	0x0	sw_ref1_valid_flag Reference picture1 used flag 1'b0: Not be valid 1'b1: Be valid
10	RW	0x0	sw_ref1_botfield_used Refer1 is bottow field flag 1'b0: Top field flag 1'b1: Bottom field flag
9	RO	0x0	reserved
8	RW	0x0	sw_ref1_field 1'b0: Frame 1'b1: Field
7:4	RO	0x0	reserved
3	RW	0x0	sw_ref0_valid_flag Reference picture0 used flag 1'b0: Not be valid 1'b1: Be valid
2	RW	0x0	sw_ref0_botfield_used Refer0 is bottow field flag 1'b0: Top field flag 1'b1: Bottom field flag
1	RO	0x0	reserved
0	RW	0x0	sw_ref0_field 1'b0: Frame 1'b1: Field

RKVDEC_SWREG99_VP9_PROB_REF_POC

Address: Operational Base(0xFF740100) + offset (0x018C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_vp9_prob_ref_poc VP9: The poc of reference prob

RKVDEC_SWREG100_AVS2_REG4_7_INFO

Address: Operational Base(0xFF740100) + offset (0x0190)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	sw_ref7_valid_flag Reference picture7 used flag 1'b0: Not be valid 1'b1: Be valid
26	RW	0x0	sw_ref7_botfield_used Refer7 is bottow field flag 1'b0: Top field flag 1'b1: Bottom field flag
25	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
24	RW	0x0	sw_ref7_field 1'b0: Frame 1'b1: Field
23:20	RO	0x0	reserved
19	RW	0x0	sw_ref6_valid_flag Reference picture6 used flag 1'b0: Not be valid 1'b1: Be valid
18	RW	0x0	sw_ref6_botfield_used Refer6 is bottow field flag 1'b0: Top field flag 1'b1: Bottom field flag
17	RO	0x0	reserved
16	RW	0x0	sw_ref6_field 1'b0: Frame 1'b1: Field
15:12	RO	0x0	reserved
11	RW	0x0	sw_ref5_valid_flag Reference picture5 used flag 1'b0: Not be valid 1'b1: Be valid
10	RW	0x0	sw_ref5_botfield_used Refer5 is bottow field flag 1'b0: Top field flag 1'b1: Bottom field flag
9	RO	0x0	reserved
8	RW	0x0	sw_ref5_field 1'b0: Frame 1'b1: Field
7:4	RO	0x0	reserved
3	RW	0x0	sw_ref4_valid_flag Reference picture4 used flag 1'b0: Not be valid 1'b1: Be valid
2	RW	0x0	sw_ref4_botfield_used Refer4 is bottow field flag 1'b0: Top field flag 1'b1: Bottom field flag
1	RO	0x0	reserved
0	RW	0x0	sw_ref4_field 1'b0: Frame 1'b1: Field.

RKVDEC_SWREG100_H264_REG4_7_INFO

Address: Operational Base(0xFF740100) + offset (0x0190)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	sw_ref7_colmv_use_flag Ref7 colmv use flag
26	RW	0x0	sw_ref7_botfield_used Ref7 bottom field is used, the same meaning with ref_valid
25	RW	0x0	sw_ref7_topfield_used Ref7 top field is used, the same meaning with ref_valid

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Bit	Attr	Reset Value	Description
24	RW	0x0	sw_ref7_field 1'b0: Frame 1'b1: Field
23:20	RO	0x0	reserved
19	RW	0x0	sw_ref6_colmv_use_flag Ref6 colmv use flag
18	RW	0x0	sw_ref6_botfield_used Ref6 bottom field is used, the same meaning with ref_valid
17	RW	0x0	sw_ref6_topfield_used Ref6 top field is used, the same meaning with ref_valid
16	RW	0x0	sw_ref6_field 1'b0: Frame 1'b1: Field
15:12	RO	0x0	reserved
11	RW	0x0	sw_ref5_colmv_use_flag Ref5 colmv use flag
10	RW	0x0	sw_ref5_botfield_used Ref5 bottom field is used, the same meaning with ref_valid
9	RW	0x0	sw_ref5_topfield_used Ref5 top field is used, the same meaning with ref_valid
8	RW	0x0	sw_ref5_field 1'b0: Frame 1'b1: Field
7:4	RO	0x0	reserved
3	RW	0x0	sw_ref4_colmv_use_flag Ref4 colmv use flag
2	RW	0x0	sw_ref4_botfield_used Ref4 bottom field is used, the same meaning with ref_valid
1	RW	0x0	sw_ref4_topfield_used Ref4 top field is used, the same meaning with ref_valid
0	RW	0x0	sw_ref4_field 1'b0: Frame 1'b1: Field

RKVDEC_SWREG100_VP9_SEGID_REF_POC

Address: Operational Base(0xFF740100) + offset (0x0190)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_vp9_segid_ref_poc VP9: The poc of reference segmentid

RKVDEC_SWREG101_H264_REG8_11_INFO

Address: Operational Base(0xFF740100) + offset (0x0194)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	sw_ref11_colmv_use_flag Ref11 colmv use flag
26	RW	0x0	sw_ref11_botfield_used Ref11 bottom field is used, the same meaning with ref_valid
25	RW	0x0	sw_ref11_topfield_used Ref11 top field is used, the same meaning with ref_valid
24	RW	0x0	sw_ref11_field 1'b0: Frame 1'b1: Field
23:20	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
19	RW	0x0	sw_ref10_colmv_use_flag Ref10 colmv use flag
18	RW	0x0	sw_ref10_botfield_used Ref10 bottom field is used, the same meaning with ref_valid
17	RW	0x0	sw_ref10_topfield_used Ref10 top field is used, the same meaning with ref_valid
16	RW	0x0	sw_ref10_field 1'b0: Frame 1'b1: Field
15:12	RO	0x0	reserved
11	RW	0x0	sw_ref9_colmv_use_flag Ref9 colmv use flag
10	RW	0x0	sw_ref9_botfield_used Ref9 bottom field is used, the same meaning with ref_valid
9	RW	0x0	sw_ref9_topfield_used Ref9 top field is used, the same meaning with ref_valid
8	RW	0x0	sw_ref9_field 1'b0: Frame 1'b1: Field
7:4	RO	0x0	reserved
3	RW	0x0	sw_ref8_colmv_use_flag Ref8 colmv use flag
2	RW	0x0	sw_ref8_botfield_used Ref8 bottom field is used, the same meaning with ref_valid
1	RW	0x0	sw_ref8_topfield_used Ref8 top field is used, the same meaning with ref_valid
0	RW	0x0	sw_ref8_field 1'b0: Frame 1'b1: Field

RKVDEC_SWREG102_H264_REG12_15_INFO

Address: Operational Base(0xFF740100) + offset (0x0198)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	sw_ref15_colmv_use_flag Ref15 colmv use flag
26	RW	0x0	sw_ref15_botfield_used Ref15 bottom field is used, the same meaning with ref_valid
25	RW	0x0	sw_ref15_topfield_used Ref15 top field is used, the same meaning with ref_valid
24	RW	0x0	sw_ref15_field 1'b0: Frame 1'b1: Field
23:20	RO	0x0	reserved
19	RW	0x0	sw_ref14_colmv_use_flag Ref14 colmv use flag
18	RW	0x0	sw_ref14_botfield_used Ref14 bottom field is used, the same meaning with ref_valid
17	RW	0x0	sw_ref14_topfield_used Ref14 top field is used, the same meaning with ref_valid
16	RW	0x0	sw_ref14_field 1'b0: Frame 1'b1: Field
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11	RW	0x0	sw_ref13_colmv_use_flag Ref13 colmv use flag
10	RW	0x0	sw_ref13_botfield_used Ref13 bottom field is used, the same meaning with ref_valid
9	RW	0x0	sw_ref13_topfield_used Ref13 top field is used, the same meaning with ref_valid
8	RW	0x0	sw_ref13_field 1'b0: Frame 1'b1: Field
7:4	RO	0x0	reserved
3	RW	0x0	sw_ref12_colmv_use_flag Ref12 colmv use flag
2	RW	0x0	sw_ref12_botfield_used Ref12 bottom field is used, the same meaning with ref_valid
1	RW	0x0	sw_ref12_topfield_used Ref12 top field is used, the same meaning with ref_valid
0	RW	0x0	sw_ref12_field 1'b0: Frame 1'b1: Field

RKVDEC_SWREG103_HEVC_MVC0

Address: Operational Base(0xFF740100) + offset (0x019C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_ref_pic_layer_same_with_cur Referance picture layer same with current picture

RKVDEC_SWREG103_AVS2_CTRL_EXTRA

Address: Operational Base(0xFF740100) + offset (0x019C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	sw_avs2_slice_hor_pos_ctrl 1'b0: Use default 255 1'b1: Use fixed 256

RKVDEC_SWREG103_VP9_PROB_EN

Address: Operational Base(0xFF740100) + offset (0x019C)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_vp9_inter_coef_rfsh_flag 1'b0: Inter coef unneed refresh in current intra frame. 1'b1: Inter coef should be refresh in current intra frame.
30	RW	0x0	sw_vp9_last_key_frame_flag The flag of last frame is key frame 1'b0: Not key frame 1'b1: Key frame
29	RW	0x0	sw_vp9_allow_high_precision_mv The enable of high precision mv prob refresh update 1'b0: Disable 1'b1: Enable
28	RW	0x0	sw_vp9_interp_filter_switch_en The enable of interp filter prob refresh update 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
27	RW	0x0	sw_vp9_comp_ref_rfsh_en The enable of comp reference prob refresh update 1'b0: Disable 1'b1: Enable
26	RW	0x0	sw_vp9_single_ref_rfsh_en The enable of single reference prob refresh update 1'b0: Disable 1'b1: Enable
25	RW	0x0	sw_vp9_ref_mode_rfsh_en The enable of reference mode prob refresh update 1'b0: Disable 1'b1: Enable
24	RW	0x0	sw_vp9_txfmmode_rfsh_en The enable of tx mode prob refresh update 1'b0: Disable 1'b1: Enable
23	RW	0x0	sw_vp9_intra_only_flag The flag of intra only 1'b0: Inter frame 1'b1: Intra only frameinclude key frame
22	RW	0x0	sw_vp9_prob_save_en The flag of write updated prob to DDR 1'b0: Not need write updated prob to DDR 1'b1: Will write updated prob to DDR
21	RW	0x0	sw_vp9_refresh_en The enbale of prob backward refresh 1'b0: Disable refresh parse 1'b1: Enable refresh parse
20	RW	0x0	sw_vp9_prob_update_en The enable of used hardware to parse prob 1'b0: Software parse prob 1'b1: Hardware parse prob
19:0	RO	0x00000	reserved

RKVDEC_SWREG104_HEVC_MVC1

Address: Operational Base(0xFF740100) + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	RW	0x0	sw_mvc_poc15_valid_flag Mvc poc15 valid flag
17	RW	0x0	sw_rps_poc_lsb_aligned_flag Rps POC lsb aligned flag
16	RW	0x0	sw_poc_reset_info_present_flag The flag of poc reset infomation
15	RW	0x0	sw_max_one_active_ref_layer_flag The flag of max referance referance layer be actived
14	RW	0x0	sw_default_ref_layers_active_flag The flag of default referance layers which be actived
13:8	RW	0x00	sw_num_reflayer_pics The number of referance layer pictures
7	RO	0x0	reserved
6:1	RW	0x00	sw_num_direct_ref_layers The number of direct referance layers
0	RW	0x0	sw_poc_lsb_not_present_flag Poc lsb not present flag

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RKVDEC_SWREG105_VP9CNT_UPD_EN_AVS2_HEADLEN

Address: Operational Base(0xFF740100) + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	sw_vp9count_update_en When 1'b1, the hardware will always update count. When 1'b0, the hardware will auto check whether update the count.
3:0	RW	0x0	sw_avs2_head_len It's unit is 128bit. 4'h0: 128bit 4'h1: 2*128bit 4'h2: 3*128bit ..... 4'hf: 16*128bit

RKVDEC_SWREG106_VP9_FRAME_WIDTH_LAST

Address: Operational Base(0xFF740100) + offset (0x01A8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_framewidth_last Last frame frame_size_width

RKVDEC_SWREG107_VP9_FRAME_HEIGHT_LAST

Address: Operational Base(0xFF740100) + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_frameheight_last Last frame frame_size_height

RKVDEC_SWREG108_VP9_FRAME_WIDTH_GOLDEN

Address: Operational Base(0xFF740100) + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_framewidth_golden Golden frame_size_width

RKVDEC_SWREG109_VP9_FRAME_HEIGHT_GOLDEN

Address: Operational Base(0xFF740100) + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_frameheight_golden Golden frame_size_height

RKVDEC_SWREG110_VP9_FRAME_WIDTH_ALTREF

Address: Operational Base(0xFF740100) + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_framewidth_alfter Alfter frame_size_width

RKVDEC_SWREG111_VP9_FRAME_HEIGHT_ALTREF

Address: Operational Base(0xFF740100) + offset (0x01BC)

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Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_frameheight_alfter Alfter frame_size_height

RKVDEC_SWREG112_ERROR_REF_INFO

Address: Operational Base(0xFF740100) + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	sw_ref_error_botfield_used For inter, 1'b1: Botfield is used.
2	RW	0x0	sw_ref_error_topfield_used For inter, 1'b1: Topfield is used.
1	RW	0x0	sw_avs2_ref_error_topfield Refer error is top field flag 1'b0: Bottom field flag 1'b1: Top field flag
0	RW	0x0	sw_avs2_ref_error_field 1'b0: Frame 1'b1: Field

RKVDEC_SWREG128_STRM_RLC_BASE

Address: Operational Base(0xFF740100) + offset (0x0200)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_strm_rlc_base When SWREG2.sw_rlc_mode =1, it is base address for rlc data. When SWREG2.sw_rlc_mode =0, it is base address for stream, after a frame is decoded ready or error (stream error , time out , bus error) , it is the last address of the stream. The address should 128bit align.
3:0	RO	0x0	reserved

RKVDEC_SWREG129_RLCWRITE_BASE

Address: Operational Base(0xFF740100) + offset (0x0204)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	sw_rlcwrite_base The base address of rlcwrite(the address should 64bit align). Cabac output write to this rlcwrite base address when sw_rlc_mode_direct_write in SWREG2_sysctrl is valid.
2:0	RO	0x0	reserved

RKVDEC_SWREG129_ERROR_INFO_BASE

Address: Operational Base(0xFF740100) + offset (0x0204)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	sw_error_info_base The base address of error info
2:0	RO	0x0	reserved

RKVDEC_SWREG130_DECOUT_BASE

Address: Operational Base(0xFF740100) + offset (0x0208)

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Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_decout_base Base address of decoder output picture, the address should be 128bit align. In H264 decode format, the top field and bottom field are the same addr. Fbc mode: Fbc_head_base_addr[27:0]: the head base of fbc wr.
3:0	RO	0x0	reserved

RKVDEC_SWREG131_COLMV_CUR_BASE

Address: Operational Base(0xFF740100) + offset (0x020C)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_colmv_cur_base Only valid when sw_colmv_mode is 1'b1. Cur frame colmv base addr, for HEVC,H264 and vp9.
3:0	RO	0x0	reserved

RKVDEC_SWREG132_ERROR_REF_BASE

Address: Operational Base(0xFF740100) + offset (0x0210)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_error_ref_base Error reference frame base address
3:0	RO	0x0	reserved

RKVDEC_SWREG133_RCB_INTRAR_OFFSET

Address: Operational Base(0xFF740100) + offset (0x0214)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	sw_rcb_intrar_base Rcb intra row base address, unit: 64byts align
5:0	RO	0x00	reserved

RKVDEC_SWREG134_RCB_TRANSDR_OFFSET

Address: Operational Base(0xFF740100) + offset (0x0218)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	sw_rcb_transdr_base Rcb transd row base address, unit: 64byts align
5:0	RO	0x00	reserved

RKVDEC_SWREG135_RCB_TRANSDC_OFFSET

Address: Operational Base(0xFF740100) + offset (0x021C)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	sw_rcb_transdc_base Rcb transd col base address, unit: 64byts align
5:0	RO	0x00	reserved

RKVDEC_SWREG136_RCB_STRMDR_OFFSET

Address: Operational Base(0xFF740100) + offset (0x0220)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	sw_rcb_strmdr_base Rcb stream row base address, unit: 64byts align
5:0	RO	0x00	reserved

RKVDEC_SWREG137_RCB_INTERR_OFFSET

Address: Operational Base(0xFF740100) + offset (0x0224)

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Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	sw_rcb_interr_base Rcb inter row base address, unit: 64byts align
5:0	RO	0x00	reserved

RKVDEC_SWREG138_RCB_INTERC_OFFSET

Address: Operational Base(0xFF740100) + offset (0x0228)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	sw_rcb_interc_base Rcb inter col base address, unit: 64byts align
5:0	RO	0x00	reserved

RKVDEC_SWREG139_RCB_DBLKR_OFFSET

Address: Operational Base(0xFF740100) + offset (0x022C)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	sw_rcb_dblkr_base Rcb dblock row base address, unit: 64byts align
5:0	RO	0x00	reserved

RKVDEC_SWREG140_RCB_SAOR_OFFSET

Address: Operational Base(0xFF740100) + offset (0x0230)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	sw_rcb_saor_base Rcb sao row base address, unit: 64byts align
5:0	RO	0x00	reserved

RKVDEC_SWREG141_RCB_FBCR_OFFSET

Address: Operational Base(0xFF740100) + offset (0x0234)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	sw_rcb_fbcr_base Rcb fbc row base address, unit: 64byts align
5:0	RO	0x00	reserved

RKVDEC_SWREG142_RCB_FILTC_COL_OFFSET

Address: Operational Base(0xFF740100) + offset (0x0238)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	sw_rcb_filtc_base Rcb filter col base address, unit: 64byts align
5:0	RO	0x00	reserved

RKVDEC_SWREG143_RCB_BASE

Address: Operational Base(0xFF740100) + offset (0x023C)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	sw_rcb_base Rcb base address, unit: 64byts align
5:0	RO	0x00	reserved

RKVDEC_SWREG160_VP9_DELTA_PROB_BASE

Address: Operational Base(0xFF740100) + offset (0x0280)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_vp9_delta_prob_base The base address of prob
3:0	RO	0x0	reserved

RKVDEC_SWREG161_PPS_BASE

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Address: Operational Base(0xFF740100) + offset (0x0284)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_pps_base The base address of pps (the address should 128bit align) It is for storing sps(sequence parameter set) and pps(picture parameter set).
3:0	RO	0x0	reserved

RKVDEC_SWREG161_AVS2_HEAD_BASE

Address: Operational Base(0xFF740100) + offset (0x0284)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_avs2_head_base The base address of avs2 head (the address should 128bit align) It will include sequence and picture level syntax.
3:0	RO	0x0	reserved

RKVDEC_SWREG162_VP9_LAST_PROB_BASE

Address: Operational Base(0xFF740100) + offset (0x0288)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_vp9_last_porb_base The base address of last prob (the address should 128bit align)
3:0	RO	0x0	reserved

RKVDEC_SWREG163_RPS_BASE

Address: Operational Base(0xFF740100) + offset (0x028C)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_rps_base Rps(reference picture set) base address (the address should 128bit align)
3:0	RO	0x0	reserved

RKVDEC_SWREG164_REF0_BASE

Address: Operational Base(0xFF740100) + offset (0x0290)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer0_base Base address for reference picture index0 (the address should be 128bit align) Fbc mode: H264 & hevc & avs2 ref0 head base.
3:0	RO	0x0	reserved

RKVDEC_SWREG164_VP9_REFERLAST_BASE

Address: Operational Base(0xFF740100) + offset (0x0290)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_vp9_last_base Base address for last (the address should be 128bit align) Fbc mode: Vp9 last ref frame head base.
3:0	RO	0x0	reserved

RKVDEC_SWREG165_REF1_BASE

Address: Operational Base(0xFF740100) + offset (0x0294)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer1_base Base address for reference picture index1 (the address should be 128bit align) Fbc mode: H264 & hevc & avs2 ref1 head base.

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Bit	Attr	Reset Value	Description
3:0	RO	0x0	reserved

RKVDEC_SWREG165_VP9_REFERGOLDEN_BASE

Address: Operational Base(0xFF740100) + offset (0x0294)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_vp9golden_base Base address for golden (the address should be 128bit align) Fbc mode: Vp9 golden ref frame head base.
3:0	RO	0x0	reserved

RKVDEC_SWREG166_REF2_BASE

Address: Operational Base(0xFF740100) + offset (0x0298)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer2_base Base address for reference picture index2 (the address should be 128bit align) Fbc mode: H264 & hevc & avs2 ref2 head base.
3:0	RO	0x0	reserved

RKVDEC_SWREG166_VP9_REFERALFTER_BASE

Address: Operational Base(0xFF740100) + offset (0x0298)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_vp9alfter_base Base address for alfter (the address should be 128bit align) Fbc mode: Vp9 after ref frame head base.
3:0	RO	0x0	reserved

RKVDEC_SWREG167_VP9COUNT_BASE

Address: Operational Base(0xFF740100) + offset (0x029C)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	sw_vp9_count_prob_base Software parse prob: Used as vp9 count write base
2:0	RO	0x0	reserved

RKVDEC_SWREG167_REF3_BASE

Address: Operational Base(0xFF740100) + offset (0x029C)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer3_base Base address for reference picture index3 (the address should be 128bit align) Fbc mode: H264 & hevc & avs2 ref3 head base.
3:0	RO	0x0	reserved

RKVDEC_SWREG168_VP9_SEGIDLAST_BASE

Address: Operational Base(0xFF740100) + offset (0x02A0)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_vp9segidlast_base Base address for vp9 last frame segment id (the address should be 128bit align)
3:0	RO	0x0	reserved

RKVDEC_SWREG168_REF4_BASE

Address: Operational Base(0xFF740100) + offset (0x02A0)

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Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer4_base Base address for reference picture index4 (the address should be 128bit align) Fbc mode: H264 & hevc & avs2 ref4 head base.
3:0	RO	0x0	reserved

RKVDEC_SWREG169_AVP9_SEGIDCUR_BASE

Address: Operational Base(0xFF740100) + offset (0x02A4)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_vp9segidcur_base Base address for vp9 cur frame segment id (the address should be 128bit align)
3:0	RO	0x0	reserved

RKVDEC_SWREG169_REF5_BASE

Address: Operational Base(0xFF740100) + offset (0x02A4)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer5_base Base address for reference picture index5 (the address should be 128bit align) Fbc mode: H264 & hevc & avs2 ref5 head base.
3:0	RO	0x0	reserved

RKVDEC_SWREG170_VP9_REFCOLMV_BASE

Address: Operational Base(0xFF740100) + offset (0x02A8)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_vp9_refcolmv_base Vp9 refcolmv base addr
3:0	RO	0x0	reserved

RKVDEC_SWREG170_REF6_BASE

Address: Operational Base(0xFF740100) + offset (0x02A8)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer6_base Base address for reference picture index6 (the address should be 128bit align) Fbc mode: H264 & hevc & avs2 ref6 head base.
3:0	RO	0x0	reserved

RKVDEC_SWREG171_VP9_INTERCMD_BASE

Address: Operational Base(0xFF740100) + offset (0x02AC)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_vp9_intercmd_base Vp9 inter command base addr, when sw_rlc_mode is 1'b1 When sw_dec_mode is VP9 and sw_rlc_mode is 1'b1, when read this register, after a frame is decoded ready or error (stream error, time out, bus error), it is the end address of the intercmd.
3:0	RO	0x0	reserved

RKVDEC_SWREG171_REF7_BASE

Address: Operational Base(0xFF740100) + offset (0x02AC)

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Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer7_base Base address for reference picture index7 (the address should be 128bit align) Fbc mode: H264 & hevc & avs2 ref7 head base.
3:0	RO	0x0	reserved

RKVDEC_SWREG172_VP9_UPDATE_PROB_WR_BASE

Address: Operational Base(0xFF740100) + offset (0x02B0)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_vp9_update_prob_wr_base Hardware parse prob: Used as vp9 prob write base
3:0	RO	0x0	reserved

RKVDEC_SWREG172_H26X_REF8_BASE

Address: Operational Base(0xFF740100) + offset (0x02B0)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer8_base Base address for reference picture index8 (the address should be 128bit align) Fbc mode: H264 & hevc & avs2 ref8 head base.
3:0	RO	0x0	reserved

RKVDEC_SWREG173_H26X_REF9_BASE

Address: Operational Base(0xFF740100) + offset (0x02B4)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer9_base Base address for reference picture index9 (the address should be 128bit align) Fbc mode: H264 & hevc & avs2 ref9 head base.
3:0	RO	0x0	reserved

RKVDEC_SWREG174_H26X_REF10_BASE

Address: Operational Base(0xFF740100) + offset (0x02B8)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer10_base Base address for reference picture index10 (the address should be 128bit align) Fbc mode: H264 & hevc & avs2 ref10 head base.
3:0	RO	0x0	reserved

RKVDEC_SWREG175_H26X_REF11_BASE

Address: Operational Base(0xFF740100) + offset (0x02BC)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer11_base Base address for reference picture index11 (the address should be 128bit align) Fbc mode: H264 & hevc & avs2 ref11 head base.
3:0	RO	0x0	reserved

RKVDEC_SWREG176_H26X_REF12_BASE

Address: Operational Base(0xFF740100) + offset (0x02C0)

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Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer12_base Base address for reference picture index12 (the address should be 128bit align) Fbc mode: H264 & hevc & avs2 ref12 head base.
3:0	RO	0x0	reserved

RKVDEC_SWREG177_H26X_REF13_BASE

Address: Operational Base(0xFF740100) + offset (0x02C4)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer13_base Base address for reference picture index13 (the address should be 128bit align) Fbc mode: H264 & hevc & avs2 ref13 head base.
3:0	RO	0x0	reserved

RKVDEC_SWREG178_H26X_REF14_BASE

Address: Operational Base(0xFF740100) + offset (0x02C8)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer14_base Base address for reference picture index14 (the address should be 128bit align) Fbc mode: H264 & hevc & avs2 ref14 head base.
3:0	RO	0x0	reserved

RKVDEC_SWREG179_H26X_REF15_BASE

Address: Operational Base(0xFF740100) + offset (0x02CC)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer15_base Base address for reference picture index15 (the address should be 128bit align) Fbc mode: H264 & hevc & avs2 ref15 head base.
3:0	RO	0x0	reserved

RKVDEC_SWREG180_SCANLIST_ADDR

Address: Operational Base(0xFF740100) + offset (0x02D0)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_scanlist_addr Should be align to 16byte, and will be used for h264 and hevc.
3:0	RO	0x0	reserved

RKVDEC_SWREG181_COLMV_REF0_BASE

Address: Operational Base(0xFF740100) + offset (0x02D4)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_colmv_ref0_base Only valid when sw_colmv_mode is 1'b1. Ref0 frame colmv base addr. For H264 and HEVC.
3:0	RO	0x0	reserved

RKVDEC_SWREG182_COLMV_REF1_BASE

Address: Operational Base(0xFF740100) + offset (0x02D8)

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Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_colmv_ref1_base Only valid when sw_colmv_mode is 1'b1. Ref1 frame colmv base addr. For H264 and HEVC.
3:0	RO	0x0	reserved

RKVDEC_SWREG183_COLMV_REF2_BASE

Address: Operational Base(0xFF740100) + offset (0x02DC)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_colmv_ref2_base Only valid when sw_colmv_mode is 1'b1. Ref2 frame colmv base addr. For H264 and HEVC.
3:0	RO	0x0	reserved

RKVDEC_SWREG184_COLMV_REF3_BASE

Address: Operational Base(0xFF740100) + offset (0x02E0)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_colmv_ref3_base Only valid when sw_colmv_mode is 1'b1. Ref3 frame colmv base addr. For H264 and HEVC.
3:0	RO	0x0	reserved

RKVDEC_SWREG185_COLMV_REF4_BASE

Address: Operational Base(0xFF740100) + offset (0x02E4)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_colmv_ref4_base Only valid when sw_colmv_mode is 1'b1. Ref4 frame colmv base addr. For H264 and HEVC.
3:0	RO	0x0	reserved

RKVDEC_SWREG186_COLMV_REF5_BASE

Address: Operational Base(0xFF740100) + offset (0x02E8)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_colmv_ref5_base Only valid when sw_colmv_mode is 1'b1. Ref5 frame colmv base addr. For H264 and HEVC.
3:0	RO	0x0	reserved

RKVDEC_SWREG187_COLMV_REF6_BASE

Address: Operational Base(0xFF740100) + offset (0x02EC)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_colmv_ref6_base Only valid when sw_colmv_mode is 1'b1. Ref6 frame colmv base addr. For H264 and HEVC.
3:0	RO	0x0	reserved

RKVDEC_SWREG188_COLMV_REF7_BASE

Address: Operational Base(0xFF740100) + offset (0x02F0)

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Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_colmv_ref7_base Only valid when sw_colmv_mode is 1'b1. Ref7 frame colmv base addr. For H264 and HEVC.
3:0	RO	0x0	reserved

RKVDEC_SWREG189_COLMV_REF8_BASE

Address: Operational Base(0xFF740100) + offset (0x02F4)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_colmv_ref8_base Only valid when sw_colmv_mode is 1'b1. Ref8 frame colmv base addr. For H264 and HEVC.
3:0	RO	0x0	reserved

RKVDEC_SWREG190_COLMV_REF9_BASE

Address: Operational Base(0xFF740100) + offset (0x02F8)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_colmv_ref9_base Only valid when sw_colmv_mode is 1'b1. Ref9 frame colmv base addr. For H264 and HEVC.
3:0	RO	0x0	reserved

RKVDEC_SWREG191_COLMV_REF10_BASE

Address: Operational Base(0xFF740100) + offset (0x02FC)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_colmv_ref10_base Only valid when sw_colmv_mode is 1'b1. Ref10 frame colmv base addr. For H264 and HEVC.
3:0	RO	0x0	reserved

RKVDEC_SWREG192_COLMV_REF11_BASE

Address: Operational Base(0xFF740100) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_colmv_ref11_base Only valid when sw_colmv_mode is 1'b1. Ref11 frame colmv base addr. For H264 and HEVC.
3:0	RO	0x0	reserved

RKVDEC_SWREG193_COLMV_REF12_BASE

Address: Operational Base(0xFF740100) + offset (0x0304)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_colmv_ref12_base Only valid when sw_colmv_mode is 1'b1. Ref12 frame colmv base addr. For H264 and HEVC.
3:0	RO	0x0	reserved

RKVDEC_SWREG194_COLMV_REF13_BASE

Address: Operational Base(0xFF740100) + offset (0x0308)

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Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_colmv_ref13_base Only valid when sw_colmv_mode is 1'b1. Ref13 frame colmv base addr. For H264 and HEVC.
3:0	RO	0x0	reserved

RKVDEC_SWREG195_COLMV_REF14_BASE

Address: Operational Base(0xFF740100) + offset (0x030C)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_colmv_ref14_base Only valid when sw_colmv_mode is 1'b1. Ref14 frame colmv base addr. For H264 and HEVC.
3:0	RO	0x0	reserved

RKVDEC_SWREG196_COLMV_REF15_BASE

Address: Operational Base(0xFF740100) + offset (0x0310)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_colmv_ref15_base Only valid when sw_colmv_mode is 1'b1. Ref15 frame colmv base addr. For H264 and HEVC.
3:0	RO	0x0	reserved

RKVDEC_SWREG197_CABACTBL_BASE

Address: Operational Base(0xFF740100) + offset (0x0314)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_cabactbl_base Hevc & H264: The base address of cabac table.
3:0	RO	0x0	reserved

RKVDEC_SWREG198_SCALE_DOWN_LUMA_BASE

Address: Operational Base(0xFF740100) + offset (0x0318)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_scale_down_luma_base The base address of luma base
3:0	RO	0x0	reserved

RKVDEC_SWREG199_SCALE_DOWN_CHRO_BASE

Address: Operational Base(0xFF740100) + offset (0x031C)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_scale_down_chro_base The base address of scale down chro base
3:0	RO	0x0	reserved

RKVDEC_SWREG200_REF_POC_HIGHBIT_P0

Address: Operational Base(0xFF740100) + offset (0x0320)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	sw_ref7_poc_highbit Sw_ref7_poc_highbit
27:24	RW	0x0	sw_ref6_poc_highbit Sw_ref6_poc_highbit
23:20	RW	0x0	sw_ref5_poc_highbit Sw_ref5_poc_highbit

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Bit	Attr	Reset Value	Description
19:16	RW	0x0	sw_ref4_poc_highbit Sw_ref4_poc_highbit
15:12	RW	0x0	sw_ref3_poc_highbit Sw_ref3_poc_highbit
11:8	RW	0x0	sw_ref2_poc_highbit Sw_ref2_poc_highbit
7:4	RW	0x0	sw_ref1_poc_highbit Sw_ref1_poc_highbit
3:0	RW	0x0	sw_ref0_poc_highbit Sw_ref0_poc_highbit

RKVDEC_SWREG201_REF_POC_HIGHBIT_P1

Address: Operational Base(0xFF740100) + offset (0x0324)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	sw_ref15_poc_highbit Sw_ref15_poc_highbit
27:24	RW	0x0	sw_ref14_poc_highbit Sw_ref14_poc_highbit
23:20	RW	0x0	sw_ref13_poc_highbit Sw_ref13_poc_highbit
19:16	RW	0x0	sw_ref12_poc_highbit Sw_ref12_poc_highbit
15:12	RW	0x0	sw_ref11_poc_highbit Sw_ref11_poc_highbit
11:8	RW	0x0	sw_ref10_poc_highbit Sw_ref10_poc_highbit
7:4	RW	0x0	sw_ref9_poc_highbit Sw_ref9_poc_highbit
3:0	RW	0x0	sw_ref8_poc_highbit Sw_ref8_poc_highbit

RKVDEC_SWREG202_REF_POC_HIGHBIT_P2

Address: Operational Base(0xFF740100) + offset (0x0328)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	sw_ref23_poc_highbit Sw_ref23_poc_highbit
27:24	RW	0x0	sw_ref22_poc_highbit Sw_ref22_poc_highbit
23:20	RW	0x0	sw_ref21_poc_highbit Sw_ref21_poc_highbit
19:16	RW	0x0	sw_ref20_poc_highbit Sw_ref20_poc_highbit
15:12	RW	0x0	sw_ref19_poc_highbit Sw_ref19_poc_highbit
11:8	RW	0x0	sw_ref18_poc_highbit Sw_ref18_poc_highbit
7:4	RW	0x0	sw_ref17_poc_highbit Sw_ref17_poc_highbit
3:0	RW	0x0	sw_ref16_poc_highbit Sw_ref16_poc_highbit

RKVDEC_SWREG203_REF_POC_HIGHBIT_P3

Address: Operational Base(0xFF740100) + offset (0x032C)

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Bit	Attr	Reset Value	Description
31:28	RW	0x0	sw_ref31_poc_highbit Sw_ref31_poc_highbit
27:24	RW	0x0	sw_ref30_poc_highbit Sw_ref30_poc_highbit
23:20	RW	0x0	sw_ref29_poc_highbit Sw_ref29_poc_highbit
19:16	RW	0x0	sw_ref28_poc_highbit Sw_ref28_poc_highbit
15:12	RW	0x0	sw_ref27_poc_highbit Sw_ref27_poc_highbit
11:8	RW	0x0	sw_ref26_poc_highbit Sw_ref26_poc_highbit
7:4	RW	0x0	sw_ref25_poc_highbit Sw_ref25_poc_highbit
3:0	RW	0x0	sw_ref24_poc_highbit Sw_ref24_poc_highbit

RKVDEC_SWREG204_CUR_POC_HIGHBIT

Address: Operational Base(0xFF740100) + offset (0x0330)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	sw_cur_poc_highbit Sw_cur_poc_highbit

RKVDEC_SWREG205_DEBUG_INFO

Address: Operational Base(0xFF740100) + offset (0x0334)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	sw_pps_slice_gate_dis Dec_ctrl pps or slice generate clk gate before frame start 1'b0: Enable 1'b1: Disable
14	RW	0x0	sw_mmu_sel 1'b0: Use mmu0/1 1'b1: Use rkmmu with new version
13	RW	0x0	sw_mmu_force_busidle_req Default 0, force bus idle require not enable When 1, force bus idle require enable, and decoder do not work.
12	RW	0x0	sw_force_busidle_req Default 0, force bus idle require not enable When 1, force bus idle require enable, and decoder do not work.
11	RW	0x0	sw_dec_timeout_mode 1'b0: Normal timeout counter 1'b1: Force timeout counter at decoder working
10	RW	0x0	sw_reg_cfg_wr_dis Link table write out disable 1'b0: Enable 1'b1: Disable
9	RW	0x0	sw_dec_timeout_dis If enabled HW may return timeout interrupt in case HW gets stucked while decoding picture. 1'b0: Enable 1'b1: Disable

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Bit	Attr	Reset Value	Description
8	RW	0x0	sw_fetchcmd_merge_dis Fetch command merge disable 1'b0: Fetch cmd merge enable 1'b1: Fetch cmd merge disable
7	RW	0x0	sw_coord_realtime_report_mode Coord realtime report select 1'b0: Coord report at realtime postion 1'b1: Coord report at picture right position
6	RO	0x0	reserved
5	RW	0x0	sw_right_auto_rst_disable Decoder each frame end with auto reset select, but mmu do not auto reset Default is auto reset 1'b0: Decoder each frame end with auto reset enable 1'b1: Decoder each frame end with auto reset disable
4	RW	0x0	sw_error_auto_rst_disable Default is auto reset 1'b0: Hardware will auto reset when error occur. 1'b1: Wait software process reset when error occur.
3:2	RO	0x0	reserved
1	RW	0x0	sw_force_mmureset_valid When sw_force_mmureset_valid is 1'b1, mmu reset will always be valid to the system no matter that whether the axi bus is idle. When sw_force_mmureset_valid is 1'b0, mmu reset will only be valid when the axi bus is idle. We suggest such bit always be config to 0 except when soft want to force reset.
0	RW	0x0	sw_force_softreset_valid When sw_force_softreset_valid is 1'b1, sw_softrst_en will always be valid to the system no matter that whether the axi bus is idle. When sw_force_softreset_valid is 1'b0, sw_softrst_en will only be valid when the axi bus is idle. We suggest such bit always be config to 0 except when soft want to force reset.

RKVDEC_SWREG224_STA_INT

Address: Operational Base(0xFF740100) + offset (0x0380)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	sw_ltb_end_sta Ltb mode end sta
13	RW	0x0	sw_mmureset_rdy When it is 1'b1, it says that mmu reset has been done.
12	RW	0x0	sw_ltb_pause_sta Ltb mode pause sta
11	RW	0x0	sw_dec_line_irq_raw The raw status of sw_dec_line_irq, sw should reset this bit after interrupt is handled.
10	RW	0x0	sw_dec_line_irq When high, decoder requests an line interrrupt. Sw_dec_line_irq = sw_dec_line_irq_raw && (sw_dec_line_irq_dis == 1'b0).
9	RW	0x0	sw_softreset_rdy When it is 1'b1, it says that softreset has been done.

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Bit	Attr	Reset Value	Description
8	RW	0x0	sw_cabu_end_sta Hevc: Cabac decode end status. H264 & vp9 : Streamd decode status.
7	RW	0x0	sw_colmv_ref_error_sta Hevc & vp9: When it is 1'b1, it means that inter module read the invalid dpb frame. It will self reset the hardware. H264: When it is 1'b1, it means that inter module read the invalid dpb frame. When sw_h264_error_mode is 1'b0, it will self reset the hardware, otherwise it will not.
6	RW	0x0	sw_buf_empty_sta Buffer empty status, only when sw_buf_empty_en is 1'b1 , this bit is valid, now is for no valid.
5	RW	0x0	sw_dec_timeout_sta When high the decoder has been idling for too long. It will self reset the hardware only when sw_dec_timeout_e is 1'b1, this bit is valid.
4	RW	0x0	sw_dec_error_sta Hevc & vp9: When high, an error is found in input data stream decoding. It will self reset the hardware. H264: When high, an error is found in input data stream decoding. When sw_h264_error_mode is 1'b0, it will self reset the hardware, otherwise it will not.
3	RW	0x0	sw_dec_bus_sta When this bit is high, there is error on the axi bus, it will self reset hardware.
2	RW	0x0	sw_dec_rdy_sta When this bit is high, decoder has decoded a picture(the loop filter module send out a frame rdy).
1	RW	0x0	sw_dec_irq_raw The raw status of sw_dec_irq, sw should reset this bit after interrupt is handled.
0	RW	0x0	sw_dec_irq When high, decoder requests an interrrupt. Sw_dec_irq = sw_dec_irq_raw && (sw_dec_irq_dis == 1'b0).

RKVDEC_SWREG225_SLICE_BYTE_OFFSET_STA

Address: Operational Base(0xFF740100) + offset (0x0384)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_strmd_slice_byte_offset_sta Strmd slice byte offset

RKVDEC_SWREG226_STA_CABAC_ERROR_STATUS

Address: Operational Base(0xFF740100) + offset (0x0388)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_cabac_error_status In HEVC & H264, it is called cabac error status.

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Bit	Attr	Reset Value	Description
3:1	RW	0x0	sw_strmd_dec_error_sta Streamd dec error sta 3'b000: Normal end 3'b001: Error creat end 3'b010: Ofifo_overflow_error 3'b011: Error quit end,not error creat 3'b100: Stream_len_error 3'b101: Strmd_frame_all_error_end_sta 3'b110~3'b111: Reserved
0	RW	0x0	sw_dec_frame_error_sta 1'b1: All frame ctu error.

RKVDEC_SWREG227_STA_COLMV_ERROR_REF_PICIDX

Address: Operational Base(0xFF740100) + offset (0x038C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	sw_colmv_ref_picidx When sw_colmv_ref_error_sta is 1'b1, these bits are used for tell which dpb frame is invalid but is read by inter module. It is for H264 and HEVC.

RKVDEC_SWREG228_STA_CABAC_ERROR_CTU_OFFSET

Address: Operational Base(0xFF740100) + offset (0x0390)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_cabac_error_ctu_offset_y For all HEVC and H264 and VP9. For vp9, it is the value of {stsw_vp9_error_ctu0_y,stsw_vp9_error_ctu0_x}.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_cabac_error_ctu_offset_x For all HEVC and H264 and VP9. For vp9, it is the value of {stsw_vp9_error_ctu0_y,stsw_vp9_error_ctu0_x}.

RKVDEC_SWREG229_STA_AXI_WCH_FINISH_FLAG

Address: Operational Base(0xFF740100) + offset (0x0394)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RW	0x00000	sw_axi_wch_finish_flag Axi write channel finish flag

RKVDEC_SWREG230_STA_SLICE_DEC_NUM

Address: Operational Base(0xFF740100) + offset (0x0398)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:0	RO	0x0000000	sw_slicedec_num H264 decoded num, the max slice num for H264 is 4096.

RKVDEC_SWREG231_STA_FRAME_ERROR_CTU_NUM

Address: Operational Base(0xFF740100) + offset (0x039C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	sw_frame_ctu_error_num H264 and hevc error ctu number

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RKVDEC_SWREG232_STA_ERROR_PACKET_NUM

Address: Operational Base(0xFF740100) + offset (0x03A0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	sw_error_packet_num Error packet number

RKVDEC_SWREG233_STA_ERR_CTU_NUM_IN_ROI

Address: Operational Base(0xFF740100) + offset (0x03A4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RO	0x000000	sw_error_ctu_num_in_roi The error ctu num in roi

RKVDEC_SWREG234_BUF_EMPTY_OFFSET

Address: Operational Base(0xFF740100) + offset (0x03A8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	coord_report_offset_y Coord_report offset y
15:0	RW	0x0000	coord_report_offset_x Coord_report offset x

RKVDEC_SWREG235_COORD_REPORT_OUTBUF_HEIGHT

Address: Operational Base(0xFF740100) + offset (0x03AC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_coord_report_outbuf_height Minus pixel height

RKVDEC_SWREG256_DEBUG_PERF_LATENCY_CTRL0

Address: Operational Base(0xFF740100) + offset (0x0400)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rd_latency_thr Rd channel latency threshold
15:12	RO	0x0	reserved
11:4	RW	0x00	sw_rd_latency_id Rd channel id for performance test
3	RW	0x0	sw_axi_cnt_type 1'b0: Axi transfer num count 1'b1: Ddr align transfer num count
2	RO	0x0	reserved
1	RW	0x0	sw_axi_perf_clr 1'b0: Software clear disable 1'b1: Software clear enable Clear pulse
0	RW	0x0	sw_axi_perf_work_e 1'b0: Disable 1'b1: Enable

RKVDEC_SWREG257_DEBUG_PERF_LATENCY_CTRL1

Address: Operational Base(0xFF740100) + offset (0x0404)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
24	RW	0x0	sw_rd_band_width_mode 1'b0: Cal all id 1'b1: Cal sw_ar_count_id
23:16	RW	0x00	sw_aw_count_id Sw_aw_count_id
15:12	RO	0x0	reserved
11:4	RW	0x00	sw_ar_count_id Sw_ar_count_id
3	RW	0x0	sw_aw_cnt_id_type 1'b0: Count all wr-channels 1'b1: Count sw_wr_cont_id wr-channel only
2	RW	0x0	sw_ar_cnt_id_type 1'b0: Count all rd-channels. 1'b1: Count sw_ar_cont_id rd-channel only.
1:0	RW	0x0	sw_addr_align_type 2'b00: 16 byte align 2'b01: 32byte align 2'b10: 64byte align 2'b11: 128byte align

RKVDEC_SWREG258_DEBUG_PERF_RD_MAX_LATENCY_NUM

Address: Operational Base(0xFF740100) + offset (0x0408)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	sw_rd_max_latency_num Read max latency number

RKVDEC_SWREG259_PERF_RD_LATENCY_SAMP_NUM

Address: Operational Base(0xFF740100) + offset (0x040C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	sw_perf_rd_latency_samp_num The number of bigger than configed threshold value

RKVDEC_SWREG260_DEBUG_PERF_RD_LATENCY_ACC_SUM

Address: Operational Base(0xFF740100) + offset (0x0410)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	sw_rd_latency_acc_sum Total sample number

RKVDEC_SWREG261_DEBUG_PERF_RD_AXI_TOTAL_BYTE

Address: Operational Base(0xFF740100) + offset (0x0414)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	sw_perf_rd_axi_total_byte The bandwidth of total read bytes

RKVDEC_SWREG262_DEBUG_PERF_WR_AXI_TOTAL_BYTE

Address: Operational Base(0xFF740100) + offset (0x0418)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	sw_perf_wr_axi_total_byte The bandwidth of total write bytes

RKVDEC_SWREG263_DEBUG_PERF_WORKING_CNT

Address: Operational Base(0xFF740100) + offset (0x041C)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	sw_perf_working_cnt The total running cycle of current frame

RKVDEC_SWREG264_DEBUG_BUS_STATE

Address: Operational Base(0xFF740100) + offset (0x0420)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:0	RW	0x0000000	bus_state_flag bus status

RKVDEC_SWREG265_DEBUG_PERF_SEL

Address: Operational Base(0xFF740100) + offset (0x0424)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x00	sw_perf_cnt2_sel 6'h0: Don't work. 6'h1: Cycles counter for cabac in buffer empty. 6'h2: Cycles counter for cabac in buffer full;(may be alwasys will be 0). 6'h3: Cycles counter for cabac out buffer empty. 6'h4: Cycles counter for cabac out buffer full. 6'h5: Cycles counter for transd input data ready. 6'h6: Cycles counter for transd write data to recon allow. 6'h7: Cycles counter for dec2transd cmd empty. 6'h8: Cycles counter for dec2transd cmd full. 6'h9: Cycles counter for transd2dblk bs fifo empty. 6'ha: Cycles counter for transd2dblk bs fifo full. 6'hb: Cycles counter for dec2intra cmd fifo empty. 6'hc: Cycles counter for dec2intra cmd fifo full. 6'hd: Cycles counter for mc2recon cmd fifo empty. 6'he: Cycles counter for mc2recon cmd fifo full. 6'hf: Cycles counter for mc2recon data fifo empty. 6'h10: Cycles counter for mc2recon data fifo full. 6'h11: Cycles counter for recon2filter data write allow. 6'h12: Cycles counter for inter2busifd cmd fifo empty. 6'h13: Cycles counter for inter2busifd cmd fifo full. 6'h14: Cycles counter for busifd2mc data fifo empty. 6'h15: Cycles counter for busifd2mc data fifo full. 6'h16: Cycles counter for bus un-working status(idle status). 6'h17: Cycles counter for dec2inter cmd fifo empty. 6'h18: Cycles counter for dec2inter cmd fifo full. 6'h19: Cycles counter for inter2mc cmd fifo empty. 6'h1a: Cycles counter for inter2mc cmd fifo full. 6'h1b: Cycles counter for inter2dblk bs fifo empty. 6'h1c: Cycles counter for inter2dblk bs fifo full. 6'h1d: Cycles counter for colmv_rbuf_empty. 6'h1e: Cycles counter for colmv_rbuf_full. 6'h1f: Cycles counter for colmv_wbuf_empty. 6'h20: Cycles counter for colmv_wbuf_da_full. 6'h21: Cycles counter for dblk work status. 6'h22: Cycles counter for dblk work status. 6'h23: Cycles counter for dec2loopfilter cmd fifo empty. 6'h24: Cycles counter for dec2loopfilter cmd fifo full. 6'h25: Cycles counter for sao input data valid. 6'h26: Cycles counter for busifd hold back sao write data.

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Bit	Attr	Reset Value	Description
			6'h27: Cycles counter for bus process writing output buffer data. 6'h28: Counter for dec_ctrl read cmd num. 6'h29: Error ctu num when stream error happen. 6'h2a: Inter reflist idx which be used flag. 6'h2b: Pu num, 4*4 unit. 6'h2c: {mv_y_min[15:0], mv_x_min[15:0]}. 6'h2d: {mv_y_max[15:0], mv_x_max[15:0]}. 6'h2e: The sum value of mv_x lowbits,sum_mv_x[31:0]. 6'h2f: The sum value of mv_y lotbits, sum_mv_y[31:0]. 6'h30: The sum value of |mv_x| lowbits, sum_abs_mv_x[31:0]. 6'h31: The sum value of |mv_y| lowbits, sum_abs_mv_x[31:0]. 6'h32: The sum value of mv high bits, {sum_abs_mv_y[40:32], sum_abs_mv_x[40:32], sum_mv_y[40:32], sum_mv_x[40:32]}. 6'h33: The cu skip num, unit is 8*8. 6'h34: The tu skip num, unit is 4*4. 6'h35: The max qp of tu, {8'h0, cr_qp_max[7:0], cb_qp_max[7:0], luma_qp_max[7:0]}. 6'h36: The min qp of tu, {8'h0, cr_qp_min[7:0], cb_qp_min[7:0], luma_qp_min[7:0]}. 6'h37: The sum of luma qp, unit is 4*4. 6'h38: The sum of cb qp, unit is 4*4. 6'h39: The sum of cr qp, unit is 4*4. 6'h3a: The count of mv_x. 6'h3b: The count of mv_y. 6'h3c: The payload len,unit 16bytes
15:14	RO	0x0	reserved
13:8	RW	0x00	sw_perf_cnt1_sel 6'h0: Don't work. 6'h1: Cycles counter for cabac in buffer empty. 6'h2: Cycles counter for cabac in buffer full;(may be alwasys will be 0). 6'h3: Cycles counter for cabac out buffer empty. 6'h4: Cycles counter for cabac out buffer full. 6'h5: Cycles counter for transd input data ready. 6'h6: Cycles counter for transd write data to recon allow. 6'h7: Cycles counter for dec2transd cmd empty. 6'h8: Cycles counter for dec2transd cmd full. 6'h9: Cycles counter for transd2dblk bs fifo empty. 6'ha: Cycles counter for transd2dblk bs fifo full. 6'hb: Cycles counter for dec2intra cmd fifo empty. 6'hc: Cycles counter for dec2intra cmd fifo full. 6'hd: Cycles counter for mc2recon cmd fifo empty. 6'he: Cycles counter for mc2recon cmd fifo full. 6'hf: Cycles counter for mc2recon data fifo empty. 6'h10: Cycles counter for mc2recon data fifo full. 6'h11: Cycles counter for recon2filter data write allow. 6'h12: Cycles counter for inter2busifd cmd fifo empty. 6'h13: Cycles counter for inter2busifd cmd fifo full. 6'h14: Cycles counter for busifd2mc data fifo empty. 6'h15: Cycles counter for busifd2mc data fifo full. 6'h16: Cycles counter for bus un-working status(idle status). 6'h17: Cycles counter for dec2inter cmd fifo empty. 6'h18: Cycles counter for dec2inter cmd fifo full. 6'h19: Cycles counter for inter2mc cmd fifo empty. 6'h1a: Cycles counter for inter2mc cmd fifo full. 6'h1b: Cycles counter for inter2dblk bs fifo empty.

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Bit	Attr	Reset Value	Description
			6'h1c: Cycles counter for inter2dblk bs fifo full. 6'h1d: Cycles counter for colmv_rbuf_empty. 6'h1e: Cycles counter for colmv_rbuf_full. 6'h1f: Cycles counter for colmv_wbuf_empty. 6'h20: Cycles counter for colmv_wbuf_da_full. 6'h21: Cycles counter for dblk work status. 6'h22: Cycles counter for dblk work status. 6'h23: Cycles counter for dec2loopfilter cmd fifo empty. 6'h24: Cycles counter for dec2loopfilter cmd fifo full. 6'h25: Cycles counter for sao input data valid. 6'h26: Cycles counter for busifd hold back sao write data. 6'h27: Cycles counter for bus process writing output buffer data. 6'h28: Counter for dec_ctrl read cmd num. 6'h29: Error ctu num when stream error happen. 6'h2a: Inter reflist idx which be used flag. 6'h2b: Pu num, 4*4 unit. 6'h2c: {mv_y_min[15:0], mv_x_min[15:0]}. 6'h2d: {mv_y_max[15:0], mv_x_max[15:0]}. 6'h2e: The sum value of mv_x lowbits,sum_mv_x[31:0]. 6'h2f: The sum value of mv_y lotbits, sum_mv_y[31:0]. 6'h30: The sum value of |mv_x| lowbits, sum_abs_mv_x[31:0]. 6'h31: The sum value of |mv_y| lowbits, sum_abs_mv_x[31:0]. 6'h32: The sum value of mv high bits, {sum_abs_mv_y[40:32], sum_abs_mv_x[40:32], sum_mv_y[40:32], sum_mv_x[40:32]}. 6'h33: The cu skip num, unit is 8*8. 6'h34: The tu skip num, unit is 4*4. 6'h35: The max qp of tu, {8'h0, cr_qp_max[7:0], cb_qp_max[7:0], luma_qp_max[7:0]}. 6'h36: The min qp of tu, {8'h0, cr_qp_min[7:0], cb_qp_min[7:0], luma_qp_min[7:0]}. 6'h37: The sum of luma qp, unit is 4*4. 6'h38: The sum of cb qp, unit is 4*4. 6'h39: The sum of cr qp, unit is 4*4. 6'h3a: The count of mv_x. 6'h3b: The count of mv_y. 6'h3c: The payload len,unit 16bytes
7:6	RO	0x0	reserved
5:0	RW	0x00	sw_perf_cnt0_sel 6'h0: Don't work. 6'h1: Cycles counter for cabac in buffer empty. 6'h2: Cycles counter for cabac in buffer full;(may be alwasys will be 0). 6'h3: Cycles counter for cabac out buffer empty. 6'h4: Cycles counter for cabac out buffer full. 6'h5: Cycles counter for transd input data ready. 6'h6: Cycles counter for transd write data to recon allow. 6'h7: Cycles counter for dec2transd cmd empty. 6'h8: Cycles counter for dec2transd cmd full. 6'h9: Cycles counter for transd2dblk bs fifo empty. 6'ha: Cycles counter for transd2dblk bs fifo full. 6'hb: Cycles counter for dec2intra cmd fifo empty. 6'hc: Cycles counter for dec2intra cmd fifo full. 6'hd: Cycles counter for mc2recon cmd fifo empty. 6'he: Cycles counter for mc2recon cmd fifo full. 6'hf: Cycles counter for mc2recon data fifo empty. 6'h10: Cycles counter for mc2recon data fifo full.

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Bit	Attr	Reset Value	Description
			6'h11: Cycles counter for recon2filter data write allow. 6'h12: Cycles counter for inter2busifd cmd fifo empty. 6'h13: Cycles counter for inter2busifd cmd fifo full. 6'h14: Cycles counter for busifd2mc data fifo empty. 6'h15: Cycles counter for busifd2mc data fifo full. 6'h16: Cycles counter for bus un-working status(idle status). 6'h17: Cycles counter for dec2inter cmd fifo empty. 6'h18: Cycles counter for dec2inter cmd fifo full. 6'h19: Cycles counter for inter2mc cmd fifo empty. 6'h1a: Cycles counter for inter2mc cmd fifo full. 6'h1b: Cycles counter for inter2dblk bs fifo empty. 6'h1c: Cycles counter for inter2dblk bs fifo full. 6'h1d: Cycles counter for colmv_rbuf_empty. 6'h1e: Cycles counter for colmv_rbuf_full. 6'h1f: Cycles counter for colmv_wbuf_empty. 6'h20: Cycles counter for colmv_wbuf_da_full. 6'h21: Cycles counter for dblk work status. 6'h22: Cycles counter for dblk work status. 6'h23: Cycles counter for dec2loopfilter cmd fifo empty. 6'h24: Cycles counter for dec2loopfilter cmd fifo full. 6'h25: Cycles counter for sao input data valid. 6'h26: Cycles counter for busifd hold back sao write data. 6'h27: Cycles counter for bus process writing output buffer data. 6'h28: Counter for dec_ctrl read cmd num. 6'h29: Error ctu num when stream error happen. 6'h2a: Inter reflist idx which be used flag. 6'h2b: Pu num, 4*4 unit. 6'h2c: {mv_y_min[15:0], mv_x_min[15:0]}. 6'h2d: {mv_y_max[15:0], mv_x_max[15:0]}. 6'h2e: The sum value of mv_x lowbits,sum_mv_x[31:0]. 6'h2f: The sum value of mv_y lotbits, sum_mv_y[31:0]. 6'h30: The sum value of |mv_x| lowbits, sum_abs_mv_x[31:0]. 6'h31: The sum value of |mv_y| lowbits, sum_abs_mv_x[31:0]. 6'h32: The sum value of mv high bits, {sum_abs_mv_y[40:32], sum_abs_mv_x[40:32], sum_mv_y[40:32], sum_mv_x[40:32]}. 6'h33: The cu skip num, unit is 8*8. 6'h34: The tu skip num, unit is 4*4. 6'h35: The max qp of tu, {8'h0, cr_qp_max[7:0], cb_qp_max[7:0], luma_qp_max[7:0]}. 6'h36: The min qp of tu, {8'h0, cr_qp_min[7:0], cb_qp_min[7:0], luma_qp_min[7:0]}. 6'h37: The sum of luma qp, unit is 4*4. 6'h38: The sum of cb qp, unit is 4*4. 6'h39: The sum of cr qp, unit is 4*4. 6'h3a: The count of mv_x. 6'h3b: The count of mv_y. 6'h3c: The payload len,unit 16bytes

RKVDEC_SWREG266_DEBUG_PERF_CNT0

Address: Operational Base(0xFF740100) + offset (0x0428)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	sw_perf_cnt0 Performance count value0

RKVDEC_SWREG267_DEBUG_PERF_CNT1

Address: Operational Base(0xFF740100) + offset (0x042C)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	sw_perf_cnt1 Performance count value1

RKVDEC_SWREG268_DEBUG_PERF_CNT2

Address: Operational Base(0xFF740100) + offset (0x0430)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	sw_perf_cnt2 Performance count value2

RKVDEC_SWREG269_VP9_ERROR_INFO

Address: Operational Base(0xFF740100) + offset (0x0434)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_vp9_error_ctu1_en If the error ctu offset be valid.
30:26	RO	0x00	reserved
25:16	RW	0x000	sw_vp9_error_ctu1_y The error ctu offset y
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_vp9_error_ctu1_x The error ctu offset x

RKVDEC_SWREG270_DEBUG_QOS_CTRL

Address: Operational Base(0xFF740100) + offset (0x0438)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RW	0x0	sw_axi_rd_qos wr qos level from 0~7
27	RO	0x0	reserved
26:24	RW	0x0	sw_axi_rd_hurry_level 2'b00: Hurry off 2'b01~2'b11: Hurry level
23	RO	0x0	reserved
22:20	RW	0x0	sw_axi_wr_qos wr qos level from 0~7
19	RO	0x0	reserved
18:16	RW	0x0	sw_axi_wr_hurry_level 2'b00: Hurry off 2'b01~2'b11: Hurry level
15:8	RO	0x00	reserved
7:0	RW	0x00	sw_bus2mc_buf_qos_level Range is: 0~255. The value is means that sw_bus2mc_buffer_qos_level <= left space, it will give hurry.

RKVDEC_SWREG271_DEBUG_WAIT_CYCLE_QOS

Address: Operational Base(0xFF740100) + offset (0x043C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_wr_hurry_wait_cycle Hw find sw_wr_wait_cycle_qos cycle can't wr to ddr,it will give hurry.

RKVDEC_SWREG272_DEBUG_INT

Address: Operational Base(0xFF740100) + offset (0x0440)

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	mmu_wr_transer_cnt Axi integrity process wr transer count
23	RO	0x0	reserved
22:16	RO	0x00	sw_streamfifo_space2full It is for debug use, to tell the stream fifo space to full. For HEVC , H264 and VP9.
15:14	RO	0x0	reserved
13:6	RO	0x00	wr_tansfer_cnt Axi integrity process wr transer count
5	RW	0x0	mmu_busidle_flag 1'b0: Bus busy 1'b1: Bus idle
4:1	RO	0x0	reserved
0	RO	0x0	busidle_flag 1'b0: Bus busy 1'b1: Bus idle

RKVDEC_SWREG273_STA_B_FRAME_FLAG

Address: Operational Base(0xFF740100) + offset (0x0444)

Bit	Attr	Reset Value	Description
31	RO	0x0	sw_pps_no_ref_bframe_dec_r 1'b1: Find this frame is not referace B frame.
30:25	RO	0x00	reserved
24:0	RO	0x0000000	sw_bus_status_flag Debug info

RKVDEC_SWREG274_PIX_RANGE_Y

Address: Operational Base(0xFF740100) + offset (0x0448)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	sw_y_max_value The max value of luma
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_y_min_value The min value of luma

RKVDEC_SWREG275_PIX_RANGE_U

Address: Operational Base(0xFF740100) + offset (0x044C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RO	0x000	sw_u_max_value The max value of chroma u
15:10	RO	0x00	reserved
9:0	RO	0x000	sw_u_min_value The min value of chroma u

RKVDEC_SWREG276_PIX_RANGE_V

Address: Operational Base(0xFF740100) + offset (0x0450)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_v_max_value The max value of chroma v
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RO	0x000	sw_v_min_value The min value of chroma v

RKVDEC_SWREG277_ERROR_SPREAD_NUM

Address: Operational Base(0xFF740100) + offset (0x0454)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	sw_err_spread_cnt_sum Current frame error counters at ctu unit, active when sw_error_spread_e is 1.

RKVDEC_SWREG278_DEC_LINE_OFFSET_Y

Address: Operational Base(0xFF740100) + offset (0x0458)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_dec_line_offset_y Decoder line offset y state from lpf report

10.5.4 VDPU382 CACHE Registers Summary

Name	Offset	Size	Reset Value	Description
PREF_CACHE_VERSION	0x0000	W	0xCAC20101	VERSION register
PREF_CACHE_SIZE	0x0004	W	0x07100206	L2 cache SIZE
PREF_CACHE_STATUS	0x0008	W	0x00000000	Status register
PREF_CACHE_COMMAND	0x0010	W	0x00000000	Command setting register
PREF_CACHE_CLEAR_PAGE	0x0014	W	0x00000000	Clear page register
PREF_CACHE_MAX_READS	0x0018	W	0x0000001C	Maximum read register
PREF_CACHE_ENABLE	0x001C	W	0x00000003	Enables cacheable accesses and cache read allocation
PREF_CACHE_PERFCNT_SRC0	0x0020	W	0x00000000	Performance counter 0 source register
PREF_CACHE_PERFCNT_VAL0	0x0024	W	0x00000000	Performance counter 0 value register
PREF_CACHE_PERFCNT_SRC1	0x0028	W	0x00000000	This register holds all the possible source values for Performance Counter 00: total clock cycles1: active clock cycles2: read transactions, master3: word reads, master4: read transactions, slave5: word reads, slave6: read hit, slave7: read misses, slave8: read invalidates, slave9: cacheable read transactions, slave10: bad hit nmber, slave
PREF_CACHE_PERFCNT_VAL1	0x002C	W	0x00000000	Performance counter 1 value register

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

10.5.5 VDPU382 CACHE Detail Registers Description

PREF_CACHE_VERSION

Address: Operational Base(0xFF740600) + offset (0x0000)

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Bit	Attr	Reset Value	Description
31:16	RO	0xcac2	product_id The id of product
15:8	RO	0x01	version_major Major verision
7:0	RO	0x01	version_minor Minor verision

PREF_CACHE_SIZE

Address: Operational Base(0xFF740600) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:24	RO	0x07	external_bus_width Log2 external bus width in bits
23:16	RO	0x10	cache_size Log2 cache size in bytes For Y channel , its value is 0x10. For UV channel, its value is 0xf.
15:8	RO	0x02	associativity Log2 associativity
7:0	RO	0x06	line_size Log2 line size in bytes

PREF_CACHE_STATUS

Address: Operational Base(0xFF740600) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	data_busy Set when the cache is busy handling data
0	RW	0x0	cmd_busy Set when the cache is busy handling commands

PREF_CACHE_COMMAND

Address: Operational Base(0xFF740600) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:4	RW	0x0	sw_addrb_sel 2'b00: To sel b[14:6] 2'b01: To sel b[15:9], b[7:6] 2'b10: To sel b[16:10], b[7:6] 2'b11: To sel b[17:11], b[7:6]
3:0	RW	0x0	command The possible command is 1 = Clear entire cache

PREF_CACHE_CLEAR_PAGE

Address: Operational Base(0xFF740600) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	clear_page Writing an address, invlidates all lines in that page from the cache

PREF_CACHE_MAX_READS

Address: Operational Base(0xFF740600) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
4:0	RW	0x1c	max_reads Limit the number of outstanding read transactions to this amount

PREF_CACHE_ENABLE

Address: Operational Base(0xFF740600) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	sw_cache_linsize 1'b0: The cache line is 32bytes 1'b1: The cache line is 64bytes
3	RW	0x0	sw_cache_clk_disgate Cache clk disgate When it is 1'b0, enable cache clk auto clkgating When it is 1'b1, disable cache clk auto clkgating
2	RW	0x0	sw_readbuffer_counter_reject_en Default is 1'b0, for enhance cacheable read performnace in readbuffer. 1'b1: normal origin counter reject
1	RW	0x1	permit_cache_read_allocate 1'b1: Permit cache read allocate
0	RW	0x1	permit_cacheable_access 1'b1: Permit cacheable access

PREF_CACHE_PERFCNT_SRC0

Address: Operational Base(0xFF740600) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x00	perfcnt_src0 This register holds all the possible source values for Performance Counter 0 0: disabled 1: total clock cycles 2: active clock cycles 3: read transactions, master 4: word reads, master 5: read transactions, slave 6: word reads, slave 7: read hit, slave 8: read misses, slave 9: read invalidates, slave 10: cacheable read transactions, slave 11: bad hit nmber, slave

PREF_CACHE_PERFCNT_VAL0

Address: Operational Base(0xFF740600) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perfcnt_val0 Performance counter 0 value

PREF_CACHE_PERFCNT_SRC1

Address: Operational Base(0xFF740600) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
6:0	RW	0x00	perfcnt_src1 This register holds all the possible source values for Performance Counter 1 0: disabled 1: total clock cycles 2: active clock cycles 3: read transactions, master 4: word reads, master 5: read transactions, slave 6: word reads, slave 7: read hit, slave 8: read misses, slave 9: read invalidates, slave 10: cacheable read transactions, slave 11: bad hit nmber, slave

PREF_CACHE_PERFCNT_VAL1

Address: Operational Base(0xFF740600) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perfcnt_val1 Performance counter 1 value

10.5.6 VDPU382 MMU Registers Summary

Name	Offset	Size	Reset Value	Description
RKVDEC_MMU_DTE_ADDR	0x0000	W	0x00000000	MMU current page Table addressIt is only can be written when MMU state is disable or page fault or mmu enable stall state
RKVDEC_MMU_STATUS	0x0004	W	0x00000018	MMU status register
RKVDEC_MMU_COMMAND	0x0008	W	0x00000000	MMU command register
RKVDEC_MMU_PAGE_FAULT_ADDR	0x000C	W	0x00000000	MMU logical address of last page fault
RKVDEC_MMU_ZAP_ONE_LINE	0x0010	W	0x00000000	MMU Zap cache line register
RKVDEC_MMU_INT_RAWSTAT	0x0014	W	0x00000000	MMU raw interrupt status register
RKVDEC_MMU_INT_CLEAR	0x0018	W	0x00000000	MMU raw interrupt status register
RKVDEC_MMU_INT_MASK	0x001C	W	0x00000000	MMU raw interrupt status register
RKVDEC_MMU_INT_STATUS	0x0020	W	0x00000000	MMU raw interrupt status register
RKVDEC_MMU_AUTO_GATING	0x0024	W	0x00000001	MMU auto gating

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

10.5.7 VDPU382 MMU Detail Registers Description

RKVDEC_MMU_DTE_ADDR

Address: Operational Base(0xFF740800) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MMU_DTE_ADDR MMU dte base addr , the address must be 4kb aligned.

RKVDEC_MMU_STATUS

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Address: Operational Base(0xFF740800) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:6	RO	0x00	PAGE_FAULT_BUS_ID Index of master reponsible for last page fault
5	RO	0x0	PAGE_FAULT_IS_WRITE The direction of access for last page fault: 1'b0: Read 1'b1: Write
4	RO	0x1	REPLAY_BUFFER_EMPTY The MMU replay buffer is empty
3	RO	0x1	MMU_IDLE The MMU is idle when accesses are being translated and there are no unfinished translated accesses.
2	RO	0x0	STAIL_ACTIVE MMU stall mode currently enabled. The mode is enabled by command
1	RO	0x0	PAGE_FAULT_ACTIVE MMU page fault mode currently enabled . The mode is enabled by command.
0	RO	0x0	PAGING_ENABLED Paging is enabled

RKVDEC_MMU_COMMAND

Address: Operational Base(0xFF740800) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	WO	0x0	MMU_CMD MMU_CMD. This can be: 3'b000: MMU_ENABLE_PAGING 3'b001: MMU_DISABLE_PAGING 3'b010: MMU_ENABLE_STALL 3'b011: MMU_DISABLE_STALL 3'b100: MMU_ZAP_CACHE 3'b101: MMU_PAGE_FAULT_DONE 3'b110: MMU_FORCE_RESET Others: Reserved

RKVDEC_MMU_PAGE_FAULT_ADDR

Address: Operational Base(0xFF740800) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	PAGE_FAULT_ADDR Address of last page fault

RKVDEC_MMU_ZAP_ONE_LINE

Address: Operational Base(0xFF740800) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	MMU_ZAP_ONE_LINE Address to be invalidated from the page table cache

RKVDEC_MMU_INT_RAWSTAT

Address: Operational Base(0xFF740800) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	READ_BUS_ERROR Read bus error

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Bit	Attr	Reset Value	Description
0	RW	0x0	PAGE_FAULT Page fault

RKVDEC_MMU_INT_CLEAR

Address: Operational Base(0xFF740800) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	WO	0x0	READ_BUS_ERROR Read bus error
0	WO	0x0	PAGE_FAULT Page fault

RKVDEC_MMU_INT_MASK

Address: Operational Base(0xFF740800) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	READ_BUS_ERROR Read bus error, enable an interrupt source if the corresponding mask bit is set to 1
0	RW	0x0	PAGE_FAULT Page fault, enable an interrupt source if the corresponding mask bit is set to 1

RKVDEC_MMU_INT_STATUS

Address: Operational Base(0xFF740800) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	READ_BUS_ERROR Read bus error
0	RO	0x0	PAGE_FAULT Page fault

RKVDEC_MMU_AUTO_GATING

Address: Operational Base(0xFF740800) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x1	MMU_AUTO_GATING When it is 1'b1, the MMU will auto gating itself.

10.5.8 VDPU382 LLP Registers Summary

Name	Offset	Size	Reset Value	Description
RKVDEC_LLP_SWREG0_LINK_MODE_IRQ	0x0000	W	0x00000000	The interrupt of LLP mode
RKVDEC_LLP_SWREG1_CFG_START_ADDR	0x0004	W	0x00000000	the address of register data
RKVDEC_LLP_SWREG2_LINK_MODE	0x0008	W	0x00000000	The LLP table add ctrl
RKVDEC_LLP_SWREG3_CONFIG_DONE	0x000C	W	0x00000000	Config finish ctrl register

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Name	Offset	Size	Reset Value	Description
RKVDEC_LLP_SWREG4_DECODERED_NUM	0x0010	W	0x00000000	The frame number which have been decodered(decoder_num + skip_num) <= dec_total_numhardware will be idle when the adder equal with dec_total_num.
RKVDEC_LLP_SWREG5_DEC_TOTAL_NUM	0x0014	W	0x00000000	The total needed decoder number
RKVDEC_LLP_SWREG6_LINK_MODE_EN	0x0018	W	0x00000000	LLP enable flag
RKVDEC_LLP_SWREG7_NXT_DEC_LTB_BASE	0x001C	W	0x00000000	Next address of register data
RKVDEC_LLP_SWREG9_LINK_STA	0x0024	W	0x00000000	The interrupt of LLP mode line irq ctrl

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

10.5.9 VDPU382 LLP Detail Register Description

RKVDEC_LLP_SWREG0_LINK_MODE_IRQ

Address: Operational Base(0xFF740000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RW	0x0	sw_ltb_pause_flag Link mode pause flag active Hardware will pause work at current frame dec done.
20	RW	0x0	sw_rcb_buffer_base_fixed 1'b0: Rcb buffer base can be config by ltb table. 1'b1: Rcb buffer will not be changed when ltb table be read,so it need to be config by normal reigster in first.
19:18	RO	0x0	reserved
17	RW	0x0	sw_ccu_core_work_mode 1'b0: Dec core will be used separate 1'b1: Dec core will ctrl by ccu
16	RW	0x0	sw_core_work_mode 1'b0: Ccu auto ctrl and decision mode 1'b1: Cpu ctrl ccu decision mode
15:10	RO	0x00	reserved
9	RW	0x0	rkvdec_irq_raw The irq of decodered
8	RW	0x0	link_table_irq When high, decoder requests an interrrupt. link table irq = sw_dec_irq_raw && (sw_dec_irq_dis == 1'b0)
7:3	RO	0x00	reserved
2	RW	0x0	sw_error_irq_dis 1'b0: If there are any error, not matter sw_dec_irq_dis, it will give an interrept. 1'b1: If it will give interrept, it only according to sw_dec_irq_dis.
1:0	RO	0x0	reserved

RKVDEC_LLP_SWREG1_CFG_START_ADDR

Address: Operational Base(0xFF740000) + offset (0x0004)

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Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	reg_cfg_addr It should be align to 32 byte.
3:0	RO	0x0	reserved

RKVDEC_LLP_SWREG2_LINK_MODE

Address: Operational Base(0xFF740000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31	RW	0x0	link_mode 1'b0: Normal mode, the first to start link mode 1'b1: Add extra ready frame to decoder
30	RO	0x0	reserved
29:0	RW	0x00000000	pre_frame_num 1'b1: Config 1 frame

RKVDEC_LLP_SWREG3_CONFIG_DONE

Address: Operational Base(0xFF740000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1C	0x0	config_done After config okay, config this bit to 1

RKVDEC_LLP_SWREG4_DECODERED_NUM

Address: Operational Base(0xFF740000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	skip_num The frame number which have been skipped
19:0	RO	0x00000	decoder_num The frame number which have been decodered

RKVDEC_LLP_SWREG5_DEC_TOTAL_NUM

Address: Operational Base(0xFF740000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RO	0x00000000	dec_total_num The total needed decoder number

RKVDEC_LLP_SWREG6_LINK_MODE_EN

Address: Operational Base(0xFF740000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	link_mode_en When error see by hw, it will auto reset to 0.

RKVDEC_LLP_SWREG7_NXT_DEC_LTB_BASE

Address: Operational Base(0xFF740000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	nxt_dec_ltb_base Bytes unit

RKVDEC_LLP_SWREG9_LINK_STA

Address: Operational Base(0xFF740000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
8	RW	0x0	decoder_error_flag 1'b0: No error 1'b1: Error, you will need to see swreg1 to check error type.
7:6	RO	0x0	reserved
5	RW	0x0	sw_ltb_end_flag Link mode end flag sta Hardware will disable link_mode_en at current frame dec done.
4	RO	0x0	sw_ltb_skip_flag Link mode skip flag sta Hardware will skip current frame and load next frame link table.
3:2	RO	0x0	reserved
1	RW	0x0	sw_dec_line_irq_raw The line irq of decodered
0	RW	0x0	sw_dec_line_irq When high, decoder requests an interrrupt. link table line irq = sw_dec_line_irq_raw && (sw_dec_line_irq_dis == 1'b0)

10.5.10 VDPU720 Registers Summary

Name	Offset	Size	Reset Value	Description
RKDJPEG_SWREG0_ID	0x0000	W	0x00000000	ID register (read only)
RKDJPEG_SWREG1_INT	0x0004	W	0x00000000	Interrupt and decoder enable register
RKDJPEG_SWREG2_SYS	0x0008	W	0x00000000	Rk jpeg decoder system ctrl
RKDJPEG_SWREG3_PIC_SIZE	0x000C	W	0x00000000	Picture width and height size
RKDJPEG_SWREG4_PIC_FORMAT	0x0010	W	0x00000000	Jpeg picture format configurate
RKDJPEG_SWREG5_HOR_VIRSTRIDE	0x0014	W	0x00000000	Sw_y_hor_virstride and sw_uv_hor_virstride configurate
RKDJPEG_SWREG6_Y_VIRSTRIDE	0x0018	W	0x00000000	Sw_y_virstride configurate
RKDJPEG_SWREG7_TABLE_LEN	0x001C	W	0x00000000	Dequant table and huffman table length Description
RKDJPEG_SWREG8_STRM_LEN	0x0020	W	0x00000000	Rk jpeg stream length and start byte info Description
RKDJPEG_SWREG9_QTBL_BASE	0x0024	W	0x00000000	Dequant table DDR base address Description
RKDJPEG_SWREG10_HTBL_MINCODE_BASE	0x0028	W	0x00000000	Huffman mincode table DDR base address Description
RKDJPEG_SWREG11_HTBL_VALUE_BASE	0x002C	W	0x00000000	Huffman value table DDR base address Description
RKDJPEG_SWREG12_STRM_BASE	0x0030	W	0x00000000	Stream data DDR base address Description
RKDJPEG_SWREG13_DEC_OUT_BASE	0x0034	W	0x00000000	Rk jpeg recon decoder output data DDR address Description
RKDJPEG_SWREG14_STRM_ERROR	0x0038	W	0x00000000	Rk jpeg decoder stream error process
RKDJPEG_SWREG15_STRM_MASK	0x003C	W	0x00000000	Rk jpeg decoder special marker process
RKDJPEG_SWREG16_CLK_GATE	0x0040	W	0x00000000	Rk jpeg decoder clk gate enable

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Name	Offset	Size	Reset Value	Description
RKDJPEG_SWREG30_PERF_LATENCY_CTRL0	0x0078	W	0x00000000	Rk jpeg decoder axi performance ctrl0 Description
RKDJPEG_SWREG31_PERF_LATENCY_CTRL1	0x007C	W	0x00000000	Rk jpeg decoder axi performance ctrl1 Description
RKDJPEG_SWREG32_DBG_MCU_POS	0x0080	W	0x00000000	Rk jpeg debug register with mcu position Description
RKDJPEG_SWREG33_DBG_ERROR_INFO	0x0084	W	0x00000000	Rk jpeg debug register with error info Description
RKDJPEG_SWREG34_PERF_RD_MAX_LATENCY_NUM0	0x0088	W	0x00000000	Rd_max_latency_num Description
RKDJPEG_SWREG35_PERF_RD_LATENCY_SAMP_NUM	0x008C	W	0x00000000	Rd_latency_thr_num Description
RKDJPEG_SWREG36_PERF_RD_LATENCY_ACC_SUM	0x0090	W	0x00000000	Rd_latency_acc_sum Description
RKDJPEG_SWREG37_PERF_RD_AXI_TOTAL_BYTE	0x0094	W	0x00000000	Perf_rd_axi_total_byte Description
RKDJPEG_SWREG38_PERF_WR_AXI_TOTAL_BYTE	0x0098	W	0x00000000	Perf_wr_axi_total_byte Description
RKDJPEG_SWREG39_PERF_WORKING_CNT	0x009C	W	0x00000000	Perf_working_cnt Description
RKDJPEG_SWREG40_DBG_BUS_STA	0x00A0	W	0x00000000	Rk decoder bus status flag Description
RKDJPEG_SWREG41_DBG_WORK_STA	0x00A4	W	0x00000000	Rk decoder work status flag Description

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

10.5.11 VDPU720 Detail Registers Description

RKDJPEG_SWREG0_ID

Address: Operational Base(0xFF870000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	prod_num RKDJPEG verision
15:9	RO	0x00	reserved
8	RO	0x0	bit_depth Max bit_depth support 1'b0: 8bits 1'b1: 12bits
7:0	RO	0x00	minor_ver 1'b0: Default 1'b1: 8k

RKDJPEG_SWREG1_INT

Address: Operational Base(0xFF870000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	sw_care_strm_error_e Use for sw_error_prc_mode=1 1'b0: Not care stream error, when sw_care_strm_error_e=0, sw_dec_error_sta will not valid, mmu will not be reset at frame end, link table mode will continue without care stream error, only active error info registers. 1'b1: Care stream error

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Bit	Attr	Reset Value	Description
15	RW	0x0	sw_buf_empty_force_end_flag 1'b0: Invalid 1'b1: Valid Buffer empty interrupt with stream real empty, so should force hardware decoder current frame end.
14	RW	0x0	sw_softreset_rdy When it is 1'b1, it says that softreset has been done.
13	RW	0x0	sw_dec_buf_empty_sta Buffer empty status, only when sw_buf_empty_e is 1'b1, this bit is valid. Software should clean stream buffer empty state and set sw_buf_empty_reload_p enbale at the same time.
12	RW	0x0	sw_dec_timeout_sta When high the decoder has been idling for too long. it will self reset the hardware. Only when sw_dec_timeout_e is 1'b1, this bit is valid.
11	RW	0x0	sw_dec_error_sta When high, an error is found in input data stream decoding. When sw_error_prc_mode is 1'b0, it will self reset the hardware, otherwise it will not.
10	RW	0x0	sw_dec_bus_sta When this bit is high, there is error on the axi bus, it will self reset hardware.
9	RW	0x0	sw_dec_rdy_sta When this bit is high, decoder has decoded a picture (the output module send out a frame rdy).
8	RW	0x0	sw_dec_irq When high, decoder requests an interrrupt. sw_dec_irq = sw_dec_irq_raw && (sw_dec_irq_dis == 1'b0).
7	RW	0x0	sw_wait_reset_e The enable flag of wait software system to reset flag. 1'b0: Hardware will auto reset when error occur. 1'b1: Wait software process reset when error occur.
6	RW	0x0	sw_dec_irq_raw The raw status of sw_dec_irq, SW should reset this bit after interrupt is handled.
5	RW	0x0	sw_softrst_en_p Softreset enable signal, write 1 to soft reset, write 0 invalid, puls register.
4	RW	0x0	sw_buf_empty_reload_p Buffer empty stream reload enable signal. Write 1 to reload stream data ready pulse register with hardware auto clean valid at next cycle. Before reload enable, strm_len register should be reset and start_of_type is zero sw_strm_base addr may be reset also. Note: Sw_error_prc_mode should be set to 1 when sw_buf_empty_e valid otherwise the hardware would be reset and not support buffer buffer empty reload.
3	RW	0x0	sw_buf_empty_e Buffer empty interrupt enable.
2	RW	0x0	sw_dec_timeout_e If enabled HW may return timeout interrupt in case HW gets stucked while decoding picture.
1	RW	0x0	sw_dec_irq_dis When hight, there are no interrupts concerning decoder from HW. Polling must be used to see the interrupt status.

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Bit	Attr	Reset Value	Description
0	RW	0x0	sw_dec_e Decoder enable. Setting this bit high will start the decoding operation. HW will reset this when the picture is decoded ready or bus error or time out interrupt is given for all decode format.

RKDJPEG_SWREG2_SYS

Address: Operational Base(0xFF870000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_yuv2rgb_range Jpeg decoder yuv2rgb range 1'b0: Range0 limit (Y[16:235],UV[16:240],RGB[0:255]). 1'b1: Range1 full (YUV[0:255],RGB[0:255]).
30	RW	0x0	sw_yuv2rgb_rec Jpeg decoder yuv2rgb rec 1'b0: BT601 1'b1: BT709
29:27	RW	0x0	sw_yuv_out_format Jpeg decoder yuv output transmit format. 3'b000: Yuv out without transmit format. 3'b001: Yuv2rgb888. 3'b010: Yuv2rgb565. 3'b011: Yuv2yuv420sp(not support yuv400 transmit to yuv420sp). 3'b100: Yuv2yuyv(only support yuv422 or yuv444, yuv444 should uv scaledown).
26	RW	0x0	sw_dec_out_sequence Recon data out format when afbc off. 1'b0: Raster sequence out. 1'b1: Tile sequence out.
25	RW	0x0	sw_fill_right_e When JPEG picture width pixels is not a multiple of 16 pixels. 1'b0: Not fill picture width to multiple of 16 pixels. 1'b1: Fill picture width to multiple of 16 pixels. HW must fill one block of zero pixel data to the right border of the picture.
24	RW	0x0	sw_fill_down_e When JPEG picture height pixels is not a multiple of 16 pixels. 1'b0: Not fill picture height to multiple of 16 pixels. 1'b1: Fill picture height to multiple of 16 pixels. HW must fill one block row of zero pixel data for the last block row of picture.
23	RW	0x0	sw_bgr_sequence Jpeg decoder rgb sequence 1'b0: Rgb565/rgb888 1'b1: Bgr565/bgr888 Default is be mode
22	RW	0x0	sw_fbc_force_uncompress 1'b0: Allow fbce compress yuv block. 1'b1: Force all yuv block use uncompress mode. (No used)
21	RW	0x0	sw_allow_16x8_cp_flag 1'b0: Not allow 1'b1: Allow The configurate value is depend on vop work mode. (No used)

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Bit	Attr	Reset Value	Description
20	RW	0x0	sw_fbc_e 1'b0: Disable 1'b1: Fbc enable (No used)
19:18	RO	0x0	reserved
17	RW	0x0	sw_force_softreset_valid When sw_force_softreset_valid is 1'b1, sw_softrst_en will always be valid to the system no matter that whether the axi bus is idle. When sw_force_softreset_valid is 1'b0, sw_softrst_en will only be valid when the axi bus is idle.
16	RW	0x0	sw_timeout_mode Timeout mode select. 1'b0: TIMEOUT_CYCLES is {24{1'b1}}. 1'b1: TIMEOUT_CYCLES is {18{1'b1}}.
15	RW	0x0	sw_dec_timeout_mode 1'b0: Normal timeout counter clean by axi working. 1'b1: Force timeout counter at decoder working.
14	RO	0x0	reserved
13:12	RW	0x0	sw_scaledown_mode Jpeg decoder scaledown mode 2'b00: Not scaledown 2'b01: 1/2 scaledown 2'b10: 1/4 scaledown 2'b11: 1/8 scaledown
11	RO	0x0	reserved
10	RW	0x0	sw_out_byte_swap May be used for 16 bits sequence output info. 1'b0: No swapping of 8 bits data, 0x1234. 1'b1: 8 bits data are swapped, 0x3412.
9	RW	0x0	sw_out_cbcr_swap 1'b0: Cb(u) is in the lower address, cr(v) is in the higher address. 1'b1: Cb(u) is in the higher address, cr(v) is in the lower address. Sw_in_cbcr_swap is the same with sw_out_cbcr_swap. Jpeg decoder only support for yuv4xxsp.
8	RW	0x0	sw_out_swap64_e May be used for 128 bit environment. 1'b0: No swapping of 64 bit words. 1'b1: 64 bit data words are swapped.
7	RW	0x0	sw_out_swap32_e May be used for 64 or 128 bit environment. 1'b0: No swapping of 32 bit words. 1'b1: 32 bit data words are swapped.
6	RW	0x0	sw_out_endian 1'b0: Little endian 1'b1: Big endian For litter enadian, a data 0x12345678, 0x78 is stored in lower address, 0x12 is stored in higher address.
5	RW	0x0	sw_str_swap64_e May be used for 128 bit environment. 1'b0: No swapping of 64 bit words. 1'b1: 64 bit data words are swapped.
4	RW	0x0	sw_str_swap32_e May be used for 64 or 128 bit environment. 1'b0: No swapping of 32 bit words. 1'b1: 32 bit data words are swapped.

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Bit	Attr	Reset Value	Description
3	RW	0x0	sw_str_endian 1'b0: Little endian 1'b1: Big endian For litter enadian, a data 0x12345678, 0x78 is stored in lower address, 0x12 is stored in higher address.
2	RW	0x0	sw_in_swap64_e May be used for 128 bit environment. 1'b0: No swapping of 64 bit words. 1'b1: 64 bit data words are swapped.
1	RW	0x0	sw_in_swap32_e May be used for 64 or 128 bit environment. 1'b0: No swapping of 32 bit words. 1'b1: 32 bit data words are swapped.
0	RW	0x0	sw_in_endian 1'b0: Little endian 1'b1: Big endian For litter enadian, a data 0x12345678, 0x78 is stored in lower address, 0x12 is stored in higher address.

RKDJPEG_SWREG3_PIC_SIZE

Address: Operational Base(0xFF870000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_pic_height_m1 Picture height in pixels unit minus1(should be mcu align by hardware).
15:0	RW	0x0000	sw_pic_width_m1 Picture width in pixels unit minus1(should be mcu align by hardware).

RKDJPEG_SWREG4_PIC_FORMAT

Address: Operational Base(0xFF870000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_dri_mcu_num_m1 Restart marker frequency. Tells the amount of coding units between restart markers Specifies the number of MCU in the restart. The number is minus1.
15	RW	0x0	sw_dri_e Define restart interval marker enable 1'b0: Restart interval marker disable. 1'b1: Restart interval marker enable.
14	RO	0x0	reserved
13:12	RW	0x0	sw_htables_sel Amount of Huffman tables in external memory. 2'b00: No Huffman tables. 2'b01: One Huffman table. Used when picture is single type. 2'b10: Two Huffman tables. One for luminance and one for chominances. 2'b11: Three Huffman tables. Each type (Lu, Cb, Cr) has own Huffman table.
11:10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9:8	RW	0x0	sw_qtables_sel Amount of Quantization tables in external memory. 2'b00: No quantization tables. 2'b01: One quantization table, Used when picture is single type. 2'b10: Two quantization tables, One for luminance and one for chominances. 2'b11: Three quantization tables, Each type (Lu, Cr, Cb) has own QP-table.
7	RO	0x0	reserved
6:4	RW	0x0	sw_pixel_depth Picture luma pixel depth minus8. 3'b000: 8bits 3'b100: 12bits
3	RO	0x0	reserved
2:0	RW	0x0	sw_jpeg_mode Input picture sampling format 3'b000: Single type, MB 1 block (4:0:0) 3'b001: Single type, MB 6 blocks (4:1:1) 3'b010: Three types, MB 6 blocks (4:2:0) 3'b011: Three types, MB 4 blocks (4:2:2) 3'b100: Three types, MB 4 blocks (4:4:0) 3'b101: Three types, MB 3 blocks (4:4:4)

RKDJPEG_SWREG5_HOR_VIRSTRIDE

Address: Operational Base(0xFF870000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_uv_hor_virstride Picture horizontal virtual stride (the unit is 128bit). The max is 65536x2/16 = 0x2000. Suggest this register to configuration to even for advance DDR performance. Yuv444 tile mode, uv_hor_virstride will use 16bits.
15:0	RW	0x0000	sw_y_hor_virstride Picture horizontal virtual stride (the unit is 128bit) The max is 65536x2/16 = 0x2000. Suggest this register to configuration to even for advance DDR performance. Fbc mode: used for head virtual stride. But rgb888 tile mode, y_hor_virstride 16bits is not enought, will be use 17bits.

RKDJPEG_SWREG6_Y_VIRSTRIDE

Address: Operational Base(0xFF870000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_y_virstride Base address with 16 byte precision for decoder output luminance picture virtual stride.
3:0	RO	0x0	reserved

RKDJPEG_SWREG7_TABLE_LEN

Address: Operational Base(0xFF870000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	sw_y_hor_virstride_h Picture horizontal virtual stride (the unit is 128bit). High bit when rgb888 tile mode use, y_hor_virstride 16bits is not enought,will be use 17bits.
23:22	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
21:16	RW	0x00	sw_htbl_value_len Huffman value tables length(minus 1) with 16 byte align(128bits).
15:13	RO	0x0	reserved
12:8	RW	0x00	sw_htbl_mincode_len Huffman maxcode mincode and accaddr length(minus 1) with 16 byte align(128bits).
7:5	RO	0x0	reserved
4:0	RW	0x00	sw_qtbl_len Quant table length(minus 1) with 16 byte align(128bits).

RKDJPEG_SWREG8_STRM_LEN

Address: Operational Base(0xFF870000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_stream_len Amount of stream data 16 bytes(minus 1) in input buffer. If the given buffer size is not enough for finishing the picture the corresponding interrupt is given and new stream buffer base address and stream buffer size information should be given (assosiates with sw_strm_in_base).
3:0	RW	0x0	sw_strm_start_byte Input stream start byte offset 4'h0: 0 type, of the base addr(16bytes) offset. 4'h1: 1 type, of the base addr(16bytes) offset. 4'h2: 2 type, of the base addr(16bytes) offset. 4'h3: 3 type, of the base addr(16bytes) offset. 4'h4: 4 type, of the base addr(16bytes) offset. 4'h5: 5 type, of the base addr(16bytes) offset. 4'h6: 6 type, of the base addr(16bytes) offset. 4'h7: 7 type, of the base addr(16bytes) offset.

RKDJPEG_SWREG9_QTBL_BASE

Address: Operational Base(0xFF870000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	sw_qtbl_base Base address for standard dependent tables: AC,DC, QP tables64 byte align.
5:0	RO	0x00	reserved

RKDJPEG_SWREG10_HTBL_MINCODE_BASE

Address: Operational Base(0xFF870000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	sw_htbl_mincode_base Base address for standard dependent tables. Huffman mincode and accaddr tables64 byte align.
5:0	RO	0x00	reserved

RKDJPEG_SWREG11_HTBL_VALUE_BASE

Address: Operational Base(0xFF870000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	sw_htbl_value_base Base address for standard dependent tables. Huffman value tables64 byte align.
5:0	RO	0x00	reserved

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RKDJPEG_SWREG12_STRM_BASE

Address: Operational Base(0xFF870000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_strm_in_base Stream start address with 16 byte precision. Actually, start byte number in stream_start_byte.
3:0	RO	0x0	reserved

RKDJPEG_SWREG13_DEC_OUT_BASE

Address: Operational Base(0xFF870000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	sw_dec_out_base Base address with 64 byte precision for decoder output luminance picture.
5:0	RO	0x00	reserved

RKDJPEG_SWREG14_STRM_ERROR

Address: Operational Base(0xFF870000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:16	RW	0x00	sw_hfm_force_stop 1'b0: Huffman decoder error and continue. 1'b1: Huffman decoder error force stop the decoder and wait soft reset. [12]: AXI stream buffer empty, and without detect EOI marker stop or not(0:support fill coefficient). [11]:Huffman get EOI marker without frame end stop or not(0:support fill coefficient). [10]:Huffman coefficient overflow detect and stop or not(0:support decode next coefficient). [9]:Huffman decode DRI stream stop or not, when MCU counter is not zero with DRI marker detect(0:support fill coefficient). [8]:Huffman decode DRI stream stop or not, when MCU counter is zero without DRI marker detect(0:support skip dummy stream).
15:10	RO	0x00	reserved
9	RW	0x0	sw_strm_dri_seq_err_mode 1'b0: Stream dri sequence error do not report error pos. 1'b1: Stream dri sequence error should be report error pos(if it's first error). Note: Error state should be report at all case.
8:7	RW	0x0	sw_strm_other_mark_mode 2'b00: Stream detect other marker do skip process and not report error pos. 2'b01: Stream detect another marker stop the decoder and wait soft reset. 2'b10: Stream detect other marker do skip process. 2'b11: Stream detect other marker do with normal stream. Note: Error state should be report at all case.

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Bit	Attr	Reset Value	Description
6:5	RW	0x0	sw_strm_ffff_err_mode 2'b00: Stream detect ffff marker do skip first 0xff process and not report error pos. 2'b01: Stream detect another marker stop the decoder and wait soft reset. 2'b10: Stream detect ffff marker do skip first 0xff process. 2'b11: Stream detect ffff marker do with normal stream at first 0xff. Note: Error state should be report at all case.
4:3	RW	0x0	sw_strm_r1_err_mode Stream detect second select marker process mode configuration. 2'b00: Ignore second select marker. 2'b01: Force stop decoder when meet the second select marker. 2'b10: Do skip process when meet the second select marker. 2'b11: Do with normal stream when meet the second select marker.
2:1	RW	0x0	sw_strm_r0_err_mode Stream detect first select marker process mode configuration. 2'b00: Ignore first select marker. 2'b01: Force stop decoder when meet the first select marker. 2'b10: Do skip process when meet the first select marker. 2'b11: Do with normal stream when meet the first select marker.
0	RW	0x0	sw_error_prc_mode 1'b0: When there is any stream error, the hardware will stop the decoder and reset itself. 1'b1: When there is any stream error, the hardware will wait the end signal of recon and then reset request.

RKDJPEG_SWREG15_STRM_MASK

Address: Operational Base(0xFF870000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_strm_r1_mask Mark the mask info 1: Stream value[7-0] will mask and not care. 0: Stream value[7-0] shall match SW marker value.
23:16	RW	0x00	sw_strm_r1_marker 0xffxx marker low 8bits value.
15:8	RW	0x00	sw_strm_r0_mask Mark the mask info. 1: Stream value[7-0] will mask and not care. 0: Stream value[7-0] shall match SW marker value.
7:0	RW	0x00	sw_strm_r0_marker 0xffxx marker low 8bits value.

RKDJPEG_SWREG16_CLK_GATE

Address: Operational Base(0xFF870000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	sw_dec_sram_gate_e 1'b0: Clock gate is not enable. 1'b1: Clock gate is enable when busifd block is not working.
6	RW	0x0	sw_post_prs_gate_e 1'b0: Clock gate is not enable. 1'b1: Clock gate is enable when post process block is not working.

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Bit	Attr	Reset Value	Description
5	RW	0x0	sw_busifd_gate_e 1'b0: Clock gate is not enable. 1'b1: Clock gate is enable when busifd block is not working.
4	RW	0x0	sw_dec_idct_gate_e 1'b0: Clock gate is not enable. 1'b1: Clock gate is enable when IDCT block is not working.
3	RW	0x0	sw_dec_izq_gate_e 1'b0: Clock gate is not enable. 1'b1: Clock gate is enable when IZQ block is not working.
2	RW	0x0	sw_dec_huffman_gate_e 1'b0: Clock gate is not enable. 1'b1: Clock gate is enable when Huffman block is not working.
1	RW	0x0	sw_dec_strm_gate_e 1'b0: Clock gate is not enable. 1'b1: Clock gate is enable when stream block is not working.
0	RW	0x0	sw_dec_clk_gate_e Decoder dynamic clock gating enable: 1'b0: Clock is running for all structures. 1'b1: Clock is gated for decoder structures that are not used. Note: Clock gating value can be changed only when decoder is disabled.

RKDJPEG_SWREG30_PERF_LATENCY_CTRL0

Address: Operational Base(0xFF870000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:8	RW	0x000	sw_rd_latency_thr Rd channel latency threshold.
7:4	RW	0x0	sw_rd_latency_id Rd channel id for performance test.
3	RW	0x0	sw_axi_cnt_type Sw_axi_cnt_type 1'b0: Axi transfer num count. 1'b1: Ddr align transfer num count.
2	RW	0x0	sw_axi_perf_frm_type 1'b0: Clear by frame end. 1'b1: Clear by software configuration.
1	RW	0x0	sw_axi_perf_clr_e 1'b0: Software clear disable 1'b1: Software clear enalbe. Clear pulse
0	RW	0x0	sw_axi_perf_work_e 1'b0: Disable 1'b1: Enable

RKDJPEG_SWREG31_PERF_LATENCY_CTRL1

Address: Operational Base(0xFF870000) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	sw_rd_total_bytes_mode 1'b0: Cal all id 1'b1: Cal sw_ar_count_id
11:8	RW	0x0	sw_aw_count_id Sw_aw_count_id

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	sw_ar_count_id Sw_ar_count_id
3	RW	0x0	sw_aw_cnt_id_type Sw_aw_cnt_id_type 1'b0: Count all wr-channels. 1'b1: Count sw_wr_cont_id wr-channel only.
2	RW	0x0	sw_ar_cnt_id_type Sw_ar_cnt_id_type 1'b0: Count all rd-channels. 1'b1: Count sw_ar_cont_id rd-channel only.
1:0	RW	0x0	sw_addr_align_type Sw_addr_align_type 2'h0: 16 byte align 2'h1: 32byte align 2'h2: 64byte align 2'h3: 128byte align

RKDJPEG_SWREG32_DBG_MCU_POS

Address: Operational Base(0xFF870000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	mcu_pos_y Decoder mcu position at x coordinal with first error detect, only for read enable.
15:0	RO	0x0000	mcu_pos_x Decoder mcu position at y coordinal with first error detect, only for read enable.

RKDJPEG_SWREG33_DBG_ERROR_INFO

Address: Operational Base(0xFF870000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x0	jpeg_first_error_idx Jpeg decoder first error index 4'h0: Stream_dri_seq_err_sta 4'h1: Stream_r0_err_sta 4'h2: Stream_r1_err_sta 4'h3: Stream_ffff_err_sta 4'h4: Stream_other_mark_err_sta 4'h8: Huffman_mcu_cnt_l 4'h9: Huffman_mcu_cnt_m 4'ha: Huffman_eoi_without_end 4'hb: Huffman_end_without_eoi 4'hc: Huffman_overflow 4'hd: Huffman_buf_empty
15:14	RO	0x0	reserved
13	RW	0x0	huffman_buf_empty Decoder picture not complete, and not detect EOI with buffer empty. 1'b0: Buffer not empty. 1'b1: Buffer empty.
12	RW	0x0	huffman_overflow Decoder Huffman coefficient overflow.
11	RW	0x0	huffman_end_without_eoi Decoder Huffman frame end without get EOI marker.

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Bit	Attr	Reset Value	Description
10	RW	0x0	huffman_eoi_without_end Decoder Huffman get EOI marker without frame end.
9	RW	0x0	huffman_mcu_cnt_m Decoder dri stream mcu count more, mcu count 0 without restart mark.
8	RW	0x0	huffman_mcu_cnt_l Decoder dri stream mcu count low, restart mark is coming without mcu count 0.
7:5	RO	0x0	reserved
4	RW	0x0	stream_other_mark_err_sta Decoder stream other marker error detect flag, only for read enable. 1'b0: Other marker not detect 1'b1: Other marker detect
3	RW	0x0	stream_ffff_err_sta Decoder stream ffff error detect flag, only for read enable. 1'b0: Other marker not detect. 1'b1: Other marker detect.
2	RW	0x0	stream_r1_err_sta Decoder stream special marker1 error detect flag, only for read enable. 1'b0: Special marker1 not detect. 1'b1: Special marker1 detect.
1	RW	0x0	stream_r0_err_sta Decoder stream special marker0 error detect flag, only for read enable. 1'b0: Special marker0 not detect. 1'b1: Special marker0 detect.
0	RW	0x0	stream_dri_seq_err_sta 1'b0: Stream DRI at normal sequence. 1'b1: Stream error with DRI not at normal sequence.

RKDJPEG_SWREG34_PERF_RD_MAX_LATENCY_NUM0

Address: Operational Base(0xFF870000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	rd_max_latency_num_ch0 Rd_max_latency_num_ch0

RKDJPEG_SWREG35_PERF_RD_LATENCY_SAMP_NUM

Address: Operational Base(0xFF870000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rd_latency_thr_num_ch0 Rd_latency_thr_num_ch0

RKDJPEG_SWREG36_PERF_RD_LATENCY_ACC_SUM

Address: Operational Base(0xFF870000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rd_latency_acc_sum Rd_latency_acc_sum

RKDJPEG_SWREG37_PERF_RD_AXI_TOTAL_BYTE

Address: Operational Base(0xFF870000) + offset (0x0094)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_rd_axi_total_byte Perf_rd_axi_total_byte

RKDJPEG_SWREG38_PERF_WR_AXI_TOTAL_BYTE

Address: Operational Base(0xFF870000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_wr_axi_total_byte Perf_wr_axi_total_byte

RKDJPEG_SWREG39_PERF_WORKING_CNT

Address: Operational Base(0xFF870000) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_working_cnt Perf_working_cnt

RKDJPEG_SWREG40_DBG_BUS_STA

Address: Operational Base(0xFF870000) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RO	0x00000	bus_status_flag Bus_status_flag

RKDJPEG_SWREG41_DBG_WORK_STA

Address: Operational Base(0xFF870000) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	work_status_flag Work_status_flag

10.5.12 VDPU720 MMU Registers Summary

Name	Offset	Size	Reset Value	Description
RKVDEC_MMU_DTE_ADDR	0x0000	W	0x00000000	MMU current page Table address. It is only can be written when MMU state is disable or page fault or mmu enable stall state.
RKVDEC_MMU_STATUS	0x0004	W	0x00000018	MMU status register
RKVDEC_MMU_COMMAND	0x0008	W	0x00000000	MMU command register
RKVDEC_MMU_PAGE_FAULT_ADDR	0x000c	W	0x00000000	MMU logical address of last page fault
RKVDEC_MMU_ZAP_ONE_LINE	0x0010	W	0x00000000	MMU Zap cache line register
RKVDEC_MMU_INT_RAWSTAT	0x0014	W	0x00000000	MMU raw interrupt status register
RKVDEC_MMU_INT_CLEAR	0x0018	W	0x00000000	MMU raw interrupt status register
RKVDEC_MMU_INT_MASK	0x001c	W	0x00000000	MMU raw interrupt status register
RKVDEC_MMU_INT_STATUS	0x0020	W	0x00000000	MMU raw interrupt status register
RKVDEC_MMU_AUTO_GATING	0x0024	W	0x00000001	MMU auto gating

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

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10.5.13 VDPU720 MMU Detail Registers Description

RKVDEC_MMU_DTE_ADDR

Address: Operational Base(0xFF870480) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MMU_DTE_ADDR MMU dte base addr, the address must be 4kb aligned.

RKVDEC_MMU_STATUS

Address: Operational Base(0xFF870480) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:6	RO	0x00	PAGE_FAULT_BUS_ID Index of master reponsible for last page fault.
5	RO	0x0	PAGE_FAULT_IS_WRITE The direction of access for last page fault: 1'b0: Read 1'b1: Write
4	RO	0x1	REPLAY_BUFFER_EMPTY The MMU replay buffer is empty.
3	RO	0x1	MMU_IDLE The MMU is idle when accesses are being translated and there are no unfinished translated accesses.
2	RO	0x0	STAIL_ACTIVE MMU stall mode currently enabled. The mode is enabled by command.
1	RO	0x0	PAGE_FAULT_ACTIVE MMU page fault mode currently enabled . The mode is enabled by command.
0	RO	0x0	PAGING_ENABLED Paging is enabled

RKVDEC_MMU_COMMAND

Address: Operational Base(0xFF870480) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	WO	0x0	MMU_CMD MMU_CMD. This can be: 3'b000: MMU_ENABLE_PAGING 3'b001: MMU_DISABLE_PAGING 3'b010: MMU_ENABLE_STALL 3'b011: MMU_DISABLE_STALL 3'b100: MMU_ZAP_CACHE 3'b101: MMU_PAGE_FAULT_DONE 3'b110: MMU_FORCE_RESET 3'b111: Reserved

RKVDEC_MMU_PAGE_FAULT_ADDR

Address: Operational Base(0xFF870480) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	PAGE_FAULT_ADDR Address of last page fault

RKVDEC_MMU_ZAP_ONE_LINE

Address: Operational Base(0xFF870480) + offset (0x0010)

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Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	MMU_ZAP_ONE_LINE Address to be invalidated from the page table cache.

RKVDEC_MMU_INT_RAWSTAT

Address: Operational Base(0xFF870480) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	READ_BUS_ERROR Read bus error
0	RW	0x0	PAGE_FAULT Page fault

RKVDEC_MMU_INT_CLEAR

Address: Operational Base(0xFF870480) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	WO	0x0	READ_BUS_ERROR Read bus error
0	WO	0x0	PAGE_FAULT Page fault

RKVDEC_MMU_INT_MASK

Address: Operational Base(0xFF870480) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	READ_BUS_ERROR Read bus error Enable an interrupt source if the corresponding mask bit is set to 1.
0	RW	0x0	PAGE_FAULT Page fault Enable an interrupt source if the corresponding mask bit is set to 1.

RKVDEC_MMU_INT_STATUS

Address: Operational Base(0xFF870480) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	READ_BUS_ERROR Read bus error
0	RO	0x0	PAGE_FAULT Page fault

RKVDEC_MMU_AUTO_GATING

Address: Operational Base(0xFF870480) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x1	MMU_AUTO_GATING When it is 1'b1, the mmu will auto gating it self.

10.5.14 VDPU720 LLP Registers Summary

Name	Offset	Size	Reset Value	Description
RKDJPEG_LINK_SWREG0_LINK_MODE_IRQ	0x0000	W	0x00000000	LLP mode and irq info

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Name	Offset	Size	Reset Value	Description
RKDJPEG_LINK_SWREG1_CFG_START_ADDR	0x0004	W	0x00000000	the address of register data
RKDJPEG_LINK_SWREG2_LINK_MODE	0x0008	W	0x00000000	Link mode and pre frame num
RKDJPEG_LINK_SWREG3_CONFIG_DONE	0x000C	W	0x00000000	Config done
RKDJPEG_LINK_SWREG4_DECODERED_NUM	0x0010	W	0x00000000	Decoder num and error flag
RKDJPEG_LINK_SWREG5_DEC_TOTAL_NUM	0x0014	W	0x00000000	Decoder total num
RKDJPEG_LINK_SWREG6_LINK_MODE_EN	0x0018	W	0x00000000	Link mode enable and softrst enable

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

10.5.15 VDPU720 LLP Registers Description

RKDJPEG_LINK_SWREG0_LINK_MODE_IRQ

Address: Operational Base(0xFF870300) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10	RW	0x0	sw_link_softreset_rdy When it is 1'b1, it says that softreset has been done.
9	RW	0x0	rkvdec_irq_raw Rkvdec_irq_raw
8	RW	0x0	link_table_irq When high, decoder requests an interrrupt. Link table irq = sw_dec_irq_raw && (sw_dec_irq_dis == 1'b0).
7:3	RO	0x00	reserved
2	RW	0x0	sw_error_irq_dis 1'b0: If there are any error, not matter sw_dec_irq_dis, it will give an interrept. 1'b1: If it will give interrept, it only according to sw_dec_irq_dis.
1	RW	0x0	cache_cfg_mode_sel 1'b0: Use rtl default value to config cache, ip will auto clr cache when it begin to start dec a frame. 1'b1: Use config in ddr to config cache.
0	RO	0x0	reserved

RKDJPEG_LINK_SWREG1_CFG_START_ADDR

Address: Operational Base(0xFF870300) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	reg_cfg_addr It should be align to 32 byte.
3:0	RO	0x0	reserved

RKDJPEG_LINK_SWREG2_LINK_MODE

Address: Operational Base(0xFF870300) + offset (0x0008)

Bit	Attr	Reset Value	Description
31	RW	0x0	link_mode 1'b0: Normal mode, the first to start link mode. 1'b1: Add extra ready frame to decoder.
30	RO	0x0	reserved
29:0	RW	0x00000000	pre_frame_num 30'h1: Config 1 frame .....

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RKDJPEG_LINK_SWREG3_CONFIG_DONE

Address: Operational Base(0xFF870300) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1C	0x0	config_done After config okay, config this bit to 1.

RKDJPEG_LINK_SWREG4_DECODERED_NUM

Address: Operational Base(0xFF870300) + offset (0x0010)

Bit	Attr	Reset Value	Description
31	RW	0x0	decoder_error_flag 1'b0: No error 1'b1: Error, you will need to see swreg1 to check error type.
30	RO	0x0	reserved
29:0	RO	0x00000000	decoder_num Decoder_num

RKDJPEG_LINK_SWREG5_DEC_TOTAL_NUM

Address: Operational Base(0xFF870300) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RO	0x00000000	dec_total_num Dec_total_num

RKDJPEG_LINK_SWREG6_LINK_MODE_EN

Address: Operational Base(0xFF870300) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	sw_link_softrst_en_p Link mode software force hardware self reset enable signal. Write 1 to soft reset, write 0 invalid, puls register.
3:1	RO	0x0	reserved
0	RW	0x0	link_mode_en When error see by hw, it will auto reset to 0.

10.5.16 VEPU540 Registers Summary

Name	Offset	Size	Reset Value	Description
VEPU_VERSION	0x0000	W	0x5060030B	VEPU Version Register
VEPU_ENC_STRT	0x0010	W	0x00000000	VEPU Start Command
VEPU_ENC_CLR	0x0014	W	0x00000000	VEPU Clear Command
VEPU_VS_LDLY	0x0018	W	0x00000000	Video Source Low Delay
VEPU_INT_EN	0x0020	W	0x00000000	VEPU Interrupt Enable
VEPU_INT_MSK	0x0024	W	0x00000000	VEPU Interrupt Mask
VEPU_INT_CLR	0x0028	W	0x00000000	VEPU Interrupt Clear
VEPU_INT_STA	0x002C	W	0x00000000	VEPU Interrupt State
VEPU_DBUS_ENDN	0x0030	W	0x00000000	Data Bus Endian
VEPU_DBUS_CFG	0x0034	W	0x00000000	Data Bus Configuration
VEPU_ENC_WDG	0x0038	W	0x00000000	VEPU watch dog configure register
VEPU_QOS_CFG	0x003C	W	0x00000000	Data Bus Qos Configuration
VEPU_QOS_PERD	0x0040	W	0x00000000	Data Bus Qos Period
VEPU_QOS_THD_L	0x0044	W	0x00000000	Data Bus Qos for Low Priority
VEPU_QOS_THD_M	0x0048	W	0x00000000	Data Bus Qos for Middle Priority
VEPU_QOS_THD_H	0x004C	W	0x00000000	Data Bus Qos for High Priority

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Name	Offset	Size	Reset Value	Description
VEPU_FREQ_RDCT	0x0050	W	0x00000000	VEPU Frequency Reduction
VEPU_OPT_STRG	0x0054	W	0x0000000D	Encoder Operation Strategy
VEPU_RDO_CKG_H264	0x0058	W	0x00000000	H264 RDO clock-gating enable.
VEPU_CORE_ID	0x005C	W	0x00000000	VEPU Core ID
VEPU_DVBM_CFG	0x0060	W	0x00000000	DVBM Configuration
VEPU_LKT_BASE_ADDR	0x0070	W	0x00000000	Link Table Base Address.
VEPU_NODE_OCFG	0x0100	W	0x00000000	Link Table Node Operation Configuration
VEPU_NODE_SCT_PCFG	0x0104	W	0x00000000	Picture Configuration Node Section Configuration
VEPU_NODE_SCT_RC	0x0108	W	0x00000000	Rate Control Node Section Configuration
VEPU_NODE_SCT_PAR	0x010C	W	0x00000000	Parameter Node Section Configuration
VEPU_NODE_SCT_SQI	0x0110	W	0x00000000	Subjective Quality Improvement Node Section Configuration
VEPU_NODE_SCT_SCAL	0x0114	W	0x00000000	Scaling List Node Section Configuration
VEPU_NODE_SCT_OSD	0x0118	W	0x00000000	OSD Node Section Configuration
VEPU_NODE_SCT_ST	0x011C	W	0x00000000	Status Node Section Configuration
VEPU_NODE_NXT	0x0120	W	0x00000000	Next Node Pointer
VEPU_ADR_VSBY_T	0x0270	W	0x00000000	Top Address of Luma Video Source Buffer
VEPU_ADR_VSBC_T	0x0274	W	0x00000000	Top Address of Chroma Video Source Buffer
VEPU_ADR_VSBY_B	0x0278	W	0x00000000	Bottom Address of Luma Video Source Buffer
VEPU_ADR_VSBC_B	0x027C	W	0x00000000	Bottom Address of Chroma Video Source Buffer
VEPU_ADR_VSB0_S	0x0280	W	0x00000000	Start Address of the 1st Video Source Buffer
VEPU_ADR_VSB1_S	0x0284	W	0x00000000	Start Address of the 2nd Video Source Buffer
VEPU_ADR_VSB2_S	0x0288	W	0x00000000	Start Address of the 3rd Video Source Buffer
VEPU_ADR_RFPH_W	0x028C	W	0x00000000	Write Address of FBC Reference Picture Header Buffer
VEPU_ADR_RFPB_W	0x0290	W	0x00000000	Write Address of FBC Reference Picture Header Buffer
VEPU_ADR_RFPH_R	0x0294	W	0x00000000	Read Address of FBC Reference Picture Header Buffer
VEPU_ADR_RFPB_R	0x0298	W	0x00000000	Read Address of FBC Reference Picture Header Buffer
VEPU_ADR_CMV_W	0x029C	W	0x00000000	Write Address of ColMv Buffer
VEPU_ADR_CMV_R	0x02A0	W	0x00000000	Read Address of ColMv Buffer
VEPU_ADR_DSP_W	0x02A4	W	0x00000000	Write Address of Down-sampled Picture Buffer
VEPU_ADR_DSP_R	0x02A8	W	0x00000000	Read Address of Down-sampled Picture Buffer
VEPU_ADR_MEI_W	0x02AC	W	0x00000000	Write Address of ME Information Buffer
VEPU_ADR_BSB_T	0x02B0	W	0x00000000	Top Address of Video Bit Stream Buffer

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Name	Offset	Size	Reset Value	Description
VEPU_ADR_BSB_B	0x02B4	W	0x00000000	Bottom Address of Video Bit Stream Buffer
VEPU_ADR_BSB_S	0x02B8	W	0x00000000	Start Address of Video Bit Stream Buffer
VEPU_ADR_BSB_R	0x02BC	W	0x00000000	Read Address of Video Bit Stream Buffer
VEPU_ADR_LPF_W	0x02C0	W	0x00000000	Base Address of LPF Buffer for wirte
VEPU_ADR_LPF_R	0x02C4	W	0x00000000	Base Address of LPF Buffer for read
VEPU_ADR_EBUF_T	0x02C8	W	0x00000000	Top Address of External Line Buffer
VEPU_ADR_EBUF_B	0x02CC	W	0x00000000	Bottom Address of External Line Buffer
VEPU_ADR_RFPH_T	0x02D0	W	0x00000000	Top Address of FBC Reference Picture Header Buffer
VEPU_ADR_RFPH_B	0x02D4	W	0x00000000	Bottom Address of FBC Reference Picture Header Buffer
VEPU_ADR_RFPB_T	0x02D8	W	0x00000000	Top Address of FBC Reference Picture Body Buffer
VEPU_ADR_RFPB_B	0x02DC	W	0x00000000	Bottom Address of FBC Reference Picture Body Buffer
VEPU_ADR_SMR_R	0x02E0	W	0x00000000	Read Address of Smear Buffer
VEPU_ADR_SMR_W	0x02E4	W	0x00000000	Write Address of Smear Buffer
VEPU_ADR_ROI_R	0x02E8	W	0x00000000	Read Address of ROI Block Mapping Buffer
VEPU_ENC_PIC	0x0300	W	0x00000000	VEPU Common Encoding Configuration
VEPU_DVBM_ID	0x0308	W	0x00000000	DVBM id
VEPU_VBSB_SCT	0x030C	W	0x00000000	Video Bit Stream Buffer Section
VEPU_ENC_RSL	0x0310	W	0x00000000	Resolution
VEPU_VSP_FILL	0x0314	W	0x00000000	Video Source Process filling pixels for alignment.
VEPU_VSP_FMT	0x0318	W	0x00000000	Video Source Process Format
VEPU_SRC_UDFY	0x031C	W	0x00000000	Weight of user defined formula for RGB to Y conversion
VEPU_SRC_UDFU	0x0320	W	0x00000000	Weight of user defined formula for RGB to U conversion
VEPU_SRC_UDFV	0x0324	W	0x00000000	Weight of user defined formula for RGB to V conversion
VEPU_SRC_UDFO	0x0328	W	0x00000000	Offset of user defined formula for RGB to YUV conversion
VEPU_SRC_PROC	0x032C	W	0x00000000	Video Source Process
VEPU_PIC_OFST	0x0330	W	0x00000000	Encoding Picture Offset
VEPU_SRC_STRD0	0x0334	W	0x00000000	Video Source Stride0
VEPU_SRC_STRD1	0x0338	W	0x00000000	Video Source Stride1
VEPU_RC_CFG	0x0350	W	0x00000000	Rate Control Configuration
VEPU_RC_QP	0x0354	W	0x00000000	QP Configuration for Rate Control
VEPU_RC_TGT	0x0358	W	0x00000000	The Target Bit Rate for Rate Control
VEPU_SLI_SPLT	0x0360	W	0x00000000	Slice Split Configuration
VEPU_SLI_BYTE	0x0364	W	0x00000000	Number of bytes for Slice Split
VEPU_SLI_CNUM	0x0368	W	0x00000000	Number of CTU/MB for Slice Split

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Name	Offset	Size	Reset Value	Description
VEPU_BS_PAD	0x036C	W	0x00000000	Bistream Padding Configuration
VEPU_ME_RNGE	0x0370	W	0x00000000	Motion Estimation Range
VEPU_ME_CFG	0x0374	W	0x00000000	Motion Estimation Configuration
VEPU_ME_CACH	0x0378	W	0x00000000	ME cache configuration
VEPU_RDO_CFG_H264	0x03A0	W	0x00000000	H.264 RDO configuration, share address with HEVC
VEPU_RDO_MASK_MODE	0x03A4	W	0x00000000	Mode Mask of mode decision
VEPU_SYNT_NAL_H264	0x03B0	W	0x00000000	NAL configuration for H.264, share address with HEVC
VEPU_SYNT_SPS_H264	0x03B4	W	0x00000000	Sequence parameter set syntax configuration for H.264, share address with HEVC
VEPU_SYNT_PPS_H264	0x03B8	W	0x00000000	Picture parameter set configuration for H.264, share address with HEVC
VEPU_SYNT_SLI0_H264	0x03BC	W	0x00000000	Slice header configuration0 for H.264, share address with HEVC
VEPU_SYNT_SLI1_H264	0x03C0	W	0x00000000	Slice header configuration1 for H.264, share address with HEVC
VEPU_SYNT_SLI2_H264	0x03C4	W	0x00000000	Slice header configuration2 for H.264, share address with HEVC
VEPU_SYNT_REFM0_H264	0x03C8	W	0x00000000	Reference frame mark0 for H.264, share address with HEVC
VEPU_SYNT_REFM1_H264	0x03CC	W	0x00000000	Reference frame mark1 for H.264, share address with HEVC
VEPU_SYNT_REFM2_H264	0x03D0	W	0x00000000	Reference frame mark2 for H264
VEPU_H264_MV_LMT	0x03F0	W	0x00000000	H.264 Mv Limitation
VEPU_ADR_BSBT_JPEG	0x0400	W	0x00000000	Top Address of JPEG Bit Stream Buffer
VEPU_ADR_BSBB_JPEG	0x0404	W	0x00000000	Bottom Address of JPEG Bit Stream Buffer
VEPU_ADR_BSBS_JPEG	0x0408	W	0x00000000	Start Address of JPEG Bit Stream Buffer
VEPU_ADR_BSBR_JPEG	0x040C	W	0x00000000	Read Address of JPEG Bit Stream Buffer
VEPU_ADR_VSY_B_JPEG	0x0410	W	0x00000000	Bottom Address of Luma JPEG Source Buffer
VEPU_ADR_VSC_B_JPEG	0x0414	W	0x00000000	Bottom Address of Chroma JPEG Source Buffer
VEPU_ADR_VSY_T_JPEG	0x0418	W	0x00000000	Top Address of Luma JPEG Source Buffer
VEPU_ADR_VSC_T_JPEG	0x041C	W	0x00000000	Top Address of Chroma JPEG Source Buffer
VEPU_ADR_SRC0_JPEG	0x0420	W	0x00000000	Base address of the 1st storage area for video source
VEPU_ADR_SRC1_JPEG	0x0424	W	0x00000000	Base address of the 2nd storage area for video source
VEPU_ADR_SRC2_JPEG	0x0428	W	0x00000000	Base address of the 3rd storage area for video source
VEPU_BSP_SIZE_JPEG	0x042C	W	0x00000000	JPEG Bit Stream Buffer Section
VEPU_ENC_RSL_JPEG	0x0440	W	0x00000000	Resolution
VEPU_SRC_FILL_JPEG	0x0444	W	0x00000000	JPEG source filling pixels for align.
VEPU_SRC_FMT_JPEG	0x0448	W	0x00000000	JPEG source format and

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Name	Offset	Size	Reset Value	Description
VEPU_SRC_UDFY_JPEG	0x044C	W	0x00000000	Weight of user defined formula for RGB to Y conversion
VEPU_SRC_UDFU_JPEG	0x0450	W	0x00000000	Weight of user defined formula for RGB to U conversion
VEPU_SRC_UDFV_JPEG	0x0454	W	0x00000000	Weight of user defined formula for RGB to V conversion
VEPU_SRC_UDFO_JPEG	0x0458	W	0x00000000	Offset of user defined formula for RGB to YUV conversion
VEPU_SRC_PROC_JPEG	0x045C	W	0x00000000	JPEG source process
VEPU_PIC_OFST_JPEG	0x0460	W	0x00000000	Encoding picture offset
VEPU_SRC_STRD0_JPEG	0x0464	W	0x00000000	JPEG source stride0
VEPU_SRC_STRD1_JPEG	0x0468	W	0x00000000	JPEG source stride1
VEPU_JPEG_Y_CFG	0x0470	W	0x00000000	JPEG Quantization Bias for Y Component
VEPU_JPEG_U_CFG	0x0474	W	0x00000000	JPEG Quantization Bias for U Component
VEPU_JPEG_V_CFG	0x0478	W	0x00000000	JPEG Quantization Bias for V Component
VEPU_JPEG_BASE_CFG	0x047C	W	0x00000000	JPEG Base Configuration
VEPU_JPEG_BS_PART	0x0480	W	0x00000000	JPEG Bit Stream Partition
VEPU_RC_ADJ0	0x1000	W	0x00000000	QP adjust configuration for rate control
VEPU_RC_ADJ1	0x1004	W	0x00000000	QP adjust configuration for rate control
VEPU_RC_DTHD0	0x1008	W	0x00000000	Bits rate deviation threshold0
VEPU_RC_DTHD1	0x100C	W	0x00000000	Bits rate deviation threshold1
VEPU_RC_DTHD2	0x1010	W	0x00000000	Bits rate deviation threshold2
VEPU_RC_DTHD3	0x1014	W	0x00000000	Bits rate deviation threshold3
VEPU_RC_DTHD4	0x1018	W	0x00000000	Bits rate deviation threshold4
VEPU_RC_DTHD5	0x101C	W	0x00000000	Bits rate deviation threshold5
VEPU_RC_DTHD6	0x1020	W	0x00000000	Bits rate deviation threshold6
VEPU_RC_DTHD7	0x1024	W	0x00000000	Bits rate deviation threshold7
VEPU_RC_DTHD8	0x1028	W	0x00000000	Bits rate deviation threshold8
VEPU_ROI_QTHD0	0x1030	W	0x00000000	ROI QP threshold configuration0
VEPU_ROI_QTHD1	0x1034	W	0x00000000	ROI QP threshold configuration1
VEPU_ROI_QTHD2	0x1038	W	0x00000000	ROI QP threshold configuration2
VEPU_ROI_QTHD3	0x103C	W	0x00000000	ROI QP threshold configuration3
VEPU_AQ_TTHD0	0x1044	W	0x00000000	Texture threshold configuration0 for adaptive QP adjustment.
VEPU_AQ_TTHD1	0x1048	W	0x00000000	Texture threshold configuration1 for adaptive QP adjustment.
VEPU_AQ_TTHD2	0x104C	W	0x00000000	Texture threshold configuration2 for adaptive QP adjustment.
VEPU_AQ_TTHD3	0x1050	W	0x00000000	Texture threshold configuration3 for adaptive QP adjustment.
VEPU_AQ_STP0	0x1054	W	0x00000000	Adjustment step configuration0 for adaptive QP adjustment.
VEPU_AQ_STP1	0x1058	W	0x00000000	Adjustment step configuration1 for adaptive QP adjustment.
VEPU_AQ_STP2	0x105C	W	0x00000000	Adjustment step configuration2 for adaptive QP adjustment.
VEPU_AQ_STP3	0x1060	W	0x00000000	Adjustment step configuration3 for adaptive QP adjustment.

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Name	Offset	Size	Reset Value	Description
VEPU_MADI_ST_THD	0x1064	W	0x00000000	The Threshold Used for MADI Counting.
VEPU_MADP_ST_THD0	0x1068	W	0x00000000	The Threshold Configuration0/1 Used for MADP Counting.
VEPU_MADP_ST_THD1	0x106C	W	0x00000000	The Threshold Configuration2 Used for MADP Counting.
VEPU_KLUT_OFST	0x107C	W	0x00000000	Offset of (RDO) chroma cost weight table
VEPU_FMDC_ADJ0	0x1080	W	0x00000000	Frame Level Mode Decision Adjustment0
VEPU_BMAP_CFG	0x108C	W	0x00000000	Block Mapping ROI Configuration
VEPU_ROI0_POS_LT	0x1090	W	0x00000000	Regional ROI0 Left Top
VEPU_ROI0_POS_RB	0x1094	W	0x00000000	Regional ROI0 Right Bottom
VEPU_ROI0_BASE	0x1098	W	0x00000000	Regional ROI0 Base Configuration
VEPU_ROI0_MDC	0x109C	W	0x00000000	Regional ROI0 Mode Adjustment
VEPU_ROI1_POS_LT	0x10A0	W	0x00000000	Regional ROI1 Left Top
VEPU_ROI1_POS_RB	0x10A4	W	0x00000000	Regional ROI1 Right Bottom
VEPU_ROI1_BASE	0x10A8	W	0x00000000	Regional ROI1 Base Configuration
VEPU_ROI1_MDC	0x10AC	W	0x00000000	Regional ROI1 Mode Adjustment
VEPU_ROI2_POS_LT	0x10B0	W	0x00000000	Regional ROI2 Left Top
VEPU_ROI2_POS_RB	0x10B4	W	0x00000000	Regional ROI2 Right Bottom
VEPU_ROI2_BASE	0x10B8	W	0x00000000	Regional ROI2 Base Configuration
VEPU_ROI2_MDC	0x10BC	W	0x00000000	Regional ROI2 Mode Adjustment
VEPU_ROI3_POS_LT	0x10C0	W	0x00000000	Regional ROI3 Left Top
VEPU_ROI3_POS_RB	0x10C4	W	0x00000000	Regional ROI3 Right Bottom
VEPU_ROI3_BASE	0x10C8	W	0x00000000	Regional ROI3 Base Configuration
VEPU_ROI3_MDC	0x10CC	W	0x00000000	Regional ROI3 Mode Adjustment
VEPU_ROI4_POS_LT	0x10D0	W	0x00000000	Regional ROI4 Left Top
VEPU_ROI4_POS_RB	0x10D4	W	0x00000000	Regional ROI4 Right Bottom
VEPU_ROI4_BASE	0x10D8	W	0x00000000	Regional ROI4 Base Configuration
VEPU_ROI4_MDC	0x10DC	W	0x00000000	Regional ROI4 Mode Adjustment
VEPU_ROI5_POS_LT	0x10E0	W	0x00000000	Regional ROI5 Left Top
VEPU_ROI5_POS_RB	0x10E4	W	0x00000000	Regional ROI5 Right Bottom
VEPU_ROI5_BASE	0x10E8	W	0x00000000	Regional ROI5 Base Configuration
VEPU_ROI5_MDC	0x10EC	W	0x00000000	Regional ROI5 Mode Adjustment
VEPU_ROI6_POS_LT	0x10F0	W	0x00000000	Regional ROI6 Left Top
VEPU_ROI6_POS_RB	0x10F4	W	0x00000000	Regional ROI6 Right Bottom
VEPU_ROI6_BASE	0x10F8	W	0x00000000	Regional ROI6 Base Configuration
VEPU_ROI6_MDC	0x10FC	W	0x00000000	Regional ROI6 Mode Adjustment
VEPU_ROI7_POS_LT	0x1100	W	0x00000000	Regional ROI7 Left Top
VEPU_ROI7_POS_RB	0x1104	W	0x00000000	Regional ROI7 Right Bottom
VEPU_ROI7_BASE	0x1108	W	0x00000000	Regional ROI7 Base Configuration
VEPU_ROI7_MDC	0x110C	W	0x00000000	Regional ROI7 Mode Adjustment
VEPU_IPRD_TTHDY4_0_H264	0x1700	W	0x00000000	Texture thredsholds register0 for H.264 LUMA 4x4 intra prediction, share address with HEVC.
VEPU_IPRD_TTHDY4_1_H264	0x1704	W	0x00000000	Texture thredsholds register1 for H.264 LUMA 4x4 intra prediction, share address with HEVC.
VEPU_IPRD_TTHDC8_0_H264	0x1708	W	0x00000000	Texture thredsholds register0 for H.264 CHROMA 8x8 intra prediction, share address with HEVC.

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Name	Offset	Size	Reset Value	Description
VEPU_IPRD_TTHDC8_1_H264	0x170C	W	0x00000000	Texture thredsholds register1 for H.264 CHROMA 8x8 intra prediction, share address with HEVC.
VEPU_IPRD_TTHDY8_0_H264	0x1710	W	0x00000000	Texture thredsholds register0 for H.264 LUMA 8x8 intra prediction.
VEPU_IPRD_TTHDY8_1_H264	0x1714	W	0x00000000	texture thredsholds register1 for H.264 LUMA 8x8 intra prediction.
VEPU_IPRD_TTHD_UL_H264	0x1718	W	0x00000000	Texture thredsholds of up and left MB for H.264 LUMA intra prediction.
VEPU_IPRD_WGTY8_H264	0x171C	W	0x00000000	Teights of the cost for H.264 LUMA 8x8 intra prediction, share address with HEVC.
VEPU_IPRD_WGTY4_H264	0x1720	W	0x00000000	Weights of the cost for H.264 LUMA 4x4 intra prediction, share address with HEVC.
VEPU_IPRD_WGTY16_H264	0x1724	W	0x00000000	Weights of the cost for H.264 LUMA 16x16 intra prediction, share address with HEVC.
VEPU_IPRD_WGTC8_H264	0x1728	W	0x00000000	Weights of the cost for H.264 CHROMA 8x8 intra prediction, share address with HEVC.
VEPU_QNT_BIAS_COMB	0x1730	W	0x00000000	Quantization bias for H.264 and HEVC.
VEPU_ATR_THD0_H264	0x1740	W	0x00000000	H.264 anti ringing noise threshold configuration0.
VEPU_ATR_THD1_H264	0x1744	W	0x00000000	H.264 anti ringing noise threshold configuration1.
VEPU_ATR_WGT16_H264	0x1750	W	0x00000000	Weights of 16x16 cost for H.264 anti ringing noise.
VEPU_ATR_WGT8_H264	0x1754	W	0x00000000	Weights of 8x8 cost for H.264 anti ringing noise.
VEPU_ATR_WGT4_H264	0x1758	W	0x00000000	Weights of 4x4 cost for H.264 anti ringing noise.
VEPU_ME_SQI_COMB	0x1760	W	0x00000000	ME Subjective Quality Improvement
VEPU_CIME_MVD_TH_COMB	0x1764	W	0x00000000	CME Mvd Threshold
VEPU_CIME_MADP_TH_COMB	0x1768	W	0x00000000	CME MAPD Threshold
VEPU_CIME_MULTI_COMB	0x176C	W	0x00000000	CME Cost Multiplier
VEPU_RIME_MVD_TH_COMB	0x1770	W	0x00000000	RME Mvd Threshold
VEPU_RIME_MADP_TH_COMB	0x1774	W	0x00000000	RME MADP Threshold
VEPU_RIME_MULTI_COMB	0x1778	W	0x00000000	RME Cost Multiplier
VEPU_CMV_ST_TH_COMB	0x177C	W	0x00000000	CME Mv Status Threshold
VEPU_RDO_WGT_QP0	0x1900	W	0x00000000	Weight of RDO mode decision when QP is 0.
VEPU_RDO_WGT_QP1	0x1904	W	0x00000000	Weight of RDO mode decision when QP is 1.
VEPU_RDO_WGT_QP2	0x1908	W	0x00000000	Weight of RDO mode decision when QP is 2.

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Name	Offset	Size	Reset Value	Description
VEPU_RDO_WGT_QP3	0x190C	W	0x00000000	Weight of RDO mode decision when QP is 3.
VEPU_RDO_WGT_QP4	0x1910	W	0x00000000	Weight of RDO mode decision when QP is 4.
VEPU_RDO_WGT_QP5	0x1914	W	0x00000000	Weight of RDO mode decision when QP is 5.
VEPU_RDO_WGT_QP6	0x1918	W	0x00000000	Weight of RDO mode decision when QP is 6.
VEPU_RDO_WGT_QP7	0x191C	W	0x00000000	Weight of RDO mode decision when QP is 7.
VEPU_RDO_WGT_QP8	0x1920	W	0x00000000	Weight of RDO mode decision when QP is 8.
VEPU_RDO_WGT_QP9	0x1924	W	0x00000000	Weight of RDO mode decision when QP is 9.
VEPU_RDO_WGT_QP10	0x1928	W	0x00000000	Weight of group A for HEVC and H.264 RDO mode decision when QP is 10.
VEPU_RDO_WGT_QP11	0x192C	W	0x00000000	Weight of RDO mode decision when QP is 11.
VEPU_RDO_WGT_QP12	0x1930	W	0x00000000	Weight of RDO mode decision when QP is 12.
VEPU_RDO_WGT_QP13	0x1934	W	0x00000000	Weight of RDO mode decision when QP is 13.
VEPU_RDO_WGT_QP14	0x1938	W	0x00000000	Weight of RDO mode decision when QP is 14.
VEPU_RDO_WGT_QP15	0x193C	W	0x00000000	Weight of RDO mode decision when QP is 15.
VEPU_RDO_WGT_QP16	0x1940	W	0x00000000	Weight of RDO mode decision when QP is 16.
VEPU_RDO_WGT_QP17	0x1944	W	0x00000000	Weight of RDO mode decision when QP is 17.
VEPU_RDO_WGT_QP18	0x1948	W	0x00000000	Weight of RDO mode decision when QP is 18.
VEPU_RDO_WGT_QP19	0x194C	W	0x00000000	Weight of RDO mode decision when QP is 19.
VEPU_RDO_WGT_QP20	0x1950	W	0x00000000	Weight of RDO mode decision when QP is 20.
VEPU_RDO_WGT_QP21	0x1954	W	0x00000000	Weight of RDO mode decision when QP is 21.
VEPU_RDO_WGT_QP22	0x1958	W	0x00000000	Weight of RDO mode decision when QP is 22.
VEPU_RDO_WGT_QP23	0x195C	W	0x00000000	Weight of RDO mode decision when QP is 23.
VEPU_RDO_WGT_QP24	0x1960	W	0x00000000	Weight of RDO mode decision when QP is 24.
VEPU_RDO_WGT_QP25	0x1964	W	0x00000000	Weight of RDO mode decision when QP is 25.
VEPU_RDO_WGT_QP26	0x1968	W	0x00000000	Weight of RDO mode decision when QP is 26.
VEPU_RDO_WGT_QP27	0x196C	W	0x00000000	Weight of RDO mode decision when QP is 27.
VEPU_RDO_WGT_QP28	0x1970	W	0x00000000	Weight of RDO mode decision when QP is 28.

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Name	Offset	Size	Reset Value	Description
VEPU_RDO_WGT_QP29	0x1974	W	0x00000000	Weight of RDO mode decision when QP is 29.
VEPU_RDO_WGT_QP30	0x1978	W	0x00000000	Weight of RDO mode decision when QP is 30.
VEPU_RDO_WGTA_QP31	0x197C	W	0x00000000	Weight of RDO mode decision when QP is 31.
VEPU_RDO_WGT_QP32	0x1980	W	0x00000000	Weight of RDO mode decision when QP is 32.
VEPU_RDO_WGT_QP33	0x1984	W	0x00000000	Weight of RDO mode decision when QP is 33.
VEPU_RDO_WGT_QP34	0x1988	W	0x00000000	Weight of RDO mode decision when QP is 34.
VEPU_RDO_WGT_QP35	0x198C	W	0x00000000	Weight of RDO mode decision when QP is 35.
VEPU_RDO_WGT_QP36	0x1990	W	0x00000000	Weight of RDO mode decision when QP is 36.
VEPU_RDO_WGT_QP37	0x1994	W	0x00000000	Weight of RDO mode decision when QP is 37.
VEPU_RDO_WGT_QP38	0x1998	W	0x00000000	Weight of RDO mode decision when QP is 38.
VEPU_RDO_WGT_QP39	0x199C	W	0x00000000	Weight of RDO mode decision when QP is 39.
VEPU_RDO_WGT_QP40	0x19A0	W	0x00000000	Weight of RDO mode decision when QP is 40.
VEPU_RDO_WGT_QP41	0x19A4	W	0x00000000	Weight of RDO mode decision when QP is 41.
VEPU_RDO_WGT_QP42	0x19A8	W	0x00000000	Weight of RDO mode decision when QP is 42.
VEPU_RDO_WGT_QP43	0x19AC	W	0x00000000	Weight of RDO mode decision when QP is 43.
VEPU_RDO_WGT_QP44	0x19B0	W	0x00000000	Weight of RDO mode decision when QP is 44.
VEPU_RDO_WGT_QP45	0x19B4	W	0x00000000	Weight of RDO mode decision when QP is 45.
VEPU_RDO_WGT_QP46	0x19B8	W	0x00000000	Weight of RDO mode decision when QP is 46.
VEPU_RDO_WGT_QP47	0x19BC	W	0x00000000	Weight of RDO mode decision when QP is 47.
VEPU_RDO_WGT_QP48	0x19C0	W	0x00000000	Weight of RDO mode decision when QP is 48.
VEPU_RDO_WGT_QP49	0x19C4	W	0x00000000	Weight of RDO mode decision when QP is 49.
VEPU_RDO_WGT_QP50	0x19C8	W	0x00000000	Weight of RDO mode decision when QP is 50.
VEPU_RDO_WGT_QP51	0x19CC	W	0x00000000	Weight of RDO mode decision when QP is 51.
VEPU_WP_CFG	0x2000	W	0x00000000	Weight Prediction Configuration
VEPU_WP_GAIN	0x2004	W	0x00000000	Weight Prediction Gains
VEPU_WP_OFST	0x2008	W	0x00000000	Weight Prediction Offset
VEPU_RDO_SMEAR_CFG_COMB	0x2014	W	0x00000000	Smear Base Configuration.
VEPU_RDO_SMEAR_MADP_THD0_COMB	0x2018	W	0x00000000	Smear MADP Threshold0

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Name	Offset	Size	Reset Value	Description
VEPU_RDO_SMEAR_MADP_THD1_COMB	0x201C	W	0x00000000	Smear MADP Threshold1
VEPU_RDO_SMEAR_MADP_THD2_COMB	0x2020	W	0x00000000	Smear MADP Threshold2
VEPU_RDO_SMEAR_MADP_THD3_COMB	0x2024	W	0x00000000	Smear MADP Threshold3
VEPU_RDO_SMEAR_MADP_THD4_COMB	0x2028	W	0x00000000	Smear MADP Threshold4
VEPU_RDO_SMEAR_MADP_THD5_COMB	0x202C	W	0x00000000	Smear MADP Threshold5
VEPU_RDO_SMEAR_CNT_THD0_COMB	0x2030	W	0x00000000	Smear Block Count Threshold0
VEPU_RDO_SMEAR_CNT_THD1_COMB	0x2034	W	0x00000000	Smear Block Count Threshold1
VEPU_RDO_SMEAR_CNT_THD2_COMB	0x2038	W	0x00000000	Smear Block Count Threshold2
VEPU_RDO_SMEAR_CNT_THD3_COMB	0x203C	W	0x00000000	Smear Block Count Threshold3
VEPU_RDO_SMEAR_RESI_THD0_COMB	0x2040	W	0x00000000	Smear Residual Threshold0
VEPU_RDO_SMEAR_RESI_THD1_COMB	0x2044	W	0x00000000	Smear Residual Threshold1
VEPU_RDO_SMEAR_RESI_THD2_COMB	0x2048	W	0x00000000	Smear Residual Threshold2
VEPU_RDO_SMEAR_RESI_THD3_COMB	0x204C	W	0x00000000	Smear Residual Threshold3
VEPU_RDO_SMEAR_ST_THD0_COMB	0x2050	W	0x00000000	Smear Residual Threshold4
VEPU_RDO_SMEAR_ST_THD1_COMB	0x2054	W	0x00000000	Smear MADP Count Threshold
VEPU_RDO_B16_SKIP_ATF_THD0_COMB	0x2070	W	0x00000000	Anti-Flash threshold configuration0 for Skip Mode.
VEPU_RDO_B16_SKIP_ATF_THD1_COMB	0x2074	W	0x00000000	Anti-Flash threshold configuration1 for Skip Mode.
VEPU_RDO_B16_SKIP_ATF_WGT0_COMB	0x2078	W	0x00000000	Weights Configuration0 of Skip Mode for ATF Adjustment.
VEPU_RDO_B16_SKIP_ATF_WGT1_COMB	0x207C	W	0x00000000	Weights Configuration1 of Skip Mode for ATF Adjustment.
VEPU_RDO_B16_INTER_ATF_THD0_COMB	0x208C	W	0x00000000	Anti-Flash threshold configuration0 for Inter Mode.
VEPU_RDO_B16_INTER_ATF_THD1_COMB	0x2090	W	0x00000000	Anti-Flash threshold configuration1 for Inter Mode.
VEPU_RDO_B16_INTER_ATF_WGT_COMB	0x2094	W	0x00000000	Weights of Inter Mode for ATF Adjustment.
VEPU_RDO_B16_INTRA_ATF_THD0_COMB	0x20A4	W	0x00000000	Anti-Flash threshold configuration0 for Intra Mode.
VEPU_RDO_B16_INTRA_ATF_THD1_COMB	0x20A8	W	0x00000000	Anti-Flash threshold configuration1 for Intra Mode.
VEPU_RDO_B16_INTRA_ATF_WGT_COMB	0x20AC	W	0x00000000	Weights of Intra Mode for ATF Adjustment.
VEPU_RDO_B16_INTRA_ATF_CNT_THD_COMB	0x20B4	W	0x00000000	Anti-Flash histogram threshold configuration for Intra Mode.
VEPU_RDO_ATF_RESI_THD_COMB	0x20B8	W	0x00000000	Anti-Flash statistics threshold configuration.

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Name	Offset	Size	Reset Value	Description
VEPU_SCAL_H264_FST	0x2200	W	0x00000000	H.264 Scaling List Table First
VEPU_SCAL_H264_LST	0x2AFC	W	0x00000000	H.264 Scaling List Table Last
VEPU_QUA_TAB_JPEG_FST	0x2C80	W	0x00000000	JPEG Quantization Table0~2 First
VEPU_QUA_TAB_JPEG_LST	0x2DFC	W	0x00000000	JPEG Quantization Table0~2 Last
VEPU_ST_BSL_L32	0x4000	W	0x00000000	Low 32bits of bit stream length for current frame.
VEPU_ST_SSE_BSL	0x4004	W	0x00000000	High 8 bits of bit stream length for current frame and low 16 bits of encoding distortion (SSE).
VEPU_ST_SSE_H32	0x4008	W	0x00000000	High 32 bits of encoding distortion (SSE).
VEPU_ST_SSE_QP	0x400C	W	0x00000000	Sum of QP for the encoded frame.
VEPU_ST_SAO	0x4010	W	0x00000000	Number of CTUs which adjusted by SAO
VEPU_ST_HEAD_BL_L32	0x4014	W	0x00000000	Low 32 bits of RDO HeaderBits length.
VEPU_ST_HEAD_RES_BL	0x4018	W	0x00000000	High 8 bits of RDO HeaderBits length and low 16 bits of RDO ResidualBits length.
VEPU_ST_RES_BL_H24	0x401C	W	0x00000000	High 24 bits of RDO ResidualBits length.
VEPU_ST_ENC	0x4020	W	0x00000000	VEPU working status
VEPU_ST_LKT	0x4024	W	0x00000000	Status of link table mode encoding
VEPU_ST_NADR	0x4028	W	0x00000000	Address of the processing link table node
VEPU_ST_VBSB	0x402C	W	0x00000000	Status of video bit stream buffer
VEPU_ST_BUS	0x4030	W	0x00000000	VEPU bus status
VEPU_ST_SNUM	0x4034	W	0x00000000	Slice number status.
VEPU_ST_SLEN	0x4038	W	0x00000000	Status of slice length
VEPU_ST_LINK_TASK	0x403C	W	0x00000000	Link Table Task Status
VEPU_ST_SLEN_JPEG	0x4060	W	0x00000000	JPEG ECS Length
VEPU_ST_BSL_L32_JPEG	0x4064	W	0x00000000	Low 32 bit of JPEG Bit Stream Length
VEPU_ST_BSL_H8_JPEG	0x4068	W	0x00000000	High 8 bit of JPEG Bit Stream Length
VEPU_ST_JBSB	0x406C	W	0x00000000	Status of jpeg bit stream buffer
VEPU_ST_PNUM_P64	0x4080	W	0x00000000	Number of 64x64 inter predicted blocks
VEPU_ST_PNUM_P32	0x4084	W	0x00000000	Number of 32x32 inter predicted blocks
VEPU_ST_PNUM_P16	0x4088	W	0x00000000	Number of 16x16 inter predicted blocks
VEPU_ST_PNUM_P8	0x408C	W	0x00000000	Number of 8x8 inter predicted blocks
VEPU_ST_PNUM_I32	0x4090	W	0x00000000	Number of 32x32 intra predicted blocks
VEPU_ST_PNUM_I16	0x4094	W	0x00000000	Number of 16x16 intra predicted blocks
VEPU_ST_PNUM_I8	0x4098	W	0x00000000	Number of 8x8 intra predicted blocks

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Name	Offset	Size	Reset Value	Description
VEPU_ST_PNUM_I4	0x409C	W	0x00000000	Number of 4x4 intra predicted blocks
VEPU_ST_BNUM_B16	0x40A0	W	0x00000000	Number of 16x16 blocks in frame. H.264: number of macro-blocks in encoding frame. HEVC: number of 16x16 blocks in 16x16 aligned extended frame.
VEPU_ST_SMEAR_CNT	0x40A4	W	0x00000000	Number of 16x16 Smear Blocks
VEPU_ST_CPLX_SPT	0x40A8	W	0x00000000	Spatial complexity(MADI) for current encoding frame
VEPU_ST_MADI_LT_NUM0	0x40C0	W	0x00000000	Statistics0 of MADI 16x16 Blocks in Frame Top Left
VEPU_ST_MADI_LT_NUM1	0x40C4	W	0x00000000	Statistics1 of MADI 16x16 Blocks in Frame Top Left
VEPU_ST_MADI_RT_NUM0	0x40C8	W	0x00000000	Statistics0 of MADI 16x16 Blocks in Frame Top Right
VEPU_ST_MADI_RT_NUM1	0x40CC	W	0x00000000	Statistics1 of MADI 16x16 Blocks in Frame Top Right
VEPU_ST_MADI_LB_NUM0	0x40D0	W	0x00000000	Statistics0 of MADI 16x16 Blocks in Frame Bottom Left
VEPU_ST_MADI_LB_NUM1	0x40D4	W	0x00000000	Statistics1 of MADI 16x16 Blocks in Frame Bottom Left
VEPU_ST_MADI_RB_NUM0	0x40D8	W	0x00000000	Statistics0 of MADI 16x16 Blocks in Frame Bottom Right
VEPU_ST_MADI_RB_NUM1	0x40DC	W	0x00000000	Statistics1 of MADI 16x16 Blocks in Frame Bottom Right
VEPU_ST_MADP_LT_NUM0	0x40E0	W	0x00000000	Statistics0 of MADP 16x16 Blocks in Frame Top Left
VEPU_ST_MADP_LT_NUM1	0x40E4	W	0x00000000	Statistics1 of MADP 16x16 Blocks in Frame Top Left
VEPU_ST_MADP_RT_NUM0	0x40E8	W	0x00000000	Statistics0 of MADP 16x16 Blocks in Frame Top Right
VEPU_ST_MADP_RT_NUM1	0x40EC	W	0x00000000	Statistics1 of MADP 16x16 Blocks in Frame Top Right
VEPU_ST_MADP_LB_NUM0	0x40F0	W	0x00000000	Statistics0 of MADP 16x16 Blocks in Frame Bottom Left
VEPU_ST_MADP_LB_NUM1	0x40F4	W	0x00000000	Statistics1 of MADP 16x16 Blocks in Frame Bottom Left
VEPU_ST_MADP_RB_NUM0	0x40F8	W	0x00000000	Statistics0 of MADP 16x16 Blocks in Frame Bottom Right
VEPU_ST_MADP_RB_NUM1	0x40FC	W	0x00000000	Statistics1 of MADP 16x16 Blocks in Frame Bottom Right
VEPU_ST_CMV_LT_NUM0	0x4100	W	0x00000000	Statistics0 of CMV 16x16 Blocks in Frame Top Left
VEPU_ST_CMV_LT_NUM1	0x4104	W	0x00000000	Statistics1 of CMV 16x16 Blocks in Frame Top Left
VEPU_ST_CMV_RT_NUM0	0x4108	W	0x00000000	Statistics0 of CMV 16x16 Blocks in Frame Top Right
VEPU_ST_CMV_RT_NUM1	0x410C	W	0x00000000	Statistics1 of CMV 16x16 Blocks in Frame Top Right
VEPU_ST_CMV_LB_NUM0	0x4110	W	0x00000000	Statistics0 of CMV 16x16 Blocks in Frame Bottom Left
VEPU_ST_CMV_LB_NUM1	0x4114	W	0x00000000	Statistics1 of CMV 16x16 Blocks in Frame Bottom Left

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Name	Offset	Size	Reset Value	Description
VEPU_ST_CMV_RB_NUM0	0x4118	W	0x00000000	Statistics0 of CMV 16x16 Blocks in Frame Bottom Right
VEPU_ST_CMV_RB_NUM1	0x411C	W	0x00000000	Statistics1 of CMV 16x16 Blocks in Frame Bottom Right
VEPU_ST_VSP_ORG_VALUE0	0x4120	W	0x00000000	Extremum Value0 of Video YUV
VEPU_ST_VSP_ORG_VALUE1	0x4124	W	0x00000000	Extremum Value1 of Video YUV
VEPU_ST_VSP_JPEG_VALUE0	0x4128	W	0x00000000	Extremum Value0 of JPEG YUV
VEPU_ST_VSP_JPEG_VALUE1	0x412C	W	0x00000000	Extremum Value1 of JPEG YUV
VEPU_ST_DSP_Y_SUM	0x4130	W	0x00000000	Summation of Frame DSP Y Data
VEPU_ST_B8_QP0	0x4180	W	0x00000000	Number of block8x8s with QP=0
VEPU_ST_B8_QP1	0x4184	W	0x00000000	Number of block8x8s with QP=1
VEPU_ST_B8_QP2	0x4188	W	0x00000000	Number of block8x8s with QP=2
VEPU_ST_B8_QP3	0x418C	W	0x00000000	Number of block8x8s with QP=3
VEPU_ST_B8_QP4	0x4190	W	0x00000000	Number of block8x8s with QP=4
VEPU_ST_B8_QP5	0x4194	W	0x00000000	Number of block8x8s with QP=5
VEPU_ST_B8_QP6	0x4198	W	0x00000000	Number of block8x8s with QP=6
VEPU_ST_B8_QP7	0x419C	W	0x00000000	Number of block8x8s with QP=7
VEPU_ST_B8_QP8	0x41A0	W	0x00000000	Number of block8x8s with QP=8
VEPU_ST_B8_QP9	0x41A4	W	0x00000000	Number of block8x8s with QP=9
VEPU_ST_B8_QP10	0x41A8	W	0x00000000	Number of block8x8s with QP=10
VEPU_ST_B8_QP11	0x41AC	W	0x00000000	Number of block8x8s with QP=11
VEPU_ST_B8_QP12	0x41B0	W	0x00000000	Number of block8x8s with QP=12
VEPU_ST_B8_QP13	0x41B4	W	0x00000000	Number of block8x8s with QP=13
VEPU_ST_B8_QP14	0x41B8	W	0x00000000	Number of block8x8s with QP=14
VEPU_ST_B8_QP15	0x41BC	W	0x00000000	Number of block8x8s with QP=15
VEPU_ST_B8_QP16	0x41C0	W	0x00000000	Number of block8x8s with QP=16
VEPU_ST_B8_QP17	0x41C4	W	0x00000000	Number of block8x8s with QP=17
VEPU_ST_B8_QP18	0x41C8	W	0x00000000	Number of block8x8s with QP=18
VEPU_ST_B8_QP19	0x41CC	W	0x00000000	Number of block8x8s with QP=19
VEPU_ST_B8_QP20	0x41D0	W	0x00000000	Number of block8x8s with QP=20
VEPU_ST_B8_QP21	0x41D4	W	0x00000000	Number of block8x8s with QP=21
VEPU_ST_B8_QP22	0x41D8	W	0x00000000	Number of block8x8s with QP=22
VEPU_ST_B8_QP23	0x41DC	W	0x00000000	Number of block8x8s with QP=23
VEPU_ST_B8_QP24	0x41E0	W	0x00000000	Number of block8x8s with QP=24
VEPU_ST_B8_QP25	0x41E4	W	0x00000000	Number of block8x8s with QP=25
VEPU_ST_B8_QP26	0x41E8	W	0x00000000	Number of block8x8s with QP=26
VEPU_ST_B8_QP27	0x41EC	W	0x00000000	Number of block8x8s with QP=27
VEPU_ST_B8_QP28	0x41F0	W	0x00000000	Number of block8x8s with QP=28
VEPU_ST_B8_QP29	0x41F4	W	0x00000000	Number of block8x8s with QP=29
VEPU_ST_B8_QP30	0x41F8	W	0x00000000	Number of block8x8s with QP=0
VEPU_ST_B8_QP31	0x41FC	W	0x00000000	Number of block8x8s with QP=31
VEPU_ST_B8_QP32	0x4200	W	0x00000000	Number of block8x8s with QP=32
VEPU_ST_B8_QP33	0x4204	W	0x00000000	Number of block8x8s with QP=33
VEPU_ST_B8_QP34	0x4208	W	0x00000000	Number of block8x8s with QP=34
VEPU_ST_B8_QP35	0x420C	W	0x00000000	Number of block8x8s with QP=35
VEPU_ST_B8_QP36	0x4210	W	0x00000000	Number of block8x8s with QP=36
VEPU_ST_B8_QP37	0x4214	W	0x00000000	Number of block8x8s with QP=37
VEPU_ST_B8_QP38	0x4218	W	0x00000000	Number of block8x8s with QP=38
VEPU_ST_B8_QP39	0x421C	W	0x00000000	Number of block8x8s with QP=39

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Name	Offset	Size	Reset Value	Description
VEPU_ST_B8_QP40	0x4220	W	0x00000000	Number of block8x8s with QP=40
VEPU_ST_B8_QP41	0x4224	W	0x00000000	Number of block8x8s with QP=41
VEPU_ST_B8_QP42	0x4228	W	0x00000000	Number of block8x8s with QP=42
VEPU_ST_B8_QP43	0x422C	W	0x00000000	Number of block8x8s with QP=43
VEPU_ST_B8_QP44	0x4230	W	0x00000000	Number of block8x8s with QP=44
VEPU_ST_B8_QP45	0x4234	W	0x00000000	Number of block8x8s with QP=45
VEPU_ST_B8_QP46	0x4238	W	0x00000000	Number of block8x8s with QP=46
VEPU_ST_B8_QP47	0x423C	W	0x00000000	Number of block8x8s with QP=47
VEPU_ST_B8_QP48	0x4240	W	0x00000000	Number of block8x8s with QP=48
VEPU_ST_B8_QP49	0x4244	W	0x00000000	Number of block8x8s with QP=49
VEPU_ST_B8_QP50	0x4248	W	0x00000000	Number of block8x8s with QP=50
VEPU_ST_B8_QP51	0x424C	W	0x00000000	Number of block8x8s with QP=51
VEPU_ST_WDG	0x5000	W	0x00000000	VEPU watch dog status
VEPU_ST_PPL	0x5004	W	0x00000000	VEPU pipe line status
VEPU_ST_PPL_POS_VSP0	0x5008	W	0x00000000	Position of CTU/MB which is processed by pre-process0
VEPU_ST_PPL_POS_VSP1	0x500C	W	0x00000000	Position of CTU/MB which is processed by pre-process1
VEPU_ST_PPL_POS_CME	0x5010	W	0x00000000	Position of CTU/MB which is processed by CME
VEPU_ST_PPL_POS_SWIN	0x5014	W	0x00000000	Position of CTU/MB which is processed by SWIN
VEPU_ST_PPL_POS_RFME	0x5018	W	0x00000000	Position of CTU/MB which is processed by RFME
VEPU_ST_PPL_POS_PREN	0x501C	W	0x00000000	Position of CTU/MB which is processed by pre-intra
VEPU_ST_PPL_POS_RDO	0x5020	W	0x00000000	Position of CTU/MB which is processed by RDO
VEPU_ST_PPL_POS_LPF	0x5024	W	0x00000000	Position of CTU/MB which is processed by LPF
VEPU_ST_PPL_POS_ETPY	0x5028	W	0x00000000	Position of CTU/MB which is processed by ETPY
VEPU_ST_PPL_POS_JSP0	0x502C	W	0x00000000	Position of CTU/MB which is processed by pre-process0 of jpeg
VEPU_ST_PPL_POS_JSP1	0x5030	W	0x00000000	Position of CTU/MB which is processed by pre-process1 of jpeg
VEPU_ST_PPL_POS_JPEG	0x5034	W	0x00000000	Position of CTU/MB which is processed by JPEG
VEPU_ST_SLI_NUM	0x5040	W	0x00000000	Number of slices
VEPU_MMU_ADDR	0xF000	W	0x00000000	Page table address for AXI MMU
VEPU_MMU_ST	0xF004	W	0x00000000	Status of the MMU for AXI
VEPU_MMU_CMD	0xF008	W	0x00000000	MMU command for AXI
VEPU_MMU_PFA	0xF00C	W	0x00000000	Address of the last page fault for MMU
VEPU_MMU_ZAP	0xF010	W	0x00000000	Zap address for MMU
VEPU_MMU_ERR	0xF014	W	0x00000000	MMU error
VEPU_MMU_INT_CLR	0xF018	W	0x00000000	Interrupt clear for MMU
VEPU_MMU_INT_MSK	0xF01C	W	0x00000000	Interrupt mask for MMU
VEPU_MMU_INT_STA	0xF020	W	0x00000000	Interrupt status for MMU
VEPU_MMU_ACKG	0xF024	W	0x00000001	Auto clock gating for MMU

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

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10.5.17 VEPU540 Detail Registers Description

VEPU_VERSION

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:24	RW	0x50	ip_id VEPU ID. It is contant 0x50.
23	RO	0x0	reserved
22:21	RW	0x3	fbc_cap FBC capability: 2'h0: No FBC 2'h3: Support AFBC for video source and FBC for reconstructed picture Others: Reserved
20	RW	0x0	bfrm_cap B frame encoding capability. 1 means VEPU supports B frame encoding while 0 means not.
19:18	RW	0x0	filtr_cap Pre-process filter capability 2'h0: Basic pre-process filter 2'h3: No pre-process filter Others: Reserved
17:16	RW	0x0	osd_cap OSD capability. 2'h0: 8-area OSD with 256-color palette 2'h3: No OSD Others: Reserved
15:12	RW	0x0	res_cap Max resolution 4'h0: 4096x2304; 4'h1: 1920x1088; 4'h2: 8192x8192; 4'h3: 16384x16384; Others: Reserved.
11:10	RO	0x0	reserved
9	RW	0x1	hevc_cap HEVC encoding capability. 1 means VEPU supports HEVC encoding while 0 means not
8	RW	0x1	h264_cap H.264 encoding capability. 1 means VEPU supports H.264 encoding, while 0 means not.
7:0	RW	0x0b	sub_ver VEPU sub-version. 0x11: PUMA 0x12: ORION 0x13: 1126B 0x14: Otter

VEPU_ENC_STRT

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
10:8	RW	0x0	vepu_cmd VEPU command: 3'h0: N/A 3'h1: One-frame encoding by register configuration 3'h2: Multi-frame encoding start with link table mode 3'h3: Multi-frame encoding update (with link table mode) 3'h4: One-frame encoding by register configuration (frame configuration by link table) 3'h5: Link table encoding force pause
7:0	RW	0x00	lkt_num Number of new nodes added to Link Table.

VEPU_ENC_CLR

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	force_clr Force clear. Clear all sub-modules besides Configuration Registers and AHB Data Path.
0	RW	0x0	safe_clr Safe clear. It only clears DMA module to confirm AXI transaction integrity. 1'h0: Safe clear is not performing. 1'h1: Safe clear is performing.

VEPU_VS_LDLY

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RW	0x0	dvbm_inf_sel DVBM VINF Information selector 1'h0: Hardware INF Information. 1'h1: Software INF Information.
25	RW	0x0	dvbm_ack_sel DVBM VCNT Acknowledge selector 1'h0: Hardware VCNT Acknowledge. 1'h1: Software VCNT Acknowledge.
24	RW	0x0	dvbm_ack_soft Software DVBM VCNT Acknowledge. 1'h0: DVBM VCNT disconnection finish. 1'h1: DVBM VCNT connection finish.
23:22	RO	0x0	reserved
21:14	RW	0x00	vswm_fcnt_soft Source video water mark, frame count.
13:0	RW	0x0000	vswm_lcnt_soft Source video water mark, line count.

VEPU_INT_EN

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	dvbm_dcnt_en DVBM disconnect interrupt enable.
14	RW	0x0	jbsb_sct_en JPEG bit stream buffer write section interrupt enable.

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Bit	Attr	Reset Value	Description
13	RW	0x0	jbsb_oflw_en JPEG bit stream buffer overflow interrupt enable.
12	RW	0x0	jslc_done_en One slice of JPEG encoding finish interrupt enable.
11	RW	0x0	lkt_fstp_en Link Table force stop interrupt enable
10	RW	0x0	lkt_estp_en Link Table encoding error stop interrupt enable.
9	RW	0x0	lkt_oerr_en Link Table opertaion error interrupt enable.
8	RW	0x0	wdg_en Watch dog(time out) interrupt enable.
7	RW	0x0	dvbm_ferr_en DVBM frame number matching error interrupt enable.
6	RW	0x0	fenc_err_en Frame encoding error interrupt enable.
5	RW	0x0	vbsb_sct_en Video bit stream buffer write section interrupt enable.
4	RW	0x0	vbsb_oflw_en Video Bit stream buffer overflow enable.
3	RW	0x0	vslc_done_en One slice of video encoding finish interrupt enable.
2	RW	0x0	sclr_done_en Safe clear finish interrupt enable.
1	RW	0x0	lkt_node_done_en Link table one node finish interrupt enable.
0	RW	0x0	fenc_done_en One frame encoding finish interrupt enable.

VEPU_INT_MSK

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	dvbm_dcnt_msk DVBM disconnect interrupt mask.
14	RW	0x0	jbsb_sct_msk JPEG bit stream buffer write section interrupt mask.
13	RW	0x0	jbsb_oflw_msk JPEG bit stream buffer overflow interrupt mask.
12	RW	0x0	jslc_done_msk One slice of JPEG encoding finish interrupt mask.
11	RW	0x0	lkt_fstp_msk Link Table force stop interrupt mask.
10	RW	0x0	lkt_estp_msk Link Table encoding error stop interrupt mask.
9	RW	0x0	lkt_oerr_msk Link Table opertaion error interrupt mask.
8	RW	0x0	wdg_msk Watch dog(time out) interrupt mask.
7	RW	0x0	dvbm_ferr_msk DVBM frame number matching error interrupt mask.
6	RW	0x0	fenc_err_msk Frame encoding error interrupt mask.
5	RW	0x0	vbsb_sct_msk Video Bit stream buffer write section interrupt mask.

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Bit	Attr	Reset Value	Description
4	RW	0x0	vbsb_oflw_msk Video Bit stream buffer overflow mask.
3	RW	0x0	vslc_done_msk One slice of video encoding finish interrupt mask.
2	RW	0x0	sclr_done_msk Safe clear finish interrupt mask.
1	RW	0x0	lkt_node_done_msk Link table one node finish interrupt mask.
0	RW	0x0	fenc_done_msk One frame encoding finish interrupt mask.

VEPU_INT_CLR

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	dvbm_dcnt_clr DVBM disconnect interrupt clear.
14	RW	0x0	jbsb_sct_clr JPEG bit stream buf write section interrupt clear.
13	RW	0x0	jbsb_oflw_clr JPEG bit stream buffer overflow interrupt clear.
12	RW	0x0	jslc_done_clr One slice of JPEG encoding finish interrupt clear.
11	RW	0x0	lkt_fstp_clr Link Table force stop interrupt clear.
10	RW	0x0	lkt_estp_clr Link Table encoding error stop interrupt clear.
9	RW	0x0	lkt_oerr_clr Link Table opertaion error interrupt clear.
8	RW	0x0	wdg_clr Watch dog(time out) interrupt clear.
7	RW	0x0	dvbm_ferr_clr DVBM frame number matching error interrupt clear.
6	RW	0x0	fenc_err_clr Frame encoding error interrupt clear.
5	RW	0x0	vbsb_sct_clr Video bit stream buffer write section interrupt clear.
4	RW	0x0	vbsb_oflw_clr Video bit stream buffer overflow clear.
3	RW	0x0	vslc_done_clr One slice of video encoding finish interrupt clear.
2	RW	0x0	sclr_done_clr Safe clear finish interrupt clear.
1	RW	0x0	lkt_node_done_clr Link table one node finish interrupt clear.
0	RW	0x0	fenc_done_clr One frame encoding finish interrupt clear.

VEPU_INT_STA

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	dvbm_dcnt_sta DVBM disconnect interrupt status.

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Bit	Attr	Reset Value	Description
14	RW	0x0	jbsb_sct_sta JPEG bit stream buffer write section interrupt status.
13	RW	0x0	jbsb_oflw_sta JPEG bit stream buffer overflow interrupt status.
12	RW	0x0	jslc_done_sta One slice of JPEG encoding finish interrupt status.
11	RW	0x0	lkt_fstp_sta Link Table force stop interrupt status.
10	RW	0x0	lkt_estp_sta Link Table encoding error stop interrupt status.
9	RW	0x0	lkt_oerr_sta Link Table opertaion error interrupt status.
8	RW	0x0	wdg_sta Watch dog(time out) interrupt status.
7	RW	0x0	dvbm_ferr_sta DVBM frame number matching error interrupt status.
6	RW	0x0	fenc_err_sta Frame encoding error interrupt status.
5	RW	0x0	vbsb_sct_sta Bit stream buffer write section interrupt status.
4	RW	0x0	vbsb_oflw_sta Bit stream buffer of video overflow status.
3	RW	0x0	vslc_done_sta One slice of video encoding finish interrupt status.
2	RW	0x0	sclr_done_sta Safe clear finish interrupt status.
1	RW	0x0	lkt_node_done_sta Link table one node finish interrupt status.
0	RW	0x0	fenc_done_sta One frame encoding finish interrupt status.

VEPU_DBUS_ENDN

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	rec_nfbc_bus_edin Data swap for reference picture channel without fbc. [3]: Swap 64 bits in 128 bits [2]: Swap 32 bits in 64 bits [1]: Swap 16 bits in 32 bits [0]: Swap 8 bits in 16 bits
27:24	RW	0x0	lktw_bus_edin Data swap for link table write channel. [3]: Swap 64 bits in 128 bits [2]: Swap 32 bits in 64 bits [1]: Swap 16 bits in 32 bits [0]: Swap 8 bits in 16 bits
23:20	RW	0x0	roir_bus_edin Data swap for ROI configuration read channel. [3]: Swap 64 bits in 128 bits [2]: Swap 32 bits in 64 bits [1]: Swap 16 bits in 32 bits [0]: Swap 8 bits in 16 bits

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Bit	Attr	Reset Value	Description
19:16	RW	0x0	lktr_bus_edin Data swap for link table read channel. [3]: Swap 64 bits in 128 bits [2]: Swap 32 bits in 64 bits [1]: Swap 16 bits in 32 bits [0]: Swap 8 bits in 16 bits
15:12	RW	0x0	bsw_bus_edin Data swap for bis stream write channel. [3]: Swap 64 bits in 128 bits [2]: Swap 32 bits in 64 bits [1]: Swap 16 bits in 32 bits [0]: Swap 8 bits in 16 bits
11:8	RW	0x0	meiw_bus_edin Data swap for ME information write channel. [3]: Swap 64 bits in 128 bits [2]: Swap 32 bits in 64 bits [1]: Swap 16 bits in 32 bits [0]: Swap 8 bits in 16 bits
7:4	RW	0x0	vsl_bus_edin Data swap for video source loading channel. [3]: Swap 64 bits in 128 bits [2]: Swap 32 bits in 64 bits [1]: Swap 16 bits in 32 bits [0]: Swap 8 bits in 16 bits
3:0	RW	0x0	jbsw_bus_edin Data swap for jpeg bit stream write channel. [3]: Swap 64 bits in 128 bits [2]: Swap 32 bits in 64 bits [1]: Swap 16 bits in 32 bits [0]: Swap 8 bits in 16 bits

VEPU_DBUS_CFG

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	axi_brsp_cke AXI write response channel check enable. [9]: JPEG bit stream mode write reponse check enable. [8]: Smear state-d write reponse check enable. [7]: Link table mode write reponse check enable. [6]: External line buffer write response check enable. [5]: Lpf write response check enable. [4]: Reconstructed picture write response check enable. [3]: ME information write response check enable. [2]: Co-located Mv write response check enable. [1]: Down-sampled picture write response check enable. [0]: Video bit stream write response check enable.
15:0	RO	0x0000	reserved

VEPU_ENC_WDG

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
23:0	RW	0x000000	wdg_cnt One frame encoding watch dog counter. 24'h0: No time limit 24'hx: x*1024 core clock cycles

VEPU_QOS_CFG

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:7	RW	0x0	hurry_high The hurry value for high priority.
6:4	RW	0x0	hurry_mid The hurry value for middle priority.
3:1	RW	0x0	hurry_low The hurry value for low priority.
0	RW	0x0	hurry_en AXI Bus hurry signal adjustment enable.

VEPU_QOS_PERD

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	qos_period Qos adjustment period.

VEPU_QOS_THD_L

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hurry_thd_low Delay threshold for low priority.

VEPU_QOS_THD_M

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hurry_thd_mid Delay threshold for middle priority.

VEPU_QOS_THD_H

Address: Operational Base + offset (0x004C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hurry_thd_high Delay threshold for high priority.

VEPU_FREQ_RDCT

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	ahb_frdct_en AHB clock frequency reduction enable
1	RW	0x0	axi_frdct_en AXI clock frequency reduction enable
0	RW	0x0	core_frdct_en Core clock frequency reduction enable

VEPU_OPT_STRG

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Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	lkt_estp_en Link table stop after encoding error.
3	RW	0x1	sram_ckg_en Sram auto clock gating enable.
2	RW	0x1	tmvp_flush TMVP flush before frame encoding finish.
1	RW	0x0	auto_reset Core clock domain auto reset after frame finished.
0	RW	0x1	cke VEPU auto clock gating enable.

VEPU_RDO_CKG_H264

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	intra4_ckg H264 RDO intra4 clock-gating enable.
8	RW	0x0	intra8_ckg H264 RDO intra8 clock-gating enable.
7	RW	0x0	inter_pred_ckg H264 RDO inter prediction clock-gating enable.
6	RW	0x0	inter_ctrl_ckg H264 RDO inter control clock-gating enable.
5	RW	0x0	inter_mode_ckg H264 RDO inter mode clock-gating enable.
4	RW	0x0	4x4_0_bits_ckg H264 RDO 4x4_0_bits clock-gating enable.
3	RW	0x0	4x4_1_bits_ckg H264 RDO 4x4_1_bits clock-gating enable.
2	RW	0x0	8x8_bits_ckg H264 RDO 8x8_bits clock-gating enable.
1	RW	0x0	tq4_ckg H264 RDO tq4 clock-gating enable.
0	RW	0x0	tq8_ckg H264 RDO tq8 clock-gating enable.

VEPU_CORE_ID

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	core_id VEPU core ID.

VEPU_DVBM_CFG

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	vrsp_half_cycle DVBM vrsp channel transaction half cycle.
3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2	RW	0x0	vinf_frm_match DVBM frame ID matching enable. 1'h0: VEPU encodes all the DVBM frames. 1'h1: VEPU only encode the frames with ID equal to ENC_ID.frame_id.
1	RW	0x0	src_badr_sel DVBM video source address select. 1'h0: from DVBM information. 1'h1: from ST register.
0	RW	0x0	dvbm_en DVBM enable.

VEPU_LKT_BASE_ADDR

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	lkt_addr High 28 bits of the address for the first node in link table.
3:0	RO	0x0	reserved

VEPU_NODE_OCFG

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RW	0x000	node_id Link table node ID
3	RO	0x0	reserved
2	RW	0x0	node_int Send lkt_node_done interrupt after this node finish encoding.
1:0	RW	0x0	core_id Only the VEPU with the same core ID can use this node.

VEPU_NODE_SCT_PCFG

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	addr_sct_pcfg High 28 bits of the address of Picture Configuration Node Section.
3:1	RO	0x0	reserved
0	RW	0x0	pcfg_len Picture Configuration Node Section load enable.

VEPU_NODE_SCT_RC

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	addr_sct_rc High 28 bits of the address of Rate Control Node Section.
3:1	RO	0x0	reserved
0	RW	0x0	rc_len Rate Control Node Section load enable.

VEPU_NODE_SCT_PAR

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	addr_sct_par High 28 bits of the address of Parameter Node Section.
3:1	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	par_len Parameter Node Section load enable.

VEPU_NODE_SCT_SQI

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	addr_sct_sqi High 28 bits of the address of SQI Node Section.
3:1	RO	0x0	reserved
0	RW	0x0	sqi_len SQI Node Section load enable.

VEPU_NODE_SCT_SCAL

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	addr_sct_scal High 28 bits of the address of Scaling List Node Section.
3:1	RO	0x0	reserved
0	RW	0x0	scal_len Scaling List Node Section load enable.

VEPU_NODE_SCT_OSD

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	addr_sct_osd High 28 bits of the address of OSD Node Section.
3:1	RO	0x0	reserved
0	RW	0x0	osd_len OSD Node Section load enable.

VEPU_NODE_SCT_ST

Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	addr_sct_st High 28 bits of the address of Status Node Section.
3:1	RO	0x0	reserved
0	RW	0x0	st_oen Status Node Section output enable.

VEPU_NODE_NXT

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	addr_nxt_node High 28 bits of the next node address.
3:1	RO	0x0	reserved
0	RW	0x0	nxt_node_vld Next node is valid.

VEPU_ADR_VSBY_T

Address: Operational Base + offset (0x0270)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	addr_vsby_t Top address of Luma Video Source Buffer.
3:0	RO	0x0	reserved

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VEPU_ADR_VSBC_T

Address: Operational Base + offset (0x0274)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	addr_vsbc_t Top address of Chroma Video Source Buffer.
3:0	RO	0x0	reserved

VEPU_ADR_VSBY_B

Address: Operational Base + offset (0x0278)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	addr_vsby_b Bottom address of Luma Video Source Buffer.
3:0	RO	0x0	reserved

VEPU_ADR_VSBC_B

Address: Operational Base + offset (0x027C)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	addr_vsbc_b Bottom address of Chroma Video Source Buffer.
3:0	RO	0x0	reserved

VEPU_ADR_VSB0_S

Address: Operational Base + offset (0x0280)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	addr_vsb0_s Start address of the 1st Video Source Buffer. ARGB8888, BGR888, RGB565, YUYV422 and UYUV422 have only one video source buffer, while addr_vsb0_s is configured as the start address of video source frame buffer. YUV422/420 semi-planar have 2 vdieo source buffers, while addr_vsb0_s is configured as the start address of Y buffer. YUV422/420 planar have 3 vdieo source buffers, while addr_vsb0_s is configured as the start address of Y frame buffer. Note that if the video source is compressed by AFBC, addr_vsb0_s is configured as the start address of header buffer, and it is 16-byte aligned.

VEPU_ADR_VSB1_S

Address: Operational Base + offset (0x0284)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	addr_vsb1_s Start address of the 2nd video source buffer. ARGB8888, BGR888, RGB565, YUYV422 and UYUV422 have only one video source buffer, while addr_vsb1_s is reserved. YUV422/420 semi-planar have 2 video source buffers, while addr_vsb1_s is configured as the start address of CHROMA buffer. YUV422/420 planar have 3 video source buffers, while addr_vsb1_s is configured as the start address of U buffer. Note that if the video source is compressed by AFBC, addr_vsb1_s is configured as the start address of body buffer.

VEPU_ADR_VSB2_S

Address: Operational Base + offset (0x0288)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	addr_vsb2_s Start address of V frame buffer when video source is uncompress and color format is YUV422/420 planar.

VEPU_ADR_RFPH_W

Address: Operational Base + offset (0x028C)

Bit	Attr	Reset Value	Description
31:12	RW	0x00000	addr_rfph_w High 20 bits write address of the FBC reference picture header buffer.
11:0	RO	0x000	reserved

VEPU_ADR_RFPB_W

Address: Operational Base + offset (0x0290)

Bit	Attr	Reset Value	Description
31:12	RW	0x00000	addr_rfpb_w High 20 bits write address of the FBC reference picture body buffer.
11:0	RO	0x000	reserved

VEPU_ADR_RFPH_R

Address: Operational Base + offset (0x0294)

Bit	Attr	Reset Value	Description
31:12	RW	0x00000	addr_rfph_r High 20 bits read address of the FBC reference picture header buffer.
11:0	RO	0x000	reserved

VEPU_ADR_RFPB_R

Address: Operational Base + offset (0x0298)

Bit	Attr	Reset Value	Description
31:12	RW	0x00000	addr_rfpb_r High 20 bits read address of the FBC reference picture body buffer.
11:0	RO	0x000	reserved

VEPU_ADR_CMV_W

Address: Operational Base + offset (0x029C)

Bit	Attr	Reset Value	Description
31:10	RW	0x000000	addr_cmv_w High 22 bits write address of col-located Mv buffer, HEVC only.
9:0	RO	0x000	reserved

VEPU_ADR_CMV_R

Address: Operational Base + offset (0x02A0)

Bit	Attr	Reset Value	Description
31:10	RW	0x000000	addr_cmv_r High 22 bits read address of col-located Mv buffer, HEVC only.
9:0	RO	0x000	reserved

VEPU_ADR_DSP_W

Address: Operational Base + offset (0x02A4)

Bit	Attr	Reset Value	Description
31:10	RW	0x000000	addr_dsp_w High 22 bits write address of down-sampled picture buffer.

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Bit	Attr	Reset Value	Description
9:0	RO	0x000	reserved

VEPU_ADR_DSP_R

Address: Operational Base + offset (0x02A8)

Bit	Attr	Reset Value	Description
31:10	RW	0x000000	addr_dsp_r High 22 bits read address of down-sampled picture buffer.
9:0	RO	0x000	reserved

VEPU_ADR_MEI_W

Address: Operational Base + offset (0x02AC)

Bit	Attr	Reset Value	Description
31:10	RW	0x000000	addr_mei_w High 22 bits write address of ME information buffer.
9:0	RO	0x000	reserved

VEPU_ADR_BSB_T

Address: Operational Base + offset (0x02B0)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	addr_bsb_t High 25 bits top address of video bit stream buffer.
7:0	RO	0x00	reserved

VEPU_ADR_BSB_B

Address: Operational Base + offset (0x02B4)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	addr_bsb_b High 25 bits bottom address of video bit stream buffer.
7:0	RO	0x00	reserved

VEPU_ADR_BSB_S

Address: Operational Base + offset (0x02B8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	addr_bsb_s Start address of video bit stream buffer. VEPU begins to write bit stream from this address and increase address automatically.

VEPU_ADR_BSB_R

Address: Operational Base + offset (0x02BC)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	addr_bsb_r Read address of video bit stream buffer, 128B aligned. VEPU will pause when write address meets read address and then send an interrupt. SW should move some data out from bit stream buffer and change this register accordingly. After that VEPU will continue processing automatically.
7:4	RO	0x0	reserved
3:0	RW	0x0	addr_bsb_msk Video bit stream buffer address mask. Note that the VEPU's real-time write address is marked in BSB_STUS. [0]: addr_bsbw mask; [1]: addr_bsbr mask; [2]: addr_bsbt mask; [3]: addr_bsbb mask;

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VEPU_ADR_LPF_W

Address: Operational Base + offset (0x02C0)

Bit	Attr	Reset Value	Description
31:10	RW	0x000000	addr_lpf_w High 22 bits base address of the buffer for loop-filter write between tiles, hevc only.
9:0	RO	0x000	reserved

VEPU_ADR_LPF_R

Address: Operational Base + offset (0x02C4)

Bit	Attr	Reset Value	Description
31:10	RW	0x000000	addr_lpf_r High 22 bits base address of the buffer for loop-filter read between tiles, hevc only.
9:0	RO	0x000	reserved

VEPU_ADR_EBUF_T

Address: Operational Base + offset (0x02C8)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	addr_ebuf_t High 24 bits of the top address for external line buffer.
7:0	RO	0x00	reserved

VEPU_ADR_EBUF_B

Address: Operational Base + offset (0x02CC)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	addr_ebuf_b High 24 bits of the bottom address for external line buffer.
7:0	RO	0x00	reserved

VEPU_ADR_RFPH_T

Address: Operational Base + offset (0x02D0)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	addr_rfph_t High 28 bit top address of FBC reference picture header buffer.
3:0	RO	0x0	reserved

VEPU_ADR_RFPH_B

Address: Operational Base + offset (0x02D4)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	addr_rfph_b High 28 bit bottom address of FBC reference picture header buffer.
3:0	RO	0x0	reserved

VEPU_ADR_RFPB_T

Address: Operational Base + offset (0x02D8)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	addr_rfpb_t High 28 bit top address of FBC reference picture body buffer.
3:0	RO	0x0	reserved

VEPU_ADR_RFPB_B

Address: Operational Base + offset (0x02DC)

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Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	addr_rfpb_b High 28 bit bottom address of FBC reference picture body buffer.
3:0	RO	0x0	reserved

VEPU_ADR_SMR_R

Address: Operational Base + offset (0x02E0)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	addr_smr_rd High 28 bit read address of smear buffer.
3:0	RO	0x0	reserved

VEPU_ADR_SMR_W

Address: Operational Base + offset (0x02E4)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	addr_smr_w High 28 bit write address of smear buffer.
3:0	RO	0x0	reserved

VEPU_ADR_ROI_R

Address: Operational Base + offset (0x02E8)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	addr_roi_r High 28 bit read address of ROI block mapping buffer.
3:0	RO	0x0	reserved

VEPU_ENC_PIC

Address: Operational Base + offset (0x0300)

Bit	Attr	Reset Value	Description
31	RW	0x0	rec_fbc_dis Recon data fbc disable.
30	RW	0x0	slen_fifo Slice length fifo enable.
29:24	RO	0x00	reserved
23:19	RW	0x00	log2_ctu_num_hevc Logarithm of bit width to express ctu number in current picture, HEVC only.
18:14	RW	0x00	num_pic_tot_cur_hevc NumPicTotalCurr for HEVC reference picture list modification.
13:8	RW	0x00	pic_qp QP value for current frame encoding.
7:5	RO	0x0	reserved
4	RW	0x0	bs_scp Output start code prefix.
3	RW	0x0	mei_stor Output ME(motion estimation) information.
2	RW	0x0	cur_frm_ref Current frame should be referenced in future.
1:0	RW	0x0	enc_stnd Video standard. 2'h0: H.264 encoding 2'h1: HEVC encoding 2'h2: Video disable

VEPU_DVBM_ID

Address: Operational Base + offset (0x0308)

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Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	RW	0x0	vrsp_rtn_en DVBM vrsp channel transaction enable.
17:16	RW	0x0	ch_id Video source channel ID 2'b00: frame buffer 2'b01: DVBM buffer others: reserved
15:8	RO	0x00	reserved
7:0	RW	0x00	frame_id DVBM frame ID.

VEPU_VBSB_SCT

Address: Operational Base + offset (0x030C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	vbsb_sct Video bit stream buffer section size, 0 is disable.

VEPU_ENC_RSL

Address: Operational Base + offset (0x0310)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	pic_hd8_m1 Ceil(encoding picture height/8) -1
15:11	RO	0x00	reserved
10:0	RW	0x000	pic_wd8_m1 Ceil(encoding picture width/8) -1

VEPU_VSP_FILL

Address: Operational Base + offset (0x0314)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x00	pic_hfill Filling pixels to keep (encoding) picture height is 8 pixels aligned for HEVC and 16 pixels aligned for H.264.
15:6	RO	0x000	reserved
5:0	RW	0x00	pic_wfill Filling pixels to keep (encoding) picture width is 8 pixels aligned for HEVC and 16 pixels aligned for H.264.

VEPU_VSP_FMT

Address: Operational Base + offset (0x0318)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10	RW	0x0	chr_ds_fltr Chroma down sample filter. 1'b0: decimation chroma down sample. 1'b1: interpolation chroma down sample.
9	RW	0x0	rngc_mode Video source full range and limit range conversion mode. 1'b0: full range to limit range. 1'b1: limit range to full range.
8	RW	0x0	rngc_en Video Source range conversion enable.

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Bit	Attr	Reset Value	Description
7	RW	0x0	enc_fmt Encoding color format. 1'h0: YUV400; 1'h1: YUV420;
6	RW	0x0	src_rcne Video source is reconstructed picture.
5:2	RW	0x0	src_cfmt Video source color format. 4'h0: BGRA8888 4'h1: RGB888 4'h2: RGB565 4'h4: YUV422SP 4'h5: YUV422P 4'h6: YUV420SP 4'h7: YUV420P 4'h8: YUYV422 4'h9: UYVY422 4'ha: YUV400 4'hc: YUV444SP 4'hd: YUV444P Others: Reserved
1	RW	0x0	rbuv_swap Swap the position of R and B for BGRA8888, RGB888, RGB 656 format; Swap the position of U and V for YUV422-SP, YUV420-SP, YUYV422 and UYUV422 format. 1'h0: RGB or YUYV or UYVY. 1'h1: BGR or YVYU or VYUY.
0	RW	0x0	alpha_swap Swap the position of alpha and RGB for ARBG8888. 1'h0: BGRA8888 or RGBA8888. 1'h1: ABGR8888 or ARGB8888.

VEPU_SRC_UDFY

Address: Operational Base + offset (0x031C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:18	RW	0x000	csc_wgt_r2y Weight of RED in RGB to Y conversion formula.
17:9	RW	0x000	csc_wgt_g2y Weight of GREEN in RGB to Y conversion formula.
8:0	RW	0x000	csc_wgt_b2y Weight of BLUE in RGB to Y conversion formula.

VEPU_SRC_UDFU

Address: Operational Base + offset (0x0320)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:18	RW	0x000	csc_wgt_r2u Weight of RED in RGB to U conversion formula.
17:9	RW	0x000	csc_wgt_g2u Weight of GREEN in RGB to U conversion formula.
8:0	RW	0x000	csc_wgt_b2u Weight of BLUE in RGB to U conversion formula.

VEPU_SRC_UDFV

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Address: Operational Base + offset (0x0324)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:18	RW	0x000	csc_wgt_r2v Weight of RED in RGB to V conversion formula.
17:9	RW	0x000	csc_wgt_g2v Weight of GREEN in RGB to V conversion formula.
8:0	RW	0x000	csc_wgt_b2v Weight of BLUE in RGB to V conversion formula.

VEPU_SRC_UDFO

Address: Operational Base + offset (0x0328)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:16	RW	0x00	csc_ofst_y Offset of RGB to Y conversion formula.
15:8	RW	0x00	csc_ofst_u Offset of RGB to U conversion formula.
7:0	RW	0x00	csc_ofst_v Offset of RGB to V conversion formula.

VEPU_SRC_PROC

Address: Operational Base + offset (0x032C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:27	RW	0x0	src_rot Video source rotation mode. 2'h0: 0 degree 2'h1: Clockwise 90 degree 2'h2: Clockwise 180 degree 2'h3: Clockwise 270 degree
26	RW	0x0	src_mirr Video source mirror mode enable.
25:0	RO	0x0000000	reserved

VEPU_PIC_OFST

Address: Operational Base + offset (0x0330)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	pic_ofst_y Horizontal offset for encoding picture.
15:14	RO	0x0	reserved
13:0	RW	0x0000	pic_ofst_x Vertical offset for encoding picture.

VEPU_SRC_STRD0

Address: Operational Base + offset (0x0334)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
16:0	RW	0x00000	src_strd0 Video source stride0, based on pixel (byte). Note that if the video format is YUYV/UYVY/RGB/ARGB, src_strd0 is the only one component stride, if the video format is YUV420P/YUV420SP/YUV422P/YUV422SP, src_strd0 is the LUMA component stride. Note that if the video source is compressed by AFBC, src_strd0 is the header stride and it is 16-byte aligned.

VEPU_SRC_STRD1

Address: Operational Base + offset (0x0338)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	src_strd1 Chroma stride of video source, only for YUV format. Note that U and V stride must be the same when color format is YUV planar.

VEPU_RC_CFG

Address: Operational Base + offset (0x0350)

Bit	Attr	Reset Value	Description
31:12	RW	0x00000	rc_ctu_num RC adjustment intervals, base on CTU number.
11:3	RO	0x000	reserved
2	RW	0x0	aq_mode_hevc Mode of aq_delta calculation for CU32 and CU64. HEVC only. 1'b0: aq_delta of CU32/CU64 is calculated by corresponding MADI32/64; 1'b1: aq_delta of CU32/CU64 is calculated by corresponding 4/16 CU16 qp_deltas.
1	RW	0x0	aq_en Adaptive quantization enable.
0	RW	0x0	rc_en Rate control enable.

VEPU_RC_QP

Address: Operational Base + offset (0x0354)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	rc_min_qp Min QP for rate control and AQ mode.
25:20	RW	0x00	rc_max_qp Max QP for rate control and AQ mode.
19:16	RW	0x0	rc_qp_range QP adjust range(delta_qp) in rate control. Delta_qp is constrained between -rc_qp_range to rc_qp_range.
15:0	RO	0x0000	reserved

VEPU_RC_TGT

Address: Operational Base + offset (0x0358)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	ctu_ebit Target bit num for one 64x64 CTU(for HEVC) or one 16x16 MB(for H.264), with 1/16 precision.

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VEPU_SLI_SPLT

Address: Operational Base + offset (0x0360)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0000	sli_max_num_m1 Max slice num in one frame.
15	RW	0x0	sli_flsh Slice flush. Flush all the bit stream after each slice finished.
14:3	RO	0x000	reserved
2	RW	0x0	sli_splt_cpst Slice split compensation when slice is splited by byte. Byte distortion of current slice will be compensated in the next slice.
1	RW	0x0	sli_splt_mode Slice split mode. 1'h0: Slice splited by byte. 1'h1: Slice splited by number of MB(H.264)/CTU(HEVC).
0	RW	0x0	sli_splt Slice split enable.

VEPU_SLI_BYTE

Address: Operational Base + offset (0x0364)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sli_splt_byte Byte number for each slice when slice is splited by byte.

VEPU_SLI_CNUM

Address: Operational Base + offset (0x0368)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sli_splt_cnum_m1 Number of CTU/MB for slice split. Valid when slice is splited by CTU/MB.

VEPU_BS_PAD

Address: Operational Base + offset (0x036C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	bs_pad_len Bit stream padding length.
23:12	RW	0x000	bs_pad_gap The cyclic gaps between bistream paddings.
11:0	RW	0x000	bs_pad_gap0 The 1st gap before bistream padding.

VEPU_ME_RNGE

Address: Operational Base + offset (0x0370)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	dlt_frm_num reserved
15:12	RW	0x0	cime_srch_lftw CME left search range in 16 pixels. It values from 4 to 12, the typical value is 12.
11:8	RW	0x0	cime_srch_rgtw CME right search range in 16 pixels. It values from 4 to 12, the typical value is 12.

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	cime_srch_uph CME up search range in 8 pixels. It values from 4 to 14, the typical value is 14. Note that do not make it greater than 7 when encoding H.264 level 1 and 1b to make sure vertical Mv range is less than 64.
3:0	RW	0x0	cime_srch_dwnh CME down search range in 8 pixels. It values from 4 to 15, the typical value is 15. Note that do not make it greater than 7 when encoding H.264 level 1 and 1b to make sure vertical Mv range is less than 64.

VEPU_ME_CFG

Address: Operational Base + offset (0x0374)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RW	0x0	fme_dis reserved
27	RO	0x0	reserved
26:24	RW	0x0	rme_dis reserved
23:22	RW	0x0	rme_srch_v RME vertical search range, values from 0 to 3. The Typical value is 3.
21:20	RW	0x0	rme_srch_h RME horizontal search range, values from 0 to 3. The tyical value is 3.
19:7	RW	0x0000	cime_dist_thre CME Mv consistency threshold, values from 0 to 8191, typical value is 1024.
6:0	RW	0x00	srgn_max_num Size of internal reference picuture buffer in 16(width)x4(height). The typical value is 72.

VEPU_ME_CACH

Address: Operational Base + offset (0x0378)

Bit	Attr	Reset Value	Description
31	RW	0x0	colmv_load_hevc Load co-located Mvs as predicated Mv candidates, HEVC only.
30	RW	0x0	colmv_stor_hevc Store col-Mv information to external memory, HEVC only.
29:28	RW	0x0	fme_prefsu_en Fme hardware speedup.
27:18	RW	0x000	cme_linebuf_w The width of CIME down-sample recon data linebuf.
17:16	RO	0x0	reserved
15:11	RW	0x00	cime_hgt_rama Height of CME RAMA district, base on 4 pixels.
10	RO	0x0	reserved
9:0	RW	0x000	cime_size_rama CME's max RAM address.

VEPU_RDO_CFG_H264

Address: Operational Base + offset (0x03A0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29	RW	0x0	atr_mult_sel_e Atr multiplier selection enable.
28	RW	0x0	atf_e Intra mode anti-flicker enable.
27:22	RO	0x00	reserved
21:20	RW	0x0	scl_lst_sel Scale list selection. 2'h0: Flat scale list. 2'h1: Default scale list. 2'h2: User defined. 2'h3: Reserved.
19:16	RO	0x0	reserved
15	RW	0x0	atr_e Anti-ring enable.
14	RO	0x0	reserved
13	RW	0x0	ccwa_e Chroma cost weight adjustment(KLUT) enable.
12:5	RO	0x00	reserved
4	RW	0x0	chrm_spcl Chroma special candidates enable.
3	RW	0x0	vlc_lmt CAVLC syntax limit.
2:1	RO	0x0	reserved
0	RW	0x0	rect_size Limit sub_mb_rect_size for low level.

VEPU_RDO_MASK_MODE

Address: Operational Base + offset (0x03A4)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x000	rdo_mark_mode RDO mode mark. [0]: Skip mode mask. [1]: Inter16x16_t8 mode mask. [2]: Inter16x16_t4 mode mask. [3]: Inter8x8_t8 mode mask. [4]: Inter8x8_t4 mode mask. [5]: Intra16x16 mode mask. [6]: Intra8x8 mode mask. [7]: Intra4x4 mode mask. [8]: Inter4x4 mode mask.

VEPU_SYNT_NAL_H264

Address: Operational Base + offset (0x03B0)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:2	RW	0x00	nal_unit_type nal_unit_type
1:0	RW	0x0	nal_ref_idc nal_ref_idc

VEPU_SYNT_SPS_H264

Address: Operational Base + offset (0x03B4)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
10:9	RW	0x0	poc_type h264 picture order count type.
8:5	RW	0x0	mpoc_lm4 log2_max_pic_order_cnt_lsb_minus4
4	RW	0x0	drct_8x8 direct_8x8_inference_flag
3:0	RW	0x0	max_fnum log2_max_frame_num_minus4

VEPU_SYNT_PPS_H264

Address: Operational Base + offset (0x03B8)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	dbf_cp_flg deblocking_filter_control_present_flag
23	RO	0x0	reserved
22:18	RW	0x00	cr_ofst second_chroma_qp_index_offset
17:13	RW	0x00	cb_ofst chroma_qp_index_offset
12:7	RW	0x00	pic_init_qp pic_init_qp_minus26 + 26
6:5	RW	0x0	num_ref1_idx num_ref_idx_l1_active_minus1
4:3	RW	0x0	num_ref0_idx num_ref_idx_l0_active_minus1
2	RW	0x0	csip_flag constrained_intra_pred_flag
1	RW	0x0	trns_8x8 transform_8x8_mode_flag
0	RW	0x0	etpy_mode entropy_coding_mode_flag

VEPU_SYNT_SLI0_H264

Address: Operational Base + offset (0x03BC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	frm_num frame_num
15:14	RO	0x0	reserved
13:12	RW	0x0	cbc_init_idc cabac_init_idc
11	RW	0x0	num_ref_ovrd num_ref_idx_active_override_flag
10	RW	0x0	drct_smvp direct_spatial_mv_pred_flag
9:2	RW	0x00	pps_id pic_parameter_set_id
1:0	RW	0x0	sli_type slice_type: 0->P, 1->B, 2->I.

VEPU_SYNT_SLI1_H264

Address: Operational Base + offset (0x03C0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	poc_lsb pic_order_cnt_lsb

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	idr_pid idr_pic_id

VEPU_SYNT_SLI2_H264

Address: Operational Base + offset (0x03C4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	rodr_pic_num abs_diff_pic_num_minus1/long_term_pic_num
15:13	RO	0x0	reserved
12:11	RW	0x0	dis_dblk_idc disable_deblocking_filter_idc
10:7	RW	0x0	sli_alph_ofst slice_alpha_c0_offset_div2
6:3	RW	0x0	sli_beta_ofst slice_beta_offset_div2
2	RW	0x0	ref_list0_rodr ref_pic_list_reordering_flag_l0
1:0	RW	0x0	rodr_pic_idx reordering_of_pic_nums_idc

VEPU_SYNT_REFM0_H264

Address: Operational Base + offset (0x03C8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:26	RW	0x0	mmco_type2 memory_management_control_operation[2]
25:23	RW	0x0	mmco_type1 memory_management_control_operation[1]
22:7	RW	0x0000	mmco_parm0 MMCO parameters which have different meanings according to different mmco_parm0 valus. difference_of_pic_nums_minus1 for mmco_parm0 equals 0 or 3. long_term_pic_num for mmco_parm0 equals 2. long_term_frame_idx for mmco_parm0 equals 6. max_long_term_frame_idx_plus1 for mmco_parm0 equals 4.
6:4	RW	0x0	mmco_type0 memory_management_control_operation
3	RW	0x0	mmco4_pre A No.4 MMCO should be executed firstly if mmo4_pre is 1
2	RW	0x0	arpm_flg adaptive_ref_pic_marking_mode_flag
1	RW	0x0	ltrf_flg long_term_reference_flag
0	RW	0x0	nopp_flg no_output_of_prior_pics_flag

VEPU_SYNT_REFM1_H264

Address: Operational Base + offset (0x03CC)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mmco_parm2 MMCO parameters which have different meanings according to different mmco_parm2 valus. difference_of_pic_nums_minus1 for mmco_parm2 equals 0 or 3. long_term_pic_num for mmco_parm2 equals 2. long_term_frame_idx for mmco_parm2 equals 6. max_long_term_frame_idx_plus1 for mmco_parm2 equals 4.
15:0	RW	0x0000	mmco_parm1 MMCO parameters which have different meanings according to different mmco_parm1 valus. difference_of_pic_nums_minus1 for mmco_parm1 equals 0 or 3. long_term_pic_num for mmco_parm1 equals 2. long_term_frame_idx for mmco_parm1 equals 6. max_long_term_frame_idx_plus1 for mmco_parm1 equals 4.

VEPU_SYNT_REFM2_H264

Address: Operational Base + offset (0x03D0)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	long_term_frame_idx2 long_term_frame_idx[2] (when mmco equal 3)
7:4	RW	0x0	long_term_frame_idx1 long_term_frame_idx[1] (when mmco equal 3)
3:0	RW	0x0	long_term_frame_idx0 long_term_frame_idx[0] (when mmco equal 3)

VEPU_H264_MV_LMT

Address: Operational Base + offset (0x03F0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	mv_v_lmt_en According the profile, motion vector limit enable.
14	RO	0x0	reserved
13:0	RW	0x0000	mv_v_lmt_thd According the profile, motion vector limit (by level) , H.264 only, based on 1 pixel.

VEPU_ADR_BSBT_JPEG

Address: Operational Base + offset (0x0400)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	bsbt_addr_jpeg High 25 bits top address of JPEG bit stream buffer.
7:0	RO	0x00	reserved

VEPU_ADR_BSBB_JPEG

Address: Operational Base + offset (0x0404)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	bsbb_addr_jpeg High 25 bits bottom address of JPEG bit stream buffer.
7:0	RO	0x00	reserved

VEPU_ADR_BSBS_JPEG

Address: Operational Base + offset (0x0408)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	adr_bsbs_jpeg Start address of JPEG bit stream buffer. VEPU begins to write bit stream from this address and increase address automatically. Note that the VEPU's real-time write address is marked in JPEG_BSB_STUS.

VEPU_ADR_BSBR_JPEG

Address: Operational Base + offset (0x040C)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	bsbr_addr_jpeg Read address of JPEG bit stream buffer, 128B aligned. VEPU will pause when write address meets read address and then send an interrupt. SW should move some data out from bit stream buffer and change this register accordingly. After that VEPU will continue processing automatically.
7:4	RO	0x0	reserved
3:0	RW	0x0	bsadr_msk_jpeg Mask of JPEG bit stream buffer address. [0]: wptr_bsw badr mask; [1]: rptr_bsw badr mask; [2]: bot_bsw badr mask; [3]: top_bsw badr mask;

VEPU_ADR_VSY_B_JPEG

Address: Operational Base + offset (0x0410)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	adr_vsy_b_jpeg Bottom address of luma JPEG source buffer
3:0	RO	0x0	reserved

VEPU_ADR_VSC_B_JPEG

Address: Operational Base + offset (0x0414)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	adr_vsc_b_jpeg Bottom address of chroma JPEG source buffer
3:0	RO	0x0	reserved

VEPU_ADR_VSY_T_JPEG

Address: Operational Base + offset (0x0418)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	adr_vsy_t_jpeg Top address of Luma JPEG source buffer
3:0	RO	0x0	reserved

VEPU_ADR_VSC_T_JPEG

Address: Operational Base + offset (0x041C)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	adr_vsc_t_jpeg Top address of Chroma JPEG source buffer
3:0	RO	0x0	reserved

VEPU_ADR_SRC0_JPEG

Address: Operational Base + offset (0x0420)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	adr_src0_jpeg Base address of the 1st storage area for video source, based on byte. ARGB8888, BGR888, RGB565, YUYV422 and UYUV422 have only one storage area, while adr_src0 is configured as the base address of video source frame buffer. YUV422/420 semi-planar have 2 storage area, while adr_src0 is configured as the base address of Y frame buffer. YUV422/420 planar have 3 storage area, while adr_src0 is configured as the base address of Y frame buffer. Note that if the video source is compressed by AFBC, adr_src0 is configured as the base address of header buffer, and it is 16-byte aligned.

VEPU_ADR_SRC1_JPEG

Address: Operational Base + offset (0x0424)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	adr_src1_jpeg Base address of the 2nd storage area for video source. ARGB8888, BGR888, RGB565, YUYV422 and UYUV422 have only one storage area, while adr_src1 is reserved. YUV422/420 semi-planar have 2 storage area, while adr_src1 is configured as the base address of CHROMA frame buffer. YUV422/420 planar have 3 storage area, while adr_src1 is configured as the base address of U frame buffer. Note that if the video source is compressed by AFBC, adr_src1 is configured as the base address of body buffer.

VEPU_ADR_SRC2_JPEG

Address: Operational Base + offset (0x0428)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	adr_src2_jpeg Base address of V frame buffer when video source is uncompress and color format is YUV422/420 planar.

VEPU_BSP_SIZE_JPEG

Address: Operational Base + offset (0x042C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	bsp_size_jpeg Set the bit stream packet size of jpeg, 0 is disable.

VEPU_ENC_RSL_JPEG

Address: Operational Base + offset (0x0440)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	pic_hd8_m1_jpeg Ceil(encoding picture height/8) -1
15:11	RO	0x00	reserved
10:0	RW	0x000	pic_wd8_m1_jpeg Ceil(encoding picture width/8) -1

VEPU_SRC_FILL_JPEG

Address: Operational Base + offset (0x0444)

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Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x00	pic_hfill_jpeg Filling pixels to keep (encoding) picture height is 8 pixels aligned for HEVC and 16 pixels aligned for H.264.
15:6	RO	0x000	reserved
5:0	RW	0x00	pic_wfill_jpeg Filling pixels to keep (encoding) picture width is 8 pixels aligned for HEVC and 16 pixels aligned for H.264.

VEPU_SRC_FMT_JPEG

Address: Operational Base + offset (0x0448)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10	RW	0x0	chroma_ds_mode_jpeg Chroma down sample filter. 1'b0: interpolation chroma down sample. 1'b1: decimation chroma down sample.
9	RW	0x0	src_range_trns_sel_jpeg Video source full range and limit range conversion mode. 1'b0: full range to limit range. 1'b1: limit range to full range.
8	RW	0x0	src_range_trns_en_jpeg Video Source range conversion enable.
7	RW	0x0	out_fmt_jpeg The color format of output from preprocess. 1'h0: YUV400; 1'h1: YUV420;
6	RO	0x0	reserved
5:2	RW	0x0	src_cfmt_jpeg Video source color format. 4'h0: BGRA8888 4'h1: RGB888 4'h2: RGB565 4'h4: YUV422SP 4'h5: YUV422P 4'h6: YUV420SP 4'h7: YUV420P 4'h8: YUYV422 4'h9: UYVY422 4'ha: YUV400 4'hc: YUV444SP 4'hd: YUV444P Others: Reserved
1	RW	0x0	rbuv_swap_jpeg Swap the position of R and B for BGRA8888, RGB888, RGB 656 format; Swap the position of U and V for YUV422-SP, YUV420-SP, YUYV422 and UYUV422 format. 1'h0: RGB or YUYV or UYVY. 1'h1: BGR or YVYU or VYUY.
0	RW	0x0	alpha_swap_jpeg Swap the position of alpha and RGB for ARBG8888. 1'h0: BGRA8888 or RGBA8888. 1'h1: ABGR8888 or ARGB8888.

VEPU_SRC_UDFY_JPEG

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Address: Operational Base + offset (0x044C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:18	RW	0x000	csc_wgt_r2y_jpeg Weight of RED in RGB to Y conversion formula.
17:9	RW	0x000	csc_wgt_g2y_jpeg Weight of GREEN in RGB to Y conversion formula.
8:0	RW	0x000	csc_wgt_b2y_jpeg Weight of BLUE in RGB to Y conversion formula.

VEPU_SRC_UDFU_JPEG

Address: Operational Base + offset (0x0450)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:18	RW	0x000	csc_wgt_r2u_jpeg Weight of RED in RGB to U conversion formula.
17:9	RW	0x000	csc_wgt_g2u_jpeg Weight of GREEN in RGB to U conversion formula.
8:0	RW	0x000	csc_wgt_b2u_jpeg Weight of BLUE in RGB to U conversion formula.

VEPU_SRC_UDFV_JPEG

Address: Operational Base + offset (0x0454)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:18	RW	0x000	csc_wgt_r2v_jpeg Weight of RED in RGB to V conversion formula.
17:9	RW	0x000	csc_wgt_g2v_jpeg Weight of GREEN in RGB to V conversion formula.
8:0	RW	0x000	csc_wgt_b2v_jpeg Weight of BLUE in RGB to V conversion formula.

VEPU_SRC_UDFO_JPEG

Address: Operational Base + offset (0x0458)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:16	RW	0x00	csc_ofst_y_jpeg Offset of RGB to Y conversion formula.
15:8	RW	0x00	csc_ofst_u_jpeg Offset of RGB to U conversion formula.
7:0	RW	0x00	csc_ofst_v_jpeg Offset of RGB to V conversion formula.

VEPU_SRC_PROC_JPEG

Address: Operational Base + offset (0x045C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:27	RW	0x0	src_rot_jpeg Video source rotation mode. 2'h0: 0 degree 2'h1: Clockwise 90 degree 2'h2: Clockwise 180 degree 2'h3: Clockwise 270 degree
26	RW	0x0	src_mirr_jpeg Video source mirror mode enable.
25:0	RO	0x0000000	reserved

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VEPU_PIC_OFST_JPEG

Address: Operational Base + offset (0x0460)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	pic_ofst_y_jpeg Horizontal offset for encoding picture.
15:14	RO	0x0	reserved
13:0	RW	0x0000	pic_ofst_x_jpeg Vertical offset for encoding picture.

VEPU_SRC_STRD0_JPEG

Address: Operational Base + offset (0x0464)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RW	0x00000	src_strd0_jpeg Video source stride0, based on pixel (byte). Note that if the video format is YUYV/UYVY/RGB/ARGB, src_strd0 is the only one component stride, if the video format is YUV420P/YUV420SP/YUV422P/YUV422SP, src_strd0 is the LUMA component stride. Note that if the video source is compressed by AFBC, src_strd0 is the header stride and it is 16-byte aligned.

VEPU_SRC_STRD1_JPEG

Address: Operational Base + offset (0x0468)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	src_strd1_jpeg CHROMA stride of video source, only for YUV format. Note that U and V stride must be the same when color format is YUV planar.

VEPU_JPEG_Y_CFG

Address: Operational Base + offset (0x0470)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	jpeg_bias_y Quantization bias of JPEG Y component.

VEPU_JPEG_U_CFG

Address: Operational Base + offset (0x0474)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	jpeg_bias_u Quantization bias of JPEG U component.

VEPU_JPEG_V_CFG

Address: Operational Base + offset (0x0478)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	jpeg_bias_v Quantization bias of JPEG V component.

VEPU_JPEG_BASE_CFG

Address: Operational Base + offset (0x047C)

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Bit	Attr	Reset Value	Description
31	RW	0x0	jpeg_stnd JPEG standard. 1'h0: JPEG disable 1'h1: JPEG enable
30	RW	0x0	jpeg_slen_fifo JPEG slice length fifo enable.
29	RW	0x0	jpeg_pic_last_ecs Send EOI at the tail of bitstream.
28:26	RW	0x0	jpeg_start_rst_m The first JPEG restart counter(RSTm).
25	RW	0x0	jpeg_out_mode JPEG bitstream output mode. 1'b0: Frame flush. 1'b1: ECS flush for low delay.
24:0	RW	0x0000000	jpeg_ri JPEG restart interval size in MCU.

VEPU_JPEG_BS_PART

Address: Operational Base + offset (0x0480)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	uvc_skip_len_jpeg Length of the Gap between each JPEG Bit Stream Partitions.
23:12	RW	0x000	uvc_partition_len_jpeg Length of the subsequent JPEG Bit Stream partitions.
11:0	RW	0x000	uvc_partition0_len_jpeg Length of the 1st JPEG Bit Stream partition.

VEPU_RC_ADJ0

Address: Operational Base + offset (0x1000)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:20	RW	0x00	qp_adj4 QP adjust step4 for rate control. It's a signed number and the valid value is from -16 to 15.
19:15	RW	0x00	qp_adj3 QP adjust step3 for rate control. It's a signed number and the valid value is from -16 to 15.
14:10	RW	0x00	qp_adj2 QP adjust step2 for rate control. It's a signed number and the valid value is from -16 to 15.
9:5	RW	0x00	qp_adj1 QP adjust step1 for rate control. It's a signed number and the valid value is from -16 to 15.
4:0	RW	0x00	qp_adj0 QP adjust step0 for rate control. It's a signed number and the valid value is from -16 to 15.

VEPU_RC_ADJ1

Address: Operational Base + offset (0x1004)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:15	RW	0x00	qp_adj8 QP adjust step8 for rate control. It's a signed number and the valid value is from -16 to 15.

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Bit	Attr	Reset Value	Description
14:10	RW	0x00	qp_adj7 QP adjust step7 for rate control. It's a signed number and the valid value is from -16 to 15.
9:5	RW	0x00	qp_adj6 QP adjust step6 for rate control. It's a signed number and the valid value is from -16 to 15.
4:0	RW	0x00	qp_adj5 QP adjust step5 for rate control. It's a signed number and the valid value is from -16 to 15.

VEPU_RC_DTHD0

Address: Operational Base + offset (0x1008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rc_dthd0 Bits rate deviation threshold0.

VEPU_RC_DTHD1

Address: Operational Base + offset (0x100C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rc_dthd1 Bits rate deviation threshold1.

VEPU_RC_DTHD2

Address: Operational Base + offset (0x1010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rc_dthd2 Bits rate deviation threshold2.

VEPU_RC_DTHD3

Address: Operational Base + offset (0x1014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rc_dthd3 Bits rate deviation threshold3.

VEPU_RC_DTHD4

Address: Operational Base + offset (0x1018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rc_dthd4 Bits rate deviation threshold4.

VEPU_RC_DTHD5

Address: Operational Base + offset (0x101C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rc_dthd5 Bits rate deviation threshold5.

VEPU_RC_DTHD6

Address: Operational Base + offset (0x1020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rc_dthd6 Bits rate deviation threshold6.

VEPU_RC_DTHD7

Address: Operational Base + offset (0x1024)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rc_dthd7 Bits rate deviation threshold7.

VEPU_RC_DTHD8

Address: Operational Base + offset (0x1028)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rc_dthd8 Bits rate deviation threshold8.

VEPU_ROI_QTHD0

Address: Operational Base + offset (0x1030)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	qpmin_area2 Min QP for 16x16 CU inside ROI area2.
23:18	RW	0x00	qpmax_area1 Max QP for 16x16 CU inside ROI area1.
17:12	RW	0x00	qpmin_area1 Min QP for 16x16 CU inside ROI area1.
11:6	RW	0x00	qpmax_area0 Max QP for 16x16 CU inside ROI area0.
5:0	RW	0x00	qpmin_area0 Min QP for 16x16 CU inside ROI area0.

VEPU_ROI_QTHD1

Address: Operational Base + offset (0x1034)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	qpmax_area4 Max QP for 16x16 CU inside ROI area4.
23:18	RW	0x00	qpmin_area4 Min QP for 16x16 CU inside ROI area4.
17:12	RW	0x00	qpmax_area3 Max QP for 16x16 CU inside ROI area3.
11:6	RW	0x00	qpmin_area3 Min QP for 16x16 CU inside ROI area3.
5:0	RW	0x00	qpmax_area2 Max QP for 16x16 CU inside ROI area2.

VEPU_ROI_QTHD2

Address: Operational Base + offset (0x1038)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	qpmin_area7 Min QP for 16x16 CU inside ROI area7.
23:18	RW	0x00	qpmax_area6 Max QP for 16x16 CU inside ROI area6.
17:12	RW	0x00	qpmin_area6 Min QP for 16x16 CU inside ROI area6.
11:6	RW	0x00	qpmax_area5 Max QP for 16x16 CU inside ROI area5.
5:0	RW	0x00	qpmin_area5 Min QP for 16x16 CU inside ROI area5.

VEPU_ROI_QTHD3

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Address: Operational Base + offset (0x103C)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	qpmap_mode QP theshold generation for the CUs whose size is bigger than 16x16. 2'h0: Mean value of 16x16 CU QP thesholds 2'h1: Max value of 16x16 CU QP thesholds 2'h2: Min value of 16x16 CU QP thesholds 2'h3: Reserved
29:6	RO	0x000000	reserved
5:0	RW	0x00	qpmax_area7 Max QP for 16x16 CU inside ROI area7.

VEPU_AQ_TTHD0

Address: Operational Base + offset (0x1044)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	aq_tthd3 Texture threshold3 for adaptive QP adjustment.
23:16	RW	0x00	aq_tthd2 Texture threshold2 for adaptive QP adjustment.
15:8	RW	0x00	aq_tthd1 Texture threshold1 for adaptive QP adjustment.
7:0	RW	0x00	aq_tthd0 Texture threshold0 for adaptive QP adjustment.

VEPU_AQ_TTHD1

Address: Operational Base + offset (0x1048)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	aq_tthd7 Texture threshold7 for adaptive QP adjustment.
23:16	RW	0x00	aq_tthd6 Texture threshold6 for adaptive QP adjustment.
15:8	RW	0x00	aq_tthd5 Texture threshold5 for adaptive QP adjustment.
7:0	RW	0x00	aq_tthd4 Texture threshold4 for adaptive QP adjustment.

VEPU_AQ_TTHD2

Address: Operational Base + offset (0x104C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	aq_tthd11 Texture threshold11 for adaptive QP adjustment.
23:16	RW	0x00	aq_tthd10 Texture threshold10 for adaptive QP adjustment.
15:8	RW	0x00	aq_tthd9 Texture threshold9 for adaptive QP adjustment.
7:0	RW	0x00	aq_tthd8 Texture threshold8 for adaptive QP adjustment.

VEPU_AQ_TTHD3

Address: Operational Base + offset (0x1050)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	aq_tthd15 Texture threshold15 for adaptive QP adjustment.
23:16	RW	0x00	aq_tthd14 Texture threshold14 for adaptive QP adjustment.

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	aq_tthd13 Texture threshold13 for adaptive QP adjustment.
7:0	RW	0x00	aq_tthd12 Texture threshold12 for adaptive QP adjustment.

VEPU_AQ_STP0

Address: Operational Base + offset (0x1054)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	aq_stp_2t3 QP adjust step when current texture strength >= aq_tthd2 and < aq_tthd3. It's a signed number and the valid value is from -32 to 31.
23:22	RO	0x0	reserved
21:16	RW	0x00	aq_stp_1t2 QP adjust step when current texture strength >= aq_tthd1 and < aq_tthd2. It's a signed number and the valid value is from -32 to 31.
15:14	RO	0x0	reserved
13:8	RW	0x00	aq_stp_0t1 QP adjust step when current texture strength >= aq_tthd0 and < aq_tthd1. It's a signed number and the valid value is from -32 to 31.
7:6	RO	0x0	reserved
5:0	RW	0x00	aq_stp_s0 QP adjust step when current texture strength < aq_tthd0. It's a signed number and the valid value is from -32 to 31.

VEPU_AQ_STP1

Address: Operational Base + offset (0x1058)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	aq_stp_6t7 QP adjust step when current texture strength >= aq_tthd6 and < aq_tthd7. It's a signed number and the valid value is from -32 to 31.
23:22	RO	0x0	reserved
21:16	RW	0x00	aq_stp_5t6 QP adjust step when current texture strength >= aq_tthd5 and < aq_tthd6. It's a signed number and the valid value is from -32 to 31.
15:14	RO	0x0	reserved
13:8	RW	0x00	aq_stp_4t5 QP adjust step when current texture strength >= aq_tthd4 and < aq_tthd5. It's a signed number and the valid value is from -32 to 31.
7:6	RO	0x0	reserved
5:0	RW	0x00	aq_stp_3t4 QP adjust step when current texture strength >= aq_tthd3 and < aq_tthd4. It's a signed number and the valid value is from -32 to 31.

VEPU_AQ_STP2

Address: Operational Base + offset (0x105C)

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Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	aq_stp_11t12 QP adjust step when current texture strength > aq_tthd11 and <= aq_tthd12. It's a signed number and the valid value is from -32 to 31.
23:22	RO	0x0	reserved
21:16	RW	0x00	aq_stp_10t11 QP adjust step when current texture strength > aq_tthd10 and <= aq_tthd11. It's a signed number and the valid value is from -32 to 31.
15:14	RO	0x0	reserved
13:8	RW	0x00	aq_stp_9t10 QP adjust step when current texture strength > aq_tthd9 and <= aq_tthd10. It's a signed number and the valid value is from -32 to 31.
7:6	RO	0x0	reserved
5:0	RW	0x00	aq_stp_8t9 QP adjust step when current texture strength > aq_tthd8 and <= aq_tthd9. It's a signed number and the valid value is from -32 to 31.

VEPU_AQ_STP3

Address: Operational Base + offset (0x1060)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	aq_stp_b15 QP adjust step when current texture strength > aq_tthd15. It's a signed number and the valid value is from -32 to 31.
23:22	RO	0x0	reserved
21:16	RW	0x00	aq_stp_14t15 QP adjust step when current texture strength > aq_tthd14 and <= aq_tthd15. It's a signed number and the valid value is from -32 to 31.
15:14	RO	0x0	reserved
13:8	RW	0x00	aq_stp_13t14 QP adjust step when current texture strength > aq_tthd13 and <= aq_tthd14. It's a signed number and the valid value is from -32 to 31.
7:6	RO	0x0	reserved
5:0	RW	0x00	aq_stp_12t13 QP adjust step when current texture strength > aq_tthd12 and <= aq_tthd13. It's a signed number and the valid value is from -32 to 31.

VEPU_MADI_ST_THD

Address: Operational Base + offset (0x1064)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	madi_th2 The 3rd threshold for MADI statistics.
15:8	RW	0x00	madi_th1 The 2nd threshold for MADI statistics.
7:0	RW	0x00	madi_th0 The 1st threshold for MADI statistics.

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VEPU_MADP_ST_THD0

Address: Operational Base + offset (0x1068)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	madp_th1 The 2nd threshold for MADP statistics.
15:12	RO	0x0	reserved
11:0	RW	0x000	madp_th0 The 1st threshold for MADP statistics.

VEPU_MADP_ST_THD1

Address: Operational Base + offset (0x106C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	madp_th2 The 3rd threshold for MADP statistics.

VEPU_KLUT_OFST

Address: Operational Base + offset (0x107C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RW	0x00	inter_chrm_dist_multi_hevc Inter Chroma no residual mode decision weight.
7:4	RO	0x0	reserved
3:0	RW	0x0	chrm_klut_ofst Offset of (RDO) chroma cost weight table, values from 0 to 6.

VEPU_FMDC_ADJ0

Address: Operational Base + offset (0x1080)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	fmdc_adj_pri Priority of frame level mode decision adjustment.
23:12	RO	0x000	reserved
11:8	RW	0x0	fmdc_adju_intra16 Frame level mode decision adjustment for intra16x16.
7:4	RW	0x0	fmdc_adju_skip16 Frame level mode decision adjustment for skip16x16.
3:0	RW	0x0	fmdc_adju_inter16 Frame level mode decision adjustment for inter16x16.

VEPU_BMAP_CFG

Address: Operational Base + offset (0x108C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:12	RW	0x00	bmap_qpmax Block Mapping ROI Max QP.
11:6	RW	0x00	bmap_qpmin Block Mapping ROI Min QP.
5:1	RW	0x00	bmap_pri Block Mapping ROI priority.
0	RW	0x0	bmap_en Block Mapping ROI enable

VEPU_ROI0_POS_LT

Address: Operational Base + offset (0x1090)

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Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	roi0_lt_y Y ordiante of the left top of ROI region0
15:10	RO	0x00	reserved
9:0	RW	0x000	roi0_lt_x X ordiante of the left top of ROI region0

VEPU_ROI0_POS_RB

Address: Operational Base + offset (0x1094)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	roi0_rb_y Y ordiante of the right bottom of ROI region0
15:10	RO	0x00	reserved
9:0	RW	0x000	roi0_rb_x X ordiante of the right bottom of ROI region0

VEPU_ROI0_BASE

Address: Operational Base + offset (0x1098)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RW	0x0	roi0_en ROI region0 enable.
12:8	RW	0x00	roi0_pri ROI region0 priority.
7	RW	0x0	roi0_qp_adj_mode ROI region0 QP adjustment mode. 1'b0: relative QP adjustment. 1'b1: absolute QP adjustment.
6:0	RW	0x00	roi0_qp_value ROI region0 QP adjust value.

VEPU_ROI0_MDC

Address: Operational Base + offset (0x109C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	roi0_mdc_intra16 ROI region0 mode decision adjust for intra16x16.
7:4	RW	0x0	roi0_mdc_skip16 ROI region0 mode decision adjust for skip16x16.
3:0	RW	0x0	roi0_mdc_inter16 ROI region0 mode decision adjust for inter16x16.

VEPU_ROI1_POS_LT

Address: Operational Base + offset (0x10A0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	roi1_lt_y Y ordiante of the left top of ROI region1
15:10	RO	0x00	reserved
9:0	RW	0x000	roi1_lt_x X ordiante of the left top of ROI region1

VEPU_ROI1_POS_RB

Address: Operational Base + offset (0x10A4)

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Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	roi1_rb_y Y ordiante of the right bottom of ROI region1
15:10	RO	0x00	reserved
9:0	RW	0x000	roi1_rb_x X ordiante of the right bottom of ROI region1

VEPU_ROI1_BASE

Address: Operational Base + offset (0x10A8)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RW	0x0	roi1_en ROI region1 enable.
12:8	RW	0x00	roi1_pri ROI region1 priority.
7	RW	0x0	roi1_qp_adj_mode ROI region1 QP adjustment mode. 1'b0: relative QP adjustment. 1'b1: absolute QP adjustment.
6:0	RW	0x00	roi1_qp_value ROI region1 QP adjust value.

VEPU_ROI1_MDC

Address: Operational Base + offset (0x10AC)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	roi1_mdc_intra16 ROI region1 mode decision adjust for intra16x16.
7:4	RW	0x0	roi1_mdc_skip16 ROI region1 mode decision adjust for skip16x16.
3:0	RW	0x0	roi1_mdc_inter16 ROI region1 mode decision adjust for inter16x16.

VEPU_ROI2_POS_LT

Address: Operational Base + offset (0x10B0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	roi2_lt_y Y ordiante of the left top of ROI region2
15:10	RO	0x00	reserved
9:0	RW	0x000	roi2_lt_x X ordiante of the left top of ROI region2

VEPU_ROI2_POS_RB

Address: Operational Base + offset (0x10B4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	roi2_rb_y Y ordiante of the right bottom of ROI region2
15:10	RO	0x00	reserved
9:0	RW	0x000	roi2_rb_x X ordiante of the right bottom of ROI region2

VEPU_ROI2_BASE

Address: Operational Base + offset (0x10B8)

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Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RW	0x0	roi2_en ROI region2 enable.
12:8	RW	0x00	roi2_pri ROI region2 priority.
7	RW	0x0	roi2_qp_adj_mode ROI region2 QP adjustment mode. 1'b0: relative QP adjustment. 1'b1: absolute QP adjustment.
6:0	RW	0x00	roi2_qp_value ROI region2 QP adjust value.

VEPU_ROI2_MDC

Address: Operational Base + offset (0x10BC)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	roi2_mdc_intra16 ROI region2 mode decision adjust for intra16x16.
7:4	RW	0x0	roi2_mdc_skip16 ROI region2 mode decision adjust for skip16x16.
3:0	RW	0x0	roi2_mdc_inter16 ROI region2 mode decision adjust for inter16x16.

VEPU_ROI3_POS_LT

Address: Operational Base + offset (0x10C0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	roi3_lt_y Y ordiante of the left top of ROI region3
15:10	RO	0x00	reserved
9:0	RW	0x000	roi3_lt_x X ordiante of the left top of ROI region3

VEPU_ROI3_POS_RB

Address: Operational Base + offset (0x10C4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	roi3_rb_y Y ordiante of the right bottom of ROI region3
15:10	RO	0x00	reserved
9:0	RW	0x000	roi3_rb_x X ordiante of the right bottom of ROI region3

VEPU_ROI3_BASE

Address: Operational Base + offset (0x10C8)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RW	0x0	roi3_en ROI region3 enable.
12:8	RW	0x00	roi3_pri ROI region3 priority.
7	RW	0x0	roi3_qp_adj_mode ROI region3 QP adjustment mode. 1'b0: relative QP adjustment. 1'b1: absolute QP adjustment.

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Bit	Attr	Reset Value	Description
6:0	RW	0x00	roi3_qp_value ROI region3 QP adjust value.

VEPU_ROI3_MDC

Address: Operational Base + offset (0x10CC)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	roi3_mdc_intra16 ROI region3 mode decision adjust for intra16x16.
7:4	RW	0x0	roi3_mdc_skip16 ROI region3 mode decision adjust for skip16x16.
3:0	RW	0x0	roi3_mdc_inter16 ROI region3 mode decision adjust for inter16x16.

VEPU_ROI4_POS_LT

Address: Operational Base + offset (0x10D0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	roi4_lt_y Y ordiante of the left top of ROI region4
15:10	RO	0x00	reserved
9:0	RW	0x000	roi4_lt_x X ordiante of the left top of ROI region4

VEPU_ROI4_POS_RB

Address: Operational Base + offset (0x10D4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	roi4_rb_y Y ordiante of the right bottom of ROI region4
15:10	RO	0x00	reserved
9:0	RW	0x000	roi4_rb_x X ordiante of the right bottom of ROI region4

VEPU_ROI4_BASE

Address: Operational Base + offset (0x10D8)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RW	0x0	roi4_en ROI region4 enable.
12:8	RW	0x00	roi4_pri ROI region4 priority.
7	RW	0x0	roi4_qp_adj_mode ROI region4 QP adjustment mode. 1'b0: relative QP adjustment. 1'b1: absolute QP adjustment.
6:0	RW	0x00	roi4_qp_value ROI region4 QP adjust value.

VEPU_ROI4_MDC

Address: Operational Base + offset (0x10DC)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	roi4_mdc_intra16 ROI region4 mode decision adjust for intra16x16.

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	roi4_mdc_skip16 ROI region4 mode decision adjust for skip16x16.
3:0	RW	0x0	roi4_mdc_inter16 ROI region4 mode decision adjust for inter16x16.

VEPU_ROI5_POS_LT

Address: Operational Base + offset (0x10E0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	roi5_lt_y Y ordiante of the left top of ROI region5
15:10	RO	0x00	reserved
9:0	RW	0x000	roi5_lt_x X ordiante of the left top of ROI region5

VEPU_ROI5_POS_RB

Address: Operational Base + offset (0x10E4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	roi5_rb_y Y ordiante of the right bottom of ROI region5
15:10	RO	0x00	reserved
9:0	RW	0x000	roi5_rb_x X ordiante of the right bottom of ROI region5

VEPU_ROI5_BASE

Address: Operational Base + offset (0x10E8)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RW	0x0	roi5_en ROI region5 enable.
12:8	RW	0x00	roi5_pri ROI region5 priority.
7	RW	0x0	roi5_qp_adj_mode ROI region5 QP adjustment mode. 1'b0: relative QP adjustment. 1'b1: absolute QP adjustment.
6:0	RW	0x00	roi5_qp_value ROI region5 QP adjust value.

VEPU_ROI5_MDC

Address: Operational Base + offset (0x10EC)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	roi5_mdc_intra16 ROI region5 mode decision adjust for intra16x16.
7:4	RW	0x0	roi5_mdc_skip16 ROI region5 mode decision adjust for skip16x16.
3:0	RW	0x0	roi5_mdc_inter16 ROI region5 mode decision adjust for inter16x16.

VEPU_ROI6_POS_LT

Address: Operational Base + offset (0x10F0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RW	0x000	roi6_lt_y Y ordiante of the left top of ROI region6
15:10	RO	0x00	reserved
9:0	RW	0x000	roi6_lt_x X ordiante of the left top of ROI region6

VEPU_ROI6_POS_RB

Address: Operational Base + offset (0x10F4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	roi6_rb_y Y ordiante of the right bottom of ROI region6
15:10	RO	0x00	reserved
9:0	RW	0x000	roi6_rb_x X ordiante of the right bottom of ROI region6

VEPU_ROI6_BASE

Address: Operational Base + offset (0x10F8)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RW	0x0	roi6_en ROI region6 enable.
12:8	RW	0x00	roi6_pri ROI region6 priority.
7	RW	0x0	roi6_qp_adj_mode ROI region6 QP adjustment mode. 1'b0: relative QP adjustment. 1'b1: absolute QP adjustment.
6:0	RW	0x00	roi6_qp_value ROI region6 QP adjust value.

VEPU_ROI6_MDC

Address: Operational Base + offset (0x10FC)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	roi6_mdc_intra16 ROI region6 mode decision adjust for intra16x16.
7:4	RW	0x0	roi6_mdc_skip16 ROI region6 mode decision adjust for skip16x16.
3:0	RW	0x0	roi6_mdc_inter16 ROI region6 mode decision adjust for inter16x16.

VEPU_ROI7_POS_LT

Address: Operational Base + offset (0x1100)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	roi7_lt_y Y ordiante of the left top of ROI region7
15:10	RO	0x00	reserved
9:0	RW	0x000	roi7_lt_x X ordiante of the left top of ROI region7

VEPU_ROI7_POS_RB

Address: Operational Base + offset (0x1104)

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Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	roi7_rb_y Y ordiante of the right bottom of ROI region7
15:10	RO	0x00	reserved
9:0	RW	0x000	roi7_rb_x X ordiante of the right bottom of ROI region7

VEPU_ROI7_BASE

Address: Operational Base + offset (0x1108)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RW	0x0	roi7_en ROI region7 enable.
12:8	RW	0x00	roi7_pri ROI region6 priority.
7	RW	0x0	roi7_qp_adj_mode ROI region7 QP adjustment mode. 1'b0: relative QP adjustment. 1'b1: absolute QP adjustment.
6:0	RW	0x00	roi7_qp_value ROI region7 QP adjust value.

VEPU_ROI7_MDC

Address: Operational Base + offset (0x110C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	roi7_mdc_intra16 ROI region7 mode decision adjust for intra16x16.
7:4	RW	0x0	roi7_mdc_skip16 ROI region7 mode decision adjust for skip16x16.
3:0	RW	0x0	roi7_mdc_inter16 ROI region7 mode decision adjust for inter16x16.

VEPU_IPRD_TTHDY4_0_H264

Address: Operational Base + offset (0x1700)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	iprd_tthdy4_1 The 2nd texture threshold for H.264 LUMA 4x4 intra prediction.
15:12	RO	0x0	reserved
11:0	RW	0x000	iprd_tthdy4_0 The 1st texture threshold for H.264 LUMA 4x4 intra prediction.

VEPU_IPRD_TTHDY4_1_H264

Address: Operational Base + offset (0x1704)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	iprd_tthdy4_3 The 4th texture threshold for H.264 LUMA 4x4 intra prediction.
15:12	RO	0x0	reserved
11:0	RW	0x000	iprd_tthdy4_2 The 3rd texture threshold for H.264 LUMA 4x4 intra prediction.

VEPU_IPRD_TTHDC8_0_H264

Address: Operational Base + offset (0x1708)

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Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	iprd_tthdc8_1 The 2nd texture threshold for H.264 CHROMA 8x8 intra prediction.
15:12	RO	0x0	reserved
11:0	RW	0x000	iprd_tthdc8_0 The 1st texture threshold for H.264 CHROMA 8x8 intra prediction.

VEPU_IPRD_TTHDC8_1_H264

Address: Operational Base + offset (0x170C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	iprd_tthdc8_3 The 4th texture threshold for H.264 CHROMA 8x8 intra prediction.
15:12	RO	0x0	reserved
11:0	RW	0x000	iprd_tthdc8_2 The 3rd texture threshold for H.264 CHROMA 8x8 intra prediction.

VEPU_IPRD_TTHDY8_0_H264

Address: Operational Base + offset (0x1710)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	iprd_tthdy8_1 The 2nd texture threshold for H.264 LUMA 8x8 intra prediction.
15:12	RO	0x0	reserved
11:0	RW	0x000	iprd_tthdy8_0 The 1st texture threshold for H.264 LUMA 8x8 intra prediction.

VEPU_IPRD_TTHDY8_1_H264

Address: Operational Base + offset (0x1714)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	iprd_tthdy8_3 The 4th texture threshold for H.264 LUMA 8x8 intra prediction.
15:12	RO	0x0	reserved
11:0	RW	0x000	iprd_tthdy8_2 The 3rd texture threshold for H.264 LUMA 8x8 intra prediction.

VEPU_IPRD_TTHD_UL_H264

Address: Operational Base + offset (0x1718)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	iprd_tthd_ul Texture thredsholds of up and left MB for H.264 LUMA intra prediction.

VEPU_IPRD_WGTY8_H264

Address: Operational Base + offset (0x171C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	iprd_wgty8_3 The 4th cost weight for H.264 LUMA 8x8 intra prediction
23:16	RW	0x00	iprd_wgty8_2 The 3rd cost weight for H.264 LUMA 8x8 intra prediction.

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	iprd_wgty8_1 The 2nd cost weight for H.264 LUMA 8x8 intra prediction.
7:0	RW	0x00	iprd_wgty8_0 The 1st cost weight for H.264 LUMA 8x8 intra prediction.

VEPU_IPRD_WGTY4_H264

Address: Operational Base + offset (0x1720)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	iprd_wgty4_3 The 4th cost weight for H.264 LUMA 4x4 intra prediction
23:16	RW	0x00	iprd_wgty4_2 The 3rd cost weight for H.264 LUMA 4x4 intra prediction.
15:8	RW	0x00	iprd_wgty4_1 The 2nd cost weight for H.264 LUMA 4x4 intra prediction.
7:0	RW	0x00	iprd_wgty4_0 The 1st cost weight for H.264 LUMA 4x4 intra prediction.

VEPU_IPRD_WGTY16_H264

Address: Operational Base + offset (0x1724)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	iprd_wgty16_3 The 4th cost weight for H.264 LUMA 16x16 intra prediction.
23:16	RW	0x00	iprd_wgty16_2 The 3rd cost weight for H.264 LUMA 16x16 intra prediction.
15:8	RW	0x00	iprd_wgty16_1 The 2nd cost weight for H.264 LUMA 16x16 intra prediction.
7:0	RW	0x00	iprd_wgty16_0 The 1st cost weight for H.264 LUMA 16x16 intra prediction.

VEPU_IPRD_WGTC8_H264

Address: Operational Base + offset (0x1728)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	iprd_wgtc8_3 The 4th cost weight for H.264 CHROMA 8x8 intra prediction.
23:16	RW	0x00	iprd_wgtc8_2 The 3rd cost weight for H.264 CHROMA 8x8 intra prediction.
15:8	RW	0x00	iprd_wgtc8_1 The 2nd cost weight for H.264 CHROMA 8x8 intra prediction.
7:0	RW	0x00	iprd_wgtc8_0 The 1st cost weight for H.264 CHROMA 8x8 intra prediction.

VEPU_QNT_BIAS_COMB

Address: Operational Base + offset (0x1730)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:10	RW	0x000	qnt_bias_p Quantization bias for HEVC (9bit) and H.264 (10bit) P block.
9:0	RW	0x000	qnt_bias_i Quantization bias for HEVC (9bit) and H.264 (10bit) I block.

VEPU_ATR_THD0_H264

Address: Operational Base + offset (0x1740)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
23:16	RW	0x00	atr_thd1 The 2nd threshold for H.264 anti-ringing-noise.
15:8	RO	0x00	reserved
7:0	RW	0x00	atr_thd0 The 1st threshold for H.264 anti-ringing-noise.

VEPU_ATR_THD1_H264

Address: Operational Base + offset (0x1744)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x00	atr_qp QP threshold of P frame for H.264 anti-ringing-nois.
15:8	RO	0x00	reserved
7:0	RW	0x00	atr_thd2 The 3rd threshold for H.264 anti-ringing-noise.

VEPU_ATR_WGT16_H264

Address: Operational Base + offset (0x1750)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	atr_lv16_wgt2 The 3rd weight for H.264 16x16 anti-ringing-noise.
15:8	RW	0x00	atr_lv16_wgt1 The 2nd weight for H.264 16x16 anti-ringing-noise.
7:0	RW	0x00	atr_lv16_wgt0 The 1st weight for H.264 16x16 anti-ringing-noise.

VEPU_ATR_WGT8_H264

Address: Operational Base + offset (0x1754)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	atr_lv8_wgt2 The 3rd weight for H.264 8x8 anti-ringing-noise.
15:8	RW	0x00	atr_lv8_wgt1 The 2nd weight for H.264 8x8 anti-ringing-noise.
7:0	RW	0x00	atr_lv8_wgt0 The 1st weight for H.264 8x8 anti-ringing-noise.

VEPU_ATR_WGT4_H264

Address: Operational Base + offset (0x1758)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	atr_lv4_wgt2 The 3rd weight for H.264 4x4 anti-ringing-noise.
15:8	RW	0x00	atr_lv4_wgt1 The 2nd weight for H.264 4x4 anti-ringing-noise.
7:0	RW	0x00	atr_lv4_wgt0 The 1st weight for H.264 4x4 anti-ringing-noise.

VEPU_ME_SQI_COMB

Address: Operational Base + offset (0x1760)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
14:12	RW	0x0	rime_prersu_en enable signal about whether searching refer to last search unit [0] level4 [1] level8 [2] level16
11:10	RW	0x0	rime_prelvl_en enable signal about whether searching refer to last level [0] level4 [1] level8
9:8	RW	0x0	rime_lvl_mrg levels bind enable for search center and scope [0]level4 and level8 bind [1]level8 and level16 bind
7:4	RW	0x0	move_lambda FME lambda move adjustment
3	RO	0x0	reserved
2	RW	0x0	itp_mode reserved
1	RW	0x0	cime_fuse Signal fine search window. It should be constant 1.
0	RW	0x0	cime_pmv_num CME mv stable enable.

VEPU_CIME_MVD_TH_COMB

Address: Operational Base + offset (0x1764)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:20	RW	0x000	cime_mvd_th2 CME mvd threshold2.
19	RO	0x0	reserved
18:10	RW	0x000	cime_mvd_th1 CME mvd threshold1.
9	RO	0x0	reserved
8:0	RW	0x000	cime_mvd_th0 CME mvd threshold0.

VEPU_CIME_MADP_TH_COMB

Address: Operational Base + offset (0x1768)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	cime_madp_th CME MAPD threshold.

VEPU_CIME_MULTI_COMB

Address: Operational Base + offset (0x176C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	cime_multi3 CME cost multiplier3
23:16	RW	0x00	cime_multi2 CME cost multiplier2
15:8	RW	0x00	cime_multi1 CME cost multiplier1
7:0	RW	0x00	cime_multi0 CME cost multiplier0

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VEPU_RIME_MVD_TH_COMB

Address: Operational Base + offset (0x1770)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	fme_madp_th FME MADP threshold.
15:7	RO	0x000	reserved
6:4	RW	0x0	rime_mvd_th1 RME mvd threshold1.
3	RO	0x0	reserved
2:0	RW	0x0	rime_mvd_th0 RME mvd threshold0.

VEPU_RIME_MADP_TH_COMB

Address: Operational Base + offset (0x1774)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	rime_madp_th1 RME MADP threshold1.
15:12	RO	0x0	reserved
11:0	RW	0x000	rime_madp_th0 RME MADP threshold0.

VEPU_RIME_MULTI_COMB

Address: Operational Base + offset (0x1778)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	rime_multi2 RME Cost Multiplier2.
19:10	RW	0x000	rime_multi1 RME Cost Multiplier1.
9:0	RW	0x000	rime_multi0 RME Cost Multiplier0.

VEPU_CMV_ST_TH_COMB

Address: Operational Base + offset (0x177C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	cmv_th2 Threshold2 used for cme_mv counting.
15:8	RW	0x00	cmv_th1 Threshold1 used for cme_mv counting.
7:0	RW	0x00	cmv_th0 Threshold0 used for cme_mv counting.

VEPU_RDO_WGT_QP0

Address: Operational Base + offset (0x1900)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp0 Weight of RDO mode decision when QP is 0.

VEPU_RDO_WGT_QP1

Address: Operational Base + offset (0x1904)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
23:0	RW	0x000000	wgt_rdo_qp1 Weight of RDO mode decision when QP is 1.

VEPU_RDO_WGT_QP2

Address: Operational Base + offset (0x1908)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp2 Weight of RDO mode decision when QP is 2.

VEPU_RDO_WGT_QP3

Address: Operational Base + offset (0x190C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp3 Weight of RDO mode decision when QP is 3.

VEPU_RDO_WGT_QP4

Address: Operational Base + offset (0x1910)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp4 Weight of RDO mode decision when QP is 4.

VEPU_RDO_WGT_QP5

Address: Operational Base + offset (0x1914)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp5 Weight of RDO mode decision when QP is 5.

VEPU_RDO_WGT_QP6

Address: Operational Base + offset (0x1918)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp6 Weight of RDO mode decision when QP is 6.

VEPU_RDO_WGT_QP7

Address: Operational Base + offset (0x191C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp7 Weight of RDO mode decision when QP is 7.

VEPU_RDO_WGT_QP8

Address: Operational Base + offset (0x1920)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp8 Weight of RDO mode decision when QP is 8.

VEPU_RDO_WGT_QP9

Address: Operational Base + offset (0x1924)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp9 Weight of RDO mode decision when QP is 9.

VEPU_RDO_WGT_QP10

Address: Operational Base + offset (0x1928)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp10 Weight of gourp A for HEVC and H.264 RDO mode decision when QP is 10.

VEPU_RDO_WGT_QP11

Address: Operational Base + offset (0x192C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp11 Weight of RDO mode decision when QP is 11.

VEPU_RDO_WGT_QP12

Address: Operational Base + offset (0x1930)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp12 Weight of RDO mode decision when QP is 12.

VEPU_RDO_WGT_QP13

Address: Operational Base + offset (0x1934)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp13 Weight of RDO mode decision when QP is 13.

VEPU_RDO_WGT_QP14

Address: Operational Base + offset (0x1938)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp14 Weight of RDO mode decision when QP is 14.

VEPU_RDO_WGT_QP15

Address: Operational Base + offset (0x193C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp15 Weight of RDO mode decision when QP is 15.

VEPU_RDO_WGT_QP16

Address: Operational Base + offset (0x1940)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp16 Weight of RDO mode decision when QP is 16.

VEPU_RDO_WGT_QP17

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Address: Operational Base + offset (0x1944)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp17 Weight of RDO mode decision when QP is 17.

VEPU_RDO_WGT_QP18

Address: Operational Base + offset (0x1948)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp18 Weight of RDO mode decision when QP is 18.

VEPU_RDO_WGT_QP19

Address: Operational Base + offset (0x194C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp19 Weight of RDO mode decision when QP is 19.

VEPU_RDO_WGT_QP20

Address: Operational Base + offset (0x1950)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp20 Weight of RDO mode decision when QP is 20.

VEPU_RDO_WGT_QP21

Address: Operational Base + offset (0x1954)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp21 Weight of RDO mode decision when QP is 21.

VEPU_RDO_WGT_QP22

Address: Operational Base + offset (0x1958)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp22 Weight of RDO mode decision when QP is 22.

VEPU_RDO_WGT_QP23

Address: Operational Base + offset (0x195C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp23 Weight of RDO mode decision when QP is 23.

VEPU_RDO_WGT_QP24

Address: Operational Base + offset (0x1960)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp24 Weight of RDO mode decision when QP is 24.

VEPU_RDO_WGT_QP25

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Address: Operational Base + offset (0x1964)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp25 Weight of RDO mode decision when QP is 25.

VEPU_RDO_WGT_QP26

Address: Operational Base + offset (0x1968)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp26 Weight of RDO mode decision when QP is 26.

VEPU_RDO_WGT_QP27

Address: Operational Base + offset (0x196C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp27 Weight of RDO mode decision when QP is 27.

VEPU_RDO_WGT_QP28

Address: Operational Base + offset (0x1970)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp28 Weight of RDO mode decision when QP is 28.

VEPU_RDO_WGT_QP29

Address: Operational Base + offset (0x1974)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp29 Weight of RDO mode decision when QP is 29.

VEPU_RDO_WGT_QP30

Address: Operational Base + offset (0x1978)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp30 Weight of RDO mode decision when QP is 30.

VEPU_RDO_WGTA_QP31

Address: Operational Base + offset (0x197C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp31 Weight of RDO mode decision when QP is 31.

VEPU_RDO_WGT_QP32

Address: Operational Base + offset (0x1980)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp32 Weight of RDO mode decision when QP is 32.

VEPU_RDO_WGT_QP33

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Address: Operational Base + offset (0x1984)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp33 Weight of RDO mode decision when QP is 33.

VEPU_RDO_WGT_QP34

Address: Operational Base + offset (0x1988)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp34 Weight of RDO mode decision when QP is 34.

VEPU_RDO_WGT_QP35

Address: Operational Base + offset (0x198C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp35 Weight of RDO mode decision when QP is 35.

VEPU_RDO_WGT_QP36

Address: Operational Base + offset (0x1990)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp36 Weight of RDO mode decision when QP is 36.

VEPU_RDO_WGT_QP37

Address: Operational Base + offset (0x1994)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp37 Weight of RDO mode decision when QP is 37.

VEPU_RDO_WGT_QP38

Address: Operational Base + offset (0x1998)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp38 Weight of RDO mode decision when QP is 38.

VEPU_RDO_WGT_QP39

Address: Operational Base + offset (0x199C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp39 Weight of RDO mode decision when QP is 39.

VEPU_RDO_WGT_QP40

Address: Operational Base + offset (0x19A0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp40 Weight of RDO mode decision when QP is 40.

VEPU_RDO_WGT_QP41

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Address: Operational Base + offset (0x19A4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp41 Weight of RDO mode decision when QP is 41.

VEPU_RDO_WGT_QP42

Address: Operational Base + offset (0x19A8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp42 Weight of RDO mode decision when QP is 42.

VEPU_RDO_WGT_QP43

Address: Operational Base + offset (0x19AC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp43 Weight of RDO mode decision when QP is 43.

VEPU_RDO_WGT_QP44

Address: Operational Base + offset (0x19B0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp44 Weight of RDO mode decision when QP is 44.

VEPU_RDO_WGT_QP45

Address: Operational Base + offset (0x19B4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp45 Weight of RDO mode decision when QP is 45.

VEPU_RDO_WGT_QP46

Address: Operational Base + offset (0x19B8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp46 Weight of RDO mode decision when QP is 46.

VEPU_RDO_WGT_QP47

Address: Operational Base + offset (0x19BC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp47 Weight of RDO mode decision when QP is 47.

VEPU_RDO_WGT_QP48

Address: Operational Base + offset (0x19C0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp48 Weight of RDO mode decision when QP is 48.

VEPU_RDO_WGT_QP49

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Address: Operational Base + offset (0x19C4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp49 Weight of RDO mode decision when QP is 49.

VEPU_RDO_WGT_QP50

Address: Operational Base + offset (0x19C8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp50 Weight of RDO mode decision when QP is 50.

VEPU_RDO_WGT_QP51

Address: Operational Base + offset (0x19CC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	wgt_rdo_qp51 Weight of RDO mode decision when QP is 51.

VEPU_WP_CFG

Address: Operational Base + offset (0x2000)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	cme_wp_en CME weight prediction enable.
8	RW	0x0	wp_en Weight prediction enable.
7	RW	0x0	wpy_en Luma weight prediction enable.
6	RW	0x0	wpc_en Chroma weight prediction enable.
5:3	RW	0x0	log2w_luma luma_log2_weight_denom
2:0	RW	0x0	log2w_chroma chroma_log2_weight_denom

VEPU_WP_GAIN

Address: Operational Base + offset (0x2004)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:20	RW	0x000	wp_gain_y The gain of component Y for weight prediction.
19	RO	0x0	reserved
18:10	RW	0x000	wp_gain_u The gain of component U for weight prediction.
9	RO	0x0	reserved
8:0	RW	0x000	wp_gain_v The gain of component V for weight prediction.

VEPU_WP_OFST

Address: Operational Base + offset (0x2008)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:20	RW	0x00	wp_offset_y The offset of component Y for weight prediction.

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Bit	Attr	Reset Value	Description
19:18	RO	0x0	reserved
17:10	RW	0x00	wp_offset_u The offset of component U for weight prediction.
9:8	RO	0x0	reserved
7:0	RW	0x00	wp_offset_v The offset of component V for weight prediction.

VEPU_RDO_SMEAR_CFG_COMB

Address: Operational Base + offset (0x2014)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	smear_stride Smear state_abcd stride of off-line mode, 16 byte.
19:17	RO	0x0	reserved
16	RW	0x0	online_en state_data source from 1'b0: use online state_data from CIME 1'b1: use offline state_data from VEPU_PP
15	RW	0x0	rdo_smear_en Smear judgement enable
14:13	RW	0x0	stated_mode state_d calculation mode 2'h0 : state_d is "1" 2'h1 : state_d is "0" 2'h2 : state_d is from reference frame
12	RO	0x0	reserved
11:8	RW	0x0	rdo_smear_dlt_qp QP adjust step when smear_flag==1. It's a signed number and the valid value is from -8 to 7.
7:0	RW	0x00	rdo_smear_lvl16_multi Smear cost multiplier for MB.

VEPU_RDO_SMEAR_MADP_THD0_COMB

Address: Operational Base + offset (0x2018)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	rdo_smear_madp_cur_thd1 cu16 movement judgement threshold1
15:12	RO	0x0	reserved
11:0	RW	0x000	rdo_smear_madp_cur_thd0 cu16 movement judgement threshold0

VEPU_RDO_SMEAR_MADP_THD1_COMB

Address: Operational Base + offset (0x201C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	rdo_smear_madp_cur_thd3 cu16 movement judgement threshold3
15:12	RO	0x0	reserved
11:0	RW	0x000	rdo_smear_madp_cur_thd2 cu16 movement judgement threshold2

VEPU_RDO_SMEAR_MADP_THD2_COMB

Address: Operational Base + offset (0x2020)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:16	RW	0x000	rdo_smear_madp_around_thd1 cu16 around-movement judgement threshold1
15:12	RO	0x0	reserved
11:0	RW	0x000	rdo_smear_madp_around_thd0 cu16 around-movement judgement threshold0

VEPU_RDO_SMEAR_MADP_THD3_COMB

Address: Operational Base + offset (0x2024)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	rdo_smear_madp_around_thd3 cu16 around-movement judgement threshold3
15:12	RO	0x0	reserved
11:0	RW	0x000	rdo_smear_madp_around_thd2 cu16 around-movement judgement threshold2

VEPU_RDO_SMEAR_MADP_THD4_COMB

Address: Operational Base + offset (0x2028)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	rdo_smear_madp_around_thd5 cu16 around-movement judgement threshold5
15:12	RO	0x0	reserved
11:0	RW	0x000	rdo_smear_madp_around_thd4 cu16 around-movement judgement threshold4

VEPU_RDO_SMEAR_MADP_THD5_COMB

Address: Operational Base + offset (0x202C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	rdo_smear_madp_ref_thd1 cu16 refence movement judgement threshold1
15:12	RO	0x0	reserved
11:0	RW	0x000	rdo_smear_madp_ref_thd0 cu16 refence movement judgement threshold0

VEPU_RDO_SMEAR_CNT_THD0_COMB

Address: Operational Base + offset (0x2030)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	rdo_smear_cnt_cur_thd3 cu16 counting threshold3
23:20	RO	0x0	reserved
19:16	RW	0x0	rdo_smear_cnt_cur_thd2 cu16 counting threshold2
15:12	RO	0x0	reserved
11:8	RW	0x0	rdo_smear_cnt_cur_thd1 cu16 counting threshold1
7:4	RO	0x0	reserved
3:0	RW	0x0	rdo_smear_cnt_cur_thd0 cu16 counting threshold0

VEPU_RDO_SMEAR_CNT_THD1_COMB

Address: Operational Base + offset (0x2034)

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Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	rdo_smear_cnt_around_thd3 cu16 nearby counting threshold0
23:20	RO	0x0	reserved
19:16	RW	0x0	rdo_smear_cnt_around_thd2 cu16 nearby counting threshold0
15:12	RO	0x0	reserved
11:8	RW	0x0	rdo_smear_cnt_around_thd1 cu16 nearby counting threshold0
7:4	RO	0x0	reserved
3:0	RW	0x0	rdo_smear_cnt_around_thd0 cu16 nearby counting threshold0

VEPU_RDO_SMEAR_CNT_THD2_COMB

Address: Operational Base + offset (0x2038)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	rdo_smear_cnt_around_thd7 cu16 nearby counting threshold7
23:20	RO	0x0	reserved
19:16	RW	0x0	rdo_smear_cnt_around_thd6 cu16 nearby counting threshold6
15:12	RO	0x0	reserved
11:8	RW	0x0	rdo_smear_cnt_around_thd5 cu16 nearby counting threshold5
7:4	RO	0x0	reserved
3:0	RW	0x0	rdo_smear_cnt_around_thd4 cu16 nearby counting threshold4

VEPU_RDO_SMEAR_CNT_THD3_COMB

Address: Operational Base + offset (0x203C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	rdo_smear_cnt_ref_thd1 cu16 refence counting threshold1
7:4	RO	0x0	reserved
3:0	RW	0x0	rdo_smear_cnt_ref_thd0 cu16 refence counting threshold0

VEPU_RDO_SMEAR_RESI_THD0_COMB

Address: Operational Base + offset (0x2040)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	rdo_smear_resi_big_cur_th1 cu16 big-residuals number threshold0
23:22	RO	0x0	reserved
21:16	RW	0x00	rdo_smear_resi_small_cur_th1 cu16 small-residuals number threshold1
15:14	RO	0x0	reserved
13:8	RW	0x00	rdo_smear_resi_big_cur_th0 cu16 big-residuals number threshold0
7:6	RO	0x0	reserved
5:0	RW	0x00	rdo_smear_resi_small_cur_th0 cu16 small-residuals number threshold0

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VEPU_RDO_SMEAR_RESI_THD1_COMB

Address: Operational Base + offset (0x2044)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	rdo_smear_resi_big_around_th1 cu16 nearby big-residuals number threshold1
23:22	RO	0x0	reserved
21:16	RW	0x00	rdo_smear_resi_small_around_th1 cu16 nearby small-residuals number threshold1
15:14	RO	0x0	reserved
13:8	RW	0x00	rdo_smear_resi_big_around_th0 cu16 nearby big-residuals number threshold1
7:6	RO	0x0	reserved
5:0	RW	0x00	rdo_smear_resi_small_around_th0 cu16 nearby small-residuals number threshold0

VEPU_RDO_SMEAR_RESI_THD2_COMB

Address: Operational Base + offset (0x2048)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	rdo_smear_resi_big_around_th3 cu16 nearby big-residuals number threshold3
23:22	RO	0x0	reserved
21:16	RW	0x00	rdo_smear_resi_small_around_th3 cu16 nearby small-residuals number threshold3
15:14	RO	0x0	reserved
13:8	RW	0x00	rdo_smear_resi_big_around_th2 cu16 nearby big-residuals number threshold2
7:6	RO	0x0	reserved
5:0	RW	0x00	rdo_smear_resi_small_around_th2 cu16 nearby small-residuals number threshold2

VEPU_RDO_SMEAR_RESI_THD3_COMB

Address: Operational Base + offset (0x204C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RW	0x00	rdo_smear_resi_big_ref_th0 cu16 refence big-residuals number threshold0
7:6	RO	0x0	reserved
5:0	RW	0x00	rdo_smear_resi_small_ref_th0 cu16 refence small-residuals number threshold0

VEPU_RDO_SMEAR_ST_THD0_COMB

Address: Operational Base + offset (0x2050)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	rdo_smear_resi_th1 right-border and left-border residuals threshold1
15:8	RO	0x00	reserved
7:0	RW	0x00	rdo_smear_resi_th0 right-border and left-border residuals threshold0

VEPU_RDO_SMEAR_ST_THD1_COMB

Address: Operational Base + offset (0x2054)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:20	RW	0x0	rdo_smear_madp_cnt_th5 border residuals statistics threshold5
19:16	RW	0x0	rdo_smear_madp_cnt_th4 border residuals statistics threshold4
15:12	RW	0x0	rdo_smear_madp_cnt_th3 border residuals statistics threshold3
11:8	RW	0x0	rdo_smear_madp_cnt_th2 border residuals statistics threshold2
7:4	RW	0x0	rdo_smear_madp_cnt_th1 border residuals statistics threshold1
3:0	RW	0x0	rdo_smear_madp_cnt_th0 border residuals statistics threshold0

VEPU_RDO_B16_SKIP_ATF_THD0_COMB

Address: Operational Base + offset (0x2070)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	cu16_rdo_skip_atf_madp_thd1 Madp threshold1 of skip 16x16 for ATF adjust.
15:12	RO	0x0	reserved
11:0	RW	0x000	cu16_rdo_skip_atf_madp_thd0 Madp threshold0 of skip 16x16 for ATF adjust.

VEPU_RDO_B16_SKIP_ATF_THD1_COMB

Address: Operational Base + offset (0x2074)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	cu16_rdo_skip_atf_madp_thd3 Madp threshold3 of skip 16x16 for ATF adjust.
15:12	RO	0x0	reserved
11:0	RW	0x000	cu16_rdo_skip_atf_madp_thd2 Madp threshold2 of skip 16x16 for ATF adjust.

VEPU_RDO_B16_SKIP_ATF_WGT0_COMB

Address: Operational Base + offset (0x2078)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	cu16_rdo_skip_atf_wgt3 Weight3 of ATF adjust for skip 16x16.
23:16	RW	0x00	cu16_rdo_skip_atf_wgt2 Weight2 of ATF adjust for skip 16x16.
15:8	RW	0x00	cu16_rdo_skip_atf_wgt1 Weight1 of ATF adjust for skip 16x16.
7:0	RW	0x00	cu16_rdo_skip_atf_wgt0 Weight0 of ATF adjust for skip 16x16.

VEPU_RDO_B16_SKIP_ATF_WGT1_COMB

Address: Operational Base + offset (0x207C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	cu16_rdo_skip_atf_wgt4 Weight4 of ATF adjust for skip 16x16.

VEPU_RDO_B16_INTER_ATF_THD0_COMB

Address: Operational Base + offset (0x208C)

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Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	cu16_rdo_inter_atf_madp_thd1 Madp threshold1 of inter 16x16 for ATF adjust.
15:12	RO	0x0	reserved
11:0	RW	0x000	cu16_rdo_inter_atf_madp_thd0 Madp threshold0 of inter 16x16 for ATF adjust.

VEPU_RDO_B16_INTER_ATF_THD1_COMB

Address: Operational Base + offset (0x2090)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	cu16_rdo_inter_atf_madp_thd2 Madp threshold2 of inter 16x16 for ATF adjust.

VEPU_RDO_B16_INTER_ATF_WGT_COMB

Address: Operational Base + offset (0x2094)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	cu16_rdo_inter_atf_wgt3 Weight3 of ATF adjust for inter 16x16.
23:16	RW	0x00	cu16_rdo_inter_atf_wgt2 Weight2 of ATF adjust for inter 16x16.
15:8	RW	0x00	cu16_rdo_inter_atf_wgt1 Weight1 of ATF adjust for inter 16x16.
7:0	RW	0x00	cu16_rdo_inter_atf_wgt0 Weight0 of ATF adjust for inter 16x16.

VEPU_RDO_B16_INTRA_ATF_THD0_COMB

Address: Operational Base + offset (0x20A4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	cu16_rdo_intra_atf_madp_thd1 Madp threshold1 of intra 16x16 for ATF adjust.
15:12	RO	0x0	reserved
11:0	RW	0x000	cu16_rdo_intra_atf_madp_thd0 Madp threshold0 of intra 16x16 for ATF adjust.

VEPU_RDO_B16_INTRA_ATF_THD1_COMB

Address: Operational Base + offset (0x20A8)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	cu16_rdo_intra_atf_madp_thd2 Madp threshold2 of intra 16x16 for ATF adjust.

VEPU_RDO_B16_INTRA_ATF_WGT_COMB

Address: Operational Base + offset (0x20AC)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	cu16_rdo_intra_atf_wgt3 Weight3 of ATF adjust for intra 16x16.
23:16	RW	0x00	cu16_rdo_intra_atf_wgt2 Weight2 of ATF adjust for intra 16x16.
15:8	RW	0x00	cu16_rdo_intra_atf_wgt1 Weight1 of ATF adjust for intra 16x16.
7:0	RW	0x00	cu16_rdo_intra_atf_wgt0 Weight0 of ATF adjust for intra 16x16.

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VEPU_RDO_B16_INTRA_ATF_CNT_THD_COMB

Address: Operational Base + offset (0x20B4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	cu16_rdo_intra_atf_cnt_thd3 histogram threshold3 for intra16x16.
23:20	RO	0x0	reserved
19:16	RW	0x0	cu16_rdo_intra_atf_cnt_thd2 histogram threshold2 for intra16x16.
15:12	RO	0x0	reserved
11:8	RW	0x0	cu16_rdo_intra_atf_cnt_thd1 histogram threshold1 for intra16x16.
7:4	RO	0x0	reserved
3:0	RW	0x0	cu16_rdo_intra_atf_cnt_thd0 histogram threshold0 for intra16x16.

VEPU_RDO_ATF_RESI_THD_COMB

Address: Operational Base + offset (0x20B8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	rdo_atf_resi_small_th1 resi_cnt threshold3 for intra16x16 .
23:22	RO	0x0	reserved
21:16	RW	0x00	rdo_atf_resi_small_th0 resi_cnt threshold2 for intra16x16 .
15:14	RO	0x0	reserved
13:8	RW	0x00	rdo_atf_resi_big_th1 resi_cnt threshold1 for intra16x16 .
7:6	RO	0x0	reserved
5:0	RW	0x00	rdo_atf_resi_big_th0 resi_cnt threshold0 for intra16x16 .

VEPU_SCAL_H264_FST

Address: Operational Base + offset (0x2200)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	scal_intra_q8

VEPU_SCAL_H264_LST

Address: Operational Base + offset (0x2AFC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	scal_inter_q8

VEPU_QUA_TAB_JPEG_FST

Address: Operational Base + offset (0x2C80)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	jpeg_qua_tab0_data

VEPU_QUA_TAB_JPEG_LST

Address: Operational Base + offset (0x2DFC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	jpeg_qua_tab2_data

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VEPU_ST_BSL_L32
Address: Operational Base + offset (0x4000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	bs_lgth_l32 Low 32 bits of bit stream length for current frame.

VEPU_ST_SSE_BSL
Address: Operational Base + offset (0x4004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sse_l16 Low 16 bits of encoding distortion (SSE).
15:8	RO	0x00	reserved
7:0	RW	0x00	bs_lgth_h8 High 8 bits of bit stream length for current frame.

VEPU_ST_SSE_H32
Address: Operational Base + offset (0x4008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sse_h32 High 32 bits of encoding distortion (SSE).

VEPU_ST_SSE_QP
Address: Operational Base + offset (0x400C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	qp_sum Sum of QP for the encoded frame.

VEPU_ST_SAO
Address: Operational Base + offset (0x4010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sao_ynum Number of CTUs whose LUMA component are adjusted by SAO.
15:0	RW	0x0000	sao_cnum Number of CTUs whose CHROMA component are adjusted by SAO.

VEPU_ST_HEAD_BL_L32
Address: Operational Base + offset (0x4014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rdo_head_bits_l32 Low 32 bits of RDO HeaderBits length.

VEPU_ST_HEAD_RES_BL
Address: Operational Base + offset (0x4018)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	rdo_res_bits_l16 Low 16 bits of RDO ResidualBits length.
15:8	RO	0x00	reserved
7:0	RW	0x00	rdo_head_bits_h8 High 8 bits of RDO HeaderBits length.

VEPU_ST_RES_BL_H24
Address: Operational Base + offset (0x401C)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rdo_res_bits_h24 High 24 bits of RDO ResidualBits length.

VEPU_ST_ENC

Address: Operational Base + offset (0x4020)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	st_sclr Status of safe clear. 1'h0: Safe clear is finished or not started. 1'h1: VEPU is performing safe clear.
1:0	RW	0x0	st_enc VEPU working status. 2'h0: Idle. 2'h1: Working in register conifguration mode. 2'h2: Working in link table configuration mode.

VEPU_ST_LKT

Address: Operational Base + offset (0x4024)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	fnum_enc_done Number modulo 256 of frames has been encoded done since link table mode started.
23:16	RW	0x00	fnum_int Number modulo 256 of frames has been encoded since link table mode started, updated only when corresponding link table node send interrupt (VEPU_ENC_PIC_node_int==1).
15:8	RW	0x00	fnum_cfg Number modulo 256 of frames has been configured since link table mode started.
7:0	RW	0x00	fnum_cfg_done Number modulo 256 of frames has been config done since link table mode started.

VEPU_ST_NADR

Address: Operational Base + offset (0x4028)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	node_addr High 28 bits of the address for the processing linke table node.
3:0	RO	0x0	reserved

VEPU_ST_VBSB

Address: Operational Base + offset (0x402C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:3	RW	0x0000000	vbsbw_addr High 28 bits of bit stream buffer write address.
2:1	RO	0x0	reserved
0	RW	0x0	vbsbw_ovfl Bit stream buffer full (overflow).

VEPU_ST_BUS

Address: Operational Base + offset (0x4030)

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	axir_err AXI read error. [7]: ROI configuration channel (AXI_ARID==11) [6]: LPF read data between tiles channel (AXI_ARID==9) [5]: External line buffer configuration channel (AXI_ARID==7) [4]: Down-sampled picture channel (AXI_ARID==6) [3]: Co-located Mv channel (AXI_ARID==5) | Smear state data channel (AXI_ARID==12) [2]: Link table channel (AXI_ARID==4) [1]: Video source load channel (AXI_ARID==10) [0]: Reference picture channel (AXI_ARID==1,2,3,8)
23:16	RW	0x00	axib_err AXI write response error. [7]: JPEG bit stream mode write channel (AXI0_WID==9) [6]: Link table node channel (AXI0_WID==7) [5]: LPF write-back data between tiles channel(AXI0_WID==5) | External line buffer channel (AXI0_WID==6) [4]: Reconstructed picture channel (AXI0_WID==4) [3]: ME information channel (AXI0_WID==3) [2]: Co-located Mv channel (AXI0_WID==2) | Smear state-d write channel (AXI0_WID==8) [1]: Down-sampled picture channel (AXI0_WID==1) [0]: Bit stream channel (AXI0_WID==0)
15:8	RW	0x00	axib_ovfl AXI write response outstanding overflow. [7]: JPEG bit stream mode write channel (AXI0_WID==9) [6]: Link table node channel (AXI0_WID==7) [5]: LPF write-back data between tiles channel(AXI0_WID==5) | External line buffer channel (AXI0_WID==6) [4]: Reconstructed picture channel (AXI0_WID==4) [3]: ME information channel (AXI0_WID==3) [2]: Co-located Mv channel (AXI0_WID==2) | Smear state-d write channel (AXI0_WID==8) [1]: Down-sampled picture channel (AXI0_WID==1) [0]: Bit stream channel (AXI0_WID==0)
7:0	RW	0x00	axib_idl AXI write response idle. [7]: JPEG bit stream mode write channel (AXI0_WID==9) [6]: Link table node channel (AXI0_WID==7) [5]: LPF write-back data between tiles channel(AXI0_WID==5) & External line buffer channel (AXI0_WID==6) [4]: Reconstructed picture channel (AXI0_WID==4) [3]: ME information channel (AXI0_WID==3) [2]: Co-located Mv channel (AXI0_WID==2) & Smear state-d write channel (AXI0_WID==8) [1]: Down-sampled picture channel (AXI0_WID==1) [0]: Bit stream channel (AXI0_WID==0)

VEPU_ST_SNUM

Address: Operational Base + offset (0x4034)

Bit	Attr	Reset Value	Description
31	RW	0x0	bpkt_lst_jpeg The last bit stream packet of jpeg.
30:24	RW	0x00	bpkt_num_jpeg Bit stream packet number of jpeg.

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Bit	Attr	Reset Value	Description
23	RW	0x0	bpkt_lst_video The last bit stream packet of video.
22:16	RW	0x00	bpkt_num_video Bit stream packet number of video.
15:12	RO	0x0	reserved
11:6	RW	0x00	sli_num_jpeg Number for slices has been encoded and not read out for JPEG(by reading ST_SLEN).
5:0	RW	0x00	sli_num_video Number for slices has been encoded and not read out for video(by reading ST_SLEN).

VEPU_ST_SLEN

Address: Operational Base + offset (0x4038)

Bit	Attr	Reset Value	Description
31	RW	0x0	sli_lst Last slice in this frame of video.
30:0	RW	0x00000000	sli_len Byte length for the earlist encoded slice which has not been read out for video(by reading VEPU_ST_SLEN).

VEPU_ST_LINK_TASK

Address: Operational Base + offset (0x403C)

Bit	Attr	Reset Value	Description
31	RW	0x0	rfpr_ovrb_err Reference Picture FBC body address error.
30	RO	0x0	reserved
29	RW	0x0	dvbm_fmch_err DVBM frame match error.
28	RW	0x0	dvbm_enc_err DVBM overflow when encoding DVBM frame.
27:25	RW	0x0	task_lkt_err Linktable mode error interrupt info: [0]: lkt node error; [1]: lkt command error; [2]: lkt fifo full.
24	RW	0x0	task_done The currently processed link table has been done.
23:12	RW	0x000	task_id_done Link table task id of the processed.
11:0	RW	0x000	task_id_proc Link table task id being processed.

VEPU_ST_SLEN_JPEG

Address: Operational Base + offset (0x4060)

Bit	Attr	Reset Value	Description
31	RW	0x0	sli_lst_jpeg Last slice in this frame of jpeg.
30:0	RW	0x00000000	sli_len_jpeg Byte length for the earlist encoded slice which has not been read out for JPEG(by reading VEPU_ST_SLEN).

VEPU_ST_BSL_L32_JPEG

Address: Operational Base + offset (0x4064)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	jpeg_head_bits_l32 Low 32 bits of JPEG HeaderBits length.

VEPU_ST_BSL_H8_JPEG

Address: Operational Base + offset (0x4068)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	jpeg_head_bits_h8 High 8 bits of JPEG bit stream length.

VEPU_ST_JBSB

Address: Operational Base + offset (0x406C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:3	RW	0x0000000	jbsbw_addr High 28 bits of bit stream buffer write address.
2:1	RO	0x0	reserved
0	RW	0x0	jbsbw_ovfl Bit stream buffer full (overflow).

VEPU_ST_PNUM_P64

Address: Operational Base + offset (0x4080)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RW	0x00000	pnum_p64 Number of 64x64 inter predicted blocks.

VEPU_ST_PNUM_P32

Address: Operational Base + offset (0x4084)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RW	0x00000	pnum_p32 Number of 32x32 inter predicted blocks.

VEPU_ST_PNUM_P16

Address: Operational Base + offset (0x4088)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:0	RW	0x000000	pnum_p16 Number of 16x16 inter predicted blocks.

VEPU_ST_PNUM_P8

Address: Operational Base + offset (0x408C)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:0	RW	0x000000	pnum_p8 Number of 8x8 inter predicted blocks.

VEPU_ST_PNUM_I32

Address: Operational Base + offset (0x4090)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RW	0x00000	pnum_i32 Number of 32x32 intra predicted blocks.

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VEPU_ST_PNUM_I16

Address: Operational Base + offset (0x4094)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:0	RW	0x000000	pnum_i16 Number of 16x16 intra predicted blocks.

VEPU_ST_PNUM_I8

Address: Operational Base + offset (0x4098)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:0	RW	0x000000	pnum_i8 Number of 8x8 intra predicted blocks.

VEPU_ST_PNUM_I4

Address: Operational Base + offset (0x409C)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:0	RW	0x000000	pnum_i4 Number of 4x4 intra predicted blocks.

VEPU_ST_BNUM_B16

Address: Operational Base + offset (0x40A0)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:0	RW	0x000000	num_b16 Number of valid 16x16 blocks for one frame.

VEPU_ST_SMEAR_CNT

Address: Operational Base + offset (0x40A4)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	rdo_smear_cnt3 Number of 16x16 smear blocks in frame bottom right.
23:16	RW	0x00	rdo_smear_cnt2 Number of 16x16 smear blocks in frame bottom left.
15:8	RW	0x00	rdo_smear_cnt1 Number of 16x16 smear blocks in frame top right.
7:0	RW	0x00	rdo_smear_cnt0 Number of 16x16 smear blocks in frame top left.

VEPU_ST_CPLX_SPT

Address: Operational Base + offset (0x40A8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	madi_sum Mean absolute differences for current encoding frame.

VEPU_ST_MADI_LT_NUM0

Address: Operational Base + offset (0x40C0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	madi_th_lt_cnt1 MADI statistics result1 in frame top left.
15:0	RW	0x0000	madi_th_lt_cnt0 MADI statistics result0 in frame top left.

VEPU_ST_MADI_LT_NUM1

Address: Operational Base + offset (0x40C4)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	madi_th_lt_cnt3 MADI statistics result3 in frame top left.
15:0	RW	0x0000	madi_th_lt_cnt2 MADI statistics result2 in frame top left.

VEPU_ST_MADI_RT_NUM0

Address: Operational Base + offset (0x40C8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	madi_th_rt_cnt1 MADI statistics result1 in frame top right.
15:0	RW	0x0000	madi_th_rt_cnt0 MADI statistics result0 in frame top right.

VEPU_ST_MADI_RT_NUM1

Address: Operational Base + offset (0x40CC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	madi_th_rt_cnt3 MADI statistics result3 in frame top right.
15:0	RW	0x0000	madi_th_rt_cnt2 MADI statistics result2 in frame top right.

VEPU_ST_MADI_LB_NUM0

Address: Operational Base + offset (0x40D0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	madi_th_lb_cnt1 MADI statistics result1 in frame left bottom.
15:0	RW	0x0000	madi_th_lb_cnt0 MADI statistics result0 in frame left bottom.

VEPU_ST_MADI_LB_NUM1

Address: Operational Base + offset (0x40D4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	madi_th_lb_cnt3 MADI statistics result3 in frame left bottom.
15:0	RW	0x0000	madi_th_lb_cnt2 MADI statistics result2 in frame left bottom.

VEPU_ST_MADI_RB_NUM0

Address: Operational Base + offset (0x40D8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	madi_th_rb_cnt1 MADI statistics result1 in frame right bottom.
15:0	RW	0x0000	madi_th_rb_cnt0 MADI statistics result0 in frame right bottom.

VEPU_ST_MADI_RB_NUM1

Address: Operational Base + offset (0x40DC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	madi_th_rb_cnt3 MADI statistics result3 in frame right bottom.
15:0	RW	0x0000	madi_th_rb_cnt2 MADI statistics result2 in frame right bottom.

VEPU_ST_MADP_LT_NUM0

Address: Operational Base + offset (0x40E0)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	madp_th_lt_cnt1 MADP statistics result1 in frame top left.
15:0	RW	0x0000	madp_th_lt_cnt0 MADP statistics result0 in frame top left.

VEPU_ST_MADP_LT_NUM1

Address: Operational Base + offset (0x40E4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	madp_th_lt_cnt3 MADP statistics result3 in frame top left.
15:0	RW	0x0000	madp_th_lt_cnt2 MADP statistics result2 in frame top left.

VEPU_ST_MADP_RT_NUM0

Address: Operational Base + offset (0x40E8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	madp_th_rt_cnt1 MADP statistics result1 in frame top right.
15:0	RW	0x0000	madp_th_rt_cnt0 MADP statistics result0 in frame top right.

VEPU_ST_MADP_RT_NUM1

Address: Operational Base + offset (0x40EC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	madp_th_rt_cnt3 MADP statistics result3 in frame top right.
15:0	RW	0x0000	madp_th_rt_cnt2 MADP statistics result2 in frame top right.

VEPU_ST_MADP_LB_NUM0

Address: Operational Base + offset (0x40F0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	madp_th_lb_cnt1 MADP statistics result1 in frame left bottom.
15:0	RW	0x0000	madp_th_lb_cnt0 MADP statistics result0 in frame left bottom.

VEPU_ST_MADP_LB_NUM1

Address: Operational Base + offset (0x40F4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	madp_th_lb_cnt3 MADP statistics result3 in frame left bottom.
15:0	RW	0x0000	madp_th_lb_cnt2 MADP statistics result2 in frame left bottom.

VEPU_ST_MADP_RB_NUM0

Address: Operational Base + offset (0x40F8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	madp_th_rb_cnt1 MADP statistics result1 in frame right bottom.
15:0	RW	0x0000	madp_th_rb_cnt0 MADP statistics result0 in frame right bottom.

VEPU_ST_MADP_RB_NUM1

Address: Operational Base + offset (0x40FC)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	madp_th_rb_cnt3 MADP statistics result3 in frame right bottom.
15:0	RW	0x0000	madp_th_rb_cnt2 MADP statistics result2 in frame right bottom.

VEPU_ST_CMV_LT_NUM0

Address: Operational Base + offset (0x4100)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	cmv_th_lt_cnt1 cme_mv statistics result1 in frame left top.
15:0	RW	0x0000	cmv_th_lt_cnt0 cme_mv statistics result0 in frame left top.

VEPU_ST_CMV_LT_NUM1

Address: Operational Base + offset (0x4104)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	cmv_th_lt_cnt3 cme_mv statistics result3 in frame left top.
15:0	RW	0x0000	cmv_th_lt_cnt2 cme_mv statistics result2 in frame left top.

VEPU_ST_CMV_RT_NUM0

Address: Operational Base + offset (0x4108)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	cmv_th_rt_cnt1 cme_mv statistics result1 in frame right top.
15:0	RW	0x0000	cmv_th_rt_cnt0 cme_mv statistics result0 in frame right top.

VEPU_ST_CMV_RT_NUM1

Address: Operational Base + offset (0x410C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	cmv_th_rt_cnt3 cme_mv statistics result3 in frame right top.
15:0	RW	0x0000	cmv_th_rt_cnt2 cme_mv statistics result2 in frame right top.

VEPU_ST_CMV_LB_NUM0

Address: Operational Base + offset (0x4110)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	cmv_th_lb_cnt1 cme_mv statistics result1 in frame left bottom.
15:0	RW	0x0000	cmv_th_lb_cnt0 cme_mv statistics result0 in frame left bottom.

VEPU_ST_CMV_LB_NUM1

Address: Operational Base + offset (0x4114)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	cmv_th_lb_cnt3 cme_mv statistics result3 in frame left bottom.
15:0	RW	0x0000	cmv_th_lb_cnt2 cme_mv statistics result2 in frame left bottom.

VEPU_ST_CMV_RB_NUM0

Address: Operational Base + offset (0x4118)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	cmv_th_rb_cnt1 cme_mv statistics result1 in frame right bottom.
15:0	RW	0x0000	cmv_th_rb_cnt0 cme_mv statistics result0 in frame right bottom.

VEPU_ST_CMV_RB_NUM1

Address: Operational Base + offset (0x411C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	cmv_th_rb_cnt3 cme_mv statistics result3 in frame right bottom.
15:0	RW	0x0000	cmv_th_rb_cnt2 cme_mv statistics result2 in frame right bottom.

VEPU_ST_VSP_ORG_VALUE0

Address: Operational Base + offset (0x4120)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	org_u_g_min_value min value of source_data_u
23:16	RW	0x00	org_u_g_max_value max value of source_data_u
15:8	RW	0x00	org_y_r_min_value min value of source_data_y
7:0	RW	0x00	org_y_r_max_value max value of source_data_y

VEPU_ST_VSP_ORG_VALUE1

Address: Operational Base + offset (0x4124)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	org_v_b_min_value min value of source_data_v
7:0	RW	0x00	org_v_b_max_value max value of source_data_v

VEPU_ST_VSP_JPEG_VALUE0

Address: Operational Base + offset (0x4128)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	jpeg_u_g_min_value min value of jpeg_u
23:16	RW	0x00	jpeg_u_g_max_value max value of jpeg_u
15:8	RW	0x00	jpeg_y_r_min_value min value of jpeg_y
7:0	RW	0x00	jpeg_y_r_max_value max value of jpeg_y

VEPU_ST_VSP_JPEG_VALUE1

Address: Operational Base + offset (0x412C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	jpeg_v_b_min_value min value of jpeg_v
7:0	RW	0x00	jpeg_v_b_max_value max value of jpeg_v

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VEPU_ST_DSP_Y_SUM

Address: Operational Base + offset (0x4130)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dsp_y_sum summation of DSP Y in current frame

VEPU_ST_B8_QP0

Address: Operational Base + offset (0x4180)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp0 Number of block8x8s with QP=0. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP1

Address: Operational Base + offset (0x4184)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp1 Number of block8x8s with QP=1. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP2

Address: Operational Base + offset (0x4188)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp2 Number of block8x8s with QP=2. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP3

Address: Operational Base + offset (0x418C)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp3 Number of block8x8s with QP=3. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP4

Address: Operational Base + offset (0x4190)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp4 Number of block8x8s with QP=4. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP5

Address: Operational Base + offset (0x4194)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
21:0	RW	0x000000	b8num_qp5 Number of block8x8s with QP=5. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP6

Address: Operational Base + offset (0x4198)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp6 Number of block8x8s with QP=6. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP7

Address: Operational Base + offset (0x419C)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp7 Number of block8x8s with QP=7. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP8

Address: Operational Base + offset (0x41A0)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp8 Number of block8x8s with QP=8. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP9

Address: Operational Base + offset (0x41A4)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp9 Number of block8x8s with QP=9. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP10

Address: Operational Base + offset (0x41A8)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp10 Number of block8x8s with QP=10. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP11

Address: Operational Base + offset (0x41AC)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
21:0	RW	0x000000	b8num_qp11 Number of block8x8s with QP=11. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP12

Address: Operational Base + offset (0x41B0)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp12 Number of block8x8s with QP=12. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP13

Address: Operational Base + offset (0x41B4)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp13 Number of block8x8s with QP=13. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP14

Address: Operational Base + offset (0x41B8)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp14 Number of block8x8s with QP=14. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP15

Address: Operational Base + offset (0x41BC)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp15 Number of block8x8s with QP=15. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP16

Address: Operational Base + offset (0x41C0)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp16 Number of block8x8s with QP=16. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP17

Address: Operational Base + offset (0x41C4)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
21:0	RW	0x000000	b8num_qp17 Number of block8x8s with QP=17. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP18

Address: Operational Base + offset (0x41C8)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp18 Number of block8x8s with QP=18. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP19

Address: Operational Base + offset (0x41CC)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp19 Number of block8x8s with QP=19. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP20

Address: Operational Base + offset (0x41D0)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp20 Number of block8x8s with QP=20. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP21

Address: Operational Base + offset (0x41D4)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp21 Number of block8x8s with QP=21. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP22

Address: Operational Base + offset (0x41D8)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp22 Number of block8x8s with QP=22. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP23

Address: Operational Base + offset (0x41DC)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
21:0	RW	0x000000	b8num_qp23 Number of block8x8s with QP=23. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP24

Address: Operational Base + offset (0x41E0)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp24 Number of block8x8s with QP=24. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP25

Address: Operational Base + offset (0x41E4)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp25 Number of block8x8s with QP=25. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP26

Address: Operational Base + offset (0x41E8)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp26 Number of block8x8s with QP=26. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP27

Address: Operational Base + offset (0x41EC)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp27 Number of block8x8s with QP=27. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP28

Address: Operational Base + offset (0x41F0)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp28 Number of block8x8s with QP=28. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP29

Address: Operational Base + offset (0x41F4)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
21:0	RW	0x000000	b8num_qp29 Number of block8x8s with QP=29. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP30

Address: Operational Base + offset (0x41F8)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp30 Number of block8x8s with QP=30. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP31

Address: Operational Base + offset (0x41FC)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp31 Number of block8x8s with QP=31. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP32

Address: Operational Base + offset (0x4200)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp32 Number of block8x8s with QP=32. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP33

Address: Operational Base + offset (0x4204)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp33 Number of block8x8s with QP=33. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP34

Address: Operational Base + offset (0x4208)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp34 Number of block8x8s with QP=34. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP35

Address: Operational Base + offset (0x420C)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
21:0	RW	0x000000	b8num_qp35 Number of block8x8s with QP=35. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP36

Address: Operational Base + offset (0x4210)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp36 Number of block8x8s with QP=36. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP37

Address: Operational Base + offset (0x4214)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp37 Number of block8x8s with QP=37. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP38

Address: Operational Base + offset (0x4218)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp38 Number of block8x8s with QP=38. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP39

Address: Operational Base + offset (0x421C)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp39 Number of block8x8s with QP=39. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP40

Address: Operational Base + offset (0x4220)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp40 Number of block8x8s with QP=40. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP41

Address: Operational Base + offset (0x4224)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
21:0	RW	0x000000	b8num_qp41 Number of block8x8s with QP=41. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP42

Address: Operational Base + offset (0x4228)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp42 Number of block8x8s with QP=42. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP43

Address: Operational Base + offset (0x422C)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp43 Number of block8x8s with QP=43. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP44

Address: Operational Base + offset (0x4230)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp44 Number of block8x8s with QP=44. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP45

Address: Operational Base + offset (0x4234)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp45 Number of block8x8s with QP=45. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP46

Address: Operational Base + offset (0x4238)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp46 Number of block8x8s with QP=46. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP47

Address: Operational Base + offset (0x423C)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
21:0	RW	0x000000	b8num_qp47 Number of block8x8s with QP=47. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP48

Address: Operational Base + offset (0x4240)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp48 Number of block8x8s with QP=48. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP49

Address: Operational Base + offset (0x4244)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp49 Number of block8x8s with QP=49. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP50

Address: Operational Base + offset (0x4248)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp50 Number of block8x8s with QP=50. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_B8_QP51

Address: Operational Base + offset (0x424C)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x000000	b8num_qp51 Number of block8x8s with QP=51. HEVC CUs of which size are bigger that 8x8 are considered as (CU_size/8)*(CU_size/8) clock8x8s; while H.264 MB is considered as 4 block8x8s.

VEPU_ST_WDG

Address: Operational Base + offset (0x5000)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10	RW	0x0	frm_tout Frame encoding time out.
9	RW	0x0	jpeg_tout JPEG time out.
8	RW	0x0	etpy_tout Entropy time out.
7	RW	0x0	lpf_tout Loop filter time out.
6	RW	0x0	rdo_tout RDO time out.

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Bit	Attr	Reset Value	Description
5	RW	0x0	pren_tout Pre-intra time out.
4	RW	0x0	rfme_tout RFME time out.
3	RW	0x0	swn_tout Search window load time out.
2	RW	0x0	cme_tout CME time out.
1	RW	0x0	pp1_out Pre-process1 time out.
0	RW	0x0	pp0_tout Pre-process0 time out.

VEPU_ST_PPL

Address: Operational Base + offset (0x5004)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10	RW	0x0	frm_wrk Frame encoding is working.
9	RW	0x0	jpeg_wrk JPEG is working.
8	RW	0x0	etpy_wrk Entropy is working.
7	RW	0x0	lpf_wrk Loop filter is working.
6	RW	0x0	rdo_wrk RDO is working.
5	RW	0x0	pren_wrk Pre-intra is working.
4	RW	0x0	rfme_wrk RFME is working.
3	RW	0x0	swn_wrk Search window load is working.
2	RW	0x0	cme_wrk CME is working.
1	RW	0x0	pp1_wrk Pre-process0 is working.
0	RW	0x0	pp0_wrk Pre-process0 is working.

VEPU_ST_PPL_POS_VSP0

Address: Operational Base + offset (0x5008)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	vsp0_pos_y Y position of CTU/MB which is processed by pre-process0.
15:0	RW	0x0000	vsp0_pos_x X position of CTU/MB which is processed by pre-process0.

VEPU_ST_PPL_POS_VSP1

Address: Operational Base + offset (0x500C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	vsp1_pos_y Y position of CTU/MB which is processed by pre-process1.
15:0	RW	0x0000	vsp1_pos_x X position of CTU/MB which is processed by pre-process1.

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VEPU_ST_PPL_POS_CME

Address: Operational Base + offset (0x5010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	cme_pos_y Y position of CTU/MB which is processed by CME.
15:0	RW	0x0000	cme_pos_x X position of CTU/MB which is processed by CME.

VEPU_ST_PPL_POS_SWIN

Address: Operational Base + offset (0x5014)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	swin_pos_y Y position of CTU/MB which is processed by SWIN.
15:0	RW	0x0000	swin_pos_x X position of CTU/MB which is processed by SWIN.

VEPU_ST_PPL_POS_RFME

Address: Operational Base + offset (0x5018)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	rfme_pos_y Y position of CTU/MB which is processed by RFME.
15:0	RW	0x0000	rfme_pos_x X position of CTU/MB which is processed by RFME.

VEPU_ST_PPL_POS_PREN

Address: Operational Base + offset (0x501C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	pren_pos_y Y position of CTU/MB which is processed by pre-intra.
15:0	RW	0x0000	pren_pos_x X position of CTU/MB which is processed by pre-intra.

VEPU_ST_PPL_POS_RDO

Address: Operational Base + offset (0x5020)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	rdo_pos_y Y position of CTU/MB which is processed by RDO.
15:0	RW	0x0000	rdo_pos_x X position of CTU/MB which is processed by RDO.

VEPU_ST_PPL_POS_LPF

Address: Operational Base + offset (0x5024)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	lpf_pos_y Y position of CTU/MB which is processed by LPF.
15:0	RW	0x0000	lpf_pos_x X position of CTU/MB which is processed by LPF.

VEPU_ST_PPL_POS_ETPY

Address: Operational Base + offset (0x5028)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	etpy_pos_y Y position of CTU/MB which is processed by ETPY.
15:0	RW	0x0000	etpy_pos_x X position of CTU/MB which is processed by ETPY.

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VEPU_ST_PPL_POS_JSP0

Address: Operational Base + offset (0x502C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	vsp0_pos_y Y position of CTU/MB which is processed by pre-process0.
15:0	RW	0x0000	vsp0_pos_x X position of CTU/MB which is processed by pre-process0.

VEPU_ST_PPL_POS_JSP1

Address: Operational Base + offset (0x5030)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	vsp1_pos_y Y position of CTU/MB which is processed by pre-process1.
15:0	RW	0x0000	vsp1_pos_x X position of CTU/MB which is processed by pre-process1.

VEPU_ST_PPL_POS_JPEG

Address: Operational Base + offset (0x5034)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	jpeg_pos_y Y position of CTU/MB which is processed by JPEG.
15:0	RW	0x0000	jpeg_pos_x X position of CTU/MB which is processed by JPEG.

VEPU_ST_SLI_NUM

Address: Operational Base + offset (0x5040)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	sli_num Number of slices.

VEPU_MMU_ADDR

Address: Operational Base + offset (0xF000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_dte_addr DTE address for AXI MMU.

VEPU_MMU_ST

Address: Operational Base + offset (0xF004)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:6	RW	0x00	mmu_flt_id ID for the last MMU fault.
5	RW	0x0	mmu_flt_typ Type of MMU fault. 1'h0: Read fault. 1'h1: Write fault.
4	RW	0x0	mmu_rbly_epty MMU replay buffer is empty.
3	RW	0x0	mmu_idl MMU idle.
2	RW	0x0	mmu_stl MMU stall.
1	RW	0x0	mmu_flt MMU page fault.

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Bit	Attr	Reset Value	Description
0	RW	0x0	mmu_e MMU is enabled.

VEPU_MMU_CMD

Address: Operational Base + offset (0xF008)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	mmu_cmd MMU command. 3'h0: MMU mapping enable. 3'h1: MMU mapping disable. 3'h2: MMU stall enable. 3'h3: MMU stall disable. 3'h4: Zap(disable) page table cache line. 3'h5: Leave fault mode. 3'h6: MMU reset.

VEPU_MMU_PFA

Address: Operational Base + offset (0xF00C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_pfa Address of the last page fault.

VEPU_MMU_ZAP

Address: Operational Base + offset (0xF010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_zpa Invalid address for page table cache mapping.

VEPU_MMU_ERR

Address: Operational Base + offset (0xF014)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	rb_err Read bus error.
0	RW	0x0	pf_err Page fault error.

VEPU_MMU_INT_CLR

Address: Operational Base + offset (0xF018)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	rbe_clr Read bus error interrupt clear.
0	RW	0x0	pfe_clr Page fault error interrupt clear.

VEPU_MMU_INT_MSK

Address: Operational Base + offset (0xF01C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	rbe_msk Read bus error interrupt mask.
0	RW	0x0	pfe_msk Page fault error interrupt mask.

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VEPU_MMU_INT_STA

Address: Operational Base + offset (0xF020)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	rbe_sta Read bus error interrupt status.
0	RW	0x0	pfe_sta Page fault error interrupt status.

VEPU_MMU_ACKG

Address: Operational Base + offset (0xF024)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x1	mmu_ackg Auto clock gating enable.

10.6 Application Notes

10.6.1 MMU Config Flow

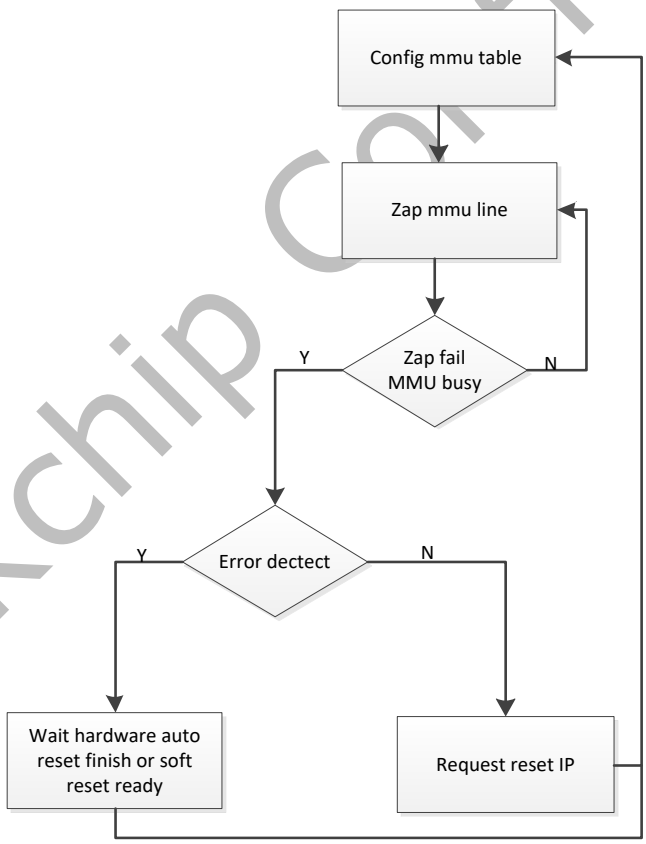


Fig.10-11 MMU Config Flow

1. Prepare mmu table to ddr and config DTE address before begin to decoder.
2. If the mmu table have been changed, you will zap one mmu line.
3. If you zap successed, you can continus to zap next line.
4. If you zap fail, maybe some error happened, then you should check if there any error happens when decoding.
5. If some error happens, you should wait reset finish, and then re-start mmu config.

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6. If don’t have any error find, it will still need to reset, and then re-start mmu config.

10.6.2 VDPU382 decoder Configuration Flow

1. Prepare the data in the DDR.
2. Set the H265 general system configuration. such as working mode in RKVDEC.swreg9, in/out endian in RKVDEC.swreg8.
3. Set the picture parameters with RKVDEC.swreg0~ RKVDEC.swreg63.
4. Set the input and output data base address and H265 reference configuration with RKVDEC.swreg64~ RKVDEC.swreg127.
5. If CABAC error detection is desired, set the RKVDEC.swreg21 to enable the corresponding error detection.
6. Set the interrupt configuration with RKVDEC.swreg11 and start the H265 with RKVDEC.swreg10.
7. Wait for the frame interrupt, and then get the processed results in the target DDR.
8. Clear all the interrupts, and repeat Process2~Process8 to start a new frame decoding if the decoding is not finished yet.

10.6.3 VDPU382 Link table Pointer mode configuration flow

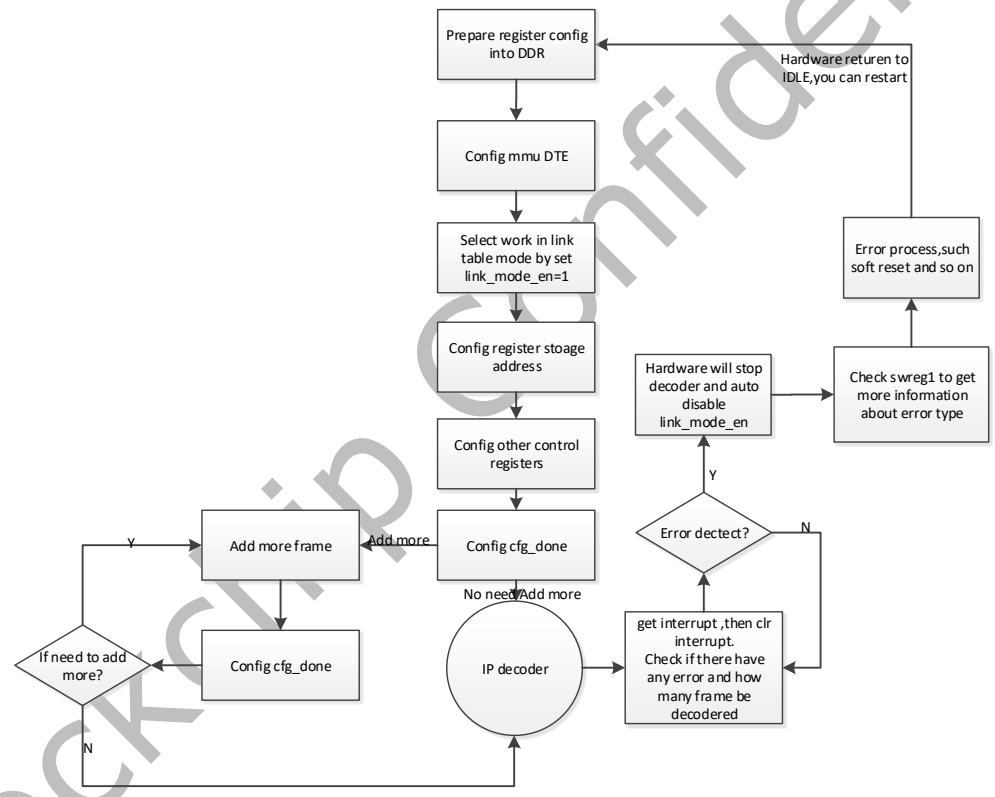


Fig.10-12 Link Table Mode Work Flow

1. Prepare all the register config value into DDR.
2. Config mmu DTE and enable mmu before config link table mode.
3. Config link_mode_irq and other link table mode register. The register is from link_tale_swreg0~link_table_swreg2.
4. Config config_done(set link_table_swreg3[0]=1’b1) to make the link table register configuration effect, after that, hardware will begin to decoder frame by frame.
5. If you need to add more frame, you can use superaddition mode, you can add more frame when decoder at any status.
6. If all config be rdy, you should enable the working flag by config link_mode_en (link_table_swreg6[0]) to 1.
7. If all the frame be decodered, the hardware will hold the working status wait user to process, you can add more frame or set link_mode_en=0(need to set config_done=1’b1) to finish link table mode.

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8. When you get interrupt, at first, you should clear the irq, and then, goto check if there have any error by check link_table_swreg4[31]=1'b1 or not. If any error found by hardware, the hardware will disable link table mode and stop decoder until user restart next link table mode. And then you can get more information about error type from normal register swreg225.
9. When you get interrupt, if there doesn't have any error, you may be to check the frame number which have been decoded.
10. Please note that: Any link table register be config, you need to config swreg3[0]=1'b1 to make it effective.

10.6.4 VDPU720 JPEG decoder Configuration flow

1. Prepare the decoder data in the DDR memory, and in decoder other than JPEG decoder, the input stream buffer should at least contain a slice or a frame data, otherwise the decoder will produce an interrupt and show error and then reset itself.
2. Config all the registers will be used.
3. You should config VDPU720_SWREG1[0] as 1'b1 to enable JPEG decoder.
4. Wait for the frame interrupt, and then check if the frame decoder ready interrupt is right or not, after that, you can get the processed results in the target DDR.
5. Clear all the interrupts, repeat step 2~4 to start a new frame decoder or encoder.

10.6.5 VEPU540 Application Notes

10.6.5.1 Buffer Allocation

User should allocate the following buffers and informs VEPU before the corresponding frame encoding starts.

- Video Source Buffer: H.264 and JPEG each have up to 3 buffers.
- ROI Buffers: Blocking Mapping ROI configuration buffer only for H.264.
- Reference Frame Buffer: H.264 have 2 buffers. One is for FBC(Frame Buffer Compression) header, the other for FBC body.
- Reconstructed Frame buffer: H.264 have 2 buffers. One is for FBC(Frame Buffer Compression) header, the other for FBC body.
- Down-sampled reference frame buffer: It is for H.264 P frame encoding.
- Down-sampled current Frame Buffer: It is for H.264 frames which should be referred.
- Motion Information Buffer: ME(motion estimation) information for user application.
- Bitstream Buffer: H.264 and JPEG each have one bit stream buffer.
- Smear Buffer: It is for subjective quality improvement.
- External Line buffer: It should be allocated when the width of encoding picture is bigger than 3072.

10.6.5.2 H.264 Block Mapping ROI

Each MB has one Block Mapping ROI struct called BCFG_STRUCT stored in Block Mapping buffer.

Table 10-14 BCFG_STRUCT for H.264

STRUCT	BIT	DESCRIPTION
BCFG_STRUCT	[31:20]	Reserved
	[19:16]	MB intra mode adjustment 4'd0: no adjustment 4'd1: force intra 4'd2: force intra with no split 4'd8 to 4'd3: improve the tendency of intra mode 4'd9 to 4'd14: reduce the tendency of intra mode 4'd15: disable intra mode
	[15:12]	MB transparent mode adjustment 4'd0: no adjustment 4'd1: force transparent 4'd2: force inter no residual mode 4'd8 to 4'd3: improve the tendency of transparent mode 4'd9 to 4'd14: reduce the tendency of transparent mode 4'd15: disable inter mode
	[11:8]	MB inter mode adjustment

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		4'd0: no adjustment 4'd1 to 4'd2: reserved 4'd8 to 4'd3: improve the tendency of inter mode 4'd9 to 4'd14: reduce the tendency of inter mode 4'd15: reserved
	[7:0]	MB QP adjustment bit[7]: 0 for relative QP adjustment and 1 for absolute. bit[6:0]: QP adjustment value.

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Chapter 11 MCU Subsystem

11.1 Overview

The MCU Subsystem embedded one MCU processor(Cortex-M0,r0p0-03rel0), a 16KB unified I/D cache and interrupt multiplexer(INTMUX). It allowed fast & efficient data exchange. And the Level 1 Instruction/Data Cache designed for MCU can improve the memory access performance significantly.

The following features may or may not be present in the actual product. Please contact Rockchip for the actual feature configurations and the third-party licensing requirements.

The MCU features and benefits are:

- Two MCU processors: PMU_M0 and BUS_M0
- Optional debug support
  - Two hardware breakpoints
  - One watch points
  - Support Serial Wire debug connection
- Interrupt multiplexer(INTMUX)
  - Mux 4 interrupts from 256 interrupt sources using round-robin algorithm
  - Each 4 adjacent interrupts are seen as a group which share same INTMUX_INT_ENABLE_GROUPx and INTMUX_INT_FLAG_GROUPx register
- 16KB unified I/D Cache
  - Support 2-way set-associative with 32Byte cache line size
  - Support one 128bit AHB-Lite bus master interface to SoC interconnect
  - Support memory cacheable access and peripheral bypass access
  - Support Write-Through with No-Write-Allocate and Read-Allocate
  - Support Write-Back with Write-Allocate and Read-Allocate
  - Support cache maintenance operations (clean/invalidate/clean & invalidate) by address
  - Support cache invalidate/clean & invalidate operations for all cache lines
  - Support cache initialization by software configuration
  - Support RAM debug mode for tag RAM and data RAM
  - Support one interrupt source

There are two MCU subsystem in RK3562, PMU_M0 and BUS_M0 respectively. Their main configurations are different, as shown below.

Table 11-1 MCU Subsystem Configurations

	PMU_M0	BUS_M0
CACHE	NA	16K
IRQ_NUM	8	8
INTMUX	NA	YES

11.2 Block Diagram

The Int_in[255:0] will connect with all interrupt source of RK3562, and please refer to "Chapter System Overview" for the detail interrupt number. MCU Subsystem are shown below.

Table 11-2 MCU NVIC ID

PMU_M0	Interrupt ID	BUS_M0	Interrupt ID
int_0	|irq_mailbox_pmu1_bb[3:0]	int_0	intmux_out[0]
int_1	irq_pmu0hptimer	int_1	intmux_out[1]
int_2	irq_uart0_pmu	int_2	intmux_out[2]
int_3	irq_wdtns_pmu	int_3	intmux_out[3]
int_4	irq_gpio	int_4	|irq_mailbox_bb[3:0]
int_5	irq_spi0	int_5	irq_timer0
int_6	irq_pwm	int_6	NA
int_7	irq_i2c0_pmu	int_7	NA

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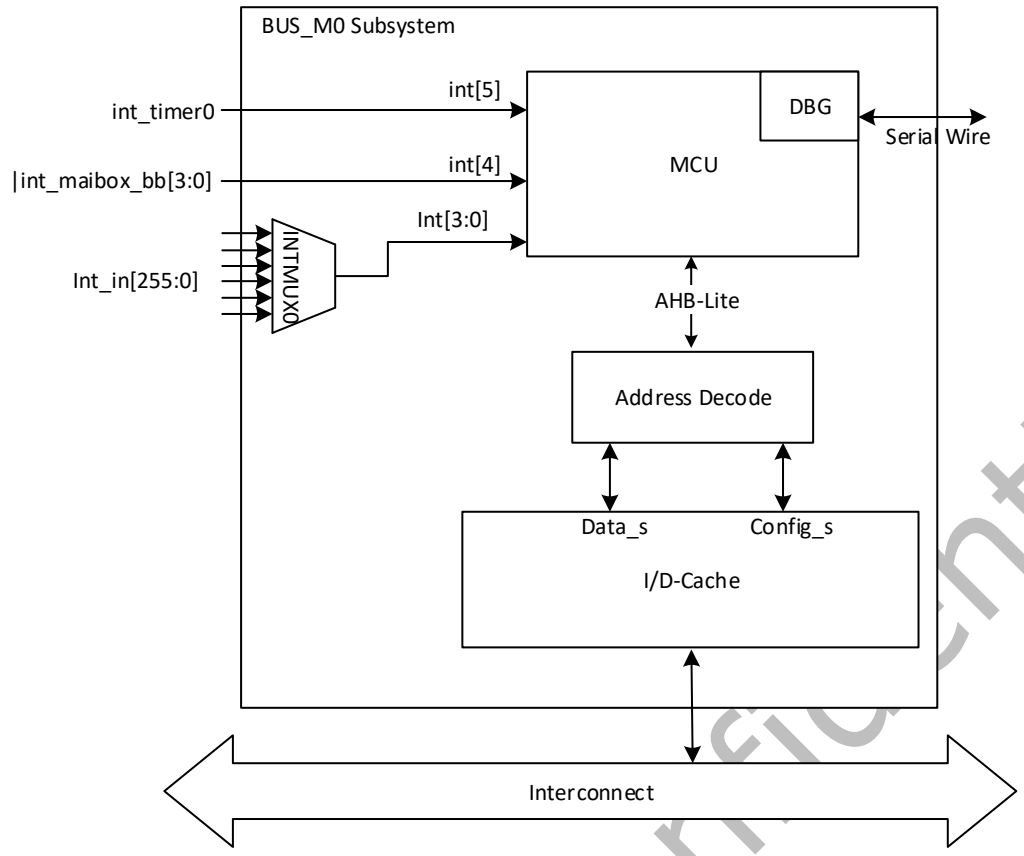


Fig.11-1 Block Diagram of BUS_M0 Subsystem

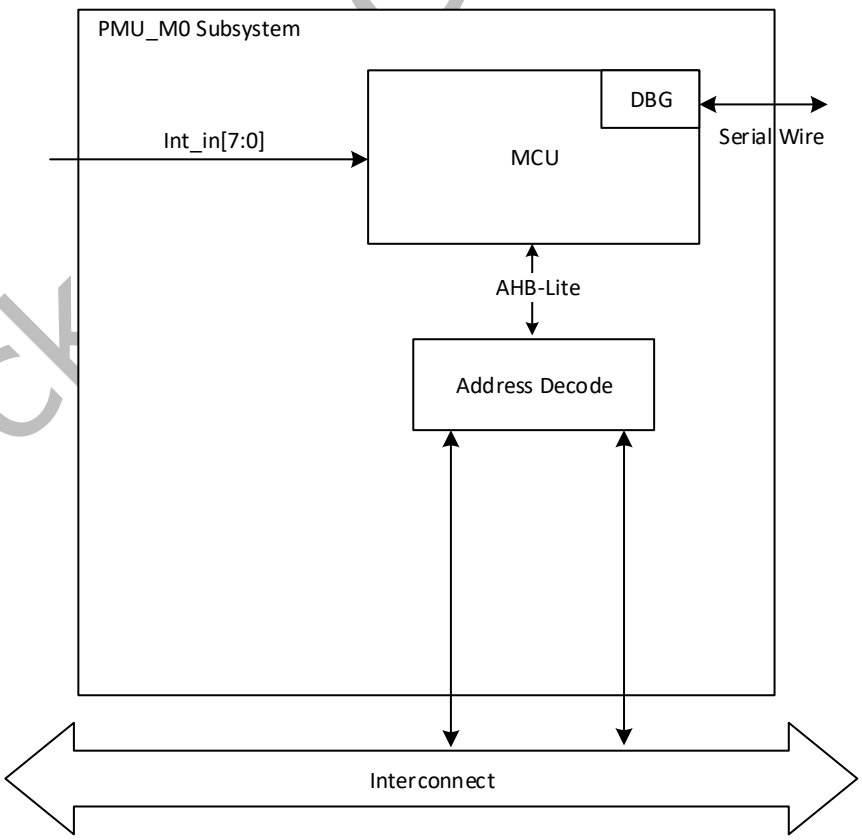


Fig.11-2 Block Diagram of PMU_M0 Subsystem

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11.3 Register Description

11.3.1 Registers Summary(cache)

Name	Offset	Size	Reset Value	Description
CACHE_CACHE_CTRL	0x0000	W	0x000006cc	Cache Control Register
CACHE_MAINTAIN0	0x0004	W	0x00000000	Cache Maintain 0 Register
CACHE_MAINTAIN1	0x0008	W	0x00000000	Cache Maintain 1 Register
CACHE_STB_TIMEOUT_CTRL	0x000c	W	0x4000000c	Store Buffer Timeout Control Register
CACHE_RAM_DEBUG	0x0010	W	0x00000000	Cache RAM Debug Register
CACHE_CACHE_INT_EN	0x0020	W	0x00000000	Cache Interrupt Enable Register
CACHE_CACHE_INT_ST	0x0024	W	0x00000000	Cache Interrupt Status Register
CACHE_CACHE_ERR_HADDR	0x0028	W	0x00000000	Cache Error Address Register
CACHE_CACHE_STATUS	0x0030	W	0x00000000	Cache Status Register
CACHE_PMU_RD_NUM_CNT	0x0040	W	0x00000000	PMU Read Number Count Register
CACHE_PMU_WR_NUM_CNT	0x0044	W	0x00000000	PMU Write Number Count Register
CACHE_PMU_SRAM_RD_HIT_CNT	0x0048	W	0x00000000	PMU RAM Read Hit Count Register
CACHE_PMU_HB_RD_HIT_CNT	0x004c	W	0x00000000	PMU Hot Buffer Read Hit Count Register
CACHE_PMU_STB_RD_HIT_CNT	0x0050	W	0x00000000	PMU Store Buffer Read Hit Count Register
CACHE_PMU_RD_HIT_CNT	0x0054	W	0x00000000	PMU Read Hit Count Register
CACHE_PMU_WR_HIT_CNT	0x0058	W	0x00000000	PMU Write Hit Count Register
CACHE_PMU_RD_MISS_PENALTY_CNT	0x005c	W	0x00000000	PMU Read Miss Penalty Count Register
CACHE_PMU_WR_MISS_PENALTY_CNT	0x0060	W	0x00000000	PMU Write Miss Penalty Count Register
CACHE_PMU_RD_LAT_CNT	0x0064	W	0x00000000	PMU Read Latency Count Register
CACHE_PMU_WR_LAT_CNT	0x0068	W	0x00000000	PMU Write Latency Count Register
CACHE_REVISION	0x00f0	W	0x00000100	Cache Design Revision Register

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

11.3.2 Detail Registers Description

CACHE_CACHE_CTRL

Address: Operational Base(0xFF9F0000) + offset (0x0000)

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Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RW	0x0	cache_pf_en Cache prefetch enable register. 1'b0: Disable 1'b1: Enable
12	RW	0x0	cache_mpu_mode Cache MPU mode enable register. When this bit is set to 1, the cacheability policy is determined by MPU of Cortex-M4. 1'b0: Disable 1'b1: Enable
11	RO	0x0	reserved
10:8	RW	0x6	stb_entry_thresh Store buffer entry threshold control register. The depth of the store buffer entry is 8. When the number of the used data entries is greater than or equal to threshold value, the write data will be written to Cache RAM.
7	RW	0x1	stb_timeout_en Store buffer timeout enable register. When this bit is set to 1, the data in the store buffer must be flushed to Cache RAM if the counter value is equal to the timeout value. 1'b0: Disable 1'b1: Enable
6	RW	0x1	cache_bypass Cache bypass mode enable register. When this bit is set to 1, data will bypass the Cache. 1'b0: Disable 1'b1: Enable
5	RW	0x0	cache_pmu_en Cache Performance Monitor Unit enable register. 1'b0: Disable 1'b1: Enable
4	RW	0x0	cache_flush Cache flush enable register. When this bit is set to 1, the dirty data is flushed to external memory and the cache line are invalidated. 1'b0: Disable 1'b1: Enable
3	RW	0x1	cache_stb_en Cache store buffer enable register. This bit must be set to 0 when Write-Through mode is selected and must be set to 1 when Write-Back mode is selected. 1'b0: Disable 1'b1: Enable
2	RW	0x1	cache_hb_en Cache hot buffer enable register. 1'b0: Disable 1'b1: Enable
1	RW	0x0	cache_wt_en Cache mode control register. 1'b0: Write-Back 1'b1: Write-Through
0	RW	0x0	cache_en Cache initialization enable register. 1'b0: Disable 1'b1: Enable

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CACHE_MAINTAIN0

Address: Operational Base(0xFF9F0000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:5	RW	0x0000000	cache_m_addr Cache maintain start address. This address is 32Byte cache line aligned, that is, the bits[4:0] are always 0.
4:3	RO	0x0	reserved
2:1	RW	0x0	cache_m_cmd Cache maintain command register. 2'b00: Clean by address 2'b01: Invalidate by address 2'b10: Clean and Invalidate by address 2'b11: Invalidate all
0	WO	0x0	cache_m_valid Cache maintain valid register. The maintenance operation is valid only when this bit is set to 1.

CACHE_MAINTAIN1

Address: Operational Base(0xFF9F0000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:0	RW	0x0000000	cache_m_offset Cache maintain offset. This bit field indicates the end offset of cache line, that is, the value plus 1 determines the number of cache line to be maintained. The bit field of cache_m_addr is treated as the start offset of cache line, so the maintain address range is from (cache_m_addr * 32) to (cache_m_addr * 32 + 31 + cache_m_offset * 32).

CACHE_STB_TIMEOUT_CTRL

Address: Operational Base(0xFF9F0000) + offset (0x000c)

Bit	Attr	Reset Value	Description
31:0	RW	0x4000000c	stb_timeout_value Store buffer timeout value.

CACHE_RAM_DEBUG

Address: Operational Base(0xFF9F0000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	ram_debug_en Cache RAM debug mode enable register. 1'b0: Disable 1'b1: Enable

CACHE_CACHE_INT_EN

Address: Operational Base(0xFF9F0000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	err_record_en AHB master bus error record enable. 1'b0: Disable 1'b1: Enable

CACHE_CACHE_INT_ST

Address: Operational Base(0xFF9F0000) + offset (0x0024)

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Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	ahb_error_status Error status bit for AHB master bus. 1'b0: Nothing 1'b1: Bus error

CACHE_CACHE_ERR_HADDR

Address: Operational Base(0xFF9F0000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	status_haddr Recent record of AHB bus error address.

CACHE_CACHE_STATUS

Address: Operational Base(0xFF9F0000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RO	0x0	cache_flush_done Cache flush done status register. 1'b0: Nothing 1'b1: Flush done
1	RO	0x0	cache_m_busy Cache maintain busy status register. 1'b0: Idle 1'b1: Busy
0	RO	0x0	cache_init_finish Cache initialization finish status register. 1'b0: Cache is uninitialized 1'b1: Cache is initialized

CACHE_PMU_RD_NUM_CNT

Address: Operational Base(0xFF9F0000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pmu_rd_num_cnt Total count of read transfers.

CACHE_PMU_WR_NUM_CNT

Address: Operational Base(0xFF9F0000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pmu_wr_num_cnt Total count of write transfers.

CACHE_PMU_SRAM_RD_HIT_CNT

Address: Operational Base(0xFF9F0000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pmu_ram_rd_hit_cnt Count of read hits on Cache RAM.

CACHE_PMU_HB_RD_HIT_CNT

Address: Operational Base(0xFF9F0000) + offset (0x004c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pmu_hb_rd_hit_cnt Count of read hits on hot buffer.

CACHE_PMU_STB_RD_HIT_CNT

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Address: Operational Base(0xFF9F0000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pmu_stb_rd_hit_cnt Count of read hits on store buffer.

CACHE_PMU_RD_HIT_CNT

Address: Operational Base(0xFF9F0000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pmu_rd_hit_cnt Total count of read hits.

CACHE_PMU_WR_HIT_CNT

Address: Operational Base(0xFF9F0000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pmu_wr_hit_cnt Total count of write hits.

CACHE_PMU_RD_MISS_PENALTY_CNT

Address: Operational Base(0xFF9F0000) + offset (0x005c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pmu_rd_miss_penalty_cnt Total count of read miss penalty (in clock cycles).

CACHE_PMU_WR_MISS_PENALTY_CNT

Address: Operational Base(0xFF9F0000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pmu_wr_miss_penalty_cnt Total count of write miss penalty (in clock cycles).

CACHE_PMU_RD_LAT_CNT

Address: Operational Base(0xFF9F0000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pmu_rd_lat_cnt Total count of read latency (in clock cycles).

CACHE_PMU_WR_LAT_CNT

Address: Operational Base(0xFF9F0000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pmu_wr_lat_cnt Total count of write latency (in clock cycles).

CACHE_REVISION

Address: Operational Base(0xFF9F0000) + offset (0x00f0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000100	revision Cache revision number.

11.3.3 Registers Summary (INTMUX)

Name	Offset	Size	Reset Value	Description
INTMUX_INT_ENABLE_GROUP0	0x0000	W	0x00000000	Interrupt Group0 Enable Register
INTMUX_INT_ENABLE_GROUP1	0x0004	W	0x00000000	Interrupt Group1 Enable Register
INTMUX_INT_ENABLE_GROUP2	0x0008	W	0x00000000	Interrupt Group2 Enable Register

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Name	Offset	Size	Reset Value	Description
INTMUX_INT_ENABLE_GROUP3	0x000C	W	0x00000000	Interrupt Group3 Enable Register
INTMUX_INT_ENABLE_GROUP4	0x0010	W	0x00000000	Interrupt Group4 Enable Register
INTMUX_INT_ENABLE_GROUP5	0x0014	W	0x00000000	Interrupt Group5 Enable Register
INTMUX_INT_ENABLE_GROUP6	0x0018	W	0x00000000	Interrupt Group6 Enable Register
INTMUX_INT_ENABLE_GROUP7	0x001C	W	0x00000000	Interrupt Group7 Enable Register
INTMUX_INT_ENABLE_GROUP8	0x0020	W	0x00000000	Interrupt Group8 Enable Register
INTMUX_INT_ENABLE_GROUP9	0x0024	W	0x00000000	Interrupt Group9 Enable Register
INTMUX_INT_ENABLE_GROUP10	0x0028	W	0x00000000	Interrupt Group10 Enable Register
INTMUX_INT_ENABLE_GROUP11	0x002C	W	0x00000000	Interrupt Group11 Enable Register
INTMUX_INT_ENABLE_GROUP12	0x0030	W	0x00000000	Interrupt Group12 Enable Register
INTMUX_INT_ENABLE_GROUP13	0x0034	W	0x00000000	Interrupt Group13 Enable Register
INTMUX_INT_ENABLE_GROUP14	0x0038	W	0x00000000	Interrupt Group14 Enable Register
INTMUX_INT_ENABLE_GROUP15	0x003C	W	0x00000000	Interrupt Group15 Enable Register
INTMUX_INT_ENABLE_GROUP16	0x0040	W	0x00000000	Interrupt Group16 Enable Register
INTMUX_INT_ENABLE_GROUP17	0x0044	W	0x00000000	Interrupt Group17 Enable Register
INTMUX_INT_ENABLE_GROUP18	0x0048	W	0x00000000	Interrupt Group18 Enable Register
INTMUX_INT_ENABLE_GROUP19	0x004C	W	0x00000000	Interrupt Group19 Enable Register
INTMUX_INT_ENABLE_GROUP20	0x0050	W	0x00000000	Interrupt Group20 Enable Register
INTMUX_INT_ENABLE_GROUP21	0x0054	W	0x00000000	Interrupt Group21 Enable Register
INTMUX_INT_ENABLE_GROUP22	0x0058	W	0x00000000	Interrupt Group22 Enable Register
INTMUX_INT_ENABLE_GROUP23	0x005C	W	0x00000000	Interrupt Group23 Enable Register
INTMUX_INT_ENABLE_GROUP24	0x0060	W	0x00000000	Interrupt Group24 Enable Register
INTMUX_INT_ENABLE_GROUP25	0x0064	W	0x00000000	Interrupt Group25 Enable Register
INTMUX_INT_ENABLE_GROUP26	0x0068	W	0x00000000	Interrupt Group26 Enable Register
INTMUX_INT_ENABLE_GROUP27	0x006C	W	0x00000000	Interrupt Group27 Enable Register
INTMUX_INT_ENABLE_GROUP28	0x0070	W	0x00000000	Interrupt Group28 Enable Register
INTMUX_INT_ENABLE_GROUP29	0x0074	W	0x00000000	Interrupt Group29 Enable Register

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Name	Offset	Size	Reset Value	Description
INTMUX_INT_ENABLE_GROUP30	0x0078	W	0x00000000	Interrupt Group30 Enable Register
INTMUX_INT_ENABLE_GROUP31	0x007C	W	0x00000000	Interrupt Group31 Enable Register
INTMUX_INT_FLAG_GROUP0	0x0080	W	0x00000000	Interrupt Group0 Flag Register
INTMUX_INT_FLAG_GROUP1	0x0084	W	0x00000000	Interrupt Group1 Flag Register
INTMUX_INT_FLAG_GROUP2	0x0088	W	0x00000000	Interrupt Group2 Flag Register
INTMUX_INT_FLAG_GROUP3	0x008C	W	0x00000000	Interrupt Group3 Flag Register
INTMUX_INT_FLAG_GROUP4	0x0090	W	0x00000000	Interrupt Group4 Flag Register
INTMUX_INT_FLAG_GROUP5	0x0094	W	0x00000000	Interrupt Group5 Flag Register
INTMUX_INT_FLAG_GROUP6	0x0098	W	0x00000000	Interrupt Group6 Flag Register
INTMUX_INT_FLAG_GROUP7	0x009C	W	0x00000000	Interrupt Group7 Flag Register
INTMUX_INT_FLAG_GROUP8	0x00A0	W	0x00000000	Interrupt Group8 Flag Register
INTMUX_INT_FLAG_GROUP9	0x00A4	W	0x00000000	Interrupt Group9 Flag Register
INTMUX_INT_FLAG_GROUP10	0x00A8	W	0x00000000	Interrupt Group10 Flag Register
INTMUX_INT_FLAG_GROUP11	0x00AC	W	0x00000000	Interrupt Group11 Flag Register
INTMUX_INT_FLAG_GROUP12	0x00B0	W	0x00000000	Interrupt Group12 Flag Register
INTMUX_INT_FLAG_GROUP13	0x00B4	W	0x00000000	Interrupt Group13 Flag Register
INTMUX_INT_FLAG_GROUP14	0x00B8	W	0x00000000	Interrupt Group14 Flag Register
INTMUX_INT_FLAG_GROUP15	0x00BC	W	0x00000000	Interrupt Group15 Flag Register
INTMUX_INT_FLAG_GROUP16	0x00C0	W	0x00000000	Interrupt Group16 Flag Register
INTMUX_INT_FLAG_GROUP17	0x00C4	W	0x00000000	Interrupt Group17 Flag Register
INTMUX_INT_FLAG_GROUP18	0x00C8	W	0x00000000	Interrupt Group18 Flag Register
INTMUX_INT_FLAG_GROUP19	0x00CC	W	0x00000000	Interrupt Group19 Flag Register
INTMUX_INT_FLAG_GROUP20	0x00D0	W	0x00000000	Interrupt Group20 Flag Register
INTMUX_INT_FLAG_GROUP21	0x00D4	W	0x00000000	Interrupt Group21 Flag Register
INTMUX_INT_FLAG_GROUP22	0x00D8	W	0x00000000	Interrupt Group22 Flag Register
INTMUX_INT_FLAG_GROUP23	0x00DC	W	0x00000000	Interrupt Group23 Flag Register
INTMUX_INT_FLAG_GROUP24	0x00E0	W	0x00000000	Interrupt Group24 Flag Register

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Name	Offset	Size	Reset Value	Description
INTMUX_INT_FLAG_GROUP25	0x00E4	W	0x00000000	Interrupt Group25 Flag Register
INTMUX_INT_FLAG_GROUP26	0x00E8	W	0x00000000	Interrupt Group26 Flag Register
INTMUX_INT_FLAG_GROUP27	0x00EC	W	0x00000000	Interrupt Group27 Flag Register
INTMUX_INT_FLAG_GROUP28	0x00F0	W	0x00000000	Interrupt Group28 Flag Register
INTMUX_INT_FLAG_GROUP29	0x00F4	W	0x00000000	Interrupt Group29 Flag Register
INTMUX_INT_FLAG_GROUP30	0x00F8	W	0x00000000	Interrupt Group30 Flag Register
INTMUX_INT_FLAG_GROUP31	0x00FC	W	0x00000000	Interrupt Group31 Flag Register

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

11.3.4 Detail Registers Description

INTMUX_INT_ENABLE_GROUP0

Address: Operational Base(0xFFAF0000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disabled 1'b1: Interrupt enabled

INTMUX_INT_ENABLE_GROUP1

Address: Operational Base(0xFFAF0000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disabled 1'b1: Interrupt enabled

INTMUX_INT_ENABLE_GROUP2

Address: Operational Base(0xFFAF0000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disabled 1'b1: Interrupt enabled

INTMUX_INT_ENABLE_GROUP3

Address: Operational Base(0xFFAF0000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disabled 1'b1: Interrupt enabled

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INTMUX_INT_ENABLE_GROUP4

Address: Operational Base(0xFFAF0000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disabled 1'b1: Interrupt enabled

INTMUX_INT_ENABLE_GROUP5

Address: Operational Base(0xFFAF0000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disabled 1'b1: Interrupt enabled

INTMUX_INT_ENABLE_GROUP6

Address: Operational Base(0xFFAF0000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disabled 1'b1: Interrupt enabled

INTMUX_INT_ENABLE_GROUP7

Address: Operational Base(0xFFAF0000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disabled 1'b1: Interrupt enabled

INTMUX_INT_ENABLE_GROUP8

Address: Operational Base(0xFFAF0000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disabled 1'b1: Interrupt enabled

INTMUX_INT_ENABLE_GROUP9

Address: Operational Base(0xFFAF0000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disabled 1'b1: Interrupt enabled

INTMUX_INT_ENABLE_GROUP10

Address: Operational Base(0xFFAF0000) + offset (0x0028)

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Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disabled 1'b1: Interrupt enabled

INTMUX_INT_ENABLE_GROUP11

Address: Operational Base(0xFFAF0000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disabled 1'b1: Interrupt enabled

INTMUX_INT_ENABLE_GROUP12

Address: Operational Base(0xFFAF0000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disabled 1'b1: Interrupt enabled

INTMUX_INT_ENABLE_GROUP13

Address: Operational Base(0xFFAF0000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disabled 1'b1: Interrupt enabled

INTMUX_INT_ENABLE_GROUP14

Address: Operational Base(0xFFAF0000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disabled 1'b1: Interrupt enabled

INTMUX_INT_ENABLE_GROUP15

Address: Operational Base(0xFFAF0000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disabled 1'b1: Interrupt enabled

INTMUX_INT_ENABLE_GROUP16

Address: Operational Base(0xFFAF0000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disabled 1'b1: Interrupt enabled

INTMUX_INT_ENABLE_GROUP17

Address: Operational Base(0xFFAF0000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disabled 1'b1: Interrupt enabled

INTMUX_INT_ENABLE_GROUP18

Address: Operational Base(0xFFAF0000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disabled 1'b1: Interrupt enabled

INTMUX_INT_ENABLE_GROUP19

Address: Operational Base(0xFFAF0000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disabled 1'b1: Interrupt enabled

INTMUX_INT_ENABLE_GROUP20

Address: Operational Base(0xFFAF0000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disabled 1'b1: Interrupt enabled

INTMUX_INT_ENABLE_GROUP21

Address: Operational Base(0xFFAF0000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disabled 1'b1: Interrupt enabled

INTMUX_INT_ENABLE_GROUP22

Address: Operational Base(0xFFAF0000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disabled 1'b1: Interrupt enabled

INTMUX_INT_ENABLE_GROUP23

Address: Operational Base(0xFFAF0000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disabled 1'b1: Interrupt enabled

INTMUX_INT_ENABLE_GROUP24

Address: Operational Base(0xFFAF0000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disabled 1'b1: Interrupt enabled

INTMUX_INT_ENABLE_GROUP25

Address: Operational Base(0xFFAF0000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disabled 1'b1: Interrupt enabled

INTMUX_INT_ENABLE_GROUP26

Address: Operational Base(0xFFAF0000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disabled 1'b1: Interrupt enabled

INTMUX_INT_ENABLE_GROUP27

Address: Operational Base(0xFFAF0000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disabled 1'b1: Interrupt enabled

INTMUX_INT_ENABLE_GROUP28

Address: Operational Base(0xFFAF0000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disabled 1'b1: Interrupt enabled

INTMUX_INT_ENABLE_GROUP29

Address: Operational Base(0xFFAF0000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disabled 1'b1: Interrupt enabled

INTMUX_INT_ENABLE_GROUP30

Address: Operational Base(0xFFAF0000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disabled 1'b1: Interrupt enabled

INTMUX_INT_ENABLE_GROUP31

Address: Operational Base(0xFFAF0000) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disabled 1'b1: Interrupt enabled

INTMUX_INT_FLAG_GROUP0

Address: Operational Base(0xFFAF0000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP1

Address: Operational Base(0xFFAF0000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP2

Address: Operational Base(0xFFAF0000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RO	0x00	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP3

Address: Operational Base(0xFFAF0000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP4

Address: Operational Base(0xFFAF0000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP5

Address: Operational Base(0xFFAF0000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP6

Address: Operational Base(0xFFAF0000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP7

Address: Operational Base(0xFFAF0000) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP8

Address: Operational Base(0xFFAF0000) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RO	0x00	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP9

Address: Operational Base(0xFFAF0000) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP10

Address: Operational Base(0xFFAF0000) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP11

Address: Operational Base(0xFFAF0000) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP12

Address: Operational Base(0xFFAF0000) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP13

Address: Operational Base(0xFFAF0000) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP14

Address: Operational Base(0xFFAF0000) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RO	0x00	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP15

Address: Operational Base(0xFFAF0000) + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP16

Address: Operational Base(0xFFAF0000) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP17

Address: Operational Base(0xFFAF0000) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP18

Address: Operational Base(0xFFAF0000) + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP19

Address: Operational Base(0xFFAF0000) + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP20

Address: Operational Base(0xFFAF0000) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP21

Address: Operational Base(0xFFAF0000) + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP22

Address: Operational Base(0xFFAF0000) + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP23

Address: Operational Base(0xFFAF0000) + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP24

Address: Operational Base(0xFFAF0000) + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP25

Address: Operational Base(0xFFAF0000) + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP26

Address: Operational Base(0xFFAF0000) + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP27

Address: Operational Base(0xFFAF0000) + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP28

Address: Operational Base(0xFFAF0000) + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP29

Address: Operational Base(0xFFAF0000) + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP30

Address: Operational Base(0xFFAF0000) + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP31

Address: Operational Base(0xFFAF0000) + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

11.4 Interface Description

There are two sets of serial debug interface for the two MCUs. When we debug using serial

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wire, not only set IOMUX, but also configure the PMUIOC_GRF_JTAG_CON1[2:1] or VCCIO234_IOC_GRF_JTAG_CON0[2:1] to select the MCU that you want to debug.

Table 11-3 MCU Serial Wire Debug Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
mcujtag_tckm0	I	UART0_TX_M0/JTAG_CPU_MCU_TCK_M0/GPIO0_D1_u	PMU_IOC_GPIO0D_IOMUX_SEL_L[7:4]=2
mcujtag_tmsm0	I/O	UART0_RX_M0/JTAG_CPU_MCU_TMS_M0/GPIO0_D0_u	PMU_IOC_GPIO0D_IOMUX_SEL_L[3:0]=2
mcujtag_tckm1	I	SDMMC0_D2/JTAG_CPU_MCU_TCK_M1/UART5_CTSN_M0/SPI1_CSN1_M1/PWM10_M0/DSM_AUD_RP/GPIO1_B5_u	GPIO1_IOC_GPIO1B_IOMUX_SEL_H[7:4]=2
mcujtag_tmsm1	I/O	SDMMC0_D3/JTAG_CPU_MCU_TMS_M1/UART5_RTSN_M0/SPI1_CSN0_M1/PWM11_M0/DSM_AUD_RN/GPIO1_B6_u	GPIO1_IOC_GPIO1B_IOMUX_SEL_H[11:8]=2

Notes: I=input, O=output, I/O=input/output, bidirectional

11.5 Application Notes

11.5.1 Clock and Reset Generation

Please refer to "Chapter CRU" for more detailed information.

11.5.2 Memory Remap

The memory map is divided into different memory types for different usage.

To avoid the memory map conflict between different processors, the source space can be remapped to another. In addition, these remap operation could not take effect until the MCU soft reset.

Table 11-4 PMU_M0 Address Remap

Before Remap	Memory Type	Usage	After Remap
0xA0000000 - 0xDFFFFFFF	Device XN	Peripherals	Before Remap - 0xA0000000 + {pmugrf_soc_con12[15:0],16'h0}
0x80000000 - 0x9FFFFFFF	Normal WT	Off chip RAM	Before Remap - 0x60000000 + {pmugrf_soc_con11[15:0],16'h0}
0x60000000 - 0x7FFFFFFF	Normal WBWA	Off chip RAM	Before Remap - 0x60000000 + {pmugrf_soc_con11[15:0],16'h0}
0x40000000 - 0x5FFFFFFF	Device XN	Peripherals	Before Remap - 0x40000000 + 0xF0000000
0x20000000 - 0x3FFFFFFF	Normal WBWA	On chip RAM	Before Remap - 0x20000000 + {pmugrf_soc_con10[15:0],16'h0}
0x00000000 - 0x1FFFFFFF	Normal WT	ROM or flash	Before Remap - 0x0000000 + {pmugrf_soc_con9[15:0],16'h0}

Table 11-5 BUS_M0 Address Remap

Before Remap	Memory Type	Usage	After Remap
0xA0000000 - 0xDFFFFFFF	Device XN	Peripherals	Before Remap - 0xA0000000 + {sgrf_soc_con12[15:0],16'h0}
0x80000000 - 0x9FFFFFFF	Normal WT	Off chip RAM	Before Remap - 0x60000000 + {sgrf_soc_con11[15:0],16'h0}
0x60000000 - 0x7FFFFFFF	Normal WBWA	Off chip RAM	Before Remap - 0x60000000 + {sgrf_soc_con11[15:0],16'h0}
0x40000000 - 0x5FFFFFFF	Device XN	Peripherals	Before Remap - 0x40000000 + 0xF0000000
0x20000000 - 0x3FFFFFFF	Normal WBWA	On chip RAM	Before Remap - 0x20000000 + {sgrf_soc_con10[15:0],16'h0}
0x00000000 - 0x1FFFFFFF	Normal WT	ROM or flash	Before Remap - 0x0000000 + {sgrf_soc_con9[15:0],16'h0}

Notes:

- *XN means execute-never.*
- *WT means write-through.*
- *WBWA means write-back-write-allocate.*
- *WT means write-through*

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11.5.3 Interrupt for MCU

Table 11-6 BUS_M0 Interrupt

IRQ ID	IRQ Source	IRQ ID	IRQ Source
0	intmux_out[0]	4	|int_mailbox_bb[3:0]
1	intmux_out[1]	5	int_timer0
2	intmux_out[2]	6	NA
3	intmux_out[3]	7	NA

Table 11-7 PMU_M0 Interrupt

IRQ ID	IRQ Source	IRQ ID	IRQ Source
0	|int_mailbox_bb_pmu[3:0]	4	int_gpio0_pmu
1	int_hptimer_pmu	5	int_spi0_pmu
2	int_uart0_pmu	6	int_pwm0_pmu
3	int_wdtns_pmu	7	int_i2c0_pmu

11.5.4 Cache Initialization

The Cache is bypassed after reset and need to be initialized by the MCU. The basic initialization flow is:

1. Configure to Write-Back or Write-Through mode by setting CACHE_CTRL.cache_wt_en and start initialization by configuring CACHE_CTRL.cache_en to high while keeping the Cache in bypass mode (CACHE_CTRL.cache_bypass is high). The store buffer must and only can be enabled for Write-Back mode, so you must disable the store buffer when Write-Through mode is selected. You can also enable the hot buffer for better performance. It is recommended that configure the I-Cache to Write-Through mode and configure the D-Cache to Write-Back mode.
2. Wait for cache initialization to be finished by polling CACHE_STATUS.cache_init_finish.
3. Disable cache bypass mode by configuring CACHE_CTRL.cache_bypass to low. Now that the Cache is enabled.
4. Simply configure CACHE_CTRL.cache_bypass to bypass or enable the Cache again after the initialization flow.

11.5.5 Cache Maintenance

The Cache Controller support the following cache maintenance operations:

- Clean by address: push the specified cache line data to external memory if it is valid and dirty.
- Invalidate by address: unconditionally clear the valid and dirty data of the specified cache lines.
- Clean and invalidate by address: clean and then invalidate the specified cache lines.
- Invalidate all: unconditionally clear the valid and dirty data for all the cache lines.
- Clean and invalidate all (Flush): clean and then invalidate all the cache lines.

For the operation of cache clean and invalidate all, configure CACHE_CTRL.cache_flush to high first, and then wait for flush to be done by polling CACHE_STATUS.cache_flush_done. Finally, if the flush is done, you should configure CACHE_CTRL.cache_flush to low.

For the other four maintenance operations, you should set the maintenance command and the address range of the cache lines by configuring CACHE_MAINTAIN0 and CACHE_MAINTAIN1, then start by configuring CACHE_MAINTAIN0.cache_m_valid to high. When the operation is finished, CACHE_MAINTAIN0.cache_m_valid will be automatically cleared to low. You can also poll CACHE_STATUS.cache_m_busy to judge whether the operation is done.

11.5.6 Other Hints

One interrupt request source is supported for the I/D-Cache, so you can query the interrupt register in the ISR if it is enabled. When CACHE_INT_EN.err_record_en is high, the Cache

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will generate a bus error interrupt if access to a wrong address. You can read CACHE_INT_ST.ahb_error_status for the cache interrupt status and get the recent error address information from CACHE_ERR_HADDR.status_haddr.

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Chapter 12 DMA Controller (DMAC)

12.1 Overview

This device supports one Direct Memory Access (DMA) Controller. DMAC0 supports transfers between memory and memory, peripheral and memory. DMAC0 is under Non-secure state after reset, and the Secure state can be changed by configurable SGRF module.

DMAC0 supports the following features:

- DMAC0 Supports 32 peripheral requests
- Up to 64 bits data size
- 8 channel at the same time
- Up to burst 16
- 16 interrupts output and 1 abort output
- Supports 128 MFIFO depth

Following table shows the DMAC request mapping scheme.

Table 12-1 DMAC Request Mapping Table

DMAC0		
Req number	**Source**	**Polarity**
0	UART0_RX	High level
1	UART1_RX	High level
2	UART2_RX	High level
3	UART3_RX	High level
4	UART4_RX	High level
5	UART5_CAN1_RX	High level
6	UART6_RX	High level
7	UART7_RX	High level
8	UART8_RX	High level
9	UART9_RX	High level
10	UART1_TX	High level
11	UART5_CAN1_TX	High level
12	SPI0_RX	High level
13	SPI0_TX	High level
14	SPI1_RX	High level
15	SPI1_TX	High level
16	SPI2_RX	High level
17	SPI2_TX	High level
18	SAI0_8CH_RX	High level
19	SAI0_8CH_TX	High level
20	SAI1_8CH_RX	High level
21	SAI1_8CH_TX	High level
22	SAI2_2CH_RX	High level
23	SAI2_2CH_TX	High level
24	CAN0_RX	High level
25	CAN0_TX	High level
26	PWM0_RX	High level
27	PWM1_RX	High level
28	PWM2_RX	High level
29	PWM3_RX	High level
30	SPDIF_8CH_TX	High level
31	PDM_RX	High level

DMAC supports incrementing-address burst and fixed-address burst. But in the case of access to SPI and UART at byte or halfword size, DMAC only supports fixed-address burst and the address must be aligned to word.

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UART5 and CAN1 share request number 5 and 11, which is determined by the register GRF_PERI_CON1[11]; When GRF_PERI_CON1[11]=1, CAN1 can work; When GRF_PERI_CON1[11]=0, UART5 can work; The default value of the register is 0.

12.2 Block Diagram

Following figure shows the block diagram of DMAC.

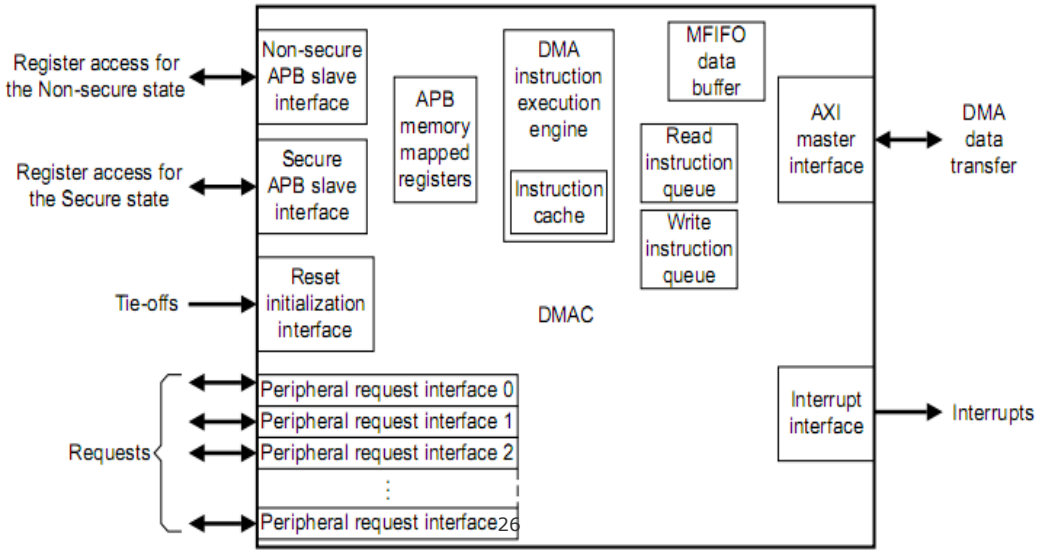


Fig.12-1 Block Diagram of DMAC

As the DMAC supports TrustZone technology, so dual APB interfaces enable the operation of the DMAC to be partitioned into the Secure state and Non-secure state. You can use the APB interfaces to access status registers and also directly execute instructions in the DMAC. The default interface after reset is Non-secure APB interface.

12.3 Function Description

12.3.1 Introduction

The DMAC contains an instruction processing block that enables it to process program code that controls a DMA transfer. The program code is stored in a region of system memory that the DMAC accesses using its AXI interface. The DMAC stores instructions temporarily in a cache. It supports 8 channels, each channel capable of supporting a single concurrent thread of DMA operation. In addition, a single DMA manager thread exists, and you can use it to initialize the DMA channel threads. The DMAC executes up to one instruction for each AXI clock cycle. To ensure that it regularly executes each active thread, it alternates by processing the DMA manager thread and then a DMA channel thread. It uses a round-robin process when selecting the next active DMA channel thread to execute.

The DMAC uses variable-length instructions that consist of one to six bytes. It provides a separate Program Counter (PC) register for each DMA channel. When a thread requests an instruction from an address, the cache performs a look-up. If a cache hit occurs, then the cache immediately provides the data. Otherwise, the thread is stalled while the DMAC uses the AXI interface to perform a cache line fill. If an instruction is greater than 4 bytes, or spans the end of a cache line, the DMAC performs multiple cache accesses to fetch the instruction.

When a cache line fill is in progress, the DMAC enables other threads to access the cache, but if another cache miss occurs, this stalls the pipeline until the first line fill is complete. When a DMA channel thread executes a load or store instruction, the DMAC adds the instruction to the relevant read or write queue. The DMAC uses these queues as an instruction storage buffer prior to it issuing the instructions on the AXI bus. The DMAC also contains a Multi First-In-First-Out (MFIFO) data buffer that it uses to store data that it reads, or writes, during a DMA transfer.

12.3.2 Operating states

Following figure shows the operating states for the DMA manager thread and DMA channel

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threads.

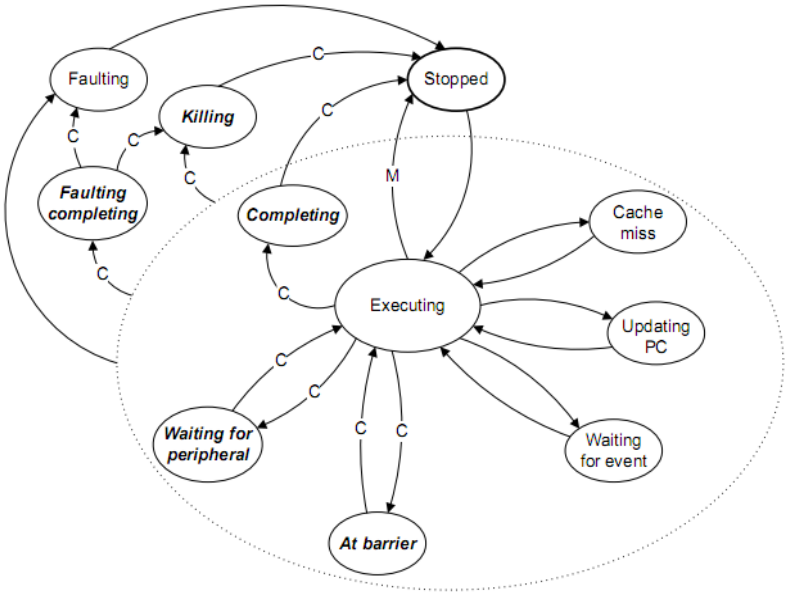


Fig.12-2 DMAC Operation State

Notes: arcs with no letter designator indicate state transitions for the DMA manager and DMA channel threads, otherwise use is restricted as follows:
C DMA channel threads only.
M DMA manager thread only.

After the DMAC exits from reset, it sets all DMA channel threads to the stopped state, and DMA manager thread moves to the Stopped state.

12.4 Register Description

12.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
SDMAC_BASE	0xFF980000
DMAC_BASE	0xFF990000

12.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
DMA_DSR	0x0000	W	0x00000200	DMA Manager Status Register
DMA_DPC	0x0004	W	0x00000000	DMA Program Counter Register
DMA_INTEN	0x0020	W	0x00000000	Interrupt Enable Register
DMA_EVENT_RIS	0x0024	W	0x00000000	Event-Interrupt Raw Status Register
DMA_INTMIS	0x0028	W	0x00000000	Interrupt Status Register
DMA_INTCLR	0x002C	W	0x00000000	Interrupt Clear Register
DMA_FSRD	0x0030	W	0x00000000	Fault Status DMA Manager Register
DMA_FSRC	0x0034	W	0x00000000	Fault Status DMA Channel Register
DMA_FTRD	0x0038	W	0x00000000	Fault Type DMA Manager Register
DMA_FTR0	0x0040	W	0x00000000	Fault Type DMA Channel Register
DMA_FTR1	0x0044	W	0x00000000	Fault Type DMA Channel Register
DMA_FTR2	0x0048	W	0x00000000	Fault Type DMA Channel Register
DMA_FTR3	0x004C	W	0x00000000	Fault Type DMA Channel Register
DMA_FTR4	0x0050	W	0x00000000	Fault Type DMA Channel Register

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Name	Offset	Size	Reset Value	Description
DMA_FTR5	0x0054	W	0x00000000	Fault Type DMA Channel Register
DMA_FTR6	0x0058	W	0x00000000	Fault Type DMA Channel Register
DMA_FTR7	0x005C	W	0x00000000	Fault Type DMA Channel Register
DMA_CSR0	0x0100	W	0x00000000	Channel Status Registers
DMA_CPC0	0x0104	W	0x00000000	Channel Program Counter Registers
DMA_CSR1	0x0108	W	0x00000000	Channel Status Registers
DMA_CPC1	0x010C	W	0x00000000	Channel Program Counter Registers
DMA_CSR2	0x0110	W	0x00000000	Channel Status Registers
DMA_CPC2	0x0114	W	0x00000000	Channel Program Counter Registers
DMA_CSR3	0x0118	W	0x00000000	Channel Status Registers
DMA_CPC3	0x011C	W	0x00000000	Channel Program Counter Registers
DMA_CSR4	0x0120	W	0x00000000	Channel Status Registers
DMA_CPC4	0x0124	W	0x00000000	Channel Program Counter Registers
DMA_CSR5	0x0128	W	0x00000000	Channel Status Registers
DMA_CPC5	0x012C	W	0x00000000	Channel Program Counter Registers
DMA_CSR6	0x0130	W	0x00000000	Channel Status Registers
DMA_CPC6	0x0134	W	0x00000000	Channel Program Counter Registers
DMA_CSR7	0x0138	W	0x00000000	Channel Status Registers
DMA_CPC7	0x013C	W	0x00000000	Channel Program Counter Registers
DMA_SAR0	0x0400	W	0x00000000	Source Address Registers
DMA_DAR0	0x0404	W	0x00000000	Destination Address Registers
DMA_CCR0	0x0408	W	0x00000000	Channel Control Registers
DMA_LC0_0	0x040C	W	0x00000000	Loop Counter 0 Registers
DMA_LC1_0	0x0410	W	0x00000000	Loop Counter 1 Registers
DMA_SAR1	0x0420	W	0x00000000	Source Address Registers
DMA_DAR1	0x0424	W	0x00000000	Destination Address Registers
DMA_CCR1	0x0428	W	0x00000000	Channel Control Registers
DMA_LC0_1	0x042C	W	0x00000000	Loop Counter 0 Registers
DMA_LC1_1	0x0430	W	0x00000000	Loop Counter 1 Registers
DMA_SAR2	0x0440	W	0x00000000	Source Address Registers
DMA_DAR2	0x0444	W	0x00000000	Destination Address Registers
DMA_CCR2	0x0448	W	0x00000000	Channel Control Registers
DMA_LC0_2	0x044C	W	0x00000000	Loop Counter 0 Registers
DMA_LC1_2	0x0450	W	0x00000000	Loop Counter 1 Registers
DMA_SAR3	0x0460	W	0x00000000	Source Address Registers
DMA_DAR3	0x0464	W	0x00000000	Destination Address Registers
DMA_CCR3	0x0468	W	0x00000000	Channel Control Registers
DMA_LC0_3	0x046C	W	0x00000000	Loop Counter 0 Registers
DMA_LC1_3	0x0470	W	0x00000000	Loop Counter 1 Registers
DMA_SAR4	0x0480	W	0x00000000	Source Address Registers
DMA_DAR4	0x0484	W	0x00000000	Destination Address Registers
DMA_CCR4	0x0488	W	0x00000000	Channel Control Registers
DMA_LC0_4	0x048C	W	0x00000000	Loop Counter 0 Registers
DMA_LC1_4	0x0490	W	0x00000000	Loop Counter 1 Registers
DMA_SAR5	0x04A0	W	0x00000000	Source Address Registers

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Name	Offset	Size	Reset Value	Description
DMA_DAR5	0x04A4	W	0x00000000	Destination Address Registers
DMA_CCR5	0x04A8	W	0x00000000	Channel Control Registers
DMA_LC0_5	0x04AC	W	0x00000000	Loop Counter 0 Registers
DMA_LC1_5	0x04B0	W	0x00000000	Loop Counter 1 Registers
DMA_SAR6	0x04C0	W	0x00000000	Source Address Registers
DMA_DAR6	0x04C4	W	0x00000000	Destination Address Registers
DMA_CCR6	0x04C8	W	0x00000000	Channel Control Registers
DMA_LC0_6	0x04CC	W	0x00000000	Loop Counter 0 Registers
DMA_LC1_6	0x04D0	W	0x00000000	Loop Counter 1 Registers
DMA_SAR7	0x04E0	W	0x00000000	Source Address Registers
DMA_DAR7	0x04E4	W	0x00000000	Destination Address Registers
DMA_CCR7	0x04E8	W	0x00000000	Channel Control Registers
DMA_LC0_7	0x04EC	W	0x00000000	Loop Counter 0 Registers
DMA_LC1_7	0x04F0	W	0x00000000	Loop Counter 1 Registers
DMA_DBGSTATUS	0x0D00	W	0x00000000	Debug Status Register
DMA_DBGCMD	0x0D04	W	0x00000000	Debug Command Register
DMA_DBGINST0	0x0D08	W	0x00000000	Debug Instruction-0 Register
DMA_DBGINST1	0x0D0C	W	0x00000000	Debug Instruction-1 Register
DMA_CR0	0x0E00	W	0x001FF075	Configuration Register 0
DMA_CR1	0x0E04	W	0x000000B5	Configuration Register 1
DMA_CR2	0x0E08	W	0x00000000	Configuration Register 2
DMA_CR3	0x0E0C	W	0x0000FFFF	Configuration Register 3
DMA_CR4	0x0E10	W	0xFFFFFFFF	Configuration Register 4
DMA_CRDn	0x0E14	W	0x07FF7F73	Configuration Register
DMA_WD	0x0E80	W	0x00000000	DMA Watchdog Register

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

12.4.3 Detail Registers Description

DMA_DSR

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RO	0x1	dns 1'b0: DMA manager operates in the Secure state 1'b1: DMA manager operates in the Non-secure state
8:4	RO	0x00	wakeup_event 5'b00000: event[0] 5'b00001: event[1] 5'b00010: event[2] 5'b11111: event[31]
3:0	RO	0x0	dma_status 4'b0000: Stopped 4'b0001: Executing 4'b0010: Cache miss 4'b0011: Updating PC 4'b0100: Waiting for event 4'b0101-4'b1110: reserved 4'b1111: Faulting

DMA_DPC

Address: **Operational Base** + offset (0x0004)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pc_mgr Program counter for the DMA manager thread

DMA_INTEN

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	event_irq_select Bit [N] 1'b0: If the DMAC executes DMASEV for the event-interrupt resource N then the DMAC signals event N to all of the threads. Set bit [N] to 0 if your system design does not use irq[N] to signal an interrupt request 1'b1: If the DMAC executes DMASEV for the event-interrupt resource N then the DMAC sets irq[N] HIGH. Set bit [N] to 1 if your system designer requires irq[N] to signal an interrupt request

DMA_EVENT_RIS

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dmasev_active Bit [N] 1'b0: Event N is inactive or irq[N] is LOW 1'b1: Event N is active or irq[N] is HIGH

DMA_INTMIS

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	irq_status Bit [N] 1'b0: Interrupt N is inactive and therefore irq[N] is LOW 1'b1: Interrupt N is active and therefore irq[N] is HIGH

DMA_INTCLR

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	irq_clr Bit [N] 1'b0: The status of irq[N] does not change 1'b1: The DMAC sets irq[N] LOW if the INTEN Register programs the DMAC to signal an interrupt. Otherwise, the status of irq[N] does not change

DMA_FSRD

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	fs_mgr 1'b0: the DMA manager thread is not in the Faulting state 1'b1: the DMA manager thread is in the Faulting state

DMA_FSRC

Address: **Operational Base** + offset (0x0034)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RO	0x00	fault_status Bit [N] 1'b0: No fault is present on DMA channel N. 1'b1: DMA channel N is in the Faulting or Faulting completing state

DMA_FTRD

Address: **Operational Base** + offset (0x0038)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	dbg_instr memory or from the debug interface: 1'b0: instruction that generated an abort was read from system memory 1'b1: instruction that generated an abort was read from the debug interface
29:17	RO	0x0000	reserved
16	RO	0x0	instr_fetch_err performs an instruction fetch: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response
15:6	RO	0x000	reserved
5	RO	0x0	mgr_evnt_err 1'b0: the DMA manager has appropriate security to execute DMAWFE or DMASEV 1'b1: a DMA manager thread in the Non-secure state attempted to execute either: o DMAWFE to wait for a secure event o DMASEV to create a secure event or secure interrupt
4	RO	0x0	dmago_err 1'b0: the DMA manager has appropriate security to execute DMAGO 1'b1: a DMA manager thread in the Non-secure state attempted to execute DMAGO to create a DMA channel operating in the Secure state
3:2	RO	0x0	reserved
1	RO	0x0	operand_invalid the configuration of the DMAC: 1'b0: valid operand 1'b1: invalid operand
0	RW	0x0	undef_instr 1'b0: defined instruction 1'b1: undefined instruction

DMA_FTR0

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31	RO	0x0	lockup_err 1'b0: DMA channel has adequate resources 1'b1: DMA channel has locked-up because of insufficient resources This fault is an imprecise abort.

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Bit	Attr	Reset Value	Description
30	RO	0x0	dbg_instr memory or from the debug interface: 1'b0: instruction that generated an abort was read from system memory 1'b1: instruction that generated an abort was read from the debug interface This fault is an imprecise abort but the bit is only valid when a precise abort occurs.
29:19	RO	0x000	reserved
18	RO	0x0	data_read_err thread performs a data read: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
17	RO	0x0	data_write_err thread performs a data write: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
16	RO	0x0	instr_fetch_err thread performs an instruction fetch: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is a precise abort.
15:14	RO	0x0	reserved
13	RO	0x0	st_data_unavailable 1'b0: MFIFO contains all the data to enable the DMAST to complete 1'b1: previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete This fault is a precise abort.
12	RO	0x0	mfifo_err DMALD 1'b0: MFIFO contains sufficient space 1'b1: MFIFO is too small to hold the data that DMALD requires DMAST 1'b0: MFIFO contains sufficient data 1'b1: MFIFO is too small to store the data to enable DMAST to complete This fault is an imprecise abort.
11:8	RO	0x0	reserved
7	RO	0x0	ch_rdwr_err to perform a secure read or secure write: 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to perform a secure read or secure write This fault is a precise abort.

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Bit	Attr	Reset Value	Description
6	RO	0x0	ch_periph_err DMASTP, or DMAFLUSHP with inappropriate security permissions: 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to execute either: o DMAWFP to wait for a secure peripheral o DMALDP or DMASTP to notify a secure peripheral o DMAFLUSHP to flush a secure peripheral This fault is a precise abort.
5	RO	0x0	ch_event_err 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to execute either: o DMAWFE to wait for a secure event o DMASEV to create a secure event or secure interrupt This fault is a precise abort.
4:2	RO	0x0	reserved
1	RO	0x0	operand_invalid valid for the configuration of the DMAC: 1'b0: valid operand 1'b1: invalid operand This fault is a precise abort.
0	RO	0x0	undef_instr 1'b0: defined instruction 1'b1: undefined instruction This fault is a precise abort.

DMA_FTR1

Address: **Operational Base** + offset (0x0044)

Bit	Attr	Reset Value	Description
31	RO	0x0	lockup_err 1'b0: DMA channel has adequate resources 1'b1: DMA channel has locked-up because of insufficient resources This fault is an imprecise abort.
30	RO	0x0	dbg_instr memory or from the debug interface: 1'b0: instruction that generated an abort was read from system memory 1'b1: instruction that generated an abort was read from the debug interface This fault is an imprecise abort but the bit is only valid when a precise abort occurs.
29:19	RO	0x000	reserved
18	RO	0x0	data_read_err thread performs a data read: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
17	RO	0x0	data_write_err thread performs a data write: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.

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Bit	Attr	Reset Value	Description
16	RO	0x0	instr_fetch_err thread performs an instruction fetch: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is a precise abort.
15:14	RO	0x0	reserved
13	RO	0x0	st_data_unavailable 1'b0: MFIFO contains all the data to enable the DMAST to complete 1'b1: previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete This fault is a precise abort.
12	RO	0x0	mfifo_err DMALD 1'b0: MFIFO contains sufficient space 1'b1: MFIFO is too small to hold the data that DMALD requires DMAST 1'b0: MFIFO contains sufficient data 1'b1: MFIFO is too small to store the data to enable DMAST to complete This fault is an imprecise abort.
11:8	RO	0x0	reserved
7	RO	0x0	ch_rdwr_err to perform a secure read or secure write: 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to perform a secure read or secure write This fault is a precise abort.
6	RO	0x0	ch_periph_err DMASTP, or DMAFLUSHP with inappropriate security permissions: 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to execute either: o DMAWFP to wait for a secure peripheral o DMALDP or DMASTP to notify a secure peripheral o DMAFLUSHP to flush a secure peripheral This fault is a precise abort.
5	RO	0x0	ch_event_err 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to execute either: o DMAWFE to wait for a secure event o DMASEV to create a secure event or secure interrupt This fault is a precise abort.
4:2	RO	0x0	reserved
1	RO	0x0	operand_invalid valid for the configuration of the DMAC: 1'b0: valid operand 1'b1: invalid operand This fault is a precise abort.

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Bit	Attr	Reset Value	Description
0	RO	0x0	undef_instr 1'b0: defined instruction 1'b1: undefined instruction This fault is a precise abort.

DMA_FTR2

Address: **Operational Base** + offset (0x0048)

Bit	Attr	Reset Value	Description
31	RO	0x0	lockup_err 1'b0: DMA channel has adequate resources 1'b1: DMA channel has locked-up because of insufficient resources This fault is an imprecise abort.
30	RO	0x0	dbg_instr memory or from the debug interface: 1'b0: instruction that generated an abort was read from system memory 1'b1: instruction that generated an abort was read from the debug interface This fault is an imprecise abort but the bit is only valid when a precise abort occurs.
29:19	RO	0x000	reserved
18	RO	0x0	data_read_err thread performs a data read: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
17	RO	0x0	data_write_err thread performs a data write: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
16	RO	0x0	instr_fetch_err thread performs an instruction fetch: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is a precise abort.
15:14	RO	0x0	reserved
13	RO	0x0	st_data_unavailable 1'b0: MFIFO contains all the data to enable the DMAST to complete 1'b1: previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete This fault is a precise abort.
12	RO	0x0	mfifo_err DMALD 1'b0: MFIFO contains sufficient space 1'b1: MFIFO is too small to hold the data that DMALD requires DMAST 1'b0: MFIFO contains sufficient data 1'b1: MFIFO is too small to store the data to enable DMAST to complete This fault is an imprecise abort.
11:8	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
7	RO	0x0	ch_rdwr_err to perform a secure read or secure write: 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to perform a secure read or secure write This fault is a precise abort.
6	RO	0x0	ch_periph_err DMASTP, or DMAFLUSHP with inappropriate security permissions: 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to execute either: o DMAWFP to wait for a secure peripheral o DMALDP or DMASTP to notify a secure peripheral o DMAFLUSHP to flush a secure peripheral This fault is a precise abort.
5	RO	0x0	ch_event_err 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to execute either: o DMAWFE to wait for a secure event o DMASEV to create a secure event or secure interrupt This fault is a precise abort.
4:2	RO	0x0	reserved
1	RO	0x0	operand_invalid valid for the configuration of the DMAC: 1'b0: valid operand 1'b1: invalid operand This fault is a precise abort.
0	RO	0x0	undef_instr 1'b0: defined instruction 1'b1: undefined instruction This fault is a precise abort.

DMA_FTR3

Address: **Operational Base** + offset (0x004C)

Bit	Attr	Reset Value	Description
31	RO	0x0	lockup_err 1'b0: DMA channel has adequate resources 1'b1: DMA channel has locked-up because of insufficient resources This fault is an imprecise abort.
30	RO	0x0	dbg_instr memory or from the debug interface: 1'b0: instruction that generated an abort was read from system memory 1'b1: instruction that generated an abort was read from the debug interface This fault is an imprecise abort but the bit is only valid when a precise abort occurs.
29:19	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
18	RO	0x0	data_read_err thread performs a data read: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
17	RO	0x0	data_write_err thread performs a data write: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
16	RO	0x0	instr_fetch_err thread performs an instruction fetch: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is a precise abort.
15:14	RO	0x0	reserved
13	RO	0x0	st_data_unavailable 1'b0: MFIFO contains all the data to enable the DMAST to complete 1'b1: previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete This fault is a precise abort.
12	RO	0x0	mfifo_err DMALD 1'b0: MFIFO contains sufficient space 1'b1: MFIFO is too small to hold the data that DMALD requires DMAST 1'b0: MFIFO contains sufficient data 1'b1: MFIFO is too small to store the data to enable DMAST to complete This fault is an imprecise abort.
11:8	RO	0x0	reserved
7	RO	0x0	ch_rdwr_err to perform a secure read or secure write: 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to perform a secure read or secure write This fault is a precise abort.
6	RO	0x0	ch_periph_err DMASTP, or DMAFLUSHP with inappropriate security permissions: 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to execute either: o DMAWFP to wait for a secure peripheral o DMALDP or DMASTP to notify a secure peripheral o DMAFLUSHP to flush a secure peripheral This fault is a precise abort.

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Bit	Attr	Reset Value	Description
5	RO	0x0	ch_event_err 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to execute either: o DMAWFE to wait for a secure event o DMASEV to create a secure event or secure interrupt This fault is a precise abort.
4:2	RO	0x0	reserved
1	RO	0x0	operand_invalid valid for the configuration of the DMAC: 1'b0: valid operand 1'b1: invalid operand This fault is a precise abort.
0	RO	0x0	undef_instr 1'b0: defined instruction 1'b1: undefined instruction This fault is a precise abort.

DMA_FTR4

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31	RO	0x0	lockup_err 1'b0: DMA channel has adequate resources 1'b1: DMA channel has locked-up because of insufficient resources This fault is an imprecise abort.
30	RO	0x0	dbg_instr memory or from the debug interface: 1'b0: instruction that generated an abort was read from system memory 1'b1: instruction that generated an abort was read from the debug interface This fault is an imprecise abort but the bit is only valid when a precise abort occurs.
29:19	RO	0x000	reserved
18	RO	0x0	data_read_err thread performs a data read: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
17	RO	0x0	data_write_err thread performs a data write: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
16	RO	0x0	instr_fetch_err thread performs an instruction fetch: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is a precise abort.
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13	RO	0x0	st_data_unavailable 1'b0: MFIFO contains all the data to enable the DMAST to complete 1'b1: previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete This fault is a precise abort.
12	RO	0x0	mfifo_err DMALD 1'b0: MFIFO contains sufficient space 1'b1: MFIFO is too small to hold the data that DMALD requires DMAST 1'b0: MFIFO contains sufficient data 1'b1: MFIFO is too small to store the data to enable DMAST to complete This fault is an imprecise abort.
11:8	RO	0x0	reserved
7	RO	0x0	ch_rdwr_err to perform a secure read or secure write: 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to perform a secure read or secure write This fault is a precise abort.
6	RO	0x0	ch_periph_err DMASTP, or DMAFLUSHP with inappropriate security permissions: 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to execute either: o DMAWFP to wait for a secure peripheral o DMALDP or DMASTP to notify a secure peripheral o DMAFLUSHP to flush a secure peripheral This fault is a precise abort.
5	RO	0x0	ch_event_err 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to execute either: o DMAWFE to wait for a secure event o DMASEV to create a secure event or secure interrupt This fault is a precise abort.
4:2	RO	0x0	reserved
1	RO	0x0	operand_invalid valid for the configuration of the DMAC: 1'b0: valid operand 1'b1: invalid operand This fault is a precise abort.
0	RO	0x0	undef_instr 1'b0: defined instruction 1'b1: undefined instruction This fault is a precise abort.

DMA_FTR5

Address: **Operational Base** + offset (0x0054)

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Bit	Attr	Reset Value	Description
31	RO	0x0	lockup_err 1'b0: DMA channel has adequate resources 1'b1: DMA channel has locked-up because of insufficient resources This fault is an imprecise abort.
30	RO	0x0	dbg_instr memory or from the debug interface: 1'b0: instruction that generated an abort was read from system memory 1'b1: instruction that generated an abort was read from the debug interface This fault is an imprecise abort but the bit is only valid when a precise abort occurs.
29:19	RO	0x000	reserved
18	RO	0x0	data_read_err thread performs a data read: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
17	RO	0x0	data_write_err thread performs a data write: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
16	RO	0x0	instr_fetch_err thread performs an instruction fetch: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is a precise abort.
15:14	RO	0x0	reserved
13	RO	0x0	st_data_unavailable 1'b0: MFIFO contains all the data to enable the DMAST to complete 1'b1: previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete This fault is a precise abort.
12	RO	0x0	mfifo_err DMALD 1'b0: MFIFO contains sufficient space 1'b1: MFIFO is too small to hold the data that DMALD requires DMAST 1'b0: MFIFO contains sufficient data 1'b1: MFIFO is too small to store the data to enable DMAST to complete This fault is an imprecise abort.
11:8	RO	0x0	reserved
7	RO	0x0	ch_rdwr_err to perform a secure read or secure write: 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to perform a secure read or secure write This fault is a precise abort.

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Bit	Attr	Reset Value	Description
6	RO	0x0	ch_periph_err DMASTP, or DMAFLUSHP with inappropriate security permissions: 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to execute either: o DMAWFP to wait for a secure peripheral o DMALDP or DMASTP to notify a secure peripheral o DMAFLUSHP to flush a secure peripheral This fault is a precise abort.
5	RO	0x0	ch_event_err 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to execute either: o DMAWFE to wait for a secure event o DMASEV to create a secure event or secure interrupt This fault is a precise abort.
4:2	RO	0x0	reserved
1	RO	0x0	operand_invalid valid for the configuration of the DMAC: 1'b0: valid operand 1'b1: invalid operand This fault is a precise abort.
0	RO	0x0	undef_instr 1'b0: defined instruction 1'b1: undefined instruction This fault is a precise abort.

DMA_FTR6

Address: **Operational Base** + offset (0x0058)

Bit	Attr	Reset Value	Description
31	RO	0x0	lockup_err 1'b0: DMA channel has adequate resources 1'b1: DMA channel has locked-up because of insufficient resources This fault is an imprecise abort.
30	RO	0x0	dbg_instr memory or from the debug interface: 1'b0: instruction that generated an abort was read from system memory 1'b1: instruction that generated an abort was read from the debug interface This fault is an imprecise abort but the bit is only valid when a precise abort occurs.
29:19	RO	0x000	reserved
18	RO	0x0	data_read_err thread performs a data read: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
17	RO	0x0	data_write_err thread performs a data write: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.

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Bit	Attr	Reset Value	Description
16	RO	0x0	instr_fetch_err thread performs an instruction fetch: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is a precise abort.
15:14	RO	0x0	reserved
13	RO	0x0	st_data_unavailable 1'b0: MFIFO contains all the data to enable the DMAST to complete 1'b1: previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete This fault is a precise abort.
12	RO	0x0	mfifo_err DMALD 1'b0: MFIFO contains sufficient space 1'b1: MFIFO is too small to hold the data that DMALD requires DMAST 1'b0: MFIFO contains sufficient data 1'b1: MFIFO is too small to store the data to enable DMAST to complete This fault is an imprecise abort.
11:8	RO	0x0	reserved
7	RO	0x0	ch_rdwr_err to perform a secure read or secure write: 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to perform a secure read or secure write This fault is a precise abort.
6	RO	0x0	ch_periph_err DMASTP, or DMAFLUSHP with inappropriate security permissions: 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to execute either: o DMAWFP to wait for a secure peripheral o DMALDP or DMASTP to notify a secure peripheral o DMAFLUSHP to flush a secure peripheral This fault is a precise abort.
5	RO	0x0	ch_event_err 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to execute either: o DMAWFE to wait for a secure event o DMASEV to create a secure event or secure interrupt This fault is a precise abort.
4:2	RO	0x0	reserved
1	RO	0x0	operand_invalid valid for the configuration of the DMAC: 1'b0: valid operand 1'b1: invalid operand This fault is a precise abort.

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Bit	Attr	Reset Value	Description
0	RO	0x0	undef_instr 1'b0: defined instruction 1'b1: undefined instruction This fault is a precise abort.

DMA_FTR7

Address: **Operational Base** + offset (0x005C)

Bit	Attr	Reset Value	Description
31	RO	0x0	lockup_err 1'b0: DMA channel has adequate resources 1'b1: DMA channel has locked-up because of insufficient resources This fault is an imprecise abort.
30	RO	0x0	dbg_instr memory or from the debug interface: 1'b0: instruction that generated an abort was read from system memory 1'b1: instruction that generated an abort was read from the debug interface This fault is an imprecise abort but the bit is only valid when a precise abort occurs.
29:19	RO	0x000	reserved
18	RO	0x0	data_read_err thread performs a data read: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
17	RO	0x0	data_write_err thread performs a data write: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
16	RO	0x0	instr_fetch_err thread performs an instruction fetch: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is a precise abort.
15:14	RO	0x0	reserved
13	RO	0x0	st_data_unavailable 1'b0: MFIFO contains all the data to enable the DMAST to complete 1'b1: previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete This fault is a precise abort.
12	RO	0x0	mfifo_err DMALD 1'b0: MFIFO contains sufficient space 1'b1: MFIFO is too small to hold the data that DMALD requires DMAST 1'b0: MFIFO contains sufficient data 1'b1: MFIFO is too small to store the data to enable DMAST to complete This fault is an imprecise abort.
11:8	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
7	RO	0x0	ch_rdwr_err to perform a secure read or secure write: 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to perform a secure read or secure write This fault is a precise abort.
6	RO	0x0	ch_periph_err DMASTP, or DMAFLUSHP with inappropriate security permissions: 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to execute either: o DMAWFP to wait for a secure peripheral o DMALDP or DMASTP to notify a secure peripheral o DMAFLUSHP to flush a secure peripheral This fault is a precise abort.
5	RO	0x0	ch_event_err 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to execute either: o DMAWFE to wait for a secure event o DMASEV to create a secure event or secure interrupt This fault is a precise abort.
4:2	RO	0x0	reserved
1	RO	0x0	operand_invalid valid for the configuration of the DMAC: 1'b0: valid operand 1'b1: invalid operand This fault is a precise abort.
0	RO	0x0	undef_instr 1'b0: defined instruction 1'b1: undefined instruction This fault is a precise abort.

DMA_CSR0

Address: **Operational Base** + offset (0x0100)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RO	0x0	cns 1'b0: DMA channel operates in the Secure state 1'b1: DMA channel operates in the Non-secure state
20:16	RO	0x00	reserved
15	RO	0x0	dmawfp_periph 1'b0: DMAWFP executed with the periph operand not set 1'b1: DMAWFP executed with the periph operand set
14	RO	0x0	dmawfp_b_ns 1'b0: DMAWFP executed with the single operand set 1'b1: DMAWFP executed with the burst operand set
13:9	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
8:4	RO	0x00	wakeup_number indicate the event or peripheral number that the channel is waiting for: 5'b00000: DMA channel is waiting for event, or peripheral, 0 5'b00001: DMA channel is waiting for event, or peripheral, 1 5'b00010: DMA channel is waiting for event, or peripheral, 2 5'b11111: DMA channel is waiting for event, or peripheral, 31
3:0	RO	0x0	channel_status 4'b0000: Stopped 4'b0001: Executing 4'b0010: Cache miss 4'b0011: Updating PC 4'b0100: Waiting for event 4'b0101: At barrier 4'b0110: reserved 4'b0111: Waiting for peripheral 4'b1000: Killing 4'b1001: Completing b1010-b1101 = reserved b1110 = Faulting completing b1111 = Faulting

DMA_CPC0

Address: **Operational Base** + offset (0x0104)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pc_chnl Program counter for the DMA channel 0 thread

DMA_CSR1

Address: **Operational Base** + offset (0x0108)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RO	0x0	cns 1'b0: DMA channel operates in the Secure state 1'b1: DMA channel operates in the Non-secure state
20:16	RO	0x00	reserved
15	RO	0x0	dmawfp_periph 1'b0: DMAWFP executed with the periph operand not set 1'b1: DMAWFP executed with the periph operand set
14	RO	0x0	dmawfp_b_ns 1'b0: DMAWFP executed with the single operand set 1'b1: DMAWFP executed with the burst operand set
13:9	RO	0x00	reserved
8:4	RO	0x00	wakeup_number indicate the event or peripheral number that the channel is waiting for: 5'b00000: DMA channel is waiting for event, or peripheral, 0 5'b00001: DMA channel is waiting for event, or peripheral, 1 5'b00010: DMA channel is waiting for event, or peripheral, 2 5'b11111: DMA channel is waiting for event, or peripheral, 31

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Bit	Attr	Reset Value	Description
3:0	RO	0x0	channel_status 4'b0000: Stopped 4'b0001: Executing 4'b0010: Cache miss 4'b0011: Updating PC 4'b0100: Waiting for event 4'b0101: At barrier 4'b0110: reserved 4'b0111: Waiting for peripheral 4'b1000: Killing 4'b1001: Completing b1010-b1101 = reserved b1110 = Faulting completing b1111 = Faulting

DMA_CPC1

Address: **Operational Base** + offset (0x010C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pc_chnl Program counter for the DMA channel 1 thread

DMA_CSR2

Address: **Operational Base** + offset (0x0110)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RO	0x0	cns 1'b0: DMA channel operates in the Secure state 1'b1: DMA channel operates in the Non-secure state
20:16	RO	0x00	reserved
15	RO	0x0	dmawfp_periph 1'b0: DMAWFP executed with the periph operand not set 1'b1: DMAWFP executed with the periph operand set
14	RO	0x0	dmawfp_b_ns 1'b0: DMAWFP executed with the single operand set 1'b1: DMAWFP executed with the burst operand set
13:9	RO	0x00	reserved
8:4	RO	0x00	wakeup_number indicate the event or peripheral number that the channel is waiting for: 5'b00000: DMA channel is waiting for event, or peripheral, 0 5'b00001: DMA channel is waiting for event, or peripheral, 1 5'b00010: DMA channel is waiting for event, or peripheral, 2 5'b11111: DMA channel is waiting for event, or peripheral, 31

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Bit	Attr	Reset Value	Description
3:0	RO	0x0	channel_status 4'b0000: Stopped 4'b0001: Executing 4'b0010: Cache miss 4'b0011: Updating PC 4'b0100: Waiting for event 4'b0101: At barrier 4'b0110: reserved 4'b0111: Waiting for peripheral 4'b1000: Killing 4'b1001: Completing b1010-b1101 = reserved b1110 = Faulting completing b1111 = Faulting

DMA_CPC2

Address: **Operational Base** + offset (0x0114)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pc_chnl Program counter for the DMA channel 2 thread

DMA_CSR3

Address: **Operational Base** + offset (0x0118)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RO	0x0	cns 1'b0: DMA channel operates in the Secure state 1'b1: DMA channel operates in the Non-secure state
20:16	RO	0x00	reserved
15	RO	0x0	dmawfp_periph 1'b0: DMAWFP executed with the periph operand not set 1'b1: DMAWFP executed with the periph operand set
14	RO	0x0	dmawfp_b_ns 1'b0: DMAWFP executed with the single operand set 1'b1: DMAWFP executed with the burst operand set
13:9	RO	0x00	reserved
8:4	RO	0x00	wakeup_number indicate the event or peripheral number that the channel is waiting for: 5'b00000: DMA channel is waiting for event, or peripheral, 0 5'b00001: DMA channel is waiting for event, or peripheral, 1 5'b00010: DMA channel is waiting for event, or peripheral, 2 5'b11111: DMA channel is waiting for event, or peripheral, 31

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Bit	Attr	Reset Value	Description
3:0	RO	0x0	channel_status 4'b0000: Stopped 4'b0001: Executing 4'b0010: Cache miss 4'b0011: Updating PC 4'b0100: Waiting for event 4'b0101: At barrier 4'b0110: reserved 4'b0111: Waiting for peripheral 4'b1000: Killing 4'b1001: Completing b1010-b1101 = reserved b1110 = Faulting completing b1111 = Faulting

DMA_CPC3

Address: **Operational Base** + offset (0x011C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pc_chnl Program counter for the DMA channel 3 thread

DMA_CSR4

Address: **Operational Base** + offset (0x0120)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RO	0x0	cns 1'b0: DMA channel operates in the Secure state 1'b1: DMA channel operates in the Non-secure state
20:16	RO	0x00	reserved
15	RO	0x0	dmawfp_periph 1'b0: DMAWFP executed with the periph operand not set 1'b1: DMAWFP executed with the periph operand set
14	RO	0x0	dmawfp_b_ns 1'b0: DMAWFP executed with the single operand set 1'b1: DMAWFP executed with the burst operand set
13:9	RO	0x00	reserved
8:4	RO	0x00	wakeup_number indicate the event or peripheral number that the channel is waiting for: 5'b00000: DMA channel is waiting for event, or peripheral, 0 5'b00001: DMA channel is waiting for event, or peripheral, 1 5'b00010: DMA channel is waiting for event, or peripheral, 2 5'b11111: DMA channel is waiting for event, or peripheral, 31

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Bit	Attr	Reset Value	Description
3:0	RO	0x0	channel_status 4'b0000: Stopped 4'b0001: Executing 4'b0010: Cache miss 4'b0011: Updating PC 4'b0100: Waiting for event 4'b0101: At barrier 4'b0110: reserved 4'b0111: Waiting for peripheral 4'b1000: Killing 4'b1001: Completing b1010-b1101 = reserved b1110 = Faulting completing b1111 = Faulting

DMA_CPC4

Address: **Operational Base** + offset (0x0124)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pc_chnl Program counter for the DMA channel 4 thread

DMA_CSR5

Address: **Operational Base** + offset (0x0128)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RO	0x0	cns 1'b0: DMA channel operates in the Secure state 1'b1: DMA channel operates in the Non-secure state
20:16	RO	0x00	reserved
15	RO	0x0	dmawfp_periph 1'b0: DMAWFP executed with the periph operand not set 1'b1: DMAWFP executed with the periph operand set
14	RO	0x0	dmawfp_b_ns 1'b0: DMAWFP executed with the single operand set 1'b1: DMAWFP executed with the burst operand set
13:9	RO	0x00	reserved
8:4	RO	0x00	wakeup_number indicate the event or peripheral number that the channel is waiting for: 5'b00000: DMA channel is waiting for event, or peripheral, 0 5'b00001: DMA channel is waiting for event, or peripheral, 1 5'b00010: DMA channel is waiting for event, or peripheral, 2 5'b11111: DMA channel is waiting for event, or peripheral, 31

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Bit	Attr	Reset Value	Description
3:0	RO	0x0	channel_status 4'b0000: Stopped 4'b0001: Executing 4'b0010: Cache miss 4'b0011: Updating PC 4'b0100: Waiting for event 4'b0101: At barrier 4'b0110: reserved 4'b0111: Waiting for peripheral 4'b1000: Killing 4'b1001: Completing b1010-b1101 = reserved b1110 = Faulting completing b1111 = Faulting

DMA_CPC5

Address: **Operational Base** + offset (0x012C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pc_chnl Program counter for the DMA channel 5 thread

DMA_CSR6

Address: **Operational Base** + offset (0x0130)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RO	0x0	cns 1'b0: DMA channel operates in the Secure state 1'b1: DMA channel operates in the Non-secure state
20:16	RO	0x00	reserved
15	RO	0x0	dmawfp_periph 1'b0: DMAWFP executed with the periph operand not set 1'b1: DMAWFP executed with the periph operand set
14	RO	0x0	dmawfp_b_ns 1'b0: DMAWFP executed with the single operand set 1'b1: DMAWFP executed with the burst operand set
13:9	RO	0x00	reserved
8:4	RO	0x00	wakeup_number indicate the event or peripheral number that the channel is waiting for: 5'b00000: DMA channel is waiting for event, or peripheral, 0 5'b00001: DMA channel is waiting for event, or peripheral, 1 5'b00010: DMA channel is waiting for event, or peripheral, 2 5'b11111: DMA channel is waiting for event, or peripheral, 31

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Bit	Attr	Reset Value	Description
3:0	RO	0x0	channel_status 4'b0000: Stopped 4'b0001: Executing 4'b0010: Cache miss 4'b0011: Updating PC 4'b0100: Waiting for event 4'b0101: At barrier 4'b0110: reserved 4'b0111: Waiting for peripheral 4'b1000: Killing 4'b1001: Completing b1010-b1101 = reserved b1110 = Faulting completing b1111 = Faulting

DMA_CPC6

Address: **Operational Base** + offset (0x0134)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pc_chnl Program counter for the DMA channel 6 thread

DMA_CSR7

Address: **Operational Base** + offset (0x0138)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RO	0x0	cns 1'b0: DMA channel operates in the Secure state 1'b1: DMA channel operates in the Non-secure state
20:16	RO	0x00	reserved
15	RO	0x0	dmawfp_periph 1'b0: DMAWFP executed with the periph operand not set 1'b1: DMAWFP executed with the periph operand set
14	RO	0x0	dmawfp_b_ns 1'b0: DMAWFP executed with the single operand set 1'b1: DMAWFP executed with the burst operand set
13:9	RO	0x00	reserved
8:4	RO	0x00	wakeup_number indicate the event or peripheral number that the channel is waiting for: 5'b00000: DMA channel is waiting for event, or peripheral, 0 5'b00001: DMA channel is waiting for event, or peripheral, 1 5'b00010: DMA channel is waiting for event, or peripheral, 2 5'b11111: DMA channel is waiting for event, or peripheral, 31

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Bit	Attr	Reset Value	Description
3:0	RO	0x0	channel_status 4'b0000: Stopped 4'b0001: Executing 4'b0010: Cache miss 4'b0011: Updating PC 4'b0100: Waiting for event 4'b0101: At barrier 4'b0110: reserved 4'b0111: Waiting for peripheral 4'b1000: Killing 4'b1001: Completing b1010-b1101 = reserved b1110 = Faulting completing b1111 = Faulting

DMA_CPC7

Address: **Operational Base** + offset (0x013C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pc_chnl Program counter for the DMA channel 7 thread

DMA_SAR0

Address: **Operational Base** + offset (0x0400)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	src_addr Address of the source data for DMA channel 0

DMA_DAR0

Address: **Operational Base** + offset (0x0404)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dst_addr Address of the Destinationdata for DMA channel 0

DMA_CCR0

Address: **Operational Base** + offset (0x0408)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:25	RO	0x0	dst_cache_ctrl Bit [27] 1'b0: AWCACHE[3] is LOW 1'b1: AWCACHE[3] is HIGH Bit [26] 1'b0: AWCACHE[1] is LOW 1'b1: AWCACHE[1] is HIGH Bit [25] 1'b0: AWCACHE[0] is LOW 1'b1: AWCACHE[0] is HIGH

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Bit	Attr	Reset Value	Description
24:22	RO	0x0	dst_prot_ctrl Bit [24] 1'b0: AWPROT[2] is LOW 1'b1: AWPROT[2] is HIGH Bit [23] 1'b0: AWPROT[1] is LOW 1'b1: AWPROT[1] is HIGH Bit [22] 1'b0: AWPROT[0] is LOW 1'b1: AWPROT[0] is HIGH
21:18	RO	0x0	dst_burst_len the destination data: 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers 4'b1111: 16 data transfers The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
17:15	RO	0x0	dst_burst_size 3'b000: writes 1 byte per beat 3'b001: writes 2 bytes per beat 3'b010: writes 4 bytes per beat 3'b011: writes 8 bytes per beat 3'b100: writes 16 bytes per beat 3'b101-3'b111: reserved The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
14	RO	0x0	dst_inc 1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH.
13:11	RO	0x0	src_cache_ctrl Bit [13] 1'b0: ARCACHE[2] is LOW 1'b1: ARCACHE[2] is HIGH Bit [12] 1'b0: ARCACHE[1] is LOW 1'b1: ARCACHE[1] is HIGH Bit [11] 1'b0: ARCACHE[0] is LOW 1'b1: ARCACHE[0] is HIGH
10:8	RO	0x0	src_prot_ctrl Bit [10] 1'b0: ARPROT[2] is LOW 1'b1: ARPROT[2] is HIGH Bit [9] 1'b0: ARPROT[1] is LOW 1'b1: ARPROT[1] is HIGH Bit [8] 1'b0: ARPROT[0] is LOW 1'b1: ARPROT[0] is HIGH

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Bit	Attr	Reset Value	Description
7:4	RO	0x0	src_burst_len 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers 4'b1111: 16 data transfers The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
3:1	RO	0x0	src_burst_size 3'b000: reads 1 byte per beat 3'b001: reads 2 bytes per beat 3'b010: reads 4 bytes per beat 3'b011: reads 8 bytes per beat 3'b100: reads 16 bytes per beat 3'b101-3'b111: reserved The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
0	RO	0x0	src_inc 1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH.

DMA_LC0_0

Address: **Operational Base** + offset (0x040C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 0 iterations

DMA_LC1_0

Address: **Operational Base** + offset (0x0410)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 1 iterations

DMA_SAR1

Address: **Operational Base** + offset (0x0420)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	src_addr Address of the source data for DMA channel 1

DMA_DAR1

Address: **Operational Base** + offset (0x0424)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dst_addr Address of the Destinationdata for DMA channel 1

DMA_CCR1

Address: **Operational Base** + offset (0x0428)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:25	RO	0x0	dst_cache_ctrl Bit [27] 1'b0: AWCACHE[3] is LOW 1'b1: AWCACHE[3] is HIGH Bit [26] 1'b0: AWCACHE[1] is LOW 1'b1: AWCACHE[1] is HIGH Bit [25] 1'b0: AWCACHE[0] is LOW 1'b1: AWCACHE[0] is HIGH
24:22	RO	0x0	dst_prot_ctrl Bit [24] 1'b0: AWPROT[2] is LOW 1'b1: AWPROT[2] is HIGH Bit [23] 1'b0: AWPROT[1] is LOW 1'b1: AWPROT[1] is HIGH Bit [22] 1'b0: AWPROT[0] is LOW 1'b1: AWPROT[0] is HIGH
21:18	RO	0x0	dst_burst_len the destination data: 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers 4'b1111: 16 data transfers The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
17:15	RO	0x0	dst_burst_size 3'b000: writes 1 byte per beat 3'b001: writes 2 bytes per beat 3'b010: writes 4 bytes per beat 3'b011: writes 8 bytes per beat 3'b100: writes 16 bytes per beat 3'b101-3'b111: reserved The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
14	RO	0x0	dst_inc 1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH.
13:11	RO	0x0	src_cache_ctrl Bit [13] 1'b0: ARCACHE[2] is LOW 1'b1: ARCACHE[2] is HIGH Bit [12] 1'b0: ARCACHE[1] is LOW 1'b1: ARCACHE[1] is HIGH Bit [11] 1'b0: ARCACHE[0] is LOW 1'b1: ARCACHE[0] is HIGH

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Bit	Attr	Reset Value	Description
10:8	RO	0x0	src_prot_ctrl Bit [10] 1'b0: ARPROT[2] is LOW 1'b1: ARPROT[2] is HIGH Bit [9] 1'b0: ARPROT[1] is LOW 1'b1: ARPROT[1] is HIGH Bit [8] 1'b0: ARPROT[0] is LOW 1'b1: ARPROT[0] is HIGH
7:4	RO	0x0	src_burst_len 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers 4'b1111: 16 data transfers The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
3:1	RO	0x0	src_burst_size 3'b000: reads 1 byte per beat 3'b001: reads 2 bytes per beat 3'b010: reads 4 bytes per beat 3'b011: reads 8 bytes per beat 3'b100: reads 16 bytes per beat 3'b101-3'b111: reserved The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
0	RO	0x0	src_inc 1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH.

DMA_LC0_1

Address: **Operational Base** + offset (0x042C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 0 iterations

DMA_LC1_1

Address: **Operational Base** + offset (0x0430)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 1 iterations

DMA_SAR2

Address: **Operational Base** + offset (0x0440)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	src_addr Address of the source data for DMA channel 2

DMA_DAR2

Address: **Operational Base** + offset (0x0444)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dst_addr Address of the Destinationdata for DMA channel 2

DMA_CCR2

Address: **Operational Base** + offset (0x0448)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:25	RO	0x0	dst_cache_ctrl Bit [27] 1'b0: AWCACHE[3] is LOW 1'b1: AWCACHE[3] is HIGH Bit [26] 1'b0: AWCACHE[1] is LOW 1'b1: AWCACHE[1] is HIGH Bit [25] 1'b0: AWCACHE[0] is LOW 1'b1: AWCACHE[0] is HIGH
24:22	RO	0x0	dst_prot_ctrl Bit [24] 1'b0: AWPROT[2] is LOW 1'b1: AWPROT[2] is HIGH Bit [23] 1'b0: AWPROT[1] is LOW 1'b1: AWPROT[1] is HIGH Bit [22] 1'b0: AWPROT[0] is LOW 1'b1: AWPROT[0] is HIGH
21:18	RO	0x0	dst_burst_len the destination data: 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers 4'b1111: 16 data transfers The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
17:15	RO	0x0	dst_burst_size 3'b000: writes 1 byte per beat 3'b001: writes 2 bytes per beat 3'b010: writes 4 bytes per beat 3'b011: writes 8 bytes per beat 3'b100: writes 16 bytes per beat 3'b101-3'b111: reserved The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
14	RO	0x0	dst_inc 1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH.

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Bit	Attr	Reset Value	Description
13:11	RO	0x0	src_cache_ctrl Bit [13] 1'b0: ARCACHE[2] is LOW 1'b1: ARCACHE[2] is HIGH Bit [12] 1'b0: ARCACHE[1] is LOW 1'b1: ARCACHE[1] is HIGH Bit [11] 1'b0: ARCACHE[0] is LOW 1'b1: ARCACHE[0] is HIGH
10:8	RO	0x0	src_prot_ctrl Bit [10] 1'b0: ARPROT[2] is LOW 1'b1: ARPROT[2] is HIGH Bit [9] 1'b0: ARPROT[1] is LOW 1'b1: ARPROT[1] is HIGH Bit [8] 1'b0: ARPROT[0] is LOW 1'b1: ARPROT[0] is HIGH
7:4	RO	0x0	src_burst_len 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers 4'b1111: 16 data transfers The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
3:1	RO	0x0	src_burst_size 3'b000: reads 1 byte per beat 3'b001: reads 2 bytes per beat 3'b010: reads 4 bytes per beat 3'b011: reads 8 bytes per beat 3'b100: reads 16 bytes per beat 3'b101-3'b111: reserved The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
0	RO	0x0	src_inc 1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH.

DMA_LC0_2

Address: **Operational Base** + offset (0x044C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 0 iterations

DMA_LC1_2

Address: **Operational Base** + offset (0x0450)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 1 iterations

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DMA_SAR3

Address: **Operational Base** + offset (0x0460)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	src_addr Address of the source data for DMA channel 3

DMA_DAR3

Address: **Operational Base** + offset (0x0464)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dst_addr Address of the Destinationdata for DMA channel 3

DMA_CCR3

Address: **Operational Base** + offset (0x0468)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:25	RO	0x0	dst_cache_ctrl Bit [27] 1'b0: AWCACHE[3] is LOW 1'b1: AWCACHE[3] is HIGH Bit [26] 1'b0: AWCACHE[1] is LOW 1'b1: AWCACHE[1] is HIGH Bit [25] 1'b0: AWCACHE[0] is LOW 1'b1: AWCACHE[0] is HIGH
24:22	RO	0x0	dst_prot_ctrl Bit [24] 1'b0: AWPROT[2] is LOW 1'b1: AWPROT[2] is HIGH Bit [23] 1'b0: AWPROT[1] is LOW 1'b1: AWPROT[1] is HIGH Bit [22] 1'b0: AWPROT[0] is LOW 1'b1: AWPROT[0] is HIGH
21:18	RO	0x0	dst_burst_len the destination data: 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers 4'b1111: 16 data transfers The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
17:15	RO	0x0	dst_burst_size 3'b000: writes 1 byte per beat 3'b001: writes 2 bytes per beat 3'b010: writes 4 bytes per beat 3'b011: writes 8 bytes per beat 3'b100: writes 16 bytes per beat 3'b101-3'b111: reserved The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.

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Bit	Attr	Reset Value	Description
14	RO	0x0	dst_inc 1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH.
13:11	RO	0x0	src_cache_ctrl Bit [13] 1'b0: ARCACHE[2] is LOW 1'b1: ARCACHE[2] is HIGH Bit [12] 1'b0: ARCACHE[1] is LOW 1'b1: ARCACHE[1] is HIGH Bit [11] 1'b0: ARCACHE[0] is LOW 1'b1: ARCACHE[0] is HIGH
10:8	RO	0x0	src_prot_ctrl Bit [10] 1'b0: ARPROT[2] is LOW 1'b1: ARPROT[2] is HIGH Bit [9] 1'b0: ARPROT[1] is LOW 1'b1: ARPROT[1] is HIGH Bit [8] 1'b0: ARPROT[0] is LOW 1'b1: ARPROT[0] is HIGH
7:4	RO	0x0	src_burst_len 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers 4'b1111: 16 data transfers The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
3:1	RO	0x0	src_burst_size 3'b000: reads 1 byte per beat 3'b001: reads 2 bytes per beat 3'b010: reads 4 bytes per beat 3'b011: reads 8 bytes per beat 3'b100: reads 16 bytes per beat 3'b101-3'b111: reserved The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
0	RO	0x0	src_inc 1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH.

DMA_LC0_3

Address: **Operational Base** + offset (0x046C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 0 iterations

DMA_LC1_3

Address: **Operational Base** + offset (0x0470)

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Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 1 iterations

DMA_SAR4

Address: **Operational Base** + offset (0x0480)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	src_addr Address of the source data for DMA channel 4

DMA_DAR4

Address: **Operational Base** + offset (0x0484)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dst_addr Address of the Destinationdata for DMA channel 4

DMA_CCR4

Address: **Operational Base** + offset (0x0488)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:25	RO	0x0	dst_cache_ctrl Bit [27] 1'b0: AWCACHE[3] is LOW 1'b1: AWCACHE[3] is HIGH Bit [26] 1'b0: AWCACHE[1] is LOW 1'b1: AWCACHE[1] is HIGH Bit [25] 1'b0: AWCACHE[0] is LOW 1'b1: AWCACHE[0] is HIGH
24:22	RO	0x0	dst_prot_ctrl Bit [24] 1'b0: AWPROT[2] is LOW 1'b1: AWPROT[2] is HIGH Bit [23] 1'b0: AWPROT[1] is LOW 1'b1: AWPROT[1] is HIGH Bit [22] 1'b0: AWPROT[0] is LOW 1'b1: AWPROT[0] is HIGH
21:18	RO	0x0	dst_burst_len the destination data: 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers 4'b1111: 16 data transfers The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.

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Bit	Attr	Reset Value	Description
17:15	RO	0x0	dst_burst_size 3'b000: writes 1 byte per beat 3'b001: writes 2 bytes per beat 3'b010: writes 4 bytes per beat 3'b011: writes 8 bytes per beat 3'b100: writes 16 bytes per beat 3'b101-3'b111: reserved The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
14	RO	0x0	dst_inc 1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH.
13:11	RO	0x0	src_cache_ctrl Bit [13] 1'b0: ARCACHE[2] is LOW 1'b1: ARCACHE[2] is HIGH Bit [12] 1'b0: ARCACHE[1] is LOW 1'b1: ARCACHE[1] is HIGH Bit [11] 1'b0: ARCACHE[0] is LOW 1'b1: ARCACHE[0] is HIGH
10:8	RO	0x0	src_prot_ctrl Bit [10] 1'b0: ARPROT[2] is LOW 1'b1: ARPROT[2] is HIGH Bit [9] 1'b0: ARPROT[1] is LOW 1'b1: ARPROT[1] is HIGH Bit [8] 1'b0: ARPROT[0] is LOW 1'b1: ARPROT[0] is HIGH
7:4	RO	0x0	src_burst_len 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers 4'b1111: 16 data transfers The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
3:1	RO	0x0	src_burst_size 3'b000: reads 1 byte per beat 3'b001: reads 2 bytes per beat 3'b010: reads 4 bytes per beat 3'b011: reads 8 bytes per beat 3'b100: reads 16 bytes per beat 3'b101-3'b111: reserved The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
0	RO	0x0	src_inc 1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH.

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DMA_LC0_4

Address: **Operational Base** + offset (0x048C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 0 iterations

DMA_LC1_4

Address: **Operational Base** + offset (0x0490)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 1 iterations

DMA_SAR5

Address: **Operational Base** + offset (0x04A0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	src_addr Address of the source data for DMA channel 5

DMA_DAR5

Address: **Operational Base** + offset (0x04A4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dst_addr Address of the Destinationdata for DMA channel 5

DMA_CCR5

Address: **Operational Base** + offset (0x04A8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:25	RO	0x0	dst_cache_ctrl Bit [27] 1'b0: AWCACHE[3] is LOW 1'b1: AWCACHE[3] is HIGH Bit [26] 1'b0: AWCACHE[1] is LOW 1'b1: AWCACHE[1] is HIGH Bit [25] 1'b0: AWCACHE[0] is LOW 1'b1: AWCACHE[0] is HIGH
24:22	RO	0x0	dst_prot_ctrl Bit [24] 1'b0: AWPROT[2] is LOW 1'b1: AWPROT[2] is HIGH Bit [23] 1'b0: AWPROT[1] is LOW 1'b1: AWPROT[1] is HIGH Bit [22] 1'b0: AWPROT[0] is LOW 1'b1: AWPROT[0] is HIGH

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Bit	Attr	Reset Value	Description
21:18	RO	0x0	dst_burst_len the destination data: 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers 4'b1111: 16 data transfers The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
17:15	RO	0x0	dst_burst_size 3'b000: writes 1 byte per beat 3'b001: writes 2 bytes per beat 3'b010: writes 4 bytes per beat 3'b011: writes 8 bytes per beat 3'b100: writes 16 bytes per beat 3'b101-3'b111: reserved The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
14	RO	0x0	dst_inc 1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH.
13:11	RO	0x0	src_cache_ctrl Bit [13] 1'b0: ARCACHE[2] is LOW 1'b1: ARCACHE[2] is HIGH Bit [12] 1'b0: ARCACHE[1] is LOW 1'b1: ARCACHE[1] is HIGH Bit [11] 1'b0: ARCACHE[0] is LOW 1'b1: ARCACHE[0] is HIGH
10:8	RO	0x0	src_prot_ctrl Bit [10] 1'b0: ARPROT[2] is LOW 1'b1: ARPROT[2] is HIGH Bit [9] 1'b0: ARPROT[1] is LOW 1'b1: ARPROT[1] is HIGH Bit [8] 1'b0: ARPROT[0] is LOW 1'b1: ARPROT[0] is HIGH
7:4	RO	0x0	src_burst_len 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers 4'b1111: 16 data transfers The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.

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Bit	Attr	Reset Value	Description
3:1	RO	0x0	src_burst_size 3'b000: reads 1 byte per beat 3'b001: reads 2 bytes per beat 3'b010: reads 4 bytes per beat 3'b011: reads 8 bytes per beat 3'b100: reads 16 bytes per beat 3'b101-3'b111: reserved The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
0	RO	0x0	src_inc 1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH.

DMA_LC0_5

Address: **Operational Base** + offset (0x04AC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 0 iterations

DMA_LC1_5

Address: **Operational Base** + offset (0x04B0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 1 iterations

DMA_SAR6

Address: **Operational Base** + offset (0x04C0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	src_addr Address of the source data for DMA channel 6

DMA_DAR6

Address: **Operational Base** + offset (0x04C4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dst_addr Address of the Destinationdata for DMA channel 6

DMA_CCR6

Address: **Operational Base** + offset (0x04C8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:25	RO	0x0	dst_cache_ctrl Bit [27] 1'b0: AWCACHE[3] is LOW 1'b1: AWCACHE[3] is HIGH Bit [26] 1'b0: AWCACHE[1] is LOW 1'b1: AWCACHE[1] is HIGH Bit [25] 1'b0: AWCACHE[0] is LOW 1'b1: AWCACHE[0] is HIGH

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Bit	Attr	Reset Value	Description
24:22	RO	0x0	dst_prot_ctrl Bit [24] 1'b0: AWPROT[2] is LOW 1'b1: AWPROT[2] is HIGH Bit [23] 1'b0: AWPROT[1] is LOW 1'b1: AWPROT[1] is HIGH Bit [22] 1'b0: AWPROT[0] is LOW 1'b1: AWPROT[0] is HIGH
21:18	RO	0x0	dst_burst_len the destination data: 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers 4'b1111: 16 data transfers The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
17:15	RO	0x0	dst_burst_size 3'b000: writes 1 byte per beat 3'b001: writes 2 bytes per beat 3'b010: writes 4 bytes per beat 3'b011: writes 8 bytes per beat 3'b100: writes 16 bytes per beat 3'b101-3'b111: reserved The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
14	RO	0x0	dst_inc 1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH.
13:11	RO	0x0	src_cache_ctrl Bit [13] 1'b0: ARCACHE[2] is LOW 1'b1: ARCACHE[2] is HIGH Bit [12] 1'b0: ARCACHE[1] is LOW 1'b1: ARCACHE[1] is HIGH Bit [11] 1'b0: ARCACHE[0] is LOW 1'b1: ARCACHE[0] is HIGH
10:8	RO	0x0	src_prot_ctrl Bit [10] 1'b0: ARPROT[2] is LOW 1'b1: ARPROT[2] is HIGH Bit [9] 1'b0: ARPROT[1] is LOW 1'b1: ARPROT[1] is HIGH Bit [8] 1'b0: ARPROT[0] is LOW 1'b1: ARPROT[0] is HIGH

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Bit	Attr	Reset Value	Description
7:4	RO	0x0	src_burst_len 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers 4'b1111: 16 data transfers The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
3:1	RO	0x0	src_burst_size 3'b000: reads 1 byte per beat 3'b001: reads 2 bytes per beat 3'b010: reads 4 bytes per beat 3'b011: reads 8 bytes per beat 3'b100: reads 16 bytes per beat 3'b101-3'b111: reserved The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
0	RO	0x0	src_inc 1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH.

DMA_LC0_6

Address: **Operational Base** + offset (0x04CC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 0 iterations

DMA_LC1_6

Address: **Operational Base** + offset (0x04D0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 1 iterations

DMA_SAR7

Address: **Operational Base** + offset (0x04E0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	src_addr Address of the source data for DMA channel 7

DMA_DAR7

Address: **Operational Base** + offset (0x04E4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dst_addr Address of the Destinationdata for DMA channel 7

DMA_CCR7

Address: **Operational Base** + offset (0x04E8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:25	RO	0x0	dst_cache_ctrl Bit [27] 1'b0: AWCACHE[3] is LOW 1'b1: AWCACHE[3] is HIGH Bit [26] 1'b0: AWCACHE[1] is LOW 1'b1: AWCACHE[1] is HIGH Bit [25] 1'b0: AWCACHE[0] is LOW 1'b1: AWCACHE[0] is HIGH
24:22	RO	0x0	dst_prot_ctrl Bit [24] 1'b0: AWPROT[2] is LOW 1'b1: AWPROT[2] is HIGH Bit [23] 1'b0: AWPROT[1] is LOW 1'b1: AWPROT[1] is HIGH Bit [22] 1'b0: AWPROT[0] is LOW 1'b1: AWPROT[0] is HIGH
21:18	RO	0x0	dst_burst_len the destination data: 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers 4'b1111: 16 data transfers The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
17:15	RO	0x0	dst_burst_size 3'b000: writes 1 byte per beat 3'b001: writes 2 bytes per beat 3'b010: writes 4 bytes per beat 3'b011: writes 8 bytes per beat 3'b100: writes 16 bytes per beat 3'b101-3'b111: reserved The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
14	RO	0x0	dst_inc 1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH.
13:11	RO	0x0	src_cache_ctrl Bit [13] 1'b0: ARCACHE[2] is LOW 1'b1: ARCACHE[2] is HIGH Bit [12] 1'b0: ARCACHE[1] is LOW 1'b1: ARCACHE[1] is HIGH Bit [11] 1'b0: ARCACHE[0] is LOW 1'b1: ARCACHE[0] is HIGH

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Bit	Attr	Reset Value	Description
10:8	RO	0x0	src_prot_ctrl Bit [10] 1'b0: ARPROT[2] is LOW 1'b1: ARPROT[2] is HIGH Bit [9] 1'b0: ARPROT[1] is LOW 1'b1: ARPROT[1] is HIGH Bit [8] 1'b0: ARPROT[0] is LOW 1'b1: ARPROT[0] is HIGH
7:4	RO	0x0	src_burst_len 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers 4'b1111: 16 data transfers The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
3:1	RO	0x0	src_burst_size 3'b000: reads 1 byte per beat 3'b001: reads 2 bytes per beat 3'b010: reads 4 bytes per beat 3'b011: reads 8 bytes per beat 3'b100: reads 16 bytes per beat 3'b101-3'b111: reserved The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
0	RO	0x0	src_inc 1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH.

DMA_LC0_7

Address: **Operational Base** + offset (0x04EC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 0 iterations

DMA_LC1_7

Address: **Operational Base** + offset (0x04F0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	loop_counter_iterations Loop counter 1 iterations

DMA_DBGSTATUS

Address: **Operational Base** + offset (0x0D00)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	dbgstatus 1'b0: idle 1'b1: busy

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DMA_DBGCMD

Address: **Operational Base** + offset (0x0D04)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	WO	0x0	dbgcmd 2'b00: execute the instruction that the DBGINST [1:0] Registers contain 2'b01: reserved 2'b10: reserved 2'b11: reserved

DMA_DBGINST0

Address: **Operational Base** + offset (0x0D08)

Bit	Attr	Reset Value	Description
31:24	WO	0x00	instruction_byte1 Instruction byte 1
23:16	WO	0x00	instruction_byte0 Instruction byte 0
15:11	RO	0x00	reserved
10:8	WO	0x0	channel_number 3'b000: DMA channel 0 3'b001: DMA channel 1 3'b010: DMA channel 2 3'b111: DMA channel 7
7:1	RO	0x00	reserved
0	WO	0x0	debug_thread 1'b0: DMA manager thread 1'b1: DMA channel

DMA_DBGINST1

Address: **Operational Base** + offset (0x0D0C)

Bit	Attr	Reset Value	Description
31:24	WO	0x00	instruction_byte5 Instruction byte 5
23:16	WO	0x00	instruction_byte4 Instruction byte 4
15:8	WO	0x00	instruction_byte3 Instruction byte 3
7:0	WO	0x00	instruction_byte2 Instruction byte 2

DMA_CR0

Address: **Operational Base** + offset (0x0E00)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:17	RO	0x0f	num_events 5'b00000: 1 interrupt output, irq[0] 5'b00001: 2 interrupt outputs, irq[1:0] 5'b00010: 3 interrupt outputs, irq[2:0] 5'b11111: 32 interrupt outputs, irq[31:0]
16:12	RO	0x1f	num_periph_req 5'b00000: 1 peripheral request interface 5'b00001: 2 peripheral request interfaces 5'b00010: 3 peripheral request interfaces 5'b11111: 32 peripheral request interfaces
11:7	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
6:4	RO	0x7	num_chnls 3'b000: 1 DMA channel 3'b001: 2 DMA channels 3'b010: 3 DMA channels 3'b111: 8 DMA channels
3	RO	0x0	reserved
2	RO	0x1	mgr_ns_at_rst 1'b0: boot_manager_ns was LOW 1'b1: boot_manager_ns was HIGH
1	RO	0x0	boot_en 1'b0: boot_from_pc was LOW 1'b1: boot_from_pc was HIGH
0	RO	0x1	periph_req 1'b0: the DMAC does not provide a peripheral request interface 1'b1: the DMAC provides the number of peripheral request interfaces that the num_periph_req field specifies

DMA_CR1

Address: **Operational Base** + offset (0x0E04)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RO	0xb	num_i_cache_lines 4'b0000: 1 i-cache line 4'b0001: 2 i-cache lines 4'b0010: 3 i-cache lines 4'b1111: 16 i-cache lines
3	RO	0x0	reserved
2:0	RO	0x5	i_cache_len 3'b000-3'b001: reserved 3'b010: 4 bytes 3'b011: 8 bytes 3'b100: 16 bytes 3'b101: 32 bytes 3'b110-3'b111: reserved

DMA_CR2

Address: **Operational Base** + offset (0x0E08)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	boot_addr Provides the value of boot_addr[31:0] when the DMAC exited from reset

DMA_CR3

Address: **Operational Base** + offset (0x0E0C)

Bit	Attr	Reset Value	Description
31:0	RO	0x0000ffff	ins Bit [N] 1'b0: Assigns event<N> or irq[N] to the Secure state 1'b1: Assigns event<N> or irq[N] to the Non-secure state

DMA_CR4

Address: **Operational Base** + offset (0x0E10)

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Bit	Attr	Reset Value	Description
31:0	RO	0xffffffff	pns Bit [N] 1'b0: Assigns peripheral request interface N to the Secure state 1'b1: Assigns peripheral request interface N to the Non-secure state

DMA_CRDn

Address: **Operational Base** + offset (0x0E14)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RO	0x07f	data_buffer_dep 10'b000000000: 1 line 10'b000000001: 2 lines 10'b111111111: 1024 lines
19:16	RO	0xf	rd_q_dep 4'b0000: 1 line 4'b0001: 2 lines 4'b1111: 16 lines
15	RO	0x0	reserved
14:12	RO	0x7	rd_cap 3'b000: 1 3'b001: 2 3'b111: 8
11:8	RO	0xf	wr_q_dep 4'b0000: 1 line 4'b0001: 2 lines 4'b1111: 16 lines
7	RO	0x0	reserved
6:4	RO	0x7	wr_cap 3'b000: 1 3'b001: 2 3'b111: 8
3	RO	0x0	reserved
2:0	RO	0x3	data_width 3'b000: reserved 3'b001: reserved 3'b010: 32-bit 3'b011: 64-bit 3'b100: 128-bit 3'b101-3'b111: reserved

DMA_WD

Address: **Operational Base** + offset (0x0E80)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	wd_irq_only 1'b0: the DMAC aborts all of the contributing DMA channels and sets irq_abort HIGH 1'b1: the DMAC sets irq_abort HIGH

12.5 Timing Diagram

Following picture shows the relationship between dma_req and dma_ack.

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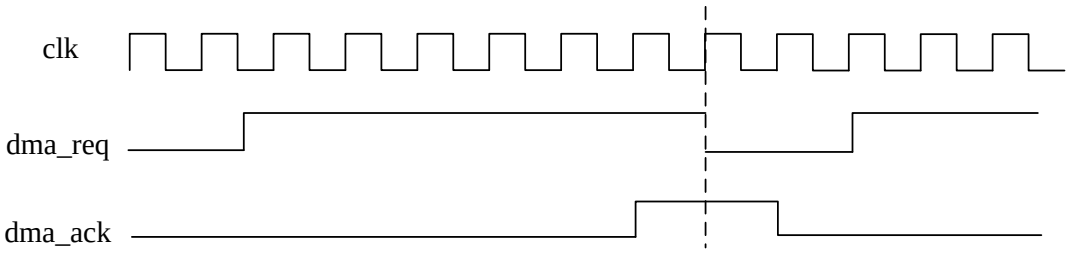


Fig.12-3 DMAC Request and Acknowledge Timing

12.6 Interface Description

DMAC has the following tie-off signals. It can be configured by GRF register. (Please refer to the GRF chapter to find them)

Table 12-2 DMAC Boot Interface

DMAC0		
Interface	**Reset value**	**Control source**
boot_irq_ns	0xFFFF	grf_dmac0_con0[15:0]
boot_periph_ns	0xFFFFFFFF	{grf_dmac0_con2[15:0],grf_dmac0_con1[15:0]}
boot_manager_ns	0x1	grf_dmac0_con3[0]
grf_drtype_ch0	0x1	grf_dmac0_con4[1:0]
grf_drtype_ch1	0x1	grf_dmac0_con4[3:2]
grf_drtype_ch2	0x1	grf_dmac0_con4[5:4]
grf_drtype_ch3	0x1	grf_dmac0_con4[7:6]
grf_drtype_ch4	0x1	grf_dmac0_con4[9:8]
grf_drtype_ch5	0x1	grf_dmac0_con4[11:10]
grf_drtype_ch6	0x1	grf_dmac0_con4[13:12]
grf_drtype_ch7	0x1	grf_dmac0_con4[15:14]
grf_drtype_ch8	0x1	grf_dmac0_con5[1:0]
grf_drtype_ch9	0x1	grf_dmac0_con5[3:2]
grf_drtype_ch10	0x1	grf_dmac0_con5[5:4]
grf_drtype_ch11	0x1	grf_dmac0_con5[7:6]
grf_drtype_ch12	0x1	grf_dmac0_con5[9:8]
grf_drtype_ch13	0x1	grf_dmac0_con5[11:10]
grf_drtype_ch14	0x1	grf_dmac0_con5[13:12]
grf_drtype_ch15	0x1	grf_dmac0_con5[15:14]
grf_drtype_ch16	0x1	grf_dmac0_con6[1:0]
grf_drtype_ch17	0x1	grf_dmac0_con6[3:2]
grf_drtype_ch18	0x1	grf_dmac0_con6[5:4]
grf_drtype_ch19	0x1	grf_dmac0_con6[7:6]
grf_drtype_ch20	0x1	grf_dmac0_con6[9:8]
grf_drtype_ch21	0x1	grf_dmac0_con6[11:10]
grf_drtype_ch22	0x1	grf_dmac0_con6[13:12]
grf_drtype_ch23	0x1	grf_dmac0_con6[15:14]
grf_drtype_ch24	0x1	grf_dmac0_con7[1:0]
grf_drtype_ch25	0x1	grf_dmac0_con7[3:2]
grf_drtype_ch26	0x1	grf_dmac0_con7[5:4]
grf_drtype_ch27	0x1	grf_dmac0_con7[7:6]

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DMAC0		
Interface	**Reset value**	**Control source**
grf_drtype_ch28	0x1	grf_dmac0_con7[9:8]
grf_drtype_ch29	0x1	grf_dmac0_con7[11:10]
grf_drtype_ch30	0x1	grf_dmac0_con7[13:12]
grf_drtype_ch31	0x1	grf_dmac0_con7[15:14]
grf_modify_dis_ch0	0x0	grf_dmac0_con8[0]
grf_modify_dis_ch1	0x0	grf_dmac0_con8[1]
grf_modify_dis_ch2	0x0	grf_dmac0_con8[2]
grf_modify_dis_ch3	0x0	grf_dmac0_con8[3]
grf_modify_dis_ch4	0x0	grf_dmac0_con8[4]
grf_modify_dis_ch5	0x0	grf_dmac0_con8[5]
grf_modify_dis_ch6	0x0	grf_dmac0_con8[6]
grf_modify_dis_ch7	0x0	grf_dmac0_con8[7]
grf_modify_dis_ch8	0x0	grf_dmac0_con8[8]
grf_modify_dis_ch9	0x0	grf_dmac0_con8[9]
grf_modify_dis_ch10	0x0	grf_dmac0_con8[10]
grf_modify_dis_ch11	0x0	grf_dmac0_con8[11]
grf_modify_dis_ch12	0x0	grf_dmac0_con8[12]
grf_modify_dis_ch13	0x0	grf_dmac0_con8[13]
grf_modify_dis_ch14	0x0	grf_dmac0_con8[14]
grf_modify_dis_ch15	0x0	grf_dmac0_con8[15]
grf_modify_dis_ch16	0x0	grf_dmac0_con9[0]
grf_modify_dis_ch17	0x0	grf_dmac0_con9[1]
grf_modify_dis_ch18	0x0	grf_dmac0_con9[2]
grf_modify_dis_ch19	0x0	grf_dmac0_con9[3]
grf_modify_dis_ch20	0x0	grf_dmac0_con9[4]
grf_modify_dis_ch21	0x0	grf_dmac0_con9[5]
grf_modify_dis_ch22	0x0	grf_dmac0_con9[6]
grf_modify_dis_ch23	0x0	grf_dmac0_con9[7]
grf_modify_dis_ch24	0x0	grf_dmac0_con9[8]
grf_modify_dis_ch25	0x0	grf_dmac0_con9[9]
grf_modify_dis_ch26	0x0	grf_dmac0_con9[10]
grf_modify_dis_ch27	0x0	grf_dmac0_con9[11]
grf_modify_dis_ch28	0x0	grf_dmac0_con9[12]
grf_modify_dis_ch29	0x0	grf_dmac0_con9[13]
grf_modify_dis_ch30	0x0	grf_dmac0_con9[14]
grf_modify_dis_ch31	0x0	grf_dmac0_con9[15]

boot_manager_ns
When the DMAC exits from reset, this signal controls the security state of the DMA manager thread:
0 = assigns DMA manager to the Secure state
1 = assigns DMA manager to the Non-secure state.
boot_irq_ns
Controls the security state of an event-interrupt resource, when the DMAC exits from reset:

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boot_irq_ns[x] is LOW
The DMAC assigns event<x> or irq[x] to the Secure state.
boot_irq_ns[x] is HIGH
The DMAC assigns event<x> or irq[x] to the Non-secure state.

boot_periph_ns

Controls the security state of a peripheral request interface, when the DMAC exits from reset:
boot_periph_ns[x] is LOW
The DMAC assigns peripheral request interface x to the Secure state.
boot_periph_ns[x] is HIGH
The DMAC assigns peripheral request interface x to the Non-secure state.

grf_drtype_<x>

The DMAC sets the state of the request_type flag:
grf_drtype_<x>[1:0]=b00: request_type<x> = Single.
grf_drtype_<x>[1:0]=b01: request_type<x> = Burst.

12.7 Application Notes

12.7.1 Using the APB Slave Interfaces

You must ensure that you use the appropriate APB interface, depending on the security state in which the boot_manager_ns initializes the DMAC to operate. For example, if the DMAC is in the secure state, you must issue the instruction using the secure APB interface, otherwise the DMAC ignores the instruction. You can use the secure APB interface, or the non-secure APB interface, to start or restart a DMA channel when the DMAC is in the Non-secure state.
The necessary steps to start a DMA channel thread using the debug instruction registers as following:
1. Create a program for the DMA channel.
2. Store the program in a region of system memory.
3. Poll the DMAC_DBGSTATUS Register to ensure that debug is idle, that is, the dbgstatus bit is 0.
4. Write to the DMAC_DBGINST0 Register and enter the:
   - Instruction byte 0 encoding for DMAGO.
   - Instruction byte 1 encoding for DMAGO.
   - Debug thread bit to 0. This selects the DMA manager thread.
5. Write to the DBGINST1 Register with the DMAGO instruction byte [5:2] data, see Debug Instruction-1 Register o. You must set these four bytes to the address of the first instruction in the program that was written to system memory in step 2.
6. Writing zero to the DMAC_DBGCMD Register. The DMAC starts the DMA channel thread and sets the dbgstatus bit to 1.

12.7.2 Security Usage

DMA manager thread is in the secure state

If the DNS bit is 0, the DMA manager thread operates in the secure state and it only performs secure instruction fetches. When a DMA manager thread in the secure state processes:

DMAGO

It uses the status of the ns bit, to set the security state of the DMA channel thread by writing to the CNS bit for that channel.

DMAWFE

It halts execution of the thread until the event occurs. When the event occurs, the DMAC continues execution of the thread, irrespective of the security state of the corresponding INS bit.

DMASEV

It sets the corresponding bit in the INT_EVENT_RIS Register, irrespective of the security state of the corresponding INS bit.

DMA manager thread is in the Non-secure state

If the DNS bit is 1, the DMA manager thread operates in the Non-secure state, and it only

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performs non-secure instruction fetches. When a DMA manager thread in the Non-secure state processes:

DMAGO

The DMAC uses the status of the ns bit, to control if it starts a DMA channel thread. If:

ns = 0

The DMAC does not start a DMA channel thread and instead it:

1. Executes a NOP.
2. Sets the DMAC_FSRD Register, see Fault Status DMA Manager
3. Sets the dmago_err bit in the DMAC_FTRD Register, see Fault Type DMA Manager Register.
4. Moves the DMA manager to the Faulting state.

ns = 1

The DMAC starts a DMA channel thread in the Non-secure state and programs the CNS bit to be non-secure.

DMAWFE

The DMAC uses the status of the corresponding INS bit, in the DMAC_CR3 Register, to control if it waits for the event. If:

INS = 0

The event is in the Secure state. The DMAC:

1. Executes a NOP.
2. Sets the DMAC_FSRD Register, see Fault Status DMA Manager Register.
3. Sets the mgr_evnt_err bit in the DMAC_FTRD Register, see Fault Type DMA Manager Register.
4. Moves the DMA manager to the Faulting state.

INS = 1

The event is in the Non-secure state. The DMAC halts execution of the thread and waits for the event to occur.

DMASEV

The DMAC uses the status of the corresponding INS bit, in the CR3Register, to control if it creates the event-interrupt. If:

INS = 0

The event-interrupt resource is in the secure state. The DMAC:

1. Executes a NOP.
2. Sets the DMAC_FSRD Register, see Fault Status DMA Manager Register.
3. Sets the mgr_evnt_err bit in the DMAC_FTRD Register, see Fault Type DMA Manager Register.
4. Moves the DMA manager to the Faulting state.

INS = 1

The event-interrupt resource is in the Non-secure state. The DMAC creates the event-interrupt.

DMA channel thread is in the secure state

When the CNS bit is 0, the DMA channel thread is programmed to operate in the Secure state and it only performs secure instruction fetches.

When a DMA channel thread in the secure state processes the following instructions:

DMAWFE

The DMAC halts execution of the thread until the event occurs. When the event occurs, the DMAC continues execution of the thread, irrespective of the security state of the corresponding INS bit, in the DMAC_CR3 Register.

DMASEV

The DMAC creates the event-interrupt, irrespective of the security state of the corresponding INS bit, in the DMAC_CR3 Register.

DMAWFP

The DMAC halts execution of the thread until the peripheral signals a DMA request. When this occurs, the DMAC continues execution of the thread, irrespective of the security state of the corresponding PNS bit, in the DMAC_CR4 Register.

DMALDP, DMASTP

The DMAC sends a message to the peripheral to communicate that data transfer

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is complete, irrespective of the security state of the corresponding PNS bit, in the DMAC_CR4 Register.

DMAFLUSHP

The DMAC clears the state of the peripheral and sends a message to the peripheral to resend its level status, irrespective of the security state of the corresponding PNS bit, in the DMAC_CR4 Register.

When a DMA channel thread is in the Secure state, it enables the DMAC to perform secure and non-secure AXI accesses.

DMA channel thread is in the Non-secure state

When the CNS bit is 1, the DMA channel thread is programmed to operate in the Non-secure state and it only performs non-secure instruction fetches.

When a DMA channel thread in the Non-secure state processes the following instructions:

DMAWFE

The DMAC uses the status of the corresponding INS bit, in the DMAC_CR3 Register, to control if it waits for the event. If:

INS = 0

The event is in the Secure state. The DMAC:

1. Executes a NOP.
2. Sets the appropriate bit in the DMAC_FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_evnt_err bit in the DMAC_FTRn(n=0~7) Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.

INS = 1

The event is in the Non-secure state. The DMAC halts execution of the thread and waits for the event to occur.

DMASEV

The DMAC uses the status of the corresponding INS bit, in the DMAC_CR3 Register, to control if it creates the event. If:

INS = 0

The event-interrupt resource is in the Secure state. The DMAC:

1. Executes a NOP.
2. Sets the appropriate bit in the DMAC_FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_evnt_err bit in the DMAC_FTRn(n=0~7) Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.

INS = 1

The event-interrupt resource is in the Non-secure state. The DMAC creates the event-interrupt.

DMAWFP

The DMAC uses the status of the corresponding PNS bit, in the DMAC_CR4 Register, to control if it waits for the peripheral to signal a request. If:

PNS = 0

The peripheral is in the Secure state. The DMAC:

1. Executes a NOP.
2. Sets the appropriate bit in the DMAC_FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_periph_err bit in the DMAC_FTRn(n=0~7) Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.

PNS = 1

The peripheral is in the Non-secure state. The DMAC halts execution of the thread and waits for the peripheral to signal a request.

DMALDP, DMASTP

The DMAC uses the status of the corresponding PNS bit, in the DMAC_CR4 Register, to control if it sends an acknowledgement to the peripheral. If:

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PNS = 0
The peripheral is in the secure state. The DMAC:
1. Executes a NOP.
2. Sets the appropriate bit in the DMAC_FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_periph_err bit in the DMAC_FTRn(n=0~7) Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.
PNS = 1
The peripheral is in the Non-secure state. The DMAC sends a message to the peripheral to communicate when the data transfer is complete.

DMAFLUSHP

The DMAC uses the status of the corresponding PNS bit, in the DMAC_CR4 Register, to control if it sends a flush request to the peripheral. If:
PNS = 0
The peripheral is in the secure state. The DMAC:
1. Executes a NOP.
2. Sets the appropriate bit in the DMAC_FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_periph_err bit in the DMAC_FTRn(n=0~7) Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.
PNS = 1
The peripheral is in the Non-secure state. The DMAC clears the state of the peripheral and sends a message to the peripheral to resend its level status.
When a DMA channel thread is in the Non-secure state, and a DMAMOV CCR instruction attempts to program the channel to perform a secure AXI transaction, the DMAC:
1. Executes a DMANOP.
2. Sets the appropriate bit in the DMAC_FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_rdwr_err bit in the DMAC_FTRn(n=0~7) Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel thread to the Faulting completing state.

12.7.3 Programming Restrictions

Fixed unaligned bursts

The DMAC does not support fixed unaligned bursts. If you program the following conditions, the DMAC treats this as a programming error:
Unaligned read
- src_inc field is 0 in the DMAC_CCRn(n=0~7) Register
- the DMAC_SARn(n=0~7) Register contains an address that is not aligned to the size of data that the src_burst_size field contain

Unaligned write
- dst_inc field is 0 in the DMAC_CCRn(n=0~7) Register
- the DMAC_DARn(n=0~7) Register contains an address that is not aligned to the size of data that the dst_burst_size field contains

Endian swap size restrictions

If you program the endian_swap_size field in the DMAC_CCRn(n=0~7) Register, to enable a DMA channel to perform an endian swap then you must set the corresponding DMAC_SARn(n=0~7) Register and the corresponding DMAC_DARn(n=0~7) Register to contain an address that is aligned to the value that the endian_swap_size field contains.

Updating DMA channel control registers during a DMA cycle restrictions

Prior to the DMAC executing a sequence of DMALD and DMAST instructions, the values you program in to the DMAC_CCRn(n=0~7) Register, DMAC_SARn(n=0~7) Register, and DMAC_DARn(n=0~7) Register control the data byte lane manipulation that the DMAC performs when it transfers the data from the source address to the destination address. You'd better not update these registers during a DMA cycle.

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Resource sharing between DMA channels

DMA channel programs share the MFIFO data storage resource. You must not start a set of concurrently running DMA channel programs with a resource requirement that exceeds the configured size of the MFIFO. If you exceed this limit then the DMAC might lock up and generate a Watchdog abort.

12.7.4 Unaligned Transfers

For a configuration with more than one channel, if any of channels 1 to 7 is performing transfers between certain types of misaligned source and destination addresses, then the output data may be corrupted by the action of channel 0.

Data corruption might occur if all of the following are true:

1. Two beats of AXI read data are received for one of channels 1 to 7.
2. Source and destination address alignments mean that each read data beat is split across two lines in the data buffer (see Splitting data, below).
3. There is one idle cycle between the two read data beats.
4. Channel 0 performs an operation that updates channel control information during this idle cycle (see Updates to channel control information, below).

Splitting data

Depending upon the programmed values for the DMA transfer, one beat of read data from the AXI interface need to be split across two lines in the internal data buffer. This occurs when the read data beat contains data bytes which will be written to addresses that wrap around at the AXI interface data width, so that these bytes could not be transferred by a single AXI write data beat of the full interface width.

Most applications of DMA do not split data in this way, so are NOT vulnerable to data corruption from this defect.

The following cases are NOT vulnerable to data corruption because they do not split data:

- Byte lane offset between source and destination addresses is 0 when source and destination addresses have the same byte lane alignment, the offset is 0 and a wrap operation that splits data cannot occur.
- Byte lane offset between source and destination addresses is a multiple of source size.

Table 12-3 Source Size in DMAC_CCRn

Source size in DMAC_CCRn	Allowed offset between DMAC_SARn and DMAC_DARn
SS8	any offset allowed.
SS16	0,2,4,6,8,10,12,14
SS32	0,4,8,12
SS64	0,8

12.7.5 Interrupt Sharing between Channels

As the DMAC does not record which channel (or list of channels) have asserted an interrupt. So it will depend on your program and whether any of the visible information for that program can be used to determine progress, and help identify the interrupt source.

There are 4 likely information sources that can be used to determine the progress made by a program:

- Program counter (PC)
- Source address
- Destination address
- Loop counters (LC)

For example, a program might emit an interrupt each time that it iterates around a loop. In this case, the interrupt service routine (ISR) would need to store the loop value of each channel when it is called, and then compare against the new value when it is next called. A change in value would indicate that the program has progressed.

The ISR must be carefully written to ensure that no interrupts are lost. The sequence of operations is as follows:

1. Disable interrupts
2. Immediately clear the interrupt in DMA-330
3. Check the relevant registers for both channels to determine which must be serviced

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4. Take appropriate action for the channels
5. Re-enable interrupts and exit ISR

12.7.6 Instruction Sets

Table 12-4 DMAC Instruction Sets

Mnemonic	Instruction	Thread Usage
DMAADDH	Add Halfword	C
DMAEND	End	M/C
DMAFLUSHP	Flush and notify Peripheral	C
DMAGO	Go	M
DMAKILL	Kill	C
DMALD	Load	C
DMALDP	Load Peripheral	C
DMALP	Loop	C
DMALPEND	Loop End	C
DMALPFE	Loop Forever	C
DMAMOV	Move	C
DMANOP	No operation	M/C
DMARMB	Read Memory Barrier	C
DMASEV	Send Event	M/C
DMAST	Store	C
DMASTP	Store and notify Peripheral	C
DMASTZ	Store Zero	C
DMAWFE	Wait for Event M	M/C
DMAWFP	Wait for Peripheral	C
DMAWMB	Write Memory Barrier	C
DMAADNH	Add Negative Halfword	C

Notes: Thread usage: C=DMA channel, M=DMA manager

12.7.7 Assembler Directives

In this document, only DMMADNH instruction is took as an example to show the way the instruction assembled. For the other instructions, please refer to pl330_trm.pdf.

DMAADNH

Add Negative Halfword adds an immediate negative 16-bit value to the DMAC_SARn(n=0~7) Register or DMAC_DARn(n=0~7) Register, for the DMA channel thread. This enables the DMAC to support 2D DMA operations, or reading or writing an area of memory in a different order to naturally incrementing addresses. See Source Address Registers and Destination Address Registers.

The immediate unsigned 16-bit value is one-extended to 32 bits, to create a value that is the two's complement representation of a negative number between -65536 and -1, before the DMAC adds it to the address using 32-bit addition. The DMAC discards the carry bit so that addresses wrap from 0xFFFFFFFF to 0x00000000. The net effect is to subtract between 65536 and 1 from the current value in the Source or Destination Address Register.

Following table shows the instruction encoding.

Table 12-5 DMAC Instruction Encoding

Imm[15:8]	Imm[7:0]	0	1	0	1	1	1	ra	0

Assembler syntax

DMAADNH <address_register>, <16-bit immediate>

where:

<address_register>

Selects the address register to use. It must be either:

SAR

DMAC_SARn(n=0~7) Register and sets ra to 0.

DAR

DMAC_DARn(n=0~7) Register and sets ra to 1.

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<16-bit immediate>

The immediate value to be added to the <address_register>.

You should specify the 16-bit immediate as the number that is to be represented in the instruction encoding. For example, DMAADNH DAR, 0xFFF0 causes the value 0xFFFFFFF0 to be added to the current value of the Destination Address Register, effectively subtracting 16 from the DAR.

You can only use this instruction in a DMA channel thread.

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Chapter 13 Dynamic Memory Interface (DMC)

13.1 Overview

The DMC includes DDR enhanced memory controller(UMCTL2) and DDRPHY which are a complete memory interface solution for DDR memory subsystems.
The UMCTL2 SoC application bus interface supports AXI interface, with flexible address mapper logic allow application-specific mapping of row, column, bank, bank group and rank bits to achieve industry leading high-efficiency, low-latency and high-performance from memory interface.
The DDR PHY provides control features to ease the customer implementation of digitally controlled features of the PHY such as initialization, DQS gate training, write leveling training and programmable configuration controls.
The DMC supports the following features:

- Support DDR3/DDR3L/DDR4/LPDDR3/LPDDR4
- Support up to 4 ranks for LPDDR3/LPDDR4 and up to 2 ranks for DDR3/DDR4
- Support up to 8GB capacity
- Support 32-bit, 16-bit, 8-bit DDR data bus width
- Support up to 20-type address mapping
- Support up to 64-bank (including bank group)
- Support DDR burst8 for DDR3/DDR3L/DDR4/LPDDR3 and burst16 for LPDDR4
- Support different CL/WL latency
- Support DDR3/DDR3L/DDR4/LPDDR3/LPDDR4 SW frequency change
- Support auto gated clock through DDRC and AXI low power interface
- Support auto put DDR PHYentry or exit self-refresh by DFI lower power interface
- Support auto or SW issue entry or exit clock stop/power-down/self-refresh/deep power-down/max power saving mode
- Support SW or PMU auto control DDR PHY entry or exit retention/self-refresh
- Support open, close, intelligent precharge paging policy
- Support advance refresh control
- Support APB interface for UMCTL2 and PHY software-accessible registers
- Support RX DQS gate training, write leveling training, write training and read training for DDR3/DDR4/LPDDR3/LPDDR4
- Support command bus training for LPDDR3/LPDDR4
- Support scramble DDR transaction, to enhance security
- Support inconsistent DDR capacity within a rank
- Support DDR monitor for debug:
  - AMBA 32-bit APB slave interface
  - Support to monitor DDR read or write address
  - Support to observe whether DDR access address within a specified range
  - Support to do the statistics about DDR read number, write number and active number
    - Hardware mode
    - Software mode
  - Support monitor interrupt

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13.2 Block Diagram

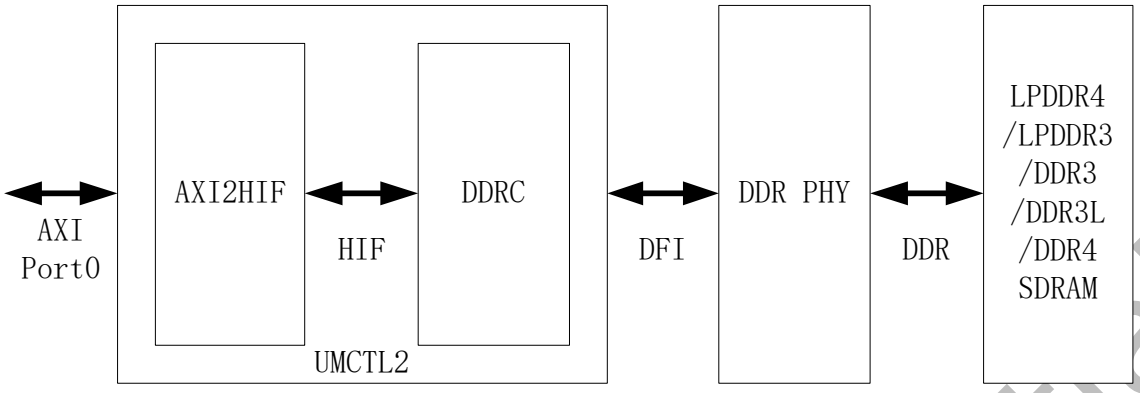


Fig.13-1 DMC Block Diagram

13.3 Function Description

13.3.1 UMCTL2

UMCTL2 supports only one AXI Port0, it receives AXI transactions from memory schedule of interconnect. These transactions are queued internally and scheduled for access in order to the SDRAM while satisfying SDRAM protocol timing requirements. It in turn issues commands on the DFI interface to the DDR PHY block which launches and captures data to and from the SDRAM. UMCTL2 contains the following main components:

- AXI2HIF block: This block provides the AXI interface to system level and HIF interface to DDRC block. It provides bus protocol handing, data buffering, data bus size conversion and memory burst alignment. Read is stored in a SRAM, read re-order buffer and return in order to the AXI Port.
- DDRC block: This block issues the read/write commands in order, carries out the DRAM page management, issues DRAM maintenance commands, and implement the DFI interface. Write data is stored in an SRAM until its associated command is issued to the PHY. Read data is handled by the response engine in the DDRC and is returned in order on the HIF.

13.3.2 DDR PHY

DDR PHY supports DDR3/DDR3L/DDR4/LPDDR3/LPDDR4 SDRAM and provides turnkey physical interface solutions for ICs requiring access to JEDEC compatible SDRAM devices. It supports all JEDEC DDR3/DDR3L/DDR4/LPDDR3/LPDDR4 SDRAM components in the market. The PHY components contain DDR specialized functional, critical timing synchronization module (TSM) and a low power/jitter DLLs with programmable fine-grain control for any SDRAM interface.

13.3.3 DDR Hardware Low Power Controller

DDR Hardware low power(HWLP) controller reduces the power consumption of the DMC when the DMC is idle. HWLP is configured through APB slave interface and it is disabled by default. If it is enabled, when there is not any bus access to DDR and the DDRCTL is idle for a period of time, the HWLP controller will generate a low power mode entry request to DDRCTL2. If the DDRCTL2 accept the request, it put DDR device into low power mode. Then HWLP controller is going to gate the clock of DDR controller, DDRPHY and memory scheduler according to the actual configuration.

13.3.4 Scramble

The function of Scramble module is to scramble and descramble data written to or read from DDR SDRAM. This module is defaultly bypassed. If it is enabled, it receives data from DDR memory scheduler, scramble written data and then send it to the AXI port of DDRCTL. It also descrambles date received from AXI port of DDRCTL and send it back to DDR memory scheduler.

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13.3.5 DDR Monitor

The DDR Monitor Module has three functions, the first function is used when debug, it will monitor the DDR read or write address. The second function is also used when debug, it will observe whether DDR access address within a specified range. The third function is used to do the statistics about DDR bandwidth and utilization.

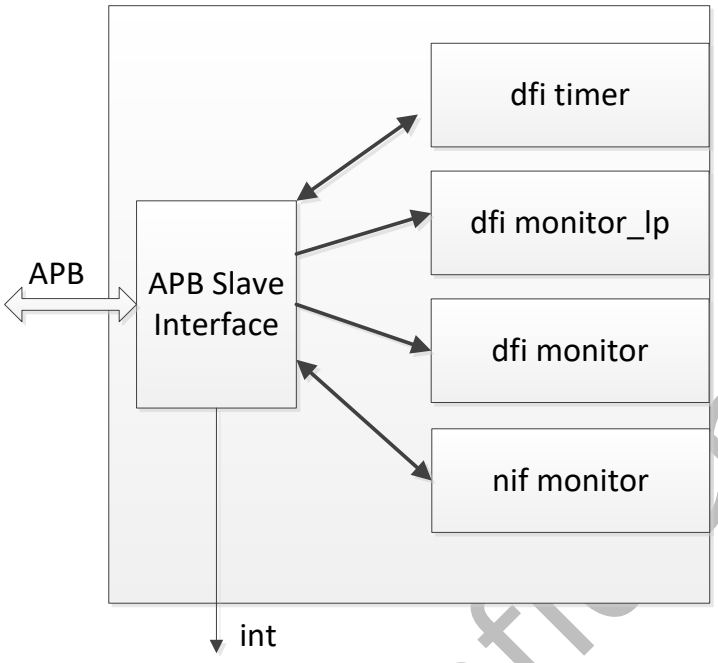


Fig.13-2 DDR Monitor Block Diagram

The host processor gets access to DDR Monitor Register Block through the APB slave interface with 32-bit bus width, and asserts the active-high level interrupt.
DDR Monitor does the monitor and statistics by dfi monitor module, nif monitor module and dfi monitor_lp module.

13.4 Register Description

13.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Table 13-1 DMC Address Mapping

Base Address[31:0]	Device	Address Length	Offset Address Range
32'hff4d8000	HWLP	32K BYTE	0x0000 ~ 0x7fff
32'hff4e0000	DDRCTL	64K BYTE	0x0000 ~ 0xffff
32'hff4f0000	DDRPHY	64K BYTE	0x0000 ~ 0xffff
32'hff4c0000	DDR MONITOR	32K BYTE	0x0000 ~ 0x7fff

13.4.2 Registers Summary for DDRCTL

Name	Offset	Size	Reset Value	Description
DDRCTL_MSTR	0x0000	W	0x03040001	Master Register0
DDRCTL_STAT	0x0004	W	0x00000000	Operating Mode Status Register
DDRCTL_MRCTRL0	0x0010	W	0x00000030	Mode Register Read/Write Control Register 0
DDRCTL_MRCTRL1	0x0014	W	0x00000000	Mode Register Read/Write Control Register 1
DDRCTL_MRSTAT	0x0018	W	0x00000000	Mode Register Read/Write Status Register

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Name	Offset	Size	Reset Value	Description
DDRCTL_MRCTRL2	0x001C	W	0x00000000	Mode Register Read/Write Control Register 2
DDRCTL_DERATEEN	0x0020	W	0x00000000	Temperature Derate Enable Register
DDRCTL_DERATEINT	0x0024	W	0x00800000	Temperature Derate Interval Register
DDRCTL_MSTR2	0x0028	W	0x00000001	Master Register2
DDRCTL_DERATECTL	0x002C	W	0x00000001	Temperature Derate Control Register
DDRCTL_PWRCTL	0x0030	W	0x00000000	Low Power Control Register
DDRCTL_PWRTMG	0x0034	W	0x00402010	Low Power Timing Register
DDRCTL_HWLPCTL	0x0038	W	0x00000003	Hardware Low Power Control Register
DDRCTL_RFSHCTL0	0x0050	W	0x00210000	Refresh Control Register 0
DDRCTL_RFSHCTL1	0x0054	W	0x00000000	Refresh Control Register 1
DDRCTL_RFSHCTL3	0x0060	W	0x00000000	Refresh Control Register 3
DDRCTL_RFSHTMG	0x0064	W	0x0062008C	Refresh Timing Register
DDRCTL_RFSHTMG1	0x0068	W	0x008C0000	Refresh Timing Register1
DDRCTL_CRCPARCTL0	0x00C0	W	0x00000000	CRC Parity Control Register0
DDRCTL_CRCPARCTL1	0x00C4	W	0x00001000	CRC Parity Control Register1
DDRCTL_CRCPARSTAT	0x00CC	W	0x00000000	CRC Parity Status Register
DDRCTL_INIT0	0x00D0	W	0x0002004E	SDRAM Initialization Register 0
DDRCTL_INIT1	0x00D4	W	0x00000000	SDRAM Initialization Register 1
DDRCTL_INIT2	0x00D8	W	0x00000D00	SDRAM Initialization Register 2
DDRCTL_INIT3	0x00DC	W	0x00000510	SDRAM Initialization Register 3
DDRCTL_INIT4	0x00E0	W	0x00000000	SDRAM Initialization Register 4
DDRCTL_INIT5	0x00E4	W	0x00100004	SDRAM Initialization Register 5
DDRCTL_INIT6	0x00E8	W	0x00000000	SDRAM Initialization Register 6
DDRCTL_INIT7	0x00EC	W	0x00000000	SDRAM Initialization Register 7
DDRCTL_DIMMCTL	0x00F0	W	0x00000000	DIMM Control Register
DDRCTL_RANKCTL	0x00F4	W	0x00000660	Rank Control Register
DDRCTL_DRAMTMG0	0x0100	W	0x0F101B0F	SDRAM Timing Register 0
DDRCTL_DRAMTMG1	0x0104	W	0x00080414	SDRAM Timing Register 1
DDRCTL_DRAMTMG2	0x0108	W	0x0305060D	SDRAM Timing Register 2
DDRCTL_DRAMTMG3	0x010C	W	0x0050400C	SDRAM Timing Register 3
DDRCTL_DRAMTMG4	0x0110	W	0x05040405	SDRAM Timing Register 4
DDRCTL_DRAMTMG5	0x0114	W	0x05050403	SDRAM Timing Register 5
DDRCTL_DRAMTMG6	0x0118	W	0x02020005	SDRAM Timing Register 6
DDRCTL_DRAMTMG7	0x011C	W	0x00000202	SDRAM Timing Register 7
DDRCTL_DRAMTMG8	0x0120	W	0x03034405	SDRAM Timing Register 8
DDRCTL_DRAMTMG9	0x0124	W	0x0004040D	SDRAM Timing Register 9
DDRCTL_DRAMTMG10	0x0128	W	0x001C180A	SDRAM Timing Register 10
DDRCTL_DRAMTMG11	0x012C	W	0x440C021C	SDRAM Timing Register 11
DDRCTL_DRAMTMG12	0x0130	W	0x1A020010	SDRAM Timing Register 12
DDRCTL_DRAMTMG13	0x0134	W	0x1C200004	SDRAM Timing Register 13
DDRCTL_DRAMTMG14	0x0138	W	0x000000A0	SDRAM Timing Register 14
DDRCTL_DRAMTMG15	0x013C	W	0x00000000	SDRAM Timing Register 15
DDRCTL_ZQCTL0	0x0180	W	0x02000040	ZQ Control Register 0
DDRCTL_ZQCTL1	0x0184	W	0x02000100	ZQ Control Register 1
DDRCTL_ZQCTL2	0x0188	W	0x00000000	ZQ Control Register 2
DDRCTL_ZQSTAT	0x018C	W	0x00000000	ZQ Status Register
DDRCTL_DFITMG0	0x0190	W	0x07020002	DFI Timing Register 0
DDRCTL_DFITMG1	0x0194	W	0x00000404	DFI Timing Register 1

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Name	Offset	Size	Reset Value	Description
DDRCTL_DFILPCFG0	0x0198	W	0x07000000	DFI Low Power Configuration Register 0
DDRCTL_DFILPCFG1	0x019C	W	0x00000000	DFI Low Power Configuration Register 1
DDRCTL_DFIUPD0	0x01A0	W	0x00400003	DFI Update Register 0
DDRCTL_DFIUPD1	0x01A4	W	0x00010001	DFI Update Register 1
DDRCTL_DFIUPD2	0x01A8	W	0x80000000	DFI Update Register 2
DDRCTL_DFIMISC	0x01B0	W	0x00000041	DFI Miscellaneous Control Register
DDRCTL_DFITMG2	0x01B4	W	0x00000202	DFI Timing Register 2
DDRCTL_DFITMG3	0x01B8	W	0x00000000	DFI Timing Register 3
DDRCTL_DFISTAT	0x01BC	W	0x00000000	DFI Status Register
DDRCTL_DBICTL	0x01C0	W	0x00000001	DM/DBI Control Register
DDRCTL_DFIPHYMSTR	0x01C4	W	0x80000001	DFI PHY Master
DDRCTL_ADDRMAP0	0x0200	W	0x00000000	Address Map Register 0
DDRCTL_ADDRMAP1	0x0204	W	0x00000000	Address Map Register 1
DDRCTL_ADDRMAP2	0x0208	W	0x00000000	Address Map Register 2
DDRCTL_ADDRMAP3	0x020C	W	0x00000000	Address Map Register 3
DDRCTL_ADDRMAP4	0x0210	W	0x00000000	Address Map Register 4
DDRCTL_ADDRMAP5	0x0214	W	0x00000000	Address Map Register 5
DDRCTL_ADDRMAP6	0x0218	W	0x00000000	Address Map Register 6
DDRCTL_ADDRMAP7	0x021C	W	0x00000000	Address Map Register 7
DDRCTL_ADDRMAP8	0x0220	W	0x00000000	Address Map Register 8
DDRCTL_ADDRMAP9	0x0224	W	0x00000000	Address Map Register 9
DDRCTL_ADDRMAP10	0x0228	W	0x00000000	Address Map Register 10
DDRCTL_ADDRMAP11	0x022C	W	0x00000000	Address Map Register 11
DDRCTL_ODTCFG	0x0240	W	0x04000400	ODT Configuration Register
DDRCTL_ODTMAP	0x0244	W	0x00002211	ODT/Rank Map Register
DDRCTL_SCHED	0x0250	W	0x00000004	Scheduler Control Register
DDRCTL_SCHED1	0x0254	W	0x00000000	Scheduler Control Register 1
DDRCTL_PERFLPR1	0x0264	W	0x0F00007F	Low Priority Read CAM Register 1
DDRCTL_PERFWR1	0x026C	W	0x0F00007F	Write CAM Register 1
DDRCTL_DBG0	0x0300	W	0x00000000	Debug Register 0
DDRCTL_DBG1	0x0304	W	0x00000000	Debug Register 1
DDRCTL_DBGCAM	0x0308	W	0x00000000	CAM Debug Register
DDRCTL_DBGCMD	0x030C	W	0x00000000	Command Debug Register
DDRCTL_DBGSTAT	0x0310	W	0x00000000	Status Debug Register
DDRCTL_SWCTL	0x0320	W	0x00000001	Software Register Programming Control Enable
DDRCTL_SWSTAT	0x0324	W	0x00000001	Software Register Programming Control Status
DDRCTL_SWCTLSTATIC	0x0328	W	0x00000000	Static Registers Write Enable
DDRCTL_POISONCFG	0x036C	W	0x00110011	AXI Poison Configuration Register
DDRCTL_POISONSTAT	0x0370	W	0x00000000	AXI Poison Status Register
DDRCTL_DERATESTAT	0x03F0	W	0x00000000	Temperature Derate Status Register
DDRCTL_MP_PSTAT	0x03FC	W	0x00000000	Port Status Register
DDRCTL_MP_PCCFG	0x0400	W	0x00000000	Port Common Configuration Register
DDRCTL_MP_PCFGR_0	0x0404	W	0x00000000	Port n Configuration Read Register
DDRCTL_MP_PCFGW_0	0x0408	W	0x00004000	Port n Configuration Write Register
DDRCTL_MP_PCTRL_0	0x0490	W	0x00000000	Port n Control Register

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Name	Offset	Size	Reset Value	Description
DDRCTL_MP_VER_NUMBER	0x0FF0	W	0x3339302A	UMCTL2 Version Number Register
DDRCTL_MP_VER_TYPE	0x0FF4	W	0x67612A2A	UMCTL2 Version Type Register
DDRCTL_FREQ1_DERATEEN	0x2020	W	0x00000000	Temperature Derate Enable Register
DDRCTL_FREQ1_DERATEINT	0x2024	W	0x00800000	Temperature Derate Interval Register
DDRCTL_FREQ1_PWRTMG	0x2034	W	0x00402010	Low Power Timing Register
DDRCTL_FREQ1_RFSHCTL0	0x2050	W	0x00210000	Refresh Control Register 0
DDRCTL_FREQ1_RFSHTMG	0x2064	W	0x0062008C	Refresh Timing Register
DDRCTL_FREQ1_RFSHTMG1	0x2068	W	0x008C0000	Refresh Timing Register1
DDRCTL_FREQ1_INIT3	0x20DC	W	0x00000510	SDRAM Initialization Register 3
DDRCTL_FREQ1_INIT4	0x20E0	W	0x00000000	SDRAM Initialization Register 4
DDRCTL_FREQ1_INIT6	0x20E8	W	0x00000000	SDRAM Initialization Register 6
DDRCTL_FREQ1_INIT7	0x20EC	W	0x00000000	SDRAM Initialization Register 7
DDRCTL_FREQ1_RANKCTL	0x20F4	W	0x00000660	Rank Control Register
DDRCTL_FREQ1_DRAMTMG0	0x2100	W	0x0F101B0F	SDRAM Timing Register 0
DDRCTL_FREQ1_DRAMTMG1	0x2104	W	0x00080414	SDRAM Timing Register 1
DDRCTL_FREQ1_DRAMTMG2	0x2108	W	0x0305060D	SDRAM Timing Register 2
DDRCTL_FREQ1_DRAMTMG3	0x210C	W	0x0050400C	SDRAM Timing Register 3
DDRCTL_FREQ1_DRAMTMG4	0x2110	W	0x05040405	SDRAM Timing Register 4
DDRCTL_FREQ1_DRAMTMG5	0x2114	W	0x05050403	SDRAM Timing Register 5
DDRCTL_FREQ1_DRAMTMG6	0x2118	W	0x02020005	SDRAM Timing Register 6
DDRCTL_FREQ1_DRAMTMG7	0x211C	W	0x00000202	SDRAM Timing Register 7
DDRCTL_FREQ1_DRAMTMG8	0x2120	W	0x03034405	SDRAM Timing Register 8
DDRCTL_FREQ1_DRAMTMG9	0x2124	W	0x0004040D	SDRAM Timing Register 9
DDRCTL_FREQ1_DRAMTMG10	0x2128	W	0x001C180A	SDRAM Timing Register 10
DDRCTL_FREQ1_DRAMTMG11	0x212C	W	0x440C021C	SDRAM Timing Register 11
DDRCTL_FREQ1_DRAMTMG12	0x2130	W	0x1A020010	SDRAM Timing Register 12
DDRCTL_FREQ1_DRAMTMG13	0x2134	W	0x1C200004	SDRAM Timing Register 13
DDRCTL_FREQ1_DRAMTMG14	0x2138	W	0x000000A0	SDRAM Timing Register 14
DDRCTL_FREQ1_DRAMTMG15	0x213C	W	0x00000000	SDRAM Timing Register 15
DDRCTL_FREQ1_ZQCTL0	0x2180	W	0x02000040	ZQ Control Register 0
DDRCTL_FREQ1_DFITMG0	0x2190	W	0x07020002	DFI Timing Register 0

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Name	Offset	Size	Reset Value	Description
DDRCTL_FREQ1_DFITMG1	0x2194	W	0x00000404	DFI Timing Register 1
DDRCTL_FREQ1_DFITMG2	0x21B4	W	0x00000202	DFI Timing Register 2
DDRCTL_FREQ1_DFITMG3	0x21B8	W	0x00000000	DFI Timing Register 3
DDRCTL_FREQ1_ODTCFG	0x2240	W	0x04000400	ODT Configuration Register
DDRCTL_FREQ2_DERATEEN	0x3020	W	0x00000000	Temperature Derate Enable Register
DDRCTL_FREQ2_DERATEINT	0x3024	W	0x00800000	Temperature Derate Interval Register
DDRCTL_FREQ2_PWRTMG	0x3034	W	0x00402010	Low Power Timing Register
DDRCTL_FREQ2_RFSHCTL0	0x3050	W	0x00210000	Refresh Control Register 0
DDRCTL_FREQ2_RFSHTMG	0x3064	W	0x0062008C	Refresh Timing Register
DDRCTL_FREQ2_RFSHTMG1	0x3068	W	0x008C0000	Refresh Timing Register1
DDRCTL_FREQ2_INIT3	0x30DC	W	0x00000510	SDRAM Initialization Register 3
DDRCTL_FREQ2_INIT4	0x30E0	W	0x00000000	SDRAM Initialization Register 4
DDRCTL_FREQ2_INIT6	0x30E8	W	0x00000000	SDRAM Initialization Register 6
DDRCTL_FREQ2_INIT7	0x30EC	W	0x00000000	SDRAM Initialization Register 7
DDRCTL_FREQ2_RANKCTL	0x30F4	W	0x00000660	Rank Control Register
DDRCTL_FREQ2_DRAMTMG0	0x3100	W	0x0F101B0F	SDRAM Timing Register 0
DDRCTL_FREQ2_DRAMTMG1	0x3104	W	0x00080414	SDRAM Timing Register 1
DDRCTL_FREQ2_DRAMTMG2	0x3108	W	0x0305060D	SDRAM Timing Register 2
DDRCTL_FREQ2_DRAMTMG3	0x310C	W	0x0050400C	SDRAM Timing Register 3
DDRCTL_FREQ2_DRAMTMG4	0x3110	W	0x05040405	SDRAM Timing Register 4
DDRCTL_FREQ2_DRAMTMG5	0x3114	W	0x05050403	SDRAM Timing Register 5
DDRCTL_FREQ2_DRAMTMG6	0x3118	W	0x02020005	SDRAM Timing Register 6
DDRCTL_FREQ2_DRAMTMG7	0x311C	W	0x00000202	SDRAM Timing Register 7
DDRCTL_FREQ2_DRAMTMG8	0x3120	W	0x03034405	SDRAM Timing Register 8
DDRCTL_FREQ2_DRAMTMG9	0x3124	W	0x0004040D	SDRAM Timing Register 9
DDRCTL_FREQ2_DRAMTMG10	0x3128	W	0x001C180A	SDRAM Timing Register 10
DDRCTL_FREQ2_DRAMTMG11	0x312C	W	0x440C021C	SDRAM Timing Register 11
DDRCTL_FREQ2_DRAMTMG12	0x3130	W	0x1A020010	SDRAM Timing Register 12
DDRCTL_FREQ2_DRAMTMG13	0x3134	W	0x1C200004	SDRAM Timing Register 13
DDRCTL_FREQ2_DRAMTMG14	0x3138	W	0x000000A0	SDRAM Timing Register 14
DDRCTL_FREQ2_DRAMTMG15	0x313C	W	0x00000000	SDRAM Timing Register 15

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Name	Offset	Size	Reset Value	Description
DDRCTL_FREQ2_ZQCTL0	0x3180	W	0x02000040	ZQ Control Register 0
DDRCTL_FREQ2_DFITMG0	0x3190	W	0x07020002	DFI Timing Register 0
DDRCTL_FREQ2_DFITMG1	0x3194	W	0x00000404	DFI Timing Register 1
DDRCTL_FREQ2_DFITMG2	0x31B4	W	0x00000202	DFI Timing Register 2
DDRCTL_FREQ2_DFITMG3	0x31B8	W	0x00000000	DFI Timing Register 3
DDRCTL_FREQ2_ODTCFG	0x3240	W	0x04000400	ODT Configuration Register
DDRCTL_FREQ3_DERATEEN	0x4020	W	0x00000000	Temperature Derate Enable Register
DDRCTL_FREQ3_DERATEINT	0x4024	W	0x00800000	Temperature Derate Interval Register
DDRCTL_FREQ3_PWRTMG	0x4034	W	0x00402010	Low Power Timing Register
DDRCTL_FREQ3_RFSHCTL0	0x4050	W	0x00210000	Refresh Control Register 0
DDRCTL_FREQ3_RFSHTMG	0x4064	W	0x0062008C	Refresh Timing Register
DDRCTL_FREQ3_RFSHTMG1	0x4068	W	0x008C0000	Refresh Timing Register1
DDRCTL_FREQ3_INIT3	0x40DC	W	0x00000510	SDRAM Initialization Register 3
DDRCTL_FREQ3_INIT4	0x40E0	W	0x00000000	SDRAM Initialization Register 4
DDRCTL_FREQ3_INIT6	0x40E8	W	0x00000000	SDRAM Initialization Register 6
DDRCTL_FREQ3_INIT7	0x40EC	W	0x00000000	SDRAM Initialization Register 7
DDRCTL_FREQ3_RANKCTL	0x40F4	W	0x00000660	Rank Control Register
DDRCTL_FREQ3_DRAMTMG0	0x4100	W	0x0F101B0F	SDRAM Timing Register 0
DDRCTL_FREQ3_DRAMTMG1	0x4104	W	0x00080414	SDRAM Timing Register 1
DDRCTL_FREQ3_DRAMTMG2	0x4108	W	0x0305060D	SDRAM Timing Register 2
DDRCTL_FREQ3_DRAMTMG3	0x410C	W	0x0050400C	SDRAM Timing Register 3
DDRCTL_FREQ3_DRAMTMG4	0x4110	W	0x05040405	SDRAM Timing Register 4
DDRCTL_FREQ3_DRAMTMG5	0x4114	W	0x05050403	SDRAM Timing Register 5
DDRCTL_FREQ3_DRAMTMG6	0x4118	W	0x02020005	SDRAM Timing Register 6
DDRCTL_FREQ3_DRAMTMG7	0x411C	W	0x00000202	SDRAM Timing Register 7
DDRCTL_FREQ3_DRAMTMG8	0x4120	W	0x03034405	SDRAM Timing Register 8
DDRCTL_FREQ3_DRAMTMG9	0x4124	W	0x0004040D	SDRAM Timing Register 9
DDRCTL_FREQ3_DRAMTMG10	0x4128	W	0x001C180A	SDRAM Timing Register 10
DDRCTL_FREQ3_DRAMTMG11	0x412C	W	0x440C021C	SDRAM Timing Register 11
DDRCTL_FREQ3_DRAMTMG12	0x4130	W	0x1A020010	SDRAM Timing Register 12
DDRCTL_FREQ3_DRAMTMG13	0x4134	W	0x1C200004	SDRAM Timing Register 13
DDRCTL_FREQ3_DRAMTMG14	0x4138	W	0x000000A0	SDRAM Timing Register 14

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Name	Offset	Size	Reset Value	Description
DDRCTL_FREQ3_DRAMTMG15	0x413C	W	0x00000000	SDRAM Timing Register 15
DDRCTL_FREQ3_ZQCTL0	0x4180	W	0x02000040	ZQ Control Register 0
DDRCTL_FREQ3_DFITMG0	0x4190	W	0x07020002	DFI Timing Register 0
DDRCTL_FREQ3_DFITMG1	0x4194	W	0x00000404	DFI Timing Register 1
DDRCTL_FREQ3_DFITMG2	0x41B4	W	0x00000202	DFI Timing Register 2
DDRCTL_FREQ3_DFITMG3	0x41B8	W	0x00000000	DFI Timing Register 3
DDRCTL_FREQ3_ODTCFG	0x4240	W	0x04000400	ODT Configuration Register

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

13.4.3 Detail Registers Description

DDRCTL_MSTR

Address: Operational Base(0xFF4E0000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	device_config Indicates the configuration of the device used in the system. 00 - x4 device 01 - x8 device 10 - x16 device 11 - x32 device Value After Reset:0x0 Programming Mode:Static
29	RW	0x0	frequency_mode Selects which registers are used. 0 - Original registers 1 - When UMCTL2_FREQUENCY_NUM=2: FREQ1 registers When UMCTL2_FREQUENCY_NUM>2: Choosen by MSTR2.target_frequency register. At boot time, this register must be set to 0 and the original register values are used. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2
28:26	RW	0x0	Reserved4 Reserved Field:Yes
25:24	RW	0x3	active_ranks Only present for multi-rank configurations. Each bit represents one rank. For two-rank configurations, only bits[25:24] are present. 1 - Populated 0 - Unpopulated LSB is the lowest rank number. For two ranks following combinations are legal: 01 - One rank 11 - Two ranks Others - Reserved For four ranks following combinations are legal: 0001 - One rank 0011 - Two ranks 1111 - Four ranks Value After Reset:0x3 Programming Mode:Static
23:20	RW	0x0	Reserved3 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
19:16	RW	0x4	burst_rdwr Indicates SDRAM burst length used: 0001 - Burst length of 2 (only supported for mDDR) 0010 - Burst length of 4 0100 - Burst length of 8 1000 - Burst length of 16 (only supported for mDDR, LPDDR2, and LPDDR4) All other values are reserved. This bit controls the burst size used to access the SDRAM. This must match the burst length mode register setting in the SDRAM. (For BC4/8 on-the-fly mode of DDR3 and DDR4, set this field to 0x0100) Burst length of 2 is not supported with AXI ports when MEMC_BURST_LENGTH is 8. Burst length of 2 is only supported when the controller is operating in 1:1 frequency mode. For DDR3, DDR4 and LPDDR3, this must be set to 0x0100 (BL8). For LPDDR4, this must be set to 0x1000 (BL16). Value After Reset:0x4 Programming Mode:Static
15	RW	0x0	dll_off_mode Set to: 1 - When the uMCTL2 and DRAM has to be put in DLL-off mode for low frequency operation 0 - To put uMCTL2 and DRAM in DLL-on mode for normal frequency operation If DDR4 CRC/parity retry is enabled (CRCPARCTL1.crc_parity_retry_enable = 1), dll_off_mode is not supported, and this bit must be set to '0'. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2
14	RW	0x0	Reserved2 Reserved Field:Yes
13:12	RW	0x0	data_bus_width Selects proportion of DQ bus width that is used by the SDRAM. 00 - Full DQ bus width to SDRAM 01 - Half DQ bus width to SDRAM 10 - Quarter DQ bus width to SDRAM 11 - Reserved Note that half bus width mode is only supported when the SDRAM bus width is a multiple of 16, and quarter bus width mode is only supported when the SDRAM bus width is a multiple of 32 and the configuration parameter MEMC_QBUS_SUPPORT is set. Bus width refers to DQ bus width (excluding any ECC width). Value After Reset:0x0 Programming Mode:Static

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Bit	Attr	Reset Value	Description
11	RW	0x0	geardown_mode 1 - Indicates the DRAM in geardown mode (2N) 0 - Indicates the DRAM in normal mode (1N) This register can be changed, only when the controller is in the self-refresh mode. This signal must be set the same value as MR3 bit A3. Note: Geardown mode is not supported if the configuration parameter MEMC_CMD_RTN2IDLE is set Geardown mode is not supported if the configuration parameter UMCTL2_SHARED_AC is set (in Shared-AC mode) and the register value is don't care Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2
10	RW	0x0	en_2t_timing_mode If 1, then uMCTL2 uses 2T timing, otherwise uses 1T timing. In 2T timing, all command signals (except chip select) are held for 2 clocks on the SDRAM bus. Chip select is asserted on the second cycle of the command. Note: 2T timing is not supported in LPDDR2/LPDDR3/LPDDR4 mode 2T timing is not supported if the configuration parameter MEMC_CMD_RTN2IDLE is set 2T timing is not supported in DDR4 geardown mode 2T timing is not supported in Shared-AC dual channel mode and the register value is don't care Value After Reset:0x0 Programming Mode:Static
9	RW	0x0	burstchop When this bit is set, enables burst-chop (BC4 or 8 on-the-fly) in DDR3/DDR4. Burst Chop for reads is exercised only: In HIF configurations (UMCTL2_INCL_ARB not set) If in full bus width mode (MSTR.data_bus_width = 00) If MEMC_BURST_LENGTH=8 or 16 Burst Chop for writes is exercised only: If CRC is disabled (CRCPARCTL1.crc_enable = 0) BC4 (fixed) mode is not supported. Value After Reset:0x0 Programming Mode:Static
8:6	RW	0x0	Reserved1 Reserved Field:Yes
5	RW	0x0	lpddr4 Selects LPDDR4 SDRAM. 1 - LPDDR4 SDRAM device in use 0 - non-LPDDR4 device in use Present only in designs configured to support LPDDR4. Value After Reset:0x0 Programming Mode:Static
4	RW	0x0	ddr4 Selects DDR4 SDRAM. 1 - DDR4 SDRAM device in use 0 - non-DDR4 device in use Present only in designs configured to support DDR4. Value After Reset:0x0 Programming Mode:Static

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Bit	Attr	Reset Value	Description
3	RW	0x0	lpddr3 Selects LPDDR3 SDRAM. 1 - LPDDR3 SDRAM device in use 0 - non-LPDDR3 device in use Present only in designs configured to support LPDDR3. Value After Reset:0x0 Programming Mode:Static
2	RW	0x0	lpddr2 Selects LPDDR2 SDRAM. 1 - LPDDR2 SDRAM device in use 0 - non-LPDDR2 device in use Present only in designs configured to support LPDDR2. Value After Reset:0x0 Programming Mode:Static
1	RW	0x0	Reserved0 Reserved Field:Yes
0	RW	0x1	ddr3 Selects DDR3 SDRAM. 1 - DDR3 SDRAM device in use 0 - non-DDR3 SDRAM device in use Present only in designs configured to support DDR3. Value After Reset:0x1 Programming Mode:Static

DDRCTL_STAT

Address: Operational Base(0xFF4E0000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:13	RW	0x00000	Reserved3 Reserved Field:Yes
12	RO	0x0	selfref_cam_not_empty Self-refresh with CAMs not empty. Set to 1 when self-refresh is entered but CAMs are not drained. Cleared after exiting self-refresh. Value After Reset:0x0 Programming Mode:Static
11:10	RW	0x0	Reserved2 Reserved Field:Yes
9:8	RO	0x0	selfref_state This indicates self-refresh or self-refresh power down state for LPDDR4. This register is used for frequency change and MRR/MRW access during self-refresh. 00 - SDRAM is not in self-refresh 01 - Self-refresh 1 10 - Self-refresh power down 11 - Self-refresh 2 Value After Reset:0x0 Programming Mode:Static
7:6	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
5:4	RO	0x0	selfref_type Flags if self-refresh (except LPDDR4), or SR-Powerdown (LPDDR4) is entered, and if it is under automatic self-refresh control only or not. 00 - SDRAM is not in self-refresh (except LPDDR4) or SR-Powerdown (LPDDR4). If retry is enabled by CRCPARCTL1.crc_parity_retry_enable, this also indicates that the SRE command is still in parity error window or retry is in-progress. 11 - SDRAM is in self-refresh (except LPDDR4) or SR-Powerdown (LPDDR4), which was caused by Automatic self-refresh only. If retry is enabled, this ensures that the SRE command is executed correctly without parity error. 10 - SDRAM is in self-refresh (except LPDDR4) or SR-Powerdown (LPDDR4), which was not caused solely under automatic self-refresh control. It could have been caused by Hardware Low Power Interface and/or Software (PWRCTL.selfref_sw). If retry is enabled, this ensures that the SRE command is executed correctly without parity error. 01 - SDRAM is in self-refresh, which is caused by PHY Master Request. Value After Reset:0x0 Programming Mode:Static
3	RW	0x0	Reserved0 Reserved Field:Yes
2:0	RO	0x0	operating_mode This is 3-bits wide in configurations with mDDR/LPDDR2/LPDDR3/LPDDR4/DDR4 support and 2-bits in all other configurations. non-mDDR/LPDDR2/LPDDR3/LPDDR4 and non-DDR4 designs: 00 - Init 01 - Normal 10 - Power-down 11 - Self-refresh mDDR/LPDDR2/LPDDR3 or DDR4 designs: 000 - Init 001 - Normal 010 - Power-down 011 - Self-refresh 1XX - Deep power-down/Maximum Power Saving Mode LPDDR4 designs: 000 - Init 001 - Normal 010 - Power-down 011 - Self-refresh/Self-refresh power-down Value After Reset:0x0 Programming Mode:Static

DDRCTL_MRCTRL0

Address: Operational Base(0xFF4E0000) + offset (0x0010)

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Bit	Attr	Reset Value	Description
31	RW	0x0	mr_wr Setting this register bit to 1 triggers a mode register read or write operation. When the MR operation is complete, the uMCTL2 automatically clears this bit. The other fields of this register must be written in a separate APB transaction, before setting this mr_wr bit. It is recommended NOT to set this signal if in Init, Deep power-down, or MPSM operating modes. Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic
30	RW	0x0	pba_mode Indicates whether PBA access is executed. When setting this bit to 1 along with setting pda_en to 1, uMCTL2 initiates PBA access instead of PDA access. 0 - Per DRAM Addressability mode 1 - Per Buffer Addressability mode The completion of PBA access is confirmed by MRSTAT.pda_done in the same way as PDA. Value After Reset:0x0 Programming Mode:Dynamic
29:16	RW	0x0000	Reserved1 Reserved Field:Yes
15:12	RW	0x0	mr_addr Address of the mode register that is to be written to. 0000 - MR0 0001 - MR1 0010 - MR2 0011 - MR3 0100 - MR4 0101 - MR5 0110 - MR6 0111 - MR7 Don't Care for LPDDR2/LPDDR3/LPDDR4 (see MRCTRL1.mr_data for mode register addressing in LPDDR2/LPDDR3/LPDDR4). This signal is also used for writing to control words of the register chip on RDIMMs/LRDIMMs. In this case, it corresponds to the bank address bits sent to the RDIMM/LRDIMM. In case of DDR4, the bit[3:2] corresponds to the bank group bits. Therefore, the bit[3] as well as the bit[2:0] must be set to an appropriate value which is considered both the Address Mirroring of UDIMMs/RDIMMs/LRDIMMs and the Output Inversion of RDIMMs/LRDIMMs. Value After Reset:0x0 Programming Mode:Dynamic
11:6	RW	0x00	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
5:4	RW	0x3	mr_rank Controls which rank is accessed by MRCTRL0.mr_wr. Normally, it is desired to access all ranks, so all bits must be set to 1. However, for multi-rank UDIMMs/RDIMMs/LRDIMMs which implement address mirroring, it might be necessary to access ranks individually. Examples (assuming uMCTL2 is configured for 4 ranks): 0x1 - Select rank 0 only 0x2 - Select rank 1 only 0x5 - Select ranks 0 and 2 0xA - Select ranks 1 and 3 0xF - Select ranks 0, 1, 2 and 3 Value After Reset:0x3 Programming Mode:Dynamic
3	RW	0x0	sw_init_int Indicates whether software intervention is allowed through MRCTRL0/MRCTRL1 before automatic SDRAM initialization routine or not. For DDR4, this bit can be used to initialize the DDR4 RCD (MR7) before automatic SDRAM initialization. For LPDDR4, this bit can be used to program additional mode registers before automatic SDRAM initialization if necessary. In LPDDR4 dual channel mode, note that this must be programmed to both channels beforehand. Note that this must be cleared to 0 after completing Software operation. Otherwise, SDRAM initialization routine does not re-start. 0 - Software intervention is not allowed 1 - Software intervention is allowed Value After Reset:0x0 Programming Mode:Dynamic
2	RW	0x0	pda_en Indicates whether the mode register operation is MRS in PDA mode or not. 0 - MRS 1 - MRS in Per DRAM Addressability mode Note that when pba_mode=1, PBA access is initiated instead of PDA access. Value After Reset:0x0 Programming Mode:Dynamic
1	RW	0x0	mpr_en Indicates whether the mode register operation is MRS or WR/RD for MPR (only supported for DDR4). 0 - MRS 1 - WR/RD for MPR Value After Reset:0x0 Programming Mode:Dynamic
0	RW	0x0	mr_type Indicates whether the mode register operation is read or write. Only used for LPDDR2/LPDDR3/LPDDR4/DDR4. 0 - Write 1 - Read Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_MRCTRL1

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Address: Operational Base(0xFF4E0000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	Reserved0 Reserved Field:Yes
17:0	RW	0x00000	mr_data Mode register write data for all non-LPDDR2/non-LPDDR3/non-LPDDR4 modes. For LPDDR2/LPDDR3/LPDDR4, MRCTRL1[15:0] are interpreted as: [15:8] - MR Address [7:0] - MR data for writes, don't care for reads This is 18-bits wide in configurations with DDR4 support and 16-bits in all other configurations. Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_MRSTAT

Address: Operational Base(0xFF4E0000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:9	RW	0x000000	Reserved1 Reserved Field:Yes
8	RO	0x0	pda_done The SoC might initiate a MR write operation in PDA/PBA mode only if this signal is low. This signal goes: High when three consecutive MRS commands related to the PDA/PBA mode are issued to the SDRAM Low when MRCTRL0.pda_en becomes 0 Therefore, it is recommended to write MRCTRL0.pda_en to 0 after this signal goes high in order to prepare to perform PDA operation next time. 0 - Indicates that mode register write operation related to PDA/PBA is in progress or has not started yet 1 - Indicates that mode register write operation related to PDA/PBA has competed Value After Reset:0x0 Programming Mode:Dynamic
7:1	RW	0x00	Reserved0 Reserved Field:Yes
0	RO	0x0	mr_wr_busy The SoC might initiate a MR write operation only if this signal is low. This signal goes: High in the clock after the uMCTL2 accepts the MRW/MRR request Low when the MRW/MRR command is issued to the SDRAM It is recommended not to perform MRW/MRR commands when 'MRSTAT.mr_wr_busy' is high. 0 - Indicates that the SoC can initiate a mode register write operation 1 - Indicates that mode register write operation is in progress Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_MRCTRL2

Address: Operational Base(0xFF4E0000) + offset (0x001C)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mr_device_sel Indicates the devices to be selected during the MRS that happens in PDA mode. Each bit is associated with one device. For example, bit[0] corresponds to Device 0, bit[1] to Device 1 and so on. 1 - Indicates that the MRS command must be applied to that device 0 - Indicates that the MRS commands must be skipped for that device Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_DERATEEN

Address: Operational Base(0xFF4E0000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	Reserved2 Reserved Field:Yes
13	RW	0x0	derate_mr4_pause_fc Pauses MR4 reads. Must only be set to 1 as part of Frequency Change procedures, if DERATEEN.derate_enable=1 Value After Reset:0x0 Programming Mode:Dynamic
12	RW	0x0	derate_mr4_tuf_dis Disables use of MR4 TUF flag (MR4[7]) bit. 0 - Use MR4 TUF flag (MR4[7]) 1 - Do not use MR4 TUF Flag (MR4[7]) For LPDDR4, it is recommended to set this register to 1. For LPDDR2 and LPDDR3, contact your memory vendor for recommended usage. This affects both the periodic derate logic (DERATEEN.derate_enable) and the derate_temp_limit_intr. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4
11	RW	0x0	Reserved1 Reserved Field:Yes
10:8	RW	0x0	rc_derate_value Derate value of tRC for LPDDR4. 0 - Derating uses +1 1 - Derating uses +2 2 - Derating uses +3 3 - Derating uses +4 4 - Derating uses +5 5 - Derating uses +6 6 - Derating uses +7 7 - Derating uses +8 Present only in designs configured to support LPDDR4. The required cycles for derating can be determined by dividing 3.75ns by the core_ddrc_core_clk period, and rounding it up to the next integer. Hence this register field must be set to the previous value - 1. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	derate_byte This bit indicates which byte of the MRR data is used for derating. The maximum valid value depends on MEMC_DRAM_TOTAL_DATA_WIDTH. Present only in designs configured to support LPDDR2/LPDDR3/LPDDR4. Value After Reset:0x0 Programming Mode:Static
3	RW	0x0	Reserved0 Reserved Field:Yes
2:1	RW	0x0	derate_value Derate value. 0 - Derating uses +1 1 - Derating uses +2 2 - Derating uses +3 3 - Derating uses +4 Present only in designs configured to support LPDDR2/LPDDR3/LPDDR4. The required cycles for derating can be determined by dividing 1.875ns by the core_ddrc_core_clk period, and rounding it up to the next integer. Hence this register field must be set to the previous value - 1. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4
0	RW	0x0	derate_enable Enables derating. 0 - Timing parameter derating is disabled 1 - Timing parameter derating is enabled using MR4 read value Present only in designs configured to support LPDDR2/LPDDR3/LPDDR4. This field must be set to '0' for non-LPDDR2/LPDDR3/LPDDR4 mode. Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_DERATEINT

Address: Operational Base(0xFF4E0000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RW	0x00800000	mr4_read_interval Interval between two MR4 reads, used to derate the timing parameters. Present only in designs configured to support LPDDR2/LPDDR3/LPDDR4. This register must not be set to zero. Unit: DFI clock cycles. Value After Reset:0x800000 Programming Mode:Static

DDRCTL_MSTR2

Address: Operational Base(0xFF4E0000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
1:0	RW	0x1	target_frequency If MSTR.frequency_mode = 1, this field specifies the target frequency. 0 - Frequency 0/Normal 1 - Frequency 1/FREQ1 2 - Frequency 2/FREQ2 3 - Frequency 3/FREQ3 If MSTR.frequency_mode=0, this field is ignored. Note: If the target frequency can be changed through Hardware Low Power Interface only, this field is not needed. Value After Reset:0x1 Programming Mode:Quasi-dynamic Group 2

DDRCTL_DERATECTL

Address: Operational Base(0xFF4E0000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	Reserved0 Reserved Field:Yes
2	RW	0x0	derate_temp_limit_intr_force Interrupt force bit for derate_temp_limit_intr. Setting this field to 1 causes the derate_temp_limit_intr output pin to be asserted. At the end of the interrupt force operation, the uMCTL2 automatically clears this bit. Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic
1	RW	0x0	derate_temp_limit_intr_clr Interrupt clear bit for derate_temp_limit_intr. At the end of the interrupt clear operation, the uMCTL2 automatically clears this bit. Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic
0	RW	0x1	derate_temp_limit_intr_en Interrupt enable bit for derate_temp_limit_intr output pin. 1 - Enabled 0 - Disabled Value After Reset:0x1 Programming Mode:Dynamic

DDRCTL_PWRCTL

Address: Operational Base(0xFF4E0000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:9	RW	0x000000	Reserved0 Reserved Field:Yes
8	RW	0x0	lpddr4_sr_allowed Indicates whether transition from SR-PD to SR and back to SR-PD is allowed. This register field cannot be modified while PWRCTL.selfref_sw == 1. 0 - SR-PD -> SR -> SR-PD not allowed 1 - SR-PD -> SR -> SR-PD allowed Value After Reset:0x0 Programming Mode:Dynamic

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Bit	Attr	Reset Value	Description
7	RW	0x0	dis_cam_drain_selfref Indicates whether skipping CAM draining is allowed when entering self-refresh. This register field cannot be modified while PWRCTL.selfref_sw == 1. 0 - CAMs must be empty before entering SR 1 - CAMs are not emptied before entering SR (unsupported) Note, PWRCTL.dis_cam_drain_selfref=1 is unsupported in this release. PWRCTL.dis_cam_drain_selfref=0 is required. Value After Reset:0x0 Programming Mode:Dynamic
6	RW	0x0	stay_in_selfref Self-refresh state is an intermediate state to enter to self-refresh power down state or exit self-refresh power down state for LPDDR4. This register controls transition from the self-refresh state. 1 - Prohibit transition from self-refresh state 0 - Allow transition from self-refresh state Value After Reset:0x0 Programming Mode:Dynamic
5	RW	0x0	selfref_sw A value of 1 to this register causes system to move to self-refresh state immediately, as long as it is not in INIT or DPD/MPSM operating_mode. This is referred to as Software Entry/Exit to self-refresh. 1 - Software Entry to self-refresh 0 - Software Exit from self-refresh Value After Reset:0x0 Programming Mode:Dynamic
4	RW	0x0	mpsm_en When this bit is 1, the uMCTL2 puts the SDRAM into maximum power saving mode when the transaction store is empty. This register must be reset to '0' to bring uMCTL2 out of maximum power saving mode. Present only in designs configured to support DDR4. For non-DDR4, this register must not be set to 1. Note that MPSM is not supported when using a Synopsys DWC DDR PHY, if the PHY parameter DWC_AC_CS_USE is disabled, as the MPSM exit sequence requires the chip-select signal to toggle. FOR PERFORMANCE ONLY. Value After Reset:0x0 Programming Mode:Dynamic

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Bit	Attr	Reset Value	Description
3	RW	0x0	en_dfi_dram_clk_disable Enables the assertion of dfi_dram_clk_disable whenever a clock is not required by the SDRAM. If set to 0, dfi_dram_clk_disable is never asserted. Assertion of dfi_dram_clk_disable is as follows: In DDR2/DDR3, can only be asserted in self-refresh. In DDR4, can be asserted in following: In Self-refresh In Maximum Power Saving Mode In mDDR/LPDDR2/LPDDR3, can be asserted in following: In Self-refresh In Power Down In Deep Power Down During Normal operation (Clock Stop) In LPDDR4, can be asserted in following: In Self-refresh Power Down In Power Down During Normal operation (Clock Stop) Value After Reset:0x0 Programming Mode:Dynamic
2	RW	0x0	deeppowerdown_en When this bit is 1, uMCTL2 puts the SDRAM into deep power-down mode when the transaction store is empty. This register must be reset to '0' to bring uMCTL2 out of deep power-down mode. The controller performs automatic SDRAM initialization on deep power-down exit. Present only in designs configured to support mDDR or LPDDR2 or LPDDR3. For non-mDDR/non-LPDDR2/non-LPDDR3, this register must not be set to 1. FOR PERFORMANCE ONLY. Value After Reset:0x0 Programming Mode:Dynamic
1	RW	0x0	powerdown_en If true then the uMCTL2 goes into power-down after a programmable number of cycles "maximum idle clocks before power down" (PWRTMG.powerdown_to_x32). This register bit may be re-programmed during the course of normal operation. Value After Reset:0x0 Programming Mode:Dynamic
0	RW	0x0	selfref_en If true then the uMCTL2 puts the SDRAM into self-refresh after a programmable number of cycles "maximum idle clocks before self-refresh (PWRTMG.selfref_to_x32)". This register bit may be re-programmed during the course of normal operation. Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_PWRTMG

Address: Operational Base(0xFF4E0000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
23:16	RW	0x40	selfref_to_x32 After this many clocks of the DDRC command channel being idle the uMCTL2 automatically puts the SDRAM into self-refresh. The DDRC command channel is considered idle when there are no HIF commands outstanding. This must be enabled in the PWRCTL.selfref_en. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x40 Programming Mode:Quasi-dynamic Group 4
15:8	RW	0x20	t_dpd_x4096 Minimum deep power-down time. For mDDR, value from the JEDEC specification is 0 as mDDR exits from deep power-down mode immediately after PWRCTL.deeppowerdown_en is de-asserted. For LPDDR2/LPDDR3, value from the JEDEC specification is 500us. Present only in designs configured to support mDDR, LPDDR2 or LPDDR3. FOR PERFORMANCE ONLY. Unit: Multiples of 4096 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x20 Programming Mode:Quasi-dynamic Group 4
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4:0	RW	0x10	powerdown_to_x32 After this many clocks of the DDRC command channel being idle the uMCTL2 automatically puts the SDRAM into power-down. The DDRC command channel is considered idle when there are no HIF commands outstanding. This must be enabled in the PWRCTL.powerdown_en. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x10 Programming Mode:Quasi-dynamic Group 4

DDRCTL_HWLPCTL

Address: Operational Base(0xFF4E0000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
27:16	RW	0x000	hw_lp_idle_x32 Hardware idle period. The cactive_ddrc output is driven low if the DDRC command channel is idle for hw_lp_idle * 32 cycles if not in INIT or DPD/MPSM operating_mode. The DDRC command channel is considered idle when there are no HIF commands outstanding. The hardware idle function is disabled when hw_lp_idle_x32=0. hw_lp_idle_x32=1 is an illegal value. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x0 Programming Mode:Static
15:2	RW	0x0000	Reserved0 Reserved Field:Yes
1	RW	0x1	hw_lp_exit_idle_en When this bit is programmed to 1 the cactive_in_ddrc pin of the DDRC can be used to exit from the automatic clock stop, automatic power down or automatic self-refresh modes. Note, it does not cause exit of self-refresh that was caused by Hardware Low Power Interface and/or Software (PWRCTL.selfref_sw). Value After Reset:0x1 Programming Mode:Static
0	RW	0x1	hw_lp_en Enable this bit for Hardware Low Power Interface. Value After Reset:0x1 Programming Mode:Quasi-dynamic Group 2

DDRCTL_RFSHCTL0

Address: Operational Base(0xFF4E0000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved4 Reserved Field:Yes
23:20	RW	0x2	refresh_margin Threshold value in number of DFI clock cycles before the critical refresh or page timer expires. A critical refresh is to be issued before this threshold is reached. It is recommended that this not be changed from the default value, currently shown as 0x2. It must always be less than internally used t_rfc_nom/32. Note that internally used t_rfc_nom is equal to RFSHTMG.t_rfc_nom_x1_x32 * 32 if RFSHTMG.t_rfc_nom_x1_sel=0. If RFSHTMG.t_rfc_nom_x1_sel=1 (for LPDDR2/LPDDR3/LPDDR4 per-bank refresh only), internally used t_rfc_nom is equal to RFSHTMG.t_rfc_nom_x1_x32. Note that, in LPDDR2/LPDDR3/LPDDR4, internally used t_rfc_nom may be divided by four if derating is enabled (DERATEEN.derate_enable=1). Unit: Multiples of 32 DFI clock cycles. Value After Reset:0x2 Programming Mode:Dynamic - Refresh Related

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Bit	Attr	Reset Value	Description
19:17	RW	0x0	Reserved3 Reserved Field:Yes
16:12	RW	0x10	refresh_to_x1_x32 If the refresh timer (tRFCnom, also known as tREFI) has expired at least once, then a speculative refresh may be performed. A speculative refresh is a refresh performed at a time when refresh would be useful. When the SDRAM bus is idle for a period of time determined by this RFSHCTL0.refresh_to_x1_x32 and the refresh timer has expired at least once since the last refresh, then a speculative refresh is performed. Speculative refreshes continues successively until there are no refreshes pending or until new reads or writes are issued to the uMCTL2. FOR PERFORMANCE ONLY. Unit: DFI clock cycles or multiples of 32 DFI clock cycles, depending on RFSHTMG.t_rfc_nom_x1_sel. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x10 Programming Mode:Dynamic - Refresh Related
11:10	RW	0x0	Reserved2 Reserved Field:Yes
9:4	RW	0x00	refresh_burst The programmed value + 1 is the number of refresh timeouts that is allowed to accumulate before traffic is blocked and the refreshes are forced to execute. Closing pages to perform a refresh is a one-time penalty that must be paid for each group of refreshes. Therefore, performing refreshes in a burst reduces the per-refresh penalty of these page closings. Higher numbers for RFSHCTL.refresh_burst slightly increases utilization; lower numbers decreases the worst-case latency associated with refreshes. 0 - Single refresh 1 - Burst-of-2 refresh 7 - Burst-of-8 refresh For more information on burst refresh feature, see section 3.9 of DDR2 JEDEC specification - JESD79-2F.pdf. For DDR2/3, the refresh is always per-rank and not per-bank. The rank refresh can be accumulated over 8*tREFI cycles using the burst refresh feature. In DDR4 mode, according to Fine Granularity feature, 8 refreshes can be postponed in 1X mode, 16 refreshes in 2X mode and 32 refreshes in 4X mode. If using PHY-initiated updates, care must be taken in the setting of RFSHCTL0.refresh_burst, to ensure that tRFCmax is not violated due to a PHY-initiated update occurring shortly before a refresh burst is due. In this situation, the refresh burst is delayed until the PHY-initiated update is complete. In per-bank refresh mode of LPDDR2/LPDDR3/LPDDR4 (RFSHCTL0.per_bank_refresh = 1), 64 refreshes can be postponed. Value After Reset:0x0 Programming Mode:Dynamic - Refresh Related

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Bit	Attr	Reset Value	Description
3	RW	0x0	Reserved1 Reserved Field:Yes
2	RW	0x0	per_bank_refresh 1 - Per bank refresh 0 - All bank refresh Per bank refresh allows traffic to flow to other banks. Per bank refresh is not supported by all LPDDR2 devices but must be supported by all LPDDR3/LPDDR4 devices. Present only in designs configured to support LPDDR2/LPDDR3/LPDDR4. Value After Reset:0x0 Programming Mode:Static
1:0	RW	0x0	Reserved0 Reserved Field:Yes

DDRCTL_RFSHCTL1

Address: Operational Base(0xFF4E0000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved1 Reserved Field:Yes
27:16	RW	0x000	refresh_timer1_start_value_x32 Refresh timer start for rank 1 (only present in multi-rank configurations). This is useful in staggering the refreshes to multiple ranks to help traffic to proceed. This is explained in Refresh Controls section of the Architecture chapter. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x0 Programming Mode:Dynamic - Refresh Related
15:12	RW	0x0	Reserved0 Reserved Field:Yes
11:0	RW	0x000	refresh_timer0_start_value_x32 Refresh timer start for rank 0 (only present in multi-rank configurations). This is useful in staggering the refreshes to multiple ranks to help traffic to proceed. This is explained in Refresh Controls section of the Architecture chapter. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x0 Programming Mode:Dynamic - Refresh Related

DDRCTL_RFSHCTL3

Address: Operational Base(0xFF4E0000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:7	RW	0x0000000	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
6:4	RW	0x0	refresh_mode Indicates fine granularity refresh mode. 000 - Fixed 1x (Normal mode) 001 - Fixed 2x 010 - Fixed 4x 101 - Enable on the fly 2x (not supported) 110 - Enable on the fly 4x (not supported) Everything else - reserved Note: Only Fixed 1x mode is supported if RFSHCTL3.dis_auto_refresh = 1 The on-the-fly modes are not supported in this version of the uMCTL2 This must be set up while the controller is in reset or while the controller is in self-refresh mode. Changing this during normal operation is not allowed. Making this a dynamic register is supported in future version of the uMCTL2 This register field has effect only if a DDR4 SDRAM device is in use (MSTR.ddr4 = 1) Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2
3:2	RW	0x0	Reserved0 Reserved Field:Yes
1	RW	0x0	refresh_update_level Toggle this signal (either from 0 to 1 or from 1 to 0) to indicate that the refresh registers have been updated. refresh_update_level must not be toggled when the DDRC is in reset (core_ddrc_rstn = 0). The refresh registers are automatically updated when exiting reset. Value After Reset:0x0 Programming Mode:Dynamic
0	RW	0x0	dis_auto_refresh When '1', disable auto-refresh generated by the uMCTL2. When auto-refresh is disabled, the SoC must generate refreshes using the registers DBGCMD.rankn_refresh. When dis_auto_refresh transitions from 0 to 1, any pending refreshes are immediately scheduled by the uMCTL2. If DDR4 CRC/parity retry is enabled (CRCPARCTL1.crc_parity_retry_enable = 1), disable auto-refresh is not supported, and this bit must be set to '0'. (DDR4 only) If FGR mode is enabled (RFSHCTL3.refresh_mode > 0), disable auto-refresh is not supported, and this bit must be set to '0'. This register field is changeable on the fly. Value After Reset:0x0 Programming Mode:Dynamic - Refresh Related

DDRCTL_RFSHTMG

Address: Operational Base(0xFF4E0000) + offset (0x0064)

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Bit	Attr	Reset Value	Description
31	RW	0x0	t_rfc_nom_x1_sel Specifies whether the RFSHTMG.t_rfc_nom_x1_x32 and RFSHCTL0.refresh_to_x1_x32 register values are x1 or x32. 0 - x32 register values are used 1 - x1 register values are used This applies only when per-bank refresh is enabled (RFSHCTL0.per_bank_refresh=1); if per-bank refresh is not enabled, the x32 register values are used and this register field is ignored. This register field does not exist for configurations which do not support LPDDR2/3/4. For such configurations, the value of this register field can be assumed to be 0, so that RFSHTMG.t_rfc_nom_x1_x32 and RFSHCTL0.refresh_t_x1_x32 are interpreted as x32 register fields Value After Reset:0x0 Programming Mode:Dynamic - Refresh Related
30:28	RW	0x0	Reserved1 Reserved Field:Yes
27:16	RW	0x062	t_rfc_nom_x1_x32 Average time interval between refreshes per rank (Specification: 7.8us for DDR2, DDR3 and DDR4. See JEDEC specification for mDDR, LPDDR2, LPDDR3 and LPDDR4). When the controller is operating in 1:1 mode, set this register to RoundDown(tREFI/tCK) When the controller is operating in 1:2 mode, set this register to RoundDown(RoundDown(tREFI/tCK)/2) In both the previous cases, if RFSHTMG.t_rfc_nom_x1_sel = 0, divide the previous result by 32 and round down. For LPDDR2/LPDDR3/LPDDR4: If using all-bank refreshes (RFSHCTL0.per_bank_refresh = 0), use tREFIab in the previous calculations If using per-bank refreshes (RFSHCTL0.per_bank_refresh = 1), use tREFIpb in the previous calculations For DDR4 mode, tREFI value is different depending on the refresh mode. You must program appropriate value from the spec based on the value programmed in the refresh mode register. Note: RFSHTMG.t_rfc_nom_x1_x32 must be greater than 0x1 If RFSHTMG.t_rfc_nom_x1_sel == 1, RFSHTMG.t_rfc_nom_x1_x32 must be greater than RFSHTMG.t_rfc_min If RFSHTMG.t_rfc_nom_x1_sel == 0, RFSHTMG.t_rfc_nom_x1_x32 * 32 must be greater than RFSHTMG.t_rfc_min In non-DDR4 or DDR4 Fixed 1x mode: RFSHTMG.t_rfc_nom_x1_x32 must be less than or equal to 0xFFE In DDR4 Fixed 2x mode: RFSHTMG.t_rfc_nom_x1_x32 must be less than or equal to 0x7FF In DDR4 Fixed 4x mode: RFSHTMG.t_rfc_nom_x1_x32 must be less than or equal to 0x3FF Unit: DFI clock cycles or multiples of 32 DFI clock cycles, depending on RFSHTMG.t_rfc_nom_x1_sel. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x62 Programming Mode:Dynamic - Refresh Related

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Bit	Attr	Reset Value	Description
15	RW	0x0	lpddr3_trefbw_en Used only when LPDDR3 memory type is connected. Must only be changed when uMCTL2 is in reset. Specifies whether to use the tREFBW parameter (required by some LPDDR3 devices which comply with earlier versions of the LPDDR3 JEDEC specification) or not: 0 - tREFBW parameter not used 1 - tREFBW parameter used Value After Reset:0x0 Programming Mode:Static
14:10	RW	0x00	Reserved0 Reserved Field:Yes
9:0	RW	0x08c	t_rfc_min tRFC (min): Minimum time from refresh to refresh or activate. When the controller is operating in 1:1 mode, t_rfc_min must be set to RoundUp(tRFCmin/tCK). When the controller is operating in 1:2 mode, t_rfc_min must be set to RoundUp(RoundUp(tRFCmin/tCK)/2). In LPDDR2/LPDDR3/LPDDR4 mode: If using all-bank refreshes, the tRFCmin value in the previous equations is equal to tRFCab If using per-bank refreshes, the tRFCmin value in the previous equations is equal to tRFCpb In DDR4 mode, the tRFCmin value in the previous equations is different depending on the refresh mode (fixed 1X,2X,4X) and the device density. You must program the appropriate value from the spec based on the 'refresh_mode' and the device density that is used. Unit: DFI clock cycles. Value After Reset:0x8c Programming Mode:Dynamic - Refresh Related

DDRCTL_RFSHTMG1

Address: Operational Base(0xFF4E0000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x8c	t_pbr2pbr LPDDR4:tpbR2pbR. Per-bank refresh to Per-bank refresh different bank Time. When the controller is operating in 1:1 frequency ratio mode, program this to RoundUp(tpbR2pbR/tCK). When the controller is operating in 1:2 frequency ratio mode, program this to RoundUp(RoundUp(tpbR2pbR/tCK)/2). The tpbR2pbR value in the previous equations is different depending on the device density. You must program the appropriate value from the specification. Register is valid only in LPDDR4 per-bank refresh mode (RFSHCTL0.per_bank_refresh_mode == 1). Value After Reset:0x8c Programming Mode:Dynamic - Refresh Related
15:0	RW	0x0000	Reserved0 Reserved Field:Yes

DDRCTL_CRCPARCTL0

Address: Operational Base(0xFF4E0000) + offset (0x00C0)

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Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	Reserved0 Reserved Field:Yes
2	RW	0x0	dfi_alert_err_cnt_clr Indicates the clear bit for DFI alert error counter. Asserting this bit clears the DFI alert error counter, CRCPARSTAT.dfi_alert_err_cnt. uMCTL2 automatically clears this bit. Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic
1	RW	0x0	dfi_alert_err_int_clr Interrupt clear bit for DFI alert error. If this bit is set, the alert error interrupt on CRCPARSTAT.dfi_alert_err_int is cleared. uMCTL2 automatically clears this bit. Value After Reset:0x0 Testable: readOnly Programming Mode: Dynamic
0	RW	0x0	dfi_alert_err_int_en Interrupt enable bit for DFI alert error. If this bit is set, any parity/CRC error detected on the dfi_alert_n input results in an interrupt being set on CRCPARSTAT.dfi_alert_err_int. Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_CRCPARCTL1

Address: Operational Base(0xFF4E0000) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:13	RW	0x00000	Reserved3 Reserved Field:Yes
12	RW	0x1	caparity_disable_before_sr If DDR4-SDRAM's CA parity is enabled by INIT6.mr5[2:0]!=0 and this register is set to 1, CA parity is automatically disabled before self-refresh entry, and enabled after self-refresh exit by issuing MR5. 1 - CA parity is disabled before self-refresh entry 0 - CA parity is not disabled before self-refresh entry If Geardown is used by MSTR.geardown_mode=1, this register must be set to 1. If this register set to 0, DRAMTMG5.t_ckesr and DRAMTMG5.t_cksre must be increased by PL(Parity latency). Value After Reset:0x1 Programming Mode:Static
11:8	RW	0x0	Reserved2 Reserved Field:Yes
7	RW	0x0	crc_inc_dm CRC calculation setting register. 1 - CRC includes DM signal 0 - CRC not includes DM signal Present only in designs configured to support DDR4. Value After Reset:0x0 Programming Mode:Static
6:5	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
4	RW	0x0	crc_enable CRC enable Register. 1 - Enable generation of CRC 0 - Disable generation of CRC The setting of this register must match the CRC mode register setting in the DRAM. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2
3:1	RW	0x0	Reserved0 Reserved Field:Yes
0	RW	0x0	parity_enable C/A Parity enable register. 1 - Enable generation of C/A parity and detection of C/A parity error 0 - Disable generation of C/A parity and disable detection of C/A parity error If RCD's parity error detection or SDRAM's parity detection is enabled, this register must be 1. Value After Reset:0x0 Programming Mode:Static

DDRCTL_CRCPARSTAT

Address: Operational Base(0xFF4E0000) + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:17	RW	0x0000	Reserved0 Reserved Field:Yes
16	RO	0x0	dfi_alert_err_int DFI alert error interrupt. If a parity/CRC error is detected on dfi_alert_n, and the interrupt is enabled by CRCPARCTL0.dfi_alert_err_int_en, this interrupt bit is set. It remains set until cleared by CRCPARCTL0.dfi_alert_err_int_clr. Value After Reset:0x0 Programming Mode:Static
15:0	RO	0x0000	dfi_alert_err_cnt DFI alert error count. If a parity/CRC error is detected on dfi_alert_n, this counter be incremented. This is independent of the setting of CRCPARCTL0.dfi_alert_err_int_en. It saturates at 0xFFFF, and can be cleared by asserting CRCPARCTL0.dfi_alert_err_cnt_clr. Value After Reset:0x0 Programming Mode:Static

DDRCTL_INIT0

Address: Operational Base(0xFF4E0000) + offset (0x00D0)

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Bit	Attr	Reset Value	Description
31:30	RW	0x0	skip_dram_init If lower bit is enabled the SDRAM initialization routine is skipped. The upper bit decides what state the controller starts up in when reset is removed. 00 - SDRAM Initialization routine is run after power-up 01 - SDRAM Initialization routine is skipped after power-up. The controller starts up in normal Mode 11 - SDRAM Initialization routine is skipped after power-up. The controller starts up in self-refresh Mode 10 - Reserved Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2
29:26	RW	0x0	Reserved1 Reserved Field:Yes
25:16	RW	0x002	post_cke_x1024 Indicates the number of cycles to wait after driving CKE high to start the SDRAM initialization sequence. DDR2 typically requires a 400 ns delay, requiring this value to be programmed to 2 at all clock speeds. LPDDR2/LPDDR3 typically requires this to be programmed for a delay of 200 us. LPDDR4 typically requires this to be programmed for a delay of 2 us. When the controller is operating in 1:2 frequency ratio mode, program this to JEDEC spec value divided by 2, and round it up to the next integer value. Unit: Multiples of 1024 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x2 Programming Mode:Static
15:12	RW	0x0	Reserved0 Reserved Field:Yes
11:0	RW	0x04e	pre_cke_x1024 Indicates the number of cycles to wait after reset before driving CKE high to start the SDRAM initialization sequence. DDR2 specifications typically require this to be programmed for a delay of >= 200 us. LPDDR2/LPDDR3: tINIT1 of 100 ns (min) LPDDR4: tINIT3 of 2 ms (min) When the controller is operating in 1:2 frequency ratio mode, program this to JEDEC spec value divided by 2, and round it up to the next integer value. For DDR3/DDR4 RDIMMs, this must include the time needed to satisfy tSTAB. Unit: Multiples of 1024 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x4e Programming Mode:Static

DDRCTL_INIT1

Address: Operational Base(0xFF4E0000) + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
24:16	RW	0x000	dram_rstn_x1024 Indicates the number of cycles to assert SDRAM reset signal during init sequence. This is only present for designs supporting DDR3, DDR4 or LPDDR4 devices. For use with a Synopsys DDR PHY, this must be set to a minimum of 1. When the controller is operating in 1:2 frequency ratio mode, program this to JEDEC spec value divided by 2, and round it up to the next integer value. Unit: Multiples of 1024 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x0 Programming Mode:Static
15:4	RW	0x000	Reserved0 Reserved Field:Yes
3:0	RW	0x0	pre_ocd_x32 Indicates the wait period before driving the OCD complete command to SDRAM. There is no known specific requirement for this; it may be set to zero. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x0 Programming Mode:Static

DDRCTL_INIT2

Address: Operational Base(0xFF4E0000) + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	Reserved1 Reserved Field:Yes
15:8	RW	0x0d	idle_after_reset_x32 Indicates the idle time after the reset command, tINIT4. Present only in designs configured to support LPDDR2. When the controller is operating in 1:2 frequency ratio mode, program this to JEDEC spec value divided by 2, and round it up to the next integer value. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0xd Programming Mode:Static
7:0	RW	0x00	Reserved0 Reserved Field:Yes

DDRCTL_INIT3

Address: Operational Base(0xFF4E0000) + offset (0x00DC)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr DDR2:Indicates the value to write to MR register. Bit 8 is for DLL and the setting here is ignored. The uMCTL2 sets this bit appropriately. DDR3/DDR4: Value loaded into MR0 register. mDDR: Value to write to MR register. LPDDR2/LPDDR3/LPDDR4 - Value to write to MR1 register Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 1, Group 4
15:0	RW	0x0510	emr DDR2: Indicates the value to write to EMR register. Bits 9:7 are for OCD and the setting in this register is ignored. The uMCTL2 sets those bits appropriately. DDR3/DDR4: Value to write to MR1 register Set bit 7 to 0. mDDR: Value to write to EMR register. LPDDR2/LPDDR3/LPDDR4 - Value to write to MR2 register. Value After Reset:0x510 Programming Mode:Quasi-dynamic Group 4

DDRCTL_INIT4

Address: Operational Base(0xFF4E0000) + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	emr2 DDR2: Indicates the value to write to EMR2 register. DDR3/DDR4: Value to write to MR2 register. LPDDR2/LPDDR3/LPDDR4: Value to write to MR3 register. mDDR: Unused. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 4
15:0	RW	0x0000	emr3 DDR2: Indicates the value to write to EMR3 register. DDR3/DDR4: Value to write to MR3 register. mDDR/LPDDR2/LPDDR3: Unused. LPDDR4: Value to write to MR13 register. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_INIT5

Address: Operational Base(0xFF4E0000) + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
23:16	RW	0x10	dev_zqinit_x32 ZQ initial calibration, tZQINIT. Present only in designs configured to support DDR3 or DDR4 or LPDDR2/LPDDR3. DDR3 typically requires 512 SDRAM clock cycles. DDR4 requires 1024 SDRAM clock cycles. LPDDR2/LPDDR3 requires 1 us. When the controller is operating in 1:2 frequency ratio mode, program this to JEDEC spec value divided by 2, and round it up to the next integer value. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x10 Programming Mode:Static
15:10	RW	0x00	Reserved0 Reserved Field:Yes
9:0	RW	0x004	max_auto_init_x1024 Indicates the maximum duration of the auto initialization, tINIT5. Present only in designs configured to support LPDDR2/LPDDR3. LPDDR2/LPDDR3 typically requires 10 us. Unit: Multiples of 1024 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x4 Programming Mode:Static

DDRCTL_INIT6

Address: Operational Base(0xFF4E0000) + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr4 DDR4 - Indicates the value to be loaded into SDRAM MR4 registers. LPDDR4- Value to be loaded into SDRAM MR11 registers. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4
15:0	RW	0x0000	mr5 DDR4 - Indicates the value to be loaded into SDRAM MR5 registers. LPDDR4- Value to be loaded into SDRAM MR12 registers. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 1, Group 4

DDRCTL_INIT7

Address: Operational Base(0xFF4E0000) + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr22 LPDDR4 - Indicates the value to be loaded into SDRAM MR22 registers. Used in LPDDR4 designs only. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 4

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	mr6 DDR4 - Indicates the value to be loaded into SDRAM MR6 registers. LPDDR4- Value to be loaded into SDRAM MR14 registers. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 4

DDRCTL_DIMMCTL

Address: Operational Base(0xFF4E0000) + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:15	RW	0x00000	Reserved1 Reserved Field:Yes
14	RW	0x0	rcd_b_output_disabled Disables RCD outputs to B-side DRAMs. This field is used only when the uMCTL2 disables CAL mode. This value is written to F0RC0 DA[3] before and after disabling CAL mode. It is recommended to set it to ~DIMMCTL.dimm_output_inv_en except for debug. 1 - Disable B outputs 0 - Enable B outputs Value After Reset:0x0 Programming Mode:Static
13	RW	0x0	rcd_a_output_disabled Disables RCD outputs to A-side DRAMs. This field is used only when the uMCTL2 disables CAL mode. This value is written to F0RC0 DA[2] before and after disabling CAL mode. It is recommended to set it to 0 except for debug. 1 - Disable A outputs 0 - Enable A outputs Value After Reset:0x0 Programming Mode:Static
12	RW	0x0	rcd_weak_drive Indicates the weak drive mode to be set to the RCD. This field is used only when the uMCTL2 disables CAL mode. When weak drive mode in the RCD is enabled during initialization, this field must be set to 1. When RCD is not used, this field must be set to 0. 1 - Enable Weak Drive mode 0 - Disable Weak Drive mode Value After Reset:0x0 Programming Mode:Static
11:7	RW	0x00	Reserved0 Reserved Field:Yes
6	RW	0x0	lrdimm_bcom_cmd_prot Protects the timing restrictions (tBCW/tMRC) between consecutive BCOM commands defined in the Data Buffer specification. When using DDR4 LRDIMM, this bit must be set to 1. Otherwise, this bit must be set to 0. Value After Reset:0x0 Programming Mode:Static

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Bit	Attr	Reset Value	Description
5	RW	0x0	dimm_dis_bg_mirroring Disables address mirroring for BG bits. When this is set to 1, BG0 and BG1 are NOT swapped even if Address Mirroring is enabled. This is required for DDR4 DIMMs with x16 devices. 1 - BG0 and BG1 are NOT swapped 0 - BG0 and BG1 are swapped if address mirroring is enabled Value After Reset:0x0 Programming Mode:Static
4	RW	0x0	mrs_bg1_en Enable this field for BG1 bit of MRS command. BG1 bit of the mode register address is specified as RFU (Reserved for Future Use) and must be programmed to 0 during MRS. In case where DRAMs that do not have BG1 are attached, and both the CA parity and the output inversion are enabled, this must be set to 0, so that the calculation of CA parity does not include BG1 bit. Note: This has no effect on the address of any other memory accesses, or of software-driven mode register accesses. If address mirroring is enabled, this is applied to BG1 of even ranks and BG0 of odd ranks. 1 - Enabled 0 - Disabled Value After Reset:0x0 Programming Mode:Static
3	RW	0x0	mrs_a17_en Enable this field for A17 bit of MRS command. A17 bit of the mode register address is specified as RFU (Reserved for Future Use) and must be programmed to 0 during MRS. In case where DRAMs that do not have A17 are attached as DDR4 RDIMM/LRDIMM, and the output inversion is enabled, this must be set to 0, so that the calculation of CA parity does not include A17 bit. To keep consistency with the RCD, DA[3] in F0RC08 of the RCD also needs to be set to 1 (that is, Disabled). Note: This has no effect on the address of any other memory accesses, or of software-driven mode register accesses. 1 - Enabled 0 - Disabled Value After Reset:0x0 Programming Mode:Static

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Bit	Attr	Reset Value	Description
2	RW	0x0	dimm_output_inv_en Enables output inversion (for DDR4 RDIMM/LRDIMM implementations only). DDR4 RDIMM/LRDIMM implements the Output Inversion feature by default, which means that the following address, bank address, and bank group bits of B-side DRAMs are inverted: A3-A9, A11, A13, A17, BA0-BA1, BG0-BG1. Setting this bit ensures that, for mode register accesses generated by the uMCTL2 during the automatic initialization routine and enabling of a particular DDR4 feature, separate A-side and B-side mode register accesses are generated. For B-side mode register accesses, these bits are inverted within the uMCTL2 to compensate for this RDIMM/LRDIMM inversion. It is recommended to set this bit always, if using DDR4 RDIMMs/LRDIMMs. Note: This has no effect on the address of any other memory accesses, or of software-driven mode register accesses. 1 - Implement output inversion for B-side DRAMs 0 - Do not implement output inversion for B-side DRAMs Value After Reset:0x0 Programming Mode:Static
1	RW	0x0	dimm_addr_mirr_en Enables address mirroring (for multi-rank UDIMM implementations and multi-rank DDR4 RDIMM/LRDIMM implementations). Some UDIMMs and DDR4 RDIMMs/LRDIMMs implement address mirroring for odd ranks, which means that the following address, bank address and bank group bits are swapped: (A3, A4), (A5, A6), (A7, A8), (BA0, BA1) and also (A11, A13), (BG0, BG1) for the DDR4. Setting this bit ensures that, for mode register accesses during the automatic initialization routine, these bits are swapped within the uMCTL2 to compensate for this UDIMM/RDIMM/LRDIMM swapping. In addition to the automatic initialization routine, in case of DDR4 UDIMM/RDIMM/LRDIMM, they are swapped during the automatic MRS access to enable/disable of a particular DDR4 feature. Note: This has no effect on the address of any other memory accesses, or of software-driven mode register accesses. This is not supported for mDDR, LPDDR2, LPDDR3 or LPDDR4 SDRAMs. Note: In case of x16 DDR4 DIMMs, BG1 output of MRS for the odd ranks is same as BG0 because BG1 is invalid, hence dimm_dis_bg_mirroring register must be set to 1. 1 - For odd ranks, implement address mirroring for MRS commands during initialization and for any automatic DDR4 MRS commands (to be used if UDIMM/RDIMM/LRDIMM implements address mirroring) 0 - Do not implement address mirroring Value After Reset:0x0 Programming Mode:Static

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Bit	Attr	Reset Value	Description
0	RW	0x0	dimm_stagger_cs_en Staggering enable for multi-rank accesses (for multi-rank UDIMM, RDIMM and LRDIMM implementations only). This is not supported for mDDR, LPDDR2, LPDDR3 or LPDDR4 SDRAMs. Note: Even if this bit is set it does not take care of software driven MR commands (through MRCTRL0/MRCTRL1), where software is responsible to send them to seperate ranks as appropriate. 1 - (DDR4) Send MRS commands to each ranks seperately 1 - (non-DDR4) Send all commands to even and odd ranks seperately 0 - Do not stagger accesses Value After Reset:0x0 Programming Mode:Static

DDRCTL_RANKCTL

Address: Operational Base(0xFF4E0000) + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	Reserved2 Reserved Field:Yes
26	RW	0x0	diff_rank_wr_gap_msb Only present for multi-rank configurations. 1-bit extension to be used when RANKCTL.diff_rank_wr_gap field needs to be set to a value greater than 0xF. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2
25	RW	0x0	Reserved1 Reserved Field:Yes
24	RW	0x0	diff_rank_rd_gap_msb Only present for multi-rank configurations. 1-bit extension to be used when RANKCTL.diff_rank_rd_gap field needs to be set to a value greater than 0xF. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2
23:16	RW	0x00	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
15:12	RW	0x0	max_rank_wr Only present for multi-rank configurations. Background: Writes to the same rank can be performed back-to-back. Writes to different ranks require additional gap dictated by the register RANKCTL.diff_rank_wr_gap. This is to avoid possible data bus contention as well as to give PHY enough time to switch the delay when changing ranks. The uMCTL2 arbitrates for bus access on a cycle-by-cycle basis; therefore after a write is scheduled, there are few clock cycles (determined by the value on RANKCTL.diff_rank_wr_gap register) in which only writes from the same rank are eligible to be scheduled. This prevents writes from other ranks from having fair access to the data bus. This parameter represents the maximum number of writes that can be scheduled consecutively to the same rank. After this number is reached, a delay equal to RANKCTL.diff_rank_wr_gap is inserted by the scheduler to allow all ranks a fair opportunity to be scheduled. Higher numbers increase bandwidth utilization, lower numbers increase fairness. This feature can be DISABLED by setting this register to 0. When set to 0, the controller stays on the same rank as long as commands are available for it. Minimum programmable value is 0 (feature disabled) and maximum programmable value is 0xF. For uPCTL2, this register field must be set to 0 (feature disabled) FOR PERFORMANCE ONLY. Value After Reset:0x0 Programming Mode:Static

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Bit	Attr	Reset Value	Description
11:8	RW	0x6	diff_rank_wr_gap Only present for multi-rank configurations. Indicates the number of clocks of gap in data responses when performing consecutive writes to different ranks. This is used to switch the delays in the PHY to match the rank requirements. This value must consider both PHY requirement and ODT requirement. PHY requirement - tphy_wrcsgap (For more information on value of tphy_wrcsgap, see PHY databook) ODT requirement - The value programmed in this register takes care of the ODT switch off timing requirement when switching ranks during writes. For LPDDR4, with DQ ODT enabled, diff_rank_wr_gap must be a minimum of ODTLoff - ODTLon - BL/2 + 1 For other cases, diff_rank_wr_gap must be a minimum of ODTCFG.wr_odt_hold - BL/2 When the controller is operating in 1:1 mode, program this to the larger of PHY requirement or ODT requirement. If CRC is enabled, the value can be decreased by 2 because the programmed value is internally increased by 1 (it is always 2 in terms of DFI PHY clock cycle as CRC is supported only with 1:2 frequency ratio). When the controller is operating in 1:2 mode, program this to the larger value divided by two and round it up to the next integer. After PHY has completed training the value programmed may need to be increased. For more information, see relevant PHY documentation. Note that, if using DDR4-LRDIMM, refer to TWRWR timing requirements in JEDEC DDR4 Data Buffer (DDR4DB01) Specification. If a value greater than 0xF is needed, the RANKCTL.diff_rank_wr_gap_msb field must be used as extension. For DFI 1:2 mode, a maximum value of {diff_rank_wr_gap_msb,diff_rank_wr_gap} < 'h11 is supported. For DFI 1:1 mode a maximum value of {diff_rank_wr_gap_msb,diff_rank_wr_gap} <= 'h1F is supported. Unit: DFI clock cycles. Value After Reset:0x6 Programming Mode:Quasi-dynamic Group 2
7:4	RW	0x6	diff_rank_rd_gap Only present for multi-rank configurations. Indicates the number of clocks of gap in data responses when performing consecutive reads to different ranks. This is used to switch the delays in the PHY to match the rank requirements. This value must consider both PHY requirement and ODT requirement. PHY requirement:tphy_rdcsgap (For more information on value of tphy_rdcsgap, see PHY databook) ODT requirement: The value programmed in this register takes care of the ODT switch off timing requirement when switching ranks during reads: Value After Reset:0x6 Programming Mode:Quasi-dynamic Group 2

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	max_rank_rd Only present for multi-rank configurations. Background: Reads to the same rank can be performed back-to-back. Reads to different ranks require additional gap dictated by the register RANKCTL.diff_rank_rd_gap. This is to avoid possible data bus contention as well as to give PHY enough time to switch the delay when changing ranks. The uMCTL2 arbitrates for bus access on a cycle-by-cycle basis; therefore after a read is scheduled, there are few clock cycles (determined by the value on RANKCTL.diff_rank_rd_gap register) in which only reads from the same rank are eligible to be scheduled. This prevents reads from other ranks from having fair access to the data bus. This parameter represents the maximum number of reads that can be scheduled consecutively to the same rank. After this number is reached, a delay equal to RANKCTL.diff_rank_rd_gap is inserted by the scheduler to allow all ranks a fair opportunity to be scheduled. Higher numbers increase bandwidth utilization, lower numbers increase fairness. This feature can be DISABLED by setting this register to 0. When set to 0, the controller stays on the same rank as long as commands are available for it. Minimum programmable value is 0 (feature disabled) and maximum programmable value is 0xF. For uPCTL2, this register field must be set to 0 (feature disabled) FOR PERFORMANCE ONLY. Value After Reset:0x0 Programming Mode:Static

DDRCTL_DRAMTMG0

Address: Operational Base(0xFF4E0000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved3 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
30:24	RW	0x0f	wr2pre Specifies the minimum time between write and precharge to same bank. Specifications: WL + BL/2 + tWR = approximately 8 cycles + 15 ns = 14 clocks @400MHz and less for lower frequencies. where: WL: Write latency BL: Burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM. BST (burst terminate) is not supported at present tWR: Write recovery time. This comes directly from the SDRAM specification Add one extra cycle for LPDDR2/LPDDR3/LPDDR4 for this parameter. When the controller is operating in 1:2 frequency ratio mode, 1T mode, divide the previous value by 2. No rounding up. When the controller is operating in 1:2 frequency ratio mode, 2T mode, geardown mode or LPDDR4 mode, divide the previous value by 2 and round it up to the next integer value. Note that, depending on the PHY, if using LRDIMM, it may be necessary to adjust the value of this parameter to compensate for the extra cycle of latency through the LRDIMM. For DDR4, LPDDR4, LPDDR3, using nWR(WR) instead of tWR to calculate the value of this parameter. Unit: DFI clock cycles. Value After Reset:0xf Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
23:22	RW	0x0	Reserved2 Reserved Field:Yes
21:16	RW	0x10	t_faw tFAW - valid only when 8 or more banks(or banks x bank groups) are present. In 8-bank design, at most 4 banks must be activated in a rolling window of tFAW cycles. When the controller is operating in 1:2 frequency ratio mode, program this to (tFAW/2) and round up to next integer value. In a 4-bank design, set this register to 0x1 independent of the 1:1/1:2 frequency mode. Unit: DFI clock cycles. Value After Reset:0x10 Programming Mode:Quasi-dynamic Group 2, Group 4
15	RW	0x0	Reserved1 Reserved Field:Yes
14:8	RW	0x1b	t_ras_max tRAS(max) - Specifies the maximum time between activate and precharge to same bank. This is the maximum time that a page can be kept open Minimum value of this register is 1. Zero is invalid. When the controller is operating in 1:1 frequency ratio mode, t_ras_max must be set to RoundDown(tRAS(max)/tCK/1024). When the controller is operating in 1:2 frequency ratio mode, t_ras_max must be set to RoundDown((RoundDown(tRAS(max)/tCK/1024)-1)/2). Unit: Multiples of 1024 DFI clock cycles. Value After Reset:0x1b Programming Mode:Quasi-dynamic Group 2, Group 4

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Bit	Attr	Reset Value	Description
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5:0	RW	0x0f	t_ras_min tRAS(min) - Specifies the minimum time between activate and precharge to the same bank. When the controller is operating in 1:1 frequency ratio mode, t_ras_min must be set to RoundUp(tRASmin/tCK) When the controller is operating in 1:2 frequency ratio mode, 1T mode, t_ras_min must be set to RoundDown(RoundUp(tRASmin/tCK)/2) When the controller is operating in 1:2 frequency ratio mode, 2T mode, geardown mode or LPDDR4 mode, t_ras min must be set to RoundUp(RoundUp(tRASmin/tCK)/2) Unit: DFI clock cycles. Value After Reset:0xf Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMTMG1

Address: Operational Base(0xFF4E0000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved2 Reserved Field:Yes
20:16	RW	0x08	t_xp tXP - Specifies the minimum time after power-down exit to any operation. For DDR3, this must be programmed to tXPDLL if slow powerdown exit is selected in MR0[12]. If C/A parity for DDR4 is used, set to (tXP+PL) instead. If LPDDR4 is selected and its spec has tCKELPD parameter, set to the larger of tXP and tCKELPD instead. When the controller is operating in 1:2 frequency ratio mode, program this to (tXP/2) and round it up to the next integer value. Units: DFI clock cycles. Value After Reset:0x8 Programming Mode:Quasi-dynamic Group 2, Group 4
15:14	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
13:8	RW	0x04	rd2pre tRTP - Specifies the minimum time from read to precharge of same bank. DDR2 - tAL + BL/2 + max(RoundUp(tRTP/tCK), 2) - 2 DDR3 - tAL + max (RoundUp(tRTP/tCK), 4) DDR4 - Max of following two equations: tAL + max (RoundUp(tRTP/tCK), 4) or, RL + BL/2 - tRP (*). mDDR - BL/2 LPDDR2 - Depends on if it is LPDDR2-S2 or LPDDR2-S4: LPDDR2-S2: BL/2 + RoundUp(tRTP/tCK) - 1. LPDDR2-S4: BL/2 + max(RoundUp(tRTP/tCK),2) - 2. LPDDR3 - BL/2 + max(RoundUp(tRTP/tCK),4) - 4 LPDDR4 - BL/2 + max(RoundUp(tRTP/tCK),8) - 8 (*) When both DDR4 SDRAM and ST-MRAM are used simultaneously, use SDRAM's tRP value for calculation. When the controller is operating in 1:2 mode, 1T mode, divide the previous value by 2. No rounding up. When the controller is operating in 1:2 mode, 2T mode, geardown mode or LPDDR4 mode, divide the previous value by 2 and round it up to the next integer value. For DDR4, using RTP instead of tRTP to calculate the value of this parameter. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
7	RW	0x0	Reserved0 Reserved Field:Yes
6:0	RW	0x14	t_rc tRC - Specifies the minimum time between activates to same bank. When the controller is operating in 1:2 frequency ratio mode, program this to (tRC/2) and round up to next integer value. Unit: DFI clock cycles. Value After Reset:0x14 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMTMG2

Address: Operational Base(0xFF4E0000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved3 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
29:24	RW	0x03	write_latency Set this field to WL. Indicates the Time from write command to write data on SDRAM interface. This must be set to WL. For mDDR, it must be set to 1. Note that, depending on the PHY, if using RDIMM/LRDIMM, it might be necessary to adjust the value of WL to compensate for the extra cycle of latency through the RDIMM/LRDIMM. When the controller is operating in 1:2 frequency ratio mode, divide the value calculated using the previous equation by 2, and round it up to next integer. This register field is not required for DDR2 and DDR3, as the DFI read and write latencies defined in DFITMG0 and DFITMG1 are sufficient for those protocols For all protocols, in addition to programming this register field, it is necessary to program DFITMG0 and DFITMG1 to control the read and write latencies Unit: DFI clock cycles. Value After Reset:0x3 Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
23:22	RW	0x0	Reserved2 Reserved Field:Yes
21:16	RW	0x05	read_latency Set this field to RL. Indicates the time from read command to read data on SDRAM interface. This must be set to RL. Note that, depending on the PHY, if using RDIMM/LRDIMM, it might be necessary to adjust the value of RL to compensate for the extra cycle of latency through the RDIMM/LRDIMM. When the controller is operating in 1:2 frequency ratio mode, divide the value calculated using the previous equation by 2, and round it up to next integer. This register field is not required for DDR2 and DDR3, as the DFI read and write latencies defined in DFITMG0 and DFITMG1 are sufficient for those protocols For all protocols, in addition to programming this register field, it is necessary to program DFITMG0 and DFITMG1 to control the read and write latencies Unit: DFI clock cycles. Value After Reset:0x5 Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
15:14	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
13:8	RW	0x06	rd2wr Minimum time from read command to write command. This must include time for bus turnaround (both within ranks and between ranks) and all PHY and system requirements. After the PHY has completed training, the value programmed may need to be increased. Please see the relevant PHY databook for details of what should be included here. The following calculations are minimum values, and do not include the PHY/system requirements mentioned above: DDR2/3/mDDR: RL + BL/2 + 2 - WL DDR4: RL + BL/2 + 1 + WR_PREAMBLE - WL LPDDR2/LPDDR3: RL + BL/2 + RU(tDQSCKmax/tCK) + 1 - WL LPDDR4(DQ ODT is Disabled): RL + BL/2 + RU(tDQSCKmax/tCK) + WR_PREAMBLE + RD_POSTAMBLE - WL LPDDR4(DQ ODT is Enabled): RL + BL/2 + RU(tDQSCKmax/tCK) + RD_POSTAMBLE - ODTLon - RU(tODTon(min)/tCK) + 1 Where: WL: Write latency BL: Burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM RL: Read latency = CAS latency WR_PREAMBLE: 1 (1tCK write preamble), 2 (2tCK write preamble). This is unique to DDR4 and LPDDR4 RD_POSTAMBLE: 0.5 (0.5tCK read postamble), 1.5 (1.5tCK read postamble). This is unique to LPDDR4 For LPDDR2/LPDDR3/LPDDR4, if derating is enabled (DERATEEN.derate_enable=1), derated tDQSCKmax must be used. When the controller is operating in 1:2 frequency ratio mode, divide the value calculated using the previous equation by 2, and round it up to next integer. Note that, depending on the PHY, if using LRDIMM, it may be necessary to adjust the value of this parameter to compensate for the extra cycle of latency through the LRDIMM. Unit: DFI clock cycles. Value After Reset:0x6 Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
7:6	RW	0x0	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
5:0	RW	0x0d	wr2rd In DDR4, minimum time from write command to read command for same bank group. In other protoocls, minimum time from write command to read command. This must include time for bus turn-around and all PHY and system requirements. After the PHY has completed training, the value programmed may need to be increased. Please see the relevant PHY databook for details of what should be included here. The following calculations are minimum values, and do not include the PHY/system requirements mentioned above: DDR4: CWL + PL + BL/2 + tWTR_L LPDDR2/3/4: WL + BL/2 + tWTR + 1 Others: CWL + BL/2 + tWTR Where: CWL: CAS write latency WL: Write latency PL: Parity latency BL: Burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM tWTR_L: Internal write to read command delay for same bank group. This comes directly from the SDRAM specification tWTR: Internal write to read command delay. This comes directly from the SDRAM specification Add one extra cycle for LPDDR2/LPDDR3/LPDDR4 operation. WTR_L must be increased by one if DDR4 2tCK write preamble is used. When the controller is operating in 1:2 mode, divide the value calculated using the previous equation by 2, and round it up to next integer. If your configuration has RANKCTL1.wr2rd_dr, write to read bus turn-around between different physical ranks are controlled by RANKCTL1.wr2rd_dr. Unit: DFI clock cycles. Value After Reset:0xd Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_DRAMTMG3

Address: Operational Base(0xFF4E0000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved2 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
29:20	RW	0x005	t_mrw Indicates the time to wait after a mode register write or read (MRW or MRR). Present only in designs configured to support LPDDR2, LPDDR3 or LPDDR4. LPDDR2 typically requires value of 5. LPDDR3 typically requires value of 10. LPDDR4: Set this to the larger of tMRW and tMRWCKEL. For LPDDR2, this register is used for the time from a MRW/MRR to all other commands. When the controller is operating in 1:2 frequency ratio mode, program this to the previous values divided by 2 and round it up to the next integer value. For LDPDR3, this register is used for the time from a MRW/MRR to a MRW/MRR. Unit: DFI clock cycles. Value After Reset:0x5 Programming Mode:Quasi-dynamic Group 2, Group 4
19:18	RW	0x0	Reserved1 Reserved Field:Yes
17:12	RW	0x04	t_mrd tMRD- Indicates the number of cycles to wait after a mode register write or read. Depending on the connected SDRAM, tMRD represents: DDR2/mDDR: Time from MRS to any command DDR3/4: Time from MRS to MRS command LPDDR2: not used LPDDR3/4: Time from MRS to non-MRS command When the controller is operating in 1:2 frequency ratio mode, program this to (tMRD/2) and round it up to the next integer value. If C/A parity for DDR4 is used, set to tMRD_PAR(tMOD+PL) instead. If CAL mode is enabled (DFITMG1.dfi_t_cmd_lat > 0), tCAL (=DFITMG1.dfi_cmd_lat) must be added to the previous calculations. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 2, Group 4
11:10	RW	0x0	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
9:0	RW	0x00c	t_mod tMOD - Parameter used only in DDR3 and DDR4. Indicates the number of cycles between load mode command and following non-load mode command. If C/A parity for DDR4 is used, set to tMOD_PAR(tMOD+PL) instead. If CAL mode is enabled (DFITMG1.dfi_t_cmd_lat > 0), tCAL (=DFITMG1.dfi_cmd_lat) must be added to the previous calculations. Set to tMOD if controller is operating in 1:1 frequency ratio mode, or tMOD/2 (rounded up to next integer) if controller is operating in 1:2 frequency ratio mode. Note that if using RDIMM/LRDIMM, depending on the PHY, it may be necessary to adjust the value of this parameter to compensate for the extra cycle of latency applied to mode register writes by the RDIMM/LRDIMM chip. Also note that if using RDIMM or LRDIMM, the minimum value of this register is tMRD_L2 if controller is operating in 1:1 frequency ratio mode, or tMRD_L2/2 (rounded up to next integer) if controller is operating in 1:2 frequency ratio mode. Unit: DFI clock cycles. Value After Reset:0xc Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMTMG4

Address: Operational Base(0xFF4E0000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved3 Reserved Field:Yes
28:24	RW	0x05	t_rcd tRCD - tAL: Indicates the minimum time from activate to read or write command to same bank. When the controller is operating in 1:2 frequency ratio mode, program this to ((tRCD - tAL)/2) and round it up to the next integer value. Minimum value allowed for this register is 1, which implies minimum (tRCD - tAL) value to be 2 when the controller is operating in 1:2 frequency ratio mode. Unit: DFI clock cycles. Value After Reset:0x5 Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
23:20	RW	0x0	Reserved2 Reserved Field:Yes
19:16	RW	0x4	t_ccd DDR4: tCCD_L: This is the minimum time between two reads or two writes for same bank group. Others: tCCD: This is the minimum time between two reads or two writes. When the controller is operating in 1:2 frequency ratio mode, program this to (tCCD_L/2 or tCCD/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 2, Group 4
15:12	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
11:8	RW	0x4	t_rrd DDR4: tRRD_L: This is the minimum time between activates from bank "a" to bank "b" for same bank group. Others: tRRD: Minimum time between activates from bank "a" to bank "b" When the controller is operating in 1:2 frequency ratio mode, program this to (tRRD_L/2 or tRRD/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 2, Group 4
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4:0	RW	0x05	t_rp tRP: Indicates the minimum time from single-bank precharge to activate of same bank. When the controller is operating in 1:1 frequency ratio mode, t_rp must be set to RoundUp(tRP/tCK). When the controller is operating in 1:2 frequency ratio mode, t_rp must be set to RoundDown(RoundUp(tRP/tCK)/2) + 1. When the controller is operating in 1:2 frequency ratio mode in LPDDR4, t_rp must be set to RoundUp(RoundUp(tRP/tCK)/2). Unit: DFI clock cycles. Value After Reset:0x5 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMTMG5

Address: Operational Base(0xFF4E0000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved3 Reserved Field:Yes
27:24	RW	0x5	t_cksrx This is the time before self-refresh Exit that CK is maintained as a valid clock before issuing SRX. Specifies the clock stable time before SRX. Recommended settings: mDDR - 1 LPDDR2 - 2 LPDDR3 - 2 LPDDR4 - tCKCKEH DDR2 - 1 DDR3 - tCKSRX DDR4 - tCKSRX When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. Unit: DFI clock cycles. Value After Reset:0x5 Programming Mode:Quasi-dynamic Group 2, Group 4
23	RW	0x0	Reserved2 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
22:16	RW	0x05	t_cksre This is the time after self-refresh Down Entry that CK is maintained as a valid clock. Specifies the clock disable delay after SRE. Recommended settings: mDDR - 0 LPDDR2 - 2 LPDDR3 - 2 LPDDR4 - tCKELCK DDR2 - 1 DDR3 - Max (10 ns, 5 tCK) DDR4(No RDIMM) - Max (10 ns, 5 tCK) (+ PL(parity latency)(*)) DDR4(RDIMM) - Max (Max (10 ns, 5 tCK) (+ PL(parity latency)(*)), tCKOff) (*)Only if CRCPARCTL1.caparity_disable_before_sr=0, this register must be increased by PL. When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. Unit: DFI clock cycles. Value After Reset:0x5 Programming Mode:Quasi-dynamic Group 2, Group 4
15:14	RW	0x0	Reserved1 Reserved Field:Yes
13:8	RW	0x04	t_ckesr Indicates the minimum CKE low width for self-refresh or self-refresh power down entry to exit timing in memory clock cycles. Recommended settings: mDDR - tRFC LPDDR2 - tCKESR LPDDR3 - tCKESR LPDDR4 - max(tCKE, tSR) DDR2 - tCKE DDR3 - tCKE + 1 DDR4(No RDIMM) - tCKE + 1 (+ PL(parity latency)(*)) DDR4(RDIMM) - t_cksre + tCKEV (*)Only if CRCPARCTL1.caparity_disable_before_sr=0, this register must be increased by PL. When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 2, Group 4
7:5	RW	0x0	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
4:0	RW	0x03	t_cke Indicates the minimum number of cycles of CKE HIGH/LOW during power-down and self-refresh. LPDDR2/LPDDR3 mode - Set this to the larger of tCKE or tCKESR LPDDR4 mode - Set this to the larger of tCKE or tSR Non-LPDDR2/non-LPDDR3/non-LPDDR4 designs - Set this to tCKE value When the controller is operating in 1:2 frequency ratio mode, program this to (value described above)/2 and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x3 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMTMG6

Address: Operational Base(0xFF4E0000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved2 Reserved Field:Yes
27:24	RW	0x2	t_ckdpde This is the time after Deep Power Down Entry that CK is maintained as a valid clock. Specifies the clock disable delay after DPDE. Recommended settings: mDDR: 0 LPDDR2: 2 LPDDR3: 2 When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. This is only present for designs supporting mDDR or LPDDR2/LPDDR3 devices. Unit: DFI clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4
23:20	RW	0x0	Reserved1 Reserved Field:Yes
19:16	RW	0x2	t_ckdpdx This is the time before Deep Power Down Exit that CK is maintained as a valid clock before issuing DPDX. Specifies the clock stable time before DPDX. Recommended settings: mDDR - 1 LPDDR2 - 2 LPDDR3 - 2 When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. This is only present for designs supporting mDDR or LPDDR2 devices. Unit: DFI clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4
15:4	RW	0x000	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
3:0	RW	0x5	t_ckcsx This is the time before Clock Stop Exit that CK is maintained as a valid clock before issuing Clock Stop Exit. Specifies the clock stable time before next command after Clock Stop Exit. Recommended settings: mDDR - 1 LPDDR2 - tXP + 2 LPDDR3 - tXP + 2 LPDDR4 - tXP + 2 When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. This is only present for designs supporting mDDR or LPDDR2/LPDDR3/LPDDR4 devices. Unit: DFI clock cycles. Value After Reset:0x5 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMTMG7

Address: Operational Base(0xFF4E0000) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:12	RW	0x00000	Reserved1 Reserved Field:Yes
11:8	RW	0x2	t_ckpde This is the time after Power Down Entry that CK is maintained as a valid clock. Specifies the clock disable delay after PDE. Recommended settings: mDDR - 0 LPDDR2 - 2 LPDDR3 - 2 LPDDR4 - tCKELCK When using DDR2/3/4 SDRAM, this register must be set to the same value as DRAMTMG5.t_cksre. When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. This is only present for designs supporting mDDR or LPDDR2/LPDDR3/LPDDR4 devices. Unit: DFI clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4
7:4	RW	0x0	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
3:0	RW	0x2	t_ckpdx This is the time before Power Down Exit that CK is maintained as a valid clock before issuing PDX. Specifies the clock stable time before PDX. Recommended settings: mDDR - 0 LPDDR2 - 2 LPDDR3 - 2 LPDDR4 - tCKCKEH When using DDR2/3/4 SDRAM, this register must be set to the same value as DRAMTMG5.t_cksrx. When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. This is only present for designs supporting mDDR or LPDDR2/LPDDR3/LPDDR4 devices. Unit: DFI clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMTMG8

Address: Operational Base(0xFF4E0000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved3 Reserved Field:Yes
30:24	RW	0x03	t_xs_fast_x32 tXS_FAST: Exit self-refresh to ZQCL, ZQCS and MRS (only CL, WR, RTP and Geardown mode). When the controller is operating in 1:2 frequency ratio mode, program this to the previous value divided by 2 and round up to next integer value. Note: This is applicable to only ZQCL/ZQCS commands. Note: Ensure this is less than or equal to t_xs_x32. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x3 Programming Mode:Quasi-dynamic Group 2, Group 4
23	RW	0x0	Reserved2 Reserved Field:Yes
22:16	RW	0x03	t_xs_abort_x32 tXS_ABORT: Exit self-refresh to commands not requiring a locked DLL in self-refresh Abort. When the controller is operating in 1:2 frequency ratio mode, program this to the previous value divided by 2 and round up to next integer value. Note: Ensure this is less than or equal to t_xs_x32. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x3 Programming Mode:Quasi-dynamic Group 2, Group 4
15	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
14:8	RW	0x44	t_xs_dll_x32 tXSDLL: Exit self-refresh to commands requiring a locked DLL. When the controller is operating in 1:2 frequency ratio mode, program this to the previous value divided by 2 and round up to next integer value. Note: Used only for DDR2, DDR3 and DDR4 SDRAMs. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x44 Programming Mode:Quasi-dynamic Group 2, Group 4
7	RW	0x0	Reserved0 Reserved Field:Yes
6:0	RW	0x05	t_xs_x32 tXS: Exit self-refresh to commands not requiring a locked DLL. When the controller is operating in 1:2 frequency ratio mode, program this to the previous value divided by 2 and round up to next integer value. Note: Used only for DDR2, DDR3 and DDR4 SDRAMs. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x5 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMTMG9

Address: Operational Base(0xFF4E0000) + offset (0x0124)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved3 Reserved Field:Yes
30	RW	0x0	ddr4_wr_preamble DDR4 Write preamble mode. 0 - 1tCK preamble 1 - 2tCK preamble Present only with MEMC_FREQ_RATIO=2. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4
29:19	RW	0x000	Reserved2 Reserved Field:Yes
18:16	RW	0x4	t_ccd_s tCCD_S: This is the minimum time between two reads or two writes for different bank group. When the controller is operating in 1:2 frequency ratio mode, program this to (tCCD_S/2) and round it up to the next integer value. Present only in designs configured to support DDR4. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 2, Group 4
15:12	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
11:8	RW	0x4	t_rrd_s tRRD_S: This is the minimum time between activates for different bank group. When the controller is operating in 1:2 frequency ratio mode, program this to (tRRD_S/2) and round it up to the next integer value. Present only in designs configured to support DDR4. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 2, Group 4
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5:0	RW	0x0d	wr2rd_s Minimum time from write command to read command for different bank group. This must include time for bus turn-around and all PHY and system requirements. After the PHY has completed training, the value programmed may need to be increased. Please see the relevant PHY databook for details of what should be included here. The following calculations are minimum values, and do not include the PHY/system requirements mentioned above: CWL + PL + BL/2 + tWTR_S Where: CWL: CAS write latency PL: Parity latency BL: Burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM tWTR_S: Internal write to read command delay for different bank group. This comes directly from the SDRAM specification WTR_S must be increased by one if DDR4 2tCK write preamble is used. When the controller is operating in 1:2 mode, divide the value calculated using the previous equation by 2, and round it up to next integer. If your configuration has RANKCTL1.wr2rd_dr, write to read bus turn-around between different physical ranks are controlled by RANKCTL1.wr2rd_dr. Unit: DFI clock cycles. Value After Reset:0xd Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_DRAMTMG10

Address: Operational Base(0xFF4E0000) + offset (0x0128)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved2 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
20:16	RW	0x1c	t_sync_gear Indicates the time between MRS command and the sync pulse time. This must be even number of clocks. For DDR4-2666 and DDR4-3200, this parameter is defined as tMOD(min)+4nCK tMOD(min) is greater of 24nCK or 15ns 15ns / .625ns = 24 Max value for this register is 24+4 = 28 When the controller is operating in 1:2 mode, program this to (tSYNC_GEAR/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x1c Programming Mode:Quasi-dynamic Group 2, Group 4
15:13	RW	0x0	Reserved1 Reserved Field:Yes
12:8	RW	0x18	t_cmd_gear Indicates a sync pulse to first valid command. For DDR4-2666 and DDR4-3200, this parameter is defined as tMOD(min) tMOD(min) is greater of 24nCK or 15ns 15ns / .625ns = 24 Max value for this register is 24 When the controller is operating in 1:2 mode, program this to (tCMD_GEAR/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x18 Programming Mode:Quasi-dynamic Group 2, Group 4
7:4	RW	0x0	Reserved0 Reserved Field:Yes
3:2	RW	0x2	t_gear_setup Indicates the geardown setup time. Minimum value of this register is 1. Zero is invalid. For DDR4-2666 and DDR4-3200, this parameter is defined as 2 clks When the controller is operating in 1:2 frequency ratio mode, program this to (tGEAR_setup/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4
1:0	RW	0x2	t_gear_hold Indicates the geardown hold time. Minimum value of this register is 1. Zero is invalid. For DDR4-2666 and DDR4-3200, this parameter is defined as 2 clks When the controller is operating in 1:2 frequency ratio mode, program this to (tGEAR_hold/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMTMG11

Address: Operational Base(0xFF4E0000) + offset (0x012C)

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Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved3 Reserved Field:Yes
30:24	RW	0x44	post_mpsm_gap_x32 tXMPDLL: This is the minimum Exit MPSM to commands requiring a locked DLL. When the controller is operating in 1:2 frequency ratio mode, program this to (tXMPDLL/2) and round it up to the next integer value. Present only in designs configured to support DDR4. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x44 Programming Mode:Quasi-dynamic Group 2, Group 4
23:21	RW	0x0	Reserved2 Reserved Field:Yes
20:16	RW	0x0c	t_mpx_lh tMPX_LH: This is the minimum CS_n Low hold time to CKE rising edge. When the controller is operating in 1:2 frequency ratio mode, program this to RoundUp(tMPX_LH/2)+1. Present only in designs configured to support DDR4. Unit: DFI clock cycles. Value After Reset:0xc Programming Mode:Quasi-dynamic Group 2, Group 4
15:10	RW	0x00	Reserved1 Reserved Field:Yes
9:8	RW	0x2	t_mpx_s tMPX_S: This is the minimum time CS setup time to CKE. When the controller is operating in 1:2 frequency ratio mode, program this to (tMPX_S/2) and round it up to the next integer value. Present only in designs configured to support DDR4. Unit: DFI clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4:0	RW	0x1c	t_ckmpe tCKMPE: This is the minimum valid clock requirement after MPSM entry. Present only in designs configured to support DDR4. When the controller is operating in 1:2 frequency ratio mode, divide the value calculated using the previous equation by 2, and round it up to next integer. Unit: DFI clock cycles. Value After Reset:0x1c Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMTMG12

Address: Operational Base(0xFF4E0000) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved2 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
29:24	RW	0x1a	t_wr_mpr This bit is used only in DDR4. Cycles between MPR Write and other command. Set this to tMOD + AL (or tMOD + PL + AL if C/A parity is also used). When the controller is operating in 1:2 frequency ratio mode, program this to (tWR_MPR/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x1a Programming Mode:Quasi-dynamic Group 2, Group 4
23:18	RW	0x00	Reserved1 Reserved Field:Yes
17:16	RW	0x2	t_cmdcke tCMDCKE: Indicates the delay from valid command to CKE input LOW. Set this to the larger of tESCKE or tCMDCKE When the controller is operating in 1:2 frequency ratio mode, program this to (max(tESCKE, tCMDCKE)/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4
15:5	RW	0x000	Reserved0 Reserved Field:Yes
4:0	RW	0x10	t_mrd_pda tMRD_PDA: This is the Mode Register Set command cycle time in PDA mode. When the controller is operating in 1:2 frequency ratio mode, program this to (tMRD_PDA/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x10 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMTMG13

Address: Operational Base(0xFF4E0000) + offset (0x0134)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved2 Reserved Field:Yes
30:24	RW	0x1c	odtloff LPDDR4: ODTLoff: This is the latency from CAS-2 command to ODToff reference. When the controller is operating in 1:2 frequency ratio mode, program this to (ODTLoff/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x1c Programming Mode:Quasi-dynamic Group 2, Group 4
23:22	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
21:16	RW	0x20	t_ccd_mw LPDDR4: tCCDMW: This is the minimum time from write or masked write to masked write command for same bank. When the controller is operating in 1:2 frequency ratio mode, program this to (tCCDMW/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x20 Programming Mode:Quasi-dynamic Group 2, Group 4
15:3	RW	0x0000	Reserved0 Reserved Field:Yes
2:0	RW	0x4	t_ppd LPDDR4: tPPD: This is the minimum time from precharge to precharge command. When the controller is operating in 1:2 frequency ratio mode, program this to (tPPD/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMTMG14

Address: Operational Base(0xFF4E0000) + offset (0x0138)

Bit	Attr	Reset Value	Description
31:12	RW	0x00000	Reserved0 Reserved Field:Yes
11:0	RW	0x0a0	t_xsr tXSR: This is the exit self-refresh to any command. When the controller is operating in 1:2 frequency ratio mode, program this to the previous value divided by 2 and round up to next integer value. The value 0xfff is illegal for this register field. Note: Used only for mDDR/LPDDR2/LPDDR3/LPDDR4 mode. Unit: DFI clock cycles. Value After Reset:0xa0 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DRAMTMG15

Address: Operational Base(0xFF4E0000) + offset (0x013C)

Bit	Attr	Reset Value	Description
31	RW	0x0	en_dfi_lp_t_stab 1 - Enable using tSTAB when exiting DFI LP. This must be set when the PHY is stopping the clock during DFI LP to save maximum power. 0 - Disable using tSTAB when exiting DFI LP. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4
30:8	RW	0x000000	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	t_stab_x32 tSTAB: Stabilization time. It is required in the following two cases for DDR3/DDR4 RDIMM: When exiting power saving mode, if the clock is stopped, after re-enabling it the clock must be stable for a time specified by tSTAB In the case of input clock frequency change (DDR4) After issuing control words that refers to clock timing (Specification: 6us for DDR3, 5us for DDR4) Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_ZQCTL0

Address: Operational Base(0xFF4E0000) + offset (0x0180)

Bit	Attr	Reset Value	Description
31	RW	0x0	dis_auto_zq 1 - Disable uMCTL2 generation of ZQCS/MPC(ZQ calibration) command. Register DBGCMD.zq_calib_short can be used instead to issue ZQ calibration request from APB module 0 - Internally generate ZQCS/MPC(ZQ calibration) commands based on ZQCTL1.t_zq_short_interval_x1024 This is only present for designs supporting DDR3/DDR4 or LPDDR2/LPDDR3/LPDDR4 devices. Value After Reset:0x0 Programming Mode:Dynamic
30	RW	0x0	dis_srx_zqcl 1 - Disable issuing of ZQCL/MPC(ZQ calibration) command at self-refresh/SR-Powerdown exit. Only applicable when run in DDR3 or DDR4 or LPDDR2 or LPDDR3 or LPDDR4 mode 0 - Enable issuing of ZQCL/MPC(ZQ calibration) command at self-refresh/SR-Powerdown exit. Only applicable when run in DDR3 or DDR4 or LPDDR2 or LPDDR3 or LPDDR4 mode This is only present for designs supporting DDR3/DDR4 or LPDDR2/LPDDR3/LPDDR4 devices. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4
29	RW	0x0	zq_resistor_shared 1 - Denotes that ZQ resistor is shared between ranks. Means ZQinit/ZQCL/ZQCS/MPC(ZQ calibration) commands are sent to one rank at a time with tZQinit/tZQCL/tZQCS/tZQCAL/tZQLAT timing met between commands so that commands to different ranks do not overlap 0 - ZQ resistor is not shared This is only present for designs supporting DDR3/DDR4 or LPDDR2/LPDDR3/LPDDR4 devices. Value After Reset:0x0 Programming Mode:Static

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Bit	Attr	Reset Value	Description
28	RW	0x0	dis_mpsmx_zqcl 1 - Disable issuing of ZQCL command at Maximum Power Saving Mode exit. Only applicable when run in DDR4 mode 0 - Enable issuing of ZQCL command at Maximum Power Saving Mode exit. Only applicable when run in DDR4 mode This is only present for designs supporting DDR4 devices. Note: Do not issue ZQCL command at Maximum Power Save Mode exit if the UMCTL2_SHARED_AC configuration parameter is set. Program it to 1'b1. The software can send ZQCS after exiting MPSM mode. Value After Reset:0x0 Programming Mode:Static
27	RW	0x0	Reserved1 Reserved Field:Yes
26:16	RW	0x200	t_zq_long_nop tZQoper for DDR3/DDR4, tZQCL for LPDDR2/LPDDR3, tZQCAL for LPDDR4: Number of DFI clock cycles of NOP required after a ZQCL (ZQ calibration long)/MPC(ZQ Start) command is issued to SDRAM. When the controller is operating in 1:2 frequency ratio mode: DDR3/DDR4: program this to tZQoper/2 and round it up to the next integer value. LPDDR2/LPDDR3: program this to tZQCL/2 and round it up to the next integer value. LPDDR4: program this to tZQCAL/2 and round it up to the next integer value. This is only present for designs supporting DDR3/DDR4 or LPDDR2/LPDDR3/LPDDR4 devices. Unit: DFI clock cycles. Value After Reset:0x200 Programming Mode:Static
15:10	RW	0x00	Reserved0 Reserved Field:Yes
9:0	RW	0x040	t_zq_short_nop tZQCS for DDR3/DD4/LPDDR2/LPDDR3, tZQLAT for LPDDR4: Number of DFI clock cycles of NOP required after a ZQCS (ZQ calibration short)/MPC(ZQ Latch) command is issued to SDRAM. When the controller is operating in 1:2 frequency ratio mode, program this to tZQCS/2 and round it up to the next integer value. This is only present for designs supporting DDR3/DDR4 or LPDDR2/LPDDR3/LPDDR4 devices. Unit: DFI clock cycles. Value After Reset:0x40 Programming Mode:Static

DDRCTL_ZQCTL1

Address: Operational Base(0xFF4E0000) + offset (0x0184)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
29:20	RW	0x020	t_zq_reset_nop tZQReset: Number of DFI clock cycles of NOP required after a ZQReset (ZQ calibration Reset) command is issued to SDRAM. When the controller is operating in 1:2 frequency ratio mode, program this to tZQReset/2 and round it up to the next integer value. This is only present for designs supporting LPDDR2/LPDDR3/LPDDR4 devices. Unit: DFI clock cycles. Value After Reset:0x20 Programming Mode:Static
19:0	RW	0x00100	t_zq_short_interval_x1024 Indicates the average interval to wait between automatically issuing ZQCS (ZQ calibration short)/MPC(ZQ calibration) commands to DDR3/DDR4/LPDDR2/LPDDR3/LPDDR4 devices. Meaningless, if ZQCTL0.dis_auto_zq=1. This is only present for designs supporting DDR3/DDR4 or LPDDR2/LPDDR3/LPDDR4 devices. Unit: Multiples of 1024 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x100 Programming Mode:Static

DDRCTL_ZQCTL2

Address: Operational Base(0xFF4E0000) + offset (0x0188)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RW	0x0	zq_reset Setting this register bit to 1 triggers a ZQ Reset operation. When the ZQ Reset operation is complete, the uMCTL2 automatically clears this bit. It is recommended NOT to set this register bit if in Init, in self-refresh(except LPDDR4) or SR-Powerdown(LPDDR4) or Deep power-down operating modes. For self-refresh(except LPDDR4) or SR-Powerdown(LPDDR4) it is scheduled after SR(except LPDDR4) or SPRD(LPDDR4) has been exited. For Deep power down, it is not scheduled, although ZQSTAT.zq_reset_busy is de-asserted. This is only present for designs supporting LPDDR2/LPDDR3/LPDDR4 devices. Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic

DDRCTL_ZQSTAT

Address: Operational Base(0xFF4E0000) + offset (0x018C)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
0	RO	0x0	zq_reset_busy SoC might initiate a ZQ Reset operation only if this signal is low. This signal goes high in the clock after the uMCTL2 accepts the ZQ Reset request. It goes low when the ZQ Reset command is issued to the SDRAM and the associated NOP period is over. It is recommended not to perform ZQ Reset commands when this signal is high. 0 - Indicates that the SoC can initiate a ZQ Reset operation 1 - Indicates that ZQ Reset operation is in progress Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_DFITMG0

Address: Operational Base(0xFF4E0000) + offset (0x0190)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved2 Reserved Field:Yes
28:24	RW	0x07	dfi_t_ctrl_delay Specifies the number of DFI clock cycles after an assertion or de-assertion of the DFI control signals that the control signals at the PHY-DRAM interface reflect the assertion or de-assertion. If the DFI clock and the memory clock are not phase-aligned, this timing parameter must be rounded up to the next integer value. Note that if using RDIMM/LRDIMM, it is necessary to increment this parameter by RDIMM's/LRDIMM's extra cycle of latency in terms of DFI clock. Unit: DFI clock cycles. Value After Reset:0x7 Programming Mode:Quasi-dynamic Group 4
23	RW	0x0	dfi_rddata_use_dfi_phy_clk Defines whether dfi_rddata_en/dfi_rddata/dfi_rddata_valid is generated using HDR (DFI clock) or SDR (DFI PHY clock) values. Selects whether value in DFITMG0.dfi_t_rddata_en is in terms of HDR (DFI clock) or SDR (DFI PHY clock) cycles: 0 in terms of HDR (DFI clock) cycles 1 in terms of SDR (DFI PHY clock) cycles Refer to PHY specification for correct value. If using a Synopsys DWC DDR3/2 PHY, DWC DDR2/3-Lite/mDDR PHY, DWC DDR multiPHY or DWC Gen2 DDR multiPHY, this field must be set to 0; otherwise: If MEMC_PROG_FREQ_RATIO=1 and MSTR.frequency_ratio=1, this field must be set to 0 Else, it must be set to 1 Value After Reset:0x0 Programming Mode:Static

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Bit	Attr	Reset Value	Description
22:16	RW	0x02	dfi_t_rddata_en Time from the assertion of a read command on the DFI interface to the assertion of the dfi_rddata_en signal. Refer to PHY specification for correct value. This corresponds to the DFI parameter trddata_en. Note that, depending on the PHY, if using RDIMM/LRDIMM, it may be necessary to use the adjusted value of CL in the calculation of trddata_en. This is to compensate for the extra cycles of latency through the RDIMM/LRDIMM. Unit: DFI clock cycles or DFI PHY clock cycles, depending on DFITMG0.dfi_rddata_use_dfi_phy_clk. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 1, Group 4
15	RW	0x0	dfi_wrdata_use_dfi_phy_clk Defines whether dfi_wrdata_en/dfi_wrdata/dfi_wrdata_mask is generated using HDR (DFI clock) or SDR (DFI PHY clock) values. Selects whether value in DFITMG0.dfi_tphy_wrlat is in terms of HDR (DFI clock) or SDR (DFI PHY clock) cycles. Selects whether value in DFITMG0.dfi_tphy_wrdata is in terms of HDR (DFI clock) or SDR (DFI PHY clock) cycles. 0 in terms of HDR (DFI clock) cycles 1 in terms of SDR (DFI PHY clock) cycles Refer to PHY specification for correct value. If using a Synopsys DWC DDR3/2 PHY, DWC DDR2/3-Lite/mDDR PHY, DWC DDR multiPHY or DWC Gen2 DDR multiPHY, this field must be set to 0; otherwise: If MEMC_PROG_FREQ_RATIO=1 and MSTR.frequency_ratio=1, this field must be set to 0 Else, it must be set to 1 Value After Reset:0x0 Programming Mode:Static
14	RW	0x0	Reserved1 Reserved Field:Yes
13:8	RW	0x00	dfi_tphy_wrdata Specifies the number of clock cycles between when dfi_wrdata_en is asserted to when the associated write data is driven on the dfi_wrdata signal. This corresponds to the DFI timing parameter tphy_wrdata. For more information on correct value, see PHY specification. Note, maximum supported value is 8. Unit: DFI clock cycles or DFI PHY clock cycles, depending on DFITMG0.dfi_wrdata_use_dfi_phy_clk. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 4
7:6	RW	0x0	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
5:0	RW	0x02	dfi_tphy_wrlat Write latency. Number of clocks from the write command to write data enable (dfi_wrdata_en). This corresponds to the DFI timing parameter tphy_wrlat. Refer to PHY specification for correct value. Note that, depending on the PHY, if using RDIMM/LRDIMM, it may be necessary to use the adjusted value of CL in the calculation of tphy_wrlat. This is to compensate for the extra cycles of latency through the RDIMM/LRDIMM. For LPDDR4, dfi_tphy_wrlat>60 is not supported. Unit: DFI clock cycles or DFI PHY clock cycles, depending on DFITMG0.dfi_wrdata_use_dfi_phy_clk. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DFITMG1

Address: Operational Base(0xFF4E0000) + offset (0x0194)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	dfi_t_cmd_lat Specifies the number of DFI PHY clock cycles between when the dfi_cs signal is asserted and when the associated command is driven. This field is used for CAL mode, must be set to '0' or tCAL, which matches the CAL mode register setting in the DRAM. When enabling CAL mode with RDIMM/LRDIMM, this field must be set to tCAL-CLA (Command Latency Adder). For more information on CLA, see JEDEC DDR4 Register Specification. If the PHY can add the latency for CAL mode, this must be set to '0'. Valid Range: 0 to 8. Unit: DFI PHY clock cycles. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4
27:26	RW	0x0	Reserved3 Reserved Field:Yes
25:24	RW	0x0	dfi_t_parin_lat Specifies the number of DFI PHY clock cycles between when the dfi_cs signal is asserted and when the associated dfi_parity_in signal is driven. Unit: DFI PHY clock cycles. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 4
23:21	RW	0x0	Reserved2 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
20:16	RW	0x00	dfi_t_wrdata_delay Specifies the number of DFI clock cycles between when the dfi_wrdata_en signal is asserted and when the corresponding write data transfer is completed on the DRAM bus. This corresponds to the DFI timing parameter twrdata_delay. For more information on correct value, see PHY specification. For DFI 3.0 PHY, set to twrdata_delay, a new timing parameter introduced in DFI 3.0. For DFI 2.1 PHY, set to tphy_wrdata + (delay of DFI write data to the DRAM). Value to be programmed is in terms of DFI clocks, not PHY clocks. In FREQ_RATIO=2, divide PHY's value by 2 and round up to next integer. If using DFITMG0.dfi_wrdata_use_dfi_phy_clk=1, add 1 to the value. Unit: DFI clock cycles. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 4
15:13	RW	0x0	Reserved1 Reserved Field:Yes
12:8	RW	0x04	dfi_t_dram_clk_disable Specifies the number of DFI clock cycles from the assertion of the dfi_dram_clk_disable signal on the DFI until the clock to the DRAM memory devices, at the PHY-DRAM boundary, maintains a low value. If the DFI clock and the memory clock are not phase aligned, this timing parameter must be rounded up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 4
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4:0	RW	0x04	dfi_t_dram_clk_enable Specifies the number of DFI clock cycles from the de-assertion of the dfi_dram_clk_disable signal on the DFI until the first valid rising edge of the clock to the DRAM memory devices, at the PHY-DRAM boundary. If the DFI clock and the memory clock are not phase aligned, this timing parameter must be rounded up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 4

DDRCTL_DFILPCFG0

Address: Operational Base(0xFF4E0000) + offset (0x0198)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved3 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
28:24	RW	0x07	dfi_tlp_resp Indicates the setting in DFI clock cycles for DFI's tlp_resp time. Same value is used for both Power Down, self-refresh, Deep Power Down and Maximum Power Saving modes. For more information on recommended values, see PHY databook Unit: DFI clock cycles. Value After Reset:0x7 Programming Mode:Static
23:20	RW	0x0	dfi_lp_wakeup_dpd Indicates the value in DFI clock cycles to drive on dfi_lp_wakeup signal when Deep Power Down mode is entered. Determines the DFI's tlp_wakeup time: 0x0 - 16 cycles 0x1 - 32 cycles 0x2 - 64 cycles 0x3 - 128 cycles 0x4 - 256 cycles 0x5 - 512 cycles 0x6 - 1024 cycles 0x7 - 2048 cycles 0x8 - 4096 cycles 0x9 - 8192 cycles 0xA - 16384 cycles 0xB - 32768 cycles 0xC - 65536 cycles 0xD - 131072 cycles 0xE - 262144 cycles 0xF - Unlimited This is only present for designs supporting mDDR or LPDDR2/LPDDR3 devices. Unit: DFI clock cycles. Value After Reset:0x0 Programming Mode:Static
19:17	RW	0x0	Reserved2 Reserved Field:Yes
16	RW	0x0	dfi_lp_en_dpd Enables DFI Low Power interface handshaking during Deep Power Down Entry/Exit. 0 - Disabled 1 - Enabled This is only present for designs supporting mDDR or LPDDR2/LPDDR3 devices. Value After Reset:0x0 Programming Mode:Static

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Bit	Attr	Reset Value	Description
15:12	RW	0x0	dfi_lp_wakeup_sr Indicates the value in DFI clock cycles to drive on dfi_lp_wakeup signal when self-refresh mode is entered. Determines the DFI's tlp_wakeup time: 0x0 - 16 cycles 0x1 - 32 cycles 0x2 - 64 cycles 0x3 - 128 cycles 0x4 - 256 cycles 0x5 - 512 cycles 0x6 - 1024 cycles 0x7 - 2048 cycles 0x8 - 4096 cycles 0x9 - 8192 cycles 0xA - 16384 cycles 0xB - 32768 cycles 0xC - 65536 cycles 0xD - 131072 cycles 0xE - 262144 cycles 0xF - Unlimited Unit: DFI clock cycles. Value After Reset:0x0 Programming Mode:Static
11:9	RW	0x0	Reserved1 Reserved Field:Yes
8	RW	0x0	dfi_lp_en_sr Enables DFI Low Power interface handshaking during self-refresh Entry/Exit. 0 - Disabled 1 - Enabled Value After Reset:0x0 Programming Mode:Static
7:4	RW	0x0	dfi_lp_wakeup_pd Indicates the value in DFI clock cycles to drive on dfi_lp_wakeup signal when Power Down mode is entered. Determines the DFI's tlp_wakeup time: 0x0 - 16 cycles 0x1 - 32 cycles 0x2 - 64 cycles 0x3 - 128 cycles 0x4 - 256 cycles 0x5 - 512 cycles 0x6 - 1024 cycles 0x7 - 2048 cycles 0x8 - 4096 cycles 0x9 - 8192 cycles 0xA - 16384 cycles 0xB - 32768 cycles 0xC - 65536 cycles 0xD - 131072 cycles 0xE - 262144 cycles 0xF - Unlimited Unit: DFI clock cycles. Value After Reset:0x0 Programming Mode:Static

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Bit	Attr	Reset Value	Description
3:1	RW	0x0	Reserved0 Reserved Field:Yes
0	RW	0x0	dfi_lp_en_pd Enables DFI Low Power interface handshaking during Power Down Entry/Exit. 0 - Disabled 1 - Enabled Value After Reset:0x0 Programming Mode:Static

DDRCTL_DFILPCFG1

Address: Operational Base(0xFF4E0000) + offset (0x019C)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved1 Reserved Field:Yes
7:4	RW	0x0	dfi_lp_wakeup_mpsm Indicates the value in DFI clock cycles to drive on dfi_lp_wakeup signal when Maximum Power Saving Mode is entered. Determines the DFI's tlp_wakeup time: 0x0 - 16 cycles 0x1 - 32 cycles 0x2 - 64 cycles 0x3 - 128 cycles 0x4 - 256 cycles 0x5 - 512 cycles 0x6 - 1024 cycles 0x7 - 2048 cycles 0x8 - 4096 cycles 0x9 - 8192 cycles 0xA - 16384 cycles 0xB - 32768 cycles 0xC - 65536 cycles 0xD - 131072 cycles 0xE - 262144 cycles 0xF - Unlimited This is only present for designs supporting DDR4 devices. Unit: DFI clock cycles. Value After Reset:0x0 Programming Mode:Static
3:1	RW	0x0	Reserved0 Reserved Field:Yes
0	RW	0x0	dfi_lp_en_mpsm Enables DFI Low Power interface handshaking during Maximum Power Saving Mode Entry/Exit. 0 - Disabled 1 - Enabled This is only present for designs supporting DDR4 devices. Value After Reset:0x0 Programming Mode:Static

DDRCTL_DFIUPD0

Address: Operational Base(0xFF4E0000) + offset (0x01A0)

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Bit	Attr	Reset Value	Description
31	RW	0x0	dis_auto_ctrlupd When '1', disable the automatic dfi_ctrlupd_req generation by the uMCTL2. The controller must issue the dfi_ctrlupd_req signal using register DBGCMD.ctrlupd. When '0', uMCTL2 issues dfi_ctrlupd_req periodically. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 3
30	RW	0x0	dis_auto_ctrlupd_srx When '1', disable the automatic dfi_ctrlupd_req generation by the uMCTL2 at self-refresh exit. When '0', uMCTL2 issues a dfi_ctrlupd_req before or after exiting self-refresh, depending on DFIUPD0.ctrlupd_pre_srx. Value After Reset:0x0 Programming Mode:Static
29	RW	0x0	ctrlupd_pre_srx Selects dfi_ctrlupd_req requirements at SRX: 0 - Send ctrlupd after SRX 1 - Send ctrlupd before SRX If DFIUPD0.dis_auto_ctrlupd_srx=1, this register has no impact, because no dfi_ctrlupd_req is issued when SRX. For SNPS DDR32 PHY, please keep the default value 0x0. Value After Reset:0x0 Programming Mode:Static
28:26	RW	0x0	Reserved1 Reserved Field:Yes
25:16	RW	0x040	dfi_t_ctrlup_max Specifies the maximum number of DFI clock cycles that the dfi_ctrlupd_req signal can assert. Lowest value to assign to this variable is 0x40. Unit: DFI clock cycles. Value After Reset:0x40 Programming Mode:Static
15:10	RW	0x00	Reserved0 Reserved Field:Yes
9:0	RW	0x003	dfi_t_ctrlup_min Specifies the minimum number of DFI clock cycles that the dfi_ctrlupd_req signal must be asserted. The uMCTL2 expects the PHY to respond within this time. If the PHY does not respond, the uMCTL2 de-asserts dfi_ctrlupd_req after dfi_t_ctrlup_min + 2 cycles. Lowest value to assign to this variable is 0x1. Unit: DFI clock cycles. Value After Reset:0x3 Programming Mode:Static

DDRCTL_DFIUPD1

Address: Operational Base(0xFF4E0000) + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
23:16	RW	0x01	dfi_t_ctrlupd_interval_min_x1024 This is the minimum amount of time between uMCTL2 initiated DFI update requests (which is executed whenever the uMCTL2 is idle). Set this number higher to reduce the frequency of update requests, which can have a small impact on the latency of the first read request when the uMCTL2 is idle. The minimum allowed value for this field is 1. Unit: Multiples of 1024 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x1 Programming Mode:Static
15:8	RW	0x00	Reserved0 Reserved Field:Yes
7:0	RW	0x01	dfi_t_ctrlupd_interval_max_x1024 This is the maximum amount of time between uMCTL2 initiated DFI update requests. This timer resets with each update request; when the timer expires dfi_ctrlupd_req is sent and traffic is blocked until the dfi_ctrlupd_ackx is received. PHY can use this idle time to recalibrate the delay lines to the DLLs. The DFI controller update is also used to reset PHY FIFO pointers in case of data capture errors. Updates are required to maintain calibration over PVT, but frequent updates may impact performance. Minimum allowed value for this field is 1. Note: Value programmed for DFIUPD1.dfi_t_ctrlupd_interval_max_x1024 must be greater than DFIUPD1.dfi_t_ctrlupd_interval_min_x1024. Unit: Multiples of 1024 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x1 Programming Mode:Static

DDRCTL_DFIUPD2

Address: Operational Base(0xFF4E0000) + offset (0x01A8)

Bit	Attr	Reset Value	Description
31	RW	0x1	dfi_phyupd_en Enables the support for acknowledging PHY-initiated updates: 0 - Disabled 1 - Enabled Value After Reset:0x1 Programming Mode:Static
30:0	RW	0x00000000	Reserved0 Reserved Field:Yes

DDRCTL_DFIMISC

Address: Operational Base(0xFF4E0000) + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:13	RW	0x00000	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
12:8	RW	0x00	dfi_frequency Indicates the operating frequency of the system. The number of supported frequencies and the mapping of signal values to clock frequencies are defined by the PHY. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 1
7	RW	0x0	lp_optimized_write If this bit is 1, LPDDR4 write DQ is set to 8'hF8 if masked write with enabling DBI; otherwise, that value is set to 8'hFF. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 3
6	RW	0x1	dis_dyn_adr_tri If this bit is 1, PHY specific Dynamic Tristating, which is a specific feature to certain Synopsys PHYs, is disabled. If this bit is 0, a special IDLE command is issued on the DFI while dfi_cs is inactive state so that the PHY can detect it to turn the command/address bus Hi-Z. This functionality works only in DFI 1:2 frequency ratio mode regardless of MSTR.en_2t_timing_mode, so if either of the following condition is met no special IDLE command is issued on the DFI bus: MEMC_FREQ_RATIO==1 MEMC_PROG_FREQ_RATIO=1 and MSTR.frequency_ratio=1 The special IDLE command means the following codes with the case where all the dfi_cs is 1: (phase 0 and 1) dfi_ras_n=1 (phase 0 and 1) dfi_cas_n= 1 phase 0 and 1) dfi_we_n= 1 (phase 0 and 1) dfi_bank [0]= 0 (phase 0 and 1) dfi_act_n= 1 Note: If CAL mode is enabled this register field must be set to 1 (They are mutually exclusive). Value After Reset:0x1 Programming Mode:Quasi-dynamic Group 3
5	RW	0x0	dfi_init_start PHY init start request signal.When asserted it triggers the PHY init start request. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 3
4	RW	0x0	ctl_idle_en Enables support of ctl_idle signal, which is non-DFI related pin specific to certain Synopsys PHYs. For more information on ctl_idle functionality, see signal description of ctl_idle signal. Value After Reset:0x0 Programming Mode:Static
3	RW	0x0	Reserved0 Reserved Field:Yes
2	RW	0x0	dfi_data_cs_polarity Defines polarity of dfi_wrdata_cs and dfi_rddata_cs signals. 0 - Signals are active low 1 - Signals are active high Value After Reset:0x0 Programming Mode:Static

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Bit	Attr	Reset Value	Description
1	RW	0x0	phy_dbi_mode DBI implemented in DDRC or PHY. 0 - DDRC implements DBI functionality 1 - PHY implements DBI functionality Present only in designs configured to support DDR4 and LPDDR4. Value After Reset:0x0 Programming Mode:Static
0	RW	0x1	dfi_init_complete_en PHY initialization complete enable signal. When asserted the dfi_init_complete signal can be used to trigger SDRAM initialisation Value After Reset:0x1 Programming Mode:Quasi-dynamic Group 3

DDRCTL_DFITMG2

Address: Operational Base(0xFF4E0000) + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:15	RW	0x00000	Reserved1 Reserved Field:Yes
14:8	RW	0x02	dfi_tphy_rdcslat specifies the number of DFI PHY clock cycles between when a read command is sent on the DFI control interface and when the associated dfi_rddata_cs signal is asserted. This corresponds to the DFI timing parameter tphy_rdcslat. Refer to PHY specification for correct value. Unit: DFI PHY clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5:0	RW	0x02	dfi_tphy_wrcslat Specifies the number of DFI PHY clock cycles between when a write command is sent on the DFI control interface and when the associated dfi_wrdata_cs signal is asserted. This corresponds to the DFI timing parameter tphy_wrcslat. For more information on correct value, see PHY specification. Unit: DFI PHY clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_DFITMG3

Address: Operational Base(0xFF4E0000) + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:5	RW	0x0000000	Reserved0 Reserved Field:Yes
4:0	RW	0x00	dfi_t_geardown_delay The delay from dfi_geardown_en assertion to the time of the PHY being ready to receive commands. Refer to PHY specification for correct value. When the controller is operating in 1:2 frequency ratio mode, program this to (tgeardown_delay/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x0 Programming Mode:Static

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DDRCTL_DFISTAT

Address: Operational Base(0xFF4E0000) + offset (0x01BC)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Reserved0 Reserved Field:Yes
1	RO	0x0	dfi_lp_ack Stores the value of the dfi_lp_ack input to the controller. Value After Reset:0x0 Programming Mode:Dynamic
0	RO	0x0	dfi_init_complete This a status flag register which announces when the DFI initialization has been completed. The DFI INIT triggered by dfi_init_start signal and then the dfi_init_complete flag is polled to know when the initialization is done. Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_DBICTL

Address: Operational Base(0xFF4E0000) + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	Reserved0 Reserved Field:Yes
2	RW	0x0	rd_dbi_en Read DBI enable signal in DDRC. 0 - Read DBI is disabled 1 - Read DBI is enabled This signal must be set the same value as DRAM's mode register. DDR4 - MR5 bit A12. When x4 devices are used, this signal must be set to 0 LPDDR4 - MR3[6] Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 1
1	RW	0x0	wr_dbi_en Write DBI enable signal in DDRC. 0 - Write DBI is disabled 1 - Write DBI is enabled This signal must be set the same value as DRAM's mode register. DDR4 - MR5 bit A11. When x4 devices are used, this signal must be set to 0 LPDDR4 - MR3[7] Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 1
0	RW	0x1	dm_en Indicates the DM enable signal in DDRC. 0 - DM is disabled 1 - DM is enabled This signal must be set the same logical value as DRAM's mode register. DDR4 - Set this to same value as MR5 bit A10. When x4 devices are used, this signal must be set to 0 LPDDR4 - Set this to inverted value of MR13[5] which is opposite polarity from this signal Value After Reset:0x1 Programming Mode:Static

DDRCTL_DFIPHYMSTR

Address: Operational Base(0xFF4E0000) + offset (0x01C4)

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Bit	Attr	Reset Value	Description
31:24	RW	0x80	dfi_phymstr_blk_ref_x32 The programmed value x32 is the maximum number of DFI clock cycles that allows to send pending refreshes before starting self-refresh entry process. - 0x00 - 0 DFI clock cycles, no delay - 0x01 - 32 DFI clock cycles - ... - 0xFF - 8160 DFI clock cycles Unit: Multiples of 32 DFI clock cycles. Note: Use as default value (0x80) unless Synopsys suggest to change value. Value After Reset:0x80 Programming Mode:Static
23:1	RW	0x000000	Reserved0 Reserved Field:Yes
0	RW	0x1	dfi_phymstr_en Enables the PHY Master Interface: 0 - Disabled 1 - Enabled Value After Reset:0x1 Programming Mode:Static

DDRCTL_ADDRMAP0

Address: Operational Base(0xFF4E0000) + offset (0x0200)

Bit	Attr	Reset Value	Description
31:5	RW	0x0000000	Reserved0 Reserved Field:Yes
4:0	RW	0x00	addrmap_cs_bit0 Selects the HIF address bit used as rank address bit 0. Valid Range: 0 to 29, and 31 Internal Base: 6 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then rank address bit 0 is set to 0. Value After Reset:0x0 Programming Mode:Static

DDRCTL_ADDRMAP1

Address: Operational Base(0xFF4E0000) + offset (0x0204)

Bit	Attr	Reset Value	Description
31:22	RW	0x000	Reserved2 Reserved Field:Yes
21:16	RW	0x00	addrmap_bank_b2 Selects the HIF address bit used as bank address bit 2. Valid Range: 0 to 31, and 63 Internal Base: 4 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank address bit 2 is set to 0. Value After Reset:0x0 Programming Mode:Static
15:14	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
13:8	RW	0x00	addrmap_bank_b1 Selects the HIF address bits used as bank address bit 1. Valid Range: 0 to 32, and 63 Internal Base: 3 The selected HIF address bit for each of the bank address bits is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank address bit 1 is set to 0. Value After Reset:0x0 Programming Mode:Static
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5:0	RW	0x00	addrmap_bank_b0 Selects the HIF address bits used as bank address bit 0. Valid Range: 0 to 32, and 63 Internal Base: 2 The selected HIF address bit for each of the bank address bits is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank address bit 0 is set to 0. Value After Reset:0x0 Programming Mode:Static

DDRCTL_ADDRMAP2

Address: Operational Base(0xFF4E0000) + offset (0x0208)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved3 Reserved Field:Yes
27:24	RW	0x0	addrmap_col_b5 Full bus width mode - Selects the HIF address bit used as column address bit 5 Half bus width mode - Selects the HIF address bit used as column address bit 6 Quarter bus width mode - Selects the HIF address bit used as column address bit 7 Valid Range: 0 to 7, and 15 Internal Base: 5 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then this column address bit is set to 0. Value After Reset:0x0 Programming Mode:Static
23:20	RW	0x0	Reserved2 Reserved Field:Yes
19:16	RW	0x0	addrmap_col_b4 Full bus width mode - Selects the HIF address bit used as column address bit 4 Half bus width mode - Selects the HIF address bit used as column address bit 5 Quarter bus width mode - Selects the HIF address bit used as column address bit 6 Valid Range: 0 to 7, and 15 Internal Base: 4 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then this column address bit is set to 0. Value After Reset:0x0 Programming Mode:Static

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Bit	Attr	Reset Value	Description
15:13	RW	0x0	Reserved1 Reserved Field:Yes
12:8	RW	0x00	addrmap_col_b3 Full bus width mode - Selects the HIF address bit used as column address bit 3 Half bus width mode - Selects the HIF address bit used as column address bit 4 Quarter bus width mode - Selects the HIF address bit used as column address bit 5 Valid Range: 0 to 7, x. x indicates a valid value in the inline ECC configuration. Internal Base: 3 The selected HIF address bit is determined by adding the internal base to the value of this field. Note, if UMCTL2_INCL_ARB=1, MEMC_BURST_LENGTH=16, Full bus width (MSTR.data_bus_width=00) and BL16 (MSTR.burst_rdwr=1000), it is recommended to program this to 0. In Inline ECC configuration (MEMC_INLINE_ECC=1) and Inline ECC mode is enabled (ECCCFG0.ecc_mode=4), if MEMC_BURST_LENGTH is 16, number of column address is 10 and work on half bus width mode, column bit 8, column bit 7 and column bit 3 must map to the highest 3 valid HIF address bits. This register need be set to x. (x = the highest valid HIF address bit - internal base - 2) Value After Reset:0x0 Programming Mode:Static
7:4	RW	0x0	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	addrmap_col_b2 Full bus width mode - Selects the HIF address bit used as column address bit 2 Half bus width mode - Selects the HIF address bit used as column address bit 3 Quarter bus width mode - Selects the HIF address bit used as column address bit 4 Valid Range: 0 to 7 Internal Base: 2 The selected HIF address bit is determined by adding the internal base to the value of this field. Note, if UMCTL2_INCL_ARB=1 and MEMC_BURST_LENGTH=8, it is required to program this to 0 unless: In Half or Quarter bus width (MSTR.data_bus_width!=00) and PCCFG.bl_exp_mode==1 and either In DDR4 and ADDRMAP8.addrmap_bg_b0==0 or In LPDDR4 and ADDRMAP1.addrmap_bank_b0==0 If UMCTL2_INCL_ARB=1 and MEMC_BURST_LENGTH=16, it is required to program this to 0 unless: In Half or Quarter bus width (MSTR.data_bus_width!=00) and PCCFG.bl_exp_mode==1 and In DDR4 and ADDRMAP8.addrmap_bg_b0==0 Otherwise, if MEMC_BURST_LENGTH=8 and Full Bus Width (MSTR.data_bus_width==00), it is recommended to program this to 0 so that HIF[2] maps to column address bit 2. If MEMC_BURST_LENGTH=16 and Full Bus Width (MSTR.data_bus_width==00), it is recommended to program this to 0 so that HIF[2] maps to column address bit 2. If MEMC_BURST_LENGTH=16 and Half Bus Width (MSTR.data_bus_width==01), it is recommended to program this to 0 so that HIF[2] maps to column address bit 3. Value After Reset:0x0 Programming Mode:Static

DDRCTL_ADDRMAP3

Address: Operational Base(0xFF4E0000) + offset (0x020C)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved3 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
28:24	RW	0x00	addrmap_col_b9 Full bus width mode - Selects the HIF address bit used as column address bit 9 Half bus width mode - Selects the HIF address bit used as column address bit 11 (10 in LPDDR2/LPDDR3 mode) Quarter bus width mode - Selects the HIF address bit used as column address bit 13 (11 in LPDDR2/LPDDR3 mode) Valid Range: 0 to 7, x, and 31. x indicates a valid value in the inline ECC configuration. Internal Base: 9 The selected HIF address bit is determined by adding the internal base to the value of this field. Note: Per JEDEC DDR2/3/mDDR specification, column address bit 10 is reserved for indicating auto-precharge, and hence no source address bit can be mapped to column address bit 10. In LPDDR2/LPDDR3, there is a dedicated bit for auto-precharge in the CA bus and hence column bit 10 is used. In Inline ECC configuration (MEMC_INLINE_ECC=1) and Inline ECC mode is enabled (ECCCFG0.ecc_mode=4), the highest 3 column address bits must map to the highest 3 valid HIF address bits. If column bit 9 is the highest column address bit, it must map to the highest valid HIF address bit. (x = the highest valid HIF address bit - internal base) If column bit 9 is the second highest column address bit, it must map to the second highest valid HIF address bit. (x = the highest valid HIF address bit - 1 - internal base) If column bit 9 is the third highest column address bit, it must map to the third highest valid HIF address bit. (x = the highest valid HIF address bit - 2 - internal base) If unused, set to 31 and then this column address bit is set to 0. Value After Reset:0x0 Programming Mode:Static
23:21	RW	0x0	Reserved2 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
20:16	RW	0x00	addrmap_col_b8 Full bus width mode - Selects the HIF address bit used as column address bit 8 Half bus width mode - Selects the HIF address bit used as column address bit 9 Quarter bus width mode - Selects the HIF address bit used as column address bit 11 (10 in LPDDR2/LPDDR3 mode) Valid Range: 0 to 7, x, and 31. x indicates a valid value in the inline ECC configuration. Internal Base: 8 The selected HIF address bit is determined by adding the internal base to the value of this field. Note: Per JEDEC DDR2/3/mDDR specification, column address bit 10 is reserved for indicating auto-precharge, and hence no source address bit can be mapped to column address bit 10. In LPDDR2/LPDDR3, there is a dedicated bit for auto-precharge in the CA bus and hence column bit 10 is used. In Inline ECC configuration (MEMC_INLINE_ECC=1) and Inline ECC mode is enabled (ECCCFG0.ecc_mode=4), the highest 3 column address bits must map to the highest 3 valid HIF address bits. If column bit 8 is the second highest column address bit, it must map to the second highest valid HIF address bit. (x = the highest valid HIF address bit - 1 - internal base) If column bit 8 is the third highest column address bit, it must map to the third highest valid HIF address bit. (x = the highest valid HIF address bit - 2 - internal base) If unused, set to 31 and then this column address bit is set to 0. Value After Reset:0x0 Programming Mode:Static
15:13	RW	0x0	Reserved1 Reserved Field:Yes
12:8	RW	0x00	addrmap_col_b7 Full bus width mode - Selects the HIF address bit used as column address bit 7 Half bus width mode - Selects the HIF address bit used as column address bit 8 Quarter bus width mode - Selects the HIF address bit used as column address bit 9 Valid Range: 0 to 7, x, and 31. x indicates a valid value in the inline ECC configuration. Internal Base: 7 The selected HIF address bit is determined by adding the internal base to the value of this field. In Inline ECC configuration (MEMC_INLINE_ECC=1) and Inline ECC mode is enabled (ECCCFG0.ecc_mode=4), the highest 3 column address bits must map to the highest 3 valid HIF address bits. If column bit 7 is the third highest column address bit, it must map to the third highest valid HIF address bit. (x = the highest valid HIF address bit - 2 - internal base) If unused, set to 31 and then this column address bit is set to 0. Value After Reset:0x0 Programming Mode:Static
7:5	RW	0x0	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
4:0	RW	0x00	addrmap_col_b6 Full bus width mode - Selects the HIF address bit used as column address bit 6. Half bus width mode - Selects the HIF address bit used as column address bit 7. Quarter bus width mode - Selects the HIF address bit used as column address bit 8. Valid Range: 0 to 7, x and 31. x indicates a valid value in the inline ECC configuration. Internal Base: 6 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then this column address bit is set to 0. In Inline ECC configuration (MEMC_INLINE_ECC=1) and Inline ECC mode is enabled (ECCCFG0.ecc_mode=4), if MEMC_BURST_LENGTH is 8, number of column address is 10 and work on half bus width mode, column bit 8, column bit 7 and column bit 6 must map to the highest 3 valid HIF address bits. This register need be set to x. (x = the highest valid HIF address bit - internal base - 2) Value After Reset:0x0 Programming Mode:Static

DDRCTL_ADDRMAP4

Address: Operational Base(0xFF4E0000) + offset (0x0210)

Bit	Attr	Reset Value	Description
31:13	RW	0x00000	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
12:8	RW	0x00	addrmap_col_b11 Full bus width mode - Selects the HIF address bit used as column address bit 13 (11 in LPDDR2/LPDDR3 mode) Half bus width mode - UNUSED. See later in this description for value you need to set to make it unused Quarter bus width mode - UNUSED. See later in this description for value you need to set to make it unused Valid Range: 0 to 7, x, and 31. x indicates a valid value in the inline ECC configuration. Internal Base: 11 The selected HIF address bit is determined by adding the internal base to the value of this field. Note: Per JEDEC DDR2/3/mDDR specification, column address bit 10 is reserved for indicating auto-precharge, and hence no source address bit can be mapped to column address bit 10. In LPDDR2/LPDDR3, there is a dedicated bit for auto-precharge in the CA bus and hence column bit 10 is used. In Inline ECC configuration (MEMC_INLINE_ECC=1) and Inline ECC mode is enabled (ECCCFG0.ecc_mode=4), the highest 3 column address bits must map to the highest 3 valid HIF address bits. If column bit 11 is the highest column address bit, it must map to the highest valid HIF address bit. (x = the highest valid HIF address bit - internal base) If column bit 11 is the second highest column address bit, it must map to the second highest valid HIF address bit. (x = the highest valid HIF address bit - 1 - internal base) If column bit 11 is the third highest column address bit, it must map to the third highest valid HIF address bit. (x = the highest valid HIF address bit - 2 - internal base) If unused, set to 31 and then this column address bit is set to 0. Value After Reset:0x0 Programming Mode:Static
7:5	RW	0x0	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
4:0	RW	0x00	addrmap_col_b10 Full bus width mode: Selects the HIF address bit used as column address bit 11 (10 in LPDDR2/LPDDR3 mode) Half bus width mode: Selects the HIF address bit used as column address bit 13 (11 in LPDDR2/LPDDR3 mode) Quarter bus width mode: UNUSED. See later in this description for value you need to set to make it unused Valid Range: 0 to 7, x, and 31. x indicates a valid value in the inline ECC configuration. Internal Base: 10 The selected HIF address bit is determined by adding the internal base to the value of this field. Note: Per JEDEC DDR2/3/mDDR specification, column address bit 10 is reserved for indicating auto-precharge, and hence no source address bit can be mapped to column address bit 10. In LPDDR2/LPDDR3, there is a dedicated bit for auto-precharge in the CA bus and hence column bit 10 is used. In Inline ECC configuration (MEMC_INLINE_ECC=1) and Inline ECC mode is enabled (ECCCFG0.ecc_mode=4), the highest 3 column address bits must map to the highest 3 valid HIF address bits. If column bit 10 is the highest column address bit, it must map to the highest valid HIF address bit. (x = the highest valid HIF address bit - internal base) If column bit 10 is the second highest column address bit, it must map to the second highest valid HIF address bit. (x = the highest valid HIF address bit - 1 - internal base) If column bit 10 is the third highest column address bit, it must map to the third highest valid HIF address bit. (x = the highest valid HIF address bit - 2 - internal base) If unused, set to 31 and then this column address bit is set to 0. Value After Reset:0x0 Programming Mode:Static

DDRCTL_ADDRMAP5

Address: Operational Base(0xFF4E0000) + offset (0x0214)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved3 Reserved Field:Yes
27:24	RW	0x0	addrmap_row_b11 Selects the HIF address bit used as row address bit 11. Valid Range: 0 to 11, and 15 Internal Base: 17 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then row address bit 11 is set to 0. Value After Reset:0x0 Programming Mode:Static
23:20	RW	0x0	Reserved2 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
19:16	RW	0x0	addrmap_row_b2_10 Selects the HIF address bits used as row address bits 2 to 10. Valid Range: 0 to 11, and 15 Internal Base: 8 (for row address bit 2), 9 (for row address bit 3), 10 (for row address bit 4) and so on, increasing to 16 (for row address bit 10) The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. When set to 15, the values of row address bits 2 to 10 are defined by registers ADDRMAP9, ADDRMAP10, ADDRMAP11. Value After Reset:0x0 Programming Mode:Static
15:12	RW	0x0	Reserved1 Reserved Field:Yes
11:8	RW	0x0	addrmap_row_b1 Selects the HIF address bits used as row address bit 1. Valid Range: 0 to 11 Internal Base: 7 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. Value After Reset:0x0 Programming Mode:Static
7:4	RW	0x0	Reserved0 Reserved Field:Yes
3:0	RW	0x0	addrmap_row_b0 Selects the HIF address bits used as row address bit 0. Valid Range: 0 to 11 Internal Base: 6 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. Value After Reset:0x0 Programming Mode:Static

DDRCTL_ADDRMAP6

Address: Operational Base(0xFF4E0000) + offset (0x0218)

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Bit	Attr	Reset Value	Description
31:29	RW	0x0	lpddr34_3gb_6gb_12gb Indicate what type of LPDDR3/LPDDR4 SDRAM device is in use. Here, the density size is per channel. When LPDDR3 device is used: 3'b100 - LPDDR3 SDRAM 6Gb/12Gb device in use. Every address having row[14:13]==2'b11 is considered as invalid 3'b000 - non-LPDDR3 6Gb/12Gb device in use. All addresses are valid Present only in designs configured to support LPDDR3. When LPDDR4 device is used: 3'b000: No LPDDR4 SDRAM 3Gb/6Gb/12Gb device in use. All addresses are valid. 3'b001: LPDDR4 SDRAM 3Gb device with x16 mode is in use. Every address having row[14:13]==2'b11 is considered as invalid. 3'b010: LPDDR4 SDRAM 6Gb device with x16 mode or 3Gb device with byte mode is in use. Every address having row[15:14]==2'b11 is considered as invalid. 3'b011: LPDDR4 SDRAM 12Gb device with x16 mode or 6Gb device with byte mode is in use. Every address having row[16:15]==2'b11 is considered as invalid. 3'b101: LPDDR4 SDRAM 12Gb device with byte mode is in use. Every address having row[17:16]==2'b11 is considered as invalid. Value After Reset:0x0 Programming Mode:Static
28	RW	0x0	Reserved3 Reserved Field:Yes
27:24	RW	0x0	addrmap_row_b15 Selects the HIF address bit used as row address bit 15. Valid Range: 0 to 11, and 15 Internal Base: 21 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then row address bit 15 is set to 0. Value After Reset:0x0 Programming Mode:Static
23:20	RW	0x0	Reserved2 Reserved Field:Yes
19:16	RW	0x0	addrmap_row_b14 Selects the HIF address bit used as row address bit 14. Valid Range: 0 to 11, and 15 Internal Base: 20 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then row address bit 14 is set to 0. Value After Reset:0x0 Programming Mode:Static
15:12	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
11:8	RW	0x0	addrmap_row_b13 Selects the HIF address bit used as row address bit 13. Valid Range: 0 to 11, and 15 Internal Base: 19 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then row address bit 13 is set to 0. Value After Reset:0x0 Programming Mode:Static
7:4	RW	0x0	Reserved0 Reserved Field:Yes
3:0	RW	0x0	addrmap_row_b12 Selects the HIF address bit used as row address bit 12. Valid Range: 0 to 11, and 15 Internal Base: 18 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then row address bit 12 is set to 0. Value After Reset:0x0 Programming Mode:Static

DDRCTL_ADDRMAP7

Address: Operational Base(0xFF4E0000) + offset (0x021C)

Bit	Attr	Reset Value	Description
31:12	RW	0x00000	Reserved1 Reserved Field:Yes
11:8	RW	0x0	addrmap_row_b17 Selects the HIF address bit used as row address bit 17. Valid Range: 0 to 11, and 15 Internal Base: 23 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then row address bit 17 is set to 0 for DDR4 or set to 1 for LPDDR4 backward compability. Value After Reset:0x0 Programming Mode:Static
7:4	RW	0x0	Reserved0 Reserved Field:Yes
3:0	RW	0x0	addrmap_row_b16 Selects the HIF address bit used as row address bit 16. Valid Range: 0 to 11, and 15 Internal Base: 22 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then row address bit 16 is set to 0. Value After Reset:0x0 Programming Mode:Static

DDRCTL_ADDRMAP8

Address: Operational Base(0xFF4E0000) + offset (0x0220)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
13:8	RW	0x00	addrmap_bg_b1 Selects the HIF address bits used as bank group address bit 1. Valid Range: 0 to 32, and 63 Internal Base: 3 The selected HIF address bit for each of the bank group address bits is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank group address bit 1 is set to 0. Value After Reset:0x0 Programming Mode:Static
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5:0	RW	0x00	addrmap_bg_b0 Selects the HIF address bits used as bank group address bit 0. Valid Range: 0 to 32, and 63 Internal Base: 2 The selected HIF address bit for each of the bank group address bits is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank group address bit 0 is set to 0. Value After Reset:0x0 Programming Mode:Static

DDRCTL_ADDRMAP9

Address: Operational Base(0xFF4E0000) + offset (0x0224)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved3 Reserved Field:Yes
27:24	RW	0x0	addrmap_row_b5 Selects the HIF address bits used as row address bit 5. Valid Range: 0 to 11 Internal Base: 11 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. This register field is used only when ADDRMAP5.addrmap_row_b2_10 is set to value 15. Value After Reset:0x0 Programming Mode:Static
23:20	RW	0x0	Reserved2 Reserved Field:Yes
19:16	RW	0x0	addrmap_row_b4 Selects the HIF address bits used as row address bit 4. Valid Range: 0 to 11 Internal Base: 10 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. This register field is used only when ADDRMAP5.addrmap_row_b2_10 is set to value 15. Value After Reset:0x0 Programming Mode:Static
15:12	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
11:8	RW	0x0	addrmap_row_b3 Selects the HIF address bits used as row address bit 3. Valid Range: 0 to 11 Internal Base: 9 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. This register field is used only when ADDRMAP5.addrmap_row_b2_10 is set to value 15. Value After Reset:0x0 Programming Mode:Static
7:4	RW	0x0	Reserved0 Reserved Field:Yes
3:0	RW	0x0	addrmap_row_b2 Selects the HIF address bits used as row address bit 2. Valid Range: 0 to 11 Internal Base: 8 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. This register field is used only when ADDRMAP5.addrmap_row_b2_10 is set to value 15. Value After Reset:0x0 Programming Mode:Static

DDRCTL_ADDRMAP10

Address: Operational Base(0xFF4E0000) + offset (0x0228)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved3 Reserved Field:Yes
27:24	RW	0x0	addrmap_row_b9 Selects the HIF address bits used as row address bit 9. Valid Range: 0 to 11 Internal Base: 15 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. This register field is used only when ADDRMAP5.addrmap_row_b2_10 is set to value 15. Value After Reset:0x0 Programming Mode:Static
23:20	RW	0x0	Reserved2 Reserved Field:Yes
19:16	RW	0x0	addrmap_row_b8 Selects the HIF address bits used as row address bit 8. Valid Range: 0 to 11 Internal Base: 14 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. This register field is used only when ADDRMAP5.addrmap_row_b2_10 is set to value 15. Value After Reset:0x0 Programming Mode:Static
15:12	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
11:8	RW	0x0	addrmap_row_b7 Selects the HIF address bits used as row address bit 7. Valid Range: 0 to 11 Internal Base: 13 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. This register field is used only when ADDRMAP5.addrmap_row_b2_10 is set to value 15. Value After Reset:0x0 Programming Mode:Static
7:4	RW	0x0	Reserved0 Reserved Field:Yes
3:0	RW	0x0	addrmap_row_b6 Selects the HIF address bits used as row address bit 6. Valid Range: 0 to 11 Internal Base: 12 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. This register field is used only when ADDRMAP5.addrmap_row_b2_10 is set to value 15. Value After Reset:0x0 Programming Mode:Static

DDRCTL_ADDRMAP11

Address: Operational Base(0xFF4E0000) + offset (0x022C)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	Reserved0 Reserved Field:Yes
3:0	RW	0x0	addrmap_row_b10 Selects the HIF address bits used as row address bit 10. Valid Range: 0 to 11 Internal Base: 16 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. This register field is used only when ADDRMAP5.addrmap_row_b2_10 is set to value 15. Value After Reset:0x0 Programming Mode:Static

DDRCTL_ODTCFG

Address: Operational Base(0xFF4E0000) + offset (0x0240)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved4 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
27:24	RW	0x4	wr_odt_hold DFI PHY clock cycles to hold ODT for a write command. The minimum supported value is 2. Recommended values: DDR2: BL8 - 0x5 (DDR2-400/533/667), 0x6 (DDR2-800), 0x7 (DDR2-1066) BL4 - 0x3 (DDR2-400/533/667), 0x4 (DDR2-800), 0x5 (DDR2-1066) DDR3: BL8 - 0x6 DDR4: BL8 - 5 + WR_PREAMBLE + CRC_MODE WR_PREAMBLE = 1 (1tCK write preamble), 2 (2tCK write preamble) CRC_MODE = 0 (not CRC mode), 1 (CRC mode) LPDDR3: BL8 - 7 + RU(tODTon(max)/tCK) Unit: DFI PHY clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 1, Group 4
23:21	RW	0x0	Reserved3 Reserved Field:Yes
20:16	RW	0x00	wr_odt_delay Indicates the delay, in DFI PHY clock cycles, from issuing a write command to setting ODT values associated with that command. ODT setting must remain constant for the entire time that DQS is driven by the uMCTL2. Recommended values: DDR2: CWL + AL - 3 (DDR2-400/533/667), CWL + AL - 4 (DDR2-800), CWL + AL - 5 (DDR2-1066) If (CWL + AL - 3 < 0), uMCTL2 does not support ODT for write operation. DDR3: 0x0 DDR4: DFITMG1.dfi_t_cmd_lat (to adjust for CAL mode) LPDDR3: WL - 1 - RU(tODTon(max)/tCK)) Unit: DFI PHY clock cycles. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 1, Group 4
15:12	RW	0x0	Reserved2 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
11:8	RW	0x4	rd_odt_hold DFI PHY clock cycles to hold ODT for a read command. The minimum supported value is 2. Recommended values: DDR2: BL8 - 0x6 (not DDR2-1066), 0x7 (DDR2-1066) BL4 - 0x4 (not DDR2-1066), 0x5 (DDR2-1066) DDR3: BL8 - 0x6 DDR4: BL8 - 5 + RD_PREAMBLE RD_PREAMBLE = 1 (1tCK read preamble), 2 (2tCK read preamble) LPDDR3: BL8 - 5 + RU(tDQSCK(max)/tCK) - RD(tDQSCK(min)/tCK) + RU(tODTon(max)/tCK) Unit: DFI PHY clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 1, Group 4
7	RW	0x0	Reserved1 Reserved Field:Yes
6:2	RW	0x00	rd_odt_delay Indicates the delay, in DFI PHY clock cycles, from issuing a read command to setting ODT values associated with that command. ODT setting must remain constant for the entire time that DQS is driven by the uMCTL2. Recommended values: DDR2: CL + AL - 4 (not DDR2-1066), CL + AL - 5 (DDR2-1066) If (CL + AL - 4 < 0), uMCTL2 does not support ODT for read operation. DDR3: CL - CWL DDR4: CL - CWL - RD_PREAMBLE + WR_PREAMBLE + DFITMG1.dfi_t_cmd_lat (to adjust for CAL mode) WR_PREAMBLE = 1 (1tCK write preamble), 2 (2tCK write preamble) LPDDR3: RL + RD(tDQSCK(min)/tCK) - 1 - RU(tODTon(max)/tCK) Unit: DFI PHY clock cycles. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 1, Group 4
1:0	RW	0x0	Reserved0 Reserved Field:Yes

DDRCTL_ODTMAP

Address: Operational Base(0xFF4E0000) + offset (0x0244)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	Reserved3 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
13:12	RW	0x2	rank1_rd_odt Indicates which remote ODTs must be turned on during a read from rank 1. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, and so on. For each rank, set its bit to 1 to enable its ODT. Present only in configurations that have 2 or more ranks. Value After Reset:0x2 Programming Mode:Static
11:10	RW	0x0	Reserved2 Reserved Field:Yes
9:8	RW	0x2	rank1_wr_odt Indicates which remote ODTs must be turned on during a write to rank 1. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, and so on. For each rank, set its bit to 1 to enable its ODT. Present only in configurations that have 2 or more ranks. Value After Reset:0x2 Programming Mode:Static
7:6	RW	0x0	Reserved1 Reserved Field:Yes
5:4	RW	0x1	rank0_rd_odt Indicates which remote ODTs must be turned on during a read from rank 0. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, and so on. For each rank, set its bit to 1 to enable its ODT. Value After Reset:0x1 Programming Mode:Static
3:2	RW	0x0	Reserved0 Reserved Field:Yes
1:0	RW	0x1	rank0_wr_odt Indicates which remote ODTs must be turned on during a write to rank 0. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, and so on. For each rank, set its bit to 1 to enable its ODT. Value After Reset:0x1 Programming Mode:Static

DDRCTL_SCHED

Address: Operational Base(0xFF4E0000) + offset (0x0250)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved2 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
30:24	RW	0x00	rdwr_idle_gap When the preferred transaction store is empty for these many clock cycles, switch to the alternate transaction store if it is non-empty. The read transaction store (both high and low priority) is the default preferred transaction store and the write transaction store is the alternative store. When prefer write over read is set this is reversed. 0x0 is a legal value for this register. When set to 0x0, the transaction store switching happens immediately when the switching conditions become true. FOR PERFORMANCE ONLY. Unit: DFI clock cycles. Value After Reset:0x0 Programming Mode:Static
23:16	RW	0x00	go2critical_hysteresis UNUSED. Value After Reset:0x0 Programming Mode:Static
15	RW	0x0	lpddr4_opt_act_timing Optimized ACT timing control for LPDDR4. In LPDDR4, RD/WR/ACT takes 4 cycle. To stream Read/Write, there are only 4 cycle space between Reads/Writes. If ACT is scheduled-out after RD/WR with 1, 2 or 3 cycle gap, next RD/WR may be pushed by 1, 2 or 3 cycle and create a gap on DQ. When this register is set, ACT is not scheduled-out with the gap = 1, 2 and 3 cycle. If enabled, there could be performance impact especially for random traffic. (Latency/Utilization) 1 - Enable this feature 0 - Disable this feature This register is ignored when MSTR.lpddr4==0. Value After Reset:0x0 Programming Mode:Static
14:3	RW	0x000	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
2	RW	0x1	pageclose If true, bank is kept open only while there are page hit transactions available in the CAM to that bank. The last read or write command in the CAM with a bank and page hit is executed with auto-precharge if SCHED1.pageclose_timer=0. Even if this register set to 1 and SCHED1.pageclose_timer is set to 0, explicit precharge (and not auto-precharge) may be issued in some cases where there is a mode switch between Write and Read or between LPR and HPR. The Read and Write commands that are executed as part of the ECC scrub requests are also executed without auto-precharge. If false, the bank remains open until there is a need to close it (to open a different page, or for page timeout or refresh timeout) - also known as open page policy. The open page policy can be overridden by setting the per-command-autopre bit on the HIF interface (hif_cmd_autopre). The pageclose feature provids a midway between Open and Close page policies. FOR PERFORMANCE ONLY. Value After Reset:0x1 Programming Mode:Quasi-dynamic Group 3
1:0	RW	0x0	Reserved0 Reserved Field:Yes

DDRCTL_SCHED1

Address: Operational Base(0xFF4E0000) + offset (0x0254)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved0 Reserved Field:Yes
7:0	RW	0x00	pageclose_timer This field works in conjunction with SCHED.pageclose.It only has meaning if SCHED.pageclose==1. If SCHED.pageclose==1 and pageclose_timer==0, then an auto-precharge may be scheduled for last read or write command in the CAM with a bank and page hit. Note, sometimes an explicit precharge is scheduled instead of the auto-precharge. For more information, see SCHED.pageclose. If SCHED.pageclose==1 and pageclose_timer>0, then an auto-precharge is not scheduled for last read or write command in the CAM with a bank and page hit. Instead, a timer is started, with pageclose_timer as the initial value. There is a timer on a per bank basis. The timer decrements unless the next read or write in the CAM to a bank is a page hit. It gets reset to pageclose_timer value if the next read or write in the CAM to a bank is a page hit. Once the timer has reached zero, an explcit precharge is attempted to be scheduled. Unit: DFI clock cycles. Value After Reset:0x0 Programming Mode:Static

DDRCTL_PERFLPR1

Address: Operational Base(0xFF4E0000) + offset (0x0264)

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Bit	Attr	Reset Value	Description
31:24	RW	0x0f	lpr_xact_run_length Indicates the number of transactions that are serviced once the LPR queue goes critical is the smaller of: (a) This number (b) Number of transactions available Unit: Transaction. FOR PERFORMANCE ONLY. Value After Reset:0xf Programming Mode:Quasi-dynamic Group 3
23:16	RW	0x00	Reserved0 Reserved Field:Yes
15:0	RW	0x007f	lpr_max_starve Indicates the number of DFI clocks that the LPR queue can be starved before it goes critical. The minimum valid functional value for this register is 0x1. Programming it to 0x0 disables the starvation functionality. During normal operation, this function must not be disabled as it causes excessive latencies. FOR PERFORMANCE ONLY. Unit: DFI clock cycles. Value After Reset:0x7f Programming Mode:Quasi-dynamic Group 3

DDRCTL_PERFWR1

Address: Operational Base(0xFF4E0000) + offset (0x026C)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	w_xact_run_length Indicates the number of transactions that are serviced once the WR queue goes critical is the smaller of: (a) This number (b) Number of transactions available Unit: Transaction. FOR PERFORMANCE ONLY. Value After Reset:0xf Programming Mode:Quasi-dynamic Group 3
23:16	RW	0x00	Reserved0 Reserved Field:Yes
15:0	RW	0x007f	w_max_starve Indicates the number of DFI clocks that the WR queue can be starved before it goes critical. The minimum valid functional value for this register is 0x1. Programming it to 0x0 disables the starvation functionality. During normal operation, this function must not be disabled as it causes excessive latencies. FOR PERFORMANCE ONLY. Unit: DFI clock cycles. Value After Reset:0x7f Programming Mode:Quasi-dynamic Group 3

DDRCTL_DBG0

Address: Operational Base(0xFF4E0000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved2 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
7	RW	0x0	dis_max_rank_wr_opt Indicates the disable optimized max_rank_wr and max_logical_rank_wr feature. This register is for debug purpose only. For normal operation, this register must be set to 0. Value After Reset:0x0 Programming Mode:Static
6	RW	0x0	dis_max_rank_rd_opt Indicates the disable optimized max_rank_rd and max_logical_rank_rd feature. This register is for debug purpose only. For normal operation, this register must be set to 0. Value After Reset:0x0 Programming Mode:Static
5	RW	0x0	Reserved1 Reserved Field:Yes
4	RW	0x0	dis_collision_page_opt When this is set to '0', auto-precharge is disabled for the flushed command in a collision case. Collision cases are write followed by read to same address, read followed by write to same address, or write followed by write to same address with DBG0.dis_wc bit = 1 (where same address comparisons exclude the two address bits representing critical word). FOR DEBUG ONLY. Value After Reset:0x0 Programming Mode:Static
3:0	RW	0x0	Reserved0 Reserved Field:Yes

DDRCTL_DBG1

Address: Operational Base(0xFF4E0000) + offset (0x0304)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	Reserved0 Reserved Field:Yes
1	RW	0x0	dis_hif When 1, uMCTL2 asserts the HIF command signal hif_cmd_stall. uMCTL2 ignores the hif_cmd_valid and all other associated request signals. This bit is intended to be switched on-the-fly. Value After Reset:0x0 Programming Mode:Dynamic

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Bit	Attr	Reset Value	Description
0	RW	0x0	dis_dq When 1, uMCTL2 does not de-queue any transactions from the CAM. Bypass is also disabled. All transactions are queued in the CAM. No reads or writes are issued to SDRAM as long as this is asserted. This bit may be used to prevent reads or writes being issued by the uMCTL2, which makes it safe to modify certain register fields associated with reads and writes (For more information, see Programming chapter). After setting this bit, it is strongly recommended to poll DBGCAM.wr_data_pipeline_empty and DBGCAM.rd_data_pipeline_empty, before making changes to any registers which affect reads and writes. This ensures that the relevant logic in the DDRC is idle. This bit is intended to be switched on-the-fly. Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_DBGCAM

Address: Operational Base(0xFF4E0000) + offset (0x0308)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved4 Reserved Field:Yes
29	RO	0x0	wr_data_pipeline_empty This bit indicates that the write data pipeline on the DFI interface is empty. This register is intended to be polled at least twice after setting DBG1.dis_dq, to ensure that all remaining commands/data have completed. Value After Reset:0x0 Programming Mode:Dynamic
28	RO	0x0	rd_data_pipeline_empty This bit indicates that the read data pipeline on the DFI interface is empty. This register is intended to be polled at least twice after setting DBG1.dis_dq, to ensure that all remaining commands/data have completed. Value After Reset:0x0 Programming Mode:Dynamic
27	RW	0x0	Reserved3 Reserved Field:Yes
26	RO	0x0	dbg_wr_q_empty When 1, all the Write command queues and Write data buffers inside DDRC are empty. This register is to be used for debug purpose. An example use-case scenario: When the controller enters self-refresh using the Low-Power entry sequence, controller is expected to have executed all the commands in its queues and the write and read data drained. Hence this register must be 1 at that time. FOR DEBUG ONLY Value After Reset:0x0 Programming Mode:Dynamic

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Bit	Attr	Reset Value	Description
25	RO	0x0	dbg_rd_q_empty When 1, all the Read command queues and Read data buffers inside DDRC are empty. This register is to be used for debug purpose. An example use-case scenario: When the controller enters self-refresh using the Low-Power entry sequence, controller is expected to have executed all the commands in its queues and the write and read data drained. Hence this register must be 1 at that time. FOR DEBUG ONLY Value After Reset:0x0 Programming Mode:Dynamic
24	RO	0x0	dbg_stall Stall. FOR DEBUG ONLY. Value After Reset:0x0 Programming Mode:Dynamic
23:22	RW	0x0	Reserved2 Reserved Field:Yes
21:16	RO	0x00	dbg_w_q_depth This field indicates the Write queue depth. The last entry of WR queue is reserved for ECC SCRUB operation. This entry is not included in the calculation of the queue depth. FOR DEBUG ONLY Value After Reset:0x0 Programming Mode:Dynamic
15:14	RW	0x0	Reserved1 Reserved Field:Yes
13:8	RO	0x00	dbg_lpr_q_depth This field indicates the low priority read queue depth. The last entry of Lpr queue is reserved for ECC SCRUB operation. This entry is not included in the calculation of the queue depth. FOR DEBUG ONLY Value After Reset:0x0 Programming Mode:Dynamic
7:0	RW	0x00	Reserved0 Reserved Field:Yes

DDRCTL_DBGCMD

Address: Operational Base(0xFF4E0000) + offset (0x030C)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	Reserved1 Reserved Field:Yes
5	RW	0x0	ctrlupd Setting this register bit to 1 indicates to the uMCTL2 to issue a dfi_ctrlupd_req to the PHY. When this request is stored in the uMCTL2, the bit is automatically cleared. This operation must only be performed when DFIUPD0.dis_auto_ctrlupd=1. Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic

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Bit	Attr	Reset Value	Description
4	RW	0x0	zq_calib_short Setting this register bit to 1 indicates to the uMCTL2 to issue a ZQCS (ZQ calibration short)/MPC(ZQ calibration) command to the SDRAM. When this request is stored in the uMCTL2, the bit is automatically cleared. This operation can be performed only when ZQCTL0.dis_auto_zq=1. It is recommended NOT to set this register bit if in Init, in self-refresh(except LPDDR4) or SR-Powerdown(LPDDR4) or Deep power-down operating modes or Maximum Power Saving Mode. For self-refresh(except LPDDR4) or SR-Powerdown(LPDDR4) it is scheduled after SR(except LPDDR4) or SPRD(LPDDR4) has been exited. For Deep power down and Maximum Power Saving Mode, it is not scheduled, although DBGSTAT.zq_calib_short_busy is de-asserted. Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic
3:2	RW	0x0	Reserved0 Reserved Field:Yes
1	RW	0x0	rank1_refresh Setting this register bit to 1 indicates to the uMCTL2 to issue a refresh to rank 1. Writing to this bit causes DBGSTAT.rank1_refresh_busy to be set. When DBGSTAT.rank1_refresh_busy is cleared, the command has been stored in uMCTL2. For 3DS configuration, refresh is sent to rank index 1. This operation can be performed only when RFSHCTL3.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Deep power-down operating modes or Maximum Power Saving Mode. Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic
0	RW	0x0	rank0_refresh Setting this register bit to 1 indicates to the uMCTL2 to issue a refresh to rank 0. Writing to this bit causes DBGSTAT.rank0_refresh_busy to be set. When DBGSTAT.rank0_refresh_busy is cleared, the command has been stored in uMCTL2. For 3DS configuration, refresh is sent to rank index 0. This operation can be performed only when RFSHCTL3.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Deep power-down operating modes or Maximum Power Saving Mode. Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic

DDRCTL_DBGSTAT

Address: Operational Base(0xFF4E0000) + offset (0x0310)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
5	RO	0x0	ctrlupd_busy SoC might initiate a ctrlupd operation only if this signal is low. This signal goes high in the clock after the uMCTL2 accepts the ctrlupd request. It goes low when the ctrlupd operation is initiated in the uMCTL2. It is recommended not to perform ctrlupd operations when this signal is high. 0 - Indicates that the SoC can initiate a ctrlupd operation 1 - Indicates that ctrlupd operation has not been initiated yet in the uMCTL2 Value After Reset:0x0 Programming Mode:Dynamic
4	RO	0x0	zq_calib_short_busy SoC might initiate a ZQCS (ZQ calibration short) operation only if this signal is low. This signal goes high in the clock after the uMCTL2 accepts the ZQCS request. It goes low when the ZQCS operation is initiated in the uMCTL2. It is recommended not to perform ZQCS operations when this signal is high. 0 - Indicates that the SoC can initiate a ZQCS operation 1 - Indicates that ZQCS operation has not been initiated yet in the uMCTL2 Value After Reset:0x0 Programming Mode:Dynamic
3:2	RW	0x0	Reserved0 Reserved Field:Yes
1	RO	0x0	rank1_refresh_busy SoC might initiate a rank1_refresh operation (refresh operation to rank 1) only if this signal is low. This signal goes high in the clock after DBGCMD.rank1_refresh is set to one. It goes low when the rank1_refresh operation is stored in the uMCTL2. It is recommended not to perform rank1_refresh operations when this signal is high. 0 - Indicates that the SoC can initiate a rank1_refresh operation 1 - Indicates that rank1_refresh operation has not been stored yet in the uMCTL2 Value After Reset:0x0 Programming Mode:Dynamic
0	RO	0x0	rank0_refresh_busy SoC might initiate a rank0_refresh operation (refresh operation to rank 0) only if this signal is low. This signal goes high in the clock after DBGCMD.rank0_refresh is set to one. It goes low when the rank0_refresh operation is stored in the uMCTL2. It is recommended not to perform rank0_refresh operations when this signal is high. 0 - Indicates that the SoC can initiate a rank0_refresh operation 1 - Indicates that rank0_refresh operation has not been stored yet in the uMCTL2 Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_SWCTL

Address: Operational Base(0xFF4E0000) + offset (0x0320)

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Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RW	0x1	sw_done Enables quasi-dynamic register programming outside reset. Program this register to 0 to enable quasi-dynamic programming. Set back register to 1 once programming is done. Value After Reset:0x1 Programming Mode:Dynamic

DDRCTL_SWSTAT

Address: Operational Base(0xFF4E0000) + offset (0x0324)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RO	0x1	sw_done_ack Register programming done. This register is the echo of SWCTL.sw_done. Wait for sw_done value 1 to propagate to sw_done_ack at the end of the programming sequence to ensure that the correct registers values are propagated to the destination clock domains. Value After Reset:0x1 Testable:untestable Programming Mode:Static

DDRCTL_SWCTLSTATIC

Address: Operational Base(0xFF4E0000) + offset (0x0328)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RW	0x0	sw_static_unlock Enables static register programming outside reset. Program this register to 1 to enable static register programming. Set register back to 0 once programming is done. Note: This ability is not supported. Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_POISONCFG

Address: Operational Base(0xFF4E0000) + offset (0x036C)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved5 Reserved Field:Yes
24	RW	0x0	rd_poison_intr_clr Interrupt clear for read transaction poisoning. Allow 2/3 clock cycles for correct value to propagate to controller logic and clear the interrupts. uMCTL2 automatically clears this bit. Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic
23:21	RW	0x0	Reserved4 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
20	RW	0x1	rd_poison_intr_en If set to 1, enables interrupts for read transaction poisoning. Value After Reset:0x1 Programming Mode:Dynamic
19:17	RW	0x0	Reserved3 Reserved Field:Yes
16	RW	0x1	rd_poison_slverr_en If set to 1, enables SLVERR response for read transaction poisoning. Value After Reset:0x1 Programming Mode:Dynamic
15:9	RW	0x00	Reserved2 Reserved Field:Yes
8	RW	0x0	wr_poison_intr_clr Interrupt clear for write transaction poisoning. Allow 2/3 clock cycles for correct value to propagate to controller logic and clear the interrupts. uMCTL2 automatically clears this bit. Value After Reset:0x0 Testable:readOnly Programming Mode:Dynamic
7:5	RW	0x0	Reserved1 Reserved Field:Yes
4	RW	0x1	wr_poison_intr_en If set to 1, enables interrupts for write transaction poisoning. Value After Reset:0x1 Programming Mode:Dynamic
3:1	RW	0x0	Reserved0 Reserved Field:Yes
0	RW	0x1	wr_poison_slverr_en If set to 1, enables SLVERR response for write transaction poisoning. Value After Reset:0x1 Programming Mode:Dynamic

DDRCTL_POISONSTAT

Address: Operational Base(0xFF4E0000) + offset (0x0370)

Bit	Attr	Reset Value	Description
31:17	RW	0x0000	Reserved1 Reserved Field:Yes
16	RO	0x0	rd_poison_intr_0 Read transaction poisoning error interrupt for port 0. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's read address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register rd_poison_intr_clr, then value propagated to APB clock. Value After Reset:0x0 Programming Mode:Dynamic
15:1	RW	0x0000	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
0	RO	0x0	wr_poison_intr_0 Write transaction poisoning error interrupt for port 0. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's write address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register wr_poison_intr_clr, then value propagated to APB clock. Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_DERATESTAT

Address: Operational Base(0xFF4E0000) + offset (0x03F0)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes
0	RO	0x0	derate_temp_limit_intr Derate temperature interrupt indicating LPDDR2/3/4 SDRAM temperature operating limit is exceeded. This register field is set to 1 when the value read from MR4[2:0] is 3'b000 or 3'b111. Cleared by register DERATECTL.derate_temp_limit_intr_clr. Value After Reset:0x0 Testable:readOnly Programming Mode:Static

DDRCTL_MP_PSTAT

Address: Operational Base(0xFF4E0000) + offset (0x03FC)

Bit	Attr	Reset Value	Description
31:17	RW	0x0000	Reserved1 Reserved Field:Yes
16	RO	0x0	wr_port_busy_0 Indicates if there are outstanding writes for AXI port 0. Value After Reset:0x0 Programming Mode:Dynamic
15:1	RW	0x0000	Reserved0 Reserved Field:Yes
0	RO	0x0	rd_port_busy_0 Indicates if there are outstanding reads for AXI port 0. Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_MP_PCCFG

Address: Operational Base(0xFF4E0000) + offset (0x0400)

Bit	Attr	Reset Value	Description
31:9	RW	0x000000	Reserved2 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
8	RW	0x0	bl_exp_mode Burst length expansion mode. By default (that is, bl_exp_mode==0) XPI expands every AXI burst into multiple HIF commands, using the memory burst length as a unit. If set to 1, then XPI uses half of the memory burst length as a unit. This applies to both reads and writes. When MSTR.data_bus_width==00, setting bl_exp_mode to 1 has no effect. This can be used in order to avoid or minimize t_ccd_l penalty in DDR4 and t_ccd_mw penalty in LPDDR4. Hence, bl_exp_mode=1 is only recommended if DDR4 or LPDDR4. Note that if DBICTL.dm_en=0, functionality is not supported in the following cases: MSTR.data_bus_width=01, MEMC_BURST_LENGTH=8 and MSTR.burst_rdwr=1000 (LPDDR4 only) MSTR.data_bus_width=01, MEMC_BURST_LENGTH=4 and MSTR.burst_rdwr=0100 (DDR4 only), with either MSTR.burstchop=0 or CRCPARCTL1.crc_enable=1 Functionality is also not supported if Data Channel Interleave is enabled. Value After Reset:0x0 Programming Mode:Static
7:5	RW	0x0	Reserved1 Reserved Field:Yes
4	RW	0x0	pagematch_limit Page match four limit. If set to 1, limits the number of consecutive same page DDRC transactions that can be granted by the Port Arbiter to four when Page Match feature is enabled. If set to 0, there is no limit imposed on number of consecutive same page DDRC transactions. Value After Reset:0x0 Programming Mode:Static
3:1	RW	0x0	Reserved0 Reserved Field:Yes
0	RW	0x0	go2critical_en If set to 1 (enabled), sets co_gs_go2critical_wr and co_gs_go2critical_lpr/co_gs_go2critical_hpr signals going to DDRC based on urgent input (awurgent, arurgent) coming from AXI master. If set to 0 (disabled), co_gs_go2critical_wr and co_gs_go2critical_lpr/co_gs_go2critical_hpr signals at DDRC are driven to 1b'0. For uPCTL2, this register field must be set to 0. Value After Reset:0x0 Programming Mode:Static

DDRCTL_MP_PCFGR_0

Address: Operational Base(0xFF4E0000) + offset (0x0404)

Bit	Attr	Reset Value	Description
31:15	RW	0x00000	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
14	RW	0x0	rd_port_pagematch_en If set to 1, enables the Page Match feature. If enabled, once a requesting port is granted, the port is continued to be granted if the following immediate commands are to the same memory page (same rank, same bank and same row). See also related PCCFG.pagematch_limit register. Value After Reset:0x0 Programming Mode:Static
13	RW	0x0	rd_port_urgent_en If set to 1, enables the AXI urgent sideband signal (arurgent). When enabled and arurgent is asserted by the master, that port becomes the highest priority and co_gs_go2critical_lpr/co_gs_go2critical_hpr signal to DDRC is asserted if enabled in PCCFG.go2critical_en register. Note that arurgent signal can be asserted anytime and as long as required which is independent of address handshaking (it is not associated with any particular command). Value After Reset:0x0 Programming Mode:Static
12	RW	0x0	rd_port_aging_en If set to 1, enables aging function for the read channel of the port. Value After Reset:0x0 Programming Mode:Static
11:10	RW	0x0	Reserved0 Reserved Field:Yes
9:0	RW	0x000	rd_port_priority Determines the initial load value of read aging counters. These counters are parallel loaded after reset, or after each grant to the corresponding port. The aging counters down-count every clock cycle where the port is requesting but not granted. The higher significant 5-bits of the read aging counter sets the priority of the read channel of a given port. Port's priority increases as the higher significant 5-bits of the counter starts to decrease. When the aging counter becomes 0, the corresponding port channel has the highest priority level (timeout condition - Priority0). For multi-port configurations, the aging counters cannot be used to set port priorities when external dynamic priority inputs (arqos) are enabled (timeout is still applicable). For single port configurations, the aging counters are only used when they timeout (become 0) to force read-write direction switching. In this case, external dynamic priority input, arqos (for reads only) can still be used to set the DDRC read priority (2 priority levels: low priority read - LPR, high priority read - HPR) on a command by command basis. Note: The two LSBs of this register field are tied internally to 2'b00. Value After Reset:0x0 Programming Mode:Static

DDRCTL_MP_PCFGW_0

Address: Operational Base(0xFF4E0000) + offset (0x0408)

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Bit	Attr	Reset Value	Description
31:15	RW	0x00000	Reserved1 Reserved Field:Yes
14	RW	0x1	wr_port_pagematch_en If set to 1, enables the Page Match feature. If enabled, once a requesting port is granted, the port is continued to be granted if the following immediate commands are to the same memory page (same rank, same bank and same row). See also related PCCFG.pagematch_limit register. Value After Reset:0x1 Programming Mode:Static
13	RW	0x0	wr_port_urgent_en If set to 1, enables the AXI urgent sideband signal (awurgent). When enabled and awurgent is asserted by the master, that port becomes the highest priority and co_gs_go2critical_wr signal to DDRC is asserted if enabled in PCCFG.go2critical_en register. Note that awurgent signal can be asserted anytime and as long as required which is independent of address handshaking (it is not associated with any particular command). Value After Reset:0x0 Programming Mode:Static
12	RW	0x0	wr_port_aging_en If set to 1, enables aging function for the write channel of the port. Value After Reset:0x0 Programming Mode:Static
11:10	RW	0x0	Reserved0 Reserved Field:Yes
9:0	RW	0x000	wr_port_priority Determines the initial load value of write aging counters. These counters are parallel loaded after reset, or after each grant to the corresponding port. The aging counters down-count every clock cycle where the port is requesting but not granted. The higher significant 5-bits of the write aging counter sets the initial priority of the write channel of a given port. Port's priority increases as the higher significant 5-bits of the counter starts to decrease. When the aging counter becomes 0, the corresponding port channel has the highest priority level. For multi-port configurations, the aging counters cannot be used to set port priorities when external dynamic priority inputs (awqos) are enabled (timeout is still applicable). For single port configurations, the aging counters are only used when they timeout (become 0) to force read-write direction switching. Note: The two LSBs of this register field are tied internally to 2'b00. Value After Reset:0x0 Programming Mode:Static

DDRCTL_MP_PCTRL_0

Address: Operational Base(0xFF4E0000) + offset (0x0490)

Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
0	RW	0x0	port_en Enables AXI port n. Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_MP_VER_NUMBER

Address: Operational Base(0xFF4E0000) + offset (0x0FF0)

Bit	Attr	Reset Value	Description
31:0	RO	0x3339302a	ver_number Indicates the Device Version Number value. This is in ASCII format, with each byte corresponding to a character of the version number Value After Reset:0x3339302a Programming Mode:Static

DDRCTL_MP_VER_TYPE

Address: Operational Base(0xFF4E0000) + offset (0x0FF4)

Bit	Attr	Reset Value	Description
31:0	RO	0x67612a2a	ver_type Indicates the Device Version Type value. This is in ASCII format, with each byte corresponding to a character of the version type Value After Reset:0x67612a2a Programming Mode:Static

DDRCTL_FREQ1_DERATEEN

Address: Operational Base(0xFF4E0000) + offset (0x2020)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	Reserved2 Reserved Field:Yes
13	RW	0x0	derate_mr4_pause_fc Pauses MR4 reads. Must only be set to 1 as part of Frequency Change procedures, if DERATEEN.derate_enable=1 Value After Reset:0x0 Programming Mode:Dynamic
12	RW	0x0	derate_mr4_tuf_dis Disables use of MR4 TUF flag (MR4[7]) bit. 0 - Use MR4 TUF flag (MR4[7]) 1 - Do not use MR4 TUF Flag (MR4[7]) For LPDDR4, it is recommended to set this register to 1. For LPDDR2 and LPDDR3, contact your memory vendor for recommended usage. This affects both the periodic derate logic (DERATEEN.derate_enable) and the derate_temp_limit_intr. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4
11	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
10:8	RW	0x0	rc_derate_value Derate value of tRC for LPDDR4. 0 - Derating uses +1 1 - Derating uses +2 2 - Derating uses +3 3 - Derating uses +4 4 - Derating uses +5 5 - Derating uses +6 6 - Derating uses +7 7 - Derating uses +8 Present only in designs configured to support LPDDR4. The required cycles for derating can be determined by dividing 3.75ns by the core_ddrc_core_clk period, and rounding it up to the next integer. Hence this register field must be set to the previous value - 1. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4
7:4	RW	0x0	derate_byte This bit indicates which byte of the MRR data is used for derating. The maximum valid value depends on MEMC_DRAM_TOTAL_DATA_WIDTH. Present only in designs configured to support LPDDR2/LPDDR3/LPDDR4. Value After Reset:0x0 Programming Mode:Static
3	RW	0x0	Reserved0 Reserved Field:Yes
2:1	RW	0x0	derate_value Derate value. 0 - Derating uses +1 1 - Derating uses +2 2 - Derating uses +3 3 - Derating uses +4 Present only in designs configured to support LPDDR2/LPDDR3/LPDDR4. The required cycles for derating can be determined by dividing 1.875ns by the core_ddrc_core_clk period, and rounding it up to the next integer. Hence this register field must be set to the previous value - 1. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4
0	RW	0x0	derate_enable Enables derating. 0 - Timing parameter derating is disabled 1 - Timing parameter derating is enabled using MR4 read value Present only in designs configured to support LPDDR2/LPDDR3/LPDDR4. This field must be set to '0' for non-LPDDR2/LPDDR3/LPDDR4 mode. Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_FREQ1_DERATEINT

Address: Operational Base(0xFF4E0000) + offset (0x2024)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00800000	mr4_read_interval Interval between two MR4 reads, used to derate the timing parameters. Present only in designs configured to support LPDDR2/LPDDR3/LPDDR4. This register must not be set to zero. Unit: DFI clock cycles. Value After Reset:0x800000 Programming Mode:Static

DDRCTL_FREQ1_PWRTMG

Address: Operational Base(0xFF4E0000) + offset (0x2034)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x40	selfref_to_x32 After this many clocks of the DDRC command channel being idle the uMCTL2 automatically puts the SDRAM into self-refresh. The DDRC command channel is considered idle when there are no HIF commands outstanding. This must be enabled in the PWRCTL.selfref_en. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x40 Programming Mode:Quasi-dynamic Group 4
15:8	RW	0x20	t_dpd_x4096 Minimum deep power-down time. For mDDR, value from the JEDEC specification is 0 as mDDR exits from deep power-down mode immediately after PWRCTL.deeppowerdown_en is de-asserted. For LPDDR2/LPDDR3, value from the JEDEC specification is 500us. Present only in designs configured to support mDDR, LPDDR2 or LPDDR3. FOR PERFORMANCE ONLY. Unit: Multiples of 4096 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x20 Programming Mode:Quasi-dynamic Group 4
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4:0	RW	0x10	powerdown_to_x32 After this many clocks of the DDRC command channel being idle the uMCTL2 automatically puts the SDRAM into power-down. The DDRC command channel is considered idle when there are no HIF commands outstanding. This must be enabled in the PWRCTL.powerdown_en. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x10 Programming Mode:Quasi-dynamic Group 4

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DDRCTL_FREQ1_RFSHCTL0

Address: Operational Base(0xFF4E0000) + offset (0x2050)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved4 Reserved Field:Yes
23:20	RW	0x2	refresh_margin Threshold value in number of DFI clock cycles before the critical refresh or page timer expires. A critical refresh is to be issued before this threshold is reached. It is recommended that this not be changed from the default value, currently shown as 0x2. It must always be less than internally used t_rfc_nom/32. Note that internally used t_rfc_nom is equal to RFSHTMG.t_rfc_nom_x1_x32 * 32 if RFSHTMG.t_rfc_nom_x1_sel=0. If RFSHTMG.t_rfc_nom_x1_sel=1 (for LPDDR2/LPDDR3/LPDDR4 per-bank refresh only), internally used t_rfc_nom is equal to RFSHTMG.t_rfc_nom_x1_x32. Note that, in LPDDR2/LPDDR3/LPDDR4, internally used t_rfc_nom may be divided by four if derating is enabled (DERATEEN.derate_enable=1). Unit: Multiples of 32 DFI clock cycles. Value After Reset:0x2 Programming Mode:Dynamic - Refresh Related
19:17	RW	0x0	Reserved3 Reserved Field:Yes
16:12	RW	0x10	refresh_to_x1_x32 If the refresh timer (tRFCnom, also known as tREFI) has expired at least once, then a speculative refresh may be performed. A speculative refresh is a refresh performed at a time when refresh would be useful. When the SDRAM bus is idle for a period of time determined by this RFSHCTL0.refresh_to_x1_x32 and the refresh timer has expired at least once since the last refresh, then a speculative refresh is performed. Speculative refreshes continues successively until there are no refreshes pending or until new reads or writes are issued to the uMCTL2. FOR PERFORMANCE ONLY. Unit: DFI clock cycles or multiples of 32 DFI clock cycles, depending on RFSHTMG.t_rfc_nom_x1_sel. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x10 Programming Mode:Dynamic - Refresh Related
11:10	RW	0x0	Reserved2 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
9:4	RW	0x00	refresh_burst The programmed value + 1 is the number of refresh timeouts that is allowed to accumulate before traffic is blocked and the refreshes are forced to execute. Closing pages to perform a refresh is a one-time penalty that must be paid for each group of refreshes. Therefore, performing refreshes in a burst reduces the per-refresh penalty of these page closings. Higher numbers for RFSHCTL.refresh_burst slightly increases utilization; lower numbers decreases the worst-case latency associated with refreshes. 0 - Single refresh 1 - Burst-of-2 refresh 7 - Burst-of-8 refresh For more information on burst refresh feature, see section 3.9 of DDR2 JEDEC specification - JESD79-2F.pdf. For DDR2/3, the refresh is always per-rank and not per-bank. The rank refresh can be accumulated over 8*tREFI cycles using the burst refresh feature. In DDR4 mode, according to Fine Granularity feature, 8 refreshes can be postponed in 1X mode, 16 refreshes in 2X mode and 32 refreshes in 4X mode. If using PHY-initiated updates, care must be taken in the setting of RFSHCTL0.refresh_burst, to ensure that tRFCmax is not violated due to a PHY-initiated update occurring shortly before a refresh burst is due. In this situation, the refresh burst is delayed until the PHY-initiated update is complete. In per-bank refresh mode of LPDDR2/LPDDR3/LPDDR4 (RFSHCTL0.per_bank_refresh = 1), 64 refreshes can be postponed. Value After Reset:0x0 Programming Mode:Dynamic - Refresh Related
3	RW	0x0	Reserved1 Reserved Field:Yes
2	RW	0x0	per_bank_refresh 1 - Per bank refresh 0 - All bank refresh Per bank refresh allows traffic to flow to other banks. Per bank refresh is not supported by all LPDDR2 devices but must be supported by all LPDDR3/LPDDR4 devices. Present only in designs configured to support LPDDR2/LPDDR3/LPDDR4. Value After Reset:0x0 Programming Mode:Static
1:0	RW	0x0	Reserved0 Reserved Field:Yes

DDRCTL_FREQ1_RFSHTMG

Address: Operational Base(0xFF4E0000) + offset (0x2064)

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Bit	Attr	Reset Value	Description
31	RW	0x0	t_rfc_nom_x1_sel Specifies whether the RFSHTMG.t_rfc_nom_x1_x32 and RFSHCTL0.refresh_to_x1_x32 register values are x1 or x32. 0 - x32 register values are used 1 - x1 register values are used This applies only when per-bank refresh is enabled (RFSHCTL0.per_bank_refresh=1); if per-bank refresh is not enabled, the x32 register values are used and this register field is ignored. This register field does not exist for configurations which do not support LPDDR2/3/4. For such configurations, the value of this register field can be assumed to be 0, so that RFSHTMG.t_rfc_nom_x1_x32 and RFSHCTL0.refresh_t_x1_x32 are interpreted as x32 register fields Value After Reset:0x0 Programming Mode:Dynamic - Refresh Related
30:28	RW	0x0	Reserved1 Reserved Field:Yes
27:16	RW	0x062	t_rfc_nom_x1_x32 Average time interval between refreshes per rank (Specification: 7.8us for DDR2, DDR3 and DDR4. See JEDEC specification for mDDR, LPDDR2, LPDDR3 and LPDDR4). When the controller is operating in 1:1 mode, set this register to RoundDown(tREFI/tCK) When the controller is operating in 1:2 mode, set this register to RoundDown(RoundDown(tREFI/tCK)/2) In both the previous cases, if RFSHTMG.t_rfc_nom_x1_sel = 0, divide the previous result by 32 and round down. For LPDDR2/LPDDR3/LPDDR4: If using all-bank refreshes (RFSHCTL0.per_bank_refresh = 0), use tREFIab in the previous calculations If using per-bank refreshes (RFSHCTL0.per_bank_refresh = 1), use tREFIpb in the previous calculations For DDR4 mode, tREFI value is different depending on the refresh mode. You must program appropriate value from the spec based on the value programmed in the refresh mode register. Note: RFSHTMG.t_rfc_nom_x1_x32 must be greater than 0x1 If RFSHTMG.t_rfc_nom_x1_sel == 1, RFSHTMG.t_rfc_nom_x1_x32 must be greater than RFSHTMG.t_rfc_min If RFSHTMG.t_rfc_nom_x1_sel == 0, RFSHTMG.t_rfc_nom_x1_x32 * 32 must be greater than RFSHTMG.t_rfc_min In non-DDR4 or DDR4 Fixed 1x mode: RFSHTMG.t_rfc_nom_x1_x32 must be less than or equal to 0xFFE In DDR4 Fixed 2x mode: RFSHTMG.t_rfc_nom_x1_x32 must be less than or equal to 0x7FF In DDR4 Fixed 4x mode: RFSHTMG.t_rfc_nom_x1_x32 must be less than or equal to 0x3FF Unit: DFI clock cycles or multiples of 32 DFI clock cycles, depending on RFSHTMG.t_rfc_nom_x1_sel. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x62 Programming Mode:Dynamic - Refresh Related

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Bit	Attr	Reset Value	Description
15	RW	0x0	lpddr3_trefbw_en Used only when LPDDR3 memory type is connected. Must only be changed when uMCTL2 is in reset. Specifies whether to use the tREFBW parameter (required by some LPDDR3 devices which comply with earlier versions of the LPDDR3 JEDEC specification) or not: 0 - tREFBW parameter not used 1 - tREFBW parameter used Value After Reset:0x0 Programming Mode:Static
14:10	RW	0x00	Reserved0 Reserved Field:Yes
9:0	RW	0x08c	t_rfc_min tRFC (min): Minimum time from refresh to refresh or activate. When the controller is operating in 1:1 mode, t_rfc_min must be set to RoundUp(tRFCmin/tCK). When the controller is operating in 1:2 mode, t_rfc_min must be set to RoundUp(RoundUp(tRFCmin/tCK)/2). In LPDDR2/LPDDR3/LPDDR4 mode: If using all-bank refreshes, the tRFCmin value in the previous equations is equal to tRFCab If using per-bank refreshes, the tRFCmin value in the previous equations is equal to tRFCpb In DDR4 mode, the tRFCmin value in the previous equations is different depending on the refresh mode (fixed 1X,2X,4X) and the device density. You must program the appropriate value from the spec based on the 'refresh_mode' and the device density that is used. Unit: DFI clock cycles. Value After Reset:0x8c Programming Mode:Dynamic - Refresh Related

DDRCTL_FREQ1_RFSHTMG1

Address: Operational Base(0xFF4E0000) + offset (0x2068)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x8c	t_pbr2pbr LPDDR4:tpbR2pbR. Per-bank refresh to Per-bank refresh different bank Time. When the controller is operating in 1:1 frequency ratio mode, program this to RoundUp(tpbR2pbR/tCK). When the controller is operating in 1:2 frequency ratio mode, program this to RoundUp(RoundUp(tpbR2pbR/tCK)/2). The tpbR2pbR value in the previous equations is different depending on the device density. You must program the appropriate value from the specification. Register is valid only in LPDDR4 per-bank refresh mode (RFSHCTL0.per_bank_refresh_mode == 1). Value After Reset:0x8c Programming Mode:Dynamic - Refresh Related
15:0	RW	0x0000	Reserved0 Reserved Field:Yes

DDRCTL_FREQ1_INIT3

Address: Operational Base(0xFF4E0000) + offset (0x20DC)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr DDR2:Indicates the value to write to MR register. Bit 8 is for DLL and the setting here is ignored. The uMCTL2 sets this bit appropriately. DDR3/DDR4: Value loaded into MR0 register. mDDR: Value to write to MR register. LPDDR2/LPDDR3/LPDDR4 - Value to write to MR1 register Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 1, Group 4
15:0	RW	0x0510	emr DDR2: Indicates the value to write to EMR register. Bits 9:7 are for OCD and the setting in this register is ignored. The uMCTL2 sets those bits appropriately. DDR3/DDR4: Value to write to MR1 register Set bit 7 to 0. mDDR: Value to write to EMR register. LPDDR2/LPDDR3/LPDDR4 - Value to write to MR2 register. Value After Reset:0x510 Programming Mode:Quasi-dynamic Group 4

DDRCTL_FREQ1_INIT4

Address: Operational Base(0xFF4E0000) + offset (0x20E0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	emr2 DDR2: Indicates the value to write to EMR2 register. DDR3/DDR4: Value to write to MR2 register. LPDDR2/LPDDR3/LPDDR4: Value to write to MR3 register. mDDR: Unused. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 4
15:0	RW	0x0000	emr3 DDR2: Indicates the value to write to EMR3 register. DDR3/DDR4: Value to write to MR3 register. mDDR/LPDDR2/LPDDR3: Unused. LPDDR4: Value to write to MR13 register. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ1_INIT6

Address: Operational Base(0xFF4E0000) + offset (0x20E8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr4 DDR4 - Indicates the value to be loaded into SDRAM MR4 registers. LPDDR4- Value to be loaded into SDRAM MR11 registers. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4
15:0	RW	0x0000	mr5 DDR4 - Indicates the value to be loaded into SDRAM MR5 registers. LPDDR4- Value to be loaded into SDRAM MR12 registers. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 1, Group 4

DDRCTL_FREQ1_INIT7

Address: Operational Base(0xFF4E0000) + offset (0x20EC)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr22 LPDDR4 - Indicates the value to be loaded into SDRAM MR22 registers. Used in LPDDR4 designs only. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 4
15:0	RW	0x0000	mr6 DDR4 - Indicates the value to be loaded into SDRAM MR6 registers. LPDDR4- Value to be loaded into SDRAM MR14 registers. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 4

DDRCTL_FREQ1_RANKCTL

Address: Operational Base(0xFF4E0000) + offset (0x20F4)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	Reserved2 Reserved Field:Yes
26	RW	0x0	diff_rank_wr_gap_msb Only present for multi-rank configurations. 1-bit extension to be used when RANKCTL.diff_rank_wr_gap field needs to be set to a value greater than 0xF. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2
25	RW	0x0	Reserved1 Reserved Field:Yes
24	RW	0x0	diff_rank_rd_gap_msb Only present for multi-rank configurations. 1-bit extension to be used when RANKCTL.diff_rank_rd_gap field needs to be set to a value greater than 0xF. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2
23:16	RW	0x00	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
15:12	RW	0x0	max_rank_wr Only present for multi-rank configurations. Background: Writes to the same rank can be performed back-to-back. Writes to different ranks require additional gap dictated by the register RANKCTL.diff_rank_wr_gap. This is to avoid possible data bus contention as well as to give PHY enough time to switch the delay when changing ranks. The uMCTL2 arbitrates for bus access on a cycle-by-cycle basis; therefore after a write is scheduled, there are few clock cycles (determined by the value on RANKCTL.diff_rank_wr_gap register) in which only writes from the same rank are eligible to be scheduled. This prevents writes from other ranks from having fair access to the data bus. This parameter represents the maximum number of writes that can be scheduled consecutively to the same rank. After this number is reached, a delay equal to RANKCTL.diff_rank_wr_gap is inserted by the scheduler to allow all ranks a fair opportunity to be scheduled. Higher numbers increase bandwidth utilization, lower numbers increase fairness. This feature can be DISABLED by setting this register to 0. When set to 0, the controller stays on the same rank as long as commands are available for it. Minimum programmable value is 0 (feature disabled) and maximum programmable value is 0xF. For uPCTL2, this register field must be set to 0 (feature disabled) FOR PERFORMANCE ONLY. Value After Reset:0x0 Programming Mode:Static

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Bit	Attr	Reset Value	Description
11:8	RW	0x6	diff_rank_wr_gap Only present for multi-rank configurations. Indicates the number of clocks of gap in data responses when performing consecutive writes to different ranks. This is used to switch the delays in the PHY to match the rank requirements. This value must consider both PHY requirement and ODT requirement. PHY requirement - tphy_wrcsgap (For more information on value of tphy_wrcsgap, see PHY databook) ODT requirement - The value programmed in this register takes care of the ODT switch off timing requirement when switching ranks during writes. For LPDDR4, with DQ ODT enabled, diff_rank_wr_gap must be a minimum of ODTLoff - ODTLon - BL/2 + 1 For other cases, diff_rank_wr_gap must be a minimum of ODTCFG.wr_odt_hold - BL/2 When the controller is operating in 1:1 mode, program this to the larger of PHY requirement or ODT requirement. If CRC is enabled, the value can be decreased by 2 because the programmed value is internally increased by 1 (it is always 2 in terms of DFI PHY clock cycle as CRC is supported only with 1:2 frequency ratio). When the controller is operating in 1:2 mode, program this to the larger value divided by two and round it up to the next integer. After PHY has completed training the value programmed may need to be increased. For more information, see relevant PHY documentation. Note that, if using DDR4-LRDIMM, refer to TWRWR timing requirements in JEDEC DDR4 Data Buffer (DDR4DB01) Specification. If a value greater than 0xF is needed, the RANKCTL.diff_rank_wr_gap_msb field must be used as extension. For DFI 1:2 mode, a maximum value of {diff_rank_wr_gap_msb,diff_rank_wr_gap} < 'h11 is supported. For DFI 1:1 mode a maximum value of {diff_rank_wr_gap_msb,diff_rank_wr_gap} <= 'h1F is supported. Unit: DFI clock cycles. Value After Reset:0x6 Programming Mode:Quasi-dynamic Group 2
7:4	RW	0x6	diff_rank_rd_gap Only present for multi-rank configurations. Indicates the number of clocks of gap in data responses when performing consecutive reads to different ranks. This is used to switch the delays in the PHY to match the rank requirements. This value must consider both PHY requirement and ODT requirement. PHY requirement:tphy_rdcsgap (For more information on value of tphy_rdcsgap, see PHY databook) ODT requirement: The value programmed in this register takes care of the ODT switch off timing requirement when switching ranks during reads: Value After Reset:0x6 Programming Mode:Quasi-dynamic Group 2

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	max_rank_rd Only present for multi-rank configurations. Background: Reads to the same rank can be performed back-to-back. Reads to different ranks require additional gap dictated by the register RANKCTL.diff_rank_rd_gap. This is to avoid possible data bus contention as well as to give PHY enough time to switch the delay when changing ranks. The uMCTL2 arbitrates for bus access on a cycle-by-cycle basis; therefore after a read is scheduled, there are few clock cycles (determined by the value on RANKCTL.diff_rank_rd_gap register) in which only reads from the same rank are eligible to be scheduled. This prevents reads from other ranks from having fair access to the data bus. This parameter represents the maximum number of reads that can be scheduled consecutively to the same rank. After this number is reached, a delay equal to RANKCTL.diff_rank_rd_gap is inserted by the scheduler to allow all ranks a fair opportunity to be scheduled. Higher numbers increase bandwidth utilization, lower numbers increase fairness. This feature can be DISABLED by setting this register to 0. When set to 0, the controller stays on the same rank as long as commands are available for it. Minimum programmable value is 0 (feature disabled) and maximum programmable value is 0xF. For uPCTL2, this register field must be set to 0 (feature disabled) FOR PERFORMANCE ONLY. Value After Reset:0x0 Programming Mode:Static

DDRCTL_FREQ1_DRAMTMG0

Address: Operational Base(0xFF4E0000) + offset (0x2100)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved3 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
30:24	RW	0x0f	wr2pre Specifies the minimum time between write and precharge to same bank. Specifications: WL + BL/2 + tWR = approximately 8 cycles + 15 ns = 14 clocks @400MHz and less for lower frequencies. where: WL: Write latency BL: Burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM. BST (burst terminate) is not supported at present tWR: Write recovery time. This comes directly from the SDRAM specification Add one extra cycle for LPDDR2/LPDDR3/LPDDR4 for this parameter. When the controller is operating in 1:2 frequency ratio mode, 1T mode, divide the previous value by 2. No rounding up. When the controller is operating in 1:2 frequency ratio mode, 2T mode, geardown mode or LPDDR4 mode, divide the previous value by 2 and round it up to the next integer value. Note that, depending on the PHY, if using LRDIMM, it may be necessary to adjust the value of this parameter to compensate for the extra cycle of latency through the LRDIMM. For DDR4, LPDDR4, LPDDR3, using nWR(WR) instead of tWR to calculate the value of this parameter. Unit: DFI clock cycles. Value After Reset:0xf Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
23:22	RW	0x0	Reserved2 Reserved Field:Yes
21:16	RW	0x10	t_faw tFAW - valid only when 8 or more banks(or banks x bank groups) are present. In 8-bank design, at most 4 banks must be activated in a rolling window of tFAW cycles. When the controller is operating in 1:2 frequency ratio mode, program this to (tFAW/2) and round up to next integer value. In a 4-bank design, set this register to 0x1 independent of the 1:1/1:2 frequency mode. Unit: DFI clock cycles. Value After Reset:0x10 Programming Mode:Quasi-dynamic Group 2, Group 4
15	RW	0x0	Reserved1 Reserved Field:Yes
14:8	RW	0x1b	t_ras_max tRAS(max) - Specifies the maximum time between activate and precharge to same bank. This is the maximum time that a page can be kept open Minimum value of this register is 1. Zero is invalid. When the controller is operating in 1:1 frequency ratio mode, t_ras_max must be set to RoundDown(tRAS(max)/tCK/1024). When the controller is operating in 1:2 frequency ratio mode, t_ras_max must be set to RoundDown((RoundDown(tRAS(max)/tCK/1024)-1)/2). Unit: Multiples of 1024 DFI clock cycles. Value After Reset:0x1b Programming Mode:Quasi-dynamic Group 2, Group 4

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Bit	Attr	Reset Value	Description
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5:0	RW	0x0f	t_ras_min tRAS(min) - Specifies the minimum time between activate and precharge to the same bank. When the controller is operating in 1:1 frequency ratio mode, t_ras_min must be set to RoundUp(tRASmin/tCK) When the controller is operating in 1:2 frequency ratio mode, 1T mode, t_ras_min must be set to RoundDown(RoundUp(tRASmin/tCK)/2) When the controller is operating in 1:2 frequency ratio mode, 2T mode, geardown mode or LPDDR4 mode, t_ras min must be set to RoundUp(RoundUp(tRASmin/tCK)/2) Unit: DFI clock cycles. Value After Reset:0xf Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ1_DRAMTMG1

Address: Operational Base(0xFF4E0000) + offset (0x2104)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved2 Reserved Field:Yes
20:16	RW	0x08	t_xp tXP - Specifies the minimum time after power-down exit to any operation. For DDR3, this must be programmed to tXPDLL if slow powerdown exit is selected in MR0[12]. If C/A parity for DDR4 is used, set to (tXP+PL) instead. If LPDDR4 is selected and its spec has tCKELPD parameter, set to the larger of tXP and tCKELPD instead. When the controller is operating in 1:2 frequency ratio mode, program this to (tXP/2) and round it up to the next integer value. Units: DFI clock cycles. Value After Reset:0x8 Programming Mode:Quasi-dynamic Group 2, Group 4
15:14	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
13:8	RW	0x04	rd2pre tRTP - Specifies the minimum time from read to precharge of same bank. DDR2 - tAL + BL/2 + max(RoundUp(tRTP/tCK), 2) - 2 DDR3 - tAL + max (RoundUp(tRTP/tCK), 4) DDR4 - Max of following two equations: tAL + max (RoundUp(tRTP/tCK), 4) or, RL + BL/2 - tRP (*). mDDR - BL/2 LPDDR2 - Depends on if it is LPDDR2-S2 or LPDDR2-S4: LPDDR2-S2: BL/2 + RoundUp(tRTP/tCK) - 1. LPDDR2-S4: BL/2 + max(RoundUp(tRTP/tCK),2) - 2. LPDDR3 - BL/2 + max(RoundUp(tRTP/tCK),4) - 4 LPDDR4 - BL/2 + max(RoundUp(tRTP/tCK),8) - 8 (*) When both DDR4 SDRAM and ST-MRAM are used simultaneously, use SDRAM's tRP value for calculation. When the controller is operating in 1:2 mode, 1T mode, divide the previous value by 2. No rounding up. When the controller is operating in 1:2 mode, 2T mode, geardown mode or LPDDR4 mode, divide the previous value by 2 and round it up to the next integer value. For DDR4, using RTP instead of tRTP to calculate the value of this parameter. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
7	RW	0x0	Reserved0 Reserved Field:Yes
6:0	RW	0x14	t_rc tRC - Specifies the minimum time between activates to same bank. When the controller is operating in 1:2 frequency ratio mode, program this to (tRC/2) and round up to next integer value. Unit: DFI clock cycles. Value After Reset:0x14 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ1_DRAMTMG2

Address: Operational Base(0xFF4E0000) + offset (0x2108)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved3 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
29:24	RW	0x03	write_latency Set this field to WL. Indicates the Time from write command to write data on SDRAM interface. This must be set to WL. For mDDR, it must be set to 1. Note that, depending on the PHY, if using RDIMM/LRDIMM, it might be necessary to adjust the value of WL to compensate for the extra cycle of latency through the RDIMM/LRDIMM. When the controller is operating in 1:2 frequency ratio mode, divide the value calculated using the previous equation by 2, and round it up to next integer. This register field is not required for DDR2 and DDR3, as the DFI read and write latencies defined in DFITMG0 and DFITMG1 are sufficient for those protocols For all protocols, in addition to programming this register field, it is necessary to program DFITMG0 and DFITMG1 to control the read and write latencies Unit: DFI clock cycles. Value After Reset:0x3 Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
23:22	RW	0x0	Reserved2 Reserved Field:Yes
21:16	RW	0x05	read_latency Set this field to RL. Indicates the time from read command to read data on SDRAM interface. This must be set to RL. Note that, depending on the PHY, if using RDIMM/LRDIMM, it might be necessary to adjust the value of RL to compensate for the extra cycle of latency through the RDIMM/LRDIMM. When the controller is operating in 1:2 frequency ratio mode, divide the value calculated using the previous equation by 2, and round it up to next integer. This register field is not required for DDR2 and DDR3, as the DFI read and write latencies defined in DFITMG0 and DFITMG1 are sufficient for those protocols For all protocols, in addition to programming this register field, it is necessary to program DFITMG0 and DFITMG1 to control the read and write latencies Unit: DFI clock cycles. Value After Reset:0x5 Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
15:14	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
13:8	RW	0x06	rd2wr Minimum time from read command to write command. This must include time for bus turnaround (both within ranks and between ranks) and all PHY and system requirements. After the PHY has completed training, the value programmed may need to be increased. Please see the relevant PHY databook for details of what should be included here. The following calculations are minimum values, and do not include the PHY/system requirements mentioned above: DDR2/3/mDDR: RL + BL/2 + 2 - WL DDR4: RL + BL/2 + 1 + WR_PREAMBLE - WL LPDDR2/LPDDR3: RL + BL/2 + RU(tDQSCKmax/tCK) + 1 - WL LPDDR4(DQ ODT is Disabled): RL + BL/2 + RU(tDQSCKmax/tCK) + WR_PREAMBLE + RD_POSTAMBLE - WL LPDDR4(DQ ODT is Enabled): RL + BL/2 + RU(tDQSCKmax/tCK) + RD_POSTAMBLE - ODTLon - RU(tODTon(min)/tCK) + 1 Where: WL: Write latency BL: Burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM RL: Read latency = CAS latency WR_PREAMBLE: 1 (1tCK write preamble), 2 (2tCK write preamble). This is unique to DDR4 and LPDDR4 RD_POSTAMBLE: 0.5 (0.5tCK read postamble), 1.5 (1.5tCK read postamble). This is unique to LPDDR4 For LPDDR2/LPDDR3/LPDDR4, if derating is enabled (DERATEEN.derate_enable=1), derated tDQSCKmax must be used. When the controller is operating in 1:2 frequency ratio mode, divide the value calculated using the previous equation by 2, and round it up to next integer. Note that, depending on the PHY, if using LRDIMM, it may be necessary to adjust the value of this parameter to compensate for the extra cycle of latency through the LRDIMM. Unit: DFI clock cycles. Value After Reset:0x6 Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
7:6	RW	0x0	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
5:0	RW	0x0d	wr2rd In DDR4, minimum time from write command to read command for same bank group. In other protoocls, minimum time from write command to read command. This must include time for bus turn-around and all PHY and system requirements. After the PHY has completed training, the value programmed may need to be increased. Please see the relevant PHY databook for details of what should be included here. The following calculations are minimum values, and do not include the PHY/system requirements mentioned above: DDR4: CWL + PL + BL/2 + tWTR_L LPDDR2/3/4: WL + BL/2 + tWTR + 1 Others: CWL + BL/2 + tWTR Where: CWL: CAS write latency WL: Write latency PL: Parity latency BL: Burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM tWTR_L: Internal write to read command delay for same bank group. This comes directly from the SDRAM specification tWTR: Internal write to read command delay. This comes directly from the SDRAM specification Add one extra cycle for LPDDR2/LPDDR3/LPDDR4 operation. WTR_L must be increased by one if DDR4 2tCK write preamble is used. When the controller is operating in 1:2 mode, divide the value calculated using the previous equation by 2, and round it up to next integer. If your configuration has RANKCTL1.wr2rd_dr, write to read bus turn-around between different physical ranks are controlled by RANKCTL1.wr2rd_dr. Unit: DFI clock cycles. Value After Reset:0xd Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_FREQ1_DRAMTMG3

Address: Operational Base(0xFF4E0000) + offset (0x210C)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved2 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
29:20	RW	0x005	t_mrw Indicates the time to wait after a mode register write or read (MRW or MRR). Present only in designs configured to support LPDDR2, LPDDR3 or LPDDR4. LPDDR2 typically requires value of 5. LPDDR3 typically requires value of 10. LPDDR4: Set this to the larger of tMRW and tMRWCKEL. For LPDDR2, this register is used for the time from a MRW/MRR to all other commands. When the controller is operating in 1:2 frequency ratio mode, program this to the previous values divided by 2 and round it up to the next integer value. For LDPDR3, this register is used for the time from a MRW/MRR to a MRW/MRR. Unit: DFI clock cycles. Value After Reset:0x5 Programming Mode:Quasi-dynamic Group 2, Group 4
19:18	RW	0x0	Reserved1 Reserved Field:Yes
17:12	RW	0x04	t_mrd tMRD- Indicates the number of cycles to wait after a mode register write or read. Depending on the connected SDRAM, tMRD represents: DDR2/mDDR: Time from MRS to any command DDR3/4: Time from MRS to MRS command LPDDR2: not used LPDDR3/4: Time from MRS to non-MRS command When the controller is operating in 1:2 frequency ratio mode, program this to (tMRD/2) and round it up to the next integer value. If C/A parity for DDR4 is used, set to tMRD_PAR(tMOD+PL) instead. If CAL mode is enabled (DFITMG1.dfi_t_cmd_lat > 0), tCAL (=DFITMG1.dfi_cmd_lat) must be added to the previous calculations. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 2, Group 4
11:10	RW	0x0	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
9:0	RW	0x00c	t_mod tMOD - Parameter used only in DDR3 and DDR4. Indicates the number of cycles between load mode command and following non-load mode command. If C/A parity for DDR4 is used, set to tMOD_PAR(tMOD+PL) instead. If CAL mode is enabled (DFITMG1.dfi_t_cmd_lat > 0), tCAL (=DFITMG1.dfi_cmd_lat) must be added to the previous calculations. Set to tMOD if controller is operating in 1:1 frequency ratio mode, or tMOD/2 (rounded up to next integer) if controller is operating in 1:2 frequency ratio mode. Note that if using RDIMM/LRDIMM, depending on the PHY, it may be necessary to adjust the value of this parameter to compensate for the extra cycle of latency applied to mode register writes by the RDIMM/LRDIMM chip. Also note that if using RDIMM or LRDIMM, the minimum value of this register is tMRD_L2 if controller is operating in 1:1 frequency ratio mode, or tMRD_L2/2 (rounded up to next integer) if controller is operating in 1:2 frequency ratio mode. Unit: DFI clock cycles. Value After Reset:0xc Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ1_DRAMTMG4

Address: Operational Base(0xFF4E0000) + offset (0x2110)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved3 Reserved Field:Yes
28:24	RW	0x05	t_rcd tRCD - tAL: Indicates the minimum time from activate to read or write command to same bank. When the controller is operating in 1:2 frequency ratio mode, program this to ((tRCD - tAL)/2) and round it up to the next integer value. Minimum value allowed for this register is 1, which implies minimum (tRCD - tAL) value to be 2 when the controller is operating in 1:2 frequency ratio mode. Unit: DFI clock cycles. Value After Reset:0x5 Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
23:20	RW	0x0	Reserved2 Reserved Field:Yes
19:16	RW	0x4	t_ccd DDR4: tCCD_L: This is the minimum time between two reads or two writes for same bank group. Others: tCCD: This is the minimum time between two reads or two writes. When the controller is operating in 1:2 frequency ratio mode, program this to (tCCD_L/2 or tCCD/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 2, Group 4
15:12	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
11:8	RW	0x4	t_rrd DDR4: tRRD_L: This is the minimum time between activates from bank "a" to bank "b" for same bank group. Others: tRRD: Minimum time between activates from bank "a" to bank "b" When the controller is operating in 1:2 frequency ratio mode, program this to (tRRD_L/2 or tRRD/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 2, Group 4
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4:0	RW	0x05	t_rp tRP: Indicates the minimum time from single-bank precharge to activate of same bank. When the controller is operating in 1:1 frequency ratio mode, t_rp must be set to RoundUp(tRP/tCK). When the controller is operating in 1:2 frequency ratio mode, t_rp must be set to RoundDown(RoundUp(tRP/tCK)/2) + 1. When the controller is operating in 1:2 frequency ratio mode in LPDDR4, t_rp must be set to RoundUp(RoundUp(tRP/tCK)/2). Unit: DFI clock cycles. Value After Reset:0x5 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ1_DRAMTMG5

Address: Operational Base(0xFF4E0000) + offset (0x2114)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved3 Reserved Field:Yes
27:24	RW	0x5	t_cksrx This is the time before self-refresh Exit that CK is maintained as a valid clock before issuing SRX. Specifies the clock stable time before SRX. Recommended settings: mDDR - 1 LPDDR2 - 2 LPDDR3 - 2 LPDDR4 - tCKCKEH DDR2 - 1 DDR3 - tCKSRX DDR4 - tCKSRX When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. Unit: DFI clock cycles. Value After Reset:0x5 Programming Mode:Quasi-dynamic Group 2, Group 4
23	RW	0x0	Reserved2 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
22:16	RW	0x05	t_cksre This is the time after self-refresh Down Entry that CK is maintained as a valid clock. Specifies the clock disable delay after SRE. Recommended settings: mDDR - 0 LPDDR2 - 2 LPDDR3 - 2 LPDDR4 - tCKELCK DDR2 - 1 DDR3 - Max (10 ns, 5 tCK) DDR4(No RDIMM) - Max (10 ns, 5 tCK) (+ PL(parity latency)(*)) DDR4(RDIMM) - Max (Max (10 ns, 5 tCK) (+ PL(parity latency)(*)), tCKOff) (*)Only if CRCPARCTL1.caparity_disable_before_sr=0, this register must be increased by PL. When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. Unit: DFI clock cycles. Value After Reset:0x5 Programming Mode:Quasi-dynamic Group 2, Group 4
15:14	RW	0x0	Reserved1 Reserved Field:Yes
13:8	RW	0x04	t_ckesr Indicates the minimum CKE low width for self-refresh or self-refresh power down entry to exit timing in memory clock cycles. Recommended settings: mDDR - tRFC LPDDR2 - tCKESR LPDDR3 - tCKESR LPDDR4 - max(tCKE, tSR) DDR2 - tCKE DDR3 - tCKE + 1 DDR4(No RDIMM) - tCKE + 1 (+ PL(parity latency)(*)) DDR4(RDIMM) - t_cksre + tCKEV (*)Only if CRCPARCTL1.caparity_disable_before_sr=0, this register must be increased by PL. When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 2, Group 4
7:5	RW	0x0	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
4:0	RW	0x03	t_cke Indicates the minimum number of cycles of CKE HIGH/LOW during power-down and self-refresh. LPDDR2/LPDDR3 mode - Set this to the larger of tCKE or tCKESR LPDDR4 mode - Set this to the larger of tCKE or tSR Non-LPDDR2/non-LPDDR3/non-LPDDR4 designs - Set this to tCKE value When the controller is operating in 1:2 frequency ratio mode, program this to (value described above)/2 and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x3 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ1_DRAMTMG6

Address: Operational Base(0xFF4E0000) + offset (0x2118)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved2 Reserved Field:Yes
27:24	RW	0x2	t_ckdpde This is the time after Deep Power Down Entry that CK is maintained as a valid clock. Specifies the clock disable delay after DPDE. Recommended settings: mDDR: 0 LPDDR2: 2 LPDDR3: 2 When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. This is only present for designs supporting mDDR or LPDDR2/LPDDR3 devices. Unit: DFI clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4
23:20	RW	0x0	Reserved1 Reserved Field:Yes
19:16	RW	0x2	t_ckdpdx This is the time before Deep Power Down Exit that CK is maintained as a valid clock before issuing DPDX. Specifies the clock stable time before DPDX. Recommended settings: mDDR - 1 LPDDR2 - 2 LPDDR3 - 2 When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. This is only present for designs supporting mDDR or LPDDR2 devices. Unit: DFI clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4
15:4	RW	0x000	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
3:0	RW	0x5	t_ckcsx This is the time before Clock Stop Exit that CK is maintained as a valid clock before issuing Clock Stop Exit. Specifies the clock stable time before next command after Clock Stop Exit. Recommended settings: mDDR - 1 LPDDR2 - tXP + 2 LPDDR3 - tXP + 2 LPDDR4 - tXP + 2 When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. This is only present for designs supporting mDDR or LPDDR2/LPDDR3/LPDDR4 devices. Unit: DFI clock cycles. Value After Reset:0x5 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ1_DRAMTMG7

Address: Operational Base(0xFF4E0000) + offset (0x211C)

Bit	Attr	Reset Value	Description
31:12	RW	0x00000	Reserved1 Reserved Field:Yes
11:8	RW	0x2	t_ckpde This is the time after Power Down Entry that CK is maintained as a valid clock. Specifies the clock disable delay after PDE. Recommended settings: mDDR - 0 LPDDR2 - 2 LPDDR3 - 2 LPDDR4 - tCKELCK When using DDR2/3/4 SDRAM, this register must be set to the same value as DRAMTMG5.t_cksre. When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. This is only present for designs supporting mDDR or LPDDR2/LPDDR3/LPDDR4 devices. Unit: DFI clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4
7:4	RW	0x0	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
3:0	RW	0x2	t_ckpdx This is the time before Power Down Exit that CK is maintained as a valid clock before issuing PDX. Specifies the clock stable time before PDX. Recommended settings: mDDR - 0 LPDDR2 - 2 LPDDR3 - 2 LPDDR4 - tCKCKEH When using DDR2/3/4 SDRAM, this register must be set to the same value as DRAMTMG5.t_cksrx. When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. This is only present for designs supporting mDDR or LPDDR2/LPDDR3/LPDDR4 devices. Unit: DFI clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ1_DRAMTMG8

Address: Operational Base(0xFF4E0000) + offset (0x2120)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved3 Reserved Field:Yes
30:24	RW	0x03	t_xs_fast_x32 tXS_FAST: Exit self-refresh to ZQCL, ZQCS and MRS (only CL, WR, RTP and Geardown mode). When the controller is operating in 1:2 frequency ratio mode, program this to the previous value divided by 2 and round up to next integer value. Note: This is applicable to only ZQCL/ZQCS commands. Note: Ensure this is less than or equal to t_xs_x32. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x3 Programming Mode:Quasi-dynamic Group 2, Group 4
23	RW	0x0	Reserved2 Reserved Field:Yes
22:16	RW	0x03	t_xs_abort_x32 tXS_ABORT: Exit self-refresh to commands not requiring a locked DLL in self-refresh Abort. When the controller is operating in 1:2 frequency ratio mode, program this to the previous value divided by 2 and round up to next integer value. Note: Ensure this is less than or equal to t_xs_x32. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x3 Programming Mode:Quasi-dynamic Group 2, Group 4
15	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
14:8	RW	0x44	t_xs_dll_x32 tXSDLL: Exit self-refresh to commands requiring a locked DLL. When the controller is operating in 1:2 frequency ratio mode, program this to the previous value divided by 2 and round up to next integer value. Note: Used only for DDR2, DDR3 and DDR4 SDRAMs. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x44 Programming Mode:Quasi-dynamic Group 2, Group 4
7	RW	0x0	Reserved0 Reserved Field:Yes
6:0	RW	0x05	t_xs_x32 tXS: Exit self-refresh to commands not requiring a locked DLL. When the controller is operating in 1:2 frequency ratio mode, program this to the previous value divided by 2 and round up to next integer value. Note: Used only for DDR2, DDR3 and DDR4 SDRAMs. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x5 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ1_DRAMTMG9

Address: Operational Base(0xFF4E0000) + offset (0x2124)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved3 Reserved Field:Yes
30	RW	0x0	ddr4_wr_preamble DDR4 Write preamble mode. 0 - 1tCK preamble 1 - 2tCK preamble Present only with MEMC_FREQ_RATIO=2. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4
29:19	RW	0x000	Reserved2 Reserved Field:Yes
18:16	RW	0x4	t_ccd_s tCCD_S: This is the minimum time between two reads or two writes for different bank group. When the controller is operating in 1:2 frequency ratio mode, program this to (tCCD_S/2) and round it up to the next integer value. Present only in designs configured to support DDR4. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 2, Group 4
15:12	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
11:8	RW	0x4	t_rrd_s tRRD_S: This is the minimum time between activates for different bank group. When the controller is operating in 1:2 frequency ratio mode, program this to (tRRD_S/2) and round it up to the next integer value. Present only in designs configured to support DDR4. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 2, Group 4
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5:0	RW	0x0d	wr2rd_s Minimum time from write command to read command for different bank group. This must include time for bus turn-around and all PHY and system requirements. After the PHY has completed training, the value programmed may need to be increased. Please see the relevant PHY databook for details of what should be included here. The following calculations are minimum values, and do not include the PHY/system requirements mentioned above: CWL + PL + BL/2 + tWTR_S Where: CWL: CAS write latency PL: Parity latency BL: Burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM tWTR_S: Internal write to read command delay for different bank group. This comes directly from the SDRAM specification WTR_S must be increased by one if DDR4 2tCK write preamble is used. When the controller is operating in 1:2 mode, divide the value calculated using the previous equation by 2, and round it up to next integer. If your configuration has RANKCTL1.wr2rd_dr, write to read bus turn-around between different physical ranks are controlled by RANKCTL1.wr2rd_dr. Unit: DFI clock cycles. Value After Reset:0xd Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_FREQ1_DRAMTMG10

Address: Operational Base(0xFF4E0000) + offset (0x2128)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved2 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
20:16	RW	0x1c	t_sync_gear Indicates the time between MRS command and the sync pulse time. This must be even number of clocks. For DDR4-2666 and DDR4-3200, this parameter is defined as tMOD(min)+4nCK tMOD(min) is greater of 24nCK or 15ns 15ns / .625ns = 24 Max value for this register is 24+4 = 28 When the controller is operating in 1:2 mode, program this to (tSYNC_GEAR/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x1c Programming Mode:Quasi-dynamic Group 2, Group 4
15:13	RW	0x0	Reserved1 Reserved Field:Yes
12:8	RW	0x18	t_cmd_gear Indicates a sync pulse to first valid command. For DDR4-2666 and DDR4-3200, this parameter is defined as tMOD(min) tMOD(min) is greater of 24nCK or 15ns 15ns / .625ns = 24 Max value for this register is 24 When the controller is operating in 1:2 mode, program this to (tCMD_GEAR/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x18 Programming Mode:Quasi-dynamic Group 2, Group 4
7:4	RW	0x0	Reserved0 Reserved Field:Yes
3:2	RW	0x2	t_gear_setup Indicates the geardown setup time. Minimum value of this register is 1. Zero is invalid. For DDR4-2666 and DDR4-3200, this parameter is defined as 2 clks When the controller is operating in 1:2 frequency ratio mode, program this to (tGEAR_setup/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4
1:0	RW	0x2	t_gear_hold Indicates the geardown hold time. Minimum value of this register is 1. Zero is invalid. For DDR4-2666 and DDR4-3200, this parameter is defined as 2 clks When the controller is operating in 1:2 frequency ratio mode, program this to (tGEAR_hold/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ1_DRAMTMG11

Address: Operational Base(0xFF4E0000) + offset (0x212C)

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Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved3 Reserved Field:Yes
30:24	RW	0x44	post_mpsm_gap_x32 tXMPDLL: This is the minimum Exit MPSM to commands requiring a locked DLL. When the controller is operating in 1:2 frequency ratio mode, program this to (tXMPDLL/2) and round it up to the next integer value. Present only in designs configured to support DDR4. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x44 Programming Mode:Quasi-dynamic Group 2, Group 4
23:21	RW	0x0	Reserved2 Reserved Field:Yes
20:16	RW	0x0c	t_mpx_lh tMPX_LH: This is the minimum CS_n Low hold time to CKE rising edge. When the controller is operating in 1:2 frequency ratio mode, program this to RoundUp(tMPX_LH/2)+1. Present only in designs configured to support DDR4. Unit: DFI clock cycles. Value After Reset:0xc Programming Mode:Quasi-dynamic Group 2, Group 4
15:10	RW	0x00	Reserved1 Reserved Field:Yes
9:8	RW	0x2	t_mpx_s tMPX_S: This is the minimum time CS setup time to CKE. When the controller is operating in 1:2 frequency ratio mode, program this to (tMPX_S/2) and round it up to the next integer value. Present only in designs configured to support DDR4. Unit: DFI clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4:0	RW	0x1c	t_ckmpe tCKMPE: This is the minimum valid clock requirement after MPSM entry. Present only in designs configured to support DDR4. When the controller is operating in 1:2 frequency ratio mode, divide the value calculated using the previous equation by 2, and round it up to next integer. Unit: DFI clock cycles. Value After Reset:0x1c Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ1_DRAMTMG12

Address: Operational Base(0xFF4E0000) + offset (0x2130)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved2 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
29:24	RW	0x1a	t_wr_mpr This bit is used only in DDR4. Cycles between MPR Write and other command. Set this to tMOD + AL (or tMOD + PL + AL if C/A parity is also used). When the controller is operating in 1:2 frequency ratio mode, program this to (tWR_MPR/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x1a Programming Mode:Quasi-dynamic Group 2, Group 4
23:18	RW	0x00	Reserved1 Reserved Field:Yes
17:16	RW	0x2	t_cmdcke tCMDCKE: Indicates the delay from valid command to CKE input LOW. Set this to the larger of tESCKE or tCMDCKE When the controller is operating in 1:2 frequency ratio mode, program this to (max(tESCKE, tCMDCKE)/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4
15:5	RW	0x000	Reserved0 Reserved Field:Yes
4:0	RW	0x10	t_mrd_pda tMRD_PDA: This is the Mode Register Set command cycle time in PDA mode. When the controller is operating in 1:2 frequency ratio mode, program this to (tMRD_PDA/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x10 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ1_DRAMTMG13

Address: Operational Base(0xFF4E0000) + offset (0x2134)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved2 Reserved Field:Yes
30:24	RW	0x1c	odtloff LPDDR4: ODTLoff: This is the latency from CAS-2 command to ODToff reference. When the controller is operating in 1:2 frequency ratio mode, program this to (ODTLoff/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x1c Programming Mode:Quasi-dynamic Group 2, Group 4
23:22	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
21:16	RW	0x20	t_ccd_mw LPDDR4: tCCDMW: This is the minimum time from write or masked write to masked write command for same bank. When the controller is operating in 1:2 frequency ratio mode, program this to (tCCDMW/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x20 Programming Mode:Quasi-dynamic Group 2, Group 4
15:3	RW	0x0000	Reserved0 Reserved Field:Yes
2:0	RW	0x4	t_ppd LPDDR4: tPPD: This is the minimum time from precharge to precharge command. When the controller is operating in 1:2 frequency ratio mode, program this to (tPPD/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ1_DRAMTMG14

Address: Operational Base(0xFF4E0000) + offset (0x2138)

Bit	Attr	Reset Value	Description
31:12	RW	0x00000	Reserved0 Reserved Field:Yes
11:0	RW	0x0a0	t_xsr tXSR: This is the exit self-refresh to any command. When the controller is operating in 1:2 frequency ratio mode, program this to the previous value divided by 2 and round up to next integer value. The value 0xfff is illegal for this register field. Note: Used only for mDDR/LPDDR2/LPDDR3/LPDDR4 mode. Unit: DFI clock cycles. Value After Reset:0xa0 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ1_DRAMTMG15

Address: Operational Base(0xFF4E0000) + offset (0x213C)

Bit	Attr	Reset Value	Description
31	RW	0x0	en_dfi_lp_t_stab 1 - Enable using tSTAB when exiting DFI LP. This must be set when the PHY is stopping the clock during DFI LP to save maximum power. 0 - Disable using tSTAB when exiting DFI LP. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4
30:8	RW	0x000000	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	t_stab_x32 tSTAB: Stabilization time. It is required in the following two cases for DDR3/DDR4 RDIMM: When exiting power saving mode, if the clock is stopped, after re-enabling it the clock must be stable for a time specified by tSTAB In the case of input clock frequency change (DDR4) After issuing control words that refers to clock timing (Specification: 6us for DDR3, 5us for DDR4) Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ1_ZQCTL0

Address: Operational Base(0xFF4E0000) + offset (0x2180)

Bit	Attr	Reset Value	Description
31	RW	0x0	dis_auto_zq 1 - Disable uMCTL2 generation of ZQCS/MPC(ZQ calibration) command. Register DBGCMD.zq_calib_short can be used instead to issue ZQ calibration request from APB module 0 - Internally generate ZQCS/MPC(ZQ calibration) commands based on ZQCTL1.t_zq_short_interval_x1024 This is only present for designs supporting DDR3/DDR4 or LPDDR2/LPDDR3/LPDDR4 devices. Value After Reset:0x0 Programming Mode:Dynamic
30	RW	0x0	dis_srx_zqcl 1 - Disable issuing of ZQCL/MPC(ZQ calibration) command at self-refresh/SR-Powerdown exit. Only applicable when run in DDR3 or DDR4 or LPDDR2 or LPDDR3 or LPDDR4 mode 0 - Enable issuing of ZQCL/MPC(ZQ calibration) command at self-refresh/SR-Powerdown exit. Only applicable when run in DDR3 or DDR4 or LPDDR2 or LPDDR3 or LPDDR4 mode This is only present for designs supporting DDR3/DDR4 or LPDDR2/LPDDR3/LPDDR4 devices. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4
29	RW	0x0	zq_resistor_shared 1 - Denotes that ZQ resistor is shared between ranks. Means ZQinit/ZQCL/ZQCS/MPC(ZQ calibration) commands are sent to one rank at a time with tZQinit/tZQCL/tZQCS/tZQCAL/tZQLAT timing met between commands so that commands to different ranks do not overlap 0 - ZQ resistor is not shared This is only present for designs supporting DDR3/DDR4 or LPDDR2/LPDDR3/LPDDR4 devices. Value After Reset:0x0 Programming Mode:Static

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Bit	Attr	Reset Value	Description
28	RW	0x0	dis_mpsmx_zqcl 1 - Disable issuing of ZQCL command at Maximum Power Saving Mode exit. Only applicable when run in DDR4 mode 0 - Enable issuing of ZQCL command at Maximum Power Saving Mode exit. Only applicable when run in DDR4 mode This is only present for designs supporting DDR4 devices. Note: Do not issue ZQCL command at Maximum Power Save Mode exit if the UMCTL2_SHARED_AC configuration parameter is set. Program it to 1'b1. The software can send ZQCS after exiting MPSM mode. Value After Reset:0x0 Programming Mode:Static
27	RW	0x0	Reserved1 Reserved Field:Yes
26:16	RW	0x200	t_zq_long_nop tZQoper for DDR3/DDR4, tZQCL for LPDDR2/LPDDR3, tZQCAL for LPDDR4: Number of DFI clock cycles of NOP required after a ZQCL (ZQ calibration long)/MPC(ZQ Start) command is issued to SDRAM. When the controller is operating in 1:2 frequency ratio mode: DDR3/DDR4: program this to tZQoper/2 and round it up to the next integer value. LPDDR2/LPDDR3: program this to tZQCL/2 and round it up to the next integer value. LPDDR4: program this to tZQCAL/2 and round it up to the next integer value. This is only present for designs supporting DDR3/DDR4 or LPDDR2/LPDDR3/LPDDR4 devices. Unit: DFI clock cycles. Value After Reset:0x200 Programming Mode:Static
15:10	RW	0x00	Reserved0 Reserved Field:Yes
9:0	RW	0x040	t_zq_short_nop tZQCS for DDR3/DD4/LPDDR2/LPDDR3, tZQLAT for LPDDR4: Number of DFI clock cycles of NOP required after a ZQCS (ZQ calibration short)/MPC(ZQ Latch) command is issued to SDRAM. When the controller is operating in 1:2 frequency ratio mode, program this to tZQCS/2 and round it up to the next integer value. This is only present for designs supporting DDR3/DDR4 or LPDDR2/LPDDR3/LPDDR4 devices. Unit: DFI clock cycles. Value After Reset:0x40 Programming Mode:Static

DDRCTL_FREQ1_DFITMG0

Address: Operational Base(0xFF4E0000) + offset (0x2190)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved2 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
28:24	RW	0x07	dfi_t_ctrl_delay Specifies the number of DFI clock cycles after an assertion or de-assertion of the DFI control signals that the control signals at the PHY-DRAM interface reflect the assertion or de-assertion. If the DFI clock and the memory clock are not phase-aligned, this timing parameter must be rounded up to the next integer value. Note that if using RDIMM/LRDIMM, it is necessary to increment this parameter by RDIMM's/LRDIMM's extra cycle of latency in terms of DFI clock. Unit: DFI clock cycles. Value After Reset:0x7 Programming Mode:Quasi-dynamic Group 4
23	RW	0x0	dfi_rddata_use_dfi_phy_clk Defines whether dfi_rddata_en/dfi_rddata/dfi_rddata_valid is generated using HDR (DFI clock) or SDR (DFI PHY clock) values. Selects whether value in DFITMG0.dfi_t_rddata_en is in terms of HDR (DFI clock) or SDR (DFI PHY clock) cycles: 0 in terms of HDR (DFI clock) cycles 1 in terms of SDR (DFI PHY clock) cycles Refer to PHY specification for correct value. If using a Synopsys DWC DDR3/2 PHY, DWC DDR2/3-Lite/mDDR PHY, DWC DDR multiPHY or DWC Gen2 DDR multiPHY, this field must be set to 0; otherwise: If MEMC_PROG_FREQ_RATIO=1 and MSTR.frequency_ratio=1, this field must be set to 0 Else, it must be set to 1 Value After Reset:0x0 Programming Mode:Static
22:16	RW	0x02	dfi_t_rddata_en Time from the assertion of a read command on the DFI interface to the assertion of the dfi_rddata_en signal. Refer to PHY specification for correct value. This corresponds to the DFI parameter trddata_en. Note that, depending on the PHY, if using RDIMM/LRDIMM, it may be necessary to use the adjusted value of CL in the calculation of trddata_en. This is to compensate for the extra cycles of latency through the RDIMM/LRDIMM. Unit: DFI clock cycles or DFI PHY clock cycles, depending on DFITMG0.dfi_rddata_use_dfi_phy_clk. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 1, Group 4

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Bit	Attr	Reset Value	Description
15	RW	0x0	dfi_wrdata_use_dfi_phy_clk Defines whether dfi_wrdata_en/dfi_wrdata/dfi_wrdata_mask is generated using HDR (DFI clock) or SDR (DFI PHY clock) values. Selects whether value in DFITMG0.dfi_tphy_wrlat is in terms of HDR (DFI clock) or SDR (DFI PHY clock) cycles. Selects whether value in DFITMG0.dfi_tphy_wrdata is in terms of HDR (DFI clock) or SDR (DFI PHY clock) cycles. 0 in terms of HDR (DFI clock) cycles 1 in terms of SDR (DFI PHY clock) cycles Refer to PHY specification for correct value. If using a Synopsys DWC DDR3/2 PHY, DWC DDR2/3-Lite/mDDR PHY, DWC DDR multiPHY or DWC Gen2 DDR multiPHY, this field must be set to 0; otherwise: If MEMC_PROG_FREQ_RATIO=1 and MSTR.frequency_ratio=1, this field must be set to 0 Else, it must be set to 1 Value After Reset:0x0 Programming Mode:Static
14	RW	0x0	Reserved1 Reserved Field:Yes
13:8	RW	0x00	dfi_tphy_wrdata Specifies the number of clock cycles between when dfi_wrdata_en is asserted to when the associated write data is driven on the dfi_wrdata signal. This corresponds to the DFI timing parameter tphy_wrdata. For more information on correct value, see PHY specification. Note, maximum supported value is 8. Unit: DFI clock cycles or DFI PHY clock cycles, depending on DFITMG0.dfi_wrdata_use_dfi_phy_clk. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 4
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5:0	RW	0x02	dfi_tphy_wrlat Write latency. Number of clocks from the write command to write data enable (dfi_wrdata_en). This corresponds to the DFI timing parameter tphy_wrlat. Refer to PHY specification for correct value. Note that, depending on the PHY, if using RDIMM/LRDIMM, it may be necessary to use the adjusted value of CL in the calculation of tphy_wrlat. This is to compensate for the extra cycles of latency through the RDIMM/LRDIMM. For LPDDR4, dfi_tphy_wrlat>60 is not supported. Unit: DFI clock cycles or DFI PHY clock cycles, depending on DFITMG0.dfi_wrdata_use_dfi_phy_clk. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ1_DFITMG1

Address: Operational Base(0xFF4E0000) + offset (0x2194)

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Bit	Attr	Reset Value	Description
31:28	RW	0x0	dfi_t_cmd_lat Specifies the number of DFI PHY clock cycles between when the dfi_cs signal is asserted and when the associated command is driven. This field is used for CAL mode, must be set to '0' or tCAL, which matches the CAL mode register setting in the DRAM. When enabling CAL mode with RDIMM/LRDIMM, this field must be set to tCAL-CLA (Command Latency Adder). For more information on CLA, see JEDEC DDR4 Register Specification. If the PHY can add the latency for CAL mode, this must be set to '0'. Valid Range: 0 to 8. Unit: DFI PHY clock cycles. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4
27:26	RW	0x0	Reserved3 Reserved Field:Yes
25:24	RW	0x0	dfi_t_parin_lat Specifies the number of DFI PHY clock cycles between when the dfi_cs signal is asserted and when the associated dfi_parity_in signal is driven. Unit: DFI PHY clock cycles. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 4
23:21	RW	0x0	Reserved2 Reserved Field:Yes
20:16	RW	0x00	dfi_t_wrdata_delay Specifies the number of DFI clock cycles between when the dfi_wrdata_en signal is asserted and when the corresponding write data transfer is completed on the DRAM bus. This corresponds to the DFI timing parameter twrdata_delay. For more information on correct value, see PHY specification. For DFI 3.0 PHY, set to twrdata_delay, a new timing parameter introduced in DFI 3.0. For DFI 2.1 PHY, set to tphy_wrdata + (delay of DFI write data to the DRAM). Value to be programmed is in terms of DFI clocks, not PHY clocks. In FREQ_RATIO=2, divide PHY's value by 2 and round up to next integer. If using DFITMG0.dfi_wrdata_use_dfi_phy_clk=1, add 1 to the value. Unit: DFI clock cycles. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 4
15:13	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
12:8	RW	0x04	dfi_t_dram_clk_disable Specifies the number of DFI clock cycles from the assertion of the dfi_dram_clk_disable signal on the DFI until the clock to the DRAM memory devices, at the PHY-DRAM boundary, maintains a low value. If the DFI clock and the memory clock are not phase aligned, this timing parameter must be rounded up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 4
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4:0	RW	0x04	dfi_t_dram_clk_enable Specifies the number of DFI clock cycles from the de-assertion of the dfi_dram_clk_disable signal on the DFI until the first valid rising edge of the clock to the DRAM memory devices, at the PHY-DRAM boundary. If the DFI clock and the memory clock are not phase aligned, this timing parameter must be rounded up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 4

DDRCTL_FREQ1_DFITMG2

Address: Operational Base(0xFF4E0000) + offset (0x21B4)

Bit	Attr	Reset Value	Description
31:15	RW	0x00000	Reserved1 Reserved Field:Yes
14:8	RW	0x02	dfi_tphy_rdcslat specifies the number of DFI PHY clock cycles between when a read command is sent on the DFI control interface and when the associated dfi_rddata_cs signal is asserted. This corresponds to the DFI timing parameter tphy_rdcslat. Refer to PHY specification for correct value. Unit: DFI PHY clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5:0	RW	0x02	dfi_tphy_wrcslat Specifies the number of DFI PHY clock cycles between when a write command is sent on the DFI control interface and when the associated dfi_wrdata_cs signal is asserted. This corresponds to the DFI timing parameter tphy_wrcslat. For more information on correct value, see PHY specification. Unit: DFI PHY clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ1_DFITMG3

Address: Operational Base(0xFF4E0000) + offset (0x21B8)

Bit	Attr	Reset Value	Description
31:5	RW	0x0000000	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
4:0	RW	0x00	dfi_t_geardown_delay The delay from dfi_geardown_en assertion to the time of the PHY being ready to receive commands. Refer to PHY specification for correct value. When the controller is operating in 1:2 frequency ratio mode, program this to (tgeardown_delay/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x0 Programming Mode:Static

DDRCTL_FREQ1_ODTCFG

Address: Operational Base(0xFF4E0000) + offset (0x2240)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved4 Reserved Field:Yes
27:24	RW	0x4	wr_odt_hold DFI PHY clock cycles to hold ODT for a write command. The minimum supported value is 2. Recommended values: DDR2: BL8 - 0x5 (DDR2-400/533/667), 0x6 (DDR2-800), 0x7 (DDR2-1066) BL4 - 0x3 (DDR2-400/533/667), 0x4 (DDR2-800), 0x5 (DDR2-1066) DDR3: BL8 - 0x6 DDR4: BL8 - 5 + WR_PREAMBLE + CRC_MODE WR_PREAMBLE = 1 (1tCK write preamble), 2 (2tCK write preamble) CRC_MODE = 0 (not CRC mode), 1 (CRC mode) LPDDR3: BL8 - 7 + RU(tODTon(max)/tCK) Unit: DFI PHY clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 1, Group 4
23:21	RW	0x0	Reserved3 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
20:16	RW	0x00	wr_odt_delay Indicates the delay, in DFI PHY clock cycles, from issuing a write command to setting ODT values associated with that command. ODT setting must remain constant for the entire time that DQS is driven by the uMCTL2. Recommended values: DDR2: CWL + AL - 3 (DDR2-400/533/667), CWL + AL - 4 (DDR2-800), CWL + AL - 5 (DDR2-1066) If (CWL + AL - 3 < 0), uMCTL2 does not support ODT for write operation. DDR3: 0x0 DDR4: DFITMG1.dfi_t_cmd_lat (to adjust for CAL mode) LPDDR3: WL - 1 - RU(tODTon(max)/tCK)) Unit: DFI PHY clock cycles. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 1, Group 4
15:12	RW	0x0	Reserved2 Reserved Field:Yes
11:8	RW	0x4	rd_odt_hold DFI PHY clock cycles to hold ODT for a read command. The minimum supported value is 2. Recommended values: DDR2: BL8 - 0x6 (not DDR2-1066), 0x7 (DDR2-1066) BL4 - 0x4 (not DDR2-1066), 0x5 (DDR2-1066) DDR3: BL8 - 0x6 DDR4: BL8 - 5 + RD_PREAMBLE RD_PREAMBLE = 1 (1tCK read preamble), 2 (2tCK read preamble) LPDDR3: BL8 - 5 + RU(tDQSCK(max)/tCK) - RD(tDQSCK(min)/tCK) + RU(tODTon(max)/tCK) Unit: DFI PHY clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 1, Group 4
7	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
6:2	RW	0x00	rd_odt_delay Indicates the delay, in DFI PHY clock cycles, from issuing a read command to setting ODT values associated with that command. ODT setting must remain constant for the entire time that DQS is driven by the uMCTL2. Recommended values: DDR2: CL + AL - 4 (not DDR2-1066), CL + AL - 5 (DDR2-1066) If (CL + AL - 4 < 0), uMCTL2 does not support ODT for read operation. DDR3: CL - CWL DDR4: CL - CWL - RD_PREAMBLE + WR_PREAMBLE + DFITMG1.dfi_t_cmd_lat (to adjust for CAL mode) WR_PREAMBLE = 1 (1tCK write preamble), 2 (2tCK write preamble) LPDDR3: RL + RD(tDQSCK(min)/tCK) - 1 - RU(tODTon(max)/tCK) Unit: DFI PHY clock cycles. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 1, Group 4
1:0	RW	0x0	Reserved0 Reserved Field:Yes

DDRCTL_FREQ2_DERATEEN

Address: Operational Base(0xFF4E0000) + offset (0x3020)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	Reserved2 Reserved Field:Yes
13	RW	0x0	derate_mr4_pause_fc Pauses MR4 reads. Must only be set to 1 as part of Frequency Change procedures, if DERATEEN.derate_enable=1 Value After Reset:0x0 Programming Mode:Dynamic
12	RW	0x0	derate_mr4_tuf_dis Disables use of MR4 TUF flag (MR4[7]) bit. 0 - Use MR4 TUF flag (MR4[7]) 1 - Do not use MR4 TUF Flag (MR4[7]) For LPDDR4, it is recommended to set this register to 1. For LPDDR2 and LPDDR3, contact your memory vendor for recommended usage. This affects both the periodic derate logic (DERATEEN.derate_enable) and the derate_temp_limit_intr. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4
11	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
10:8	RW	0x0	rc_derate_value Derate value of tRC for LPDDR4. 0 - Derating uses +1 1 - Derating uses +2 2 - Derating uses +3 3 - Derating uses +4 4 - Derating uses +5 5 - Derating uses +6 6 - Derating uses +7 7 - Derating uses +8 Present only in designs configured to support LPDDR4. The required cycles for derating can be determined by dividing 3.75ns by the core_ddrc_core_clk period, and rounding it up to the next integer. Hence this register field must be set to the previous value - 1. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4
7:4	RW	0x0	derate_byte This bit indicates which byte of the MRR data is used for derating. The maximum valid value depends on MEMC_DRAM_TOTAL_DATA_WIDTH. Present only in designs configured to support LPDDR2/LPDDR3/LPDDR4. Value After Reset:0x0 Programming Mode:Static
3	RW	0x0	Reserved0 Reserved Field:Yes
2:1	RW	0x0	derate_value Derate value. 0 - Derating uses +1 1 - Derating uses +2 2 - Derating uses +3 3 - Derating uses +4 Present only in designs configured to support LPDDR2/LPDDR3/LPDDR4. The required cycles for derating can be determined by dividing 1.875ns by the core_ddrc_core_clk period, and rounding it up to the next integer. Hence this register field must be set to the previous value - 1. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4
0	RW	0x0	derate_enable Enables derating. 0 - Timing parameter derating is disabled 1 - Timing parameter derating is enabled using MR4 read value Present only in designs configured to support LPDDR2/LPDDR3/LPDDR4. This field must be set to '0' for non-LPDDR2/LPDDR3/LPDDR4 mode. Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_FREQ2_DERATEINT

Address: Operational Base(0xFF4E0000) + offset (0x3024)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00800000	mr4_read_interval Interval between two MR4 reads, used to derate the timing parameters. Present only in designs configured to support LPDDR2/LPDDR3/LPDDR4. This register must not be set to zero. Unit: DFI clock cycles. Value After Reset:0x800000 Programming Mode:Static

DDRCTL_FREQ2_PWRTMG

Address: Operational Base(0xFF4E0000) + offset (0x3034)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x40	selfref_to_x32 After this many clocks of the DDRC command channel being idle the uMCTL2 automatically puts the SDRAM into self-refresh. The DDRC command channel is considered idle when there are no HIF commands outstanding. This must be enabled in the PWRCTL.selfref_en. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x40 Programming Mode:Quasi-dynamic Group 4
15:8	RW	0x20	t_dpd_x4096 Minimum deep power-down time. For mDDR, value from the JEDEC specification is 0 as mDDR exits from deep power-down mode immediately after PWRCTL.deeppowerdown_en is de-asserted. For LPDDR2/LPDDR3, value from the JEDEC specification is 500us. Present only in designs configured to support mDDR, LPDDR2 or LPDDR3. FOR PERFORMANCE ONLY. Unit: Multiples of 4096 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x20 Programming Mode:Quasi-dynamic Group 4
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4:0	RW	0x10	powerdown_to_x32 After this many clocks of the DDRC command channel being idle the uMCTL2 automatically puts the SDRAM into power-down. The DDRC command channel is considered idle when there are no HIF commands outstanding. This must be enabled in the PWRCTL.powerdown_en. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x10 Programming Mode:Quasi-dynamic Group 4

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DDRCTL_FREQ2_RFSHCTL0

Address: Operational Base(0xFF4E0000) + offset (0x3050)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved4 Reserved Field:Yes
23:20	RW	0x2	refresh_margin Threshold value in number of DFI clock cycles before the critical refresh or page timer expires. A critical refresh is to be issued before this threshold is reached. It is recommended that this not be changed from the default value, currently shown as 0x2. It must always be less than internally used t_rfc_nom/32. Note that internally used t_rfc_nom is equal to RFSHTMG.t_rfc_nom_x1_x32 * 32 if RFSHTMG.t_rfc_nom_x1_sel=0. If RFSHTMG.t_rfc_nom_x1_sel=1 (for LPDDR2/LPDDR3/LPDDR4 per-bank refresh only), internally used t_rfc_nom is equal to RFSHTMG.t_rfc_nom_x1_x32. Note that, in LPDDR2/LPDDR3/LPDDR4, internally used t_rfc_nom may be divided by four if derating is enabled (DERATEEN.derate_enable=1). Unit: Multiples of 32 DFI clock cycles. Value After Reset:0x2 Programming Mode:Dynamic - Refresh Related
19:17	RW	0x0	Reserved3 Reserved Field:Yes
16:12	RW	0x10	refresh_to_x1_x32 If the refresh timer (tRFCnom, also known as tREFI) has expired at least once, then a speculative refresh may be performed. A speculative refresh is a refresh performed at a time when refresh would be useful. When the SDRAM bus is idle for a period of time determined by this RFSHCTL0.refresh_to_x1_x32 and the refresh timer has expired at least once since the last refresh, then a speculative refresh is performed. Speculative refreshes continues successively until there are no refreshes pending or until new reads or writes are issued to the uMCTL2. FOR PERFORMANCE ONLY. Unit: DFI clock cycles or multiples of 32 DFI clock cycles, depending on RFSHTMG.t_rfc_nom_x1_sel. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x10 Programming Mode:Dynamic - Refresh Related
11:10	RW	0x0	Reserved2 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
9:4	RW	0x00	refresh_burst The programmed value + 1 is the number of refresh timeouts that is allowed to accumulate before traffic is blocked and the refreshes are forced to execute. Closing pages to perform a refresh is a one-time penalty that must be paid for each group of refreshes. Therefore, performing refreshes in a burst reduces the per-refresh penalty of these page closings. Higher numbers for RFSHCTL.refresh_burst slightly increases utilization; lower numbers decreases the worst-case latency associated with refreshes. 0 - Single refresh 1 - Burst-of-2 refresh 7 - Burst-of-8 refresh For more information on burst refresh feature, see section 3.9 of DDR2 JEDEC specification - JESD79-2F.pdf. For DDR2/3, the refresh is always per-rank and not per-bank. The rank refresh can be accumulated over 8*tREFI cycles using the burst refresh feature. In DDR4 mode, according to Fine Granularity feature, 8 refreshes can be postponed in 1X mode, 16 refreshes in 2X mode and 32 refreshes in 4X mode. If using PHY-initiated updates, care must be taken in the setting of RFSHCTL0.refresh_burst, to ensure that tRFCmax is not violated due to a PHY-initiated update occurring shortly before a refresh burst is due. In this situation, the refresh burst is delayed until the PHY-initiated update is complete. In per-bank refresh mode of LPDDR2/LPDDR3/LPDDR4 (RFSHCTL0.per_bank_refresh = 1), 64 refreshes can be postponed. Value After Reset:0x0 Programming Mode:Dynamic - Refresh Related
3	RW	0x0	Reserved1 Reserved Field:Yes
2	RW	0x0	per_bank_refresh 1 - Per bank refresh 0 - All bank refresh Per bank refresh allows traffic to flow to other banks. Per bank refresh is not supported by all LPDDR2 devices but must be supported by all LPDDR3/LPDDR4 devices. Present only in designs configured to support LPDDR2/LPDDR3/LPDDR4. Value After Reset:0x0 Programming Mode:Static
1:0	RW	0x0	Reserved0 Reserved Field:Yes

DDRCTL_FREQ2_RFSHTMG

Address: Operational Base(0xFF4E0000) + offset (0x3064)

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Bit	Attr	Reset Value	Description
31	RW	0x0	t_rfc_nom_x1_sel Specifies whether the RFSHTMG.t_rfc_nom_x1_x32 and RFSHCTL0.refresh_to_x1_x32 register values are x1 or x32. 0 - x32 register values are used 1 - x1 register values are used This applies only when per-bank refresh is enabled (RFSHCTL0.per_bank_refresh=1); if per-bank refresh is not enabled, the x32 register values are used and this register field is ignored. This register field does not exist for configurations which do not support LPDDR2/3/4. For such configurations, the value of this register field can be assumed to be 0, so that RFSHTMG.t_rfc_nom_x1_x32 and RFSHCTL0.refresh_t_x1_x32 are interpreted as x32 register fields Value After Reset:0x0 Programming Mode:Dynamic - Refresh Related
30:28	RW	0x0	Reserved1 Reserved Field:Yes
27:16	RW	0x062	t_rfc_nom_x1_x32 Average time interval between refreshes per rank (Specification: 7.8us for DDR2, DDR3 and DDR4. See JEDEC specification for mDDR, LPDDR2, LPDDR3 and LPDDR4). When the controller is operating in 1:1 mode, set this register to RoundDown(tREFI/tCK) When the controller is operating in 1:2 mode, set this register to RoundDown(RoundDown(tREFI/tCK)/2) In both the previous cases, if RFSHTMG.t_rfc_nom_x1_sel = 0, divide the previous result by 32 and round down. For LPDDR2/LPDDR3/LPDDR4: If using all-bank refreshes (RFSHCTL0.per_bank_refresh = 0), use tREFIab in the previous calculations If using per-bank refreshes (RFSHCTL0.per_bank_refresh = 1), use tREFIpb in the previous calculations For DDR4 mode, tREFI value is different depending on the refresh mode. You must program appropriate value from the spec based on the value programmed in the refresh mode register. Note: RFSHTMG.t_rfc_nom_x1_x32 must be greater than 0x1 If RFSHTMG.t_rfc_nom_x1_sel == 1, RFSHTMG.t_rfc_nom_x1_x32 must be greater than RFSHTMG.t_rfc_min If RFSHTMG.t_rfc_nom_x1_sel == 0, RFSHTMG.t_rfc_nom_x1_x32 * 32 must be greater than RFSHTMG.t_rfc_min In non-DDR4 or DDR4 Fixed 1x mode: RFSHTMG.t_rfc_nom_x1_x32 must be less than or equal to 0xFFE In DDR4 Fixed 2x mode: RFSHTMG.t_rfc_nom_x1_x32 must be less than or equal to 0x7FF In DDR4 Fixed 4x mode: RFSHTMG.t_rfc_nom_x1_x32 must be less than or equal to 0x3FF Unit: DFI clock cycles or multiples of 32 DFI clock cycles, depending on RFSHTMG.t_rfc_nom_x1_sel. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x62 Programming Mode:Dynamic - Refresh Related

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Bit	Attr	Reset Value	Description
15	RW	0x0	lpddr3_trefbw_en Used only when LPDDR3 memory type is connected. Must only be changed when uMCTL2 is in reset. Specifies whether to use the tREFBW parameter (required by some LPDDR3 devices which comply with earlier versions of the LPDDR3 JEDEC specification) or not: 0 - tREFBW parameter not used 1 - tREFBW parameter used Value After Reset:0x0 Programming Mode:Static
14:10	RW	0x00	Reserved0 Reserved Field:Yes
9:0	RW	0x08c	t_rfc_min tRFC (min): Minimum time from refresh to refresh or activate. When the controller is operating in 1:1 mode, t_rfc_min must be set to RoundUp(tRFCmin/tCK). When the controller is operating in 1:2 mode, t_rfc_min must be set to RoundUp(RoundUp(tRFCmin/tCK)/2). In LPDDR2/LPDDR3/LPDDR4 mode: If using all-bank refreshes, the tRFCmin value in the previous equations is equal to tRFCab If using per-bank refreshes, the tRFCmin value in the previous equations is equal to tRFCpb In DDR4 mode, the tRFCmin value in the previous equations is different depending on the refresh mode (fixed 1X,2X,4X) and the device density. You must program the appropriate value from the spec based on the 'refresh_mode' and the device density that is used. Unit: DFI clock cycles. Value After Reset:0x8c Programming Mode:Dynamic - Refresh Related

DDRCTL_FREQ2_RFSHTMG1

Address: Operational Base(0xFF4E0000) + offset (0x3068)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x8c	t_pbr2pbr LPDDR4:tpbR2pbR. Per-bank refresh to Per-bank refresh different bank Time. When the controller is operating in 1:1 frequency ratio mode, program this to RoundUp(tpbR2pbR/tCK). When the controller is operating in 1:2 frequency ratio mode, program this to RoundUp(RoundUp(tpbR2pbR/tCK)/2). The tpbR2pbR value in the previous equations is different depending on the device density. You must program the appropriate value from the specification. Register is valid only in LPDDR4 per-bank refresh mode (RFSHCTL0.per_bank_refresh_mode == 1). Value After Reset:0x8c Programming Mode:Dynamic - Refresh Related
15:0	RW	0x0000	Reserved0 Reserved Field:Yes

DDRCTL_FREQ2_INIT3

Address: Operational Base(0xFF4E0000) + offset (0x30DC)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr DDR2:Indicates the value to write to MR register. Bit 8 is for DLL and the setting here is ignored. The uMCTL2 sets this bit appropriately. DDR3/DDR4: Value loaded into MR0 register. mDDR: Value to write to MR register. LPDDR2/LPDDR3/LPDDR4 - Value to write to MR1 register Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 1, Group 4
15:0	RW	0x0510	emr DDR2: Indicates the value to write to EMR register. Bits 9:7 are for OCD and the setting in this register is ignored. The uMCTL2 sets those bits appropriately. DDR3/DDR4: Value to write to MR1 register Set bit 7 to 0. mDDR: Value to write to EMR register. LPDDR2/LPDDR3/LPDDR4 - Value to write to MR2 register. Value After Reset:0x510 Programming Mode:Quasi-dynamic Group 4

DDRCTL_FREQ2_INIT4

Address: Operational Base(0xFF4E0000) + offset (0x30E0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	emr2 DDR2: Indicates the value to write to EMR2 register. DDR3/DDR4: Value to write to MR2 register. LPDDR2/LPDDR3/LPDDR4: Value to write to MR3 register. mDDR: Unused. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 4
15:0	RW	0x0000	emr3 DDR2: Indicates the value to write to EMR3 register. DDR3/DDR4: Value to write to MR3 register. mDDR/LPDDR2/LPDDR3: Unused. LPDDR4: Value to write to MR13 register. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ2_INIT6

Address: Operational Base(0xFF4E0000) + offset (0x30E8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr4 DDR4 - Indicates the value to be loaded into SDRAM MR4 registers. LPDDR4- Value to be loaded into SDRAM MR11 registers. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4
15:0	RW	0x0000	mr5 DDR4 - Indicates the value to be loaded into SDRAM MR5 registers. LPDDR4- Value to be loaded into SDRAM MR12 registers. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 1, Group 4

DDRCTL_FREQ2_INIT7

Address: Operational Base(0xFF4E0000) + offset (0x30EC)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr22 LPDDR4 - Indicates the value to be loaded into SDRAM MR22 registers. Used in LPDDR4 designs only. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 4
15:0	RW	0x0000	mr6 DDR4 - Indicates the value to be loaded into SDRAM MR6 registers. LPDDR4- Value to be loaded into SDRAM MR14 registers. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 4

DDRCTL_FREQ2_RANKCTL

Address: Operational Base(0xFF4E0000) + offset (0x30F4)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	Reserved2 Reserved Field:Yes
26	RW	0x0	diff_rank_wr_gap_msb Only present for multi-rank configurations. 1-bit extension to be used when RANKCTL.diff_rank_wr_gap field needs to be set to a value greater than 0xF. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2
25	RW	0x0	Reserved1 Reserved Field:Yes
24	RW	0x0	diff_rank_rd_gap_msb Only present for multi-rank configurations. 1-bit extension to be used when RANKCTL.diff_rank_rd_gap field needs to be set to a value greater than 0xF. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2
23:16	RW	0x00	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
15:12	RW	0x0	max_rank_wr Only present for multi-rank configurations. Background: Writes to the same rank can be performed back-to-back. Writes to different ranks require additional gap dictated by the register RANKCTL.diff_rank_wr_gap. This is to avoid possible data bus contention as well as to give PHY enough time to switch the delay when changing ranks. The uMCTL2 arbitrates for bus access on a cycle-by-cycle basis; therefore after a write is scheduled, there are few clock cycles (determined by the value on RANKCTL.diff_rank_wr_gap register) in which only writes from the same rank are eligible to be scheduled. This prevents writes from other ranks from having fair access to the data bus. This parameter represents the maximum number of writes that can be scheduled consecutively to the same rank. After this number is reached, a delay equal to RANKCTL.diff_rank_wr_gap is inserted by the scheduler to allow all ranks a fair opportunity to be scheduled. Higher numbers increase bandwidth utilization, lower numbers increase fairness. This feature can be DISABLED by setting this register to 0. When set to 0, the controller stays on the same rank as long as commands are available for it. Minimum programmable value is 0 (feature disabled) and maximum programmable value is 0xF. For uPCTL2, this register field must be set to 0 (feature disabled) FOR PERFORMANCE ONLY. Value After Reset:0x0 Programming Mode:Static

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Bit	Attr	Reset Value	Description
11:8	RW	0x6	diff_rank_wr_gap Only present for multi-rank configurations. Indicates the number of clocks of gap in data responses when performing consecutive writes to different ranks. This is used to switch the delays in the PHY to match the rank requirements. This value must consider both PHY requirement and ODT requirement. PHY requirement - tphy_wrcsgap (For more information on value of tphy_wrcsgap, see PHY databook) ODT requirement - The value programmed in this register takes care of the ODT switch off timing requirement when switching ranks during writes. For LPDDR4, with DQ ODT enabled, diff_rank_wr_gap must be a minimum of ODTLoff - ODTLon - BL/2 + 1 For other cases, diff_rank_wr_gap must be a minimum of ODTCFG.wr_odt_hold - BL/2 When the controller is operating in 1:1 mode, program this to the larger of PHY requirement or ODT requirement. If CRC is enabled, the value can be decreased by 2 because the programmed value is internally increased by 1 (it is always 2 in terms of DFI PHY clock cycle as CRC is supported only with 1:2 frequency ratio). When the controller is operating in 1:2 mode, program this to the larger value divided by two and round it up to the next integer. After PHY has completed training the value programmed may need to be increased. For more information, see relevant PHY documentation. Note that, if using DDR4-LRDIMM, refer to TWRWR timing requirements in JEDEC DDR4 Data Buffer (DDR4DB01) Specification. If a value greater than 0xF is needed, the RANKCTL.diff_rank_wr_gap_msb field must be used as extension. For DFI 1:2 mode, a maximum value of {diff_rank_wr_gap_msb,diff_rank_wr_gap} < 'h11 is supported. For DFI 1:1 mode a maximum value of {diff_rank_wr_gap_msb,diff_rank_wr_gap} <= 'h1F is supported. Unit: DFI clock cycles. Value After Reset:0x6 Programming Mode:Quasi-dynamic Group 2
7:4	RW	0x6	diff_rank_rd_gap Only present for multi-rank configurations. Indicates the number of clocks of gap in data responses when performing consecutive reads to different ranks. This is used to switch the delays in the PHY to match the rank requirements. This value must consider both PHY requirement and ODT requirement. PHY requirement:tphy_rdcsgap (For more information on value of tphy_rdcsgap, see PHY databook) ODT requirement: The value programmed in this register takes care of the ODT switch off timing requirement when switching ranks during reads: Value After Reset:0x6 Programming Mode:Quasi-dynamic Group 2

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	max_rank_rd Only present for multi-rank configurations. Background: Reads to the same rank can be performed back-to-back. Reads to different ranks require additional gap dictated by the register RANKCTL.diff_rank_rd_gap. This is to avoid possible data bus contention as well as to give PHY enough time to switch the delay when changing ranks. The uMCTL2 arbitrates for bus access on a cycle-by-cycle basis; therefore after a read is scheduled, there are few clock cycles (determined by the value on RANKCTL.diff_rank_rd_gap register) in which only reads from the same rank are eligible to be scheduled. This prevents reads from other ranks from having fair access to the data bus. This parameter represents the maximum number of reads that can be scheduled consecutively to the same rank. After this number is reached, a delay equal to RANKCTL.diff_rank_rd_gap is inserted by the scheduler to allow all ranks a fair opportunity to be scheduled. Higher numbers increase bandwidth utilization, lower numbers increase fairness. This feature can be DISABLED by setting this register to 0. When set to 0, the controller stays on the same rank as long as commands are available for it. Minimum programmable value is 0 (feature disabled) and maximum programmable value is 0xF. For uPCTL2, this register field must be set to 0 (feature disabled) FOR PERFORMANCE ONLY. Value After Reset:0x0 Programming Mode:Static

DDRCTL_FREQ2_DRAMTMG0

Address: Operational Base(0xFF4E0000) + offset (0x3100)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved3 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
30:24	RW	0x0f	wr2pre Specifies the minimum time between write and precharge to same bank. Specifications: WL + BL/2 + tWR = approximately 8 cycles + 15 ns = 14 clocks @400MHz and less for lower frequencies. where: WL: Write latency BL: Burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM. BST (burst terminate) is not supported at present tWR: Write recovery time. This comes directly from the SDRAM specification Add one extra cycle for LPDDR2/LPDDR3/LPDDR4 for this parameter. When the controller is operating in 1:2 frequency ratio mode, 1T mode, divide the previous value by 2. No rounding up. When the controller is operating in 1:2 frequency ratio mode, 2T mode, geardown mode or LPDDR4 mode, divide the previous value by 2 and round it up to the next integer value. Note that, depending on the PHY, if using LRDIMM, it may be necessary to adjust the value of this parameter to compensate for the extra cycle of latency through the LRDIMM. For DDR4, LPDDR4, LPDDR3, using nWR(WR) instead of tWR to calculate the value of this parameter. Unit: DFI clock cycles. Value After Reset:0xf Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
23:22	RW	0x0	Reserved2 Reserved Field:Yes
21:16	RW	0x10	t_faw tFAW - valid only when 8 or more banks(or banks x bank groups) are present. In 8-bank design, at most 4 banks must be activated in a rolling window of tFAW cycles. When the controller is operating in 1:2 frequency ratio mode, program this to (tFAW/2) and round up to next integer value. In a 4-bank design, set this register to 0x1 independent of the 1:1/1:2 frequency mode. Unit: DFI clock cycles. Value After Reset:0x10 Programming Mode:Quasi-dynamic Group 2, Group 4
15	RW	0x0	Reserved1 Reserved Field:Yes
14:8	RW	0x1b	t_ras_max tRAS(max) - Specifies the maximum time between activate and precharge to same bank. This is the maximum time that a page can be kept open Minimum value of this register is 1. Zero is invalid. When the controller is operating in 1:1 frequency ratio mode, t_ras_max must be set to RoundDown(tRAS(max)/tCK/1024). When the controller is operating in 1:2 frequency ratio mode, t_ras_max must be set to RoundDown((RoundDown(tRAS(max)/tCK/1024)-1)/2). Unit: Multiples of 1024 DFI clock cycles. Value After Reset:0x1b Programming Mode:Quasi-dynamic Group 2, Group 4

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Bit	Attr	Reset Value	Description
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5:0	RW	0x0f	t_ras_min tRAS(min) - Specifies the minimum time between activate and precharge to the same bank. When the controller is operating in 1:1 frequency ratio mode, t_ras_min must be set to RoundUp(tRASmin/tCK) When the controller is operating in 1:2 frequency ratio mode, 1T mode, t_ras_min must be set to RoundDown(RoundUp(tRASmin/tCK)/2) When the controller is operating in 1:2 frequency ratio mode, 2T mode, geardown mode or LPDDR4 mode, t_ras min must be set to RoundUp(RoundUp(tRASmin/tCK)/2) Unit: DFI clock cycles. Value After Reset:0xf Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ2_DRAMTMG1

Address: Operational Base(0xFF4E0000) + offset (0x3104)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved2 Reserved Field:Yes
20:16	RW	0x08	t_xp tXP - Specifies the minimum time after power-down exit to any operation. For DDR3, this must be programmed to tXPDLL if slow powerdown exit is selected in MR0[12]. If C/A parity for DDR4 is used, set to (tXP+PL) instead. If LPDDR4 is selected and its spec has tCKELPD parameter, set to the larger of tXP and tCKELPD instead. When the controller is operating in 1:2 frequency ratio mode, program this to (tXP/2) and round it up to the next integer value. Units: DFI clock cycles. Value After Reset:0x8 Programming Mode:Quasi-dynamic Group 2, Group 4
15:14	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
13:8	RW	0x04	rd2pre tRTP - Specifies the minimum time from read to precharge of same bank. DDR2 - tAL + BL/2 + max(RoundUp(tRTP/tCK), 2) - 2 DDR3 - tAL + max (RoundUp(tRTP/tCK), 4) DDR4 - Max of following two equations: tAL + max (RoundUp(tRTP/tCK), 4) or, RL + BL/2 - tRP (*). mDDR - BL/2 LPDDR2 - Depends on if it is LPDDR2-S2 or LPDDR2-S4: LPDDR2-S2: BL/2 + RoundUp(tRTP/tCK) - 1. LPDDR2-S4: BL/2 + max(RoundUp(tRTP/tCK),2) - 2. LPDDR3 - BL/2 + max(RoundUp(tRTP/tCK),4) - 4 LPDDR4 - BL/2 + max(RoundUp(tRTP/tCK),8) - 8 (*) When both DDR4 SDRAM and ST-MRAM are used simultaneously, use SDRAM's tRP value for calculation. When the controller is operating in 1:2 mode, 1T mode, divide the previous value by 2. No rounding up. When the controller is operating in 1:2 mode, 2T mode, geardown mode or LPDDR4 mode, divide the previous value by 2 and round it up to the next integer value. For DDR4, using RTP instead of tRTP to calculate the value of this parameter. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
7	RW	0x0	Reserved0 Reserved Field:Yes
6:0	RW	0x14	t_rc tRC - Specifies the minimum time between activates to same bank. When the controller is operating in 1:2 frequency ratio mode, program this to (tRC/2) and round up to next integer value. Unit: DFI clock cycles. Value After Reset:0x14 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ2_DRAMTMG2

Address: Operational Base(0xFF4E0000) + offset (0x3108)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved3 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
29:24	RW	0x03	write_latency Set this field to WL. Indicates the Time from write command to write data on SDRAM interface. This must be set to WL. For mDDR, it must be set to 1. Note that, depending on the PHY, if using RDIMM/LRDIMM, it might be necessary to adjust the value of WL to compensate for the extra cycle of latency through the RDIMM/LRDIMM. When the controller is operating in 1:2 frequency ratio mode, divide the value calculated using the previous equation by 2, and round it up to next integer. This register field is not required for DDR2 and DDR3, as the DFI read and write latencies defined in DFITMG0 and DFITMG1 are sufficient for those protocols For all protocols, in addition to programming this register field, it is necessary to program DFITMG0 and DFITMG1 to control the read and write latencies Unit: DFI clock cycles. Value After Reset:0x3 Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
23:22	RW	0x0	Reserved2 Reserved Field:Yes
21:16	RW	0x05	read_latency Set this field to RL. Indicates the time from read command to read data on SDRAM interface. This must be set to RL. Note that, depending on the PHY, if using RDIMM/LRDIMM, it might be necessary to adjust the value of RL to compensate for the extra cycle of latency through the RDIMM/LRDIMM. When the controller is operating in 1:2 frequency ratio mode, divide the value calculated using the previous equation by 2, and round it up to next integer. This register field is not required for DDR2 and DDR3, as the DFI read and write latencies defined in DFITMG0 and DFITMG1 are sufficient for those protocols For all protocols, in addition to programming this register field, it is necessary to program DFITMG0 and DFITMG1 to control the read and write latencies Unit: DFI clock cycles. Value After Reset:0x5 Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
15:14	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
13:8	RW	0x06	rd2wr Minimum time from read command to write command. This must include time for bus turnaround (both within ranks and between ranks) and all PHY and system requirements. After the PHY has completed training, the value programmed may need to be increased. Please see the relevant PHY databook for details of what should be included here. The following calculations are minimum values, and do not include the PHY/system requirements mentioned above: DDR2/3/mDDR: RL + BL/2 + 2 - WL DDR4: RL + BL/2 + 1 + WR_PREAMBLE - WL LPDDR2/LPDDR3: RL + BL/2 + RU(tDQSCKmax/tCK) + 1 - WL LPDDR4(DQ ODT is Disabled): RL + BL/2 + RU(tDQSCKmax/tCK) + WR_PREAMBLE + RD_POSTAMBLE - WL LPDDR4(DQ ODT is Enabled): RL + BL/2 + RU(tDQSCKmax/tCK) + RD_POSTAMBLE - ODTLon - RU(tODTon(min)/tCK) + 1 Where: WL: Write latency BL: Burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM RL: Read latency = CAS latency WR_PREAMBLE: 1 (1tCK write preamble), 2 (2tCK write preamble). This is unique to DDR4 and LPDDR4 RD_POSTAMBLE: 0.5 (0.5tCK read postamble), 1.5 (1.5tCK read postamble). This is unique to LPDDR4 For LPDDR2/LPDDR3/LPDDR4, if derating is enabled (DERATEEN.derate_enable=1), derated tDQSCKmax must be used. When the controller is operating in 1:2 frequency ratio mode, divide the value calculated using the previous equation by 2, and round it up to next integer. Note that, depending on the PHY, if using LRDIMM, it may be necessary to adjust the value of this parameter to compensate for the extra cycle of latency through the LRDIMM. Unit: DFI clock cycles. Value After Reset:0x6 Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
7:6	RW	0x0	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
5:0	RW	0x0d	wr2rd In DDR4, minimum time from write command to read command for same bank group. In other protoocls, minimum time from write command to read command. This must include time for bus turn-around and all PHY and system requirements. After the PHY has completed training, the value programmed may need to be increased. Please see the relevant PHY databook for details of what should be included here. The following calculations are minimum values, and do not include the PHY/system requirements mentioned above: DDR4: CWL + PL + BL/2 + tWTR_L LPDDR2/3/4: WL + BL/2 + tWTR + 1 Others: CWL + BL/2 + tWTR Where: CWL: CAS write latency WL: Write latency PL: Parity latency BL: Burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM tWTR_L: Internal write to read command delay for same bank group. This comes directly from the SDRAM specification tWTR: Internal write to read command delay. This comes directly from the SDRAM specification Add one extra cycle for LPDDR2/LPDDR3/LPDDR4 operation. WTR_L must be increased by one if DDR4 2tCK write preamble is used. When the controller is operating in 1:2 mode, divide the value calculated using the previous equation by 2, and round it up to next integer. If your configuration has RANKCTL1.wr2rd_dr, write to read bus turn-around between different physical ranks are controlled by RANKCTL1.wr2rd_dr. Unit: DFI clock cycles. Value After Reset:0xd Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_FREQ2_DRAMTMG3

Address: Operational Base(0xFF4E0000) + offset (0x310C)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved2 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
29:20	RW	0x005	t_mrw Indicates the time to wait after a mode register write or read (MRW or MRR). Present only in designs configured to support LPDDR2, LPDDR3 or LPDDR4. LPDDR2 typically requires value of 5. LPDDR3 typically requires value of 10. LPDDR4: Set this to the larger of tMRW and tMRWCKEL. For LPDDR2, this register is used for the time from a MRW/MRR to all other commands. When the controller is operating in 1:2 frequency ratio mode, program this to the previous values divided by 2 and round it up to the next integer value. For LDPDR3, this register is used for the time from a MRW/MRR to a MRW/MRR. Unit: DFI clock cycles. Value After Reset:0x5 Programming Mode:Quasi-dynamic Group 2, Group 4
19:18	RW	0x0	Reserved1 Reserved Field:Yes
17:12	RW	0x04	t_mrd tMRD- Indicates the number of cycles to wait after a mode register write or read. Depending on the connected SDRAM, tMRD represents: DDR2/mDDR: Time from MRS to any command DDR3/4: Time from MRS to MRS command LPDDR2: not used LPDDR3/4: Time from MRS to non-MRS command When the controller is operating in 1:2 frequency ratio mode, program this to (tMRD/2) and round it up to the next integer value. If C/A parity for DDR4 is used, set to tMRD_PAR(tMOD+PL) instead. If CAL mode is enabled (DFITMG1.dfi_t_cmd_lat > 0), tCAL (=DFITMG1.dfi_cmd_lat) must be added to the previous calculations. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 2, Group 4
11:10	RW	0x0	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
9:0	RW	0x00c	t_mod tMOD - Parameter used only in DDR3 and DDR4. Indicates the number of cycles between load mode command and following non-load mode command. If C/A parity for DDR4 is used, set to tMOD_PAR(tMOD+PL) instead. If CAL mode is enabled (DFITMG1.dfi_t_cmd_lat > 0), tCAL (=DFITMG1.dfi_cmd_lat) must be added to the previous calculations. Set to tMOD if controller is operating in 1:1 frequency ratio mode, or tMOD/2 (rounded up to next integer) if controller is operating in 1:2 frequency ratio mode. Note that if using RDIMM/LRDIMM, depending on the PHY, it may be necessary to adjust the value of this parameter to compensate for the extra cycle of latency applied to mode register writes by the RDIMM/LRDIMM chip. Also note that if using RDIMM or LRDIMM, the minimum value of this register is tMRD_L2 if controller is operating in 1:1 frequency ratio mode, or tMRD_L2/2 (rounded up to next integer) if controller is operating in 1:2 frequency ratio mode. Unit: DFI clock cycles. Value After Reset:0xc Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ2_DRAMTMG4

Address: Operational Base(0xFF4E0000) + offset (0x3110)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved3 Reserved Field:Yes
28:24	RW	0x05	t_rcd tRCD - tAL: Indicates the minimum time from activate to read or write command to same bank. When the controller is operating in 1:2 frequency ratio mode, program this to ((tRCD - tAL)/2) and round it up to the next integer value. Minimum value allowed for this register is 1, which implies minimum (tRCD - tAL) value to be 2 when the controller is operating in 1:2 frequency ratio mode. Unit: DFI clock cycles. Value After Reset:0x5 Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
23:20	RW	0x0	Reserved2 Reserved Field:Yes
19:16	RW	0x4	t_ccd DDR4: tCCD_L: This is the minimum time between two reads or two writes for same bank group. Others: tCCD: This is the minimum time between two reads or two writes. When the controller is operating in 1:2 frequency ratio mode, program this to (tCCD_L/2 or tCCD/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 2, Group 4
15:12	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
11:8	RW	0x4	t_rrd DDR4: tRRD_L: This is the minimum time between activates from bank "a" to bank "b" for same bank group. Others: tRRD: Minimum time between activates from bank "a" to bank "b" When the controller is operating in 1:2 frequency ratio mode, program this to (tRRD_L/2 or tRRD/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 2, Group 4
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4:0	RW	0x05	t_rp tRP: Indicates the minimum time from single-bank precharge to activate of same bank. When the controller is operating in 1:1 frequency ratio mode, t_rp must be set to RoundUp(tRP/tCK). When the controller is operating in 1:2 frequency ratio mode, t_rp must be set to RoundDown(RoundUp(tRP/tCK)/2) + 1. When the controller is operating in 1:2 frequency ratio mode in LPDDR4, t_rp must be set to RoundUp(RoundUp(tRP/tCK)/2). Unit: DFI clock cycles. Value After Reset:0x5 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ2_DRAMTMG5

Address: Operational Base(0xFF4E0000) + offset (0x3114)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved3 Reserved Field:Yes
27:24	RW	0x5	t_cksrx This is the time before self-refresh Exit that CK is maintained as a valid clock before issuing SRX. Specifies the clock stable time before SRX. Recommended settings: mDDR - 1 LPDDR2 - 2 LPDDR3 - 2 LPDDR4 - tCKCKEH DDR2 - 1 DDR3 - tCKSRX DDR4 - tCKSRX When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. Unit: DFI clock cycles. Value After Reset:0x5 Programming Mode:Quasi-dynamic Group 2, Group 4
23	RW	0x0	Reserved2 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
22:16	RW	0x05	t_cksre This is the time after self-refresh Down Entry that CK is maintained as a valid clock. Specifies the clock disable delay after SRE. Recommended settings: mDDR - 0 LPDDR2 - 2 LPDDR3 - 2 LPDDR4 - tCKELCK DDR2 - 1 DDR3 - Max (10 ns, 5 tCK) DDR4(No RDIMM) - Max (10 ns, 5 tCK) (+ PL(parity latency)(*)) DDR4(RDIMM) - Max (Max (10 ns, 5 tCK) (+ PL(parity latency)(*)), tCKOff) (*)Only if CRCPARCTL1.caparity_disable_before_sr=0, this register must be increased by PL. When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. Unit: DFI clock cycles. Value After Reset:0x5 Programming Mode:Quasi-dynamic Group 2, Group 4
15:14	RW	0x0	Reserved1 Reserved Field:Yes
13:8	RW	0x04	t_ckesr Indicates the minimum CKE low width for self-refresh or self-refresh power down entry to exit timing in memory clock cycles. Recommended settings: mDDR - tRFC LPDDR2 - tCKESR LPDDR3 - tCKESR LPDDR4 - max(tCKE, tSR) DDR2 - tCKE DDR3 - tCKE + 1 DDR4(No RDIMM) - tCKE + 1 (+ PL(parity latency)(*)) DDR4(RDIMM) - t_cksre + tCKEV (*)Only if CRCPARCTL1.caparity_disable_before_sr=0, this register must be increased by PL. When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 2, Group 4
7:5	RW	0x0	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
4:0	RW	0x03	t_cke Indicates the minimum number of cycles of CKE HIGH/LOW during power-down and self-refresh. LPDDR2/LPDDR3 mode - Set this to the larger of tCKE or tCKESR LPDDR4 mode - Set this to the larger of tCKE or tSR Non-LPDDR2/non-LPDDR3/non-LPDDR4 designs - Set this to tCKE value When the controller is operating in 1:2 frequency ratio mode, program this to (value described above)/2 and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x3 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ2_DRAMTMG6

Address: Operational Base(0xFF4E0000) + offset (0x3118)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved2 Reserved Field:Yes
27:24	RW	0x2	t_ckdpde This is the time after Deep Power Down Entry that CK is maintained as a valid clock. Specifies the clock disable delay after DPDE. Recommended settings: mDDR: 0 LPDDR2: 2 LPDDR3: 2 When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. This is only present for designs supporting mDDR or LPDDR2/LPDDR3 devices. Unit: DFI clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4
23:20	RW	0x0	Reserved1 Reserved Field:Yes
19:16	RW	0x2	t_ckdpdx This is the time before Deep Power Down Exit that CK is maintained as a valid clock before issuing DPDX. Specifies the clock stable time before DPDX. Recommended settings: mDDR - 1 LPDDR2 - 2 LPDDR3 - 2 When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. This is only present for designs supporting mDDR or LPDDR2 devices. Unit: DFI clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4
15:4	RW	0x000	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
3:0	RW	0x5	t_ckcsx This is the time before Clock Stop Exit that CK is maintained as a valid clock before issuing Clock Stop Exit. Specifies the clock stable time before next command after Clock Stop Exit. Recommended settings: mDDR - 1 LPDDR2 - tXP + 2 LPDDR3 - tXP + 2 LPDDR4 - tXP + 2 When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. This is only present for designs supporting mDDR or LPDDR2/LPDDR3/LPDDR4 devices. Unit: DFI clock cycles. Value After Reset:0x5 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ2_DRAMTMG7

Address: Operational Base(0xFF4E0000) + offset (0x311C)

Bit	Attr	Reset Value	Description
31:12	RW	0x00000	Reserved1 Reserved Field:Yes
11:8	RW	0x2	t_ckpde This is the time after Power Down Entry that CK is maintained as a valid clock. Specifies the clock disable delay after PDE. Recommended settings: mDDR - 0 LPDDR2 - 2 LPDDR3 - 2 LPDDR4 - tCKELCK When using DDR2/3/4 SDRAM, this register must be set to the same value as DRAMTMG5.t_cksre. When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. This is only present for designs supporting mDDR or LPDDR2/LPDDR3/LPDDR4 devices. Unit: DFI clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4
7:4	RW	0x0	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
3:0	RW	0x2	t_ckpdx This is the time before Power Down Exit that CK is maintained as a valid clock before issuing PDX. Specifies the clock stable time before PDX. Recommended settings: mDDR - 0 LPDDR2 - 2 LPDDR3 - 2 LPDDR4 - tCKCKEH When using DDR2/3/4 SDRAM, this register must be set to the same value as DRAMTMG5.t_cksrx. When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. This is only present for designs supporting mDDR or LPDDR2/LPDDR3/LPDDR4 devices. Unit: DFI clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ2_DRAMTMG8

Address: Operational Base(0xFF4E0000) + offset (0x3120)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved3 Reserved Field:Yes
30:24	RW	0x03	t_xs_fast_x32 tXS_FAST: Exit self-refresh to ZQCL, ZQCS and MRS (only CL, WR, RTP and Geardown mode). When the controller is operating in 1:2 frequency ratio mode, program this to the previous value divided by 2 and round up to next integer value. Note: This is applicable to only ZQCL/ZQCS commands. Note: Ensure this is less than or equal to t_xs_x32. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x3 Programming Mode:Quasi-dynamic Group 2, Group 4
23	RW	0x0	Reserved2 Reserved Field:Yes
22:16	RW	0x03	t_xs_abort_x32 tXS_ABORT: Exit self-refresh to commands not requiring a locked DLL in self-refresh Abort. When the controller is operating in 1:2 frequency ratio mode, program this to the previous value divided by 2 and round up to next integer value. Note: Ensure this is less than or equal to t_xs_x32. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x3 Programming Mode:Quasi-dynamic Group 2, Group 4
15	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
14:8	RW	0x44	t_xs_dll_x32 tXSDLL: Exit self-refresh to commands requiring a locked DLL. When the controller is operating in 1:2 frequency ratio mode, program this to the previous value divided by 2 and round up to next integer value. Note: Used only for DDR2, DDR3 and DDR4 SDRAMs. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x44 Programming Mode:Quasi-dynamic Group 2, Group 4
7	RW	0x0	Reserved0 Reserved Field:Yes
6:0	RW	0x05	t_xs_x32 tXS: Exit self-refresh to commands not requiring a locked DLL. When the controller is operating in 1:2 frequency ratio mode, program this to the previous value divided by 2 and round up to next integer value. Note: Used only for DDR2, DDR3 and DDR4 SDRAMs. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x5 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ2_DRAMTMG9

Address: Operational Base(0xFF4E0000) + offset (0x3124)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved3 Reserved Field:Yes
30	RW	0x0	ddr4_wr_preamble DDR4 Write preamble mode. 0 - 1tCK preamble 1 - 2tCK preamble Present only with MEMC_FREQ_RATIO=2. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4
29:19	RW	0x000	Reserved2 Reserved Field:Yes
18:16	RW	0x4	t_ccd_s tCCD_S: This is the minimum time between two reads or two writes for different bank group. When the controller is operating in 1:2 frequency ratio mode, program this to (tCCD_S/2) and round it up to the next integer value. Present only in designs configured to support DDR4. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 2, Group 4
15:12	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
11:8	RW	0x4	t_rrd_s tRRD_S: This is the minimum time between activates for different bank group. When the controller is operating in 1:2 frequency ratio mode, program this to (tRRD_S/2) and round it up to the next integer value. Present only in designs configured to support DDR4. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 2, Group 4
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5:0	RW	0x0d	wr2rd_s Minimum time from write command to read command for different bank group. This must include time for bus turn-around and all PHY and system requirements. After the PHY has completed training, the value programmed may need to be increased. Please see the relevant PHY databook for details of what should be included here. The following calculations are minimum values, and do not include the PHY/system requirements mentioned above: CWL + PL + BL/2 + tWTR_S Where: CWL: CAS write latency PL: Parity latency BL: Burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM tWTR_S: Internal write to read command delay for different bank group. This comes directly from the SDRAM specification WTR_S must be increased by one if DDR4 2tCK write preamble is used. When the controller is operating in 1:2 mode, divide the value calculated using the previous equation by 2, and round it up to next integer. If your configuration has RANKCTL1.wr2rd_dr, write to read bus turn-around between different physical ranks are controlled by RANKCTL1.wr2rd_dr. Unit: DFI clock cycles. Value After Reset:0xd Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_FREQ2_DRAMTMG10

Address: Operational Base(0xFF4E0000) + offset (0x3128)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved2 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
20:16	RW	0x1c	t_sync_gear Indicates the time between MRS command and the sync pulse time. This must be even number of clocks. For DDR4-2666 and DDR4-3200, this parameter is defined as tMOD(min)+4nCK tMOD(min) is greater of 24nCK or 15ns 15ns / .625ns = 24 Max value for this register is 24+4 = 28 When the controller is operating in 1:2 mode, program this to (tSYNC_GEAR/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x1c Programming Mode:Quasi-dynamic Group 2, Group 4
15:13	RW	0x0	Reserved1 Reserved Field:Yes
12:8	RW	0x18	t_cmd_gear Indicates a sync pulse to first valid command. For DDR4-2666 and DDR4-3200, this parameter is defined as tMOD(min) tMOD(min) is greater of 24nCK or 15ns 15ns / .625ns = 24 Max value for this register is 24 When the controller is operating in 1:2 mode, program this to (tCMD_GEAR/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x18 Programming Mode:Quasi-dynamic Group 2, Group 4
7:4	RW	0x0	Reserved0 Reserved Field:Yes
3:2	RW	0x2	t_gear_setup Indicates the geardown setup time. Minimum value of this register is 1. Zero is invalid. For DDR4-2666 and DDR4-3200, this parameter is defined as 2 clks When the controller is operating in 1:2 frequency ratio mode, program this to (tGEAR_setup/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4
1:0	RW	0x2	t_gear_hold Indicates the geardown hold time. Minimum value of this register is 1. Zero is invalid. For DDR4-2666 and DDR4-3200, this parameter is defined as 2 clks When the controller is operating in 1:2 frequency ratio mode, program this to (tGEAR_hold/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ2_DRAMTMG11

Address: Operational Base(0xFF4E0000) + offset (0x312C)

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Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved3 Reserved Field:Yes
30:24	RW	0x44	post_mpsm_gap_x32 tXMPDLL: This is the minimum Exit MPSM to commands requiring a locked DLL. When the controller is operating in 1:2 frequency ratio mode, program this to (tXMPDLL/2) and round it up to the next integer value. Present only in designs configured to support DDR4. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x44 Programming Mode:Quasi-dynamic Group 2, Group 4
23:21	RW	0x0	Reserved2 Reserved Field:Yes
20:16	RW	0x0c	t_mpx_lh tMPX_LH: This is the minimum CS_n Low hold time to CKE rising edge. When the controller is operating in 1:2 frequency ratio mode, program this to RoundUp(tMPX_LH/2)+1. Present only in designs configured to support DDR4. Unit: DFI clock cycles. Value After Reset:0xc Programming Mode:Quasi-dynamic Group 2, Group 4
15:10	RW	0x00	Reserved1 Reserved Field:Yes
9:8	RW	0x2	t_mpx_s tMPX_S: This is the minimum time CS setup time to CKE. When the controller is operating in 1:2 frequency ratio mode, program this to (tMPX_S/2) and round it up to the next integer value. Present only in designs configured to support DDR4. Unit: DFI clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4:0	RW	0x1c	t_ckmpe tCKMPE: This is the minimum valid clock requirement after MPSM entry. Present only in designs configured to support DDR4. When the controller is operating in 1:2 frequency ratio mode, divide the value calculated using the previous equation by 2, and round it up to next integer. Unit: DFI clock cycles. Value After Reset:0x1c Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ2_DRAMTMG12

Address: Operational Base(0xFF4E0000) + offset (0x3130)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved2 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
29:24	RW	0x1a	t_wr_mpr This bit is used only in DDR4. Cycles between MPR Write and other command. Set this to tMOD + AL (or tMOD + PL + AL if C/A parity is also used). When the controller is operating in 1:2 frequency ratio mode, program this to (tWR_MPR/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x1a Programming Mode:Quasi-dynamic Group 2, Group 4
23:18	RW	0x00	Reserved1 Reserved Field:Yes
17:16	RW	0x2	t_cmdcke tCMDCKE: Indicates the delay from valid command to CKE input LOW. Set this to the larger of tESCKE or tCMDCKE When the controller is operating in 1:2 frequency ratio mode, program this to (max(tESCKE, tCMDCKE)/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4
15:5	RW	0x000	Reserved0 Reserved Field:Yes
4:0	RW	0x10	t_mrd_pda tMRD_PDA: This is the Mode Register Set command cycle time in PDA mode. When the controller is operating in 1:2 frequency ratio mode, program this to (tMRD_PDA/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x10 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ2_DRAMTMG13

Address: Operational Base(0xFF4E0000) + offset (0x3134)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved2 Reserved Field:Yes
30:24	RW	0x1c	odtloff LPDDR4: ODTLoff: This is the latency from CAS-2 command to ODToff reference. When the controller is operating in 1:2 frequency ratio mode, program this to (ODTLoff/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x1c Programming Mode:Quasi-dynamic Group 2, Group 4
23:22	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
21:16	RW	0x20	t_ccd_mw LPDDR4: tCCDMW: This is the minimum time from write or masked write to masked write command for same bank. When the controller is operating in 1:2 frequency ratio mode, program this to (tCCDMW/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x20 Programming Mode:Quasi-dynamic Group 2, Group 4
15:3	RW	0x0000	Reserved0 Reserved Field:Yes
2:0	RW	0x4	t_ppd LPDDR4: tPPD: This is the minimum time from precharge to precharge command. When the controller is operating in 1:2 frequency ratio mode, program this to (tPPD/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ2_DRAMTMG14

Address: Operational Base(0xFF4E0000) + offset (0x3138)

Bit	Attr	Reset Value	Description
31:12	RW	0x00000	Reserved0 Reserved Field:Yes
11:0	RW	0x0a0	t_xsr tXSR: This is the exit self-refresh to any command. When the controller is operating in 1:2 frequency ratio mode, program this to the previous value divided by 2 and round up to next integer value. The value 0xfff is illegal for this register field. Note: Used only for mDDR/LPDDR2/LPDDR3/LPDDR4 mode. Unit: DFI clock cycles. Value After Reset:0xa0 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ2_DRAMTMG15

Address: Operational Base(0xFF4E0000) + offset (0x313C)

Bit	Attr	Reset Value	Description
31	RW	0x0	en_dfi_lp_t_stab 1 - Enable using tSTAB when exiting DFI LP. This must be set when the PHY is stopping the clock during DFI LP to save maximum power. 0 - Disable using tSTAB when exiting DFI LP. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4
30:8	RW	0x000000	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	t_stab_x32 tSTAB: Stabilization time. It is required in the following two cases for DDR3/DDR4 RDIMM: When exiting power saving mode, if the clock is stopped, after re-enabling it the clock must be stable for a time specified by tSTAB In the case of input clock frequency change (DDR4) After issuing control words that refers to clock timing (Specification: 6us for DDR3, 5us for DDR4) Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ2_ZQCTL0

Address: Operational Base(0xFF4E0000) + offset (0x3180)

Bit	Attr	Reset Value	Description
31	RW	0x0	dis_auto_zq 1 - Disable uMCTL2 generation of ZQCS/MPC(ZQ calibration) command. Register DBGCMD.zq_calib_short can be used instead to issue ZQ calibration request from APB module 0 - Internally generate ZQCS/MPC(ZQ calibration) commands based on ZQCTL1.t_zq_short_interval_x1024 This is only present for designs supporting DDR3/DDR4 or LPDDR2/LPDDR3/LPDDR4 devices. Value After Reset:0x0 Programming Mode:Dynamic
30	RW	0x0	dis_srx_zqcl 1 - Disable issuing of ZQCL/MPC(ZQ calibration) command at self-refresh/SR-Powerdown exit. Only applicable when run in DDR3 or DDR4 or LPDDR2 or LPDDR3 or LPDDR4 mode 0 - Enable issuing of ZQCL/MPC(ZQ calibration) command at self-refresh/SR-Powerdown exit. Only applicable when run in DDR3 or DDR4 or LPDDR2 or LPDDR3 or LPDDR4 mode This is only present for designs supporting DDR3/DDR4 or LPDDR2/LPDDR3/LPDDR4 devices. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4
29	RW	0x0	zq_resistor_shared 1 - Denotes that ZQ resistor is shared between ranks. Means ZQinit/ZQCL/ZQCS/MPC(ZQ calibration) commands are sent to one rank at a time with tZQinit/tZQCL/tZQCS/tZQCAL/tZQLAT timing met between commands so that commands to different ranks do not overlap 0 - ZQ resistor is not shared This is only present for designs supporting DDR3/DDR4 or LPDDR2/LPDDR3/LPDDR4 devices. Value After Reset:0x0 Programming Mode:Static

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Bit	Attr	Reset Value	Description
28	RW	0x0	dis_mpsmx_zqcl 1 - Disable issuing of ZQCL command at Maximum Power Saving Mode exit. Only applicable when run in DDR4 mode 0 - Enable issuing of ZQCL command at Maximum Power Saving Mode exit. Only applicable when run in DDR4 mode This is only present for designs supporting DDR4 devices. Note: Do not issue ZQCL command at Maximum Power Save Mode exit if the UMCTL2_SHARED_AC configuration parameter is set. Program it to 1'b1. The software can send ZQCS after exiting MPSM mode. Value After Reset:0x0 Programming Mode:Static
27	RW	0x0	Reserved1 Reserved Field:Yes
26:16	RW	0x200	t_zq_long_nop tZQoper for DDR3/DDR4, tZQCL for LPDDR2/LPDDR3, tZQCAL for LPDDR4: Number of DFI clock cycles of NOP required after a ZQCL (ZQ calibration long)/MPC(ZQ Start) command is issued to SDRAM. When the controller is operating in 1:2 frequency ratio mode: DDR3/DDR4: program this to tZQoper/2 and round it up to the next integer value. LPDDR2/LPDDR3: program this to tZQCL/2 and round it up to the next integer value. LPDDR4: program this to tZQCAL/2 and round it up to the next integer value. This is only present for designs supporting DDR3/DDR4 or LPDDR2/LPDDR3/LPDDR4 devices. Unit: DFI clock cycles. Value After Reset:0x200 Programming Mode:Static
15:10	RW	0x00	Reserved0 Reserved Field:Yes
9:0	RW	0x040	t_zq_short_nop tZQCS for DDR3/DD4/LPDDR2/LPDDR3, tZQLAT for LPDDR4: Number of DFI clock cycles of NOP required after a ZQCS (ZQ calibration short)/MPC(ZQ Latch) command is issued to SDRAM. When the controller is operating in 1:2 frequency ratio mode, program this to tZQCS/2 and round it up to the next integer value. This is only present for designs supporting DDR3/DDR4 or LPDDR2/LPDDR3/LPDDR4 devices. Unit: DFI clock cycles. Value After Reset:0x40 Programming Mode:Static

DDRCTL_FREQ2_DFITMG0

Address: Operational Base(0xFF4E0000) + offset (0x3190)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved2 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
28:24	RW	0x07	dfi_t_ctrl_delay Specifies the number of DFI clock cycles after an assertion or de-assertion of the DFI control signals that the control signals at the PHY-DRAM interface reflect the assertion or de-assertion. If the DFI clock and the memory clock are not phase-aligned, this timing parameter must be rounded up to the next integer value. Note that if using RDIMM/LRDIMM, it is necessary to increment this parameter by RDIMM's/LRDIMM's extra cycle of latency in terms of DFI clock. Unit: DFI clock cycles. Value After Reset:0x7 Programming Mode:Quasi-dynamic Group 4
23	RW	0x0	dfi_rddata_use_dfi_phy_clk Defines whether dfi_rddata_en/dfi_rddata/dfi_rddata_valid is generated using HDR (DFI clock) or SDR (DFI PHY clock) values. Selects whether value in DFITMG0.dfi_t_rddata_en is in terms of HDR (DFI clock) or SDR (DFI PHY clock) cycles: 0 in terms of HDR (DFI clock) cycles 1 in terms of SDR (DFI PHY clock) cycles Refer to PHY specification for correct value. If using a Synopsys DWC DDR3/2 PHY, DWC DDR2/3-Lite/mDDR PHY, DWC DDR multiPHY or DWC Gen2 DDR multiPHY, this field must be set to 0; otherwise: If MEMC_PROG_FREQ_RATIO=1 and MSTR.frequency_ratio=1, this field must be set to 0 Else, it must be set to 1 Value After Reset:0x0 Programming Mode:Static
22:16	RW	0x02	dfi_t_rddata_en Time from the assertion of a read command on the DFI interface to the assertion of the dfi_rddata_en signal. Refer to PHY specification for correct value. This corresponds to the DFI parameter trddata_en. Note that, depending on the PHY, if using RDIMM/LRDIMM, it may be necessary to use the adjusted value of CL in the calculation of trddata_en. This is to compensate for the extra cycles of latency through the RDIMM/LRDIMM. Unit: DFI clock cycles or DFI PHY clock cycles, depending on DFITMG0.dfi_rddata_use_dfi_phy_clk. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 1, Group 4

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Bit	Attr	Reset Value	Description
15	RW	0x0	dfi_wrdata_use_dfi_phy_clk Defines whether dfi_wrdata_en/dfi_wrdata/dfi_wrdata_mask is generated using HDR (DFI clock) or SDR (DFI PHY clock) values. Selects whether value in DFITMG0.dfi_tphy_wrlat is in terms of HDR (DFI clock) or SDR (DFI PHY clock) cycles. Selects whether value in DFITMG0.dfi_tphy_wrdata is in terms of HDR (DFI clock) or SDR (DFI PHY clock) cycles. 0 in terms of HDR (DFI clock) cycles 1 in terms of SDR (DFI PHY clock) cycles Refer to PHY specification for correct value. If using a Synopsys DWC DDR3/2 PHY, DWC DDR2/3-Lite/mDDR PHY, DWC DDR multiPHY or DWC Gen2 DDR multiPHY, this field must be set to 0; otherwise: If MEMC_PROG_FREQ_RATIO=1 and MSTR.frequency_ratio=1, this field must be set to 0 Else, it must be set to 1 Value After Reset:0x0 Programming Mode:Static
14	RW	0x0	Reserved1 Reserved Field:Yes
13:8	RW	0x00	dfi_tphy_wrdata Specifies the number of clock cycles between when dfi_wrdata_en is asserted to when the associated write data is driven on the dfi_wrdata signal. This corresponds to the DFI timing parameter tphy_wrdata. For more information on correct value, see PHY specification. Note, maximum supported value is 8. Unit: DFI clock cycles or DFI PHY clock cycles, depending on DFITMG0.dfi_wrdata_use_dfi_phy_clk. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 4
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5:0	RW	0x02	dfi_tphy_wrlat Write latency. Number of clocks from the write command to write data enable (dfi_wrdata_en). This corresponds to the DFI timing parameter tphy_wrlat. Refer to PHY specification for correct value.Note that, depending on the PHY, if using RDIMM/LRDIMM, it may be necessary to use the adjusted value of CL in the calculation of tphy_wrlat. This is to compensate for the extra cycles of latency through the RDIMM/LRDIMM. For LPDDR4, dfi_tphy_wrlat>60 is not supported. Unit: DFI clock cycles or DFI PHY clock cycles, depending on DFITMG0.dfi_wrdata_use_dfi_phy_clk. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ2_DFITMG1

Address: Operational Base(0xFF4E0000) + offset (0x3194)

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Bit	Attr	Reset Value	Description
31:28	RW	0x0	dfi_t_cmd_lat Specifies the number of DFI PHY clock cycles between when the dfi_cs signal is asserted and when the associated command is driven. This field is used for CAL mode, must be set to '0' or tCAL, which matches the CAL mode register setting in the DRAM. When enabling CAL mode with RDIMM/LRDIMM, this field must be set to tCAL-CLA (Command Latency Adder). For more information on CLA, see JEDEC DDR4 Register Specification. If the PHY can add the latency for CAL mode, this must be set to '0'. Valid Range: 0 to 8. Unit: DFI PHY clock cycles. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4
27:26	RW	0x0	Reserved3 Reserved Field:Yes
25:24	RW	0x0	dfi_t_parin_lat Specifies the number of DFI PHY clock cycles between when the dfi_cs signal is asserted and when the associated dfi_parity_in signal is driven. Unit: DFI PHY clock cycles. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 4
23:21	RW	0x0	Reserved2 Reserved Field:Yes
20:16	RW	0x00	dfi_t_wrdata_delay Specifies the number of DFI clock cycles between when the dfi_wrdata_en signal is asserted and when the corresponding write data transfer is completed on the DRAM bus. This corresponds to the DFI timing parameter twrdata_delay. For more information on correct value, see PHY specification. For DFI 3.0 PHY, set to twrdata_delay, a new timing parameter introduced in DFI 3.0. For DFI 2.1 PHY, set to tphy_wrdata + (delay of DFI write data to the DRAM). Value to be programmed is in terms of DFI clocks, not PHY clocks. In FREQ_RATIO=2, divide PHY's value by 2 and round up to next integer. If using DFITMG0.dfi_wrdata_use_dfi_phy_clk=1, add 1 to the value. Unit: DFI clock cycles. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 4
15:13	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
12:8	RW	0x04	dfi_t_dram_clk_disable Specifies the number of DFI clock cycles from the assertion of the dfi_dram_clk_disable signal on the DFI until the clock to the DRAM memory devices, at the PHY-DRAM boundary, maintains a low value. If the DFI clock and the memory clock are not phase aligned, this timing parameter must be rounded up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 4
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4:0	RW	0x04	dfi_t_dram_clk_enable Specifies the number of DFI clock cycles from the de-assertion of the dfi_dram_clk_disable signal on the DFI until the first valid rising edge of the clock to the DRAM memory devices, at the PHY-DRAM boundary. If the DFI clock and the memory clock are not phase aligned, this timing parameter must be rounded up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 4

DDRCTL_FREQ2_DFITMG2

Address: Operational Base(0xFF4E0000) + offset (0x31B4)

Bit	Attr	Reset Value	Description
31:15	RW	0x00000	Reserved1 Reserved Field:Yes
14:8	RW	0x02	dfi_tphy_rdcslat specifies the number of DFI PHY clock cycles between when a read command is sent on the DFI control interface and when the associated dfi_rddata_cs signal is asserted. This corresponds to the DFI timing parameter tphy_rdcslat. Refer to PHY specification for correct value. Unit: DFI PHY clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5:0	RW	0x02	dfi_tphy_wrcslat Specifies the number of DFI PHY clock cycles between when a write command is sent on the DFI control interface and when the associated dfi_wrdata_cs signal is asserted. This corresponds to the DFI timing parameter tphy_wrcslat. For more information on correct value, see PHY specification. Unit: DFI PHY clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ2_DFITMG3

Address: Operational Base(0xFF4E0000) + offset (0x31B8)

Bit	Attr	Reset Value	Description
31:5	RW	0x0000000	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
4:0	RW	0x00	dfi_t_geardown_delay The delay from dfi_geardown_en assertion to the time of the PHY being ready to receive commands. Refer to PHY specification for correct value. When the controller is operating in 1:2 frequency ratio mode, program this to (tgeardown_delay/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x0 Programming Mode:Static

DDRCTL_FREQ2_ODTCFG

Address: Operational Base(0xFF4E0000) + offset (0x3240)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved4 Reserved Field:Yes
27:24	RW	0x4	wr_odt_hold DFI PHY clock cycles to hold ODT for a write command. The minimum supported value is 2. Recommended values: DDR2: BL8 - 0x5 (DDR2-400/533/667), 0x6 (DDR2-800), 0x7 (DDR2-1066) BL4 - 0x3 (DDR2-400/533/667), 0x4 (DDR2-800), 0x5 (DDR2-1066) DDR3: BL8 - 0x6 DDR4: BL8 - 5 + WR_PREAMBLE + CRC_MODE WR_PREAMBLE = 1 (1tCK write preamble), 2 (2tCK write preamble) CRC_MODE = 0 (not CRC mode), 1 (CRC mode) LPDDR3: BL8 - 7 + RU(tODTon(max)/tCK) Unit: DFI PHY clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 1, Group 4
23:21	RW	0x0	Reserved3 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
20:16	RW	0x00	wr_odt_delay Indicates the delay, in DFI PHY clock cycles, from issuing a write command to setting ODT values associated with that command. ODT setting must remain constant for the entire time that DQS is driven by the uMCTL2. Recommended values: DDR2: CWL + AL - 3 (DDR2-400/533/667), CWL + AL - 4 (DDR2-800), CWL + AL - 5 (DDR2-1066) If (CWL + AL - 3 < 0), uMCTL2 does not support ODT for write operation. DDR3: 0x0 DDR4: DFITMG1.dfi_t_cmd_lat (to adjust for CAL mode) LPDDR3: WL - 1 - RU(tODTon(max)/tCK)) Unit: DFI PHY clock cycles. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 1, Group 4
15:12	RW	0x0	Reserved2 Reserved Field:Yes
11:8	RW	0x4	rd_odt_hold DFI PHY clock cycles to hold ODT for a read command. The minimum supported value is 2. Recommended values: DDR2: BL8 - 0x6 (not DDR2-1066), 0x7 (DDR2-1066) BL4 - 0x4 (not DDR2-1066), 0x5 (DDR2-1066) DDR3: BL8 - 0x6 DDR4: BL8 - 5 + RD_PREAMBLE RD_PREAMBLE = 1 (1tCK read preamble), 2 (2tCK read preamble) LPDDR3: BL8 - 5 + RU(tDQSCK(max)/tCK) - RD(tDQSCK(min)/tCK) + RU(tODTon(max)/tCK) Unit: DFI PHY clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 1, Group 4
7	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
6:2	RW	0x00	rd_odt_delay Indicates the delay, in DFI PHY clock cycles, from issuing a read command to setting ODT values associated with that command. ODT setting must remain constant for the entire time that DQS is driven by the uMCTL2. Recommended values: DDR2: CL + AL - 4 (not DDR2-1066), CL + AL - 5 (DDR2-1066) If (CL + AL - 4 < 0), uMCTL2 does not support ODT for read operation. DDR3: CL - CWL DDR4: CL - CWL - RD_PREAMBLE + WR_PREAMBLE + DFITMG1.dfi_t_cmd_lat (to adjust for CAL mode) WR_PREAMBLE = 1 (1tCK write preamble), 2 (2tCK write preamble) LPDDR3: RL + RD(tDQSCK(min)/tCK) - 1 - RU(tODTon(max)/tCK) Unit: DFI PHY clock cycles. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 1, Group 4
1:0	RW	0x0	Reserved0 Reserved Field:Yes

DDRCTL_FREQ3_DERATEEN

Address: Operational Base(0xFF4E0000) + offset (0x4020)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	Reserved2 Reserved Field:Yes
13	RW	0x0	derate_mr4_pause_fc Pauses MR4 reads. Must only be set to 1 as part of Frequency Change procedures, if DERATEEN.derate_enable=1 Value After Reset:0x0 Programming Mode:Dynamic
12	RW	0x0	derate_mr4_tuf_dis Disables use of MR4 TUF flag (MR4[7]) bit. 0 - Use MR4 TUF flag (MR4[7]) 1 - Do not use MR4 TUF Flag (MR4[7]) For LPDDR4, it is recommended to set this register to 1. For LPDDR2 and LPDDR3, contact your memory vendor for recommended usage. This affects both the periodic derate logic (DERATEEN.derate_enable) and the derate_temp_limit_intr. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4
11	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
10:8	RW	0x0	rc_derate_value Derate value of tRC for LPDDR4. 0 - Derating uses +1 1 - Derating uses +2 2 - Derating uses +3 3 - Derating uses +4 4 - Derating uses +5 5 - Derating uses +6 6 - Derating uses +7 7 - Derating uses +8 Present only in designs configured to support LPDDR4. The required cycles for derating can be determined by dividing 3.75ns by the core_ddrc_core_clk period, and rounding it up to the next integer. Hence this register field must be set to the previous value - 1. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4
7:4	RW	0x0	derate_byte This bit indicates which byte of the MRR data is used for derating. The maximum valid value depends on MEMC_DRAM_TOTAL_DATA_WIDTH. Present only in designs configured to support LPDDR2/LPDDR3/LPDDR4. Value After Reset:0x0 Programming Mode:Static
3	RW	0x0	Reserved0 Reserved Field:Yes
2:1	RW	0x0	derate_value Derate value. 0 - Derating uses +1 1 - Derating uses +2 2 - Derating uses +3 3 - Derating uses +4 Present only in designs configured to support LPDDR2/LPDDR3/LPDDR4. The required cycles for derating can be determined by dividing 1.875ns by the core_ddrc_core_clk period, and rounding it up to the next integer. Hence this register field must be set to the previous value - 1. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4
0	RW	0x0	derate_enable Enables derating. 0 - Timing parameter derating is disabled 1 - Timing parameter derating is enabled using MR4 read value Present only in designs configured to support LPDDR2/LPDDR3/LPDDR4. This field must be set to '0' for non-LPDDR2/LPDDR3/LPDDR4 mode. Value After Reset:0x0 Programming Mode:Dynamic

DDRCTL_FREQ3_DERATEINT

Address: Operational Base(0xFF4E0000) + offset (0x4024)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00800000	mr4_read_interval Interval between two MR4 reads, used to derate the timing parameters. Present only in designs configured to support LPDDR2/LPDDR3/LPDDR4. This register must not be set to zero. Unit: DFI clock cycles. Value After Reset:0x800000 Programming Mode:Static

DDRCTL_FREQ3_PWRTMG

Address: Operational Base(0xFF4E0000) + offset (0x4034)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x40	selfref_to_x32 After this many clocks of the DDRC command channel being idle the uMCTL2 automatically puts the SDRAM into self-refresh. The DDRC command channel is considered idle when there are no HIF commands outstanding. This must be enabled in the PWRCTL.selfref_en. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x40 Programming Mode:Quasi-dynamic Group 4
15:8	RW	0x20	t_dpd_x4096 Minimum deep power-down time. For mDDR, value from the JEDEC specification is 0 as mDDR exits from deep power-down mode immediately after PWRCTL.deeppowerdown_en is de-asserted. For LPDDR2/LPDDR3, value from the JEDEC specification is 500us. Present only in designs configured to support mDDR, LPDDR2 or LPDDR3. FOR PERFORMANCE ONLY. Unit: Multiples of 4096 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x20 Programming Mode:Quasi-dynamic Group 4
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4:0	RW	0x10	powerdown_to_x32 After this many clocks of the DDRC command channel being idle the uMCTL2 automatically puts the SDRAM into power-down. The DDRC command channel is considered idle when there are no HIF commands outstanding. This must be enabled in the PWRCTL.powerdown_en. FOR PERFORMANCE ONLY. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x10 Programming Mode:Quasi-dynamic Group 4

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DDRCTL_FREQ3_RFSHCTL0

Address: Operational Base(0xFF4E0000) + offset (0x4050)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved4 Reserved Field:Yes
23:20	RW	0x2	refresh_margin Threshold value in number of DFI clock cycles before the critical refresh or page timer expires. A critical refresh is to be issued before this threshold is reached. It is recommended that this not be changed from the default value, currently shown as 0x2. It must always be less than internally used t_rfc_nom/32. Note that internally used t_rfc_nom is equal to RFSHTMG.t_rfc_nom_x1_x32 * 32 if RFSHTMG.t_rfc_nom_x1_sel=0. If RFSHTMG.t_rfc_nom_x1_sel=1 (for LPDDR2/LPDDR3/LPDDR4 per-bank refresh only), internally used t_rfc_nom is equal to RFSHTMG.t_rfc_nom_x1_x32. Note that, in LPDDR2/LPDDR3/LPDDR4, internally used t_rfc_nom may be divided by four if derating is enabled (DERATEEN.derate_enable=1). Unit: Multiples of 32 DFI clock cycles. Value After Reset:0x2 Programming Mode:Dynamic - Refresh Related
19:17	RW	0x0	Reserved3 Reserved Field:Yes
16:12	RW	0x10	refresh_to_x1_x32 If the refresh timer (tRFCnom, also known as tREFI) has expired at least once, then a speculative refresh may be performed. A speculative refresh is a refresh performed at a time when refresh would be useful. When the SDRAM bus is idle for a period of time determined by this RFSHCTL0.refresh_to_x1_x32 and the refresh timer has expired at least once since the last refresh, then a speculative refresh is performed. Speculative refreshes continues successively until there are no refreshes pending or until new reads or writes are issued to the uMCTL2. FOR PERFORMANCE ONLY. Unit: DFI clock cycles or multiples of 32 DFI clock cycles, depending on RFSHTMG.t_rfc_nom_x1_sel. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x10 Programming Mode:Dynamic - Refresh Related
11:10	RW	0x0	Reserved2 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
9:4	RW	0x00	refresh_burst The programmed value + 1 is the number of refresh timeouts that is allowed to accumulate before traffic is blocked and the refreshes are forced to execute. Closing pages to perform a refresh is a one-time penalty that must be paid for each group of refreshes. Therefore, performing refreshes in a burst reduces the per-refresh penalty of these page closings. Higher numbers for RFSHCTL.refresh_burst slightly increases utilization; lower numbers decreases the worst-case latency associated with refreshes. 0 - Single refresh 1 - Burst-of-2 refresh 7 - Burst-of-8 refresh For more information on burst refresh feature, see section 3.9 of DDR2 JEDEC specification - JESD79-2F.pdf. For DDR2/3, the refresh is always per-rank and not per-bank. The rank refresh can be accumulated over 8*tREFI cycles using the burst refresh feature. In DDR4 mode, according to Fine Granularity feature, 8 refreshes can be postponed in 1X mode, 16 refreshes in 2X mode and 32 refreshes in 4X mode. If using PHY-initiated updates, care must be taken in the setting of RFSHCTL0.refresh_burst, to ensure that tRFCmax is not violated due to a PHY-initiated update occurring shortly before a refresh burst is due. In this situation, the refresh burst is delayed until the PHY-initiated update is complete. In per-bank refresh mode of LPDDR2/LPDDR3/LPDDR4 (RFSHCTL0.per_bank_refresh = 1), 64 refreshes can be postponed. Value After Reset:0x0 Programming Mode:Dynamic - Refresh Related
3	RW	0x0	Reserved1 Reserved Field:Yes
2	RW	0x0	per_bank_refresh 1 - Per bank refresh 0 - All bank refresh Per bank refresh allows traffic to flow to other banks. Per bank refresh is not supported by all LPDDR2 devices but must be supported by all LPDDR3/LPDDR4 devices. Present only in designs configured to support LPDDR2/LPDDR3/LPDDR4. Value After Reset:0x0 Programming Mode:Static
1:0	RW	0x0	Reserved0 Reserved Field:Yes

DDRCTL_FREQ3_RFSHTMG

Address: Operational Base(0xFF4E0000) + offset (0x4064)

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Bit	Attr	Reset Value	Description
31	RW	0x0	t_rfc_nom_x1_sel Specifies whether the RFSHTMG.t_rfc_nom_x1_x32 and RFSHCTL0.refresh_to_x1_x32 register values are x1 or x32. 0 - x32 register values are used 1 - x1 register values are used This applies only when per-bank refresh is enabled (RFSHCTL0.per_bank_refresh=1); if per-bank refresh is not enabled, the x32 register values are used and this register field is ignored. This register field does not exist for configurations which do not support LPDDR2/3/4. For such configurations, the value of this register field can be assumed to be 0, so that RFSHTMG.t_rfc_nom_x1_x32 and RFSHCTL0.refresh_t_x1_x32 are interpreted as x32 register fields Value After Reset:0x0 Programming Mode:Dynamic - Refresh Related
30:28	RW	0x0	Reserved1 Reserved Field:Yes
27:16	RW	0x062	t_rfc_nom_x1_x32 Average time interval between refreshes per rank (Specification: 7.8us for DDR2, DDR3 and DDR4. See JEDEC specification for mDDR, LPDDR2, LPDDR3 and LPDDR4). When the controller is operating in 1:1 mode, set this register to RoundDown(tREFI/tCK) When the controller is operating in 1:2 mode, set this register to RoundDown(RoundDown(tREFI/tCK)/2) In both the previous cases, if RFSHTMG.t_rfc_nom_x1_sel = 0, divide the previous result by 32 and round down. For LPDDR2/LPDDR3/LPDDR4: If using all-bank refreshes (RFSHCTL0.per_bank_refresh = 0), use tREFIab in the previous calculations If using per-bank refreshes (RFSHCTL0.per_bank_refresh = 1), use tREFIpb in the previous calculations For DDR4 mode, tREFI value is different depending on the refresh mode. You must program appropriate value from the spec based on the value programmed in the refresh mode register. Note: RFSHTMG.t_rfc_nom_x1_x32 must be greater than 0x1 If RFSHTMG.t_rfc_nom_x1_sel == 1, RFSHTMG.t_rfc_nom_x1_x32 must be greater than RFSHTMG.t_rfc_min If RFSHTMG.t_rfc_nom_x1_sel == 0, RFSHTMG.t_rfc_nom_x1_x32 * 32 must be greater than RFSHTMG.t_rfc_min In non-DDR4 or DDR4 Fixed 1x mode: RFSHTMG.t_rfc_nom_x1_x32 must be less than or equal to 0xFFE In DDR4 Fixed 2x mode: RFSHTMG.t_rfc_nom_x1_x32 must be less than or equal to 0x7FF In DDR4 Fixed 4x mode: RFSHTMG.t_rfc_nom_x1_x32 must be less than or equal to 0x3FF Unit: DFI clock cycles or multiples of 32 DFI clock cycles, depending on RFSHTMG.t_rfc_nom_x1_sel. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x62 Programming Mode:Dynamic - Refresh Related

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Bit	Attr	Reset Value	Description
15	RW	0x0	lpddr3_trefbw_en Used only when LPDDR3 memory type is connected. Must only be changed when uMCTL2 is in reset. Specifies whether to use the tREFBW parameter (required by some LPDDR3 devices which comply with earlier versions of the LPDDR3 JEDEC specification) or not: 0 - tREFBW parameter not used 1 - tREFBW parameter used Value After Reset:0x0 Programming Mode:Static
14:10	RW	0x00	Reserved0 Reserved Field:Yes
9:0	RW	0x08c	t_rfc_min tRFC (min): Minimum time from refresh to refresh or activate. When the controller is operating in 1:1 mode, t_rfc_min must be set to RoundUp(tRFCmin/tCK). When the controller is operating in 1:2 mode, t_rfc_min must be set to RoundUp(RoundUp(tRFCmin/tCK)/2). In LPDDR2/LPDDR3/LPDDR4 mode: If using all-bank refreshes, the tRFCmin value in the previous equations is equal to tRFCab If using per-bank refreshes, the tRFCmin value in the previous equations is equal to tRFCpb In DDR4 mode, the tRFCmin value in the previous equations is different depending on the refresh mode (fixed 1X,2X,4X) and the device density. You must program the appropriate value from the spec based on the 'refresh_mode' and the device density that is used. Unit: DFI clock cycles. Value After Reset:0x8c Programming Mode:Dynamic - Refresh Related

DDRCTL_FREQ3_RFSHTMG1

Address: Operational Base(0xFF4E0000) + offset (0x4068)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Reserved1 Reserved Field:Yes
23:16	RW	0x8c	t_pbr2pbr LPDDR4:tpbR2pbR. Per-bank refresh to Per-bank refresh different bank Time. When the controller is operating in 1:1 frequency ratio mode, program this to RoundUp(tpbR2pbR/tCK). When the controller is operating in 1:2 frequency ratio mode, program this to RoundUp(RoundUp(tpbR2pbR/tCK)/2). The tpbR2pbR value in the previous equations is different depending on the device density. You must program the appropriate value from the specification. Register is valid only in LPDDR4 per-bank refresh mode (RFSHCTL0.per_bank_refresh_mode == 1). Value After Reset:0x8c Programming Mode:Dynamic - Refresh Related
15:0	RW	0x0000	Reserved0 Reserved Field:Yes

DDRCTL_FREQ3_INIT3

Address: Operational Base(0xFF4E0000) + offset (0x40DC)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr DDR2:Indicates the value to write to MR register. Bit 8 is for DLL and the setting here is ignored. The uMCTL2 sets this bit appropriately. DDR3/DDR4: Value loaded into MR0 register. mDDR: Value to write to MR register. LPDDR2/LPDDR3/LPDDR4 - Value to write to MR1 register Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 1, Group 4
15:0	RW	0x0510	emr DDR2: Indicates the value to write to EMR register. Bits 9:7 are for OCD and the setting in this register is ignored. The uMCTL2 sets those bits appropriately. DDR3/DDR4: Value to write to MR1 register Set bit 7 to 0. mDDR: Value to write to EMR register. LPDDR2/LPDDR3/LPDDR4 - Value to write to MR2 register. Value After Reset:0x510 Programming Mode:Quasi-dynamic Group 4

DDRCTL_FREQ3_INIT4

Address: Operational Base(0xFF4E0000) + offset (0x40E0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	emr2 DDR2: Indicates the value to write to EMR2 register. DDR3/DDR4: Value to write to MR2 register. LPDDR2/LPDDR3/LPDDR4: Value to write to MR3 register. mDDR: Unused. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 4
15:0	RW	0x0000	emr3 DDR2: Indicates the value to write to EMR3 register. DDR3/DDR4: Value to write to MR3 register. mDDR/LPDDR2/LPDDR3: Unused. LPDDR4: Value to write to MR13 register. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ3_INIT6

Address: Operational Base(0xFF4E0000) + offset (0x40E8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr4 DDR4 - Indicates the value to be loaded into SDRAM MR4 registers. LPDDR4- Value to be loaded into SDRAM MR11 registers. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4
15:0	RW	0x0000	mr5 DDR4 - Indicates the value to be loaded into SDRAM MR5 registers. LPDDR4- Value to be loaded into SDRAM MR12 registers. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 1, Group 4

DDRCTL_FREQ3_INIT7

Address: Operational Base(0xFF4E0000) + offset (0x40EC)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr22 LPDDR4 - Indicates the value to be loaded into SDRAM MR22 registers. Used in LPDDR4 designs only. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 4
15:0	RW	0x0000	mr6 DDR4 - Indicates the value to be loaded into SDRAM MR6 registers. LPDDR4- Value to be loaded into SDRAM MR14 registers. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 4

DDRCTL_FREQ3_RANKCTL

Address: Operational Base(0xFF4E0000) + offset (0x40F4)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	Reserved2 Reserved Field:Yes
26	RW	0x0	diff_rank_wr_gap_msb Only present for multi-rank configurations. 1-bit extension to be used when RANKCTL.diff_rank_wr_gap field needs to be set to a value greater than 0xF. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2
25	RW	0x0	Reserved1 Reserved Field:Yes
24	RW	0x0	diff_rank_rd_gap_msb Only present for multi-rank configurations. 1-bit extension to be used when RANKCTL.diff_rank_rd_gap field needs to be set to a value greater than 0xF. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2
23:16	RW	0x00	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
15:12	RW	0x0	max_rank_wr Only present for multi-rank configurations. Background: Writes to the same rank can be performed back-to-back. Writes to different ranks require additional gap dictated by the register RANKCTL.diff_rank_wr_gap. This is to avoid possible data bus contention as well as to give PHY enough time to switch the delay when changing ranks. The uMCTL2 arbitrates for bus access on a cycle-by-cycle basis; therefore after a write is scheduled, there are few clock cycles (determined by the value on RANKCTL.diff_rank_wr_gap register) in which only writes from the same rank are eligible to be scheduled. This prevents writes from other ranks from having fair access to the data bus. This parameter represents the maximum number of writes that can be scheduled consecutively to the same rank. After this number is reached, a delay equal to RANKCTL.diff_rank_wr_gap is inserted by the scheduler to allow all ranks a fair opportunity to be scheduled. Higher numbers increase bandwidth utilization, lower numbers increase fairness. This feature can be DISABLED by setting this register to 0. When set to 0, the controller stays on the same rank as long as commands are available for it. Minimum programmable value is 0 (feature disabled) and maximum programmable value is 0xF. For uPCTL2, this register field must be set to 0 (feature disabled) FOR PERFORMANCE ONLY. Value After Reset:0x0 Programming Mode:Static

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Bit	Attr	Reset Value	Description
11:8	RW	0x6	diff_rank_wr_gap Only present for multi-rank configurations. Indicates the number of clocks of gap in data responses when performing consecutive writes to different ranks. This is used to switch the delays in the PHY to match the rank requirements. This value must consider both PHY requirement and ODT requirement. PHY requirement - tphy_wrcsgap (For more information on value of tphy_wrcsgap, see PHY databook) ODT requirement - The value programmed in this register takes care of the ODT switch off timing requirement when switching ranks during writes. For LPDDR4, with DQ ODT enabled, diff_rank_wr_gap must be a minimum of ODTLoff - ODTLon - BL/2 + 1 For other cases, diff_rank_wr_gap must be a minimum of ODTCFG.wr_odt_hold - BL/2 When the controller is operating in 1:1 mode, program this to the larger of PHY requirement or ODT requirement. If CRC is enabled, the value can be decreased by 2 because the programmed value is internally increased by 1 (it is always 2 in terms of DFI PHY clock cycle as CRC is supported only with 1:2 frequency ratio). When the controller is operating in 1:2 mode, program this to the larger value divided by two and round it up to the next integer. After PHY has completed training the value programmed may need to be increased. For more information, see relevant PHY documentation. Note that, if using DDR4-LRDIMM, refer to TWRWR timing requirements in JEDEC DDR4 Data Buffer (DDR4DB01) Specification. If a value greater than 0xF is needed, the RANKCTL.diff_rank_wr_gap_msb field must be used as extension. For DFI 1:2 mode, a maximum value of {diff_rank_wr_gap_msb,diff_rank_wr_gap} < 'h11 is supported. For DFI 1:1 mode a maximum value of {diff_rank_wr_gap_msb,diff_rank_wr_gap} <= 'h1F is supported. Unit: DFI clock cycles. Value After Reset:0x6 Programming Mode:Quasi-dynamic Group 2
7:4	RW	0x6	diff_rank_rd_gap Only present for multi-rank configurations. Indicates the number of clocks of gap in data responses when performing consecutive reads to different ranks. This is used to switch the delays in the PHY to match the rank requirements. This value must consider both PHY requirement and ODT requirement. PHY requirement:tphy_rdcsgap (For more information on value of tphy_rdcsgap, see PHY databook) ODT requirement: The value programmed in this register takes care of the ODT switch off timing requirement when switching ranks during reads: Value After Reset:0x6 Programming Mode:Quasi-dynamic Group 2

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	max_rank_rd Only present for multi-rank configurations. Background: Reads to the same rank can be performed back-to-back. Reads to different ranks require additional gap dictated by the register RANKCTL.diff_rank_rd_gap. This is to avoid possible data bus contention as well as to give PHY enough time to switch the delay when changing ranks. The uMCTL2 arbitrates for bus access on a cycle-by-cycle basis; therefore after a read is scheduled, there are few clock cycles (determined by the value on RANKCTL.diff_rank_rd_gap register) in which only reads from the same rank are eligible to be scheduled. This prevents reads from other ranks from having fair access to the data bus. This parameter represents the maximum number of reads that can be scheduled consecutively to the same rank. After this number is reached, a delay equal to RANKCTL.diff_rank_rd_gap is inserted by the scheduler to allow all ranks a fair opportunity to be scheduled. Higher numbers increase bandwidth utilization, lower numbers increase fairness. This feature can be DISABLED by setting this register to 0. When set to 0, the controller stays on the same rank as long as commands are available for it. Minimum programmable value is 0 (feature disabled) and maximum programmable value is 0xF. For uPCTL2, this register field must be set to 0 (feature disabled) FOR PERFORMANCE ONLY. Value After Reset:0x0 Programming Mode:Static

DDRCTL_FREQ3_DRAMTMG0

Address: Operational Base(0xFF4E0000) + offset (0x4100)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved3 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
30:24	RW	0x0f	wr2pre Specifies the minimum time between write and precharge to same bank. Specifications: WL + BL/2 + tWR = approximately 8 cycles + 15 ns = 14 clocks @400MHz and less for lower frequencies. where: WL: Write latency BL: Burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM. BST (burst terminate) is not supported at present tWR: Write recovery time. This comes directly from the SDRAM specification Add one extra cycle for LPDDR2/LPDDR3/LPDDR4 for this parameter. When the controller is operating in 1:2 frequency ratio mode, 1T mode, divide the previous value by 2. No rounding up. When the controller is operating in 1:2 frequency ratio mode, 2T mode, geardown mode or LPDDR4 mode, divide the previous value by 2 and round it up to the next integer value. Note that, depending on the PHY, if using LRDIMM, it may be necessary to adjust the value of this parameter to compensate for the extra cycle of latency through the LRDIMM. For DDR4, LPDDR4, LPDDR3, using nWR(WR) instead of tWR to calculate the value of this parameter. Unit: DFI clock cycles. Value After Reset:0xf Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
23:22	RW	0x0	Reserved2 Reserved Field:Yes
21:16	RW	0x10	t_faw tFAW - valid only when 8 or more banks(or banks x bank groups) are present. In 8-bank design, at most 4 banks must be activated in a rolling window of tFAW cycles. When the controller is operating in 1:2 frequency ratio mode, program this to (tFAW/2) and round up to next integer value. In a 4-bank design, set this register to 0x1 independent of the 1:1/1:2 frequency mode. Unit: DFI clock cycles. Value After Reset:0x10 Programming Mode:Quasi-dynamic Group 2, Group 4
15	RW	0x0	Reserved1 Reserved Field:Yes
14:8	RW	0x1b	t_ras_max tRAS(max) - Specifies the maximum time between activate and precharge to same bank. This is the maximum time that a page can be kept open Minimum value of this register is 1. Zero is invalid. When the controller is operating in 1:1 frequency ratio mode, t_ras_max must be set to RoundDown(tRAS(max)/tCK/1024). When the controller is operating in 1:2 frequency ratio mode, t_ras_max must be set to RoundDown((RoundDown(tRAS(max)/tCK/1024)-1)/2). Unit: Multiples of 1024 DFI clock cycles. Value After Reset:0x1b Programming Mode:Quasi-dynamic Group 2, Group 4

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Bit	Attr	Reset Value	Description
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5:0	RW	0x0f	t_ras_min tRAS(min) - Specifies the minimum time between activate and precharge to the same bank. When the controller is operating in 1:1 frequency ratio mode, t_ras_min must be set to RoundUp(tRASmin/tCK) When the controller is operating in 1:2 frequency ratio mode, 1T mode, t_ras_min must be set to RoundDown(RoundUp(tRASmin/tCK)/2) When the controller is operating in 1:2 frequency ratio mode, 2T mode, geardown mode or LPDDR4 mode, t_ras min must be set to RoundUp(RoundUp(tRASmin/tCK)/2) Unit: DFI clock cycles. Value After Reset:0xf Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ3_DRAMTMG1

Address: Operational Base(0xFF4E0000) + offset (0x4104)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved2 Reserved Field:Yes
20:16	RW	0x08	t_xp tXP - Specifies the minimum time after power-down exit to any operation. For DDR3, this must be programmed to tXPDLL if slow powerdown exit is selected in MR0[12]. If C/A parity for DDR4 is used, set to (tXP+PL) instead. If LPDDR4 is selected and its spec has tCKELPD parameter, set to the larger of tXP and tCKELPD instead. When the controller is operating in 1:2 frequency ratio mode, program this to (tXP/2) and round it up to the next integer value. Units: DFI clock cycles. Value After Reset:0x8 Programming Mode:Quasi-dynamic Group 2, Group 4
15:14	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
13:8	RW	0x04	rd2pre tRTP - Specifies the minimum time from read to precharge of same bank. DDR2 - tAL + BL/2 + max(RoundUp(tRTP/tCK), 2) - 2 DDR3 - tAL + max (RoundUp(tRTP/tCK), 4) DDR4 - Max of following two equations: tAL + max (RoundUp(tRTP/tCK), 4) or, RL + BL/2 - tRP (*). mDDR - BL/2 LPDDR2 - Depends on if it is LPDDR2-S2 or LPDDR2-S4: LPDDR2-S2: BL/2 + RoundUp(tRTP/tCK) - 1. LPDDR2-S4: BL/2 + max(RoundUp(tRTP/tCK),2) - 2. LPDDR3 - BL/2 + max(RoundUp(tRTP/tCK),4) - 4 LPDDR4 - BL/2 + max(RoundUp(tRTP/tCK),8) - 8 (*) When both DDR4 SDRAM and ST-MRAM are used simultaneously, use SDRAM's tRP value for calculation. When the controller is operating in 1:2 mode, 1T mode, divide the previous value by 2. No rounding up. When the controller is operating in 1:2 mode, 2T mode, geardown mode or LPDDR4 mode, divide the previous value by 2 and round it up to the next integer value. For DDR4, using RTP instead of tRTP to calculate the value of this parameter. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
7	RW	0x0	Reserved0 Reserved Field:Yes
6:0	RW	0x14	t_rc tRC - Specifies the minimum time between activates to same bank. When the controller is operating in 1:2 frequency ratio mode, program this to (tRC/2) and round up to next integer value. Unit: DFI clock cycles. Value After Reset:0x14 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ3_DRAMTMG2

Address: Operational Base(0xFF4E0000) + offset (0x4108)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved3 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
29:24	RW	0x03	write_latency Set this field to WL. Indicates the Time from write command to write data on SDRAM interface. This must be set to WL. For mDDR, it must be set to 1. Note that, depending on the PHY, if using RDIMM/LRDIMM, it might be necessary to adjust the value of WL to compensate for the extra cycle of latency through the RDIMM/LRDIMM. When the controller is operating in 1:2 frequency ratio mode, divide the value calculated using the previous equation by 2, and round it up to next integer. This register field is not required for DDR2 and DDR3, as the DFI read and write latencies defined in DFITMG0 and DFITMG1 are sufficient for those protocols For all protocols, in addition to programming this register field, it is necessary to program DFITMG0 and DFITMG1 to control the read and write latencies Unit: DFI clock cycles. Value After Reset:0x3 Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
23:22	RW	0x0	Reserved2 Reserved Field:Yes
21:16	RW	0x05	read_latency Set this field to RL. Indicates the time from read command to read data on SDRAM interface. This must be set to RL. Note that, depending on the PHY, if using RDIMM/LRDIMM, it might be necessary to adjust the value of RL to compensate for the extra cycle of latency through the RDIMM/LRDIMM. When the controller is operating in 1:2 frequency ratio mode, divide the value calculated using the previous equation by 2, and round it up to next integer. This register field is not required for DDR2 and DDR3, as the DFI read and write latencies defined in DFITMG0 and DFITMG1 are sufficient for those protocols For all protocols, in addition to programming this register field, it is necessary to program DFITMG0 and DFITMG1 to control the read and write latencies Unit: DFI clock cycles. Value After Reset:0x5 Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
15:14	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
13:8	RW	0x06	rd2wr Minimum time from read command to write command. This must include time for bus turnaround (both within ranks and between ranks) and all PHY and system requirements. After the PHY has completed training, the value programmed may need to be increased. Please see the relevant PHY databook for details of what should be included here. The following calculations are minimum values, and do not include the PHY/system requirements mentioned above: DDR2/3/mDDR: RL + BL/2 + 2 - WL DDR4: RL + BL/2 + 1 + WR_PREAMBLE - WL LPDDR2/LPDDR3: RL + BL/2 + RU(tDQSCKmax/tCK) + 1 - WL LPDDR4(DQ ODT is Disabled): RL + BL/2 + RU(tDQSCKmax/tCK) + WR_PREAMBLE + RD_POSTAMBLE - WL LPDDR4(DQ ODT is Enabled): RL + BL/2 + RU(tDQSCKmax/tCK) + RD_POSTAMBLE - ODTLon - RU(tODTon(min)/tCK) + 1 Where: WL: Write latency BL: Burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM RL: Read latency = CAS latency WR_PREAMBLE: 1 (1tCK write preamble), 2 (2tCK write preamble). This is unique to DDR4 and LPDDR4 RD_POSTAMBLE: 0.5 (0.5tCK read postamble), 1.5 (1.5tCK read postamble). This is unique to LPDDR4 For LPDDR2/LPDDR3/LPDDR4, if derating is enabled (DERATEEN.derate_enable=1), derated tDQSCKmax must be used. When the controller is operating in 1:2 frequency ratio mode, divide the value calculated using the previous equation by 2, and round it up to next integer. Note that, depending on the PHY, if using LRDIMM, it may be necessary to adjust the value of this parameter to compensate for the extra cycle of latency through the LRDIMM. Unit: DFI clock cycles. Value After Reset:0x6 Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
7:6	RW	0x0	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
5:0	RW	0x0d	wr2rd In DDR4, minimum time from write command to read command for same bank group. In other protoocls, minimum time from write command to read command. This must include time for bus turn-around and all PHY and system requirements. After the PHY has completed training, the value programmed may need to be increased. Please see the relevant PHY databook for details of what should be included here. The following calculations are minimum values, and do not include the PHY/system requirements mentioned above: DDR4: CWL + PL + BL/2 + tWTR_L LPDDR2/3/4: WL + BL/2 + tWTR + 1 Others: CWL + BL/2 + tWTR Where: CWL: CAS write latency WL: Write latency PL: Parity latency BL: Burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM tWTR_L: Internal write to read command delay for same bank group. This comes directly from the SDRAM specification tWTR: Internal write to read command delay. This comes directly from the SDRAM specification Add one extra cycle for LPDDR2/LPDDR3/LPDDR4 operation. WTR_L must be increased by one if DDR4 2tCK write preamble is used. When the controller is operating in 1:2 mode, divide the value calculated using the previous equation by 2, and round it up to next integer. If your configuration has RANKCTL1.wr2rd_dr, write to read bus turn-around between different physical ranks are controlled by RANKCTL1.wr2rd_dr. Unit: DFI clock cycles. Value After Reset:0xd Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_FREQ3_DRAMTMG3

Address: Operational Base(0xFF4E0000) + offset (0x410C)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved2 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
29:20	RW	0x005	t_mrw Indicates the time to wait after a mode register write or read (MRW or MRR). Present only in designs configured to support LPDDR2, LPDDR3 or LPDDR4. LPDDR2 typically requires value of 5. LPDDR3 typically requires value of 10. LPDDR4: Set this to the larger of tMRW and tMRWCKEL. For LPDDR2, this register is used for the time from a MRW/MRR to all other commands. When the controller is operating in 1:2 frequency ratio mode, program this to the previous values divided by 2 and round it up to the next integer value. For LDPDR3, this register is used for the time from a MRW/MRR to a MRW/MRR. Unit: DFI clock cycles. Value After Reset:0x5 Programming Mode:Quasi-dynamic Group 2, Group 4
19:18	RW	0x0	Reserved1 Reserved Field:Yes
17:12	RW	0x04	t_mrd tMRD- Indicates the number of cycles to wait after a mode register write or read. Depending on the connected SDRAM, tMRD represents: DDR2/mDDR: Time from MRS to any command DDR3/4: Time from MRS to MRS command LPDDR2: not used LPDDR3/4: Time from MRS to non-MRS command When the controller is operating in 1:2 frequency ratio mode, program this to (tMRD/2) and round it up to the next integer value. If C/A parity for DDR4 is used, set to tMRD_PAR(tMOD+PL) instead. If CAL mode is enabled (DFITMG1.dfi_t_cmd_lat > 0), tCAL (=DFITMG1.dfi_cmd_lat) must be added to the previous calculations. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 2, Group 4
11:10	RW	0x0	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
9:0	RW	0x00c	t_mod tMOD - Parameter used only in DDR3 and DDR4. Indicates the number of cycles between load mode command and following non-load mode command. If C/A parity for DDR4 is used, set to tMOD_PAR(tMOD+PL) instead. If CAL mode is enabled (DFITMG1.dfi_t_cmd_lat > 0), tCAL (=DFITMG1.dfi_cmd_lat) must be added to the previous calculations. Set to tMOD if controller is operating in 1:1 frequency ratio mode, or tMOD/2 (rounded up to next integer) if controller is operating in 1:2 frequency ratio mode. Note that if using RDIMM/LRDIMM, depending on the PHY, it may be necessary to adjust the value of this parameter to compensate for the extra cycle of latency applied to mode register writes by the RDIMM/LRDIMM chip. Also note that if using RDIMM or LRDIMM, the minimum value of this register is tMRD_L2 if controller is operating in 1:1 frequency ratio mode, or tMRD_L2/2 (rounded up to next integer) if controller is operating in 1:2 frequency ratio mode. Unit: DFI clock cycles. Value After Reset:0xc Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ3_DRAMTMG4

Address: Operational Base(0xFF4E0000) + offset (0x4110)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved3 Reserved Field:Yes
28:24	RW	0x05	t_rcd tRCD - tAL: Indicates the minimum time from activate to read or write command to same bank. When the controller is operating in 1:2 frequency ratio mode, program this to ((tRCD - tAL)/2) and round it up to the next integer value. Minimum value allowed for this register is 1, which implies minimum (tRCD - tAL) value to be 2 when the controller is operating in 1:2 frequency ratio mode. Unit: DFI clock cycles. Value After Reset:0x5 Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4
23:20	RW	0x0	Reserved2 Reserved Field:Yes
19:16	RW	0x4	t_ccd DDR4: tCCD_L: This is the minimum time between two reads or two writes for same bank group. Others: tCCD: This is the minimum time between two reads or two writes. When the controller is operating in 1:2 frequency ratio mode, program this to (tCCD_L/2 or tCCD/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 2, Group 4
15:12	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
11:8	RW	0x4	t_rrd DDR4: tRRD_L: This is the minimum time between activates from bank "a" to bank "b" for same bank group. Others: tRRD: Minimum time between activates from bank "a" to bank "b" When the controller is operating in 1:2 frequency ratio mode, program this to (tRRD_L/2 or tRRD/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 2, Group 4
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4:0	RW	0x05	t_rp tRP: Indicates the minimum time from single-bank precharge to activate of same bank. When the controller is operating in 1:1 frequency ratio mode, t_rp must be set to RoundUp(tRP/tCK). When the controller is operating in 1:2 frequency ratio mode, t_rp must be set to RoundDown(RoundUp(tRP/tCK)/2) + 1. When the controller is operating in 1:2 frequency ratio mode in LPDDR4, t_rp must be set to RoundUp(RoundUp(tRP/tCK)/2). Unit: DFI clock cycles. Value After Reset:0x5 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ3_DRAMTMG5

Address: Operational Base(0xFF4E0000) + offset (0x4114)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved3 Reserved Field:Yes
27:24	RW	0x5	t_cksrx This is the time before self-refresh Exit that CK is maintained as a valid clock before issuing SRX. Specifies the clock stable time before SRX. Recommended settings: mDDR - 1 LPDDR2 - 2 LPDDR3 - 2 LPDDR4 - tCKCKEH DDR2 - 1 DDR3 - tCKSRX DDR4 - tCKSRX When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. Unit: DFI clock cycles. Value After Reset:0x5 Programming Mode:Quasi-dynamic Group 2, Group 4
23	RW	0x0	Reserved2 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
22:16	RW	0x05	t_cksre This is the time after self-refresh Down Entry that CK is maintained as a valid clock. Specifies the clock disable delay after SRE. Recommended settings: mDDR - 0 LPDDR2 - 2 LPDDR3 - 2 LPDDR4 - tCKELCK DDR2 - 1 DDR3 - Max (10 ns, 5 tCK) DDR4(No RDIMM) - Max (10 ns, 5 tCK) (+ PL(parity latency)(*)) DDR4(RDIMM) - Max (Max (10 ns, 5 tCK) (+ PL(parity latency)(*)), tCKOff) (*)Only if CRCPARCTL1.caparity_disable_before_sr=0, this register must be increased by PL. When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. Unit: DFI clock cycles. Value After Reset:0x5 Programming Mode:Quasi-dynamic Group 2, Group 4
15:14	RW	0x0	Reserved1 Reserved Field:Yes
13:8	RW	0x04	t_ckesr Indicates the minimum CKE low width for self-refresh or self-refresh power down entry to exit timing in memory clock cycles. Recommended settings: mDDR - tRFC LPDDR2 - tCKESR LPDDR3 - tCKESR LPDDR4 - max(tCKE, tSR) DDR2 - tCKE DDR3 - tCKE + 1 DDR4(No RDIMM) - tCKE + 1 (+ PL(parity latency)(*)) DDR4(RDIMM) - t_cksre + tCKEV (*)Only if CRCPARCTL1.caparity_disable_before_sr=0, this register must be increased by PL. When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 2, Group 4
7:5	RW	0x0	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
4:0	RW	0x03	t_cke Indicates the minimum number of cycles of CKE HIGH/LOW during power-down and self-refresh. LPDDR2/LPDDR3 mode - Set this to the larger of tCKE or tCKESR LPDDR4 mode - Set this to the larger of tCKE or tSR Non-LPDDR2/non-LPDDR3/non-LPDDR4 designs - Set this to tCKE value When the controller is operating in 1:2 frequency ratio mode, program this to (value described above)/2 and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x3 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ3_DRAMTMG6

Address: Operational Base(0xFF4E0000) + offset (0x4118)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved2 Reserved Field:Yes
27:24	RW	0x2	t_ckdpde This is the time after Deep Power Down Entry that CK is maintained as a valid clock. Specifies the clock disable delay after DPDE. Recommended settings: mDDR: 0 LPDDR2: 2 LPDDR3: 2 When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. This is only present for designs supporting mDDR or LPDDR2/LPDDR3 devices. Unit: DFI clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4
23:20	RW	0x0	Reserved1 Reserved Field:Yes
19:16	RW	0x2	t_ckdpdx This is the time before Deep Power Down Exit that CK is maintained as a valid clock before issuing DPDX. Specifies the clock stable time before DPDX. Recommended settings: mDDR - 1 LPDDR2 - 2 LPDDR3 - 2 When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. This is only present for designs supporting mDDR or LPDDR2 devices. Unit: DFI clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4
15:4	RW	0x000	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
3:0	RW	0x5	t_ckcsx This is the time before Clock Stop Exit that CK is maintained as a valid clock before issuing Clock Stop Exit. Specifies the clock stable time before next command after Clock Stop Exit. Recommended settings: mDDR - 1 LPDDR2 - tXP + 2 LPDDR3 - tXP + 2 LPDDR4 - tXP + 2 When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. This is only present for designs supporting mDDR or LPDDR2/LPDDR3/LPDDR4 devices. Unit: DFI clock cycles. Value After Reset:0x5 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ3_DRAMTMG7

Address: Operational Base(0xFF4E0000) + offset (0x411C)

Bit	Attr	Reset Value	Description
31:12	RW	0x00000	Reserved1 Reserved Field:Yes
11:8	RW	0x2	t_ckpde This is the time after Power Down Entry that CK is maintained as a valid clock. Specifies the clock disable delay after PDE. Recommended settings: mDDR - 0 LPDDR2 - 2 LPDDR3 - 2 LPDDR4 - tCKELCK When using DDR2/3/4 SDRAM, this register must be set to the same value as DRAMTMG5.t_cksre. When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. This is only present for designs supporting mDDR or LPDDR2/LPDDR3/LPDDR4 devices. Unit: DFI clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4
7:4	RW	0x0	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
3:0	RW	0x2	t_ckpdx This is the time before Power Down Exit that CK is maintained as a valid clock before issuing PDX. Specifies the clock stable time before PDX. Recommended settings: mDDR - 0 LPDDR2 - 2 LPDDR3 - 2 LPDDR4 - tCKCKEH When using DDR2/3/4 SDRAM, this register must be set to the same value as DRAMTMG5.t_cksrx. When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. This is only present for designs supporting mDDR or LPDDR2/LPDDR3/LPDDR4 devices. Unit: DFI clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ3_DRAMTMG8

Address: Operational Base(0xFF4E0000) + offset (0x4120)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved3 Reserved Field:Yes
30:24	RW	0x03	t_xs_fast_x32 tXS_FAST: Exit self-refresh to ZQCL, ZQCS and MRS (only CL, WR, RTP and Geardown mode). When the controller is operating in 1:2 frequency ratio mode, program this to the previous value divided by 2 and round up to next integer value. Note: This is applicable to only ZQCL/ZQCS commands. Note: Ensure this is less than or equal to t_xs_x32. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x3 Programming Mode:Quasi-dynamic Group 2, Group 4
23	RW	0x0	Reserved2 Reserved Field:Yes
22:16	RW	0x03	t_xs_abort_x32 tXS_ABORT: Exit self-refresh to commands not requiring a locked DLL in self-refresh Abort. When the controller is operating in 1:2 frequency ratio mode, program this to the previous value divided by 2 and round up to next integer value. Note: Ensure this is less than or equal to t_xs_x32. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x3 Programming Mode:Quasi-dynamic Group 2, Group 4
15	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
14:8	RW	0x44	t_xs_dll_x32 tXSDLL: Exit self-refresh to commands requiring a locked DLL. When the controller is operating in 1:2 frequency ratio mode, program this to the previous value divided by 2 and round up to next integer value. Note: Used only for DDR2, DDR3 and DDR4 SDRAMs. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x44 Programming Mode:Quasi-dynamic Group 2, Group 4
7	RW	0x0	Reserved0 Reserved Field:Yes
6:0	RW	0x05	t_xs_x32 tXS: Exit self-refresh to commands not requiring a locked DLL. When the controller is operating in 1:2 frequency ratio mode, program this to the previous value divided by 2 and round up to next integer value. Note: Used only for DDR2, DDR3 and DDR4 SDRAMs. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x5 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ3_DRAMTMG9

Address: Operational Base(0xFF4E0000) + offset (0x4124)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved3 Reserved Field:Yes
30	RW	0x0	ddr4_wr_preamble DDR4 Write preamble mode. 0 - 1tCK preamble 1 - 2tCK preamble Present only with MEMC_FREQ_RATIO=2. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4
29:19	RW	0x000	Reserved2 Reserved Field:Yes
18:16	RW	0x4	t_ccd_s tCCD_S: This is the minimum time between two reads or two writes for different bank group. When the controller is operating in 1:2 frequency ratio mode, program this to (tCCD_S/2) and round it up to the next integer value. Present only in designs configured to support DDR4. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 2, Group 4
15:12	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
11:8	RW	0x4	t_rrd_s tRRD_S: This is the minimum time between activates for different bank group. When the controller is operating in 1:2 frequency ratio mode, program this to (tRRD_S/2) and round it up to the next integer value. Present only in designs configured to support DDR4. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 2, Group 4
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5:0	RW	0x0d	wr2rd_s Minimum time from write command to read command for different bank group. This must include time for bus turn-around and all PHY and system requirements. After the PHY has completed training, the value programmed may need to be increased. Please see the relevant PHY databook for details of what should be included here. The following calculations are minimum values, and do not include the PHY/system requirements mentioned above: CWL + PL + BL/2 + tWTR_S Where: CWL: CAS write latency PL: Parity latency BL: Burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM tWTR_S: Internal write to read command delay for different bank group. This comes directly from the SDRAM specification WTR_S must be increased by one if DDR4 2tCK write preamble is used. When the controller is operating in 1:2 mode, divide the value calculated using the previous equation by 2, and round it up to next integer. If your configuration has RANKCTL1.wr2rd_dr, write to read bus turn-around between different physical ranks are controlled by RANKCTL1.wr2rd_dr. Unit: DFI clock cycles. Value After Reset:0xd Programming Mode:Quasi-dynamic Group 1, Group 2, Group 4

DDRCTL_FREQ3_DRAMTMG10

Address: Operational Base(0xFF4E0000) + offset (0x4128)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved2 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
20:16	RW	0x1c	t_sync_gear Indicates the time between MRS command and the sync pulse time. This must be even number of clocks. For DDR4-2666 and DDR4-3200, this parameter is defined as tMOD(min)+4nCK tMOD(min) is greater of 24nCK or 15ns 15ns / .625ns = 24 Max value for this register is 24+4 = 28 When the controller is operating in 1:2 mode, program this to (tSYNC_GEAR/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x1c Programming Mode:Quasi-dynamic Group 2, Group 4
15:13	RW	0x0	Reserved1 Reserved Field:Yes
12:8	RW	0x18	t_cmd_gear Indicates a sync pulse to first valid command. For DDR4-2666 and DDR4-3200, this parameter is defined as tMOD(min) tMOD(min) is greater of 24nCK or 15ns 15ns / .625ns = 24 Max value for this register is 24 When the controller is operating in 1:2 mode, program this to (tCMD_GEAR/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x18 Programming Mode:Quasi-dynamic Group 2, Group 4
7:4	RW	0x0	Reserved0 Reserved Field:Yes
3:2	RW	0x2	t_gear_setup Indicates the geardown setup time. Minimum value of this register is 1. Zero is invalid. For DDR4-2666 and DDR4-3200, this parameter is defined as 2 clks When the controller is operating in 1:2 frequency ratio mode, program this to (tGEAR_setup/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4
1:0	RW	0x2	t_gear_hold Indicates the geardown hold time. Minimum value of this register is 1. Zero is invalid. For DDR4-2666 and DDR4-3200, this parameter is defined as 2 clks When the controller is operating in 1:2 frequency ratio mode, program this to (tGEAR_hold/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ3_DRAMTMG11

Address: Operational Base(0xFF4E0000) + offset (0x412C)

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Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved3 Reserved Field:Yes
30:24	RW	0x44	post_mpsm_gap_x32 tXMPDLL: This is the minimum Exit MPSM to commands requiring a locked DLL. When the controller is operating in 1:2 frequency ratio mode, program this to (tXMPDLL/2) and round it up to the next integer value. Present only in designs configured to support DDR4. Unit: Multiples of 32 DFI clock cycles. For more information on how to program this register field, see "Note 1" in the "Notes on Timing Registers" section. Value After Reset:0x44 Programming Mode:Quasi-dynamic Group 2, Group 4
23:21	RW	0x0	Reserved2 Reserved Field:Yes
20:16	RW	0x0c	t_mpx_lh tMPX_LH: This is the minimum CS_n Low hold time to CKE rising edge. When the controller is operating in 1:2 frequency ratio mode, program this to RoundUp(tMPX_LH/2)+1. Present only in designs configured to support DDR4. Unit: DFI clock cycles. Value After Reset:0xc Programming Mode:Quasi-dynamic Group 2, Group 4
15:10	RW	0x00	Reserved1 Reserved Field:Yes
9:8	RW	0x2	t_mpx_s tMPX_S: This is the minimum time CS setup time to CKE. When the controller is operating in 1:2 frequency ratio mode, program this to (tMPX_S/2) and round it up to the next integer value. Present only in designs configured to support DDR4. Unit: DFI clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4:0	RW	0x1c	t_ckmpe tCKMPE: This is the minimum valid clock requirement after MPSM entry. Present only in designs configured to support DDR4. When the controller is operating in 1:2 frequency ratio mode, divide the value calculated using the previous equation by 2, and round it up to next integer. Unit: DFI clock cycles. Value After Reset:0x1c Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ3_DRAMTMG12

Address: Operational Base(0xFF4E0000) + offset (0x4130)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved2 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
29:24	RW	0x1a	t_wr_mpr This bit is used only in DDR4. Cycles between MPR Write and other command. Set this to tMOD + AL (or tMOD + PL + AL if C/A parity is also used). When the controller is operating in 1:2 frequency ratio mode, program this to (tWR_MPR/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x1a Programming Mode:Quasi-dynamic Group 2, Group 4
23:18	RW	0x00	Reserved1 Reserved Field:Yes
17:16	RW	0x2	t_cmdcke tCMDCKE: Indicates the delay from valid command to CKE input LOW. Set this to the larger of tESCKE or tCMDCKE When the controller is operating in 1:2 frequency ratio mode, program this to (max(tESCKE, tCMDCKE)/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4
15:5	RW	0x000	Reserved0 Reserved Field:Yes
4:0	RW	0x10	t_mrd_pda tMRD_PDA: This is the Mode Register Set command cycle time in PDA mode. When the controller is operating in 1:2 frequency ratio mode, program this to (tMRD_PDA/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x10 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ3_DRAMTMG13

Address: Operational Base(0xFF4E0000) + offset (0x4134)

Bit	Attr	Reset Value	Description
31	RW	0x0	Reserved2 Reserved Field:Yes
30:24	RW	0x1c	odtloff LPDDR4: ODTLoff: This is the latency from CAS-2 command to ODToff reference. When the controller is operating in 1:2 frequency ratio mode, program this to (ODTLoff/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x1c Programming Mode:Quasi-dynamic Group 2, Group 4
23:22	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
21:16	RW	0x20	t_ccd_mw LPDDR4: tCCDMW: This is the minimum time from write or masked write to masked write command for same bank. When the controller is operating in 1:2 frequency ratio mode, program this to (tCCDMW/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x20 Programming Mode:Quasi-dynamic Group 2, Group 4
15:3	RW	0x0000	Reserved0 Reserved Field:Yes
2:0	RW	0x4	t_ppd LPDDR4: tPPD: This is the minimum time from precharge to precharge command. When the controller is operating in 1:2 frequency ratio mode, program this to (tPPD/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ3_DRAMTMG14

Address: Operational Base(0xFF4E0000) + offset (0x4138)

Bit	Attr	Reset Value	Description
31:12	RW	0x00000	Reserved0 Reserved Field:Yes
11:0	RW	0x0a0	t_xsr tXSR: This is the exit self-refresh to any command. When the controller is operating in 1:2 frequency ratio mode, program this to the previous value divided by 2 and round up to next integer value. The value 0xfff is illegal for this register field. Note: Used only for mDDR/LPDDR2/LPDDR3/LPDDR4 mode. Unit: DFI clock cycles. Value After Reset:0xa0 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ3_DRAMTMG15

Address: Operational Base(0xFF4E0000) + offset (0x413C)

Bit	Attr	Reset Value	Description
31	RW	0x0	en_dfi_lp_t_stab 1 - Enable using tSTAB when exiting DFI LP. This must be set when the PHY is stopping the clock during DFI LP to save maximum power. 0 - Disable using tSTAB when exiting DFI LP. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4
30:8	RW	0x000000	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	t_stab_x32 tSTAB: Stabilization time. It is required in the following two cases for DDR3/DDR4 RDIMM: When exiting power saving mode, if the clock is stopped, after re-enabling it the clock must be stable for a time specified by tSTAB In the case of input clock frequency change (DDR4) After issuing control words that refers to clock timing (Specification: 6us for DDR3, 5us for DDR4) Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ3_ZQCTL0

Address: Operational Base(0xFF4E0000) + offset (0x4180)

Bit	Attr	Reset Value	Description
31	RW	0x0	dis_auto_zq 1 - Disable uMCTL2 generation of ZQCS/MPC(ZQ calibration) command. Register DBGCMD.zq_calib_short can be used instead to issue ZQ calibration request from APB module 0 - Internally generate ZQCS/MPC(ZQ calibration) commands based on ZQCTL1.t_zq_short_interval_x1024 This is only present for designs supporting DDR3/DDR4 or LPDDR2/LPDDR3/LPDDR4 devices. Value After Reset:0x0 Programming Mode:Dynamic
30	RW	0x0	dis_srx_zqcl 1 - Disable issuing of ZQCL/MPC(ZQ calibration) command at self-refresh/SR-Powerdown exit. Only applicable when run in DDR3 or DDR4 or LPDDR2 or LPDDR3 or LPDDR4 mode 0 - Enable issuing of ZQCL/MPC(ZQ calibration) command at self-refresh/SR-Powerdown exit. Only applicable when run in DDR3 or DDR4 or LPDDR2 or LPDDR3 or LPDDR4 mode This is only present for designs supporting DDR3/DDR4 or LPDDR2/LPDDR3/LPDDR4 devices. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4
29	RW	0x0	zq_resistor_shared 1 - Denotes that ZQ resistor is shared between ranks. Means ZQinit/ZQCL/ZQCS/MPC(ZQ calibration) commands are sent to one rank at a time with tZQinit/tZQCL/tZQCS/tZQCAL/tZQLAT timing met between commands so that commands to different ranks do not overlap 0 - ZQ resistor is not shared This is only present for designs supporting DDR3/DDR4 or LPDDR2/LPDDR3/LPDDR4 devices. Value After Reset:0x0 Programming Mode:Static

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Bit	Attr	Reset Value	Description
28	RW	0x0	dis_mpsmx_zqcl 1 - Disable issuing of ZQCL command at Maximum Power Saving Mode exit. Only applicable when run in DDR4 mode 0 - Enable issuing of ZQCL command at Maximum Power Saving Mode exit. Only applicable when run in DDR4 mode This is only present for designs supporting DDR4 devices. Note: Do not issue ZQCL command at Maximum Power Save Mode exit if the UMCTL2_SHARED_AC configuration parameter is set. Program it to 1'b1. The software can send ZQCS after exiting MPSM mode. Value After Reset:0x0 Programming Mode:Static
27	RW	0x0	Reserved1 Reserved Field:Yes
26:16	RW	0x200	t_zq_long_nop tZQoper for DDR3/DDR4, tZQCL for LPDDR2/LPDDR3, tZQCAL for LPDDR4: Number of DFI clock cycles of NOP required after a ZQCL (ZQ calibration long)/MPC(ZQ Start) command is issued to SDRAM. When the controller is operating in 1:2 frequency ratio mode: DDR3/DDR4: program this to tZQoper/2 and round it up to the next integer value. LPDDR2/LPDDR3: program this to tZQCL/2 and round it up to the next integer value. LPDDR4: program this to tZQCAL/2 and round it up to the next integer value. This is only present for designs supporting DDR3/DDR4 or LPDDR2/LPDDR3/LPDDR4 devices. Unit: DFI clock cycles. Value After Reset:0x200 Programming Mode:Static
15:10	RW	0x00	Reserved0 Reserved Field:Yes
9:0	RW	0x040	t_zq_short_nop tZQCS for DDR3/DD4/LPDDR2/LPDDR3, tZQLAT for LPDDR4: Number of DFI clock cycles of NOP required after a ZQCS (ZQ calibration short)/MPC(ZQ Latch) command is issued to SDRAM. When the controller is operating in 1:2 frequency ratio mode, program this to tZQCS/2 and round it up to the next integer value. This is only present for designs supporting DDR3/DDR4 or LPDDR2/LPDDR3/LPDDR4 devices. Unit: DFI clock cycles. Value After Reset:0x40 Programming Mode:Static

DDRCTL_FREQ3_DFITMG0

Address: Operational Base(0xFF4E0000) + offset (0x4190)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved2 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
28:24	RW	0x07	dfi_t_ctrl_delay Specifies the number of DFI clock cycles after an assertion or de-assertion of the DFI control signals that the control signals at the PHY-DRAM interface reflect the assertion or de-assertion. If the DFI clock and the memory clock are not phase-aligned, this timing parameter must be rounded up to the next integer value. Note that if using RDIMM/LRDIMM, it is necessary to increment this parameter by RDIMM's/LRDIMM's extra cycle of latency in terms of DFI clock. Unit: DFI clock cycles. Value After Reset:0x7 Programming Mode:Quasi-dynamic Group 4
23	RW	0x0	dfi_rddata_use_dfi_phy_clk Defines whether dfi_rddata_en/dfi_rddata/dfi_rddata_valid is generated using HDR (DFI clock) or SDR (DFI PHY clock) values. Selects whether value in DFITMG0.dfi_t_rddata_en is in terms of HDR (DFI clock) or SDR (DFI PHY clock) cycles: 0 in terms of HDR (DFI clock) cycles 1 in terms of SDR (DFI PHY clock) cycles Refer to PHY specification for correct value. If using a Synopsys DWC DDR3/2 PHY, DWC DDR2/3-Lite/mDDR PHY, DWC DDR multiPHY or DWC Gen2 DDR multiPHY, this field must be set to 0; otherwise: If MEMC_PROG_FREQ_RATIO=1 and MSTR.frequency_ratio=1, this field must be set to 0 Else, it must be set to 1 Value After Reset:0x0 Programming Mode:Static
22:16	RW	0x02	dfi_t_rddata_en Time from the assertion of a read command on the DFI interface to the assertion of the dfi_rddata_en signal. Refer to PHY specification for correct value. This corresponds to the DFI parameter trddata_en. Note that, depending on the PHY, if using RDIMM/LRDIMM, it may be necessary to use the adjusted value of CL in the calculation of trddata_en. This is to compensate for the extra cycles of latency through the RDIMM/LRDIMM. Unit: DFI clock cycles or DFI PHY clock cycles, depending on DFITMG0.dfi_rddata_use_dfi_phy_clk. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 1, Group 4

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Bit	Attr	Reset Value	Description
15	RW	0x0	dfi_wrdata_use_dfi_phy_clk Defines whether dfi_wrdata_en/dfi_wrdata/dfi_wrdata_mask is generated using HDR (DFI clock) or SDR (DFI PHY clock) values. Selects whether value in DFITMG0.dfi_tphy_wrlat is in terms of HDR (DFI clock) or SDR (DFI PHY clock) cycles. Selects whether value in DFITMG0.dfi_tphy_wrdata is in terms of HDR (DFI clock) or SDR (DFI PHY clock) cycles. 0 in terms of HDR (DFI clock) cycles 1 in terms of SDR (DFI PHY clock) cycles Refer to PHY specification for correct value. If using a Synopsys DWC DDR3/2 PHY, DWC DDR2/3-Lite/mDDR PHY, DWC DDR multiPHY or DWC Gen2 DDR multiPHY, this field must be set to 0; otherwise: If MEMC_PROG_FREQ_RATIO=1 and MSTR.frequency_ratio=1, this field must be set to 0 Else, it must be set to 1 Value After Reset:0x0 Programming Mode:Static
14	RW	0x0	Reserved1 Reserved Field:Yes
13:8	RW	0x00	dfi_tphy_wrdata Specifies the number of clock cycles between when dfi_wrdata_en is asserted to when the associated write data is driven on the dfi_wrdata signal. This corresponds to the DFI timing parameter tphy_wrdata. For more information on correct value, see PHY specification. Note, maximum supported value is 8. Unit: DFI clock cycles or DFI PHY clock cycles, depending on DFITMG0.dfi_wrdata_use_dfi_phy_clk. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 4
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5:0	RW	0x02	dfi_tphy_wrlat Write latency. Number of clocks from the write command to write data enable (dfi_wrdata_en). This corresponds to the DFI timing parameter tphy_wrlat. Refer to PHY specification for correct value.Note that, depending on the PHY, if using RDIMM/LRDIMM, it may be necessary to use the adjusted value of CL in the calculation of tphy_wrlat. This is to compensate for the extra cycles of latency through the RDIMM/LRDIMM. For LPDDR4, dfi_tphy_wrlat>60 is not supported. Unit: DFI clock cycles or DFI PHY clock cycles, depending on DFITMG0.dfi_wrdata_use_dfi_phy_clk. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ3_DFITMG1

Address: Operational Base(0xFF4E0000) + offset (0x4194)

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Bit	Attr	Reset Value	Description
31:28	RW	0x0	dfi_t_cmd_lat Specifies the number of DFI PHY clock cycles between when the dfi_cs signal is asserted and when the associated command is driven. This field is used for CAL mode, must be set to '0' or tCAL, which matches the CAL mode register setting in the DRAM. When enabling CAL mode with RDIMM/LRDIMM, this field must be set to tCAL-CLA (Command Latency Adder). For more information on CLA, see JEDEC DDR4 Register Specification. If the PHY can add the latency for CAL mode, this must be set to '0'. Valid Range: 0 to 8. Unit: DFI PHY clock cycles. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 2, Group 4
27:26	RW	0x0	Reserved3 Reserved Field:Yes
25:24	RW	0x0	dfi_t_parin_lat Specifies the number of DFI PHY clock cycles between when the dfi_cs signal is asserted and when the associated dfi_parity_in signal is driven. Unit: DFI PHY clock cycles. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 4
23:21	RW	0x0	Reserved2 Reserved Field:Yes
20:16	RW	0x00	dfi_t_wrdata_delay Specifies the number of DFI clock cycles between when the dfi_wrdata_en signal is asserted and when the corresponding write data transfer is completed on the DRAM bus. This corresponds to the DFI timing parameter twrdata_delay. For more information on correct value, see PHY specification. For DFI 3.0 PHY, set to twrdata_delay, a new timing parameter introduced in DFI 3.0. For DFI 2.1 PHY, set to tphy_wrdata + (delay of DFI write data to the DRAM). Value to be programmed is in terms of DFI clocks, not PHY clocks. In FREQ_RATIO=2, divide PHY's value by 2 and round up to next integer. If using DFITMG0.dfi_wrdata_use_dfi_phy_clk=1, add 1 to the value. Unit: DFI clock cycles. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 4
15:13	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
12:8	RW	0x04	dfi_t_dram_clk_disable Specifies the number of DFI clock cycles from the assertion of the dfi_dram_clk_disable signal on the DFI until the clock to the DRAM memory devices, at the PHY-DRAM boundary, maintains a low value. If the DFI clock and the memory clock are not phase aligned, this timing parameter must be rounded up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 4
7:5	RW	0x0	Reserved0 Reserved Field:Yes
4:0	RW	0x04	dfi_t_dram_clk_enable Specifies the number of DFI clock cycles from the de-assertion of the dfi_dram_clk_disable signal on the DFI until the first valid rising edge of the clock to the DRAM memory devices, at the PHY-DRAM boundary. If the DFI clock and the memory clock are not phase aligned, this timing parameter must be rounded up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 4

DDRCTL_FREQ3_DFITMG2

Address: Operational Base(0xFF4E0000) + offset (0x41B4)

Bit	Attr	Reset Value	Description
31:15	RW	0x00000	Reserved1 Reserved Field:Yes
14:8	RW	0x02	dfi_tphy_rdcslat specifies the number of DFI PHY clock cycles between when a read command is sent on the DFI control interface and when the associated dfi_rddata_cs signal is asserted. This corresponds to the DFI timing parameter tphy_rdcslat. Refer to PHY specification for correct value. Unit: DFI PHY clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4
7:6	RW	0x0	Reserved0 Reserved Field:Yes
5:0	RW	0x02	dfi_tphy_wrcslat Specifies the number of DFI PHY clock cycles between when a write command is sent on the DFI control interface and when the associated dfi_wrdata_cs signal is asserted. This corresponds to the DFI timing parameter tphy_wrcslat. For more information on correct value, see PHY specification. Unit: DFI PHY clock cycles. Value After Reset:0x2 Programming Mode:Quasi-dynamic Group 2, Group 4

DDRCTL_FREQ3_DFITMG3

Address: Operational Base(0xFF4E0000) + offset (0x41B8)

Bit	Attr	Reset Value	Description
31:5	RW	0x0000000	Reserved0 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
4:0	RW	0x00	dfi_t_geardown_delay The delay from dfi_geardown_en assertion to the time of the PHY being ready to receive commands. Refer to PHY specification for correct value. When the controller is operating in 1:2 frequency ratio mode, program this to (tgeardown_delay/2) and round it up to the next integer value. Unit: DFI clock cycles. Value After Reset:0x0 Programming Mode:Static

DDRCTL_FREQ3_ODTCFG

Address: Operational Base(0xFF4E0000) + offset (0x4240)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved4 Reserved Field:Yes
27:24	RW	0x4	wr_odt_hold DFI PHY clock cycles to hold ODT for a write command. The minimum supported value is 2. Recommended values: DDR2: BL8 - 0x5 (DDR2-400/533/667), 0x6 (DDR2-800), 0x7 (DDR2-1066) BL4 - 0x3 (DDR2-400/533/667), 0x4 (DDR2-800), 0x5 (DDR2-1066) DDR3: BL8 - 0x6 DDR4: BL8 - 5 + WR_PREAMBLE + CRC_MODE WR_PREAMBLE = 1 (1tCK write preamble), 2 (2tCK write preamble) CRC_MODE = 0 (not CRC mode), 1 (CRC mode) LPDDR3: BL8 - 7 + RU(tODTon(max)/tCK) Unit: DFI PHY clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 1, Group 4
23:21	RW	0x0	Reserved3 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
20:16	RW	0x00	wr_odt_delay Indicates the delay, in DFI PHY clock cycles, from issuing a write command to setting ODT values associated with that command. ODT setting must remain constant for the entire time that DQS is driven by the uMCTL2. Recommended values: DDR2: CWL + AL - 3 (DDR2-400/533/667), CWL + AL - 4 (DDR2-800), CWL + AL - 5 (DDR2-1066) If (CWL + AL - 3 < 0), uMCTL2 does not support ODT for write operation. DDR3: 0x0 DDR4: DFITMG1.dfi_t_cmd_lat (to adjust for CAL mode) LPDDR3: WL - 1 - RU(tODTon(max)/tCK)) Unit: DFI PHY clock cycles. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 1, Group 4
15:12	RW	0x0	Reserved2 Reserved Field:Yes
11:8	RW	0x4	rd_odt_hold DFI PHY clock cycles to hold ODT for a read command. The minimum supported value is 2. Recommended values: DDR2: BL8 - 0x6 (not DDR2-1066), 0x7 (DDR2-1066) BL4 - 0x4 (not DDR2-1066), 0x5 (DDR2-1066) DDR3: BL8 - 0x6 DDR4: BL8 - 5 + RD_PREAMBLE RD_PREAMBLE = 1 (1tCK read preamble), 2 (2tCK read preamble) LPDDR3: BL8 - 5 + RU(tDQSCK(max)/tCK) - RD(tDQSCK(min)/tCK) + RU(tODTon(max)/tCK) Unit: DFI PHY clock cycles. Value After Reset:0x4 Programming Mode:Quasi-dynamic Group 1, Group 4
7	RW	0x0	Reserved1 Reserved Field:Yes

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Bit	Attr	Reset Value	Description
6:2	RW	0x00	rd_odt_delay Indicates the delay, in DFI PHY clock cycles, from issuing a read command to setting ODT values associated with that command. ODT setting must remain constant for the entire time that DQS is driven by the uMCTL2. Recommended values: DDR2: CL + AL - 4 (not DDR2-1066), CL + AL - 5 (DDR2-1066) If (CL + AL - 4 < 0), uMCTL2 does not support ODT for read operation. DDR3: CL - CWL DDR4: CL - CWL - RD_PREAMBLE + WR_PREAMBLE + DFITMG1.dfi_t_cmd_lat (to adjust for CAL mode) WR_PREAMBLE = 1 (1tCK write preamble), 2 (2tCK write preamble) LPDDR3: RL + RD(tDQSCK(min)/tCK) - 1 - RU(tODTon(max)/tCK) Unit: DFI PHY clock cycles. Value After Reset:0x0 Programming Mode:Quasi-dynamic Group 1, Group 4
1:0	RW	0x0	Reserved0 Reserved Field:Yes

13.4.4 Registers Summary for DDRPHY

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
DDRPHY_BYTE0	0xFF4F0400
DDRPHY_BYTE1	0xFF4F0580
DDRPHY_BYTE2	0xFF4F0700
DDRPHY_BYTE3	0xFF4F0880

DDRPHY_COM Registers Summary:

Name	Offset	Size	Reset Value	Description
DDRPHY_COM_REG_0x0	0x0000	W	0x00000F87	REG_0x0
DDRPHY_COM_REG_0x1	0x0004	W	0x00000E38	REG_0x1
DDRPHY_COM_REG_0x2	0x0008	W	0x00000000	REG_0x2
DDRPHY_COM_REG_0x3	0x000C	W	0x06060606	REG_0x3
DDRPHY_COM_REG_0x4	0x0010	W	0x00000000	REG_0x4
DDRPHY_COM_REG_0x5	0x0014	W	0x00000000	REG_0x5
DDRPHY_COM_REG_0x6	0x0018	W	0xFFFFFFFF	REG_0x6
DDRPHY_COM_REG_0x7	0x001C	W	0x00C20023	REG_0x7
DDRPHY_COM_REG_0x8	0x0020	W	0x0000E400	REG_0x8
DDRPHY_COM_REG_0x9	0x0024	W	0x08F205FC	REG_0x9
DDRPHY_COM_REG_0xa	0x0028	W	0x1B280F1F	REG_0xa
DDRPHY_COM_REG_0xb	0x002C	W	0x00000000	REG_0xb
DDRPHY_COM_REG_0xc	0x0030	W	0x00000000	REG_0xc
DDRPHY_COM_REG_0xd	0x0034	W	0x3F001F1F	REG_0xd
DDRPHY_COM_REG_0xe	0x0038	W	0x88881148	REG_0xe

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Name	Offset	Size	Reset Value	Description
DDRPHY_COM_REG_0xf	0x003C	W	0x09FF1506	REG_0xf
DDRPHY_COM_REG_0x10	0x0040	W	0x06061515	REG_0x10
DDRPHY_COM_REG_0x11	0x0044	W	0x00300120	REG_0x11
DDRPHY_COM_REG_0x12	0x0048	W	0x0000403F	REG_0x12
DDRPHY_COM_REG_0x13	0x004C	W	0x00401000	REG_0x13
DDRPHY_COM_REG_0x14	0x0050	W	0x00000C10	REG_0x14
DDRPHY_COM_REG_0x15	0x0054	W	0x00010203	REG_0x15
DDRPHY_COM_REG_0x16	0x0058	W	0x04050607	REG_0x16
DDRPHY_COM_REG_0x17	0x005C	W	0x08090A0B	REG_0x17
DDRPHY_COM_REG_0x18	0x0060	W	0x0C0D0E0F	REG_0x18
DDRPHY_COM_REG_0x19	0x0064	W	0x10111213	REG_0x19
DDRPHY_COM_REG_0x1a	0x0068	W	0x14151617	REG_0x1a
DDRPHY_COM_REG_0x1b	0x006C	W	0x18191A1B	REG_0x1b
DDRPHY_COM_REG_0x1c	0x0070	W	0x1C1D1E00	REG_0x1c
DDRPHY_COM_REG_0x1d	0x0074	W	0x05380000	REG_0x1d
DDRPHY_COM_REG_0x1e	0x0078	W	0x00008101	REG_0x1e
DDRPHY_COM_REG_0x1f	0x007C	W	0x00000010	REG_0x1f
DDRPHY_COM_REG_0x20	0x0080	W	0x0001020B	REG_0x20
DDRPHY_COM_REG_0x21	0x0084	W	0x000759BF	REG_0x21
DDRPHY_COM_REG_0x22	0x0088	W	0x00161388	REG_0x22
DDRPHY_COM_REG_0x23	0x008C	W	0x1FF0FC08	REG_0x23
DDRPHY_COM_REG_0x24	0x0090	W	0x0E0E0707	REG_0x24
DDRPHY_COM_REG_0x25	0x0094	W	0x0F000000	REG_0x25
DDRPHY_COM_REG_0x26	0x0098	W	0x55555A3C	REG_0x26
DDRPHY_COM_REG_0x27	0x009C	W	0x00000000	REG_0x27
DDRPHY_COM_REG_0x28	0x00A0	W	0x01000400	REG_0x28
DDRPHY_COM_REG_0x29	0x00A4	W	0x00000001	REG_0x29
DDRPHY_COM_REG_0x2a	0x00A8	W	0x25808C80	REG_0x2a
DDRPHY_COM_REG_0x2b	0x00AC	W	0x00000000	REG_0x2b
DDRPHY_COM_REG_0x2c	0x00B0	W	0x00005555	REG_0x2c
DDRPHY_COM_REG_0x2d	0x00B4	W	0x00005555	REG_0x2d
DDRPHY_COM_REG_0x2e	0x00B8	W	0x00015555	REG_0x2e
DDRPHY_COM_REG_0x2f	0x00BC	W	0x00005555	REG_0x2f
DDRPHY_COM_REG_0x30	0x00C0	W	0x1A00607F	REG_0x30
DDRPHY_COM_REG_0x31	0x00C4	W	0x00000004	REG_0x31
DDRPHY_COM_REG_0x32	0x00C8	W	0x641F1F1F	REG_0x32
DDRPHY_COM_REG_0x33	0x00CC	W	0x0000005F	REG_0x33
DDRPHY_COM_REG_0x34	0x00D0	W	0x00000003	REG_0x34
DDRPHY_COM_REG_0x35	0x00D4	W	0x00000008	REG_0x35
DDRPHY_COM_REG_0x36	0x00D8	W	0x80808080	REG_0x36
DDRPHY_COM_REG_0x37	0x00DC	W	0x00000080	REG_0x37
DDRPHY_COM_REG_0x38	0x00E0	W	0x00003F3F	REG_0x38
DDRPHY_COM_REG_0x39	0x00E4	W	0x00000000	REG_0x39
DDRPHY_COM_REG_0x3a	0x00E8	W	0x00002400	REG_0x3a
DDRPHY_COM_REG_0x3b	0x00EC	W	0x007FFFFF	REG_0x3b
DDRPHY_COM_REG_0x3c	0x00F0	W	0x00002000	REG_0x3c
DDRPHY_COM_REG_0x3d	0x00F4	W	0x0E0E0E0E	REG_0x3d
DDRPHY_COM_REG_0x3e	0x00F8	W	0x00800E0E	REG_0x3e
DDRPHY_COM_REG_0x3f	0x00FC	W	0x00000000	REG_0x3f
DDRPHY_COM_REG_0x41	0x0104	W	0x80808080	REG_0x41
DDRPHY_COM_REG_0x42	0x0108	W	0x80808080	REG_0x42
DDRPHY_COM_REG_0x43	0x010C	W	0x80808080	REG_0x43

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Name	Offset	Size	Reset Value	Description
DDRPHY_COM_REG_0x44	0x0110	W	0x80808080	REG_0x44
DDRPHY_COM_REG_0x45	0x0114	W	0x80808080	REG_0x45
DDRPHY_COM_REG_0x46	0x0118	W	0x80808080	REG_0x46
DDRPHY_COM_REG_0x47	0x011C	W	0x80808080	REG_0x47
DDRPHY_COM_REG_0x48	0x0120	W	0x80808080	REG_0x48
DDRPHY_COM_REG_0x54	0x0150	W	0x5AA5C33C	REG_0x54
DDRPHY_COM_REG_0x55	0x0154	W	0xFF5500AA	REG_0x55
DDRPHY_COM_REG_0x56	0x0158	W	0x0000F00F	REG_0x56
DDRPHY_COM_REG_0x57	0x015C	W	0xA55A3CC3	REG_0x57
DDRPHY_COM_REG_0x58	0x0160	W	0x00AAFF55	REG_0x58
DDRPHY_COM_REG_0x59	0x0164	W	0x00000FF0	REG_0x59
DDRPHY_COM_REG_0x5a	0x0168	W	0x5AA5C33C	REG_0x5a
DDRPHY_COM_REG_0x5b	0x016C	W	0xFF5500AA	REG_0x5b
DDRPHY_COM_REG_0x5c	0x0170	W	0x0000F00F	REG_0x5c
DDRPHY_COM_REG_0x5d	0x0174	W	0xA55A3CC3	REG_0x5d
DDRPHY_COM_REG_0x5e	0x0178	W	0x00AAFF55	REG_0x5e
DDRPHY_COM_REG_0x5f	0x017C	W	0x00000FF0	REG_0x5f
DDRPHY_COM_REG_0x60	0x0180	W	0x5AA5C33C	REG_0x60
DDRPHY_COM_REG_0x61	0x0184	W	0xFF5500AA	REG_0x61
DDRPHY_COM_REG_0x62	0x0188	W	0x0000F00F	REG_0x62
DDRPHY_COM_REG_0x63	0x018C	W	0xA55A3CC3	REG_0x63
DDRPHY_COM_REG_0x64	0x0190	W	0x00AAFF55	REG_0x64
DDRPHY_COM_REG_0x65	0x0194	W	0x00000FF0	REG_0x65
DDRPHY_COM_REG_0x66	0x0198	W	0x5AA5C33C	REG_0x66
DDRPHY_COM_REG_0x67	0x019C	W	0xFF5500AA	REG_0x67
DDRPHY_COM_REG_0x68	0x01A0	W	0x0000F00F	REG_0x68
DDRPHY_COM_REG_0x69	0x01A4	W	0xA55A3CC3	REG_0x69
DDRPHY_COM_REG_0x6a	0x01A8	W	0x00AAFF55	REG_0x6a
DDRPHY_COM_REG_0x6b	0x01AC	W	0x00010FF0	REG_0x6b
DDRPHY_COM_REG_0x6c	0x01B0	W	0x14285140	REG_0x6c
DDRPHY_COM_REG_0x6e	0x01B8	W	0x0000003F	REG_0x6e
DDRPHY_COM_REG_0x6f	0x01BC	W	0x5AA5C33C	REG_0x6f
DDRPHY_COM_REG_0x70	0x01C0	W	0xFF5500AA	REG_0x70
DDRPHY_COM_REG_0x71	0x01C4	W	0x0000F00F	REG_0x71
DDRPHY_COM_REG_0x7c	0x01F0	W	0x00000000	REG_0x7c
DDRPHY_COM_REG_0x7d	0x01F4	W	0x00000000	REG_0x7d
DDRPHY_COM_REG_0x7e	0x01F8	W	0x00000000	REG_0x7e
DDRPHY_COM_REG_0x7f	0x01FC	W	0x00000000	REG_0x7f
DDRPHY_COM_REG_0x80	0x0200	W	0x00000000	REG_0x80
DDRPHY_COM_REG_0x81	0x0204	W	0x00000000	REG_0x81
DDRPHY_COM_REG_0x82	0x0208	W	0x00000000	REG_0x82
DDRPHY_COM_REG_0x83	0x020C	W	0x00000000	REG_0x83
DDRPHY_COM_REG_0x84	0x0210	W	0x00000000	REG_0x84
DDRPHY_COM_REG_0x85	0x0214	W	0x00000000	REG_0x85
DDRPHY_COM_REG_0x86	0x0218	W	0x00000000	REG_0x86
DDRPHY_COM_REG_0x87	0x021C	W	0x00000000	REG_0x87
DDRPHY_COM_REG_0x8c	0x0230	W	0x00000000	REG_0x8c
DDRPHY_COM_REG_0x8d	0x0234	W	0x00000000	REG_0x8d
DDRPHY_COM_REG_0x8e	0x0238	W	0x00000000	REG_0x8e
DDRPHY_COM_REG_0x8f	0x023C	W	0x00000000	REG_0x8f
DDRPHY_COM_REG_0x90	0x0240	W	0x00000000	REG_0x90
DDRPHY_COM_REG_0x91	0x0244	W	0x00000000	REG_0x91

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Name	Offset	Size	Reset Value	Description
DDRPHY_COM_REG_0x92	0x0248	W	0x00000000	REG_0x92
DDRPHY_COM_REG_0x93	0x024C	W	0x00000000	REG_0x93
DDRPHY_COM_REG_0x94	0x0250	W	0x00000000	REG_0x94
DDRPHY_COM_REG_0x95	0x0254	W	0x00000000	REG_0x95
DDRPHY_COM_REG_0x96	0x0258	W	0x00000000	REG_0x96
DDRPHY_COM_REG_0x97	0x025C	W	0x00000000	REG_0x97
DDRPHY_COM_REG_0x98	0x0260	W	0x00000000	REG_0x98
DDRPHY_COM_REG_0x99	0x0264	W	0x00000000	REG_0x99
DDRPHY_COM_REG_0x9a	0x0268	W	0x00000000	REG_0x9a
DDRPHY_COM_REG_0x9b	0x026C	W	0x00000000	REG_0x9b
DDRPHY_COM_REG_0x9c	0x0270	W	0x00000000	REG_0x9c
DDRPHY_COM_REG_0x9d	0x0274	W	0x00000000	REG_0x9d
DDRPHY_COM_REG_0x9e	0x0278	W	0x00000000	REG_0x9e
DDRPHY_COM_REG_0x9f	0x027C	W	0x00000000	REG_0x9f
DDRPHY_COM_REG_0xa0	0x0280	W	0x00000000	REG_0xa0
DDRPHY_COM_REG_0xa1	0x0284	W	0x00000000	REG_0xa1
DDRPHY_COM_REG_0xa2	0x0288	W	0x00000000	REG_0xa2
DDRPHY_COM_REG_0xa3	0x028C	W	0x00000000	REG_0xa3
DDRPHY_COM_REG_0xa4	0x0290	W	0x00000000	REG_0xa4
DDRPHY_COM_REG_0xa5	0x0294	W	0x00000000	REG_0xa5
DDRPHY_COM_REG_0xa6	0x0298	W	0x00000000	REG_0xa6
DDRPHY_COM_REG_0xa7	0x029C	W	0x00000000	REG_0xa7
DDRPHY_COM_REG_0xa8	0x02A0	W	0x00000000	REG_0xa8
DDRPHY_COM_REG_0xa9	0x02A4	W	0x00000000	REG_0xa9
DDRPHY_COM_REG_0xaa	0x02A8	W	0x00000000	REG_0xaa
DDRPHY_COM_REG_0xab	0x02AC	W	0x00000000	REG_0xab
DDRPHY_COM_REG_0xac	0x02B0	W	0x00000000	REG_0xac
DDRPHY_COM_REG_0xad	0x02B4	W	0x00000000	REG_0xad
DDRPHY_COM_REG_0xae	0x02B8	W	0x00000000	REG_0xae
DDRPHY_COM_REG_0xaf	0x02BC	W	0x00000000	REG_0xaf
DDRPHY_COM_REG_0xb0	0x02C0	W	0x00000001	REG_0xb0
DDRPHY_COM_REG_0xb1	0x02C4	W	0x00000000	REG_0xb1
DDRPHY_COM_REG_0xb2	0x02C8	W	0x40010000	REG_0xb2
DDRPHY_COM_REG_0xb3	0x02CC	W	0x00003FFC	REG_0xb3
DDRPHY_COM_REG_0xb4	0x02D0	W	0x0AAB0000	REG_0xb4
DDRPHY_COM_REG_0xb5	0x02D4	W	0x00000000	REG_0xb5
DDRPHY_COM_REG_0xb6	0x02D8	W	0x00000000	REG_0xb6
DDRPHY_COM_REG_0xb7	0x02DC	W	0x00000000	REG_0xb7
DDRPHY_COM_REG_0xb8	0x02E0	W	0x0040501F	REG_0xb8
DDRPHY_COM_REG_0xb9	0x02E4	W	0x0E0E0E0E	REG_0xb9
DDRPHY_COM_REG_0xba	0x02E8	W	0x00000000	REG_0xba
DDRPHY_COM_REG_0xbb	0x02EC	W	0x00000000	REG_0xbb
DDRPHY_COM_REG_0xbc	0x02F0	W	0x00000000	REG_0xbc
DDRPHY_COM_REG_0xbd	0x02F4	W	0x00000000	REG_0xbd
DDRPHY_COM_REG_0xbe	0x02F8	W	0x00000000	REG_0xbe
DDRPHY_COM_REG_0xbf	0x02FC	W	0x00000000	REG_0xbf
DDRPHY_COM_REG_0xc0	0x0300	W	0x00000000	REG_0xc0
DDRPHY_COM_REG_0xc1	0x0304	W	0x00000000	REG_0xc1
DDRPHY_COM_REG_0xc2	0x0308	W	0x00000000	REG_0xc2
DDRPHY_COM_REG_0xc3	0x030C	W	0x00000000	REG_0xc3
DDRPHY_COM_REG_0xc4	0x0310	W	0x00000000	REG_0xc4
DDRPHY_COM_REG_0xc5	0x0314	W	0x00000000	REG_0xc5

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Name	Offset	Size	Reset Value	Description
DDRPHY_COM_REG_0xc6	0x0318	W	0x00000000	REG_0xc6
DDRPHY_COM_REG_0xc7	0x031C	W	0x00000000	REG_0xc7
DDRPHY_COM_REG_0xc8	0x0320	W	0x00000000	REG_0xc8
DDRPHY_COM_REG_0xc9	0x0324	W	0x00000000	REG_0xc9
DDRPHY_COM_REG_0xca	0x0328	W	0x00000000	REG_0xca
DDRPHY_COM_REG_0xcb	0x032C	W	0x00000000	REG_0xcb
DDRPHY_COM_REG_0xcc	0x0330	W	0x00000000	REG_0xcc
DDRPHY_COM_REG_0xcd	0x0334	W	0x00000000	REG_0xcd
DDRPHY_COM_REG_0xce	0x0338	W	0x00000AAA	REG_0xce

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

DDRPHY_BYTE0/1/2/3 Registers Summary:

Name	Offset	Size	Reset Value	Description
DDRPHY_BYTE_REG_0x0	0x0000	W	0x800800A0	REG_0x0
DDRPHY_BYTE_REG_0x1	0x0004	W	0x0E0E0505	REG_0x1
DDRPHY_BYTE_REG_0x2	0x0008	W	0x00100203	REG_0x2
DDRPHY_BYTE_REG_0x3	0x000C	W	0x00FAC688	REG_0x3
DDRPHY_BYTE_REG_0x4	0x0010	W	0x01E801E8	REG_0x4
DDRPHY_BYTE_REG_0x5	0x0014	W	0x02840284	REG_0x5
DDRPHY_BYTE_REG_0x6	0x0018	W	0x006F8800	REG_0x6
DDRPHY_BYTE_REG_0x7	0x001C	W	0x00009606	REG_0x7
DDRPHY_BYTE_REG_0x8	0x0020	W	0x00000080	REG_0x8
DDRPHY_BYTE_REG_0x9	0x0024	W	0x80808080	REG_0x9
DDRPHY_BYTE_REG_0xa	0x0028	W	0x80808080	REG_0xa
DDRPHY_BYTE_REG_0xb	0x002C	W	0x80008000	REG_0xb
DDRPHY_BYTE_REG_0xc	0x0030	W	0x00000000	REG_0xc
DDRPHY_BYTE_REG_0xd	0x0034	W	0x00000000	REG_0xd
DDRPHY_BYTE_REG_0xe	0x0038	W	0x00000000	REG_0xe
DDRPHY_BYTE_REG_0xf	0x003C	W	0x1F001F00	REG_0xf
DDRPHY_BYTE_REG_0x10	0x0040	W	0x00000080	REG_0x10
DDRPHY_BYTE_REG_0x11	0x0044	W	0x80808080	REG_0x11
DDRPHY_BYTE_REG_0x12	0x0048	W	0x80808080	REG_0x12
DDRPHY_BYTE_REG_0x13	0x004C	W	0x80008000	REG_0x13
DDRPHY_BYTE_REG_0x14	0x0050	W	0x00000000	REG_0x14
DDRPHY_BYTE_REG_0x15	0x0054	W	0x00000000	REG_0x15
DDRPHY_BYTE_REG_0x16	0x0058	W	0x00000000	REG_0x16
DDRPHY_BYTE_REG_0x17	0x005C	W	0x1F001F00	REG_0x17
DDRPHY_BYTE_REG_0x18	0x0060	W	0x1F073F00	REG_0x18
DDRPHY_BYTE_REG_0x19	0x0064	W	0x00000000	REG_0x19
DDRPHY_BYTE_REG_0x1c	0x0070	W	0x00000000	REG_0x1c
DDRPHY_BYTE_REG_0x1d	0x0074	W	0x00000000	REG_0x1d
DDRPHY_BYTE_REG_0x1e	0x0078	W	0x00000000	REG_0x1e
DDRPHY_BYTE_REG_0x1f	0x007C	W	0x00000000	REG_0x1f
DDRPHY_BYTE_REG_0x20	0x0080	W	0x00000000	REG_0x20
DDRPHY_BYTE_REG_0x21	0x0084	W	0x00000000	REG_0x21
DDRPHY_BYTE_REG_0x22	0x0088	W	0x00000000	REG_0x22
DDRPHY_BYTE_REG_0x23	0x008C	W	0x00000000	REG_0x23
DDRPHY_BYTE_REG_0x24	0x0090	W	0x00000000	REG_0x24
DDRPHY_BYTE_REG_0x25	0x0094	W	0x00000000	REG_0x25
DDRPHY_BYTE_REG_0x26	0x0098	W	0x00000000	REG_0x26
DDRPHY_BYTE_REG_0x27	0x009C	W	0x00000000	REG_0x27

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Name	Offset	Size	Reset Value	Description
DDRPHY_BYTE_REG_0x28	0x00A0	W	0x00000000	REG_0x28
DDRPHY_BYTE_REG_0x29	0x00A4	W	0x00000000	REG_0x29
DDRPHY_BYTE_REG_0x2a	0x00A8	W	0x00000000	REG_0x2a
DDRPHY_BYTE_REG_0x2b	0x00AC	W	0x00000000	REG_0x2b
DDRPHY_BYTE_REG_0x2c	0x00B0	W	0x00000000	REG_0x2c
DDRPHY_BYTE_REG_0x2d	0x00B4	W	0x00000000	REG_0x2d
DDRPHY_BYTE_REG_0x2e	0x00B8	W	0x00000000	REG_0x2e
DDRPHY_BYTE_REG_0x2f	0x00BC	W	0x00000000	REG_0x2f
DDRPHY_BYTE_REG_0x30	0x00C0	W	0x00000000	REG_0x30
DDRPHY_BYTE_REG_0x31	0x00C4	W	0x00000000	REG_0x31
DDRPHY_BYTE_REG_0x32	0x00C8	W	0x00000000	REG_0x32
DDRPHY_BYTE_REG_0x40	0x0100	W	0x80808080	REG_0x40
DDRPHY_BYTE_REG_0x41	0x0104	W	0x80808080	REG_0x41
DDRPHY_BYTE_REG_0x42	0x0108	W	0x80008000	REG_0x42
DDRPHY_BYTE_REG_0x43	0x010C	W	0x00008000	REG_0x43
DDRPHY_BYTE_REG_0x44	0x0110	W	0x00000000	REG_0x44
DDRPHY_BYTE_REG_0x45	0x0114	W	0x00000000	REG_0x45
DDRPHY_BYTE_REG_0x46	0x0118	W	0x1F001F00	REG_0x46
DDRPHY_BYTE_REG_0x47	0x011C	W	0x00000080	REG_0x47
DDRPHY_BYTE_REG_0x48	0x0120	W	0x80808080	REG_0x48
DDRPHY_BYTE_REG_0x49	0x0124	W	0x80808080	REG_0x49
DDRPHY_BYTE_REG_0x4a	0x0128	W	0x80008000	REG_0x4a
DDRPHY_BYTE_REG_0x4b	0x012C	W	0x00000000	REG_0x4b
DDRPHY_BYTE_REG_0x4c	0x0130	W	0x00000000	REG_0x4c
DDRPHY_BYTE_REG_0x4d	0x0134	W	0x00000000	REG_0x4d
DDRPHY_BYTE_REG_0x4e	0x0138	W	0x1F001F00	REG_0x4e
DDRPHY_BYTE_REG_0x4f	0x013C	W	0x01E801E8	REG_0x4f
DDRPHY_BYTE_REG_0x50	0x0140	W	0x02840284	REG_0x50
DDRPHY_BYTE_REG_0x51	0x0144	W	0x00002400	REG_0x51
DDRPHY_BYTE_REG_0x52	0x0148	W	0x00000000	REG_0x52
DDRPHY_BYTE_REG_0x53	0x014C	W	0x00000000	REG_0x53
DDRPHY_BYTE_REG_0x54	0x0150	W	0x00000000	REG_0x54
DDRPHY_BYTE_REG_0x55	0x0154	W	0x00000000	REG_0x55
DDRPHY_BYTE_REG_0x56	0x0158	W	0x0E0E0505	REG_0x56

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

13.4.5 Detail Registers Description

DDRPHY_COM Registers Description:

DDRPHY_COM_REG_0x0

Address: Operational Base(0xFF4F0000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RW	0x0	reg_signal_grounded_en The enable signal for CA signal grounding. High is valid. The default value will close this function. 1'b1: Open this function, CA signals are grounded. 0'b0:Don't use this function.
20	RW	0x0	reg_rank4_en enable the 4 rank of lpddr3 and lpddr4
19:12	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
11:8	RW	0xf	reg_channel_en The byte enable signal of the PHY. High is valid. The defautl mode will open the four bytes at the same time. [0]: The byte0 enable signal, corresponding to A_DQ0~A_DQ7. [1]: The byte1 enable signal, corresponding to A_DQ8~A_DQ15. [2]: The byte2 enable signal, corresponding to B_DQ0~B_DQ7. [3]: The byte3 enable signal, corresponding to B_DQ8~B_DQ15. [4]: The byte4 enable signal, corresponding to C_DQ0~C_DQ7 If the user only wants to use two bytes, we suggest to choose the byte0 and byte1.
7	RW	0x1	reg_burst_sel According to the SDRAM type to choose the burst type that the PHY needs to support. 1: Support the BL8/BL16 0: Reserved.
6:4	RW	0x0	mem_select_t Choose the SDRAM that the PHY need to support. 3'h0:DDR2 PHY mode. 3'h1:LPDDR2 PHY mode. 3'h2:DDR3 PHY mode. 3'h3:LPDDR3 PHY mode. 3'h4:DDR4 PHY mode. 3'h5: LPDDR4 PHY mode. Others: Reserved.
3	RO	0x0	reserved
2	RW	0x1	soft_reset1 The reset signal of digital core, Active low.
1	RW	0x1	soft_reset0 The reset signal of analog logic, Active low.
0	RW	0x1	soft_reset The reset signal of digital core and analog logic. Active low.

DDRPHY_COM_REG_0x1

Address: Operational Base(0xFF4F0000) + offset (0x0004)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	reg_wl_loadmode [23:16]Write leveling load mode [7:0]. The PHY needs to configure the load mode to enable the write leveling function. In case of that write leveling operation changs the load mode value in the SDRAM which is written by the MC, so we need to use this register to keep the same setting with the MC for the mode register which is related to the write leveling. This is the low 8bits of the mode register which is related to the write leveling. For DDR3/DDR4, this register should keep the same value with the MR1[7:0]. For LPDDR3/LPDDR4, this register should keep the same value with the MR2[7:0]. Please reference to the section 4.5.2 to get more information. [31:24] Write leveling load mode [15:8]. Relate to the register 10'h002 [2]. The PHY needs to configure the load mode to enable the write leveling function. In case of that write leveling operation changs the load mode value in the SDRAM which is written by the MC, so we need to use this register to keep the same setting with the MC for the mode register which is related to the write leveling. This is the low 8bits of the mode register which is related to the write leveling. For DDR3/DDR4, this register [13:8] should keep the same value with the MR1[13:8] and this register [15:14] should set 2'b01. For LPDDR3/LPDDR4, this register should set to 8'h0. Please reference to the section 4.5.2 to get more information.
15:12	RO	0x0	reserved
11:8	RW	0xe	reg_wlcs_sel The rank select signal of the write-leveling fuction. Low is valid. 4'b0000: The write-leveling result will auto switch between the RANK0,RANK1,RANK2,RANK3 according to the DFI interface command after the write-leveling training. 4'b0111: Choose the RANK3. The chip which connects to CS3 will be chooses to enable the write-leveling training. 4'b1011: Choose the RANK2. The chip which connects to CS2 will be chooses to enable the write-leveling training. 4'b1101: Choose the RANK1. The chip which connects to CS1 will be chooses to enable the write-leveling training. 4'b1110: Choose the RANK0. The chip which connects to CS0 will be chooses to enable the write-leveling training. 4'b1111: Reserved. Note: Can't set to 4'b0000 when enable the write-levleing training funciton. If the PHY needs to support two ranks, this register should set to 2'b00 after the write-leveling training.
7	RW	0x0	reg_wl_bypass The tx perbit-skew bypass function enable signal. High is valid. 0: Use the write-leveling training result to control the tx perbit-skew delay. The A_DQ0~A_DQ7/A_DM0 will use the A_DQS0 training result. The A_DQ8~A_DQ15/A_DM1 will use the A_DQS1 training result. The B_DQ0~A_DQ7/A_DM0 will use the B_DQS0 training result. The B_DQ8~A_DQ15/A_DM0 will use the B_DQS1 training result. 1: Use the register to control the tx perbit-skew delay. Each data pad has an independet controller register.

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Bit	Attr	Reset Value	Description
6	RW	0x0	reg_wl_enable The write-leveling training enable signal. High is valid. 0: Keep current state or exit the write-leveling training state. 1: Eanble the write-leveling training function.
5:2	RW	0xe	reg_calcs_sel The rank select signal of the rx-dqs calibration fuction. Low is valid. 4'b0000: The rx-dqs calibration result will auto switch between the RANK0, RANK1,RANK2,RANK3 according to the DFI interface command after the rx-dqs calibration training. 4'b0111: Choose the RANK3. The chip which connects to CS3 will be chooses to enable the auto rx-dqs calibration training. 4'b1011: Choose the RANK2. The chip which connects to CS2 will be chooses to enable the auto rx-dqs calibration training. 4'b1101: Choose the RANK1. The chip which connects to CS1 will be chooses to enable the auto rx-dqs calibration training. 4'b1110: Choose the RANK0. The chip which connects to CS0 will be chooses to enable the auto rx-dqs calibration training. 4'b11: Reserved. Note: Can't set to 2'b00 when enable the rx-dqs calibration training funciton. If the PHY needs to support two ranks, this register should set to 2'b00 after the rx-dqs calibration training.
1	RW	0x0	reg_calib_bypass Reserved.
0	RW	0x0	reg_start_calib The auto rx-dqs calibration training enable signal. High is valid. 0: Keep current state or exit the auto rx-dqs calibration training. 1: Enable the auto rx-dqs calibration training function.

DDRPHY_COM_REG_0x2

Address: Operational Base(0xFF4F0000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	AL_FRE_OP0 Setting the AL vlaue of the PHY for frequency point 0. When enable the Fast Frequency Change Mode, the PHY will choose AL_FEE_OP0 as the AL setting of the PHY when the freq== 2'b00.. For LPDDRn, this register should keep default value. For DDRn, this register should keep the same AL setting with the SDRAM.
23:22	RO	0x0	reserved
21:16	RW	0x00	AL_FRE_OP1 Setting the AL vlaue of the PHY for frequency point 1. When enable the Fast Frequency Change Mode, the PHY will choose AL_FEE_OP1 as the AL setting of the PHY when the freq == 2'b01.. For LPDDRn, this register should keep default value. For DDRn, this register should keep the same AL setting with the SDRAM.
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x00	AL_FRE_OP2 Setting the AL vlaue of the PHY for frequency point 2. When enable the Fast Frequency Change Mode, the PHY will choose AL_FEE_OP2 as the AL setting of the PHY when the freq == 2'b10.. For LPDDRn, this register should keep default value. For DDRn, this register should keep the same AL setting with the SDRAM.
7:6	RO	0x0	reserved
5:0	RW	0x00	AL_FRE_OP3 Setting the AL vlaue of the PHY for frequency point 3. When enable the Fast Frequency Change Mode, the PHY will choose AL_FEE_OP3 as the AL setting of the PHY when the freq == 2'b11.. For LPDDRn, this register should keep default value. For DDRn, this register should keep the same AL setting with the SDRAM.

DDRPHY_COM_REG_0x3

Address: Operational Base(0xFF4F0000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x06	CL_FRE_OP0 Setting the CL/RL vlaue of the PHY for frequency point 0. When enable the Fast Frequency Change Mode, the PHY will choose CL_FEE_OP0 as the CL/RL setting of the PHY when the freq == 2'b00. For LPDDRn, this register should keep the same RL setting with the SDRAM. For DDRn, this register should keep the same CL setting with the SDRAM.
23:22	RO	0x0	reserved
21:16	RW	0x06	CL_FRE_OP1 Setting the CL/RL vlaue of the PHY for frequency point 1. When enable the Fast Frequency Change Mode, the PHY will choose CL_FEE_OP0 as the CL/RL setting of the PHY when the freq == 2'b01. For LPDDRn, this register should keep the same RL setting with the SDRAM. For DDRn, this register should keep the same CL setting with the SDRAM.
15:14	RO	0x0	reserved
13:8	RW	0x06	CL_FRE_OP2 Setting the CL/RL vlaue of the PHY for frequency point 2. When enable the Fast Frequency Change Mode, the PHY will choose CL_FEE_OP0 as the CL/RL setting of the PHY when the freq == 2'b10. For LPDDRn, this register should keep the same RL setting with the SDRAM. For DDRn, this register should keep the same CL setting with the SDRAM.
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x06	CL_FRE_OP3 Setting the CL/RL vlaue of the PHY for frequency point 3. When enable the Fast Frequency Change Mode, the PHY will choose CL_FEE_OP0 as the CL/RL setting of the PHY when the freq == 2'b11. For LPDDRn, this register should keep the same RL setting with the SDRAM. For DDRn, this register should keep the same CL setting with the SDRAM.

DDRPHY_COM_REG_0x4

Address: Operational Base(0xFF4F0000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	CWL_FRE_OP0 Setting the CWL/WL vlaue of the PHY for frequency point 0. When enable the Fast Frequency Change Mode, the PHY will choose CWL_FEE_OP0 as the CWL/WL setting of the PHY when the freq == 2'b00. For LPDDRn, this register should keep the same WL setting with the SDRAM. For DDRn, this register should keep the same CWL setting with the SDRAM.
23:22	RO	0x0	reserved
21:16	RW	0x00	CWL_FRE_OP1 Setting the CWL/WL vlaue of the PHY for frequency point 1. When enable the Fast Frequency Change Mode, the PHY will choose CWL_FEE_OP0 as the CWL/WL setting of the PHY when the freq == 2'b00. For LPDDRn, this register should keep the same WL setting with the SDRAM. For DDRn, this register should keep the same CWL setting with the SDRAM.
15:14	RO	0x0	reserved
13:8	RW	0x00	CWL_FRE_OP2 Setting the CWL/WL vlaue of the PHY for frequency point 2. When enable the Fast Frequency Change Mode, the PHY will choose CWL_FEE_OP0 as the CWL/WL setting of the PHY when the freq == 2'b00. For LPDDRn, this register should keep the same WL setting with the SDRAM. For DDRn, this register should keep the same CWL setting with the SDRAM.
7:6	RO	0x0	reserved
5:0	RW	0x00	CWL_FRE_OP3 Setting the CWL/WL vlaue of the PHY for frequency point 3. When enable the Fast Frequency Change Mode, the PHY will choose CWL_FEE_OP0 as the CWL/WL setting of the PHY when the freq == 2'b00. For LPDDRn, this register should keep the same WL setting with the SDRAM. For DDRn, this register should keep the same CWL setting with the SDRAM.

DDRPHY_COM_REG_0x5

Address: Operational Base(0xFF4F0000) + offset (0x0014)

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Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	reg_fb1xclk_invdelaysel_dqcmd Used to adjust the hold timing of the digital to analog interface. When increase this register, it will increase the hold time of the digital to analog interface.
23:21	RO	0x0	reserved
20:16	RW	0x00	reg_h4xclk_invdelaysel_dqcmd Reserved.
15:13	RO	0x0	reserved
12:8	RW	0x00	reg_h4xclkdqs_invdelaysel_dqcmd Reserved.
7:5	RO	0x0	reserved
4:0	RW	0x00	reg_h1xclk_invdelaysel_dqcmd Reserved.

DDRPHY_COM_REG_0x6

Address: Operational Base(0xFF4F0000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0xffffffff	reg_cmd_ph90en_bp The command 90 degree control signal. High means eanble the command 90 degree conrol and low means the disalbe the command 90 degree control. [0]:A0 [1]:A1 [2]:A2 [3]:A3 [4]:A4 [5]:A5 [6]:A6 [7]:A7 [8]:A8 [9]:A9 [10]:A10 [11]:A11 [12]:A12 [13]:A13 [14]:A14 [15]:A15 [16]:A16 [17]:A17 [18]:ACTN [19]:BA0 [20]:BA1 [21]:BG0 [22]:BG1 [23]:CK [24]:CKB [25]:CKE0 [26]:CSB0 [27]:CSB1 [28]:ODT0 [29]:ODT1 [30]:CKE1 [31]:RESETN [7]:RESETN

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DDRPHY_COM_REG_0x7

Address: Operational Base(0xFF4F0000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	reg_dfi_clk_gate_bp Reserved.
27	RW	0x0	reg_rx_lock_code_bp_en The rx dll lock value bypass. Active High. 1: use the dll lock value from the register reg_rx_lock_code_bp_value[7:0]. 0: use the dll lock value from dll module automatically.
26	RW	0x0	reg_tx_lock_code_bp_en The tx dll lock value bypass. Active High. 1: use the dll lock value from the register reg_tx_lock_code_bp_value[7:0]. 0: use the dll lock value from dll module automatically.
25	RW	0x0	reg_oscen_t Reserved.
24	RW	0x0	reg_x1clk_div_sel Reserved.
23	RW	0x1	reg_vt_comp_bp The rx vt compensation disable signal. Active High. 1: Disable the rx vt compensation function. 0: Enable the rx vt compensation funciton.
22	RW	0x1	reg_cmdout_mux The timing control of the command path between the digital part and analog part. 1: The command signal from the digital part to the analog part is align to the posedge of the dfi_clk1x. 0: The command signal from the ditial part to the analog part is align to the negedge of the dfi_clk1x.
21	RW	0x0	ph90en_bp The 90 degree control bypass enable signal of the command path. In the normal mode, the 90 degree control of the command path is setting automatically based on the sdram type. The user also can use this register to choose the bypass mode, then use the register reg_cmd_ph90en_bp to control the 90 degree of each command pad. 1: Choose the bypass mode. 0: Choose the auto mode.
20	RW	0x0	ph90en_bp_dq The 90 degree control bypass enable signal of the data path. In the normal mode, the 90 degree control of the data path is setting automatically based on the sdram type. The user also can use this register to choose the bypass mode, then use the register reg_a/b/c_l/h_dq_ph90en_bp ,reg_a/b/c_l/h_dqs_ph90en_bp to control the 90 degree of each dq pad. 1: Choose the bypass mode. 0: Choose the auto mode.
19	RW	0x0	reg_rden_bypass Then enable signal of the rx fifo read control bypass mode. High is valid. 0: Disable the bypass mode. 1: Enable the bypass mode and use the reg_rden_delay to control the rx fifo read timing.

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Bit	Attr	Reset Value	Description
18:16	RW	0x2	reg_rden_delay This register is used to control read timing of the rx fifo when enable the rx fifo read control bypass mode. When the dfi_rddata_en change to high, the phy will read out the rx data from the rx fifo afther the following delay. 0: 9+max(reg_ar_cycsel,reg_al_cycsel,reg_br_cycsel,reg_bl_cycsel) 1: 10+max(reg_ar_cycsel,reg_al_cycsel,reg_br_cycsel,reg_bl_cycsel) 2: 11+max(reg_ar_cycsel,reg_al_cycsel,reg_br_cycsel,reg_bl_cycsel) 3: 12+max(reg_ar_cycsel,reg_al_cycsel,reg_br_cycsel,reg_bl_cycsel) 4: 13+max(reg_ar_cycsel,reg_al_cycsel,reg_br_cycsel,reg_bl_cycsel) 5: 14+max(reg_ar_cycsel,reg_al_cycsel,reg_br_cycsel,reg_bl_cycsel) 6: 15+max(reg_ar_cycsel,reg_al_cycsel,reg_br_cycsel,reg_bl_cycsel) 7: 16+max(reg_ar_cycsel,reg_al_cycsel,reg_br_cycsel,reg_bl_cycsel) For auto mode, the delay = 11+max(reg_ar_cycsel,reg_al_cycsel,reg_br_cycsel,reg_bl_cycsel).
15	RO	0x0	reserved
14	RW	0x0	reg_rdodt_bypass The bypass enable signal of the rx odt bypass function. When enable this function, the user can use the register reg_a/b/c_l/h_rdodt0/1/2/3_delay[2:0](eg reg_a_l_rdodt0_delay[2:0]),reg_a/b/c_l/h_rdodt0/1/2/3_ophsel[2:0],reg_a/b/c_l/h_rdodt0/1/2/3_dllsel[4:0] to adjust the timing of the rx odt .
13	RW	0x0	reg_rxodt_st_bypass The enable signal of the rx odt start point bypass mode, when enable this function , using the register reg_rxodt_stdelay to control the start point of the rx odt. High is valid.
12	RO	0x0	reserved
11:8	RW	0x0	reg_rxodt_stdelay Using to control the rx odt start point when enable the rx odt start point bypass mode(reg_rxodt_st_bypass). Decrease this value will left shift the rx odt window, increase this value will right shift the rx odt window. Unit:dfi_clk1x. For auto mode, the start_point = (RL-1)>>1.

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Bit	Attr	Reset Value	Description
7:4	RW	0x2	reg_rxodt_length Used to control the length of the RX ODT. The step is 1x clock cycle. When the value +1, the length of RX ODT will increase 1x clock cycle. Related register 0x00f. It combines with the register reg_rxodt_start_point to decide the range of the RX ODT. The default RX ODT length is 4*dfi_clk1x cycles.
3:0	RW	0x3	reg_rxodt_start_point Used to control the start point of the RX ODT. When the value +1, the start point of RX ODT will increase 1x clock cycle. If the user wants to keep the length of the RX ODT unchanged, the users need to increase 1x clock cycle of the length of the RX ODT using the register reg_rxodt_length. The default RX ODT start point is RL-2 in regard to the read command.

DDRPHY_COM_REG_0x8

Address: Operational Base(0xFF4F0000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	reg_cmd_rank_switch_dis The cmd rank switch disable signal. 1: Disable the cmd rank switch, the all rank command will keep the tx perbit de-skew delay with rank0. 0:The each rank will use its commans bus training result to control the tx perbit de-skew delay.
27:24	RW	0x0	reg_cat_fspy_rank If the user chooses to set the FSP[Y] in the command bus train flow by set tingthe reg_cat_ske_fspy = 1'b0, the use can use this register to choose the RANK which need to be set. 4'b0000: Choose RANK0 and RANK1. 4'b1110: Choose Rank0. 4'b1101: Choose Rank1. 4'b1011: Choose Rank2. 4'b0111: Choose Rank3.
23:20	RW	0x0	reg_cat_bp_rank_sel Used to choose the rank when enable the bypass command bus train or only enable one rank of auto command bus train. 2'b10: Choose the Rank0 to do the command bus train. 2'b01: Choose the Rank1 to do the command bus train.
19	RO	0x0	reserved
18:15	RW	0x1	reg_cat_rank_num Define the rank number of the command bus train should support. 4'b0000: Four ranks. 4'b1110: rank 0. 4'b1101: rank 1. 4'b1011: rank 2. 4'b0111: rank 3. Others: Not support.

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Bit	Attr	Reset Value	Description
14:13	RW	0x3	reg_cat_channel_num The command channel enable signal of command bus train. High is valid. 2'b11: Enable Channel A and Channel B. 2'b01: Only enable Channel A. 2'b10: Only enable Channel B.
12:8	RW	0x04	reg_clk_div_cnt This register is used to control the divider of the dfi_clk1x which used for the initialization of the SDRAM and command bus training. The dfi_clk1x will be clock divided to the low speed based on this register. Tclkinit = Tdfi_clk1x/(2*reg_clk_div_cnt).
7:6	RO	0x0	reserved
5	RW	0x0	reg_cat_bp_cmd_send Used to send the command bus train command when enable the command bus training bpass mode. Posedge is valid. When this signal change from low to high, it will send the command bus train command to the SDRAM. The command bus value depends on the reg_cat_bp_mode, reg_cat_cs_train_value and reg_ca_train_value.
4	RW	0x0	reg_cat_bp_mode Choose the command bus train stage for the byass mode. 0: Current is CS bypass command bus train. 1: Current is CA bypass command bus train.
3	RW	0x0	reg_cat_bp_en The Bypass command bus train enable signal. High is valid. When this bit set to high, the command path will choose the command bus train module and the tx delay line of command will be controlled by the register directly through the logic in the command bus training logic.
2	RW	0x0	reg_cat_bp_start The Bypass command bus train start signal. High is valid. When this bit set to high, the command bus module will go into the bypass command bus train flow.
1	RW	0x0	reg_cat_start The Auto command bus train start signal. High is valid. When this signal enable, it will begin the command bus train.
0	RW	0x0	reg_cat_enable The Auto command bus train enable signal. High is valid. When this signal enable, the command path will switch to the command bus train module.

DDRPHY_COM_REG_0x9

Address: Operational Base(0xFF4F0000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x04	reg_txcbt Used to control the timing parameter tcs_VREF/tCKCKEH/tMRZ. The delay should >= MAX(1.5ns,2nCK).
24:20	RW	0x0f	reg_tadr Used to control the check time of the read back data from the DQ. The delay should >= 20ns.

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Bit	Attr	Reset Value	Description
19:15	RW	0x04	reg_tckelck Used to control the clock and command valid after CKE low(tCKELCK). The delay should >= max(7.5ns,3nCK)
14:10	RW	0x01	reg_tdstrain Data Setup/Hold for Vref(CA) Training Mode.
9:5	RW	0x0f	reg_tmrw Used to control the delay between the MRW command and valid clock/CS requirement after CKE input LOW after MRW command. The delay >= MAX(14ns, 10nCK).
4:0	RW	0x1c	reg_tcacd Used to control the CA Bus Training Command to CA Bus Training Command Delay(tCACD). The delay should >= RU(20ns/tCK).

DDRPHY_COM_REG_0xa

Address: Operational Base(0xFF4F0000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x1b	reg_wl_dqs_lock_point
23:16	RW	0x28	reg_tvrefca_long Used to control the Vref(CA) step time.
15:8	RW	0x0f	reg_tcaent Used to control the first CA Bus Training Command following CKE Low(tCAENT). The delay should >= 250ns.
7:0	RW	0x1f	reg_tfc Used to control the frequency set point switching time(tFC). The delay should >= 250ns.

DDRPHY_COM_REG_0xb

Address: Operational Base(0xFF4F0000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	reg_mr1 Used to control the LPDDR4 load mode value of MR1 when command bus train.
23:16	RW	0x00	reg_mr2 Used to control the LPDDR4 load mode value of MR2 when command bus train.
15:8	RW	0x00	reg_mr3 Used to control the LPDDR4 load mode value of MR3 when command bus train.
7:0	RW	0x00	reg_mr11 Used to control the LPDDR4 load mode value of MR11 when command bus train.

DDRPHY_COM_REG_0xc

Address: Operational Base(0xFF4F0000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	reg_mr13 Used to control the LPDDR4 load mode value of MR13 when command bus train.
15:8	RW	0x00	reg_mr14 Used to control the LPDDR4 load mode value of MR14 when command bus train.

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	reg_mr22_rank0 Used to control the LPDDR4 load mode value of MR22 when command bus train.

DDRPHY_COM_REG_0xd

Address: Operational Base(0xFF4F0000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31	RW	0x0	reg_ca_vref_update Reserved.
30	RW	0x0	reg_cat_vref_scan_disable Disable the CA_VREF train when do the Auto command but train. High is valid. 1: Only scan the timing window of the CA and CS based on the current CA_VREF setting. 0: Will scan the CA_VREF to find the best point.
29:24	RW	0x3f	reg_cat_vref_scan_max Set the max value that the Vref train. When the Vref scan arrive to the reg_cat_vref_scan_max, it will stop the Vref scan.
23:22	RO	0x0	reserved
21:16	RW	0x00	reg_cat_vref_scan_min Set the min value that the perbit skew train. The tx delay line scan will start from this delay point.
15	RO	0x0	reserved
14:8	RW	0x1f	reg_cha_cat_vref_bp_value Reserved.
7	RO	0x0	reserved
6:0	RW	0x1f	reg_chb_cat_vref_bp_value Reserved.

DDRPHY_COM_REG_0xe

Address: Operational Base(0xFF4F0000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:28	RW	0x8	reg_cs_perbit_skew_offest_fsp0 The FSP[0] compensation value of CSB tx delay after the command bus train. When the PHY do the command bus train to scan the CSB delay window, the CSB has 75%*2UI. So after the command bus train, we need to make the compensation for the 25%*2UI. The compensation value is the half of the lost pulse width = 1/4UI.
27:24	RW	0x8	reg_cs_perbit_skew_offest_fsp1 The FSP[1] compensation value of CSB tx delay after the command bus train. When the PHY do the command bus train to scan the CSB delay window, the CSB has 75%*2UI. So after the command bus train, we need to make the compensation for the 25%*2UI. The compensation value is the half of the lost pulse width = 1/4UI.
23:20	RW	0x8	reg_cs_perbit_skew_offest_fsp2 The FSP[2] compensation value of CSB tx delay after the command bus train. When the PHY do the command bus train to scan the CSB delay window, the CSB has 75%*2UI. So after the command bus train, we need to make the compensation for the 25%*2UI. The compensation value is the half of the lost pulse width = 1/4UI.

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Bit	Attr	Reset Value	Description
19:16	RW	0x8	reg_cs_perbit_skew_offest_fsp3 The FSP[3] compensation value of CSB tx delay after the command bus train. When the PHY do the command bus train to scan the CSB delay window, the CSB has 75%*2UI. So after the command bus train, we need to make the compensation for the 25%*2UI. The compensation value is the half of the lost pulse width = 1/4UI.
15:12	RW	0x1	reg_lpddr4_ca_odt When enable the register control mode of CA ODT, the PHY will use this register to control the CA_ODT.
11	RW	0x0	reg_lpddr4_ca_odt_sel Choose the CA ODT control mode in LPDDR4 mode. 1: Use the register reg_lpddr4_ca_odt[1:0] to control. 0: Use the dfi_odt to control.
10:8	RW	0x1	reg_cat_vref_scan_steps Used to control the CA_VREF scan steps. When the reg_cat_vref_scan_disable is set to 1'b0 to open the CA_VREF scan mode, the use can use this register to control the scan steps to decrease the scan time.
7	RW	0x0	reg_cs_pwc_disable The disable signal of pulse width control of CS. High is valid. For command bus train, when the PHY do the command bus train of CS, if enable the pulse width control function, the pulse width will decrease 25% for command bus train. Before enter command bus train and after exit command bus train, the pulse width of CS will keep the normal pulse width.
6	RW	0x1	reg_cat_skip_fspy For the command bus train, the user can choose to set the FSP[Y](assume that the current is FSP[X]) at the low speed based on the setting in the register (reg_mr1~regmr22). This register is used to control to enable this function or not. 1: Enable the function to set the FSP[Y] before the command bus train. 0: Disable the function to set the FSP[Y]] before the command bus train. When the user chooses this mode, the user need to set the FSP[Y] before to enable the command bus trian. Note: For the first time of high speed command bus training, the phy will complete the sdram initialization and skip this operation automatically.
5:4	RO	0x0	reserved
3	RW	0x1	reg_cat_fc_pd_en Reserved.
2	RW	0x0	reg_cat_skip_cs_train The disable signal to skip the cs train flow of the auto command bus train. 1: Skip the CS train and go to the ca training directly. 0: Begin the CS train firstly and go to the ca training.
1	RW	0x0	reg_cmd_perbit_skew_bp The tx delay line of the command pad bypass enable signal. 1: For LPDDR4 mode, it can use the register to control the tx delay line of the command pad. 0: For LPDDR4 mode, it will use the command bus training module to control the tx delay line of the command pad. Note: For other sdram types, the tx delay line is always control by the register directly. This register is unsed.

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Bit	Attr	Reset Value	Description
0	RW	0x0	reg_ca_perbit_skew_update Used to update the perbit skew of the command in the command bus train module through the registers. Posedge is valid. When this signal change from low to high, it will update the perbit skew value setting by the register to the command bus train module according to the current reg_freq_choose(reg0x0c[3:2]).

DDRPHY_COM_REG_0xf

Address: Operational Base(0xFF4F0000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	reg_cat_choose_result when set 1, means cha's ca train result choose average of rank0 and rank1, chb's ca train result choose average of rank2 and rank3
27	RW	0x1	reg_cat_ca_then_cs
26	RW	0x0	reg_cat_clear
25	RW	0x0	reg_cat_cke_mode Reserved.
24	RW	0x1	reg_cat_ck_cke_odt_fix_perbit_skew Reserved.
23:16	RW	0xff	reg_cat_ca_scan_max Set the max value that the perbit skew train. When the perbit skew scan arrive to the reg_cat_ca_scan_max, it will stop the tx delay line scan of the command.
15:14	RO	0x0	reserved
13:8	RW	0x15	reg_cat_ca_train_value The signal is used to control the CA command bus train pattern. The user can use this register to control the training patter for CA command bus train.
7:6	RO	0x0	reserved
5:0	RW	0x06	reg_cat_cs_train_value The signal is used to control the CS command bus train pattern. The user can use this register to control the command bus train patter for cs train stage.

DDRPHY_COM_REG_0x10

Address: Operational Base(0xFF4F0000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x06	reg_cha_cat_cs_check_value The check pattern of cs train mode for channel A.
23:22	RO	0x0	reserved
21:16	RW	0x06	reg_chb_cat_cs_check_value The check pattern of cs train mode for channel B.
15:14	RO	0x0	reserved
13:8	RW	0x15	reg_cha_cat_ca_check_value The check pattern of ca train mode for channel A.
7:6	RO	0x0	reserved
5:0	RW	0x15	reg_chb_cat_ca_check_value The check pattern of ca train mode for channel A.

DDRPHY_COM_REG_0x11

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Address: Operational Base(0xFF4F0000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	reg_freq_choose_op_t Used for Fast Frequency Changing. Valid only when reg_freq_choose_bypass is high. 00: Freq Point 0. 01: Freq Point 1. 10: Freq Point 2. 11: Freq Point 3. In the normal mode, the current frequency point is set by the dfi_frequency[4:0] at the initialization and frequency change. If the user want to change the current working frequency or update the registers which used to control other frequency points. The user can use this register to set the frequency point firstly. After choose the freq point using this register, the user can switch the training result belong to this freq point fastly.
29	RW	0x0	reg_lpddr4_rd_preamble Choose the read preamble mode when PHY is in LPDDR4 mode. 0: Static. 1: Toggle. Note: This setting should keep the same setting with the MR#1[3] of the LPDDR4.
28	RW	0x0	reg_wl_freq_update The data tx delay line control value update signal. Active high. In the default mode, the tx delay line is controlled by the write-levevling/write training result according to the frequency point. If the user wants to change the value to adjust the delay line, the user can use the bypass registers (invdelay_t) to set the value and set this signal 1. Then the bypass register value will be updated to the control register of the tx perbit skew base on the current frequency point. Note: Please recover to 0 after the setting.
27	RW	0x0	reg_calib_freq_update The RX DQS Gating control value update signal. Active high. In the default mode, after the RX DQS Gating, the training value will control the RX DQS Gating delay. If the user wants to change the value to adjust the RX DQS Gating window, the user can use the bypass registers. If this bit set to 1, then the setting value will be update to the control register of the RX DQS Gating base on the current frequency point. Note: Please recover to 0 after the setting.
26	RW	0x0	reg_cmd_abutobsmodeen Reserved.
25	RW	0x0	reg_sdram_vref_update Reserved.
24	RW	0x0	reg_calib_mode_sel The DQS-Gating model sel. 1: Use the Read Preamble Training mode (Only used for DDR4). 0: Use the Normal Read mode (Can used for DDR2/3/4 and LPDDR2/3). When the DQS Gating mode chooses the Normal Read mode for DDR4, the Read DQS will be pulling down to 1'b0. So the register reg_a/b/c_l/h_weakpub_reg[1:0] should set to 2'b00 to pull down the Read DQS when it is in high z state.
23	RW	0x0	reg_pwrok_pi not used

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Bit	Attr	Reset Value	Description
22:20	RW	0x3	reg_lpddr4_cmd_gap_for_diff_rank Reserved.
19:16	RW	0x0	reg_b0_cmdobsmuxsel Reserved.
15	RW	0x0	reg_b0_obsdataen Reserved.
14	RW	0x0	bist_calibst Reserved.
13	RW	0x0	reg_fiford_delay Reserved.
12	RW	0x0	bist_ck_select The register used to choose the clk which used to sample the bist command when enable the phy noraml bist. 1: Choose the feedback signal from the CK pad as the clock. 0: Choose the feedback signal from the CKB pad as the clock.
11	RW	0x0	reg_mch_odt Reserved.
10	RW	0x0	mux_sync_sel Reserved.
9	RW	0x0	reg_sync_en Reserved.
8	RW	0x1	reg_rdptr_delay Reserved.
7	RW	0x0	reg_scr_rcvmodsel Reserved.
6	RW	0x0	reg_scr_sckdimm0dis Reserved.
5	RW	0x1	reg_scr_sdhsclkb_pos1neg0sel Reserved.
4	RW	0x0	reg_scr_sdhsclk_pos1neg0sel Reserved.
3	RW	0x0	reg_scr_odttrien Reserved.
2	RW	0x0	reg_scr_csbtrien Reserved.
1	RW	0x0	reg_scr_cmdtrien Reserved.
0	RW	0x0	reg_scr_cketrirnk0 Reserved.

DDRPHY_COM_REG_0x12

Address: Operational Base(0xFF4F0000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	reg_freq_choose_wr_t
29:16	RO	0x0000	reserved
15	RW	0x0	cmd_bypassen Reserved.
14	RW	0x1	reg_cmd_iobufact_bp Reserved.
13	RW	0x0	reg_cmd_bist_err_inject Reserved.

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Bit	Attr	Reset Value	Description
12	RW	0x0	reg_ram_vref1_pd The power down signal of RAM VREF. 1: Power Down. 0: Open. Not used in this design
11:8	RW	0x0	bypassen Reserved.
7:0	RW	0x3f	reg_mpr_cnt Used to control the timing of the MPR command for DDR4 rx dqs calibration. Timing interval between MPR = reg_mpr_cnt * dficlk1x.

DDRPHY_COM_REG_0x13

Address: Operational Base(0xFF4F0000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x40	reg_max_rdvalue Use to set the max number of the read command when do the DQS Gating. When the read commands are more than the max number, it is the DQS Gating Error and this state can be read from the register 0x91[5].
15:0	RW	0x1000	reg_calib_timeout The bit[15:0] of the timer used for DQS Gating. When the clock cycle exceed the bits[15:0] of the timer, it is the DQS Gating Error and this state can be read from the register calib_error .

DDRPHY_COM_REG_0x14

Address: Operational Base(0xFF4F0000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	reg_rx_calib_use_rdc_cmd
11	RW	0x1	reg_cat_rxodt_en
10	RW	0x1	reg_rrankdly_4x_dec The delay control signal of the read rank switch. Unit: dfi_clk4x. 1: Decrease 1 dfi_clk4x delay for the read rank switch. 0: Keep current state.
9:8	RW	0x0	reg_rdrank_4xdly not used
7	RW	0x0	reg_rdrank_delay_bp The bypass mode of read rank switch point at 4x clock cycle precision. The user can use the register 0xa6 and 0xd6 to adjust the read rank switch point.
6:4	RW	0x1	reg_rdrank_1xdly not used
3	RO	0x0	reserved
2:0	RW	0x0	reg_wrrank_1xdly The delay control signal of the write rank witch. Unit:dfi_clk1x.

DDRPHY_COM_REG_0x15

Address: Operational Base(0xFF4F0000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28:24	RW	0x00	reg_cmd0_wrap_sel The pin wrap sel of pad A0 for DDRn/LPDDRn Please reference the section 4.3.1 get more information about the pin wrap sel. Not used , the command map is given by RK
23:21	RO	0x0	reserved
20:16	RW	0x01	reg_cmd1_wrap_sel The pin wrap sel of pad A1 for DDRn/LPDDRn Please reference the section 4.3.1 get more information about the pin wrap sel. Not used , the command map is given by RK
15:13	RO	0x0	reserved
12:8	RW	0x02	reg_cmd2_wrap_sel The pin wrap sel of pad A2 for DDRn/LPDDRn Please reference the section 4.3.1 get more information about the pin wrap sel. Not used , the command wrap is given by RK
7:5	RO	0x0	reserved
4:0	RW	0x03	reg_cmd3_wrap_sel The pin wrap sel of pad A3 for DDRn/LPDDRn Please reference the section 4.3.1 get more information about the pin wrap sel. Not used , the command map is given by RK

DDRPHY_COM_REG_0x16

Address: Operational Base(0xFF4F0000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x04	reg_cmd4_wrap_sel The pin wrap sel of pad A4 for DDRn/LPDDRn Please reference the section 4.3.1 get more information about the pin wrap sel. Not used , the command wrap is given by RK
23:21	RO	0x0	reserved
20:16	RW	0x05	reg_cmd5_wrap_sel The pin wrap sel of pad A5 for DDRn/LPDDRn Please reference the section 4.3.1 get more information about the pin wrap sel. Not used , the command wrap is given by RK
15:13	RO	0x0	reserved
12:8	RW	0x06	reg_cmd6_wrap_sel The pin wrap sel of pad A6 for DDRn/LPDDRn Please reference the section 4.3.1 get more information about the pin wrap sel. Not used , the command wrap is given by RK
7:5	RO	0x0	reserved
4:0	RW	0x07	reg_cmd7_wrap_sel The pin wrap sel of pad A7 for DDRn/LPDDRn Please reference the section 4.3.1 get more information about the pin wrap sel. Not used , the command wrap is given by RK

DDRPHY_COM_REG_0x17

Address: Operational Base(0xFF4F0000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x08	reg_cmd8_wrap_sel The pin wrap sel of pad A8 for DDRn/LPDDRn Please reference the section 4.3.1 get more information about the pin wrap sel. Not used , the command wrap is given by RK
23:21	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
20:16	RW	0x09	reg_cmd9_wrap_sel The pin wrap sel of pad A9 for DDRn/LPDDRn Please reference the section 4.3.1 get more information about the pin wrap sel. Not used , the command wrap is given by RK
15:13	RO	0x0	reserved
12:8	RW	0x0a	reg_cmd10_wrap_sel The pin wrap sel of pad A10 for DDRn/LPDDRn Please reference the section 4.3.1 get more information about the pin wrap sel. Not used , the command wrap is given by RK
7:5	RO	0x0	reserved
4:0	RW	0x0b	reg_cmd11_wrap_sel The pin wrap sel of pad A11 for DDRn/LPDDRn Please reference the section 4.3.1 get more information about the pin wrap sel. Not used , the command wrap is given by RK

DDRPHY_COM_REG_0x18

Address: Operational Base(0xFF4F0000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x0c	reg_cmd12_wrap_sel The pin wrap sel of pad A12 for DDRn/LPDDRn Please reference the section 4.3.1 get more information about the pin wrap sel. Not used , the command wrap is given by RK
23:21	RO	0x0	reserved
20:16	RW	0x0d	reg_cmd13_wrap_sel The pin wrap sel of pad A13 for DDRn/LPDDRn Please reference the section 4.3.1 get more information about the pin wrap sel. Not used , the command wrap is given by RK
15:13	RO	0x0	reserved
12:8	RW	0x0e	reg_cmd14_wrap_sel The pin wrap sel of pad A14 for DDRn/LPDDRn Please reference the section 4.3.1 get more information about the pin wrap sel. Not used , the command wrap is given by RK
7:5	RO	0x0	reserved
4:0	RW	0x0f	reg_cmd15_wrap_sel The pin wrap sel of pad A15 for DDRn/LPDDRn Please reference the section 4.3.1 get more information about the pin wrap sel. Not used , the command wrap is given by RK

DDRPHY_COM_REG_0x19

Address: Operational Base(0xFF4F0000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x10	reg_cmd16_wrap_sel The pin wrap sel of pad A16 for DDRn/LPDDRn Please reference the section 4.3.1 get more information about the pin wrap sel. Not used , the command wrap is given by RK
23:21	RO	0x0	reserved
20:16	RW	0x11	reg_cmd17_wrap_sel The pin wrap sel of pad 170 for DDRn/LPDDRn Please reference the section 4.3.1 get more information about the pin wrap sel. Not used , the command wrap is given by RK
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:8	RW	0x12	reg_cmd18_wrap_sel The pin wrap sel of pad ACTN for DDRn/LPDDRn Please reference the section 4.3.1 get more information about the pin wrap sel. Not used , the command wrap is given by RK
7:5	RO	0x0	reserved
4:0	RW	0x13	reg_cmd19_wrap_sel The pin wrap sel of pad BA0 for DDRn/LPDDRn Please reference the section 4.3.1 get more information about the pin wrap sel. Not used , the command wrap is given by RK

DDRPHY_COM_REG_0x1a

Address: Operational Base(0xFF4F0000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x14	reg_cmd20_wrap_sel The pin wrap sel of pad BA1 for DDRn/LPDDRn Please reference the section 4.3.1 get more information about the pin wrap sel. Not used , the command wrap is given by RK
23:21	RO	0x0	reserved
20:16	RW	0x15	reg_cmd21_wrap_sel The pin wrap sel of pad BG0 for DDRn/LPDDRn Please reference the section 4.3.1 get more information about the pin wrap sel. Not used , the command wrap is given by RK
15:13	RO	0x0	reserved
12:8	RW	0x16	reg_cmd22_wrap_sel The pin wrap sel of pad BG1 for DDRn/LPDDRn Please reference the section 4.3.1 get more information about the pin wrap sel. Not used , the command wrap is given by RK
7:5	RO	0x0	reserved
4:0	RW	0x17	reg_cmd23_wrap_sel The pin wrap sel of pad CK for DDRn/LPDDRn Please reference the section 4.3.1 get more information about the pin wrap sel. Not used , the command wrap is given by RK

DDRPHY_COM_REG_0x1b

Address: Operational Base(0xFF4F0000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x18	reg_cmd24_wrap_sel The pin wrap sel of pad CKB for DDRn/LPDDRn Please reference the section 4.3.1 get more information about the pin wrap sel. Not used , the command wrap is given by RK
23:21	RO	0x0	reserved
20:16	RW	0x19	reg_cmd25_wrap_sel Not used
15:13	RO	0x0	reserved
12:8	RW	0x1a	reg_cmd26_wrap_sel Not used
7:5	RO	0x0	reserved
4:0	RW	0x1b	reg_cmd27_wrap_sel Not used

DDRPHY_COM_REG_0x1c

Address: Operational Base(0xFF4F0000) + offset (0x0070)

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Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x1c	reg_cmd28_wrap_sel Not used
23:21	RO	0x0	reserved
20:16	RW	0x1d	reg_cmd29_wrap_sel Not used
15:13	RO	0x0	reserved
12:8	RW	0x1e	reg_cmd30_wrap_sel Not used
7:0	RO	0x00	reserved

DDRPHY_COM_REG_0x1d

Address: Operational Base(0xFF4F0000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	reg_byte0_wrap_sel The wrap select signal of BYTE 0. byte 0 only can exchange with byte1, so only bit[0] can be set
28:26	RW	0x1	reg_byte1_wrap_sel The wrap select signal of BYTE 1. byte 1 only can exchange with byte0, so only bit[0] can be set
25:23	RW	0x2	reg_byte2_wrap_sel The wrap select signal of BYTE 2. byte 2 only can exchange with byte3, so only bit[0] can be set
22:20	RW	0x3	reg_byte3_wrap_sel The wrap select signal of BYTE 3. byte 3 only can exchange with byte2, so only bit[0] can be set
19:17	RW	0x4	reg_byte4_wrap_sel The wrap select signal of BYTE 4.the byte 4 can not exchange with other byte, so do not change the value
16:0	RO	0x00000	reserved

DDRPHY_COM_REG_0x1e

Address: Operational Base(0xFF4F0000) + offset (0x0078)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00008101	reg_cke_ck_cmd_pad_t Because the phy supports the command reamp, so the ck/cke may remap to the other pads, so the user need to use this register to tell the phy which pad is ck/cke. For the ck/cke output pad, the bits should set to 1'b1. [0]:A0 [1]:A1 [2]:A2 [3]:A3 [4]:A4 [5]:A5 [6]:A6 [7]:A7 [8]:A8 [9]:A9 [10]:A10 [11]:A11 [12]:A12 [13]:A13 [14]:A14 [15]:A15 [16]:A16 [17]:A17 [18]:ACTN [19]:BA0 [20]:BA1 [21]:BG0 [22]:BG1 [23]:CK [24]:CKB [25]:CKE0 [26]:CSB0 [27]:CSB1 [28]:ODT0 [29]:ODT1 [30]:CKE1 [31]:RESETN

DDRPHY_COM_REG_0x1f

Address: Operational Base(0xFF4F0000) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	reg_pllfbdiv_dqcmd The control signal of feedback div signal.
15:9	RO	0x00	reserved
8:4	RW	0x01	reg_pllprediv_dqcmd Internal PLL charge bump work frequency adjusts, it can be used to adjust PLL band width, 5'h1 has maximum band width. Please reference the section 4.8 to get more information of PLL.
3:0	RO	0x0	reserved

DDRPHY_COM_REG_0x20

Address: Operational Base(0xFF4F0000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
19:18	RW	0x0	reg_plltestsel_dqcmd Reserved.
17:16	RW	0x1	reg_pllgvco_bias_dqcmd Reserved.
15:11	RO	0x00	reserved
10:8	RW	0x2	reg_pllcpp_bias_dqcmd Reserved.
7	RW	0x0	reg_plltestouten_dqcmd Reserved.
6	RW	0x0	reg_lockenb_dqcmd The power down enable signal of the pll. Active low. 0: Enable the pll. 1: Disalbe the pll.
5	RW	0x0	reg_pllrstbsel_dqcmd Resrved.
4	RW	0x0	reg_pllref_clk_byp_dqcmd Reserved.
3	RW	0x1	reg_ssc_rstn Reserved.
2	RW	0x0	reg_pllincz_dqcmd Reserved.
1	RW	0x1	reg_pllclkouten_dqcmd_t The clock output enable signal of pll. Active high.
0	RW	0x1	reg_pllpd_dqcmd_t Internal PLL power down. Set to 0 to enable the PLL.

DDRPHY_COM_REG_0x21

Address: Operational Base(0xFF4F0000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	reg_hclk_byte4_sel The enable signal of the clock gate for the digital part of byte4. 1: Keep the clock when the byte4 is in idle state. 0: Automatically gate the clock when the byte4 is in idle state.
27	RW	0x0	reg_hclk_train_sel Used to choose the clock state of train logic. 1: Keep clock for train logic when it is in no-train state. 0: Gate clock for train logic when it is in no-train state.
26	RW	0x0	reg_hclk_bist_sel The clock gate control signal of the bist module. 1: Keep the clock of the bist module even the module is not in working state. 0: Auto disable the clock of the bist module when the module is not in working state.
25	RW	0x0	reg_hclk_zqcalib_sel The clock gate control signal of the zqcalib module. 1: Keep the clock of the zqcalib module even the module is not in the training mode. 0: Auto disable the clock of the zqcalib module when the module is not in the training model.
24	RW	0x0	reg_hclk_byte0_sel The enable signal of the clock gate for the digital part of byte0. 1: Keep the clock when the byte0 is in idle state. 0: Automatically gate the clock when the byte0 is in idle state.

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Bit	Attr	Reset Value	Description
23	RW	0x0	reg_hclk_byte1_sel The enable signal of the clock gate for the digital part of byte1. 1: Keep the clock when the byte1 is in idle state. 0: Automatically gate the clock when the byte1 is in idle state.
22	RW	0x0	reg_hclk_byte2_sel The enable signal of the clock gate for the ditial part of byte2. 1: Keep the clock when the byte2 is in idle state. 0: Automatically gate the clock when the byte2 is in idle state.
21	RW	0x0	reg_hclk_byte3_sel The enable signal of the clock gate for the digital part of byte3. 1: Keep the clock when the byte3 is in idle state. 0: Automatically gate the clock when the byte3 is in idle state.
20	RW	0x0	reg_hclk_byte_sel The clock gate control signal of the DQ path common logic. 1: Keep the clock of the common logic at idle state. 0: Auto disable the common logic at idle state.
19	RW	0x0	reg_hclk_ca_sel Used to choose the clock state of command logic. 1: Keep clock of command logic when it is in idle state. 0: Gate clock of command logic when it is in idle state.
18	RW	0x1	reg_train_reg_update_en Disable the clock gate of the train logic. Active high. 1: It will enable the clock of the train logic. 0: Automatically gate the clock when the train logic is in idle state. If the users want to use the register to update the training result through the bypass mode. This register should set to 1'b1 to enable the clock of the training control logic, then the bypass value can be updated to the lock register.
17	RW	0x1	reg_dqclken_t The enable signal of clock for DQ path in the analog circuit. This signal will be used to disable the clk of the DQ module to save the power when the DDR2/3/4 SDRAM goes to power down mode. 1: Keep the clock of the DQ path in the analog circuit. 0: Gate the clock of the DQ path in the analog circuit.
16	RW	0x1	reg_outclken The gating control signal of 1x clock of PHY. Active Low. 0: It will gate the 1x clock of the PHY. 1: The 1x clock of the PHY will be gate automatically in dfi low power mode.
15	RW	0x0	reg_lp_bypass The dfi low power disable signal. When set to high, it will ignore the signals of dfi low power interface.
14	RW	0x1	reg_deep_lp_en The deep low power mode enable signal. 1: Enable the deep low power. 0: Disable the deep low power.
13	RW	0x0	reg_lp_wakeup_sel Reserved.
12	RW	0x1	reg_lp_vref_ctrl_en Disable the bypass mode of the VREF control. 1: Using auto mode the disable VREF at dfi low power mode. 0: Using the register 0x114[4]/0x124[4]/0x134[4]/0x144[4] to disable the VREF.

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Bit	Attr	Reset Value	Description
11:8	RW	0x9	reg_lp_wakeup_threhold Configure the low power mode threshold. When the dfi_lp_wakeup<= threshold, it will go into the normal low power mode; when dfi_lp_wakeup> threshold, it will go into the deep low power mode.
7:6	RW	0x2	reg_lp_io_dis_ctrl Adjust the timing from highz the io to disable the IO when begin the low power flow.
5	RW	0x1	reg_lp_dq_clk_ctrl_en Choose the control mode of the DQ clock path when in low power mode. 1: Auto mode. 0: Bypass mode. Use the register 0x00[1] to control.
4	RW	0x1	reg_lp_dig_rst_ctrl_en Choose the control mode of the reset of the digital core. 1: Auto mode. 0: Not reset.
3	RW	0x1	reg_lp_spll_clktree_ctrl_en Choose the control mode of the clock tree of the pll. 1: Auto mode. 0: Not close.
2	RW	0x1	reg_lp_dig_clk_ctrl_en Choose the control mode of the clock of the digital core. 1: Auto mode. 0: Not close.
1	RW	0x1	reg_lp_io_ctrl_en Choose the control mode of the IO. 1: Auto mode. 0: Not close.
0	RW	0x1	reg_lp_pllpd_ctrl_en Choose the power down mode of the PLL. 1: Auto mode. 0: Not power down.

DDRPHY_COM_REG_0x22

Address: Operational Base(0xFF4F0000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:20	RW	0x1	reg_lp_stvalue The response timing when high the dfi_lp_ack. Unit: dfi_clk1x.
19:16	RW	0x6	reg_lp_ackvalue The response timing when detect the dfi_lp_req is high. Unit: dfi_clk1x.

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Bit	Attr	Reset Value	Description
15:0	RW	0x1388	reg_wait_cnt The bit[7:0] of pll lock wait signal. There are two ways to generate the pll lock. The first way is using the pll_lock from the pll module directly, the second way is using the counter to calcuate the cycle after enable the pll. For the second way, after enable the pll, the phy will start to count until the counter equal the reg_wait_cnt[15:0], the high the pll lock. The bit[15:8] of pll lock wait signal. There are two ways to generate the pll lock. The first way is using the pll_lock from the pll module directly, the second way is using the counter to calcuate the cycle after enable the pll. For the second way, after enable the pll, the phy will start to count until the counter equal the reg_wait_cnt[15:0], the high the pll lock.

DDRPHY_COM_REG_0x23

Address: Operational Base(0xFF4F0000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	reg_lpddr4x_zqcal when do zqcalib, if lpddr4x ,set this register to 1, else set it to 0
28:20	RW	0x1ff	reg_zq_chg_interval The timing interval of the zqcalib training value changing when we do the zq calibration. Unit: dfi_clk1x
19	RO	0x0	reserved
18:10	RW	0x03f	reg_pu_interval The timing interaval of the zqcalib between the pull down training state to pull up training state. Unit:dfi_clk1x.
9:4	RO	0x00	reserved
3	RW	0x1	reg_pd_zqcali The power down signal of zqcalib module when enable the zqcalib function. 1: Power down mode. 0: Normal work mode.
2	RW	0x0	reg_zqcali_clear The clean signal of zqcalib module. High is valid.
1	RW	0x0	reg_zqcali_bypass The bypass enable of zqcalib function. Active high. 1: The phy will use the register reg_drvlegn_zqcali/reg_drvlegpb_zqcali/reg_odtlegn_zqcali/reg_odtlegpb_zqcali to control zqcalib. 0: It will use the zqcali module to control.
0	RW	0x0	reg_zqcali_en The enable signal of zqcalib function.

DDRPHY_COM_REG_0x24

Address: Operational Base(0xFF4F0000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x0e	reg_drvlegpd_zqcali The drivier pull-down value when reg_zqcali_bypass(reg0x66[4]) set to 1'b1 to enable the zqcalib bypass function.
23:21	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
20:16	RW	0x0e	reg_drvlegpu_zqcali The drivier pull-up value when reg_zqcali_bypass(reg0x66[4]) set to 1'b1 to enable the zqcalib bypass function.
15:13	RO	0x0	reserved
12:8	RW	0x07	reg_odtlegpd_zqcali The odt pull-up value when reg_zqcali_bypass(reg0x66[4]) set to 1'b1 to enable the zqcalib bypass function.
7:5	RO	0x0	reserved
4:0	RW	0x07	reg_odtlegpu_zqcali The odt pull up value when reg_zqcali_bypass(reg0x66[4]) set to 1'b1 to enable the zqcalib bypass function.

DDRPHY_COM_REG_0x25

Address: Operational Base(0xFF4F0000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	reg_ddrphy_trp
23	RW	0x0	reg_ddrphy_rtrain_en
22:15	RO	0x00	reserved
14	RW	0x0	reg_rd_train_perdef_en The enable signal of the read predef training, predefine Mode. 1: Enable the predef train of the read train. 0: Exit the predef train of the read train
13	RW	0x0	reg_train_vref_en The enable signal of the vref training. 1: Enable the vref train of the read train(predefine mode)/write train. 0: Exit the vref train of the read train(predefine mode)/write train. reuse for rd perdef training and wr training
12	RW	0x0	reg_ddr4_dbi When you enable rd DBI function of DDR4, and you want to do wr training with DBI open, you should set this register to 1'b1 at first. 1: support the DBI function during wr training. 0: Nonsupports the DBI function during wr training.
11:8	RW	0x0	reg_rdtrain_cs_sel Choose the rank of the read train. 4'b0111: Choose Rank3. 4'b1011: Choose Rank2. 4'b1101: Choose Rank1. 4'b1110: Choose Rank0.
7	RW	0x0	reg_rx_vref_value_update When You want to change the PHY's vref value, you should config this register , at posedge of this register, the value of reg_a/b_l/r_vref1_margsel will be latched to PHY.
6	RW	0x0	reg_rd_train_dqs_range_bypass The enable signal to setting the DQS scan range using the register.(rd training) 1: Enable to use the register to set the DQS scan range. 0: Use the default DQS scan range[0~7'h7f].
5	RW	0x0	reg_bypass_rd_train_cmd_start_en Generate the read train command when enable bypass read training mode. High pulse valid.

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Bit	Attr	Reset Value	Description
4	RW	0x0	reg_bypass_rd_train_en Enable the bypass read train function. 1: Enable the read train bypass mode. 0: Disable the read train bypass mode.
3	RW	0x0	reg_rd_train_check_value_en Choose the check value of the read train. 0: Use the fix mode. DDR3 = 8'b10101010 LPDDR3 = 16'hcc55 LPDDR4 = {MR#40,MR#32} DDR4 = 8'haa/8'hcc/8'hf0/8'h00 1: Use the register to configure.
2	RW	0x0	reg_rd_train_freq_update When You want to change the PHY's rx per-bit skew value, you should config this register , at posedge of this signal, the value of reg_dqxx_invdelayselrx will be latched to PHY.
1	RW	0x0	reg_dqs_rd_train_en The enable signal of the DQS Scan.(rd training) 1: The auto read train will complete the DQ perbit skew train and DQS-DQ Eye train.(not suggest) 0: The auto read train will only complete the DQ perbit skew train.
0	RW	0x0	reg_dq_rd_train_en The enable signal of the read training Auto Mode. 1: Enable the auto train of the read train. 0: Exit the auto train of the read train.

DDRPHY_COM_REG_0x26

Address: Operational Base(0xFF4F0000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:24	RW	0x55	reg_lpddr4_mr15_value The load mode value of MR15 when do the read train of LPDDR4.if you want to change the check pattern of LPDDR4 , you can change the value of this register before rd training.
23:16	RW	0x55	reg_lpddr4_mr20_value The load mode value of MR20 when do the read train of LPDDR4.if you want to change the check pattern of LPDDR4 , you can change the value of this register before rd training.
15:8	RW	0x5a	reg_lpddr4_mr32_value The load mode value of MR32 when do the read train of LPDDR4.if you want to change the check pattern of LPDDR4 , you can change the value of this register before rd training.
7:0	RW	0x3c	reg_lpddr4_mr40_value The load mode value of MR40 when do the read train of LPDDR4.if you want to change the check pattern of LPDDR4 , you can change the value of this register before rd training.

DDRPHY_COM_REG_0x27

Address: Operational Base(0xFF4F0000) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	reg_ddr4_mr4_value Used to control the DDR4 load mode value of MR4 when the register reg_calib_mode_sel = 1'b1, when ddr4 calib, set this register as current SDRAM MR4(A15~A0) value. The calib operation will write new data to the MR4, so we should keep the other bits the same with the current MR4.

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Bit	Attr	Reset Value	Description
15:8	RO	0x00	reserved
7:0	RW	0x00	reg_ddr4_mr3 Used to control the DDR4 load mode value of MR3 when read training(MPR), when ddr4 read training, set this register as current SDRAM MR3(A10~A3) value. The read training operation will write new data to the MR3, so we should keep the other bits the same with the current MR3.

DDRPHY_COM_REG_0x28

Address: Operational Base(0xFF4F0000) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RW	0x0	reg_dm_wr_train_en The enable signal of the write training of dm after dq wr train. 1: Enable the dm wr training. 0: Disable the dm wr training.
24	RW	0x1	reg_wrtrain_lpddr4_vref_range Choose the adjust range of SDRAM's vref , reference to JESD-LPDDR4
23:16	RW	0x00	reg_pbit_deskew_offset_for_lpddr4 The tx delay line adjust signal of the DQS/DQSB after the write-leveling. The tx delay line value will equal the write-leveing result + reg_pbit_deskew_offset_for_lpddr4 and apply to the DQ/DM.
15:12	RO	0x0	reserved
11	RW	0x0	reg_dqs_wr_train_en The enable signal of the DQS Scan. When this bit set to 1, it will enable adjust the DQS to find the best window of the DQ. Only used for debug, because it will change the write-leveling result if the user enable the write leveling function.
10	RW	0x1	reg_wrtrain_check_data_value_random_gen 1'b1: PHY generate random data and write to SDRAM during write training. 1'b0: the user config dq0-7_train_check_data_value0-9 and PHY write it (10*BL8) to SDRAM during write training.
9:6	RW	0x0	reg_wrtrain_cs_sel Choose the rank of the write train. 4'b0111: Choose Rank3. 4'b1011: Choose Rank2. 4'b1101: Choose Rank1. 4'b1110: Choose Rank0.
5	RW	0x0	reg_wr_train_rst The wr train fsm clear signal. 1: Reset the write train fsm. 0: Keep the current state.
4	RW	0x0	reg_wr_train_dqs_default_bypass Choose the DQS default value when enable the write train (The DQS scan mode is disabled). 0: Use the write-leveling value. 1: Use the register to choose the default value.
3	RW	0x0	reg_wr_train_dqs_range_bypass The enable signal to setting the DQS scan range using the register.(wr training) 1: Enable to use the register to set the DQS scan range. 0: Use the default DQS scan range[0~6'h3f].

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Bit	Attr	Reset Value	Description
2	RW	0x0	reg_wr_train_freq_update not used
1	RW	0x0	reg_dq_wr_train_en The enable signal of the write training Auto Mode. 1: Enable the auto train of the read train. 0: Exit the auto train of the read train.
0	RW	0x0	reg_dq_wr_train_auto Choose the mode of the write train. 1: Choose the write train auto mode,you should set it to 1'b1 before write train.

DDRPHY_COM_REG_0x29

Address: Operational Base(0xFF4F0000) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RW	0x0	reg_wr_train_ba_addr The bit[2:0] of bank address for write/read operation in DDR3/4 and LPDDR3 write training mode.](reuse for rd perdef training and wr training)
27:26	RO	0x0	reserved
25:16	RW	0x000	reg_wr_train_col_addr The bit[7:0] of col address for write/read operation in DDR3/4 and LPDDR3 write training mode.](reuse for rd perdef training and wr training) The bit[9:8] of col address for write/read operation in DDR3/4 and LPDDR3 write training mode.(reuse for rd perdef training and wr training)
15:0	RW	0x0001	reg_wr_train_row_addr The bit[7:0] of row address for write/read operation in DDR3/4 and LPDDR3 write training mode.(reuse for rd perdef training and wr training) The bit[15:8] of row address for write/read operation in DDR3/4 and LPDDR3 write training mode.(reuse for rd perdef training and wr training)

DDRPHY_COM_REG_0x2a

Address: Operational Base(0xFF4F0000) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:18	RW	0x0960	reg_phy_trefi The value is Trefi/dfi_clk1x
17:8	RW	0x08c	reg_phy_trfc The register is used to control the auto-refresh interval when the phy do the training. The reg_phy_trfc[9:0] = {reg0x4e[7:6],reg0x57[7:0]}. The auto-refresh interval = reg_phy_trfc *Tdfi_clk1x. The bit9 and bit 8 of the reg_phy_trfc. The reg_phy_trfc is used to control the interval of the auto-refresh. The PHY will send the auto-refresh when it is in the training mode. Auto-refresh interval = reg_phy_trfc* Tdfi_clk1x
7:4	RW	0x8	reg_max_refi_cnt this register used in wr/rd training,if you set reg_phy_refresh_en to 1'b1. this register means how many auto refresh cmd can be accumulated at one time.the maximum is 8,and the larger the value ,the less time training takes .
3:1	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	reg_phy_refresh_en When you want to enable phy auto refresh function in training, you should set this reg to 1 at frist.

DDRPHY_COM_REG_0x2b

Address: Operational Base(0xFF4F0000) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	reg_freq_choose_wr_bypass
11:6	RW	0x00	reg_data_path_clk_gate_dly Reserved.
5	RW	0x0	reg_data_path_clk_gate_dly_bp Reserved.
4	RW	0x0	reg_freq_choose_op_bypass The bypass signal of the freq point choose. Active High. 1: It will use the reg_freq_choose_t to choose the freq point. 0: The phy will choose the freq point based on the dfi_freqeuncy at the phy initialization and fast frequency change.
3	RW	0x0	reg_all_freq_train_finish keep default
2	RW	0x0	reg_pll_lock_bypass Choose the way to wait for the pll lock after the pll enable. 0: Wait the pll lock from the pll module. 1: Wait the pll lock by enable the pll lock counter after the pll enable.
1	RW	0x0	reg_pllpd_bypass Choose the way to control the pll pd signal of the pll module. 1: Only can use the register to control. 0: Automatically control in the dfi low power mode.
0	RW	0x0	reg_lpddr4_write_postamble_sel The write postamble control signal of the LPDDR4 mode. Please keep the same setting with the LPDDR4 MR1[7]. 1:1.5*tCK. 0:0.5*tCK.

DDRPHY_COM_REG_0x2c

Address: Operational Base(0xFF4F0000) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	reg_a7_lp4x_en_reg when use lpddr4x ,this register should be set to 1.
14	RW	0x1	reg_a7_pvt_comp_en enable the pvt compensation function
13	RW	0x0	reg_a6_lp4x_en_reg when use lpddr4x ,this register should be set to 1.
12	RW	0x1	reg_a6_pvt_comp_en enable the pvt compensation function
11	RW	0x0	reg_a5_lp4x_en_reg when use lpddr4x ,this register should be set to 1.
10	RW	0x1	reg_a5_pvt_comp_en enable the pvt compensation function
9	RW	0x0	reg_a4_lp4x_en_reg when use lpddr4x ,this register should be set to 1.
8	RW	0x1	reg_a4_pvt_comp_en enable the pvt compensation function

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Bit	Attr	Reset Value	Description
7	RW	0x0	reg_a3_lp4x_en_reg when use lpddr4x ,this register should be set to 1.
6	RW	0x1	reg_a3_pvt_comp_en enable the pvt compensation function
5	RW	0x0	reg_a2_lp4x_en_reg when use lpddr4x ,this register should be set to 1.
4	RW	0x1	reg_a2_pvt_comp_en enable the pvt compensation function
3	RW	0x0	reg_a1_lp4x_en_reg when use lpddr4x ,this register should be set to 1.
2	RW	0x1	reg_a1_pvt_comp_en enable the pvt compensation function
1	RW	0x0	reg_a0_lp4x_en_reg when use lpddr4x ,this register should be set to 1.
0	RW	0x1	reg_a0_pvt_comp_en enable the pvt compensation function

DDRPHY_COM_REG_0x2d

Address: Operational Base(0xFF4F0000) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	reg_a15_lp4x_en_reg when use lpddr4x ,this register should be set to 1.
14	RW	0x1	reg_a15_pvt_comp_en enable the pvt compensation function
13	RW	0x0	reg_a14_lp4x_en_reg when use lpddr4x ,this register should be set to 1.
12	RW	0x1	reg_a14_pvt_comp_en enable the pvt compensation function
11	RW	0x0	reg_a13_lp4x_en_reg when use lpddr4x ,this register should be set to 1.
10	RW	0x1	reg_a13_pvt_comp_en enable the pvt compensation function
9	RW	0x0	reg_a12_lp4x_en_reg when use lpddr4x ,this register should be set to 1.
8	RW	0x1	reg_a12_pvt_comp_en enable the pvt compensation function
7	RW	0x0	reg_a11_lp4x_en_reg when use lpddr4x ,this register should be set to 1.
6	RW	0x1	reg_a11_pvt_comp_en enable the pvt compensation function
5	RW	0x0	reg_a10_lp4x_en_reg when use lpddr4x ,this register should be set to 1.
4	RW	0x1	reg_a10_pvt_comp_en enable the pvt compensation function
3	RW	0x0	reg_a9_lp4x_en_reg when use lpddr4x ,this register should be set to 1.
2	RW	0x1	reg_a9_pvt_comp_en enable the pvt compensation function
1	RW	0x0	reg_a8_lp4x_en_reg when use lpddr4x ,this register should be set to 1.
0	RW	0x1	reg_a8_pvt_comp_en enable the pvt compensation function

DDRPHY_COM_REG_0x2e

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Address: Operational Base(0xFF4F0000) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x1	reg_cmd_ca_enb_lp4 When the value is 1'b0, enble the Lpddr4's Tx drive pull down , you can keep it to 1
15	RW	0x0	reg_resetn_lp4x_en_reg this register should also keep 0.
14	RW	0x1	reg_resetn_pvt_comp_en enable the pvt compensation function
13	RW	0x0	reg_bg1_lp4x_en_reg when use lpddr4x, this register should be set to 1.
12	RW	0x1	reg_bg1_pvt_comp_en enable the pvt compensation function
11	RW	0x0	reg_bg0_lp4x_en_reg when use lpddr4x, this register should be set to 1.
10	RW	0x1	reg_bg0_pvt_comp_en enable the pvt compensation function
9	RW	0x0	reg_ba1_lp4x_en_reg when use lpddr4x, this register should be set to 1.
8	RW	0x1	reg_ba1_pvt_comp_en enable the pvt compensation function
7	RW	0x0	reg_ba0_lp4x_en_reg when use lpddr4x, this register should be set to 1.
6	RW	0x1	reg_ba0_pvt_comp_en enable the pvt compensation function
5	RW	0x0	reg_actn_lp4x_en_reg when use lpddr4x, this register should be set to 1.
4	RW	0x1	reg_actn_pvt_comp_en enable the pvt compensation function
3	RW	0x0	reg_a17_lp4x_en_reg when use lpddr4x, this register should be set to 1.
2	RW	0x1	reg_a17_pvt_comp_en enable the pvt compensation function
1	RW	0x0	reg_a16_lp4x_en_reg when use lpddr4x, this register should be set to 1.
0	RW	0x1	reg_a16_pvt_comp_en enable the pvt compensation function

DDRPHY_COM_REG_0x2f

Address: Operational Base(0xFF4F0000) + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	reg_odt1_lp4x_en_reg this register should also keep 0.
14	RW	0x1	reg_odt1_pvt_comp_en enable the pvt compensation function
13	RW	0x0	reg_odt0_lp4x_en_reg this register should also keep 0.
12	RW	0x1	reg_odt0_pvt_comp_en enable the pvt compensation function
11	RW	0x0	reg_csb1_lp4x_en_reg when use lpddr4x ,this register should be set to 1.
10	RW	0x1	reg_csb1_pvt_comp_en enable the pvt compensation function

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Bit	Attr	Reset Value	Description
9	RW	0x0	reg_csb0_lp4x_en_reg when use lpddr4x, this register should be set to 1.
8	RW	0x1	reg_csb0_pvt_comp_en enable the pvt compensation function
7	RW	0x0	reg_cke1_lp4x_en_reg this register should also keep 0.
6	RW	0x1	reg_cke1_pvt_comp_en enable the pvt compensation function
5	RW	0x0	reg_cke0_lp4x_en_reg this register should also keep 0.
4	RW	0x1	reg_cke0_pvt_comp_en enable the pvt compensation function
3	RW	0x0	reg_ckb_lp4x_en_reg when use lpddr4x, this register should be set to 1.
2	RW	0x1	reg_ckb_pvt_comp_en enable the pvt compensation function
1	RW	0x0	reg_ck_lp4x_en_reg when use lpddr4x, this register should be set to 1.
0	RW	0x1	reg_ck_pvt_comp_en enable the pvt compensation function

DDRPHY_COM_REG_0x30

Address: Operational Base(0xFF4F0000) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RW	0x1	reg_pllpostdiv_ls The reigister used to control the post div for low speed(which will be used for CA Training and PHY initializaiton). For different freuency range, the value of post div enable state is different. The user needs to based on the frequency of the low speed to set this register. Please reference to the chapter 9 to get more information about how to set register based on different frequency.
27	RW	0x1	reg_pllpostdiven_ls The reigister used to control the post div enable for low speed(which will be used for CA Training and PHY initialization). For different freuency range, the state of post div enable state is different. The user needs to based on the frequency of the low speed to set this register. Please reference to the chapter 9 to get more information about how to set register based on different frequency
26:24	RW	0x2	reg_pllcpi_bias_ls
23:21	RO	0x0	reserved
20	RW	0x0	reg_io_highz_dis
19	RO	0x0	reserved
18	RW	0x0	reg_cmd_delay_one_ui delay the cmd for one ui,base on the cmd 2t mode(reg_cmd_2t_mode=1).
17	RW	0x0	reg_cmd_2t_mode enable cmd 2t mode,
16	RW	0x0	reg_phy_sdram_initial initial the sdram through phy. When lpddr4 ca training, this register should be set to 1'b1, phy will initial the sdram itself.
15:8	RW	0x60	reg_wl_dqs_start_point write leveling's dqs tx delay start point

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Bit	Attr	Reset Value	Description
7:1	RW	0x3f	reg_rd_train_dqs_scan_max the max rx dqs delay when do rd training dqs scan.
0	RW	0x1	reg_pvt_comp_dis disable pvt compensation fuction

DDRPHY_COM_REG_0x31

Address: Operational Base(0xFF4F0000) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	reg_mdll_update_cnt_clear clear the counter of dll_update.
7:0	RW	0x04	reg_mdll_chg_margin when the diff of dll lock value more than this value , the phy will send a pvt compensation req.

DDRPHY_COM_REG_0x32

Address: Operational Base(0xFF4F0000) + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:24	RW	0x64	reg_ddrc_treset_h_x1024 when lpddr4 initial , reset need keep high 2ms, so this register's value = 2ms/(1024*dfi1xclk)
23:16	RW	0x1f	reg_ddrc_treset_l_x1024 when lpddr4 initial , phy need to wait 2us, so this register's value = 2us/(1024*dfi1xclk)
15:8	RW	0x1f	reg_ddrc_tckeh when lpddr4 initial , this register's value = tckeh/(32*dfi1xclk)
7:0	RW	0x1f	reg_ddrc_tzqlat when lpddr4 initial , this register's value = tzqlat/(dfi1xclk)

DDRPHY_COM_REG_0x33

Address: Operational Base(0xFF4F0000) + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x5f	reg_ddrc_tzqinit when lpddr4 initial , this register's value = tzqinit/(dfi1xclk)

DDRPHY_COM_REG_0x34

Address: Operational Base(0xFF4F0000) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RW	0x0	reg_pllpostdiv_fsp3 The reigister used to control the post div for low speed(which will be used for CA Training and PHY initializaiton). For different freuency range, the value of post div enable state is different. The user needs to based on the frequency of the low speed to set this register. Please reference to the chapter 9 to get more information about how to set register based on different frequency.

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Bit	Attr	Reset Value	Description
27	RW	0x0	reg_pllpostdiven_fsp3 The reigister used to control the post div enable for low speed(which will be used for CA Training and PHY initialization). For different freuency range, the state of post div enable state is different. The user needs to based on the frequency of the low speed to set this register. Please reference to the chapter 9 to get more information about how to set register based on different frequency
26:24	RW	0x0	reg_pllcpi_bias_fsp3
23	RO	0x0	reserved
22:20	RW	0x0	reg_pllpostdiv_fsp2 The reigister used to control the post div for low speed(which will be used for CA Training and PHY initializaiton). For different freuency range, the value of post div enable state is different. The user needs to based on the frequency of the low speed to set this register. Please reference to the chapter 9 to get more information about how to set register based on different frequency.
19	RW	0x0	reg_pllpostdiven_fsp2 The reigister used to control the post div enable for low speed(which will be used for CA Training and PHY initialization). For different freuency range, the state of post div enable state is different. The user needs to based on the frequency of the low speed to set this register. Please reference to the chapter 9 to get more information about how to set register based on different frequency
18:16	RW	0x0	reg_pllcpi_bias_fsp2
15	RO	0x0	reserved
14:12	RW	0x0	reg_pllpostdiv_fsp1 The reigister used to control the post div for low speed(which will be used for CA Training and PHY initializaiton). For different freuency range, the value of post div enable state is different. The user needs to based on the frequency of the low speed to set this register. Please reference to the chapter 9 to get more information about how to set register based on different frequency.
11	RW	0x0	reg_pllpostdiven_fsp1 The reigister used to control the post div enable for low speed(which will be used for CA Training and PHY initialization). For different freuency range, the state of post div enable state is different. The user needs to based on the frequency of the low speed to set this register. Please reference to the chapter 9 to get more information about how to set register based on different frequency
10:8	RW	0x0	reg_pllcpi_bias_fsp1
7	RO	0x0	reserved
6:4	RW	0x0	reg_pllpostdiv_fsp0 The reigister used to control the post div for low speed(which will be used for CA Training and PHY initializaiton). For different freuency range, the value of post div enable state is different. The user needs to based on the frequency of the low speed to set this register. Please reference to the chapter 9 to get more information about how to set register based on different frequency.

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Bit	Attr	Reset Value	Description
3	RW	0x0	reg_pllpostdiven_fsp0 The reigister used to control the post div enable for low speed(which will be used for CA Training and PHY initialization). For different freuency range, the state of post div enable state is different. The user needs to based on the frequency of the low speed to set this register. Please reference to the chapter 9 to get more information about how to set register based on different frequency
2:0	RW	0x3	reg_pllcpi_bias_fsp0

DDRPHY_COM_REG_0x35

Address: Operational Base(0xFF4F0000) + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	reg_rx_lock_code_bp_value when reg_rx_lock_code_bp_en=1 , the value of register reg_rx_lock_code_bp_value is dll lock value
15:8	RW	0x00	reg_tx_lock_code_bp_value when reg_tx_lock_code_bp_en=1 , the value of register reg_tx_lock_code_bp_value is dll lock value
7:0	RW	0x08	reg_pvt_comp_req_wait_cnt when phy send a pvt req(dfi_phymstr_req),it need get a pvt ack(dfi_phymstr_ack) from ctrl, this register is used to change the time of timeout

DDRPHY_COM_REG_0x36

Address: Operational Base(0xFF4F0000) + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:24	RW	0x80	reg_drvpd_zqcali_vref_sel Reference selection register for driver pull down zq calib, see chapter4.6 zqcalib
23:16	RW	0x80	reg_drvpu_zqcali_vref_sel Reference selection register for driver pull up zq calib,see chapter4.6 zqcalib
15:8	RW	0x80	reg_odtpd_zqcali_vref_sel Reference selection register for odt pull down zq calib,see chapter4.6 zqcalib
7:0	RW	0x80	reg_odtpu_zqcali_vref_sel Reference selection register for odt pull up zq calib,see chapter4.6 zqcalib

DDRPHY_COM_REG_0x37

Address: Operational Base(0xFF4F0000) + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10	RW	0x0	reg_osc_sel The osc select signal. 0: transform reg_invdelaysel_osc_reg with dll decode . 1: Choose the register reg_invdelaysel_osc_reg directly.
9:8	RO	0x0	reserved
7:0	RW	0x80	reg_invdelaysel_osc_reg used to measure the delay capability of invdealysel

DDRPHY_COM_REG_0x38

Address: Operational Base(0xFF4F0000) + offset (0x00E0)

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Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x3f	reg_cat_cs_right_scan_steps
7:0	RW	0x3f	reg_cat_cs_left_scan_steps

DDRPHY_COM_REG_0x39

Address: Operational Base(0xFF4F0000) + offset (0x00E4)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:0	RW	0x00000000	reg_cmd_io_highz set 1 to highz io

DDRPHY_COM_REG_0x3a

Address: Operational Base(0xFF4F0000) + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RW	0x0	reg_dfx_pvt_cmp_cnt_clr
24:17	RW	0x00	reg_dfx_pvt_data_sel
16:13	RW	0x1	reg_rtrain_rank_num
12:5	RW	0x20	reg_rtrain_chk_done_prd
4	RW	0x0	reg_rtrain_cnt_clear
3	RW	0x0	reg_pvt_compensation_cnt_clear
2	RO	0x0	reserved
1	RW	0x0	reg_ddrphy_pvt_rtrain_en
0	RO	0x0	reserved

DDRPHY_COM_REG_0x3b

Address: Operational Base(0xFF4F0000) + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:0	RW	0x007fffff	reg_cmd_2t_mode_value

DDRPHY_COM_REG_0x3c

Address: Operational Base(0xFF4F0000) + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:18	RW	0x00	reg_abutslewpu_ck_chb CMD/CK rising edge slew rate control, larger value means larger rising slew rate.
17	RW	0x0	reg_cmd_invdelay_lp_en Reserved.
16	RW	0x0	reg_cmd_drv_zqcalib_en The comand driver control signal. 1: Choose the zqcalibration result as the control signal. 0: Choose the register as the conrol signal.
15	RW	0x0	reg_cmd_fbsel_reg The phy bist command path seletc signal. 0: Choose to arrive the pad. 1: Choose the interal as the end.
14	RW	0x0	reg_cmd_fben_reg The phy bist cmmand feebback enable signal. Active high. Just used for debug.
13	RW	0x1	reg_cmd_abutweakpub_reg The enable signal of CMD PAD weak pull up. Active Low.

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Bit	Attr	Reset Value	Description
12:8	RW	0x00	reg_cmd_abutslewpu_reg CMD/CK rising edge slew rate control, larger value means larger risign slew rate.
7:6	RO	0x0	reserved
5	RW	0x0	reg_cmd_abutweakpd_reg The enable signal of CMD PAD weak pull down. Active high.
4:0	RW	0x00	reg_cmd_abutslewpd_reg CMD/CK falling edge slew rate control, larger value means larger falling slew rate.

DDRPHY_COM_REG_0x3d

Address: Operational Base(0xFF4F0000) + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	reg_cmd_abutnrcomp4_reg The pull-down resistance of CMD except CK. The resistance relation with the configuration show in Table 4 7 and Table 4 8.
27	RW	0x1	reg_cmd_abutnrcomp3_reg The pull-down resistance of CMD except CK. The resistance relation with the configuration show in Table 4 7 and Table 4 8.
26	RW	0x1	reg_cmd_abutnrcomp2_reg The pull-down resistance of CMD except CK. The resistance relation with the configuration show in Table 4 7 and Table 4 8.
25	RW	0x1	reg_cmd_abutnrcomp1_reg The pull-down resistance of CMD except CK. The resistance relation with the configuration show in Table 4 7 and Table 4 8.
24	RW	0x0	reg_cmd_abutnrcomp0_reg The pull-down resistance of CMD except CK. The resistance relation with the configuration show in Table 4 7 and Table 4 8.
23:21	RO	0x0	reserved
20	RW	0x0	reg_cmd_abutprcomp4_reg The pull-up resistance of CMD except CK. The resistance relation with the configuration show in Table 4 7 and Table 4 8.
19	RW	0x1	reg_cmd_abutprcomp3_reg The pull-up resistance of CMD except CK. The resistance relation with the configuration show in Table 4 7 and Table 4 8.
18	RW	0x1	reg_cmd_abutprcomp2_reg The pull-up resistance of CMD except CK. The resistance relation with the configuration show in Table 4 7 and Table 4 8.
17	RW	0x1	reg_cmd_abutprcomp1_reg The pull-up resistance of CMD except CK. The resistance relation with the configuration show in Table 4 7 and Table 4 8.
16	RW	0x0	reg_cmd_abutprcomp0_reg The pull-up resistance of CMD except CK. The resistance relation with the configuration show in Table 4 7 and Table 4 8.

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Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12	RW	0x0	reg_cmd_abutnrcomp4_ck0_reg The pull-down resistance of CK and CKB. The resistance relation with the configuration show in Table 4 7 and Table 4 8.
11	RW	0x1	reg_cmd_abutnrcomp3_ck0_reg The pull-down resistance of CK and CKB. The resistance relation with the configuration show in Table 4 7 and Table 4 8.
10	RW	0x1	reg_cmd_abutnrcomp2_ck0_reg The pull-down resistance of CK and CKB. The resistance relation with the configuration show in Table 4 7 and Table 4 8.
9	RW	0x1	reg_cmd_abutnrcomp1_ck0_reg The pull-down resistance of CK and CKB. The resistance relation with the configuration show in Table 4 7 and Table 4 8.
8	RW	0x0	reg_cmd_abutnrcomp0_ck0_reg The pull-down resistance of CK and CKB. The resistance relation with the configuration show in Table 4 7 and Table 4 8.
7:5	RO	0x0	reserved
4	RW	0x0	reg_cmd_abutprcomp4_ck0_reg The pull-up resistance of CK and CKB. The resistance relation with the configuration show in Table 4 7 and Table 4 8.
3	RW	0x1	reg_cmd_abutprcomp3_ck0_reg The pull-up resistance of CK and CKB. The resistance relation with the configuration show in Table 4 7 and Table 4 8.
2	RW	0x1	reg_cmd_abutprcomp2_ck0_reg The pull-up resistance of CK and CKB. The resistance relation with the configuration show in Table 4 7 and Table 4 8.
1	RW	0x1	reg_cmd_abutprcomp1_ck0_reg The pull-up resistance of CK and CKB. The resistance relation with the configuration show in Table 4 7 and Table 4 8.
0	RW	0x0	reg_cmd_abutprcomp0_ck0_reg The pull-up resistance of CK and CKB. The resistance relation with the configuration show in Table 4 7 and Table 4 8.

DDRPHY_COM_REG_0x3e

Address: Operational Base(0xFF4F0000) + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x080	reg_ram_vref1_margsel_reg Reserved.
15:13	RO	0x0	reserved
12	RW	0x0	reg_cmd_abutnrcomp4_special_reg Reserved.
11	RW	0x1	reg_cmd_abutnrcomp3_special_reg Reserved.

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Bit	Attr	Reset Value	Description
10	RW	0x1	reg_cmd_abutnrcomp2_special_reg Reserved.
9	RW	0x1	reg_cmd_abutnrcomp1_special_reg Reserved.
8	RW	0x0	reg_cmd_abutnrcomp0_special_reg Reserved.
7:5	RO	0x0	reserved
4	RW	0x0	reg_cmd_abutprcomp4_special_reg Reserved.
3	RW	0x1	reg_cmd_abutprcomp3_special_reg Reserved.
2	RW	0x1	reg_cmd_abutprcomp2_special_reg Reserved.
1	RW	0x1	reg_cmd_abutprcomp1_special_reg Reserved.
0	RW	0x0	reg_cmd_abutprcomp0_special_reg Reserved.

DDRPHY_COM_REG_0x3f

Address: Operational Base(0xFF4F0000) + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	reg_mr22_rank3 rank3' mr22 for lpddr4
15:8	RW	0x00	reg_mr22_rank2 rank2' mr22 for lpddr4
7:0	RW	0x00	reg_mr22_rank1 rank1' mr22 for lpddr4

DDRPHY_COM_REG_0x41

Address: Operational Base(0xFF4F0000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:24	RW	0x80	reg_a0_invdelaysel_bp The register used to control the tx delay line of the A0.Each step is 4UI/256.
23:16	RW	0x80	reg_a1_invdelaysel_bp The register used to control the tx delay line of the A1.Each step is 4UI/256.
15:8	RW	0x80	reg_a2_invdelaysel_bp The register used to control the tx delay line of the A2.Each step is 4UI/256.
7:0	RW	0x80	reg_a3_invdelaysel_bp The register used to control the tx delay line of the A3.Each step is 4UI/256.

DDRPHY_COM_REG_0x42

Address: Operational Base(0xFF4F0000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:24	RW	0x80	reg_a4_invdelaysel_bp The register used to control the tx delay line of the A4.Each step is 4UI/256.
23:16	RW	0x80	reg_a5_invdelaysel_bp The register used to control the tx delay line of the A5.Each step is 4UI/256.

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Bit	Attr	Reset Value	Description
15:8	RW	0x80	reg_a6_invdelaysel_bp The register used to control the tx delay line of the A6.Each step is 4UI/256.
7:0	RW	0x80	reg_a7_invdelaysel_bp The register used to control the tx delay line of the A7.Each step is 4UI/256.

DDRPHY_COM_REG_0x43

Address: Operational Base(0xFF4F0000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:24	RW	0x80	reg_a8_invdelaysel_bp The register used to control the tx delay line of the A8.Each step is 4UI/256.
23:16	RW	0x80	reg_a9_invdelaysel_bp The register used to control the tx delay line of the A9.Each step is 4UI/256.
15:8	RW	0x80	reg_a10_invdelaysel_bp The register used to control the tx delay line of the A10.Each step is 4UI/256.
7:0	RW	0x80	reg_a11_invdelaysel_bp The register used to control the tx delay line of the A11.Each step is 4UI/256.

DDRPHY_COM_REG_0x44

Address: Operational Base(0xFF4F0000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:24	RW	0x80	reg_a12_invdelaysel_bp The register used to control the tx delay line of the A12.Each step is 4UI/256.
23:16	RW	0x80	reg_a13_invdelaysel_bp The register used to control the tx delay line of the A13.Each step is 4UI/256.
15:8	RW	0x80	reg_a14_invdelaysel_bp The register used to control the tx delay line of the A14.Each step is 4UI/256.
7:0	RW	0x80	reg_a15_invdelaysel_bp The register used to control the tx delay line of the A15.Each step is 4UI/256.

DDRPHY_COM_REG_0x45

Address: Operational Base(0xFF4F0000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:24	RW	0x80	reg_a16_invdelaysel_bp The register used to control the tx delay line of the A16.Each step is 4UI/256.
23:16	RW	0x80	reg_a17_invdelaysel_bp The register used to control the tx delay line of the A17.Each step is 4UI/256.
15:8	RW	0x80	reg_ba0_invdelaysel_bp The register used to control the tx delay line of the BA0.Each step is 4UI/256.
7:0	RW	0x80	reg_ba1_invdelaysel_bp The register used to control the tx delay line of the BA1.Each step is 4UI/256.

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DDRPHY_COM_REG_0x46

Address: Operational Base(0xFF4F0000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:24	RW	0x80	reg_bg0_invdelaysel_bp The register used to control the tx delay line of the BG0.Each step is 4UI/256.
23:16	RW	0x80	reg_bg1_invdelaysel_bp The register used to control the tx delay line of the BG1.Each step is 4UI/256.
15:8	RW	0x80	reg_cke0_invdelaysel_bp The register used to control the tx delay line of the CKE0.Each step is 4UI/256.
7:0	RW	0x80	reg_cke1_invdelaysel_bp The register used to control the tx delay line of the CKE1.Each step is 4UI/256.

DDRPHY_COM_REG_0x47

Address: Operational Base(0xFF4F0000) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:24	RW	0x80	reg_ckb_invdelaysel_bp The register used to control the tx delay line of the CKB.Each step is 4UI/256.
23:16	RW	0x80	reg_ck_invdelaysel_bp The register used to control the tx delay line of the CK.Each step is 4UI/256.
15:8	RW	0x80	reg_odt0_invdelaysel_bp The register used to control the tx delay line of the ODT0.Each step is 4UI/256.
7:0	RW	0x80	reg_odt1_invdelaysel_bp The register used to control the tx delay line of the ODT1.Each step is 4UI/256.

DDRPHY_COM_REG_0x48

Address: Operational Base(0xFF4F0000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:24	RW	0x80	reg_csb0_invdelaysel_bp The register used to control the tx delay line of the CSB0.Each step is 4UI/256.
23:16	RW	0x80	reg_csb1_invdelaysel_bp The register used to control the tx delay line of the CSB1.Each step is 4UI/256.
15:8	RW	0x80	reg_resetn_invdelaysel_bp The register used to control the tx delay line of the RESETN.Each step is 4UI/256.
7:0	RW	0x80	reg_actn_invdelaysel_bp The register used to control the tx delay line of the ACTN.Each step is 4UI/256.

DDRPHY_COM_REG_0x54

Address: Operational Base(0xFF4F0000) + offset (0x0150)

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Bit	Attr	Reset Value	Description
31:24	RW	0x5a	dq0_train_check_data_value0 For the write training of DDR4, it is the data pattern of the first burst8 which will be written to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the predef read training of DDR4, it is the check pattern used to check the read back data of the first burst8 which will read from the SDRAM through the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of first burst16 which will be written to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the predef read training of LPDDR4, it is the check pattern used to check the read back data of the previous 8 bits of first burst16 which will read from the SDRAM through the A_DQ0/A_DQ8/B_DQ0/B_DQ8.
23:16	RW	0xa5	dq0_train_check_data_value1 For the write training of DDR4, it is the data pattern of the second burst8 which will be written to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the predef read training of DDR4, it is the check pattern used to check the read back data of the second burst8 which will read from the SDRAM through the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the write training of LPDDR4, it is the data pattern of the last 8 bits of first burst16 which will be written to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the predef read training of LPDDR4, it is the check pattern used to check the read back data of the last 8 bits of first burst16 which will read from the SDRAM through the A_DQ0/A_DQ8/B_DQ0/B_DQ8.
15:8	RW	0xc3	dq0_train_check_data_value2 For the write training of DDR4, it is the data pattern of the third burst8 which will be written to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the predef read training of DDR4, it is the check pattern used to check the read back data of the third burst8 which will read from the SDRAM through the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of second burst16 which will be written to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the predef read training of LPDDR4, it is the check pattern used to check the read back data of the previous 8 bits of second burst16 which will read from the SDRAM through the A_DQ0/A_DQ8/B_DQ0/B_DQ8.
7:0	RW	0x3c	dq0_train_check_data_value3 For the write training of DDR4, it is the data pattern of the fourth burst8 which will be written to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the predef read training of DDR4, it is the check pattern used to check the read back data of the fourth burst8 which will read from the SDRAM through the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the write training of LPDDR4, it is the data pattern of the last 8 bits of second burst16 which will be written to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the predef read training of LPDDR4, it is the check pattern used to check the read back data of the last 8 bits of second burst16 which will read from the SDRAM through the A_DQ0/A_DQ8/B_DQ0/B_DQ8.

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DDRPHY_COM_REG_0x55

Address: Operational Base(0xFF4F0000) + offset (0x0154)

Bit	Attr	Reset Value	Description
31:24	RW	0xff	dq0_train_check_data_value4 For the write training of DDR4, it is the data pattern of the fifth burst8 which will be written to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of third burst16 which will be written to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8.
23:16	RW	0x55	dq0_train_check_data_value5 For the write training of DDR4, it is the data pattern of the sixth burst8 which will be written to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the write training of LPDDR4, it is the data pattern of the last 8 bits of third burst16 which will be written to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8.
15:8	RW	0x00	dq0_train_check_data_value6 For the write training of DDR4, it is the data pattern of the seventh burst8 which will be written to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of fourth burst16 which will be written to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8.
7:0	RW	0xaa	dq0_train_check_data_value7 For the write training of DDR4, it is the data pattern of the eighth burst8 which will be written to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the write training of LPDDR4, it is the data pattern of the last 8 bits of fourth burst16 which will be written to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8.

DDRPHY_COM_REG_0x56

Address: Operational Base(0xFF4F0000) + offset (0x0158)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0xf0	dq0_train_check_data_value8 For the write training of DDR4, it is the data pattern of the ninth burst8 which will be written to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of fifth burst16 which will be written to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8.
7:0	RW	0x0f	dq0_train_check_data_value9 For the write training of DDR4, it is the data pattern of the tenth burst8 which will be written to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8. For the write training of LPDDR4, it is the data pattern of the last 8 bits of fifth burst16 which will be written to the SDRAM through to the A_DQ0/A_DQ8/B_DQ0/B_DQ8.

DDRPHY_COM_REG_0x57

Address: Operational Base(0xFF4F0000) + offset (0x015C)

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Bit	Attr	Reset Value	Description
31:24	RW	0xa5	dq1_train_check_data_value0 For the write training of DDR4, it is the data pattern of the first burst8 which will be written to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9. For the predef read training of DDR4, it is the check pattern used to check the read back data of the first burst8 which will read from the SDRAM through the A_DQ1/A_DQ9/B_DQ1/B_DQ9. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of first burst16 which will be written to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9. For the predef read training of LPDDR4, it is the check pattern used to check the read back data of the previous 8 bits of first burst16 which will read from the SDRAM through the A_DQ1/A_DQ9/B_DQ1/B_DQ9.
23:16	RW	0x5a	dq1_train_check_data_value1 For the write training of DDR4, it is the data pattern of the second burst8 which will be written to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9. For the predef read training of DDR4, it is the check pattern used to check the read back data of the second burst8 which will read from the SDRAM through the A_DQ1/A_DQ9/B_DQ1/B_DQ9. For the write training of LPDDR4, it is the data pattern of the last 8 bits of first burst16 which will be written to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9. For the predef read training of LPDDR4, it is the check pattern used to check the read back data of the last 8 bits of first burst16 which will read from the SDRAM through the A_DQ1/A_DQ9/B_DQ1/B_DQ9.
15:8	RW	0x3c	dq1_train_check_data_value2 For the write training of DDR4, it is the data pattern of the third burst8 which will be written to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9. For the predef read training of DDR4, it is the check pattern used to check the read back data of the third burst8 which will read from the SDRAM through the A_DQ1/A_DQ9/B_DQ1/B_DQ9. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of second burst16 which will be written to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9. For the predef read training of LPDDR4, it is the check pattern used to check the read back data of the previous 8 bits of second burst16 which will read from the SDRAM through the A_DQ1/A_DQ9/B_DQ1/B_DQ9.
7:0	RW	0xc3	dq1_train_check_data_value3 For the write training of DDR4, it is the data pattern of the fourth burst8 which will be written to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9. For the predef read training of DDR4, it is the check pattern used to check the read back data of the fourth burst8 which will read from the SDRAM through the A_DQ1/A_DQ9/B_DQ1/B_DQ9. For the write training of LPDDR4, it is the data pattern of the last 8 bits of second burst16 which will be written to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9. For the predef read training of LPDDR4, it is the check pattern used to check the read back data of the last 8 bits of second burst16 which will read from the SDRAM through the A_DQ1/A_DQ9/B_DQ1/B_DQ9.

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DDRPHY_COM_REG_0x58

Address: Operational Base(0xFF4F0000) + offset (0x0160)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	dq1_train_check_data_value4 For the write training of DDR4, it is the data pattern of the fifth burst8 which will be written to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of third burst16 which will be written to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9.
23:16	RW	0xaa	dq1_train_check_data_value5 For the write training of DDR4, it is the data pattern of the sixth burst8 which will be written to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9. For the write training of LPDDR4, it is the data pattern of the last 8 bits of third burst16 which will be written to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9.
15:8	RW	0xff	dq1_train_check_data_value6 For the write training of DDR4, it is the data pattern of the seventh burst8 which will be written to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of fourth burst16 which will be written to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9.
7:0	RW	0x55	dq1_train_check_data_value7 For the write training of DDR4, it is the data pattern of the eighth burst8 which will be written to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9. For the write training of LPDDR4, it is the data pattern of the last 8 bits of fourth burst16 which will be written to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9.

DDRPHY_COM_REG_0x59

Address: Operational Base(0xFF4F0000) + offset (0x0164)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x0f	dq1_train_check_data_value8 For the write training of DDR4, it is the data pattern of the ninth burst8 which will be written to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of fifth burst16 which will be written to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9.
7:0	RW	0xf0	dq1_train_check_data_value9 For the write training of DDR4, it is the data pattern of the tenth burst8 which will be written to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9. For the write training of LPDDR4, it is the data pattern of the last 8 bits of fifth burst16 which will be written to the SDRAM through to the A_DQ1/A_DQ9/B_DQ1/B_DQ9.

DDRPHY_COM_REG_0x5a

Address: Operational Base(0xFF4F0000) + offset (0x0168)

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Bit	Attr	Reset Value	Description
31:24	RW	0x5a	dq2_train_check_data_value0 For the write training of DDR4, it is the data pattern of the first burst8 which will be written to the SDRAM through to the A_DQ2/A_DQ10/B_DQ2/B_DQ10. For the predef read training of DDR4, it is the check pattern used to check the read back data of the first burst8 which will read from the SDRAM through the A_DQ2/A_DQ10/B_DQ2/B_DQ10. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of first burst16 which will be written to the SDRAM through to the A_DQ2/A_DQ10/B_DQ2/B_DQ10. For the predef read training of LPDDR4, it is the check pattern used to check the read back data of the previous 8 bits of first burst16 which will read from the SDRAM through the A_DQ2/A_DQ10/B_DQ2/B_DQ10.
23:16	RW	0xa5	dq2_train_check_data_value1 For the write training of DDR4, it is the data pattern of the second burst8 which will be written to the SDRAM through to the A_DQ2/A_DQ10/B_DQ2/B_DQ10. For the predef read training of DDR4, it is the check pattern used to check the read back data of the second burst8 which will read from the SDRAM through the A_DQ2/A_DQ10/B_DQ2/B_DQ10. For the write training of LPDDR4, it is the data pattern of the last 8 bits of first burst16 which will be written to the SDRAM through to the A_DQ2/A_DQ10/B_DQ2/B_DQ10. For the predef read training of LPDDR4, it is the check pattern used to check the read back data of the last 8 bits of first burst16 which will read from the SDRAM through the A_DQ2/A_DQ10/B_DQ2/B_DQ10.
15:8	RW	0xc3	dq2_train_check_data_value2 For the write training of DDR4, it is the data pattern of the third burst8 which will be written to the SDRAM through to the A_DQ2/A_DQ10/B_DQ2/B_DQ10. For the predef read training of DDR4, it is the check pattern used to check the read back data of the third burst8 which will read from the SDRAM through the A_DQ2/A_DQ10/B_DQ2/B_DQ10. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of second burst16 which will be written to the SDRAM through to the A_DQ2/A_DQ10/B_DQ2/B_DQ10. For the predef read training of LPDDR4, it is the check pattern used to check the read back data of the previous 8 bits of second burst16 which will read from the SDRAM through the A_DQ2/A_DQ10/B_DQ2/B_DQ10.
7:0	RW	0x3c	dq2_train_check_data_value3 For the write training of DDR4, it is the data pattern of the fourth burst8 which will be written to the SDRAM through to the A_DQ2/A_DQ10/B_DQ2/B_DQ10. For the predef read training of DDR4, it is the check pattern used to check the read back data of the fourth burst8 which will read from the SDRAM through the A_DQ2/A_DQ10/B_DQ2/B_DQ10. For the write training of LPDDR4, it is the data pattern of the last 8 bits of second burst16 which will be written to the SDRAM through to the A_DQ2/A_DQ10/B_DQ2/B_DQ10. For the predef read training of LPDDR4, it is the check pattern used to check the read back data of the last 8 bits of second burst16 which will read from the SDRAM through the A_DQ2/A_DQ10/B_DQ2/B_DQ10.

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DDRPHY_COM_REG_0x5b

Address: Operational Base(0xFF4F0000) + offset (0x016C)

Bit	Attr	Reset Value	Description
31:24	RW	0xff	dq2_train_check_data_value4 For the write training of DDR4, it is the data pattern of the fifth burst8 which will be written to the SDRAM through to the A_DQ2/A_DQ10/B_DQ2/B_DQ10. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of third burst16 which will be written to the SDRAM through to the A_DQ2/A_DQ10/B_DQ2/B_DQ10.
23:16	RW	0x55	dq2_train_check_data_value5 For the write training of DDR4, it is the data pattern of the sixth burst8 which will be written to the SDRAM through to the A_DQ2/A_DQ10/B_DQ2/B_DQ10. For the write training of LPDDR4, it is the data pattern of the last 8 bits of third burst16 which will be written to the SDRAM through to the A_DQ2/A_DQ10/B_DQ2/B_DQ10.
15:8	RW	0x00	dq2_train_check_data_value6 For the write training of DDR4, it is the data pattern of the seventh burst8 which will be written to the SDRAM through to the A_DQ2/A_DQ10/B_DQ2/B_DQ10. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of fourth burst16 which will be written to the SDRAM through to the A_DQ2/A_DQ10/B_DQ2/B_DQ10.
7:0	RW	0xaa	dq2_train_check_data_value7 For the write training of DDR4, it is the data pattern of the eighth burst8 which will be written to the SDRAM through to the A_DQ2/A_DQ10/B_DQ2/B_DQ10. For the write training of LPDDR4, it is the data pattern of the last 8 bits of fourth burst16 which will be written to the SDRAM through to the A_DQ2/A_DQ10/B_DQ2/B_DQ10.

DDRPHY_COM_REG_0x5c

Address: Operational Base(0xFF4F0000) + offset (0x0170)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0xf0	dq2_train_check_data_value8 For the write training of DDR4, it is the data pattern of the ninth burst8 which will be written to the SDRAM through to the A_DQ2/A_DQ10/B_DQ2/B_DQ10. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of fifth burst16 which will be written to the SDRAM through to the A_DQ2/A_DQ10/B_DQ2/B_DQ10.
7:0	RW	0x0f	dq2_train_check_data_value9 For the write training of DDR4, it is the data pattern of the tenth burst8 which will be written to the SDRAM through to the A_DQ2/A_DQ10/B_DQ2/B_DQ10. For the write training of LPDDR4, it is the data pattern of the last 8 bits of fifth burst16 which will be written to the SDRAM through to the A_DQ2/A_DQ10/B_DQ2/B_DQ10.

DDRPHY_COM_REG_0x5d

Address: Operational Base(0xFF4F0000) + offset (0x0174)

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Bit	Attr	Reset Value	Description
31:24	RW	0xa5	dq3_train_check_data_value0 For the write training of DDR4, it is the data pattern of the first burst8 which will be written to the SDRAM through to the A_DQ3/A_DQ11/B_DQ3/B_DQ11. For the predef read training of DDR4, it is the check pattern used to check the read back data of the first burst8 which will read from the SDRAM through the A_DQ3/A_DQ11/B_DQ3/B_DQ11. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of first burst16 which will be written to the SDRAM through to the A_DQ3/A_DQ11/B_DQ3/B_DQ11. For the predef read training of LPDDR4, it is the check pattern used to check the read back data of the previous 8 bits of first burst16 which will read from the SDRAM through the A_DQ3/A_DQ11/B_DQ3/B_DQ11.
23:16	RW	0x5a	dq3_train_check_data_value1 For the write training of DDR4, it is the data pattern of the second burst8 which will be written to the SDRAM through to the A_DQ3/A_DQ11/B_DQ3/B_DQ11. For the predef read training of DDR4, it is the check pattern used to check the read back data of the second burst8 which will read from the SDRAM through the A_DQ3/A_DQ11/B_DQ3/B_DQ11. For the write training of LPDDR4, it is the data pattern of the last 8 bits of first burst16 which will be written to the SDRAM through to the A_DQ3/A_DQ11/B_DQ3/B_DQ11. For the predef read training of LPDDR4, it is the check pattern used to check the read back data of the last 8 bits of first burst16 which will read from the SDRAM through the A_DQ3/A_DQ11/B_DQ3/B_DQ11.
15:8	RW	0x3c	dq3_train_check_data_value2 For the write training of DDR4, it is the data pattern of the third burst8 which will be written to the SDRAM through to the A_DQ3/A_DQ11/B_DQ3/B_DQ11. For the predef read training of DDR4, it is the check pattern used to check the read back data of the third burst8 which will read from the SDRAM through the A_DQ3/A_DQ11/B_DQ3/B_DQ11. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of second burst16 which will be written to the SDRAM through to the A_DQ3/A_DQ11/B_DQ3/B_DQ11. For the predef read training of LPDDR4, it is the check pattern used to check the read back data of the previous 8 bits of second burst16 which will read from the SDRAM through the A_DQ3/A_DQ11/B_DQ3/B_DQ11.
7:0	RW	0xc3	dq3_train_check_data_value3 For the write training of DDR4, it is the data pattern of the fourth burst8 which will be written to the SDRAM through to the A_DQ3/A_DQ11/B_DQ3/B_DQ11. For the predef read training of DDR4, it is the check pattern used to check the read back data of the fourth burst8 which will read from the SDRAM through the A_DQ3/A_DQ11/B_DQ3/B_DQ11. For the write training of LPDDR4, it is the data pattern of the last 8 bits of second burst16 which will be written to the SDRAM through to the A_DQ3/A_DQ11/B_DQ3/B_DQ11. For the predef read training of LPDDR4, it is the check pattern used to check the read back data of the last 8 bits of second burst16 which will read from the SDRAM through the A_DQ3/A_DQ11/B_DQ3/B_DQ11.

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DDRPHY_COM_REG_0x5e

Address: Operational Base(0xFF4F0000) + offset (0x0178)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	dq3_train_check_data_value4 For the write training of DDR4, it is the data pattern of the fifth burst8 which will be written to the SDRAM through to the A_DQ3/A_DQ11/B_DQ3/B_DQ11. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of third burst16 which will be written to the SDRAM through to the A_DQ3/A_DQ11/B_DQ3/B_DQ11.
23:16	RW	0xaa	dq3_train_check_data_value5 For the write training of DDR4, it is the data pattern of the sixth burst8 which will be written to the SDRAM through to the A_DQ3/A_DQ11/B_DQ3/B_DQ11. For the write training of LPDDR4, it is the data pattern of the last 8 bits of third burst16 which will be written to the SDRAM through to the A_DQ3/A_DQ11/B_DQ3/B_DQ11.
15:8	RW	0xff	dq3_train_check_data_value6 For the write training of DDR4, it is the data pattern of the seventh burst8 which will be written to the SDRAM through to the A_DQ3/A_DQ11/B_DQ3/B_DQ11. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of fourth burst16 which will be written to the SDRAM through to the A_DQ3/A_DQ11/B_DQ3/B_DQ11.
7:0	RW	0x55	dq3_train_check_data_value7 For the write training of DDR4, it is the data pattern of the eighth burst8 which will be written to the SDRAM through to the A_DQ3/A_DQ11/B_DQ3/B_DQ11. For the write training of LPDDR4, it is the data pattern of the last 8 bits of fourth burst16 which will be written to the SDRAM through to the A_DQ3/A_DQ11/B_DQ3/B_DQ11.

DDRPHY_COM_REG_0x5f

Address: Operational Base(0xFF4F0000) + offset (0x017C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x0f	dq3_train_check_data_value8 For the write training of DDR4, it is the data pattern of the ninth burst8 which will be written to the SDRAM through to the A_DQ3/A_DQ11/B_DQ3/B_DQ11. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of fifth burst16 which will be written to the SDRAM through to the A_DQ3/A_DQ11/B_DQ3/B_DQ11.
7:0	RW	0xf0	dq3_train_check_data_value9 For the write training of DDR4, it is the data pattern of the tenth burst8 which will be written to the SDRAM through to the A_DQ3/A_DQ11/B_DQ3/B_DQ11. For the write training of LPDDR4, it is the data pattern of the last 8 bits of fifth burst16 which will be written to the SDRAM through to the A_DQ3/A_DQ11/B_DQ3/B_DQ11.

DDRPHY_COM_REG_0x60

Address: Operational Base(0xFF4F0000) + offset (0x0180)

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Bit	Attr	Reset Value	Description
31:24	RW	0x5a	dq4_train_check_data_value0 For the write training of DDR4, it is the data pattern of the first burst8 which will be written to the SDRAM through to the A_DQ4/A_DQ12/B_DQ4/B_DQ12. For the predef read training of DDR4, it is the check pattern used to check the read back data of the first burst8 which will read from the SDRAM through the A_DQ4/A_DQ12/B_DQ4/B_DQ12. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of first burst16 which will be written to the SDRAM through to the A_DQ4/A_DQ12/B_DQ4/B_DQ12. For the predef read training of LPDDR4, it is the check pattern used to check the read back data of the previous 8 bits of first burst16 which will read from the SDRAM through the A_DQ4/A_DQ12/B_DQ4/B_DQ12.
23:16	RW	0xa5	dq4_train_check_data_value1 For the write training of DDR4, it is the data pattern of the second burst8 which will be written to the SDRAM through to the A_DQ4/A_DQ12/B_DQ4/B_DQ12. For the predef read training of DDR4, it is the check pattern used to check the read back data of the second burst8 which will read from the SDRAM through the A_DQ4/A_DQ12/B_DQ4/B_DQ12. For the write training of LPDDR4, it is the data pattern of the last 8 bits of first burst16 which will be written to the SDRAM through to the A_DQ4/A_DQ12/B_DQ4/B_DQ12. For the predef read training of LPDDR4, it is the check pattern used to check the read back data of the last 8 bits of first burst16 which will read from the SDRAM through the A_DQ4/A_DQ12/B_DQ4/B_DQ12.
15:8	RW	0xc3	dq4_train_check_data_value2 For the write training of DDR4, it is the data pattern of the third burst8 which will be written to the SDRAM through to the A_DQ4/A_DQ12/B_DQ4/B_DQ12. For the predef read training of DDR4, it is the check pattern used to check the read back data of the third burst8 which will read from the SDRAM through the A_DQ4/A_DQ12/B_DQ4/B_DQ12. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of second burst16 which will be written to the SDRAM through to the A_DQ4/A_DQ12/B_DQ4/B_DQ12. For the predef read training of LPDDR4, it is the check pattern used to check the read back data of the previous 8 bits of second burst16 which will read from the SDRAM through the A_DQ4/A_DQ12/B_DQ4/B_DQ12.
7:0	RW	0x3c	dq4_train_check_data_value3 For the write training of DDR4, it is the data pattern of the fourth burst8 which will be written to the SDRAM through to the A_DQ4/A_DQ12/B_DQ4/B_DQ12. For the predef read training of DDR4, it is the check pattern used to check the read back data of the fourth burst8 which will read from the SDRAM through the A_DQ4/A_DQ12/B_DQ4/B_DQ12. For the write training of LPDDR4, it is the data pattern of the last 8 bits of second burst16 which will be written to the SDRAM through to the A_DQ4/A_DQ12/B_DQ4/B_DQ12. For the predef read training of LPDDR4, it is the check pattern used to check the read back data of the last 8 bits of second burst16 which will read from the SDRAM through the A_DQ4/A_DQ12/B_DQ4/B_DQ12.

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DDRPHY_COM_REG_0x61

Address: Operational Base(0xFF4F0000) + offset (0x0184)

Bit	Attr	Reset Value	Description
31:24	RW	0xff	dq4_train_check_data_value4 For the write training of DDR4, it is the data pattern of the fifth burst8 which will be written to the SDRAM through to the A_DQ4/A_DQ12/B_DQ4/B_DQ12. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of third burst16 which will be written to the SDRAM through to the A_DQ4/A_DQ12/B_DQ4/B_DQ12.
23:16	RW	0x55	dq4_train_check_data_value5 For the write training of DDR4, it is the data pattern of the sixth burst8 which will be written to the SDRAM through to the A_DQ4/A_DQ12/B_DQ4/B_DQ12. For the write training of LPDDR4, it is the data pattern of the last 8 bits of third burst16 which will be written to the SDRAM through to the A_DQ4/A_DQ12/B_DQ4/B_DQ12.
15:8	RW	0x00	dq4_train_check_data_value6 For the write training of DDR4, it is the data pattern of the seventh burst8 which will be written to the SDRAM through to the A_DQ4/A_DQ12/B_DQ4/B_DQ12. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of fourth burst16 which will be written to the SDRAM through to the A_DQ4/A_DQ12/B_DQ4/B_DQ12.
7:0	RW	0xaa	dq4_train_check_data_value7 For the write training of DDR4, it is the data pattern of the eighth burst8 which will be written to the SDRAM through to the A_DQ4/A_DQ12/B_DQ4/B_DQ12. For the write training of LPDDR4, it is the data pattern of the last 8 bits of fourth burst16 which will be written to the SDRAM through to the A_DQ4/A_DQ12/B_DQ4/B_DQ12.

DDRPHY_COM_REG_0x62

Address: Operational Base(0xFF4F0000) + offset (0x0188)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0xf0	dq4_train_check_data_value8 For the write training of DDR4, it is the data pattern of the ninth burst8 which will be written to the SDRAM through to the A_DQ4/A_DQ12/B_DQ4/B_DQ12. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of fifth burst16 which will be written to the SDRAM through to the A_DQ4/A_DQ12/B_DQ4/B_DQ12.
7:0	RW	0x0f	dq4_train_check_data_value9 For the write training of DDR4, it is the data pattern of the tenth burst8 which will be written to the SDRAM through to the A_DQ4/A_DQ12/B_DQ4/B_DQ12. For the write training of LPDDR4, it is the data pattern of the last 8 bits of fifth burst16 which will be written to the SDRAM through to the A_DQ4/A_DQ12/B_DQ4/B_DQ12.

DDRPHY_COM_REG_0x63

Address: Operational Base(0xFF4F0000) + offset (0x018C)

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Bit	Attr	Reset Value	Description
31:24	RW	0xa5	dq5_train_check_data_value0 For the write training of DDR4, it is the data pattern of the first burst8 which will be written to the SDRAM through to the A_DQ5/A_DQ13/B_DQ5/B_DQ13. For the predef read training of DDR4, it is the check pattern used to check the read back data of the first burst8 which will read from the SDRAM through the A_DQ5/A_DQ13/B_DQ5/B_DQ13. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of first burst16 which will be written to the SDRAM through to the A_DQ5/A_DQ13/B_DQ5/B_DQ13. For the predef read training of LPDDR4, it is the check pattern used to check the read back data of the previous 8 bits of first burst16 which will read from the SDRAM through the A_DQ5/A_DQ13/B_DQ5/B_DQ13.
23:16	RW	0x5a	dq5_train_check_data_value1 For the write training of DDR4, it is the data pattern of the second burst8 which will be written to the SDRAM through to the A_DQ5/A_DQ13/B_DQ5/B_DQ13. For the predef read training of DDR4, it is the check pattern used to check the read back data of the second burst8 which will read from the SDRAM through the A_DQ5/A_DQ13/B_DQ5/B_DQ13. For the write training of LPDDR4, it is the data pattern of the last 8 bits of first burst16 which will be written to the SDRAM through to the A_DQ5/A_DQ13/B_DQ5/B_DQ13. For the predef read training of LPDDR4, it is the check pattern used to check the read back data of the last 8 bits of first burst16 which will read from the SDRAM through the A_DQ5/A_DQ13/B_DQ5/B_DQ13.
15:8	RW	0x3c	dq5_train_check_data_value2 For the write training of DDR4, it is the data pattern of the third burst8 which will be written to the SDRAM through to the A_DQ5/A_DQ13/B_DQ5/B_DQ13. For the predef read training of DDR4, it is the check pattern used to check the read back data of the third burst8 which will read from the SDRAM through the A_DQ5/A_DQ13/B_DQ5/B_DQ13. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of second burst16 which will be written to the SDRAM through to the A_DQ5/A_DQ13/B_DQ5/B_DQ13. For the predef read training of LPDDR4, it is the check pattern used to check the read back data of the previous 8 bits of second burst16 which will read from the SDRAM through the A_DQ5/A_DQ13/B_DQ5/B_DQ13.
7:0	RW	0xc3	dq5_train_check_data_value3 For the write training of DDR4, it is the data pattern of the fourth burst8 which will be written to the SDRAM through to the A_DQ5/A_DQ13/B_DQ5/B_DQ13. For the predef read training of DDR4, it is the check pattern used to check the read back data of the fourth burst8 which will read from the SDRAM through the A_DQ5/A_DQ13/B_DQ5/B_DQ13. For the write training of LPDDR4, it is the data pattern of the last 8 bits of second burst16 which will be written to the SDRAM through to the A_DQ5/A_DQ13/B_DQ5/B_DQ13. For the predef read training of LPDDR4, it is the check pattern used to check the read back data of the last 8 bits of second burst16 which will read from the SDRAM through the A_DQ5/A_DQ13/B_DQ5/B_DQ13.

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DDRPHY_COM_REG_0x64

Address: Operational Base(0xFF4F0000) + offset (0x0190)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	dq5_train_check_data_value4 For the write training of DDR4, it is the data pattern of the fifth burst8 which will be written to the SDRAM through to the A_DQ5/A_DQ13/B_DQ5/B_DQ13. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of third burst16 which will be written to the SDRAM through to the A_DQ5/A_DQ13/B_DQ5/B_DQ13.
23:16	RW	0xaa	dq5_train_check_data_value5 For the write training of DDR4, it is the data pattern of the sixth burst8 which will be written to the SDRAM through to the A_DQ5/A_DQ13/B_DQ5/B_DQ13. For the write training of LPDDR4, it is the data pattern of the last 8 bits of third burst16 which will be written to the SDRAM through to the A_DQ5/A_DQ13/B_DQ5/B_DQ13.
15:8	RW	0xff	dq5_train_check_data_value6 For the write training of DDR4, it is the data pattern of the seventh burst8 which will be written to the SDRAM through to the A_DQ5/A_DQ13/B_DQ5/B_DQ13. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of fourth burst16 which will be written to the SDRAM through to the A_DQ5/A_DQ13/B_DQ5/B_DQ13.
7:0	RW	0x55	dq5_train_check_data_value7 For the write training of DDR4, it is the data pattern of the eighth burst8 which will be written to the SDRAM through to the A_DQ5/A_DQ13/B_DQ5/B_DQ13. For the write training of LPDDR4, it is the data pattern of the last 8 bits of fourth burst16 which will be written to the SDRAM through to the A_DQ5/A_DQ13/B_DQ5/B_DQ13.

DDRPHY_COM_REG_0x65

Address: Operational Base(0xFF4F0000) + offset (0x0194)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x0f	dq5_train_check_data_value8 For the write training of DDR4, it is the data pattern of the ninth burst8 which will be written to the SDRAM through to the A_DQ5/A_DQ13/B_DQ5/B_DQ13. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of fifth burst16 which will be written to the SDRAM through to the A_DQ5/A_DQ13/B_DQ5/B_DQ13.
7:0	RW	0xf0	dq5_train_check_data_value9 For the write training of DDR4, it is the data pattern of the tenth burst8 which will be written to the SDRAM through to the A_DQ5/A_DQ13/B_DQ5/B_DQ13. For the write training of LPDDR4, it is the data pattern of the last 8 bits of fifth burst16 which will be written to the SDRAM through to the A_DQ5/A_DQ13/B_DQ5/B_DQ13.

DDRPHY_COM_REG_0x66

Address: Operational Base(0xFF4F0000) + offset (0x0198)

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Bit	Attr	Reset Value	Description
31:24	RW	0x5a	dq6_train_check_data_value0 For the write training of DDR4, it is the data pattern of the first burst8 which will be written to the SDRAM through to the A_DQ6/A_DQ14/B_DQ6/B_DQ14. For the predef read training of DDR4, it is the check pattern used to check the read back data of the first burst8 which will read from the SDRAM through the A_DQ6/A_DQ14/B_DQ6/B_DQ14. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of first burst16 which will be written to the SDRAM through to the A_DQ6/A_DQ14/B_DQ6/B_DQ14. For the predef read training of LPDDR4, it is the check pattern used to check the read back data of the previous 8 bits of first burst16 which will read from the SDRAM through the A_DQ6/A_DQ14/B_DQ6/B_DQ14.
23:16	RW	0xa5	dq6_train_check_data_value1 For the write training of DDR4, it is the data pattern of the second burst8 which will be written to the SDRAM through to the A_DQ6/A_DQ14/B_DQ6/B_DQ14. For the predef read training of DDR4, it is the check pattern used to check the read back data of the second burst8 which will read from the SDRAM through the A_DQ6/A_DQ14/B_DQ6/B_DQ14. For the write training of LPDDR4, it is the data pattern of the last 8 bits of first burst16 which will be written to the SDRAM through to the A_DQ6/A_DQ14/B_DQ6/B_DQ14. For the predef read training of LPDDR4, it is the check pattern used to check the read back data of the last 8 bits of first burst16 which will read from the SDRAM through the A_DQ6/A_DQ14/B_DQ6/B_DQ14.
15:8	RW	0xc3	dq6_train_check_data_value2 For the write training of DDR4, it is the data pattern of the third burst8 which will be written to the SDRAM through to the A_DQ6/A_DQ14/B_DQ6/B_DQ14. For the predef read training of DDR4, it is the check pattern used to check the read back data of the third burst8 which will read from the SDRAM through the A_DQ6/A_DQ14/B_DQ6/B_DQ14. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of second burst16 which will be written to the SDRAM through to the A_DQ6/A_DQ14/B_DQ6/B_DQ14. For the predef read training of LPDDR4, it is the check pattern used to check the read back data of the previous 8 bits of second burst16 which will read from the SDRAM through the A_DQ6/A_DQ14/B_DQ6/B_DQ14.
7:0	RW	0x3c	dq6_train_check_data_value3 For the write training of DDR4, it is the data pattern of the fourth burst8 which will be written to the SDRAM through to the A_DQ6/A_DQ14/B_DQ6/B_DQ14. For the predef read training of DDR4, it is the check pattern used to check the read back data of the fourth burst8 which will read from the SDRAM through the A_DQ6/A_DQ14/B_DQ6/B_DQ14. For the write training of LPDDR4, it is the data pattern of the last 8 bits of second burst16 which will be written to the SDRAM through to the A_DQ6/A_DQ14/B_DQ6/B_DQ14. For the predef read training of LPDDR4, it is the check pattern used to check the read back data of the last 8 bits of second burst16 which will read from the SDRAM through the A_DQ6/A_DQ14/B_DQ6/B_DQ14.

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DDRPHY_COM_REG_0x67

Address: Operational Base(0xFF4F0000) + offset (0x019C)

Bit	Attr	Reset Value	Description
31:24	RW	0xff	dq6_train_check_data_value4 For the write training of DDR4, it is the data pattern of the fifth burst8 which will be written to the SDRAM through to the A_DQ6/A_DQ14/B_DQ6/B_DQ14. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of third burst16 which will be written to the SDRAM through to the A_DQ6/A_DQ14/B_DQ6/B_DQ14.
23:16	RW	0x55	dq6_train_check_data_value5 For the write training of DDR4, it is the data pattern of the sixth burst8 which will be written to the SDRAM through to the A_DQ6/A_DQ14/B_DQ6/B_DQ14. For the write training of LPDDR4, it is the data pattern of the last 8 bits of third burst16 which will be written to the SDRAM through to the A_DQ6/A_DQ14/B_DQ6/B_DQ14.
15:8	RW	0x00	dq6_train_check_data_value6 For the write training of DDR4, it is the data pattern of the seventh burst8 which will be written to the SDRAM through to the A_DQ6/A_DQ14/B_DQ6/B_DQ14. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of fourth burst16 which will be written to the SDRAM through to the A_DQ6/A_DQ14/B_DQ6/B_DQ14.
7:0	RW	0xaa	dq6_train_check_data_value7 For the write training of DDR4, it is the data pattern of the eighth burst8 which will be written to the SDRAM through to the A_DQ6/A_DQ14/B_DQ6/B_DQ14. For the write training of LPDDR4, it is the data pattern of the last 8 bits of fourth burst16 which will be written to the SDRAM through to the A_DQ6/A_DQ14/B_DQ6/B_DQ14.

DDRPHY_COM_REG_0x68

Address: Operational Base(0xFF4F0000) + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0xf0	dq6_train_check_data_value8 For the write training of DDR4, it is the data pattern of the ninth burst8 which will be written to the SDRAM through to the A_DQ6/A_DQ14/B_DQ6/B_DQ14. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of fifth burst16 which will be written to the SDRAM through to the A_DQ6/A_DQ14/B_DQ6/B_DQ14.
7:0	RW	0x0f	dq6_train_check_data_value9 For the write training of DDR4, it is the data pattern of the tenth burst8 which will be written to the SDRAM through to the A_DQ6/A_DQ14/B_DQ6/B_DQ14. For the write training of LPDDR4, it is the data pattern of the last 8 bits of fifth burst16 which will be written to the SDRAM through to the A_DQ6/A_DQ14/B_DQ6/B_DQ14.

DDRPHY_COM_REG_0x69

Address: Operational Base(0xFF4F0000) + offset (0x01A4)

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Bit	Attr	Reset Value	Description
31:24	RW	0xa5	dq7_train_check_data_value0 For the write training of DDR4, it is the data pattern of the first burst8 which will be written to the SDRAM through to the A_DQ7/A_DQ15/B_DQ7/B_DQ15. For the predef read training of DDR4, it is the check pattern used to check the read back data of the first burst8 which will read from the SDRAM through the A_DQ7/A_DQ15/B_DQ7/B_DQ15. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of first burst16 which will be written to the SDRAM through to the A_DQ7/A_DQ15/B_DQ7/B_DQ15. For the predef read training of LPDDR4, it is the check pattern used to check the read back data of the previous 8 bits of first burst16 which will read from the SDRAM through the A_DQ7/A_DQ15/B_DQ7/B_DQ15.
23:16	RW	0x5a	dq7_train_check_data_value1 For the write training of DDR4, it is the data pattern of the second burst8 which will be written to the SDRAM through to the A_DQ7/A_DQ15/B_DQ7/B_DQ15. For the predef read training of DDR4, it is the check pattern used to check the read back data of the second burst8 which will read from the SDRAM through the A_DQ7/A_DQ15/B_DQ7/B_DQ15. For the write training of LPDDR4, it is the data pattern of the last 8 bits of first burst16 which will be written to the SDRAM through to the A_DQ7/A_DQ15/B_DQ7/B_DQ15. For the predef read training of LPDDR4, it is the check pattern used to check the read back data of the last 8 bits of first burst16 which will read from the SDRAM through the A_DQ7/A_DQ15/B_DQ7/B_DQ15.
15:8	RW	0x3c	dq7_train_check_data_value2 For the write training of DDR4, it is the data pattern of the third burst8 which will be written to the SDRAM through to the A_DQ7/A_DQ15/B_DQ7/B_DQ15. For the predef read training of DDR4, it is the check pattern used to check the read back data of the third burst8 which will read from the SDRAM through the A_DQ7/A_DQ15/B_DQ7/B_DQ15. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of second burst16 which will be written to the SDRAM through to the A_DQ7/A_DQ15/B_DQ7/B_DQ15. For the predef read training of LPDDR4, it is the check pattern used to check the read back data of the previous 8 bits of second burst16 which will read from the SDRAM through the A_DQ7/A_DQ15/B_DQ7/B_DQ15.
7:0	RW	0xc3	dq7_train_check_data_value3 For the write training of DDR4, it is the data pattern of the fourth burst8 which will be written to the SDRAM through to the A_DQ7/A_DQ15/B_DQ7/B_DQ15. For the predef read training of DDR4, it is the check pattern used to check the read back data of the fourth burst8 which will read from the SDRAM through the A_DQ7/A_DQ15/B_DQ7/B_DQ15. For the write training of LPDDR4, it is the data pattern of the last 8 bits of second burst16 which will be written to the SDRAM through to the A_DQ7/A_DQ15/B_DQ7/B_DQ15. For the predef read training of LPDDR4, it is the check pattern used to check the read back data of the last 8 bits of second burst16 which will read from the SDRAM through the A_DQ7/A_DQ15/B_DQ7/B_DQ15.

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DDRPHY_COM_REG_0x6a

Address: Operational Base(0xFF4F0000) + offset (0x01A8)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	dq7_train_check_data_value4 For the write training of DDR4, it is the data pattern of the fifth burst8 which will be written to the SDRAM through to the A_DQ7/A_DQ15/B_DQ7/B_DQ15. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of third burst16 which will be written to the SDRAM through to the A_DQ7/A_DQ15/B_DQ7/B_DQ15.
23:16	RW	0xaa	dq7_train_check_data_value5 For the write training of DDR4, it is the data pattern of the sixth burst8 which will be written to the SDRAM through to the A_DQ7/A_DQ15/B_DQ7/B_DQ15. For the write training of LPDDR4, it is the data pattern of the last 8 bits of third burst16 which will be written to the SDRAM through to the A_DQ7/A_DQ15/B_DQ7/B_DQ15.
15:8	RW	0xff	dq7_train_check_data_value6 For the write training of DDR4, it is the data pattern of the seventh burst8 which will be written to the SDRAM through to the A_DQ7/A_DQ15/B_DQ7/B_DQ15. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of fourth burst16 which will be written to the SDRAM through to the A_DQ7/A_DQ15/B_DQ7/B_DQ15.
7:0	RW	0x55	dq7_train_check_data_value7 For the write training of DDR4, it is the data pattern of the eighth burst8 which will be written to the SDRAM through to the A_DQ7/A_DQ15/B_DQ7/B_DQ15. For the write training of LPDDR4, it is the data pattern of the last 8 bits of fourth burst16 which will be written to the SDRAM through to the A_DQ7/A_DQ15/B_DQ7/B_DQ15.

DDRPHY_COM_REG_0x6b

Address: Operational Base(0xFF4F0000) + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19	RW	0x0	reg_wrtrain_odt_advance the register is used in write train,let the odt open advance when do write operation ,you can keep the default
18:16	RW	0x1	reg_wrtrain_odt_keep the register is used in write train,let the odt open keep when do wirte operation, you can keep the default
15:8	RW	0x0f	dq7_train_check_data_value8 For the write training of DDR4, it is the data pattern of the ninth burst8 which will be written to the SDRAM through to the A_DQ7/A_DQ15/B_DQ7/B_DQ15. For the write training of LPDDR4, it is the data pattern of the previous 8 bits of fifth burst16 which will be written to the SDRAM through to the A_DQ7/A_DQ15/B_DQ7/B_DQ15.
7:0	RW	0xf0	dq7_train_check_data_value9 For the write training of DDR4, it is the data pattern of the tenth burst8 which will be written to the SDRAM through to the A_DQ7/A_DQ15/B_DQ7/B_DQ15. For the write training of LPDDR4, it is the data pattern of the last 8 bits of fifth burst16 which will be written to the SDRAM through to the A_DQ7/A_DQ15/B_DQ7/B_DQ15.

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DDRPHY_COM_REG_0x6c

Address: Operational Base(0xFF4F0000) + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:24	RW	0x14	reg_wrtrain_vref_wait_vref_cnt_50ns the register is used in write train, if you enable tx vref scan function, you need to configure this register.When set a new tx vref value to sdram , we should wait 100-250ns ,then it works, you should set this register tell PHY how long is 50ns,then the phy have a reference.So the reg's value = 50ns/dfi_1xclk
23:21	RW	0x1	reg_train_vref_step_min the register is used in read predef train or write train, if you enable vref scan function, you can configure this register.this register means How many step at a time, when doing A fine vref scanning.
20:16	RW	0x08	reg_train_vref_step_max the register is used in read predef train or write train, if you enable vref scan function, you can configure this register.this register means How many step at a time, when doing A rough vref scanning.
15:10	RW	0x14	reg_cmd_invdelaysel_sel The ca train command tx delay line value obs signal. The user can use this register to get the ca train result of each command pad.the result can be read from reg_cmd_invdelaysel. 0: channel A ca0 rank0 1: channel A ca1 rank0 ....(ca2-ca4) channel A rank0 5: channel A ca5 rank0 6: channel B ca0 rank0 ....(ca1-ca4) channel B rank0 11: channel B ca5 rank0 12: channel A ca0 rank1 ....(ca1-ca4) channel A rank1 17: channel A ca5 rank1 18: channel B ca0 rank1 ...(ca1-ca4) channel B rank1 23: channel B ca5 rank1 24: channel A ck 25: channel A ckb 26: channel A cke0 27: channel A cke1 28: channel A csb0 29: channel A csb1 30: channel A odt0 31: channel A odt1 32: channel B ck 33: channel B ckb 34: channel B cke0 35: channel B cke1 36: channel B csb0 37: channel B csb1 38: channel B odt0 39: channel B odt1

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Bit	Attr	Reset Value	Description
9:0	RW	0x140	reg_rdtrain_wait_vref_valid_cnt the register is used in read predef train, if you enable rx vref scan function, you need to configure this register. When set a new rx vref value ,we should wait 800ns ,then it works.So the reg's value = 800ns/dfi_1xclk

DDRPHY_COM_REG_0x6e

Address: Operational Base(0xFF4F0000) + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x3f	reg_rd_train_dq_scan_max control the scan range of dq's rd training, set the dq's max scan value.

DDRPHY_COM_REG_0x6f

Address: Operational Base(0xFF4F0000) + offset (0x01BC)

Bit	Attr	Reset Value	Description
31:24	RW	0x5a	dm_train_check_data_value0 For the write training of DDR4,it is the dm pattern of the first burst8 For the write training of LPDDR4,it is the dm pattern of the previous 8 bits of first burst16
23:16	RW	0xa5	dm_train_check_data_value1 For the write training of DDR4,it is the dm pattern of the second burst8 For the write training of LPDDR4,it is the dm pattern of the last 8 bits of first burst16
15:8	RW	0xc3	dm_train_check_data_value2 For the write training of DDR4,it is the dm pattern of the third burst8 For the write training of LPDDR4,it is the dm pattern of the previous 8 bits of second burst16
7:0	RW	0x3c	dm_train_check_data_value3 For the write training of DDR4,it is the dm pattern of the fourth burst8 For the write training of LPDDR4,it is the dm pattern of the last 8 bits of second burst16

DDRPHY_COM_REG_0x70

Address: Operational Base(0xFF4F0000) + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:24	RW	0xff	dm_train_check_data_value4 For the write training of DDR4,it is the dm pattern of the fifth burst8 For the write training of LPDDR4,it is the dm pattern of the previous 8 bits of third burst16
23:16	RW	0x55	dm_train_check_data_value5 For the write training of DDR4,it is the dm pattern of the sixth burst8 For the write training of LPDDR4,it is the dm pattern of the last 8 bits of third burst16

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	dm_train_check_data_value6 For the write training of DDR4,it is the dm pattern of the seventh burst8 For the write training of LPDDR4,it is the dm pattern of the previous 8 bits of fourth burst16
7:0	RW	0xaa	dm_train_check_data_value7 For the write training of DDR4,it is the dm pattern of the eighth burst8 For the write training of LPDDR4,it is the dm pattern of the last 8 bits of fourth burst16

DDRPHY_COM_REG_0x71

Address: Operational Base(0xFF4F0000) + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:20	RW	0x00	reg_wrtrain_vref_scan_min control the scan range of wr vref training, set the wr train vref's min scan value
19:16	RO	0x0	reserved
15:8	RW	0xf0	dm_train_check_data_value8 For the write training of DDR4,it is the dm pattern of the ninth burst8 For the write training of LPDDR4,it is the dm pattern of the previous 8 bits of fifth burst16
7:0	RW	0x0f	dm_train_check_data_value9 For the write training of DDR4,it is the dm pattern of the tenth burst8 For the write training of LPDDR4,it is the dm pattern of the last 8 bits of fifth burst16

DDRPHY_COM_REG_0x7c

Address: Operational Base(0xFF4F0000) + offset (0x01F0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	train_all_step_done The complete signal of the write training/rd perdef training . Active high. The user need to wait this bit change to high after enable the write training. (reuse for rd perdef training and wr training)
6	RO	0x0	train_step1_delay_done The compelte signal of the delay scan before the vref scan when write training/rd perdef training. Active high.(reuse for rd perdef training and wr training)
5	RO	0x0	train_step2_vref_done The compelte signal of the vref scan when write training/rd perdef training. Active high. (reuse for rd perdef training and wr training)
4	RO	0x0	train_step3_delay_done The compelte signal of the delay scan after the vref scan when write training/rd perdef training. Active high. (reuse for rd perdef training and wr training)

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Bit	Attr	Reset Value	Description
3	RO	0x0	train_step1_error when train done ,you need to check this register.this reg's value equal to 1'b1 means step1 have error in rd perdef training or write training.(reuse for rd perdef training and wr training) . The step of training can refer to read train and write train section.
2	RO	0x0	train_step2_error when train done ,you need to check this register.this reg's value equal to 1'b1 means step2 have error in rd perdef training or write training.(reuse for rd perdef training and wr training)
1	RO	0x0	train_step3_error when train done ,you need to check this register.this reg's value equal to 1'b1 means step3 have error in rd perdef training or write training.(reuse for rd perdef training and wr training)
0	RO	0x0	train_true_done The complete signal of the read training(mpr/mpc mode). Active high.

DDRPHY_COM_REG_0x7d

Address: Operational Base(0xFF4F0000) + offset (0x01F4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	halfui_lock_code_to_reg dll lock value
23	RO	0x0	reserved
22	RO	0x0	pvt_comp_req_wait_time_out_to_reg if this register is 1, the time is out, when wait pvt ack. not used in this project.
21:15	RO	0x00	pvt_comp_cs_to_reg pvt state machine observation signal
14	RO	0x0	mdll_timeout_to_reg if this register is 1, the time is out, when wait dll lock. not used in this project.
13:7	RO	0x00	mdll_update_cnt observation signal
6	RO	0x0	reserved
5	RO	0x0	dll_lock_to_reg the dll lock flag
4	RO	0x0	user_load_mode_busy if this register is 1, can not configure load mode
3	RO	0x0	pwrok_reg_po not used
2	RO	0x0	pwrokcore not used
1	RO	0x0	lock_mpll not used
0	RO	0x0	lock_pll_dqcmd The lock signal of the pll. Active high. The pll will be locked in 5000 reference clock cycles after the pd operation.

DDRPHY_COM_REG_0x7e

Address: Operational Base(0xFF4F0000) + offset (0x01F8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28:24	RO	0x00	drvlegpd_zqcali_2reg[4:0] The zqclibration result of driver pull down after the zqcalib training.
23:21	RO	0x0	reserved
20:16	RO	0x00	drvlegpu_zqcali_2reg[4:0] The zqclibration result of driver pull up after the zqcalib training.
15:13	RO	0x0	reserved
12:8	RO	0x00	odtlegpd_zqcali_2reg[4:0] The zqclibration result of odt pull down after the zqcalib training.
7:5	RO	0x0	reserved
4:0	RO	0x00	odtlegpu_zqcali_2reg[4:0] The zqclibration result of odt pull up after the zqcalib training.

DDRPHY_COM_REG_0x7f

Address: Operational Base(0xFF4F0000) + offset (0x01FC)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:8	RO	0x000	reg_x1clk_ndiv_cnt[10:0] used to observe the delay capability of invdealysel
7:5	RO	0x0	reserved
4	RO	0x0	reg_zqcali_done The complete signal of the zacalib training. Active high.
3	RO	0x0	reg_drvpd_overflow The fail flag of driver pull down zacalib trraining. Active high.
2	RO	0x0	reg_drvpu_overflow The fail flag of driver pull up zacalib trraining. Active high.
1	RO	0x0	reg_odtpd_overflow The fail flag of odt pull down zacalib trraining. Active high.
0	RO	0x0	reg_odtpu_overflow The fail flag of odt pull up zacalib trraining. Active high.

DDRPHY_COM_REG_0x80

Address: Operational Base(0xFF4F0000) + offset (0x0200)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RO	0x0	bist_error_dm[3:0] The dm error flag of each pad when phy bist. [0]: A_DM0. [1]: A_DM1. [2]: B_DM0. [3]: B_DM1.
7:4	RO	0x0	reserved
3	RO	0x0	cmd_error_flag The error flag of CMD PADs for PHY bist. Active High. If the bist_complete and dm_error_flag are high at the same time, it means that errors occur on the CMD pads when phy bist. The user can read the register 0x80/0x81/0x82/0x83 to find which pad has error.
2	RO	0x0	dm_error_flag The error flag of DM PADs for phy bist. Active High. If the bist_compelte and dm_error_flag are high at the same time, it means that errors occur on the DM pads when phy bist. The user can read the register 0x84 to find which pad has error.

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Bit	Attr	Reset Value	Description
1	RO	0x0	dq_error_flag The error flag of DQ PADs for phy bist. Active High. If the bist_compelte and dq_error_flag are high at the same time, it means that errors occur on the DQ pads when phy bist. The user can read the register 0x85/0x86/0x87/0x88 to find which pad has error.
0	RO	0x0	bist_complete bist complete signal

DDRPHY_COM_REG_0x81

Address: Operational Base(0xFF4F0000) + offset (0x0204)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bist_error_dq[31:0] The byte 0 error flag of each pad when phy bist. Active high. [0]: A_D00. [1]: A_DQ1. [2]: A_DQ2. [3]: A_DQ3. [4]: A_DQ4. [5]: A_DQ5. [6]: A_DQ6. [7]: A_DQ7. The byte 1 error flag of each pad when phy bist. [0]: A_D08. [1]: A_DQ9. [2]: A_DQ10. [3]: A_DQ11. [4]: A_DQ12. [5]: A_DQ13. [6]: A_DQ14. [7]: A_DQ15. The byte 2 error flag of each pad when phy bist. [0]: B_D00. [1]: B_DQ1. [2]: B_DQ2. [3]: B_DQ3. [4]: B_DQ4. [5]: B_DQ5. [6]: B_DQ6. [7]: B_DQ7. The byte 3 error flag of each pad when phy bist. [0]: B_D08. [1]: B_DQ9. [2]: B_DQ10. [3]: B_DQ11. [4]: B_DQ12. [5]: B_DQ13. [6]: B_DQ14. [7]: B_DQ15.

DDRPHY_COM_REG_0x82

Address: Operational Base(0xFF4F0000) + offset (0x0208)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:0	RO	0x00000000	bist_error_cmd[29:0] The error flag of command pad when phy bist. [0]: A0. [1]: A1. [2]: A2. [3]: A3. [4]: A4. [5]: A5. [6]: A6. [7]: A7. [8]: A8. [9]: A9. [10]: A10. [11]: A11. [12]: A12. [13]: A13. [14]: A14. [15]: A15. [16]: A16. [17]: A17. [18]: BA0. [19]: BA1. [20]: BG0. [21]: BG1. [22]: ACTN. [23]: CKE0. [24]: ODT0. [25]: RESETN. [26]: ODT1. [27]: CSB1. [28]: CKE1

DDRPHY_COM_REG_0x83

Address: Operational Base(0xFF4F0000) + offset (0x020C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RO	0x0	wl_done_byte[3:0] The write leveling complete signal of each channel. Active high. [0]: The write leveling complete of byte0. [1]: The write leveling complete of byte1. [2]: The write leveling complete of byte2. [3]: The write leveling compelte of byte3. [4]: The write leveling compelte of byte4.
7	RO	0x0	reserved
6	RO	0x0	calib_end The rx dqs calib complete signal. Active high. Only change to 1'b1 when all open channel have compelte the rx dqs calibration.
5	RO	0x0	calib_error The error flag of the rx dqs calib. Active high.
4	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
3:0	RO	0x0	calib_done_byte[3:0] The rx dqs calib complete signal of each channel. Active high. [0]: The rx dqs calib complete of byte0. [1]: The rx dqs calib complete of byte1. [2]: The rx dqs calib complete of byte2. [3]: The rx dqs calib compelte of byte3. [4]: The rx dqs calib compelte of byte4.

DDRPHY_COM_REG_0x84

Address: Operational Base(0xFF4F0000) + offset (0x0210)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RO	0x0	cha_rank_cat_bp_cmd_send_rdy[3:0] [0]:The reay signal of the command bus training bypass mode of channel b RANK0. Active high. After the user enable the command bus training bypass mode, you need to wait this bit change to high. When this bit change to to high, it means the sdram has already go into the command bus training mode. Then the user can use the register to send the CBT command to do the command bus training mode. [1]:The reay signal of the command bus training bypass mode of channel a RANK1. Active high. After the user enable the command bus training bypass mode, you need to wait this bit change to high. When this bit change to to high, it means the sdram has already go into the command bus training mode. Then the user can use the register to send the CBT command to do the command bus training mode.
23:20	RO	0x0	chb_rank_cat_bp_cmd_send_rdy[3:0] [0]:The reay signal of the command bus training bypass mode of channel b RANK0. Active high. After the user enable the command bus training bypass mode, you need to wait this bit change to high. When this bit change to to high, it means the sdram has already go into the command bus training mode. Then the user can use the register to send the CBT command to do the command bus training mode. [1]:The reay signal of the command bus training bypass mode of channel a RANK0. Active high. After the user enable the command bus training bypass mode, you need to wait this bit change to high. When this bit change to to high, it means the sdram has already go into the command bus training mode. Then the user can use the register to send the CBT command to do the command bus training mode.

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Bit	Attr	Reset Value	Description
19:16	RO	0x0	cha_rank_cat_bp_done[3:0] [0]:The command bus training bypass mode compelte signal of channel b RANK1. Actve high. After the user enable the command bus training bypass mode and use the register to compelte the command bus training, the user can stop the bypass mode by set the reg_cat_bp_start to low, then the phy will exit the command bus train mode and set to this bit to 1. Then the user can set the reg_cat_bp_en to exit the command bust train mode. [1]:The command bus training bypass mode compelte signal of channel a RANK1. Actve high. After the user enable the command bus training bypass mode and use the register to compelte the command bus training, the user can stop the bypass mode by set the reg_cat_bp_start to low, then the phy will exit the command bus train mode and set to this bit to 1. Then the user can set the reg_cat_bp_en to exit the command bust train mode.
15:12	RO	0x0	chb_rank_cat_bp_done[3:0] [0]:The command bus training bypass mode compelte signal of channel b RANK0. Actve high. After the user enable the command bus training bypass mode and use the register to compelte the command bus training, the user can stop the bypass mode by set the reg_cat_bp_start to low, then the phy will exit the command bus train mode and set to this bit to 1. Then the user can set the reg_cat_bp_en to exit the command bust train mode. [1]:The command bus training bypass mode compelte signal of channel a RANK0. Actve high. After the user enable the command bus training bypass mode and use the register to compelte the command bus training, the user can stop the bypass mode by set the reg_cat_bp_start to low, then the phy will exit the command bus train mode and set to this bit to 1. Then the user can set the reg_cat_bp_en to exit the command bust train mode.
11:0	RO	0x000	ca_check_value[11:0] [5:0]:The command bus train read back data from the dq[5:0] of channel a when enable the command bus train bypass mode. When enable the command bus train bypass mode and go into the comand bus train mode, if the phy send the CBT command, the dq will read back the data on the command bus through, the read back data will be stored in this register. The user can use this register to get the read back data and judge the curren tx delay line is right or not. [6:11]:The command bus train read back data from the dq[5:0] of channel b when enable the command bus train bypass mode. When enable the command bus train bypass mode and go into the comand bus train mode, if the phy send the CBT command, the dq will read back the data on the command bus through, the read back data will be stored in this register. The user can use this register to get the read back data and judge the curren tx delay line is right or not.

DDRPHY_COM_REG_0x85

Address: Operational Base(0xFF4F0000) + offset (0x0214)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:18	RO	0x000	cha_cat_auto_cs_train_err[9:0] The auto command bus cs train error flag of channel a. [0]: The training result of csb for rank0 is abnormal if enable the cs train. [1]: The training result of csb for rank1 is abnormal if enable the cs train. [2]: Can't find the vref pass window of channel a csb for rank0 if enable the cs train. [3]: Can't find the vref pass window of channel a csb for rank1 if enable the cs train. [4]: Can't find the tx delay line pass window of channel a csb for rank0 if enable the cs train. [5]: Can't find the tx delay line pass window of channel a csb for rank1 if enable the cs train. [6]: The start point of the channel a CSB0 training is abnormal if enable the cs train. The training will be fail. [7]: The start point of the channel a CSB1 training is abnormal if enable the cs train. The training will be fail.
17:8	RO	0x000	chb_cat_auto_cs_train_err[9:0] The auto command bus cs train error flag of channel b. [0]: The training result of csb for rank0 is abnormal if enable the cs train. [1]: The training result of csb for rank1 is abnormal if enable the cs train. [2]: Can't find the vref pass window of channel b csb for rank0 if enable the cs train. [3]: Can't find the vref pass window of channel b csb for rank1 if enable the cs train. [4]: Can't find the tx delay line pass window of channel b csb for rank0 if enable the cs train. [5]: Can't find the tx delay line pass window of channel b csb for rank1 if enable the cs train. [6]: The start point of the channel b CSB0 training is abnormal if enable the cs train. The training will be fail. [7]: The start point of the channel b CSB1 training is abnormal if enable the cs train. The training will be fail.
7:5	RO	0x0	reserved
4	RO	0x0	cat_low_freq_sel
3	RO	0x0	cha_cat_done The auto command bus train complete signal of channel a. Active high.
2	RO	0x0	chb_cat_done The auto command bus train complete signal of channel b. Active high.
1	RO	0x0	cha_cat_bp_cmd_send_done The flag of channel b that the phy compelte to send the CBT command when enable the command bus training bypass mode. Active high. The user needs to wait this bit change to 1'b1 when it prepares to send the next CBT command.
0	RO	0x0	chb_cat_bp_cmd_send_done The flag of channel a that the phy compelte to send the CBT command when enable the command bus training bypass mode. Active high. The user needs to wait this bit change to 1'b1 when it prepares to send the next CBT command.

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DDRPHY_COM_REG_0x86

Address: Operational Base(0xFF4F0000) + offset (0x0218)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	reg_dfx_pvt_cmp_read_back_data[31:0]

DDRPHY_COM_REG_0x87

Address: Operational Base(0xFF4F0000) + offset (0x021C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RO	0x0	rtrain_cnt_to_reg[3:0]
3:0	RO	0x0	pvt_compensation_cnt_to_reg[3:0]

DDRPHY_COM_REG_0x8c

Address: Operational Base(0xFF4F0000) + offset (0x0230)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	reg_cmd_invdelaysel[7:0] The ca train tx delay line value obs signal. The user can use this register to get the current control value of each command pad. the command pad sel register is reg_cmd_invdelaysel_sel
15	RO	0x0	reserved
14:8	RO	0x00	reg_wrtrain_vref_max_value[6:0] The max pass point of the tx SDRAM's DQ vref for dq .
7	RO	0x0	reserved
6:0	RO	0x00	reg_wrtrain_vref_min_value[6:0] The max pass point of the tx SDRAM's DQ vref for dq .

DDRPHY_COM_REG_0x8d

Address: Operational Base(0xFF4F0000) + offset (0x0234)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	cha_rank0_ca0_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank0 channel A ca0.
23:16	RO	0x00	cha_rank0_ca1_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank0 channel A ca1.
15:8	RO	0x00	cha_rank0_ca2_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank0 channel A ca2.
7:0	RO	0x00	cha_rank0_ca3_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank0 channel A ca3.

DDRPHY_COM_REG_0x8e

Address: Operational Base(0xFF4F0000) + offset (0x0238)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	cha_rank0_ca4_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank0 channel A ca4.
23:16	RO	0x00	cha_rank0_ca5_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank0 channel A ca5.
15:8	RO	0x00	cha_rank1_ca0_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank1 channel A ca0.
7:0	RO	0x00	cha_rank1_ca1_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank1 channel A ca1.

DDRPHY_COM_REG_0x8f

Address: Operational Base(0xFF4F0000) + offset (0x023C)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	cha_rank1_ca2_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank1 channel A ca2.
23:16	RO	0x00	cha_rank1_ca3_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank1 channel A ca3.
15:8	RO	0x00	cha_rank1_ca4_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank1 channel A ca4.
7:0	RO	0x00	cha_rank1_ca5_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank1 channel A ca5.

DDRPHY_COM_REG_0x90

Address: Operational Base(0xFF4F0000) + offset (0x0240)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	cha_rank0_min_cs_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank0 channel A cs .
23:16	RO	0x00	cha_rank1_min_cs_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank1 channel A cs.
15:8	RO	0x00	cha_rank0_max_cs_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank0 channel A cs .
7:0	RO	0x00	cha_rank1_max_cs_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank1 channel A cs.

DDRPHY_COM_REG_0x91

Address: Operational Base(0xFF4F0000) + offset (0x0244)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	cha_rank0_ca0_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank0 channel A ca0.
23:16	RO	0x00	cha_rank0_ca1_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank0 channel A ca1.
15:8	RO	0x00	cha_rank0_ca2_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank0 channel A ca2.
7:0	RO	0x00	cha_rank0_ca3_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank0 channel A ca3.

DDRPHY_COM_REG_0x92

Address: Operational Base(0xFF4F0000) + offset (0x0248)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	cha_rank0_ca4_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank0 channel A ca4.
23:16	RO	0x00	cha_rank0_ca5_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank0 channel A ca5.
15:8	RO	0x00	cha_rank1_ca0_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank1 channel A ca0.
7:0	RO	0x00	cha_rank1_ca1_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank1 channel A ca1.

DDRPHY_COM_REG_0x93

Address: Operational Base(0xFF4F0000) + offset (0x024C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	cha_rank1_ca2_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank1 channel A ca2.
23:16	RO	0x00	cha_rank1_ca3_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank1 channel A ca3.
15:8	RO	0x00	cha_rank1_ca4_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank1 channel A ca4.

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Bit	Attr	Reset Value	Description
7:0	RO	0x00	cha_rank1_ca5_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank1 channel A ca5.

DDRPHY_COM_REG_0x94

Address: Operational Base(0xFF4F0000) + offset (0x0250)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	chb_rank0_ca0_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank0 channel B ca0.
23:16	RO	0x00	chb_rank0_ca1_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank0 channel B ca1.
15:8	RO	0x00	chb_rank0_ca2_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank0 channel B ca2.
7:0	RO	0x00	chb_rank0_ca3_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank0 channel B ca3.

DDRPHY_COM_REG_0x95

Address: Operational Base(0xFF4F0000) + offset (0x0254)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	chb_rank0_ca4_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank0 channel B ca4.
23:16	RO	0x00	chb_rank0_ca5_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank0 channel B ca5.
15:8	RO	0x00	chb_rank1_ca0_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank1 channel B ca0.
7:0	RO	0x00	chb_rank1_ca1_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank1 channel B ca1.

DDRPHY_COM_REG_0x96

Address: Operational Base(0xFF4F0000) + offset (0x0258)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	chb_rank1_ca2_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank1 channel B ca2.
23:16	RO	0x00	chb_rank1_ca3_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank1 channel B ca3.
15:8	RO	0x00	chb_rank1_ca4_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank1 channel B ca4.
7:0	RO	0x00	chb_rank1_ca5_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank1 channel B ca5.

DDRPHY_COM_REG_0x97

Address: Operational Base(0xFF4F0000) + offset (0x025C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	chb_rank0_min_cs_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank0 channel B cs .
23:16	RO	0x00	chb_rank1_min_cs_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank1 channel B cs.
15:8	RO	0x00	chb_rank0_max_cs_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank0 channel B cs .
7:0	RO	0x00	chb_rank1_max_cs_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank1 channel B cs.

DDRPHY_COM_REG_0x98

Address: Operational Base(0xFF4F0000) + offset (0x0260)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	chb_rank0_ca0_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank0 channel B ca0.
23:16	RO	0x00	chb_rank0_ca1_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank0 channel B ca1.
15:8	RO	0x00	chb_rank0_ca2_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank0 channel B ca2.
7:0	RO	0x00	chb_rank0_ca3_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank0 channel B ca3.

DDRPHY_COM_REG_0x99

Address: Operational Base(0xFF4F0000) + offset (0x0264)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	chb_rank0_ca4_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank0 channel B ca4.
23:16	RO	0x00	chb_rank0_ca5_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank0 channel B ca5.
15:8	RO	0x00	chb_rank1_ca0_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank1 channel B ca0.
7:0	RO	0x00	chb_rank1_ca1_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank1 channel B ca1.

DDRPHY_COM_REG_0x9a

Address: Operational Base(0xFF4F0000) + offset (0x0268)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	chb_rank1_ca2_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank1 channel B ca2.
23:16	RO	0x00	chb_rank1_ca3_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank1 channel B ca3.
15:8	RO	0x00	chb_rank1_ca4_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank1 channel B ca4.
7:0	RO	0x00	chb_rank1_ca5_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank1 channel B ca5.

DDRPHY_COM_REG_0x9b

Address: Operational Base(0xFF4F0000) + offset (0x026C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RO	0x00	cha_rank0_min_cs_vref_pass[5:0] The min pass point of the tx SDRAM's vref for rank0 channel A cs .
23:22	RO	0x0	reserved
21:16	RO	0x00	cha_rank0_max_cs_vref_pass[5:0] The max pass point of the tx delay line for rank0 channel A cs .
15:14	RO	0x0	reserved
13:8	RO	0x00	cha_rank1_min_cs_vref_pass[5:0] The min pass point of the tx SDRAM's vref for rank1 channel A cs .
7:6	RO	0x0	reserved
5:0	RO	0x00	cha_rank1_max_cs_vref_pass[5:0] The max pass point of the tx delay line for rank1 channel A cs.

DDRPHY_COM_REG_0x9c

Address: Operational Base(0xFF4F0000) + offset (0x0270)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:24	RO	0x00	chb_rank0_min_cs_vref_pass[5:0] The min pass point of the tx SDRAM's vref for rank0 channel B cs .
23:22	RO	0x0	reserved
21:16	RO	0x00	chb_rank0_max_cs_vref_pass[5:0] The max pass point of the tx delay line for rank0 channel B cs .
15:14	RO	0x0	reserved
13:8	RO	0x00	chb_rank1_min_cs_vref_pass[5:0] The min pass point of the tx SDRAM's vref for rank1 channel B cs .
7:6	RO	0x0	reserved
5:0	RO	0x00	chb_rank1_max_cs_vref_pass[5:0] The max pass point of the tx delay line for rank1 channel B cs.

DDRPHY_COM_REG_0x9d

Address: Operational Base(0xFF4F0000) + offset (0x0274)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	cha_rank2_ca0_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank2 channel A ca0.
23:16	RO	0x00	cha_rank2_ca1_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank2 channel A ca1.
15:8	RO	0x00	cha_rank2_ca2_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank2 channel A ca2.
7:0	RO	0x00	cha_rank2_ca3_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank2 channel A ca3.

DDRPHY_COM_REG_0x9e

Address: Operational Base(0xFF4F0000) + offset (0x0278)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	cha_rank2_ca4_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank2 channel A ca4.
23:16	RO	0x00	cha_rank2_ca5_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank2 channel A ca5.
15:8	RO	0x00	cha_rank3_ca0_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank3 channel A ca0.
7:0	RO	0x00	cha_rank3_ca1_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank3 channel A ca1.

DDRPHY_COM_REG_0x9f

Address: Operational Base(0xFF4F0000) + offset (0x027C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	cha_rank3_ca2_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank3 channel A ca2.
23:16	RO	0x00	cha_rank3_ca3_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank3 channel A ca3.
15:8	RO	0x00	cha_rank3_ca4_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank3 channel A ca4.
7:0	RO	0x00	cha_rank3_ca5_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank3 channel A ca5.

DDRPHY_COM_REG_0xa0

Address: Operational Base(0xFF4F0000) + offset (0x0280)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	cha_rank2_min_cs_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank2 channel A cs .

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Bit	Attr	Reset Value	Description
23:16	RO	0x00	cha_rank3_min_cs_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank3 channel A cs.
15:8	RO	0x00	cha_rank2_max_cs_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank2 channel A cs .
7:0	RO	0x00	cha_rank3_max_cs_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank3 channel A cs.

DDRPHY_COM_REG_0xa1

Address: Operational Base(0xFF4F0000) + offset (0x0284)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	cha_rank2_ca0_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank2 channel A ca0.
23:16	RO	0x00	cha_rank2_ca1_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank2 channel A ca1.
15:8	RO	0x00	cha_rank2_ca2_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank2 channel A ca2.
7:0	RO	0x00	cha_rank2_ca3_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank2 channel A ca3.

DDRPHY_COM_REG_0xa2

Address: Operational Base(0xFF4F0000) + offset (0x0288)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	cha_rank2_ca4_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank2 channel A ca4.
23:16	RO	0x00	cha_rank2_ca5_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank2 channel A ca5.
15:8	RO	0x00	cha_rank3_ca0_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank3 channel A ca0.
7:0	RO	0x00	cha_rank3_ca1_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank3 channel A ca1.

DDRPHY_COM_REG_0xa3

Address: Operational Base(0xFF4F0000) + offset (0x028C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	cha_rank3_ca2_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank3 channel A ca2.
23:16	RO	0x00	cha_rank3_ca3_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank3 channel A ca3.
15:8	RO	0x00	cha_rank3_ca4_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank3 channel A ca4.
7:0	RO	0x00	cha_rank3_ca5_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank3 channel A ca5.

DDRPHY_COM_REG_0xa4

Address: Operational Base(0xFF4F0000) + offset (0x0290)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	chb_rank2_ca0_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank2 channel B ca0.
23:16	RO	0x00	chb_rank2_ca1_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank2 channel B ca1.
15:8	RO	0x00	chb_rank2_ca2_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank2 channel B ca2.
7:0	RO	0x00	chb_rank2_ca3_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank2 channel B ca3.

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DDRPHY_COM_REG_0xa5

Address: Operational Base(0xFF4F0000) + offset (0x0294)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	chb_rank2_ca4_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank2 channel B ca4.
23:16	RO	0x00	chb_rank2_ca5_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank2 channel B ca5.
15:8	RO	0x00	chb_rank3_ca0_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank3 channel B ca0.
7:0	RO	0x00	chb_rank3_ca1_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank3 channel B ca1.

DDRPHY_COM_REG_0xa6

Address: Operational Base(0xFF4F0000) + offset (0x0298)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	chb_rank3_ca2_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank3 channel B ca2.
23:16	RO	0x00	chb_rank3_ca3_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank3 channel B ca3.
15:8	RO	0x00	chb_rank3_ca4_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank3 channel B ca4.
7:0	RO	0x00	chb_rank3_ca5_min_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank3 channel B ca5.

DDRPHY_COM_REG_0xa7

Address: Operational Base(0xFF4F0000) + offset (0x029C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	chb_rank2_min_cs_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank2 channel B cs .
23:16	RO	0x00	chb_rank3_min_cs_perbit_skew_pass[7:0] The min pass point of the tx delay line for rank3 channel B cs.
15:8	RO	0x00	chb_rank2_max_cs_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank2 channel B cs .
7:0	RO	0x00	chb_rank3_max_cs_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank3 channel B cs.

DDRPHY_COM_REG_0xa8

Address: Operational Base(0xFF4F0000) + offset (0x02A0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	chb_rank2_ca0_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank2 channel B ca0.
23:16	RO	0x00	chb_rank2_ca1_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank2 channel B ca1.
15:8	RO	0x00	chb_rank2_ca2_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank2 channel B ca2.
7:0	RO	0x00	chb_rank2_ca3_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank2 channel B ca3.

DDRPHY_COM_REG_0xa9

Address: Operational Base(0xFF4F0000) + offset (0x02A4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	chb_rank2_ca4_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank2 channel B ca4.
23:16	RO	0x00	chb_rank2_ca5_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank2 channel B ca5.

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Bit	Attr	Reset Value	Description
15:8	RO	0x00	chb_rank3_ca0_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank3 channel B ca0.
7:0	RO	0x00	chb_rank3_ca1_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank3 channel B ca1.

DDRPHY_COM_REG_0xaa

Address: Operational Base(0xFF4F0000) + offset (0x02A8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	chb_rank3_ca2_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank3 channel B ca2.
23:16	RO	0x00	chb_rank3_ca3_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank3 channel B ca3.
15:8	RO	0x00	chb_rank3_ca4_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank3 channel B ca4.
7:0	RO	0x00	chb_rank3_ca5_max_perbit_skew_pass[7:0] The max pass point of the tx delay line for rank3 channel B ca5.

DDRPHY_COM_REG_0xab

Address: Operational Base(0xFF4F0000) + offset (0x02AC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RO	0x00	cha_rank2_min_cs_vref_pass[5:0] The min pass point of the tx SDRAM's vref for rank2 channel A cs .
23:22	RO	0x0	reserved
21:16	RO	0x00	cha_rank2_max_cs_vref_pass[5:0] The max pass point of the tx delay line for rank2 channel A cs .
15:14	RO	0x0	reserved
13:8	RO	0x00	cha_rank3_min_cs_vref_pass[5:0] The min pass point of the tx SDRAM's vref for rank3 channel A cs .
7:6	RO	0x0	reserved
5:0	RO	0x00	cha_rank3_max_cs_vref_pass[5:0] The max pass point of the tx delay line for rank3 channel A cs.

DDRPHY_COM_REG_0xac

Address: Operational Base(0xFF4F0000) + offset (0x02B0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RO	0x00	chb_rank2_min_cs_vref_pass[5:0] The min pass point of the tx SDRAM's vref for rank2 channel B cs .
23:22	RO	0x0	reserved
21:16	RO	0x00	chb_rank2_max_cs_vref_pass[5:0] The max pass point of the tx delay line for rank2 channel B cs .
15:14	RO	0x0	reserved
13:8	RO	0x00	chb_rank3_min_cs_vref_pass[5:0] The min pass point of the tx SDRAM's vref for rank3 channel B cs .
7:6	RO	0x0	reserved
5:0	RO	0x00	chb_rank3_max_cs_vref_pass[5:0] The max pass point of the tx delay line for rank3 channel B cs.

DDRPHY_COM_REG_0xad

Address: Operational Base(0xFF4F0000) + offset (0x02B4)

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Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RO	0x0	cat_done_lpddr3 The lpddr3 cat done signal
23:20	RO	0x0	reg_rd_train_readback_data_valid_byte[3:0] The readback data valid signal when enable the read training bypass mode. Active High. When enable the read training bpass mode, after send out the read command and the read back data will be received by the phy and store in the following registers. When this bit is high, it means the read back data is valid. [0]: The read back data valid signal of byte0. [1]: The read back data valid signal of byte1. [2]: The read back data valid signal of byte2. [3]: The read back data valid signal of byte3. [4]: The read back data valid signal of byte4.
19	RO	0x0	reserved
18:15	RO	0x0	reg_train_done_for_rd_to_reg[3:0] The done signal of read train for byte0 to byte4. Active high. [0]: The done signal of the read train for byte0. [1]: The done signal of the read train for byte1. [2]: The done signal of the read train for byte2. [3]: The done signal of the read train for byte3. [4]: The done signal of the read train for byte4.
14	RO	0x0	reserved
13:10	RO	0x0	reg_train_error_for_rd_byte[3:0] The error signal of read train for byte0 to byte4. Active high. [0]: The error signal of the read train for byte0. [1]: The error signal of the read train for byte1. [2]: The error signal of the read train for byte2. [3]: The error signal of the read train for byte3. [4]: The error signal of the read train for byte4.
9	RO	0x0	reserved
8:5	RO	0x0	reg_wr_train_done_byte[3:0] The done flag of the write training for byte0 to byte4. High means done. [0]: The done flag of the write training for byte0. [1]: The done flag of the write training for byte1. [2]: The done flag of the write training for byte2. [3]: The done flag of the write training for byte3. [4]: The done flag of the write training for byte4.
4	RO	0x0	reserved
3:0	RO	0x0	reg_wr_train_error_byte[3:0] The error flag of the write training for byte0 to byte4. High means error. [0]: The error flag of the write training for byte0. [1]: The error flag of the write training for byte1. [2]: The error flag of the write training for byte2. [3]: The error flag of the write training for byte3. [4]: The error flag of the write training for byte4.

DDRPHY_COM_REG_0xae

Address: Operational Base(0xFF4F0000) + offset (0x02B8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:18	RO	0x00	drvleg_zqcali_s11_low_to_reg[5:0]

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Bit	Attr	Reset Value	Description
17:12	RO	0x00	drvleg_zqcali_s10_low_to_reg[5:0]
11:6	RO	0x00	drvleg_zqcali_s01_low_to_reg[5:0]
5:0	RO	0x00	drvleg_zqcali_s00_low_to_reg[5:0]

DDRPHY_COM_REG_0xaf

Address: Operational Base(0xFF4F0000) + offset (0x02BC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:18	RO	0x00	drvleg_zqcali_s11_high_to_reg[5:0]
17:12	RO	0x00	drvleg_zqcali_s10_high_to_reg[5:0]
11:6	RO	0x00	drvleg_zqcali_s01_high_to_reg[5:0]
5:0	RO	0x00	drvleg_zqcali_s00_high_to_reg[5:0]

DDRPHY_COM_REG_0xb0

Address: Operational Base(0xFF4F0000) + offset (0x02C0)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:10	RW	0x0	timer_lpddr3_pd_exit_select
9:8	RW	0x0	timer_lpddr3_pd_wait_select
7:6	RW	0x0	timer_lpddr3_pd_entry_select
5	RW	0x0	mrr_dai
4	RW	0x0	reg_init_lpddr3_pd_en
3	RW	0x0	reg_init_lpddr3_mrr_en
2	RW	0x0	reg_lpddr3_preact_before_mrwreset
1	RW	0x0	reg_lpddr3_preall_before_mrwreset
0	RW	0x1	reg_dfi_idle_en

DDRPHY_COM_REG_0xb1

Address: Operational Base(0xFF4F0000) + offset (0x02C4)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	reg_ddrc_tmrd
23:16	RW	0x00	reg_init_lpddr3_pd_exit
15:8	RW	0x00	reg_init_lpddr3_pd_wait
7:0	RW	0x00	reg_init_lpddr3_pd_entry

DDRPHY_COM_REG_0xb2

Address: Operational Base(0xFF4F0000) + offset (0x02C8)

Bit	Attr	Reset Value	Description
31:24	RW	0x40	reg_tinit1_100ns
23:16	RW	0x01	reg_ddrc_trp
15:8	RW	0x00	reg_ddrc_trpa
7:0	RW	0x00	reg_ddrc_tmrr

DDRPHY_COM_REG_0xb3

Address: Operational Base(0xFF4F0000) + offset (0x02CC)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	reg_mrwreset_1us
23:16	RW	0x00	reg_lpddr3_tinit5
15:0	RW	0x3ffc	reg_lpddr3_load_mode_mrwreset

DDRPHY_COM_REG_0xb4

Address: Operational Base(0xFF4F0000) + offset (0x02D0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0aab	reg_lpddr3_load_mode_mrwzqcl

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	reg_lpddr3_load_mode00

DDRPHY_COM_REG_0xb5

Address: Operational Base(0xFF4F0000) + offset (0x02D4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	reg_lpddr3_load_mode02
15:0	RW	0x0000	reg_lpddr3_load_mode01

DDRPHY_COM_REG_0xb6

Address: Operational Base(0xFF4F0000) + offset (0x02D8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	reg_lpddr3_load_mode48
15:0	RW	0x0000	reg_lpddr3_load_mode_read

DDRPHY_COM_REG_0xb7

Address: Operational Base(0xFF4F0000) + offset (0x02DC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	reg_lpddr3_load_mode42
15:0	RW	0x0000	reg_lpddr3_load_mode41

DDRPHY_COM_REG_0xb8

Address: Operational Base(0xFF4F0000) + offset (0x02E0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:14	RW	0x101	reg_cat_ca_check_value_lpddr3
13:4	RW	0x101	reg_cat_ca_train_value_lpddr3
3:0	RW	0xf	reg_lpddr3_tmrw

DDRPHY_COM_REG_0xb9

Address: Operational Base(0xFF4F0000) + offset (0x02E4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	reg_cmd0_abutnrcomp4_cs_chA_reg
27	RW	0x1	reg_cmd0_abutnrcomp3_cs_chA_reg
26	RW	0x1	reg_cmd0_abutnrcomp2_cs_chA_reg
25	RW	0x1	reg_cmd0_abutnrcomp1_cs_chA_reg
24	RW	0x0	reg_cmd0_abutnrcomp0_cs_chA_reg
23:21	RO	0x0	reserved
20	RW	0x0	reg_cmd0_abutprcomp4_cs_chA_reg
19	RW	0x1	reg_cmd0_abutprcomp3_cs_chA_reg
18	RW	0x1	reg_cmd0_abutprcomp2_cs_chA_reg
17	RW	0x1	reg_cmd0_abutprcomp1_cs_chA_reg
16	RW	0x0	reg_cmd0_abutprcomp0_cs_chA_reg
15:13	RO	0x0	reserved
12	RW	0x0	reg_cmd0_abutnrcomp4_cs_chB_reg
11	RW	0x1	reg_cmd0_abutnrcomp3_cs_chB_reg
10	RW	0x1	reg_cmd0_abutnrcomp2_cs_chB_reg
9	RW	0x1	reg_cmd0_abutnrcomp1_cs_chB_reg
8	RW	0x0	reg_cmd0_abutnrcomp0_cs_chB_reg
7:5	RO	0x0	reserved
4	RW	0x0	reg_cmd0_abutprcomp4_cs_chB_reg
3	RW	0x1	reg_cmd0_abutprcomp3_cs_chB_reg
2	RW	0x1	reg_cmd0_abutprcomp2_cs_chB_reg
1	RW	0x1	reg_cmd0_abutprcomp1_cs_chB_reg

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Bit	Attr	Reset Value	Description
0	RW	0x0	reg_cmd0_abutprcomp0_cs_chB_reg

DDRPHY_COM_REG_0xba

Address: Operational Base(0xFF4F0000) + offset (0x02E8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	lpddr3_rank3_min_a0_perbit_skew_pass[7:0]
23:16	RO	0x00	lpddr3_rank2_min_a0_perbit_skew_pass[7:0]
15:8	RO	0x00	lpddr3_rank1_min_a0_perbit_skew_pass[7:0]
7:0	RO	0x00	lpddr3_rank0_min_a0_perbit_skew_pass[7:0]

DDRPHY_COM_REG_0xbb

Address: Operational Base(0xFF4F0000) + offset (0x02EC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	lpddr3_rank3_min_a1_perbit_skew_pass[7:0]
23:16	RO	0x00	lpddr3_rank2_min_a1_perbit_skew_pass[7:0]
15:8	RO	0x00	lpddr3_rank1_min_a1_perbit_skew_pass[7:0]
7:0	RO	0x00	lpddr3_rank0_min_a1_perbit_skew_pass[7:0]

DDRPHY_COM_REG_0xbc

Address: Operational Base(0xFF4F0000) + offset (0x02F0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	lpddr3_rank3_min_a2_perbit_skew_pass[7:0]
23:16	RO	0x00	lpddr3_rank2_min_a2_perbit_skew_pass[7:0]
15:8	RO	0x00	lpddr3_rank1_min_a2_perbit_skew_pass[7:0]
7:0	RO	0x00	lpddr3_rank0_min_a2_perbit_skew_pass[7:0]

DDRPHY_COM_REG_0xbd

Address: Operational Base(0xFF4F0000) + offset (0x02F4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	lpddr3_rank3_min_a3_perbit_skew_pass[7:0]
23:16	RO	0x00	lpddr3_rank2_min_a3_perbit_skew_pass[7:0]
15:8	RO	0x00	lpddr3_rank1_min_a3_perbit_skew_pass[7:0]
7:0	RO	0x00	lpddr3_rank0_min_a3_perbit_skew_pass[7:0]

DDRPHY_COM_REG_0xbe

Address: Operational Base(0xFF4F0000) + offset (0x02F8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	lpddr3_rank3_min_a4_perbit_skew_pass[7:0]
23:16	RO	0x00	lpddr3_rank2_min_a4_perbit_skew_pass[7:0]
15:8	RO	0x00	lpddr3_rank1_min_a4_perbit_skew_pass[7:0]
7:0	RO	0x00	lpddr3_rank0_min_a4_perbit_skew_pass[7:0]

DDRPHY_COM_REG_0xbf

Address: Operational Base(0xFF4F0000) + offset (0x02FC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	lpddr3_rank3_min_a5_perbit_skew_pass[7:0]
23:16	RO	0x00	lpddr3_rank2_min_a5_perbit_skew_pass[7:0]
15:8	RO	0x00	lpddr3_rank1_min_a5_perbit_skew_pass[7:0]
7:0	RO	0x00	lpddr3_rank0_min_a5_perbit_skew_pass[7:0]

DDRPHY_COM_REG_0xc0

Address: Operational Base(0xFF4F0000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	lpddr3_rank3_min_a6_perbit_skew_pass[7:0]

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Bit	Attr	Reset Value	Description
23:16	RO	0x00	lpddr3_rank2_min_a6_perbit_skew_pass[7:0]
15:8	RO	0x00	lpddr3_rank1_min_a6_perbit_skew_pass[7:0]
7:0	RO	0x00	lpddr3_rank0_min_a6_perbit_skew_pass[7:0]

DDRPHY_COM_REG_0xc1

Address: Operational Base(0xFF4F0000) + offset (0x0304)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	lpddr3_rank3_min_a7_perbit_skew_pass[7:0]
23:16	RO	0x00	lpddr3_rank2_min_a7_perbit_skew_pass[7:0]
15:8	RO	0x00	lpddr3_rank1_min_a7_perbit_skew_pass[7:0]
7:0	RO	0x00	lpddr3_rank0_min_a7_perbit_skew_pass[7:0]

DDRPHY_COM_REG_0xc2

Address: Operational Base(0xFF4F0000) + offset (0x0308)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	lpddr3_rank3_min_a8_perbit_skew_pass[7:0]
23:16	RO	0x00	lpddr3_rank2_min_a8_perbit_skew_pass[7:0]
15:8	RO	0x00	lpddr3_rank1_min_a8_perbit_skew_pass[7:0]
7:0	RO	0x00	lpddr3_rank0_min_a8_perbit_skew_pass[7:0]

DDRPHY_COM_REG_0xc3

Address: Operational Base(0xFF4F0000) + offset (0x030C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	lpddr3_rank3_min_a9_perbit_skew_pass[7:0]
23:16	RO	0x00	lpddr3_rank2_min_a9_perbit_skew_pass[7:0]
15:8	RO	0x00	lpddr3_rank1_min_a9_perbit_skew_pass[7:0]
7:0	RO	0x00	lpddr3_rank0_min_a9_perbit_skew_pass[7:0]

DDRPHY_COM_REG_0xc4

Address: Operational Base(0xFF4F0000) + offset (0x0310)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	lpddr3_rank3_max_a0_perbit_skew_pass[7:0]
23:16	RO	0x00	lpddr3_rank2_max_a0_perbit_skew_pass[7:0]
15:8	RO	0x00	lpddr3_rank1_max_a0_perbit_skew_pass[7:0]
7:0	RO	0x00	lpddr3_rank0_max_a0_perbit_skew_pass[7:0]

DDRPHY_COM_REG_0xc5

Address: Operational Base(0xFF4F0000) + offset (0x0314)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	lpddr3_rank3_max_a1_perbit_skew_pass[7:0]
23:16	RO	0x00	lpddr3_rank2_max_a1_perbit_skew_pass[7:0]
15:8	RO	0x00	lpddr3_rank1_max_a1_perbit_skew_pass[7:0]
7:0	RO	0x00	lpddr3_rank0_max_a1_perbit_skew_pass[7:0]

DDRPHY_COM_REG_0xc6

Address: Operational Base(0xFF4F0000) + offset (0x0318)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	lpddr3_rank3_max_a2_perbit_skew_pass[7:0]
23:16	RO	0x00	lpddr3_rank2_max_a2_perbit_skew_pass[7:0]
15:8	RO	0x00	lpddr3_rank1_max_a2_perbit_skew_pass[7:0]
7:0	RO	0x00	lpddr3_rank0_max_a2_perbit_skew_pass[7:0]

DDRPHY_COM_REG_0xc7

Address: Operational Base(0xFF4F0000) + offset (0x031C)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	lpddr3_rank3_max_a3_perbit_skew_pass[7:0]
23:16	RO	0x00	lpddr3_rank2_max_a3_perbit_skew_pass[7:0]
15:8	RO	0x00	lpddr3_rank1_max_a3_perbit_skew_pass[7:0]
7:0	RO	0x00	lpddr3_rank0_max_a3_perbit_skew_pass[7:0]

DDRPHY_COM_REG_0xc8

Address: Operational Base(0xFF4F0000) + offset (0x0320)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	lpddr3_rank3_max_a4_perbit_skew_pass[7:0]
23:16	RO	0x00	lpddr3_rank2_max_a4_perbit_skew_pass[7:0]
15:8	RO	0x00	lpddr3_rank1_max_a4_perbit_skew_pass[7:0]
7:0	RO	0x00	lpddr3_rank0_max_a4_perbit_skew_pass[7:0]

DDRPHY_COM_REG_0xc9

Address: Operational Base(0xFF4F0000) + offset (0x0324)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	lpddr3_rank3_max_a5_perbit_skew_pass[7:0]
23:16	RO	0x00	lpddr3_rank2_max_a5_perbit_skew_pass[7:0]
15:8	RO	0x00	lpddr3_rank1_max_a5_perbit_skew_pass[7:0]
7:0	RO	0x00	lpddr3_rank0_max_a5_perbit_skew_pass[7:0]

DDRPHY_COM_REG_0xca

Address: Operational Base(0xFF4F0000) + offset (0x0328)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	lpddr3_rank3_max_a6_perbit_skew_pass[7:0]
23:16	RO	0x00	lpddr3_rank2_max_a6_perbit_skew_pass[7:0]
15:8	RO	0x00	lpddr3_rank1_max_a6_perbit_skew_pass[7:0]
7:0	RO	0x00	lpddr3_rank0_max_a6_perbit_skew_pass[7:0]

DDRPHY_COM_REG_0xcb

Address: Operational Base(0xFF4F0000) + offset (0x032C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	lpddr3_rank3_max_a7_perbit_skew_pass[7:0]
23:16	RO	0x00	lpddr3_rank2_max_a7_perbit_skew_pass[7:0]
15:8	RO	0x00	lpddr3_rank1_max_a7_perbit_skew_pass[7:0]
7:0	RO	0x00	lpddr3_rank0_max_a7_perbit_skew_pass[7:0]

DDRPHY_COM_REG_0xcc

Address: Operational Base(0xFF4F0000) + offset (0x0330)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	lpddr3_rank3_max_a8_perbit_skew_pass[7:0]
23:16	RO	0x00	lpddr3_rank2_max_a8_perbit_skew_pass[7:0]
15:8	RO	0x00	lpddr3_rank1_max_a8_perbit_skew_pass[7:0]
7:0	RO	0x00	lpddr3_rank0_max_a8_perbit_skew_pass[7:0]

DDRPHY_COM_REG_0xcd

Address: Operational Base(0xFF4F0000) + offset (0x0334)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	lpddr3_rank3_max_a9_perbit_skew_pass[7:0]
23:16	RO	0x00	lpddr3_rank2_max_a9_perbit_skew_pass[7:0]
15:8	RO	0x00	lpddr3_rank1_max_a9_perbit_skew_pass[7:0]
7:0	RO	0x00	lpddr3_rank0_max_a9_perbit_skew_pass[7:0]

DDRPHY_COM_REG_0xce

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Address: Operational Base(0xFF4F0000) + offset (0x0338)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	reg_lpddr3_use_odt02
13	RW	0x0	reg_lpddr3_only_use_odt0
12	RW	0x0	cat_skip_freq_change
11:8	RW	0xa	reg_tcackel_lpddr3
7:4	RW	0xa	reg_tcaent_lpddr3
3:0	RW	0xa	reg_tcaext_lpddr3

DDRPHY_BYTE0/1/2/3 Registers Description:

DDRPHY_BYTE_REG_0x0

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:23	RW	0x100	reg_a_l_vref1_margsel_reg Used to control the rx vref of byte0. If the user wants to change the rx vref value after the vref training, the user can use this register to set the rx vref value and set reg_rx_vref_value_update from 1'b0 to 1'b1 to update the rx vref value.
22	RW	0x0	reg_a_l_dq_odt_zqcali_en The odt control signal of byte0. 1: Choose the zqcalibration result as the control signal. 0: Choose the register as the conrol signal.
21	RW	0x0	reg_a_l_dq_drv_zqcali_en The driver control signal of byte0. 1: Choose the zqcalibration result as the control signal. 0: Choose the register as the conrol signal.
20	RW	0x0	reg_a_l_abutweakpddq_reg Weak pull down of A_DQ0~A_DQ7. Combine with reg_a_l_abutweakpubdq to control the state of the A_DQ0~A_DQ7. [1:0] = 2'b00. Pull Up. [1:0] = 2'b01. Middle level. [1:0] = 2'b10. High-Z. [1:0] = 2'b11. Pull Down.
19	RW	0x1	reg_a_l_abutweakpubdq_reg Weak pull up of A_DQ0~A_DQ7. Combine with reg_a_l_abutweakpubdq to control the state of the A_DQ0~A_DQ7. [1:0] = 2'b00. Pull Up. [1:0] = 2'b01. Middle level. [1:0] = 2'b10. High-Z. [1:0] = 2'b11. Pull Down.
18	RW	0x0	reg_a_l_abutdiffampseen_reg Reserved.
17	RW	0x0	reg_a_l_dqfben_reg The phy bist byte0 feebback enable signal. Active high.
16	RW	0x0	reg_a_l_dqfbsel_reg The phy bist dq path seletc signal. 0: Choose to arrive the pad. 1: Choose the interal as the end.
15	RW	0x0	reg_a_l_vref1_pd_reg The power down enabl signal of RX VREF for Byte0. Active low.
14:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:8	RW	0x00	reg_a_l_abutslewpu_reg Byte0 rising edge slew rate control, larger value means larger risign slew rate.
7	RW	0x1	reg_a_l_enb_lp4mode_reg When the value is 1'b0, enble the first byte of Lpddr4's Tx drive pull down, you can just keep it to 1.
6	RW	0x0	reg_a_l_dqsweakpd_reg Weak pull down of A_DQS0. Combine with reg_a_l_dqsweakpub to control the state of the A_DQS0. [7:6] = 2'b00. Pull Up. [7:6] = 2'b01. Middle level. [7:6] = 2'b10. High-Z. [7:6] = 2'b11. Pull Down.
5	RW	0x1	reg_a_l_dqsbweakpub_reg Weak pull up of A_DQS0. Combine with reg_a_l_dqsweakpd to control the state of the A_DQS0. [7:6] = 2'b00. Pull Up. [7:6] = 2'b01. Middle level. [7:6] = 2'b10. High-Z. [7:6] = 2'b11. Pull Down.
4:0	RW	0x00	reg_a_l_abutslewpd_reg Byte0 falling edge slew rate control, larger value means larger falling slew rate.

DDRPHY_BYTE_REG_0x1

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	reg_a_l_abutnrcompdq4_reg pull-down driving resistance for A_DQ[7:0]. The resistance relation with the configuration show in chapter 4.4.4
27	RW	0x1	reg_a_l_abutnrcompdq3_reg pull-down driving resistance for A_DQ[7:0]. The resistance relation with the configuration show in chapter 4.4.4.
26	RW	0x1	reg_a_l_abutnrcompdq2_reg pull-down driving resistance for A_DQ[7:0]. The resistance relation with the configuration show in chapter 4.4.4.
25	RW	0x1	reg_a_l_abutnrcompdq1_reg pull-down driving resistance for A_DQ[7:0]. The resistance relation with the configuration show in chapter 4.4.4.
24	RW	0x0	reg_a_l_abutnrcompdq0_reg pull-down driving resistance for A_DQ[7:0]. The resistance relation with the configuration show in chapter 4.4.4.
23:21	RO	0x0	reserved
20	RW	0x0	reg_a_l_abutprcompdq4_reg pull-up driving resistance for A_DQ[7:0]. The resistance relation with the configuration show in chapter 4.4.4.

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Bit	Attr	Reset Value	Description
19	RW	0x1	reg_a_l_abutprcompdq3_reg pull-up driving resistance for A_DQ[7:0]. The resistance relation with the configuration show in chapter 4.4.4.
18	RW	0x1	reg_a_l_abutprcompdq2_reg pull-up driving resistance for A_DQ[7:0]. The resistance relation with the configuration show in chapter 4.4.4.
17	RW	0x1	reg_a_l_abutprcompdq1_reg pull-up driving resistance for A_DQ[7:0]. The resistance relation with the configuration show in chapter 4.4.4.
16	RW	0x0	reg_a_l_abutprcompdq0_reg pull-up driving resistance for A_DQ[7:0]. The resistance relation with the configuration show in chapter 4.4.4.
15:13	RO	0x0	reserved
12	RW	0x0	reg_a_l_abutodtpddq4_reg pull-down ODT resistance for A_DQ[7:0]. The resistance relation with the configuration show in chapter 4.4.4.
11	RW	0x0	reg_a_l_abutodtpddq3_reg pull-down ODT resistance for A_DQ[7:0]. The resistance relation with the configuration show in chapter 4.4.4.
10	RW	0x1	reg_a_l_abutodtpddq2_reg pull-down ODT resistance for A_DQ[7:0]. The resistance relation with the configuration show in chapter 4.4.4.
9	RW	0x0	reg_a_l_abutodtpddq1_reg pull-down ODT resistance for A_DQ[7:0]. The resistance relation with the configuration show in chapter 4.4.4.
8	RW	0x1	reg_a_l_abutodtpddq0_reg pull-down ODT resistance for A_DQ[7:0]. The resistance relation with the configuration show in chapter 4.4.4.
7:5	RO	0x0	reserved
4	RW	0x0	reg_a_l_abutodtpudq4_reg pull-up ODT resistance for A_DQ[7:0]. The resistance relation with the configuration show in chapter 4.4.4.
3	RW	0x0	reg_a_l_abutodtpudq3_reg pull-up ODT resistance for A_DQ[7:0]. The resistance relation with the configuration show in chapter 4.4.4.
2	RW	0x1	reg_a_l_abutodtpudq2_reg pull-up ODT resistance for A_DQ[7:0]. The resistance relation with the configuration show in chapter 4.4.4.
1	RW	0x0	reg_a_l_abutodtpudq1_reg pull-up ODT resistance for A_DQ[7:0]. The resistance relation with the configuration show in chapter 4.4.4.

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Bit	Attr	Reset Value	Description
0	RW	0x1	reg_a_l_abutodtpudq0_reg pull-up ODT resistance for A_DQ[7:0]. The resistance relation with the configuration show in chapter 4.4.4.

DDRPHY_BYTE_REG_0x2

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x1	reg_a_l_pvt_comp_en Reserved.
19:10	RO	0x000	reserved
9	RW	0x1	reg_a_l_rxen_lp4 select receiver for different type of sdram. When lpddr4 and lpddr4x, set it to 1, when ddr3 , ddr4 , lpddr3 , set it to 0 .
8	RW	0x0	reg_a_l_lp4x_en_reg when lpddr4x , set it to 1, else set it to 0.
7:4	RO	0x0	reserved
3:2	RW	0x0	reg_a_l_weakpd_reg Reserved.
1:0	RW	0x3	reg_a_l_weakpub_reg Reserved.

DDRPHY_BYTE_REG_0x3

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:21	RW	0x7	reg_a_l_dq7_wrap_sel The wrap select signal of dq7 in BYTE0 od DQ pins on the sdram side
20:18	RW	0x6	reg_a_l_dq6_wrap_sel The wrap select signal of dq6 in BYTE0 od DQ pins on the sdram side
17:15	RW	0x5	reg_a_l_dq5_wrap_sel The wrap select signal of dq5 in BYTE0 od DQ pins on the sdram side
14:12	RW	0x4	reg_a_l_dq4_wrap_sel The wrap select signal of dq4 in BYTE0 od DQ pins on the sdram side
11:9	RW	0x3	reg_a_l_dq3_wrap_sel The wrap select signal of dq3 in BYTE0 od DQ pins on the sdram side
8:6	RW	0x2	reg_a_l_dq2_wrap_sel The wrap select signal of dq2 in BYTE0 od DQ pins on the sdram side
5:3	RW	0x1	reg_a_l_dq1_wrap_sel The wrap select signal of dq1 in BYTE0 od DQ pins on the sdram side
2:0	RW	0x0	reg_a_l_dq0_wrap_sel The wrap select signal of dq0 in BYTE0 od DQ pins on the sdram side

DDRPHY_BYTE_REG_0x4

Address: **Operational Base** + offset (0x0010)

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Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:24	RW	0x1	reg_a_l_rxmen0_delay_bp The register used to control the 1x delay of the rx dqs calibration delay for byte0 of RANK0 when enable the rx dqs calibration bypass mode at the posedge of setting reg_calib_freq_update to 1'b1. Unit = 4UI.
23:21	RW	0x7	reg_a_l_rxmen0_ophsel_bp The register used to control the 0.5*4x delay of the rx dqs calibration delay for byte 0 of RANK0 when enable the rx dqs calibration bypass mode at the posedge of setting reg_calib_freq_update to 1'b1. Unit = 0.5UI.
20:16	RW	0x08	reg_a_l_rxmen0_sdlltap_bp The register used to control the delay line of the rx dqs calibration delay for byte 0 of RANK0 when enable the rx dqs calibration bypass mode at the posedge of setting reg_calib_freq_update to 1'b1. Unit = 4UI/256.
15:11	RO	0x00	reserved
10:8	RW	0x1	reg_a_l_rxmen1_delay_bp The register used to control the 1x delay of the rx dqs calibration delay for byte0 of RANK1 when enable the rx dqs calibration bypass mode at the posedge of setting reg_calib_freq_update to 1'b1. Unit = 4UI
7:5	RW	0x7	reg_a_l_rxmen1_ophsel_bp The register used to control the 0.5*4x delay of the rx dqs calibration delay for byte 0 of RANK1 when enable the rx dqs calibration bypass mode at the posedge of setting reg_calib_freq_update to 1'b1. Unit = 0.5UI.
4:0	RW	0x08	reg_a_l_rxmen1_sdlltap_bp The register used to control the delay line of the rx dqs calibration delay for byte 0 of RANK1 when enable the rx dqs calibration bypass mode at the posedge of setting reg_calib_freq_update to 1'b1. Unit = 4UI/256.

DDRPHY_BYTE_REG_0x5

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:24	RW	0x2	reg_a_l_rdodt0_delay The register used to control the 0.5*4x delay of the rx odt delay for byte 0 of RANK0 when enable the rx odt bypass mode by setting reg_rdodt_bypass to 1'b1. Unit = 0.5UI.
23:21	RW	0x4	reg_a_l_rdodt0_ophsel The register used to control the delay line of the rx odt delay for byte 0 of RANK0 when enable the rx odt bypass mode by setting reg_rdodt_bypass to 1'b1. Unit = 4UI/256.

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Bit	Attr	Reset Value	Description
20:16	RW	0x04	reg_a_l_rdodt0_dllsel The register used to control the 1x delay of the rx odt delay for byte0 of RANK0 when enable the rx odt bypass mode by setting reg_rdodt_bypass to 1'b1. Unit = 4UI.
15:11	RO	0x00	reserved
10:8	RW	0x2	reg_a_l_rdodt1_delay The register used to control the 0.5*4x delay of the rx odt delay for byte 0 of RANK1 when enable the rx odt bypass mode by setting reg_rdodt_bypass to 1'b1. Unit = 0.5*UI.
7:5	RW	0x4	reg_a_l_rdodt1_ophsel The register used to control the delay line of the rx odt delay for byte 0 of RANK1 when enable the rx odt bypass mode by setting reg_rdodt_bypass to 1'b1. Unit = 4UI/256.
4:0	RW	0x04	reg_a_l_rdodt1_dllsel The register used to control the 1x delay of the rx odt delay for byte0 of RANK1 when enable the rx odt bypass mode by setting reg_rdodt_bypass to 1'b1. Unit = UI.

DDRPHY_BYTE_REG_0x6

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	reg_a_l_rxm4p5en_cs3 The enable signal to extend the gating signal of the rx dqs calibration for byte0 of the RANK3. 1: Increase 0.5UI to the gating signal. 0: Keep the default state.
29	RW	0x0	reg_a_l_rxm4p5en_cs2 The enable signal to extend the gating signal of the rx dqs calibration for byte0 of the RANK2. 1: Increase 0.5UI to the gating signal. 0: Keep the default state.
28	RW	0x0	reg_a_l_dm_obsdataen Reserved.
27:24	RW	0x0	reg_a_l_dqobsmuxsel Reserved.
23	RO	0x0	reserved
22	RW	0x1	reg_a_l_dqout_mux The register using to contro the timing of the dq for byte0 from the digial part to the analog part. 1: Align to the posedge of the dfi_clk1x. 0: Align to the negedge of the dfi_clk1x.
21	RW	0x1	reg_a_l_dmout_mux The register using to contro the timing of the dm for byte0 from the digial part to the analog part. 1: Align to the posedge of the dfi_clk1x. 0: Align to the negedge of the dfi_clk1x.

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Bit	Attr	Reset Value	Description
20	RW	0x0	reg_a_l_dq_ph90en_bp Used to control the 90 degree of the dq/dm for byte0 when the ph90en_bp_dq set to 1'b1. 1: Choose the 90 degree mode. 0: Disable the 90 degree mode.
19	RW	0x1	reg_a_l_dqs_ph90en_bp Used to control the 90 degree of the dqs for byte0 when the ph90en_bp_dq set to 1'b1. 1: Choose the 90 degree mode. 0: Disable the 90 degree mode.
18	RW	0x1	reg_a_l_rcvdqsmodsel Reserved.
17	RW	0x1	reg_a_l_selfclren Reserved.
16	RW	0x1	reg_a_l_wrptrclrb Reserved.
15	RW	0x1	reg_a_l_rxm_odiffampen Reserved.
14	RW	0x0	reg_a_l_abutobsmodeen Reserved.
13	RO	0x0	reserved
12	RW	0x0	reg_a_l_rxm4p5en_cs0 The enable signal to extend the gating signal of the rx dqs calibration for byte0 of the RANK0. 1: Increase 0.5UI to the gating signal. 0: Keep the default state.
11	RW	0x1	reg_a_l_tsm_iobufact_bp Reserved.
10	RW	0x0	reg_a_l_rxpst_bp Reserved.
9	RO	0x0	reserved
8	RW	0x0	reg_a_l_rxm4p5en_cs1 The enable signal to extend the gating signal of the rx dqs calibration for byte0 of the RANK1. 1: Increase 0.5UI to the gating signal. 0: Keep the default state.
7:6	RO	0x0	reserved
5:3	RW	0x0	reg_a_l_rrankdly_4x_cs0 The register used to conrol the delay of the read rank switch signal of the byte0 for RANK0. Unit= 0.5UI.
2:0	RW	0x0	reg_a_l_rrankdly_4x_cs1 The register used to conrol the delay of the read rank switch signal of the byte0 for RANK1. Unit= 0.5UI.

DDRPHY_BYTE_REG_0x7

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:15	RW	0x1	reg_a_l_rrankdly_1x_cs0 The register used to conrol the delay of the read rank switch signal of the byte0 for RANK0. Unit= dfi_clk1x.(reg_rdrank_delay_bp = 1)

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Bit	Attr	Reset Value	Description
14:12	RW	0x1	reg_a_l_rrankdly_1x_cs1 The register used to conrol the delay of the read rank switch signal of the byte0 for RANK1. Unit= dfi_clk1x.(reg_rdrank_delay_bp = 1)
11	RW	0x0	reg_a_l_dq_invdelay_lp_en
10:8	RW	0x6	reg_a_l_wrankphsel_0 The register used to control the delay of the write rank switch signal of the byte0. Unit=0.5UI.
7:3	RO	0x00	reserved
2:0	RW	0x6	reg_a_l_wrankphsel_1 The register used to control the delay of the write rank switch signal of the byte0. Unit=0.5UI.

DDRPHY_BYTE_REG_0x8

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x80	reg_a_l_cs0_dm_invdelaysel The register used to control the tx delay line of the A_DM0 for RANK0.

DDRPHY_BYTE_REG_0x9

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:24	RW	0x80	reg_a_l_cs0_dq0_invdelaysel The register used to control the tx delay line of the A_DQ0 for RANK0.
23:16	RW	0x80	reg_a_l_cs0_dq1_invdelaysel The register used to control the tx delay line of the A_DQ1 for RANK0.
15:8	RW	0x80	reg_a_l_cs0_dq2_invdelaysel The register used to control the tx delay line of the A_DQ2 for RANK0.
7:0	RW	0x80	reg_a_l_cs0_dq3_invdelaysel The register used to control the tx delay line of the A_DQ3 for RANK0.

DDRPHY_BYTE_REG_0xa

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:24	RW	0x80	reg_a_l_cs0_dq4_invdelaysel The register used to control the tx delay line of the A_DQ4 for RANK0.
23:16	RW	0x80	reg_a_l_cs0_dq5_invdelaysel The register used to control the tx delay line of the A_DQ5 for RANK0.
15:8	RW	0x80	reg_a_l_cs0_dq6_invdelaysel The register used to control the tx delay line of the A_DQ6 for RANK0.
7:0	RW	0x80	reg_a_l_cs0_dq7_invdelaysel The register used to control the tx delay line of the A_DQ7 for RANK0.

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DDRPHY_BYTE_REG_0xb

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:24	RW	0x80	reg_a_l_cs0_dqs_invdelaysel The register used to control the tx delay line of the A_DQS0 for RANK0.
23:16	RO	0x00	reserved
15:8	RW	0x80	reg_a_l_cs0_dqsb_invdelaysel The register used to control the tx delay line of the A_DQSB0 for RANK0.
7:0	RO	0x00	reserved

DDRPHY_BYTE_REG_0xc

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28:24	RW	0x00	reg_a_l_cs0_loop_invdelaysel The register used to choose the obs signal to check delay line control of the byte0 for RANK0. 5'd0: Choose to the current value to control the tx delay line of A_DQ0 for RANK0. 5'd1: Choose to the current value to control the tx delay line of A_DQ1 for RANK0. 5'd2: Choose to the current value to control the tx delay line of A_DQ2 for RANK0. 5'd3: Choose to the current value to control the tx delay line of A_DQ3 for RANK0. 5'd4: Choose to the current value to control the tx delay line of A_DQ4 for RANK0. 5'd5: Choose to the current value to control the tx delay line of A_DQ5 for RANK0. 5'd6: Choose to the current value to control the tx delay line of A_DQ6 for RANK0. 5'd7: Choose to the current value to control the tx delay line of A_DQ7 for RANK0. 5'd8: Choose to the current value to control the tx delay line of A_DM0 for RANK0. 5'd9: Choose to the current value to control the tx delay line of A_DQS0 for RANK0. 5'd10: Choose to the current value to control the tx delay line of A_DQSB0 for RANK0. 5'd16: Choose to the current value to control the rx delay line of A_DQ0 for RANK0. 5'd17: Choose to the current value to control the rx delay line of A_DQ1 for RANK0. 5'd18: Choose to the current value to control the rx delay line of A_DQ2 for RANK0. 5'd19: Choose to the current value to control the rx delay line of A_DQ3 for RANK0. 5'd20: Choose to the current value to control the rx delay line of A_DQ4 for RANK0. 5'd21: Choose to the current value to control the rx delay line of A_DQ5 for RANK0. 5'd22: Choose to the current value to control the rx delay line of A_DQ6 for RANK0. 5'd23: Choose to the current value to control the rx delay line of A_DQ7 for RANK0. 5'd24: Choose to the current value to control the rx delay line of A_DM0 for RANK0. 5'd25 Choose to the current value to control the rx delay line of A_DQS0 for RANK0. 5'd26: Choose to the current value to control the rx delay line of A_DQSB0 for RANK0.
23:15	RO	0x000	reserved
14:8	RW	0x00	reg_a_l_cs0_dm_invdelayselrx The register used to control the rx delay line of the A_DM0 for RANK0.
7:0	RO	0x00	reserved

DDRPHY_BYTE_REG_0xd

Address: **Operational Base** + offset (0x0034)

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Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	reg_a_l_cs0_dq0_invdelayselrx The register used to control the rx delay line of the A_DQ0 for RANK0.
23	RO	0x0	reserved
22:16	RW	0x00	reg_a_l_cs0_dq1_invdelayselrx The register used to control the rx delay line of the A_DQ1 for RANK0.
15	RO	0x0	reserved
14:8	RW	0x00	reg_a_l_cs0_dq2_invdelayselrx The register used to control the rx delay line of the A_DQ2 for RANK0.
7	RO	0x0	reserved
6:0	RW	0x00	reg_a_l_cs0_dq3_invdelayselrx The register used to control the rx delay line of the A_DQ3 for RANK0.

DDRPHY_BYTE_REG_0xe

Address: **Operational Base** + offset (0x0038)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	reg_a_l_cs0_dq4_invdelayselrx The register used to control the rx delay line of the A_DQ4 for RANK0.
23	RO	0x0	reserved
22:16	RW	0x00	reg_a_l_cs0_dq5_invdelayselrx The register used to control the rx delay line of the A_DQ5 for RANK0.
15	RO	0x0	reserved
14:8	RW	0x00	reg_a_l_cs0_dq6_invdelayselrx The register used to control the rx delay line of the A_DQ6 for RANK0.
7	RO	0x0	reserved
6:0	RW	0x00	reg_a_l_cs0_dq7_invdelayselrx The register used to control the rx delay line of the A_DQ7 for RANK0.

DDRPHY_BYTE_REG_0xf

Address: **Operational Base** + offset (0x003C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x1f	reg_a_l_cs0_dqs_invdelayselrx The register used to control the rx delay line of the A_DQS0 for RANK0.
23:15	RO	0x000	reserved
14:8	RW	0x1f	reg_a_l_cs0_dqsb_invdelayselrx The register used to control the rx delay line of the A_DQSB0 for RANK0.
7:0	RO	0x00	reserved

DDRPHY_BYTE_REG_0x10

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x80	reg_a_l_cs1_dm_invdelaysel The register used to control the tx delay line of the A_DM0 for RANK1.

DDRPHY_BYTE_REG_0x11

Address: **Operational Base** + offset (0x0044)

Bit	Attr	Reset Value	Description
31:24	RW	0x80	reg_a_l_cs1_dq0_invdelaysel The register used to control the tx delay line of the A_DQ0 for RANK1.
23:16	RW	0x80	reg_a_l_cs1_dq1_invdelaysel The register used to control the tx delay line of the A_DQ1 for RANK1.
15:8	RW	0x80	reg_a_l_cs1_dq2_invdelaysel The register used to control the tx delay line of the A_DQ2 for RANK1.
7:0	RW	0x80	reg_a_l_cs1_dq3_invdelaysel The register used to control the tx delay line of the A_DQ3 for RANK1.

DDRPHY_BYTE_REG_0x12

Address: **Operational Base** + offset (0x0048)

Bit	Attr	Reset Value	Description
31:24	RW	0x80	reg_a_l_cs1_dq4_invdelaysel The register used to control the tx delay line of the A_DQ4 for RANK1.
23:16	RW	0x80	reg_a_l_cs1_dq5_invdelaysel The register used to control the tx delay line of the A_DQ5 for RANK1.
15:8	RW	0x80	reg_a_l_cs1_dq6_invdelaysel The register used to control the tx delay line of the A_DQ6 for RANK1.
7:0	RW	0x80	reg_a_l_cs1_dq7_invdelaysel The register used to control the tx delay line of the A_DQ7 for RANK1.

DDRPHY_BYTE_REG_0x13

Address: **Operational Base** + offset (0x004C)

Bit	Attr	Reset Value	Description
31:24	RW	0x80	reg_a_l_cs1_dqs_invdelaysel The register used to control the tx delay line of the A_DQS0 for RANK1.
23:16	RO	0x00	reserved
15:8	RW	0x80	reg_a_l_cs1_dqsb_invdelaysel The register used to control the tx delay line of the A_DQSB0 for RANK1.
7:0	RO	0x00	reserved

DDRPHY_BYTE_REG_0x14

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28:24	RW	0x00	reg_a_l_cs1_loop_invdelaysel The register used to choose the obs signal to check delay line control of the byte0 for RANK1. 5'd0: Choose to the current value to control the tx delay line of A_DQ0 for RANK1. 5'd1: Choose to the current value to control the tx delay line of A_DQ1 for RANK1. 5'd2: Choose to the current value to control the tx delay line of A_DQ2 for RANK1. 5'd3: Choose to the current value to control the tx delay line of A_DQ3 for RANK1. 5'd4: Choose to the current value to control the tx delay line of A_DQ4 for RANK1. 5'd5: Choose to the current value to control the tx delay line of A_DQ5 for RANK1. 5'd6: Choose to the current value to control the tx delay line of A_DQ6 for RANK1. 5'd7: Choose to the current value to control the tx delay line of A_DQ7 for RANK1. 5'd8: Choose to the current value to control the tx delay line of A_DM0 for RANK1. 5'd9: Choose to the current value to control the tx delay line of A_DQS0 for RANK1. 5'd10: Choose to the current value to control the tx delay line of A_DQSB0 for RANK1. 5'd16: Choose to the current value to control the rx delay line of A_DQ0 for RANK1. 5'd17: Choose to the current value to control the rx delay line of A_DQ1 for RANK1. 5'd18: Choose to the current value to control the rx delay line of A_DQ2 for RANK1. 5'd19: Choose to the current value to control the rx delay line of A_DQ3 for RANK1. 5'd20: Choose to the current value to control the rx delay line of A_DQ4 for RANK1. 5'd21: Choose to the current value to control the rx delay line of A_DQ5 for RANK1. 5'd22: Choose to the current value to control the rx delay line of A_DQ6 for RANK1. 5'd23: Choose to the current value to control the rx delay line of A_DQ7 for RANK1. 5'd24: Choose to the current value to control the rx delay line of A_DM0 for RANK1. 5'd25 Choose to the current value to control the rx delay line of A_DQS0 for RANK1. 5'd26: Choose to the current value to control the rx delay line of A_DQSB0 for RANK1.
23:15	RO	0x000	reserved
14:8	RW	0x00	reg_a_l_cs1_dm_invdelayselrx The register used to control the rx delay line of the A_DM0 for RANK1.
7:0	RO	0x00	reserved

DDRPHY_BYTE_REG_0x15

Address: **Operational Base** + offset (0x0054)

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Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	reg_a_l_cs1_dq0_invdelayselrx The register used to control the rx delay line of the A_DQ0 for RANK1.
23	RO	0x0	reserved
22:16	RW	0x00	reg_a_l_cs1_dq1_invdelayselrx The register used to control the rx delay line of the A_DQ1 for RANK1.
15	RO	0x0	reserved
14:8	RW	0x00	reg_a_l_cs1_dq2_invdelayselrx The register used to control the rx delay line of the A_DQ2 for RANK1.
7	RO	0x0	reserved
6:0	RW	0x00	reg_a_l_cs1_dq3_invdelayselrx The register used to control the rx delay line of the A_DQ3 for RANK1.

DDRPHY_BYTE_REG_0x16

Address: **Operational Base** + offset (0x0058)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	reg_a_l_cs1_dq4_invdelayselrx The register used to control the rx delay line of the A_DQ4 for RANK1.
23	RO	0x0	reserved
22:16	RW	0x00	reg_a_l_cs1_dq5_invdelayselrx The register used to control the rx delay line of the A_DQ5 for RANK1.
15	RO	0x0	reserved
14:8	RW	0x00	reg_a_l_cs1_dq6_invdelayselrx The register used to control the rx delay line of the A_DQ6 for RANK1.
7	RO	0x0	reserved
6:0	RW	0x00	reg_a_l_cs1_dq7_invdelayselrx The register used to control the rx delay line of the A_DQ7 for RANK1.

DDRPHY_BYTE_REG_0x17

Address: **Operational Base** + offset (0x005C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x1f	reg_a_l_cs1_dqs_invdelayselrx The register used to control the rx delay line of the A_DQS0 for RANK1.
23:15	RO	0x000	reserved
14:8	RW	0x1f	reg_a_l_cs1_dqsb_invdelayselrx The register used to control the rx delay line of the A_DQSB0 for RANK1.
7:0	RO	0x00	reserved

DDRPHY_BYTE_REG_0x18

Address: **Operational Base** + offset (0x0060)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
30:24	RW	0x1f	reg_a_l_rd_train_dqs_default This register is used to control the start point of the rx delay line of the dqs when read training for byte0. The read training will base on this value to begin the read train.
23:16	RW	0x07	reg_a_l_train_dqs_default In the default mode, the write training will use the write training result to control the tx delay line of the dqs and keep unchanged. The user also can set the reg_wr_train_dqs_default_bypass to 1'b1 to use this register to control the tx delay line of the dqs for write training for byte0.
15	RO	0x0	reserved
14:8	RW	0x3f	reg_a_l_rd_train_dqs_range_max The register is used to set the max scan range of the rx delay line of the dqs when read training for byte0. The phy will stop to scan when it increase the rx delay line to this value.
7	RO	0x0	reserved
6:0	RW	0x00	reg_a_l_rd_train_dqs_range_min The register is used to set the max scan range of the rx delay line of the dqs when read training for byte0. The phy will stop to scan when it iderease the rx delay line to this value.

DDRPHY_BYTE_REG_0x19

Address: **Operational Base** + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	reg_a_l_rdtrain_check_wrap0 The register used to control the read check pattern after the reamp in byte0. Valid only when the reg_rd_train_check_value_en set to 1'b1. For the read training of LPDDR4, the even DQ pads such as the DQ0/DQ2/DQ4/DQ6 have different check pattern with the odd DQS pads such as the DQ1/DQ3/DQ5/DQ7. After the remap in one byte, the DQ0 of the PHY may connect the DQ1 of the SDRAM. So the read back data from the odd DQ PAD will be send to the even DQ PAD to check. So the PHY need to know the remap releation between the PHY and SDRAM. For LPDDR4 mode, If the DQ PAD of the PHY connect to the event PAD of the SDRAM, the corresponding bit should set to 1'b1, or it will set to 1'b0. eg. If the DQ6 of the SDRAM connects to the DQ1 of the PHY. The bit[1] should set to 1'b1. if the DQ7 of the SDRAM connects to the DQ2 of the PHY. The bit[7] should set to 1'b0. For the read training of DDR4, the DQ0/DQ1/DQ2/DQ3 have different check pattern and DQ4/DQ5/DQ6/DQ7 repeat the check pattern of the DQ0/DQ1/DQ2/DQ3. After the remap in byte0, the user need to accord to the connect between the PHY and the SDRAM to set choose the check pattern. If the DQ0/DQ4 of the SDRAM connect to current pad of the PHY, the current pad should set to 2'b00. If the DQ1/DQ5 of the SDRAM connect to current pad of the PHY, the current pad should set to 2'b01. If the DQ2/DQ6 of the SDRAM connect to current pad of the PHY, the current pad should set to 2'b00. If the DQ3/DQ7 of the SDRAM connect to current pad of the PHY, the current pad should set to 2'b01. [1:0]: Used to control the check pattern of the DQ0 for byte0. [3:2]: Used to control the check pattern of the DQ1 for byte0. [5:4]: Used to control the check pattern of the DQ2 for byte0. [7:6]: Used to control the check pattern of the DQ3 for byte0. you can find more information in read train section

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	reg_a_l_rdtrain_check_wrap1 The register used to control the read check pattern after the reamp in byte0. Valid only when the reg_rd_train_check_value_en set to 1'b1. For the read training of DDR4, the DQ0/DQ1/DQ2/DQ3 have different check pattern and DQ4/DQ5/DQ6/DQ7 repeat the check pattern of the DQ0/DQ1/DQ2/DQ3. After the remap in byte0, the user need to accord to the connect between the PHY and the SDRAM to set choose the check pattern. If the DQ0/DQ4 of the SDRAM connect to current pad of the PHY, the current pad should set to 2'b00. If the DQ1/DQ5 of the SDRAM connect to current pad of the PHY, the current pad should set to 2'b01. If the DQ2/DQ6 of the SDRAM connect to current pad of the PHY, the current pad should set to 2'b00. If the DQ3/DQ7 of the SDRAM connect to current pad of the PHY, the current pad should set to 2'b01. [1:0]: Used to control the check pattern of the DQ4 for byte0. [3:2]: Used to control the check pattern of the DQ5 for byte0. [5:4]: Used to control the check pattern of the DQ6 for byte0. [7:6]: Used to control the check pattern of the DQ7 for byte0. you can find more information in read train section

DDRPHY_BYTE_REG_0x1c

Address: **Operational Base** + offset (0x0070)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	reg_a_l_dqs_idqshigh
29:24	RO	0x00	reserved
23:16	RO	0x00	reg_a_l_tdqs_invdelaysel0[7:0] The write-leveling result of byte0 for RANK0. The user can get the write-leveling result after the write-leveling training compelte.
15:8	RO	0x00	reserved
7:0	RO	0x00	reg_a_l_tdqs_invdelaysel1[7:0] The write-leveling result of byte0 for RANK1. The user can get the write-leveling result after the write-leveling training compelte.

DDRPHY_BYTE_REG_0x1d

Address: **Operational Base** + offset (0x0074)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:8	RO	0x0	reg_a_l_cycsel[2:0] The training reuslt of 4UI delay for rx dqs calibration of byte0. The value will be unchanged after the rx dqs calibration. When the reg_calcs_sel[1:0] == 2'b10 at the rx dqs calibration, it means the rx dqs calibration training result of RANK0, when the reg_calcs_sel[1:0] == 2'b01 at the rx dqs calibration, it means the rx dqs calibration training result of RANK1. After the rx dqs calibration of RANK0 and RANK1, the result will be lock into the correspongding register independently. In the normal mode, the reg_calcs_sel[1:0] will be set to 2'b00, so the phy will accord to the rank to swith automaticallly.

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Bit	Attr	Reset Value	Description
7:5	RO	0x0	reg_a_l_ophsel[2:0] The training reuslt of 0.5UI delay for rx dqs calibration of byte0. The value will be unchanged after the rx dqs calibration. When the reg_calcs_sel[1:0] == 2'b10 at the rx dqs calibration, it means the rx dqs calibration training result of RANK0, when the reg_calcs_sel[1:0] == 2'b01 at the rx dqs calibration, it means the rx dqs calibration training result of RANK1. After the rx dqs calibration of RANK0 and RANK1, the result will be lock into the correspongding register independently. In the normal mode, the reg_calcs_sel[1:0] will be set to 2'b00, so the phy will accord to the rank to swith automaticallly.
4:0	RO	0x00	reg_a_l_dllsel[4:0] The training reuslt of delay line for rx dqs calibration of byte0. The value will be unchanged after the rx dqs calibration. When the reg_calcs_sel[1:0] == 2'b10 at the rx dqs calibration, it means the rx dqs calibration training result of RANK0, when the reg_calcs_sel[1:0] == 2'b01 at the rx dqs calibration, it means the rx dqs calibration training result of RANK1. After the rx dqs calibration of RANK0 and RANK1, the result will be lock into the correspongding register independently. In the normal mode, the reg_calcs_sel[1:0] will be set to 2'b00, so the phy will accord to the rank to swith automaticallly.

DDRPHY_BYTE_REG_0x1e

Address: **Operational Base** + offset (0x0078)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RO	0x000	reg_a_l_calib_result_cs0[10:0] The current delay of the rx dqs calibration of byte0 for RANK0. The user can using this register to get the current working state of the rx dqs calibration. [4:0]: Means the tx delay line value of the rx dqs calibration. [7:5]: Means the 0.5UI delay value of the rx dqs calibration. [10:8]:The current 4UI delay of the rx dqs calibration of the byte0 for RANK0.The user can using this register to get the current working state of the rx dqs calibration.
15:11	RO	0x00	reserved
10:0	RO	0x000	reg_a_l_calib_result_cs1[10:0] The current delay of the rx dqs calibration of byte0 for RANK1. The user can using this register to get the current working state of the rx dqs calibration. [4:0]: Means the tx delay line value of the rx dqs calibration. [7:5]: Means the 0.5UI delay value of the rx dqs calibration. [10:8]:The current 4UI delay of the rx dqs calibration of the byte0 for RANK1.The user can using this register to get the current working state of the rx dqs calibration.

DDRPHY_BYTE_REG_0x1f

Address: **Operational Base** + offset (0x007C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	reg_a_l_cs0_value_dqx_invdelaysel[7:0] The delay line value of the current obs signal choosing of reg_cs0_a_l_loop_invdelaysel.

DDRPHY_BYTE_REG_0x20

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Address: **Operational Base** + offset (0x0080)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	reg_a_l_cs1_value_dqx_invdelaysel[7:0] The delay line value of the current obs signal choosing of reg_cs1_a_l_loop_invdelaysel.

DDRPHY_BYTE_REG_0x21

Address: **Operational Base** + offset (0x0084)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RO	0x00	reg_a_l_train_min_for_rd_dq0[6:0] The min pass point of the rx delay line for A_DQ0.
23	RO	0x0	reserved
22:16	RO	0x00	reg_a_l_train_min_for_rd_dq1[6:0] The min pass point of the rx delay line for A_DQ1.
15	RO	0x0	reserved
14:8	RO	0x00	reg_a_l_train_min_for_rd_dq2[6:0] The min pass point of the rx delay line for A_DQ2.
7	RO	0x0	reserved
6:0	RO	0x00	reg_a_l_train_min_for_rd_dq3[6:0] The min pass point of the rx delay line for A_DQ3.

DDRPHY_BYTE_REG_0x22

Address: **Operational Base** + offset (0x0088)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RO	0x00	reg_a_l_train_min_for_rd_dq4[6:0] The min pass point of the rx delay line for A_DQ4.
23	RO	0x0	reserved
22:16	RO	0x00	reg_a_l_train_min_for_rd_dq5[6:0] The min pass point of the rx delay line for A_DQ5.
15	RO	0x0	reserved
14:8	RO	0x00	reg_a_l_train_min_for_rd_dq6[6:0] The min pass point of the rx delay line for A_DQ6.
7	RO	0x0	reserved
6:0	RO	0x00	reg_a_l_train_min_for_rd_dq7[6:0] The min pass point of the rx delay line for A_DQ7.

DDRPHY_BYTE_REG_0x23

Address: **Operational Base** + offset (0x008C)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:8	RO	0x00	reg_a_l_train_min_for_rd_dm[6:0] The min pass point of the rx delay line for A_DM0, only for lp4.
7	RO	0x0	reserved
6:0	RO	0x00	reg_a_l_train_min_for_rd_dqs[6:0] The min pass point of the rx delay line for A_DQS0/A_DQSB0.

DDRPHY_BYTE_REG_0x24

Address: **Operational Base** + offset (0x0090)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RO	0x00	reg_a_l_train_max_for_rd_dq0[6:0] The max pass point of the rx delay line for A_DQ0.

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Bit	Attr	Reset Value	Description
23	RO	0x0	reserved
22:16	RO	0x00	reg_a_l_train_max_for_rd_dq1[6:0] The max pass point of the rx delay line for A_DQ1.
15	RO	0x0	reserved
14:8	RO	0x00	reg_a_l_train_max_for_rd_dq2[6:0] The max pass point of the rx delay line for A_DQ2.
7	RO	0x0	reserved
6:0	RO	0x00	reg_a_l_train_max_for_rd_dq3[6:0] The max pass point of the rx delay line for A_DQ3.

DDRPHY_BYTE_REG_0x25

Address: **Operational Base** + offset (0x0094)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RO	0x00	reg_a_l_train_max_for_rd_dq4[6:0] The max pass point of the rx delay line for A_DQ4.
23	RO	0x0	reserved
22:16	RO	0x00	reg_a_l_train_max_for_rd_dq5[6:0] The max pass point of the rx delay line for A_DQ5.
15	RO	0x0	reserved
14:8	RO	0x00	reg_a_l_train_max_for_rd_dq6[6:0] The max pass point of the rx delay line for A_DQ6.
7	RO	0x0	reserved
6:0	RO	0x00	reg_a_l_train_max_for_rd_dq7[6:0] The max pass point of the rx delay line for A_DQ7.

DDRPHY_BYTE_REG_0x26

Address: **Operational Base** + offset (0x0098)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:8	RO	0x00	reg_a_l_train_max_for_rd_dm[6:0] The max pass point of the rx delay line for A_DM0, only for lp4.
7	RO	0x0	reserved
6:0	RO	0x00	reg_a_l_train_max_for_rd_dqs[6:0] The max pass point of the rx delay line for A_DQS0/A_DQSB0.

DDRPHY_BYTE_REG_0x27

Address: **Operational Base** + offset (0x009C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:18	RO	0x00	reg_a_l_train_result_for_rd_base_dqs[6:0] The best point of the rx delay line for A_DQS0/A_DQSB0 after the read training.
17:6	RO	0x000	reserved
5	RO	0x0	reg_a_l_change_rd_dqs_default The flag that can't find the pass window of the read training for byte0. Active High.
4	RO	0x0	reserved
3	RO	0x0	reg_a_l_left_boundary_overflow_for_rd The flag that the dqs rx delay line has arrived the max value when do the read training of byte0.
2:1	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
0	RO	0x0	reg_a_l_right_boundary_overflow_for_rd The flag that the dqs rx delay line has arrived the min value when do the read training of byte0.

DDRPHY_BYTE_REG_0x28

Address: **Operational Base** + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reg_a_l_rd_train_readback_data_dq0[15:0] The low 8bit of the read back data of the read training for A_DQ0. Used for LPDDR4 read training bypass mode. The high 8bit of the read back data of the read training for A_DQ0. Used for LPDDR4 read training bypass mode.
15:0	RO	0x0000	reg_a_l_rd_train_readback_data_dq1[15:0] The low 8bit of the read back data of the read training for A_DQ1. Used for LPDDR4 read training bypass mode. The high 8bit of the read back data of the read training for A_DQ1. Used for LPDDR4 read training bypass mode.

DDRPHY_BYTE_REG_0x29

Address: **Operational Base** + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reg_a_l_rd_train_readback_data_dq2[15:0] The low 8bit of the read back data of the read training for A_DQ2. Used for LPDDR4 read training bypass mode. The high 8bit of the read back data of the read training for A_DQ2. Used for LPDDR4 read training bypass mode.
15:0	RO	0x0000	reg_a_l_rd_train_readback_data_dq3[15:0] The low 8bit of the read back data of the read training for A_DQ3. Used for LPDDR4 read training bypass mode. The high 8bit of the read back data of the read training for A_DQ3. Used for LPDDR4 read training bypass mode.

DDRPHY_BYTE_REG_0x2a

Address: **Operational Base** + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reg_a_l_rd_train_readback_data_dq4[15:0] The low 8bit of the read back data of the read training for A_DQ4. Used for LPDDR4 read training bypass mode. The high 8bit of the read back data of the read training for A_DQ4. Used for LPDDR4 read training bypass mode.
15:0	RO	0x0000	reg_a_l_rd_train_readback_data_dq5[15:0] The low 8bit of the read back data of the read training for A_DQ5. Used for LPDDR4 read training bypass mode. The high 8bit of the read back data of the read training for A_DQ5. Used for LPDDR4 read training bypass mode.

DDRPHY_BYTE_REG_0x2b

Address: **Operational Base** + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reg_a_l_rd_train_readback_data_dq6[15:0] The low 8bit of the read back data of the read training for A_DQ6. Used for LPDDR4 read training bypass mode. The high 8bit of the read back data of the read training for A_DQ6. Used for LPDDR4 read training bypass mode.

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Bit	Attr	Reset Value	Description
15:0	RO	0x0000	reg_a_l_rd_train_readback_data_dq7[15:0] The low 8bit of the read back data of the read training for A_DQ7. Used for LPDDR4 read training bypass mode. The high 8bit of the read back data of the read training for A_DQ7. Used for LPDDR4 read training bypass mode.

DDRPHY_BYTE_REG_0x2c

Address: **Operational Base** + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RO	0x0	reg_a_l_change_dqs_default The flag that can't find the pass window of the dq after scan all the tx delay line of the DQ for byte0. When this signal change to high after the write training, it means that the current dqs is not in the good point
15:8	RO	0x00	reg_a_l_train_min_for_dm[7:0] The min pass point of the tx delay line for A_DM0.
7:0	RO	0x00	reg_a_l_train_min_for_dqs[7:0] The min pass point of the tx delay line for A_DQS0/A_DQSB0.

DDRPHY_BYTE_REG_0x2d

Address: **Operational Base** + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reg_a_l_train_min_for_dq0[7:0] The min pass point of the tx delay line for A_DQ0.
23:16	RO	0x00	reg_a_l_train_min_for_dq1[7:0] The min pass point of the tx delay line for A_DQ1.
15:8	RO	0x00	reg_a_l_train_min_for_dq2[7:0] The min pass point of the tx delay line for A_DQ2.
7:0	RO	0x00	reg_a_l_train_min_for_dq3[7:0] The min pass point of the tx delay line for A_DQ3.

DDRPHY_BYTE_REG_0x2e

Address: **Operational Base** + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reg_a_l_train_min_for_dq4[7:0] The min pass point of the tx delay line for A_DQ4.
23:16	RO	0x00	reg_a_l_train_min_for_dq5[7:0] The min pass point of the tx delay line for A_DQ5.
15:8	RO	0x00	reg_a_l_train_min_for_dq6[7:0] The min pass point of the tx delay line for A_DQ6.
7:0	RO	0x00	reg_a_l_train_min_for_dq7[7:0] The min pass point of the tx delay line for A_DQ7.

DDRPHY_BYTE_REG_0x2f

Address: **Operational Base** + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RO	0x00	reg_a_l_train_max_for_dm[7:0] The max pass point of the tx delay line for A_DM0
7:0	RO	0x00	reg_a_l_train_max_for_dqs[7:0] The max pass point of the tx delay line for A_DQS0/A_DQSB0.

DDRPHY_BYTE_REG_0x30

Address: **Operational Base** + offset (0x00C0)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	reg_a_l_train_max_for_dq0[7:0] The max pass point of the tx delay line for A_DQ0.
23:16	RO	0x00	reg_a_l_train_max_for_dq1[7:0] The max pass point of the tx delay line for A_DQ1.
15:8	RO	0x00	reg_a_l_train_max_for_dq2[7:0] The max pass point of the tx delay line for A_DQ2.
7:0	RO	0x00	reg_a_l_train_max_for_dq3[7:0] The max pass point of the tx delay line for A_DQ3.

DDRPHY_BYTE_REG_0x31

Address: **Operational Base** + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reg_a_l_train_max_for_dq4[7:0] The max pass point of the tx delay line for A_DQ4.
23:16	RO	0x00	reg_a_l_train_max_for_dq5[7:0] The max pass point of the tx delay line for A_DQ5.
15:8	RO	0x00	reg_a_l_train_max_for_dq6[7:0] The max pass point of the tx delay line for A_DQ6.
7:0	RO	0x00	reg_a_l_train_max_for_dq7[7:0] The max pass point of the tx delay line for A_DQ7.

DDRPHY_BYTE_REG_0x32

Address: **Operational Base** + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RO	0x000	reg_a_l_rdtrain_vref_max[8:0] [7:0]The max pass pint of the rx vref of byte0. [8]The bit8 of the max pass point for the rd vref of byte0.
15:9	RO	0x00	reserved
8:0	RO	0x000	reg_a_l_rdtrain_vref_min[8:0] [7:0]]The min pass pint of the rx vref of byte0. [8]The bit8 of the min pass point for the rd vref of byte0.

DDRPHY_BYTE_REG_0x40

Address: **Operational Base** + offset (0x0100)

Bit	Attr	Reset Value	Description
31:24	RW	0x80	reg_a_l_cs2_dq0_invdelaysel The register used to control the tx delay line of the A_DQ0 for RANK2.
23:16	RW	0x80	reg_a_l_cs2_dq1_invdelaysel The register used to control the tx delay line of the A_DQ1 for RANK2.
15:8	RW	0x80	reg_a_l_cs2_dq2_invdelaysel The register used to control the tx delay line of the A_DQ2 for RANK2.
7:0	RW	0x80	reg_a_l_cs2_dq3_invdelaysel The register used to control the tx delay line of the A_DQ3 for RANK2.

DDRPHY_BYTE_REG_0x41

Address: **Operational Base** + offset (0x0104)

Bit	Attr	Reset Value	Description
31:24	RW	0x80	reg_a_l_cs2_dq4_invdelaysel The register used to control the tx delay line of the A_DQ4 for RANK2.

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Bit	Attr	Reset Value	Description
23:16	RW	0x80	reg_a_l_cs2_dq5_invdelaysel The register used to control the tx delay line of the A_DQ5 for RANK2.
15:8	RW	0x80	reg_a_l_cs2_dq6_invdelaysel The register used to control the tx delay line of the A_DQ6 for RANK2.
7:0	RW	0x80	reg_a_l_cs2_dq7_invdelaysel The register used to control the tx delay line of the A_DQ7 for RANK2.

DDRPHY_BYTE_REG_0x42

Address: **Operational Base** + offset (0x0108)

Bit	Attr	Reset Value	Description
31:24	RW	0x80	reg_a_l_cs2_dqs_invdelaysel The register used to control the tx delay line of the A_DQS0 for RANK2.
23:16	RO	0x00	reserved
15:8	RW	0x80	reg_a_l_cs2_dqsb_invdelaysel The register used to control the tx delay line of the A_DQSB0 for RANK2.
7:0	RO	0x00	reserved

DDRPHY_BYTE_REG_0x43

Address: **Operational Base** + offset (0x010C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28:24	RW	0x00	reg_a_l_cs2_loop_invdelaysel The register used to choose the obs signal to check delay line control of the byte0 for RANK2. 5'd0: Choose to the current value to control the rx delay line of A_DQ0 for RANK2. 5'd1: Choose to the current value to control the rx delay line of A_DQ1 for RANK2. 5'd2: Choose to the current value to control the rx delay line of A_DQ2 for RANK2. 5'd3: Choose to the current value to control the rx delay line of A_DQ3 for RANK2. 5'd4: Choose to the current value to control the rx delay line of A_DQ4 for RANK2. 5'd5: Choose to the current value to control the rx delay line of A_DQ5 for RANK2. 5'd6: Choose to the current value to control the rx delay line of A_DQ6 for RANK2. 5'd7: Choose to the current value to control the rx delay line of A_DQ7 for RANK2. 5'd8: Choose to the current value to control the rx delay line of A_DM0 for RANK2. 5'd9: Choose to the current value to control the rx delay line of A_DQS0 for RANK2. 5'd10: Choose to the current value to control the rx delay line of A_DQSB0 for RANK2. 5'd16: Choose to the current value to control the tx delay line of A_DQ0 for RANK2. 5'd17: Choose to the current value to control the tx delay line of A_DQ1 for RANK2. 5'd18: Choose to the current value to control the tx delay line of A_DQ2 for RANK2. 5'd19: Choose to the current value to control the tx delay line of A_DQ3 for RANK2. 5'd20: Choose to the current value to control the tx delay line of A_DQ4 for RANK2. 5'd21: Choose to the current value to control the tx delay line of A_DQ5 for RANK2. 5'd22: Choose to the current value to control the tx delay line of A_DQ6 for RANK2. 5'd23: Choose to the current value to control the tx delay line of A_DQ7 for RANK2. 5'd24: Choose to the current value to control the tx delay line of A_DM0 for RANK2. 5'd25 Choose to the current value to control the tx delay line of A_DQS0 for RANK2. 5'd26: Choose to the current value to control the tx delay line of A_DQSB0 for RANK2.
23:16	RO	0x00	reserved
15:8	RW	0x80	reg_a_l_cs2_dm_invdelaysel The register used to control the tx delay line of the A_DM0 for RANK2.
7	RO	0x0	reserved
6:0	RW	0x00	reg_a_l_cs2_dm_invdelayselrx The register used to control the rx delay line of the A_DM0 for RANK2.

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DDRPHY_BYTE_REG_0x44

Address: **Operational Base** + offset (0x0110)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	reg_a_l_cs2_dq0_invdelayselrx The register used to control the rx delay line of the A_DQ0 for RANK2.
23	RO	0x0	reserved
22:16	RW	0x00	reg_a_l_cs2_dq1_invdelayselrx The register used to control the rx delay line of the A_DQ1 for RANK2.
15	RO	0x0	reserved
14:8	RW	0x00	reg_a_l_cs2_dq2_invdelayselrx The register used to control the rx delay line of the A_DQ2 for RANK2.
7	RO	0x0	reserved
6:0	RW	0x00	reg_a_l_cs2_dq3_invdelayselrx The register used to control the rx delay line of the A_DQ3 for RANK2.

DDRPHY_BYTE_REG_0x45

Address: **Operational Base** + offset (0x0114)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	reg_a_l_cs2_dq4_invdelayselrx The register used to control the rx delay line of the A_DQ4 for RANK2.
23	RO	0x0	reserved
22:16	RW	0x00	reg_a_l_cs2_dq5_invdelayselrx The register used to control the rx delay line of the A_DQ5 for RANK2.
15	RO	0x0	reserved
14:8	RW	0x00	reg_a_l_cs2_dq6_invdelayselrx The register used to control the rx delay line of the A_DQ6 for RANK2.
7	RO	0x0	reserved
6:0	RW	0x00	reg_a_l_cs2_dq7_invdelayselrx The register used to control the rx delay line of the A_DQ7 for RANK2.

DDRPHY_BYTE_REG_0x46

Address: **Operational Base** + offset (0x0118)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x1f	reg_a_l_cs2_dqs_invdelayselrx The register used to control the rx delay line of the A_DQS0 for RANK2.
23:15	RO	0x000	reserved
14:8	RW	0x1f	reg_a_l_cs2_dqsb_invdelayselrx The register used to control the rx delay line of the A_DQSB0 for RANK2.
7:0	RO	0x00	reserved

DDRPHY_BYTE_REG_0x47

Address: **Operational Base** + offset (0x011C)

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Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x80	reg_a_l_cs3_dm_invdelaysel The register used to control the tx delay line of the A_DM0 for RANK3.

DDRPHY_BYTE_REG_0x48

Address: **Operational Base** + offset (0x0120)

Bit	Attr	Reset Value	Description
31:24	RW	0x80	reg_a_l_cs3_dq0_invdelaysel The register used to control the tx delay line of the A_DQ0 for RANK3.
23:16	RW	0x80	reg_a_l_cs3_dq1_invdelaysel The register used to control the tx delay line of the A_DQ1 for RANK3.
15:8	RW	0x80	reg_a_l_cs3_dq2_invdelaysel The register used to control the tx delay line of the A_DQ2 for RANK3.
7:0	RW	0x80	reg_a_l_cs3_dq3_invdelaysel The register used to control the tx delay line of the A_DQ3 for RANK3.

DDRPHY_BYTE_REG_0x49

Address: **Operational Base** + offset (0x0124)

Bit	Attr	Reset Value	Description
31:24	RW	0x80	reg_a_l_cs3_dq4_invdelaysel The register used to control the tx delay line of the A_DQ4 for RANK3.
23:16	RW	0x80	reg_a_l_cs3_dq5_invdelaysel The register used to control the tx delay line of the A_DQ5 for RANK3.
15:8	RW	0x80	reg_a_l_cs3_dq6_invdelaysel The register used to control the tx delay line of the A_DQ6 for RANK3.
7:0	RW	0x80	reg_a_l_cs3_dq7_invdelaysel The register used to control the tx delay line of the A_DQ7 for RANK3.

DDRPHY_BYTE_REG_0x4a

Address: **Operational Base** + offset (0x0128)

Bit	Attr	Reset Value	Description
31:24	RW	0x80	reg_a_l_cs3_dqs_invdelaysel The register used to control the tx delay line of the A_DQS0 for RANK3.
23:16	RO	0x00	reserved
15:8	RW	0x80	reg_a_l_cs3_dqsb_invdelaysel The register used to control the tx delay line of the A_DQSB0 for RANK3.
7:0	RO	0x00	reserved

DDRPHY_BYTE_REG_0x4b

Address: **Operational Base** + offset (0x012C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28:24	RW	0x00	reg_a_l_cs3_loop_invdelaysel The register used to choose the obs signal to check delay line control of the byte0 for RANK3. 5'd0: Choose to the current value to control the tx delay line of A_DQ0 for RANK3. 5'd1: Choose to the current value to control the tx delay line of A_DQ1 for RANK3. 5'd2: Choose to the current value to control the tx delay line of A_DQ2 for RANK3. 5'd3: Choose to the current value to control the tx delay line of A_DQ3 for RANK3. 5'd4: Choose to the current value to control the tx delay line of A_DQ4 for RANK3. 5'd5: Choose to the current value to control the tx delay line of A_DQ5 for RANK3. 5'd6: Choose to the current value to control the tx delay line of A_DQ6 for RANK3. 5'd7: Choose to the current value to control the tx delay line of A_DQ7 for RANK3. 5'd8: Choose to the current value to control the tx delay line of A_DM0 for RANK3. 5'd9: Choose to the current value to control the tx delay line of A_DQS0 for RANK3. 5'd10: Choose to the current value to control the tx delay line of A_DQSB0 for RANK3. 5'd16: Choose to the current value to control the rx delay line of A_DQ0 for RANK3. 5'd17: Choose to the current value to control the rx delay line of A_DQ1 for RANK3. 5'd18: Choose to the current value to control the rx delay line of A_DQ2 for RANK3. 5'd19: Choose to the current value to control the rx delay line of A_DQ3 for RANK3. 5'd20: Choose to the current value to control the rx delay line of A_DQ4 for RANK3. 5'd21: Choose to the current value to control the rx delay line of A_DQ5 for RANK3. 5'd22: Choose to the current value to control the rx delay line of A_DQ6 for RANK3. 5'd23: Choose to the current value to control the rx delay line of A_DQ7 for RANK3. 5'd24: Choose to the current value to control the rx delay line of A_DM0 for RANK3. 5'd25 Choose to the current value to control the rx delay line of A_DQS0 for RANK3. 5'd26: Choose to the current value to control the rx delay line of A_DQSB0 for RANK3.
23:15	RO	0x000	reserved
14:8	RW	0x00	reg_a_l_cs3_dm_invdelayselrx The register used to control the rx delay line of the A_DM0 for RANK3.
7:0	RO	0x00	reserved

DDRPHY_BYTE_REG_0x4c

Address: **Operational Base** + offset (0x0130)

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Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	reg_a_l_cs3_dq0_invdelayselrx The register used to control the rx delay line of the A_DQ0 for RANK3.
23	RO	0x0	reserved
22:16	RW	0x00	reg_a_l_cs3_dq1_invdelayselrx The register used to control the rx delay line of the A_DQ1 for RANK3.
15	RO	0x0	reserved
14:8	RW	0x00	reg_a_l_cs3_dq2_invdelayselrx The register used to control the rx delay line of the A_DQ2 for RANK3.
7	RO	0x0	reserved
6:0	RW	0x00	reg_a_l_cs3_dq3_invdelayselrx The register used to control the rx delay line of the A_DQ3 for RANK3.

DDRPHY_BYTE_REG_0x4d

Address: **Operational Base** + offset (0x0134)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	reg_a_l_cs3_dq4_invdelayselrx The register used to control the rx delay line of the A_DQ4 for RANK3.
23	RO	0x0	reserved
22:16	RW	0x00	reg_a_l_cs3_dq5_invdelayselrx The register used to control the rx delay line of the A_DQ5 for RANK3.
15	RO	0x0	reserved
14:8	RW	0x00	reg_a_l_cs3_dq6_invdelayselrx The register used to control the rx delay line of the A_DQ6 for RANK3.
7	RO	0x0	reserved
6:0	RW	0x00	reg_a_l_cs3_dq7_invdelayselrx The register used to control the rx delay line of the A_DQ7 for RANK3.

DDRPHY_BYTE_REG_0x4e

Address: **Operational Base** + offset (0x0138)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x1f	reg_a_l_cs3_dqs_invdelayselrx The register used to control the rx delay line of the A_DQS0 for RANK3.
23:15	RO	0x000	reserved
14:8	RW	0x1f	reg_a_l_cs3_dqsb_invdelayselrx The register used to control the rx delay line of the A_DQSB0 for RANK3.
7:0	RO	0x00	reserved

DDRPHY_BYTE_REG_0x4f

Address: **Operational Base** + offset (0x013C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
26:24	RW	0x1	reg_a_l_rxmen2_delay_bp The register used to control the 1x delay of the rx dqs calibration delay for byte0 of RANK2 when enable the rx dqs calibration bypass mode at the posedge of setting reg_calib_freq_update to 1'b1. Unit = 4UI.
23:21	RW	0x7	reg_a_l_rxmen2_ophsel_bp The register used to control the 0.5*4x delay of the rx dqs calibration delay for byte 0 of RANK2 when enable the rx dqs calibration bypass mode at the posedge of setting reg_calib_freq_update to 1'b1. Unit = 0.5UI.
20:16	RW	0x08	reg_a_l_rxmen2_sdlltap_bp The register used to control the delay line of the rx dqs calibration delay for byte 0 of RANK2 when enable the rx dqs calibration bypass mode at the posedge of setting reg_calib_freq_update to 1'b1. Unit = 4UI/256.
15:11	RO	0x00	reserved
10:8	RW	0x1	reg_a_l_rxmen3_delay_bp The register used to control the 1x delay of the rx dqs calibration delay for byte0 of RANK3 when enable the rx dqs calibration bypass mode at the posedge of setting reg_calib_freq_update to 1'b1. Unit = 4UI
7:5	RW	0x7	reg_a_l_rxmen3_ophsel_bp The register used to control the 0.5*4x delay of the rx dqs calibration delay for byte 0 of RANK3 when enable the rx dqs calibration bypass mode at the posedge of setting reg_calib_freq_update to 1'b1. Unit = 0.5UI.
4:0	RW	0x08	reg_a_l_rxmen3_sdlltap_bp The register used to control the delay line of the rx dqs calibration delay for byte 0 of RANK3 when enable the rx dqs calibration bypass mode at the posedge of setting reg_calib_freq_update to 1'b1. Unit = 4UI/256.

DDRPHY_BYTE_REG_0x50

Address: **Operational Base** + offset (0x0140)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:24	RW	0x2	reg_a_l_rdodt2_delay The register used to control the 0.5*4x delay of the rx odt delay for byte 0 of RANK2 when enable the rx odt bypass mode by setting reg_rdodt_bypass to 1'b1. Unit = 0.5UI.
23:21	RW	0x4	reg_a_l_rdodt2_ophsel The register used to control the delay line of the rx odt delay for byte 0 of RANK2 when enable the rx odt bypass mode by setting reg_rdodt_bypass to 1'b1. Unit = 4UI/256.

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Bit	Attr	Reset Value	Description
20:16	RW	0x04	reg_a_l_rdodt2_dllsel The register used to control the 1x delay of the rx odt delay for byte0 of RANK2 when enable the rx odt bypass mode by setting reg_rdodt_bypass to 1'b1. Unit = 4UI.
15:11	RO	0x00	reserved
10:8	RW	0x2	reg_a_l_rdodt3_delay The register used to control the 0.5*4x delay of the rx odt delay for byte 0 of RANK3 when enable the rx odt bypass mode by setting reg_rdodt_bypass to 1'b1. Unit = 0.5*UI.
7:5	RW	0x4	reg_a_l_rdodt3_ophsel The register used to control the delay line of the rx odt delay for byte 0 of RANK3 when enable the rx odt bypass mode by setting reg_rdodt_bypass to 1'b1. Unit = 4UI/256.
4:0	RW	0x04	reg_a_l_rdodt3_dllsel The register used to control the 1x delay of the rx odt delay for byte0 of RANK3 when enable the rx odt bypass mode by setting reg_rdodt_bypass to 1'b1. Unit = UI.

DDRPHY_BYTE_REG_0x51

Address: **Operational Base** + offset (0x0144)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:13	RW	0x1	reg_a_l_rrankdly_1x_cs2 The register used to conrol the delay of the read rank switch signal of the byte0 for RANK2. Unit= dfi_clk1x.(reg_rdrank_delay_bp = 1)
12:10	RW	0x1	reg_a_l_rrankdly_1x_cs3 The register used to conrol the delay of the read rank switch signal of the byte0 for RANK3. Unit= dfi_clk1x.(reg_rdrank_delay_bp = 1)
9:6	RO	0x0	reserved
5:3	RW	0x0	reg_a_l_rrankdly_4x_cs2 The register used to conrol the delay of the read rank switch signal of the byte0 for RANK2. Unit= 0.5UI.(reg_rdrank_delay_bp = 1)
2:0	RW	0x0	reg_a_l_rrankdly_4x_cs3 The register used to conrol the delay of the read rank switch signal of the byte0 for RANK3. Unit= 0.5UI.(reg_rdrank_delay_bp = 1)

DDRPHY_BYTE_REG_0x52

Address: **Operational Base** + offset (0x0148)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
26:16	RO	0x000	reg_a_l_calib_result_cs2[10:0] The current delay of the rx dqs calibration of byte0 for RANK2. The user can using this register to get the current working state of the rx dqs calibration. [4:0]: Means the tx delay line value of the rx dqs calibration. [7:5]: Means the 0.5UI delay value of the rx dqs calibration. [10:8]:The current 4UI delay of the rx dqs calibration of the byte0 for RANK2.The user can using this register to get the current working state of the rx dqs calibration.
15:11	RO	0x00	reserved
10:0	RO	0x000	reg_a_l_calib_result_cs3[10:0] The current delay of the rx dqs calibration of byte0 for RANK3. The user can using this register to get the current working state of the rx dqs calibration. [4:0]: Means the tx delay line value of the rx dqs calibration. [7:5]: Means the 0.5UI delay value of the rx dqs calibration. [10:8]:The current 4UI delay of the rx dqs calibration of the byte0 for RANK3.The user can using this register to get the current working state of the rx dqs calibration.

DDRPHY_BYTE_REG_0x53

Address: **Operational Base** + offset (0x014C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	reg_a_l_tdqs_invdelaysel2[7:0] The write-leveling result of byte0 for RANK2. The user can get the write-leveling result after the write-leveling training compelte.
15:8	RO	0x00	reserved
7:0	RO	0x00	reg_a_l_tdqs_invdelaysel3[7:0] The write-leveling result of byte0 for RANK3. The user can get the write-leveling result after the write-leveling training compelte.

DDRPHY_BYTE_REG_0x54

Address: **Operational Base** + offset (0x0150)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	reg_a_l_cs2_value_dqx_invdelaysel[7:0] The delay line value of the current obs signal choosing of reg_cs2_a_l_loop_invdelaysel.

DDRPHY_BYTE_REG_0x55

Address: **Operational Base** + offset (0x0154)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	reg_a_l_cs3_value_dqx_invdelaysel[7:0] The delay line value of the current obs signal choosing of reg_cs3_a_l_loop_invdelaysel.

DDRPHY_BYTE_REG_0x56

Address: **Operational Base** + offset (0x0158)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	reg_a_l_abutnrcomp4_dqs_reg
27	RW	0x1	reg_a_l_abutnrcomp3_dqs_reg
26	RW	0x1	reg_a_l_abutnrcomp2_dqs_reg

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Bit	Attr	Reset Value	Description
25	RW	0x1	reg_a_l_abutnrcomp1_dqs_reg
24	RW	0x0	reg_a_l_abutnrcomp0_dqs_reg
23:21	RO	0x0	reserved
20	RW	0x0	reg_a_l_abutprcomp4_dqs_reg
19	RW	0x1	reg_a_l_abutprcomp3_dqs_reg
18	RW	0x1	reg_a_l_abutprcomp2_dqs_reg
17	RW	0x1	reg_a_l_abutprcomp1_dqs_reg
16	RW	0x0	reg_a_l_abutprcomp0_dqs_reg
15:13	RO	0x0	reserved
12	RW	0x0	reg_a_l_abutodtpd4_dqs_reg
11	RW	0x0	reg_a_l_abutodtpd3_dqs_reg
10	RW	0x1	reg_a_l_abutodtpd2_dqs_reg
9	RW	0x0	reg_a_l_abutodtpd1_dqs_reg
8	RW	0x1	reg_a_l_abutodtpd0_dqs_reg
7:5	RO	0x0	reserved
4	RW	0x0	reg_a_l_abutodtpu4_dqs_reg
3	RW	0x0	reg_a_l_abutodtpu3_dqs_reg
2	RW	0x1	reg_a_l_abutodtpu2_dqs_reg
1	RW	0x0	reg_a_l_abutodtpu1_dqs_reg
0	RW	0x1	reg_a_l_abutodtpu0_dqs_reg

13.4.6 Registers Summary for DDRMON

Name	Offset	Size	Reset Value	Description
DDRMON_IP_VERSION	0x0000	W	0x00000030	DDR Monitor IP Version
DDRMON_CTRL	0x0004	W	0x00000008	DDR Monitor Control Register
DDRMON_INT_STATUS	0x0008	W	0x00000000	Interrupt Status
DDRMON_DDRC_IDLE_CNT_NUM	0x000C	W	0x00000000	DDRC IDLE time
DDRMON_TIMER_COUNT	0x0010	W	0x00000000	The DFI Timer Threshold
DDRMON_FLOOR_NUMBER	0x0014	W	0x00000000	The Low Threshold in the Comparison of DDR Access
DDRMON_TOP_NUMBER	0x0018	W	0x00000000	The High Threshold in the Comparison of DDR Access
DDRMON_COUNT_NUM	0x0028	W	0x00000000	Timer Count Number
DDRMON_DFI_ACCESS_NUM	0x002C	W	0x00000000	DFI Read and Write Command Number
DDRMON_TOP_LP_NUMBER	0x0030	W	0x00000000	The High Threshold in The Comparison Of DDR Cke Low
DDRMON_FLOOR_LP_NUMBER	0x0034	W	0x00000000	The Low Threshold in The Comparison Of DDR Cke Low
DDRMON_DFI_SREX_NUM	0x0038	W	0x00000000	Number Of DFI Self-refresh cycles
DDRMON_DFI_PDEX_NUM	0x003C	W	0x00000000	Number Of DFI Power Down cycles
DDRMON_DFI_CLKSTOP_NUM	0x0040	W	0x00000000	Number Of DFI Clkstop cycles
DDRMON_DFI_SRPDEX_NUM	0x0044	W	0x00000000	Number Of DFI SRPD cycles
DDRMON_DFI_DSMEX_NUM	0x0048	W	0x00000000	Number Of DFI DSM cycles

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Name	Offset	Size	Reset Value	Description
DDRMON_DFI_LP_NUM	0x004C	W	0x00000000	Total Number DFI low power cycles
DDRMON_DFI_PHY_LP_CTRL_NUM	0x0050	W	0x00000000	DDR Phy Low Power
DDRMON_DFI_PHY_LP_DATA_NUM	0x0054	W	0x00000000	DDR Phy Low Power
DDRMON_INT_MASK0	0x0058	W	0x00000000	Interrupt mask control
DDRMON_INT_MASK1	0x005C	W	0x00000000	Interrupt mask control
DDRMON_CS_CTRL	0x0060	W	0x00000000	
DDRMON_PER_BANK_ACT_NUM	0x0100	W	0x00000000	Per-bank Active Number
DDRMON_PER_BANK_RD_NUM	0x0104	W	0x00000000	Per-bank Read Number
DDRMON_PER_BANK_WR_NUM	0x0108	W	0x00000000	Per-bank Write Number
DDRMON_PER_BANK_RD_WR_PER_ACT_MAX_NUM	0x010C	W	0x00000000	Per-bank Read-Write Per-Active Max Number
DDRMON_PER_BANK_SERIES_RD_BURST_MAX_NUM	0x0110	W	0x00000000	Per-bank Series Read Burst Max Number
DDRMON_PER_BANK_SERIES_RD_BURST_TIMES_NUM	0x0114	W	0x00000000	Per-bank Series Read Burst Times Number
DDRMON_PER_BANK_SERIES_WR_BURST_MAX_NUM	0x0118	W	0x00000000	Per-bank Series Write Burst Max Number
DDRMON_PER_BANK_SERIES_WR_BURST_TIMES_NUM	0x011C	W	0x00000000	Per-bank Series Write Burst Times Number
DDRMON_PER_BANK_RD2RD_PAGE_HIT_NUM	0x0120	W	0x00000000	Per-bank Read to Read Page-hit Number
DDRMON_PER_BANK_WR2WR_PAGE_HIT_NUM	0x0124	W	0x00000000	Per-bank Write to Write Page Hit Number
DDRMON_PER_BANK_RD2WR_PAGE_HIT_NUM	0x0128	W	0x00000000	Per-bank Read to Write Page Hit Number
DDRMON_PER_BANK_WR2RD_PAGE_HIT_NUM	0x012C	W	0x00000000	Per-bank Write To Write Page Hit Number
DDRMON_PER_BANK_RD2RD_PAGE_MISS_NUM	0x0130	W	0x00000000	Per-bank Read To Read Page Miss Number
DDRMON_PER_BANK_WR2WR_PAGE_MISS_NUM	0x0134	W	0x00000000	Per-bank Write To Write Page Miss Number
DDRMON_PER_BANK_RD2WR_PAGE_MISS_NUM	0x0138	W	0x00000000	Per-bank Read To Write Page Miss Number
DDRMON_PER_BANK_WR2RD_PAGE_MISS_NUM	0x013C	W	0x00000000	Per-bank Write To Read Page Miss Number
DDRMON_ALL_BANK_ACT_NUM	0x0140	W	0x00000000	All-bank Active Command Number
DDRMON_ALL_BANK_WR_NUM	0x0144	W	0x00000000	All-bank Write Command Number
DDRMON_ALL_BANK_RD_NUM	0x0148	W	0x00000000	All-bank Read Command Number
DDRMON_ALL_BANK_ACT_ACT_NUM	0x014C	W	0x00000000	All-bank Active To Active Number

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Name	Offset	Size	Reset Value	Description
DDRMON_ALL_BANK_ACT_PRE_NUM	0x0150	W	0x00000000	All-bank Active Precharge Number
DDRMON_ALL_BANK_ACT_RDWR_SAME_NUM	0x0154	W	0x00000000	All-bank Active Read-Write Same Number
DDRMON_ALL_BANK_PRE_ACT_NUM	0x0158	W	0x00000000	All-bank Precharge To Active Number
DDRMON_ALL_BANK_RDWR_PRE_SAME_NUM	0x015C	W	0x00000000	All-bank Read-Write Precharge Same Number
DDRMON_ALL_BANK_RD2WR_NUM	0x0160	W	0x00000000	All-bank Read To Write Number
DDRMON_ALL_BANK_WR2RD_NUM	0x0164	W	0x00000000	All-bank Write To Read Number
DDRMON_ALL_BANK_SERIES_RD_TOTAL_CNT_NUM	0x0168	W	0x00000000	All-bank Series Read Total Count Number
DDRMON_ALL_BANK_SERIES_WR_TOTAL_CNT_NUM	0x016C	W	0x00000000	All-bank Series Write Total Count Number
DDRMON_ALL_BANK_SERIES_RD_BURST_MAX_NUM	0x0170	W	0x00000000	All-bank Series Read Burst Max Number
DDRMON_ALL_BANK_SERIES_RD_BURST_TIMES_NUM	0x0174	W	0x00000000	All-bank Series Read Burst Times Number
DDRMON_ALL_BANK_SERIES_WR_BURST_MAX_NUM	0x0178	W	0x00000000	All-bank Series Write Burst Max Number
DDRMON_ALL_BANK_SERIES_WR_BURST_TIMES_NUM	0x017C	W	0x00000000	All-bank Series Write Burst Times Number
DDRMON_ALL_BANK_TCCDMW_CNT_NUM	0x0180	W	0x00000000	All-bank TCCDMW Count Number
DDRMON_ALL_BANK_TCCD_L_CNT_NUM	0x0184	W	0x00000000	All-bank TCCD_L Count Number
DDRMON_IF_CTRL	0x0200	W	0x00000000	DDR Interface Control Register
DDRMON_MSTID	0x0204	W	0x00000000	Master and AXI ID Of DDR Command
DDRMON_IDMSK	0x0208	W	0x00000000	Master and AXI ID MASK Of DDR Command
DDRMON_WR_START_ADDR	0x020C	W	0x00000000	Write Start Address
DDRMON_WR_END_ADDR	0x0210	W	0x00000000	Write End Address
DDRMON_RD_START_ADDR	0x0214	W	0x00000000	Read Start Address
DDRMON_RD_END_ADDR	0x0218	W	0x00000000	Read End Address
DDRMON_FIFO0_ADDR	0x0240	W	0x00000000	DDR Controller Interface Address FIFO0
DDRMON_FIFO0_ID	0x0244	W	0x00000000	DDR Controller Interface Command ID FIFO0
DDRMON_FIFO1_ADDR	0x0248	W	0x00000000	DDR Controller Interface Address FIFO1
DDRMON_FIFO1_ID	0x024C	W	0x00000000	DDR Controller Interface Command ID FIFO1
DDRMON_FIFO2_ADDR	0x0250	W	0x00000000	DDR Controller Interface Address FIFO2

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Name	Offset	Size	Reset Value	Description
DDRMON_FIFO2_ID	0x0254	W	0x00000000	DDR Controller Interface Command ID FIFO2
DDRMON_FIFO3_ADDR	0x0258	W	0x00000000	DDR Controller Interface Address FIFO3
DDRMON_FIFO3_ID	0x025C	W	0x00000000	DDR Controller Interface Command ID FIFO3

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

13.4.7 Detail Registers Description

DDRMON_IP_VERSION

Address: Operational Base(0xFF4C0000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x30	ip_version DDR monitor IP version

DDRMON_CTRL

Address: Operational Base(0xFF4C0000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable When bit 16=1, bit 0 can be written by softwar. When bit 16=0, bit 0 cannot be written by software. When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software. ..... When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software.
15	RW	0x0	ddr3_en 1'b1: Enable 1'b0: Disable
14:11	RW	0x0	hot_bank to define which bank is currently monitored for per-bank statistics for ddr3/ddr4/lpddr2/lpddr3/lpddr4, bit[13:11] is used to support 8 bank
10:7	RW	0x0	hot_rank to define which rank is currently monitored for per-bank statistics 4'b0001: rank 0 4'b0010: rank 1 4'b0100: rank 2 4'b1000: rank 3 Other value is forbbiden
6	RO	0x0	reserved
5	RW	0x0	ddr4_en 1'b1: Enable 1'b0: Disable
4	RW	0x0	lpddr4_en 1'b1: Enable 1'b0: Disable
3	RW	0x1	hardware_en 1'b1: Enable 1'b0: Disable
2	RW	0x0	lpddr23_en 1'b1: Enable 1'b0: Disable

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Bit	Attr	Reset Value	Description
1	RW	0x0	software_en 1'b1: Enable 1'b0: Disable
0	RW	0x0	timer_cnt_en 1'b1: Enable 1'b0: Disable

DDRMON_INT_STATUS

Address: Operational Base(0xFF4C0000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	RW	0x0	rd_addr_hit This is the interrupt status read address hit the setting range.
17	RW	0x0	wr_addr_hit This is the interrupt status write address hit the setting range.
16	RW	0x0	over_int_srpdex This is the interrupt status of DDR SRPD over than high threshold. Only for LPDDR4/LPDDR5
15	RW	0x0	bellow_int_srpdex This is the interrupt status of DDR SRPD less than low threshold. Only for LPDDR4/LPDDR5
14	RO	0x0	over_int_dsmex This is the interrupt status of DDR deep sleep over than high threshold. Only for LPDDR5
13	RO	0x0	bellow_int_dsmex This is the interrupt status of DDR deep sleep less than low threshold. Only for LPDDR5
12	RO	0x0	over_int_phy_lp_ctrl This is the interrupt status of DDR low power ctrl interface onver than high threshold.
11	RO	0x0	bellow_int_phy_lp_ctrl This is the interrupt status of DDR low power ctrl interface less than low threshold.
10	RO	0x0	over_int_phy_lp_data This is the interrupt status of DDR low power data interface onver than high threshold.
9	RO	0x0	below_int_phy_lp_data This is the interrupt status of DDR low power data interface less than low threshold.
8	RW	0x0	over_int_clkstop This is the interrupt status of DDR clk stop number over than high threshold. Only valid for lpddr4/lpddr5.
7	RW	0x0	below_int_clkstop This is the interrupt status of DDR clk stop number less than low threshold. Only valid for lpddr4/lpddr5.
6	RO	0x0	over_int_pdex This is the interrupt status of DDR power down number over than high threshold.
5	RO	0x0	below_int_pdex This is the interrupt status of DDR power down number less than low threshold.
4	RW	0x0	compare_statistics This is the interrupt status to statistics the number of activate, write or read command and so on.

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Bit	Attr	Reset Value	Description
3	RW	0x0	over_int_srex This is the interrupt status of DDR self refresh number over than high threshold.
2	RW	0x0	below_int_srex This is the interrupt status of DDR self refresh number less than low threshold.
1	RO	0x0	over_int This is the interrupt status of DDR read and write burst number more than high threshold.
0	RO	0x0	below_int This is the interrupt status of DDR read and write burst number less than low threshold.

DDRMON_DDRC_IDLE_CNT_NUM

Address: Operational Base(0xFF4C0000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ddrc_idle_cnt_number The DDRC idle time, which is calculated by DFI clock

DDRMON_TIMER_COUNT

Address: Operational Base(0xFF4C0000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	timer_count The timer counter threshold, the statistics of DDR access only be done when timer counter is less then this threshold in hardware mode, in OSC clock cycle.

DDRMON_FLOOR_NUMBER

Address: Operational Base(0xFF4C0000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	floor_number The low threshold in the comparison of DDR access.

DDRMON_TOP_NUMBER

Address: Operational Base(0xFF4C0000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	top_number The high threshold in the comparison of DDR access.

DDRMON_COUNT_NUM

Address: Operational Base(0xFF4C0000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_count_num The DFI counter number in the statistics range, in DDR clock cycle.

DDRMON_DFI_ACCESS_NUM

Address: Operational Base(0xFF4C0000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_access_num DFI read and write command number in the statistics range.

DDRMON_TOP_LP_NUMBER

Address: Operational Base(0xFF4C0000) + offset (0x0030)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	top_lp_number The high threshold in the comparison of DDR self-refresh, power down or clkstop.

DDRMON_FLOOR_LP_NUMBER

Address: Operational Base(0xFF4C0000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	floor_lp_number The low threshold in the comparison of DDR self-refresh, power down or clkstop.

DDRMON_DFI_SREX_NUM

Address: Operational Base(0xFF4C0000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_srex_num DFI self-refresh number during cke low.

DDRMON_DFI_PDEX_NUM

Address: Operational Base(0xFF4C0000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_pdex_num DFI power down number during cke low.

DDRMON_DFI_CLKSTOP_NUM

Address: Operational Base(0xFF4C0000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_clkstop_num DFI clkstop number during cke low. Only valid for lpddr2/3/4.

DDRMON_DFI_SRPDEX_NUM

Address: Operational Base(0xFF4C0000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_srpdex_num DFI SRPD number during cke low. Only valid for lpddr4/5.

DDRMON_DFI_DSMEX_NUM

Address: Operational Base(0xFF4C0000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_dsmex_num DFI Deep Sleep Mode number during cke low. Only valid for lpddr5.

DDRMON_DFI_LP_NUM

Address: Operational Base(0xFF4C0000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_lp_num The sum of DFI self-refresh, power down, clock stop, self-refresh-pd and dsm cycles

DDRMON_DFI_PHY_LP_CTRL_NUM

Address: Operational Base(0xFF4C0000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dfi_phy_lp_ctrl_num Phy low power count number during the time both dfi_lp_ctrl_req and dfi_lp_ctrl_ack assert.

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DDRMON_DFI_PHY_LP_DATA_NUM

Address: Operational Base(0xFF4C0000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dfi_phy_lp_data_num Phy low power count number during the time both dfi_lp_data_req and dfi_lp_data_ack assert.

DDRMON_INT_MASK0

Address: Operational Base(0xFF4C0000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable When bit 16=1, bit 0 can be written by softwar. When bit 16=0, bit 0 cannot be written by software. When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software. ..... When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software.
15	RW	0x0	bellow_int_srpdex Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
14	RW	0x0	over_int_dsmex Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
13	RW	0x0	bellow_int_dsmex Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
12	RW	0x0	over_int_phy_lp_ctrl Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
11	RW	0x0	bellow_int_phy_lp_ctrl Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
10	RW	0x0	over_int_phy_lp_data_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
9	RW	0x0	below_int_phy_lp_data_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
8	RW	0x0	over_int_clkstop_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
7	RW	0x0	below_int_clkstop_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
6	RO	0x0	over_int_pdex_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
5	RO	0x0	below_int_pdex_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
4	RW	0x0	compare_statistics_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.

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Bit	Attr	Reset Value	Description
3	RW	0x0	over_int_srex_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
2	RW	0x0	below_int_srex_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
1	RW	0x0	over_int_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
0	RW	0x0	below_int_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.

DDRMON_INT_MASK1

Address: Operational Base(0xFF4C0000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	WO	0x0	write_enable When bit 16=1, bit 0 can be written by softwar. When bit 16=0, bit 0 cannot be written by software. When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software. ..... When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software.
15:2	RO	0x0000	reserved
1	RW	0x0	rd_addr_hit_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.
0	RW	0x0	wr_addr_hit_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable.

DDRMON_CS_CTRL

Address: Operational Base(0xFF4C0000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	rank_cs_num define active rank number

DDRMON_PER_BANK_ACT_NUM

Address: Operational Base(0xFF4C0000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	per_bank_act_number Active command number for per bank statistics

DDRMON_PER_BANK_RD_NUM

Address: Operational Base(0xFF4C0000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	per_bank_rd_number Read command number for per bank statistics

DDRMON_PER_BANK_WR_NUM

Address: Operational Base(0xFF4C0000) + offset (0x0108)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	per_bank_wr_number Write command number for per bank statistics

DDRMON_PER_BANK_RD_WR_PER_ACT_MAX_NUM

Address: Operational Base(0xFF4C0000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	per_bank_rd_wr_per_act_max_number Per_bank_rd_wr_per_act_max_number number for per bank statistics Count the max read or write command in every ACT to PRE period.

DDRMON_PER_BANK_SERIES_RD_BURST_MAX_NUM

Address: Operational Base(0xFF4C0000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	per_bank_series_rd_burst_max_number per_bank_series_rd_burst_max_number number for per bank statistics

DDRMON_PER_BANK_SERIES_RD_BURST_TIMES_NUM

Address: Operational Base(0xFF4C0000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	per_bank_series_rd_burst_times_number per_bank_series_rd_burst_times_number number for per bank statistics

DDRMON_PER_BANK_SERIES_WR_BURST_MAX_NUM

Address: Operational Base(0xFF4C0000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	per_bank_series_wr_burst_max_number per_bank_series_wr_burst_max_number number for per bank statistics

DDRMON_PER_BANK_SERIES_WR_BURST_TIMES_NUM

Address: Operational Base(0xFF4C0000) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	per_bank_series_wr_burst_times_number per_bank_series_wr_burst_times_number number for per bank statistics

DDRMON_PER_BANK_RD2RD_PAGE_HIT_NUM

Address: Operational Base(0xFF4C0000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	per_rank_rd2rd_page_hit_number per_rank_rd2rd_page_hit_number for per bank statistics

DDRMON_PER_BANK_WR2WR_PAGE_HIT_NUM

Address: Operational Base(0xFF4C0000) + offset (0x0124)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	per_rank_wr2wr_page_hit_number per_rank_wr2wr_page_hit_number for per bank statistics

DDRMON_PER_BANK_RD2WR_PAGE_HIT_NUM

Address: Operational Base(0xFF4C0000) + offset (0x0128)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	per_rank_rd2wr_page_hit_number per_rank_rd2wr_page_hit_number for per bank statistics

DDRMON_PER_BANK_WR2RD_PAGE_HIT_NUM

Address: Operational Base(0xFF4C0000) + offset (0x012C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	per_rank_wr2rd_page_hit_number per_rank_wr2rd_page_hit_number for per bank statistics

DDRMON_PER_BANK_RD2RD_PAGE_MISS_NUM

Address: Operational Base(0xFF4C0000) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	per_rank_rd2rd_page_miss_number per_rank_rd2rd_page_miss_number for per bank statistics

DDRMON_PER_BANK_WR2WR_PAGE_MISS_NUM

Address: Operational Base(0xFF4C0000) + offset (0x0134)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	per_rank_wr2wr_page_miss_number per_rank_wr2wr_page_miss_number for per bank statistics

DDRMON_PER_BANK_RD2WR_PAGE_MISS_NUM

Address: Operational Base(0xFF4C0000) + offset (0x0138)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	per_rank_rd2wr_page_miss_number per_rank_rd2wr_page_miss_number for per bank statistics

DDRMON_PER_BANK_WR2RD_PAGE_MISS_NUM

Address: Operational Base(0xFF4C0000) + offset (0x013C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	per_rank_wr2rd_page_miss_number per_rank_wr2rd_page_miss_number for per bank statistics

DDRMON_ALL_BANK_ACT_NUM

Address: Operational Base(0xFF4C0000) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_act_num DFI active command number in the statistics range.

DDRMON_ALL_BANK_WR_NUM

Address: Operational Base(0xFF4C0000) + offset (0x0144)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_wr_num DFI write command number in the statistics range.

DDRMON_ALL_BANK_RD_NUM

Address: Operational Base(0xFF4C0000) + offset (0x0148)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_rd_num DFI read command number in the statistics range.

DDRMON_ALL_BANK_ACT_ACT_NUM

Address: Operational Base(0xFF4C0000) + offset (0x014C)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	all_bank_act_act_number all_rank_act_act_number for all bank statistics

DDRMON_ALL_BANK_ACT_PRE_NUM

Address: Operational Base(0xFF4C0000) + offset (0x0150)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	all_bank_act_pre_number all_rank_act_pre_number for all bank statistics

DDRMON_ALL_BANK_ACT_RDWR_SAME_NUM

Address: Operational Base(0xFF4C0000) + offset (0x0154)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	all_bank_act_rdwr_same_number all_rank_act_rdwr_same_number for all bank statistics

DDRMON_ALL_BANK_PRE_ACT_NUM

Address: Operational Base(0xFF4C0000) + offset (0x0158)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	all_bank_pre_act_number all_rank_pre_act_number for all bank statistics

DDRMON_ALL_BANK_RDWR_PRE_SAME_NUM

Address: Operational Base(0xFF4C0000) + offset (0x015C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	all_bank_rdwr_pre_same_number all_rank_rdwr_pre_same_number for all bank statistics

DDRMON_ALL_BANK_RD2WR_NUM

Address: Operational Base(0xFF4C0000) + offset (0x0160)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	all_bank_rd2wr_number all_rank_rd2wr_number for all bank statistics

DDRMON_ALL_BANK_WR2RD_NUM

Address: Operational Base(0xFF4C0000) + offset (0x0164)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	all_bank_rd2wr_number all_rank_wr2rd_number for all bank statistics

DDRMON_ALL_BANK_SERIES_RD_TOTAL_CNT_NUM

Address: Operational Base(0xFF4C0000) + offset (0x0168)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	all_bank_series_rd_total_cnt_number all_bank_series_rd_total_cnt_number for all bank statistics

DDRMON_ALL_BANK_SERIES_WR_TOTAL_CNT_NUM

Address: Operational Base(0xFF4C0000) + offset (0x016C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	all_bank_series_wr_total_cnt_number all_bank_series_wr_total_cnt_number for all bank statistics

DDRMON_ALL_BANK_SERIES_RD_BURST_MAX_NUM

Address: Operational Base(0xFF4C0000) + offset (0x0170)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	all_bank_series_rd_burst_max_number all_bank_series_rd_burst_max_number for all bank statistics

DDRMON_ALL_BANK_SERIES_RD_BURST_TIMES_NUM

Address: Operational Base(0xFF4C0000) + offset (0x0174)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	all_bank_series_rd_burst_times_number all_bank_series_rd_burst_times_number for all bank statistics

DDRMON_ALL_BANK_SERIES_WR_BURST_MAX_NUM

Address: Operational Base(0xFF4C0000) + offset (0x0178)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	all_bank_series_wr_burst_max_number all_bank_series_wr_burst_max_number for all bank statistics

DDRMON_ALL_BANK_SERIES_WR_BURST_TIMES_NUM

Address: Operational Base(0xFF4C0000) + offset (0x017C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	all_bank_series_wr_burst_times_number all_bank_series_wr_burst_times_number for all bank statistics

DDRMON_ALL_BANK_TCCDMW_CNT_NUM

Address: Operational Base(0xFF4C0000) + offset (0x0180)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	all_bank_tccdmw_cnt_number all_bank_tccdmw_cnt_number for all bank statistics

DDRMON_ALL_BANK_TCCD_L_CNT_NUM

Address: Operational Base(0xFF4C0000) + offset (0x0184)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	all_bank_tccd_l_cnt_number all_bank_tccd_l_cnt_number for all bank statistics

DDRMON_IF_CTRL

Address: Operational Base(0xFF4C0000) + offset (0x0200)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable When bit 16=1, bit 0 can be written by software. When bit 16=0, bit 0 cannot be written by software. When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software. ..... When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software.
15:3	RO	0x0000	reserved
2	RW	0x0	if_mon_en 1'b1: Enable 1'b0: Disable
1	RO	0x0	reserved
0	RW	0x0	direction 1'b1: Read 1'b0: Write

DDRMON_MSTID

Address: Operational Base(0xFF4C0000) + offset (0x0204)

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Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RW	0x00000	ddr_mstid High 7 bits: Master ID Low 10 bits: AXI command ID

DDRMON_IDMSK

Address: Operational Base(0xFF4C0000) + offset (0x0208)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RW	0x00000	ddr_idmsk When bit set to high, this bit of MSTID will be masked, and does not take part in the ID comparison.

DDRMON_WR_START_ADDR

Address: Operational Base(0xFF4C0000) + offset (0x020C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wr_start_addr Write start address for address comparison.

DDRMON_WR_END_ADDR

Address: Operational Base(0xFF4C0000) + offset (0x0210)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wr_end_addr Write end address for address comparison.

DDRMON_RD_START_ADDR

Address: Operational Base(0xFF4C0000) + offset (0x0214)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rd_start_addr Read start address for address comparison.

DDRMON_RD_END_ADDR

Address: Operational Base(0xFF4C0000) + offset (0x0218)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rd_end_addr Read end address for address comparison.

DDRMON_FIFO0_ADDR

Address: Operational Base(0xFF4C0000) + offset (0x0240)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ddr_fifo0_addr DDR controller interface address FIFO0.

DDRMON_FIFO0_ID

Address: Operational Base(0xFF4C0000) + offset (0x0244)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RO	0x00000	ddr_fifo0_id DDR controller interface command ID FIFO0.

DDRMON_FIFO1_ADDR

Address: Operational Base(0xFF4C0000) + offset (0x0248)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ddr_fifo1_addr DDR controller interface address FIFO1.

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DDRMON_FIFO1_ID

Address: Operational Base(0xFF4C0000) + offset (0x024C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RO	0x00000	ddr_fifo1_id DDR controller interface command ID FIFO1.

DDRMON_FIFO2_ADDR

Address: Operational Base(0xFF4C0000) + offset (0x0250)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ddr_fifo2_addr DDR controller interface address FIFO2.

DDRMON_FIFO2_ID

Address: Operational Base(0xFF4C0000) + offset (0x0254)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RO	0x00000	ddr_fifo2_id DDR controller interface command ID FIFO2.

DDRMON_FIFO3_ADDR

Address: Operational Base(0xFF4C0000) + offset (0x0258)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ddr_fifo3_addr DDR controller interface address FIFO3.

DDRMON_FIFO3_ID

Address: Operational Base(0xFF4C0000) + offset (0x025C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RO	0x00000	ddr_fifo3_id DDR controller interface command ID FIFO3.

13.4.8 Registers Summary for HWLP

Name	Offset	Size	Reset Value	Description
DDR_HWLP_CTRL0	0x0000	W	0x00000000	DDR Hardware Low Power Control Register0
DDR_HWLP_CTRL1	0x0004	W	0x00000000	DDR Hardware Low Power Control Register1
DDR_HWLP_CTRL2	0x0008	W	0x00000000	DDR Hardware Low Power Control Register2
DDR_HWLP_STATUS0	0x0020	W	0x00000000	DDR Hardware Low Power Status Register
DDR_HWLP_VER	0x0040	W	0x00000100	DDR Hardware Low Power Version Register

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

13.4.9 Detail Registers Description

DDR_HWLP_CTRL0

Address: Operational Base(0xFF4D8000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
9	RW	0x0	hwlp_msch_active_exit_en 1'b0: DDRC/AXI doesn't exit low power state when msch_active==1'b1. 1'b1: DDRC/AXI exits low power state when msch_active==1'b1.
8	RW	0x0	hwlp_msch_active_enter_en 1'b0: DDRC is allowed to enter self-refresh mode when msch_active==1'b1. 1'b1: DDRC is not allowed to enter self-refresh mode when msch_active==1'b1.
7:4	RO	0x0	reserved
3	RW	0x0	hwlp_cg_en_ddrphy Enable gating DDR PHY clocks when current_st_ddrc==3'b100. 1'b0: keep DDR PHY clocks 1'b1: Gating DDR PHY clocks
2	RW	0x0	hwlp_cg_en_msch Enable gating memory schedule clocks when DDRC is in self-refresh state. 1'b0: keep memory schedule clocks 1'b1: Gating memory schedule clocks
1	RW	0x0	hwlp_cg_en_axi Hardware low power enable signal for AXI bus. 1'b0: Disable 1'b1: Enable
0	RW	0x0	hwlp_cg_en_ddrc Hardware low power enable signal for DDRC. 1'b0: Disable 1'b1: Enable DDRC are able to enter hardware low power mode only when hwlp_cg_en_axi==1'b1.

DDR_HWLP_CTRL1

Address: Operational Base(0xFF4D8000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	silent_threshold_axi Under the condition that current_st_axi==3'b000 and AXI hardware low power mode is enabled, when the AXI bus remains idle for (silent_threshold_axi+1) cycles, AXI bus will be requested to enter low-power state.
15:0	RW	0x0000	silent_threshold_ddrc Controls the waiting time from AXI entering low-power state to requesting the DDRC to enter self-refresh mode. The waiting time is equal to silent_threshold_ddrc +1.

DDR_HWLP_CTRL2

Address: Operational Base(0xFF4D8000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	exit_threshold_ret Controls the waiting time from requesting the PHY to exit low-power mode to requesting the DDR to exit self-refresh mode The waiting time is equal to exit_threshold_ret +1.

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	enter_threshold_ret When trying to put DDR PHY to enter low power mode, controls the waiting time between asserting dfi_init_start and deasserting bufferen_core. The waiting time is equal to enter_threshold_ret +1.

DDR_HWLP_STATUS0

Address: Operational Base(0xFF4D8000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:3	RO	0x0	current_st_axi The current state of the state machine in the Hardware Low Power module that controls the AXI low-power interface. 3'b000: The state machine is in idle state, while axi bus may be busy. 3'b001: Request AXI to enter low power mode 3'b010: AXI is in low power mode 3'b100: Request AXI to exit low power mode
2:0	RW	0x0	current_st_ddrc The current state of the state machine in the Hardware Low Power module that controls the DDRC low-power interface. 3'b000: The state machine is in idle state, while DDRC may be busy. 3'b001: DDRC is trying to enter self-refresh mode. 3'b010: DDR PHY is trying to enter low power mode, with bufferen_core set to 0. 3'b011: DDR PHY is trying to enter low power mode, with dfi_init_start set to 1. 3'b100: DDRC is in self-refresh mode. 3'b101: DDR PHY is trying to exit low power mode. 3'b110: DDR PHY exit low power mode. 3'b111: DDRC exit self-refresh mode.

DDR_HWLP_VER

Address: Operational Base(0xFF4D8000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000100	version The version information of Hardware Low Power module, the current version number is 0x00000100.

13.5 Interface Description

DDR IOs from DDR PHY are listed as following Table.

Table 13-2 DDR IO description

Pin Name	Description
CK	Positive differential clock
CKB	Negative differential clock
CKE	Active-high clock enable signal for two chip select.
CSBi (i=0,1)	Active-low chip select signal. There are two chip select.
ACTN	Activation command input.
BA[1:0] BG[1:0]	Bank address signal. For DDR3, BA0 should connect to the BA0.

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	BA1 should connect to BA1. BG0 should connect to BA2. For DDR4, please connect directly. Unused for LPDDRn.
A[17:0]	Address signal.
DQ[31:0]	Bidirectional data line
DQS[3:0]	Positive differential bidirectional data strobes
DQSB[3:0]	Negative differential bidirectional data strobes.
DM[3:0]	Active-low data mask signal.
ODTi (i=0,1)	On-Die Termination output signal for two chip select.
RESETN	Reset signal.

The DDR PHY supports more than one SDRAM type and the command pad of DDR PHY is named in the format of DDR4. The PHY supports different command map for different SDRAM type and also supports to use the register to control the map between the commands, and then the user can be very conveniently to design the Combo Memory System based on the different command map function. The default command map relationship shows in the following table. When the user uses the mem_select_t[2:0](REG0[6:4])to choose the memory type, the command will change to the default command map. The user should accord to the following table to connectthe command pad to the SDRAM pad.

Table 13-3 DDR IO Mapping Table

CMD PAD OF PHY (DDR4)	DDR3	LPDDR3	LPDDR3 4RANK	LPDDR4	LPDDR4 4rank
A0	A9	-	-	CKB_B	CKB_2
A1	A2	-	-	-	-
A2	A4	A6	A6	CA1_A	CA1_A
A3	A3	-	-	CKE1_A	CKE2
A4	BA1	-	CSB3	CA3_B	CA3_B
A5	A11	-	-	CA5_B	CA5_B
A6	A14	A1	A1	CA1_B	CA1_B
A7	A8	ODT1	ODT1	ODT0_B	ODT0_B
A8	A7	A9	A9	ODT0_A	ODT0_A
A9	A13	-	-	CK_B	CK_2
A10	A10	CSB0	CSB0	CKE0_B	CKE1
A11	A6	A8	A8	CA0_A	CA0_A
A12	BA0	-	-	CA3_A	CA3_A
A13	A5	A0	A0	CA0_B	CA0_B
A14	A15	-	-	CA4_A	CA4_A
A15	A0	A7	A7	CA2_A	CA2_A
A16	RASB	-	CSB2	CA5_A	CA5_A
A17	-	-	-	-	-
ACTN	CASB	CSB1	CSB1	CKE1_B	CKE3
BA0	A1	A3	A3	CA2_B	CA2_B
BA1	A12	-	-	CA4_B	CA4_B
BG0	WEN	-	ODT2	ODT1_B	ODT2_B
BG1	BA2	-	ODT3	ODT1_A	ODT2_A
CKE	CKE	CKE	CKE	CKE0_A	CKE0
CKB	CKB	CKB	CKB	CK_A	CKB_0
CK	CK	CK	CK	CKB_A	CK_0
CSB0	ODT1	ODT0	ODT0	CSB0_A	CSB0
CSB1	CSB1	A5	A5	CSB1_A	CSB2
ODT0	ODT0	A4	A4	CSB1_B	CSB3
ODT1	CSB0	A2	A2	CSB0_B	CSB1
RESETN	RESETN	-	-	RESETN	RESETN

At the PHY top-level, the mapping relationships between the DQ pads and dfi_wrdata/dfi_rddata shows in the following table. When connecting a DDR3/DDR4/LPDDR3 memory to the interface, there is a default mapping between the DDR3/DDR4/LPDDR3 signals to the PHY top-level pins.

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Table 13-4 Default DDR DQ IO Mapping Table for DDR3/DDR4/LPDDR3/LPDDR4

PHY TOP-LEVEL PINS	SDRAM	dfi_wrdata/dfi_rddata
A_DQ[7:0]	DQ[7:0]	dfi_wrdata[7:0]/dfi_rddata[7:0]
A_DQ[15:8]	DQ[15:8]	dfi_wrdata[15:8]/dfi_rddata[15:8]
B_DQ[7:0]	DQ[15:8]	dfi_wrdata[23:16]/dfi_rddata[23:16]
B_DQ[15:8]	DQ[31:24]	dfi_wrdata[31:24]/dfi_rddata[31:24]

RK3562 support a remap feature from DFI DQ byte to SDRAM DQ byte. By default, DRAM DQ0 maps to DFI DQ0, DRAM DQ1 maps to DFI DQ1, and so on. If software wants to map DRAM DQ0 with DFI DQ1, and DRAM DQ1 map to DFI DQ2, DRAM DQ2 maps to DFI DQ3 and DRAM DQ3 map to DFI DQ0, it should configure DDR_GRF_CON3 before DRAM access.

Table 13-5 Example DDR DQ IO <-> DFI Remapping

PHY TOP-LEVEL PINS	GRF	dfi_wrdata/dfi_rddata
A_DQ[7:0]	grf_ddr_con3[9:8]=1	dfi_wrdata[15:8]/dfi_rddata[15:8]
A_DQ[15:8]	grf_ddr_con3[11:10]=2	dfi_wrdata[23:16]/dfi_rddata[23:16]
B_DQ[23:16]	grf_ddr_con3[13:12]=3	dfi_wrdata[31:24]/dfi_rddata[31:24]
B_DQ[31:24]	grf_ddr_con3[15:14]=0	dfi_wrdata[7:0]/dfi_rddata[7:0]

13.6 Application Notes

13.6.1 Initialization

1. UMCTL2 & DDR PHY Initialization

1. Assert the resets (presetn, core_ddrc_rstn and aresetn_0 of UMCTL2)
2. Configure PLL of DDR PHY and wait PLL lock.
3. De-assert presetn if clocks are active and stable.
4. Initial UMCTL2 register and PHY Register
5. Start PHY initialization with DFIMISC[5] register of UMCTL2
6. De-assert the remaining resets (core_ddrc_rstn and aresetn_0 of UMCTL2)
7. Wait UMCTL2 initialization done (STAT.operation_mode==normal)
8. Start PHY dqs calibrationwith PHYREG2 register and wait calibration finish with PHY REG91 register.
9. (Optional) After dqs calibration, start write leveling training with PHYREG2 register and wait write leveling training finish with PHY REG92 register.
10. Start to write and read

2. DDR3/DDR3L Initialization Sequence

The initialization steps for DDR3/DDR3L SDRAMs are as follows:

1. Power-up.
2. Maintain dfi_reset_n low for duration specified by INIT1.dram_rstn_x1024. Specification requires atleast 200 us with stable power.
3. Issue NOP/deselect for duration specified by INIT0.pre_cke_x1024. Specification requires at least 500us.
4. Assert CKE and issue NOP/deselect for INIT0.post_cke_x1024 (specification requires at least tXPR).
5. Issue MRS (mode register set) command to load MR2 with INIT4.emr2 value followed byNOP/deselect for duration of DRAMTMG3.t_mrd.
6. Issue MRS command to load MR3 with INIT4.emr3 followed by NOP/deselect for duration ofDRAMTMG3.t_mrd.
7. Issue MRS command to load MR1 with INIT4.emr followed by NOP/deselect for duration ofDRAMTMG3.t_mrd.
8. Issue MRS command to load MR0 with INIT3.mr followed by NOP/deselect for duration ofDRAMTMG3.t_mod.
9. Issue ZQCL command to start ZQ calibration and wait for INIT5.dev_zqinit_x32.
10. Wait for INIT5.dev_zqinit_x32 counting to finish. Ensure wait from step 8 is larger than tDLLK.
11. The UMCTL2 controller is now ready for normal operation.

3. DDR4 Initialization Sequence

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The initialization steps for DDR4 SDRAMs are as follows:
1. Power-up.
2. Maintain dfi_reset_n low for duration specified by INIT1.dram_rstn_x1024. Specification requires atleast 200 us with stable power.
3. Issue NOP/deselect for duration specified by INIT0.pre_cke_x1024. Specification requires at least 500 us.
4. Assert CKE and issue NOP/deselect for INIT0.post_cke_x1024 (specification requires at least tXPR).
5. Issue MRS (mode register set) command to load MR3 with INIT4.emr3 value followed by NOP/deselect for duration of DRAMTMG3.t_mrd.
6. Issue MRS (mode register set) command to load MR6 with INIT7.mr6 value followed byNOP/deselect for duration of DRAMTMG3.t_mrd.
7. Issue MRS (mode register set) command to load MR5 with INIT6.mr5 value followed by NOP/deselect for duration of DRAMTMG3.t_mrd.
8. Issue MRS (mode register set) command to load MR4 with INIT7.mr4 value followed by NOP/deselect for duration of DRAMTMG3.t_mrd.
9. Issue MRS command to load MR2 with INIT4.emr2 followed by NOP/deselect for duration of DRAMTMG3.t_mrd.
10. Issue MRS command to load MR1 with INIT4.emr followed by NOP/deselect for duration of DRAMTMG3.t_mrd.
11. Issue MRS command to load MR0 with INIT3.mr followed by NOP/deselect for duration of DRAMTMG3.t_mod.
12. Issue ZQCL command to start ZQ calibration and wait for INIT5.dev_zqinit_x32.
13. Wait for INIT5.dev_zqinit_x32 counting to finish. Ensure wait from step 8 is larger than tDLLK.
14. The UMCTL2 controller is now ready for normal operation.

4. LPDDR3 Initialization Sequence

The initialization steps for LPDDR3 SDRAMs are as follows:
1. Power-up.
2. CKE is held low for a duration specified by INIT0.pre_cke_x1024. The clock is checked to be stable forduration specified by INIT2.min_stable_clock_x1 (minimum of 5 clock cycles) prior to the first low tohigh transition of CKE.
3. Assert CKE for INIT0.post_cke_x1024 (specification requires at least 200 us).
4. A MRW (Reset) command is issued to MRW63 register. Values of MA<7:0> = 3FH and OP<7:0> =00H is used for this command. The MRW reset command brings the device to the device autoinitialization (resetting) state in the power-on initialization sequence.
5. Issue NOP/deselect for duration specified by INIT2.idle_after_reset_x32 (specification requires 1 usminimum) and INIT5.max_auto_init_x1024 (specification requires maximum time of 10 us).
6. An MRW ZQ initialization calibration command is issued to the memory to register MR10 to initiatethe ZQ calibration. Values of MA<7:0> = 0AH and OP<7:0>= FFH is used for this command.
7. Issue NOP/deselect for duration specified by INIT5.dev_zqinit_x32 (specification requires aminimum time of 1us).
8. Program MR2 register by setting MR2 register to INIT3.emr followed by a NOP/deselect for aduration specified by DRAMTMG3.t_mrw (typical value of 5 clock cycles).
9. Program MR1 register by setting MR1 register to INIT3.mr followed by a NOP/deselect for aduration specified by DRAMTMG3.t_mrw (typical value of 5 clock cycles).
10. Program MR3 register by setting MR3 register to INIT4.emr2 followed by a NOP/deselect for aduration specified by DRAMTMG3.t_mrw (typical value of 5 clock cycles).
11. Schedule multiple all bank refresh.
12. The UMCTL2 controller is now ready for normal operation.

5. LPDDR4 Initialization Sequence

The initialization steps for LPDDR4 SDRAMs are as follows:
1. Power-up.
2. Maintain dfi_reset_n and dfi_reset_n_ref low for duration specified by INIT1.dram_rstn_x1024.Specification requires at least 200 us with stable power.

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3. Issue NOP/deselect for duration specified by INIT0.pre_cke_x1024. Specification requires at least 2ms.
4. Assert CKE and issue NOP/deselect for INIT0.post_cke_x1024. Specification requires at least 2 us.
5. Issue MRS (mode register set) command to load MR13 with INIT4.emr3 value followed by
NOP/deselect for duration of DRAMTMG3.t_mrw.
6. Issue MRS (mode register set) command to load MR1 with INIT3.mr value followed by NOP/deselect for duration of DRAMTMG3.t_mrw.
7. Issue MRS (mode register set) command to load MR2 with INIT3.emr value followed by NOP/deselect for duration of DRAMTMG3.t_mrw.
8. Issue MRS (mode register set) command to load MR3 with INIT4.emr2 value followed by NOP/deselect for duration of DRAMTMG3.t_mrd.
9. Issue ZQCal Start command and wait for ZQCTL0.t_zq_long_nop.
10. Issue ZQCal Latch command and wait for ZQCTL0.t_zq_short_nop.
11. Schedule multiple refresh.
12. The UMCTL2 controller is now ready for normal operation.

13.6.2 High Speed IO Drive Strength

The register related to the CMD IO drive strength shows in the following table.

Table 13-6 Related register of the DATA IO drive strength

ADDR	RW	NAME	BITS	DEF	DESCRIPTIONS
0xf4	RW	reg_cmd_abutnrcomp_reg	[28:24]	5'b01110	The pull-down resistance of CMD except CK. The resistance relation with the configuration show in table " Drive Strength and ODT Resistance table”
	RW	reg_cmd_abutprcomp_reg	[20:16]	5'b01110	The pull-up resistance of CMD except CK. The resistance relation with the configuration show in table " Drive Strength and ODT Resistance table”
	RW	reg_cmd_abutnrcomp_ck0_reg	[12:8]	5'b01110	The pull-down resistance of CK and CKB. The resistance relation with the configuration show in table " Drive Strength and ODT Resistance table”
	RW	reg_cmd_abutprcomp_ck0_reg	[4:0]	5'b01110	The pull-up resistance of CK and CKB. The resistance relation with the configuration show in table " Drive Strength and ODT Resistance table”

The register related to the DATA IO drive strength shows in the following table.

Table 13-7 Related register of the DATA IO drive strength

ADDR	RW	NAME	BITS	DEF	DESCRIPTIONS
0x404	RW	reg_a_l_abutnrcompdq_reg	[28:24]	5’b01110	pull-down driving resistance for A_DQ[7:0]. The resistance relation with the configuration show in table " Drive Strength and ODT Resistance

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ADDR	RW	NAME	BITS	DEF	DESCRIPTIONS
					table”
		reg_a_l_abutprcompdq_reg	[20:16]	5’b01110	pull-up driving resistance for A_DQ[7:0]. The resistance relation with the configuration show in table " Drive Strength and ODT Resistance table”
		reg_a_l_abutodtpddq_reg	[12:8]	5’b00101	pull-down ODT resistance for A_DQ[7:0]. The resistance relation with the configuration show in table " Drive Strength and ODT Resistance table "
		reg_a_l_abutodtpudq_reg	[4:0]	5’b00101	pull-up ODT resistance for A_DQ[7:0]. The resistance relation with the configuration show in table " Drive Strength and ODT Resistance table "
0x604	RW	reg_a_h_abutnrcompdq_reg	[28:24]	5’b01110	pull-down driving resistance for A_DQ[15:8]. The resistance relation with the configuration show in table " Drive Strength and ODT Resistance table "
		reg_a_h_abutprcompdq_reg	[20:16]	5’b01110	pull-up driving resistance for A_DQ[15:8]. The resistance relation with the configuration show in table " Drive Strength and ODT Resistance table "
		reg_a_h_abutodtpddq_reg	[12:8]	5’b00101	pull-down ODT resistance for A_DQ[15:8]. The resistance relation with the configuration show in table " Drive Strength and ODT Resistance table "
		reg_a_h_abutodtpudq_reg	[4:0]	5’b00101	pull-up ODT resistance for A_DQ[15:8]. The resistance relation with the configuration show in table “Drive Strength and ODT Resistance table”
0x804	RW	reg_b_l_abutnrcompdq_reg	[28:24]	5’b01110	pull-down driving resistance for B_DQ[7:0]. The resistance relation with the configuration show in table " Drive Strength and ODT Resistance table "
		reg_b_l_abutprcompdq_reg	[20:16]	5’b01110	pull-up driving resistance for B_DQ[7:0]. The resistance relation with the configuration show in table " Drive Strength and ODT Resistance table "

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ADDR	RW	NAME	BITS	DEF	DESCRIPTIONS
		reg_b_l_abutodtpddq_reg	[12:8]	5’b00101	pull-down ODT resistance for B_DQ[7:0]. The resistance relation with the configuration show in table " Drive Strength and ODT Resistance table "
		reg_b_l_abutodtpudq_reg	[4:0]	5’b00101	pull-up ODT resistance for B_DQ[7:0]. The resistance relation with the configuration show in table " Drive Strength and ODT Resistance table "
0xa04	RW	reg_b_h_abutnrcompdq_reg	[28:24]	5’b01110	pull-down driving resistance for B_DQ[15:8]. The resistance relation with the configuration show in table " Drive Strength and ODT Resistance table "
		reg_b_h_abutprcompdq_reg	[20:16]	5’b01110	pull-up driving resistance for B_DQ[15:8]. The resistance relation with the configuration show in table " Drive Strength and ODT Resistance table "
		reg_b_h_abutodtpddq_reg	[12:8]	5’b00101	pull-down ODT resistance for B_DQ[15:8]. The resistance relation with the configuration show in table " Drive Strength and ODT Resistance table "
		reg_b_h_abutodtpudq_reg	[4:0]	5’b00101	pull-up ODT resistance for B_DQ[15:8]. The resistance relation with the configuration show in table " Drive Strength and ODT Resistance table "

Table 13-8 DDR4 Drive Strength and ODT Resistance table

Control bit	5'b11111	5'b11110	5'b11101	5'b11100	units
pull-up	22.08	23.09	24.19	25.4	ohm
pull-down	20.75	21.69	22.72	23.86	ohm
Control bit	5'b11011	5'b11010	5'b11001	5'b11000	units
pull-up	26.73	28.22	29.88	31.74	ohm
pull-down	25.12	26.51	28.07	29.83	ohm
Control bit	5'b10111	5'b10110	5'b10101	5'b10100	units
pull-up	33.86	36.28	39.07	42.33	ohm
pull-down	31.81	34.09	36.71	39.77	ohm
Control bit	5'b10011	5'b10010	5'b10001	5'b10000	units
pull-up	46.17	50.79	56.43	63.49	ohm
pull-down	43.38	47.72	53.02	59.65	ohm
Control bit	5'b01111	5'b01110	5'b01101	5'b01100	units
pull-up	33.86	36.28	39.07	42.33	ohm

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pull-down	31.81	34.09	36.71	39.77	ohm
Control bit	5'b01011	5'b01010	5'b01001	5'b01000	units
pull-up	46.17	50.79	56.43	63.49	ohm
pull-down	43.38	47.72	53.02	59.65	ohm
Control bit	5'b00111	5'b00110	5'b00101	5'b00100	units
pull-up	72.56	84.65	101.58	126.98	ohm
pull-down	68.17	79.53	95.44	119.3	ohm
Control bit	5'b00011	5'b00010	5'b00001	5'b00000	units
pull-up	169.3	253.95	507.9	+∞	ohm
pull-down	159.07	238.6	477.2	+∞	ohm

Table 13-9 LPDDR4/DDR3 Drive Strength and ODT Resistance table

Control bit	5'b11111	5'b11110	5'b11101	5'b11100	units
pull-up	23.53	24.6	25.77	27.06	ohm
pull-down	20.72	21.66	22.69	23.83	ohm
Control bit	5'b11011	5'b11010	5'b11001	5'b11000	units
pull-up	28.48	30.07	31.84	33.83	ohm
pull-down	25.08	26.47	28.03	29.78	ohm
Control bit	5'b10111	5'b10110	5'b10101	5'b10100	units
pull-up	36.08	38.66	41.63	45.1	ohm
pull-down	31.77	34.04	36.65	39.71	ohm
Control bit	5'b10011	5'b10010	5'b10001	5'b10000	units
pull-up	49.2	54.12	60.13	67.65	ohm
pull-down	43.32	47.65	52.94	59.56	ohm
Control bit	5'b01111	5'b01110	5'b01101	5'b01100	units
pull-up	36.08	38.66	41.63	45.1	ohm
pull-down	31.77	34.04	36.65	39.71	ohm
Control bit	5'b01011	5'b01010	5'b01001	5'b01000	units
pull-up	49.2	54.12	60.13	67.65	ohm
pull-down	43.32	47.65	52.94	59.56	ohm
Control bit	5'b00111	5'b00110	5'b00101	5'b00100	units
pull-up	77.31	90.2	108.24	135.3	ohm
pull-down	68.07	79.42	95.3	119.13	ohm
Control bit	5'b00011	5'b00010	5'b00001	5'b00000	units
pull-up	180.4	270.6	541.2	+∞	ohm
pull-down	158.83	238.25	476.5	+∞	ohm

Table 13-10 LPDDR3 Drive Strength and ODT Resistance table

Control bit	5'b11111	5'b11110	5'b11101	5'b11100	units
pull-up	22.08	23.09	24.19	25.4	ohm
pull-down	20.75	21.69	22.72	23.86	ohm
Control bit	5'b11011	5'b11010	5'b11001	5'b11000	units
pull-up	26.73	28.22	29.88	31.74	ohm
pull-down	25.12	26.51	28.07	29.83	ohm
Control bit	5'b10111	5'b10110	5'b10101	5'b10100	units
pull-up	33.86	36.28	39.07	42.33	ohm
pull-down	31.81	34.09	36.71	39.77	ohm

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Control bit	5'b10011	5'b10010	5'b10001	5'b10000	units
pull-up	46.17	50.79	56.43	63.49	ohm
pull-down	43.38	47.72	53.02	59.65	ohm
Control bit	5'b01111	5'b01110	5'b01101	5'b01100	units
pull-up	33.86	36.28	39.07	42.33	ohm
pull-down	31.81	34.09	36.71	39.77	ohm
Control bit	5'b01011	5'b01010	5'b01001	5'b01000	units
pull-up	46.17	50.79	56.43	63.49	ohm
pull-down	43.38	47.72	53.02	59.65	ohm
Control bit	5'b00111	5'b00110	5'b00101	5'b00100	units
pull-up	72.56	84.65	101.58	126.98	ohm
pull-down	68.17	79.53	95.44	119.3	ohm
Control bit	5'b00011	5'b00010	5'b00001	5'b00000	units
pull-up	169.3	253.95	507.9	+∞	ohm
pull-down	159.07	238.6	477.2	+∞	ohm

13.6.3 Command Perbit De-Skew Control

The DDR PHY supports to use the per-bit de-skew to adjust the delay of the command PAD to change the phase of the command which will be sent to the SDRAM.
For DDR4, the user can use the register to change the per-bit de-skew of the command directly.
Because the PHY supports the default command pad mapping, the user needs to change the corresponding register after the command pad mapping.
For example, if the user chooses DDR4 SDRAM mode, it can change the phase A0 directly through the reg_a0_invdelaysel register. The following table gives the detail description about the relationship between the control register and SDRAM PAD.

Table 13-11 CMD Per Bit De-skew Control Map for SDRAM

NAME	ADDR	BIT	DEFAULT	SDRAM PAD			
				DDR4	DDR3	LPDDR3	LPDDR4
reg_a0_invdelaysel	0x104	[31,24]	8'h80	A0	A9	-	CKB_B
reg_a1_invdelaysel		[23,16]	8'h80	A1	A2	-	-
reg_a2_invdelaysel		[15,8]	8'h80	A2	A4	A6	CA1_A
reg_a3_invdelaysel		[7,0]	8'h80	A3	A3	-	CKE1_A
reg_a4_invdelaysel	0x108	[31,24]	8'h80	A4	BA1	-	CA3_B
reg_a5_invdelaysel		[23,16]	8'h80	A5	A11	-	CA5_B
reg_a6_invdelaysel		[15,8]	8'h80	A6	A14	A1	CA1_B
reg_a7_invdelaysel		[7,0]	8'h80	A7	A8	ODT1	ODT0_B
reg_a8_invdelaysel	0x10c	[31,24]	8'h80	A8	A7	A9	ODT0_A
reg_a9_invdelaysel		[23,16]	8'h80	A9	A13	-	CK_B
reg_a10_invdelaysel		[15,8]	8'h80	A10	A10	CSB0	CKE0_B
reg_a11_invdelaysel		[7,0]	8'h80	A11	A6	A8	CA0_A
reg_a12_invdelaysel	0x110	[31,24]	8'h80	A12	BA0	-	CA3_A
reg_a13_invdelaysel		[23,16]	8'h80	A13	A5	A0	CA0_B
reg_a14_invdelaysel		[15,8]	8'h80	A14	A15	-	CA4_A
reg_a15_invdelaysel		[7,0]	8'h80	A15	A0	A7	CA2_A
reg_a16_invdelaysel	0x114	[31,24]	8'h80	A16	RASB	-	CA5_A
reg_a17_invdelaysel		[23,16]	8'h80	A17	-	-	-
reg_ba0_invdelaysel		[15,8]	8'h80	BA0	A1	A3	CA2_B
reg_ba1_invdelaysel		[7,0]	8'h80	BA1	A12	-	CA4_B
reg_bg0_invdelaysel	0x118	[31,24]	8'h80	BG0	WEN	-	ODT1_B
reg_bg1_invdelaysel		[23,16]	8'h80	BG1	BA2	-	ODT1_A

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reg_cke0_invdelaysel		[15,8]	8'h80	CKE	CKE	CKE	CKE0_A
reg_cke1_invdelaysel		[7,0]	8'h80	-	-	-	-
reg_ckb_invdelaysel	0x11c	[31,24]	8'h80	CKB	CKB	CKB	CK_A
reg_ck_invdelaysel		[23,16]	8'h80	CK	CK	CK	CKB_A
reg_odt0_invdelaysel		[15,8]	8'h80	ODT0	ODT0	A4	CSB1_B
reg_odt1_invdelaysel		[7,0]	8'h80	ODT1	CSB0	A2	CSB0_B
reg_csb0_invdelaysel	0x120	[31,24]	8'h80	CSB0	ODT1	ODT0	CSB0_A
reg_csb1_invdelaysel		[23,16]	8'h80	CSB1	CSB1	A5	CSB1_A
reg_resetn_invdelaysel		[15,8]	8'h80	RESETN	RESETN	-	RESETN
reg_actn_invdelaysel		[7,0]	8'h80	ACTN	CASB	CSB1	CKE1_B

For LPDDR4, the SDRAM supports the command bus train function, so the command per-bit de-skew can be controlled by the register directly or it can be control by the command bus trainmodule. The command per-bit de-skew control path shows in the following figure.

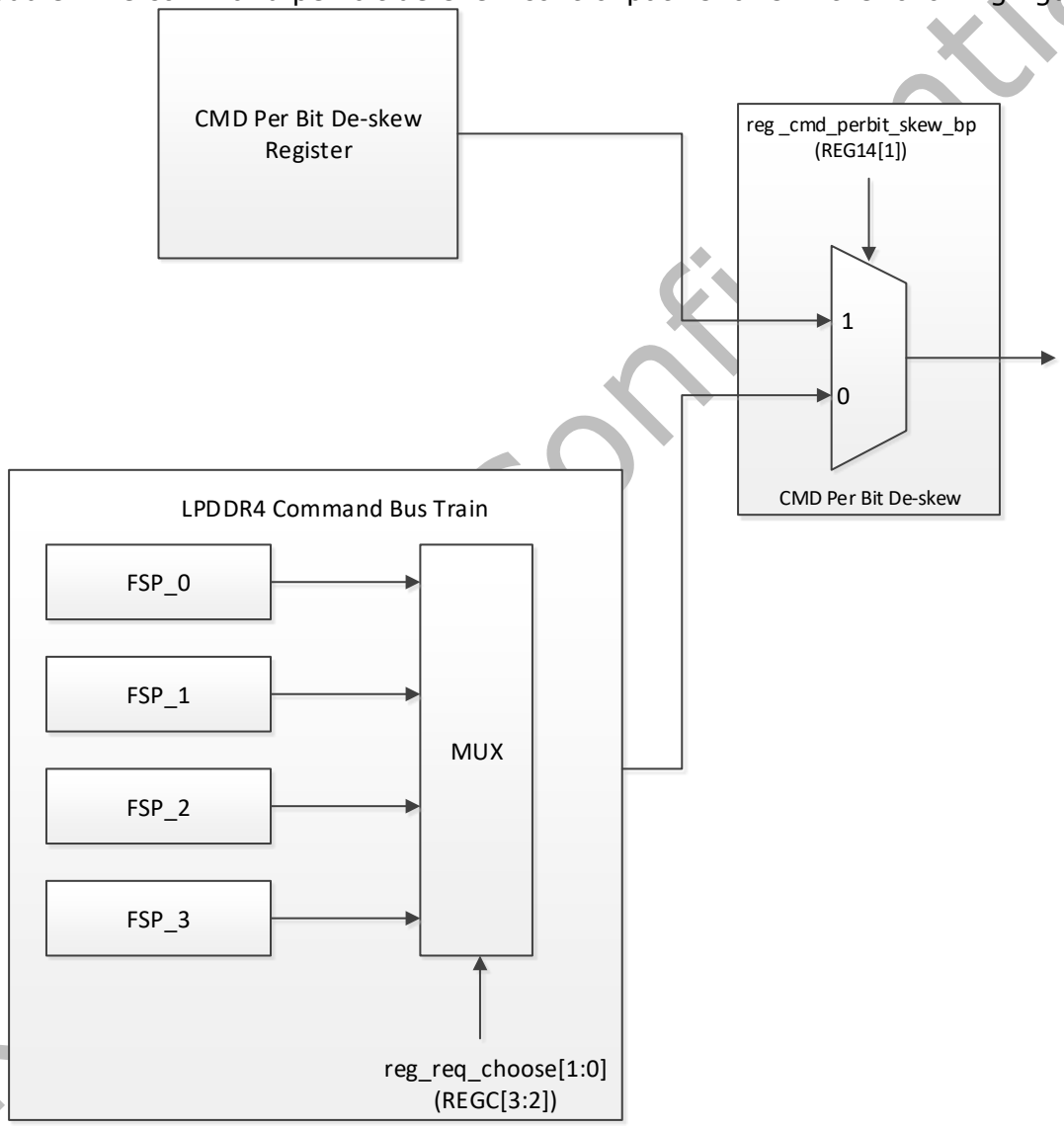


Fig.13-3 CMD Per Bit De-skew Ctrl Path of LPDDR4

After power up, apb reset and phy reset, reg_cmd_perbit_skew_bp(REG14[1]) is 1'b0. The PHY will choose the command bus train reset value to control the command per-bit de-skew.

When set reg_cmd_perbit_skew_bp(REG14[1])to 1'b1, then the user can use the register to

control the command per-bit de-skew directly.

The FSP_0/FSP_1/FSP_2/FSP_3 blocks in the command bus train module are used to control thecommand per-bit de-skew for different frequency groups. When enable the auto command bustrain function, the FSP_n will control the command per-bit de-skew according

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to the
reg_freq_choose[1:0](REG17[31:30]) automatically. After complete the auto command bus train, the train value will be locked in the FSP_n module, then the user canusethereg_freq_choose[1:0](REG17[31:30])to switch frequency quickly. The user also canuse the register to update the FSP_n lock value after the command bus train. The steps show below:
1. Configure the per-bit de-skew value of the command through the corresponding register. For example, if you want to change the per-bit de-skew of the CA1_A, configure the desired value to the reg_a13_invdelaysel.
2. Use the register reg_freq_choose[1:0](REG17[31:30]) to choose the frequency point. For example, if you want to change the per-bit de-skew of the command at frequency point 2,
configure the 0x02 to reg_freq_choose[1:0](REG17[31:30]).
3. Set the reg_ca_perbit_skew_update(REG14[0]) to 1'b1 to update the lock value and recover to 1'b0.
4. After these steps, the per-bit de-sew of command belong to frequency point 2 will change
and be locked again.
The above configure path is enabled when reg_cmd_perbit_skew_bp(REG14[1]) set to 1'b0.
When reg_cmd_perbit_skew_bp(REG14[1])set to 1'b1, the user can use the register to controlthe per-bit de-skew directly. The register directly control path is useful when enable the commandbus train bypass mode.

13.6.4 Data Perbit De-Skew Control

The address offset of different data channels shows in following table.

Table 13-12 Address offset of each channel

CHANNEL	ADDRESS_OFFSET
Byte0(CS0)	0x420(0x20)
Byte0(CS1)	0x440(0x20)
Byte0(CS2)	0x500(0x1c)
Byte0(CS3)	0x51c(0x20)
Byte1(CS0)	0x620(0x20)
Byte1(CS1)	0x640(0x20)
Byte1(CS2)	0x700(0x1c)
Byte1(CS3)	0x71c(0x20)
Byte2(CS0)	0x820(0x20)
Byte2(CS1)	0x840(0x20)
Byte2(CS2)	0x900(0x1c)
Byte2(CS3)	0x91c(0x20)
Byte3(CS0)	0xa20(0x20)
Byte3(CS1)	0xa40(0x20)
Byte3(CS2)	0xb00(0x1c)
Byte3(CS3)	0xb1c(0x20)

Byte0 CS0/CS1/CS3 bit has a following feature for TX and RX

ADDR	NAME	BIT	DEFAULT	DESCRIPTIONS
0x420	reg_a_l_cs0_dm_in_vdelaysel	[7,0]	0x80	The register used to control the tx delay line of the A_DM0 for RANK0
0x424	reg_a_l_cs0_dq0_in_vdelaysel	[31,24]	0x80	The register used to control the tx delay line of the A_DQ0 for RANK0
	reg_a_l_cs0_dq1_in_vdelaysel	[23,16]	0x80	The register used to control the tx delay line of the A_DQ1 for RANK0

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ADDR	NAME	BIT	DEFAULT	DESCRIPTIONS
	reg_a_l_cs0_dq2_in_vdelaysel	[15,8]	0x80	The register used to control the tx delay line of the A_DQ2 for RANK0
	reg_a_l_cs0_dq3_in_vdelaysel	[7,0]	0x80	The register used to control the tx delay line of the A_DQ3 for RANK0
0x428	reg_a_l_cs0_dq4_in_vdelaysel	[31,24]	0x80	The register used to control the tx delay line of the A_DQ4 for RANK0
	reg_a_l_cs0_dq5_in_vdelaysel	[23,16]	0x80	The register used to control the tx delay line of the A_DQ5 for RANK0
	reg_a_l_cs0_dq6_in_vdelaysel	[15,8]	0x80	The register used to control the tx delay line of the A_DQ6 for RANK0
	reg_a_l_cs0_dq7_in_vdelaysel	[7,0]	0x80	The register used to control the tx delay line of the A_DQ7 for RANK0
0x42c	reg_a_l_cs0_dqs_in_vdelaysel	[31,24]	0x80	The register used to control the tx delay line of the A_DQS for RANK0
	reg_a_l_cs0_dqs_in_vdelaysel	[15,8]	0x80	The register used to control the tx delay line of the A_DQSB for RANK0
0x430	reg_a_l_cs0_loop_invdelaysel	[28,24]	0x0	The register used to choose the obs signal to check delay line control of the byte0 for RANK0. 5'd0: Choose to the current value to control the rx delay line of A_DQ0 for RANK0. 5'd1: Choose to the current value to control the rx delay line of A_DQ1 for RANK0. 5'd2: Choose to the current value to control the rx delay line of A_DQ2 for RANK0. 5'd3: Choose to the current value to control the rx delay line of A_DQ3 for RANK0. 5'd4: Choose to the current value to control the rx delay line of A_DQ4 for RANK0. 5'd5: Choose to the current value to control the rx delay line of A_DQ5 for RANK0. 5'd6: Choose to the current value to control the rx delay line of A_DQ6 for RANK0. 5'd7: Choose to the current value to control the rx delay line of A_DQ7 for RANK0. 5'd8: Choose to the current value to control the rx delay line of A_DM0 for RANK0.

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ADDR	NAME	BIT	DEFAULT	DESCRIPTIONS
				5'd9: Choose to the current value to control the rx delay line of A_DQS0 for RANK0. 5'd10: Choose to the current value to control the rx delay line of A_DQSB0 for RANK0. 5'd16: Choose to the current value to control the tx delay line of A_DQ0 for RANK0 5'd17: Choose to the current value to control the tx delay line of A_DQ1 for RANK0. 5'd18: Choose to the current value to control the tx delay line of A_DQ2 for RANK0. 5'd19: Choose to the current value to control the tx delay line of A_DQ3 for RANK0. 5'd20: Choose to the current value to control the tx delay line of A_DQ4 for RANK0. 5'd21: Choose to the current value to control the tx delay line of A_DQ5 for RANK0. 5'd22: Choose to the current value to control the tx delay line of A_DQ6 for RANK0. 5'd23: Choose to the current value to control the tx delay line of A_DQ7 for RANK0. 5'd24: Choose to the current value to control the tx delay line of A_DM0 for RANK0. 5'd25 Choose to the current value to control the tx delay line of A_DQS0 for RANK0. 5'd26: Choose to the current value to control the tx delay line of A_DQSB0 for RANK0.
	reg_a_l_cs0_dm_invdelayselrx	[14,8]	0x0	The register used to control the rx delay line of the A_DM0 for RANK0
0x434	reg_a_l_cs0_dq0_in_vdelayselrx	[31,24]	0x80	The register used to control the rx delay line of the A_DQ0 for RANK0
	reg_a_l_cs0_dq1_in_vdelayselrx	[23,16]	0x80	The register used to control the rx delay line of the A_DQ1 for RANK0
	reg_a_l_cs0_dq2_in_vdelayselrx	[15,8]	0x80	The register used to control the rx delay line of the A_DQ2 for RANK0
	reg_a_l_cs0_dq3_in_vdelayselrx	[7,0]	0x80	The register used to control the rx delay line of the A_DQ3 for RANK0

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ADDR	NAME	BIT	DEFAULT	DESCRIPTIONS
0x438	reg_a_l_cs0_dq4_in_vdelay selrx	[31,24]	0x80	The register used to control the rx delay line of the A_DQ4 for RANK0
	reg_a_l_cs0_dq5_in_vdelay selrx	[23,16]	0x80	The register used to control the rx delay line of the A_DQ5 for RANK0
	reg_a_l_cs0_dq6_in_vdelay selrx	[15,8]	0x80	The register used to control the rx delay line of the A_DQ6 for RANK0
	reg_a_l_cs0_dq7_in_vdelay selrx	[7,0]	0x80	The register used to control the rx delay line of the A_DQ7 for RANK0
0x43c	reg_a_l_cs0_dqs_in_vdelay selrx	[31,24]	0x80	The register used to control the rx delay line of the A_DQS for RANK0
	reg_a_l_cs0_dqs_in_vdelay selrx	[15,8]	0x80	The register used to control the rx delay line of the A_DQSB for RANK0

Byte0 CS2 bit has a following feature for TX and RX

ADDR	NAME	BIT	DEFAULT	DESCRIPTIONS
0x500	reg_a_l_cs2_dq0_invdelays el	[31,24]	0x80	The register used to control the tx delay line of the A_DQ0 for RANK2.
	reg_a_l_cs2_dq1_invdelays el	[23,16]	0x80	The register used to control the tx delay line of the A_DQ1 for RANK2.
	reg_a_l_cs2_dq2_invdelays el	[15,8]	0x80	The register used to control the tx delay line of the A_DQ2 for RANK2.
	reg_a_l_cs2_dq3_invdelays el	[7,0]	0x80	The register used to control the tx delay line of the A_DQ3 for RANK2.
0x504	reg_a_l_cs2_dq4_invdelays el	[31,24]	0x80	The register used to control the tx delay line of the A_DQ4 for RANK2.
	reg_a_l_cs2_dq5_invdelays el	[23,16]	0x80	The register used to control the tx delay line of the A_DQ5 for RANK2.
	reg_a_l_cs2_dq6_invdelays el	[15,8]	0x80	The register used to control the tx delay line of the A_DQ6 for RANK2.
	reg_a_l_cs2_dq7_invdelays el	[7,0]	0x80	The register used to control the tx delay line of the A_DQ7 for RANK2.
0x508	reg_a_l_cs2_dqs_invdelays el	[31,24]	0x80	The register used to control the tx delay line of the A_DQS0 for RANK2.
	reg_a_l_cs2_dqsb_invdelay sel	[15,8]	0x80	The register used to control the tx delay line of the A_DQSB0 for RANK2.
0x50c	reg_a_l_cs2_loop_invdelay sel	[28,24]	0x0	The register used to choose the obs signal to check delay line control of the byte0 for RANK2.

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ADDR	NAME	BIT	DEFAULT	DESCRIPTIONS
				5'd0: Choose to the current value to control the rx delay line of A_DQ0 for RANK2. 5'd1: Choose to the current value to control the rx delay line of A_DQ1 for RANK2. 5'd2: Choose to the current value to control the rx delay line of A_DQ2 for RANK2. 5'd3: Choose to the current value to control the rx delay line of A_DQ3 for RANK2. 5'd4: Choose to the current value to control the rx delay line of A_DQ4 for RANK2. 5'd5: Choose to the current value to control the rx delay line of A_DQ5 for RANK2. 5'd6: Choose to the current value to control the rx delay line of A_DQ6 for RANK2. 5'd7: Choose to the current value to control the rx delay line of A_DQ7 for RANK2. 5'd8: Choose to the current value to control the rx delay line of A_DM0 for RANK2. 5'd9: Choose to the current value to control the rx delay line of A_DQS0 for RANK2. 5'd10: Choose to the current value to control the rx delay line of A_DQSB0 for RANK2. 5'd16: Choose to the current value to control the tx delay line of A_DQ0 for RANK2 5'd17: Choose to the current value to control the tx delay line of A_DQ1 for RANK2. 5'd18: Choose to the current value to control the tx delay line of A_DQ2 for RANK2. 5'd19: Choose to the current value to control the tx delay line of A_DQ3 for RANK2. 5'd20: Choose to the current value to control the tx delay line of A_DQ4 for RANK2. 5'd21: Choose to the current value to control the tx delay line of A_DQ5 for RANK2. 5'd22: Choose to the current value to control the tx delay line of A_DQ6 for RANK2. 5'd23: Choose to the current value to control the tx delay

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ADDR	NAME	BIT	DEFAULT	DESCRIPTIONS
				line of A_DQ7 for RANK2. 5'd24: Choose to the current value to control the tx delay line of A_DM0 for RANK2. 5'd25 Choose to the current value to control the tx delay line of A_DQS0 for RANK2. 5'd26: Choose to the current value to control the tx delay line of A_DQSB0 for RANK2.
	reg_a_l_cs2_dm_invdelaysel	[15,8]	0x80	The register used to control the tx delay line of the A_DM0 for RANK2.
	reg_a_l_cs2_dm_invdelayselrx	[6,0]	0x0	The register used to control the rx delay line of the A_DM0 for RANK2.
0x510	reg_a_l_cs2_dq0_invdelayselrx	[30,24]	0x0	The register used to control the rx delay line of the A_DQ0 for RANK2.
	reg_a_l_cs2_dq1_invdelayselrx	[22,16]	0x0	The register used to control the rx delay line of the A_DQ1 for RANK2.
	reg_a_l_cs2_dq2_invdelayselrx	[14,8]	0x0	The register used to control the rx delay line of the A_DQ2 for RANK2.
	reg_a_l_cs2_dq3_invdelayselrx	[6,0]	0x0	The register used to control the rx delay line of the A_DQ3 for RANK2.
0x514	reg_a_l_cs2_dq4_invdelayselrx	[30,24]	0x0	The register used to control the rx delay line of the A_DQ4 for RANK2.
	reg_a_l_cs2_dq5_invdelayselrx	[22,16]	0x0	The register used to control the rx delay line of the A_DQ5 for RANK2.
	reg_a_l_cs2_dq6_invdelayselrx	[14,8]	0x0	The register used to control the rx delay line of the A_DQ6 for RANK2.
	reg_a_l_cs2_dq7_invdelayselrx	[6,0]	0x0	The register used to control the rx delay line of the A_DQ7 for RANK2.
0x518	reg_a_l_cs2_dqs_invdelayselrx	[30,24]	0x1f	The register used to control the rx delay line of the A_DQS0 for RANK2.
	reg_a_l_cs2_dqsb_invdelayselrx	[14,8]	0x1f	The register used to control the rx delay line of the A_DQSB0 for RANK2.

There are three paths to control the TX data Perbit de-skew show in thefollowing table.

Table 13-13 TX data Perbit de-skew path

PATH	DESCRIPTION	CONFIGURE
Register	Using the register to update the TX data Perbit de-skew directly.	reg_dq_wr_train_en(REG40[1]) set to 0. reg_wl_bypass(REG1[7]) set to 1. Generate the posedge of reg_wl_freq_update(REG17[28])
Write	Using the write	reg_wl_bypass(REG1[7]) set to 0.

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Leveling	levelingresult.	
Write Training	Using the write trainingresult.	reg_dq_wr_train_en(REG40[1]) set to 1. reg_wl_bypass(REG1[7]) set to 1.

There are two paths to control the RX data Perbit de-skew show in thefollowing table.

Table 13-14 RX data Perbit de-skew path

PATH	DESCRIPTION	CONFIGURE
Register	Using the register to update the RX data Perbit de-skew directly.	reg_dq_rd_train_en(REG37[0]) set to 0 and reg_rd_train_predef_en(REG37[14]) set to 0. Generate the posedge of reg_rd_train_freq_update(REG37[2])
Read Training	Using the read trainingresult.	reg_dq_rd_train_en(REG37[0]) set to 1 or reg_rd_train_predef_en(REG37[14]) set to 1.

13.6.5 DDR PHY Command Bus Training

The LPDDR4-SDRAM command bus must be trained before enabling termination forhigh-frequency operation. The DDR PHY supports the auto command bus trainfunction to center the internal VREF(ca) in the CA data eye and adjustment of the CS and CAsignals to meet setup/hold requirements.

When enable the auto command bus train function, the PHY will complete the train of the VREF(ca), CS and CA automatically. The auto command bus train flow shows in the following steps.

1. Configure reg_phy_sdram_initial(REG48[16]) to 1'b1 to fix the input of the command path
2. PHY initialization
3. Configure reg_clk_div_cnt(REG8[12:8]) to choose the divider for the low speed
4. Configure reg_tmrw(REG9[9:5]/reg_tcacd(REG9[4:0])/reg_tvrefca(REG10[23:16]/reg_tcaent(REG10[7:0])/reg_tckelck(REG9[19:15])/reg_tdstrain(REG9[14:10])/reg_tadr(REG9[24:20])/reg_txcbt(REG9[29:25])/reg_tfc(REG10[7:0]) to configure the timing parameter for auto cat train
5. Configure reg_cat_rank_num(REG8[19:15]) = 4'b0000/4'b1110/4'b1101/4'b1011/4'b0111(4RANK/RANK0/RANK1/RANK2/RANK3) to chosse the ca train rank, set reg_lpddr4_ca_odt_sel=1'b1 to select the reg control odt, reg_lpddr4_ca_odt(REG14[15:12]=4'b0001 to terminate the rank0 (or reg_lpddr4_ca_odt(REG14[15:12]=4'b0010 to terminate the rank1)
6. Configure reg_cat_cs_train_value(REG15[5:0]) reg_cat_ca_train_value(REG15[13:8]) to choose the cs and ca training pattern
7. Configure reg_cha_cat_cs_check_value(REG16[29:24]) reg_chb_cat_cs_check_value(REG16[21:16]) reg_cha_cat_ca_check_value(REG16[13:8]) reg_chb_cat_ca_check_value(REG16[5:0]) to choose the cs and ca training pattern
8. Configure reg_cat_enable(REG8[0]) to 1'b1 to enable the auto command bus train
9. Configure reg_cat_start(REG8[1]) to 1'b1 to start the auto command bus train
10. Wait auto command bus train done by read REG133[1:0], when it equals to 2'b11(for two ranks), it means complete the auto command bus train.
11. Configure reg_cat_start(REG8[1]) to 1'b0 to exit the auto command bus train
12. Configure reg_cat_enable(REG8[0]) to 1'b0 to disable the auto command bus train
13. Configure reg_cmd_invdelaysel_sel(REG108[15:10]) and then read register REG140[23:16] to get the ca train result

reg_cmd_invdelaysel_sel[5:0]
0:channel A ca0 rank0
1:channel A ca1 rank0
....(ca2-ca4) channel A rank0
5:channel A ca5 rank0
6:channel B ca0 rank0
....(ca1-ca4) channel B rank0
11:channel B ca5 rank0
12:channel A ca0 rank1
....(ca1-ca4) channel A rank1

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17:channel A ca5 rank1
18:channel B ca0 rank1
...(ca1-ca4) channel B rank1
23:channel B ca5 rank1
24:channel A ck
25:channel A ckb
26:channel A cke0
27:channel A cke1
28:channel A csb0
29:channel A csb1
30:channel A odt0
31:channel A odt1
32:channel B ck
33:channel B ckb
34:channel B cke0
35:channel B cke1
36:channel B csb0
37:channel B csb1
38:channel B odt0
39:channel B odt1

The command bus train not only adjusts the phase of the CA bus but also adjusts the phase of the CS. The user can use the reg_cat_skip_cs_train(REG14[2]) to control the enable or disable ofthe cstrain. When this signal sets to 1, the PHY will skip the cstrain; when this signal sets to0, the PHY will enable the cstrain.

The PHY support two modes cstrain controlled by the reg_cs_pwc_disable(REG14[7]):

Normal cstrain (reg_cs_pwc_disable = 1): When choose the normal cstrain mode, the pulse
width of the CS will keep the same width of the CK period.

Modulation cstrain (reg_cs_pwc_disable =0): It is the default mode. When choose this mode,
the pulse width of the CS will the 75% of the CK period when the CS is in the train mode (after
the frequency changes from the FSP[X] to FSP[Y]). The state shows in the following figure.

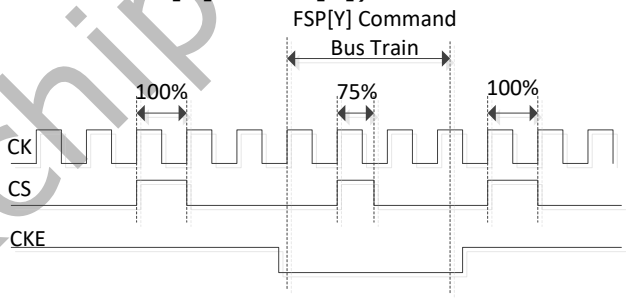


Fig.13-4 Modulation Cstrain Mode

If the user enables the Modulation cstrain mode, the CS Train is based on the 75% pulse widthof the normal CS. So the cstrain result has fixed 25% offset and need to compensate 12.5% offset using the special register after the command bus train. After that, the CS will go to the bestpoint of the cstrain.

The user uses the following registers to complete the compensation of the cs train result.

Table 13-15 Compensation of the ca and cs train result

ADDR	SIGNAL	DESCRIPTION
REG16[29:24]	reg_cha_cat_cs_check_value	The check value of channel A when do the cs train
REG16[21:16]	reg_chb_cat_cs_check_value	The check value of channel A when do the cs train
REG16[13:8]	reg_cha_cat_ca_check_value	The check value of channel A when do the ca train
REG16[5:0]	reg_chb_cat_ca_check_value	The check value of channel A when do

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		the ca train

This register should be set after the command bus train and before change the frequency to the train frequency point.

13.6.6 DDR PHY RX DQS Calibration

DDR PHY auto dqs calibration function has been implemented in the PHY. The entire training processes only need to configure the register to start andwait for finish.
The entire training process is as follows:
1. PHY’s register is reset, the setup is complete.
2. Send the initial command to dram and complete dram initialization.
3. Set the PHY's register beginning calibration.

ADDR	BIT	DEFAULT	DESCRIPTION
0x04(REG1)	5:2	0xe	The rank select signal of the rx-dqs calibration fuction. Low is valid. 4'b0000: The rx-dqs calibration result will auto switch between the RANK0, RANK1,RANK2,RANK3 according to the DFI interface command after the rx-dqs calibration training. 4'b0111: Choose the RANK3. The chip which connects to CS3 will be chooses to enable the auto rx-dqs calibration training. 4'b1011: Choose the RANK2. The chip which connects to CS2 will be chooses to enable the auto rx-dqs calibration training. 4'b1101: Choose the RANK1. The chip which connects to CS1 will be chooses to enable the auto rx-dqs calibration training. 4'b1110: Choose the RANK0. The chip which connects to CS0 will be chooses to enable the auto rx-dqs calibration training. 4'b11: Reserved. Note: Can't set to 2'b00 when enable the rx-dqs calibration training funciton. If the PHY needs to support two ranks, this register should set to 2'b00 after the rx-dqs calibration training.
	1	0x0	set calibration bypass mode(1:bypass mode; 0:nomal)
	0	0x0	The auto rx-dqs calibration training enable signal. High is valid. 0: Keep current state or exit the auto rx-dqs calibration training. 1: Enable the auto rx-dqs calibration training function.
0x20c(REG131)	6		The rx dqs calib complete signal. Active high. Only change to 1'b1 when all open channel have compelte the rx dqs calibration
	5		The error flag of the rx dqs calib. Active high.
	4:0		The rx dqs calib complete signal of each channel. Active high. [0]: The rx dqs calib complete of byte0. [1]: The rx dqs calib complete of byte1. [2]: The rx dqs calib complete of byte2. [3]: The rx dqs calib compelte of byte3. [4]: The rx dqs calib compelte of byte4

4. Wait for the calibration finish by PHYREG0x20c.
5. Normal read and writes operation can begin.

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13.6.7 DDR PHY Write Leveling Training

DDR PHY auto write leveling training function has been implemented in the PHY. The entire training processes only need to configure the register to start and wait for finish。

The entire training process is as follows:

1. PHY’s register is reset, the setup is complete.
2. Send the initial command to dram and complete dram initialization.
3. Set the PHY REG0x4 to configure the dram mode register which used to enable dram write leveling training function.
4. Set the PHY's register to begintraining.

ADDR	BIT	DEFAULT	DESCRIPTION
0x4(REG1)	31:16	0x0	[23:16]Write leveling load mode [7:0]. The PHY needs to configure the load mode to enable the write leveling function. In case of that write leveling operation changs the load mode value in the SDRAM which is written by the MC, so we need to use this register to keep the same setting with the MC for the mode register which is related to the write leveling. This is the low 8bits of the mode register which is related to the write leveling. For DDR3/DDR4, this register should keep the same value with the MR1[7:0]. For LPDDR3/LPDDR4, this register should keep the same value with the MR2[7:0]. Please reference to the section 4.5.2 to get more information. [31:24]"Write leveling load mode [15:8]. Relate to the register 10’h002 [2]. The PHY needs to configure the load mode to enable the write leveling function. In case of that write leveling operation changs the load mode value in the SDRAM which is written by the MC, so we need to use this register to keep the same setting with the MC for the mode register which is related to the write leveling. This is the low 8bits of the mode register which is related to the write leveling. For DDR3/DDR4, this register [13:8] should keep the same value with the MR1[13:8] and this register[15:14] should set 2'b01. For LPDDR3/LPDDR4, this register should set to 8'h0.
	11:8	0xe	The rank select signal of the write-leveling fuction. Low is valid. 4'b0000: The write-leveling result will auto switch between the RANK0 ,RANK1,RANK2,RANK3 according to the DFI interface command after the write-leveling training. 4'b0111: Choose the RANK3. The chip which connects to CS3 will be chooses to enable the write-leveling training. 4'b1011: Choose the RANK2. The chip which connects to CS2 will be chooses to enable the write-leveling training. 4'b1101: Choose the RANK1. The chip which connects to CS1 will be chooses to enable the

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ADDR	BIT	DEFAULT	DESCRIPTION
			write-leveling training. 4'b1110: Choose the RANK0. The chip which connects to CS0 will be chooses to enable the write-leveling training. 4'b1111: Reserved. Note: Can't set to 4'b0000 when enable the write-levleing training funciton. If the PHY needs to support two ranks, this register should set to 2'b00 after the write-leveling training.
	7	0x0	The tx perbit-skew bypass function enable signal. High is valid. 0: Use the write-leveling training result to control the tx perbit-skew delay. The A_DQ0~A_DQ7/A_DM0 will use the A_DQS0 training result. The A_DQ8~A_DQ15/A_DM1 will use the A_DQS1 training result. The B_DQ0~A_DQ7/A_DM0 will use the B_DQS0 training result. The B_DQ8~A_DQ15/A_DM0 will use the B_DQS1 training result. 1: Use the register to control the tx perbit-skew delay. Each data pad has an independet controller register.
	6	0x0	The write-leveling training enable signal. High is valid. 0: Keep current state or exit the write-leveling training state. 1: Eanble the write-leveling training function
0x44(REG17)	28	0x0	The data tx delay line control value update signal. Active high. In the default mode, the tx delay line is controlled by the write-levevling/write training result according to the frequency point. If the user wants to change the value to adjust the delay line, the user can use the bypass registers (invdelay_t) that show in the Table "Data Perbit De-skew Control Registers for TX and RX" to set the value and set this signal “1”. Then the bypass register value will be updated to the control register of the tx perbit skew base on the current frequency point.
0x20c(REG131)	12:8		The write leveling complete signal of each channel. Active high. [0]: The write leveling complete of byte0. [1]: The write leveling complete of byte1. [2]: The write leveling complete of byte2. [3]: The write leveling compelte of byte3. [4]: The write leveling compelte of byte4

5. Wait for the calibration finish by polling PHY REG131. The write leveling results can be read from the following registers.

Table 13-16 Write leveling result for all bytes

ADDR	BIT	DEFAULT	DESCRIPTION
0x470	[23:16]	0x0	The write-leveling result of byte0 for RANK0. The user can get the write-leveling result after the

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ADDR	BIT	DEFAULT	DESCRIPTION
			write-leveling training complete
	[7:0]	0x0	The write-leveling result of byte0 for RANK1. The user can get the write-leveling result after the write-leveling training complete
0x54c	[23:16]	0x0	The write-leveling result of byte0 for RANK2. The user can get the write-leveling result after the write-leveling training complete
	[7:0]	0x0	The write-leveling result of byte0 for RANK3. The user can get the write-leveling result after the write-leveling training complete
0x670	[23:16]	0x0	The write-leveling result of byte1 for RANK0. The user can get the write-leveling result after the write-leveling training complete
	[7:0]	0x0	The write-leveling result of byte1 for RANK1. The user can get the write-leveling result after the write-leveling training complete
0x74c	[23:16]	0x0	The write-leveling result of byte1 for RANK2. The user can get the write-leveling result after the write-leveling training complete
	[7:0]	0x0	The write-leveling result of byte1 for RANK3. The user can get the write-leveling result after the write-leveling training complete
0x870	[23:16]	0x0	The write-leveling result of byte2 for RANK0. The user can get the write-leveling result after the write-leveling training complete
	[7:0]	0x0	The write-leveling result of byte2 for RANK1. The user can get the write-leveling result after the write-leveling training complete
0x94c	[23:16]	0x0	The write-leveling result of byte2 for RANK2. The user can get the write-leveling result after the write-leveling training complete
	[7:0]	0x0	The write-leveling result of byte2 for RANK3. The user can get the write-leveling result after the write-leveling training complete
0xa70	[23:16]	0x0	The write-leveling result of byte3 for RANK0. The user can get the write-leveling result after the write-leveling training complete
	[7:0]	0x0	The write-leveling result of byte3 for RANK1. The user can get the write-leveling result after the write-leveling training complete
0xb4c	[23:16]	0x0	The write-leveling result of byte3 for RANK2. The user can get the write-leveling result after the

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ADDR	BIT	DEFAULT	DESCRIPTION
			write-leveling training complete
	[7:0]	0x0	The write-leveling result of byte3 for RANK3. The user can get the write-leveling result after the write-leveling training complete

6. Normal read and writes operation can begin.

13.6.8 DDR PHY Read Train

The DDR PHY supports the read training. It includes three modes:

- Auto MPR/MPC Mode (Only support for DDR3/DDR4/LPDDR3/LPDDR4)
- Predefined mode (Only support DDR3/DDR4/LPDDR3/LPDDR4)
- Bypass Mode (Only support LPDDR3 and LPDDR4)

Auto MPR/MPC Mode: When the PHY chooses the DDR3/DDR4, it will use the MPR command to complete the read training of the Auto-Mode. When the PHY chooses theLPDDR3/LPDDR4, it will use the RD DQ Calibration command to complete the read training of the Auto-Mode and BP-Mode.

Predefine mode: you should write data to SDRAM and make sure the data has been written to the SDRAM at the specified location. For example, you can write data when SDRAM working at low frequency. Then the PHY read the data which you write to SDRAM.

When we enable the read training, the PHY will adjust the per-bit de-skew to change the delay ofthe RX DQS and RX DQ to find the optimal position. The adjust range of the per-bit de-skew isfrom 6'h0 to 6'h3f.

In rx vref training, we change the value of phy's vref. When set a new vref value to PHY, we should wait 800ns to update it. And the adjust range of the vref is from 8'h00 to 8'hff. You can

change the PHY's vref value yourself by configuring the associated register.

For predefined mode, the phy can support rx vref training. If you enable the vref training function, the predefinedread training have 3 steps, step1 adjust per-bitde-skew (step1_delay),step2 adjust vref(step2_vref), step3 adjust per-bit de-skew(step3_delay) again. When you disable vreftraining function, the predefinedread training only have step1.When step1 done, all steps done.

During the training, if you set reg_phy_refresh_en to 1'b1, the PHY support to do auto refresh

by itself. If you use this function, the controller should send a refresh (both rank in themeantime) after training enable, otherwise the PHY will keep waiting.

When the user enables the normal read training function, it will complete the read training automatically. The normal read training using the following steps.

1. Open PHY auto refresh function in training(if you need) by configuring reg_phy_refresh_en=0x1.
2. Choose the read training rank using the reg_rdtrain_cs_sel=2'b10(rank0).
3. Configure the MR15/MR20/MR32/MR40 through reg_lpddr4_mr15_value/reg_lpddr4_mr20_value/reg_lpddr4_mr32_value/reg_lpddr4_mr40_value to choose the read training pattern(Only for lpddr4).
4. choose the dqs phase before read training by setting cha_reg_l_rd_train_dqs_default/cha_reg_r_rd_train_dqs_default/chb_reg_l_rd_train_dqs_default/chb_reg_r_rd_train_dqs_default=0xe.
5. Enable the read training by setting reg_dq_rd_train_en=0x1.
6. Send a auto refresh(rank0 and rank1 in the meantime) if you open PHY auto refresh function.
7. Wait the train done by polling the reg_train_true_done=0x1.
8. Check the read train state by read cha(b)_train_done_for_rd_to_reg[1:0].High means error.
9. Exit the Read train by setting reg_dq_rd_train_en=0x0.

13.6.9 DDR PHY Write Train

The DDR PHY supports the write training. It only supports the auto mode. when the PHY chooses the DDR3/DDR4/LPDDR3, it will use the normal write and readcommand to complete the write training. When the PHY chooses the LPDDR4, it will use theDQS-DQ

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training mode command to complete the write training.
When we enable the write training, the PHY will adjust the per-bit de-skew to change the delay ofthe TX DQ to find the optimal position(The dqs will keep to the phase find by the write-levelingwhen enable the write leveling function). The adjust range of the per-bit de-skew is from 6'h0 to6'h3f.
The PHY can support tx vref training(only for LPDDR4). If you enable the vref training function,the wr training have 3 steps, step1 adjust per-bit de-skew(step1_delay), step2 adjust vref(step2_vref), step3 adjust per-bit de-skew(step3_delay) again. When you close vref trainingfunction, the wr training only have step1, when step1 done, all step done.
When the user enables the normal write training function, it will complete the write trainingautomatically. The normal write training using steps shows below.
1. Configure the initial address(write data to this address) reg_train_col_address/reg_train_ba_address/reg_train_row_address.
2. If you set reg_wrtrain_check_data_value_random_gen=0x0, configure the check data value as the data you want to write to SDRAM(10*BL8).
3. If you need the PHY do refresh in training, you should configure the reg_phy_trefi, reg_phy_trfc, reg_max_refi_cnt. Then enable the reg_phy_refresh_en=0x1.
4. Choose the write training rank using the reg_wrtrain_cs_sel=0x2(rank0).
5. If you need the PHY do tx vref training, you should configure reg_train_vref_step_max, reg_train_vref_step_min, reg_wrtrain_lpddr4_vref_range, reg_wrtrain_vref_wait_vref_cnt_50ns.
6. If you enable the DBI function, and want to do wr training with DBI function open, you should set reg_ddr4_dbi=0x1 first(Only for DDR4).
7. Choose the dqs phase before write training by setting reg_wr_train_dqs_default_bypass=0x1. Otherwise PHY will choose the write leveling training result.
8. Choose the write training auto mode by setting reg_dq_wr_train_auto=0x1.
9. Enable the tx vref training by setting(if need) reg_train_vref_en=0x1. Enable the write training by setting reg_dq_wr_train_en=0x1.
10. Send an auto refresh if you open PHY auto refresh function.
11. Wait the wr train done by polling the train_all_step_done=0x1.
12. Check the wr train state by read train_step1_error, train_step2_error, train_step3_error. High means error.
13. Exit the write training by setting reg_dq_wr_train_en=0x0.

13.6.10 DDR Monitor

13.6.10.1 DDR read or write address monitor

DDR monitor module can store 4 consecutive read or write addresses in real time. We can read these addresses by APB bus for debug when system enters abnormal state.
The steps of configuration to monitor DDR read or write address is as follows.

- Configure DDRMON_IF_CTRL.direction to select storing read or write address.
- Set DDRMON_IF_CTRL.if_mon_en to 1 to enable DDR monitor.
- When system is abnormal, we can read the register to get the current four addresses.

13.6.10.2 DDR access address monitor within a specified range

Sometimes we want to confirm whether DDR read or write within a specified address range, then we can configure the address range and enable this function.
The steps of configuration to monitor DDR access address within a specified range is as follows.

- Configure the write address range registers DDRMON_WR_START_ADDR, DDRMON_WR_END_ADDR, and read address registers DDRMON _RD_START_ADDR, DDRMON _RD_END_ADDR.
- Enable interrupt by configuring the register DDRMON_INT_MASK1[1:0] to 2'b00.
- Set DDRMON_IF_CTRL.if_mon_en to 1 to enable DDR address monitor.
- If the read or write addresses hit the range, then interrupt will assert, and we can read the interrupt status register DDRMON_INT_STATUS.

13.6.10.3 DDR access command statistics

This module can do the statistics about DDR access command, like write, read and active by monitoring DFI interface. There are two mode to do statistics, hardware mode and

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software mode. Two thresholds can be set, if read and write command number is more than high threshold, or less than low threshold, the interrupt will be asserted.

13.6.10.4 DDR low power statistics

It does the statistics about the low power period such as DDR self-refresh, power down, clk stop and PHY low power. After compare statistics interrupt asserts, the low power period represent in correspond count register will be updated and can be accessed through APB bus interface.

13.6.10.5 DDR special pattern statistics for a designated bank

In this module, for a designated bank, which is software configured. DDRMON will statistic the count for special DDR command patterns:

- per_bank_rd_wr_per_act_max_number: count the max read and write commands in an active command to a precharge command interval.
- per_bank_series_rd_burst_max_number: count the max series read command in an active command to a precharge command interval.
- per_bank_series_rd_burst_times_number: count the total number of series read command.
- per_bank_series_wr_burst_max_number: count the max series write command in an active command to a precharge command interval.
- per_bank_series_wr_burst_times_number: count the total number of series write command.
- per_bank_rd2rd_page_hit_number: count the total number of back to back read command.
- per_bank_wr2wr_page_hit_number: count the total number of back to back write command.
- per_bank_rd2wr_page_hit_number: count the total number of read next to write command.
- per_bank_rd2rd_page_miss_number: count all RD-PRE-ACT-RD pattern.
- per_bank_wr2wr_page_miss_number: count all WR-PRE-ACT-WR pattern.
- per_bank_rd2wr_page_miss_number: count all RD-PRE-ACT-WR pattern.
- per_bank_wr2rd_page_miss_number: count all WR-PRE-ACT-RD pattern.

13.6.10.6 DDR special pattern statistics for all banks

In this module, DDRMON count the special pattern for all ranks and all banks.

- all_bank_act_act_number: count all ACT-ACT pattern
- all_bank_act_pre_number: count all ACT-PRE pattern
- all_bank_act_rdwr_same_number: count ACT-RD and ACT-WR pattern, which active command and read/write command with the same rank, same bank and same row.
- all_bank_rd2wr_number: count all RD-WR pattern.
- all_bank_wr2rd_number: count all WR-RD pattern.
- all_bank_series_rd_total_cnt_number: count all back to back read pattern.
- all_bank_series_wr_total_cnt_number: count all back to back write pattern.
- all_bank_series_rd_burst_max_number: count the longest series read command.
- all_bank_series_wr_burst_max_number: count the longest series write command.
- all_bank_series_rd_burst_times_number: count the count of all series read command interval.
- all_bank_series_wr_burst_times_number: count the count of all series write command interval.
- all_bank_tccdmw_cnt_number: count all mask write command.

13.6.10.7 Hardware mode

In hardware mode, a dfi timer is used to specify a statistics period, the command statistics is done in the statistics period. The dfi timer is running in 24MHz. After dfi timer counts to the threshold, and update the statistics value, the dfi timer will restart automatically, and count again.

The steps of hardware mode of DDR access command statistics is as follows.

- Configure register DDRMON_CTRL.hardware_en as 1 to enable hardware mode.
- Configure register DDRMON_TIMER_COUNT to set the dfi timer count threshold, the statistics is done in the period of timer being less than the value of DDRMON_TIMER_COUNT.

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- Configure register DDRMON_CTRL.lpddr23_en or DDRMON_CTRL.ddr4_en or DDRMON_CTRL.ddr3_en or DDRMON_CTRL.lpddr4_en to set the DDR mode. Notice that DDR2 and DDR3 use the same mode.
- Configure register CS_CONTROL.rank_cs_num, if there is only one rank.
- Configure register DDRMON_FLOOR_NUMBER to specify the low threshold of interrupt, and configure register DDRMON_TOP_NUMBER to specify the high threshold of interrupt.
- Configure register DDRMON_CTRL.timer_cnt_en as 1 to start hardware mode.
- Wait for the interrupt to do following process. We also can read the read, write and active command number separately.

13.6.10.8 Software mode

In software mode, the statistics is controlled by software.
The steps of hardware mode of DDR access command statistics is as follows.

- Configure register DDRMON_CTRL to set the DDR mode like hardware mode.
- Configure register DDRMON_CTRL.software_en as 1 to enable software mode statistics.

Configure register DDRMON_CTRL.software_en as 0 to stop the statistics, and generate the statistics result. We can read the read, write and active command number separately.

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Chapter 14 DDR Converter of Frequency (DCF)

14.1 Overview

DDR Converter of Frequency (DCF) is used to implement DDR frequency conversion without the participation of CPU. DCF is connected to SOC through an AXI Master and an APB Slave, with a DMAC and instruction buffer inside. Beforehand, software puts into SRAM formulary pieces of instructions which consist of all the register-related configurations in the process of frequency conversion. When started-up, DCF automatically reads instructions to the inside buffer by means of DMA, and implement register configuration after analysis. A done signal will be provided for CPU after all the instructions are analyzed.
DCF supports the following features:

- AMBA 32-bit AXI compliant
- Support DMA operation from SRAM to buffer
  - Support burst8 only
  - LLP not supported
- Support 2 internal instruction registers: r0 & r1
- Support following software instructions:
  - IDL (delay)
  - LDR (read register)
  - STR (write register)
  - ISB (write with flush)
  - Bitwise AND
  - Bitwise OR
  - Bitwise INV
  - LSR (left shift)
  - RSR (right shift)
  - ADD
  - SUB
  - POLLEQ (poll a register until the value match)
  - POLLNEQ (poll a register until the value mismatch)
  - CMPEQ (compare if equal)
  - CMPNEQ (compare if unequal)
  - BL (jump upwards or downwards, 8bytes align)
- Support following program functions through combination of basic instructions
  - If-else
  - while
  - loop
  - for

14.2 Block Diagram

DCF is comprised of:

- An AXI Master Interface
- An APB Slave Interface
- A DMA controller
- An Instruction Buffer
- Instruction analyzer

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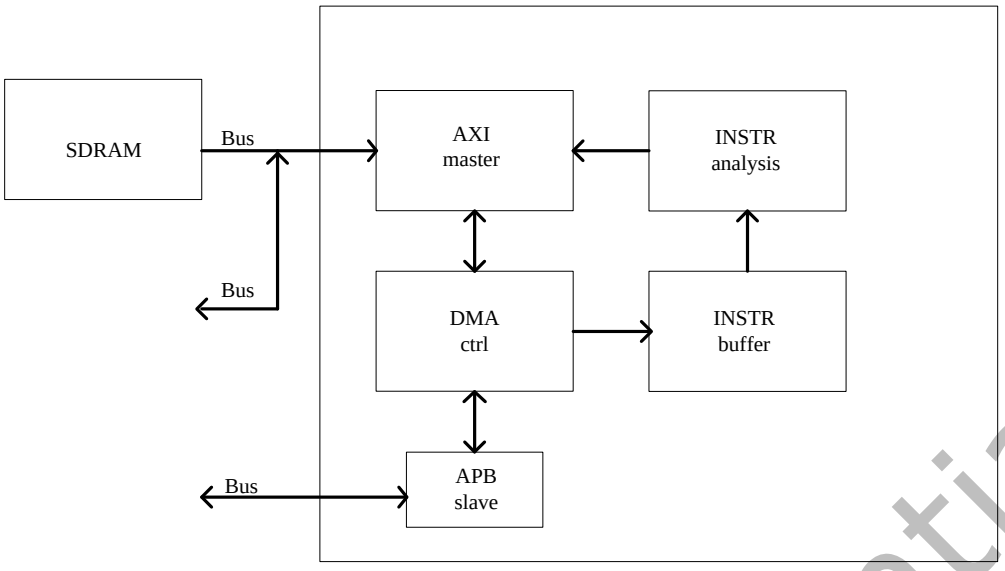


Fig.14-1 DCF Block Diagram

14.3 Register Description

14.3.1 Registers Summary

Name	Offset	Size	Reset Value	Description
DCF_CTRL	0x0000	W	0x00000000	DCF Control Register
DCF_STATUS	0x0004	W	0x00000001	DCF Internal Status Register
DCF_ADDR	0x0008	W	0x00000000	DCF Instruction Start Address Register
DCF_ISR	0x000C	W	0x00000000	DCF Interrupt Status Register
DCF_TIMEOUT_CYC	0x0014	W	0xFFFFFFFF	DCF Instruction Timeout Cycle Register
DCF_CURR_R0	0x0020	W	0x00000000	Current Internal R0 Value Register
DCF_CURR_R1	0x0024	W	0x00000000	Current Internal R1 Value Register
DCF_CMD_COUNTER	0x0028	W	0x00000000	Current Command Counter Value Register
DCF_LAST_ADDR1	0x0030	W	0x00000000	Last 1 Instruction Address Register
DCF_LAST_ADDR2	0x0034	W	0x00000000	Last 2 Instruction Address Register
DCF_LAST_ADDR3	0x0038	W	0x00000000	Last 3 Instruction Address Register
DCF_LAST_ADDR4	0x003C	W	0x00000000	Last 4 Instruction Address Register

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

14.3.2 Detail Registers Description

DCF_CTRL

Address: Operational Base(0xFFB00000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
2	RW	0x0	vop_hw_en 1'b1 : Enable 1'b0 : Disable
1	R/WSC	0x0	timeout_en 1'b1: Enable 1'b0: Disable
0	R/WSC	0x0	start This bit will be auto cleared when DCF is done. 1'b1: Start DCF 1'b0: Stop DCF

DCF_STATUS

Address: Operational Base(0xFFB00000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	W1C	0x0	dma_done_st 1'b1: DCF has fetched all the instructions.
6	W1C	0x0	instr_done_st 1'b1: DCF has done all the instructions analysis.
5	W1C	0x0	dma_error_st 1'b1 : Error response received when DCF is fetching instructions.
4	W1C	0x0	instr_error_st 1'b1 : Error response received when DCF is handling instructions.
3	W1C	0x0	dcf_timeout_st 1'b1: DCF timeout
2	W1C	0x0	dcf_edge_trigger_st 1'b1 : DCF is triggered by dma_finish from vop.
1	W1C	0x0	dcf_level_trigger_st 1'b1 : DCF is triggered by one of the following sources: vop_standby / vop_clockgating / vop_powndown
0	RO	0x1	dcf_idle_st 1'b1 : DCF is idle 1'b0 : DCF is busy

DCF_ADDR

Address: Operational Base(0xFFB00000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	addr DCF instruction fetch start address

DCF_ISR

Address: Operational Base(0xFFB00000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
1	W1C	0x0	dcf_error 1'b1: Error response or timeout during DDR change frequency.
0	W1C	0x0	dcf_done 1'b1: DDR change frequency completed. 1'b0: DDR change frequency not completed.

DCF_TIMEOUT_CYC

Address: Operational Base(0xFFB00000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0xffffffff	timeout Calculated by axi clock

DCF_CURR_R0

Address: Operational Base(0xFFB00000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	curr_r0 R0 value is sampled when dcf_done or dcf_error occurs.

DCF_CURR_R1

Address: Operational Base(0xFFB00000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	curr_r1 R1 value is sampled when dcf_done or dcf_error occurs.

DCF_CMD_COUNTER

Address: Operational Base(0xFFB00000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	cmd_counter cmd_counter value is sampled when dcf_done or dcf_error occurs. it records the number of pieces of instructions among DCF.

DCF_LAST_ADDR1

Address: Operational Base(0xFFB00000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	last_addr1 Value is sampled when dcf_done or dcf_error occurs. it records the last 1 instruction address.

DCF_LAST_ADDR2

Address: Operational Base(0xFFB00000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	last_addr2 Value is sampled when dcf_done or dcf_error occurs. it records the last 2 instruction address.

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DCF_LAST_ADDR3

Address: Operational Base(0xFFB00000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	last_addr3 Value is sampled when dcf_done or dcf_error occurs. it records the last 3 instruction address.

DCF_LAST_ADDR4

Address: Operational Base(0xFFB00000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	last_addr4 Value is sampled when dcf_done or dcf_error occurs. it records the last 4 instruction address.

14.4 Application Notes

14.4.1 DCF Work Flow

1、 Software needs to open up a separate space in SRAM and loads a series of instructions in advance. The instruction should consist of:
   a、 Configure msch and cpu idle.
   b、 Configure Memory Controller to move DDR into Low-power State.
   c、 Reset DDRPHY if needed.
   d、 Configure Clock frequency, wait for PLL lock.
   e、 Configure all the Timing-relative registers.
   f、 De-assert DDRPHY reset if needed.
   g、 Initialize DDRPHY, do calibration.
   h、 Configure Memory Controller to move DDR into Access State.
2、 Software configure DCF, notifying the start_addr, and then start DCF.
3、 DCF will transfer instruction data through DMA from SRAM to an internal buffer.
4、 In the meanwhile, an instruction analysis module will read these instructions from buffer, and transform them to corresponding bus-relative operations, including Write&Read registers, delay some clock cycles, arithmetic operation and so on.
5、 By Axi master, DCF will configure uPCTL、DDRPHY、CRU module to implement the procedure of DDR frequency conversion.
6、 DCF will recognize the last command, and generate a dcf_done interrupt for CPU.

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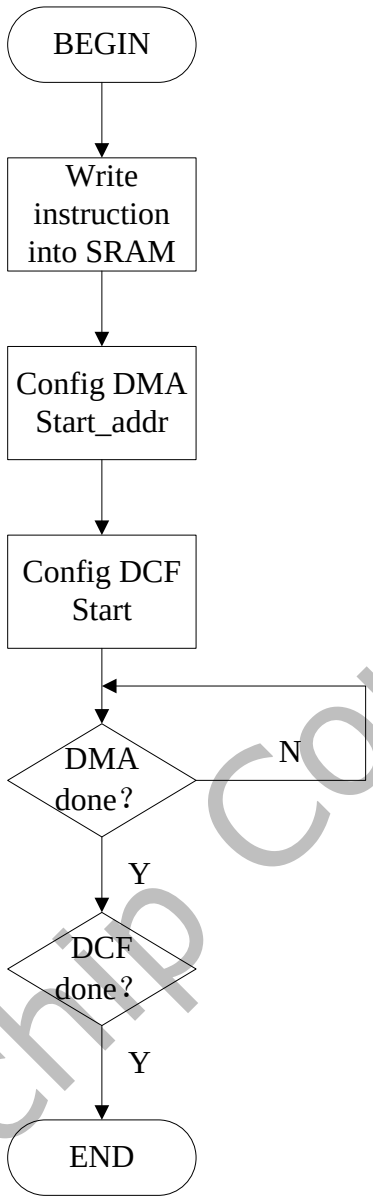


Fig.14-2 DCF Work Flow

14.4.2 Instruction Format

One piece of instruction, which is 64bit, should consist of the information of:

1、 Address
2、 Data
3、 Command

63:59	58:34	33:32	31:0
cmd[4:0]	addr[26:2]	(r1,r0)	data

The overall principle of instruction information is:

1、 Address[31:27] is reserved for 5bit command, which represents the corresponding operation.
2、 Address[1:0] is used to indicate operation of r0 or r1.

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3、 Address[26:2] is the real bus address. If 0, it means no bus operation; if not 0, it means a combination of 2 instructions with a bus operation ahead and an arithmetic c operation followed in order to improve efficiency.

For example, let us analyze the instruction: 0f620002_00000003

1、 Command is 1, which represents a bitwise AND operation.

2、 Address is 0xff620000, represents a bus-read operation.

3、 R1 is indicated, represents that the middle result is stored into internal register r1.

4、 Data is 0x00000003, represents that the operation value is 0x3.

So, this instruction will do following operations:

- LDR #0xff620000, r1; //read register 0xff620000, and store value into r1
- AND r1, 0x00000003; //r1 is bitwise AND with 0x3, and re-store the result

The following table lists all the supported command

INSTR	cmd[4:0]	addr[26:2]	R1	R0	Data[31:0]	
IDLE	5'h00	NA	NA	NA	#data	IDL #data
AND	5'h01	#addr	0	0	NA	ldr #addr r0 ; ldr #addr r1
			0	1	#data	ldr #addr r0 ; AND r0 #data
			1	0	#data	ldr #addr r1 ; AND r1 #data
			1	1	NA	ldr #addr r1 ; AND r1 r0
		All 0	0	0	NA	mov r0 r0 ; mov r1 r1
			0	1	#data	AND r0 #data
			1	0	#data	AND r1 #data
			1	1	NA	AND r1 r0
OR	5'h02	#addr	0	0	NA	ldr #addr r0 ; ldr #addr r1
			0	1	#data	ldr #addr r0 ; OR r0 #data
			1	0	#data	ldr #addr r1 ; OR r1 #data
			1	1	NA	ldr #addr r1 ; OR r1 r0
		All 0	0	0	NA	mov r0 r0 ; mov r1 r1
			0	1	#data	OR r0 #data
			1	0	#data	OR r1 #data
			1	1	NA	OR r1 r0
INV	5'h03	#addr	0	0	NA	ldr #addr r0 ; ldr #addr r1
			0	1	#data	ldr #addr r0 ; XOR r0 ^#data
			1	0	#data	ldr #addr r1 ; XOR r1 ^#data
			1	1	#data	ldr #addr r1 ; XOR r1 ^r0
		All 0	0	0	NA	mov r0 r0 ; mov r1 r1
			0	1	NA	INV r0
			1	0	NA	INV R1
			1	1	NA	SWP r0 r1
LSR	5'h04	#addr	0	0	NA	ldr #addr r0 ; ldr #addr r1
			0	1	#data	ldr #addr r0 ; LSR r0 #data
			1	0	#data	ldr #addr r1 ; LSR r1 #data
			1	1	NA	ldr #addr r1 ; LSR r1 r0
		All 0	0	0	NA	mov r0 r0 ; mov r1 r1
			0	1	#data	LSR r0 #data
			1	0	#data	LSR r1 #data
			1	1	NA	LSR r1 r0

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INSTR	cmd[4:0]	addr[26:2]	R1	R0	Data[31:0]	
RSR	5'h05	#addr	0	0	NA	ldr #addr r0 ; ldr #addr r1
			0	1	#data	ldr #addr r0 ; RSR r0 #data
			1	0	#data	ldr #addr r1 ; RSR r1 #data
			1	1	NA	ldr #addr r1 ; RSR r1 r0
		All 0	0	0	NA	mov r0 r0 ; mov r1 r1
			0	1	#data	RSR r0 #data
			1	0	#data	RSR r1 #data
			1	1	NA	RSR r1 r0
CMPEQ	5'h06	#addr	0	0	NA	ldr #addr r0 ; ldr #addr r1
			0	1	#data	ldr #addr r0 ; CMPEQ r0 #data,flag
			1	0	#data	ldr #addr r0 ; CMPEQ r1 #data,flag
			1	1	NA	ldr #addr r0 ; CMPEQ r1 r0,flag
		All 0	0	0	NA	mov r0 r0 ; mov r1 r1
			0	1	#data	CMPEQ r0 #data, flag
			1	0	#data	CMPEQ r1 #data, flag
			1	1	NA	CMPEQ r1 r0, flag
CMPNE	5'h07	#addr	0	0	NA	ldr #addr r0 ; ldr #addr r1
			0	1	#data	ldr #addr r0 ; CMPNE r0 #data,flag
			1	0	#data	ldr #addr r1 ; CMPNE r1 #data,flag
			1	1	NA	ldr #addr r1 ; CMPNE r1 r0,flag
		All 0	0	0	NA	mov r0 r0 ; mov r1 r1
			0	1	#data	CMPNE r0 #data, flag
			1	0	#data	CMPNE r1 #data, flag
			1	1	NA	CMPNE r1 r0, flag
ADD	5'h08	#addr	0	0	NA	ldr #addr r0 ; ldr #addr r1
			0	1	#data	ldr #addr r0 ; ADD r0 #data
			1	0	#data	ldr #addr r0 ; ADD r1 #data
			1	1	NA	ldr #addr r0 ; ADD r1 r0
		All 0	0	0	NA	mov r0 r0 ; mov r1 r1
			0	1	#data	ADD r0 #data
			1	0	#data	ADD r1 #data
			1	1	NA	ADD r1 r0
SUB	5'h09	#addr	0	0	NA	ldr #addr r0 ; ldr #addr r1
			0	1	#data	ldr #addr r0 ; SUB r0 #data
			1	0	#data	ldr #addr r0 ; SUB r1 #data
			1	1	NA	ldr #addr r0 ; SUB r1 r0
		All 0	0	0	NA	mov r0 r0 ; mov r1 r1
			0	1	#data	SUB r0 #data
			1	0	#data	SUB r1 #data
			1	1	NA	SUB r1 r0
STR	5'h0a	#addr	0	0	#data	STR #addr #data
			0	1	NA	STR #ADDR r0
			1	0	NA	STR #ADDR r1
			1	1	#data	STR #addr #data

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INSTR	cmd[4:0]	addr[26:2]	R1	R0	Data[31:0]	
ISB	5'h0b	#addr	0	0	#data	STR #addr #data
			0	1	NA	STR #ADDR r0
			1	0	NA	STR #ADDR r1
			1	1	#data	STR #addr #data
POLEQ	5'h0c	NA	0	1	#data	poll r0=#data,repeat last command
			1	0	#data	poll r1=#data,repeat last command
			1	1	NA	poll r1=r0,repeat last command
POLNEQ	5'h0d	NA	0	1	#data	poll r0!=#data,repeat last command
			1	0	#data	poll r1!=#data,repeat last command
			1	1	NA	poll r1!=r0,repeat last command
BL_U	5'h0e	ALL 0	NA	NA	#data	brr #data,?flag (upwards)
			0	1	NA	brr r0, ?flag
			1	0	NA	brr r1, ?flag
		ALL 1	NA	NA	#data	brr #data (upwards)
			0	1	NA	brr r0
			1	0	NA	brr r1
BL_D	5'h0f	ALL 0	NA	NA	#data	brr #data,?flag (downwards)
			0	1	NA	brr r0, ?flag
			1	0	NA	brr r1, ?flag
		ALL 1	NA	NA	#data	brr #data (downwards)
			0	1	NA	brr r0
			1	0	NA	brr r1
DMA_S	5'h10	NA	NA	NA	#data	set dma_start_addr = #data
DMA_D	5'h11	NA	NA	NA	#data	set dma_end_addr = #data
DMA_DO	5'h12	NA	NA	NA	#data	set dma_length = #data (byte) dma_start
END	5'h13	NA	NA	NA	NA	End of instruction

14.4.3 Hardware Trigger Flow

When DCF_CTRL.vop_hw_en is enabled, DCF can be triggered by any of the followed three sources: dma_finish 、vop_standby、vop_clkgate_en.

DCF is edge sensitive for dma_finish signal, and level sensitive for vop_standby and vop_clkgate_en signal.

When DCF is working, a dcf_idle is driven to low to indicate vop not to exit vop_standby status. And when DCF is not working, dcf_idle is driven to high for SOC and VOP to inquire.

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Chapter 15 SPINLOCK

15.1 Overview

The hardware spinlock used for spinlock status storage. All the CPU can access spinlock to get the lock status.

15.2 Block Diagram

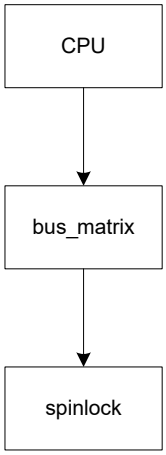


Fig.15-1 Spinlock in System

15.3 Register Description

15.3.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

15.3.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SPINLOCK_status_n (range of n is 0~63)	0x0+4*n	W	0x00000000	spinlock status controller register_n

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

15.3.3 Detail Register Description

SPINLOCK_status_n

Address: Operational Base(0xFF9E0000) + offset (0x0000+4*n)

Bit	Attr	Reset Value	Description
31:4	RO	0x000000	reserved reserved
3:0	RW	0x0	spinlock_status when 4bits is 0, 4bits can be written with new value. when 4bits is not 0, 4bits cannot be written. when write data is 0x0000, 4bits clean to 0.

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Chapter 16 CRYPTO

16.1 Overview

CRYPTO is a hardware accelerator for encrypting or decrypting. It supports the most commonly used algorithm: symmetric block cipher, HASH and PKA.

The CRYPTO supports following features:

- Support Link List Item (LLI) DMA transfer
- Support SHA-1, SHA-256/224, MD5 with hardware padding
- Support HMAC of SHA-1, SHA-256, MD5 with hardware padding
- Support AES-128, AES-192, AES-256 cipher
- Support DES & TDES cipher
- Support AES ECB/CBC/OFB/CFB/CTR/CTS/XTS/CCM/GCM/CBC-MAC/CMAC mode
- Support DES/TDES ECB/CBC/OFB/CFB mode
- Support up to 4096 bits PKA mathematical operations for RSA
- Support data output directly, without calculation
- Support using the key in KEY TABLE as encryption and decryption key

16.2 Block Diagram

CRYPTO contains several modules: AHB Slave, DMA, CIPHER, PKA, GRANT, KEY TABLE, APB Master.

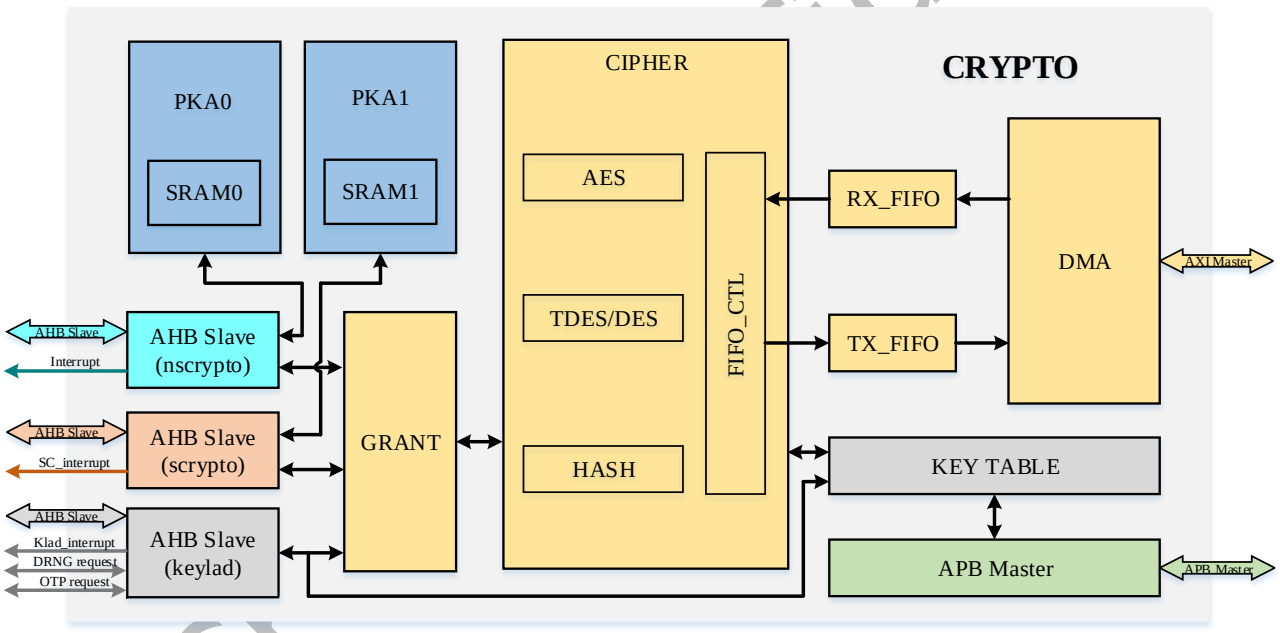


Fig.16-1 Crypot Architecture

16.3 Function Description

16.3.1 AHB Interface

There are three AHB slave interfaces in CRYPTO, AHB Slave(nscrypto) is used to configure registers in non-secure world, AHB Slave(scrypto) and AHB Slave(keylad) are used to configure registers in secure world. These modules are in hclk domain.

16.3.2 DMA

DMA is used to transfer data from external memory to RX_FIFO, or from TX_FIFO to external memory. DMA uses AXI3 protocol with 33-bits address width, 64-bits data width and max burst length to 16. LLI transfer is also supported for performance and convenience consideration. This module is in aclk domain.

16.3.3 CIPHER

CIPHER contains AES, DES/TDES and HASH engines. And it also supports various mode operations. The source data is either from RX_FIFO, or from other engine output. The

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result data is sending either to TX_FIFO, or Registers in module AHB_Slave. This module is in clk_core domain.

16.3.4 PKA

PKA is used to accelerate mathematical operations for big numbers. It supports - Modular arithmetic (addition, subtraction, multiplication and division), Regular arithmetic (addition, subtraction, multiplication and division), Modular inversion, Modular exponentiation, Logical operations (AND, OR, XOR, SHIFT). PKA has a SRAM which is used to store source, result and intermediate data for PKA operations. The software driver could use PKA operations to implement complicate calculation, such as RSA, ECC etc. It could support up to 4096 bits RSA modular exponentiation calculation. This module is in clk_pka domain.

16.3.5 KEY TABLE

KEY TABLE is used to receive and temporarily store the KEY sent by KEYLAD through APB, and provide the KEY to CIPHER operation. The size of KEY TABLE that CRYPTO can use is 16 word. This module is in aclk domain.

16.4 Register Description

16.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

16.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
CRYPTO_CLK_CTL	0x0000	W	0x00000001	Clock Control Register
CRYPTO_RST_CTL	0x0004	W	0x00000000	Reset Control Register
CRYPTO_DMA_INT_EN	0x0008	W	0x00000000	DMA Interrupt Enable Register
CRYPTO_DMA_INT_ST	0x000C	W	0x00000000	DMA Interrupt Status Register
CRYPTO_DMA_CTL	0x0010	W	0x00000000	DMA Control Register
CRYPTO_DMA_LLI_ADDR	0x0014	W	0x00000000	DMA LIST Start Address Register
CRYPTO_DMA_ST	0x0018	W	0x00000000	DMA Status Register
CRYPTO_DMA_STATE	0x001C	W	0x00000000	DMA State Register
CRYPTO_DMA_LLI_RADDR	0x0020	W	0x00000000	DMA LLI Read Address Register
CRYPTO_DMA_SRC_RADDR	0x0024	W	0x00000000	DMA Source Data Read Address Register
CRYPTO_DMA_DST_WADDR	0x0028	W	0x00000000	DMA Destination Data Read Address Register
CRYPTO_DMA_ITEM_ID	0x002C	W	0x00000000	DMA Descriptor ID Register
CRYPTO_BC_CTL	0x0044	W	0x00000000	Block Cipher Control Register
CRYPTO_HASH_CTL	0x0048	W	0x00000004	Hash Control Register
CRYPTO_CIPHER_ST	0x004C	W	0x00000000	Cipher Status Register
CRYPTO_CIPHER_STATE	0x0050	W	0x00000400	Cipher Current State Register
CRYPTO_BC_MID_IV_0	0x0060	W	0x00000000	Block Cipher Median IV 0
CRYPTO_BC_MID_IV_1	0x0064	W	0x00000000	Block Cipher Median IV 1
CRYPTO_BC_MID_IV_2	0x0068	W	0x00000000	Block Cipher Median IV 2
CRYPTO_BC_MID_IV_3	0x006C	W	0x00000000	Block Cipher Median IV 3
CRYPTO_BC_MID_IV_4	0x0070	W	0x00000000	Block Cipher Median IV 4
CRYPTO_BC_MID_IV_5	0x0074	W	0x00000000	Block Cipher Median IV 5
CRYPTO_CH0_IV_0	0x0100	W	0x00000000	Channel 0 iv 0
CRYPTO_CH0_IV_1	0x0104	W	0x00000000	Channel 0 iv 1
CRYPTO_CH0_IV_2	0x0108	W	0x00000000	Channel 0 iv 2
CRYPTO_CH0_IV_3	0x010C	W	0x00000000	Channel 0 iv 3
CRYPTO_CH0_KEY_0	0x0180	W	0x00000000	Channel 0 key 0
CRYPTO_CH0_KEY_1	0x0184	W	0x00000000	Channel 0 key 1
CRYPTO_CH0_KEY_2	0x0188	W	0x00000000	Channel 0 key 2
CRYPTO_CH0_KEY_3	0x018C	W	0x00000000	Channel 0 key 3
CRYPTO_CH1_KEY_0	0x0190	W	0x00000000	Channel 1 key 0

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Name	Offset	Size	Reset Value	Description
CRYPTO_CH1_KEY_1	0x0194	W	0x00000000	Channel 1 key 1
CRYPTO_CH1_KEY_2	0x0198	W	0x00000000	Channel 1 key 2
CRYPTO_CH1_KEY_3	0x019C	W	0x00000000	Channel 1 key 3
CRYPTO_CH2_KEY_0	0x01A0	W	0x00000000	Channel 2 key 0
CRYPTO_CH2_KEY_1	0x01A4	W	0x00000000	Channel 2 key 1
CRYPTO_CH2_KEY_2	0x01A8	W	0x00000000	Channel 2 key 2
CRYPTO_CH2_KEY_3	0x01AC	W	0x00000000	Channel 2 key 3
CRYPTO_CH3_KEY_0	0x01B0	W	0x00000000	Channel 3 key 0
CRYPTO_CH3_KEY_1	0x01B4	W	0x00000000	Channel 3 key 1
CRYPTO_CH3_KEY_2	0x01B8	W	0x00000000	Channel 3 key 2
CRYPTO_CH3_KEY_3	0x01BC	W	0x00000000	Channel 3 key 3
CRYPTO_CH4_KEY_0	0x01C0	W	0x00000000	Channel 4 key 0
CRYPTO_CH4_KEY_1	0x01C4	W	0x00000000	Channel 4 key 1
CRYPTO_CH4_KEY_2	0x01C8	W	0x00000000	Channel 4 key 2
CRYPTO_CH4_KEY_3	0x01CC	W	0x00000000	Channel 4 key 3
CRYPTO_CH5_KEY_0	0x01D0	W	0x00000000	Channel 5 key 0
CRYPTO_CH5_KEY_1	0x01D4	W	0x00000000	Channel 5 key 1
CRYPTO_CH5_KEY_2	0x01D8	W	0x00000000	Channel 5 key 2
CRYPTO_CH5_KEY_3	0x01DC	W	0x00000000	Channel 5 key 3
CRYPTO_CH6_KEY_0	0x01E0	W	0x00000000	Channel 6 key 0
CRYPTO_CH6_KEY_1	0x01E4	W	0x00000000	Channel 6 key 1
CRYPTO_CH6_KEY_2	0x01E8	W	0x00000000	Channel 6 key 2
CRYPTO_CH6_KEY_3	0x01EC	W	0x00000000	Channel 6 key 3
CRYPTO_CH7_KEY_0	0x01F0	W	0x00000000	Channel 7 key 0
CRYPTO_CH7_KEY_1	0x01F4	W	0x00000000	Channel 7 key 1
CRYPTO_CH7_KEY_2	0x01F8	W	0x00000000	Channel 7 key 2
CRYPTO_CH7_KEY_3	0x01FC	W	0x00000000	Channel 7 key 3
CRYPTO_CH0_PC_LEN_0	0x0280	W	0x00000000	Channel 0 pc_len_0
CRYPTO_CH0_PC_LEN_1	0x0284	W	0x00000000	Channel 0 pc_len_1
CRYPTO_CH0_AAD_LEN_0	0x02C0	W	0x00000000	Channel 0 aad_len_0
CRYPTO_CH0_AAD_LEN_1	0x02C4	W	0x00000000	Channel 0 aad_len_1
CRYPTO_CH0_IV_LEN_0	0x0300	W	0x00000000	Channel 0 iv_len_0
CRYPTO_CH0_TAG_0	0x0320	W	0x00000000	Channel 0 tag 0
CRYPTO_CH0_TAG_1	0x0324	W	0x00000000	Channel 0 tag 1
CRYPTO_CH0_TAG_2	0x0328	W	0x00000000	Channel 0 tag 2
CRYPTO_CH0_TAG_3	0x032C	W	0x00000000	Channel 0 tag 3
CRYPTO_HASH_DOUT_0	0x03A0	W	0x00000000	HASH Data Output Register 0
CRYPTO_HASH_DOUT_1	0x03A4	W	0x00000000	HASH Data Output Register 1
CRYPTO_HASH_DOUT_2	0x03A8	W	0x00000000	HASH Data Output Register 2
CRYPTO_HASH_DOUT_3	0x03AC	W	0x00000000	HASH Data Output Register 3
CRYPTO_HASH_DOUT_4	0x03B0	W	0x00000000	HASH Data Output Register 4
CRYPTO_HASH_DOUT_5	0x03B4	W	0x00000000	HASH Data Output Register 5
CRYPTO_HASH_DOUT_6	0x03B8	W	0x00000000	HASH Data Output Register 6
CRYPTO_HASH_DOUT_7	0x03BC	W	0x00000000	HASH Data Output Register 7
CRYPTO_TAG_VALID	0x03E0	W	0x00000000	TAG Valid Register
CRYPTO_HASH_VALID	0x03E4	W	0x00000000	HASH Output Valid Register
CRYPTO_MID_VALID	0x03E8	W	0x00000000	Block Cipher or Hash Middle Data is Valid
CRYPTO_RAM_CTL	0x0480	W	0x00000000	RAM Control Register
CRYPTO_RAM_ST	0x0484	W	0x00000001	RAM Status Register
CRYPTO_DEBUG_CTL	0x04A0	W	0x00000000	PKA Debug Control Register
CRYPTO_DEBUG_ST	0x04A4	W	0x00000001	PKA Debug Status Register

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Name	Offset	Size	Reset Value	Description
CRYPTO_DEBUG_MONITOR	0x04A8	W	0x0000FEEF	PKA Debug Monitor Bus Register
CRYPTO_CRYPTO_KL_KEY_STATUS	0x0600	W	0x00000000	Key Ladder's Key Valid
CRYPTO_CRYPTO_KEY_SEL	0x0610	W	0x00000000	Key Select Register
CRYPTO_CRYPTO_LOCKSTEP	0x0618	W	0x00000000	Lock Step Status Register
CRYPTO_CRYPTO_LOCKSTEP_EN	0x061C	W	0x00000000	Lock Step Enable Register
CRYPTO_MID_VALID_SWITCH	0x0630	W	0x00000000	How the application obtains MID_VALID_DATA
CRYPTO_AES_VERSION	0x0680	W	0x000717FF	AES_VERSION
CRYPTO_DES_VERSION	0x0684	W	0x00070033	DES_VERSION
CRYPTO_SM4_VERSION	0x0688	W	0x00000000	SM4_VERSION
CRYPTO_HASH_VERSION	0x068C	W	0x00000087	HASH_VERSION
CRYPTO_HMAC_VERSION	0x0690	W	0x0000000B	HMAC_VERSION
CRYPTO_PKA_VERSION	0x0698	W	0x01000000	PKA_VERSION
CRYPTO_EXTRA_FEATURE	0x069C	W	0x00000002	Extra Feature Register
CRYPTO_CRYPTO_VERSION	0x06F0	W	0x04000001	CRYPTO_VERSION
CRYPTO_HASH_MID_DATA_0	0x0700	W	0x00000000	Hash Mid Data 0 Register
CRYPTO_HASH_MID_DATA_1	0x0704	W	0x00000000	Hash Mid Data 1 Register
CRYPTO_HASH_MID_DATA_2	0x0708	W	0x00000000	Hash Mid Data 2 Register
CRYPTO_HASH_MID_DATA_3	0x070C	W	0x00000000	Hash Mid Data 3 Register
CRYPTO_HASH_MID_DATA_4	0x0710	W	0x00000000	Hash Mid Data 4 Register
CRYPTO_HASH_MID_DATA_5	0x0714	W	0x00000000	Hash Mid Data 5 Register
CRYPTO_HASH_MID_DATA_6	0x0718	W	0x00000000	Hash Mid Data 6 Register
CRYPTO_HASH_MID_DATA_7	0x071C	W	0x00000000	Hash Mid Data 7 Register
CRYPTO_HASH_MID_DATA_8	0x0720	W	0x00000000	Hash Mid Data 8 Register
CRYPTO_HASH_MID_DATA_9	0x0724	W	0x00000000	Hash Mid Data 9 Register
CRYPTO_HASH_MID_DATA_10	0x0728	W	0x00000000	Hash Mid Data 10 Register
CRYPTO_HASH_MID_DATA_11	0x072C	W	0x00000000	Hash Mid Data 11 Register
CRYPTO_HASH_MID_DATA_12	0x0730	W	0x00000000	Hash Mid Data 12 Register
CRYPTO_HASH_MID_DATA_13	0x0734	W	0x00000000	Hash Mid Data 13 Register
CRYPTO_HASH_MID_DATA_14	0x0738	W	0x00000000	Hash Mid Data 14 Register
CRYPTO_HASH_MID_DATA_15	0x073C	W	0x00000000	Hash Mid Data 15 Register

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Name	Offset	Size	Reset Value	Description
CRYPTO_HASH_MID_DATA_16	0x0740	W	0x00000000	Hash Mid Data 16 Register
CRYPTO_HASH_MID_DATA_17	0x0744	W	0x00000000	Hash Mid Data 17 Register
CRYPTO_HASH_MID_DATA_18	0x0748	W	0x00000000	Hash Mid Data 18 Register
CRYPTO_HASH_MID_DATA_19	0x074C	W	0x00000000	Hash Mid Data 19 Register
CRYPTO_HASH_MID_DATA_20	0x0750	W	0x00000000	Hash Mid Data 20 Register
CRYPTO_HASH_MID_DATA_21	0x0754	W	0x00000000	Hash Mid Data 21 Register
CRYPTO_HASH_MID_DATA_22	0x0758	W	0x00000000	Hash Mid Data 22 Register
CRYPTO_HASH_MID_DATA_23	0x075C	W	0x00000000	Hash Mid Data 23 Register
CRYPTO_HASH_MID_DATA_24	0x0760	W	0x00000000	Hash Mid Data 24 Register
CRYPTO_HASH_MID_DATA_25	0x0764	W	0x00000000	Hash Mid Data 25 Register
CRYPTO_PKA_MEM_MAP0	0x0800	W	0x00000000	PKA Memory Map 0 Register
CRYPTO_PKA_MEM_MAP1	0x0804	W	0x00000000	PKA Memory Map 1 Register
CRYPTO_PKA_MEM_MAP2	0x0808	W	0x00000000	PKA Memory Map 2 Register
CRYPTO_PKA_MEM_MAP3	0x080C	W	0x00000000	PKA Memory Map 3 Register
CRYPTO_PKA_MEM_MAP4	0x0810	W	0x00000000	PKA Memory Map 4 Register
CRYPTO_PKA_MEM_MAP5	0x0814	W	0x00000000	PKA Memory Map 5 Register
CRYPTO_PKA_MEM_MAP6	0x0818	W	0x00000000	PKA Memory Map 6 Register
CRYPTO_PKA_MEM_MAP7	0x081C	W	0x00000000	PKA Memory Map 7 Register
CRYPTO_PKA_MEM_MAP8	0x0820	W	0x00000000	PKA Memory Map 8 Register
CRYPTO_PKA_MEM_MAP9	0x0824	W	0x00000000	PKA Memory Map 9 Register
CRYPTO_PKA_MEM_MAP10	0x0828	W	0x00000000	PKA Memory Map 10 Register
CRYPTO_PKA_MEM_MAP11	0x082C	W	0x00000000	PKA Memory Map 11 Register
CRYPTO_PKA_MEM_MAP12	0x0830	W	0x00000000	PKA Memory Map 12 Register
CRYPTO_PKA_MEM_MAP13	0x0834	W	0x00000000	PKA Memory Map 13 Register
CRYPTO_PKA_MEM_MAP14	0x0838	W	0x00000000	PKA Memory Map 14 Register
CRYPTO_PKA_MEM_MAP15	0x083C	W	0x00000000	PKA Memory Map 15 Register
CRYPTO_PKA_MEM_MAP16	0x0840	W	0x00000000	PKA Memory Map 16 Register
CRYPTO_PKA_MEM_MAP17	0x0844	W	0x00000000	PKA Memory Map 17 Register
CRYPTO_PKA_MEM_MAP18	0x0848	W	0x00000000	PKA Memory Map 18 Register
CRYPTO_PKA_MEM_MAP19	0x084C	W	0x00000000	PKA Memory Map 19 Register
CRYPTO_PKA_MEM_MAP20	0x0850	W	0x00000000	PKA Memory Map 20 Register

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Name	Offset	Size	Reset Value	Description
CRYPTO_PKA_MEM_MAP21	0x0854	W	0x00000000	PKA Memory Map 21 Register
CRYPTO_PKA_MEM_MAP22	0x0858	W	0x00000000	PKA Memory Map 22 Register
CRYPTO_PKA_MEM_MAP23	0x085C	W	0x00000000	PKA Memory Map 23 Register
CRYPTO_PKA_MEM_MAP24	0x0860	W	0x00000000	PKA Memory Map 24 Register
CRYPTO_PKA_MEM_MAP25	0x0864	W	0x00000000	PKA Memory Map 25 Register
CRYPTO_PKA_MEM_MAP26	0x0868	W	0x00000000	PKA Memory Map 26 Register
CRYPTO_PKA_MEM_MAP27	0x086C	W	0x00000000	PKA Memory Map 27 Register
CRYPTO_PKA_MEM_MAP28	0x0870	W	0x00000000	PKA Memory Map 28 Register
CRYPTO_PKA_MEM_MAP29	0x0874	W	0x00000000	PKA Memory Map 29 Register
CRYPTO_PKA_MEM_MAP30	0x0878	W	0x00000000	PKA Memory Map 30 Register
CRYPTO_PKA_MEM_MAP31	0x087C	W	0x00000000	PKA Memory Map 31 Register
CRYPTO_PKA_OPCODE	0x0880	W	0x00000000	PKA Operation Code Register
CRYPTO_N_NP_T0_T1_ADDR	0x0884	W	0x000FF820	N_NP_T0_T1_ADDR Register
CRYPTO_PKA_STATUS	0x0888	W	0x00000001	PKA Status Register
CRYPTO_PKA_SW_RESET	0x088C	W	0x00000000	Software Reset of PKA
CRYPTO_PKA_L0	0x0890	W	0x00000000	PKA Length 0 Register
CRYPTO_PKA_L1	0x0894	W	0x00000000	PKA Length 1 Register
CRYPTO_PKA_L2	0x0898	W	0x00000000	PKA Length 2 Register
CRYPTO_PKA_L3	0x089C	W	0x00000000	PKA Length 3 Register
CRYPTO_PKA_L4	0x08A0	W	0x00000000	PKA Length 4 Register
CRYPTO_PKA_L5	0x08A4	W	0x00000000	PKA Length 5 Register
CRYPTO_PKA_L6	0x08A8	W	0x00000000	PKA Length 6 Register
CRYPTO_PKA_L7	0x08AC	W	0x00000000	PKA Length 7 Register
CRYPTO_PKA_PIPE_RDY	0x08B0	W	0x00000001	PKA ready for new Operation Code.
CRYPTO_PKA_DONE	0x08B4	W	0x00000001	PKA Done Register
CRYPTO_PKA_MON_SELECT	0x08B8	W	0x00000000	PKA Monitor Select Register
CRYPTO_PKA_DEBUG_REG_EN	0x08BC	W	0x00000000	PKA Debug Enable Register
CRYPTO_DEBUG_CNT_ADDR	0x08C0	W	0x00000000	Debug Counter Address Register
CRYPTO_DEBUG_EXT_ADDR	0x08C4	W	0x00000000	Debug Extra Address Register
CRYPTO_PKA_DEBUG_HALT	0x08C8	W	0x00000000	PKA Debug Halt State Register
CRYPTO_PKA_MON_READ	0x08D0	W	0x0000FEEF	PKA Monitor Read Register
CRYPTO_PKA_INT_ENA	0x08D4	W	0x00000000	PKA Interrupt Enable Register
CRYPTO_PKA_INT_ST	0x08D8	W	0x00000000	PKA Interrupt Status Register
CRYPTO_SRAM_ADDR	0x1000	W	0x00000000	SRAM Base Address

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

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16.4.3 Detail Registers Description

CRYPTO_CLK_CTL

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	WO	0x0	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x1	auto_clkgate_en CRYPTO will gate unused Block Cipher and HASH module automatically 1'b0: Disable 1'b1: Enable

CRYPTO_RST_CTL

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:16	RW	0x0	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2	R/WSC	0x0	sw_pka_reset Software set this bit to start a reset to PKA module. After the reset is done, CRYPTO will clear this bit.
1	RO	0x0	reserved
0	R/WSC	0x0	sw_cc_reset Software set this bit to start a reset to Symmetric Cipher and HASH module. After the reset is done, CRYPTO will clear this bit.

CRYPTO_DMA_INT_EN

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	unequal_len_int_en 1'b0: Disable 1'b1: Enable
8	RO	0x0	reserved
7	RW	0x0	lockstep_int_en 1'b0: Disable 1'b1: Enable
6	RW	0x0	zero_len_int_en 1'b0: Disable 1'b1: Enable
5	RW	0x0	list_err_int_en 1'b0: Disable 1'b1: Enable
4	RW	0x0	src_err_int_en 1'b0: Disable 1'b1: Enable
3	RW	0x0	dst_err_int_en 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
2	RW	0x0	src_item_done_int_en 1'b0: Disable 1'b1: Enable
1	RW	0x0	dst_item_done_int_en 1'b0: Disable 1'b1: Enable
0	RW	0x0	list_done_int_en 1'b0: Disable 1'b1: Enable

CRYPTO_DMA_INT_ST

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	unequal_len 1'b0: Nothing 1'b1: indicate that DMA has met an unequal transfer length in list descriptors. After the bit is read, the application should write 1 to clear this bit for next time use
8	RO	0x0	reserved
7	RW	0x0	lockstep_flag 1'b0: Nothing 1'b1: Indicate that crypto was attacked
6	RW	0x0	zero_len 1'b0: Nothing 1'b1: Indicate that DMA has met an 0 byte source transfer length in list descriptors. After the bit is read, the application should write 1 to clear this bit for next time use
5	RW	0x0	list_err 1'b0: Nothing 1'b1: Indicate that DMA has met an error response when transfer list descriptors. The state machine will exit current transfer and then return to IDLE state. After the bit is read, the application should write 1 to clear this bit for next time use
4	W1C	0x0	src_err 1'b0: Nothing 1'b1: Indicate that DMA has met an error response when transfer source data. The state machine will exit current transfer and then return to IDLE state. After the bit is read, the application should write 1 to clear this bit for next time use
3	W1C	0x0	dst_err 1'b0: Nothing 1'b1: Indicate that DMA has met an error response when transfer destination data. The state machine will exit current transfer and then return to IDLE state. After the bit is read, the application should write 1 to clear this bit for next time use
2	W1C	0x0	src_item_done 1'b0: Nothing 1'b1: Indicate that DMA has completed a read transfers which the current list descriptor pointed to. After the bit is read, the application should write 1 to clear this bit for next time use

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Bit	Attr	Reset Value	Description
1	W1C	0x0	dst_item_done 1'b0: Nothing 1'b1: Indicate that DMA has completed a write transfers which the current list descriptor pointed to. After the bit is read, the application should write 1 to clear this bit for next time use
0	W1C	0x0	list_done 1'b0: Nothing 1'b1: Indicate that DMA has completed all the transfers which the list descriptors pointed to. After the bit is read, the application should write 1 to clear this bit for next time use

CRYPTO_DMA_CTL

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	WO	0x0	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	R/WSC	0x0	dma_restart If DMA data for next stage is not ready, application could pause DMA by descriptor commands. DMA will stop prefetching next descriptor. The application could restart DMA by asserting this bit when DMA data for next state is ready. Crypto will continue with previous transfer, and clear the bit automatically.
0	R/WSC	0x0	dma_start DMA asserts the bit to start DMA transfer, then Crypto will clear the bit automatically.

CRYPTO_DMA_LLI_ADDR

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dma_lli_addr When DMA_CTL start asserted, Crypto will read the address to get the 1'st descriptor. It should be 8-bytes align. We suggest dma_lli_addr 64-byte align for best performance consideration.

CRYPTO_DMA_ST

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	dma_busy 1'b1: DMA busy 1'b0: DMA idle

CRYPTO_DMA_STATE

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
5:4	RO	0x0	dma_lli_state For debug use only 2'b00: IDLE STATE 2'b01: FETCH STATE 2'b10: WORK STATE Others: Reserved
3:2	RO	0x0	dma_src_state For debug use only 2'b00: IDLE STATE 2'b01: LOAD STATE 2'b10: WORK STATE Others: Reserved
1:0	RO	0x0	dma_dst_state For debug use only 2'b00: IDLE STATE 2'b01: LOAD STATE 2'b10: WORK STATE Others: Reserved

CRYPTO_DMA_LLI_RADDR

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dma_lli_raddr For debug use only It indicates the current DMA lli read address

CRYPTO_DMA_SRC_RADDR

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dma_src_raddr For debug use only It represents the value of the current DMA source read address shifted EXTRA_FEATURE.axi_expand_bit bits to the right

CRYPTO_DMA_DST_WADDR

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dma_dst_waddr For debug use only It represents the value of the current DMA destination write address shifted EXTRA_FEATURE.axi_expand_bit bits to the right

CRYPTO_DMA_ITEM_ID

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	dma_item_id For debug use only It indicates the current descriptor ID

CRYPTO_BC_CTL

Address: **Operational Base** + offset (0x0044)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	WO	0x000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9:8	RW	0x0	bc_cipher_sel 2'b00: AES 2'b01: SM4 2'b10: DES 2'b11: TDES Others: Reserved Note: The algorithm mode actually supported is subject to XXX_VERSION(XXX can be AES, DES, SM4)
7:4	RW	0x0	mode For AES 4'h0: ECB 4'h1: CBC 4'h2: CTS 4'h3: CTR 4'h4: CFB 4'h5: OFB 4'h6: XTS 4'h7: CCM 4'h8: GCM 4'h9: CMAC 4'hA: CBC-MAC Others: Reserved For TDES/DES 4'h0: ECB 4'h1: CBC 4'h4: CFB 4'h5: OFB Others: Reserved 4'hf: through Note: The algorithm mode actually supported is subject to XXX_VERSION(XXX can be AES, DES, SM4)
3:2	RW	0x0	key_size For AES 2'b00: 128 bit 2'b01: 192 bit 2'b10: 256 bit 2'b11: Reserved For TDES/DES, it is reserved
1	RW	0x0	decrypt 1'b0: Encrypt 1'b1: Decrypt
0	RW	0x0	bc_enable 1'b0: Disable 1'b1: Enable

CRYPTO_HASH_CTL

Address: **Operational Base** + offset (0x0048)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
23:16	WO	0x00	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:4	RW	0x0	hash_cipher_sel 4'h0: SHA-1 4'h1: MD-5 4'h2: SHA-256 4'h3: SHA-224 4'h6: SM3 4'h8: SHA-512 4'h9: SHA-384 4'hA: SHA-512/224 4'hB: SHA-512/256 Others: Reserved Note: The algorithm mode actually supported is subject to XXX_VERSION(XXX can be HASH, HMAC)
3	RW	0x0	hmac_enable Crypto supports HMAC-SHA1, HMAC-SHA256, HMAC_SHA512, HMAC-MD5, HMAC-SM3 1'b0: Disable 1'b1: Enable Note: If hmac_enable set '1', hash_cipher_sel must set 0x6 when chose HMAC-SM3 mode, hash_cipher_sel set the corresponding value when chose other mode
2	RW	0x1	hw_pad_enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	hash_src_sel 1'b0: From RX-FIFO 1'b1: From TX-FIFO
0	RW	0x0	hash_enable 1'b0: Disable 1'b1: Enable

CRYPTO_CIPHER_ST

Address: **Operational Base** + offset (0x004C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	hash_busy 1'b0: IDLE 1'b1: BUSY
0	RO	0x0	block_cipher_busy 1'b0: IDLE 1'b1: BUSY

CRYPTO_CIPHER_STATE

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
14:10	RO	0x01	hash_state For debug use only 5'h01: IDLE State 5'h02: IPAD State 5'h04: TEXT State 5'h08: OPAD State 5'h10: OPAD EXT State
9:8	RO	0x0	gcm_state For debug use only 2'b00: IDLE State 2'b01: PRE State 2'b10: NA State 2'b11: PC State
7:6	RO	0x0	ccm_state For debug use only 2'b00: IDLE State 2'b01: PRE State 2'b10: NA State 2'b11: PC State
5:4	RO	0x0	parallel_state For debug use only 2'b00: IDLE State 2'b01: PRE State 2'b10: BULK State Others: Reserved
3:2	RO	0x0	mac_state For debug use only 2'b00: IDLE State 2'b01: PRE State 2'b10: BULK State Others: Reserved
1:0	RO	0x0	serial_state For debug use only 2'b00: IDLE State 2'b01: PRE State 2'b10: BULK State 2'b11: Reserved

CRYPTO_BC_MID_IV_0

Address: **Operational Base** + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	bc_mid_iv_0 BC_MID_IV_0[31:0]

CRYPTO_BC_MID_IV_1

Address: **Operational Base** + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	bc_mid_iv_1 BC_MID_IV_1[31:0]

CRYPTO_BC_MID_IV_2

Address: **Operational Base** + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	bc_mid_iv_2 BC_MID_IV_2[31:0]

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CRYPTO_BC_MID_IV_3

Address: **Operational Base** + offset (0x006C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	bc_mid_iv_3 BC_MID_IV_3[31:0]

CRYPTO_BC_MID_IV_4

Address: **Operational Base** + offset (0x0070)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	bc_mid_iv_4 BC_MID_IV_4[31:0]

CRYPTO_BC_MID_IV_5

Address: **Operational Base** + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	bc_mid_iv_5 BC_MID_IV_5[31:0]

CRYPTO_CH0_IV_0

Address: **Operational Base** + offset (0x0100)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ch0_iv_0 Channel 0 IV[127:96].

CRYPTO_CH0_IV_1

Address: **Operational Base** + offset (0x0104)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ch0_iv_1 Channel 0 IV[95:64].

CRYPTO_CH0_IV_2

Address: **Operational Base** + offset (0x0108)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ch0_iv_2 Channel 0 IV[63:32].

CRYPTO_CH0_IV_3

Address: **Operational Base** + offset (0x010C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ch0_iv_3 Channel 0 IV[31:0].

CRYPTO_CH0_KEY_0

Address: **Operational Base** + offset (0x0180)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	ch0_key_0 Channel 0 Key[127:96].

CRYPTO_CH0_KEY_1

Address: **Operational Base** + offset (0x0184)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	ch0_key_1 Channel 0 Key[95:64].

CRYPTO_CH0_KEY_2

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Address: **Operational Base** + offset (0x0188)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	ch0_key_2 Channel 0 Key[63:32].

CRYPTO_CH0_KEY_3

Address: **Operational Base** + offset (0x018C)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	ch0_key_3 Channel 0 Key[31:0].

CRYPTO_CH1_KEY_0

Address: **Operational Base** + offset (0x0190)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	ch1_key_0 Channel 1 Key[127:96].

CRYPTO_CH1_KEY_1

Address: **Operational Base** + offset (0x0194)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	ch1_key_1 Channel 1 Key[95:64].

CRYPTO_CH1_KEY_2

Address: **Operational Base** + offset (0x0198)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	ch1_key_2 Channel 1 Key[63:32].

CRYPTO_CH1_KEY_3

Address: **Operational Base** + offset (0x019C)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	ch1_key_3 Channel 1 Key[31:0].

CRYPTO_CH2_KEY_0

Address: **Operational Base** + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	ch2_key_0 Channel 2 Key[127:96].

CRYPTO_CH2_KEY_1

Address: **Operational Base** + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	ch2_key_1 Channel 2 Key[95:64].

CRYPTO_CH2_KEY_2

Address: **Operational Base** + offset (0x01A8)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	ch2_key_2 Channel 2 Key[63:32].

CRYPTO_CH2_KEY_3

Address: **Operational Base** + offset (0x01AC)

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Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	ch2_key_3 Channel 2 Key[31:0].

CRYPTO_CH3_KEY_0

Address: **Operational Base** + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	ch3_key_0 Channel 3 Key[127:96].

CRYPTO_CH3_KEY_1

Address: **Operational Base** + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	ch3_key_1 Channel 3 Key[95:64].

CRYPTO_CH3_KEY_2

Address: **Operational Base** + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	ch3_key_2 Channel 3 Key[63:32].

CRYPTO_CH3_KEY_3

Address: **Operational Base** + offset (0x01BC)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	ch3_key_3 Channel 3 Key[31:0].

CRYPTO_CH4_KEY_0

Address: **Operational Base** + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	ch4_key_0 Channel 4 Key[127:96].

CRYPTO_CH4_KEY_1

Address: **Operational Base** + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	ch4_key_1 Channel 4 Key[95:64].

CRYPTO_CH4_KEY_2

Address: **Operational Base** + offset (0x01C8)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	ch4_key_2 Channel 4 Key[63:32].

CRYPTO_CH4_KEY_3

Address: **Operational Base** + offset (0x01CC)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	ch4_key_3 Channel 4 Key[31:0].

CRYPTO_CH5_KEY_0

Address: **Operational Base** + offset (0x01D0)

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Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	ch5_key_0 Channel 5 Key[127:96].

CRYPTO_CH5_KEY_1

Address: **Operational Base** + offset (0x01D4)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	ch5_key_1 Channel 5 Key[95:64].

CRYPTO_CH5_KEY_2

Address: **Operational Base** + offset (0x01D8)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	ch5_key_2 Channel 5 Key[63:32].

CRYPTO_CH5_KEY_3

Address: **Operational Base** + offset (0x01DC)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	ch5_key_3 Channel 5 Key[31:0].

CRYPTO_CH6_KEY_0

Address: **Operational Base** + offset (0x01E0)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	ch6_key_0 Channel 6 Key[127:96].

CRYPTO_CH6_KEY_1

Address: **Operational Base** + offset (0x01E4)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	ch6_key_1 Channel 6 Key[95:64].

CRYPTO_CH6_KEY_2

Address: **Operational Base** + offset (0x01E8)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	ch6_key_2 Channel 6 Key[63:32].

CRYPTO_CH6_KEY_3

Address: **Operational Base** + offset (0x01EC)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	ch6_key_3 Channel 6 Key[31:0].

CRYPTO_CH7_KEY_0

Address: **Operational Base** + offset (0x01F0)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	ch7_key_0 Channel 7 Key[127:96].

CRYPTO_CH7_KEY_1

Address: **Operational Base** + offset (0x01F4)

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Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	ch7_key_1 Channel 7 Key[95:64].

CRYPTO_CH7_KEY_2

Address: **Operational Base** + offset (0x01F8)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	ch7_key_2 Channel 7 Key[63:32].

CRYPTO_CH7_KEY_3

Address: **Operational Base** + offset (0x01FC)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	ch7_key_3 Channel 7 Key[31:0].

CRYPTO_CH0_PC_LEN_0

Address: **Operational Base** + offset (0x0280)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ch0_pc_len_0 Channel 0 Plain/Cipher Text Length[31:0].

CRYPTO_CH0_PC_LEN_1

Address: **Operational Base** + offset (0x0284)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	ch0_pc_len_1 Channel 0 Plain/Cipher Text Length[60:32].

CRYPTO_CH0_AAD_LEN_0

Address: **Operational Base** + offset (0x02C0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ch0_aad_len_0 Channel 0 additional data Length[31:0].

CRYPTO_CH0_AAD_LEN_1

Address: **Operational Base** + offset (0x02C4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	ch0_aad_len_1 Channel 0 additional data Length[60:32].

CRYPTO_CH0_IV_LEN_0

Address: **Operational Base** + offset (0x0300)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x00	ch0_iv_len Channel 0 initial vector length. Up to 16 byte IV for GCM.

CRYPTO_CH0_TAG_0

Address: **Operational Base** + offset (0x0320)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ch0_tag_0 Channel 0 tag[127:96].

CRYPTO_CH0_TAG_1

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Address: **Operational Base** + offset (0x0324)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ch0_tag_1 Channel 0 tag[95:64].

CRYPTO_CH0_TAG_2

Address: **Operational Base** + offset (0x0328)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ch0_tag_2 Channel 0 tag[63:32].

CRYPTO_CH0_TAG_3

Address: **Operational Base** + offset (0x032C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ch0_tag_3 Channel 0 tag[31:0].

CRYPTO_HASH_DOUT_0

Address: **Operational Base** + offset (0x03A0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_0 0'th output word for all hash function, in big endian.

CRYPTO_HASH_DOUT_1

Address: **Operational Base** + offset (0x03A4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_1 1'th output word for all hash function, in big endian.

CRYPTO_HASH_DOUT_2

Address: **Operational Base** + offset (0x03A8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_2 2'th output word for all hash function, in big endian.

CRYPTO_HASH_DOUT_3

Address: **Operational Base** + offset (0x03AC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_3 3'th output word for all hash function, in big endian. This is MD5 last output word. HASH_DOUT_4 ~ HASH_DOUT_15 is invalid data for MD5.

CRYPTO_HASH_DOUT_4

Address: **Operational Base** + offset (0x03B0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_4 4'th output word for all hash function, in big endian. This is SHA-1 last output word. HASH_DOUT_5 ~ HASH_DOUT_15 is invalid data for SHA-1.

CRYPTO_HASH_DOUT_5

Address: **Operational Base** + offset (0x03B4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_5 5'th output word for all hash function, in big endian.

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CRYPTO_HASH_DOUT_6

Address: **Operational Base** + offset (0x03B8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_6 6'th output word for all hash function, in big endian.

CRYPTO_HASH_DOUT_7

Address: **Operational Base** + offset (0x03BC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_7 7'th output word for all hash function, in big endian. This is SHA-256/224 last output word. HASH_DOUT_8 ~ HASH_DOUT_15 is invalid data for SHA-256/224.

CRYPTO_TAG_VALID

Address: **Operational Base** + offset (0x03E0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	W1C	0x0	ch7_tag_valid When channel 7 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit 1'b0: Channel 7 tag is invalid 1'b1: Channel 7 tag is valid
6	W1C	0x0	ch6_tag_valid When channel 6 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit 1'b0: Channel 6 tag is invalid 1'b1: Channel 6 tag is valid
5	W1C	0x0	ch5_tag_valid When channel 5 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit 1'b0: Channel 5 tag is invalid 1'b1: Channel 5 tag is valid
4	W1C	0x0	ch4_tag_valid When channel 4 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit 1'b0: Channel 4 tag is invalid 1'b1: Channel 4 tag is valid
3	W1C	0x0	ch3_tag_valid When channel 3 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit 1'b0: Channel 3 tag is invalid 1'b1: Channel 3 tag is valid
2	W1C	0x0	ch2_tag_valid When channel 2 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit 1'b0: Channel 2 tag is invalid 1'b1: Channel 2 tag is valid

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Bit	Attr	Reset Value	Description
1	W1C	0x0	ch1_tag_valid When channel 1 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit 1'b0: Channel 1 tag is invalid 1'b1: Channel 1 tag is valid
0	W1C	0x0	ch0_tag_valid When channel 0 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit 1'b0: Channel 0 tag is invalid 1'b1: Channel 0 tag is valid

CRYPTO_HASH_VALID

Address: **Operational Base** + offset (0x03E4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1C	0x0	hash_valid When HASH calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit 1'b0: HASH_DOUT is invalid 1'b1: HASH_DOUT is valid

CRYPTO_MID_VALID

Address: **Operational Base** + offset (0x03E8)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	W1C	0x0	hash_mid_valid When hash calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit. 1'b0: CRYPTO_HASH_MID_DATA is invalid 1'b1: CRYPTO_HASH_MID_DATA is valid
0	W1C	0x0	bc_mid_valid When block cipher calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit. 1'b0: CRYPTO_BC_MID_IV is invalid 1'b1: CRYPTO_BC_MID_IV is valid

CRYPTO_RAM_CTL

Address: **Operational Base** + offset (0x0480)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	WO	0x0	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	ram_pka_rdy Indicate whether ram is controlled by PKA engine 1'b0: Ram is controlled by CPU 1'b1: Ram is controlled by CRYPTO PKA engine

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CRYPTO_RAM_ST

Address: **Operational Base** + offset (0x0484)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x1	clk_ram_rdy Indicate whether clk_ram is stable, and ready for use. 1'b0: Not stable 1'b1: Stable

CRYPTO_DEBUG_CTL

Address: **Operational Base** + offset (0x04A0)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	WO	0x0	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	pka_debug_mode 1'b0: PKA is in normal mode 1'b1: PKA is in debug mode

CRYPTO_DEBUG_ST

Address: **Operational Base** + offset (0x04A4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x1	pka_debug_clk_en For debug use only 1'b0: Disable 1'b1: Enable

CRYPTO_DEBUG_MONITOR

Address: **Operational Base** + offset (0x04A8)

Bit	Attr	Reset Value	Description
31:0	RO	0x0000feef	pka_monitor_bus For debug use only.

CRYPTO_CRYPTO_KL_KEY_STATUS

Address: **Operational Base** + offset (0x0600)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	kl_key_flag Key ladder key valid flag of keytable0~15 1'b0: Invalid 1'b1: Valid

CRYPTO_CRYPTO_KEY_SEL

Address: **Operational Base** + offset (0x0610)

Bit	Attr	Reset Value	Description
31	RW	0x0	klad_kl_high_sel 1'b0: big endian 1'b1: little endian
30:0	RW	0x00000000	key_select Select internal temp key or configed key from ahb_slv. 31'h5a5a5a5a: Internal temp key Others: Configed key from ahb_slv

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CRYPTO_CRYPTO_LOCKSTEP

Address: **Operational Base** + offset (0x0618)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	lock_step_flag Lock step status: 1'b0: No mistake 1'b1: Mistake happened

CRYPTO_CRYPTO_LOCKSTEP_EN

Address: **Operational Base** + offset (0x061C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	lockstep_en 1'b0: Disable 1'b1: Enable Note: Whether the lockstep_en takes effect depends on whether this IP has the function of lockstep described in register XXX_VERSION(XXX can be AES, DES, SM4, HASH, HMAC, ect.)

CRYPTO_MID_VALID_SWITCH

Address: **Operational Base** + offset (0x0630)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	mid valid switch How the application obtains MID_VALID_DATA 1'b0: The src_done_init interrupt is used to obtain MID DATA. The mid_VALID flag bit is cleared when the interrupt is cleared 1'b1: Obtains MID DATA by polling the MID_VALID register

CRYPTO_AES_VERSION

Address: **Operational Base** + offset (0x0680)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	RW	0x0	multichannel_flag Whether the AES supports multichannel 1'b0: No support 1'b1: Support
21	RW	0x0	secure_flag Whether the AES supports anti-side channel attack 1'b0: No support 1'b1: Support
20	RW	0x0	lockstep_flag Whether the AES supports lockstep 1'b0: No support 1'b1: Support
19	RO	0x0	reserved
18	RO	0x1	aes256_flag Whether the AES supports AES256 1'b0: No support 1'b1: Support
17	RO	0x1	aes192_flag Whether the AES supports AES192 1'b0: No support 1'b1: Support

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Bit	Attr	Reset Value	Description
16	RO	0x1	aes128_flag Whether the AES supports AES128 1'b0: No support 1'b1: Support
15:13	RO	0x0	reserved
12	RO	0x1	bypass Whether IP supports data bypass 1'b0: No support 1'b1: Support
11	RO	0x0	reserved
10	RO	0x1	cbc-mac_flag Whether the AES supports CBC-MAC 1'b0: No support 1'b1: Support
9	RO	0x1	cmac_flag Whether the AES supports CMAC 1'b0: No support 1'b1: Support
8	RO	0x1	gcm_flag Whether the AES supports GCM 1'b0: No support 1'b1: Support
7	RO	0x1	ccm_flag Whether the AES supports CCM 1'b0: No support 1'b1: Support
6	RO	0x1	xts_flag Whether the AES supports XTS 1'b0: No support 1'b1: Support
5	RO	0x1	ofb_flag Whether the AES supports OFB 1'b0: No support 1'b1: Support
4	RO	0x1	cfb_flag Whether the AES supports CFB 1'b0: No support 1'b1: Support
3	RO	0x1	ctr_flag Whether the AES supports CTR 1'b0: No support 1'b1: Support
2	RO	0x1	cts_flag Whether the AES supports CTS 1'b0: No support 1'b1: Support
1	RO	0x1	cbc_flag Whether the AES supports CBC 1'b0: No support 1'b1: Support
0	RO	0x1	ecb_flag Whether the AES supports ECB 1'b0: No support 1'b1: Support

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CRYPTO_DES_VERSION

Address: **Operational Base** + offset (0x0684)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	RW	0x0	multichannel_flag Whether the DES supports multichannel 1'b0: No support 1'b1: Support
21	RW	0x0	secure_flag Whether the DES supports anti-side channel attack 1'b0: No support 1'b1: Support
20	RW	0x0	lockstep_flag Whether the DES supports lockstep 1'b0: No support 1'b1: Support
19	RO	0x0	reserved
18	RW	0x1	ede_flag Whether the DES supports EDE mode 1'b0: No support 1'b1: Support
17	RO	0x1	eee_flag Whether the DES supports EEE mode 1'b0: No support 1'b1: Support
16	RO	0x1	tdes_flag Whether the DES supports TDES 1'b0: No support 1'b1: Support
15:6	RO	0x000	reserved
5	RO	0x1	ofb_flag Whether the DES supports OFB 1'b0: No support 1'b1: Support
4	RO	0x1	cfb_flag Whether the DES supports CFB 1'b0: No support 1'b1: Support
3:2	RO	0x0	reserved
1	RO	0x1	cbc_flag Whether the DES supports CBC 1'b0: No support 1'b1: Support
0	RO	0x1	ecb_flag Whether the DES supports ECB 1'b0: No support 1'b1: Support

CRYPTO_SM4_VERSION

Address: **Operational Base** + offset (0x0688)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	RW	0x0	multichannel_flag Whether the SM4 supports multichannel 1'b0: No support 1'b1: Support

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Bit	Attr	Reset Value	Description
21	RW	0x0	secure_flag Whether the SM4 supports anti-side channel attack 1'b0: No support 1'b1: Support
20	RW	0x0	lockstep_flag Whether the SM4 supports lockstep 1'b0: No support 1'b1: Support
19:11	RO	0x000	reserved
10	RO	0x0	cbc-mac_flag Whether the SM4 supports CBC-MAC 1'b0: No support 1'b1: Support
9	RO	0x0	cmac_flag Whether the SM4 supports CMAC 1'b0: No support 1'b1: Support
8	RO	0x0	gcm_flag Whether the SM4 supports GCM 1'b0: No support 1'b1: Support
7	RO	0x0	ccm_flag Whether the SM4 supports CCM 1'b0: No support 1'b1: Support
6	RO	0x0	xts_flag Whether the SM4 supports XTS 1'b0: No support 1'b1: Support
5	RO	0x0	ofb_flag Whether the SM4 supports OFB 1'b0: No support 1'b1: Support
4	RO	0x0	cfb_flag Whether the SM4 supports CFB 1'b0: No support 1'b1: Support
3	RO	0x0	ctr_flag Whether the SM4 supports CTR 1'b0: No support 1'b1: Support
2	RO	0x0	cts_flag Whether the SM4 supports CTS 1'b0: No support 1'b1: Support
1	RO	0x0	cbc_flag Whether the SM4 supports CBC 1'b0: No support 1'b1: Support
0	RO	0x0	ecb_flag Whether the SM4 supports ECB 1'b0: No support 1'b1: Support

CRYPTO_HASH_VERSION

Address: **Operational Base** + offset (0x068C)

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Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	lockstep_flag Whether the HASH supports lockstep 1'b0: No support 1'b1: Support
19:9	RO	0x000	reserved
8	RO	0x0	sm3_flag Whether the HASH supports SM3 1'b0: No support 1'b1: Support
7	RO	0x1	md5_flag Whether the HASH supports MD5 1'b0: No support 1'b1: Support
6	RO	0x0	sha512-256_flag Whether the HASH supports SHA-512/256 1'b0: No support 1'b1: Support
5	RO	0x0	sha512-224_flag Whether the HASH supports SHA-512/224 1'b0: No support 1'b1: Support
4	RO	0x0	sha512_flag Whether the HASH supports SHA-512 1'b0: No support 1'b1: Support
3	RO	0x0	sha384_flag Whether the HASH supports SHA-384 1'b0: No support 1'b1: Support
2	RO	0x1	sha256_flag Whether the HASH supports SHA-256 1'b0: No support 1'b1: Support
1	RO	0x1	sha224_flag Whether the HASH supports SHA-224 1'b0: No support 1'b1: Support
0	RO	0x1	sha1_flag Whether the HASH supports SHA-1 1'b0: No support 1'b1: Support

CRYPTO_HMAC_VERSION

Address: **Operational Base** + offset (0x0690)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	RW	0x0	multichannel Whether the HMAC supports multichannel 1'b0: No support 1'b1: Support
21	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
20	RW	0x0	lockstep_flag Whether the HMAC supports lockstep 1'b0: No support 1'b1: Support
19:5	RO	0x0000	reserved
4	RO	0x0	sm3_flag Whether the HMAC supports SM3 1'b0: No support 1'b1: Support
3	RO	0x1	md5_flag Whether the HMAC supports MD5 1'b0: No support 1'b1: Support
2	RO	0x0	sha512_flag Whether the HMAC supports SHA-512 1'b0: No support 1'b1: Support
1	RO	0x1	sha256_flag Whether the HMAC supports SHA-256 1'b0: No support 1'b1: Support
0	RO	0x1	sha1_flag Whether the HMAC supports SHA-1 1'b0: No support 1'b1: Support

CRYPTO_PKA_VERSION

Address: **Operational Base** + offset (0x0698)

Bit	Attr	Reset Value	Description
31:0	RW	0x01000000	pka_version_code PKA version_code is 0x0100_0000.

CRYPTO_EXTRA_FEATURE

Address: **Operational Base** + offset (0x069C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RO	0x2	axi_expand_bit AXI Address extension width. The real axi address width is (32+ axi_expand_bit-1) when (axi_expand_bit >0), or 32 when (axi_expand_bit =0)

CRYPTO_CRYPTO_VERSION

Address: **Operational Base** + offset (0x06F0)

Bit	Attr	Reset Value	Description
31:0	RW	0x04000001	crypto_version_code NSCRYPTO version_code is 0x0400_0001. SCRYPTO version_code is 0x0400_0002.

CRYPTO_HASH_MID_DATA_0

Address: **Operational Base** + offset (0x0700)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hash_mid_data_0 HASH mid data 0

CRYPTO_HASH_MID_DATA_1

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Address: **Operational Base** + offset (0x0704)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hash_mid_data_1 HASH mid data 1

CRYPTO_HASH_MID_DATA_2

Address: **Operational Base** + offset (0x0708)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hash_mid_data_2 HASH mid data 2

CRYPTO_HASH_MID_DATA_3

Address: **Operational Base** + offset (0x070C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hash_mid_data_3 HASH mid data 3

CRYPTO_HASH_MID_DATA_4

Address: **Operational Base** + offset (0x0710)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hash_mid_data_4 HASH mid data 4

CRYPTO_HASH_MID_DATA_5

Address: **Operational Base** + offset (0x0714)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hash_mid_data_5 HASH mid data 5

CRYPTO_HASH_MID_DATA_6

Address: **Operational Base** + offset (0x0718)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hash_mid_data_6 HASH mid data 6

CRYPTO_HASH_MID_DATA_7

Address: **Operational Base** + offset (0x071C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hash_mid_data_7 HASH mid data 7

CRYPTO_HASH_MID_DATA_8

Address: **Operational Base** + offset (0x0720)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hash_mid_data_8 HASH mid data 8

CRYPTO_HASH_MID_DATA_9

Address: **Operational Base** + offset (0x0724)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hash_mid_data_9 HASH mid data 9

CRYPTO_HASH_MID_DATA_10

Address: **Operational Base** + offset (0x0728)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hash_mid_data_10 HASH mid data 10

CRYPTO_HASH_MID_DATA_11
Address: **Operational Base** + offset (0x072C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hash_mid_data_11 HASH mid data 11

CRYPTO_HASH_MID_DATA_12
Address: **Operational Base** + offset (0x0730)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hash_mid_data_12 HASH mid data 12

CRYPTO_HASH_MID_DATA_13
Address: **Operational Base** + offset (0x0734)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hash_mid_data_13 HASH mid data 13

CRYPTO_HASH_MID_DATA_14
Address: **Operational Base** + offset (0x0738)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hash_mid_data_14 HASH mid data 14

CRYPTO_HASH_MID_DATA_15
Address: **Operational Base** + offset (0x073C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hash_mid_data_15 HASH mid data 15

CRYPTO_HASH_MID_DATA_16
Address: **Operational Base** + offset (0x0740)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hash_mid_data_16 HASH mid data 16

CRYPTO_HASH_MID_DATA_17
Address: **Operational Base** + offset (0x0744)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hash_mid_data_17 HASH mid data 17

CRYPTO_HASH_MID_DATA_18
Address: **Operational Base** + offset (0x0748)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hash_mid_data_18 HASH mid data 18

CRYPTO_HASH_MID_DATA_19
Address: **Operational Base** + offset (0x074C)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hash_mid_data_19 HASH mid data 19

CRYPTO_HASH_MID_DATA_20

Address: **Operational Base** + offset (0x0750)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hash_mid_data_20 HASH mid data 20

CRYPTO_HASH_MID_DATA_21

Address: **Operational Base** + offset (0x0754)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hash_mid_data_21 HASH mid data 21

CRYPTO_HASH_MID_DATA_22

Address: **Operational Base** + offset (0x0758)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hash_mid_data_22 HASH mid data 22

CRYPTO_HASH_MID_DATA_23

Address: **Operational Base** + offset (0x075C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hash_mid_data_23 HASH mid data 23

CRYPTO_HASH_MID_DATA_24

Address: **Operational Base** + offset (0x0760)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hash_mid_data_24 HASH mid data 24

CRYPTO_HASH_MID_DATA_25

Address: **Operational Base** + offset (0x0764)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hash_mid_data_25 HASH mid data 25

CRYPTO_PKA_MEM_MAP0

Address: **Operational Base** + offset (0x0800)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map0 Memory map 0 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP1

Address: **Operational Base** + offset (0x0804)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map1 Memory map 1 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

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CRYPTO_PKA_MEM_MAP2

Address: **Operational Base** + offset (0x0808)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map2 Memory map 2 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP3

Address: **Operational Base** + offset (0x080C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map3 Memory map 3 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP4

Address: **Operational Base** + offset (0x0810)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map4 Memory map 4 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP5

Address: **Operational Base** + offset (0x0814)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map5 Memory map 5 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP6

Address: **Operational Base** + offset (0x0818)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map6 Memory map 6 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP7

Address: **Operational Base** + offset (0x081C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map7 Memory map 7 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP8

Address: **Operational Base** + offset (0x0820)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map8 Memory map 8 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

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CRYPTO_PKA_MEM_MAP9

Address: **Operational Base** + offset (0x0824)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map9 Memory map 9 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP10

Address: **Operational Base** + offset (0x0828)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map10 Memory map 10 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP11

Address: **Operational Base** + offset (0x082C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map11 Memory map 11 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP12

Address: **Operational Base** + offset (0x0830)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map12 Memory map 12 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP13

Address: **Operational Base** + offset (0x0834)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map13 Memory map 13 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP14

Address: **Operational Base** + offset (0x0838)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map14 Memory map 14 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP15

Address: **Operational Base** + offset (0x083C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map15 Memory map 15 [11:2], bit[1:0] is stuck to 0.

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Bit	Attr	Reset Value	Description
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP16

Address: **Operational Base** + offset (0x0840)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map16 Memory map 16 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP17

Address: **Operational Base** + offset (0x0844)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map17 Memory map 17 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP18

Address: **Operational Base** + offset (0x0848)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map18 Memory map 18 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP19

Address: **Operational Base** + offset (0x084C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map19 Memory map 19 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP20

Address: **Operational Base** + offset (0x0850)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map20 Memory map 20 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP21

Address: **Operational Base** + offset (0x0854)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map21 Memory map 21 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP22

Address: **Operational Base** + offset (0x0858)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
11:2	RW	0x000	memory_map22 Memory map 22 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP23

Address: **Operational Base** + offset (0x085C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map23 Memory map 23 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP24

Address: **Operational Base** + offset (0x0860)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map24 Memory map 24 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP25

Address: **Operational Base** + offset (0x0864)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map25 Memory map 25 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP26

Address: **Operational Base** + offset (0x0868)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map26 Memory map 26 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP27

Address: **Operational Base** + offset (0x086C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map27 Memory map 27 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP28

Address: **Operational Base** + offset (0x0870)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map28 Memory map 28 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP29

Address: **Operational Base** + offset (0x0874)

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Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map29 Memory map 29 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP30

Address: **Operational Base** + offset (0x0878)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map30 Memory map 30 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP31

Address: **Operational Base** + offset (0x087C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:2	RW	0x000	memory_map31 Memory map 30 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_OPCODE

Address: **Operational Base** + offset (0x0880)

Bit	Attr	Reset Value	Description
31:27	WO	0x00	opcode Defines the PKA operation. 5'h00: Terminate 5'h04: Add, Inc 5'h05: Sub, Dec, Neg 5'h06: ModAdd, ModInc 5'h07: ModSub, ModDec, ModNeg 5'h08: AND, TST0, CLR0 5'h09: OR, COPY, SET0 5'h0A: XOR, FLIP0, INVERT, COMPARE 5'h0B: SHR0 5'h0D: SHR1 5'h0E: SHL0 5'h0F: SHL1 5'h10: MulLow 5'h11: ModMul 5'h12: ModMulN 5'h13: ModExp 5'h14: Division 5'h15: Div 5'h16: ModDiv Others: Reserved
26:24	WO	0x0	len The virtual length address 0-7 Virtual address 0 point to PKA_L0 Virtual address 1 point to PKA_L1 ... Virtual address 7 point to PKA_L7

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Bit	Attr	Reset Value	Description
23:18	WO	0x00	reg_a Operand A virtual address 0-15 Virtual address 0 point to PKA_MEM_MAP0 Virtual address 1 point to PKA_MEM_MAP1 ... Virtual address 15 point to PKA_MEM_MAP15
17:12	WO	0x00	reg_b Operand B virtual address 0-15 Virtual address 0 point to PKA_MEM_MAP0 Virtual address 1 point to PKA_MEM_MAP1 ... Virtual address 15 point to PKA_MEM_MAP15
11:6	WO	0x00	reg_r Result register virtual address 0-15 Virtual address 0 point to PKA_MEM_MAP0 Virtual address 1 point to PKA_MEM_MAP1 ... Virtual address 15 point to PKA_MEM_MAP15
5:0	WO	0x00	tag Tag

CRYPTO_N_NP_T0_T1_ADDR

Address: **Operational Base** + offset (0x0884)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:15	RW	0x1f	reg_t1 Virtual address of temporary register number 1 Virtual address 0 point to PKA_MEM_MAP0 Virtual address 1 point to PKA_MEM_MAP1 ... Virtual address 15 point to PKA_MEM_MAP15
14:10	RW	0x1e	reg_t0 Virtual address of temporary register number 0 Virtual address 0 point to PKA_MEM_MAP0 Virtual address 1 point to PKA_MEM_MAP1 ... Virtual address 15 point to PKA_MEM_MAP15
9:5	RW	0x01	reg_np Virtual address of register np Virtual address 0 point to PKA_MEM_MAP0 Virtual address 1 point to PKA_MEM_MAP1 ... Virtual address 15 point to PKA_MEM_MAP15
4:0	RW	0x00	reg_n Virtual address of register n Virtual address 0 point to PKA_MEM_MAP0 Virtual address 1 point to PKA_MEM_MAP1 ... Virtual address 15 point to PKA_MEM_MAP15

CRYPTO_PKA_STATUS

Address: **Operational Base** + offset (0x0888)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
19:14	RO	0x00	tag Tag of the Last Operation.
13:9	RO	0x00	opcode The last OPCODE.
8	RO	0x0	pka_cpu_busy PKA is busy memory control is by PKA.
7	RO	0x0	modinv_of_zero Modular inverse of zero flag.
6	RO	0x0	alu_sign_out Sign of the last operation(MSB).
5	RO	0x0	alu_carry Carry of the last ALU operation.
4	RO	0x0	div_by_zero Division by 0.
3	RO	0x0	alu_mod_ovflw Modular overflow flag.
2	RO	0x0	alu_out_zero ALU out is 0.
1	RO	0x0	pka_busy PKA is busy.
0	RO	0x1	pipe_is_busy PKA ready signal 1'b0: Pipe full 1'b1: PKA ready for new command

CRYPTO_PKA_SW_RESET

Address: **Operational Base** + offset (0x088C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	WO	0x0	pka_sw_reset PKA software reset the reset mechanism will take about four PKA clocks until the reset line is de-asserted.

CRYPTO_PKA_L0

Address: **Operational Base** + offset (0x0890)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	pka_l0 PKA length 0, in bit unit.

CRYPTO_PKA_L1

Address: **Operational Base** + offset (0x0894)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	pka_l1 PKA length 1, in bit unit.

CRYPTO_PKA_L2

Address: **Operational Base** + offset (0x0898)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	pka_l2 PKA length 2, in bit unit.

CRYPTO_PKA_L3

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Address: **Operational Base** + offset (0x089C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	pka_l3 PKA length 3, in bit unit.

CRYPTO_PKA_L4

Address: **Operational Base** + offset (0x08A0)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	pka_l4 PKA length 4, in bit unit.

CRYPTO_PKA_L5

Address: **Operational Base** + offset (0x08A4)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	pka_l5 PKA length 5, in bit unit.

CRYPTO_PKA_L6

Address: **Operational Base** + offset (0x08A8)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	pka_l6 PKA length 6, in bit unit.

CRYPTO_PKA_L7

Address: **Operational Base** + offset (0x08AC)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	pka_l7 PKA length 7, in bit unit.

CRYPTO_PKA_PIPE_RDY

Address: **Operational Base** + offset (0x08B0)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x1	pka_pipe_rdy PKA pipe is ready for new opcode.

CRYPTO_PKA_DONE

Address: **Operational Base** + offset (0x08B4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x1	pka_done PKA operation is completed and pipe is empty.

CRYPTO_PKA_MON_SELECT

Address: **Operational Base** + offset (0x08B8)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	pka_mon_select PKA monitor select which PKA fsm monitor is being output.

CRYPTO_PKA_DEBUG_REG_EN

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Address: **Operational Base** + offset (0x08BC)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	pka_debug_reg_en Enable all the debug mechanism when set.

CRYPTO_DEBUG_CNT_ADDR

Address: **Operational Base** + offset (0x08C0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	R/WSC	0x00000	debug_cnt_addr The clock counter initial values. clock is disabled when counter expires. Triggered when pka_debug_en is set.

CRYPTO_DEBUG_EXT_ADDR

Address: **Operational Base** + offset (0x08C4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	WO	0x0	debug_ext_addr Disable the debug Mechanism.

CRYPTO_PKA_DEBUG_HALT

Address: **Operational Base** + offset (0x08C8)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	pka_debug_halt In debug mode: PKA is in halt state.

CRYPTO_PKA_MON_READ

Address: **Operational Base** + offset (0x08D0)

Bit	Attr	Reset Value	Description
31:0	RO	0x0000feef	pka_mon_read This is the PKA monitor bus register output.

CRYPTO_PKA_INT_ENA

Address: **Operational Base** + offset (0x08D4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	pka_int_ena 1'b0: Disable pka interrupt 1'b1: Enable pka interrupt

CRYPTO_PKA_INT_ST

Address: **Operational Base** + offset (0x08D8)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1C	0x0	pka_int_st Indicate that PKA operation completes. After the bit is read, the application should write 1 to clear this bit for next time use.

CRYPTO_SRAM_ADDR

Address: **Operational Base** + offset (0x1000)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sram_addr Sram address starts from 0x1000 to 0x1fff. When RAM_CTL.ram_pka_rdy == 0, application could access sram. Otherwise, application can't.

16.5 Application Notes

16.5.1 Clock and Reset

There are 4 clock domains in CRYPTO. The clock and reset signals are described in the following table.

Table 16-1 CRYPTO Clock & Reset Description

Signal	Attr	Description
hclk	clock	AHB clock
aclk	clock	AXI master clock
pclk	clock	APB master clock
clk_core	clock	Cipher work clock
clk_pka	clock	PKA work clock
hresetn	reset	Asynchronously assert, synchronously de-assert to hclk, low active
aresetn	reset	Asynchronously assert, synchronously de-assert to aclk, low active
presetn	reset	Asynchronously assert, synchronously de-assert to pclk, low active
resetn_core	reset	Asynchronously assert, synchronously de-assert to clk_core, low active
resetn_pka	reset	Asynchronously assert, synchronously de-assert to clk_pka, low active

Each function need different clocks. The applications could gate the un-used clock to save power. Please see the following table for detail information.

Table 16-2 CRYPTO Auto Clock Gate Description

Operation	HCLK	ACLK	CLK_CORE	CLK_PKA
AES	ON	ON	ON	OFF
DES/TDES	ON	ON	ON	OFF
HASH/HMAC	ON	ON	ON	OFF
PKA	ON	OFF	OFF	ON

Even when clk_core is on, CRYPTO is doing some cipher job. And CRYPTO could still be able to automatically gate most parts of un-used blocks to save more power, if CRYPTO_CLK_CTL. auto_clkgate_en is set to '1'. The default value for this bit is also '1'. Application could do a soft reset to a certain clock domain. Please refer to "Chapter CRU" for more details.

16.5.2 Performance

Cipher performance is shown in the following table.

Table 16-3 CRYPTO Performance Description

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Algorithm	block size (Byte)	clk_core frequency (Mhz)	cycle	serial max throughput (MBps)	parallel max throughput (MBps)
DES	8	200	18	89	356
TDES	8	200	55	29	116
AES-128	16	200	12	267	1067
AES-192	16	200	14	229	914
AES-256	16	200	16	158	800
SHA-1	64	200	81	197	NA
MD5	64	200	65	197	NA
SHA-256/224	64	200	65	158	NA
RSA-2048	NA	300	130K	NA	NA

There are 2 column throughput rates in the table, 1 is serial mode, the other is parallel mode. In parallel mode, there are 4 engines working at the same time. So the speed is 4 times than serial mode. Parallel mode includes ECB/CTR/XTS both encryption and decryption mode, CFB/CBC/CTS only decryption mode. Other modes are serial. HASH doesn't have parallel mode.
For RSA-2048, the time-consuming MODEXP operation needs about 130K clock cycles.

16.5.3 DMA

DMA supports Link List Item (LLI) DMA transaction.

- Each item contains 8 word when LLI Item DMA_CTL.bit[2] =0 , or 10 word when LLI Item DMA_CTL.bit[2] =1, and start address should be 8 bytes align
- We suggest that DATA start address is 8 bytes align
- Total DATA length is byte align
- Support segmenting HASH/HMAC DATA into multi sections. There is no requirement for the length of each data segment.

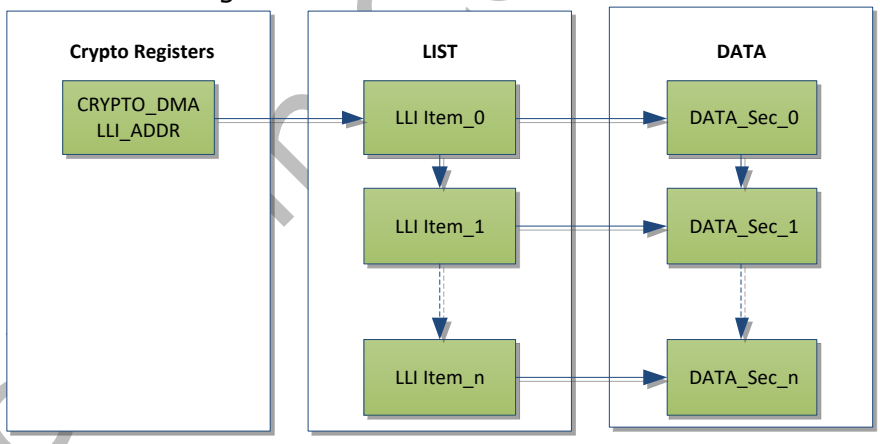


Fig.16-2 LLI DMA Usage

As shown in the figure above, Register CRYPTO_DMA_LLI_ADDR points to 1'st LLI item in external memory. Each LLI item contains DATA address, length, control information and next LLI item pointer, except the last LLI item. The last item doesn't have the next LLI Item pointer. After the last LLI item is finished, DMA will go to idle state.
LLI item definition is shown in the following table.

Table 16-4 LLI Item Description

offset	Def	Description
0x00	SRC_ADDRESS[31:0]	The lower 32 bits of source data start address
0x04	SRC_LENGTH[31:0]	Source data length, in byte unit
0x08	DST_ADDRESS[31:0]	The lower 32 bits of destination data start address
0x0c	DST_LENGTH[31:0]	Destination data length, in byte unit

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offset	Def	Description
0x10	USER_DEFINE[31:0]	Used in cipher block
0x14	IV_OFFSET	IV offset
0x18	DMA_CTRL[31:0]	Used in DMA block
0x1c	NEXT_ADDRESS[31:0]	Next LLI item address. When DMA_CTRL.LAST = "1", NEXT_ADDRESS is invalid
0x20	SRC_ADDRESS[63:32]	The higher 32 bits of source data start address
0x24	DST_ADDRESS[63:32]	The higher 32 bits of destination data start address

DMA_CTRL: the definition is shown in the following table.

Table 16-5 LLI Item DMA_CTL Description

Bit	Def	Definition
[31:24]	ITEM_ID[7:0]	Used to identify LLI items
[23:16]	Reserved	Reserved
[15:11]	Reserved	Reserved
10	Source_item_done enable	When source data fetch is completed, CRYPTO_DMA_INT_ST.source_item_done will assert if this bit is set
9	Dst_item_done enable	When destination data fetch is completed, CRYPTO_DMA_INT_ST.dst_item_done will assert if this bit is set
8	List_done enable	When all LLI items transfer is completed, CRYPTO_DMA_INT_ST.list_done will assert if this bit is set
[7:3]	Reserved	Reserved
2	Flag of extend addr width	Indicates whether the bit width of the SRC_ADDRESS and DST_ADDRESS is greater than 32bit. 1: extend 0：no extend
1	PAUSE	Indicate DMA will hold on after executes current item. DMA won't go on unless CRYPTO_DMA_CTL.restart is configured
0	LAST	Indicate current item is the last one. After executes current item, DMA will return to IDLE state

Table 16-6 LLI Item user_define Description

Bit	Signal	Description
31:7	Reserved	Reserved
6:4	Chnl_num	Channel number, from 0 to 7
3	String_attr	Indicate current item's attribution 1: ADA; 0: PC(plaintext or ciphertext)
2	String_last	Indicate current item is the string last item
1	String_start	Indicate current item is the string first item
0	Cipher_start	Indicate current item is the cipher first item

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16.5.4 Use of KEY TABLE

KEY Table is used to receive and temporarily store the KEY sent by KEYLAD through APB, and provide the KEY to CIPHER operation. If CRYPTO uses the KEY in the KEY Table as the KEY of the CIPHER operation, it also needs to configure the SCRYPTO_KEY_SEL register to be the value of 0x5a5a5a5a.

16.5.5 Bypass Mode

When working at bypass mode, CRYPTO will transfer data from source address to destination address without calculation. To working at bypass mode, application must set CRYPTO_BC_CTL.enable to 0x1 and CRYPTO_BC_CTL.mode to 0xf. And note that the transfer length of data must not be 0.

16.5.6 Multi-Channel Map

There are 1-channel configurations for AES or DES/TDES operation. For different key-size, the map is different. Please find the register map in the following table.

Table 16-7 Register Map of Different Key Size

Cipher sel	Chnl num	Key	Iv(tag/…)
AES-128/ DES	0	CH0_KEY0-3/ CH0_KEY0-1	CH0_IV0-3/ CH0_IV0-1
AES-192/ TDES	0	CH0_KEY0-3, CH1_KEY0-1	CH0_IV0-3/ CH0_IV0-1
AES-256	0	CH0_KEY0-3, CH1_KEY0-3	CH0_IV0-3/ CH0_IV0-1

In AES-XTS mode, there are 2 keys, and only AES-128 and AES-256 mode are. Please refer to the following table for detail information.

Table 16-8 Register Map in AES-XTS Mode

Cipher sel	Chnl num	Key1	Key2	Tweak
AES-128	0	CH0_KEY0-3	CH4_KEY0-3	CH0_IV0-3
AES-256	0	CH0_KEY0-3, CH1_KEY0-3	CH4_KEY0-CH5_KEY3	CH0_IV0-3

16.5.7 HASH Data Path

HASH and AES could run in parallel way. There are 2 paths lead to AES-HASH function. One is AES-HASH-RX mode, the other is AES-HASH-TX mode.

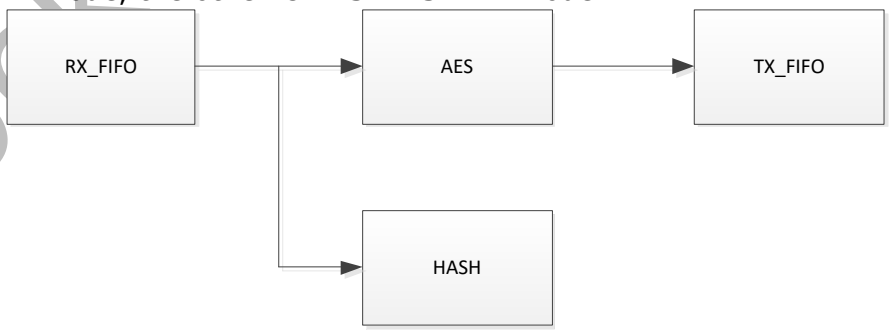


Fig.16-3 AES-HASH-RX Mode

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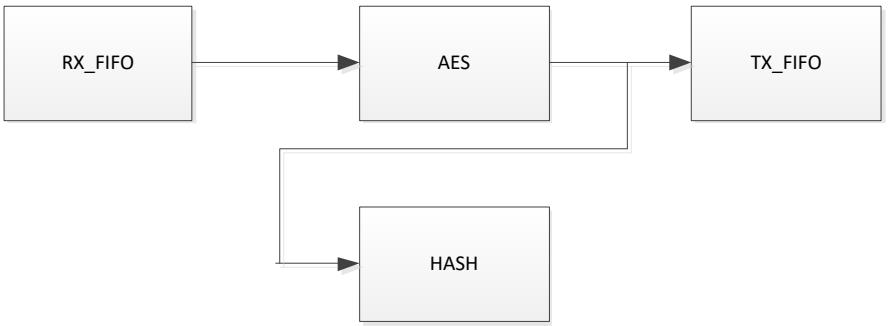


Fig.16-4 AES-HASH-TX Mode

As shown in the figures above, we could facilitate operations in some cases. For example, secure boot, we need both AES and HASH operations for the same blocks of data. The data HASH gets from RX_FIFO or TX_FIFO is byte swapped if the byte swap function is configured.

16.5.8 Programming Step

The application could succeed various CRYPTO operations if they program properly.

- Program the LLI address to DMA_LLI_ADDR
- Program KEY, IV, or other parameter if needed
- Program BC_CTL or HASH_CTL for control information
- Prepare LLI Item
- Enable interrupt, or do nothing

All these operations could be in any order.

- Program DMA_CTL.start or DMA_CTL.restart to start the operation

This step should be the last configuration step. After this register is configured, other registers should not be changed

- Wait interrupt asserted, or just poll the DMA_INT_ST bits
- Program DMA_INT_ST to clear interrupt status, and get the result
- Wait HASH_VALID or TAG_VALID, then get the hsah or tag result if needed. After the bit is read by application, it should be cleared by writing 1 to this bit.

The application could also use LLI.pause when the next LLI item is not ready. After the new item is prepared, the application could program BC_MID_IV0~5 or HASH_MID_DATA0~25, and then program DMA_CTL.restart to continue previous operation. When LLI.pause of LLI's last item is 1, the application also need to poll BC_MID_VALID or HASH_VALID to_get the intermediate value.

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Chapter 17 Mobile Storage Host Controller(SDMMC&SDIO)

17.1 Overview

The Mobile Storage Host Controller is designed to support Secure Digital memory (SD-max version 3.01) with 1 bits or 4 bits data width, Multimedia Card(MMC-max version 4.51) with 1 bits or 4 bits or 8 bits data width.
The Host Controller is instantiated for SDMMC0, SDMMC1. The interface difference between these instances is shown in "Interface Description".
The Host Controller supports following features:

- Bus Interface Features:
  - Support AMBA AHB interface for master and slave
  - Supports internal DMA interface(IDMAC)
    - Supports 16/32-bit data transfers
    - Single engine used for Transmit and Receive, which are mutually exclusive
    - Dual-buffer and chained descriptor linked list
    - Each descriptor can transfer up to 4KB of data in chained mode and 8KB of data in dual-buffer mode
    - Programmable burst size for optimal host bus utilization
  - Support combined single FIFO for both transmit and receive operations
  - Support FIFO size of 256x32
  - Support FIFO over-run and under-run prevention by stopping card clock
- Card Interface Features:
  - Support Secure Digital memory protocol commands
  - Support Secure Digital I/O protocol commands
  - Support Multimedia Card protocol commands
  - Support Command Completion Signal and interrupts to host
  - Support CRC generation and error detection
  - Support programmable baud rate
  - Support power management and power switch
  - Support card detection
  - Support write protection
  - Support hardware reset
  - Support SDIO interrupts in 1-bit and 4-bit modes
  - Support 4-bit mode in SDIO3.0
  - Support SDIO suspend and resume operation
  - Support SDIO read wait
  - Support block size of 1 to 65,535 bytes
  - Support 1-bit, 4-bit and 8-bit SDR modes
  - Supports 4-bit and 8-bit DDR
  - Support boot in 1-bit, 4-bit and 8-bit SDR modes
- Clock Interface Features:
  - Support 0/90/180/270-degree phase shift operation for sample clock (cclk_in_sample) and drive clock(cclk_in_drv) relative to function clock(cclk_in) respectively
  - Support phase tuning using delay line for sample clock(cclk_in_sample) and drive clock(cclk_in_drv) relative to function clock (cclk_in) respectively. The max number of delay element number is 128.

17.2 Block Diagram

The Host Controller consists of the following main functional blocks.

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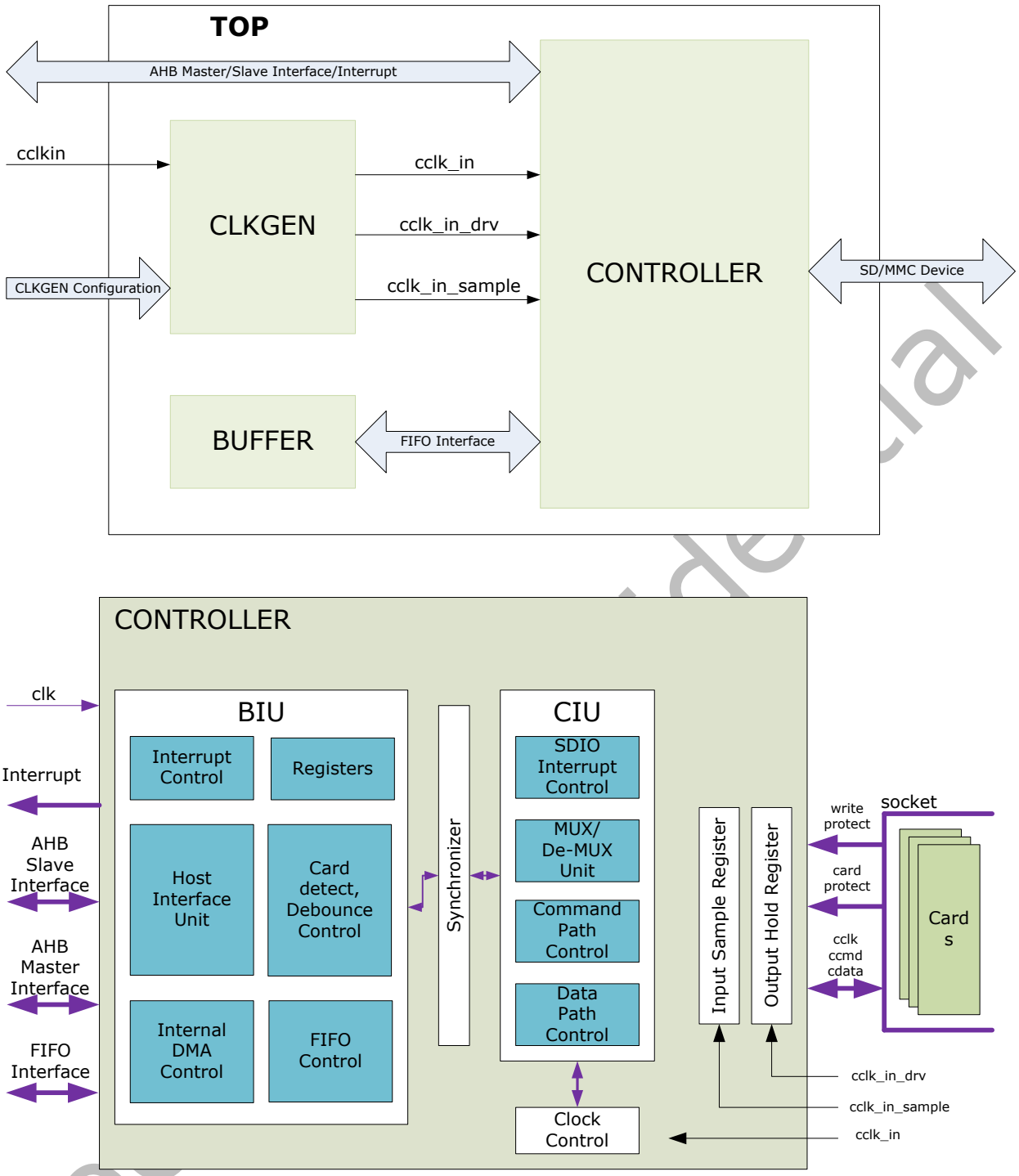


Fig.17-1 Mobile Storage Host Control Block Diagram

- Clock Generate Unit (CLKGEN): Generates card interface clock cclk_in/ cclk_sample/cclk_drv based on cclkin and configuration information.
  - cclkin: original clock
  - cclk_in: functional clock
  - cclk_sample: sample clock
  - cclk_drv: driver clock
- Asynchronous dual-port memory (BUFFER): Use a two-clock synchronous read and synchronous write dual-port RAM. One of the ports is connected to the host clock, and the other port is connected to the card clock.
- Bus Interface Unit (BIU): Provides AMBA AHB interfaces for register and data read/write.

Card Interface Unit (CIU): Takes care of the SD/MMC protocols and provides clock management.

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17.3 Function Description

17.3.1 17.3.1 Bus Interface Unit

The Bus Interface Unit provides the following functions:

- Host interface
- Interrupt control
- Register access
- External FIFO access
- Card detection

17.3.1.1 Host Interface Unit

The Host Interface Unit is an AHB slave interface, which provides the interface between the SD/MMC card and the host bus.

17.3.1.2 Register Unit

The register unit is part of the bus interface unit; it provides read and write access to the registers.

All registers reside in the Bus Interface Unit clock domain. When a command is sent to a card by setting the start_bit, which is bit[31] of the SDMMC_CMD register, all relevant registers needed for the CIU operation are transferred to the CIU block. During this time, the registers that are transferred from the BIU to the CIU should not be written. The software should wait for the hardware to clear the start bit before writing to these registers again. The register unit has a hardware locking feature to prevent illegal writes to registers. The lock is necessary in order to avoid metastability violations, both because the host and card clock domains are different and to prevent illegal software operations.

Once a command start is issued by setting the start_bit of the SDMMC_CMD register, the following registers cannot be reprogrammed until the command is accepted by the card interface unit:

- SDMMC_CMD
- SDMMC_CMDARG
- SDMMC_BYTCNT
- SDMMC_BLKSIZ
- SDMMC_CLKDIV
- SDMMC_CLKENA
- SDMMC_CLKSRC
- SDMMC_TMOUT
- SDMMC_CTYPE

The hardware resets the start_bit once the CIU accepts the command. If a host write to any of these registers is attempted during this locked time, then the write is ignored and the hardware lock error bit is set in the raw interrupt status register. Additionally, if the interrupt is enabled and not masked for a hardware lock error, then an interrupt is sent to the host.

When the Card Interface Unit is in an idle state, it typically takes the following number of clocks for the command handshake, where clk is the BIU clock and cclk_in is the CIU clock:
3 (clk) + 3 (cclk_in)

Once a command is accepted, you can send another command to the CIU-which has a one-deep command queue-under the following conditions:

- If the previous command was not a data transfer command, the new command is sent to the SD/MMC card once the previous command completes.
- If the previous command is a data transfer command and if wait_prvdata_complete (bit[13]) of the SDMMC_CMD register is set for the new command, the new command is sent to the SD/MMC card only when the data transfer completes.

If the wait_prvdata_complete is 0, then the new command is sent to the SD/MMC card as soon as the previous command is sent. Typically, you should use this only to stop or abort a previous data transfer or query the card status in the middle of a data transfer.

17.3.1.3 Interrupt Controller Unit

The interrupt controller unit generates an interrupt that depends on the controller raw interrupt status, the interrupt-mask register, and the global interrupt-enable register bit.

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Once an interrupt condition is detected, it sets the corresponding interrupt bit in the raw interrupt status register SDMMC_RINTSTS. The raw interrupt status bit stays on until the software clears the bit by writing a 1 to the interrupt bit; a 0 leaves the bit untouched.
The interrupt port is an active-high, level-sensitive interrupt. The interrupt port is active only when any bit in the raw interrupt status register is active, the corresponding interrupt mask bit is 1, and the global interrupt enable bit is 1. The interrupt port is registered in order to avoid any combinational glitches.
The int_enable is reset to 0 on power-on, and the interrupt mask bits are set to 32'h0, which masks all the interrupts.

Notes:
Before enabling the interrupt, it is always recommended that you write 32'hffff_ffff to the raw interrupt status register in order to clear any pending unserviced interrupts. When clearing interrupts during normal operation, ensure that you clear only the interrupt bits that you serviced.
The SDIO Interrupts, Receive FIFO Data Request (RXDR), and Transmit FIFO Data Request (TXDR) are set by level-sensitive interrupt sources. Therefore, the interrupt source should be first cleared before you can clear the interrupt bit of the Raw Interrupt register. For example, on seeing the Receive FIFO Data Request (RXDR) interrupt, the FIFO should be emptied so that the "FIFO count greater than the RX-Watermark" condition, which triggers the interrupt, becomes inactive. The rest of the interrupts are triggered by a single clock-pulse-width source.

Table 17-1 Bits in Interrupt Status Register

Bits	Interrupt	Description
24	sdio_interrupt	Interrupt from SDIO card. In MMC-Ver3.3-only mode, these bits are always 0.
16	Card no-busy	If card exit busy status, the interrupt happened.
15	End Bit Error (read) / Write no CRC (EBE)	Error in end-bit during read operation, or no data CRC received during write operation. For MMC CMD19, there may be no CRC status returned by the card. Hence, EBE is set for CMD19. The application should not treat this as an error.
14	Auto Command Done (ACD)	Stop/abort commands automatically sent by card unit and not initiated by host; similar to Command Done (CD) interrupt. Recommendation: Software typically need not enable this for non CE-ATA accesses; Data Transfer Over (DTO) interrupt that comes after this interrupt determines whether data transfer has correctly competed.
13	Start Bit Error (SBE)	Error in data start bit when data is read from a card. In 4-bit mode, if DAT[0] line indicates start bit-that is, 0-and any of the other data bits do not have start bit, then this error is set. Busy Complete Interrupt when data is written to the card. This interrupt is generated after completion of busy driven by the card after the last data block is written into the card.
12	Hardware Locked write Error (HLE)	During hardware-lock period, write attempted to one of locked registers. When software sets the start_cmd bit in the SDMMC_CMD register, the Host Controller tries to load the command. If the command buffer is already filled with a command, this error is raised. The software then has to reload the command.
11	FIFO Underrun/ Overrun Error (FRUN)	Host tried to push data when FIFO was full, or host tried to read data when FIFO was empty. Typically this should not happen, except due to error in software. Card unit never pushes data into FIFO when FIFO is full, and pop data when FIFO is empty. If IDMAC is enabled, FIFO under-run/over-run can

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Bits	Interrupt	Description
		occur due to a programming error on MSIZE and watermark values in SDMMC_FIFOTH register.
10	Data Starvation by Host Timeout (HTO)	To avoid data loss, card clock out is stopped if FIFO is empty when writing to card, or FIFO is full when reading from card. Whenever card clock is stopped to avoid data loss, data-starvation timeout counter is started with data-timeout value. This interrupt is set if host does not fill data into FIFO during write to card, or does not read from FIFO during read from card before timeout period. Even after timeout, card clock stays in stopped state, with CIU state machines waiting. It is responsibility of host to push or pop data into FIFO upon interrupt, which automatically restarts cclk_out and card state machines. Even if host wants to send stop/abort command, it still needs to ensure it has to push or pop FIFO so that clock starts in order for stop/abort command to send on command signal along with data that is sent or received on data line.
9	Data Read Timeout (DRTO)	In Normal functioning mode: Data read timeout (DRTO) Data timeout occurred. Data Transfer Over (DTO) also set if data timeout occurs. In Boot Mode: Boot Data Start (BDS) When set, indicates that Host Controller has started to receive boot data from the card. A write to this register with a value of 1 clears this interrupt.
8	Response Timeout (RTO)	In normal functioning mode: Response timeout (RTO) Response timeout occurred. Command Done (CD) also set if response timeout occurs. If command involves data transfer and when response times out, no data transfer is attempted by Host Controller. In Boot Mode: Boot Ack Received (BAR) When expect_boot_ack is set, on reception of a boot acknowledge pattern—0-1-0—this interrupt is asserted. A write to this register with a value of 1 clears this interrupt.
7	Data CRC Error (DCRC)	Received Data CRC does not match with locally-generated CRC in CIU. Can also occur if the Write CRC status is incorrectly sampled by the Host.
6	Response CRC Error (RCRC)	Response CRC does not match with locally-generated CRC in CIU.
5	Receive FIFO Data Request (RXDR)	Interrupt set during read operation from card when FIFO level is greater than Receive-Threshold level. Recommendation: In DMA modes, this interrupt should not be enabled. In non-DMA mode: pop RX_WMark + 1 data from FIFO.
4	Transmit FIFO Data Request (TXDR)	Interrupt set during write operation to card when FIFO level reaches less than or equal to Transmit-Threshold level. Recommendation: In DMA modes, this interrupt should not be enabled. In non-DMA mode:

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Bits	Interrupt	Description

		if (pending_bytes > (FIFO_DEPTH - TX_WMark))
		push (FIFO_DEPTH - TX_WMark) data into FIFO
		else
		push pending_bytes data into FIFO

3	Data Transfer Over (DTO)	Indicates Data transfer completed. Though on detection of errors-Start Bit Error, Data CRC error, and so on, DTO may or may not be set; the application must issue CMD12, which ensures that DTO is set. Recommendation: In non-DMA mode, when data is read from card, on seeing interrupt, host should read any pending data from FIFO. In DMA mode, DMA controllers guarantee FIFO is flushed before interrupt. DTO bit is set at the end of the last data block, even if the device asserts MMC busy after the last data block.
2	Command Done(CD)	Command sent to card and got response from card, even if Response Error or CRC error occurs.
1	Response Error (RE)	Error in received response set if one of following occurs: ● Transmission bit != 0 ● Command index mismatch ● End-bit != 1
0	Card-Detect (CDT)	When one or more cards inserted or removed, this interrupt occurs. Software should read card-detect register to determine current card status. Recommendation: After power-on and before enabling interrupts, software should read card detect register and store it in memory. When interrupt occurs, it should read card detect register and compare it with value stored in memory to determine which card(s) were removed/inserted. Before exiting ISR, software should update memory with new card-detect value.

17.3.1.4 FIFO Controller Unit

The FIFO controller interfaces the external FIFO to the host interface and the card controller unit. When FIFO overrun and under-run conditions occur, the card clock stops in order to avoid data loss.

The FIFO uses a two-clock synchronous read and synchronous write dual-port RAM. One of the ports is connected to the host clock(clk), and the second port is connected to the card clock(cclk_in).

17.3.1.5 Card Detection Unit

The register unit has registers that control the power. Power to each card can be selectively turned on or off.

The card detection unit looks for any changes in the card-detect signals for card insertion or card removal. It filters out the debounce associated with mechanical insertion or removal, and generates one interrupt to the host. You can program the debounce filter value.

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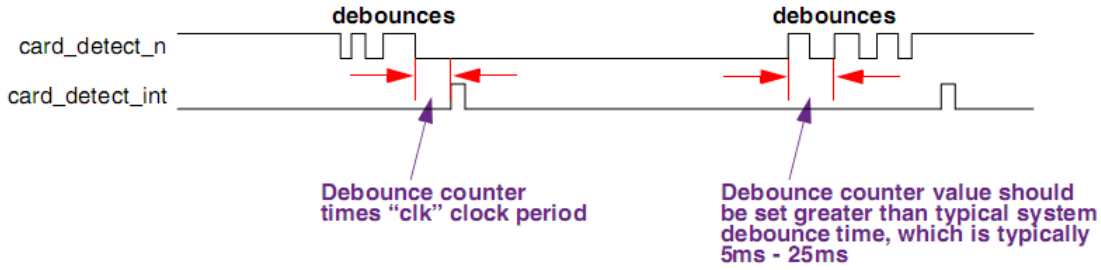


Fig.17-2 SD/MMC Card-Detect Signal

17.3.2 Card Interface Unit

The Card Interface Unit (CIU) interfaces with the Bus Interface Unit (BIU) and the external devices. The host writes command parameters to the BIU control registers, and these parameters are then passed to the CIU. Depending on control register values, the CIU generates SD/MMC command and data traffic on a selected card bus according to SD/MMC protocol. The Host Controller accordingly controls the command and data path.

The following software restrictions should be met for proper CIU operation:

- Only one data transfer command can be issued at a time.
- During an open-ended card write operation, if the card clock is stopped because the FIFO is empty, the software must first fill the data into the FIFO and start the card clock. It can then issue only a stop/abort command to the card.
- When issuing card reset commands (CMD0, CMD15 or CMD52_reset) while a card data transfer is in progress, the software must set the stop_abort_cmd bit in the SDMMC_CMD register so that the Host Controller can stop the data transfer after issuing the card reset command.
- When the data end bit error is set in the SDMMC_RINTSTS register, the Host Controller does not guarantee SDIO interrupts. The software should ignore the SDIO interrupts and issue the stop/abort command to the card, so that the card stops sending the read data.
- If the card clock is stopped because the FIFO is full during a card read, the software should read at least two FIFO locations to start the card clock.

The CIU block consists of the following primary functional blocks:

- Command path
- Data path
- SDIO interrupt control
- Clock control
- Error detection

17.3.2.1 Command Path

The command path performs the following functions:

- Loads clock parameters
- Loads card command parameters
- Sends commands to card bus (ccmd_out line)
- Receives responses from card bus (ccmd_in line)
- Sends responses to BIU
- Drives the P-bit on command line

A new command is issued to the Host Controller by programming the BIU registers and setting the start_cmd bit in the SDMMC_CMD register. The BIU asserts start_cmd, which indicates that a new command is issued to the SD/MMC device. The command path loads this new command (command, command argument, timeout) and sends acknowledge to the BIU by asserting cmd_taken.

Once the new command is loaded, the command path state machine sends a command to the device bus-including the internally generated CRC7-and receives a response, if any. The state machine then sends the received response and signals to the BIU that the command is done, and then waits for eight clocks before loading a new command.

Load Command Parameters

One of the following commands or responses is loaded in the command path:

- New command from BIU – When start_cmd is asserted, then the start_cmd bit is set in the SDMMC_CMD register.

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- Internally generated auto-stop command – When the data path ends, the stop command request is loaded.
- IRQ response with RCA 0x000 – When the command path is waiting for an IRQ response from the MMC card and a "send irq response" request is signaled by the BIU, then the send_irq_response bit is set in the SDMMC_CTRL register.

Loading a new command from the BIU in the command path depends on the following SDMMC_CMD register bit settings:

- update_clock_registers_only – If this bit is set in the SDMMC_CMD register, the command path updates only the clock enable, clock divider, and clock source registers. If this bit is not set, the command path loads the command, command argument, and timeout registers; it then starts processing the new command.
- wait_prvdata_complete – If this bit is set, the command path loads the new command under one of the following conditions:
  - Immediately, if the data path is free (that is, there is no data transfer in progress), or if an open-ended data transfer is in progress (byte_count = 0).
  - After completion of the current data transfer, if a predefined data transfer is in progress.

Send Command and Receive Response

Once a new command is loaded in the command path, update_clock_registers_only bit is unset – the command path state machine sends out a command on the device bus; the command path state machine is illustrated in following figure.

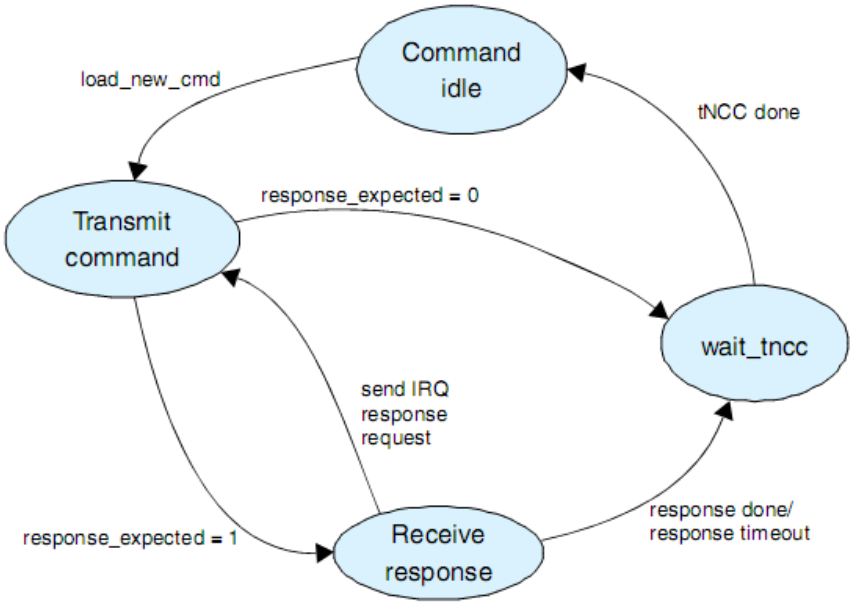


Fig.17-3 Host Controller Command Path State Machine

The command path state machine performs the following functions, according to SDMMC_CMD register bit values:

- send_initialization – Initialization sequence of 80 clocks is sent before sending the command.
- response_expected – Response is expected for the command. After the command is sent out, the command path state machine receives a 48-bit or 136-bit response and sends it to the BIU. If the start bit of the card response is not received within the number of clocks programmed in the timeout register, then the response timeout and command done bit is set in the Raw Interrupt Status register as a signal to the BIU. If the response-expected bit is not set, the command path sends out a command and signals a response done to the BIU; that is, the command done bit is set in the Raw Interrupt Status register.
- response_length – If this bit is set, a 136-bit response is received; if it is not set, a 48-bit response is received.
- check_response_crc – If this bit is set, the command path compares CRC7 received in the response with the internally-generated CRC7. If the two do not match, the response CRC error is signaled to the BIU; that is, the response CRC error bit is set in

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the Raw Interrupt Status register SDMMC_RINTSTS.

Send Response to BIU

If the response_expected bit is set in the SDMMC_CMD register, the received response is sent to the BIU. The Response0 register is updated for a short response, and the Response3, Response2, Response1, and Response0 registers are updated on a long response, after which the Command Done bit is set. If the response is for an auto_stop command sent by the CIU, the response is saved in the Response1 register, after which the Auto Command Done bit is set.

Additionally, the command path checks for the following:

- Transmission bit = 0
- Command index matches command index of the sent command
- End bit = 1 in received card response

The command index is not checked for a 136-bit response or if the check_response_crc bit is unset. For a 136-bit response and reserved CRC 48-bit responses, the command index is reserved-that is, 111111.

Polling Command Completion Signal

The device generates the Command Completion Signal in order to notify the host controller of the normal command completion or command termination.

Command Completion Signal Detection and Interrupt to Host Processor

If the ccs_expected bit is set in the SDMMC_CMD register, the Command Completion Signal (CCS) from the device is indicated by setting the Data Transfer Over (DTO) bit in the SDMMC_RINTSTS register. The Host Controller generates a Data Transfer Over (DTO) interrupt if this interrupt is not masked.

Command Completion Signal Timeout

If the command expects a CCS from the device—if the ccs_expected bit is set in the SDMMC_CMD register—the command state machine waits for the CCS and remains in a wait_CCSS state. If the device fails to send out the CCS, the host software should implement a timeout mechanism to free the command and data path. The host controller does not implement a hardware timer; it is the responsibility of the host software to maintain a software timer.

In the event of a CCS timeout, the host should issue a CCSD by setting the send_ccsd bit in the CTRL register. The host controller command state machine sends the CCSD to the device and exits to an idle state. After sending the CCSD, the host should also send a CMD12 to the device in order to abort the outstanding command.

Send Command Completion Signal Disable

If the send_ccsd bit is set in the SDMMC_CTRL register, the host sends a Command Completion Signal Disable (CCSD) pattern on the CMD line. The host can send the CCSD while waiting for the CCS or after a CCS timeout happens.

After sending the CCSD pattern, the host sets the Command Done (CD) bit in SDMMC_RINTSTS and also generates an interrupt to the host if the Command Done interrupt is not masked.

17.3.2.2 Data Path

The data path block pops the data FIFO and transmits data on cdata_out during a write data transfer, or it receives data on cdata_in and pushes it into the FIFO during a read data transfer. The data path loads new data parameters—that is, data expected, read/write data transfer, stream/block transfer, block size, byte count, card type, timeout registers—whenever a data transfer command is not in progress.

If the data_expected bit is set in the SDMMC_CMD register, the new command is a data transfer command and the data path starts one of the following:

- Transmit data if the read/write bit = 1
- Data receive if read/write bit = 0

Data Transmit

The data transmit state machine, illustrated in following figure, starts data transmission two clocks after a response for the data write command is received; this occurs even if the command path detects a response error or response CRC error. If a response is not received from the card because of a response timeout, data is not transmitted. Depending upon the value of the transfer_mode bit in the SDMMC_CMD register, the data transmit

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state machine puts data on the card data bus in a stream or in block(s).

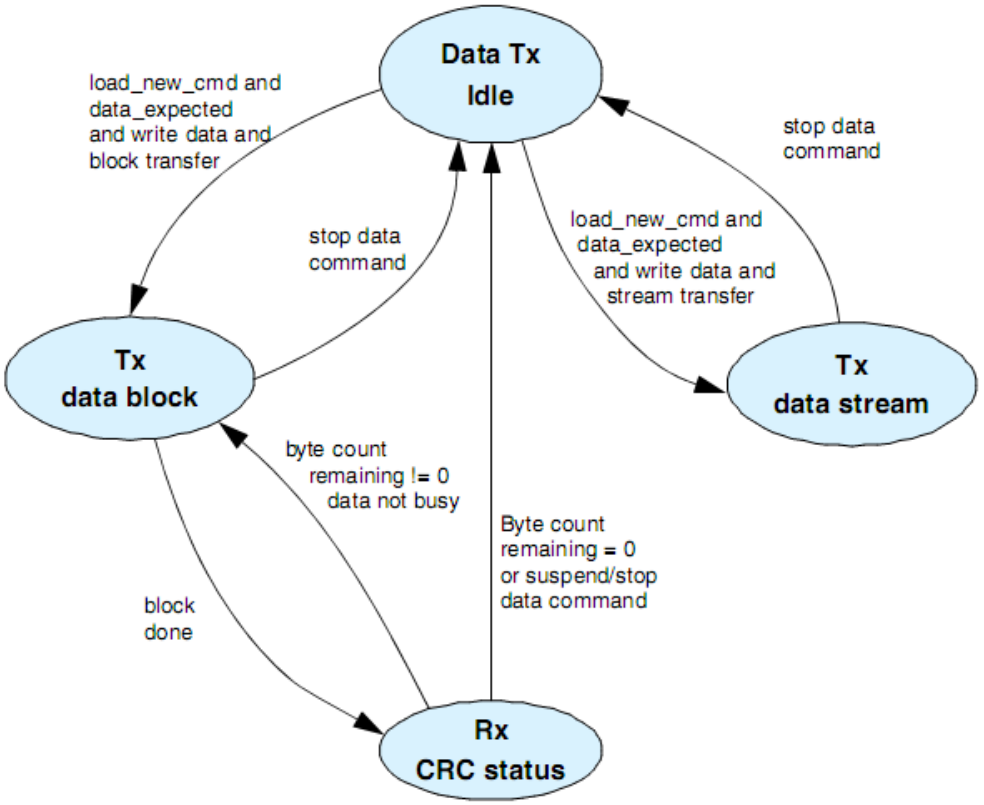


Fig.17-4 Host Controller Data Transmit State Machine

Stream Data Transmit

If the transfer_mode bit in the SDMMC_CMD register is set to 1, it is a stream-write data transfer. The data path pops the FIFO from the BIU and transmits in a stream to the card data bus. If the FIFO becomes empty, the card clock is stopped and restarted once data is available in the FIFO.

If the byte_count register is programmed to 0, it is an open-ended stream-write data transfer. During this data transfer, the data path continuously transmits data in a stream until the host software issues a stop command. A stream data transfer is terminated when the end bit of the stop command and end bit of the data match over two clocks.

If the byte_count register is programmed with a non-zero value and the send_auto_stop bit is set in the SDMMC_CMD register, the stop command is internally generated and loaded in the command path when the end bit of the stop command occurs after the last byte of the stream write transfer matches.

This data transfer can also terminate if the host issues a stop command before all the data bytes are transferred to the card bus.

Single Block Data

If the transfer_mode bit in the SDMMC_CMD register is set to 0 and the byte_count register value is equal to the value of the block_size register, a single-block write-data transfer occurs. The data transmit state machine sends data in a single block, where the number of bytes equals the block size, including the internally-generated CRC16.

If the SDMMC_CTYPE register bit for the selected card – indicated by the card_num value in the SDMMC_CMD register – is set for a 1-bit, 4-bit, or 8-bit data transfer, the data is transmitted on 1, 4, or 8 data lines, respectively, and CRC16 is separately generated and transmitted for 1, 4, or 8 data lines, respectively.

After a single data block is transmitted, the data transmit state machine receives the CRC status from the card and signals a data transfer to the BIU; this happens when the data-transfer-over bit is set in the SDMMC_RINTSTS register.

If a negative CRC status is received from the card, the data path signals a data CRC error to the BIU by setting the data CRC error bit in the SDMMC_RINTSTS register.

Additionally, if the start bit of the CRC status is not received by two clocks after the end of the data block, a CRC status start bit error is signaled to the BIU by setting the write-no-

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CRC bit in the SDMMC_RINTSTS register.

Multiple Block Data

A multiple-block write-data transfer occurs if the transfer_mode bit in the SDMMC_CMD register is set to 0 and the value in the byte_count register is not equal to the value of the block_size register. The data transmit state machine sends data in blocks, where the number of bytes in a block equals the block size, including the internally-generated CRC16. If the SDMMC_CTYPE register bit for the selected card – indicated by the card_num value in the SDMMC_CMD register – is set to 1-bit, 4-bit, or 8-bit data transfer, the data is transmitted on 1, 4, or 8 data lines, respectively, and CRC16 is separately generated and transmitted on 1, 4, or 8 data lines, respectively.

After one data block is transmitted, the data transmit state machine receives the CRC status from the card. If the remaining byte_count becomes 0, the data path signals to the BIU that the data transfer is done; this happens when the data-transfer-over bit is set in the SDMMC_RINTSTS register.

If the remaining data bytes are greater than 0, the data path state machine starts to transmit another data block.

If a negative CRC status is received from the card, the data path signals a data CRC error to the BIU by setting the data CRC error bit in the SDMMC_RINTSTS register, and continues further data transmission until all the bytes are transmitted.

Additionally, if the CRC status start bit is not received by two clocks after the end of a data block, a CRC status start bit error is signaled to the BIU by setting the write-no-CRC bit in the SDMMC_RINTSTS register; further data transfer is terminated.

If the send_auto_stop bit is set in the SDMMC_CMD register, the stop command is internally generated during the transfer of the last data block, where no extra bytes are transferred to the card. The end bit of the stop command may not exactly match the end bit of the CRC status in the last data block.

If the block size is less than 4, 16, or 32 for card data widths of 1 bit, 4 bits, or 8 bits, respectively, the data transmit state machine terminates the data transfer when all the data is transferred, at which time the internally generated stop command is loaded in the command path.

If the byte_count is 0 – the block size must be greater than 0 – it is an open-ended block transfer. The data transmit state machine for this type of data transfer continues the block-write data transfer until the host software issues a stop or abort command.

Data Receive

The data-receive state machine, illustrated in following figure, receives data two clock cycles after the end bit of a data read command, even if the command path detects a response error or response CRC error. If a response is not received from the card because a response timeout occurs, the BIU does not receive a signal that the data transfer is complete; this happens if the command sent by the Host Controller is an illegal operation for the card, which keeps the card from starting a read data transfer.

If data is not received before the data timeout, the data path signals a data timeout to the BIU and an end to the data transfer done. Based on the value of the transfer_mode bit in the SDMMC_CMD register, the data-receive state machine gets data from the card data bus in a stream or block(s).

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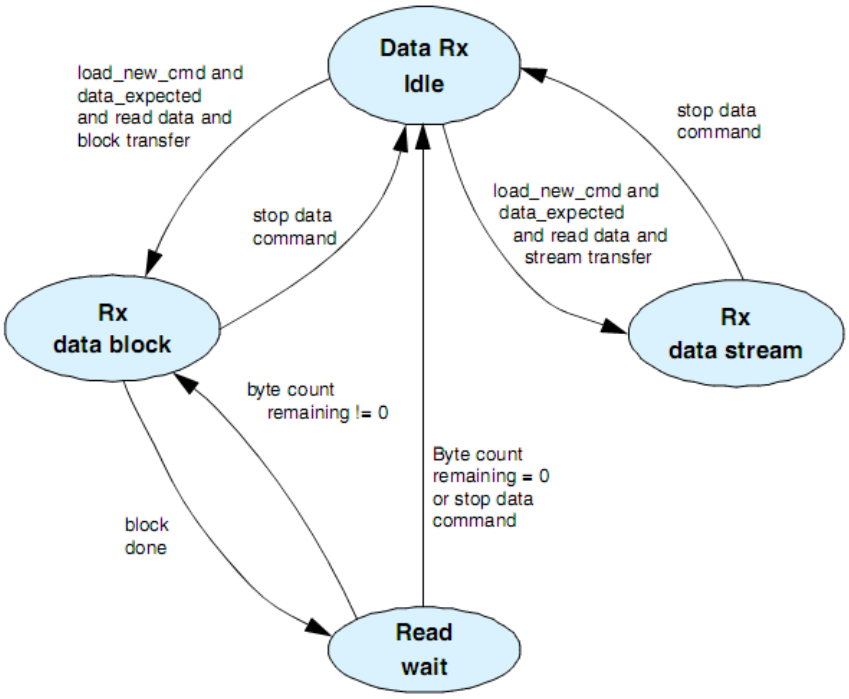


Fig.17-5 Host Controller Data Receive State Machine

Stream Data Read

A stream-read data transfer occurs if the transfer_mode bit in the SDMMC_CMD register equals 1, at which time the data path receives data from the card and pushes it to the FIFO. If the FIFO becomes full, the card clock stops and restarts once the FIFO is no longer full.

An open-ended stream-read data transfer occurs if the byte_count register equals 0. During this type of data transfer, the data path continuously receives data in a stream until the host software issues a stop command. A stream data transfer terminates two clock cycles after the end bit of the stop command.

If the byte_count register contains a non-zero value and the send_auto_stop bit is set in the SDMMC_CMD register, a stop command is internally generated and loaded into the command path, where the end bit of the stop command occurs after the last byte of the stream data transfer is received. This data transfer can terminate if the host issues a stop or abort command before all the data bytes are received from the card.

Single-Block Data Read

A single-block read-data transfer occurs if the transfer_mode bit in the SDMMC_CMD register is set to 0 and the value of the byte_count register is equal to the value of the block_size register. When a start bit is received before the data times out, data bytes equal to the block size and CRC16 are received and checked with the internally-generated CRC16. If the SDMMC_CTYPE register bit for the selected card – indicated by the card_num value in the SDMMC_CMD register – is set to a 1-bit, 4-bit, or 8-bit data transfer, data is received from 1, 4, or 8 data lines, respectively, and CRC16 is separately generated and checked for 1, 4, or 8 data lines, respectively. If there is a CRC16 mismatch, the data path signals a data CRC error to the BIU. If the received end bit is not 1, the BIU receives an end-bit error.

Multiple-Block Data Read

If the transfer_mode bit in the SDMMC_CMD register is set to 0 and the value of the byte_count register is not equal to the value of the block_size register, it is a multiple-block read-data transfer. The data-receive state machine receives data in blocks, where the number of bytes in a block is equal to the block size, including the internally-generated CRC16.

If the SDMMC_CTYPE register bit for the selected card – indicated by the card_num value in the SDMMC_CMD register – is set to a 1-bit, 4-bit, or 8-bit data transfer, data is received from 1, 4, or 8 data lines, respectively, and CRC16 is separately generated and checked for 1, 4, or 8 data lines, respectively.

After a data block is received, if the remaining byte_count becomes 0, the data path signals

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a data transfer to the BIU.
If the remaining data bytes are greater than 0, the data path state machine causes another data block to be received. If CRC16 of a received data block does not match the internally-generated CRC16, a data CRC error to the BIU and data reception continue further data transmission until all bytes are transmitted.
Additionally, if the end of a received data block is not 1, data on the data path signals terminate the bit error to the CIU and the data-receive state machine terminates data reception, waits for data timeout, and signals to the BIU that the data transfer is complete.
If the send_auto_stop bit is set in the SDMMC_CMD register, the stop command is internally generated when the last data block is transferred, where no extra bytes are transferred from the card; the end bit of the stop command may not exactly match the end bit of the last data block.
If the requested block size for data transfers to cards is less than 4, 16, or 32 bytes for 1-bit, 4-bit, or 8-bit data transfer modes, respectively, the data-transmit state machine terminates the data transfer when all data is transferred, at which point the internally-generated stop command is loaded in the command path. Data received from the card after that are then ignored by the data path.
If the byte_count is 0—the block size must be greater than 0—it is an open-ended block transfer. For this type of data transfer, the data-receive state machine continues the block-read data transfer until the host software issues a stop or abort command.

Auto-Stop

The Host Controller internally generates a stop command and is loaded in the command path when the send_auto_stop bit is set in the SDMMC_CMD register.
The software should set the send_auto_stop bit according to details listed in following table.

Table 17-2 Auto-Stop Generation

Card type	Transfer type	Byte Count	send_auto_stop bit set	Comments
MMC	Stream read	0	No	Open-ended stream
MMC	Stream read	>0	Yes	Auto-stop after all bytes transfer
MMC	Stream write	0	No	Open-ended stream
MMC	Stream write	>0	Yes	Auto-stop after all bytes transfer
MMC	Single-block read	>0	No	Byte count =0 is illegal
MMC	Single-block write	>0	No	Byte count =0 is illegal
MMC	Multiple-block read	0	No	Open-ended multiple block
MMC	Multiple-block read	>0	Yes①	Pre-defined multiple block
MMC	Multiple-block write	0	No	Open-ended multiple block
MMC	Multiple-block write	>0	Yes①	Pre-defined multiple block
SDMEM	Single-block read	>0	No	Byte count =0 is illegal
SDMEM	Single-block write	>0	No	Byte count =0 illegal
SDMEM	Multiple-block read	0	No	Open-ended multiple block
SDMEM	Multiple-block read	>0	Yes	Auto-stop after all bytes transfer
SDMEM	Multiple-block write	0	No	Open-ended multiple block
SDMEM	Multiple-block write	>0	Yes	Auto-stop after all bytes transfer
SDIO	Single-block read	>0	No	Byte count =0 is illegal
SDIO	Single-block write	>0	No	Byte count =0 illegal
SDIO	Multiple-block	0	No	Open-ended multiple block

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Card type	Transfer type	Byte Count	send_auto_stop bit set	Comments
	read			
SDIO	Multiple-block read	>0	No	Pre-defined multiple block
SDIO	Multiple-block write	0	No	Open-ended multiple block
SDIO	Multiple-block write	>0	No	Pre-defined multiple block

*①:The condition under which the transfer mode is set to block transfer and byte_count is equal to block size is treated as a single-block data transfer command for both MMC and SD cards. If byte_count = n*block_size (n = 2, 3, …), the condition is treated as a predefined multiple-block data transfer command. In the case of an MMC card, the host software can perform a predefined data transfer in two ways: 1) Issue the CMD23 command before issuing CMD18/CMD25 commands to the card – in this case, issue MD18/CMD25 commands without setting the send_auto_stop bit. 2) Issue CMD18/CMD25 commands without issuing CMD23 command to the card, with the send_auto_stop bit set. In this case, the multiple-block data transfer is terminated by an internally-generated auto-stop command after the programmed byte count.*

The following list conditions for the auto-stop command.

- Stream read for MMC card with byte count greater than 0 – The Host Controller generates an internal stop command and loads it into the command path so that the end bit of the stop command is sent out when the last byte of data is read from the card and no extra data byte is received. If the byte count is less than 6 (48 bits), a few extra data bytes are received from the card before the end bit of the stop command is sent.
- Stream write for MMC card with byte count greater than 0 - The Host Controller generates an internal stop command and loads it into the command path so that the end bit of the stop command is sent when the last byte of data is transmitted on the card bus and no extra data byte is transmitted. If the byte count is less than 6 (48 bits), the data path transmits the data last in order to meet the above condition.
- Multiple-block read memory for SD card with byte count greater than 0 – If the block size is less than 4 (single-bit data bus), 16 (4-bit data bus), or 32 (8-bit data bus), the auto-stop command is loaded in the command path after all the bytes are read. Otherwise, the top command is loaded in the command path so that the end bit of the stop command is sent after the last data block is received.
- Multiple-block write memory for SD card with byte count greater than 0 – If the block size is less than 3 (single-bit data bus), 12 (4-bit data bus), or 24 (8-bit data bus), the auto-stop command is loaded in the command path after all data blocks are transmitted. Otherwise, the stop command is loaded in the command path so that the end bit of the stop command is sent after the end bit of the CRC status is received.

Precaution for host software during auto-stop – Whenever an auto-stop command is issued, the host software should not issue a new command to the SD/MMC device until the auto-stop is sent by the Host Controller and the data transfer is complete. If the host issues a new command during a data transfer with the auto-stop in progress, an auto-stop command may be sent after the new command is sent and its response is received; this can delay sending the stop command, which transfers extra data bytes. For a stream write, extra data bytes are erroneous data that can corrupt the card data. If the host wants to terminate the data transfer before the data transfer is complete, it can issue a stop or abort command, in which case the Host Controller does not generate an auto-stop command.

17.3.2.3 Non-Data Transfer Commands that Use Data Path

Some non-data transfer commands (non-read/write commands) also use the data path. Following table lists the commands and register programming requirements for them.

Table 17-3 Non-data Transfer Commands and Requirements

Base Address [12:8]	CMD 27	CMD 30	CMD 42	ACMD 13	ACMD 22	ACMD 51
SDMMC_CMD register programming						
cmd_index	6'h1B	6'h1E	6'h2A	6'h0D	6'h16	6'h33
response_expect	1	1	1	1	1	1

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Base Address [12:8]	CMD 27	CMD 30	CMD 42	ACMD 13	ACMD 22	ACMD 51
rResponse_length	0	0	0	0	0	0
check_response_crc	1	1	1	1	1	1
data_expected	1	1	1	1	1	1
read/write	1	0	1	0	0	0
transfer_mode	0	0	0	0	0	0
send_auto_stop	0	0	0	0	0	0
wait_prevdata_complete	0	0	0	0	0	0
stop_abort_cmd	0	0	0	0	0	0
Command Argument register programming						
	stuff bits	32-bit write protect data address	stuff bits	stuff bits	stuff bits	stuff bits
Block Size register programming						
	16	4	Num_bytes①	64	4	8
Byte Count register programming						
	16	4	Num_bytes①	64	4	8

①: Num_bytes = No. of bytes specified as per the lock card data structure (Refer to the SD specification and the MMC specification)

17.3.2.4 SDIO Interrupt Control

Interrupts for SD cards are reported to the BIU by asserting an interrupt signal for two clock cycles. SDIO cards signal an interrupt by asserting cdata_in low during the interrupt period; an interrupt period for the selected card is determined by the interrupt control state machine. An interrupt period is always valid for non-active or non-selected cards, and 1-bit data mode for the selected card. An interrupt period for a wide-bus active or selected card is valid for the following conditions:

- Card is idle
- Non-data transfer command in progress
- Third clock after end bit of data block between two data blocks
- From two clocks after end bit of last data until end bit of next data transfer command

Bear in mind that, in the following situations, the controller does not sample the SDIO interrupt of the selected card when the card data width is 4 bits. Since the SDIO interrupt is level-triggered, it is sampled in a further interrupt period and the host does not lose any SDIO interrupt from the card.

- Read/Write Resume – The CIU treats the resume command as a normal data transfer command. SDIO interrupts during the resume command are handled similarly to other data commands. According to the SDIO specification, for the normal data command the interrupt period ends after the command end bit of the data command; for the resume command, it ends after the response end bit. In the case of the resume command, the Controller stops the interrupt sampling period after the resume command end bit, instead of stopping after the response end bit of the resume command.

Suspend during read transfer – If the read data transfer is suspended by the host, the host sets the abort_read_data bit in the controller to reset the data state machine. In the CIU, the SDIO interrupts are handled such that the interrupt sampling starts after the abort_read_data bit is set by the host. In this case the controller does not sample SDIO interrupts between the period from response of the suspend command to setting the abort_read_data bit, and starts sampling after setting the abort_read_data bit.

17.3.2.5 Clock Control

The clock control block provides different clock frequencies required for SD/MMC cards. The cclk_in signal is the source clock (cclk_in >= card max operating frequency) for clock divider of the clock control block. This source clock (cclk_in) is used to generate different card clock frequencies (cclk_out). The card clock can have different clock frequencies, since the card can be a low-speed card or a full-speed card. The Host Controller provides one clock signal (cclk_out).

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The clock frequency of a card depends on the following clock control registers:

- Clock Divider register – Internal clock dividers are used to generate different clock frequencies required for card. The division factor for each clock divider can be programmed by writing to the Clock Divider register. A value of 0 represents a clock-divider bypass, a value of 1 represents a divide by 2.
- Clock Control register – cclk_out can be enabled or disabled for each card under the following conditions:
  - clk_enable – cclk_out for a card is enabled if the clk_enable bit for a card in the Clock Control register is programmed (set to 1) or disabled (set to 0).
  - Low-power mode – Low-power mode of a card can be enabled by setting the low-power mode bit of the Clock Control register to 1. If low-power mode is enabled to save card power, the cclk_out is disabled when the card is idle for at least 8 card clock cycles. It is enabled when a new command is loaded and the command path goes to a non-idle state.

Additionally, cclk_out is disabled when an internal FIFO is full – card read (no more data can be received from card) – or when the FIFO is empty – card write (no data is available for transmission). This helps to avoid FIFO overrun and underrun conditions. It is used by the command and data path to qualify cclk_in for driving outputs and sampling inputs at the programmed clock frequency for the selected card, according to the Clock Divider and Clock Source register values.

Under the following conditions, the card clock is stopped or disabled, along with the active clk_en, for the selected card:

- Clock can be disabled by writing to Clock Enable register (clk_en bit = 1).
- If low-power mode is selected and card is idle, or not selected for 8 clocks.
- FIFO is full and data path cannot accept more data from the card and data transfer is incomplete –to avoid FIFO overrun.

FIFO is empty and data path cannot transmit more data to the card and data transfer is incomplete – to avoid FIFO underrun.

17.3.2.6 Error Detection

- Response
  - Response timeout – Response expected with response start bit is not received within programmed number of clocks in timeout register.
  - Response CRC error – Response is expected and check response CRC requested; response CRC7 does not match with the internally-generated CRC7.
  - Response error – Response transmission bit is not 0, command index does not match with the command index of the send command, or response end bit is not 1.
- Data transmit
  - No CRC status – During a write data transfer, if the CRC status start bit is not received two clocks after the end bit of the data block is sent out, the data path does the following:
    - Signals no CRC status error to the BIU
    - Terminates further data transfer
    - Signals data transfer done to the BIU
  - Negative CRC – If the CRC status received after the write data block is negative (that is, not 010), a data CRC error is signaled to the BIU and further data transfer is continued.
  - Data starvation due to empty FIFO – If the FIFO becomes empty during a write data transmission, or if the card clock is stopped and the FIFO remains empty for data timeout clocks, then a data-starvation error is signaled to the BIU and the data path continues to wait for data in the FIFO.
- Data receive
  - Data timeout – During a read-data transfer, if the data start bit is not received before the number of clocks that were programmed in the timeout register, the data path does the following:
    - Signals data-timeout error to the BIU
    - Terminates further data transfer
    - Signals data transfer done to BIU

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- Data start bit error – During a 4-bit or 8-bit read-data transfer, if the all-bit data line does not have a start bit, the data path signals a data start bit error to the BIU and waits for a data timeout, after which it signals that the data transfer is done.
- Data CRC error – During a read-data-block transfer, if the CRC16 received does not match with the internally generated CRC16, the data path signals a data CRC error to the BIU and continues further data transfer.
- Data end-bit error – During a read-data transfer, if the end bit of the received data is not 1, the data path signals an end-bit error to the BIU, terminates further data transfer, and signals to the BIU that the data transfer is done.

Data starvation due to FIFO full – During a read data transmission and when the FIFO becomes full, the card clock is stopped. If the FIFO remains full for data timeout clocks, a data starvation error is signaled to the BIU (Data Starvation by Host Timeout bit is set in SDMMC_RINTSTS register) and the data path continues to wait for the FIFO to start to empty.

17.3.3 Internal Direct Memory Access Controller (IDMAC)

The Internal Direct Memory Access Controller (IDMAC) has a Control and Status Register (CSR) and a single Transmit/Receive engine, which transfers data from host memory to the device port and vice versa. The controller utilizes a descriptor to efficiently move data from source to destination with minimal Host CPU intervention. You can program the controller to interrupt the Host CPU in situations such as data Transmit and Receive transfer completion from the card, as well as other normal or error conditions.

The IDMAC and the Host driver communicate through a single data structure. CSR addresses 0x80 to 0x98 are reserved for host programming.

The IDMAC transfers the data received from the card to the Data Buffer in the Host memory, and it transfers Transmit data from the Data Buffer in the Host memory to the FIFO. Descriptors that reside in the Host memory act as pointers to these buffers.

A data buffer resides in physical memory space of the Host and consists of complete data or partial data. Buffers contain only data, while buffer status is maintained in the descriptor. Data chaining refers to data that spans multiple data buffers. However, a single descriptor cannot span multiple data.

A single descriptor is used for both reception and transmission. The base address of the list is written into Descriptor List Base Address Register (SDMMC_DBADDR @0x88). A descriptor list is forward linked. The Last Descriptor can point back to the first entry in order to create a ring structure. The descriptor list resides in the physical memory address space of the Host. Each descriptor can point to a maximum of two data buffers.

17.3.3.1 IDMAC CSR Access

When an IDMAC is introduced, an additional CSR space resides in the IDMAC that controls the IDMAC functionality. The host accesses the new CSR space in addition to the existing control register set in the BIU. The IDMAC CSR primarily contains descriptor information. For a write operation to the CSR, the respective CSR logic of the IDMAC and BIU decodes the address before accepting. For a read operation from the CSR, the appropriate CSR read path is enabled.

You can enable or disable the IDMAC operation by programming bit[25] in the SDMMC_CTRL register of the BIU. This allows the data transfer by accessing the slave interface on the AMBA bus if the IDMAC is present but disabled. When IDMAC is enabled, the FIFO cannot be accessed through the slave interface.

17.3.3.2 Descriptors

- Descriptor structures

The IDMAC uses these types of descriptor structures:

- Dual-Buffer Structure – The distance between two descriptors is determined by the Skip Length value programmed in the Descriptor Skip Length (DSL) field of the Bus Mode Register (SDMMC_BMOD @0x80).

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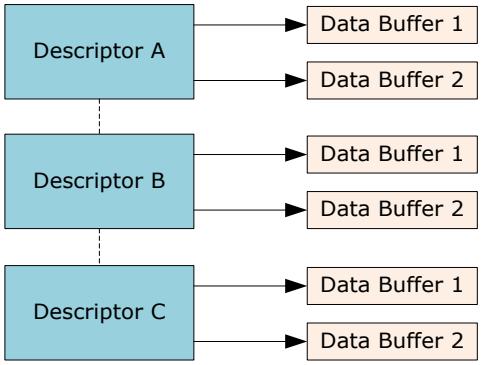


Fig.17-6 Dual-Buffer Descriptor Structure

- Chain Structure – Each descriptor points to a unique buffer and the next descriptor.

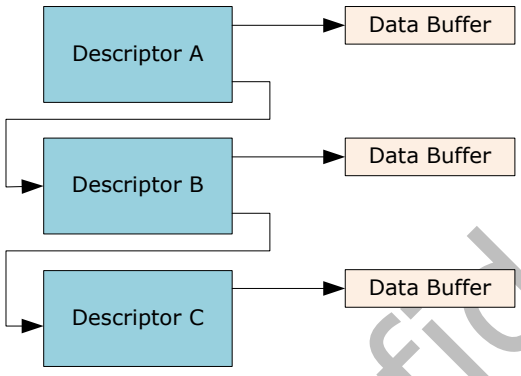


Fig.17-7 Chain Descriptor Structure

- Descriptor formats

Following figure illustrates the internal formats of a descriptor. The descriptor addresses must be aligned to the bus width used for 32-bit AHB data buses. Each descriptor contains 16 bytes of control and status information. DES0 is a notation used to denote the [31:0] bits, DES1 to denote [63:32] bits, DES2 to denote [95:64] bits, DES3 to denote [127:96] bits.

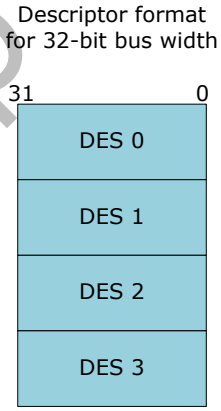


Fig.17-8 Descriptor Formats for 32-bit AHB Address Bus Width

- The DES0 element in the IDMAC contains control and status information.

Table 17-4 Bits in IDMAC DES0 Element

Bit	Name	Description
31	OWN	When set, this bit indicates that the descriptor is owned by the IDMAC. When this bit is reset, it indicates that the descriptor is owned by the Host. The IDMAC clears this bit when it completes the data transfer.
30	Card Error Summary (CES)	These error bits indicate the status of the transaction to or from the card. These bits are also present in SDMMC_RINTSTS Indicates the logical OR of the following bits:

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Bit	Name	Description
		● EBE: End Bit Error ● RTO: Response Time out ● RCRC: Response CRC ● SBE: Start Bit Error ● DRTO: Data Read Timeout ● DCRC: Data CRC for Receive ● RE: Response Error
29:6	Reserved	-
5	End of Ring (ER)	When set, this bit indicates that the descriptor list reached its final descriptor. The IDMAC returns to the base address of the list, creating a Descriptor Ring. This is meaningful for only a dual-buffer descriptor structure.
4	Second Address Chained (CH)	When set, this bit indicates that the second address in the descriptor is the Next Descriptor address rather than the second buffer address. When this bit is set, BS2 (DES1[25:13]) should be all zeros.
3	First Descriptor (FS)	When set, this bit indicates that this descriptor contains the first buffer of the data. If the size of the first buffer is 0, next Descriptor contains the beginning of the data.
2	Last Descriptor (LD)	This bit is associated with the last block of a DMA transfer. When set, the bit indicates that the buffers pointed to by this descriptor are the last buffers of the data. After this descriptor is completed, the remaining byte count is 0. In other words, after the descriptor with the LD bit set is completed, the remaining byte count should be 0.
1	Disable Interrupt on Completion (DIC)	When set, this bit will prevent the setting of the TI/RI bit of the IDMAC Status Register (IDSTS) for the data that ends in the buffer pointed to by this descriptor.
0	Reserved	-

■ The DES1 element contains the buffer size.

Table 17-5 Bits in IDMAC DES1 Element

Bit	Name	Description
31:26	Reserved	-
25:13	Buffer 2 Size (BS2)	These bits indicate the second data buffer byte size. The buffer size must be a multiple of 2, 4, or 8, depending upon the bus widths—16, 32, and 64 respectively. In the case where the buffer size is not a multiple of 2, 4, or 8, the resulting behavior is undefined. If this field is 0, the DMA ignores this buffer and proceeds to the next buffer in case of a dual-buffer structure. This field is not valid for chain structure; that is, if DES0[4] is set.
12:0	Buffer 1 Size (BS1)	Indicates the data buffer byte size, which must be a multiple of 2, 4, or 8 bytes, depending upon the bus widths—16, 32, and 64, respectively. In the case where the buffer size is not a multiple of 2, 4, or 8, the resulting behavior is undefined. This field should not be zero. Note: If there is only one buffer to be programmed, you need to use only the Buffer 1, and not Buffer 2.

■ The DES2 element contains the address pointer to the data buffer.

Table 17-6 Bits in IDMAC DES2 Element

Bit	Name	Description
31:26	Reserved	
25:13	Buffer 2 Size (BS2)	These bits indicate the second data buffer byte size. The buffer size must be a multiple of 2, 4, or 8, depending upon the bus widths—16, 32, and 64 respectively. In the case where the

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Bit	Name	Description
		buffer size is not a multiple of 2, 4, or 8, the resulting behavior is undefined. If this field is 0, the DMA ignores this buffer and proceeds to the next buffer in case of a dual-buffer structure. This field is not valid for chain structure; that is, if DES0[4] is set.
12:0	Buffer 1 Size (BS1)	Indicates the data buffer byte size, which must be a multiple of 2, 4, or 8 bytes, depending upon the bus widths—16, 32, and 64, respectively. In the case where the buffer size is not a multiple of 2, 4, or 8, the resulting behavior is undefined. This field should not be zero. Note: If there is only one buffer to be programmed, you need to use only the Buffer 1, and not Buffer 2.

- The DES3 element contains the address pointer to the next descriptor if the present descriptor is not the last descriptor in a chained descriptor structure or the second buffer address for a dual-buffer structure.

Table 17-7 Bits in IDMAC DES3 Element

Bit	Name	Description
31:0	Buffer Address Pointer 2/ Next Descriptor Address (BAP2)	These bits indicate the physical address of the second buffer when the dual-buffer structure is used. If the Second Address Chained (DES0[4]) bit is set, then this address contains the pointer to the physical memory where the Next Descriptor is present. If this is not the last descriptor, then the Next Descriptor address pointer must be bus-width aligned.

17.3.3.3 Initialization

IDMAC initialization occurs as follows:

1) Write to IDMAC Bus Mode Register—SDMMC_BMOD to set Host bus access parameters.
2) Write to IDMAC Interrupt Enable Register—SDMMC_IDINTEN to mask unnecessary interrupt causes.
3) The software driver creates either the Transmit or the Receive descriptor list. Then it writes to IDMAC Descriptor List Base Address Register (SDMMC_DBADDR), providing the IDMAC with the starting address of the list.
4) The IDMAC engine attempts to acquire descriptors from the descriptor lists.

- Host Bus Burst Access

The IDMAC attempts to execute fixed-length burst transfers on the AHB Master interface if configured using the FB bit of the IDMAC Bus Mode register. The maximum burst length is indicated and limited by the PBL field. The descriptors are always accessed in the maximum possible burst-size for the 16-bytes to be read— 16*8/bus-width.

The IDMAC initiates a data transfer only when sufficient space to accommodate the configured burst is available in the FIFO or the number of bytes to the end of data, when less than the configured burst-length.

The IDMAC indicates the start address and the number of transfers required to the AHB Master Interface. When the AHB Interface is configured for fixed-length bursts, then it transfers data using the best combination of INCR4/8/16 and SINGLE transactions. Otherwise, in no fixed-length bursts, it transfers data using INCR (undefined length) and SINGLE transactions.

- Host Data Buffer Alignment

The Transmit and Receive data buffers in host memory must be aligned, depending on the data width.

- Buffer Size Calculations

The driver knows the amount of data to transmit or receive. For transmitting to the card, the IDMAC transfers the exact number of bytes to the FIFO, indicated by the buffer size field of DES1.

If a descriptor is not marked as last-LS bit of DES0-then the corresponding buffer(s) of the descriptor are full, and the amount of valid data in a buffer is accurately indicated by its buffer size field. If a descriptor is marked as last, then the buffer cannot be full, as

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indicated by the buffer size in DES1. The driver is aware of the number of locations that are valid in this case.

- Transmission

IDMAC transmission occurs as follows:

1) The Host sets up the elements (DES0-DES3) for transmission and sets the OWN bit (DES0[31]). The Host also prepares the data buffer.
2) The Host programs the write data command in the SDMMC_CMD register in BIU.
3) The Host will also program the required transmit threshold level (TX_WMark field in SDMMC_FIFOTH register).
4) The IDMAC determines that a write data transfer needs to be done as a consequence of step 2.
5) The IDMAC engine fetches the descriptor and checks the OWN bit. If the OWN bit is not set, it means that the host owns the descriptor. In this case the IDMAC enters suspend state and asserts the Descriptor Unable interrupt in the SDMMC_IDSTS register. In such a case, the host needs to release the IDMAC by writing any value to the poll demand register.
6) It will then wait for Command Done (CD) bit and no errors from BIU which indicates that a transfer can be done.
7) The IDMAC engine will now wait for a DMA interface request from BIU. This request will be generated based on the programmed transmit threshold value. For the last bytes of data which can't be accessed using a burst, SINGLE transfers are performed on AHB Master Interface.
8) The IDMAC fetches the Transmit data from the data buffer in the Host memory and transfers to the FIFO for transmission to card.
9) When data spans across multiple descriptors, the IDMAC will fetch the next descriptor and continue with its operation with the next descriptor. The Last Descriptor bit in the descriptor indicates whether the data spans multiple descriptors or not.
10) When data transmission is complete, status information is updated in SDMMC_IDSTS register by setting Transmit Interrupt, if enabled. Also, the OWN bit is cleared by the IDMAC by performing a write transaction to DES0.

- Reception

IDMAC reception occurs as follows:

1) The Host sets up the element (DES0-DES3) for reception, sets the OWN (DES0[31]).
2) The Host programs the read data command in the SDMMC_CMD register in BIU.
3) The Host will program the required receive threshold level (RX_WMark field in FIFOTH register).
4) The IDMAC determines that a read data transfer needs to be done as a consequence of step 2.
5) The IDMAC engine fetches the descriptor and checks the OWN bit. If the OWN bit is not set, it means that the host owns the descriptor. In this case the DMA enters suspend state and asserts the Descriptor Unable interrupt in the SDMMC_IDSTS register. In such a case, the host needs to release the IDMAC by writing any value to the poll demand register.
6) It will then wait for Command Done (CD) bit and no errors from BIU which indicates that a transfer can be done.
7) The IDMAC engine will now wait for a DMA interface request from BIU. This request will be generated based on the programmed receive threshold value. For the last bytes of data which can't be accessed using a burst, SINGLE transfers are performed on AHB.
8) The IDMAC fetches the data from the FIFO and transfer to Host memory.
9) When data spans across multiple descriptors, the IDMAC will fetch the next descriptor and continue with its operation with the next descriptor. The Last Descriptor bit in the descriptor indicates whether the data spans multiple descriptors or not.
10) When data reception is complete, status information is updated in SDMMC_IDSTS register by setting Receive Interrupt, if enabled. Also, the OWN bit is cleared by the IDMAC by performing a write transaction to DES0.

- Interrupts

Interrupts can be generated as a result of various events. SDMMC_IDSTS register contains

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all the bits that might cause an interrupt. SDMMC_IDINTEN register contains an Enable bit for each of the events that can cause an interrupt.
There are two groups of summary interrupts-Normal and Abnormal-as outlined in SDMMC_IDSTS register. Interrupts are cleared by writing a 1 to the corresponding bit position. When all the enabled interrupts within a group are cleared, the corresponding summary bit is cleared. When both the summary bits are cleared, the interrupt signal dmac_intr_o is de-asserted.
Interrupts are not queued and if the interrupt event occurs before the driver has responded to it, no additional interrupts are generated. For example, Receive Interrupt—SDMMC_IDSTS[1] indicates that one or more data was transferred to the Host buffer.
An interrupt is generated only once for simultaneous, multiple events. The driver must scan SDMMC_IDSTS register for the interrupt cause.

17.3.3.4 Variable Delay/Clock Generation Unit

Variable delay mechanism for the cclk_in_drv is useful in order to meet a range of hold-time requirements across modes. Variable delay mechanism for the cclk_in_sample is mandatory and is required to achieve the correct sampling point for data.
The Clock Generation Unit (CLKGEN) includes Phase Shift Unit and Delay Line Unit.
The Phase Shift Unit can shift cclk_in_sample/cclk_in_drv by 0/90/180/270-degree relative to cclk_in. The Delay Line Unit can shift cclk_in_sample/cclk_in_drv step by step in the unit of delay element. The delay value range is 21ps~48ps for every delay element; the max delay element number is 128.
The architecture is as follows.

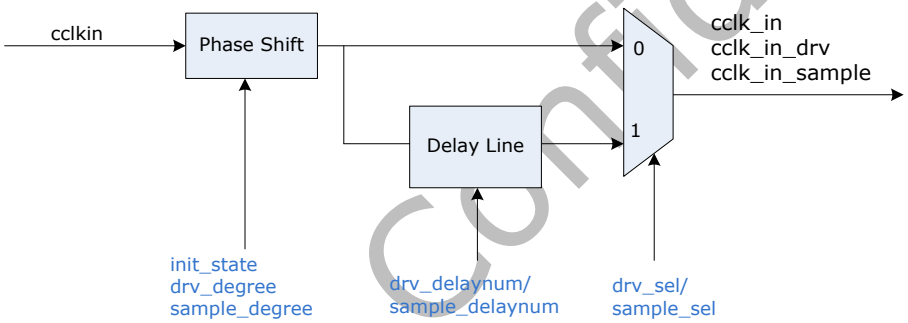


Fig.17-9 Clock Generation Unit

17.4 Register Description

17.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
SDMMC0_BASE	0xFF880000
SDMMC1_BASE	0xFF890000

17.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SDMMC_CTRL	0x0000	W	0x00000000	Control register
SDMMC_PWREN	0x0004	W	0x00000000	Power enable register
SDMMC_CLKDIV	0x0008	W	0x00000000	Clock divider register
SDMMC_CLKSRC	0x000C	W	0x00000000	SD clock source register
SDMMC_CLKENA	0x0010	W	0x00000000	Clock enable register
SDMMC_TMOUT	0x0014	W	0xFFFFFF40	Timeout register
SDMMC_CTYPE	0x0018	W	0x00000000	Card type register
SDMMC_BLKSIZ	0x001C	W	0x00000200	Block size register
SDMMC_BYTCNT	0x0020	W	0x00000200	Byte count register
SDMMC_INTMASK	0x0024	W	0x00000000	Interrupt mask register
SDMMC_CMDARG	0x0028	W	0x00000000	Command argument register

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Name	Offset	Size	Reset Value	Description
SDMMC_CMD	0x002C	W	0x20000000	Command register
SDMMC_RESP0	0x0030	W	0x00000000	Response register 0
SDMMC_RESP1	0x0034	W	0x00000000	Response register 1
SDMMC_RESP2	0x0038	W	0x00000000	Response register 2
SDMMC_RESP3	0x003C	W	0x00000000	Response register 3
SDMMC_MINTSTS	0x0040	W	0x00000000	Masked interrupt status register
SDMMC_RINTSTS	0x0044	W	0x00000000	Raw interrupt status register
SDMMC_STATUS	0x0048	W	0x00000106	Status register
SDMMC_FIFOTH	0x004C	W	0x00FF0000	FIFO threshold register
SDMMC_CDETECT	0x0050	W	0x00000001	Card detect register
SDMMC_WRTPRT	0x0054	W	0x00000000	Write protect register
SDMMC_TCBCNT	0x005C	W	0x00000000	Transferred card byte count register
SDMMC_TBBCNT	0x0060	W	0x00000000	Transferred host to FIFO byte count register
SDMMC_DEBNCE	0x0064	W	0x00FFFFFF	Debounce count register
SDMMC_USRID	0x0068	W	0x00000000	User ID register
SDMMC_VERID	0x006C	W	0x5342270A	Version ID register
SDMMC_HCON	0x0070	W	0x04C434C1	Hardware configuration register
SDMMC_UHSREG	0x0074	W	0x00000000	UHS-1 control register
SDMMC_RSTN	0x0078	W	0x00000001	Hardware reset register
SDMMC_BMOD	0x0080	W	0x00000000	Bus mode register
SDMMC_PLDMND	0x0084	W	0x00000000	Poll demand register
SDMMC_DBADDR	0x0088	W	0x00000000	Descriptor list base address register
SDMMC_IDSTS	0x008C	W	0x00000000	Internal DMAC status register
SDMMC_IDINTEN	0x0090	W	0x00000000	Internal DMAC interrupt enable register
SDMMC_DSCADDR	0x0094	W	0x00000000	Current host descriptor address register
SDMMC_BUFADDR	0x0098	W	0x00000000	Current buffer descriptor address register
SDMMC_CARDTHRCTL	0x0100	W	0x00000000	Card threshold control register
SDMMC_BACKEND_POWER	0x0104	W	0x00000000	Back-end power register
SDMMC_EMMCDDR_REG	0x010C	W	0x00000000	eMMC4.5 DDR start bit detection control register
SDMMC_RDYINT_GEN	0x0120	W	0x00FF0000	Card ready interrupt generation control register
SDMMC_FIFO_BASE	0x0200	W	0x00000000	FIFO base address register

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

17.4.3 Detail Register Description

SDMMC_CTRL

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RW	0x0	use_internal_dmac Present only for the Internal DMAC configuration; else, it is reserved. 1'b0: The host performs data transfers through the slave interface 1'b1: Internal DMAC used for data transfer

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Bit	Attr	Reset Value	Description
24:12	RO	0x0000	reserved
11	RW	0x0	ceata_device_interrupt_status 1'b0: Interrupts not enabled in CE-ATA device 1'b1: Interrupts are enabled in CE-ATA device Software should appropriately write to this bit after power-on reset or any other reset to CE-ATA device. After reset, usually CE-ATA device interrupt is disabled. If the host enables CE-ATA device interrupt, then software should set this bit.
10	RW	0x0	send_auto_stop_ccsd 1'b0: Clear bit if Host Controller does not reset the bit 1'b1: Send internally generated STOP after sending CCSD to CE-ATA device NOTE: Always set send_auto_stop_ccsd and send_ccsd bits together send_auto_stop_ccsd should not be set independent of send_ccsd. When set, the Host Controller automatically sends internally-generated STOP command (CMD12) to CE-ATA device. After sending internally-generated STOP command, Auto Command Done (ACD) bit in SDMMC_RINTSTS is set and generates interrupt to host if Auto Command Done interrupt is not masked. After sending the CCSD, the Host Controller automatically clears send_auto_stop_ccsd bit.
9	RW	0x0	send_ccsd 1'b0: Clear bit if Host Controller does not reset the bit 1'b1: Send Command Completion Signal Disable (CCSD) to CE-ATA device When set, the Host Controller sends CCSD to CE-ATA device. Software sets this bit only if current command is expecting CCS (that is, RW_BLK) and interrupts are enabled in CE-ATA device. Once the CCSD pattern is sent to device, the Host Controller automatically clears send_ccsd bit. It also sets Command Done (CD) bit in SDMMC_RINTSTS register and generates interrupt to host if Command Done interrupt is not masked. NOTE: Once send_ccsd bit is set, it takes two card clock cycles to drive the CCSD on the CMD line. Due to this, during the boundary conditions it may happen that CCSD is sent to the CE-ATA device, even if the device signalled CCS.
8	RW	0x0	abort_read_data 1'b0: No change 1'b1: After suspend command is issued during read-transfer, software polls card to find when suspend happened. Once suspend occurs, software sets bit to reset data state-machine, which is waiting for next block of data. Bit automatically clears once data state machine resets to idle. Used in SDIO card suspend sequence.
7	RW	0x0	send_irq_response 1'b0: No change 1'b1: Send auto IRQ response Bit automatically clears once response is sent. To wait for MMC card interrupts, software issues CMD40, and the Host Controller waits for interrupt response from MMC card. In meantime, if software wants the Controller to exit waiting for interrupt state, it can set this bit, at which time the Host Controller command state-machine sends CMD40 response on bus and returns to idle state.

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Bit	Attr	Reset Value	Description
6	RW	0x0	read_wait 1'b0: Clear read wait 1'b1: Assert read wait For sending read-wait to SDIO cards.
5	RW	0x0	dma_enable 1'b0: Disable DMA transfer mode 1'b1: Enable DMA transfer mode Even when DMA mode is enabled, host can still push/pop data into or from FIFO; this should not happen during the normal operation. If there is simultaneous FIFO access from host/DMA, the data coherency is lost. Also, there is no arbitration inside the controller to prioritize simultaneous host/DMA access.
4	RW	0x0	int_enable Global interrupt enable/disable bit 1'b0: Disable interrupts 1'b1: Enable interrupts The int port is 1 only when this bit is 1 and one or more unmasked interrupts are set.
3	RO	0x0	reserved
2	W1C	0x0	dma_reset 1'b0: No change 1'b1: Reset internal DMA interface control logic To reset DMA interface, firmware should set bit to 1. This bit is auto-cleared after two AHB clocks.
1	W1C	0x0	fifo_reset 1'b0: No change 1'b1: Reset to data FIFO to reset FIFO pointers To reset FIFO, firmware should set bit to 1. This bit is auto-cleared after completion of reset operation.
0	W1C	0x0	controller_reset 1'b0: No change 1'b1: Reset Host Controller To reset Host Controller, firmware should set bit to 1. This bit is auto-cleared after two AHB and two cclk_in clock cycles. This resets: a. BIU/CIU interface b. CIU and state machines c. abort_read_data, send_irq_response, and read_wait bits of SDMMC_CTRL register d. start_cmd bit of SDMMC_CMD register Does not affect any registers or DMA interface, or FIFO or controller interrupts.

SDMMC_PWREN

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	power_enable Power on/off switch for the card. Once power is turned on, firmware should wait for regulator/switch ramp-up time before trying to initialize card. 1'b0: Power off 1'b1: Power on Bit values output to card_power_en port.

SDMMC_CLKDIV

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Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	clk_divider0 Clock divider-0 value. Clock division is 2*n. For example, value of 0 means divide by 2*0 = 0 (no division, bypass), value of 1 means divide by 2*1 = 2, and so on. The recommended value is 0 or 1.

SDMMC_CLKSRC

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	clk_source Clock divider source. 2'b00: Clock divider 0 The cclk_out is always from clock divider 0, and this register is not implemented.

SDMMC_CLKENA

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	cclk_low_power Low-power control for SD card clock and MMC card clock supported. 1'b0: Non-low-power mode 1'b1: Low-power mode. Stop clock when card in IDLE (should be normally set to only MMC and SD memory cards; for SDIO cards, if interrupts must be detected, clock should not be stopped).
15:1	RO	0x0000	reserved
0	RW	0x0	cclk_enable Clock-enable control for SD card clock and MMC card clock supported. 1'b0: Clock disabled 1'b1: Clock enabled

SDMMC_TMOUT

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:8	RW	0xffffff	data_timeout Value for card data read timeout; same value also used for data starvation by host timeout. Value is in number of card output clock. Note: The software timer should be used if the timeout value is in the order of 100 ms. In this case, read data timeout interrupt needs to be disabled.
7:0	RW	0x40	response_timeout Response timeout value. Value is in number of card output clock cclk_out.

SDMMC_CTYPE

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
16	RW	0x0	card_width_8 Indicates if card is 8-bit. 1'b0: Non 8-bit mode 1'b1: 8-bit mode
15:1	RO	0x0000	reserved
0	RW	0x0	card_width Indicates if card is 1-bit or 4-bit. 1'b0: 1-bit mode 1'b1: 4-bit mode

SDMMC_BLKSIZ

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0200	block_size Block size

SDMMC_BYTCNT

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000200	byte_count Number of bytes to be transferred; should be integer multiple of block size for block transfers. For undefined number of byte transfers, byte count should be set to 0. When byte count is set to 0, it is responsibility of host to explicitly send stop/abort command to terminate data transfer.

SDMMC_INTMASK

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	sdio_int_mask 1'b0: SDIO interrupt not masked 1'b1: SDIO interrupt masked
23:17	RO	0x00	reserved
16	RW	0x0	data_nobusy_int_mask 1'b0: Data no busy interrupt not masked 1'b1: Data no busy interrupt masked

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	int_mask Bits used to mask unwanted interrupts. Value of 0 masks interrupt; value of 1 enables interrupt. bit 15: End-bit error (read)/Write no CRC (EBE) bit 14: Auto command done (ACD) bit 13: Start-bit error (SBE) bit 12: Hardware locked write error (HLE) bit 11: FIFO underrun/overrun error (FRUN) bit 10: Data starvation-by-host timeout (HTO) /Volt_switch_int bit 9: Data read timeout (DRTO) bit 8: Response timeout (RTO) bit 7: Data CRC error (DCRC) bit 6: Response CRC error (RCRC) bit 5: Receive FIFO data request (RXDR) bit 4: Transmit FIFO data request (TXDR) bit 3: Data transfer over (DTO) bit 2: Command done (CD) bit 1: Response error (RE) bit 0: Card detect (CD)

SDMMC_CMDARG

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cmd_arg Value indicates command argument to be passed to card

SDMMC_CMD

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31	RW	0x0	start_cmd Start command. Once command is taken by CIU, bit is cleared. When bit is set, host should not attempt to write to any command registers. If write is attempted, hardware lock error is set in raw interrupt register. Once command is sent and response is received from SD/MMC cards, Command Done bit is set in raw interrupt register.
30	RO	0x0	reserved
29	RW	0x1	use_hold_reg Use hold register. 1'b0: CMD and DATA sent to card bypassing hold register 1'b1: CMD and DATA sent to card through the hold register
28	RW	0x0	volt_switch Voltage switch bit. 1'b0: No voltage switching 1'b1: Voltage switching enabled; must be set for CMD11 only.
27	RW	0x0	boot_mode Boot mode selection. 1'b0: Mandatory boot operation 1'b1: Alternate boot operation
26	RW	0x0	disable_boot Disable boot. When software sets this bit along with start_cmd, CIU terminates the boot operation. Do not set disable_boot and enable_boot together.

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Bit	Attr	Reset Value	Description
25	RW	0x0	expect_boot_ack Expect boot acknowledge. When software sets this bit along with enable_boot, CIU expects a boot acknowledge start pattern of 0-1-0 from the selected card.
24	RW	0x0	enable_boot Enable boot. This bit should be set only for mandatory boot mode. When Software sets this bit along with start_cmd, CIU starts the boot sequence for the corresponding card by asserting the CMD line low. Do not set disable_boot and enable_boot together.
23	RW	0x0	ccs_expected 1'b0: Interrupts are not enabled in CE-ATA device or command does not expect CCS from device 1'b1: Interrupts are enabled in CE-ATA device and RW_BLK command expects command completion signal from CE-ATA device If the command expects command completion signal (CCS) from the CE-ATA device, the software should set this control bit. The Host Controller sets data transfer over (DTO) bit in SDMMC_RINTSTS register and generates interrupt to host if data transfer over interrupt is not masked.
22	RW	0x0	read_ceata_device 1'b0: Host is not performing read access towards CE-ATA device 1'b1: Host is performing read access towards CE-ATA device Software should set this bit to indicate that CE-ATA device is being accessed for read transfer. This bit is used to disable read data timeout indication while performing CE-ATA read transfers. Maximum value of I/O transmission delay can be no less than 10 seconds. The Host Controller should not indicate read data timeout while waiting for data from CE-ATA device.
21	RW	0x0	update_clock_regs_only 1'b0: Normal command sequence 1'b1: Do not send commands, just update clock register value into card clock domain. Following register values transferred into card clock domain: SDMMC_CLKDIV, SDMMC_CLRSRC, SDMMC_CLKENA. Changes card clocks (change frequency, truncate off or on, and set low-frequency mode); provided in order to change clock frequency or stop clock without having to send command to cards. During normal command sequence, when update_clock_regs_only = 0, following control registers are transferred from BIU to CIU: SDMMC_CMD, SDMMC_CMDARG, SDMMC_TMOUT, SDMMC_CTYPE, SDMMC_BLKSIZ, SDMMC_BYTCNT. CIU uses new register values for new command sequence to card. When bit is set, there are no Command Done interrupts because no command is sent to SD_MMC_CEATA cards.
20:16	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
15	RW	0x0	send_initialization 1'b0: Do not send initialization sequence (80 clocks of 1) before sending this command 1'b1: Send initialization sequence before sending this command After power on, 80 clocks must be sent to card for initialization before sending any commands to card. Bit should be set while sending first command to card so that controller will initialize clocks before sending command to card. This bit should not be set for either of the boot modes (alternate or mandatory).
14	RW	0x0	stop_abort_cmd 1'b0: Neither stop nor abort command to stop current data transfer in progress. If abort is sent to function-number currently selected or not in data-transfer mode, then bit should be set to 0. 1'b1: Stop or abort command intended to stop current data transfer in progress. When open-ended or predefined data transfer is in progress, and host issues stop or abort command to stop data transfer, bit should be set so that command/data state-machines of CIU can return correctly to idle state. This is also applicable for Boot mode transfers. To Abort boot mode, this bit should be set along with SDMMC_CMD[26]=disable_boot.
13	RW	0x0	wait_prvdata_complete 1'b0: Send command at once, even if previous data transfer has not completed 1'b1: Wait for previous data transfer completion before sending command The wait_prvdata_complete=0 option typically used to query status of card during data transfer or to stop current data transfer; card_number should be same as in previous command.
12	RW	0x0	send_auto_stop 1'b0: No stop command sent at end of data transfer 1'b1: Send stop command at end of data transfer When set, the Host Controller sends stop command to card at end of data transfer. a. When send_auto_stop bit should be set, since some data transfers do not need explicit stop commands b. Open-ended transfers that software should explicitly send to stop command Additionally, when "resume" is sent to resume-suspended memory access of SD-Combo card, bit should be set correctly if suspended data transfer needs send_auto_stop. Don't care if no data expected from card.
11	RW	0x0	transfer_mode 1'b0: Block data transfer command 1'b1: Stream data transfer command Don't care if no data expected.
10	RW	0x0	wr 1'b0: Read from card 1'b1: Write to card Don't care if no data expected from card.
9	RW	0x0	data_expected 1'b0: No data transfer expected (read/write) 1'b1: Data transfer expected (read/write)

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Bit	Attr	Reset Value	Description
8	RW	0x0	check_response_crc 1'b0: Do not check response CRC 1'b1: Check response CRC Some of command responses do not return valid CRC bits. Software should disable CRC checks for those commands in order to disable CRC checking by controller.
7	RW	0x0	response_length 1'b0: Short response expected from card 1'b1: Long response expected from card
6	RW	0x0	response_expect 1'b0: No response expected from card 1'b1: Response expected from card
5:0	RW	0x00	cmd_index Command index

SDMMC_RESP0

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	response0 Bit[31:0] of response

SDMMC_RESP1

Address: **Operational Base** + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	response1 Register represents bit[63:32] of long response. When CIU sends auto-stop command, then response is saved in register. Response for previous command sent by host is still preserved in response 0 register. Additional auto-stop issued only for data transfer commands, and response type is always "short" for them.

SDMMC_RESP2

Address: **Operational Base** + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	response2 Bit[95:64] of long response

SDMMC_RESP3

Address: **Operational Base** + offset (0x003C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	response3 Bit[127:96] of long response

SDMMC_MINTSTS

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RO	0x0	sdio_interrupt SDIO interrupt status when sdio_int_mask is set
23:17	RO	0x00	reserved
16	RW	0x0	data_nobusy_int_status Data no busy interrupt status when data_nobusy_int_mask is set

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Bit	Attr	Reset Value	Description
15:0	RO	0x0000	int_status Interrupt enabled only if corresponding bit in interrupt mask register is set. bit 15: End-bit error (read)/Write no CRC (EBE) bit 14: Auto command done (ACD) bit 13: Start-bit error (SBE) bit 12: Hardware locked write error (HLE) bit 11: FIFO underrun/overrun error (FRUN) bit 10: Data starvation-by-host timeout (HTO) /Volt_switch_int bit 9: Data read timeout (DRTO) bit 8: Response timeout (RTO) bit 7: Data CRC error (DCRC) bit 6: Response CRC error (RCRC) bit 5: Receive FIFO data request (RXDR) bit 4: Transmit FIFO data request (TXDR) bit 3: Data transfer over (DTO) bit 2: Command done (CD) bit 1: Response error (RE) bit 0: Card detect (CD)

SDMMC_RINTSTS

Address: **Operational Base** + offset (0x0044)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	R/WSC	0x0	sdio_interrupt Raw SDIO interrupt status. Write value of 1 clears this bit, and value of 0 leaves bit intact.
23:17	RO	0x00	reserved
16	R/WSC	0x0	data_nobusy_int_status Raw data no busy interrupt status. Write value of 1 clears this bit, and value of 0 leaves bit intact.
15:0	R/WSC	0x0000	int_status Raw interrupt status. Writes to bits clear status bit. Write value of 1 clears status bit, and value of 0 leaves bit intact. bit 15: End-bit error (read)/Write no CRC (EBE) bit 14: Auto command done (ACD) bit 13: Start-bit error (SBE) bit 12: Hardware locked write error (HLE) bit 11: FIFO underrun/overrun error (FRUN) bit 10: Data starvation-by-host timeout (HTO) /Volt_switch_int bit 9: Data read timeout (DRTO) bit 8: Response timeout (RTO) bit 7: Data CRC error (DCRC) bit 6: Response CRC error (RCRC) bit 5: Receive FIFO data request (RXDR) bit 4: Transmit FIFO data request (TXDR) bit 3: Data transfer over (DTO) bit 2: Command done (CD) bit 1: Response error (RE) bit 0: Card detect (CD)

SDMMC_STATUS

Address: **Operational Base** + offset (0x0048)

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Bit	Attr	Reset Value	Description
31	RO	0x0	dma_req DMA request signal state
30	RO	0x0	dma_ack DMA acknowledge signal state
29:17	RO	0x0000	fifo_count Number of filled locations in FIFO
16:11	RO	0x00	response_index Index of previous response, including any auto-stop sent by core.
10	RO	0x0	data_state_mc_busy Data transmit or receive state-machine is busy
9	RO	0x0	data_busy Inverted version of raw selected card_data[0]. 1'b0: Card data not busy 1'b1: Card data busy
8	RO	0x1	data_3_status Raw selected card_data[3]; checks whether card is present. 1'b0: Card not present 1'b1: Card present
7:4	RO	0x0	command_fsm_states Command FSM states: 4'h0: Idle 4'h1: Send init sequence 4'h2: Tx cmd start bit 4'h3: Tx cmd tx bit 4'h4: Tx cmd index + arg 4'h5: Tx cmd crc7 4'h6: Tx cmd end bit 4'h7: Tx resp start bit 4'h8: Rx resp IRQ response 4'h9: Rx resp tx bit 4'ha: Rx resp cmd idx 4'hb: Rx resp data 4'hc: Rx resp crc7 4'hd: Rx resp end bit 4'he: Cmd path wait NCC 4'hf: Wait; CMD-to-response turnaround The command FSM state is represented using 19 bits. The SDMMC_STATUS register[7:4] has 4 bits to represent the command FSM states. Using these 4 bits, only 16 states can be represented. Thus three states cannot be represented in the SDMMC_STATUS[7:4] register. The three states that are not represented in the SDMMC_STATUS register[7:4] are: Bit 16: Wait for CCS Bit 17: Send CCSD Bit 18: Boot Mode Due to this, while command FSM is in "Wait for CCS state" or "Send CCSD" or "Boot Mode", the SDMMC_STATUS register indicates status as 0 for the bit field [7:4].
3	RO	0x0	fifo_full FIFO is full status
2	RO	0x1	fifo_empty FIFO is empty status
1	RO	0x1	fifo_tx_watermark FIFO reached Transmit watermark level; not qualified with data transfer.

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Bit	Attr	Reset Value	Description
0	RO	0x0	fifo_rx_watermark FIFO reached Receive watermark level; not qualified with data transfer.

SDMMC_FIFOTH

Address: **Operational Base** + offset (0x004C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RW	0x0	dma_mutiple_transaction_size Burst size of multiple transaction; should be programmed same as DMA controller multiple-transaction-size SRC/DEST_MSIZE. 3'b000: 1 transfers 3'b001: 4 transfers 3'b010: 8 transfers 3'b011: 16 transfers 3'b100: 32 transfers 3'b101: 64 transfers 3'b110: 128 transfers 3'b111: 256 transfers The unit for transfer is 32bits.
27:16	RW	0x0ff	rx_wmark FIFO threshold watermark level when receiving data to card. When FIFO data count reaches greater than this number, DMA/FIFO request is raised. During end of packet, request is generated regardless of threshold programming in order to complete any remaining data. In non-DMA mode, when receiver FIFO threshold (RXDR) interrupt is enabled, then interrupt is generated instead of DMA request. During end of packet, interrupt is not generated if threshold programming is larger than any remaining data. It is responsibility of host to read remaining bytes on seeing Data Transfer Done interrupt. In DMA mode, at end of packet, even if remaining bytes are less than threshold, DMA request does single transfers to flush out any remaining bytes before Data Transfer Done interrupt is set. 12 bits-1 bit less than FIFO-count of status register, which is 13 bits. Limitation: rx_wmark <= FIFO_DEPTH-2 Recommended: (FIFO_DEPTH/2) - 1; (means greater than (FIFO_DEPTH/2) - 1) NOTE: In DMA mode during CCS time-out, the DMA does not generate the request at the end of packet, even if remaining bytes are less than threshold. In this case, there will be some data left in the FIFO. It is the responsibility of the application to reset the FIFO after the CCS timeout.
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x000	tx_wmark FIFO threshold watermark level when transmitting data to card. When FIFO data count is less than or equal to this number, DMA/FIFO request is raised. If Interrupt is enabled, then interrupt occurs. During end of packet, request or interrupt is generated, regardless of threshold programming. In non-DMA mode, when transmit FIFO threshold (TXDR) interrupt is enabled, then interrupt is generated instead of DMA request. During end of packet, on last interrupt, host is responsible for filling FIFO with only required remaining bytes (not before FIFO is full or after CIU completes data transfers, because FIFO may not be empty). In DMA mode, at end of packet, if last transfer is less than burst size, DMA controller does single cycles until required bytes are transferred. 12 bits -1 bit less than FIFO-count of status register, which is 13 bits. Limitation: tx_wmark >= 1; Recommended: FIFO_DEPTH/2; (means less than or equal to FIFO_DEPTH/2)

SDMMC_CDETECT

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x1	card_detect_n Value on card_detect_n input port. 1'b0: Represents presence of card 1'b1: Represents absence of card

SDMMC_WRTPRT

Address: **Operational Base** + offset (0x0054)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	write_protect Value on card_write_prt input port. 1 represents write protection.

SDMMC_TCBCNT

Address: **Operational Base** + offset (0x005C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	trans_card_byte_count Number of bytes transferred by CIU unit to card

SDMMC_TBBCNT

Address: **Operational Base** + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	trans_fifo_byte_count Number of bytes transferred between host/DMA memory and BIU FIFO

SDMMC_DEBNCE

Address: **Operational Base** + offset (0x0064)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
23:0	RW	0xffffff	debounce_count Number of host clock used by debounce filter logic; typical debounce time is 5-25 ms.

SDMMC_USRID

Address: **Operational Base** + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	usrid User identification register

SDMMC_VERID

Address: **Operational Base** + offset (0x006C)

Bit	Attr	Reset Value	Description
31:0	RO	0x5342270a	verid Version identification register

SDMMC_HCON

Address: **Operational Base** + offset (0x0070)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RO	0x1	area_optimized 1'b0: No area optimization 1'b1: Area optimization
25:24	RO	0x0	num_clk_div divider number-1.
23	RO	0x1	set_clk_false_path 1'b0: No false path 1'b1: False path set
22	RO	0x1	impl_hold_reg 1'b0: No hold register 1'b1: Hold register
21	RO	0x0	fifo_ram_inside 1'b0: Outside 1'b1: Inside
20:18	RO	0x1	ge_dma_data_width 3'b000: 16 bits 3'b001: 32 bits 3'b010: 64 bits Others: Reserved
17:16	RO	0x0	dma_interface 2'b00: None 2'b01: INT_DMA 2'b10: GENERIC_DMA 2'b11: NON_INT_DMA
15:10	RO	0x0d	h_addr_width 6'h8: 9 bits 6'h9: 10 bits ..... 6'h1f: 32 bits Others: Reserved
9:7	RO	0x1	h_data_width 3'b000: 16 bits 3'b001: 32 bits 3'b010: 64 bits Others: Reserved

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Bit	Attr	Reset Value	Description
6	RO	0x1	h_bus_type 1'b0: APB 1'b1: AHB
5:1	RO	0x00	card_num Card number -1.
0	RO	0x1	card_type Card type. 1'b0: MMC_ONLY 1'b1: SD_MMC

SDMMC_UHSREG

Address: **Operational Base** + offset (0x0074)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	ddr_reg DDR mode. These bits indicate DDR mode of operation to the core for the data transfer. 1'b0: Non-DDR mode 1'b1: DDR mode
15:0	RO	0x0000	reserved

SDMMC_RSTN

Address: **Operational Base** + offset (0x0078)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x1	card_reset Hardware reset. 1'b0: Active mode 1'b1: Reset These bits cause the cards to enter pre-idle state, which requires them to be re-initialized.

SDMMC_BMOD

Address: **Operational Base** + offset (0x0080)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
10:8	RO	0x0	pbl Programmable burst length. These bits indicate the maximum number of beats to be performed in one IDMAC transaction. The IDMAC will always attempt to burst as specified in PBL each time it starts a Burst transfer on the host bus. The permissible values are 1, 4, 8, 16, 32, 64, 128 and 256. This value is the mirror of MSIZE of SDMMC_FIFOTH register. In order to change this value, write the required value to SDMMC_FIFOTH register. This is an encode value as follows. 3'b000: 1 transfers 3'b001: 4 transfers 3'b010: 8 transfers 3'b011: 16 transfers 3'b100: 32 transfers 3'b101: 64 transfers 3'b110: 128 transfers 3'b111: 256 transfers Transfer unit is 32 bits. PBL is a read-only value and is applicable only for data access; it does not apply to descriptor accesses.
7	RW	0x0	de IDMAC enable. When set, the IDMAC is enabled.
6:2	RW	0x00	dsl Descriptor skip length. Specifies the number of word to skip between two unchained descriptors. This is applicable only for dual buffer structure.
1	RW	0x0	fb Fixed burst. Controls whether the AHB Master interface performs fixed burst transfers or not. When set, the AHB will use only SINGLE, INCR4, INCR8 or INCR16 during start of normal burst transfers. When reset, the AHB will use SINGLE and INCR burst transfer operations.
0	RW	0x0	swr Software reset. When set, the DMA Controller resets all its internal registers. It is automatically cleared after 1 clock cycle.

SDMMC_PLDMND

Address: **Operational Base** + offset (0x0084)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	pd Poll demand. If the OWN bit of a descriptor is not set, the FSM goes to the suspend state. The host needs to write any value into this register for the IDMAC FSM to resume normal descriptor fetch operation.

SDMMC_DBADDR

Address: **Operational Base** + offset (0x0088)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sbl Start of descriptor list. Contains the base address of the first descriptor. The LSB bits[1:0] are ignored and taken as all-zero by the IDMAC internally. Hence these LSB bits are read-only.

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SDMMC_IDSTS

Address: **Operational Base** + offset (0x008C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:13	RO	0x0	fsm DMAC FSM present state. 4'h0: DMA_IDLE 4'h1: DMA_SUSPEND 4'h2: DESC_RD 4'h3: DESC_CHK 4'h4: DMA_RD_REQ_WAI 4'h5: DMA_WR_REQ_WAI 4'h6: DMA_RD 4'h7: DMA_WR 4'h8: DESC_CLOSE Others: Reserved
12:10	RO	0x0	eb Error bits. Indicates the type of error that caused a bus error. Valid only with fatal bus. 3'h1: Host abort received during transmission 3'h2: Host abort received during reception Others: Reserved
9	RW	0x0	ais Abnormal interrupt summary. Logical OR of the following: SDMMC_IDSTS[2] fatal bus interrupt SDMMC_IDSTS[4] du bit interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes ais to be set is cleared. Writing a 1 clears this bit.
8	RW	0x0	nis Normal interrupt summary. Logical OR of the following: SDMMC_IDSTS[0] transmit interrupt SDMMC_IDSTS[1] receive interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes nis to be set is cleared. Writing a 1 clears this bit.
7:6	RO	0x0	reserved
5	RW	0x0	ces Card error summary. Indicates the status of the transaction to/from the card; also present in SDMMC_RINTSTS. Indicates the logical OR of the following bits: EBE: End Bit Error RTO: Response Timeout/Boot Ack Timeout RCRC: Response CRC SBE: Start Bit Error DRTO: Data Read Timeout/BDS timeout DCRC: Data CRC for Receive RE: Response Error Writing a 1 clears this bit. The abort condition of the IDMAC depends on the setting of this CES bit. If the CES bit is enabled, then the IDMAC aborts on a "response error"; however, it will not abort if the CES bit is cleared.

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Bit	Attr	Reset Value	Description
4	RW	0x0	dui Descriptor unavailable interrupt. This bit is set when the descriptor is unavailable due to OWN bit = 0 (DES0[31] =0). Writing a 1 clears this bit.
3	RO	0x0	reserved
2	RW	0x0	fbe Fatal bus error interrupt. Indicates that a bus error occurred (SDMMC_IDSTS[12:10]). When this bit is set, the DMA disables all its bus accesses. Writing a 1 clears this bit.
1	RW	0x0	ri Receive interrupt. Indicates the completion of data reception for a descriptor. Writing a 1 clears this bit.
0	RW	0x0	ti Transmit interrupt. Indicates that data transmission is finished for a descriptor. Writing 1 clears this bit.

SDMMC_IDINTEN

Address: **Operational Base** + offset (0x0090)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	ai Abnormal interrupt summary enable. When set, an abnormal interrupt is enabled. This bit enables the following bits: SDMMC_IDINTEN[2] fatal bus error interrupt SDMMC_IDINTEN[4] du interrupt
8	RW	0x0	ni Normal interrupt summary enable. When set, a normal interrupt is enabled. When reset, a normal interrupt is disabled. This bit enables the following bits: SDMMC_IDINTEN[0] transmit interrupt SDMMC_IDINTEN[1] receive interrupt
7:6	RO	0x0	reserved
5	RW	0x0	ces Card error summary interrupt enable. When set, it enables the card interrupt summary.
4	RW	0x0	du Descriptor unavailable interrupt. When set along with abnormal interrupt summary enable, the du interrupt is enabled.
3	RO	0x0	reserved
2	RW	0x0	fbe Fatal bus error enable. When set with abnormal interrupt summary enable, the fatal bus error interrupt is enabled. When reset, fatal bus error enable interrupt is disabled.
1	RW	0x0	ri Receive interrupt enable. When set with normal interrupt summary enable, receive interrupt is enabled. When reset, receive interrupt is disabled.

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Bit	Attr	Reset Value	Description
0	RW	0x0	ti Transmit interrupt enable. When set with normal interrupt summary enable, transmit interrupt is enabled. When reset, transmit interrupt is disabled.

SDMMC_DSCADDR

Address: **Operational Base** + offset (0x0094)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hda Host descriptor address pointer. This register points to the start address of the current descriptor read by the IDMAC. Cleared on reset. Pointer updated by IDMAC during operation.

SDMMC_BUFADDR

Address: **Operational Base** + offset (0x0098)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hba Host buffer address pointer. This register points to the current data buffer address being accessed by the IDMAC. Cleared on Reset. Pointer updated by IDMAC during operation.

SDMMC_CARDTHRCTL

Address: **Operational Base** + offset (0x0100)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	card_rd_thres Card read threshold size
15:2	RO	0x0000	reserved
1	RW	0x0	busy_clr_int_en Busy clear interrupt. 1'b0: Busy clear interrupt disabled 1'b1: Busy clear interrupt enabled Note: The application can disable this feature if it does not want to wait for a busy clear interrupt. For example, in a multi-card scenario, the application can switch to the other card without waiting for a busy to be completed. In such cases, the application can use the polling method to determine the status of busy. By default this feature is disabled and backward-compatible to the legacy drivers where polling is used.
0	RW	0x0	card_rd_thres_en Card read threshold enable. 1'b0: Card read threshold disabled 1'b1: Card read threshold enabled. The host initiates read transfer only if card_rd_thres amount of space is available in receive FIFO.

SDMMC_BACKEND_POWER

Address: **Operational Base** + offset (0x0104)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	back_end_power Back end power. 1'b0: Off; Reset 1'b1: Back-end power supplied to card application

SDMMC_EMMCDDR_REG

Address: **Operational Base** + offset (0x010C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	half_start_bit Control for start bit detection mechanism inside Host Controller based on duration of start bit. For eMMC 4.5, start bit can be: 1'b0: Full cycle (half_start_bit=0) 1'b1: Less than one full cycle (half_start_bit=1) Set half_start_bit=1 for eMMC 4.5 and above; set to 0 for SD applications.

SDMMC_RDYINT_GEN

Address: **Operational Base** + offset (0x0120)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RO	0x0	rdyint_cnt_finish Counter finish indication. When high, it indicates that the rdyint counter is finished.
23:16	RO	0xff	rdyint_cnt_status Couner status, reflect internal counter value.
15:9	RO	0x00	reserved
8	RW	0x0	rdyint_gen_working Working indication for rdyint generator. When high, Host Controller start to count and generate one rdyint trigger. After the rdyint trigger is generated, this bit will be set to 0 by Host Controller. So software should set it to 1 before detecting next interrupt.
7:0	RW	0x00	rdyint_gen_maxval Max counter value to detect cdata_in0 high value for generating rdyint, based on internal clock frequency.

SDMMC_FIFO_BASE

Address: **Operational Base** + offset (0x0200)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	fifo_base_addr FIFO base address

17.5 Interface Description

17.5.1 SDMMC0 Interface Description

Table 17-8 SDMMC0 Interface Description

Module Pin	Dir.	PAD Name	IOMUX Setting
sdmmc0_cclk	O	SDMMC0_CLK/TEST_CLK_OUT/UART5_TX_M0/SPI1_CLK_M1/CAN1_TX_M0/GPIO1_C0_d	GPIO1_IOC_GPIO1C_IOMUX_SEL_L[3:0]=4'h1
sdmmc0_ccmd	I/O	SDMMC0_CMD/SPDIF_TX_M2/UART5_RX_M0/CAN1_RX_M0/GPIO1_B7_u	GPIO1_IOC_GPIO1B_IOMUX_SEL_H[15:12]=4'h1
sdmmc0_cdata0	I/O	SDMMC0_D0/UART0_RX_M1/UART7_RX_M1/SPI1_MOSI_M1/DSM_AUD_LP/GPIO1_B3_u	GPIO1_IOC_GPIO1B_IOMUX_SEL_L[15:12]=4'h1
sdmmc0_cdata1	I/O	SDMMC0_D1/UART0_TX_M1/UART7_TX_M1/SPI1_MIS	GPIO1_IOC_GPIO1B_IOMUX_SEL_H

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Module Pin	Dir.	PAD Name	IOMUX Setting
		O_M1/DSM_AUD_LN/GPIO1_B4_u	[3:0]=4'h1
sdmmc0_cdata2	I/O	SDMMC0_D2/JTAG_CPU_MCU_TCK_M1/UART5_CTSN_M0/SPI1_CSN1_M1/PWM10_M0/DSM_AUD_RP/GPIO1_B5_u	GPIO1_IOC_GPIO1B_IOMUX_SEL_H [7:4]=4'h1
sdmmc0_cdata3	I/O	SDMMC0_D3/JTAG_CPU_MCU_TMS_M1/UART5_RTSN_M0/SPI1_CSN0_M1/PWM11_M0/DSM_AUD_RN/GPIO1_B6_u	GPIO1_IOC_GPIO1B_IOMUX_SEL_H [11:8]=4'h1
sdmmc0_cdetn	I	SDMMC0_DETN/I2C4_SDA_M1/GPIO0_A4_u	GPIO0_IOC_GPIO0A_IOMUX_SEL_H [3:0]=4'h1
sdmmc0_pwren	O	SDMMC0_PWREN/I2C4_SCL_M1/PMU_DEBUG/GPIO0_A5_d	GPIO0_IOC_GPIO0A_IOMUX_SEL_H [7:4]=4'h1

Notes: I=input, O=output, I/O=input/output, bidirectional

17.5.2 SDMMC1 Interface Description

Table 17-9 SDMMC1 Interface Description

Module Pin	Dir.	PAD Name	IOMUX Setting
sdmmc1_cclk	O	SDMMC1_CLK/RGMII_RXCLK_M1/I2S0_MCLK_M1/PWM1_M1/GPIO1_C6_d	GPIO1_IOC_GPIO1C_IOMUX_SEL_H [11:8]=4'h1
sdmmc1_ccmd	I/O	SDMMC1_CMD/RGMII_RXD3_M1/I2S0_SCLK_M1/PWM0_M1/GPIO1_C5_d	GPIO1_IOC_GPIO1C_IOMUX_SEL_H [7:4]=4'h1
sdmmc1_cdata0	I/O	SDMMC1_D0/RGMII_TXD2_M1/I2S0_SDI0_M1/PWM8_M1/GPIO1_C1_d	GPIO1_IOC_GPIO1C_IOMUX_SEL_L [7:4]=4'h1
sdmmc1_cdata1	I/O	SDMMC1_D1/RGMII_TXD3_M1/I2S0_SDI1_M1/PWM9_M1/GPIO1_C2_d	GPIO1_IOC_GPIO1C_IOMUX_SEL_L [11:8]=4'h1
sdmmc1_cdata2	I/O	SDMMC1_D2/RGMII_TXCLK_M1/I2S0_SDO0_M1/PWM10_M1/GPIO1_C3_d	GPIO1_IOC_GPIO1C_IOMUX_SEL_L [15:12]=4'h1
sdmmc1_cdata3	I/O	SDMMC1_D3/RGMII_RXD2_M1/I2S0_LRCK_M1/PWM11_M1/GPIO1_C4_d	GPIO1_IOC_GPIO1C_IOMUX_SEL_H [3:0]=4'h1
sdmmc1_cdetn	I	SDMMC1_DETN/RGMII_MDIO_M1/PWM3_M1/I2C5_SDA_M1/RMII_MDIO/GPIO1_D0_d	GPIO1_IOC_GPIO1D_IOMUX_SEL_L [3:0]=4'h1
sdmmc1_pwren	O	SDMMC1_PWREN/RGMII_MDC_M1/PWM2_M1/I2C5_SCL_M1/RMII_MDC/GPIO1_C7_d	GPIO1_IOC_GPIO1C_IOMUX_SEL_H [15:12]=4'h1

Notes: I=input, O=output, I/O=input/output, bidirectional

17.6 Application Notes

17.6.1 Software/Hardware Restriction

Before issuing a new data transfer command, the software should ensure that the card is not busy due to any previous data transfer command. Before changing the card clock frequency, the software must ensure that there are no data or command transfers in progress.

To avoid glitches in the card clock outputs, the software should use the following steps when changing the card clock frequency:

1) Before disable the clocks, ensure that the card is not busy due to any previous data command. To determine this, check for 0 in bit9 of SDMMC_STATUS register.
2) Update the Clock Enable register to disable clock. To ensure completion of any previous command before this update, send a command to the CIU to update the clock registers by setting:

- start_cmd bit
- "update clock registers only" bits
- "wait_previous data complete" bit

   Wait for the CIU to take the command by polling for 0 on the start_cmd bit.

3) Set the start_cmd bit to update the Clock Divider and/or Clock Source register, and send a command to the CIU in order to update the clock registers; wait for the CIU to take the command.
4) Set start_cmd to update the Clock Enable register in order to enable the required clocks and send a command to the CIU to update the clock registers; wait for the CIU to take the command.

In non-DMA mode, while reading from a card, the Data Transfer Over (SDMMC_RINTSTS[3]) interrupt occurs as soon as the data transfer from the card is over. There still could be some data left in the FIFO, and the RX_WMark interrupt may or may not occur, depending on the remaining bytes in the FIFO. Software should read any remaining bytes upon seeing the Data Transfer Over (DTO) interrupt. While using the external DMA interface for reading from a card, the DTO interrupt occurs only after all the

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data is flushed to memory by the DMA interface unit.
While writing to a card in external DMA mode, if an undefined-length transfer is selected by setting the Byte Count Register to 0, the DMA logic will likely request more data than it will send to the card, since it has no way of knowing at which point the software will stop the transfer. The DMA request stops as soon as the DTO is set by the CIU.
If the software issues a controller_reset command by setting control register bit[0] to 1, all the CIU state machines are reset; the FIFO is not cleared. The DMA sends all remaining bytes to the host. In addition to a card-reset, if a FIFO reset is also issued, then:

- Any pending DMA transfer on the bus completes correctly
- DMA data read is ignored
- Write data is unknown(x)

Additionally, if dma_reset is also issued, any pending DMA transfer is abruptly terminated. When the DMA is used, the DMA controller channel should also be reset and reprogrammed.
If any of the previous data commands do not properly terminate, then the software should issue the FIFO reset in order to remove any residual data, if any, in the FIFO. After asserting the FIFO reset, you should wait until this bit is cleared.
One data-transfer requirement between the FIFO and host is that the number of transfers should be a multiple of the FIFO data width (32bits). For example, you want to write only 15 bytes to an SD/MMC card (SDMMC_BYTCNT), the host should write 16 bytes to the FIFO or program the DMA to do 16-byte transfers. The software can still program the Byte Count register to only 15, at which point only 15 bytes will be transferred to the card. Similarly, when 15 bytes are read from a card, the host should still read all 16 bytes from the FIFO. It is recommended that you not change the FIFO threshold register in the middle of data transfers.

17.6.2 Programming Sequence

17.6.2.1 Initialization

Following figure illustrates the initialization flow.

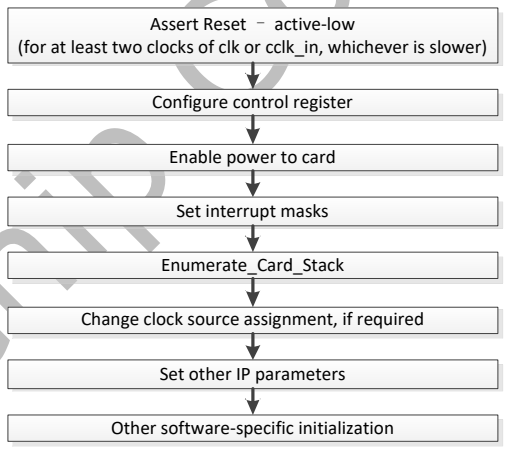


Fig.17-10 Host Controller Initialization Sequence

Once the power and clocks are stable, reset_n should be asserted(active-low) for at least two cycles of clk or cclk_in, whichever is slower. The reset initializes the registers, ports, FIFO-pointers, DMA interface controls, and state-machines in the design. After power-on reset, the software should do the following:

1) Configure control register – For MMC mode, enable the open-drain pullup by setting enable_OD_pullup(bit24) in the SDMMC_CTRL register.
2) Enable power to cards – Before enabling the power, confirm that the voltage setting to the voltage regulators is correct. Enable power to the connected cards by setting the corresponding bit to 1 in the Power Enable register. Wait for the power ramp-up time.
3) Set masks for interrupts by clearing appropriate bits in the Interrupt Mask register. Set the global int_enable bit of the SDMMC_CTRL register. It is recommended that you write 0xffff_ffff to the Raw Interrupt register in order to clear any pending interrupts before setting the int_enable bit.
4) Enumerate card stack – Each card is enumerated according to card type; for details, refer to "Enumerated Card Stack". For enumeration, you should restrict the clock

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frequency to 400KHz.
5) Changing clock source assignment – set the card frequency using the clock-divider and clock-source registers; for details, refer to "Clock Programming". MMC cards operate at a maximum of 20MHz (at maximum of 52MHz in high-speed mode). SD mode operates at a maximum of 25MHz (at maximum of 50MHz in high-speed mode).
6) Set other parameters, which normally do not need to be changed with every command, with a typical value such as timeout values in cclk_out according to SD/MMC specifications.

- ResponseTimeOut = 0x64
- DataTimeOut = highest of one of the following:
- (10*((TAAC*Fop)+(100*NSAC))
- Host FIFO read/write latency from FIFO empty/full
- Set the debounce value to 25ms(default:0x0fffff) in host clock cycle units in the SDMMC_DEBNCE register.

FIFO threshold value in bytes in the SDMMC_FIFOTH register.

17.6.2.2 Enumerated Card Stack

The card stack does the following:

- Enumerates all connected cards
- Sets the RCA for the connected cards
- Reads card-specific information
- Stores card-specific information locally

Enumeration depends on the operating mode of the SD/MMC card; the card type is first identified and the appropriate card enumeration routine is called.

1) Check if the card is connected.
2) Clear the card type register to set the card width as a single bit. For the given card number, clear the corresponding bits in the card_type register. Clear the register bit for a 1-bit, 4-bit bus width. For example, for card number=1, clear bit 0 and bit 16 of the card_type register.
3) Set clock frequency to FOD=400KHz, maximum – Program clock divider0 (bits 0-7 in the SDMMC_CLKDIV register) value to one-half of the cclk_in frequency divided by 400KHz. For example, if cclk_in is 20MHz, then the value is 20, 000/(2*400)=25.
4) Identify the card type; that is, SD, MMC, or SDIO.
   a. Send CMD5 first. If a response is received, then the card is SDIO
   b. If not, send CMD8 with the following Argument
      Bit[31:12] = 20'h0 //reserved bits
      Bit[11:8] = 4'b0001 //VHS value
      Bit[7:0] = 8'b10101010 //Preferred Check Pattern by SD2.0
   c. If Response is received the card supports High Capacity SD2.0 then send ACMD41 with the following Argument
      Bit[31] = 1'b0; //Reserved bits
      Bit[30] = 1'b1; //High Capacity Status
      Bit[29:24] = 6'h0; //Reserved bits
      Bit[23:0] = Supported Voltage Range
   d. If Response is received for ACMD41 then the card is SD. Otherwise the card is MMC.
   e. If response is not received for initial CMD8 then card does not support High Capacity SD2.0, then issue CMD0 followed by ACMD41 with the following Argument
      Bit[31] = 1'b0; //Reserved bits
      Bit[30] = 1'b0; //High Capacity Status
      Bit[29:24] = 6'h0; //Reserved bits
      Bit[23:0] = Supported Voltage Range
5) Enumerate the card according to the card type.
6) Use a clock source with a frequency = Fod (that is, 400KHz) and use the following enumeration command sequence:

- SD card – Send CMD0, CMD8, ACMD41, CMD2, CMD3.
- MMC – Send CMD0, CMD1, CMD2, CMD3.

17.6.2.3 Clock Programming

The Host Controller supports one clock source. The clock to an individual card can be

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enabled or disabled. Registers that support this are:

- SDMMC_CLKDIV – Programs individual clock source frequency. SDMMC_CLKDIV limited to 0 or 1 is recommended.
- SDMMC_CLKSRC – Assign clock source for each card.
- SDMMC_CLKENA – Enables or disables clock for individual card and enables low-power mode, which automatically stops the clock to a card when the card is idle for more than 8 clocks.

The Host Controller loads each of these registers only when the start_cmd bit and the update_clk_regs_only bit in the SDMMC_CMD register are set. When a command is successfully loaded, the Host Controller clears this bit, unless the Host Controller already has another command in the queue, at which point it gives an HLE(Hardware Locked Error). Software should look for the start_cmd and the update_clk_regs_only bits, and should also set the wait_prvdata_complete bit to ensure that clock parameters do not change during data transfer. Note that even though start_cmd is set for updating clock registers, the Host Controller does not raise a command_done signal upon command completion.

The following shows how to program these registers:

1) Confirm that no card is engaged in any transaction; if there is a transaction, wait until it finishes.
2) Stop all clocks by writing 0 to the SDMMC_CLKENA register. Set the start_cmd, Update_clk_regs_only, and wait_prvdata_complete bits in the SDMMC_CMD register. Wait until start_cmd is cleared or an HLE is set; in case of an HLE, repeat the command.
3) Program the SDMMC_CLKDIV and SDMMC_CLKSRC registers, as required. Set the start_cmd, Update_clk_regs_only, and wait_prvdata_complete bits in the SDMMC_CMD register. Wait until start_cmd is cleared or an HLE is set; in case of an HLE, repeat the command.

Re-enable all clocks by programming the SDMMC_CLKENA register. Set the start_cmd, update_clk_regs_only, and wait_prvdata_complete bits in the SDMMC_CMD register. Wait until start_cmd is cleared or an HLE is set; in case of an HLE, repeat the command.

17.6.2.4 No-Data Command With or Without Response Sequence

To send any non-data command, the software needs to program the SDMMC_CMD register @0x2C and the SDMMC_CMDARG register @0x28 with appropriate parameters. Using these two registers, the Host Controller forms the command and sends it to the command bus. The Host Controller reflects the errors in the command response through the error bits of the SDMMC_RINTSTS register.

When a response is received – either erroneous or valid – the Host Controller sets the command_done bit in the SDMMC_RINTSTS register. A short response is copied in Response Register0, while along response is copied to all four response registers @0x30, 0x34, 0x38, and 0x3C. The Response3 register bit 31 represents the MSB, and the Response0 register bit 0 represents the LSB of a long response.

For basic commands or non-data commands, follow these steps:

1) Program the Command register @0x28 with the appropriate command argument parameter.
2) Program the Command register @0x2C with the settings in following table.

Table 17-10 Command Settings for No-Data Command

Parameter	Value	Description
Default		
start_cmd	1	-
use_hold_reg	1	Choose value based on speed mode being used;ref to "use_hold_reg" on SDMMC_CMD register
update_clk_regs_only	0	No clock parameters update command
data_expected	0	No data command
card number	0	Actual card number(one controller only connect one

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Parameter	Value	Description
		card, the num is No. 0)
cmd_index	command-index	-
send_initialization	0	Can be 1, but only for card reset commands, such as CMD0
stop_abort_cmd	0	Can be 1 for commands to stop data transfer, such as CMD12
response_length	0	Can be 1 for R2(long) response
response_expect	1	Can be 0 for commands with no response; for example, CMD0, CMD4, CMD15, and so on
User-selectable		
wait_prvdata_complete	1	Before sending command on command line, host should wait for completion of any data command in process, if any (recommended to always set this bit, unless the current command is to query status or stop data transfer when transfer is in progress)
check_response_crc	1	If host should crosscheck CRC of response received

3) Wait for command acceptance by host. The following happens when the command is loaded into the Host Controller:

- Host Controller accepts the command for execution and clears the start_cmd bit in the SDMMC_CMD register, unless one command is in process, at which point the Host Controller can load and keep the second command in the buffer.
- If the Host Controller is unable to load the command – that is, a command is already in progress, a second command is in the buffer, and a third command is attempted – then it generates an HLE (hardware-locked error).

4) Check if there is an HLE.
5) Wait for command execution to complete. After receiving either a response from a card or response timeout, the Host Controller sets the command_done bit in the SDMMC_RINTSTS register. Software can either poll for this bit or respond to a generated interrupt.
6) Check if response_timeout error, response_CRC error, or response error is set. This can be done either by responding to an interrupt raised by these errors or by polling bits 1, 6, and 8 from the SDMMC_RINTSTS register @0x44. If no response error is received, then the response is valid. If required, the software can copy the response from the response registers @0x30-0x3C.

Software should not modify clock parameters while a command is being executed.

17.6.2.5 Data Transfer Commands

Data transfer commands transfer data between the memory card and the Host Controller. To send a data command, the Host Controller needs a command argument, total data size, and block size. Software can receive or send data through the FIFO.

Before a data transfer command, software should confirm that the card is not busy and is in a transfer state, which can be done using the CMD13 and CMD7 commands, respectively. For the data transfer commands, it is important that the same bus width that is programmed in the card should be set in the card type register @0x18.

The Host Controller generates an interrupt for different conditions during data transfer, which are reflected in the SDMMC_RINTSTS register @0x44 as:

1) Data_Transfer_Over (bit 3) – When data transfer is over or terminated. If there is a

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response timeout error, then the Host Controller does not attempt any data transfer and the "Data Transfer Over" bit is never set.
2) Transmit_FIFO_Data_request (bit 4) – FIFO threshold for transmitting data was reached; software is expected to write data, if available, in FIFO.
3) Receive_FIFO_Data_request (bit 5) – FIFO threshold for receiving data was reached; software is expected to read data from FIFO.
4) Data starvation by Host timeout (bit 10) – FIFO is empty during transmission or is full during reception. Unless software writes data for empty condition or reads data for full condition, the Host Controller cannot continue with data transfer. The clock to the card has been stopped.
5) Data read timeout error (bit 9) – Card has not sent data within the timeout period.
6) Data CRC error (bit 7) – CRC error occurred during data reception.
7) Start bit error (bit 13) – Start bit was not received during data reception.
8) End bit error (bit 15) – End bit was not received during data reception or for a write operation; a CRC error is indicated by the card.

Conditions 6), 7), and 8) indicate that the received data may have errors. If there was a response timeout, then no data transfer occurred.

17.6.2.6 Single-Block or Multiple-Block Read

Steps involved in a single-block or multiple-block read are:

1) Write the data size in bytes in the SDMMC_BYTCNT register @0x20.
2) Write the block size in bytes in the SDMMC_BLKSIZ register @0x1C. The Host Controller expects data from the card in blocks of size SDMMC_BLKSIZ each.
3) Program the SDMMC_CMDARG register @0x28 with the data address of the beginning of a data read.
4) Program the Command register with the parameters listed in following table. For SD and MMC cards, use CMD17 for a single-block read and CMD18 for a multiple-block read. For SDIO cards, use CMD53 for both single-block and multiple-block transfers.

Table 17-11 Command Setting for Single or Multiple-Block Read

Parameter	Value	Description
Default		
start_cmd	1	-
use_hold_reg	1	Choose value based on speed mode being used;ref to "use_hold_reg" on SDMMC_CMD register
update_clk_regs_only	0	No clock parameters update command
card number	0	Actual card number(one controller only connect one card, the num is No.0)
send_initialization	0	Can be 1, but only for card reset commands, such as CMD0
stop_abort_cmd	0	Can be 1 for commands to stop data transfer, such as CMD12
send_auto_stop	0/1	-
transfer_mode	0	Block transfer
read_write	0	Read from card
data_expected	1	Data command
response_length	0	Can be 1 for R2(long) response
response_expect	1	Can be 0 for commands with no response; for example, CMD0, CMD4, CMD15, and so on
User-selectable		

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Parameter	Value	Description
cmd_index	command-index	-
wait_prvdata_complete	1	0: Sends command immediately 1: Sends command after previous data transfer ends
check_response_crc	1	0: Host Controller should not check response CRC 1: Host Controller should check response CRC

After writing to the SDMMC_CMD register, the Host Controller starts executing the command; when the command is sent to the bus, the command_done interrupt is generated.

- Software should look for data error interrupts; that is, bits 7, 9, 13, and 15 of the SDMMC_RINTSTS register. If required, software can terminate the data transfer by sending a STOP command.
- Software should look for Receive_FIFO_Data_request and/or data starvation by host timeout conditions. In both cases, the software should read data from the FIFO and make space in the FIFO for receiving more data.

When a Data_Transfer_Over interrupt is received, the software should read the remaining data from the FIFO.

17.6.2.7 Single-Block or Multiple-Block Write

Steps involved in a single-block or multiple-block write are:

1) Write the data size in bytes in the SDMMC_BYTCNT register @0x20.
2) Write the block size in bytes in the SDMMC_BLKSIZ register @0x1C; the Host Controller sends data in blocks of size SDMMC_BLKSIZ each.
3) Program SDMMC_CMDARG register @0x28 with the data address to which data should be written.
4) Write data in the FIFO; it is usually best to start filling data the full depth of the FIFO.
5) Program the Command register with the parameters listed in following table.

Table 17-12 Command Settings for Single or Multiple-Block Write

Parameter	Value	Description
Default		
start_cmd	1	-
use_hold_reg	1	Choose value based on speed mode being used;ref to “use_hold_reg” on SDMMC_CMD register
update_clk_regs_only	0	No clock parameters update command
card number	0	Actual card number(one controller only connect one card, the num is No. 0)
send_initialization	0	Can be 1, but only for card reset commands, such as CMD0
stop_abort_cmd	0	Can be 1 for commands to stop data transfer, such as CMD12
send_auto_stop	0/1	-
transfer_mode	0	Block transfer
read_write	1	Write to card
data_expected	1	Data command
response_length	0	Can be 1 for R2(long) response
response_expect	1	Can be 0 for commands with no response; for example,

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Parameter	Value	Description
		CMD0, CMD4, CMD15, and so on
User-selectable		
cmd_index	command-index	-
wait_prvdata_complete	1	0: Sends command immediately 1: Sends command after previous data transfer ends
check_response_crc	1	0: Host Controller should not check response CRC 1: Host Controller should check response CRC

After writing to the SDMMC_CMD register, Host Controller starts executing a command; when the command is sent to the bus, a command_done interrupt is generated.

- Software should look for data error interrupts; that is, for bits 7, 9, and 15 of the SDMMC_RINTSTS register. If required, software can terminate the data transfer by sending the STOP command.
- Software should look for Transmit_FIFO_Data_Request and/or timeout conditions from data starvation by the host. In both cases, the software should write data into the FIFO.

When a Data_Transfer_Over interrupt is received, the data command is over. For an open-ended block transfer, if the byte count is 0, the software must send the STOP command. If the byte count is not 0, then upon completion of a transfer of a given number of bytes, the Host Controller should send the STOP command, if necessary. Completion of the AUTO-STOP command is reflected by the Auto_command_done interrupt – bit 14 of the SDMMC_RINTSTS register. A response to AUTO_STOP is stored in SDMMC_RESP1 @0x34.

17.6.2.8 Sending Stop or Abort in Middle of Transfer

The STOP command can terminate a data transfer between a memory card and the Controller, while the ABORT command can terminate an I/O data transfer for only the SDIO_IOONLY and SDIO_COMBO cards.

- Send STOP command – Can be sent on the command line while a data transfer is in progress; this command can be sent at any time during a data transfer.

You can also use an additional setting for this command in order to set the Command register bits (5-0) to CMD12 and set bit 14 (stop_abort_cmd) to 1. If stop_abort_cmd is not set to 1, the Controller does not know that the user stopped a data transfer. Reset bit 13 of the Command register (wait_prvdata_complete) to 0 in order to make the Controller send the command at once, even though there is a data transfer in progress.
Send ABORT command – Can be used with only an SDIO_IOONLY or SDIO_COMBO card. To abort the function that is transferring data, program the function number in ASx bits (CCCR register of card, address 0x06, bits (0-2) using CMD52.

17.6.2.9 Read_Wait Sequence

Read_wait is used with only the SDIO card and can temporarily stall the data transfer—either from function or memory—and allow the host to send commands to any function within the SDIO device. The host can stall this transfer for as long as required. The Host Controller provides the facility to signal this stall transfer to the card. The steps for doing this are:

1) Check if the card supports the read_wait facility; read SRW (bit 2) of the CCCR register @0x08. If this bit is 1, then all functions in the card support the read_wait facility. Use CMD52 to read this bit.
2) If the card supports the read_wait signal, then assert it by setting the read_wait (bit 6) in the SDMMC_CTRL register @0x00.

Clear the read_wait bit in the SDMMC_CTRL register.

17.6.2.10 Controller/DMA/FIFO Reset Usage

- Controller reset – Resets the controller by setting the controller_reset bit (bit 0) in the SDMMC_CTRL register; this resets the CIU and state machines, and also resets the BIU-to-CIU interface. Since this reset bit is self-clearing, after issuing the reset, wait

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until this bit is cleared.

- FIFO reset - Resets the FIFO by setting the fifo_reset bit (bit 1) in the SDMMC_CTRL register; this resets the FIFO pointers and counters of the FIFO. Since this reset bit is self-clearing, after issuing the reset, wait until this bit is cleared.

In external DMA transfer mode, even when the FIFO pointers are reset, if there is a DMA transfer in progress, it could push or pop data to or from the FIFO; the DMA itself completes correctly. In order to clear the FIFO, the software should issue an additional FIFO reset and clear any FIFO under-run or overrun errors in the SDMMC_RAWINTS register caused by the DMA transfers after the FIFO was reset.

17.6.2.11 Card Read Threshold

When an application needs to perform a Single or Multiple Block Read command, the application must program the SDMMC_CARDTHRCTL register with the appropriate Card Read Threshold size (CardRdThreshold) and set the Card Read Threshold Enable (CardRdThrEnable) bit to 1'b1. This additional programming ensures that the Host controller sends a Read Command only if there is space equal to the Card Read Threshold available in the Rx FIFO. This in turn ensures that the card clock is not stopped in the middle a block of data being transmitted from the card. The Card Read Threshold can be set to the block size of the transfer, which guarantees that there is a minimum of one block size of space in the RxFIFO before the controller enables the card clock. The Card Read Threshold is required when the Round Trip Delay is greater than 0.5cclk_in period.

17.6.2.12 Error Handling

The Host Controller implements error checking; errors are reflected in the SDMMC_RAWINTS register@0x44 and can be communicated to the software through an interrupt, or the software can poll for these bits. Upon power-on, interrupts are disabled (int_enable in the SDMMC_CTRL register is 0), and all the interrupts are masked (bits 0-31 of the SDMMC_INTMASK register; default is 0).

Error handling:

- Response and data timeout errors – For response timeout, software can retry the command. For data timeout, the Host Controller has not received the data start bit – either for the first block or the intermediate block – within the timeout period, so software can either retry the whole data transfer again or retry from a specified block onwards. By reading the contents of the SDMMC_TCBCNT later, the software can decide how many bytes remain to be copied.
- Response errors – Set when an error is received during response reception. In this case, the response that copied in the response registers is invalid. Software can retry the command.
- Data errors – Set when error in data reception are observed; for example, data CRC, start bit not found, end bit not found, and so on. These errors could be set for any block-first block, intermediate block, or last block. On receipt of an error, the software can issue a STOP or ABORT command and retry the command for either whole data or partial data.
- Hardware locked error – Set when the Host Controller cannot load a command issued by software. When software sets the start_cmd bit in the SDMMC_CMD register, the Host Controller tries to load the command. If the command buffer is already filled with a command, this error is raised. The software then has to reload the command.
- FIFO under-run/overrun error – If the FIFO is full and software tries to write data in the FIFO, then an overrun error is set. Conversely, if the FIFO is empty and the software tries to read data from the FIFO, an under-run error is set. Before reading or writing data in the FIFO, the software should read the fifo_empty or fifo_full bits in the Status register.
- Data starvation by host timeout – Raised when the Host Controller is waiting for software intervention to transfer the data to or from the FIFO, but the software does not transfer within the stipulated timeout period. Under this condition and when a read transfer is in process, the software should read data from the FIFO and create space for further data reception. When a transmit operation is in process, the software should fill data in the FIFO in order to start transferring data to the card.
- CRC Error on Command – If a CRC error is detected for a command, the CE-ATA device

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does not send a response, and a response timeout is expected from the Host Controller. The ATA layer is notified that an MMC transport layer error occurred.

Notes: During a multiple-block data transfer, if a negative CRC status is received from the device, the data path signals a data CRC error to the BIU by setting the data CRC error bit in the SDMMC_RINTSTS register. It then continues further data transmission until all the bytes are transmitted.

17.6.2.13 Voltage Switching

The Host Controller supports SD 3.0 Ultra High Speed (UHS-1) and is capable of voltage switching in SD-mode, which can be applied to SD High-Capacity (SDHC) and SD Extended Capacity (SDXC) cards. UHS-1 supports only 4-bit mode.

However, whether the IO voltage of 1.8v supported or not is depended on the SoC design.

SD 3.0 UHS-1 supports the following transfer speed modes for UHS-50 and/or UHS-104 cards:

- DS – default-speed up to 25MHz, 3.3V signaling
- HS – high-speed up to 50MHz, 3.3V signaling
- SDR12 – SDR up to SDR 25MHz, 1.8V signaling
- SDR25 – SDR up to 50MHz, 1.8V signaling
- SDR50 – SDR up to 100MHz, 1.8V signaling
- DDR50 – DDR up to 50MHz, 1.8V signaling

Voltage selection can be done in only SD mode. The first CMD0 selects the bus mode-either SD mode or SPI mode. The card must be in SD mode in order for 1.8V signaling mode to apply, during which time the card cannot be switched to SPI mode or 3.3V signaling without a power cycle.

If the System BIOS in an embedded system already knows that it is connected to an SD 3.0 card, then the driver programs the Controller to initiate ACMD41. The software knows from the response of ACMD41 whether or not the card supports voltage switching to 1.8V.

- If bit 32 of ACMD41 response is 1'b1: card supports voltage switching and next command-CMD11-invokes voltage switching sequence. After CMD11 is started, the software must program the IO voltage selection register based on the soc architecture.
- If bit 32 of ACMD41 response is 1'b0: card does not support voltage switching and CMD11 should not be started.

If the card and host controller accept voltage switching, then they support UHS-1 modes of data transfer. After the voltage switch to 1.8V, SDR12 is the default speed.

Since the UHS-1 can be used in only 4-bit mode, the software must start ACMD6 and change the card data width to 4-bit mode; ACMD6 is driven in any of the UHS-1 speeds. If the host wants to select the DDR mode of data transfer, then the software must program the SDMMC_DDR_REG register in the CSR space with the appropriate card number.

To choose from any of the SDR or DDR modes, appropriate values should be programmed in the SDMMC_CLKDIV register.

17.6.2.14 Voltage Switch Operation

The Voltage Switch operation must be performed in SD mode only.

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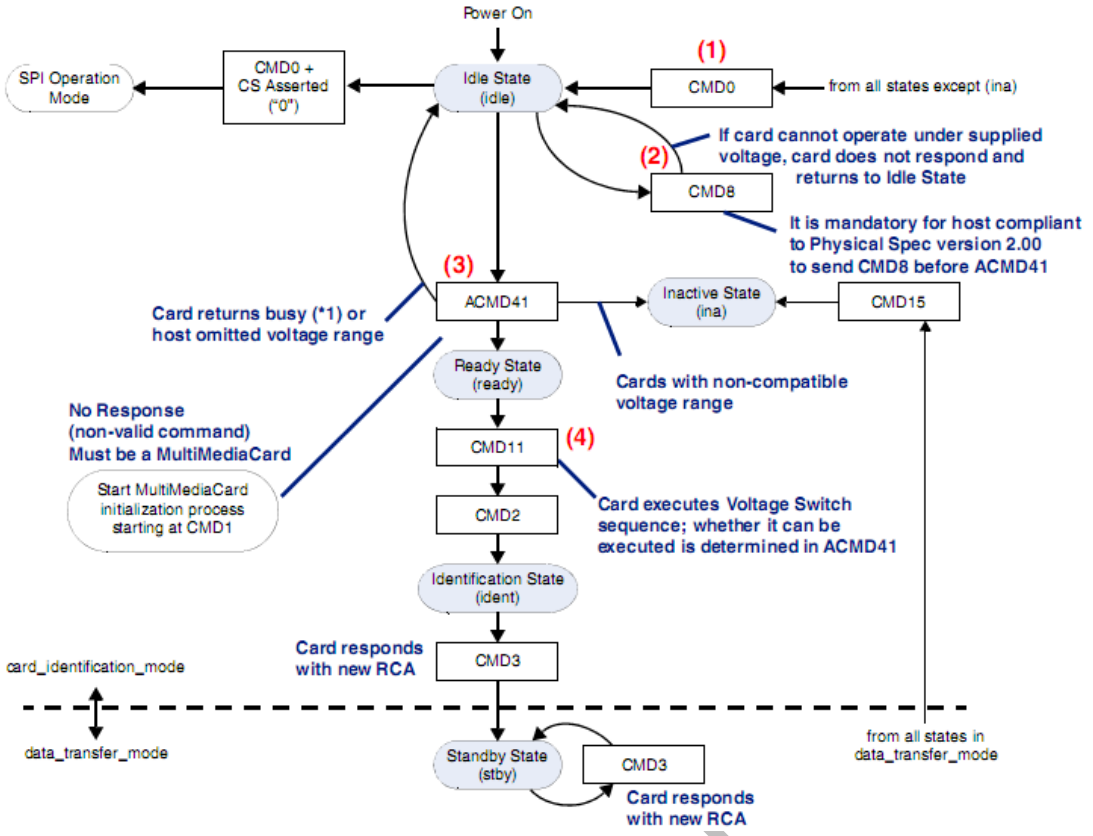


Fig.17-11 Voltage Switching Command Flow Diagram

The following outlines the steps for the voltage switch programming sequence

1) Software Driver starts CMD0, which selects the bus mode as SD.
2) After the bus is in SD card mode, CMD8 is started in order to verify if the card is compatible with the SD Memory Card Specification, Version 2. 00. CMD8 determines if the card is capable of working within the host supply voltage specified in the VHS (19:16) field of the CMD; the card supports the current host voltage if a response to CMD8 is received.
3) ACMD 41 is started. The response to this command informs the software if the card supports voltage switching; bits 38, 36, and 32 are checked by the card argument of ACMD41; refer to following figure.

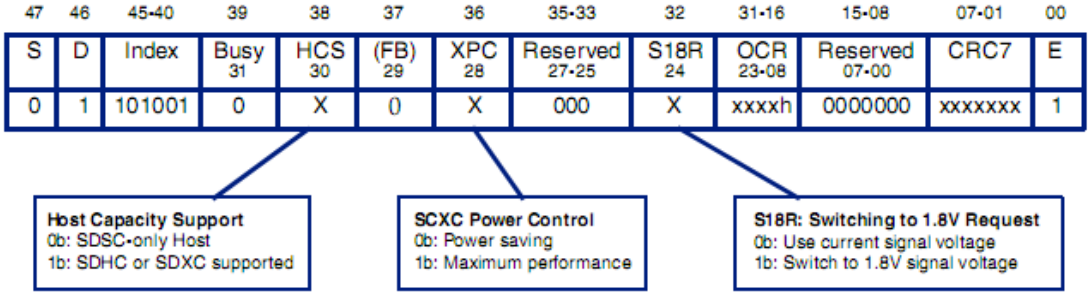


Fig.17-12 ACMD41 Argument

- Bit 30 informs the card if host supports SDHC/SDXC or not; this bit should be set to 1'b1.
- Bit 28 can be either 1 or 0.
- Bit 24 should be set to 1'b1, indicating that the host is capable of voltage switching; refer to following figure.

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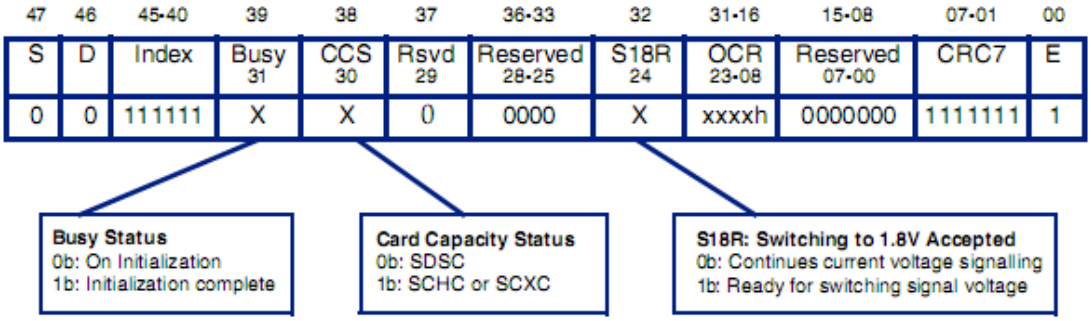


Fig.17-13 ACMD41 Response(R3)

- Bit 30 – If set to 1'b1, card supports SDHC/SDXC; if set to 1'b0, card supports only SDSC
- Bit 24 – If set to 1'b1, card supports voltage switching and is ready for the switch
- Bit 31 – If set to 1'b1, initialization is over; if set to 1'b0, means initialization in process

If the card supports voltage switching, then the software must perform the steps discussed for either the "Voltage Switch Normal Scenario" or the "Voltage Switch Error Scenario".

17.6.2.15 Voltage Switch Normal Scenario

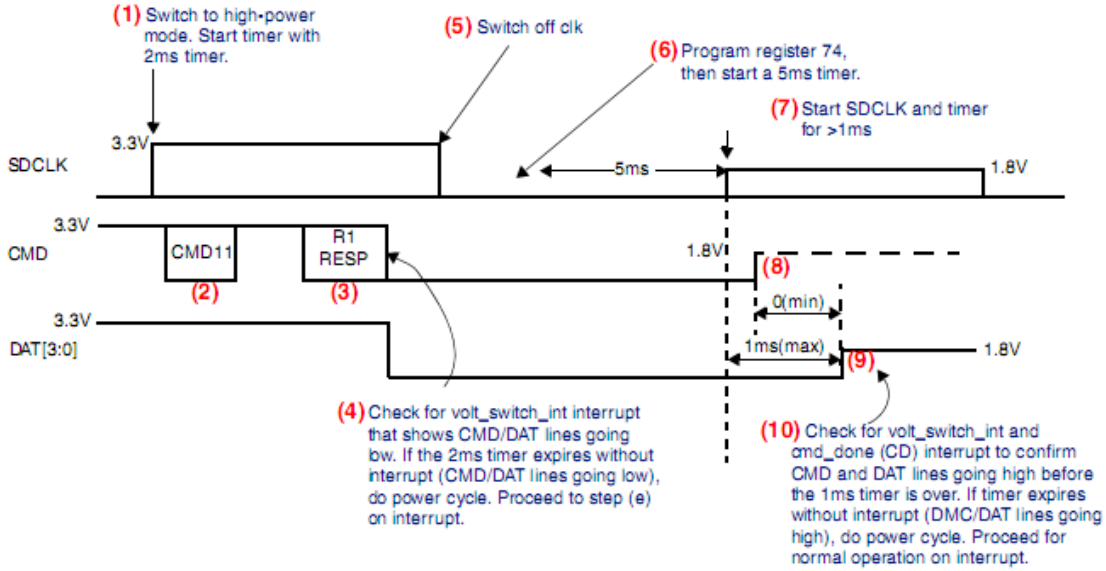


Fig.17-14 Voltage Switch Normal Scenario

1) The host programs SDMMC_CLKENA—cclk_low_power register—with zero (0) for the corresponding card, which makes the host controller move to high-power mode. The application should start a timer with a recommended value of 2ms; this value of 2 ms is determined as below: Total cycles required for CMD11 = 48 cycles
   Total cycles required for RESP R1 = 48 cycles
   Maximum clock delay between MCD11 end to start of RESP1 = 60 cycles
   Total = 48+48 + 60 = 160
   Minimum frequency during enumeration is 100 KHz; that is, 10us
   Total time = 160 * 10us = 1600us = 1. 6ms ~ 2ms
2) The host issues CMD11 to start the voltage switch sequence. Set bit 28 to 1'b1 in CMD when setting CMD11; for more information on setting bits, refer to "Boot Operation".
3) The card returns R1 response; the host controller does not generate cmd_done interrupt on receiving R1 response.
4) The card drives CMD and DAT [3:0] to low immediately after the response. The host controller generates interrupt (VOLT_SWITCH_INT) once the CMD or DAT [3:0] line goes low. The application should wait for this interrupt. If the 2ms timer expires without an interrupt (CMD/DAT lines going low), do a power cycle.

Note: Before doing a power cycle, switch off the card clock by programming SDMMC_CLKENA register

Proceed to step (5) on getting an interrupt (VOLT_SWITCH_INT).

Note: This interrupt must be cleared once this interrupt is received. Additionally, this interrupt should not be masked during the voltage switch sequence.

If the timer expires without interrupt (CMD/DAT lines going low), perform a power cycle.

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Proceed to step (5) on interrupt.

1) Program the SDMMC_CLKENA register, with 0 for the corresponding card; the host stops supplying SDCLK.
2) Program Voltage register to the required values for the corresponding card. The application should start a timer > 5ms.
3) After the 5ms timer expires, the host voltage regulator is stable. Program SDMMC_CLKENA register, with 1 for the corresponding card; the host starts providing SDCLK at 1. 8V; this can be at zero time after Voltage register has been programmed. When the SDMMC_CLKENA register is programmed, the application should start another timer > 1ms.
4) By detecting SDCLK, the card drives CMD to high at 1. 8V for at least one clock and then stops driving (tri-state); CMD is triggered by the rising edge of SDCLK (SDR timing).
5) If switching to 1. 8V signaling is completed successfully, the card drives DAT [3:0] to high at 1. 8V for at least one clock and then stops driving (tri-state); DAT [3:0] is triggered by the rising edge of SDCLK (SDR timing). DAT[3:0] must be high within 1ms from the start of SDCLK.
6) The host controller generates a voltage switch interrupt (VOLT_SWITCH_INT) and a command done (CD) interrupt once the CMD and DAT[3:0] lines go high. The application should wait for this interrupt to confirm CMD and DAT lines going high before the 1ms timer is done.

If the timer expires without the voltage switch interrupt (VOLT_SWITCH_INT), a power cycle should be performed. Program the SDMMC_CLKENA register to stop the clock for the corresponding card number. Wait for the cmd_done (CD) interrupt. Proceed for normal operation on interrupt. After the sequence is completed, the host and the card start communication in SDR12 timing.

17.6.2.16 Voltage Switch Error Scenario

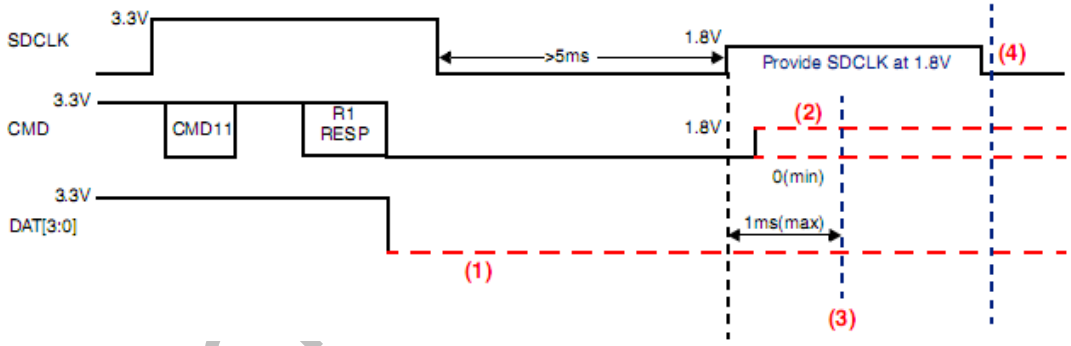


Fig.17-15 Voltage Switch Error Scenario

1) If the interrupt (VOLT_SWITCH_INT) does not come, then the 2 ms timer should time out and a power cycle should be initiated.

Note: Before performing a power cycle, switch off the card clock by programming SDMMC_CLKENA register; no cmd_done (CD) interrupt is generated.

Additionally, if the card detects a voltage error at any point in between steps (5) and (7) in the card keeps driving DAT[3:0] to low until card power off.

2) CMD can be low or tri-state.
3) The host controller generates a voltage switch interrupt once the CMD and DAT[3:0] lines go high. The application should check for an interrupt to confirm CMD and DAT lines going high before the 1 ms timer is done.

If the 1 ms timer expires without interrupt (VOLT_SWITCH_INT) and cmd_done (CD), a power cycle should be performed. Program the SDMMC_CLKENA register to stop SDCLK of the corresponding card. Wait for the cmd_done interrupt. Proceed for normal operation on interrupt.

4) If DAT[3:0] is low, the host drives SDCLK to low and then stops supplying the card power.

Note: The card checks voltages of its own regulator output and host signals to ensure they are less than 2. 5V. Errors are indicated by (1) and (2).

- If voltage switching is accepted by the card, the default speed is SDR12.
- Command Done is given:

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- If voltage switching is properly done, CMD and DAT line goes high.
- If switching is not complete, the 1ms timer expires, and the card clock is switched off.

Note: No other CMD should be driven before the voltage switching operation is completed and Command Done is received.

- The application should use CMD6 to check and select the particular function; the function appropriate-speed should be selected.

After the function switches, the application should program the correct value in the CLKDIV register, depending on the function chosen. Additionally, if Function 0x4 of the Access mode is chosen—that is, DDR50, then the application should also program 1'b1 in DDR_REG for the card number that has been selected for DDR50 mode.

17.6.3 DDR Operation

17.6.3.1 4-bit DDR Programming Sequence

DDR programming should be done only after the voltage switch operation has completed. The following outlines the steps for the DDR programming sequence:

1) Once the voltage switch operation is complete, the user must program voltage selection register to the required values for the corresponding card.

- To start a card to work in DDR mode, the application must program a bit of the newly defined SDMMC_UHSREG[16] register with a value of 1'b1.
- The bit that the user programs depends on which card is to be accessed in DDR mode.

To move back to SDR mode, a power cycle should be run on the card—putting the card in SDR12 mode—and only then should SDMMC_UHSREG[16]be set back to 1'b0 for the appropriate card.

17.6.3.2 8-bit DDR Programming Sequence

The following outlines the steps for the 8-bit DDR programming sequence:

1) The cclk_in signal should be twice the speed of the required cclk_out. Thus, if the cclk_out signal is required to be 50 MHz, the cclk_in signal should be 100 MHz.
2) The SDMMC_CLKDIV register should always be programmed with a value higher than zero (0); that is, a clock divider should always be used for 8-bit DDR mode.
3) The application must program the SDMMC_UHSREG[16] register (ddr_reg bits) by assigning it with a value of 1 for the bit corresponding to the card number; this causes the selected card to start working in DDR mode.

Depending on the card number, the SDMMC_CTYPE [16] bits should be set in order to make the host work in the 8-bit mode.

17.6.3.3 eMMC4.5 DDR START Bit

The eMMC4.5 changes the START bit definition in the following manner:

1) Receiver samples the START bit on the rising edge.
2) On the next rising edge after sampling the START bit, the receiver must sample the data.
3) Removes requirement of the START bit and END bit to be high for one full cycle.

Notes: The Host Controller does not support a START bit duration higher than one clock cycle. START bit durations of one or less than one clock cycle are supported and can be defined at the time of startup by programming the EMMC_DDR_REG register.

17.6.3.4 Reset Command/Moving from DDR50 to SDR12

To reset the mode of operation from DDR50 to SDR12, the following sequence of operations has to be done by the application:

1) Issue CMD0.
2) When CMD0 is received, the card changes from DDR50 to SDR12.
3) Program the SDMMC_CLKDIV register with an appropriate value.
4) Set ddr_reg to 0.

Note: The Voltage register should not be programmed to 0 while switching from DDR50 to SDR12, since the card is still operating in 1.8V mode after receiving CMD0.

17.6.4 H/W Reset Operation

When the RST_n signal goes low, the card enters a pre-idle state from any state other than the inactive state.

The following outlines the steps for the H/W reset programming sequence:

1) Program CMD12 to end any transfer in process.
2) Wait for DTO, even if no response is sent back by the card.

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3) Set the following resets:
- DMA reset–SDMMC_CTRL [2] bit
- FIFO reset–SDMMC_CTRL [1] bit

Note: The above steps are required only if a transfer is in process.

4) Program the SDMMC_RSTN register with a value of 0; this can be done at any time when the card is connected to the controller. This programming asserts the RST_n signal and resets the card.
5) Wait for minimum of 1 µs or cclk_in period, whichever is greater
6) After a minimum of 1 µs, the application should program a value of 0 into the SDMMC_RSTN register. This de-asserts the RST_n signal and takes the card out of reset.
7) The application can program a new CMD only after a minimum of 200 µs after the de-assertion of the RST_n signal, as per the MMC 4.41 standard.

Note: For backward compatibility, the RST_n signal is temporarily disabled in the card by default. The host may need to set the signal as either permanently enabled or permanently disabled before it uses the card.

17.6.5 FBE Scenarios

An FBE occurs due to an AHB error response on the AHB bus. This is a system error, so the software driver should not perform any further programming to the Host. The only recovery mechanism from such scenarios is to do one of the following:

- Issue a hard reset by asserting the reset_n signal
- Do a program controller reset by writing to the SDMMC_CTRL[0] bit

17.6.5.1 FIFO Overflow and Underflow

During normal data transfer conditions, FIFO overflow and underflow will not occur. However if there is a programming error, then FIFO overflow/underflow can result. For example, consider the following scenarios.

- For transmit: PBL=4, Tx watermark = 1. For the above programming values, if the FIFO has only one location empty, it issues a dma_req to IDMAC FSM. Due to PBL value=4, the IDMAC FSM performs 4 pushes into the FIFO. This will result in a FIFO overflow interrupt.
- For receive: PBL=4, Rx watermark = 1. For the above programming values, if the FIFO has only one location filled, it issues a dma_req to IDMAC FSM. Due to PBL value=4, the IDMAC FSM performs 4 pops to the FIFO. This will result in a FIFO underflow interrupt.

The driver should ensure that the number of bytes to be transferred as indicated in the descriptor should be a multiple of 4bytes with respect to H_DATA_WIDTH=32. For example, if the SDMMC_BYTCNT=13, the number of bytes indicated in the descriptor should be 16 for H_DATA_WIDTH=32.

17.6.5.2 Programming of PBL and Watermark Levels

The DMAC performs data transfers depending on the programmed PBL and threshold values.

Table 17-13 PBL and Watermark Levels

PBL (Number of transfers)	Tx/Rx Watermark Value
1	Greater than or equal to 1
4	Greater than or equal to 4
8	Greater than or equal to 8
16	Greater than or equal to 16
32	Greater than or equal to 32
64	Greater than or equal to 64
128	Greater than or equal to 128
256	Greater than or equal to 256

17.6.6 Variable Delay Usage

The delay time of every element is in the range of 36ps~68ps, varying with different voltage and temperature.

The control signals for variable delay element usage are shown as follows.

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17.6.6.1 SDMMC0 Variable Delay Usage

Table 17-14 Configuration for SDMMC0 Variable Delay Usage

Signal Name	Source	Default	Description
init_state	CRU_SDMMC0_CON0[0]	0	Enable initialization for clock source. 1'b0: Disable 1'b1: Enable When init_state=1, the host clocks including drive clock and sample clock are inactive.
drv_degree[1:0]	CRU_SDMMC0_CON0[2:1]	2	Phase selection for drive clock. 2'h0: 0-degree 2'h1: 90-degree 2'h2: 180-degree 2'h3: 270-degree It can be modified when init_state=1 and should be stable when init_state=0.
drv_delaynum[7:0]	CRU_SDMMC0_CON0[10:3]	0	Delay element number configuration for drive clock. It can be modified when init_state=1 and should be stable when init_state=0.
drv_sel	CRU_SDMMC0_CON0[11]	0	Selection for drive clock: 1'b0: Select clock delayed by phase shift 1'b1: Select clock delayed by phase shift and delay line It can be modified when init_state=1 and should be stable when init_state=0.
sample_degree[1:0]	CRU_SDMMC0_CON1[2:1]	0	Phase selection for sample clock. 2'h0: 0-degree 2'h1: 90-degree 2'h2: 180-degree 2'h3: 270-degree It can be modified when init_state=1 and should be stable when init_state=0.
sample_delaynum[7:0]	CRU_SDMMC0_CON1[10:3]	0	Delay element number configuration for sample clock. It can be modified when init_state=1 and should be stable when init_state=0.
sample_sel	CRU_SDMMC0_CON1[11]	0	Selection for sample clock: 1'b0: Select clock delayed by phase shift 1'b1: Select clock delayed by phase shift and delay line It can be modified when init_state=1 and should be stable when init_state=0.

17.6.6.2 SDMMC1 Variable Delay Usage

Table 17-15 Configuration for SDMMC1 Variable Delay Usage

Signal Name	Source	Default	Description
init_state	CRU_SDMMC1_CON0[0]	0	Enable initialization for clock

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Signal Name	Source	Default	Description
			source. 1'b0: Disable 1'b1: Enable When init_state=1, the host clocks including drive clock and sample clock are inactive.
drv_degree[1:0]	CRU_SDMMC1_CON0[2:1]	2	Phase selection for drive clock. 2'h0: 0-degree 2'h1: 90-degree 2'h2: 180-degree 2'h3: 270-degree It can be modified when init_state=1 and should be stable when init_state=0.
drv_delaynum[7:0]	CRU_SDMMC1_CON0[10:3]	0	Delay element number configuration for drive clock. It can be modified when init_state=1 and should be stable when init_state=0.
drv_sel	CRU_SDMMC1_CON0[11]	0	Selection for drive clock: 1'b0: Select clock delayed by phase shift 1'b1: Select clock delayed by phase shift and delay line It can be modified when init_state=1 and should be stable when init_state=0.
sample_degree[1:0]	CRU_SDMMC1_CON1[2:1]	0	Phase selection for sample clock. 2'h0: 0-degree 2'h1: 90-degree 2'h2: 180-degree 2'h3: 270-degree It can be modified when init_state=1 and should be stable when init_state=0.
sample_delaynum[7:0]	CRU_SDMMC1_CON1[10:3]	0	Delay element number configuration for sample clock. It can be modified when init_state=1 and should be stable when init_state=0.
sample_sel	CRU_SDMMC1_CON1[11]	0	Selection for sample clock: 1'b0: Select clock delayed by phase shift 1'b1: Select clock delayed by phase shift and delay line It can be modified when init_state=1 and should be stable when init_state=0.

17.6.7 Variable Delay Tuning

Tuning is defined by SD and MMC cards to determine the correct sampling point required for the host, especially for the speed modes SDR104 and HS200 where the output delays from the cards can be up to 2 UI. Tuning is required for other speed modes-such as DDR50-even though the output delay from the card is less than one cycle.
Command for tuning is different for different cards.

- SD Memory Card:

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- CMD19 – SD card for SDR50 and SDR104 speed modes. Tuning data is defined by card specifications.
- CMD6 – SD card for speed modes not supporting CMD19. Tuning data is the 64byte SD status.

- Multimedia Card:
  - CMD21 – MMC card for HS200 speed mode. Tuning data is defined by card specifications.
  - CMD8 – MMC card for speed modes not supporting CMD21. Tuning data is 512 byte ExtCSD data.

The following is the procedure for variable delay tuning:

1) Set a phase shift of 0-degree on cclk_in_sample.
2) Send the Tuning command to the card; the card in turn sends an R1 response on the CMD line and tuning data on the DAT line.
3) If the host sees any of the errors—start bit error, data crc error, end bit error, data read time-out, response CRC error, response error—then the sampling point is incorrect.
4) Send CMD12 to bring the host controller state machines to idle.
   - The card may treat CMD12 as an invalid command because the card has successfully sent the tuning data, and it cannot send a response.
   - The host controller may generate a response time-out interrupt that must be cleared by software.
5) Repeat steps 2) to 4) by increasing the phase shift value or delay element number on cclk_in_sample until the correct sampling point is received such that the host does not see any of the errors.
6) Mark this phase shift value as the starting point of the sampling window.
7) Repeat steps 2 to 4 by increasing the phase shift value or delay element number on cclk_in_sample until the host sees the errors starting to come again or the phase shift value reaches 360-degree.
8) Mark the last successful phase shift value as the ending point of the sampling window.

A window is established where the tuning block is matched. For example, for a scenario where the tuning block is received correctly for a phase shift window of 90-degree and 180-degree, then an appropriate sampling point is established as 135-degree. Once a sampling point is established, no errors should be visible in the tuning block.

17.6.8 Card Detection Method

There are many methods for SDMMC0/SDMMC1 device detection.

- Method1: Using SDMMC_CDETECT register, which is value on card_detect_n input port. 0 represents presence of card. This method is available only for SDMMC0/SDMMC1.
- Method2: Using card detection unit in Host Controller, outputting host interrupt. The card detection unit looks for any changes in the card-detect signals for card insertion or card removal. It filters out the debounces associated with mechanical insertion or removal, and generates one interrupt to the host. You can program the debounce filter value in SDMMC_DEBNCE [23:0]. Following figure illustrates the timing for card-detect signals. This method is available only for SDMMC0/SDMMC1.

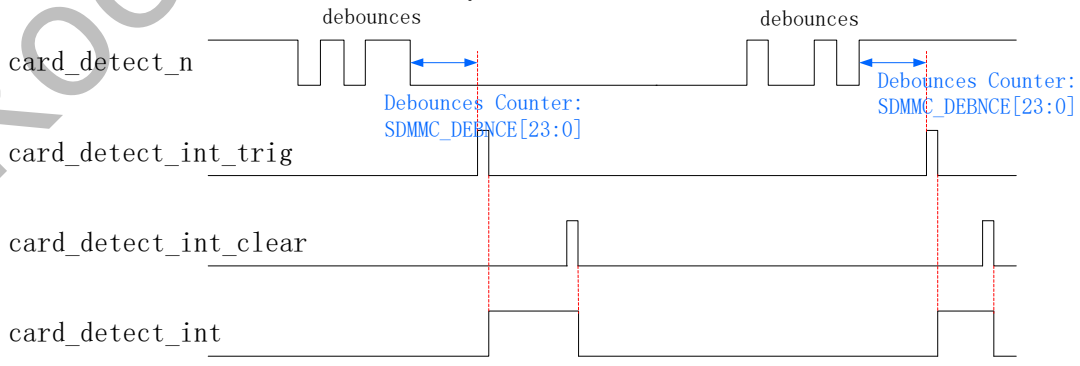


Fig.17-16 Card Detection Method 2

- Method3: Using general card detection unit, outputting detect_dual_edge_int connecting to IRQ[91] for SDMMC0 and IRQ[92] for SDMMC1. Similar to Method2, except that the debounce time is configurable by PMUGRF_SDMMC_DET; and the insertion/removal detection interrupt can be enabled or cleared respectively.

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The detailed register information is:

Table 17-16 Register for SDMMC0 Card Detection Method 3

Signal Name	Source	Default	Description
sd_detectn_rise_edge_irq_en	PMUGRF_SIG_DETECT_CON[0]	0	Enable SDMMC detect pin rising edge interrupt. 1'b0: Disable 1'b1: Enable
sd_detect_fall_edge_detect_en	PMUGRF_SIG_DETECT_CON[1]	0	Enable SDMMC detect pin falling edge interrupt. 1'b0: Disable 1'b1: Enable
sd_detect_rising_edge_dectect_status	PMUGRF_SIG_DETECT_STATUS[0]	0	SDMMC detect pin rising edge status. 1'b0: Inactive 1'b1: Active
sd_detect_fall_edge_detect_status	PMUGRF_SIG_DETECT_STATUS[1]	0	SDMMC detect pin falling edge status. 1'b0: Inactive 1'b1: Active
sd_detect_rising_edge_dectect_clr	PMUGRF_SIG_DETECT_CLR[0]	0	Enable clear for SDMMC detect pin rising edge interrupt. 1'b0: Disable 1'b1: Enable
sd_detect_fall_edge_detect_clr	PMUGRF_SIG_DETECT_CLR[1]	0	Enable clear for SDMMC detect pin falling edge interrupt. 1'b0: Disable 1'b1: Enable

Table 17-17 Register for SDMMC1 Card Detection Method 3

Signal Name	Source	Default	Description
sd_detectn_rise_edge_irq_en	PMUGRF_SIG_DETECT_CON[2]	0	Enable SDMMC detect pin rising edge interrupt. 1'b0: Disable 1'b1: Enable
sd_detect_fall_edge_detect_en	PMUGRF_SIG_DETECT_CON[3]	0	Enable SDMMC detect pin falling edge interrupt. 1'b0: Disable 1'b1: Enable
sd_detect_rising_edge_dectect_status	PMUGRF_SIG_DETECT_STATUS[2]	0	SDMMC detect pin rising edge status. 1'b0: Inactive 1'b1: Active
sd_detect_fall_edge_detect_status	PMUGRF_SIG_DETECT_STATUS[3]	0	SDMMC detect pin falling edge status. 1'b0: Inactive 1'b1: Active
sd_detect_rising_edge_dectect_clr	PMUGRF_SIG_DETECT_CLR[2]	0	Enable clear for SDMMC detect pin rising edge interrupt. 1'b0: Disable 1'b1: Enable
sd_detect_fall_edge_detect_clr	PMUGRF_SIG_DETECT_CLR[3]	0	Enable clear for SDMMC detect pin falling edge interrupt. 1'b0: Disable 1'b1: Enable

17.6.9 SDMMC IOMUX With JTAG

The VCCIO3GPIO1b5/VCCIO3GPIO1b6 for sdmmc_cdata2/sdmmc_cdata3 is shared with

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jtag_tck/jtag_tms. The condition of usage for SDMMC or JTAG usage is as follows.

- If IOC234_GRF_JTAG_CON0[0] is equal to 1 and SD/MMC card is not detected within detection time(defined in VO_GRF_SDMMC_SDDETFLT, in the unit of XIN24M clock), the GPIOs are used for JTAG.
- Otherwise, the GPIOs' usage is defined by IOMUX configuration.

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Chapter 18 EMMC Host Controller

18.1 Overview

The eMMC Host Controller is highly programmable, and provides high performance with AXI as the bus interface for data transfer (master interface) and AHB as its slave interface.
It supports following features:

- Supports SD-HCI Host version 4 mode or less
  - Supports same SD-HCI register set for eMMC transfers
  - Supports Command Queuing Engine (CQE) and compliant with eMMC CQ HCI
  - Supports the following data transfer types: CPU, SDMA, AMDM2, ADMA3
- Supports eMMC protocols including eMMC 5.1
  - Supports Auto-tuning
  - Supports 4-bit/8-bit interface
  - Supports legacy, High Speed SDR, High Speed DDR, HS200, and HS400 speed modes
  - Supports boot operation and alternative boot operation
- AHB Slave Interface:
  - Supports 32-bit data width and address width
- AXI Master Interface:
  - Supports 32-bit address width and 64-bit data width
- Phase adjustment:

Supports phase auto adjustment for transmit clock, sample clock and data strobe, command output.

18.2 Block Diagram

The Host Controller consists of the following main functional blocks.

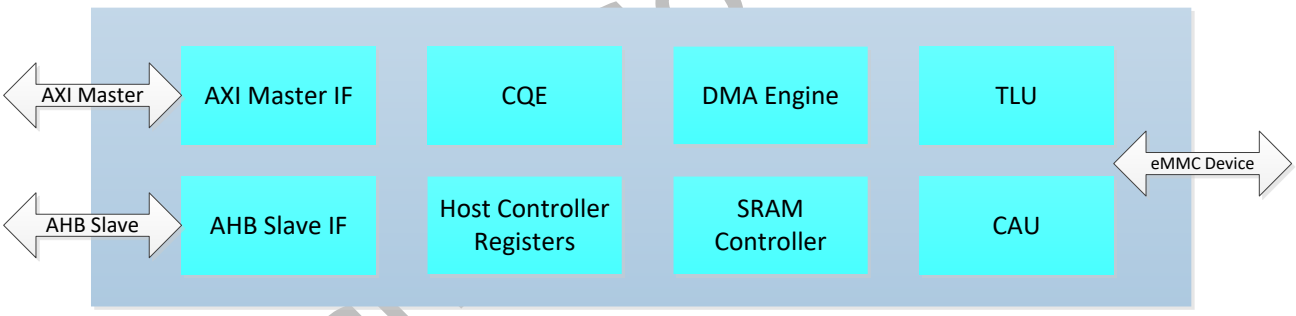


Fig.18-1 EMMC Host Control Block Diagram

18.3 Function Description

18.3.1 The AXI Master Bus Interface Unit

This Master Bus Interface Unit implements the logic to transfer data on the AMBA Extensible Interface Bus (AXI) bus. The AXI interface transfers data to and from the system memory through the AXI master bus interface, respectively.

18.3.2 The AHB Slave Bus Interface Unit

The AHB slave bus interface module implements the logic to primarily access the host registers by using an external AMBA high-performance (AHB) bus.

18.3.3 Host Controller Registers

The host controller register unit comprises of the standard SD host controller registers as specified in the SD Specifications Part A2 SD Host Controller Standard Specification Version 4.20a. It also includes Command Queuing registers compliance to JEDEC eMMC 5.1 HCI specification.

18.3.4 DMA Engine

The DMA Engine unit handles data transfer between the host and system memory.

- Support SDMA/ADMA2/ADMA3 modes
- Fetch the descriptor and data

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- The same DMA engine is used to interleave data transfer and descriptor fetch. This enables new task descriptor fetches (for CMD44 and CMD45) while DMA is moving data during task execution (for CMD46 and CMD47).
- The AXI transaction ID 0 is used for moving data and AXI transaction ID 1 is used to fetch task descriptors.
- Pre-fetch data for back-to-back eMMC write commands
- Write back the received data packets to the system memory

18.3.5 SRAM Controller

The SRAM controller interfaces the packet buffer of the host and the transaction controller units. The SRAM is a single clock single-port RAM synchronous to the core base clock. The width is 64-bit, the depth is 288-location.

18.3.6 Command Queuing Engine

This module implements command queuing and includes the following:

- Task scheduler with the ability to prioritize execution of tasks
- Control logic for descriptor fetch
- Control and sequence task submission and execution
- Status polling
- Timers and counter dedicated for CQE operation
- Interrupt coalescing logic

18.3.7 Transfer Level Unit

The TLU manages the command/response and data flow for communication with memory cards.

18.3.8 Clock Adjustment Unit

The clock adjustment unit (CAU) will detect the clock period and get the delay precision, adjust the clock phase base on the dedicate delay element. Also, you can program the register to set the delay precision. The flowing signals supports adjustment: transmit clock, sample clock and data strobe, command output.

18.4 Register Description

18.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

18.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
EMMC_SDMASA	0x0000	W	0x00000000	SDMA System Address Register
EMMC_BLOCKSIZE	0x0004	HW	0x00000000	Block Size Register
EMMC_BLOCKCOUNT	0x0006	HW	0x00000000	Block Count Register
EMMC_ARGUMENT	0x0008	W	0x00000000	Argument Register
EMMC_XFER_MODE	0x000C	HW	0x00000000	Transfer Mode Register
EMMC_CMD	0x000E	HW	0x00000000	Command Register
EMMC_RESP01	0x0010	W	0x00000000	Response Register 0/1
EMMC_RESP23	0x0014	W	0x00000000	Response Register 2/3
EMMC_RESP45	0x0018	W	0x00000000	Response Register 4/5
EMMC_RESP67	0x001C	W	0x00000000	Response Register 6/7
EMMC_BUF_DATA	0x0020	W	0x00000000	Buffer Data Port Register
EMMC_PSTATE	0x0024	W	0x19FF0000	Present State Register
EMMC_HOST_CTRL1	0x0028	B	0x00000000	Host Control 1 Register
EMMC_PWR_CTRL	0x0029	B	0x00000000	Power Control Register
EMMC_BGAP_CTRL	0x002A	B	0x00000000	Block Gap Control Register
EMMC_CLK_CTRL	0x002C	HW	0x00000000	Clock Control Register
EMMC_TOUT_CTRL	0x002E	B	0x00000000	Timeout Control Register
EMMC_SW_RST	0x002F	B	0x00000000	Software Reset Register
EMMC_NORMAL_INT_STAT	0x0030	HW	0x00000000	Normal Interrupt Status Register

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Name	Offset	Size	Reset Value	Description
EMMC_ERROR_INT_STAT	0x0032	HW	0x00000000	Error Interrupt Status Register
EMMC_NORMAL_INT_STAT_EN	0x0034	HW	0x00000000	Normal Interrupt Status Enable Register
EMMC_ERROR_INT_STAT_EN	0x0036	HW	0x00000000	Error Interrupt Status Enable Register
EMMC_NORMAL_INT_SIGNAL_EN	0x0038	HW	0x00000000	Normal Interrupt Signal Enable Register
EMMC_ERROR_INT_SIGNAL_EN	0x003A	HW	0x00000000	Error Interrupt Signal Enable Register
EMMC_AUTO_CMD_STAT	0x003C	HW	0x00000000	Auto CMD Error Status Register
EMMC_HOST_CTRL2	0x003E	HW	0x00000000	Host Control 2 Register
EMMC_CAPABILITIES1	0x0040	W	0x40EDC880	Capabilities Register 1
EMMC_CAPABILITIES2	0x0044	W	0x000A2077	Capabilities Register 2
EMMC_FORCE_AUTO_CMD_STAT	0x0050	HW	0x00000000	Force Event Register for Auto CMD Error Status Register
EMMC_FORC_ERR_INT_STAT	0x0052	HW	0x00000000	Force Event Register for Error Interrupt Status Register
EMMC_ADMA_ERR_STAT	0x0054	B	0x00000000	ADMA Error Status Register
EMMC_ADMA_SA	0x0058	W	0x00000000	ADMA System Address Register
EMMC_PRESET_INIT	0x0060	HW	0x00000000	Preset Value for Initialization Register
EMMC_PRESET_DS	0x0062	HW	0x00000000	Preset Value for Default Speed Register
EMMC_PRESET_HS	0x0064	HW	0x00000000	Preset Value for High Speed Register
EMMC_PRESET_SDR12	0x0066	HW	0x00000000	Preset Value for SDR12 Register
EMMC_PRESET_SDR25	0x0068	HW	0x00000000	Preset Value for SDR25 Register
EMMC_PRESET_SDR50	0x006A	HW	0x00000000	Preset Value for SDR50 Register
EMMC_PRESET_SDR104	0x006C	HW	0x00000000	Preset Value for SDR104 Register
EMMC_PRESET_DDR50	0x006E	HW	0x00000000	Preset Value for DDR50 Register
EMMC_ADMA_ID	0x0078	W	0x00000000	ADMA3 Integrated Descriptor Address Register
EMMC_SLOT_INTR_STATUS	0x00FC	HW	0x00000000	Slot Interrupt Status Register
EMMC_HOST_CNTRL_VERS	0x00FE	HW	0x00001005	Host Controller Version Register
EMMC_CQVER	0x0180	W	0x00000510	Command Queuing Version Register
EMMC_CQCAP	0x0184	W	0x00000000	Command Queuing Capabilities Register
EMMC_CQCFG	0x0188	W	0x00000000	Command Queuing Configuration Register
EMMC_CQCTRL	0x018C	W	0x00000000	Command Queuing Control Register
EMMC_CQIS	0x0190	W	0x00000000	Command Queuing Interrupt Status Register
EMMC_CQISE	0x0194	W	0x00000000	Command Queuing Interrupt Status Enable Register
EMMC_CQISGE	0x0198	W	0x00000000	Command Queuing Interrupt Signal Enable Register
EMMC_CQIC	0x019C	W	0x00000000	Command Queuing Interrupt Coalescing Register

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Name	Offset	Size	Reset Value	Description
EMMC_CQTDLBA	0x01A0	W	0x00000000	Command Queuing Task Descriptor List Base Address Register
EMMC_CQTDBR	0x01A8	W	0x00000000	Command Queuing Door Bell Register
EMMC_CQTCN	0x01AC	W	0x00000000	Command Queuing Task Clear Notification Register
EMMC_CQDQS	0x01B0	W	0x00000000	Command Queuing Device Queue Status Register
EMMC_CQDPT	0x01B4	W	0x00000000	Command Queuing Device Pending Tasks Register
EMMC_CQTCLR	0x01B8	W	0x00000000	Command Queuing Task Clear Register
EMMC_CQSSC1	0x01C0	W	0x00011000	Command Queuing Send Status Configuration 1 Register
EMMC_CQSSC2	0x01C4	W	0x00000000	Command Queuing Send Status Configuration 2 Register
EMMC_CQCRDCT	0x01C8	W	0x00000000	Command Queuing Command Response for Direct Command Register
EMMC_CQRMEM	0x01D0	W	0xFDF9A080	Command Queuing Command Response Mode Error Mask Register
EMMC_CQTERRI	0x01D4	W	0x00000000	Command Queuing Task Error Information Register
EMMC_CQCRI	0x01D8	W	0x00000000	Command Queuing Command Response Index Register
EMMC_CQCRA	0x01DC	W	0x00000000	Command Queuing Command Response Argument Register
EMMC_VER_ID	0x0500	W	0x00000000	Host Version ID Register
EMMC_VER_TYPE	0x0504	W	0x00000000	Host Version Type Register
EMMC_HOST_CTRL3	0x0508	B	0x00000000	Host Control 3 Register
EMMC_EMMC_CTRL	0x052C	HW	0x00000004	EMMC Control Register
EMMC_BOOT_CTRL	0x052E	HW	0x00000000	Boot Control Register
EMMC_AT_CTRL	0x0540	W	0x00000000	Tuning Control Register
EMMC_AT_STAT	0x0544	W	0x00000000	Tuning Status Register
EMMC_DLL_CTRL	0x0800	W	0x00000000	DLL Global Control Register
EMMC_DLL_RXCLK	0x0804	W	0x00000000	DLL Control Register for Receive Clock
EMMC_DLL_TXCLK	0x0808	W	0x00000000	DLL Control Register for Transmit Clock
EMMC_DLL_STRBIN	0x080C	W	0x00000000	DLL Control Register for Strobe Input
EMMC_DLL_CMDOUT	0x0810	W	0x00000000	DLL Control Register for Command Output
EMMC_DLL_STATUS0	0x0840	W	0x00000000	DLL Status Register 0
EMMC_DLL_STATUS1	0x0844	W	0x00000000	DLL Status Register 1

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

18.4.3 Detail Register Description

EMMC_SDMASA

Address: Operational Base(0xFF870000) + offset (0x0000)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	BLOCKCNT_SDMASA 32-bit Block Count (SDMA System Address). 1. SDMA System Address (Host Version 4 Enable = 0): This register contains the system memory address for an SDMA transfer in the 32-bit addressing mode. When the Host Controller stops an SDMA transfer, this register points to the system address of the next contiguous data position. It can be accessed only if no transaction is executing. Reading this register during data transfers may return an invalid value. 2. 32-bit Block Count (Host Version 4 Enable = 1): From the Host Controller Version 4.10 specification, this register is redefined as 32-bit Block Count. The Host Controller decrements the block count of this register for every block transfer and the data transfer stops when the count reaches zero. This register must be accessed when no transaction is executing. Reading this register during data transfers may return invalid value. Values: 32'hFFFFFFFF: 1 Block ..... 32'h00000002: 2 Blocks 32'h00000001: 1 Block 32'h00000000: Stop Count Note: a. For Host Version 4 Enable = 0, the Host driver does not program the system address in this register while operating in ADMA mode. The system address must be programmed in the ADMA System Address register. b. For Host Version 4 Enable = 0, the Host driver programs a non-zero 32-bit block count value in this register when Auto CMD23 is enabled for non-DMA and ADMA modes. Auto CMD23 cannot be used with SDMA. c. This register must be programmed with a non-zero value for data transfer if the 32-bit Block count register is used instead of the 16-bit Block count register.

EMMC_BLOCKSIZE

Address: Operational Base(0xFF870000) + offset (0x0004)

Bit	Attr	Reset Value	Description
15	RO	0x0	reserved
14:12	RW	0x0	SDMA_BUF_BDARY SDMA Buffer Boundary. These bits specify the size of contiguous buffer in system memory. The SDMA transfer waits at every boundary specified by these fields and the Host Controller generates the DMA interrupt to request the Host Driver to update the SDMA System Address register. Values: 3'h0: 4K bytes SDMA Buffer Boundary 3'h1: 8K bytes SDMA Buffer Boundary 3'h2: 16K bytes SDMA Buffer Boundary 3'h3: 32K bytes SDMA Buffer Boundary 3'h4: 64K bytes SDMA Buffer Boundary 3'h5: 128K bytes SDMA Buffer Boundary 3'h6: 256K bytes SDMA Buffer Boundary 3'h7: 512K bytes SDMA Buffer Boundary

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Bit	Attr	Reset Value	Description
11:0	RW	0x000	XFER_BLOCK_SIZE Transfer Block Size. These bits specify the block size of data transfers. In case of memory, it is set to 512 bytes. It can be accessed only if no transaction is executing. Read operations during transfers may return an invalid value, and write operations are ignored. Values: 12'h1: 1 byte 12'h2: 2 bytes 12'h3: 3 bytes ..... 12'h1FF: 511 byte 12'h200: 512 bytes ..... 12'h800: 2048 bytes Note: This register must be programmed with a non-zero value for data transfer.

EMMC_BLOCKCOUNT

Address: Operational Base(0xFF870000) + offset (0x0006)

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	BLOCK_CNT 16-bit Block Count. If the Host Version 4 Enable bit is set 0 or the 16-bit Block Count register is set to non-zero, the 16-bit Block Count register is selected. If the Host Version 4 Enable bit is set 1 and the 16-bit Block Count register is set to zero, the 32-bit Block Count register is selected. Values: 16'h0: Stop Count 16'h1: 1 Block 16'h2: 2 Blocks ..... 16'hFFFF: 65535 Blocks Note: For Host Version 4 Enable = 0, this register must be set to 0 before programming the 32-bit block count register when Auto CMD23 is enabled for non-DMA and ADMA modes.

EMMC_ARGUMENT

Address: Operational Base(0xFF870000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ARGUMENT Command Argument. These bits specify the SD/eMMC command argument that is specified in bits 39-8 of the Command format.

EMMC_XFER_MODE

Address: Operational Base(0xFF870000) + offset (0x000C)

Bit	Attr	Reset Value	Description
15:9	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
8	RW	0x0	RESP_INT_DISABLE Response Interrupt Disable. The Host Controller supports response check function to avoid overhead of response error check by the Host driver. Response types of only R1 and R5 can be checked by the Controller. If Host Driver checks the response error, set this bit to 0 and wait for Command Complete Interrupt and then check the response register. If the Host Controller checks the response error, set this bit to 1 and set the Response Error Check Enable bit to 1. The Command Complete Interrupt is disabled by this bit regardless of the Command Complete Signal Enable. Note: During tuning (when the Execute Tuning bit in the Host Control2 register is set), the Command Complete Interrupt is not generated irrespective of the Response Interrupt Disable setting. Values: 1'b0: Response Interrupt is enabled 1'b1: Response Interrupt is disabled
7	RW	0x0	RESP_ERR_CHK_ENABLE Response Error Check Enable. The Host Controller supports response check function to avoid overhead of response error check by Host driver. Response types of only R1 and R5 can be checked by the Controller. If the Host Controller checks the response error, set this bit to 1 and set Response Interrupt Disable to 1. If an error is detected, the Response Error interrupt is generated in the Error Interrupt Status register. Note: a. Response error check must not be enabled for any response type other than R1 and R5. b. Response check must not be enabled for the tuning command. Values: 1'b0: Response Error Check is disabled 1'b1: Response Error Check is enabled
6	RW	0x0	RESP_TYPE Response Type R1/R5. This bit selects either R1 or R5 as a response type when the Response Error Check is selected. Values: 1'b0: R1 1'b1: R5
5	RW	0x0	MULTI_BLK_SEL Multi/Single Block Select. This bit is set when issuing multiple-block transfer commands using the DAT line. If this bit is set to 0, it is not necessary to set the Block Count register. Values: 1'b0: Single Block 1'b1: Multiple Block

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Bit	Attr	Reset Value	Description
4	RW	0x0	DATA_XFER_DIR Data Transfer Direction Select. This bit defines the direction of DAT line data transfers. This bit is set to 1 by the Host Driver to transfer data from the SD/eMMC card to the Host Controller and it is set to 0 for all other commands. Values: 1'b0: Write (Host to Card) 1'b1: Read (Card to Host)
3:2	RW	0x0	AUTO_CMD_ENABLE Auto Command Enable. This field determines use of Auto Command functions. Values: 2'h0: Auto Command Disabled 2'h1: Auto CMD12 Enable 2'h2: Auto CMD23 Enable 2'h3: Auto CMD Auto Select
1	RW	0x0	BLOCK_COUNT_ENABLE Block Count Enable. This bit is used to enable the Block Count register, which is relevant for multiple block transfers. If this bit is set to 0, the Block Count register is disabled, which is useful in executing an infinite transfer. The Host Driver must set this bit to 0 when ADMA is used. Values: 1'b0: Disable 1'b1: Enable
0	RW	0x0	DMA_ENABLE DMA Enable. This bit enables the DMA functionality. If this bit is set to 1, a DMA operation begins when the Host Driver writes to the Command register. You can select one of the DMA modes by using DMA Select in the Host Control 1 register. Values: 1'b0: No data transfer or Non-DMA data transfer 1'b1: DMA Data transfer

EMMC_CMD

Address: Operational Base(0xFF870000) + offset (0x000E)

Bit	Attr	Reset Value	Description
15:14	RO	0x0	reserved
13:8	RW	0x00	CMD_INDEX Command Index. These bits are set to the command number that is specified in bits 45-40 of the command format.
7:6	RW	0x0	CMD_TYPE Command Type. These bits indicate the command type. Note: While issuing Abort CMD using CMD12/CMD52 or reset CMD using CMD0/CMD52, CMD_TYPE field shall be set to 0x3. Values: 2'h0: Normal 2'h1: Suspend 2'h2: Resume 2'h3: Abort

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Bit	Attr	Reset Value	Description
5	RW	0x0	DATA_PRESENT_SEL Data Present Select. This bit is set to 1 to indicate that data is present and that the data is transferred using the DAT line. This bit is set to 0 in the following instances: a. Command using the CMD line b. Command with no data transfer but using busy signal on the DAT[0] line c. Resume Command Values: 1'b0: No Data Present 1'b1: Data Present
4	RW	0x0	CMD_IDX_CHK_ENABLE Command Index Check Enable. This bit enables the Host Controller to check the index field in the response to verify if it has the same value as the command index. If the value is not the same, it is reported as a Command Index error. Note: a. Index check enable must be set to 0 for the command with no response, R2 response, R3 response and R4 response. b. For the tuning command, this bit must always be set to enable the index check. Values: 1'b0: Disable 1'b1: Enable
3	RW	0x0	CMD_CRC_CHK_ENABLE Command CRC Check Enable. This bit enables the Host Controller to check the CRC field in the response. If an error is detected, it is reported as a Command CRC error. Note: a. CRC check enable must be set to 0 for the command with no response, R3 response, and R4 response. b. For the tuning command, this bit must always be set to 1 to enable the CRC check. Values: 1'b0: Disable 1'b1: Enable
2	RW	0x0	SUB_CMD_FLAG Sub Command Flag. This bit distinguishes between a main command and a sub command. Values: 1'b0: Main Command 1'b1: Sub Command
1:0	RW	0x0	RESP_TYPE_SELECT Response Type Select. This bit indicates the type of response expected from the card. Values: 2'h0: No Response 2'h1: Response length 136 2'h2: Response length 48 2'h3: Response length 48, check Busy after response.

EMMC_RESP01

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Address: Operational Base(0xFF870000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RESP01 Command Response. These bits reflect 39-8 bits of SD/eMMC Response Field. Note: For Auto CMD, the 32-bit response (bits 39-8 of the Response Field) is updated in the RESP67 register.

EMMC_RESP23

Address: Operational Base(0xFF870000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RESP23 Command Response. These bits reflect 71-40 bits of the SD/eMMC Response Field.

EMMC_RESP45

Address: Operational Base(0xFF870000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	RESP45 Command Response. These bits reflect 103-72 bits of the Response Field.

EMMC_RESP67

Address: Operational Base(0xFF870000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RESP67 Command Response These bits reflect bits 135-104 of SD/EMMC Response Field. For Auto CMD, this register also reflects the 32-bit response (bits 39-8 of the Response Field).

EMMC_BUF_DATA

Address: Operational Base(0xFF870000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	BUF_DATA Buffer Data. These bits enable access to the Host Controller packet buffer.

EMMC_PSTATE

Address: Operational Base(0xFF870000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RO	0x1	SUB_CMD_STAT Sub Command Status. This bit is used to distinguish between a main command and a sub command status. Values: 1'b0: Main Command Status 1'b1: Sub Command Status

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Bit	Attr	Reset Value	Description
27	RO	0x1	CMD_ISSUE_ERR Command Not Issued by Error. This bit is set if a command cannot be issued after setting the command register due to an error except the Auto CMD12 error. Values: 1'b0: No error for issuing a command 1'b1: Command cannot be issued
26:25	RO	0x0	reserved
24	RO	0x1	CMD_LINE_LVL Command-Line Signal Level. This bit is used to check the CMD line level to recover from errors and for debugging.
23:20	RO	0xf	DAT_3_0 DAT[3:0] Line Signal Level. This bit is used to check the DAT line level to recover from errors and for debugging.
19	RO	0x1	WR_PROTECT_SW_LVL Write Protect Switch Pin Level. This bit is supported only for memory and combo cards. Values: 1'b0: Write protected 1'b1: Write enabled
18	RO	0x1	CARD_DETECT_PIN_LEVEL Card Detect Pin Level. Values: 1'b0: No card present 1'b1: Card Present
17	RO	0x1	CARD_STABLE Card Stable. This bit indicates the stability of the Card Detect Pin Level. A card is not detected if this bit is set to 1 and the value of the CARD_INSERTED bit is 0. Values: 1'b0: Reset or Debouncing 1'b1: No Card or Inserted
16	RO	0x1	CARD_INSERTED Card Inserted. This bit indicates whether a card has been inserted. The Host Controller debounces this signal so that Host Driver need not wait for it to stabilize. Values: 1'b0: Reset, Debouncing, or No card 1'b1: Card Inserted
15:12	RO	0x0	reserved
11	RO	0x0	BUF_RD_ENABLE Buffer Read Enable. This bit is used for non-DMA transfers. This bit is set if valid data exists in the Host buffer. Values: 1'b0: Read disable 1'b1: Read enable

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Bit	Attr	Reset Value	Description
10	RO	0x0	BUF_WR_ENABLE Buffer Write Enable. This bit is used for non-DMA transfers. This bit is set if space is available for writing data. Values: 1'b0: Write disable 1'b1: Write enable
9	RW	0x0	RD_XFER_ACTIVE Read Transfer Active. This bit indicates whether a read transfer is active for SD/eMMC mode. Values: 1'b0: No valid data 1'b1: Transferring data
8	RO	0x0	WR_XFER_ACTIVE Write Transfer Active. This status indicates whether a write transfer is active for SD/eMMC mode. Values: 1'b0: No valid data 1'b1: Transferring data
7:4	RO	0x0	DAT_7_4 DAT[7:4] Line Signal Level. This bit is used to check the DAT line level to recover from errors and for debugging.
3	RO	0x0	RE_TUNE_REQ Re-Tuning Request. Host Controller does not generate retuning request. The software must maintain the Retuning timer.
2	RO	0x0	DAT_LINE_ACTIVE DAT Line Active (SD/eMMC Mode only). This bit indicates whether one of the DAT lines on the SD/eMMC bus is in use. In the case of read transactions, this bit indicates whether a read transfer is executing on the SD/eMMC bus. In the case of write transactions, this bit indicates whether a write transfer is executing on the SD/eMMC bus. For a command with busy, this status indicates whether the command executing busy is executing on an SD/eMMC bus. Values: 1'b0: DAT Line Inactive 1'b1: DAT Line Active
1	RO	0x0	CMD_INHIBIT_DAT Command Inhibit (DAT). This bit is applicable for SD/eMMC mode and is generated if either DAT line active or Read transfer active is set to 1. If this bit is set to 0, it indicates that the Host Controller can issue subsequent SD/eMMC commands. Values: 1'b0: Can issue command which used DAT line 1'b1: Cannot issue command which used DAT line

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Bit	Attr	Reset Value	Description
0	RO	0x0	CMD_INHIBIT Command Inhibit (CMD). If this bit is set to 0, it indicates that the CMD line is not in use and the Host controller can issue an SD/eMMC command using the CMD line. This bit is set when the command register is written. This bit is cleared when the command response is received. This bit is not cleared by the response of auto CMD12/23 but cleared by the response of read/write command. Values: 1'b0: Host Controller is ready to issue a command 1'b1: Host Controller is not ready to issue a command

EMMC_HOST_CTRL1

Address: Operational Base(0xFF870000) + offset (0x0028)

Bit	Attr	Reset Value	Description
7	RW	0x0	CARD_DETECT_SIG_SEL Card Detect Signal Selection. This bit selects a source for card detection. When the source for the card detection is switched, the interrupt must be disabled during the switching period. Values: 1'b0: Card Detect Signal is selected (for normal use) 1'b1: Card Detect Test Level is selected (for test purpose)
6	RW	0x0	CARD_DETECT_TEST_LVL Card Detect Test Level. This bit is enabled while the Card Detect Signal Selection is set to 1 and it indicates whether a card inserted or not. Values: 1'b0: No Card 1'b1: Card Inserted
5	RW	0x0	EXT_DAT_XFER Extended Data Transfer Width. This bit controls 8-bit bus width mode of embedded device. Values: 1'b0: Bus Width is selected by the Data Transfer Width 1'b1: 8-bit Bus Width
4:3	RW	0x0	DMA_SEL DMA Select. This field is used to select the DMA type. When Host Version 4 Enable is 1 in Host Control 2 register: 2'h0: SDMA is selected 2'h1: Reserved 2'h2: ADMA2 is selected 2'h3: ADMA2 or ADMA3 is selected When Host Version 4 Enable is 0 in Host Control 2 register: 2'h0: SDMA is selected 2'h1: Reserved 2'h2: 32-bit Address ADMA2 is selected 2'h3: Reserved Values: 2'h0: SDMA is selected 2'h1: Reserved 2'h2: ADMA2 is selected 2'h3: ADMA2 or ADMA3 is selected

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Bit	Attr	Reset Value	Description
2	RW	0x0	HIGH_SPEED_EN High Speed Enable. In SD/eMMC mode, this bit is used to determine the selection of pre-set value for High Speed mode. Before setting this bit, the Host Driver checks the High Speed Support in the Capabilities register. Values: 1'b0: Normal Speed mode 1'b1: High Speed mode
1	RW	0x0	DAT_XFER_WIDTH Data Transfer Width. For SD/eMMC mode, this bit selects the data transfer width of the Host Controller. The Host Driver sets it to match the data width of the SD/eMMC card. Values: 1'b0: 1-bit mode 1'b1: 4-bit mode
0	RO	0x0	reserved

EMMC_PWR_CTRL

Address: Operational Base(0xFF870000) + offset (0x0029)

Bit	Attr	Reset Value	Description
7:1	RO	0x00	reserved
0	RW	0x0	SD_BUS_PWR If this bit is cleared, the Host Controller stops the SD Clock by clearing the SD_CLK_IN bit in the EMMC_CLK_CTRL register. Values: 1'b0: Power off 1'b1: Power on

EMMC_BGAP_CTRL

Address: Operational Base(0xFF870000) + offset (0x002A)

Bit	Attr	Reset Value	Description
7:4	RO	0x0	reserved
3	RW	0x0	INT_AT_BGAP Interrupt At Block Gap. This bit is valid only in the 4-bit mode of an SDIO card and is used to select a sample point in the interrupt cycle. Setting to 1 enables interrupt detection at the block gap for a multiple block transfer.
2	RW	0x0	RD_WAIT_CTRL Read Wait Control. This bit is used to enable the read wait protocol to stop read data using DAT[2] line if the card supports read wait. Otherwise, the Host Controller has to stop the card clock to hold the read data. Values: 1'b0: Disable Read Wait Control 1'b1: Enable Read Wait Control

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Bit	Attr	Reset Value	Description
1	RW	0x0	CONTINUE_REQ Continue Request. This bit is used to restart the transaction, which was stopped using the Stop At Block Gap Request. The Host Controller automatically clears this bit when the transaction restarts. If stop at block gap request is set to 1, any write to this bit is ignored. Values: 1'b0: No Affect 1'b1: Restart
0	RW	0x0	STOP_BG_REQ Stop At Block Gap Request. This bit is used to stop executing read and write transactions at the next block gap for non-DMA, SDMA, and ADMA transfers. Values: 1'b0: Transfer 1'b1: Stop

EMMC_CLK_CTRL

Address: Operational Base(0xFF870000) + offset (0x002C)

Bit	Attr	Reset Value	Description
15:8	RW	0x00	FREQ_SEL SDCLK Frequency Select. These bits specify the lower 8 bits of 10-bit SDCLK Frequency Select control. These bits are used to select the frequency of the SDCLK signal. These bits depend on setting of Preset Value Enable in the Host Control 2 register. If Preset Value Enable = 0, these bits are set by the Host Driver. If Preset Value Enable = 1, these bits are automatically set to a value specified in one of the Preset Value register. 1. 10-bit Divided Clock Mode: 10'h000: Base clock (10MHz - 255 MHz) 10'h001: 1/2 Divided Clock 10'h002: 1/4 Divided Clock ..... 10'h3ff: 1/2046 Divided clock 2. Programmable Clock Mode: 10'h000: Base clock * M 10'h001: Base clock * M /2 10'h002: Base clock * M /3 ..... 10'h3ff: Base clock * M /1024
7:6	RW	0x0	UPPER_FREQ_SEL These bits specify the upper 2 bits of 10-bit SDCLK Frequency Select control.
5	RW	0x0	CLK_GEN_SELECT Clock Generator Select. This bit is used to select the clock generator mode in SDCLK Frequency Select. If Preset Value Enable = 0, this bit is set by the Host Driver. If Preset Value Enable = 1, this bit is automatically set to a value specified in one of the Preset Value registers. Values: 1'b0: Divided Clock Mode 1'b1: Programmable Clock Mode
4:3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2	RW	0x0	SD_CLK_EN SD/eMMC Clock Enable. This bit stops the SDCLK when set to 0. The SDCLK Frequency Select bit can be changed when this bit is set to 0. Values: 1'b0: Disable providing SDCLK 1'b1: Enable providing SDCLK
1	RO	0x0	INTERNAL_CLK_STABLE Internal Clock Stable. Values: 1'b0: Not Ready 1'b1: Ready
0	RW	0x0	INTERNAL_CLK_EN Internal Clock Enable. This bit is set to 0 when the Host Driver is not using the Host Controller. The Host Controller must stop its internal clock to enter a very low power state. However, registers can still be read and written to. Note: If this bit is not used to control the internal clock (base clock and master clock), it is recommended to set this bit to 1. Values: 1'b0: Stop 1'b1: Oscillate

EMMC_TOUT_CTRL

Address: Operational Base(0xFF870000) + offset (0x002E)

Bit	Attr	Reset Value	Description
7:4	RO	0x0	reserved
3:0	RW	0x0	TOUT_CNT Data Timeout Counter Value. This value determines the interval by which DAT line timeouts are detected. Timeout clock frequency will be generated by dividing the base clock TMCLK by this value. When setting this register, prevent inadvertent timeout events by clearing the Data Timeout Error Status Enable (in the Error Interrupt Status Enable register). Values: 4'h0: TMCLK * 2^13 4'h1: TMCLK * 2^14 ..... 4'he: TMCLK * 2^27 4'hf: Reserved

EMMC_SW_RST

Address: Operational Base(0xFF870000) + offset (0x002F)

Bit	Attr	Reset Value	Description
7:3	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
2	RW	0x0	SW_RST_DAT Software Reset for DAT line. This bit is used in SD/eMMC mode and it resets only a part of the data circuit and the DMA circuit is also reset. The following registers and bits are cleared by this bit: a. Buffer Data Port register: Buffer is cleared and initialized. b. Present state register: Buffer Read Enable Buffer Write Enable Read Transfer Active Write Transfer Active DAT Line Active Command Inhibit (DAT) c. Block Gap Control register: Continue Request Stop At Block Gap Request d. Normal Interrupt status register: Buffer Read Ready Buffer Write Ready DMA Interrupt Block Gap Event Transfer Complete Values: 1'b0: Work 1'b1: Reset
1	RW	0x0	SW_RST_CMD Software Reset for CMD line. This bit resets only a part of the command circuit to be able to issue a command. This reset is effective only for a command issuing circuit (including response error statuses related to Command Inhibit (CMD) control) and does not affect the data transfer circuit. Host Controller can continue data transfer even after this reset is executed while handling subcommand-response errors. The following registers and bits are cleared by this bit: a. Present State register - Command Inhibit (CMD) bit b. Normal Interrupt Status register - Command Complete bit c. Error Interrupt Status - Response error statuses related to Command Inhibit (CMD) bit Values: 1'b0: Work 1'b1: Reset
0	RW	0x0	SW_RST_ALL Software Reset for All. This reset affects the entire Host Controller except for the card detection circuit. During its initialization, the Host Driver sets this bit to 1 to reset the Host Controller. All registers are reset except the capabilities register. If this bit is set to 1, the Host Driver must issue reset command and reinitialize the card. Values: 1'b0: Work 1'b1: Reset

EMMC_NORMAL_INT_STAT

Address: Operational Base(0xFF870000) + offset (0x0030)

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Bit	Attr	Reset Value	Description
15	RO	0x0	ERROR_INT_STAT Error Interrupt. If any of the bits in the Error Interrupt Status register are set, then this bit is set. Values: 1'b0: No Error 1'b1: Error
14	RC/W1C	0x0	CQE_EVENT Command Queuing Event. This status is set if Command Queuing/Crypto related event has occurred in eMMC/SD mode. Read CQHCI's CQIS/CRNQIS register for more details. Values: 1'b0: No Event 1'b1: Command Queuing Event is detected Writes to this bit clear it. Value of 1 clears bit and 0 leaves bit intact.
13	RO	0x0	FX_EVENT FX Event. This status is set when R[14] of response register is set to 1 and Response Type R1/R5 is set to 0 in Transfer Mode register. This interrupt is used with response check function. Values: 1'b0: No Event 1'b1: FX Event is detected
12	RO	0x0	RE_TUNE_EVENT Re-tuning Event. This bit is set if the Re-Tuning Request changes from 0 to 1. Re-Tuning request is not supported.
11:9	RO	0x0	reserved
8	RO	0x0	CARD_INTERRUPT Card Interrupt. This bit reflects the synchronized value of DAT[1] Interrupt Input for SD Mode. Values: 1'b0: No Card Interrupt 1'b1: Generate Card Interrupt
7	RC/W1C	0x0	CARD_REMOVAL Card Removal. This bit is set if the Card Inserted in the Present State register changes from 1 to 0. Values: 1'b0: Card state stable or Debouncing 1'b1: Card Removed Writes to this bit clear it. Value of 1 clears bit and 0 leaves bit intact.
6	RC/W1C	0x0	CARD_INSERTION Card Insertion. This bit is set if the Card Inserted in the Present State register changes from 0 to 1. Values: 1'b0: Card state stable or Debouncing 1'b1: Card Inserted Writes to this bit clear it. Value of 1 clears bit and 0 leaves bit intact.

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Bit	Attr	Reset Value	Description
5	RC/W1C	0x0	BUF_RD_READY Buffer Read Ready. This bit is set if the Buffer Read Enable changes from 0 to 1. Values: 1'b0: Not ready to read buffer 1'b1: Ready to read buffer Writes to this bit clear it. Value of 1 clears bit and 0 leaves bit intact.
4	RC/W1C	0x0	BUF_WR_READY Buffer Write Ready. This bit is set if the Buffer Write Enable changes from 0 to 1. Values: 1'b0: Not ready to write buffer 1'b1: Ready to write buffer Writes to this bit clear it. Value of 1 clears bit and 0 leaves bit intact.
3	RC/W1C	0x0	DMA_INTERRUPT DMA Interrupt. This bit is set if the Host Controller detects the SDMA Buffer Boundary during transfer. In case of ADMA, by setting the Int field in the descriptor table, the Host controller generates this interrupt. This interrupt is not generated after a Transfer Complete. Values: 1'b0: No DMA Interrupt 1'b1: DMA Interrupt is generated Writes to this bit clear it. Value of 1 clears bit and 0 leaves bit intact.
2	RC/W1C	0x0	BGAP_EVENT Block Gap Event. This bit is set when both read/write transaction is stopped at block gap due to a Stop at Block Gap Request. Values: 1'b0: No Block Gap Event 1'b1: Transaction stopped at block gap Writes to this bit clear it. Value of 1 clears bit and 0 leaves bit intact.
1	RC/W1C	0x0	XFER_COMPLETE Transfer Complete. This bit is set when a read/write transfer and a command with status busy is completed. Values: 1'b0: Not complete 1'b1: Command execution is completed Writes to this bit clear it. Value of 1 clears bit and 0 leaves bit intact.

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Bit	Attr	Reset Value	Description
0	RC/W1C	0x0	CMD_COMPLETE Command Complete. In an SD/eMMC Mode, this bit is set when the end bit of a response except for Auto CMD12 and Auto CMD23. This interrupt is not generated when the Response Interrupt Disable in Transfer Mode Register is set to 1. Values: 1'b0: No Command Complete 1'b1: Command Complete Writes to this bit clear it. Value of 1 clears bit and 0 leaves bit intact.

EMMC_ERROR_INT_STAT

Address: Operational Base(0xFF870000) + offset (0x0032)

Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12	RC/W1C	0x0	BOOT_ACK_ERR Boot Acknowledgement Error. This bit is set when there is a timeout for boot acknowledgement or when detecting boot acknowledgement status having a value other than 3'b010. This is applicable only when boot acknowledgement is expected in eMMC mode. Values: 1'b0: No Error 1'b1: Error
11	RC/W1C	0x0	RESP_ERR Response Error Host Controller Version 4.00 supports response error check function to avoid overhead of response error check by Host Driver during DMA execution. If Response Error Check Enable is set to 1 in the Transfer Mode register, Host Controller Checks R1 or R5 response. If an error is detected in a response, this bit is set to 1. Values: 1'b0: No Error 1'b1: Error
10	RC/W1C	0x0	TUNING_ERR Tuning Error. This bit is set when an unrecoverable error is detected in a tuning circuit except during the tuning procedure (occurrence of an error during tuning procedure is indicated by Sampling Clock Select in the Host Control 2 register). By detecting Tuning Error, Host Driver needs to abort a command executing and perform tuning. To reset tuning circuit, Sampling Clock Select is set to 0 before executing tuning procedure. The Tuning Error is higher priority than the other error interrupts generated during data transfer. By detecting Tuning Error, the Host Driver must discard data transferred by a current read/write command and retry data transfer after the Host Controller retrieved from the tuning circuit error. Values: 1'b0: No Error 1'b1: Error

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Bit	Attr	Reset Value	Description
9	RC/W1C	0x0	ADMA_ERR ADMA Error. This bit is set when the Host Controller detects error during ADMA-based data transfer. The error could be due to following reasons: a. Error response received from System bus b. ADMA3, ADMA2 Descriptors invalid c. CQE Task or Transfer descriptors invalid When the error occurs, the state of the ADMA is saved in the ADMA Error Status register. In eMMC CQE mode: The Host Controller generates this Interrupt when it detects an invalid descriptor data at the Fetch Descriptor state. ADMA Error State in the ADMA Error Status indicates that an error has occurred in Fetch Descriptor state. The Host Driver may find that Valid bit is not set at the error descriptor. Values: 1'b0: No Error 1'b1: Error
8	RC/W1C	0x0	AUTO_CMD_ERR Auto CMD Error. This error status is used by Auto CMD12 and Auto CMD23 in SD/eMMC mode. This bit is set when detecting that any of the bits D00 to D05 in Auto CMD Error Status register has changed from 0 to 1. D07 is effective in case of Auto CMD12. Auto CMD Error Status register is valid while this bit is set to 1 and may be cleared by clearing of this bit. Values: 1'b0: No Error 1'b0: Error
7	RO	0x0	reserved
6	RC/W1C	0x0	DATA_END_BIT_ERR Data End Bit Error. This error occurs in SD/eMMC mode either when detecting 0 at the end bit position of read data that uses the DAT line or at the end bit position of the CRC status. Values: 1'b0: No Error 1'b1: Error
5	RC/W1C	0x0	DATA_CRC_ERR Data CRC Error. This error occurs in SD/eMMC mode when detecting CRC error when transferring read data which uses the DAT line, when detecting the Write CRC status having a value of other than 010 or when write CRC status timeout. Values: 1'b0: No Error 1'b1: Error

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Bit	Attr	Reset Value	Description
4	RC/W1C	0x0	DATA_TOUT_ERR Data Timeout Error. This bit is set in SD/eMMC mode when detecting one of the following timeout conditions: a. Busy timeout for R1b, R5b type b. Busy timeout after Write CRC status c. Write CRC Status timeout d. Read Data timeout Values: 1'b0: No Error 1'b1: Time out
3	RC/W1C	0x0	CMD_IDX_ERR Command Index Error. This bit is set if a Command Index error occurs in the command response in SD/eMMC mode. Values: 1'b0: No Error 1'b1: Error
2	RC/W1C	0x0	CMD_END_BIT_ERR Command End Bit Error. This bit is set when detecting that the end bit of a command response is 0 in SD/eMMC mode. Values: 1'b0: No Error 1'b1: End Bit Error generated
1	RC/W1C	0x0	CMD_CRC_ERR Command CRC Error. Command CRC Error is generated in SD/eMMC mode for following two cases. a. If a response is returned and the Command Timeout Error is set to 0 (indicating no timeout), this bit is set to 1 when detecting a CRC error in the command response. b. The Host Controller detects a CMD line conflict by monitoring the CMD line when a command is issued. If the Host Controller drives the CMD line to 1 level, but detects 0 level on the CMD line at the next SD clock edge, then the Host Controller aborts the command (stop driving CMD line) and set this bit to 1. The Command Timeout Error is also set to 1 to distinguish a CMD line conflict. Values: 1'b0: No Error 1'b1: CRC Error generated
0	RC/W1C	0x0	CMD_TOUT_ERR Command Timeout Error. In SD/eMMC Mode, this bit is set only if no response is returned within 64 SD clock cycles from the end bit of the command. If the Host Controller detects a CMD line conflict, along with Command CRC Error bit, this bit is set to 1, without waiting for 64 SD/eMMC card clock cycles. Values: 1'b0: No Error 1'b1: Time out

EMMC_NORMAL_INT_STAT_EN

Address: Operational Base(0xFF870000) + offset (0x0034)

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Bit	Attr	Reset Value	Description
15	RO	0x0	reserved
14	RW	0x0	CQE_EVENT_STAT_EN CQE Event Status Enable. Values: 1'b0: Masked 1'b1: Enabled
13:9	RO	0x00	reserved
8	RW	0x0	CARD_INTERRUPT_STAT_EN Card Interrupt Status Enable. Values: 1'b0: Masked 1'b1: Enabled
7	RW	0x0	CARD_REMOVAL_STAT_EN Card Removal Status Enable. Values: 1'b0: Masked 1'b1: Enabled
6	RW	0x0	CARD_INSERTION_STAT_EN Card Insertion Status Enable. Values: 1'b0: Masked 1'b1: Enabled
5	RW	0x0	BUF_RD_READY_STAT_EN Buffer Read Ready Status Enable. Values: 1'b0: Masked 1'b1: Enabled
4	RW	0x0	BUF_WR_READY_STAT_EN Buffer Write Ready Status Enable. Values: 1'b0: Masked 1'b1: Enabled
3	RW	0x0	DMA_INTERRUPT_STAT_EN DMA Interrupt Status Enable. Values: 1'b0: Masked 1'b1: Enabled
2	RW	0x0	BGAP_EVENT_STAT_EN Block Gap Event Status Enable. Values: 1'b0: Masked 1'b1: Enabled
1	RW	0x0	XFER_COMPLETE_STAT_EN Transfer Complete Status Enable. Values: 1'b0: Masked 1'b1: Enabled
0	RW	0x0	CMD_COMPLETE_STAT_EN Command Complete Status Enable. Values: 1'b0: Masked 1'b1: Enabled

EMMC_ERROR_INT_STAT_EN

Address: Operational Base(0xFF870000) + offset (0x0036)

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Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12	RW	0x0	BOOT_ACK_ERR_STAT_EN Boot Acknowledgment Error Status Enable.. Values: 1'b0: Masked 1'b1: Enabled
11	RW	0x0	RESP_ERR_STAT_EN Response Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled
10	RW	0x0	TUNING_ERR_STAT_EN Tuning Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled
9	RW	0x0	ADMA_ERR_STAT_EN ADMA Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled
8	RW	0x0	AUTO_CMD_ERR_STAT_EN Auto CMD Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled
7	RO	0x0	reserved
6	RW	0x0	DATA_END_BIT_ERR_STAT_EN Data End Bit Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled
5	RW	0x0	DATA_CRC_ERR_STAT_EN Data CRC Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled
4	RW	0x0	DATA_TOUT_ERR_STAT_EN Data Timeout Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled
3	RW	0x0	CMD_IDX_ERR_STAT_EN Command Index Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled
2	RW	0x0	CMD_END_BIT_ERR_STAT_EN Command End Bit Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled

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Bit	Attr	Reset Value	Description
1	RW	0x0	CMD_CRC_ERR_STAT_EN Command CRC Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled
0	RW	0x0	CMD_TOUT_ERR_STAT_EN Command Timeout Error Status Enable. Values: 1'b0: Masked 1'b1: Enabled

EMMC_NORMAL_INT_SIGNAL_EN

Address: Operational Base(0xFF870000) + offset (0x0038)

Bit	Attr	Reset Value	Description
15	RO	0x0	reserved
14	RW	0x0	CQE_EVENT_SIGNAL_EN CQE Event Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
13:9	RO	0x00	reserved
8	RW	0x0	CARD_INTERRUPT_SIGNAL_EN Card Interrupt Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
7	RW	0x0	CARD_REMOVAL_SIGNAL_EN Card Removal Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
6	RW	0x0	CARD_INSERTION_SIGNAL_EN Card Insertion Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
5	RW	0x0	BUF_RD_READY_SIGNAL_EN Buffer Read Ready Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
4	RW	0x0	BUF_WR_READY_SIGNAL_EN Buffer Write Ready Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
3	RW	0x0	DMA_INTERRUPT_SIGNAL_EN DMA Interrupt Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
2	RW	0x0	BGAP_EVENT_SIGNAL_EN Block Gap Event Signal Enable. Values: 1'b0: Masked 1'b1: Enabled

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Bit	Attr	Reset Value	Description
1	RW	0x0	XFER_COMPLETE_SIGNAL_EN Transfer Complete Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
0	RW	0x0	CMD_COMPLETE_SIGNAL_EN Command Complete Signal Enable. Values: 1'b0: Masked 1'b1: Enabled

EMMC_ERROR_INT_SIGNAL_EN

Address: Operational Base(0xFF870000) + offset (0x003A)

Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12	RW	0x0	BOOT_ACK_ERR_SIGNAL_EN Boot Acknowledgment Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
11	RW	0x0	RESP_ERR_SIGNAL_EN Response Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
10	RW	0x0	TUNING_ERR_SIGNAL_EN Tuning Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
9	RW	0x0	ADMA_ERR_SIGNAL_EN ADMA Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
8	RW	0x0	AUTO_CMD_ERR_SIGNAL_EN Auto CMD Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
7	RO	0x0	reserved
6	RW	0x0	DATA_END_BIT_ERR_SIGNAL_EN Data End Bit Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
5	RW	0x0	DATA_CRC_ERR_SIGNAL_EN Data CRC Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
4	RW	0x0	DATA_TOUT_ERR_SIGNAL_EN Data Timeout Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled

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Bit	Attr	Reset Value	Description
3	RW	0x0	CMD_IDX_ERR_SIGNAL_EN Command Index Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
2	RW	0x0	CMD_END_BIT_ERR_SIGNAL_EN Command End Bit Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
1	RW	0x0	CMD_CRC_ERR_SIGNAL_EN Command CRC Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled
0	RW	0x0	CMD_TOUT_ERR_SIGNAL_EN Command Timeout Error Signal Enable. Values: 1'b0: Masked 1'b1: Enabled

EMMC_AUTO_CMD_STAT

Address: Operational Base(0xFF870000) + offset (0x003C)

Bit	Attr	Reset Value	Description
15:8	RO	0x00	reserved
7	RO	0x0	CMD_NOT_ISSUED_AUTO_CMD12 Command Not Issued By Auto CMD12 Error. If this bit is set to 1, CMD_wo_DAT is not executed due to an Auto CMD12 Error (D04-D01) in this register. This bit is set to 0 when Auto CMD Error is generated by Auto CMD23. Values: 1'b0: No Error 1'b1: Not Issued
6	RO	0x0	reserved
5	RO	0x0	AUTO_CMD_RESP_ERR Auto CMD Response Error. This bit is set when Response Error Check Enable in the Transfer Mode register is set to 1 and an error is detected in R1 response of either Auto CMD12 or CMD13. This status is ignored if any bit between D00 to D04 is set to 1. Values: 1'b0: No Error 1'b1: Error
4	RO	0x0	AUTO_CMD_IDX_ERR Auto CMD Index Error. This bit is set if the command index error occurs in response to a command. Values: 1'b0: No Error 1'b1: Error

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Bit	Attr	Reset Value	Description
3	RO	0x0	AUTO_CMD_EBIT_ERR Auto CMD End Bit Error. This bit is set when detecting that the end bit of command response is 0. Values: 1'b0: No Error 1'b1: End Bit Error Generated
2	RO	0x0	AUTO_CMD_CRC_ERR Auto CMD CRC Error. This bit is set when detecting a CRC error in the command response. Values: 1'b0: No Error 1'b1: CRC Error Generated
1	RO	0x0	AUTO_CMD_TOUT_ERR Auto CMD Timeout Error. This bit is set if no response is returned with 64 SDCLK cycles from the end bit of the command. If this bit is set to 1, error status bits (D04-D01) are meaningless. Values: 1'b0: No Error 1'b1: Time out
0	RO	0x0	AUTO_CMD12_NOT_EXEC Auto CMD12 Not Executed. If multiple memory block data transfer is not started due to a command error, this bit is not set because it is not necessary to issue an Auto CMD12. Setting this bit to 1 means that the Host Controller cannot issue Auto CMD12 to stop multiple memory block data transfer, due to some error. If this bit is set to 1, error status bits (D04-D01) is meaningless. This bit is set to 0 when Auto CMD Error is generated by Auto CMD23. Values: 1'b0: Executed 1'b1: Not Executed

EMMC_HOST_CTRL2

Address: Operational Base(0xFF870000) + offset (0x003E)

Bit	Attr	Reset Value	Description
15	RW	0x0	PRESET_VAL_ENABLE Preset Value Enable. This bit enables automatic selection of SDCLK frequency and Driver strength Preset Value registers. When Preset Value Enable is set, SDCLK frequency generation (Frequency Select and Clock Generator Select) and the driver strength selection are performed by the controller. These values are selected from set of Preset Value registers based on selected speed mode. Values: 1'b0: SDCLK and Driver Strength are controlled by Host Driver 1'b1: Automatic Selection by Preset Value are Enabled

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Bit	Attr	Reset Value	Description
14	RW	0x0	ASYNC_INT_ENABLE Asynchronous Interrupt Enable. This bit can be set if a card supports asynchronous interrupts and Asynchronous Interrupt Support is set to 1 in the Capabilities register. Values: 1'b0: Disabled 1'b1: Enabled
13	RW	0x0	ADDRESSING 64-bit Addressing. This bit is effective when Host Version 4 Enable is set to 1. Values: 1'b0: 32 bits addressing 1'b1: 64 bits addressing
12	RW	0x0	HOST_VER4_ENABLE Host Version 4 Enable. This bit selects either Version 3.00 compatible mode or Version 4 mode. Values: 1'b0: Version 3.00 compatible mode 1'b1: Version 4 mode
11	RW	0x0	CMD23_ENABLE CMD23 Enable. If the card supports CMD23, this bit is set to 1. This bit is used to select Auto CMD23 or Auto CMD12 for ADMA3 data transfer. Values: 1'b0: Auto CMD23 is disabled 1'b1: Auto CMD23 is enabled
10	RW	0x0	ADMA2_LEN_MODE ADMA2 Length Mode. This bit selects ADMA2 Length mode to be either 16-bit or 26-bit. Values: 1'b0: 16-bit Data Length Mode 1'b1: 26-bit Data Length Mode
9	RO	0x0	reserved
8	RW	0x0	UHS2_IF_ENABLE This bit should be set to 0 for SD/eMMC Interface.
7	RW	0x0	SAMPLE_CLK_SEL Sampling Clock Select. This bit is used by the Host Controller to select the sampling clock in SD/eMMC mode to receive CMD and DAT. This bit is set by the tuning procedure and is valid after the completion of tuning (when Execute Tuning is cleared). Setting this bit to 1 means that tuning is completed successfully and setting this bit to 0 means that tuning has failed. Values: 1'b0: Fixed clock is used to sample data 1'b1: Tuned clock is used to sample data
6	RW	0x0	EXEC_TUNING Execute Tuning. This bit is set to 1 to start the tuning procedure in SD/eMMC speed modes and this bit is automatically cleared when tuning procedure is completed. Values: 1'b0: Not Tuned or Tuning completed 1'b1: Execute Tuning

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Bit	Attr	Reset Value	Description
5:4	RO	0x0	reserved
3	RW	0x0	SIGNALING_EN 1.8V Signalling Enable. Values: 1'b0: 3.3V Signalling 1'b1: 1.8V Signalling
2:0	RW	0x0	UHS_MODE_SEL UHS Mode/eMMC Speed Mode Select. These bits are used to select UHS mode in the SD mode of operation. In eMMC mode, these bits are used to select eMMC Speed mode. Values: UHS Mode: 3'h0: SDR12 3'h1: SDR25 3'h2: SDR50 3'h3: SDR104 3'h4: DDR50 Others: Reserved eMMC Mode: 3'h0: Legacy 3'h1: High Speed SDR 3'h3: HS200 3'h4: High Speed DDR 3'h7: HS400 Others: Reserved

EMMC_CAPABILITIES1

Address: Operational Base(0xFF870000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:30	RO	0x1	SLOT_TYPE Slot Type. These bits indicate usage of a slot by a specific Host System. 2'h0: Removable Card Slot 2'h1: Embedded Slot for One Device 2'h2: Shared Bus Slot (SD mode) 2'h3: Reserved
29	RO	0x0	ASYNC_INT_SUPPORT Asynchronous Interrupt Support (SD Mode only). Values: 1'b0: Asynchronous Interrupt Not Supported 1'b1: Asynchronous Interrupt Supported
28	RO	0x0	SYS_ADDR_64_V3 64-bit System Address Support for V3. This bit sets the Host controller to support 64-bit System Addressing of V3 mode. SDMA cannot be used in 64-bit Addressing in Version 3 Mode. If this bit is set to 1, 64-bit ADMA2 with using 96-bit Descriptor can be enabled by setting Host Version 4 Enable (HOST_VER4_ENABLE = 0) and DMA select (DMA_SEL =11b). Values: 1'b0: 64-bit System Address for V3 is Not Supported 1'b1: 64-bit System Address for V3 is Supported

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Bit	Attr	Reset Value	Description
27	RO	0x0	SYS_ADDR_64_V4 64-bit System Address Support for V4. This bit sets the Host Controller to support 64-bit System Addressing of V4 mode. When this bit is set to 1, full or part of 64-bit address must be used to decode the Host Controller Registers so that Host Controller Registers can be placed above system memory area. 64-bit address decode of Host Controller registers is effective regardless of setting to 64-bit Addressing in Host Control 2. If this bit is set to 1, 64-bit DMA Addressing for version 4 is enabled by setting Host Version 4 Enable (HOST_VER4_ENABLE = 1) and by setting 64-bit Addressing (ADDRESSING =1) in the Host Control 2 register. SDMA can be used and ADMA2 uses 128-bit Descriptor. Values: 1'b0: 64-bit System Address for V4 is Not Supported 1'b1: 64-bit System Address for V4 is Supported
26:24	RO	0x0	reserved
23	RO	0x1	SUS_RES_SUPPORT Suspense/Resume Support. This bit indicates whether the Host Controller supports Suspend/Resume functionality. If this bit is 0, the Host Driver does not issue either Suspend or Resume commands because the Suspend and Resume mechanism is not supported. Values: 1'b0: Not Supported 1'b1: Supported
22	RO	0x1	SDMA_SUPPORT SDMA Support. This bit indicates whether the Host Controller is capable of using SDMA to transfer data between the system memory and the Host Controller directly. Values: 1'b0: SDMA not Supported 1'b1: SDMA Supported
21	RO	0x1	HIGH_SPEED_SUPPORT High Speed Support. This bit indicates whether the Host Controller and the Host System supports High Speed mode and they can supply the SD Clock frequency from 25 MHz to 50 MHz. Values: 1'b0: High Speed not Supported 1'b1: High Speed Supported
20	RO	0x0	reserved
19	RO	0x1	ADMA2_SUPPORT ADMA2 Support. This bit indicates whether the Host Controller is capable of using ADMA2. Values: 1'b0: ADMA2 not Supported 1'b1: ADMA2 Supported

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Bit	Attr	Reset Value	Description
18	RO	0x1	EMBEDDED_8_BIT 8-bit Support for Embedded Device. This bit indicates whether the Host Controller is capable of using an 8-bit bus width mode. Values: 1'b0: 8-bit Bus Width not Supported 1'b1: 8-bit Bus Width Supported
17:16	RO	0x1	MAX_BLK_LEN Maximum Block Length. This bit indicates the maximum block size that the Host driver can read and write to the buffer in the Host Controller. The buffer transfers this block size without wait cycles. The transfer block length is always 512 bytes for the SD Memory irrespective of this bit. Values: 2'h0: 512 Byte 2'h1: 1024 Byte 2'h2: 2048 Byte 2'h3: Reserved
15:8	RO	0xc8	BASE_CLK_FREQ Base Clock Frequency for SD clock. These bits indicate the base (maximum) clock frequency for the SD Clock. The definition of these bits depends on the Host Controller Version. (1) 6-Bit Base Clock Frequency: This mode is supported by the Host Controller version 1.00 and 2.00. The upper 2 bits are not effective and are always 0. The unit values are 1 MHz. The supported clock range is 10 MHz to 63 MHz. 8'h0: Get information through another method 8'h0: 1 MHz 8'h1: 2 MHz ..... 8'h3f: 63 MHz Others: Reserved (2) 8-Bit Base Clock Frequency: This mode is supported by the Host Controller version 3.00. The unit values are 1 MHz. The supported clock range is 10 MHz to 255 MHz. 8'h0: Get information through another method 8'h0: 1 MHz 8'h0: 2 MHz ..... 8'hff: 255 MHz
7	RO	0x1	TOUT_CLK_UNIT Timeout Clock Unit. This bit shows the unit of base clock frequency used to detect Data Timeout Error. Values: 1'b0: KHz 1'b1: MHz
6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RO	0x00	TOUT_CLK_FREQ Timeout Clock Frequency. This bit shows the base clock frequency used to detect Data Timeout Error. The Timeout Clock unit defines the unit of timeout clock frequency. It can be KHz or MHz. 6'h0: Get information through another method 6'h1: 1KHz / 1MHz 6'h2: 2KHz / 2MHz 6'h3: 3KHz / 3MHz ..... 6'h3f: 63KHz / 63MHz

EMMC_CAPABILITIES2

Address: Operational Base(0xFF870000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RO	0x0	ADMA3_SUPPORT ADMA3 Support. This bit indicates whether the Host Controller is capable of using ADMA3. Values: 1'b0: ADMA3 not Supported 1'b1: ADMA3 Supported
24	RO	0x0	reserved
23:16	RO	0x0a	CLK_MUL Clock Multiplier. These bits indicate the clock multiplier of the programmable clock generator. Setting these bits to 0 means that the Host Controller does not support a programmable clock generator. Values: 8'h0: Clock Multiplier is not Supported 8'h1: Clock Multiplier M = 2 8'h2: Clock Multiplier M = 3 ..... 8'hFF: Clock Multiplier M = 256
15:14	RO	0x0	RE_TUNING_MODES Re-Tuning Modes. Values: These bits select the re-tuning method and limit the maximum data length. Values: 2'h0: Timer 2'h1: Timer and Re-Tuning Request (Not supported) 2'h2: Auto Re-Tuning (for transfer) 2'h3: Reserved
13	RO	0x1	USE_TUNING_SDR50 Use Tuning for SDR50. Values: 1'b0: SDR50 does not require tuning 1'b1: SDR50 requires tuning
12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:8	RO	0x0	RETUNE_CNT Timer Count for Re-Tuning. Values: 4'h0: Re-Tuning Timer disabled 4'h1: 1 seconds 4'h2: 2 seconds 4'h3: 4 seconds ..... 4'hB: 1024 seconds 4'hC~4'hE: Reserved 4'hF: Get information from other source
7	RO	0x0	reserved
6	RO	0x1	DRV_TYPED This bit indicates support of Driver Type D for 1.8 Signaling. Values: 1'b0: Driver Type D is Not Supported 1'b1: Driver Type D is Supported
5	RO	0x1	DRV_TYPEC This bit indicates support of Driver Type C for 1.8 Signaling. Values: 1'b0: Driver Type C is Not Supported 1'b1: Driver Type C is Supported
4	RO	0x1	DRV_TYPEA This bit indicates support of Driver Type A for 1.8 Signaling. Values: 1'b0: Driver Type A is Not Supported 1'b1: Driver Type A is Supported
3	RO	0x0	UHS2_SUPPORT UHS-II Support. Values: 1'b0: UHS-II is Not Supported 1'b1: UHS-II is Supported
2	RO	0x1	DDR50_SUPPORT DDR50 Support. Values: 1'b0: DDR50 is Not Supported 1'b1: DDR50 is Supported
1	RO	0x1	SDR104_SUPPORT SDR104 Support. Values: 1'b0: SDR104 is Not Supported 1'b1: SDR104 is Supported
0	RO	0x1	SDR50_SUPPORT SDR50 Support. Values: 1'b0: SDR50 is Not Supported 1'b1: SDR50 is Supported

EMMC_FORCE_AUTO_CMD_STAT

Address: Operational Base(0xFF870000) + offset (0x0050)

Bit	Attr	Reset Value	Description
15:8	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
7	WO	0x0	FORCE_CMD_NOT_ISSUED_AUTO_CMD12 Force Event for Command Not Issued By Auto CMD12 Error. Values: 1'b0: Not Affected 1'b1: Command Not Issued By Auto CMD12 Error Status is set
6	RO	0x0	reserved
5	WO	0x0	FORCE_AUTO_CMD_RESP_ERR Force Event for Auto CMD Response Error. Values: 1'b0: Not Affected 1'b1: Auto CMD Response Error Status is set
4	WO	0x0	FORCE_AUTO_CMD_IDX_ERR Force Event for Auto CMD Index Error. Values: 1'b0: Not Affected 1'b1: Auto CMD Index Error Status is set
3	WO	0x0	FORCE_AUTO_CMD_EBIT_ERR Force Event for Auto CMD End Bit Error. Values: 1'b0: Not Affected 1'b1: Auto CMD End Bit Error Status is set
2	WO	0x0	FORCE_AUTO_CMD_CRC_ERR Force Event for Auto CMD CRC Error. Values: 1'b0: Not Affected 1'b1: Auto CMD CRC Error Status is set
1	WO	0x0	FORCE_AUTO_CMD12_TOUT_ERR Force Event for Auto CMD Timeout Error. Values: 1'b0: Not Affected 1'b1: Auto CMD Timeout Error Status is set
0	WO	0x0	FORCE_AUTO_CMD12_NOT_EXEC Force Event for Auto CMD12 Not Executed. Values: 1'b0: Not Affected 1'b1: Auto CMD12 Not Executed Status is set

EMMC_FORC_ERR_INT_STAT

Address: Operational Base(0xFF870000) + offset (0x0052)

Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12	WO	0x0	FORCE_BOOT_ACK_ERR Force Event for Boot Acknowledge error. Values: 1'b0: Not Affected 1'b1: Boot Acknowledge Error Status is set
11	WO	0x0	FORCE_RESP_ERR Force Event for Response Error. Values: 1'b0: Not Affected 1'b1: Response Error Status is set
10	WO	0x0	FORCE_TUNING_ERR Force Event for Tuning Error Values: 1'b0: Not Affected 1'b1: Tuning Error Status is set

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Bit	Attr	Reset Value	Description
9	WO	0x0	FORCE_ADMA_ERR Force Event for ADMA Error. Values: 1'b0: Not Affected 1'b1: ADMA Error Status is set
8	WO	0x0	FORCE_AUTO_CMD_ERR Force Event for Auto CMD Error. Values: 1'b0: Not Affected 1'b1: Auto CMD Error Status is set
7	RO	0x0	reserved
6	WO	0x0	FORCE_DATA_END_BIT_ERR Force Event for Data End Bit Error. Values: 1'b0: Not Affected 1'b1: Data End Bit Error Status is set
5	WO	0x0	FORCE_DATA_CRC_ERR Force Event for Data CRC Error. Values: 1'b0: Not Affected 1'b1: Data CRC Error Status is set
4	WO	0x0	FORCE_DATA_TOUT_ERR Force Event for Data Timeout Error. Values: 1'b0: Not Affected 1'b1: Data Timeout Error Status is set
3	WO	0x0	FORCE_CMD_IDX_ERR Force Event for Command Index Error. Values: 1'b0: Not Affected 1'b1: Command Index Error Status is set
2	WO	0x0	FORCE_CMD_END_BIT_ERR Force Event for Command End Bit Error. Values: 1'b0: Not Affected 1'b1: Command End Bit Error Status is set
1	WO	0x0	FORCE_CMD_CRC_ERR Force Event for Command CRC Error. Values: 1'b0: Not Affected 1'b1: Command CRC Error Status is set
0	WO	0x0	FORCE_CMD_TOUT_ERR Force Event for Command Timeout Error. Values: 1'b0: Not Affected 1'b1: Command Timeout Error Status is set

EMMC_ADMA_ERR_STAT

Address: Operational Base(0xFF870000) + offset (0x0054)

Bit	Attr	Reset Value	Description
7:3	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
2	RO	0x0	ADMA_LEN_ERR ADMA Length Mismatch Error States. This error occurs in the following instances: a. While the Block Count Enable is being set, the total data length specified by the Descriptor table is different from that specified by the Block Count and Block Length; b. When the total data length cannot be divided by the block length Values: 1'b0: No Error 1'b1: Error
1:0	RO	0x0	ADMA_ERR_STATES ADMA Error States. These bits indicate the state of ADMA when an error occurs during ADMA data transfer. Values: 2'h0: Stop DMA - SYS_ADR register points to a location next to the error descriptor 2'h1: Fetch Descriptor - SYS_ADR register points to the error descriptor 2'h2: Never set this state 2'h3: Transfer Data - SYS_ADR register points to a location next to the error descriptor

EMMC_ADMA_SA

Address: Operational Base(0xFF870000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ADMA_SA ADMA System Address. These bits indicate the 32 bits of the ADMA system address. a. SDMA: If Host Version 4 Enable is set to 1, this register stores the system address of the data location b. ADMA2: This register stores the byte address of the executing command of the descriptor table c. ADMA3: This register is set by ADMA3. ADMA2 increments the address of this register that points to the next line, every time a Descriptor line is fetched.

EMMC_PRESET_INIT

Address: Operational Base(0xFF870000) + offset (0x0060)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10	RO	0x0	CLK_GEN_SEL_VAL Clock Generator Select Value. This bit is effective when the Host Controller supports a programmable clock generator. Values: 1'b0: Host Controller Ver2.0 Compatible Clock Generator 1'b1: Programmable Clock Generator
9:0	RO	0x000	FREQ_SEL_VAL SDCLK Frequency Select Value. 10-bit preset value to be set in SDCLK Frequency Select field of the Clock Control register described by a Host System.

EMMC_PRESET_DS

Address: Operational Base(0xFF870000) + offset (0x0062)

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Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10	RO	0x0	CLK_GEN_SEL_VAL Clock Generator Select Value. This bit is effective when the Host Controller supports a programmable clock generator. Values: 1'b0: Host Controller Ver2.0 Compatible Clock Generator 1'b1: Programmable Clock Generator
9:0	RO	0x000	FREQ_SEL_VAL SDCLK Frequency Select Value. 10-bit preset value to be set in SDCLK Frequency Select field of the Clock Control register described by a Host System.

EMMC_PRESET_HS

Address: Operational Base(0xFF870000) + offset (0x0064)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10	RO	0x0	CLK_GEN_SEL_VAL Clock Generator Select Value. This bit is effective when the Host Controller supports a programmable clock generator. Values: 1'b0: Host Controller Ver2.0 Compatible Clock Generator 1'b1: Programmable Clock Generator
9:0	RO	0x000	FREQ_SEL_VAL SDCLK Frequency Select Value. 10-bit preset value to be set in SDCLK Frequency Select field of the Clock Control register described by a Host System.

EMMC_PRESET_SDR12

Address: Operational Base(0xFF870000) + offset (0x0066)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10	RO	0x0	CLK_GEN_SEL_VAL Clock Generator Select Value. This bit is effective when the Host Controller supports a programmable clock generator. Values: 1'b0: Host Controller Ver2.0 Compatible Clock Generator 1'b1: Programmable Clock Generator
9:0	RO	0x000	FREQ_SEL_VAL SDCLK Frequency Select Value. 10-bit preset value to be set in SDCLK Frequency Select field of the Clock Control register described by a Host System.

EMMC_PRESET_SDR25

Address: Operational Base(0xFF870000) + offset (0x0068)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
10	RO	0x0	CLK_GEN_SEL_VAL Clock Generator Select Value. This bit is effective when the Host Controller supports a programmable clock generator. Values: 1'b0: Host Controller Ver2.0 Compatible Clock Generator 1'b1: Programmable Clock Generator
9:0	RO	0x000	FREQ_SEL_VAL SDCLK Frequency Select Value. 10-bit preset value to be set in SDCLK Frequency Select field of the Clock Control register described by a Host System.

EMMC_PRESET_SDR50

Address: Operational Base(0xFF870000) + offset (0x006A)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10	RO	0x0	CLK_GEN_SEL_VAL Clock Generator Select Value. This bit is effective when the Host Controller supports a programmable clock generator. Values: 1'b0: Host Controller Ver2.0 Compatible Clock Generator 1'b1: Programmable Clock Generator
9:0	RO	0x000	FREQ_SEL_VAL SDCLK Frequency Select Value. 10-bit preset value to be set in SDCLK Frequency Select field of the Clock Control register described by a Host System.

EMMC_PRESET_SDR104

Address: Operational Base(0xFF870000) + offset (0x006C)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10	RO	0x0	CLK_GEN_SEL_VAL Clock Generator Select Value. This bit is effective when the Host Controller supports a programmable clock generator. Values: 1'b0: Host Controller Ver2.0 Compatible Clock Generator 1'b1: Programmable Clock Generator
9:0	RO	0x000	FREQ_SEL_VAL SDCLK Frequency Select Value. 10-bit preset value to be set in SDCLK Frequency Select field of the Clock Control register described by a Host System.

EMMC_PRESET_DDR50

Address: Operational Base(0xFF870000) + offset (0x006E)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10	RO	0x0	CLK_GEN_SEL_VAL Clock Generator Select Value. This bit is effective when the Host Controller supports a programmable clock generator. Values: 1'b0: Host Controller Ver2.0 Compatible Clock Generator 1'b1: Programmable Clock Generator

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Bit	Attr	Reset Value	Description
9:0	RO	0x000	FREQ_SEL_VAL SDCLK Frequency Select Value. 10-bit preset value to be set in SDCLK Frequency Select field of the Clock Control register described by a Host System.

EMMC_ADMA_ID

Address: Operational Base(0xFF870000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ADMA_ID ADMA Integrated Descriptor Address. These bits indicate the 32-bit of the ADMA Integrated Descriptor address. The start address of Integrated Descriptor is set to these register bits. The ADMA3 fetches one Descriptor Address and increments these bits to indicate the next Descriptor address.

EMMC_SLOT_INTR_STATUS

Address: Operational Base(0xFF870000) + offset (0x00FC)

Bit	Attr	Reset Value	Description
15:8	RO	0x00	reserved
7:0	RO	0x00	INTR_SLOT Interrupt signal for each Slot. Host Controller support single card slot. This register shall always return 0.

EMMC_HOST_CNTRL_VERS

Address: Operational Base(0xFF870000) + offset (0x00FE)

Bit	Attr	Reset Value	Description
15:8	RO	0x10	VENDOR_VERSION_NUM Vendor Version Number.
7:0	RO	0x05	SPEC_VERSION_NUM Specification Version Number. Values: 8'h0: SD Host Controller Specification Version 1.00 8'h1: SD Host Controller Specification Version 2.00 8'h2: SD Host Controller Specification Version 3.00 8'h3: SD Host Controller Specification Version 4.00 8'h4: SD Host Controller Specification Version 4.10 8'h5: SD Host Controller Specification Version 4.20 Others: Reserved

EMMC_CQVER

Address: Operational Base(0xFF870000) + offset (0x0180)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RO	0x5	EMMC_VER_MAJOR eMMC Major Version Number (1st digit left of decimal point) in BCD format
7:4	RO	0x1	EMMC_VER_MINOR eMMC Minor Version Number(1st digit right of decimal point) in BCD format
3:0	RO	0x0	EMMC_VER_SUFFIX eMMC Version Suffix (2nd digit right of decimal point) in BCD format

EMMC_CQCAP

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Address: Operational Base(0xFF870000) + offset (0x0184)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RO	0x0	CRYPTO_SUPPORT Crypto Support. This bit indicates whether the Host Controller supports cryptographic operations. Values: 1'b0: Crypto not Supported 1'b1: Crypto Supported
27:16	RO	0x000	reserved
15:12	RO	0x0	ITCFMUL Internal Timer Clock Frequency Multiplier. This field indicates the frequency of the clock used for interrupt coalescing timer and for determining the SQS polling period. See ITCFVAL definition for details. 4'h0: 1 KHz clock 4'h1: 10 KHz clock 4'h2: 100 KHz clock 4'h3: 1 MHz clock 4'h4: 10 MHz clock Others: Reserved
11:10	RO	0x0	reserved
9:0	RO	0x000	ITCFVAL Internal Timer Clock Frequency Value. This field scales the frequency of the timer clock provided by ITCFMUL. The Final clock frequency of actual timer clock is calculated as ITCFVAL* ITCFMUL.

EMMC_CQCFG

Address: Operational Base(0xFF870000) + offset (0x0188)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	DCMD_EN Direct Command (DCMD) Enable. This bit indicates to the hardware whether the Task Descriptor in slot #31 of the TDL is a Data Transfer Task Descriptor, or a Direct Command Task Descriptor. CQE uses this bit when a task is issued in slot #31, to determine how to decode the Task Descriptor. Values: 1'b0: Task descriptor in slot #31 is a Data Transfer Task Descriptor 1'b1: Task descriptor in slot #31 is a DCMD Task Descriptor
11:9	RO	0x0	reserved
8	RW	0x0	TASK_DESC_SIZE This bit indicates the size of task descriptor used in host memory. This bit can only be configured when Command Queueing Enable bit is 0 (command queueing is disabled) Values: 1'b0: Task descriptor size is 64 bits 1'b1: Task descriptor size is 128 bits
7:2	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x0	CR_GENERAL_EN Crypto General Enable. Enable/Disable bit for Crypto Engine. If cryptographic operations are not supported, this status bit is reserved. Values: 1'b0: Disable cryptographic operations for all transactions 1'b1: Enable cryptographic operations for transactions where TD.CE=1 or CRNQP.CE=1
0	RW	0x0	CQ_EN Command Queueing Enable. When CQE is disable, the software controls the eMMC bus using the registers between the addresses 0x000 to 0x1FF. Before the software writes to this bit, the software verifies that the eMMC host controller is in idle state and there are no ongoing commands or data transfers. When software wants to exit command queuing mode, it clears all previous tasks (if any) before setting this bit to 0. Values: 1'b0: Disable command queuing 1'b1: Enable command queuing

EMMC_CQCTRL

Address: Operational Base(0xFF870000) + offset (0x018C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	CLR_ALL_TASKS Clear all tasks. This bit can only be written when the controller is halted. This bit does not clear tasks in the device. The software has to use the CMDQ_TASK_MGMT command to clear device's queue. Values: 1'b0: Programming 0 has no effect 1'b1: Clears all the tasks in the controller
7:1	RO	0x00	reserved
0	RW	0x0	HALT Halt request and resume. Values: 1'b0: RESUME_CQE. Software writes 0 to this bit to exit from the halt state and resume CQE activity. 1'b1: HALT_CQE. Software writes 1 to this bit when it wants to acquire software control over the eMMC bus and to disable CQE from issuing command on the bus. For example, issuing a Discard Task command (CMDQ_TASK_MGMT). When the software writes 1, CQE completes the ongoing task (if any in progress). After the task is completed and the CQE is in idle state, CQE does not issue new commands and indicates to the software by setting this bit to 1. The software can poll on this bit until it is set to 1 and only then send commands on the eMMC bus.

EMMC_CQIS

Address: Operational Base(0xFF870000) + offset (0x0190)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
3	RC/W1C	0x0	TCL Task Cleared Interrupt. This status bit is asserted (if CQISTE.TCL=1) when a task clear operation is completed by CQE. The completed task clear operation is either an individual task clear (CQTCLR) or clearing of all tasks (CQCTL). Values: 1'b0: TCL Interrupt is not set 1'b1: TCL Interrupt is set
2	RC/W1C	0x0	RED Response Error Detected Interrupt. This status bit is asserted (if CQISTE.RED=1) when a response is received with an error bit set in the device status field. Software uses CQRMEM register to configure which device status bit fields may trigger an interrupt, and which are masked. Values: 1'b0: RED Interrupt is not set 1'b1: RED Interrupt is set
1	RC/W1C	0x0	TCC Task Complete Interrupt. This status bit is asserted(if CQISTE.TCC=1) when at least one of the following two conditions are met: a. A task is completed and the INT bit is set in its Task Descriptor b. Interrupt caused by Interrupt Coalescing logic Values: 1'b0: TCC Interrupt is not set 1'b1: TCC Interrupt is set
0	RC/W1C	0x0	HAC Halt Complete Interrupt. This status bit is asserted (if CQISTE.HAC=1) when halt bit in CQCTL register transitions from 0 to 1 indicating that Hhost Controller has completed its current ongoing task and has entered halt state. Values: 1'b0: HAC Interrupt is not set 1'b1: HAC Interrupt is set

EMMC_CQISE

Address: Operational Base(0xFF870000) + offset (0x0194)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	TCL_STE Task Cleared Interrupt status enable. Values: 1'b0: CQIS.TCL is disabled 1'b1: CQIS.TCL is set when its interrupt condition is active
2	RW	0x0	RED_STE Response Error Detected Interrupt status enable. Values: 1'b0: CQIS.RED is disabled 1'b1: CQIS.RED is set when its interrupt condition is active
1	RW	0x0	TCC_STE Task Complete Interrupt status enable. Values: 1'b0: CQIS.TCC is disabled 1'b1: CQIS.TCC is set when its interrupt condition is active

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Bit	Attr	Reset Value	Description
0	RW	0x0	HAC_STE Halt Complete Interrupt status enable. Values: 1'b0: CQIS.HAC is disabled 1'b1: CQIS.HAC is set when its interrupt condition is active

EMMC_CQISGE

Address: Operational Base(0xFF870000) + offset (0x0198)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	TCL_SGE Task Cleared Interrupt signal enable. Values: 1'b0: CQIS.TCL interrupt signal generation is disabled 1'b1: CQIS.TCL interrupt signal generation is active
2	RW	0x0	RED_SGE Response Error Detected Interrupt signal enable. Values: 1'b0: CQIS.RED interrupt signal generation is disabled 1'b1: CQIS.RED interrupt signal generation is active
1	RW	0x0	TCC_SGE Task Complete Interrupt signal enable. Values: 1'b0: CQIS.TCC interrupt signal generation is disabled 1'b1: CQIS.TCC interrupt signal generation is active
0	RW	0x0	HAC_SGE Halt Complete Interrupt signal enable. Values: 1'b0: CQIS.HAC interrupt signal generation is disabled 1'b1: CQIS.HAC interrupt signal generation is active

EMMC_CQIC

Address: Operational Base(0xFF870000) + offset (0x019C)

Bit	Attr	Reset Value	Description
31	RW	0x0	INTC_EN Interrupt Coalescing Enable Bit. Values: 1'b0: Interrupt coalescing mechanism is disabled 1'b1: Interrupt coalescing mechanism is active. Interrupts are counted and timed, and coalesced interrupts are generated
30:21	RO	0x000	reserved
20	RO	0x0	INTC_STAT Interrupt Coalescing Status Bit. This bit indicates to the software whether any tasks (with INT=0) have completed and counted towards interrupt coalescing (that is, this is set if and only if INTC counter > 0). Values: 1'b0: INT0 Task completions have not occurred since last counter reset (INTC counter == 0) 1'b1: At least one INT0 task completion has been counted (INTC counter > 0)
19:17	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
16	WO	0x0	INTC_RST Counter and Timer Reset. When host driver writes 1, the interrupt coalescing timer and counter are reset. Values: 1'b0: No Effect 1'b1: Interrupt coalescing timer and counter are reset
15	WO	0x0	INTC_TH_WEN Interrupt Coalescing Counter Threshold Write Enable. When software writes 1 to this bit, the value INTC_TH is updated with the contents written on the same cycle. Values: 1'b0: Clears INTC_TH_WEN 1'b1: Sets INTC_TH_WEN
14:13	RO	0x0	reserved
12:8	WO	0x00	INTC_TH Interrupt Coalescing Counter Threshold filed. Software uses this field to configure the number of task completions (only tasks with INT=0 in the Task Descriptor), which are required in order to generate an interrupt. Counter Operation: As data transfer tasks with INT=0 complete, they are counted by CQE. The counter is reset by software during the interrupt service routine. The counter stops counting when it reaches the value configured in INTC_TH, and generates interrupt. 5'h0: Interrupt coalescing feature disabled 5'h1: Interrupt coalescing interrupt generated after 1 task when INT=0 completes 5'h2: Interrupt coalescing interrupt generated after 2 tasks when INT=0 completes ..... 5'h1f: Interrupt coalescing interrupt generated after 31 tasks when INT=0 completes To write to this field, the INTC_TH_WEN bit must be set during the same write operation.
7	WO	0x0	TOUT_VAL_WEN When software writes 1 to this bit, the value TOUT_VAL is updated with the contents written on the same cycle. Values: 1'b0: clears TOUT_VAL_WEN 1'b1: Sets TOUT_VAL_WEN

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Bit	Attr	Reset Value	Description
6:0	RW	0x00	TOUT_VAL Interrupt Coalescing Timeout Value. Software uses this field to configure the maximum time allowed between the completion of a task on the bus and the generation of an interrupt. Timer Operation: The timer is reset by software during the interrupt service routine. It starts running when a data transfer task with INT=0 is completed, after the timer was reset. When the timer reaches the value configured in ICTOVAL field it generates an interrupt and stops. The timer's unit is equal to 1024 clock periods of the clock whose frequency is specified in the Internal Timer Clock Frequency field CQCAP register. 7'h0: Timer is disabled. Timeout-based interrupt is not generated 7'h1: Timeout on 01x1024 cycles of timer clock frequency 7'h2: Timeout on 02x1024 cycles of timer clock frequency ..... 7'h7f: Timeout on 127x1024 cycles of timer clock frequency In order to write to this field, the TOUT_VAL_WEN bit must be set at the same write operation.

EMMC_CQTDLBA

Address: Operational Base(0xFF870000) + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TDLBA Task Descriptor List Base Address. This register stores the LSB bits (bits 31:0) of the byte address of the head of the Task Descriptor List in system memory. The size of the task descriptor list is 32 * (Task Descriptor size + Transfer Descriptor size) as configured by Host driver. This address shall be set on 1 KB boundary. The lower 10 bits of this register shall be set to 0 by software and shall be ignored by CQE.

EMMC_CQTDBR

Address: Operational Base(0xFF870000) + offset (0x01A8)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DBR Command Queueing Task Doorbell. Software shall configure TDLBA, and enable CQE in CQCFG before using this register. Writing 1 to bit n of this register triggers CQE to start processing the task encoded in slot n of the TDL. Writing 0 by the software does not have any impact on the hardware, and does not change the value of the register bit. CQE always processes tasks in-order according to the order submitted to the list by CQTDBR write transactions. CQE processes Data Transfer tasks by reading the Task Descriptor and sending QUEUED_TASK_PARAMS (CMD44) and QUEUED_TASK_ADDRESS (CMD45) commands to the device. CQE processes DCMD tasks (in slot #31, when enabled) by reading the Task Descriptor, and generating the command encoded by its index and argument. The corresponding bit is cleared to 0 by CQE in one of the following events: a. When a task execution is completed (with success or error) b. The task is cleared using CQTCLR register c. All tasks are cleared using CQCTL register d. CQE is disabled using CQCFG register Software may initiate multiple tasks at the same time (batch submission) by writing 1 to multiple bits of this register in the same transaction. In the case of batch submission, CQE shall process the tasks in order of the task index, starting with the lowest index. If one or more tasks in the batch are marked with QBR, the ordering of execution will be based on said processing order.

EMMC_CQTCN

Address: Operational Base(0xFF870000) + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TCN Task Complete Notification. Each of the 32 bits are bit mapped to the 32 tasks. Bit-N(1): Task-N has completed execution (with success or errors) Bit-N(0): Task-N has not completed, could be pending or not submitted. On task completion, software may read this register to know which tasks have finished. After reading this register, software may clear the relevant bit fields by writing 1 to the corresponding bits.

EMMC_CQDQS

Address: Operational Base(0xFF870000) + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	DQS Device Queue Status. Each of the 32 bits are bit mapped to the 32 tasks. Bit-N(1): Device has marked task N as ready for execution Bit-N(0): Task-N is not ready for execution. This task could be pending in device or not submitted. Host controller updates this register with response of the Device Queue Status command.

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EMMC_CQDPT

Address: Operational Base(0xFF870000) + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	DPT Device Pending Tasks. Each of the 32 bits are bit mapped to the 32 tasks. Bit-N(1): Task-N has been successfully queued into the device and is awaiting execution. Bit-N(0): Task-N is not yet queued. Bit n of this register is set if and only if QUEUED_TASK_PARAMS (CMD44) and QUEUED_TASK_ADDRESS (CMD45) were sent for this specific task and if this task has not been executed yet. CQE shall set this bit after receiving a successful response for CMD45. CQE shall clear this bit after the task has completed execution. Software reads this register in the task-discard procedure to determine if the task is queued in the device.

EMMC_CQTCLR

Address: Operational Base(0xFF870000) + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TCLR Command Queueing Task Clear. Writing 1 to bit n of this register orders CQE to clear a task which software has previously issued. This bit can only be written when CQE is in Halt state as indicated in CQCFG register Halt bit. When software writes 1 to a bit in this register, CQE updates the value to 1, and starts clearing the data structures related to the task. CQE clears the bit fields (sets a value of 0) in CQTCLR and in CQTDBR once the clear operation is complete. Software must poll on the CQTCLR until it is cleared to verify that a clear operation was done.

EMMC_CQSSC1

Address: Operational Base(0xFF870000) + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
19:16	RW	0x1	SQSCMD_BLK_CNT Send Status Command Block Counter. This field indicates when SQS CMD is sent while data transfer is in progress. A value of 'n' indicates that CQE sends status command on the CMD line, during the transfer of data block BLOCK_CNT-n, on the data lines, where BLOCK_CNT is the number of blocks in the current transaction. 4'h0: SEND_QUEUE_STATUS (CMD13) command is not sent during the transaction. Instead, it is sent only when the data lines are idle. 4'h1: SEND_QUEUE_STATUS command is to be sent during the last block of the transaction. 4'h2: SEND_QUEUE_STATUS command when last 2 blocks are pending. 4'h3: SEND_QUEUE_STATUS command when last 3 blocks are pending. ..... 4'hf: SEND_QUEUE_STATUS command when last 15 blocks are pending. Should be programmed only when CQCFG.CQ_EN is '0'.
15:0	RW	0x1000	SQSCMD_IDLE_TMR Send Status Command Idle Timer. This field configures the polling period to be used when using periodic SEND_QUEUE_STATUS (CMD13) polling. Periodic polling is used when tasks are pending in the device, but no data transfer is in progress. When a SEND_QUEUE_STATUS response indicates that no task is ready for execution, CQE counts the configured time until it issues the next SEND_QUEUE_STATUS. Timer units are clock periods of the clock whose frequency is specified in the Internal Timer Clock Frequency field CQCAP register. The minimum value is 0x0001 (1 clock period) and the maximum value is 0xFFFF (65535 clock periods). For example, a CQCAP field value of 0 indicates a 19.2 MHz clock frequency (period = 52.08 ns). If the setting in CQSSC1.CIT is 0x1000, the calculated polling period is 4096*52.08 ns= 213.33 ns. Should be programmed only when CQCFG.CQ_EN is '0'.

EMMC_CQSSC2

Address: Operational Base(0xFF870000) + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	SQSCMD_RCA Send Queue RCA. This field provides CQE with the contents of the 16-bit RCA field in SEND_QUEUE_STATUS (CMD13) command argument. CQE copies this field to bits 31:16 of the argument when transmitting SEND_ QUEUE_STATUS (CMD13) command.

EMMC_CQCRDCT

Address: Operational Base(0xFF870000) + offset (0x01C8)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	DCMD_RESP Direct Command Last Response. This register contains the response of the command generated by the last direct command (DCMD) task that was sent. Contents of this register are valid only after bit 31 of CQTDBR register is cleared by the controller.

EMMC_CQRMEM

Address: Operational Base(0xFF870000) + offset (0x01D0)

Bit	Attr	Reset Value	Description
31:0	RW	0xfdf9a080	RESP_ERR_MASK Response Mode Error Mask. The bits of this field are bit mapped to the device response. This bit is used as an interrupt mask on the device status filed that is received in R1/R1b responses. The reset value of this register is set to trigger an interrupt on all "Error" type bits in the device status. 1'b0: When a R1/R1b response is received, bit i in the device status is ignored. 1'b1: When a R1/R1b response is received, with a bit i in the device status set, a RED interrupt is generated. Note: Responses to CMD13 (SQS) encode the QSR so that they are ignored by this logic.

EMMC_CQTERRI

Address: Operational Base(0xFF870000) + offset (0x01D4)

Bit	Attr	Reset Value	Description
31	RO	0x0	TRANS_ERR_FIELDS_VALID Data Transfer Error Field Valid. This bit is updated when an error is detected while a data transfer transaction was in progress. Values: 1'b0: Ignore contents of TRANS_ERR_TASKID and TRANS_ERR_CMD_INDX 1'b1: Data transfer related error detected. Check contents of TRANS_ERR_TASKID and TRANS_ERR_CMD_INDX fields
30:29	RO	0x0	reserved
28:24	RO	0x00	TRANS_ERR_TASKID Data Transfer Error Task ID. This field captures the ID of the task that was executed and whose data transfer has errors.
23:22	RO	0x0	reserved
21:16	RO	0x00	TRANS_ERR_CMD_INDX Data Transfer Error Command Index. This field captures the index of the command that was executed and whose data transfer has errors.
15	RO	0x0	RESP_ERR_FIELDS_VALID Response Mode Error Fields Valid. This bit is updated when an error is detected while a command transaction was in progress. Values: 1'b0: Ignore contents of RESP_ERR_TASKID and RESP_ERR_CMD_INDX 1'b1: Response-related error is detected. Check contents of RESP_ERR_TASKID and RESP_ERR_CMD_INDX fields
14:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:8	RO	0x00	RESP_ERR_TASKID Response Mode Error Task ID. This field captures the ID of the task which was executed on the command line when the error occurred.
7:6	RO	0x0	reserved
5:0	RO	0x00	RESP_ERR_CMD_INDX Response Mode Error Command Index. This field captures the index of the command that was executed on the command line when the error occurred.

EMMC_CQCRI

Address: Operational Base(0xFF870000) + offset (0x01D8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RO	0x00	CMD_RESP_INDX Last Command Response Index This field stores the index of the last received command response. CQE shall update the value every time a command response is received.

EMMC_CQCRA

Address: Operational Base(0xFF870000) + offset (0x01DC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CMD_RESP_ARG Last Command Response Argument. This field stores the argument of the last received command. CQE shall update the value every time a command response is received.

EMMC_VER_ID

Address: Operational Base(0xFF870000) + offset (0x0500)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	VER_ID Current version number.

EMMC_VER_TYPE

Address: Operational Base(0xFF870000) + offset (0x0504)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	VER_TYPE Version type.

EMMC_HOST_CTRL3

Address: Operational Base(0xFF870000) + offset (0x0508)

Bit	Attr	Reset Value	Description
7:5	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
4	RW	0x0	SW_CG_DIS Internal clock gating disable control. This bit must be used to disable IP's internal clock gating when required. When disabled clocks are not gated. Clocks to the core (except AHB bus clock) must be stopped when programming this bit. Values: 1'b0: Internal clock gating is disabled, clocks are not gated internally 1'b1: Internal clock gates are active and clock gating is controlled internally
3:1	RO	0x0	reserved
0	RW	0x0	CMD_CONFLICT_CHECK Command conflict check. This bit enables command conflict check. Host Controller monitors the CMD line whenever a command is issued and checks whether the value driven on command output line matches the value on command input line at next subsequent edge of transmit clock to determine command conflict error. This bit is cleared only if the feed back delay (including IO Pad delay) is more than (card clock period - flop setup time). Values: 1'b0: Disable command conflict check 1'b1: Check for command conflict after 1 card clock cycle

EMMC_EMMC_CTRL

Address: Operational Base(0xFF870000) + offset (0x052C)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10	RW	0x0	CQE_PREFETCH_DISABLE Enable or Disable CQE's PREFETCH feature. This field allows Software to disable CQE's data prefetch feature when set to 1. Values: 1'b0: CQE can prefetch data for successive WRITE transfers and pipeline successive READ transfers 1'b1: Prefetch for WRITE and Pipeline for READ are disabled
9	RW	0x0	CQE_ALGO_SEL Scheduler algorithm selected for execution. This bit selects the Algorithm used for selecting one of the many ready tasks for execution. Values: 1'b0: Priority based reordering with FCFS to resolve equal priority tasks 1'b1: First come First serve, in the order of DBR rings
8	RW	0x0	ENH_STROBE_ENABLE Enhanced Strobe Enable. This bit instructs Host to sample the CMD line using data strobe for HS400 mode. Values: 1'b0: CMD line is sampled using receive clock for HS400 mode 1'b1: CMD line is sampled using data strobe for HS400 mode
7:3	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
2	RW	0x1	EMMC_RST_N EMMC Device Reset signal control. Values: 1'b0: Reset to eMMC device asserted 1'b1: Reset to eMMC device is de-asserted
1	RW	0x0	DISABLE_DATA_CRC_CHK Disable Data CRC Check. This bit controls masking of CRC16 error for Card Write in eMMC mode. This is useful in bus testing (CMD19) for an eMMC device. In bus testing, an eMMC card does not send CRC status for a block, which may generate CRC error. This CRC error can be masked using this bit during bus testing. Values: 1'b0: DATA CRC check is enabled 1'b1: DATA CRC check is disabled
0	RW	0x0	CARD_IS_EMMC eMMC Card present. This bit indicates the type of card connected. An application program this bit based on the card connected to Host Controller. Values: 1'b0: Card connected to Host Controller is a non-eMMC card 1'b1: Card connected to Host Controller is an eMMC card

EMMC_BOOT_CTRL

Address: Operational Base(0xFF870000) + offset (0x052E)

Bit	Attr	Reset Value	Description
15:12	RW	0x0	BOOT_TOUT_CNT Boot Acknowledge Timeout Counter Value. This value determines the interval by which boot acknowledge timeout (50 ms) is detected when boot acknowledge is expected during boot operation. Values: 4'h0: TMCLK x 2^13 4'h1: TMCLK x 2^14 ..... 4'hE: TMCLK x 2^27 4'hF: Reserved
11:9	RO	0x0	reserved
8	RW	0x0	BOOT_ACK_ENABLE Boot Acknowledge Enable. When this bit set, Host checks for boot acknowledge start pattern of 0-1-0 during boot operation. This bit is applicable for both mandatory and alternate boot mode. Values: 1'b1: Boot Acknowledge enable 1'b0: Boot Acknowledge disable
7	RW	0x0	VALIDATE_BOOT Validate Mandatory Boot Enable bit. This bit is used to validate the MAN_BOOT_EN bit. Values: 1'b1: Validate Mandatory boot enable bit 1'b0: Ignore Mandatory boot Enable bit
6:1	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	MAN_BOOT_EN Mandatory Boot Enable. This bit is used to initiate the mandatory boot operation. The application sets this bit along with VALIDATE_BOOT bit. Writing 0 is ignored. The Host Controller clears this bit after the boot transfer is completed or terminated. Values: 1'b1: Mandatory boot enable 1'b0: Mandatory boot disable

EMMC_AT_CTRL

Address: Operational Base(0xFF870000) + offset (0x0540)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:19	RW	0x0	POST_CHANGE_DLY Time taken for phase switching and stable clock output. Values: 2'h0: Less than 1-cycle latency 2'h1: Less than 2-cycle latency 2'h2: Less than 3-cycle latency 2'h3: Less than 4-cycle latency
18:17	RW	0x0	PRE_CHANGE_DLY Maximum Latency specification between transmit clock and receive clock. Values: 2'h0: Less than 1-cycle latency 2'h1: Less than 2-cycle latency 2'h2: Less than 3-cycle latency 2'h3: Less than 4-cycle latency
16	RW	0x0	TUNE_CLK_STOP_EN Clock stopping control for Tuning and auto-tuning circuit. When enabled, clock gate control output is pulled low before changing phase select codes. This effectively stops the receive clock. Changing phase code when clocks are stopped ensures glitch free phase switching. Values: 1'b0: Clocks not stopped 1'b1: Clocks stopped during phase code change
15:5	RO	0x000	reserved
4	RW	0x0	SW_TUNE_EN This fields enables software-managed tuning flow. Values: 1'b0: Software-managed tuning disabled 1'b1: Software-managed tuning enabled
3	RW	0x0	RPT_TUNE_ERR Framing errors are not generated when executing tuning. This debug bit allows users to report these errors. Values: 1'b0: Default mode where per host no errors are reported 1'b1: Debug mode for reporting framing errors

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Bit	Attr	Reset Value	Description
2	RW	0x0	SWIN_TH_EN Sampling window Threshold enable. Selects the tuning mode. Field should be programmed only when SAMPLE_CLK_SEL is '0'. Values: 1'b0: Tuning engine sweeps all taps and settles at the largest window. 1'b1: Tuning engine selects the first complete sampling window that meets the threshold set by SWIN_TH_VAL field.
1:0	RO	0x0	reserved

EMMC_AT_STAT

Address: Operational Base(0xFF870000) + offset (0x0544)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	L_EDGE_PH_CODE Left Edge Phase code. Reading this field returns the phase code value used by Auto-tuning engine to sample data on Left edge of sampling window.
15:8	RO	0x00	R_EDGE_PH_CODE Right Edge Phase code. Reading this field returns the phase code value used by Auto-tuning engine to sample data on Right edge of sampling window.
7:0	RW	0x00	CENTER_PH_CODE Centered Phase code. Setting AT_CTRL.SW_TUNE_EN enables software to write to this field.

EMMC_DLL_CTRL

Address: Operational Base(0xFF870000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	DLL_BYPASS_MODE DLL bypass mode select. 1'b0: Normal 1'b1: Bypass
23:16	RW	0x00	DLL_START_POINT DLL start point for phase detect.
15:8	RW	0x00	DLL_INCRMENT DLL increment value.
7:2	RO	0x00	reserved
1	RW	0x0	DLL_SRST DLL software reset indication. 1'b0: Normal work 1'b1: Reset
0	RW	0x0	DLL_START DLL working indication. 1'b0: DLL is not working 1'b1: DLL is working

EMMC_DLL_RXCLK

Address: Operational Base(0xFF870000) + offset (0x0804)

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Bit	Attr	Reset Value	Description
31	RW	0x0	RX_CLK_ORI_GATE Receive original clock source gating enable. 1'b0: Receive original clock source is not auto gating, active when card clock is stable and enable. 1'b1: Receive original clock source is auto gating, active when card is working.
30	RO	0x0	reserved
29	RW	0x0	RX_CLK_SRC_SEL Receive clock source selection. 1'b0: Receive clock source is transmit clock output 1'b1: Receive clock source is original clock input
28	RW	0x0	RX_CLK_CHGWIN Receive clock change window configuration. When high, receive clock is gated.
27	RW	0x0	RX_CLK_DLY_ENA Delay enable for receive clock output. 1'b0: Disable delay. Receive clock output comes from receive clock source, determined by RX_CLK_SRC_SEL. 1'b1: Enable delay. Receive clock output comes from delay line output of receive clock source.
26	RW	0x0	RX_DELAY_NUM_SEL Delay element number selection for receive clock. 1'b0: Delay element number comes from hardware calculation 1'b1: Delay element number comes from software (RX_DELAY_NUM)
25	RW	0x0	RX_TAP_VALUE_SEL Tap value selection for receive clock. 1'b0: Tap value equals to (DLL_LOCK_VALUE*2)%256 1'b1: Tap value comes from software (RX_TAP_VALUE)
24	RW	0x0	RX_TAP_NUM_SEL Tap number selection for receive clock. 1'b0: Tap number comes from tuning result 1'b1: Tap number comes from software (RX_TAP_NUM)
23:16	RW	0x00	RX_DELAY_NUM Total delay element number of selected tap used for receive clock.
15:8	RW	0x00	RX_TAP_VALUE Tap value for receive clock. It denotes delay element number for receive clock cycle.
7:5	RO	0x0	reserved
4:0	RW	0x00	RX_TAP_NUM Tap number for receive clock. Every clock is divided into 32 taps equably. The selected tap number is RX_TAP_NUM+1. Use tap number to select tap used for receive clock.

EMMC_DLL_TXCLK

Address: Operational Base(0xFF870000) + offset (0x0808)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	TX_CLK_SRC_SEL Transmit clock source selection. 1'b0: Transmit clock source is invertion of original clock input 1'b1: Transmit clock source is original clock input
28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27	RW	0x0	TX_CLK_DLY_ENA Delay enable for transmit clock output. 1'b0: Disable delay. Transmit clock output comes from transmit clock source, determined by TX_CLK_SRC_SEL. 1'b1: Enable delay. Transmit clock output comes from delay line output of transmit clock source.
26	RW	0x0	TX_DELAY_NUM_SEL Delay element number selection for transmit clock. 1'b0: Delay element number comes from hardware calculation 1'b1: Delay element number comes from software (TX_DELAY_NUM)
25	RW	0x0	TX_TAP_VALUE_SEL Tap value selection for transmit clock. 1'b0: Tap value equals to (DLL_LOCK_VALUE*2)%256 1'b1: Tap value comes from software (TX_TAP_VALUE)
24	RW	0x0	TX_TAP_NUM_SEL Tap number selection for transmit clock. 1'b0: Tap number is 8 1'b1: Tap number comes from software (TX_TAP_NUM)
23:16	RW	0x00	TX_DELAY_NUM Total delay element number of selected tap used for transmit clock.
15:8	RW	0x00	TX_TAP_VALUE Tap value for transmit clock. It denotes delay element number for transmit clock cycle.
7:5	RO	0x0	reserved
4:0	RW	0x00	TX_TAP_NUM Tap number for transmit clock. Every clock is divided into 32 taps equably. The selected tap number is TX_TAP_NUM+1. Use tap number to select tap used for transmit clock.

EMMC_DLL_STRBIN

Address: Operational Base(0xFF870000) + offset (0x080C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	STRBIN_DELAY_ENA Delay enable for strobe input. 1'b0: Disable delay. Strobe input comes from original data strobe. 1'b1: Enable delay. Strobe input comes from delay line output of original data strobe.
26	RW	0x0	STRBIN_DELAY_NUM_SEL Delay element number selection for strobe input. 1'b0: Delay element number comes from hardware calculation 1'b1: Delay element number comes from software (STRBIN_DELAY_NUM)
25	RW	0x0	STRBIN_TAP_VALUE_SEL Tap value selection for strobe input. 1'b0: Tap value equals to (DLL_LOCK_VALUE*2)%256 1'b1: Tap value comes from software (STRBIN_TAP_VALUE)
24	RW	0x0	STRBIN_TAP_NUM_SEL Tap number selection for strobe input. 1'b0: Tap number is 8 1'b1: Tap number comes from software (TAPNUM_TAP_NUM)

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Bit	Attr	Reset Value	Description
23:16	RW	0x00	STRBIN_DELAY_NUM Total delay element number of selected tap used for strobe input.
15:8	RW	0x00	STRBIN_TAP_VALUE Tap value for strobe input. It denotes delay element number for strobe input cycle.
7:5	RO	0x0	reserved
4:0	RW	0x00	STRBIN_TAP_NUM Tap number for strobe input. Every clock is divided into 32 taps equably. The selected tap number is STRBIN_TAP_NUM+1. Use tap number to select tap used for strobe input.

EMMC_DLL_CMDOUT

Address: Operational Base(0xFF870000) + offset (0x0810)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:29	RW	0x0	CMDOEN_SRC_SEL Command output enable selection. 2'b00: Command output enable is from register output triggered by clock rising edge 2'b01: Command output enable is from register output triggered by clock falling edge Others: Command output enable is from both register output triggered by clock rising edge and register output triggered by clock falling edge
28	RW	0x0	CMDOUT_SRC_SEL Command output source selection. 1'b0: Command output source is from register output triggered by clock rising edge 1'b1: Command output source is from register output triggered by clock falling edge
27	RW	0x0	CMDOUT_DELAY_ENA Delay enable for command output. 1'b0: Disable delay. Command output comes from command output source, determined by CMDOUT_SRC_SEL. 1'b1: Enable delay. Command output comes from delay line output of command output source.
26	RW	0x0	CMDOUT_DELAY_NUM_SEL Delay element number selection for command output. 1'b0: Delay element number comes from hardware calculation 1'b1: Delay element number comes from software (CMDOUT_DELAY_NUM)
25	RW	0x0	CMDOUT_TAP_VALUE_SEL Tap value selection for command output. 1'b0: Tap value equals to (DLL_LOCK_VALUE*2)%256 1'b1: Tap value comes from software (CMDOUT_TAP_VALUE)
24	RW	0x0	CMDOUT_TAP_NUM_SEL Tap number selection for command output. 1'b0: Tap number is 0 1'b1: Tap number comes from software (CMDOUT_TAP_NUM)
23:16	RW	0x00	CMDOUT_DELAY_NUM Total delay element number of selected tap used for command output.

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	CMDOUT_TAP_VALUE Tap value for command output. It denotes delay element number for command output.
7:5	RO	0x0	reserved
4:0	RW	0x00	CMDOUT_TAP_NUM Tap number for command output. Every clock is divided into 32 taps equably. The selected tap number is CMDOUT_TAP_NUM+1. Use tap number to select tap used for command output.

EMMC_DLL_STATUS0

Address: Operational Base(0xFF870000) + offset (0x0840)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	DLL_CMDOUT_DELAY_VALUE Delay element number used for command output
15:10	RO	0x00	reserved
9	RO	0x0	DLL_LOCK_TIMEOUT Delay line phase detection timeout status. 1'b0: Not timeout 1'b1: Timeout
8	RO	0x0	DLL_LOCK Delay line lock indication. 1'b0: Delay line is not locked 1'b1: Delay line is locked
7:0	RO	0x00	DLL_LOCK_VALUE Delay line lock value for half card clock cycle. It denotes the delay element number needed for delay line locked. It is valid when DLL_LOCK is high.

EMMC_DLL_STATUS1

Address: Operational Base(0xFF870000) + offset (0x0844)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	DLL_STRBIN_DELAY_VALUE Delay element number used for strobe input
15:8	RO	0x00	DLL_RXCLK_DELAY_VALUE Delay element number used for receive clock
7:0	RO	0x00	DLL_TXCLK_DELAY_VALUE Delay element number used for transmit clock

18.5 Interface Description

Table 18-1 EMMC Interface Description

Module Pin	Direction	PAD Name	IOMUX Setting
emmc_cclk	O	EMMC_CLK/FSPI_CLK/GPIO1_B1_d	GPIO1_IOC_GPIO1B_IOMUX_SEL_L [7:4]=4'h1
emmc_ccmd	I/O	EMMC_CMD/FSPI_CSN0/GPIO1_B0_u	GPIO1_IOC_GPIO1B_IOMUX_SEL_L [3:0]=4'h1
emmc_cdata0	I/O	EMMC_D0/FSPI_D0/GPIO1_A0_u	GPIO1_IOC_GPIO1A_IOMUX_SEL_L [3:0]=4'h1
emmc_cdata1	I/O	EMMC_D1/FSPI_D1/GPIO1_A1_u	GPIO1_IOC_GPIO1A_IOMUX_SEL_L [7:4]=4'h1
emmc_cdata2	I/O	EMMC_D2/FSPI_D2/GPIO1_A2_u	GPIO1_IOC_GPIO1A_IOMUX_SEL_L [11:8]=4'h1
emmc_cdata3	I/O	EMMC_D3/FSPI_D3/GPIO1_A3_u	GPIO1_IOC_GPIO1A_IOMUX_SEL_L [15:12]=4'h1
emmc_cdata4	I/O	EMMC_D4/GPIO1_A4_u	GPIO1_IOC_GPIO1A_IOMUX_SEL_H

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Module Pin	Direction	PAD Name	IOMUX Setting
			[3:0]=4'h1
emmc_cdata5	I/O	EMMC_D5/GPIO1_A5_u	GPIO1_IOC_GPIO1A_IOMUX_SEL_H [7:4]=4'h1
emmc_cdata6	I/O	EMMC_D6/GPIO1_A6_u	GPIO1_IOC_GPIO1A_IOMUX_SEL_H [11:8]=4'h1
emmc_cdata7	I/O	EMMC_D7/GPIO1_A7_u	GPIO1_IOC_GPIO1A_IOMUX_SEL_H [15:12]=4'h1
emmc_strbin	I	EMMC_STRB/FSPI_CSN1/GPIO1_B2_d	GPIO1_IOC_GPIO1B_IOMUX_SEL_L [11:8]=4'h1

Notes: I=input, O=output, I/O=input/output, bidirectional

18.6 Application Notes

18.6.1 Clock Adjustment

Phase detection is needed if you want to know the card clock's precision before clock adjustment. The detection flow is as below:

(1) Set EMMC_DLL_CTRL[1]=1 to reset the EMMC DLL; then set EMMC_DLL_CTRL[1]=0 to dis-reset EMMC DLL;

(2) Set DLL_START_POINT in EMMC_DLL_CTRL[23:16]; set DLL_INCREMENT in EMMC_DLL_CTRL[15:8], and set EMMC_DLL_CTRL[0] to start the DLL phase detection.

(3) Wait for DLL lock until EMMC_DLL_STATUS0[8] equals to 1. Get the EMMC_DLL_STATUS0[7:0] as the locked value for the half card clock cycle time.

(4) If EMMC_DLL_STATUS0[9]=1 and EMMC_DLL_STATUS0[8]=0, the detection is timeout, you can adjust the DLL_START_POINT or DLL_INCREMENT to re-detection.; or bypass the detection if the total delay line length is short than half clock cycle. You need to set EMMC_DLL_CTRL[0] to 0 before you restart phase detection as(1)~(3).

After phase detection, the clock's precision is shown in EMMC_DLL_STATUS0[7:0] (DLL_LOCK_VALUE) based on delay element.

We can calculate the delay element numbers requirement for transmit clock (TXCLK), receive clock (RXCLK), data strobe input (STRBIN), command output (CMDOUT), denoted as "XX" as follows:

(1) Get tap value: if XX_TAP_VALUE_SEL=0, tap value equals to (DLL_LOCK_VALUE*2)%256; else tap value is set by software, XX_TAP_VALUE;

(2) Get tap number: if XX_TAP_NUM_SEL=0, tap number comes from Host Controller; else tap number is set by software, XX_TAP_NUM;

(3) Get required delay element numbers: if XX_DELAY_NUM_SEL=0, delay element number equals to tap value* tap number; else delay element number is set by software, XX_DELAY_NUM.

The adjustment value for every cycle (XX) is equals to required delay element numbers*delay time of every element.

The delay time of every element is in the range of 29ps~63ps, varying with different voltage and temperature.

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Chapter 19 Embedded SRAM

19.1 Overview

There are two embedded SRAMs, SYSTEM_SRAM and PMU_SRAM.

19.1.1 Features supported

- SYSTEM_SRAM
  - Provide 64KB access space
  - Support security and non-security access
  - Secure or non-secure space is software programmable
- PMU_SRAM
  - Provide 8KB access space
  - Support secure access only

19.2 Block Diagram

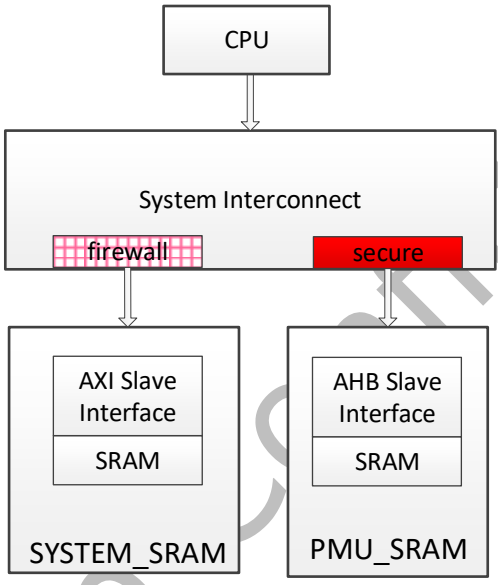


Fig.19-1 Embedded SRAM Block Diagram

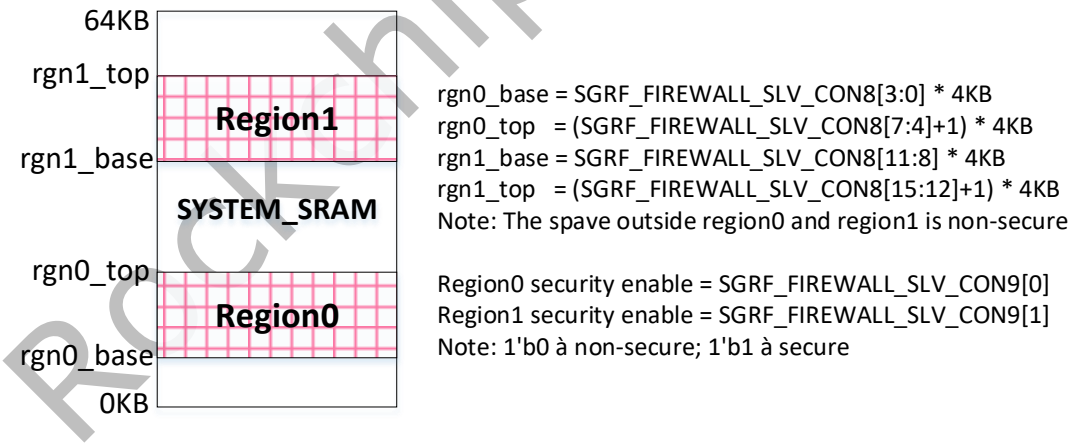


Fig.19-2 SYSTEM_SRAM Security Configuration

19.3 Function Description

19.3.1 AXI slave interface of SYSTEM_SRAM

The AXI slave interface is bridge which translates AXI bus access to SRAM interface of SYSTEM_SRAM.

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19.3.2 AHB slave interface of PMU_SRAM

The AHB slave interface is bridge which translates AHB bus access to SRAM interface of PMU_SRAM.

19.3.3 Embedded SRAM access path

The SYSTEM_SRAM can only be accessed by Cortex-A53, MCU, CRYPTO, DCF and DMAC.
The PMU_SRAM can only be accessed by Cortex-A53, MCU, DCF and DMAC.

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Chapter 20 Mailbox

20.1 Overview

The Mailbox module is a simple APB peripheral that allows CPU, MCU core to communicate with each other by writing operation to generate interrupt. The registers are accessible via APB interface.

The Mailbox has the following main features:

- Support APB interface
- Support four mailbox elements, each element includes one data word, one command word register and one flag bit that can represent one interrupt
- Support interrupts to CPU, and MCU core
- Provide 32 lock registers for software to use to indicate whether mailbox is occupied

20.2 Block Diagram

The figure below shows Mailbox block diagram:

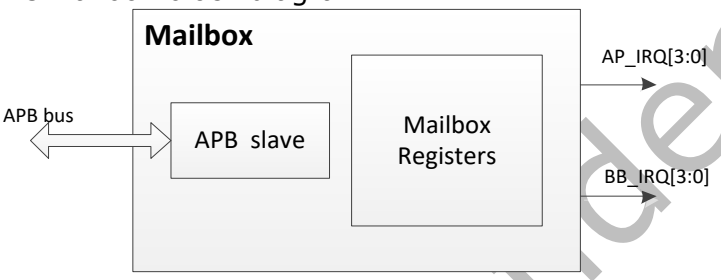


Fig.20-1 Mailbox Block Diagram

20.3 Function Description

20.3.1 Mailbox

- Regard CPU as the "AP" side of the Mailbox. The four elements combined interrupt (|mailbox_irq_ap[3:0]) to CPU is:
  - Enabled when MAILBOX_B2A_INTEN is set to 1 and the responding IRQs is enabled in GIC.
  - Generated when there are writing operation to corresponding MAILBOX_B2A_CMD_i and MAILBOX_B2A_DAT_i orderly.
  - Cleared when writing 1 to corresponding MAILBOX_B2A_STATUS.
- Regard MCU core as the "BB" side of the Mailbox. The four elements combined interrupt (|mailbox_irq_bb[3:0]) to MCU core is:
  - Enabled when MAILBOX_A2B_INTEN is set to 1 and the responding IRQs is enabled in INTC of MCU.
  - Generated when there are writing operation to corresponding MAILBOX_A2B_CMD_i and MAILBOX_A2B_DAT_i orderly.
  - Cleared when writing 1 to corresponding MAILBOX_A2B_STATUS.
- You can also regard CPU as the "BB" side of the Mailbox and regard MCU core as the "AP" side of the Mailbox. The configuration flow is similar.

20.4 Register Description

20.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

20.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
MAILBOX_A2B_INTEN	0x0000	W	0x00000000	AP to BB Interrupt Enable Register
MAILBOX_A2B_STATUS	0x0004	W	0x00000000	AP to BB Interrupt Status Register
MAILBOX_A2B_CMD_0	0x0008	W	0x00000000	AP to BB Command 0 Register
MAILBOX_A2B_DAT_0	0x000C	W	0x00000000	AP to BB Data 0 Register

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Name	Offset	Size	Reset Value	Description
MAILBOX_A2B_CMD_1	0x0010	W	0x00000000	AP to BB Command 1 Register
MAILBOX_A2B_DAT_1	0x0014	W	0x00000000	AP to BB Data 1 Register
MAILBOX_A2B_CMD_2	0x0018	W	0x00000000	AP to BB Command 2 Register
MAILBOX_A2B_DAT_2	0x001C	W	0x00000000	AP to BB Data 2 Register
MAILBOX_A2B_CMD_3	0x0020	W	0x00000000	AP to BB Command 3 Register
MAILBOX_A2B_DAT_3	0x0024	W	0x00000000	AP to BB Data 3 Register
MAILBOX_B2A_INTEN	0x0028	W	0x00000000	BB to AP Interrupt Enable Register
MAILBOX_B2A_STATUS	0x002C	W	0x00000000	BB to AP Interrupt Status Register
MAILBOX_B2A_CMD_0	0x0030	W	0x00000000	BB to AP Command 0 Register
MAILBOX_B2A_DAT_0	0x0034	W	0x00000000	BB to AP Data 0 Register
MAILBOX_B2A_CMD_1	0x0038	W	0x00000000	BB to AP Command 1 Register
MAILBOX_B2A_DAT_1	0x003C	W	0x00000000	BB to AP Data 1 Register
MAILBOX_B2A_CMD_2	0x0040	W	0x00000000	BB to AP Command 2 Register
MAILBOX_B2A_DAT_2	0x0044	W	0x00000000	BB to AP Data 2 Register
MAILBOX_B2A_CMD_3	0x0048	W	0x00000000	BB to AP Command 3 Register
MAILBOX_B2A_DAT_3	0x004C	W	0x00000000	BB to AP Data 3 Register

*Notes: Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

20.4.3 Detail Registers Description

MAILBOX_A2B_INTEN

Address: Operational Base(0xFFAE0000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	int3 Interrupt enable for int3. 1'b0: Disable 1'b1: Enable
2	RW	0x0	int2 Interrupt enable for int2. 1'b0: Disable 1'b1: Enable
1	RW	0x0	int1 Interrupt enable for int1. 1'b0: Disable 1'b1: Enable
0	RW	0x0	int0 Interrupt enable for int0. 1'b0: Disable 1'b1: Enable

MAILBOX_A2B_STATUS

Address: Operational Base(0xFFAE0000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	W1C	0x0	int3 Interrupt status for int3. Clear the interrupt by writing 1 to this bit. 1'b0: Interrupt is inactive 1'b1: Interrupt is active
2	W1C	0x0	int2 Interrupt status for int2. Clear the interrupt by writing 1 to this bit. 1'b0: Interrupt is inactive 1'b1: Interrupt is active

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Bit	Attr	Reset Value	Description
1	W1C	0x0	int1 Interrupt status for int1. Clear the interrupt by writing 1 to this bit. 1'b0: Interrupt is inactive 1'b1: Interrupt is active
0	W1C	0x0	int0 Interrupt status for int0. Clear the interrupt by writing 1 to this bit. 1'b0: Interrupt is inactive 1'b1: Interrupt is active

MAILBOX_A2B_CMD_0

Address: Operational Base(0xFFAE0000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	command Command register.

MAILBOX_A2B_DAT_0

Address: Operational Base(0xFFAE0000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	data Data register.

MAILBOX_A2B_CMD_1

Address: Operational Base(0xFFAE0000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	command Command register.

MAILBOX_A2B_DAT_1

Address: Operational Base(0xFFAE0000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	data Data register.

MAILBOX_A2B_CMD_2

Address: Operational Base(0xFFAE0000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	command Command register.

MAILBOX_A2B_DAT_2

Address: Operational Base(0xFFAE0000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	data Data register.

MAILBOX_A2B_CMD_3

Address: Operational Base(0xFFAE0000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	command Command register.

MAILBOX_A2B_DAT_3

Address: Operational Base(0xFFAE0000) + offset (0x0024)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	data Data register.

MAILBOX_B2A_INTEN

Address: Operational Base(0xFFAE0000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	int3 Interrupt enable for int3. 1'b0: Disable 1'b1: Enable
2	RW	0x0	int2 Interrupt enable for int2. 1'b0: Disable 1'b1: Enable
1	RW	0x0	int1 Interrupt enable for int1. 1'b0: Disable 1'b1: Enable
0	RW	0x0	int0 Interrupt enable for int0. 1'b0: Disable 1'b1: Enable

MAILBOX_B2A_STATUS

Address: Operational Base(0xFFAE0000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	W1C	0x0	int3 Interrupt status for int3. Clear the interrupt by writing 1 to this bit. 1'b0: Interrupt is inactive 1'b1: Interrupt is active
2	W1C	0x0	int2 Interrupt status for int2. Clear the interrupt by writing 1 to this bit. 1'b0: Interrupt is inactive 1'b1: Interrupt is active
1	W1C	0x0	int1 Interrupt status for int1. Clear the interrupt by writing 1 to this bit. 1'b0: Interrupt is inactive 1'b1: Interrupt is active
0	W1C	0x0	int0 Interrupt status for int0. Clear the interrupt by writing 1 to this bit. 1'b0: Interrupt is inactive 1'b1: Interrupt is active

MAILBOX_B2A_CMD_0

Address: Operational Base(0xFFAE0000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	command Command register.

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MAILBOX_B2A_DAT_0

Address: Operational Base(0xFFAE0000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	data Data register.

MAILBOX_B2A_CMD_1

Address: Operational Base(0xFFAE0000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	command Command register.

MAILBOX_B2A_DAT_1

Address: Operational Base(0xFFAE0000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	data Data register.

MAILBOX_B2A_CMD_2

Address: Operational Base(0xFFAE0000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	command Command register.

MAILBOX_B2A_DAT_2

Address: Operational Base(0xFFAE0000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	data Data register.

MAILBOX_B2A_CMD_3

Address: Operational Base(0xFFAE0000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	command Command register.

MAILBOX_B2A_DAT_3

Address: Operational Base(0xFFAE0000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	data Data register.

20.5 Application Notes

- It is recommended to read one ATOMIC_LOCK register first when using the Mailbox. The read value is 0 means it is available, and 1 means it has been automatically locked. Writing to the ATOMIC_LOCK register will clear this bit.
- Write to the CMD register before writing to the DAT register. If wrong order is used, then the interrupt cannot be generated successfully.
- If you want to clear the interrupt, you can read out the STATUS register and writing 1 to corresponding bit.

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