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RV1126B
Technical Reference Manual
(Part 1)

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Chapter 1 System Overview

1.1 Address Mapping

Chapter 5 RV1126B boot from internal BOOTROM, which supports remap function by software programming. Remap is controlled by PMU_SGRF_SOC_CON1[10:9]. When remap is set to 2'b01, the BOOTROM is un-accessible and SYSTEM_SRAM is mapped to address 0x00000000. When remap is set to 2'b10, the BOOTROM is un-accessible and PMU_SRAM is mapped to address 0x00000000.

Table 1-1 Address Mapping

Module	Start Address	Size	Module	Start Address	Size
TOP_CRU	0x20000000	64KB	MAILBOX_HP	0x20D00000	1MB
BUS_CRU	0x20010000	64KB	PWM0	0x20E00000	1MB
PERI_CRU	0x20020000	64KB	PWM2	0x20F00000	1MB
CORE_CRU	0x20030000	64KB	PWM3	0x21000000	1MB
PMU0_CRU	0x20040000	64KB	I2C0	0x21100000	64KB
PMU1_CRU	0x20050000	64KB	I2C1	0x21110000	64KB
DDR_CRU	0x20060000	64KB	I2C3	0x21120000	64KB
VI_CRU	0x20070000	64KB	I2C4	0x21130000	64KB
VEPU_CRU	0x20080000	64KB	I2C5	0x21140000	64KB
NPU_CRU	0x20090000	64KB	RESERVED	0x21150000	64KB
VDO_CRU	0x200A0000	64KB	UART1	0x21160000	64KB
VCP_CRU	0x200B0000	64KB	UART2	0x21170000	64KB
RESERVED	0x200C0000	256KB	UART3	0x21180000	64KB
SYS_GRF	0x20100000	64KB	UART4	0x21190000	64KB
PERI_GRF	0x20110000	32KB	UART5	0x211A0000	64KB
USB3PHYGRF	0x20118000	32KB	UART6	0x211B0000	64KB
CORE_GRF	0x20120000	64KB	UART7	0x211C0000	64KB
PMU_GRF	0x20130000	64KB	RESERVED	0x211D0000	64KB
DDR_GRF	0x20140000	64KB	SPI0	0x211E0000	64KB
VI_GRF	0x20150000	64KB	SPI1	0x211F0000	64KB
VEPU_GRF	0x20160000	64KB	GIC400	0x21200000	64KB
NPU_GRF	0x20170000	64KB	SPINLOCK	0x21210000	64KB
VDO_GRF	0x20180000	64KB	RESERVED	0x21220000	384KB
VCP_GRF	0x20190000	64KB	RTC	0x21280000	64KB
IOC_PMUIO0	0x201A0000	32KB	RESERVED	0x21290000	448KB
IOC_PMUIO1	0x201A8000	32KB	GPIO1	0x21300000	1MB
IOC_VCCIO1	0x201B0000	32KB	USB2PHY	0x21400000	64KB
IOC_VCCIO2	0x201B8000	32KB	USB3PHY	0x21410000	64KB
IOC_VCCIO3	0x201C0000	32KB	RESERVED	0x21420000	128KB
IOC_VCCIO4	0x201C8000	32KB	RESERVED	0x21440000	64KB
IOC_VCCIO5	0x201D0000	32KB	RESERVED	0x21450000	64KB
IOC_VCCIO6	0x201D8000	32KB	FSPI0	0x21460000	64KB
IOC_VCCIO7	0x201E0000	32KB	EMMC	0x21470000	64KB
RESERVED	0x201E8000	96KB	USB2HOST	0x21480000	512KB
BUS_SCRU	0x20200000	64KB	USB3DRD	0x21500000	1MB
PMU_SCRU	0x20210000	64KB	UMCTL2	0x21600000	128KB
SYS_SGRF	0x20220000	64KB	DDR_MONITOR	0x21620000	64KB
PMU_SGRF	0x20230000	64KB	DDR_DFICTRL	0x21630000	64KB
RESERVED	0x20240000	0.75MB	DMA2DDR	0x21640000	64KB
SERVICE_DDR	0x20300000	64KB	DDRPHY	0x21650000	64KB

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Module	Start Address	Size	Module	Start Address	Size
SERVICE_CPU	0x20310000	64KB	DDR FIREWALL_APB	0x21660000	64KB
SERVICE_PERI	0x20320000	64KB	RESERVED	0x21670000	576KB
SERVICE_VI	0x20330000	64KB	GPIO2	0x21700000	1MB
SERVICE_NPU	0x20340000	64KB	GPIO4	0x21800000	1MB
SERVICE_VEPU	0x20350000	64KB	GPIO5	0x21900000	1MB
SERVICE_PMU	0x20360000	64KB	GPIO6	0x21A00000	1MB
SERVICE_BUS	0x20370000	64KB	GPIO7	0x21B00000	1MB
SERVICE_VDO	0x20380000	64KB	CSI2HOST0	0x21C00000	64KB
SERVICE_VCP	0x20390000	64KB	CSI2HOST1	0x21C10000	64KB
SERVICE_PMU1	0x203A0000	64KB	CSI2HOST2	0x21C20000	64KB
SERVICE_AIISP	0x203B0000	320KB	CSI2HOST3	0x21C30000	64KB
RESERVED	0x20400000	512KB	CSIPHY0	0x21C40000	64KB
PVTPLL_CORE	0x20480000	64KB	CSIPHY1	0x21C50000	64KB
RESERVED	0x20490000	448KB	PVTPLL_ISP	0x21C60000	64KB
MAILBOX_LP	0x20500000	1MB	GMAC	0x21C70000	128KB
GPIO0	0x20600000	1MB	RKEPHY	0x21C90000	64KB
PWM1	0x20700000	1MB	MASTER DSMC	0x21CA0000	64KB
I2C2	0x20800000	64KB	SARADC1	0x21CB0000	64KB
UART0	0x20810000	64KB	SARADC2	0x21CC0000	64KB
RKTIMER_HP	0x20820000	64KB	RESERVED	0x21CD0000	192KB
PMU	0x20830000	64KB	ISP	0x21D00000	64KB
RESERVED	0x20840000	64KB	VICAP	0x21D10000	64KB
WDT_LP	0x20850000	64KB	VPSS	0x21D20000	64KB
RCOSC_CTRL	0x20860000	64KB	VPSS_LITE	0x21D30000	64KB
RESERVED	0x20870000	64KB	RKCAN0	0x21D40000	64KB
RKDMA_LP	0x20880000	64KB	RKCAN1	0x21D50000	64KB
RK_AUDIO_ADC_PMU	0x20890000	64KB	SDMMC0	0x21D60000	64KB
SPI2AHB	0x208A0000	64KB	RESERVED	0x21D70000	64KB
AOA_CTRL	0x208B0000	64KB	RESERVED	0x21D80000	64KB
FSPI1	0x208C0000	64KB	RESERVED	0x21D90000	448KB
SAI_LP	0x208D0000	64KB	GPIO3	0x21E00000	1MB
RESERVED	0x208E0000	128KB	PVTPLL_VEPU	0x21F00000	64KB
CRYPTO_S	0x20900000	64KB	SARADC0	0x21F10000	64KB
RKRNG_S	0x20910000	64KB	RESERVED	0x21F20000	128KB
KEYLAD	0x20920000	64KB	RKVENC	0x21F40000	128KB
RESERVED	0x20930000	64KB	SDMMC1	0x21F60000	64KB
CRYPTO_NS	0x20940000	64KB	RESERVED	0x21F70000	64KB
RKRNG_NS	0x20950000	64KB	FEC	0x21F80000	64KB
SAI0	0x20960000	64KB	AVSP	0x21F90000	64KB
SAI1	0x20970000	64KB	AIISP	0x21FA0000	64KB
SAI2	0x20980000	64KB	RESERVED	0x21FB0000	64KB
PDM	0x20990000	64KB	PVTPLL_VCP	0x21FC0000	64KB
RKDSM	0x209A0000	64KB	RESERVED	0x21FD0000	192KB
ASRC0	0x209B0000	64KB	RKNN	0x22000000	64KB
ASRC1	0x209C0000	64KB	RESERVED	0x22010000	448KB
HPMCU_CACHE_SLV	0x209D0000	64KB	PVTPLL_NPU	0x22080000	64KB
HPMCU_CACHE_MEM	0x209E0000	64KB	RESERVED	0x22090000	448KB

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Module	Start Address	Size	Module	Start Address	Size
RGA	0x209F0000	64KB	DECOM	0x22100000	64KB
RKTIMER_2CH	0x20A00000	1MB	DSIPHY	0x22110000	64KB
WDT_S	0x20B00000	64KB	DSI_TX	0x22120000	64KB
OTPC_S	0x20B10000	64KB	RESERVED	0x22130000	64KB
KEY_READER	0x20B20000	64KB	RKVDEC	0x22140000	64KB
RESERVED	0x20B30000	64KB	VOP	0x22150000	64KB
INTC_HP	0x20B40000	64KB	OOC	0x22160000	64KB
WDT_HP	0x20B50000	64KB	RKJPEGD	0x22170000	64KB
WDT_NS	0x20B60000	64KB	RKMMU_DECOM	0x22180000	64KB
DCF	0x20B70000	64KB	RESERVED	0x22190000	2.4375MB
RKDMA	0x20B80000	64KB	DAPLITE	0x22400000	4MB
OTPC_NS	0x20B90000	64KB	RESERVED	0x23000000	16MB
OTP_MASK	0x20BA0000	64KB	FSPI1_XIP	0x24000000	32MB
TSADC	0x20BB0000	64KB	RESERVED	0x26000000	32MB
RESERVED	0x20BC0000	64KB	FSPI0_XIP	0x28000000	128MB
RESERVED	0x20BD0000	64KB	PMU_MEM	0x3FF1E000	8KB
RESERVED	0x20BE0000	64KB	AOA_MEM	0x3FF20000	64KB
RK_AUDIO_ADC_TOP	0x20BF0000	64KB	NPU_CBUF	0x3FF30000	512KB
RKTIMER_6CH	0x20C00000	1MB	SYS_MEM	0x3FFB0000	64KB

The following table shows the boot address before remap and after remap

Table 1-2 Address Remapping

remap[1:0]=2'b00		remap[1:0]=2'b01		remap[1:0]=2'b10	
0x00000000	BOOTROM(48KB)	not accessible	BOOTROM(48KB)	not accessible	BOOTROM(48KB)
0x3FFB0000	SYS_SRAM(64KB)	0x00000000or 0x3FFB0000	SYS_SRAM(64KB)	0x3FFB0000	SYS_SRAM(64KB)
0x3FF1E000	PMU_SRAM(8KB)	0x3FF1E000	PMU_SRAM(8KB)	0x00000000or 0x3FF1E000	PMU_SRAM(8KB)

1.2 System Boot

RV1126B provides system boot from off-chip devices such as SDMMC card, eMMC memory, serial Nand or Nor flash. When boot code is not ready in these devices, the system code can also be downloaded to these devices through the USB DRD interface. All of the boot code will be stored in internal BOOTROM. The following is the whole boot procedure for boot code, which will be stored in BOOTROM in advance.

The following features are supported.

Support system boot from the following device:
Serial Nor Flash, 1bit, 4bits data width (device layout in FSPI IO)
Serial Nand Flash, 1bit, 4bits data width (device layout in FSPI IO)
eMMC Interface, 8bits data width
SDMMC Card, 4bits data width
Support system code download by USB DRD and uart.

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1.3 System Interrupt Connection

RV1126B provides an general interrupt controller (GIC) for CPU / HPMCU /LPMCU. The detailed interrupt sources connection is in the following table.

Table 1-3 RV1126B Interrupt Connection List For CPU(A53)

Number	Source	Polarity	Number	Source	Polarity
32	irq_gpio0_pmu_0	High	160	Reserved	RESERVED
33	irq_gpio0_pmu_1	High	161	irq_rkvenc	High
34	irq_gpio0_pmu_2	High	162	irq_mmu_rkvenc	High
35	irq_gpio0_pmu_3	High	163	irq_decom	High
36	irq_gpio1_0	High	164	irq_rkmmu_decom	RESERVED
37	irq_gpio1_1	High	165	irq_ooc	High
38	irq_gpio1_2	High	166	irq_rkdjpeg_dec	High
39	irq_gpio1_3	High	167	irq_rkejpeg_enc	High
40	irq_gpio2_0	High	168	irq_rkjpeg_mmu	High
41	irq_gpio2_1	High	169	irq_rkvdec_dec	High
42	irq_gpio2_2	High	170	irq_rkvdec_mmu	High
43	irq_gpio2_3	High	171	irq_vop	High
44	irq_gpio3_0	High	172	irq_vop_post_lb	High
45	irq_gpio3_1	High	173	irq_hpmcu_wdt	High
46	irq_gpio3_2	High	174	irq_rga	High
47	irq_gpio3_3	High	175	irq_cache	High
48	irq_gpio4_0	High	176	irq_rknn	High
49	irq_gpio4_1	High	177	irq_csi2host0_1	High
50	irq_gpio4_2	High	178	irq_csi2host0_2	High
51	irq_gpio4_3	High	179	irq_csi2host1_1	High
52	irq_gpio5_0	High	180	irq_csi2host1_2	High
53	irq_gpio5_1	High	181	irq_csi2host2_1	High
54	irq_gpio5_2	High	182	irq_csi2host2_2	High
55	irq_gpio5_3	High	183	irq_csi2host3_1	High
56	irq_gpio6_0	High	184	irq_csi2host3_2	High
57	irq_gpio6_1	High	185	irq_vicap	High
58	irq_gpio6_2	High	186	irq_vicap_ddr	High
59	irq_gpio6_3	High	187	irq_vicap_mmu	High
60	irq_gpio7_0	High	188	irq_isp_mipi	High
61	irq_gpio7_1	High	189	irq_isp_mi	High
62	irq_gpio7_2	High	190	irq_isp	High
63	irq_gpio7_3	High	191	irq_isp_mmu0	High
64	irq_usb3drd_id	High	192	irq_isp_pre3a_done	High
65	irq_usb3drd_bvalid	High	193	irq_vpss_mi	High
66	irq_usb3drd_linestate	High	194	irq_vpss	High
67	irq_usb2host_linestate	High	195	irq_vpss_mmu	High
68	irq_usb3drd_disconnect	High	196	irq_vpsl_mi	High
69	irq_usb2host_disconnect	High	197	irq_vpsl	High
70	irq_usb2host_bvalid	High	198	irq_vpsl_mmu	High

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Number	Source	Polarity	Number	Source	Polarity
71	irq_usb2host_id	High	199	irq_mipi_dsi_host	High
72	irq_pwm0_0	High	200	irq_rkce_ns	High
73	irq_pwm0_1	High	201	irq_rkce_s	High
74	irq_pwm0_2	High	202	irq_kl_rkce	High
75	irq_pwm0_3	High	203	irq_key_reader	High
76	irq_pwm0_4	High	204	irq_lfps_beacon	High
77	irq_pwm0_5	High	205	irq_otp_mask	High
78	irq_pwm0_6	High	206	irq_otp_ns	High
79	irq_pwm0_7	High	207	irq_otp_s	High
80	irq_i2c0	High	208	irq_rkrng_ns	High
81	irq_i2c1	High	209	irq_rkrng_s	High
82	irq_i2c2_pmu	High	210	irq_lpsai	High
83	irq_i2c3	High	211	irq_sai0	High
84	irq_i2c4	High	212	irq_sai1	High
85	irq_i2c5	High	213	irq_sai2	High
86	Reserved	RESERVED	214	irq_pdm	High
87	Reserved	RESERVED	215	irq_asrc0	High
88	irq_uart0_pmu	High	216	irq_asrc1	High
89	irq_uart1	High	217	irq_sdmmc0_detectn_grf	High
90	irq_uart2	High	218	irq_sdmmc1_detectn_grf	High
91	irq_uart3	High	219	irq_sdmmc0	High
92	irq_uart4	High	220	irq_sdi0	High
93	irq_uart5	High	221	irq_emmc	High
94	irq_uart6	High	222	irq_fspi1	High
95	irq_uart7	High	223	irq_fspi0	High
96	irq_hptimer_pmu	High	224	irq_spi0	High
97	irq_stimer0	High	225	irq_spi1	High
98	irq_stimer1	High	226	Reserved	RESERVED
99	irq_timer0	High	227	Reserved	RESERVED
100	irq_timer1	High	228	irq_spi2ahb	High
101	irq_timer2	High	229	irq_gmac_lpi_intr_0	High
102	irq_timer3	High	230	irq_gmac_mcgr_dma_req_0	High
103	irq_timer4	High	231	irq_gmac_pmt_intr_0	High
104	irq_timer5	High	232	irq_gmac_sbd_intr_0	High
105	irq_wdt_pmu	High	233	irq_gmac_sbd_perch_rx_intr_0	High
106	irq_wdt_ns	High	234	irq_gmac_sbd_perch_tx_intr_0	High
107	irq_wdt_s	High	235	irq_rkmacphy	High
108	irq_pvtpll_cpu	High	236	irq_can0	High
109	irq_pvtpll_npu	High	237	irq_can1	High
110	irq_pvtpll_vepu	High	238	irq_usb2host_arb	High
111	irq_pvtpll_vi	High	239	irq_usb2host_ehci	High
112	irq_pvtpll_vcp	High	240	irq_usb2host_ohci	High
113	irq_rkdma	High	241	irq_usb3drd	High
114	irq_lpdmac	High	242	irq_usb3drd_smi	High

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Number	Source	Polarity	Number	Source	Polarity
115	irq_lpdmac_ch	High	243	irq_saradc0	High
116	irq_arpoison_0	High	244	irq_saradc1	High
117	irq_arpoison_1	High	245	irq_saradc2	High
118	irq_arpoison_2	High	246	irq_tsadc	High
119	irq_arpoison_3	High	247	irq_rtcphy	High
120	irq_awpoison_0	High	248	irq_dsmc	High
121	irq_awpoison_1	High	249	irq_aisp	High
122	irq_awpoison_2	High	250	irq_aisp_mmu	High
123	irq_awpoison_3	High	251	rk_tsadc_ota	High
124	irq_dma2ddr	High	252	irq_pwm1_pmu_0	High
125	irq_dfi_alert_err	High	253	irq_pwm1_pmu_1	High
126	irq_derate_temp_limit	High	254	irq_pwm1_pmu_2	High
127	irq_ddrmon	High	255	irq_pwm1_pmu_3	High
128	irq_msch	High	256	irq_pwm2_0	High
129	Reserved	RESERVED	257	irq_pwm2_1	High
130	Reserved	RESERVED	258	irq_pwm2_2	High
131	Reserved	RESERVED	259	irq_pwm2_3	High
132	Reserved	RESERVED	260	irq_pwm2_4	High
133	irq_mailbox_ap_pmu_0	High	261	irq_pwm2_5	High
134	irq_mailbox_ap_pmu_1	High	262	irq_pwm2_6	High
135	irq_mailbox_ap_pmu_2	High	263	irq_pwm2_7	High
136	irq_mailbox_ap_pmu_3	High	264	irq_pwm3_0	High
137	irq_mailbox_bb_pmu_0	High	265	irq_pwm3_1	High
138	irq_mailbox_bb_pmu_1	High	266	irq_pwm3_2	High
139	irq_mailbox_bb_pmu_2	High	267	irq_pwm3_3	High
140	irq_mailbox_bb_pmu_3	High	268	irq_pwm3_4	High
141	irq_hpmcu_mailbox_ap_0	High	269	irq_pwm3_5	High
142	irq_hpmcu_mailbox_ap_1	High	270	irq_pwm3_6	High
143	irq_hpmcu_mailbox_ap_2	High	271	irq_pwm3_7	High
144	irq_hpmcu_mailbox_ap_3	High	272	Reserved	RESERVED
145	irq_hpmcu_mailbox_bb_0	High	273	Reserved	RESERVED
146	irq_hpmcu_mailbox_bb_1	High	274	irq_aad	High
147	irq_hpmcu_mailbox_bb_2	High	275	irq_a53_nexterrirq	High
148	irq_hpmcu_mailb	High	276	irq_a53_npmuirq_0	High

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Number	Source	Polarity	Number	Source	Polarity
	ox_bb_3				
149	irq_preroll_on	High	277	irq_a53_npmuirq_1	High
150	irq_preroll_off	High	278	irq_a53_npmuirq_2	High
151	irq_preroll_on_timerout	High	279	irq_a53_npmuirq_3	High
152	irq_rcosc_ctrl	High	280	irq_a53_ncommirq_0	High
153	irq_dcf	High	281	irq_a53_ncommirq_1	High
154	irq_avsp_dcp	High	282	irq_a53_ncommirq_2	High
155	irq_avsp_rcs	High	283	irq_a53_ncommirq_3	High
156	irq_avsp_mmu	High	284	irq_a53_nvcpumntirq_0	High
157	irq_fec	High	285	irq_a53_nvcpumntirq_1	High
158	irq_fec_mmu	High	286	irq_a53_nvcpumntirq_2	High
159	Reserved	RESERVED	287	irq_a53_nvcpumntirq_3	High

Table 1-4 RV1126B Interrupt Connection List For HPMCU

Number	Source	Polarity	Number	Source	Polarity
0	irq_gpio0_pmu_0	High	128	Reserved	RESERVED
1	irq_gpio0_pmu_1	High	129	irq_rkvenc	High
2	irq_gpio0_pmu_2	High	130	irq_mmu_rkvenc	High
3	irq_gpio0_pmu_3	High	131	irq_decom	High
4	irq_gpio1_0	High	132	irq_rkmmu_decom	RESERVED
5	irq_gpio1_1	High	133	irq_ooc	High
6	irq_gpio1_2	High	134	irq_rkdjpeg_dec	High
7	irq_gpio1_3	High	135	irq_rkejpeg_enc	High
8	irq_gpio2_0	High	136	irq_rkjpeg_mmu	High
9	irq_gpio2_1	High	137	irq_rkvdec_dec	High
10	irq_gpio2_2	High	138	irq_rkvdec_mmu	High
11	irq_gpio2_3	High	139	irq_vop	High
12	irq_gpio3_0	High	140	irq_vop_post_lb	High
13	irq_gpio3_1	High	141	irq_hpmcu_wdt	High
14	irq_gpio3_2	High	142	irq_rga	High
15	irq_gpio3_3	High	143	irq_cache	High
16	irq_gpio4_0	High	144	irq_rknn	High
17	irq_gpio4_1	High	145	irq_csi2host0_1	High
18	irq_gpio4_2	High	146	irq_csi2host0_2	High
19	irq_gpio4_3	High	147	irq_csi2host1_1	High
20	irq_gpio5_0	High	148	irq_csi2host1_2	High
21	irq_gpio5_1	High	149	irq_csi2host2_1	High
22	irq_gpio5_2	High	150	irq_csi2host2_2	High
23	irq_gpio5_3	High	151	irq_csi2host3_1	High
24	irq_gpio6_0	High	152	irq_csi2host3_2	High
25	irq_gpio6_1	High	153	irq_vicap	High
26	irq_gpio6_2	High	154	irq_vicap_ddr	High
27	irq_gpio6_3	High	155	irq_vicap_mmu	High
28	irq_gpio7_0	High	156	irq_isp_mipi	High
29	irq_gpio7_1	High	157	irq_isp_mi	High

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Number	Source	Polarity	Number	Source	Polarity
30	irq_gpio7_2	High	158	irq_isp	High
31	irq_gpio7_3	High	159	irq_isp_mmu0	High
32	irq_usb3drd_id	High	160	irq_isp_pre3a_done	High
33	irq_usb3drd_bvalid	High	161	irq_vpss_mi	High
34	irq_usb3drd_linestate	High	162	irq_vpss	High
35	irq_usb2host_linestate	High	163	irq_vpss_mmu	High
36	irq_usb3drd_disconnect	High	164	irq_vpsl_mi	High
37	irq_usb2host_disconnect	High	165	irq_vpsl	High
38	irq_usb2host_bvalid	High	166	irq_vpsl_mmu	High
39	irq_usb2host_id	High	167	irq_mipi_dsi_host	High
40	irq_pwm0_0	High	168	irq_rkce_ns	High
41	irq_pwm0_1	High	169	irq_rkce_s	High
42	irq_pwm0_2	High	170	irq_kl_rkce	High
43	irq_pwm0_3	High	171	irq_key_reader	High
44	irq_pwm0_4	High	172	irq_lfps_beacon	High
45	irq_pwm0_5	High	173	irq_otp_mask	High
46	irq_pwm0_6	High	174	irq_otp_ns	High
47	irq_pwm0_7	High	175	irq_otp_s	High
48	irq_i2c0	High	176	irq_rkrng_ns	High
49	irq_i2c1	High	177	irq_rkrng_s	High
50	irq_i2c2_pmu	High	178	irq_lpsai	High
51	irq_i2c3	High	179	irq_sai0	High
52	irq_i2c4	High	180	irq_sai1	High
53	irq_i2c5	High	181	irq_sai2	High
54	Reserved	RESERVED	182	irq_pdm	High
55	Reserved	RESERVED	183	irq_asrc0	High
56	irq_uart0_pmu	High	184	irq_asrc1	High
57	irq_uart1	High	185	irq_sdmmc0_detectn_grf	High
58	irq_uart2	High	186	irq_sdmmc1_detectn_grf	High
59	irq_uart3	High	187	irq_sdmmc0	High
60	irq_uart4	High	188	irq_sdi0	High
61	irq_uart5	High	189	irq_emmc	High
62	irq_uart6	High	190	irq_fspi1	High
63	irq_uart7	High	191	irq_fspi0	High
64	irq_hptimer_pmu	High	192	irq_spi0	High
65	irq_stimer0	High	193	irq_spi1	High
66	irq_stimer1	High	194	Reserved	RESERVED
67	irq_timer0	High	195	Reserved	RESERVED
68	irq_timer1	High	196	irq_spi2ahb	High
69	irq_timer2	High	197	irq_gmac_lpi_intr_0	High
70	irq_timer3	High	198	irq_gmac_mcgr_dma	High

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Number	Source	Polarity	Number	Source	Polarity
				_req_0	
71	irq_timer4	High	199	irq_gmac_pmt_intr_0	High
72	irq_timer5	High	200	irq_gmac_sbd_intr_0	High
73	irq_wdt_pmu	High	201	irq_gmac_sbd_perch_rx_intr_0	High
74	irq_wdt_ns	High	202	irq_gmac_sbd_perch_tx_intr_0	High
75	irq_wdt_s	High	203	irq_rkmacphy	High
76	irq_pvtpll_cpu	High	204	irq_can0	High
77	irq_pvtpll_npu	High	205	irq_can1	High
78	irq_pvtpll_vepu	High	206	irq_usb2host_arb	High
79	irq_pvtpll_vi	High	207	irq_usb2host_ehci	High
80	irq_pvtpll_vcp	High	208	irq_usb2host_ohci	High
81	irq_rkdma	High	209	irq_usb3drd	High
82	irq_lpdmac	High	210	irq_usb3drd_smi	High
83	irq_lpdmac_ch	High	211	irq_saradc0	High
84	irq_arpoison_0	High	212	irq_saradc1	High
85	irq_arpoison_1	High	213	irq_saradc2	High
86	irq_arpoison_2	High	214	irq_tsadc	High
87	irq_arpoison_3	High	215	irq_rtcphy	High
88	irq_awpoison_0	High	216	irq_dsmc	High
89	irq_awpoison_1	High	217	irq_aisp	High
90	irq_awpoison_2	High	218	irq_aisp_mmu	High
91	irq_awpoison_3	High	219	rk_tsadc_ota	High
92	irq_dma2ddr	High	220	irq_pwm1_pmu_0	High
93	irq_dfi_alert_err	High	221	irq_pwm1_pmu_1	High
94	irq_derate_temp_limit	High	222	irq_pwm1_pmu_2	High
95	irq_ddrmon	High	223	irq_pwm1_pmu_3	High
96	irq_msch	High	224	irq_pwm2_0	High
97	Reserved	RESERVED	225	irq_pwm2_1	High
98	Reserved	RESERVED	226	irq_pwm2_2	High
99	Reserved	RESERVED	227	irq_pwm2_3	High
100	Reserved	RESERVED	228	irq_pwm2_4	High
101	irq_mailbox_ap_pmu_0	High	229	irq_pwm2_5	High
102	irq_mailbox_ap_pmu_1	High	230	irq_pwm2_6	High
103	irq_mailbox_ap_pmu_2	High	231	irq_pwm2_7	High
104	irq_mailbox_ap_pmu_3	High	232	irq_pwm3_0	High
105	irq_mailbox_bb_pmu_0	High	233	irq_pwm3_1	High
106	irq_mailbox_bb_pmu_1	High	234	irq_pwm3_2	High
107	irq_mailbox_bb_pmu_2	High	235	irq_pwm3_3	High
108	irq_mailbox_bb_	High	236	irq_pwm3_4	High

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Number	Source	Polarity	Number	Source	Polarity
	pmu_3				
109	irq_hpmcu_mailbox_ap_0	High	237	irq_pwm3_5	High
110	irq_hpmcu_mailbox_ap_1	High	238	irq_pwm3_6	High
111	irq_hpmcu_mailbox_ap_2	High	239	irq_pwm3_7	High
112	irq_hpmcu_mailbox_ap_3	High	240	Reserved	RESERVED
113	irq_hpmcu_mailbox_bb_0	High	241	Reserved	RESERVED
114	irq_hpmcu_mailbox_bb_1	High	242	irq_aad	High
115	irq_hpmcu_mailbox_bb_2	High	243	irq_a53_nexterrirq	High
116	irq_hpmcu_mailbox_bb_3	High	244	irq_a53_npmuirq_0	High
117	irq_preroll_on	High	245	irq_a53_npmuirq_1	High
118	irq_preroll_off	High	246	irq_a53_npmuirq_2	High
119	irq_preroll_on_timerout	High	247	irq_a53_npmuirq_3	High
120	irq_rcosc_ctrl	High	248	irq_a53_ncommirq_0	High
121	irq_dcf	High	249	irq_a53_ncommirq_1	High
122	irq_avsp_dcp	High	250	irq_a53_ncommirq_2	High
123	irq_avsp_rcs	High	251	irq_a53_ncommirq_3	High
124	irq_avsp_mmu	High	252	irq_a53_nvcpumntirq_0	High
125	irq_fec	High	253	irq_a53_nvcpumntirq_1	High
126	irq_fec_mmu	High	254	irq_a53_nvcpumntirq_2	High
127	Reserved	RESERVED	255	irq_a53_nvcpumntirq_3	High

There are one LPMCU in the PD_PMU, The detailed interrupt sources connection for the LPMCU is in the following table.

Table 1-5 RV1126B Interrupt Connection List For LPMCU

Number	**Source**	**Polarity**	**Number**	**Source**	**Polarity**
0	irq_gpio0_pmu	High	8	irq_fspi1	High
1	irq_hptimer_pmu	High	9	irq_pwm1_pmu	High
2	irq_uart0_pmu	High	10	irq_preroll_on	High
3	irq_i2c2_pmu	High	11	irq_preroll_off	High
4	irq_wdt_pmu	High	12	irq_preroll_on_timeout	High
5	irq_mailbox_ap_pmu	High	13	irq_rtcphy	RESERVED
6	irq_lpsai	High	14	irq_aad	RESERVED
7	irq_spi2ahb	High	15	irq_lpdmac	RESERVED

1.4 System DMA Hardware Request Connection

RV1126B provides one DMA controller (DMAC) inside the system, the following tables are the DMA hardware request list, type, support single or not and polarity.

Table 1-6 DMAC Request Mapping Table

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Req Number	Source	TX/RX/M	Support Single	Polarity
0	DMA_PERI_UART0_RX	RX/M	Y	High level
1	DMA_PERI_UART0_TX	TX/M	N	High level
2	DMA_PERI_UART1_RX	RX/M	Y	High level
3	DMA_PERI_UART1_TX	TX/M	N	High level
4	DMA_PERI_UART2_RX	RX/M	Y	High level
5	DMA_PERI_UART2_TX	TX/M	N	High level
6	DMA_PERI_UART3_RX	RX/M	Y	High level
7	DMA_PERI_UART3_TX	TX/M	N	High level
8	DMA_PERI_UART4_RX	RX/M	Y	High level
9	DMA_PERI_UART4_TX	TX/M	N	High level
10	DMA_PERI_UART5_RX	RX/M	Y	High level
11	DMA_PERI_UART5_TX	TX/M	N	High level
12	DMA_PERI_UART6_RX	RX/M	Y	High level
13	DMA_PERI_UART6_TX	TX/M	N	High level
14	DMA_PERI_UART7_RX	RX/M	Y	High level
15	DMA_PERI_UART7_TX	TX/M	N	High level
16	DMA_PERI_SAI0_RX	RX/M	N	High level
17	DMA_PERI_SAI0_TX	TX/M	N	High level
18	DMA_PERI_SAI1_RX	RX/M	N	High level
19	DMA_PERI_SAI1_TX	TX/M	N	High level
20	DMA_PERI_SAI2_RX	RX/M	N	High level
21	DMA_PERI_SAI2_TX	TX/M	N	High level
22	DMA_PERI_ASRC0_RX	RX/M	N	High level
23	DMA_PERI_ASRC0_TX	TX/M	N	High level
24	DMA_PERI_ASRC1_RX	RX/M	N	High level
25	DMA_PERI_ASRC1_TX	TX/M	N	High level
26	DMA_PERI_PDM_RX	RX/M	N	High level
27	RSV	RESERVED	N	RESERVED
28	RSV	RESERVED	N	RESERVED
29	RSV	RESERVED	N	RESERVED
30	DMA_PERI_I2C1_RX	RX/M	Y	High level
31	DMA_PERI_I2C1_TX	TX/M	N	High level
32	RSV	RESERVED	N	RESERVED
33	RSV	RESERVED	N	RESERVED
34	DMA_PERI_I2C3_RX	RX/M	Y	High level
35	DMA_PERI_I2C3_TX	TX/M	N	High level
36	RSV	RESERVED	N	RESERVED
37	RSV	RESERVED	N	RESERVED
38	RSV	RESERVED	N	RESERVED
39	RSV	RESERVED	N	RESERVED
40	DMA_PERI_SPI0_RX	RX/M	Y	High level

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Req Number	Source	TX/RX/M	Support Single	Polarity
41	DMA_PERI_SPI0_TX	TX/M	N	High level
42	DMA_PERI_SPI1_RX	RX/M	Y	High level
43	DMA_PERI_SPI1_TX	TX/M	N	High level
44	DMA_PERI_CAN0_RX	RX/M	N	High level
45	DMA_PERI_CAN1_RX	RX/M	N	High level
46	DMA_PERI_DSMC0	RX/TX/M	N	High level
47	DMA_PERI_DSMC1	RX/TX/M	N	High level

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Chapter 2 CRU

2.1 Overview

The CRU is an APB slave module that is designed for generating all of the internal and system clocks, resets in the chip. CRU generates system clocks from PLL output clock or external clock source, and generates system reset from external power-on-reset, watchdog timer reset or software reset or temperature sensor.
The CRU is located at several addresses.

- TOPCRU : used for general system, with base address 0x20000000
- BUSCRU : used for bus system, with base address 0x20010000
- PERICRU : used for peripheral system, with base address 0x20020000
- CORECRU : used for core system, with base address 0x20030000
- PMUCRU : used for pmu always on system, with base address 0x20040000
- PMU1CRU : used for pmu1 system, with base address 0x20050000
- DDRCRU : used for general ddr system, with base address 0x20060000
- SUBDDRCRU : used for clk1x ddr system, with base address 0x20068000
- VICRU : used for isp system, with base address 0x20070000
- VEPUCRU : used for vepu system, with base address 0x20080000
- NPUCRU : used for npu system, with base address 0x20090000
- VDOCRU : used for vdo system, with base address 0x200a0000
- VCPCRU : used for vcp system, with base address 0x200b0000
- SBUSCRU : used for secure bus system, with base address 0x20200000
- SPMUCRU : used for secure pmu system, with base address 0x20210000

The CRU supports the following features:

- Compliance with AMBA APB interface
- Embedded with 4 fractional PLLs and 0 integer PLLs
- Flexible selection of clock source
- Support dividing clock separately
- Support gating clock separately
- Support software reset each module separately.

2.2 Block Diagram

The CRU comprises with:

- PLL
- Register configuration unit
- Clock generate unit
- Reset generate unit

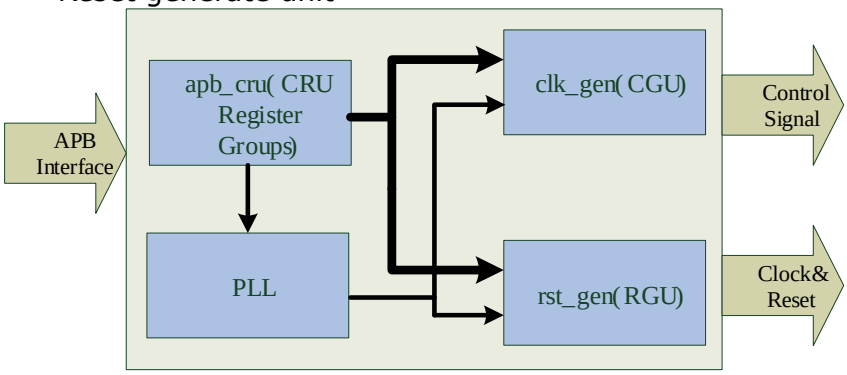

Fig.2-1 CRU Block Diagram

2.3 Function Description

2.3.1 System Clock Solution

There are 4 fractional PLLs: AUPLL/CPLL/DPLL/GPLL. Each PLL can only receive 24MHz oscillator as input reference clock and can be set to three work modes: normal mode, slow mode and deep slow mode. When power on or changing PLL setting, we must program PLL into slow mode or deep slow mode.

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To maximize the flexibility, some of clocks can select divider source from multiple PLLs. To provide some specific frequency, another solution is integrated: fractional divider. Divfree50 divider are also provided for some modules. All clocks can be gated by software.
The basic units for clock generation are:

- Gating
- MUX (multiplexer)
- Divfree (Glitch free divider)
  - clk_out_freq = clk_in_freq / divisor
  - When divisor is even, the clock duty cycle of clk_out is 50%
  - When divisor is odd, the clock duty cycle of clk_out is not 50%
- Fracdiv (Fractional divider)
  - clk_out_freq = clk_in_freq * numerator / denominator, both numerator and denominator are 16 bits or 24 bits
- Divfree50(Glitch free divider for duty cycle 50%)
  - clk_out_freq = clk_in_freq / divisor
  - When divisor is even or odd, the clock duty cycle of clk_out is 50%

The settings of all basic units are controlled by CRU registers.

2.3.2 System Reset Solution

Almost all modules have these reset source as the following figure shows. The 'xxx' in the figure is the module name.

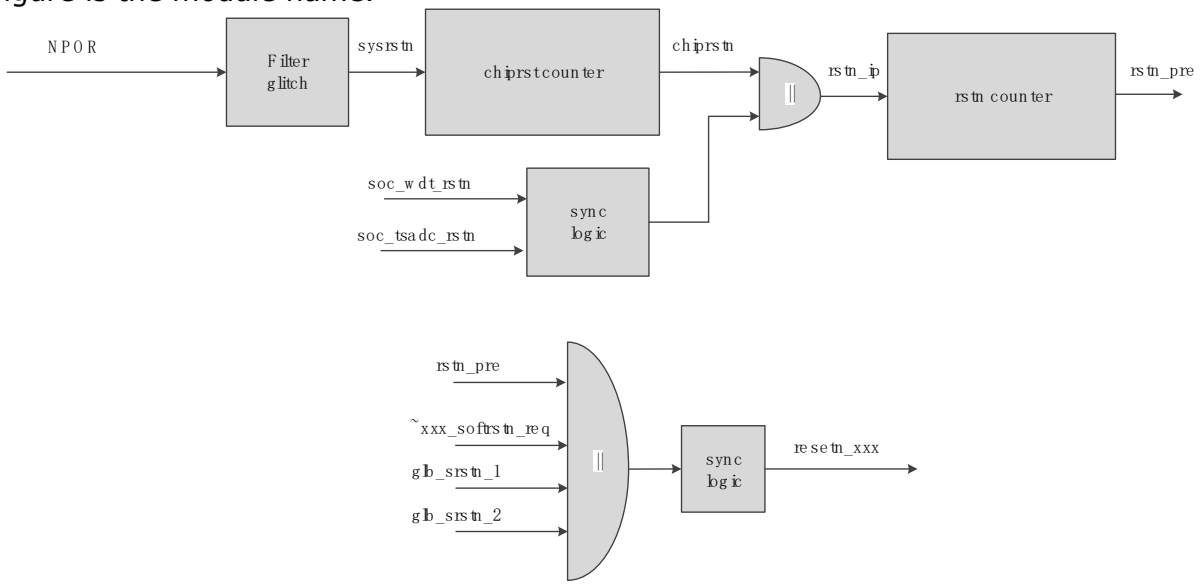

Fig.2-2 Reset Architecture Diagram

Reset source of each reset signal includes:

- NPOR: External power on reset
- soc_wdt_rstn: Reset from WDT module
- soc_tsadc_rstn: Reset from TSADC module
- softrstn_req: Software reset request by programming CRU_SOFTRST_CON
- glb_srstn_1: First global software reset by programming CRU_GLB_SRST_FST as 0xfdb9
- glb_srstn_2: Second global software reset by programming CRU_GLB_SRST_SND as 0xeca8

2.3.3 Fractional PLL Introduction

The fractional PLLs output clock's frequency up to 3.8GHz. The PLL is a general purpose, high-performance PLL-based clock generator. The PLL is a multi-function, general purpose frequency synthesizer. Ultra-wide input and output ranges along with best-in-class jitter performance allow the PLL to be used for almost any clocking application. With excellent supply noise immunity, the PLL is ideal for use in noisy mixed signal SoC environments.
The PLL supports the following features:

- Input frequency range:1MHz to 1200MHz for integer mode and 10 MHz to 1200 MHz for fractional mode

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- PFD minimum reference frequency range: 1MHz for integer mode and 10MHz for fractional mode
- Output frequency range: 19 MHz to 3.8GHz
- VCO output frequency range: 950MHz to 3.8GHz
- 24bit fractional accuracy, and fractional mode jitter performance to nearly match integer mode performance.
- 4:1 VCO frequency range allows PLL to be optimized for minimum jitter or minimum power.
- Isolated analog supply (1.8V) allows for excellent supply rejection in noisy SoC applications
- Lock detect signal indicates when frequency lock has been achieved
  PLL block diagram is shown below.

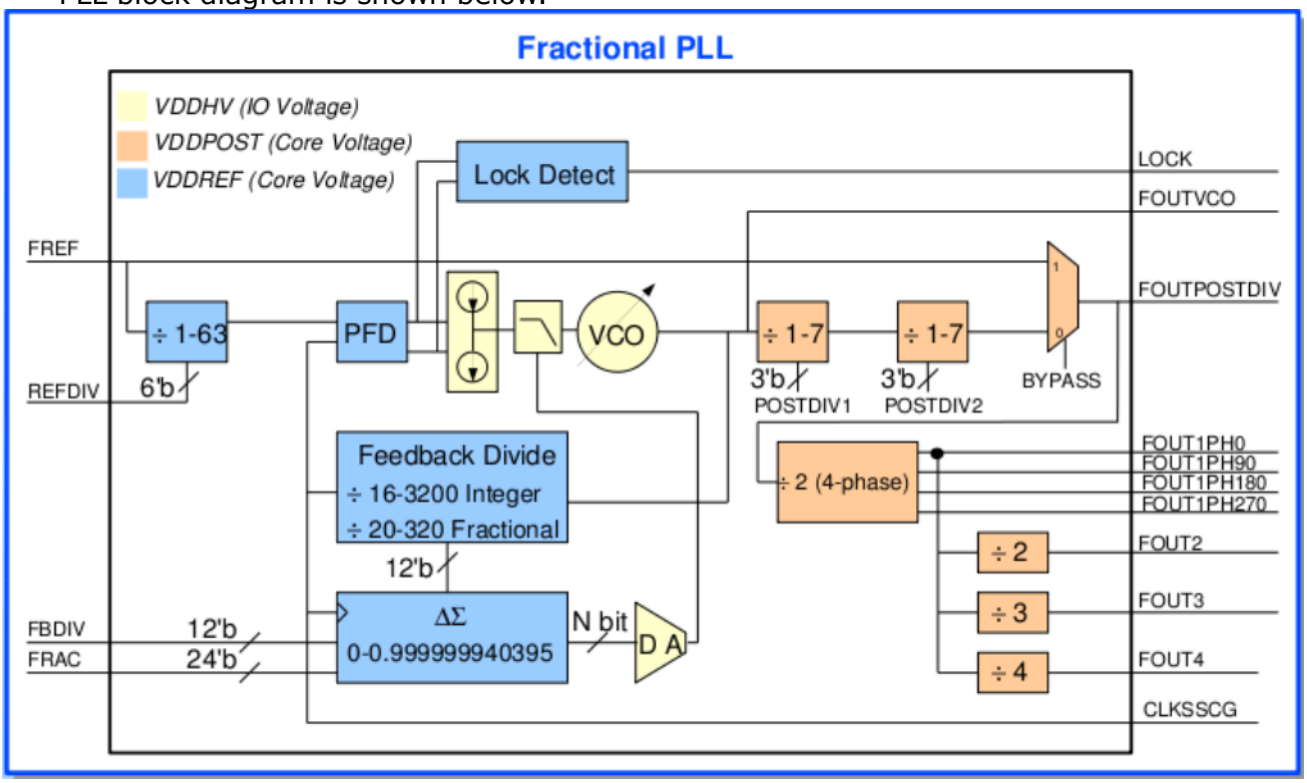

Fig.2-3 PLL Block Diagram

2.3.4 Integer PLL Introduction

The integer PLLs output clock's frequency up to 1.9GHz. The PLL is a multi-function, general purpose frequency synthesizer optimized for low power digital clocking. Wide input and output ranges along with best-in-class jitter performance allow the PLL to be used for a variety of different application. With excellent supply noise immunity, the PLL is ideal for use in noisy SoC environments.

The PLL supports the following features:

- Input frequency range:10MHz to 800MHz
- PFD minimum reference frequency range: 10MHz
- Output frequency range:9 MHz to 1.9GHz
- VCO output frequency range:475 MHz to1.9 GHz
- 4:1 VCO frequency range allows PLL to be optimized form minimum jitter or minimum power
- Low period jitter provides maximum timing margin in high frequency designs
- Lock detect signal indicates when frequency lock has been achieved
  PLL block diagram is shown below.

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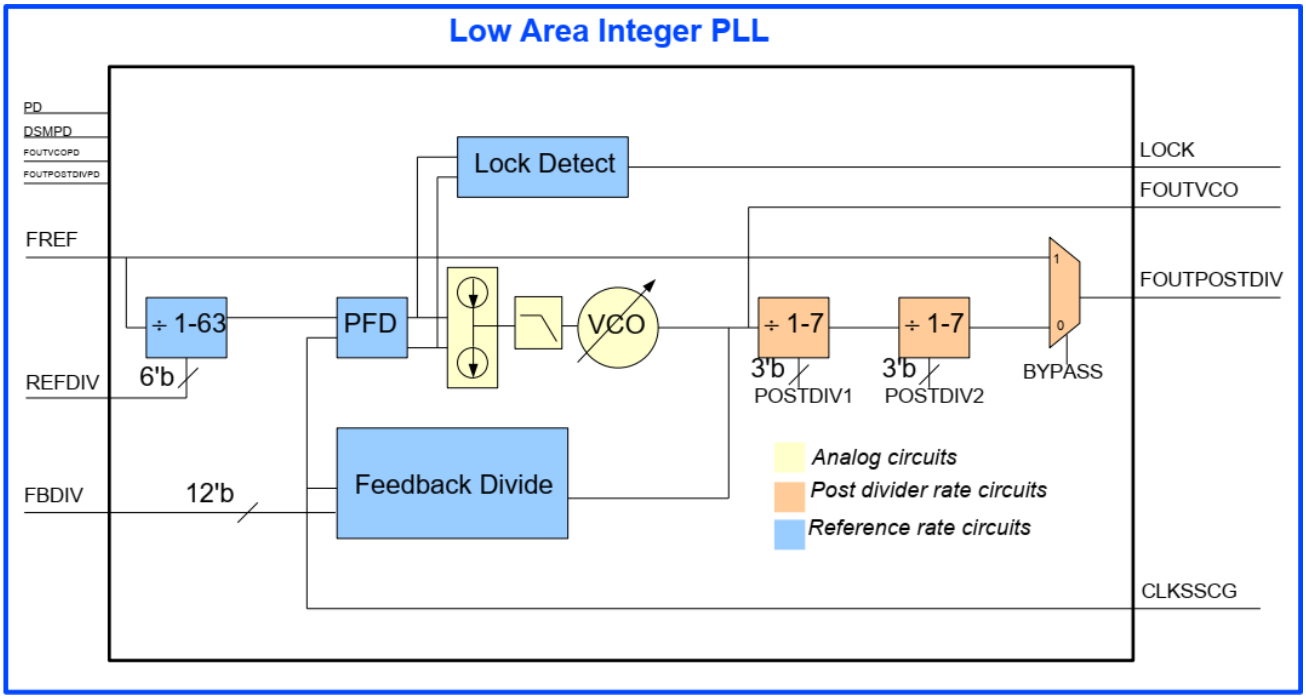

Fig.2-4 Integer PLL Block Diagram

2.4 Register Description

2.4.1 TOPCRU

2.4.1.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

2.4.1.2 Registers Summary

Name	Offset	Size	Reset Value	Description
TOPCRU_CRU_AUPLL_CON0	0x0000	W	0x00002100	PLL configuration register0
TOPCRU_CRU_AUPLL_CON1	0x0004	W	0x00001082	PLL configuration register1
TOPCRU_CRU_AUPLL_CON2	0x0008	W	0x00000000	PLL configuration register2
TOPCRU_CRU_AUPLL_CON3	0x000C	W	0x00000007	PLL configuration register3
TOPCRU_CRU_AUPLL_CON4	0x0010	W	0x00007F00	PLL configuration register4
TOPCRU_CRU_GPLL_CON0	0x0020	W	0x00002063	PLL configuration register0
TOPCRU_CRU_GPLL_CON1	0x0024	W	0x00001081	PLL configuration register1
TOPCRU_CRU_GPLL_CON2	0x0028	W	0x00000000	PLL configuration register2
TOPCRU_CRU_GPLL_CON3	0x002C	W	0x00000007	PLL configuration register3
TOPCRU_CRU_GPLL_CON4	0x0030	W	0x00007F00	PLL configuration register4
TOPCRU_CRU_SSCGTBL_CON00	0x0140	W	0x00000000	External wave table register
TOPCRU_CRU_SSCGTBL_CON01	0x0144	W	0x00000000	External wave table register

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Name	Offset	Size	Reset Value	Description
TOPCRU_CRU_SSCGTBL_CON02	0x0148	W	0x00000000	External wave table register
TOPCRU_CRU_SSCGTBL_CON03	0x014C	W	0x00000000	External wave table register
TOPCRU_CRU_SSCGTBL_CON04	0x0150	W	0x00000000	External wave table register
TOPCRU_CRU_SSCGTBL_CON05	0x0154	W	0x00000000	External wave table register
TOPCRU_CRU_SSCGTBL_CON06	0x0158	W	0x00000000	External wave table register
TOPCRU_CRU_SSCGTBL_CON07	0x015C	W	0x00000000	External wave table register
TOPCRU_CRU_SSCGTBL_CON08	0x0160	W	0x00000000	External wave table register
TOPCRU_CRU_SSCGTBL_CON09	0x0164	W	0x00000000	External wave table register
TOPCRU_CRU_SSCGTBL_CON10	0x0168	W	0x00000000	External wave table register
TOPCRU_CRU_SSCGTBL_CON11	0x016C	W	0x00000000	External wave table register
TOPCRU_CRU_SSCGTBL_CON12	0x0170	W	0x00000000	External wave table register
TOPCRU_CRU_SSCGTBL_CON13	0x0174	W	0x00000000	External wave table register
TOPCRU_CRU_SSCGTBL_CON14	0x0178	W	0x00000000	External wave table register
TOPCRU_CRU_SSCGTBL_CON15	0x017C	W	0x00000000	External wave table register
TOPCRU_CRU_SSCGTBL_CON16	0x0180	W	0x00000000	External wave table register
TOPCRU_CRU_SSCGTBL_CON17	0x0184	W	0x00000000	External wave table register
TOPCRU_CRU_SSCGTBL_CON18	0x0188	W	0x00000000	External wave table register
TOPCRU_CRU_SSCGTBL_CON19	0x018C	W	0x00000000	External wave table register
TOPCRU_CRU_SSCGTBL_CON20	0x0190	W	0x00000000	External wave table register
TOPCRU_CRU_SSCGTBL_CON21	0x0194	W	0x00000000	External wave table register
TOPCRU_CRU_SSCGTBL_CON22	0x0198	W	0x00000000	External wave table register
TOPCRU_CRU_SSCGTBL_CON23	0x019C	W	0x00000000	External wave table register
TOPCRU_CRU_SSCGTBL_CON24	0x01A0	W	0x00000000	External wave table register
TOPCRU_CRU_SSCGTBL_CON25	0x01A4	W	0x00000000	External wave table register
TOPCRU_CRU_SSCGTBL_CON26	0x01A8	W	0x00000000	External wave table register
TOPCRU_CRU_SSCGTBL_CON27	0x01AC	W	0x00000000	External wave table register
TOPCRU_CRU_SSCGTBL_CON28	0x01B0	W	0x00000000	External wave table register

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Name	Offset	Size	Reset Value	Description
TOPCRU_CRU_SSCGTBL_CON29	0x01B4	W	0x00000000	External wave table register
TOPCRU_CRU_SSCGTBL_CON30	0x01B8	W	0x00000000	External wave table register
TOPCRU_CRU_SSCGTBL_CON31	0x01BC	W	0x00000000	External wave table register
TOPCRU_MODE_CON00	0x0280	W	0x00000000	Internal clock select and division register 0
TOPCRU_CLKSEL_CON00	0x0300	W	0x00000001	Internal clock select and division register 0
TOPCRU_CLKSEL_CON01	0x0304	W	0x00009D33	Internal clock select and division register 1
TOPCRU_CLKSEL_CON02	0x0308	W	0x00000CA7	Internal clock select and division register 2
TOPCRU_CLKSEL_CON03	0x030C	W	0x00000442	Internal clock select and division register 3
TOPCRU_CLKSEL_CON04	0x0310	W	0x00000001	Internal clock select and division register 4
TOPCRU_CLKSEL_CON10	0x0328	W	0x00000000	Internal clock select and division register 10
TOPCRU_CLKSEL_CON11	0x032C	W	0x00000101	Internal clock select and division register 11
TOPCRU_CLKSEL_CON12	0x0330	W	0x00000000	Internal clock select and division register 12
TOPCRU_CLKSEL_CON13	0x0334	W	0x00000000	Internal clock select and division register 13
TOPCRU_CLKSEL_CON14	0x0338	W	0x00000000	Internal clock select and division register 14
TOPCRU_CLKSEL_CON15	0x033C	W	0x00000000	Internal clock select and division register 15
TOPCRU_CLKSEL_CON16	0x0340	W	0x00000000	Internal clock select and division register 16
TOPCRU_CLKSEL_CON17	0x0344	W	0x00000000	Internal clock select and division register 17
TOPCRU_CLKSEL_CON18	0x0348	W	0x00000000	Internal clock select and division register 18
TOPCRU_CLKSEL_CON19	0x034C	W	0x00000000	Internal clock select and division register 19
TOPCRU_CLKSEL_CON20	0x0350	W	0x0000000B	Internal clock select and division register 20
TOPCRU_CLKSEL_CON21	0x0354	W	0x00000505	Internal clock select and division register 21
TOPCRU_CLKSEL_CON25	0x0364	W	0x001403DE	Internal clock select and division register 25
TOPCRU_CLKSEL_CON26	0x0368	W	0x001403DE	Internal clock select and division register 26
TOPCRU_CLKSEL_CON27	0x036C	W	0x001403DE	Internal clock select and division register 27
TOPCRU_CLKSEL_CON28	0x0370	W	0x001403DE	Internal clock select and division register 28
TOPCRU_CLKSEL_CON29	0x0374	W	0x001403DE	Internal clock select and division register 29
TOPCRU_CLKSEL_CON30	0x0378	W	0x03355460	Internal clock select and division register 30

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Name	Offset	Size	Reset Value	Description
TOPCRU_CLKSEL_CON31	0x037C	W	0x03355460	Internal clock select and division register 31
TOPCRU_CLKSEL_CON40	0x03A0	W	0x00004449	Internal clock select and division register 40
TOPCRU_CLKSEL_CON42	0x03A8	W	0x000000C2	Internal clock select and division register 42
TOPCRU_CLKSEL_CON43	0x03AC	W	0x00000007	Internal clock select and division register 43
TOPCRU_CLKSEL_CON44	0x03B0	W	0x00000009	Internal clock select and division register 44
TOPCRU_CLKSEL_CON45	0x03B4	W	0x00003802	Internal clock select and division register 45
TOPCRU_CLKSEL_CON46	0x03B8	W	0x00000002	Internal clock select and division register 46
TOPCRU_CLKSEL_CON47	0x03BC	W	0x00000002	Internal clock select and division register 47
TOPCRU_CLKSEL_CON48	0x03C0	W	0x00000003	Internal clock select and division register 48
TOPCRU_CLKSEL_CON49	0x03C4	W	0x00000505	Internal clock select and division register 49
TOPCRU_CLKSEL_CON50	0x03C8	W	0x00000000	Internal clock select and division register 50
TOPCRU_CLKSEL_CON51	0x03CC	W	0x00000009	Internal clock select and division register 51
TOPCRU_CLKSEL_CON60	0x03F0	W	0x00000041	Internal clock select and division register 60
TOPCRU_CLKSEL_CON61	0x03F4	W	0x00000082	Internal clock select and division register 61
TOPCRU_CLKSEL_CON62	0x03F8	W	0x00000701	Internal clock select and division register 62
TOPCRU_CLKSEL_CON63	0x03FC	W	0x00007000	Internal clock select and division register 63
TOPCRU_CLKSEL_CON67	0x040C	W	0x00001800	Internal clock select and division register 67
TOPCRU_CLKSEL_CON68	0x0410	W	0x00001800	Internal clock select and division register 68
TOPCRU_CLKSEL_CON69	0x0414	W	0x000000A0	Internal clock select and division register 69
TOPCRU_CLKSEL_CON70	0x0418	W	0x00000421	Internal clock select and division register 70
TOPCRU_GATE_CON00	0x0800	W	0x00004000	Internal clock gate and division register 0
TOPCRU_GATE_CON01	0x0804	W	0x00000000	Internal clock gate and division register 1
TOPCRU_GATE_CON02	0x0808	W	0x00000000	Internal clock gate and division register 2
TOPCRU_GATE_CON05	0x0814	W	0x00000000	Internal clock gate and division register 5
TOPCRU_GATE_CON06	0x0818	W	0x00000000	Internal clock gate and division register 6
TOPCRU_GATE_CON07	0x081C	W	0x00000000	Internal clock gate and division register 7
TOPCRU_GATE_CON08	0x0820	W	0x00000000	Internal clock gate and division register 8

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Name	Offset	Size	Reset Value	Description
TOPCRU_GATE_CON09	0x0824	W	0x00000000	Internal clock gate and division register 9
TOPCRU_GATE_CON15	0x083C	W	0x0000DFF8	Internal clock gate and division register 15
TOPCRU_SOFTRST_CON15	0x0A3C	W	0x00000000	Internal clock reset register 15
TOPCRU_CRU_GLB_CNT_TH	0x0C00	W	0x00640064	CRU_GLB_CNT_TH
TOPCRU_CRU_GLBRST_ST	0x0C04	W	0x00000000	CRU_GLBRST_ST
TOPCRU_CRU_GLB_SRST_FST_VALUE	0x0C08	W	0x00000000	CRU_GLB_SRST_FST_VALUE
TOPCRU_CRU_GLB_SRST_SND_VALUE	0x0C0C	W	0x00000000	CRU_GLB_SRST_SND_VALUE
TOPCRU_CRU_GLB_RST_CON0	0x0C10	W	0x00000000	CRU_GLB_RST_CON0
TOPCRU_CRU_GLB_RST_CON1	0x0C14	W	0x00000000	CRU_GLB_RST_CON1
TOPCRU_CRU_GLB_RST_CON2	0x0C18	W	0x00000000	CRU_GLB_RST_CON2
TOPCRU_CRU_GLB_RST_ST_NCLR	0x0C20	W	0x00000000	CRU_GLB_RST_ST_NCLR
TOPCRU_CLK_CM_FRAC_MATRIX0_DIV_HIGH	0x0CC0	W	0x00000000	FRAC_DIV_HIGH
TOPCRU_CLK_CM_FRAC_MATRIX1_DIV_HIGH	0x0CC4	W	0x00000000	FRAC_DIV_HIGH
TOPCRU_CLK_CM_FRAC_MATRIX2_DIV_HIGH	0x0CC8	W	0x00000000	FRAC_DIV_HIGH
TOPCRU_CLK_UART_FRAC_MATRIX0_DIV_HIGH	0x0CCC	W	0x00000000	FRAC_DIV_HIGH
TOPCRU_CLK_UART_FRAC_MATRIX1_DIV_HIGH	0x0CD0	W	0x00000000	FRAC_DIV_HIGH
TOPCRU_CLK_AUDIO_FRAC_MATRIX0_DIV_HIGH	0x0CD4	W	0x00000000	FRAC_DIV_HIGH
TOPCRU_CLK_AUDIO_FRAC_MATRIX1_DIV_HIGH	0x0CD8	W	0x00000000	FRAC_DIV_HIGH
TOPCRU_AUTOCS_ACLK_BUS_SRC_CON0	0x0D00	W	0x00A00047	bus clock auto clock swith control 0
TOPCRU_AUTOCS_ACLK_BUS_SRC_CON1	0x0D04	W	0x00000000	bus clock auto clock swith control 1
TOPCRU_AUTOCS_ACLK_GMAC_SRC_CON0	0x0D08	W	0x00A00047	bus clock auto clock swith control 0
TOPCRU_AUTOCS_ACLK_GMAC_SRC_CON1	0x0D0C	W	0x00000000	bus clock auto clock swith control 1
TOPCRU_AUTOCS_ACLK_PERI_SRC_CON0	0x0D10	W	0x00A00047	bus clock auto clock swith control 0
TOPCRU_AUTOCS_ACLK_PERI_SRC_CON1	0x0D14	W	0x00000000	bus clock auto clock swith control 1
TOPCRU_AUTOCS_ACLK_SYSMEM_SRC_CON0	0x0D18	W	0x00A00047	bus clock auto clock swith control 0
TOPCRU_AUTOCS_ACLK_SYSMEM_SRC_CON1	0x0D1C	W	0x00000000	bus clock auto clock swith control 1
TOPCRU_AUTOCS_ACLK_TOP_SRC_CON0	0x0D20	W	0x00A00047	bus clock auto clock swith control 0

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Name	Offset	Size	Reset Value	Description
TOPCRU_AUTOCS_ACLK_TOP_SRC_CON1	0x0D24	W	0x00000000	bus clock auto clock swith control 1
TOPCRU_AUTOCS_ACLK_VCP_SRC_CON0	0x0D28	W	0x00A00047	bus clock auto clock swith control 0
TOPCRU_AUTOCS_ACLK_VCP_SRC_CON1	0x0D2C	W	0x00000000	bus clock auto clock swith control 1
TOPCRU_AUTOCS_ACLK_VDO_SRC_CON0	0x0D30	W	0x00A00047	bus clock auto clock swith control 0
TOPCRU_AUTOCS_ACLK_VDO_SRC_CON1	0x0D34	W	0x00000000	bus clock auto clock swith control 1
TOPCRU_AUTOCS_ACLK_VEPU_SRC_CON0	0x0D38	W	0x00A00047	bus clock auto clock swith control 0
TOPCRU_AUTOCS_ACLK_VEPU_SRC_CON1	0x0D3C	W	0x00000000	bus clock auto clock swith control 1
TOPCRU_AUTOCS_ACLK_VI_SRC_CON0	0x0D40	W	0x00A00047	bus clock auto clock swith control 0
TOPCRU_AUTOCS_ACLK_VI_SRC_CON1	0x0D44	W	0x00000000	bus clock auto clock swith control 1
TOPCRU_AUTOCS_HCLK_BUS_SRC_CON0	0x0D48	W	0x00A00047	bus clock auto clock swith control 0
TOPCRU_AUTOCS_HCLK_BUS_SRC_CON1	0x0D4C	W	0x00000000	bus clock auto clock swith control 1
TOPCRU_AUTOCS_HCLK_VCP_SRC_CON0	0x0D50	W	0x00A00047	bus clock auto clock swith control 0
TOPCRU_AUTOCS_HCLK_VCP_SRC_CON1	0x0D54	W	0x00000000	bus clock auto clock swith control 1
TOPCRU_AUTOCS_HCLK_VEPU_SRC_CON0	0x0D58	W	0x00A00047	bus clock auto clock swith control 0
TOPCRU_AUTOCS_HCLK_VEPU_SRC_CON1	0x0D5C	W	0x00000000	bus clock auto clock swith control 1
TOPCRU_AUTOCS_HCLK_VI_SRC_CON0	0x0D60	W	0x00A00047	bus clock auto clock swith control 0
TOPCRU_AUTOCS_HCLK_VI_SRC_CON1	0x0D64	W	0x00000000	bus clock auto clock swith control 1
TOPCRU_AUTOCS_PCLK_DDR_SRC_CON0	0x0D68	W	0x00A00047	bus clock auto clock swith control 0
TOPCRU_AUTOCS_PCLK_DDR_SRC_CON1	0x0D6C	W	0x00000000	bus clock auto clock swith control 1
TOPCRU_AUTOCS_PCLK_VEPU_SRC_CON0	0x0D70	W	0x00A00047	bus clock auto clock swith control 0
TOPCRU_AUTOCS_PCLK_VEPU_SRC_CON1	0x0D74	W	0x00000000	bus clock auto clock swith control 1
TOPCRU_AUTOCS_PCLK_VI_SRC_CON0	0x0D78	W	0x00A00047	bus clock auto clock swith control 0
TOPCRU_AUTOCS_PCLK_VI_SRC_CON1	0x0D7C	W	0x00000000	bus clock auto clock swith control 1
TOPCRU_AUTOCS_CON_MISC	0x0E00	W	0x00000000	bus clock additional autocs_ctrl bits

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

2.4.1.3 Detail Registers Description

TOPCRU_CRU_AUPLL_CON0

Address: Operational Base(0x20000000) + offset (0x0000)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	bypass PLL Bypass. FREF bypasses PLL to FOUTPOSTDIV 1'b0: No bypass 1'b1: Bypass
14:12	RW	0x2	postdiv1 First Post Divide Value, (1-7)
11:0	RW	0x100	fbdiv Feedback Divide Value, valid divider settings are: [16, 2500] in integer mode [20, 500] in fractional mode Tips: No plus one operation

TOPCRU_CRU_AUPLL_CON1
Address: Operational Base(0x20000000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pllpdsel PLL global power down source selection If pllpdsel == 1, PLL can be power down only by pllpd1, otherwise pll is power down when any one of refdiv/fbdiv/fracdiv is changed or pllpd0 is asserted
14	RW	0x0	pllpd1 PLL global power down request 1'b0: No power down 1'b1: Power down
13	RW	0x0	pllpd0 PLL global power down request 1'b0: No power down 1'b1: Power down
12	RW	0x1	dsmpd PLL delta sigma modulator enable 1'b0: Modulator is enable 1'b1: Modulator is disabled
11	RO	0x0	reserved
10	RW	0x0	pll_lock PLL lock status 1'b0: Unlock 1'b1: Lock
9	RO	0x0	reserved
8:6	RW	0x2	postdiv2 Second Post Divide Value, (1-7)
5:0	RW	0x02	refdiv Reference Clock Divide Value, (1-63)

TOPCRU_CRU_AUPLL_CON2
Address: Operational Base(0x20000000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27	RW	0x0	fout4phasepd Power down 4-phase clocks and 2X, 3X, 4X clocks 1'b0: No power down 1'b1: Power down
26	RW	0x0	foutvcopd Power down buffered VCO clock 1'b0: No power down 1'b1: Power down
25	RW	0x0	foutpostdivpd Power down all outputs except for buffered VCO clock 1'b0: No power down 1'b1: Power down
24	RW	0x0	dacpd Power down quantization noise cancellation DAC 1'b0: No power down 1'b1: Power down
23:0	RW	0x000000	fracdiv Fractional part of feedback divide (fraction = FRAC/2^24)

TOPCRU_CRU_AUPLL_CON3
Address: Operational Base(0x20000000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x00	ssmod_spread spread amplitude % = 0.1 * SPREAD[4: 0]
7:4	RW	0x0	ssmod_divval Divider required to set the modulation frequency
3	RW	0x0	ssmod_downspread Selects center spread or downs pread 1'b0: Center spread 1'b1: Down spread
2	RW	0x1	ssmod_reset Reset modulator state 1'b0: No reset 1'b1: Reset
1	RW	0x1	ssmod_disable_sscg Bypass SSMOD by module 1'b0: No bypass 1'b1: Bypass
0	RW	0x1	ssmod_bp Bypass SSMOD by integration 1'b0: No bypass 1'b1: Bypass

TOPCRU_CRU_AUPLL_CON4
Address: Operational Base(0x20000000) + offset (0x0010)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x7f	ssmod_ext_maxaddr External wave table data inputs (0-255)
7:1	RO	0x00	reserved
0	RW	0x0	ssmod_sel_ext_wave select external wave 1'b0: No select ext_wave 1'b1: Select ext_wave

TOPCRU_CRU_GPLL_CON0
Address: Operational Base(0x20000000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	bypass PLL Bypass. FREF bypasses PLL to FOUTPOSTDIV 1'b0: No bypass 1'b1: Bypass
14:12	RW	0x2	postdiv1 First Post Divide Value, (1-7)
11:0	RW	0x063	fbdiv Feedback Divide Value, valid divider settings are: [16, 2500] in integer mode [20, 500] in fractional mode Tips: No plus one operation

TOPCRU_CRU_GPLL_CON1
Address: Operational Base(0x20000000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pllpdsel PLL global power down source selection If pllpdsel == 1, PLL can be power down only by pllpd1, otherwise pll is power down when any one of refdiv/fbdiv/fracdiv is changed or pllpd0 is asserted
14	RW	0x0	pllpd1 PLL global power down request 1'b0: No power down 1'b1: Power down
13	RW	0x0	pllpd0 PLL global power down request 1'b0: No power down 1'b1: Power down

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Bit	Attr	Reset Value	Description
12	RW	0x1	dsmpd PLL delta sigma modulator enable 1'b0: Modulator is enable 1'b1: Modulator is disabled
11	RO	0x0	reserved
10	RW	0x0	pll_lock PLL lock status 1'b0: Unlock 1'b1: Lock
9	RO	0x0	reserved
8:6	RW	0x2	postdiv2 Second Post Divide Value, (1-7)
5:0	RW	0x01	refdiv Reference Clock Divide Value, (1-63)

TOPCRU_CRU_GPLL_CON2
Address: Operational Base(0x20000000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	fout4phasepd Power down 4-phase clocks and 2X, 3X, 4X clocks 1'b0: No power down 1'b1: Power down
26	RW	0x0	foutvcopd Power down buffered VCO clock 1'b0: No power down 1'b1: Power down
25	RW	0x0	foutpostdivpd Power down all outputs except for buffered VCO clock 1'b0: No power down 1'b1: Power down
24	RW	0x0	dacpd Power down quantization noise cancellation DAC 1'b0: No power down 1'b1: Power down
23:0	RW	0x000000	fracdiv Fractional part of feedback divide (fraction = FRAC/2^24)

TOPCRU_CRU_GPLL_CON3
Address: Operational Base(0x20000000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x00	ssmod_spread spread amplitude % = 0.1 * SPREAD[4: 0]
7:4	RW	0x0	ssmod_divval Divider required to set the modulation frequency

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Bit	Attr	Reset Value	Description
3	RW	0x0	ssmod_downspread Selects center spread or downs pread 1'b0: Center spread 1'b1: Down spread
2	RW	0x1	ssmod_reset Reset modulator state 1'b0: No reset 1'b1: Reset
1	RW	0x1	ssmod_disable_sscg Bypass SSMOD by module 1'b0: No bypass 1'b1: Bypass
0	RW	0x1	ssmod_bp Bypass SSMOD by integration 1'b0: No bypass 1'b1: Bypass

TOPCRU_CRU_GPLL_CON4
Address: Operational Base(0x20000000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x7f	ssmod_ext_maxaddr External wave table data inputs (0-255)
7:1	RO	0x00	reserved
0	RW	0x0	ssmod_sel_ext_wave select external wave 1'b0: No select ext_wave 1'b1: Select ext_wave

TOPCRU_CRU_SSCGTBL_CON00
Address: Operational Base(0x20000000) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cru_sscgtbl_con00 External wave table register

TOPCRU_CRU_SSCGTBL_CON01
Address: Operational Base(0x20000000) + offset (0x0144)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cru_sscgtbl_con01 External wave table register

TOPCRU_CRU_SSCGTBL_CON02
Address: Operational Base(0x20000000) + offset (0x0148)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cru_sscgtbl_con02 External wave table register

TOPCRU_CRU_SSCGTBL_CON03
Address: Operational Base(0x20000000) + offset (0x014C)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cru_sscgtbl_con03 External wave table register

TOPCRU_CRU_SSCGTBL_CON04
Address: Operational Base(0x20000000) + offset (0x0150)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cru_sscgtbl_con04 External wave table register

TOPCRU_CRU_SSCGTBL_CON05
Address: Operational Base(0x20000000) + offset (0x0154)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cru_sscgtbl_con05 External wave table register

TOPCRU_CRU_SSCGTBL_CON06
Address: Operational Base(0x20000000) + offset (0x0158)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cru_sscgtbl_con06 External wave table register

TOPCRU_CRU_SSCGTBL_CON07
Address: Operational Base(0x20000000) + offset (0x015C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cru_sscgtbl_con07 External wave table register

TOPCRU_CRU_SSCGTBL_CON08
Address: Operational Base(0x20000000) + offset (0x0160)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cru_sscgtbl_con08 External wave table register

TOPCRU_CRU_SSCGTBL_CON09
Address: Operational Base(0x20000000) + offset (0x0164)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cru_sscgtbl_con09 External wave table register

TOPCRU_CRU_SSCGTBL_CON10
Address: Operational Base(0x20000000) + offset (0x0168)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cru_sscgtbl_con10 External wave table register

TOPCRU_CRU_SSCGTBL_CON11
Address: Operational Base(0x20000000) + offset (0x016C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cru_sscgtbl_con11 External wave table register

TOPCRU_CRU_SSCGTBL_CON12
Address: Operational Base(0x20000000) + offset (0x0170)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cru_sscgtbl_con12 External wave table register

TOPCRU_CRU_SSCGTBL_CON13
Address: Operational Base(0x20000000) + offset (0x0174)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cru_sscgtbl_con13 External wave table register

TOPCRU_CRU_SSCGTBL_CON14
Address: Operational Base(0x20000000) + offset (0x0178)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cru_sscgtbl_con14 External wave table register

TOPCRU_CRU_SSCGTBL_CON15
Address: Operational Base(0x20000000) + offset (0x017C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cru_sscgtbl_con15 External wave table register

TOPCRU_CRU_SSCGTBL_CON16
Address: Operational Base(0x20000000) + offset (0x0180)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cru_sscgtbl_con16 External wave table register

TOPCRU_CRU_SSCGTBL_CON17
Address: Operational Base(0x20000000) + offset (0x0184)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cru_sscgtbl_con17 External wave table register

TOPCRU_CRU_SSCGTBL_CON18
Address: Operational Base(0x20000000) + offset (0x0188)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cru_sscgtbl_con18 External wave table register

TOPCRU_CRU_SSCGTBL_CON19
Address: Operational Base(0x20000000) + offset (0x018C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cru_sscgtbl_con19 External wave table register

TOPCRU_CRU_SSCGTBL_CON20
Address: Operational Base(0x20000000) + offset (0x0190)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cru_sscgtbl_con20 External wave table register

TOPCRU_CRU_SSCGTBL_CON21
Address: Operational Base(0x20000000) + offset (0x0194)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cru_sscgtbl_con21 External wave table register

TOPCRU_CRU_SSCGTBL_CON22
Address: Operational Base(0x20000000) + offset (0x0198)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cru_sscgtbl_con22 External wave table register

TOPCRU_CRU_SSCGTBL_CON23
Address: Operational Base(0x20000000) + offset (0x019C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cru_sscgtbl_con23 External wave table register

TOPCRU_CRU_SSCGTBL_CON24
Address: Operational Base(0x20000000) + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cru_sscgtbl_con24 External wave table register

TOPCRU_CRU_SSCGTBL_CON25
Address: Operational Base(0x20000000) + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cru_sscgtbl_con25 External wave table register

TOPCRU_CRU_SSCGTBL_CON26
Address: Operational Base(0x20000000) + offset (0x01A8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cru_sscgtbl_con26 External wave table register

TOPCRU_CRU_SSCGTBL_CON27
Address: Operational Base(0x20000000) + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cru_sscgtbl_con27 External wave table register

TOPCRU_CRU_SSCGTBL_CON28
Address: Operational Base(0x20000000) + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cru_sscgtbl_con28 External wave table register

TOPCRU_CRU_SSCGTBL_CON29
Address: Operational Base(0x20000000) + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cru_sscgtbl_con29 External wave table register

TOPCRU_CRU_SSCGTBL_CON30
Address: Operational Base(0x20000000) + offset (0x01B8)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cru_sscgtbl_con30 External wave table register

TOPCRU_CRU_SSCGTBL_CON31
Address: Operational Base(0x20000000) + offset (0x01BC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cru_sscgtbl_con31 External wave table register

TOPCRU_MODE_CON00
Address: Operational Base(0x20000000) + offset (0x0280)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5:4	RW	0x0	clk_cpll_mode clk_cpll_mux clock mux. 2'b00: xin_osc0_func 2'b01: clk_cpll 2'b10: clk_deepslow
3:2	RW	0x0	clk_gpll_mode clk_gpll_mux clock mux. 2'b00: xin_osc0_func 2'b01: clk_gpll 2'b10: clk_deepslow
1:0	RW	0x0	clk_aupll_mode clk_aupll_mux clock mux. 2'b00: xin_osc0_func 2'b01: clk_aupll 2'b10: clk_deepslow

TOPCRU_CLKSEL_CON00
Address: Operational Base(0x20000000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:4	RW	0x0	clk_testout_top_sel clk_testout_top clock mux. 4'b0000: pclk_top_root 4'b0001: clk_mipi0_out2io 4'b0010: clk_mipi1_out2io 4'b0011: clk_mipi2_out2io 4'b0100: clk_mipi3_out2io 4'b0101: clk_cif_out2io 4'b0110: clk_mac_out2io 4'b0111: mclk_sai0_out2io 4'b1000: mclk_sai1_out2io 4'b1001: mclk_sai2_out2io 4'b1010: 1'b0 4'b1011: 1'b0

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Bit	Attr	Reset Value	Description
			4'b1100: 1'b0 4'b1101: 1'b0 4'b1110: 1'b0 4'b1111: 1'b0
3	RW	0x0	clk_ref_aupll_sel clk_ref_aupll clock mux. 1'b0: xin_osc0_ref_aupll 1'b1: xin_io_ref_aupll
2	RO	0x0	reserved
1:0	RW	0x1	clk_testout_top_div Divide clk_testout_top by (div_con + 1).

TOPCRU_CLKSEL_CON01
Address: Operational Base(0x20000000) + offset (0x0304)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	clk_cpll_div10_src_sel clk_cpll_div10_src clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
14:10	RW	0x07	clk_cpll_div8_src_div Divide clk_cpll_div8_src by (div_con + 1).
9:5	RW	0x09	clk_cpll_div10_src_div Divide clk_cpll_div10_src by (div_con + 1).
4:0	RW	0x13	clk_cpll_div20_src_div Divide clk_cpll_div20_src by (div_con + 1).

TOPCRU_CLKSEL_CON02
Address: Operational Base(0x20000000) + offset (0x0308)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:10	RW	0x03	clk_gpll_div4_src_div Divide clk_gpll_div4_src by (div_con + 1).
9:5	RW	0x05	clk_gpll_div6_src_div Divide clk_gpll_div6_src by (div_con + 1).
4:0	RW	0x07	clk_gpll_div8_src_div Divide clk_gpll_div8_src by (div_con + 1).

TOPCRU_CLKSEL_CON03
Address: Operational Base(0x20000000) + offset (0x030C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:10	RW	0x01	clk_cpll_div2_src_div Divide clk_cpll_div2_src by (div_con + 1).

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Bit	Attr	Reset Value	Description
9:5	RW	0x02	clk_gpll_div3_src_div Divide clk_gpll_div3_src by (div_con + 1).
4:0	RW	0x02	clk_cpll_div3_src_div Divide clk_cpll_div3_src by (div_con + 1).

TOPCRU_CLKSEL_CON04
Address: Operational Base(0x20000000) + offset (0x0310)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4:0	RW	0x01	clk_gpll_div2_src_div Divide clk_gpll_div2_src by (div_con + 1).

TOPCRU_CLKSEL_CON10
Address: Operational Base(0x20000000) + offset (0x0328)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:12	RW	0x0	clk_audio_frac_matrix1_sel clk_audio_frac_matrix1 clock mux. 2'b00: xin_osc0_func 2'b01: clk_gpll_mux 2'b10: clk_aupll_mux
11:10	RW	0x0	clk_audio_frac_matrix0_sel clk_audio_frac_matrix0 clock mux. 2'b00: xin_osc0_func 2'b01: clk_gpll_mux 2'b10: clk_aupll_mux
9:8	RW	0x0	clk_uart_frac_matrix1_sel clk_uart_frac_matrix1 clock mux. 2'b00: xin_osc0_func 2'b01: clk_gpll_mux 2'b10: clk_cpll_mux
7:6	RW	0x0	clk_uart_frac_matrix0_sel clk_uart_frac_matrix0 clock mux. 2'b00: xin_osc0_func 2'b01: clk_gpll_mux 2'b10: clk_cpll_mux
5:4	RW	0x0	clk_cm_frac_matrix2_sel clk_cm_frac_matrix2 clock mux. 2'b00: xin_osc0_func 2'b01: clk_gpll_mux 2'b10: clk_aupll_mux 2'b11: clk_cpll_mux

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	clk_cm_frac_matrix1_sel clk_cm_frac_matrix1 clock mux. 2'b00: xin_osc0_func 2'b01: clk_gpll_mux 2'b10: clk_aupll_mux 2'b11: clk_cpll_mux
1:0	RW	0x0	clk_cm_frac_matrix0_sel clk_cm_frac_matrix0 clock mux. 2'b00: xin_osc0_func 2'b01: clk_gpll_mux 2'b10: clk_aupll_mux 2'b11: clk_cpll_mux

TOPCRU_CLKSEL_CON11
Address: Operational Base(0x20000000) + offset (0x032C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clk_audio_int_matrix1_sel clk_audio_int_matrix1 clock mux. 2'b00: xin_osc0_func 2'b01: clk_gpll_mux 2'b10: clk_aupll_mux
13	RO	0x0	reserved
12:8	RW	0x01	clk_audio_int_matrix1_div DT50 division register. Divide clk_audio_int_matrix1 by (div_con + 1).
7:6	RW	0x0	clk_audio_int_matrix0_sel clk_audio_int_matrix0 clock mux. 2'b00: xin_osc0_func 2'b01: clk_gpll_mux 2'b10: clk_aupll_mux
5	RO	0x0	reserved
4:0	RW	0x01	clk_audio_int_matrix0_div DT50 division register. Divide clk_audio_int_matrix0 by (div_con + 1).

TOPCRU_CLKSEL_CON12
Address: Operational Base(0x20000000) + offset (0x0330)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RW	0x0	sclk_uart1_src_sel sclk_uart1_src clock mux. 3'b000: xin_osc0_func 3'b001: clk_cm_frac_matrix0 3'b010: clk_cm_frac_matrix1 3'b011: clk_cm_frac_matrix2 3'b100: clk_uart_frac_matrix0 3'b101: clk_uart_frac_matrix1

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Bit	Attr	Reset Value	Description
12:8	RW	0x00	sclk_uart1_src_div Divide sclk_uart1_src by (div_con + 1).
7:5	RW	0x0	sclk_uart0_src_sel sclk_uart0_src clock mux. 3'b000: xin_osc0_func 3'b001: clk_cm_frac_matrix0 3'b010: clk_cm_frac_matrix1 3'b011: clk_cm_frac_matrix2 3'b100: clk_uart_frac_matrix0 3'b101: clk_uart_frac_matrix1
4:0	RW	0x00	sclk_uart0_src_div Divide sclk_uart0_src by (div_con + 1).

TOPCRU_CLKSEL_CON13

Address: Operational Base(0x20000000) + offset (0x0334)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RW	0x0	sclk_uart3_src_sel sclk_uart3_src clock mux. 3'b000: xin_osc0_func 3'b001: clk_cm_frac_matrix0 3'b010: clk_cm_frac_matrix1 3'b011: clk_cm_frac_matrix2 3'b100: clk_uart_frac_matrix0 3'b101: clk_uart_frac_matrix1
12:8	RW	0x00	sclk_uart3_src_div Divide sclk_uart3_src by (div_con + 1).
7:5	RW	0x0	sclk_uart2_src_sel sclk_uart2_src clock mux. 3'b000: xin_osc0_func 3'b001: clk_cm_frac_matrix0 3'b010: clk_cm_frac_matrix1 3'b011: clk_cm_frac_matrix2 3'b100: clk_uart_frac_matrix0 3'b101: clk_uart_frac_matrix1
4:0	RW	0x00	sclk_uart2_src_div Divide sclk_uart2_src by (div_con + 1).

TOPCRU_CLKSEL_CON14

Address: Operational Base(0x20000000) + offset (0x0338)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RW	0x0	sclk_uart5_src_sel sclk_uart5_src clock mux. 3'b000: xin_osc0_func 3'b001: clk_cm_frac_matrix0 3'b010: clk_cm_frac_matrix1 3'b011: clk_cm_frac_matrix2 3'b100: clk_uart_frac_matrix0 3'b101: clk_uart_frac_matrix1

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Bit	Attr	Reset Value	Description
12:8	RW	0x00	sclk_uart5_src_div Divide sclk_uart5_src by (div_con + 1).
7:5	RW	0x0	sclk_uart4_src_sel sclk_uart4_src clock mux. 3'b000: xin_osc0_func 3'b001: clk_cm_frac_matrix0 3'b010: clk_cm_frac_matrix1 3'b011: clk_cm_frac_matrix2 3'b100: clk_uart_frac_matrix0 3'b101: clk_uart_frac_matrix1
4:0	RW	0x00	sclk_uart4_src_div Divide sclk_uart4_src by (div_con + 1).

TOPCRU_CLKSEL_CON15

Address: Operational Base(0x20000000) + offset (0x033C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RW	0x0	sclk_uart7_src_sel sclk_uart7_src clock mux. 3'b000: xin_osc0_func 3'b001: clk_cm_frac_matrix0 3'b010: clk_cm_frac_matrix1 3'b011: clk_cm_frac_matrix2 3'b100: clk_uart_frac_matrix0 3'b101: clk_uart_frac_matrix1
12:8	RW	0x00	sclk_uart7_src_div Divide sclk_uart7_src by (div_con + 1).
7:5	RW	0x0	sclk_uart6_src_sel sclk_uart6_src clock mux. 3'b000: xin_osc0_func 3'b001: clk_cm_frac_matrix0 3'b010: clk_cm_frac_matrix1 3'b011: clk_cm_frac_matrix2 3'b100: clk_uart_frac_matrix0 3'b101: clk_uart_frac_matrix1
4:0	RW	0x00	sclk_uart6_src_div Divide sclk_uart6_src by (div_con + 1).

TOPCRU_CLKSEL_CON16

Address: Operational Base(0x20000000) + offset (0x0340)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:12	RW	0x0	mclk_asrc0_src_sel mclk_asrc0_src clock mux. 4'b0000: xin_osc0_func 4'b0001: clk_cm_frac_matrix0 4'b0010: clk_cm_frac_matrix1 4'b0011: clk_cm_frac_matrix2 4'b0100: clk_audio_frac_matrix0 4'b0101: clk_audio_frac_matrix1 4'b0110: clk_audio_int_matrix0 4'b0111: clk_audio_int_matrix1 4'b1000: mclk_sai0_from_io 4'b1001: mclk_sai1_from_io 4'b1010: mclk_sai2_from_io
11:8	RW	0x0	mclk_sai0_src_sel mclk_sai0_src clock mux. 4'b0000: xin_osc0_func 4'b0001: clk_cm_frac_matrix0 4'b0010: clk_cm_frac_matrix1 4'b0011: clk_cm_frac_matrix2 4'b0100: clk_audio_frac_matrix0 4'b0101: clk_audio_frac_matrix1 4'b0110: clk_audio_int_matrix0 4'b0111: clk_audio_int_matrix1 4'b1000: mclk_sai0_from_io
7:0	RW	0x00	mclk_sai0_src_div Divide mclk_sai0_src by (div_con + 1).

TOPCRU_CLKSEL_CON17

Address: Operational Base(0x20000000) + offset (0x0344)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	mclk_asrc1_src_sel mclk_asrc1_src clock mux. 4'b0000: xin_osc0_func 4'b0001: clk_cm_frac_matrix0 4'b0010: clk_cm_frac_matrix1 4'b0011: clk_cm_frac_matrix2 4'b0100: clk_audio_frac_matrix0 4'b0101: clk_audio_frac_matrix1 4'b0110: clk_audio_int_matrix0 4'b0111: clk_audio_int_matrix1 4'b1000: mclk_sai0_from_io 4'b1001: mclk_sai1_from_io 4'b1010: mclk_sai2_from_io

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Bit	Attr	Reset Value	Description
11:8	RW	0x0	mclk_sai1_src_sel mclk_sai1_src clock mux. 4'b0000: xin_osc0_func 4'b0001: clk_cm_frac_matrix0 4'b0010: clk_cm_frac_matrix1 4'b0011: clk_cm_frac_matrix2 4'b0100: clk_audio_frac_matrix0 4'b0101: clk_audio_frac_matrix1 4'b0110: clk_audio_int_matrix0 4'b0111: clk_audio_int_matrix1 4'b1000: mclk_sai1_from_io
7:0	RW	0x00	mclk_sai1_src_div Divide mclk_sai1_src by (div_con + 1).

TOPCRU_CLKSEL_CON18

Address: Operational Base(0x20000000) + offset (0x0348)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	mclk_asrc2_src_sel mclk_asrc2_src clock mux. 4'b0000: xin_osc0_func 4'b0001: clk_cm_frac_matrix0 4'b0010: clk_cm_frac_matrix1 4'b0011: clk_cm_frac_matrix2 4'b0100: clk_audio_frac_matrix0 4'b0101: clk_audio_frac_matrix1 4'b0110: clk_audio_int_matrix0 4'b0111: clk_audio_int_matrix1 4'b1000: mclk_sai0_from_io 4'b1001: mclk_sai1_from_io 4'b1010: mclk_sai2_from_io
11:8	RW	0x0	mclk_sai2_src_sel mclk_sai2_src clock mux. 4'b0000: xin_osc0_func 4'b0001: clk_cm_frac_matrix0 4'b0010: clk_cm_frac_matrix1 4'b0011: clk_cm_frac_matrix2 4'b0100: clk_audio_frac_matrix0 4'b0101: clk_audio_frac_matrix1 4'b0110: clk_audio_int_matrix0 4'b0111: clk_audio_int_matrix1 4'b1000: mclk_sai2_from_io
7:0	RW	0x00	mclk_sai2_src_div Divide mclk_sai2_src by (div_con + 1).

TOPCRU_CLKSEL_CON19

Address: Operational Base(0x20000000) + offset (0x034C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:12	RW	0x0	mclk_asrc3_src_sel mclk_asrc3_src clock mux. 4'b0000: xin_osc0_func 4'b0001: clk_cm_frac_matrix0 4'b0010: clk_cm_frac_matrix1 4'b0011: clk_cm_frac_matrix2 4'b0100: clk_audio_frac_matrix0 4'b0101: clk_audio_frac_matrix1 4'b0110: clk_audio_int_matrix0 4'b0111: clk_audio_int_matrix1 4'b1000: mclk_sai0_from_io 4'b1001: mclk_sai1_from_io 4'b1010: mclk_sai2_from_io
11:10	RO	0x0	reserved
9:6	RW	0x0	mclk_pdm_src_sel mclk_pdm_src clock mux. 4'b0000: xin_osc0_func 4'b0001: clk_cm_frac_matrix0 4'b0010: clk_cm_frac_matrix1 4'b0011: clk_cm_frac_matrix2 4'b0100: clk_audio_frac_matrix0 4'b0101: clk_audio_frac_matrix1 4'b0110: clk_audio_int_matrix0 4'b0111: clk_audio_int_matrix1 4'b1000: mclk_sai0_from_io 4'b1001: mclk_sai1_from_io 4'b1010: mclk_sai2_from_io
5	RO	0x0	reserved
4:0	RW	0x00	mclk_pdm_src_div Divide mclk_pdm_src by (div_con + 1).

TOPCRU_CLKSEL_CON20

Address: Operational Base(0x20000000) + offset (0x0350)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:8	RW	0x0	clkout_pdm_src_sel clkout_pdm_src clock mux. 4'b0000: xin_osc0_func 4'b0001: clk_cm_frac_matrix0 4'b0010: clk_cm_frac_matrix1 4'b0011: clk_cm_frac_matrix2 4'b0100: clk_audio_frac_matrix0 4'b0101: clk_audio_frac_matrix1 4'b0110: clk_audio_int_matrix0 4'b0111: clk_audio_int_matrix1 4'b1000: mclk_sai0_from_io 4'b1001: mclk_sai1_from_io 4'b1010: mclk_sai2_from_io
7:0	RW	0x0b	clkout_pdm_src_div Divide clkout_pdm_src by (div_con + 1).

TOPCRU_CLKSEL_CON21

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Address: Operational Base(0x20000000) + offset (0x0354)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	clk_asrc1_src_sel clk_asrc1_src clock mux. 1'b0: clk_gpll_mux 1'b1: clk_aupll_mux
13	RO	0x0	reserved
12:8	RW	0x05	clk_asrc1_src_div Divide clk_asrc1_src by (div_con + 1).
7	RO	0x0	reserved
6	RW	0x0	clk_asrc0_src_sel clk_asrc0_src clock mux. 1'b0: clk_gpll_mux 1'b1: clk_aupll_mux
5	RO	0x0	reserved
4:0	RW	0x05	clk_asrc0_src_div Divide clk_asrc0_src by (div_con + 1).

TOPCRU_CLKSEL_CON25

Address: Operational Base(0x20000000) + offset (0x0364)

Bit	Attr	Reset Value	Description
31:0	RW	0x001403de	clk_cm_frac_matrix0_div clk_cm_frac_matrix0 fraction division register. High 16-bit for numerator Low 16-bit for denominator

TOPCRU_CLKSEL_CON26

Address: Operational Base(0x20000000) + offset (0x0368)

Bit	Attr	Reset Value	Description
31:0	RW	0x001403de	clk_cm_frac_matrix1_div clk_cm_frac_matrix1 fraction division register. High 16-bit for numerator Low 16-bit for denominator

TOPCRU_CLKSEL_CON27

Address: Operational Base(0x20000000) + offset (0x036C)

Bit	Attr	Reset Value	Description
31:0	RW	0x001403de	clk_cm_frac_matrix2_div clk_cm_frac_matrix2 fraction division register. High 16-bit for numerator Low 16-bit for denominator

TOPCRU_CLKSEL_CON28

Address: Operational Base(0x20000000) + offset (0x0370)

Bit	Attr	Reset Value	Description
31:0	RW	0x001403de	clk_uart_frac_matrix0_div clk_uart_frac_matrix0 fraction division register. High 16-bit for numerator Low 16-bit for denominator

TOPCRU_CLKSEL_CON29

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Address: Operational Base(0x20000000) + offset (0x0374)

Bit	Attr	Reset Value	Description
31:0	RW	0x001403de	clk_uart_frac_matrix1_div clk_uart_frac_matrix1 fraction division register. High 16-bit for numerator Low 16-bit for denominator

TOPCRU_CLKSEL_CON30

Address: Operational Base(0x20000000) + offset (0x0378)

Bit	Attr	Reset Value	Description
31:0	RW	0x03355460	clk_audio_frac_matrix0_div clk_audio_frac_matrix0 fraction division register. High 16-bit for numerator Low 16-bit for denominator

TOPCRU_CLKSEL_CON31

Address: Operational Base(0x20000000) + offset (0x037C)

Bit	Attr	Reset Value	Description
31:0	RW	0x03355460	clk_audio_frac_matrix1_div clk_audio_frac_matrix1 fraction division register. High 16-bit for numerator Low 16-bit for denominator

TOPCRU_CLKSEL_CON40

Address: Operational Base(0x20000000) + offset (0x03A0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	clk_sys_dsmc_src_sel clk_sys_dsmc_src clock mux. 2'b00: xin_osc0_func 2'b01: clk_gpll_mux 2'b10: clk_cpll_mux
13:9	RW	0x02	clk_sys_dsmc_src_div DT50 division register. Divide clk_sys_dsmc_src by (div_con + 1).
8:7	RW	0x0	aclk_vi_src_sel aclk_vi_src clock mux. 2'b00: clk_cpll_div2_src 2'b01: clk_gpll_div3_src 2'b10: clk_gpll_div4_src
6	RW	0x1	aclk_gmac_src_sel aclk_gmac_src clock mux. 1'b0: clk_gpll_div4_src 1'b1: clk_gpll_div6_src
5	RW	0x0	clk_core_rga_src_sel clk_core_rga_src clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
4:2	RW	0x2	clk_core_rga_src_div Divide clk_core_rga_src by (div_con + 1).

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Bit	Attr	Reset Value	Description
1:0	RW	0x1	aclk_vepu_src_sel aclk_vepu_src clock mux. 2'b00: clk_cpll_div2_src 2'b01: clk_gpll_div3_src 2'b10: clk_gpll_div6_src

TOPCRU_CLKSEL_CON42
Address: Operational Base(0x20000000) + offset (0x03A8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10	RW	0x0	aclk_rkvdec_src_sel aclk_rkvdec_src clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
9:6	RW	0x3	aclk_rkvdec_src_div Divide aclk_rkvdec_src by (div_con + 1).
5	RW	0x0	dclk_vicap_src_sel dclk_vicap_src clock mux. 1'b0: clk_cpll_div3_src 1'b1: clk_gpll_div6_src
4	RW	0x0	aclk_vdo_src_sel aclk_vdo_src clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
3:0	RW	0x2	aclk_vdo_src_div Divide aclk_vdo_src by (div_con + 1).

TOPCRU_CLKSEL_CON43
Address: Operational Base(0x20000000) + offset (0x03AC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	dclk_vop_src_sel dclk_vop_src clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
7:0	RW	0x07	dclk_vop_src_div Divide dclk_vop_src by (div_con + 1).

TOPCRU_CLKSEL_CON44
Address: Operational Base(0x20000000) + offset (0x03B0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
10	RW	0x0	hclk_bus_src_sel hclk_bus_src clock mux. 1'b0: clk_gpll_div6_src 1'b1: clk_cpll_div10_src
9:8	RW	0x0	aclk_bus_src_sel aclk_bus_src clock mux. 2'b00: clk_gpll_div3_src 2'b01: clk_gpll_div4_src 2'b10: clk_gpll_div6_src
7:6	RW	0x0	aclk_top_src_sel aclk_top_src clock mux. 2'b00: clk_gpll_div2_src 2'b01: clk_gpll_div3_src 2'b10: clk_gpll_div6_src
5:4	RO	0x0	reserved
3	RW	0x1	aclk_sysmem_src_sel aclk_sysmem_src clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
2:0	RW	0x1	aclk_sysmem_src_div Divide aclk_sysmem_src by (div_con + 1).

TOPCRU_CLKSEL_CON45

Address: Operational Base(0x20000000) + offset (0x03B4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RW	0x07	clk_gmac_ptp_ref_src_div Divide clk_gmac_ptp_ref_src by (div_con + 1).
10	RW	0x0	clk_gmac_ptp_ref_src_sel clk_gmac_ptp_ref_src clock mux. 1'b0: clk_cpll_mux 1'b1: xin_osc0_func
9:8	RW	0x0	cclk_sdmmc0_src_sel cclk_sdmmc0_src clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: xin_osc0_func
7:0	RW	0x02	cclk_sdmmc0_src_div DT50 division register. Divide cclk_sdmmc0_src by (div_con + 1).

TOPCRU_CLKSEL_CON46

Address: Operational Base(0x20000000) + offset (0x03B8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14	RW	0x0	tclk_wdt_hpmcu_src_sel tclk_wdt_hpmcu_src clock mux. 1'b0: clk_cpll_div10_src 1'b1: xin_osc0_func
13	RW	0x0	tclk_wdt_s_src_sel tclk_wdt_s_src clock mux. 1'b0: clk_cpll_div10_src 1'b1: xin_osc0_func
12	RW	0x0	tclk_wdt_ns_src_sel tclk_wdt_ns_src clock mux. 1'b0: clk_cpll_div10_src 1'b1: xin_osc0_func
11	RW	0x0	clk_timer_src_sel clk_timer_src clock mux. 1'b0: clk_cpll_div10_src 1'b1: xin_osc0_func
10	RO	0x0	reserved
9:8	RW	0x0	cclk_sdmmc1_src_sel cclk_sdmmc1_src clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: xin_osc0_func
7:0	RW	0x02	cclk_sdmmc1_src_div DT50 division register. Divide cclk_sdmmc1_src by (div_con + 1).

TOPCRU_CLKSEL_CON47
Address: Operational Base(0x20000000) + offset (0x03BC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	aclk_peri_src_sel aclk_peri_src clock mux. 1'b0: clk_gpll_div6_src 1'b1: xin_osc0_func
12	RW	0x0	pclk_peri_src_sel pclk_peri_src clock mux. 1'b0: clk_cpll_div10_src 1'b1: xin_osc0_func
11:10	RO	0x0	reserved
9:8	RW	0x0	cclk_emmc_src_sel cclk_emmc_src clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: xin_osc0_func
7:0	RW	0x02	cclk_emmc_src_div DT50 division register. Divide cclk_emmc_src by (div_con + 1).

TOPCRU_CLKSEL_CON48
Address: Operational Base(0x20000000) + offset (0x03C0)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:12	RW	0x0	aclk_vcp_src_sel aclk_vcp_src clock mux. 2'b00: clk_cpll_div2_src 2'b01: clk_gpll_div3_src 2'b10: clk_gpll_div6_src
11:10	RO	0x0	reserved
9:8	RW	0x0	sclk_2x_fspi0_src_sel sclk_2x_fspi0_src clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: xin_osc0_func
7:0	RW	0x03	sclk_2x_fspi0_src_div DT50 division register. Divide sclk_2x_fspi0_src by (div_con + 1).

TOPCRU_CLKSEL_CON49
Address: Operational Base(0x20000000) + offset (0x03C4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	clk_can1_src_sel clk_can1_src clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: xin_osc0_func
13	RO	0x0	reserved
12:8	RW	0x05	clk_can1_src_div Divide clk_can1_src by (div_con + 1).
7:6	RW	0x0	clk_can0_src_sel clk_can0_src clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: xin_osc0_func
5	RO	0x0	reserved
4:0	RW	0x05	clk_can0_src_div Divide clk_can0_src by (div_con + 1).

TOPCRU_CLKSEL_CON50
Address: Operational Base(0x20000000) + offset (0x03C8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13	RW	0x0	aclk_rkce_src_sel aclk_rkce_src clock mux. 1'b0: clk_gpll_div6_src 1'b1: xin_osc0_func
12	RW	0x0	clk_pka_rkce_src_sel clk_pka_rkce_src clock mux. 1'b0: clk_gpll_div4_src 1'b1: clk_gpll_div6_src
11	RW	0x0	clk_pwm3_src_sel clk_pwm3_src clock mux. 1'b0: clk_cpll_div10_src 1'b1: xin_osc0_func
10	RW	0x0	clk_pwm2_src_sel clk_pwm2_src clock mux. 1'b0: clk_cpll_div10_src 1'b1: xin_osc0_func
9	RO	0x0	reserved
8	RW	0x0	clk_pwm0_src_sel clk_pwm0_src clock mux. 1'b0: clk_cpll_div10_src 1'b1: xin_osc0_func
7:6	RO	0x0	reserved
5:4	RW	0x0	clk_spi1_src_sel clk_spi1_src clock mux. 2'b00: clk_gpll_div6_src 2'b01: clk_cpll_div10_src 2'b10: clk_cpll_div20_src 2'b11: xin_osc0_func
3:2	RW	0x0	clk_spi0_src_sel clk_spi0_src clock mux. 2'b00: clk_gpll_div6_src 2'b01: clk_cpll_div10_src 2'b10: clk_cpll_div20_src 2'b11: xin_osc0_func
1	RW	0x0	clk_i2c_bus_src_sel clk_i2c_bus_src clock mux. 1'b0: clk_gpll_div6_src 1'b1: xin_osc0_func
0	RO	0x0	reserved

TOPCRU_CLKSEL_CON51

Address: Operational Base(0x20000000) + offset (0x03CC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x1	clk_core_fec_src_sel clk_core_fec_src clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
2:0	RW	0x1	clk_core_fec_src_div Divide clk_core_fec_src by (div_con + 1).

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TOPCRU_CLKSEL_CON60
Address: Operational Base(0x20000000) + offset (0x03F0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8:6	RW	0x1	clk_npu_pll_src_div Divide clk_npu_pll_src by (div_con + 1).
5:3	RO	0x0	reserved
2:0	RW	0x1	clk_core_pll_src_div Divide clk_core_pll_src by (div_con + 1).

TOPCRU_CLKSEL_CON61
Address: Operational Base(0x20000000) + offset (0x03F4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:10	RW	0x0	clk_isp_pll_src_sel clk_isp_pll_src clock mux. 2'b00: clk_gpll_mux 2'b01: clk_aupll_mux 2'b10: clk_cpll_mux
9:6	RW	0x2	clk_isp_pll_src_div Divide clk_isp_pll_src by (div_con + 1).
5:4	RW	0x0	clk_vepu_pll_src_sel clk_vepu_pll_src clock mux. 2'b00: clk_gpll_mux 2'b01: clk_aupll_mux 2'b10: clk_cpll_mux
3	RO	0x0	reserved
2:0	RW	0x2	clk_vepu_pll_src_div Divide clk_vepu_pll_src by (div_con + 1).

TOPCRU_CLKSEL_CON62
Address: Operational Base(0x20000000) + offset (0x03F8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x07	dclk_ooc_src_div DT50 division register. Divide dclk_ooc_src by (div_con + 1).
7	RW	0x0	dclk_ooc_src_sel dclk_ooc_src clock mux. 1'b0: clk_gpll_mux 1'b1: clk_cpll_mux
6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:4	RW	0x0	clk_aiisp_pll_src_sel clk_aiisp_pll_src clock mux. 2'b00: clk_gpll_mux 2'b01: clk_aupll_mux 2'b10: clk_cpll_mux
3	RO	0x0	reserved
2:0	RW	0x1	clk_aiisp_pll_src_div Divide clk_aiisp_pll_src by (div_con + 1).

TOPCRU_CLKSEL_CON63

Address: Operational Base(0x20000000) + offset (0x03FC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x1	clk_saradc2_src_sel clk_saradc2_src clock mux. 1'b0: clk_gpll_div6_src 1'b1: xin_osc0_func
13	RW	0x1	clk_saradc1_src_sel clk_saradc1_src clock mux. 1'b0: clk_gpll_div6_src 1'b1: xin_osc0_func
12	RW	0x1	clk_saradc0_src_sel clk_saradc0_src clock mux. 1'b0: clk_gpll_div6_src 1'b1: xin_osc0_func
11	RO	0x0	reserved
10:8	RW	0x0	clk_saradc2_src_div Divide clk_saradc2_src by (div_con + 1).
7	RO	0x0	reserved
6:4	RW	0x0	clk_saradc1_src_div Divide clk_saradc1_src by (div_con + 1).
3	RO	0x0	reserved
2:0	RW	0x0	clk_saradc0_src_div Divide clk_saradc0_src by (div_con + 1).

TOPCRU_CLKSEL_CON67

Address: Operational Base(0x20000000) + offset (0x040C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x1	clk_mipi1_out2io_sel clk_mipi1_out2io clock mux. 1'b0: clk_gpll_div2_src 1'b1: xin_osc0_func
11	RW	0x1	clk_mipi0_out2io_sel clk_mipi0_out2io clock mux. 1'b0: clk_gpll_div2_src 1'b1: xin_osc0_func

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Bit	Attr	Reset Value	Description
10:6	RW	0x00	clk_mipi1_out2io_div Divide clk_mipi1_out2io by (div_con + 1).
5	RO	0x0	reserved
4:0	RW	0x00	clk_mipi0_out2io_div Divide clk_mipi0_out2io by (div_con + 1).

TOPCRU_CLKSEL_CON68
Address: Operational Base(0x20000000) + offset (0x0410)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x1	clk_mipi3_out2io_sel clk_mipi3_out2io clock mux. 1'b0: clk_gpll_div2_src 1'b1: xin_osc0_func
11	RW	0x1	clk_mipi2_out2io_sel clk_mipi2_out2io clock mux. 1'b0: clk_gpll_div2_src 1'b1: xin_osc0_func
10:6	RW	0x00	clk_mipi3_out2io_div Divide clk_mipi3_out2io by (div_con + 1).
5	RO	0x0	reserved
4:0	RW	0x00	clk_mipi2_out2io_div Divide clk_mipi2_out2io by (div_con + 1).

TOPCRU_CLKSEL_CON69
Address: Operational Base(0x20000000) + offset (0x0414)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:8	RW	0x00	clk_mac_out2io_div Divide clk_mac_out2io by (div_con + 1).
7:6	RW	0x2	clk_mac_out2io_sel clk_mac_out2io clock mux. 2'b00: clk_gpll_mux 2'b01: clk_cpll_mux 2'b10: xin_osc0_func
5	RW	0x1	clk_cif_out2io_sel clk_cif_out2io clock mux. 1'b0: clk_gpll_div2_src 1'b1: xin_osc0_func
4:0	RW	0x00	clk_cif_out2io_div Divide clk_cif_out2io by (div_con + 1).

TOPCRU_CLKSEL_CON70
Address: Operational Base(0x20000000) + offset (0x0418)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:10	RW	0x1	mclk_sai2_out2io_div Divide mclk_sai2_out2io by (div_con + 1).
9	RO	0x0	reserved
8:5	RW	0x1	mclk_sai1_out2io_div Divide mclk_sai1_out2io by (div_con + 1).
4	RO	0x0	reserved
3:0	RW	0x1	mclk_sai0_out2io_div Divide mclk_sai0_out2io by (div_con + 1).

TOPCRU_GATE_CON00

Address: Operational Base(0x20000000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x1	clk_testout_top_en clk_testout_top clock gating control. When high, disable clock
13:10	RO	0x0	reserved
9	RW	0x0	clk_gpll_div2_src_en clk_gpll_div2_src clock gating control. When high, disable clock
8	RW	0x0	clk_cpll_div2_src_en clk_cpll_div2_src clock gating control. When high, disable clock
7	RW	0x0	clk_gpll_div3_src_en clk_gpll_div3_src clock gating control. When high, disable clock
6	RW	0x0	clk_cpll_div3_src_en clk_cpll_div3_src clock gating control. When high, disable clock
5	RW	0x0	clk_gpll_div4_src_en clk_gpll_div4_src clock gating control. When high, disable clock
4	RW	0x0	clk_gpll_div6_src_en clk_gpll_div6_src clock gating control. When high, disable clock
3	RW	0x0	clk_gpll_div8_src_en clk_gpll_div8_src clock gating control. When high, disable clock
2	RW	0x0	clk_cpll_div8_src_en clk_cpll_div8_src clock gating control. When high, disable clock
1	RW	0x0	clk_cpll_div10_src_en clk_cpll_div10_src clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
0	RW	0x0	clk_cpll_div20_src_en clk_cpll_div20_src clock gating control. When high, disable clock

TOPCRU_GATE_CON01

Address: Operational Base(0x20000000) + offset (0x0804)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	sclk_uart5_src_en sclk_uart5_src clock gating control. When high, disable clock
13	RW	0x0	sclk_uart4_src_en sclk_uart4_src clock gating control. When high, disable clock
12	RW	0x0	sclk_uart3_src_en sclk_uart3_src clock gating control. When high, disable clock
11	RW	0x0	sclk_uart2_src_en sclk_uart2_src clock gating control. When high, disable clock
10	RW	0x0	sclk_uart1_src_en sclk_uart1_src clock gating control. When high, disable clock
9	RW	0x0	sclk_uart0_src_en sclk_uart0_src clock gating control. When high, disable clock
8	RW	0x0	clk_audio_int_matrix1_en clk_audio_int_matrix1 clock gating control. When high, disable clock
7	RW	0x0	clk_audio_int_matrix0_en clk_audio_int_matrix0 clock gating control. When high, disable clock
6	RW	0x0	clk_audio_frac_matrix1_en clk_audio_frac_matrix1 clock gating control. When high, disable clock
5	RW	0x0	clk_audio_frac_matrix0_en clk_audio_frac_matrix0 clock gating control. When high, disable clock
4	RW	0x0	clk_uart_frac_matrix1_en clk_uart_frac_matrix1 clock gating control. When high, disable clock
3	RW	0x0	clk_uart_frac_matrix0_en clk_uart_frac_matrix0 clock gating control. When high, disable clock
2	RW	0x0	clk_cm_frac_matrix2_en clk_cm_frac_matrix2 clock gating control. When high, disable clock
1	RW	0x0	clk_cm_frac_matrix1_en clk_cm_frac_matrix1 clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
0	RW	0x0	clk_cm_frac_matrix0_en clk_cm_frac_matrix0 clock gating control. When high, disable clock

TOPCRU_GATE_CON02
Address: Operational Base(0x20000000) + offset (0x0808)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	clk_asrc1_src_en clk_asrc1_src clock gating control. When high, disable clock
11	RW	0x0	clk_asrc0_src_en clk_asrc0_src clock gating control. When high, disable clock
10	RW	0x0	mclk_asrc3_src_en mclk_asrc3_src clock gating control. When high, disable clock
9	RW	0x0	mclk_asrc2_src_en mclk_asrc2_src clock gating control. When high, disable clock
8	RW	0x0	mclk_asrc1_src_en mclk_asrc1_src clock gating control. When high, disable clock
7	RW	0x0	mclk_asrc0_src_en mclk_asrc0_src clock gating control. When high, disable clock
6	RW	0x0	clkout_pdm_src_en clkout_pdm_src clock gating control. When high, disable clock
5	RW	0x0	mclk_pdm_src_en mclk_pdm_src clock gating control. When high, disable clock
4	RW	0x0	mclk_sai2_src_en mclk_sai2_src clock gating control. When high, disable clock
3	RW	0x0	mclk_sai1_src_en mclk_sai1_src clock gating control. When high, disable clock
2	RW	0x0	mclk_sai0_src_en mclk_sai0_src clock gating control. When high, disable clock
1	RW	0x0	sclk_uart7_src_en sclk_uart7_src clock gating control. When high, disable clock
0	RW	0x0	sclk_uart6_src_en sclk_uart6_src clock gating control. When high, disable clock

TOPCRU_GATE_CON05
Address: Operational Base(0x20000000) + offset (0x0814)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	pclk_vepu_src_en pclk_vepu_src clock gating control. When high, disable clock
13	RW	0x0	hclk_vepu_src_en hclk_vepu_src clock gating control. When high, disable clock
12	RW	0x0	aclk_vepu_src_en aclk_vepu_src clock gating control. When high, disable clock
11	RW	0x0	pclk_npu_src_en pclk_npu_src clock gating control. When high, disable clock
10	RW	0x0	hclk_npu_src_en hclk_npu_src clock gating control. When high, disable clock
9	RW	0x0	hclk_core_src_en hclk_core_src clock gating control. When high, disable clock
8	RW	0x0	clk_saradc2_src_en clk_saradc2_src clock gating control. When high, disable clock
7	RW	0x0	clk_saradc1_src_en clk_saradc1_src clock gating control. When high, disable clock
6	RW	0x0	clk_saradc0_src_en clk_saradc0_src clock gating control. When high, disable clock
5	RO	0x0	reserved
4	RW	0x0	clk_aiisp_pll_src_en clk_aiisp_pll_src clock gating control. When high, disable clock
3	RW	0x0	clk_isp_pll_src_en clk_isp_pll_src clock gating control. When high, disable clock
2	RW	0x0	clk_vepu_pll_src_en clk_vepu_pll_src clock gating control. When high, disable clock
1	RW	0x0	clk_npu_pll_src_en clk_npu_pll_src clock gating control. When high, disable clock
0	RW	0x0	clk_core_pll_src_en clk_core_pll_src clock gating control. When high, disable clock

TOPCRU_GATE_CON06
Address: Operational Base(0x20000000) + offset (0x0818)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	dclk_decom_src_en dclk_decom_src clock gating control. When high, disable clock
13	RW	0x0	dclk_ooc_src_en dclk_ooc_src clock gating control. When high, disable clock
12	RW	0x0	dclk_vop_src_en dclk_vop_src clock gating control. When high, disable clock
11	RO	0x0	reserved
10	RW	0x0	pclk_vdo_src_en pclk_vdo_src clock gating control. When high, disable clock
9	RW	0x0	hclk_vdo_src_en hclk_vdo_src clock gating control. When high, disable clock
8	RW	0x0	aclk_rkvdec_src_en aclk_rkvdec_src clock gating control. When high, disable clock
7	RW	0x0	aclk_vdo_src_en aclk_vdo_src clock gating control. When high, disable clock
6	RW	0x0	clk_sys_dsmc_src_en clk_sys_dsmc_src clock gating control. When high, disable clock
5	RW	0x0	dclk_vicap_src_en dclk_vicap_src clock gating control. When high, disable clock
4	RW	0x0	pclk_vi_src_en pclk_vi_src clock gating control. When high, disable clock
3	RW	0x0	hclk_vi_src_en hclk_vi_src clock gating control. When high, disable clock
2	RW	0x0	aclk_vi_src_en aclk_vi_src clock gating control. When high, disable clock
1	RW	0x0	aclk_gmac_src_en aclk_gmac_src clock gating control. When high, disable clock
0	RW	0x0	clk_core_rga_src_en clk_core_rga_src clock gating control. When high, disable clock

TOPCRU_GATE_CON07
Address: Operational Base(0x20000000) + offset (0x081C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	clk_timer_src_en clk_timer_src clock gating control. When high, disable clock
12	RW	0x0	clk_gmac_125m_src_en clk_gmac_125m_src clock gating control. When high, disable clock
11	RW	0x0	clk_gmac_ptp_ref_src_en clk_gmac_ptp_ref_src clock gating control. When high, disable clock
10	RW	0x0	sclk_2x_fspi0_src_en sclk_2x_fspi0_src clock gating control. When high, disable clock
9	RW	0x0	cclk_emmc_src_en cclk_emmc_src clock gating control. When high, disable clock
8	RW	0x0	cclk_sdmmc1_src_en cclk_sdmmc1_src clock gating control. When high, disable clock
7	RW	0x0	cclk_sdmmc0_src_en cclk_sdmmc0_src clock gating control. When high, disable clock
6	RW	0x0	pclk_bus_src_en pclk_bus_src clock gating control. When high, disable clock
5	RW	0x0	hclk_bus_src_en hclk_bus_src clock gating control. When high, disable clock
4	RW	0x0	aclk_bus_src_en aclk_bus_src clock gating control. When high, disable clock
3	RW	0x0	aclk_top_src_en aclk_top_src clock gating control. When high, disable clock
2	RO	0x0	reserved
1	RW	0x0	aclk_sysmem_src_en aclk_sysmem_src clock gating control. When high, disable clock
0	RW	0x0	pclk_ddr_src_en pclk_ddr_src clock gating control. When high, disable clock

TOPCRU_GATE_CON08

Address: Operational Base(0x20000000) + offset (0x0820)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12	RW	0x0	busclk_pmu_src_en busclk_pmu_src clock gating control. When high, disable clock
11	RW	0x0	clk_spi1_src_en clk_spi1_src clock gating control. When high, disable clock
10	RW	0x0	clk_spi0_src_en clk_spi0_src clock gating control. When high, disable clock
9	RW	0x0	clk_i2c_bus_src_en clk_i2c_bus_src clock gating control. When high, disable clock
8	RO	0x0	reserved
7	RW	0x0	aclk_peri_src_en aclk_peri_src clock gating control. When high, disable clock
6	RW	0x0	pclk_peri_src_en pclk_peri_src clock gating control. When high, disable clock
5	RW	0x0	clk_can1_src_en clk_can1_src clock gating control. When high, disable clock
4	RW	0x0	clk_can0_src_en clk_can0_src clock gating control. When high, disable clock
3	RO	0x0	reserved
2	RW	0x0	tclk_wdt_hpmcu_src_en tclk_wdt_hpmcu_src clock gating control. When high, disable clock
1	RW	0x0	tclk_wdt_s_src_en tclk_wdt_s_src clock gating control. When high, disable clock
0	RW	0x0	tclk_wdt_ns_src_en tclk_wdt_ns_src clock gating control. When high, disable clock

TOPCRU_GATE_CON09

Address: Operational Base(0x20000000) + offset (0x0824)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	clk_matrix_50m_vi_en clk_matrix_50m_vi clock gating control. When high, disable clock
10	RO	0x0	reserved
9	RW	0x0	clk_core_fec_src_en clk_core_fec_src clock gating control. When high, disable clock
8	RW	0x0	pclk_vcp_src_en pclk_vcp_src clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
7	RW	0x0	hclk_vcp_src_en hclk_vcp_src clock gating control. When high, disable clock
6	RW	0x0	aclk_vcp_src_en aclk_vcp_src clock gating control. When high, disable clock
5	RW	0x0	aclk_rkce_src_en aclk_rkce_src clock gating control. When high, disable clock
4	RW	0x0	clk_pka_rkce_src_en clk_pka_rkce_src clock gating control. When high, disable clock
3	RW	0x0	clk_pwm3_src_en clk_pwm3_src clock gating control. When high, disable clock
2	RW	0x0	clk_pwm2_src_en clk_pwm2_src clock gating control. When high, disable clock
1	RO	0x0	reserved
0	RW	0x0	clk_pwm0_src_en clk_pwm0_src clock gating control. When high, disable clock

TOPCRU_GATE_CON15

Address: Operational Base(0x20000000) + offset (0x083C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	clk_cplltest_en clk_cplltest clock gating control. When high, disable clock
14	RW	0x1	clk_gplltest_en clk_gplltest clock gating control. When high, disable clock
13	RO	0x0	reserved
12	RW	0x1	clk_auplltest_en clk_auplltest clock gating control. When high, disable clock
11	RW	0x1	mclk_sai2_out2io_en mclk_sai2_out2io clock gating control. When high, disable clock
10	RW	0x1	mclk_sai1_out2io_en mclk_sai1_out2io clock gating control. When high, disable clock
9	RW	0x1	mclk_sai0_out2io_en mclk_sai0_out2io clock gating control. When high, disable clock
8	RW	0x1	clk_mac_out2io_en clk_mac_out2io clock gating control. When high, disable clock
7	RW	0x1	clk_cif_out2io_en clk_cif_out2io clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
6	RW	0x1	clk_mipi3_out2io_en clk_mipi3_out2io clock gating control. When high, disable clock
5	RW	0x1	clk_mipi2_out2io_en clk_mipi2_out2io clock gating control. When high, disable clock
4	RW	0x1	clk_mipi1_out2io_en clk_mipi1_out2io clock gating control. When high, disable clock
3	RW	0x1	clk_mipi0_out2io_en clk_mipi0_out2io clock gating control. When high, disable clock
2	RW	0x0	pclk_cru_biu_en pclk_cru_biu clock gating control. When high, disable clock
1	RW	0x0	pclk_cru_en pclk_cru clock gating control. When high, disable clock
0	RW	0x0	pclk_top_root_en pclk_top_root clock gating control. When high, disable clock

TOPCRU_SOFTRST_CON15

Address: Operational Base(0x20000000) + offset (0x0A3C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2	RW	0x0	presetn_cru_biu When high, reset relative logic
1	RW	0x0	presetn_cru When high, reset relative logic
0	RO	0x0	reserved

TOPCRU_CRU_GLB_CNT_TH

Address: Operational Base(0x20000000) + offset (0x0C00)

Bit	Attr	Reset Value	Description
31:16	RW	0x0064	reserved1 Reserved
15:10	RW	0x00	reserved0 Reserved
9:0	RW	0x064	global_reset_counter_threshold Global soft reset, wdt reset or tsadc_shut reset asserted time counter threshold. Measured in OSC clock cycles

TOPCRU_CRU_GLBRST_ST

Address: Operational Base(0x20000000) + offset (0x0C04)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	glb_wdt9_rst_st global WDT9 triggered reset flag 1'b0: Last hot reset is not global WDT9 triggered reset 1'b1: Last hot reset is global WDT9 triggered reset

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Bit	Attr	Reset Value	Description
14	RW	0x0	glb_wdt8_rst_st global WDT8 triggered reset flag 1'b0: Last hot reset is not global WDT8 triggered reset 1'b1: Last hot reset is global WDT8 triggered reset
13	RW	0x0	glb_wdt7_rst_st global WDT7 triggered reset flag 1'b0: Last hot reset is not global WDT7 triggered reset 1'b1: Last hot reset is global WDT7 triggered reset
12	RW	0x0	glb_wdt6_rst_st global WDT6 triggered reset flag 1'b0: Last hot reset is not global WDT6 triggered reset 1'b1: Last hot reset is global WDT6 triggered reset
11	RW	0x0	glb_wdt5_rst_st global WDT5 triggered reset flag 1'b0: Last hot reset is not global WDT5 triggered reset 1'b1: Last hot reset is global WDT5 triggered reset
10	RW	0x0	glb_wdt4_rst_st global WDT4 triggered reset flag 1'b0: Last hot reset is not global WDT4 triggered reset 1'b1: Last hot reset is global WDT4 triggered reset
9	RW	0x0	glb_wdt3_rst_st global WDT3 triggered reset flag 1'b0: Last hot reset is not global WDT3 triggered reset 1'b1: Last hot reset is global WDT3 triggered reset
8	RW	0x0	glb_wdt2_rst_st global WDT2 triggered reset flag 1'b0: Last hot reset is not global WDT2 triggered reset 1'b1: Last hot reset is global WDT2 triggered reset
7	RW	0x0	glb_wdt1_rst_st global WDT1 triggered reset flag 1'b0: Last hot reset is not global WDT1 triggered reset 1'b1: Last hot reset is global WDT1 triggered reset
6	RW	0x0	glb_wdt0_rst_st global WDT0 triggered reset flag 1'b0: Last hot reset is not global WDT0 triggered reset 1'b1: Last hot reset is global WDT0 triggered reset
5	RW	0x0	snd_glb_wdt_rst_st sencond global WDT triggered reset flag 1'b0: Last hot reset is not sencond global WDT triggered reset 1'b1: Last hot reset is sencond global WDT triggered reset
4	RW	0x0	fst_glb_wdt_rst_st first global WDT triggered reset flag 1'b0: Last hot reset is not first global WDT triggered reset 1'b1: Last hot reset is first global WDT triggered reset
3	RW	0x0	snd_glb_tsadc_rst_st sencond global TSADC triggered reset flag 1'b0: Last hot reset is not sencond global TSADC triggered reset 1'b1: Last hot reset is sencond global TSADC triggered reset
2	RW	0x0	fst_glb_tsadc_rst_st first global TSADC triggered reset flag 1'b0: Last hot reset is not first global TSADC triggered reset 1'b1: Last hot reset is first global TSADC triggered reset
1	RW	0x0	snd_glb_rst_st second global rst flag 1'b0: Last hot reset is not sencond global reset 1'b1: Last hot reset is sencond global reset

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Bit	Attr	Reset Value	Description
0	RW	0x0	fst_glb_rst_st first global rst flag 1'b0: Last hot reset is not first global reset 1'b1: Last hot reset is first global reset

TOPCRU_CRU_GLB_SRST_FST_VALUE
Address: Operational Base(0x20000000) + offset (0x0C08)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	glb_srst_fst The first global software reset config value

TOPCRU_CRU_GLB_SRST_SND_VALUE
Address: Operational Base(0x20000000) + offset (0x0C0C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	glb_srst_snd The second global software reset config value

TOPCRU_CRU_GLB_RST_CON0
Address: Operational Base(0x20000000) + offset (0x0C10)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	pmu_srstn_req software reset pmu request
14:6	RO	0x000	reserved
5	RW	0x0	wdt_tsadc_expand_en wdt_tsadc_expand_en
4	RW	0x0	pmu_srst_wdt_en 0: Enable wdt reset as pmu reset source 1: Disable wdt reset as pmu reset source
3	RW	0x0	pmu_srst_glb_en 1'b0: global reset trigger pmu reset 1'b1: global reset dont trigger pmu reset
2	RW	0x0	pmu_srst_glb_ctrl 0: Enable first global reset as pmu reset source 1: Enable second global reset as pmu reset source effective when glb_rst_con[3] enable
1	RW	0x0	tsadc_glb_srst_en 1'b0: tsadc trigger global reset disable 1'b1: tsadc trigger global reset enable
0	RW	0x0	tsadc_glb_srst_ctrl 1'b0: tsadc trigger second global reset 1'b1: tsadc trigger first global reset

TOPCRU_CRU_GLB_RST_CON1
Address: Operational Base(0x20000000) + offset (0x0C14)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	wdt_glb_srst_ctrl 1'b0: wdt trigger second global reset 1'b1: wdt trigger first global reset

TOPCRU_CRU_GLB_RST_CON2
Address: Operational Base(0x20000000) + offset (0x0C18)

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Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	wdt_glb_srst_en 1'b0: wdt trigger global reset disable 1'b1: wdt trigger global reset enable

TOPCRU_CRU_GLB_RST_ST_NCLR

Address: Operational Base(0x20000000) + offset (0x0C20)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	glb_rst_st_nclr CRU_GLBRST_ST not-cleared flag 1'b0: bit cleared in CRU_GLBRST_ST 1'b1: bit not cleared in CRU_GLBRST_ST

TOPCRU_CLK_CM_FRAC_MATRIX0_DIV_HIGH

Address: Operational Base(0x20000000) + offset (0x0CC0)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	delta_over_sel divider delta over logic select
15:8	RW	0x00	nominator_high divider nominator[23:16]
7:0	RW	0x00	denominator_high divider denominator[23:16]

TOPCRU_CLK_CM_FRAC_MATRIX1_DIV_HIGH

Address: Operational Base(0x20000000) + offset (0x0CC4)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	delta_over_sel divider delta over logic select
15:8	RW	0x00	nominator_high divider nominator[23:16]
7:0	RW	0x00	denominator_high divider denominator[23:16]

TOPCRU_CLK_CM_FRAC_MATRIX2_DIV_HIGH

Address: Operational Base(0x20000000) + offset (0x0CC8)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	delta_over_sel divider delta over logic select
15:8	RW	0x00	nominator_high divider nominator[23:16]
7:0	RW	0x00	denominator_high divider denominator[23:16]

TOPCRU_CLK_UART_FRAC_MATRIX0_DIV_HIGH

Address: Operational Base(0x20000000) + offset (0x0CCC)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	delta_over_sel divider delta over logic select
15:8	RW	0x00	nominator_high divider nominator[23:16]

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	denominator_high divider denominator[23:16]

TOPCRU_CLK_UART_FRAC_MATRIX1_DIV_HIGH
Address: Operational Base(0x20000000) + offset (0x0CD0)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	delta_over_sel divider delta over logic select
15:8	RW	0x00	nominator_high divider nominator[23:16]
7:0	RW	0x00	denominator_high divider denominator[23:16]

TOPCRU_CLK_AUDIO_FRAC_MATRIX0_DIV_HIGH
Address: Operational Base(0x20000000) + offset (0x0CD4)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	delta_over_sel divider delta over logic select
15:8	RW	0x00	nominator_high divider nominator[23:16]
7:0	RW	0x00	denominator_high divider denominator[23:16]

TOPCRU_CLK_AUDIO_FRAC_MATRIX1_DIV_HIGH
Address: Operational Base(0x20000000) + offset (0x0CD8)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	delta_over_sel divider delta over logic select
15:8	RW	0x00	nominator_high divider nominator[23:16]
7:0	RW	0x00	denominator_high divider denominator[23:16]

TOPCRU_AUTOCS_ACLK_BUS_SRC_CON0
Address: Operational Base(0x20000000) + offset (0x0D00)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original clk
15:0	RW	0x0047	idle_th idle time threshold, measured by original clk

TOPCRU_AUTOCS_ACLK_BUS_SRC_CON1
Address: Operational Base(0x20000000) + offset (0x0D04)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:14	RW	0x0	autocs_select auto switch clock selection 2'b00: div16 of original clk 2'b01: div8 of original clk 2'b10: div4 of original clk 2'b11: div2 of original clk
13	RO	0x0	reserved
12	RW	0x0	autocs_en 1'b1: enable the autocs function 1'b0: disable
11:0	RW	0x000	autocs_ctrl The autocs ctrl enable for internal hardware signal b0 : =0, disable ; =1, enable the signal ~dcf_m_I_mainNoPendingTrans b1 : =0, disable ; =1, enable the signal ~mcu_m_I_mainNoPendingTrans b2 : =0, disable ; =1, enable the signal ~rga_m_I_mainNoPendingTrans b3 : =0, disable ; =1, enable the signal ~rkdma_m_I_mainNoPendingTrans b4 : =0, disable ; =1, enable the signal dtp_busLKdr_pwrDiscTarg_ddrLKbsPwrActive b5 : =0, disable ; =1, enable the signal dtp_busLKvibrgout_pwrDiscTarg_ddrLKviPwrActive b6 : =0, disable ; =1, enable the signal dtp_busLKcs_pwrDiscTarg_cruLKsvPwrActive b7 : =0, disable ; =1, enable the signal dtp_busLKds_pwrDiscTarg_cfgddrLKsvPwrActive b8 : =0, disable ; =1, enable the signal dtp_busLKes_pwrDiscTarg_vepuLKsvPwrActive b9 : =0, disable ; =1, enable the signal dtp_busLKis_pwrDiscTarg_viLKsvPwrActive b10: =0, disable ; =1, enable the signal dtp_busLKns_pwrDiscTarg_npuLKsvPwrActive b11: =0, disable ; =1, enable the signal dtp_busLKos_pwrDiscTarg_vdoLKsvPwrActive Other bits reserved.

TOPCRU_AUTOCS_ACLK_GMAC_SRC_CON0

Address: Operational Base(0x20000000) + offset (0x0D08)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original clk
15:0	RW	0x0047	idle_th idle time threshold, measured by original clk

TOPCRU_AUTOCS_ACLK_GMAC_SRC_CON1

Address: Operational Base(0x20000000) + offset (0x0D0C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:14	RW	0x0	autocs_select auto switch clock selection 2'b00: div16 of original clk 2'b01: div8 of original clk 2'b10: div4 of original clk 2'b11: div2 of original clk
13	RO	0x0	reserved
12	RW	0x0	autocs_en 1'b1: enable the autocs function 1'b0: disable
11:0	RW	0x000	autocs_ctrl The autocs ctrl enable for internal hardware signal b0 : =0, disable ; =1, enable the signal ~gmac_m_I_mainNoPendingTrans b1 : =0, disable ; =1, enable the signal dtp_viLKdr_pwrDiscTarg_busLKvibrginPwrActive b2 : =0, disable ; =1, enable the signal dtp_viLKnn_pwrDiscTarg_npuLKviPwrActive b3 : =0, disable ; =1, enable the signal ~isp_m_I_mainNoPendingTrans b4 : =0, disable ; =1, enable the signal ~vicap_m_I_mainNoPendingTrans b5 : =0, disable ; =1, enable the signal ~vpsl_m_I_mainNoPendingTrans b6 : =0, disable ; =1, enable the signal ~vpss_m_I_mainNoPendingTrans b7 : =0, disable ; =1, enable the signal ~rkcan0_m_I_mainNoPendingTrans b8 : =0, disable ; =1, enable the signal ~rkcan1_m_I_mainNoPendingTrans b9 : =0, disable ; =1, enable the signal ~sdmmc0_m_I_mainNoPendingTrans b10: =0, disable ; =1, enable the signal ~saradc1_apb_m_I_mainNoPendingTrans b11: =0, disable ; =1, enable the signal ~saradc2_apb_m_I_mainNoPendingTrans Other bits reserved.

TOPCRU_AUTOCS_ACLK_PERI_SRC_CON0

Address: Operational Base(0x20000000) + offset (0x0D10)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original clk
15:0	RW	0x0047	idle_th idle time threshold, measured by original clk

TOPCRU_AUTOCS_ACLK_PERI_SRC_CON1

Address: Operational Base(0x20000000) + offset (0x0D14)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:14	RW	0x0	autocs_select auto switch clock selection 2'b00: div16 of original clk 2'b01: div8 of original clk 2'b10: div4 of original clk 2'b11: div2 of original clk
13	RO	0x0	reserved
12	RW	0x0	autocs_en 1'b1: enable the autocs function 1'b0: disable
11:0	RW	0x000	autocs_ctrl The autocs ctrl enable for internal hardware signal b0 : =0, disable ; =1, enable the signal dtp_periLKdr_pwrDiscTarg_vcpLKprPwrActive b1 : =0, disable ; =1, enable the signal ~emmc_m_I_mainNoPendingTrans b2 : =0, disable ; =1, enable the signal ~fspi_m_I_mainNoPendingTrans b3 : =0, disable ; =1, enable the signal ~usb2host_m_I_mainNoPendingTrans b4 : =0, disable ; =1, enable the signal ~usb3drd_m_I_mainNoPendingTrans Other bits reserved.

TOPCRU_AUTOCS_ACLK_SYSMEM_SRC_CON0

Address: Operational Base(0x20000000) + offset (0x0D18)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original clk
15:0	RW	0x0047	idle_th idle time threshold, measured by original clk

TOPCRU_AUTOCS_ACLK_SYSMEM_SRC_CON1

Address: Operational Base(0x20000000) + offset (0x0D1C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	autocs_select auto switch clock selection 2'b00: div16 of original clk 2'b01: div8 of original clk 2'b10: div4 of original clk 2'b11: div2 of original clk
13	RO	0x0	reserved
12	RW	0x0	autocs_en 1'b1: enable the autocs function 1'b0: disable

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Bit	Attr	Reset Value	Description
11:0	RW	0x000	autocs_ctrl The autocs ctrl enable for internal hardware signal b0 : =0, disable ; =1, enable the signal dtp_subddrLKaiisp_pwrDiscTarg_aiispLKmemPwrActive b1 : =0, disable ; =1, enable the signal dtp_cfgddrLKfw_pwrDiscTarg_ddrfwLKdcPwrActive Other bits reserved.

TOPCRU_AUTOCS_ACLK_TOP_SRC_CON0
Address: Operational Base(0x20000000) + offset (0x0D20)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original clk
15:0	RW	0x0047	idle_th idle time threshold, measured by original clk

TOPCRU_AUTOCS_ACLK_TOP_SRC_CON1
Address: Operational Base(0x20000000) + offset (0x0D24)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	autocs_select auto switch clock selection 2'b00: div16 of original clk 2'b01: div8 of original clk 2'b10: div4 of original clk 2'b11: div2 of original clk
13	RO	0x0	reserved
12	RW	0x0	autocs_en 1'b1: enable the autocs function 1'b0: disable
11:0	RW	0x000	autocs_ctrl The autocs ctrl enable for internal hardware signal b0 : =0, disable ; =1, enable the signal ~dcf_m_I_mainNoPendingTrans b1 : =0, disable ; =1, enable the signal ~mcu_m_I_mainNoPendingTrans b2 : =0, disable ; =1, enable the signal ~rga_m_I_mainNoPendingTrans b3 : =0, disable ; =1, enable the signal ~rkdma_m_I_mainNoPendingTrans b4 : =0, disable ; =1, enable the signal dtp_busLKdr_pwrDiscTarg_ddrLKbsPwrActive b5 : =0, disable ; =1, enable the signal dtp_busLKvibrgout_pwrDiscTarg_ddrLKviPwrActive b6 : =0, disable ; =1, enable the signal dtp_busLKcs_pwrDiscTarg_cruLKsvPwrActive b7 : =0, disable ; =1, enable the signal dtp_busLKds_pwrDiscTarg_cfgddrLKsvPwrActive b8 : =0, disable ; =1, enable the signal dtp_busLKes_pwrDiscTarg_vepuLKsvPwrActive b9 : =0, disable ; =1, enable the signal dtp_busLKis_pwrDiscTarg_viLKsvPwrActive b10: =0, disable ; =1, enable the signal

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Bit	Attr	Reset Value	Description
			dtp_busLKns_pwrDiscTarg_npuLKsvPwrActive b11: =0, disable ; =1, enable the signal dtp_busLKos_pwrDiscTarg_vdoLKsvPwrActive Other bits reserved.

TOPCRU_AUTOCS_ACLK_VCP_SRC_CON0
Address: Operational Base(0x20000000) + offset (0x0D28)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original clk
15:0	RW	0x0047	idle_th idle time threshold, measured by original clk

TOPCRU_AUTOCS_ACLK_VCP_SRC_CON1
Address: Operational Base(0x20000000) + offset (0x0D2C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	autocs_select auto switch clock selection 2'b00: div16 of original clk 2'b01: div8 of original clk 2'b10: div4 of original clk 2'b11: div2 of original clk
13	RO	0x0	reserved
12	RW	0x0	autocs_en 1'b1: enable the autocs function 1'b0: disable
11:0	RW	0x000	autocs_ctrl The autocs ctrl enable for internal hardware signal b0 : =0, disable ; =1, enable the signal ~aiisp_m_I_mainNoPendingTrans b1 : =0, disable ; =1, enable the signal dtp_aiispLKdr_pwrDiscTarg_vcpLKaiPwrActive b2 : =0, disable ; =1, enable the signal ~avsp_ro_m_I_mainNoPendingTrans b3 : =0, disable ; =1, enable the signal ~avsp_wo_m_I_mainNoPendingTrans b4 : =0, disable ; =1, enable the signal dtp_vcpLKdr_pwrDiscTarg_ddrLKvcpPwrActive b5 : =0, disable ; =1, enable the signal ~fec_ro_m_I_mainNoPendingTrans b6 : =0, disable ; =1, enable the signal ~fec_wo_m_I_mainNoPendingTrans b7 : =0, disable ; =1, enable the signal dtp_vcpLKaisv_pwrDiscTarg_aiispLksvPwrActive b8 : =0, disable ; =1, enable the signal dtp_vcpLKps_pwrDiscTarg_periLKsvPwrActive b9 : =0, disable ; =1, enable the signal dtp_vcpLKus_pwrDiscTarg_pmuLKsvPwrActive Other bits reserved.

TOPCRU_AUTOCS_ACLK_VDO_SRC_CON0
Address: Operational Base(0x20000000) + offset (0x0D30)

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Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original clk
15:0	RW	0x0047	idle_th idle time threshold, measured by original clk

TOPCRU_AUTOCS_ACLK_VDO_SRC_CON1
Address: Operational Base(0x20000000) + offset (0x0D34)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	autocs_select auto switch clock selection 2'b00: div16 of original clk 2'b01: div8 of original clk 2'b10: div4 of original clk 2'b11: div2 of original clk
13	RO	0x0	reserved
12	RW	0x0	autocs_en 1'b1: enable the autocs function 1'b0: disable
11:0	RW	0x000	autocs_ctrl The autocs ctrl enable for internal hardware signal b0 : =0, disable ; =1, enable the signal ~rkvdec_m_I_mainNoPendingTrans b1 : =0, disable ; =1, enable the signal ~decom_m_I_mainNoPendingTrans b2 : =0, disable ; =1, enable the signal dtp_vdoLKdr_pwrDiscTarg_busLKvoPwrActive b3 : =0, disable ; =1, enable the signal ~ooc_m_I_mainNoPendingTrans b4 : =0, disable ; =1, enable the signal ~rkjpeg_m_I_mainNoPendingTrans b5 : =0, disable ; =1, enable the signal ~vop_m_I_mainNoPendingTrans Other bits reserved.

TOPCRU_AUTOCS_ACLK_VEPU_SRC_CON0
Address: Operational Base(0x20000000) + offset (0x0D38)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original clk
15:0	RW	0x0047	idle_th idle time threshold, measured by original clk

TOPCRU_AUTOCS_ACLK_VEPU_SRC_CON1
Address: Operational Base(0x20000000) + offset (0x0D3C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:14	RW	0x0	autocs_select auto switch clock selection 2'b00: div16 of original clk 2'b01: div8 of original clk 2'b10: div4 of original clk 2'b11: div2 of original clk
13	RO	0x0	reserved
12	RW	0x0	autocs_en 1'b1: enable the autocs function 1'b0: disable
11:0	RW	0x000	autocs_ctrl The autocs ctrl enable for internal hardware signal b0 : =0, disable ; =1, enable the signal dtp_vepuLKdr_pwrDiscTarg_ddrLKvePwrActive b1 : =0, disable ; =1, enable the signal dtp_vepuLKnn_pwrDiscTarg_npuLKvepuPwrActive b2 : =0, disable ; =1, enable the signal ~rkvenc_m_I_mainNoPendingTrans b3 : =0, disable ; =1, enable the signal ~sdmmc1_m_I_mainNoPendingTrans b4 : =0, disable ; =1, enable the signal ~saradc0_apb_m_I_mainNoPendingTrans Other bits reserved.

TOPCRU_AUTOCS_ACLK_VI_SRC_CON0

Address: Operational Base(0x20000000) + offset (0x0D40)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original clk
15:0	RW	0x0047	idle_th idle time threshold, measured by original clk

TOPCRU_AUTOCS_ACLK_VI_SRC_CON1

Address: Operational Base(0x20000000) + offset (0x0D44)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	autocs_select auto switch clock selection 2'b00: div16 of original clk 2'b01: div8 of original clk 2'b10: div4 of original clk 2'b11: div2 of original clk
13	RO	0x0	reserved
12	RW	0x0	autocs_en 1'b1: enable the autocs function 1'b0: disable

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Bit	Attr	Reset Value	Description
11:0	RW	0x000	autocs_ctrl The autocs ctrl enable for internal hardware signal b0 : =0, disable ; =1, enable the signal ~gmac_m_I_mainNoPendingTrans b1 : =0, disable ; =1, enable the signal dtp_viLKdr_pwrDiscTarg_busLKvibrginPwrActive b2 : =0, disable ; =1, enable the signal dtp_viLKnn_pwrDiscTarg_npuLKviPwrActive b3 : =0, disable ; =1, enable the signal ~isp_m_I_mainNoPendingTrans b4 : =0, disable ; =1, enable the signal ~vicap_m_I_mainNoPendingTrans b5 : =0, disable ; =1, enable the signal ~vpsl_m_I_mainNoPendingTrans b6 : =0, disable ; =1, enable the signal ~vpss_m_I_mainNoPendingTrans b7 : =0, disable ; =1, enable the signal ~rkcan0_m_I_mainNoPendingTrans b8 : =0, disable ; =1, enable the signal ~rkcan1_m_I_mainNoPendingTrans b9 : =0, disable ; =1, enable the signal ~sdmmc0_m_I_mainNoPendingTrans b10: =0, disable ; =1, enable the signal ~saradc1_apb_m_I_mainNoPendingTrans b11: =0, disable ; =1, enable the signal ~saradc2_apb_m_I_mainNoPendingTrans Other bits reserved.

TOPCRU_AUTOCS_HCLK_BUS_SRC_CON0
Address: Operational Base(0x20000000) + offset (0x0D48)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original clk
15:0	RW	0x0047	idle_th idle time threshold, measured by original clk

TOPCRU_AUTOCS_HCLK_BUS_SRC_CON1
Address: Operational Base(0x20000000) + offset (0x0D4C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	autocs_select auto switch clock selection 2'b00: div16 of original clk 2'b01: div8 of original clk 2'b10: div4 of original clk 2'b11: div2 of original clk
13	RO	0x0	reserved
12	RW	0x0	autocs_en 1'b1: enable the autocs function 1'b0: disable

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Bit	Attr	Reset Value	Description
11:0	RW	0x000	autocs_ctrl The autocs ctrl enable for internal hardware signal b0 : =0, disable ; =1, enable the signal ~dcf_m_I_mainNoPendingTrans b1 : =0, disable ; =1, enable the signal ~mcu_m_I_mainNoPendingTrans b2 : =0, disable ; =1, enable the signal ~rga_m_I_mainNoPendingTrans b3 : =0, disable ; =1, enable the signal ~rkdma_m_I_mainNoPendingTrans b4 : =0, disable ; =1, enable the signal dtp_busLKdr_pwrDiscTarg_ddrLKbsPwrActive b5 : =0, disable ; =1, enable the signal dtp_busLKvibrgout_pwrDiscTarg_ddrLKviPwrActive b6 : =0, disable ; =1, enable the signal dtp_busLKcs_pwrDiscTarg_cruLKsvPwrActive b7 : =0, disable ; =1, enable the signal dtp_busLKds_pwrDiscTarg_cfgddrLKsvPwrActive b8 : =0, disable ; =1, enable the signal dtp_busLKes_pwrDiscTarg_vepuLKsvPwrActive b9 : =0, disable ; =1, enable the signal dtp_busLKis_pwrDiscTarg_viLKsvPwrActive b10: =0, disable ; =1, enable the signal dtp_busLKns_pwrDiscTarg_npuLKsvPwrActive b11: =0, disable ; =1, enable the signal dtp_busLKos_pwrDiscTarg_vdoLKsvPwrActive Other bits reserved.

TOPCRU_AUTOCS_HCLK_VCP_SRC_CON0
Address: Operational Base(0x20000000) + offset (0x0D50)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original clk
15:0	RW	0x0047	idle_th idle time threshold, measured by original clk

TOPCRU_AUTOCS_HCLK_VCP_SRC_CON1
Address: Operational Base(0x20000000) + offset (0x0D54)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	autocs_select auto switch clock selection 2'b00: div16 of original clk 2'b01: div8 of original clk 2'b10: div4 of original clk 2'b11: div2 of original clk
13	RO	0x0	reserved
12	RW	0x0	autocs_en 1'b1: enable the autocs function 1'b0: disable

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Bit	Attr	Reset Value	Description
11:0	RW	0x000	autocs_ctrl The autocs ctrl enable for internal hardware signal b0 : =0, disable ; =1, enable the signal ~aiisp_m_I_mainNoPendingTrans b1 : =0, disable ; =1, enable the signal dtp_aiispLKdr_pwrDiscTarg_vcpLKaiPwrActive b2 : =0, disable ; =1, enable the signal ~avsp_ro_m_I_mainNoPendingTrans b3 : =0, disable ; =1, enable the signal ~avsp_wo_m_I_mainNoPendingTrans b4 : =0, disable ; =1, enable the signal dtp_vcpLKdr_pwrDiscTarg_ddrLKvcpPwrActive b5 : =0, disable ; =1, enable the signal ~fec_ro_m_I_mainNoPendingTrans b6 : =0, disable ; =1, enable the signal ~fec_wo_m_I_mainNoPendingTrans b7 : =0, disable ; =1, enable the signal dtp_vcpLKaisv_pwrDiscTarg_aiispLksvPwrActive b8 : =0, disable ; =1, enable the signal dtp_vcpLKps_pwrDiscTarg_periLKsvPwrActive b9 : =0, disable ; =1, enable the signal dtp_vcpLKus_pwrDiscTarg_pmuLKsvPwrActive Other bits reserved.

TOPCRU_AUTOCS_HCLK_VEPU_SRC_CON0
Address: Operational Base(0x20000000) + offset (0x0D58)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original clk
15:0	RW	0x0047	idle_th idle time threshold, measured by original clk

TOPCRU_AUTOCS_HCLK_VEPU_SRC_CON1
Address: Operational Base(0x20000000) + offset (0x0D5C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	autocs_select auto switch clock selection 2'b00: div16 of original clk 2'b01: div8 of original clk 2'b10: div4 of original clk 2'b11: div2 of original clk
13	RO	0x0	reserved
12	RW	0x0	autocs_en 1'b1: enable the autocs function 1'b0: disable

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Bit	Attr	Reset Value	Description
11:0	RW	0x000	autocs_ctrl The autocs ctrl enable for internal hardware signal b0 : =0, disable ; =1, enable the signal dtp_vepuLKdr_pwrDiscTarg_ddrLKvePwrActive b1 : =0, disable ; =1, enable the signal dtp_vepuLKnn_pwrDiscTarg_npuLKvepuPwrActive b2 : =0, disable ; =1, enable the signal ~rkvenc_m_I_mainNoPendingTrans b3 : =0, disable ; =1, enable the signal ~sdmmc1_m_I_mainNoPendingTrans b4 : =0, disable ; =1, enable the signal ~saradc0_apb_m_I_mainNoPendingTrans Other bits reserved.

TOPCRU_AUTOCS_HCLK_VI_SRC_CON0

Address: Operational Base(0x20000000) + offset (0x0D60)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original clk
15:0	RW	0x0047	idle_th idle time threshold, measured by original clk

TOPCRU_AUTOCS_HCLK_VI_SRC_CON1

Address: Operational Base(0x20000000) + offset (0x0D64)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	autocs_select auto switch clock selection 2'b00: div16 of original clk 2'b01: div8 of original clk 2'b10: div4 of original clk 2'b11: div2 of original clk
13	RO	0x0	reserved
12	RW	0x0	autocs_en 1'b1: enable the autocs function 1'b0: disable
11:0	RW	0x000	autocs_ctrl The autocs ctrl enable for internal hardware signal b0 : =0, disable ; =1, enable the signal ~gmac_m_I_mainNoPendingTrans b1 : =0, disable ; =1, enable the signal dtp_viLKdr_pwrDiscTarg_busLKvibrginPwrActive b2 : =0, disable ; =1, enable the signal dtp_viLKnn_pwrDiscTarg_npuLKviPwrActive b3 : =0, disable ; =1, enable the signal ~isp_m_I_mainNoPendingTrans b4 : =0, disable ; =1, enable the signal ~vicap_m_I_mainNoPendingTrans b5 : =0, disable ; =1, enable the signal ~vpsl_m_I_mainNoPendingTrans b6 : =0, disable ; =1, enable the signal ~vpss_m_I_mainNoPendingTrans b7 : =0, disable ; =1, enable the signal

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Bit	Attr	Reset Value	Description
			~rkcan0_m_I_mainNoPendingTrans b8 : =0, disable ; =1, enable the signal ~rkcan1_m_I_mainNoPendingTrans b9 : =0, disable ; =1, enable the signal ~sdmmc0_m_I_mainNoPendingTrans b10: =0, disable ; =1, enable the signal ~saradc1_apb_m_I_mainNoPendingTrans b11: =0, disable ; =1, enable the signal ~saradc2_apb_m_I_mainNoPendingTrans Other bits reserved.

TOPCRU_AUTOCS_PCLK_DDR_SRC_CON0
Address: Operational Base(0x20000000) + offset (0x0D68)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original clk
15:0	RW	0x0047	idle_th idle time threshold, measured by original clk

TOPCRU_AUTOCS_PCLK_DDR_SRC_CON1
Address: Operational Base(0x20000000) + offset (0x0D6C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	autocs_select auto switch clock selection 2'b00: div16 of original clk 2'b01: div8 of original clk 2'b10: div4 of original clk 2'b11: div2 of original clk
13	RO	0x0	reserved
12	RW	0x0	autocs_en 1'b1: enable the autocs function 1'b0: disable
11:0	RW	0x000	autocs_ctrl The autocs ctrl enable for internal hardware signal b0 : =0, disable ; =1, enable the signal dtp_subddrLKaiisp_pwrDiscTarg_aiispLKmemPwrActive b1 : =0, disable ; =1, enable the signal dtp_cfgddrLKfw_pwrDiscTarg_ddrfwLKdcPwrActive Other bits reserved.

TOPCRU_AUTOCS_PCLK_VEPU_SRC_CON0
Address: Operational Base(0x20000000) + offset (0x0D70)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original clk
15:0	RW	0x0047	idle_th idle time threshold, measured by original clk

TOPCRU_AUTOCS_PCLK_VEPU_SRC_CON1
Address: Operational Base(0x20000000) + offset (0x0D74)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	autocs_select auto switch clock selection 2'b00: div16 of original clk 2'b01: div8 of original clk 2'b10: div4 of original clk 2'b11: div2 of original clk
13	RO	0x0	reserved
12	RW	0x0	autocs_en 1'b1: enable the autocs function 1'b0: disable
11:0	RW	0x000	autocs_ctrl The autocs ctrl enable for internal hardware signal b0 : =0, disable ; =1, enable the signal dtp_vepuLKdr_pwrDiscTarg_ddrLKvePwrActive b1 : =0, disable ; =1, enable the signal dtp_vepuLKnn_pwrDiscTarg_npuLKvepuPwrActive b2 : =0, disable ; =1, enable the signal ~rkvenc_m_I_mainNoPendingTrans b3 : =0, disable ; =1, enable the signal ~sdmmc1_m_I_mainNoPendingTrans b4 : =0, disable ; =1, enable the signal ~saradc0_apb_m_I_mainNoPendingTrans Other bits reserved.

TOPCRU_AUTOCS_PCLK_VI_SRC_CON0

Address: Operational Base(0x20000000) + offset (0x0D78)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original clk
15:0	RW	0x0047	idle_th idle time threshold, measured by original clk

TOPCRU_AUTOCS_PCLK_VI_SRC_CON1

Address: Operational Base(0x20000000) + offset (0x0D7C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	autocs_select auto switch clock selection 2'b00: div16 of original clk 2'b01: div8 of original clk 2'b10: div4 of original clk 2'b11: div2 of original clk
13	RO	0x0	reserved
12	RW	0x0	autocs_en 1'b1: enable the autocs function 1'b0: disable

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Bit	Attr	Reset Value	Description
11:0	RW	0x000	autocs_ctrl The autocs ctrl enable for internal hardware signal b0 : =0, disable ; =1, enable the signal ~gmac_m_I_mainNoPendingTrans b1 : =0, disable ; =1, enable the signal dtp_viLKdr_pwrDiscTarg_busLKvibrginPwrActive b2 : =0, disable ; =1, enable the signal dtp_viLKnn_pwrDiscTarg_npuLKviPwrActive b3 : =0, disable ; =1, enable the signal ~isp_m_I_mainNoPendingTrans b4 : =0, disable ; =1, enable the signal ~vicap_m_I_mainNoPendingTrans b5 : =0, disable ; =1, enable the signal ~vpsl_m_I_mainNoPendingTrans b6 : =0, disable ; =1, enable the signal ~vpss_m_I_mainNoPendingTrans b7 : =0, disable ; =1, enable the signal ~rkcan0_m_I_mainNoPendingTrans b8 : =0, disable ; =1, enable the signal ~rkcan1_m_I_mainNoPendingTrans b9 : =0, disable ; =1, enable the signal ~sdmmc0_m_I_mainNoPendingTrans b10: =0, disable ; =1, enable the signal ~saradc1_apb_m_I_mainNoPendingTrans b11: =0, disable ; =1, enable the signal ~saradc2_apb_m_I_mainNoPendingTrans Other bits reserved.

TOPCRU_AUTOCS_CON_MISC
Address: Operational Base(0x20000000) + offset (0x0E00)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	autocs_con The autocs ctrl enable for internal hardware signal. b0 : =0, disable ; =1, enable the signal dtp_busLKpp_pwrDiscTarg_vcpLKsvPwrActive for aclk_bus_src b1 : =0, disable ; =1, enable the signal dtp_busLKpp_pwrDiscTarg_vcpLKsvPwrActive for aclk_top_src b2 : =0, disable ; =1, enable the signal dtp_busLKpp_pwrDiscTarg_vcpLKsvPwrActive for hclk_bus_src Other bits reserved.

2.4.2 BUSCRU

2.4.2.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

2.4.2.2 Registers Summary

Name	Offset	Size	Reset Value	Description
BUSCRU_BUS_CLKSEL_CON00	0x0300	W	0x00000007	Internal clock select and division register 0

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Name	Offset	Size	Reset Value	Description
BUSCRU_BUS_CLKSEL_CON02	0x0308	W	0x00001000	Internal clock select and division register 2
BUSCRU_BUS_CLKSEL_CON03	0x030C	W	0x00000000	Internal clock select and division register 3
BUSCRU_BUS_GATE_CON00	0x0800	W	0x00008000	Internal clock gate and division register 0
BUSCRU_BUS_GATE_CON01	0x0804	W	0x00000000	Internal clock gate and division register 1
BUSCRU_BUS_GATE_CON02	0x0808	W	0x00000000	Internal clock gate and division register 2
BUSCRU_BUS_GATE_CON03	0x080C	W	0x00000000	Internal clock gate and division register 3
BUSCRU_BUS_GATE_CON04	0x0810	W	0x00000000	Internal clock gate and division register 4
BUSCRU_BUS_GATE_CON05	0x0814	W	0x00000000	Internal clock gate and division register 5
BUSCRU_BUS_GATE_CON06	0x0818	W	0x00000100	Internal clock gate and division register 6
BUSCRU_BUS_SOFTRST_CON00	0x0A00	W	0x00000000	Internal clock reset register 0
BUSCRU_BUS_SOFTRST_CON01	0x0A04	W	0x000001E0	Internal clock reset register 1
BUSCRU_BUS_SOFTRST_CON02	0x0A08	W	0x00000000	Internal clock reset register 2
BUSCRU_BUS_SOFTRST_CON03	0x0A0C	W	0x00000000	Internal clock reset register 3
BUSCRU_BUS_SOFTRST_CON04	0x0A10	W	0x00000000	Internal clock reset register 4
BUSCRU_BUS_SOFTRST_CON05	0x0A14	W	0x00000000	Internal clock reset register 5
BUSCRU_BUS_SOFTRST_CON06	0x0A18	W	0x00000000	Internal clock reset register 6
BUSCRU_BUS_SOFTRST_CON07	0x0A1C	W	0x00000000	Internal clock reset register 7

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

2.4.2.3 Detail Registers Description

BUSCRU_BUS_CLKSEL_CON00

Address: Operational Base(0x20010000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	clk_testout_bus_sel clk_testout_bus clock mux. 1'b0: clk_testout_bus_mux0 1'b1: clk_testout_bus_mux1

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Bit	Attr	Reset Value	Description
13:10	RW	0x0	clk_testout_bus_mux1_sel clk_testout_bus_mux1 clock mux. 4'b0000: clk_hpmcu_jtag_io 4'b0001: sclkin_spi0_io 4'b0010: sclkin_spi1_io 4'b0011: mclk_sai0_from_io 4'b0100: sclk_sai0_from_io 4'b0101: mclk_sai1_from_io 4'b0110: sclk_sai1_from_io 4'b0111: mclk_sai2_from_io 4'b1000: sclk_sai2_from_io 4'b1001: clk_pwm0 4'b1010: clk_pwm2 4'b1011: clk_pwm3 4'b1100: dbg2io_ch_clk_o_from_tsadc 4'b1101: 1'b0 4'b1110: 1'b0 4'b1111: 1'b0
9	RO	0x0	reserved
8:4	RW	0x00	clk_testout_bus_mux0_sel clk_testout_bus_mux0 clock mux. 5'b00000: aclk_top_root 5'b00001: aclk_rkce_root 5'b00010: clk_pka_rkce_root 5'b00011: aclk_bus_root 5'b00100: hclk_bus_root 5'b00101: pclk_bus_root 5'b00110: clk_i2c_bus_root 5'b00111: clk_timer_root 5'b01000: clk_core_rga 5'b01001: tclk_wdt_ns_src 5'b01010: tclk_wdt_s_src 5'b01011: tclk_wdt_hpmcu_src 5'b01100: clk_spi0 5'b01101: clk_spi1 5'b01110: sclk_uart1 5'b01111: sclk_uart2 5'b10000: sclk_uart3 5'b10001: sclk_uart4 5'b10010: sclk_uart5 5'b10011: sclk_uart6 5'b10100: sclk_uart7 5'b10101: mclk_sai0 5'b10110: mclk_sai1 5'b10111: mclk_sai2 5'b11000: mclk_pdm 5'b11001: clkout_pdm 5'b11010: clk_asrc0 5'b11011: clk_asrc1 5'b11100: mclk_asrc0_src 5'b11101: mclk_asrc1_src 5'b11110: mclk_asrc2_src 5'b11111: mclk_asrc3_src
3:0	RW	0x7	clk_testout_bus_div Divide clk_testout_bus by (div_con + 1).

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BUSCRU_BUS_CLKSEL_CON02
Address: Operational Base(0x20010000) + offset (0x0308)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x1	clk_user_otpc_ns_div Divide clk_user_otpc_ns by (div_con + 1).
11:10	RO	0x0	reserved
9:8	RW	0x0	clk_timer4_sel clk_timer4 clock mux. 2'b00: clk_timer_root 2'b01: mclk_asrc2_src 2'b10: mclk_asrc3_src
7:6	RW	0x0	clk_timer3_sel clk_timer3 clock mux. 2'b00: clk_timer_root 2'b01: mclk_asrc0_src 2'b10: mclk_asrc1_src
5:4	RW	0x0	clk_timer2_sel clk_timer2 clock mux. 2'b00: clk_timer_root 2'b01: mclk_sai2_from_io 2'b10: sclk_sai2_from_io
3:2	RW	0x0	clk_timer1_sel clk_timer1 clock mux. 2'b00: clk_timer_root 2'b01: mclk_sai1_from_io 2'b10: sclk_sai1_from_io
1:0	RW	0x0	clk_timer0_sel clk_timer0 clock mux. 2'b00: clk_timer_root 2'b01: mclk_sai0_from_io 2'b10: sclk_sai0_from_io

BUSCRU_BUS_CLKSEL_CON03
Address: Operational Base(0x20010000) + offset (0x030C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	lrck_dst_asrc1_sel lrck_dst_asrc1 clock mux. 3'b000: mclk_asrc0_src 3'b001: mclk_asrc1_src 3'b010: mclk_asrc2_src 3'b011: mclk_asrc3_src 3'b100: fs_inter_from_sai0 3'b101: fs_inter_from_sai1 3'b110: fs_inter_from_sai2 3'b111: clkout_pdm
11	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
10:8	RW	0x0	lrck_src_asrc1_sel lrck_src_asrc1 clock mux. 3'b000: mclk_asrc0_src 3'b001: mclk_asrc1_src 3'b010: mclk_asrc2_src 3'b011: mclk_asrc3_src 3'b100: fs_inter_from_sai0 3'b101: fs_inter_from_sai1 3'b110: fs_inter_from_sai2 3'b111: clkout_pdm
7	RO	0x0	reserved
6:4	RW	0x0	lrck_dst_asrc0_sel lrck_dst_asrc0 clock mux. 3'b000: mclk_asrc0_src 3'b001: mclk_asrc1_src 3'b010: mclk_asrc2_src 3'b011: mclk_asrc3_src 3'b100: fs_inter_from_sai0 3'b101: fs_inter_from_sai1 3'b110: fs_inter_from_sai2 3'b111: clkout_pdm
3	RO	0x0	reserved
2:0	RW	0x0	lrck_src_asrc0_sel lrck_src_asrc0 clock mux. 3'b000: mclk_asrc0_src 3'b001: mclk_asrc1_src 3'b010: mclk_asrc2_src 3'b011: mclk_asrc3_src 3'b100: fs_inter_from_sai0 3'b101: fs_inter_from_sai1 3'b110: fs_inter_from_sai2 3'b111: clkout_pdm

BUSCRU_BUS_GATE_CON00

Address: Operational Base(0x20010000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	clk_testout_bus_en clk_testout_bus clock gating control. When high, disable clock
14:12	RO	0x0	reserved
11	RW	0x0	tclk_wdt_ns_en tclk_wdt_ns clock gating control. When high, disable clock
10	RW	0x0	pclk_wdt_ns_en pclk_wdt_ns clock gating control. When high, disable clock
9	RW	0x0	aclk_spinlock_en aclk_spinlock clock gating control. When high, disable clock
8	RW	0x0	aclk_gic400_en aclk_gic400 clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
7	RW	0x0	hclk_bootrom_en hclk_bootrom clock gating control. When high, disable clock
6	RW	0x0	pclk_sys_grf_en pclk_sys_grf clock gating control. When high, disable clock
5	RW	0x0	pclk_cru_bus_en pclk_cru_bus clock gating control. When high, disable clock
4	RW	0x0	pclk_bus_biu_en pclk_bus_biu clock gating control. When high, disable clock
3	RW	0x0	hclk_bus_biu_en hclk_bus_biu clock gating control. When high, disable clock
2	RW	0x0	aclk_bus_biu_en aclk_bus_biu clock gating control. When high, disable clock
1	RW	0x0	aclk_rkce_biu_en aclk_rkce_biu clock gating control. When high, disable clock
0	RW	0x0	aclk_top_biu_en aclk_top_biu clock gating control. When high, disable clock

BUSCRU_BUS_GATE_CON01

Address: Operational Base(0x20010000) + offset (0x0804)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	aclk_rkdma_en aclk_rkdma clock gating control. When high, disable clock
11	RW	0x0	pclk_rkdma_en pclk_rkdma clock gating control. When high, disable clock
10	RW	0x0	clk_hpmcu_rtc_en clk_hpmcu_rtc clock gating control. When high, disable clock
9:6	RO	0x0	reserved
5	RW	0x0	clk_hpmcu_en clk_hpmcu clock gating control. When high, disable clock
4	RW	0x0	pclk_hpmcu_intmux_en pclk_hpmcu_intmux clock gating control. When high, disable clock
3	RW	0x0	pclk_hpmcu_mailbox_en pclk_hpmcu_mailbox clock gating control. When high, disable clock
2	RW	0x0	hclk_cache_en hclk_cache clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
1	RO	0x0	reserved
0	RW	0x0	pclk_wdt_hpmcu_en pclk_wdt_hpmcu clock gating control. When high, disable clock

BUSCRU_BUS_GATE_CON02

Address: Operational Base(0x20010000) + offset (0x0808)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	hclk_rkrng_ns_en hclk_rkrng_ns_nscru clock gating control. When high, disable clock
14	RW	0x0	hclk_rkrng_s_en hclk_rkrng_s_nscru clock gating control. When high, disable clock
13	RW	0x0	clk_pka_rkce_en clk_pka_nsrkce clock gating control. When high, disable clock
12	RW	0x0	aclk_rkce_en aclk_nsrkce clock gating control. When high, disable clock
11	RW	0x0	clk_timer5_en clk_timer5 clock gating control. When high, disable clock
10	RW	0x0	clk_timer4_en clk_timer4 clock gating control. When high, disable clock
9	RW	0x0	clk_timer3_en clk_timer3 clock gating control. When high, disable clock
8	RW	0x0	clk_timer2_en clk_timer2 clock gating control. When high, disable clock
7	RW	0x0	clk_timer1_en clk_timer1 clock gating control. When high, disable clock
6	RW	0x0	clk_timer0_en clk_timer0 clock gating control. When high, disable clock
5	RW	0x0	pclk_timer_en pclk_timer clock gating control. When high, disable clock
4	RW	0x0	clk_core_rga_en clk_core_rga clock gating control. When high, disable clock
3	RW	0x0	aclk_rga_en aclk_rga clock gating control. When high, disable clock
2	RW	0x0	hclk_rga_en hclk_rga clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
1	RW	0x0	aclk_dcf_en aclk_dcf clock gating control. When high, disable clock
0	RW	0x0	pclk_dcf_en pclk_dcf clock gating control. When high, disable clock

BUSCRU_BUS_GATE_CON03

Address: Operational Base(0x20010000) + offset (0x080C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	pclk_spi1_en pclk_spi1 clock gating control. When high, disable clock
11	RO	0x0	reserved
10	RW	0x0	pclk_spi0_en pclk_spi0 clock gating control. When high, disable clock
9	RW	0x0	clk_i2c5_en clk_i2c5 clock gating control. When high, disable clock
8	RW	0x0	pclk_i2c5_en pclk_i2c5 clock gating control. When high, disable clock
7	RW	0x0	clk_i2c4_en clk_i2c4 clock gating control. When high, disable clock
6	RW	0x0	pclk_i2c4_en pclk_i2c4 clock gating control. When high, disable clock
5	RW	0x0	clk_i2c3_en clk_i2c3 clock gating control. When high, disable clock
4	RW	0x0	pclk_i2c3_en pclk_i2c3 clock gating control. When high, disable clock
3	RW	0x0	clk_i2c1_en clk_i2c1 clock gating control. When high, disable clock
2	RW	0x0	pclk_i2c1_en pclk_i2c1 clock gating control. When high, disable clock
1	RW	0x0	clk_i2c0_en clk_i2c0 clock gating control. When high, disable clock
0	RW	0x0	pclk_i2c0_en pclk_i2c0 clock gating control. When high, disable clock

BUSCRU_BUS_GATE_CON04

Address: Operational Base(0x20010000) + offset (0x0810)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pclk_uart7_en pclk_uart7 clock gating control. When high, disable clock
14	RW	0x0	pclk_uart6_en pclk_uart6 clock gating control. When high, disable clock
13	RW	0x0	pclk_uart5_en pclk_uart5 clock gating control. When high, disable clock
12	RW	0x0	pclk_uart4_en pclk_uart4 clock gating control. When high, disable clock
11	RW	0x0	pclk_uart3_en pclk_uart3 clock gating control. When high, disable clock
10	RW	0x0	pclk_uart2_en pclk_uart2 clock gating control. When high, disable clock
9	RW	0x0	pclk_uart1_en pclk_uart1 clock gating control. When high, disable clock
8	RW	0x0	clk_rc_pwm3_en clk_rc_pwm3 clock gating control. When high, disable clock
7	RW	0x0	clk_osc_pwm3_en clk_osc_pwm3 clock gating control. When high, disable clock
6	RW	0x0	pclk_pwm3_en pclk_pwm3 clock gating control. When high, disable clock
5	RW	0x0	clk_rc_pwm2_en clk_rc_pwm2 clock gating control. When high, disable clock
4	RW	0x0	clk_osc_pwm2_en clk_osc_pwm2 clock gating control. When high, disable clock
3	RW	0x0	pclk_pwm2_en pclk_pwm2 clock gating control. When high, disable clock
2	RW	0x0	clk_rc_pwm0_en clk_rc_pwm0 clock gating control. When high, disable clock
1	RW	0x0	clk_osc_pwm0_en clk_osc_pwm0 clock gating control. When high, disable clock
0	RW	0x0	pclk_pwm0_en pclk_pwm0 clock gating control. When high, disable clock

BUSCRU_BUS_GATE_CON05
Address: Operational Base(0x20010000) + offset (0x0814)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	mclk_audio_adc_bus_en mclk_audio_adc_bus clock gating control. When high, disable clock
13	RW	0x0	pclk_audio_adc_bus_en pclk_audio_adc_bus clock gating control. When high, disable clock
12	RW	0x0	hclk_asrc1_en hclk_asrc1 clock gating control. When high, disable clock
11	RW	0x0	hclk_asrc0_en hclk_asrc0 clock gating control. When high, disable clock
10	RW	0x0	hclk_pdm_en hclk_pdm clock gating control. When high, disable clock
9	RW	0x0	mclk_rkdsm_en mclk_rkdsm clock gating control. When high, disable clock
8	RW	0x0	hclk_rkdsm_en hclk_rkdsm clock gating control. When high, disable clock
7	RO	0x0	reserved
6	RW	0x0	hclk_sai2_en hclk_sai2 clock gating control. When high, disable clock
5	RO	0x0	reserved
4	RW	0x0	hclk_sai1_en hclk_sai1 clock gating control. When high, disable clock
3	RO	0x0	reserved
2	RW	0x0	hclk_sai0_en hclk_sai0 clock gating control. When high, disable clock
1	RW	0x0	clk_tsadc_en clk_tsadc clock gating control. When high, disable clock
0	RW	0x0	pclk_tsadc_en pclk_tsadc clock gating control. When high, disable clock

BUSCRU_BUS_GATE_CON06

Address: Operational Base(0x20010000) + offset (0x0818)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	sclkin_spi1_dft_en sclkin_spi1_dft clock gating control. When high, disable clock

Bit	Attr	Reset Value	Description
14	RW	0x0	sclkin_spi0_dft_en sclkin_spi0_dft clock gating control. When high, disable clock
13	RW	0x0	clk_hpmcu_jtag_dft_en clk_hpmcu_jtag_dft clock gating control. When high, disable clock
12:9	RO	0x0	reserved
8	RW	0x1	clk_tsadc_phyctrl_en clk_tsadc_phyctrl clock gating control. When high, disable clock
7	RO	0x0	reserved
6	RW	0x0	pclk_otp_mask_en pclk_otp_mask clock gating control. When high, disable clock
5	RW	0x0	clk_otpc_arb_en clk_otpc_arb clock gating control. When high, disable clock
4	RW	0x0	clk_user_otpc_ns_en clk_user_otpc_ns clock gating control. When high, disable clock
3	RW	0x0	clk_sbpi_otpc_ns_en clk_sbpi_otpc_ns clock gating control. When high, disable clock
2	RW	0x0	pclk_otpc_ns_en pclk_otpc_ns clock gating control. When high, disable clock
1	RW	0x0	hclk_ns_rkce_en hclk_ns_rkce clock gating control. When high, disable clock
0	RW	0x0	pclk_rkce_en pclk_rkce clock gating control. When high, disable clock

BUSCRU_BUS_SOFTRST_CON00

Address: Operational Base(0x20010000) + offset (0x0A00)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	tresetn_wdt_ns When high, reset relative logic
10	RW	0x0	presetn_wdt_ns When high, reset relative logic
9	RW	0x0	aresetn_spinlock When high, reset relative logic
8	RW	0x0	aresetn_gic400 When high, reset relative logic
7	RW	0x0	hresetn_bootrom When high, reset relative logic
6	RW	0x0	presetn_sys_grf When high, reset relative logic
5	RW	0x0	presetn_cru_bus When high, reset relative logic

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Bit	Attr	Reset Value	Description
4	RW	0x0	presetn_bus_biu When high, reset relative logic
3	RW	0x0	hresetn_bus_biu When high, reset relative logic
2	RW	0x0	aresetn_bus_biu When high, reset relative logic
1	RW	0x0	aresetn_rkce_biu When high, reset relative logic
0	RW	0x0	aresetn_top_biu When high, reset relative logic

BUSCRU_BUS_SOFTRST_CON01

Address: Operational Base(0x20010000) + offset (0x0A04)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	aresetn_rkdma When high, reset relative logic
11	RW	0x0	presetn_rkdma When high, reset relative logic
10:9	RO	0x0	reserved
8	RW	0x1	tresetn_hpmcu_jtag When high, reset relative logic
7	RW	0x1	resetn_hpmcu_only_core When high, reset relative logic
6	RW	0x1	resetn_hpmcu_pwup When high, reset relative logic
5	RW	0x1	resetn_hpmcu_full_cluster When high, reset relative logic
4	RW	0x0	presetn_hpmcu_intmux When high, reset relative logic
3	RW	0x0	presetn_hpmcu_mailbox When high, reset relative logic
2	RW	0x0	hresetn_cache When high, reset relative logic
1	RW	0x0	tresetn_wdt_hpmcu When high, reset relative logic
0	RW	0x0	presetn_wdt_hpmcu When high, reset relative logic

BUSCRU_BUS_SOFTRST_CON02

Address: Operational Base(0x20010000) + offset (0x0A08)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	hresetn_rkrng_ns When high, reset relative logic
14	RW	0x0	hresetn_rkrng_s When high, reset relative logic

Bit	Attr	Reset Value	Description
13	RW	0x0	resetn_pka_rkce When high, reset relative logic
12	RW	0x0	aresetn_rkce When high, reset relative logic
11	RW	0x0	resetn_timer5 When high, reset relative logic
10	RW	0x0	resetn_timer4 When high, reset relative logic
9	RW	0x0	resetn_timer3 When high, reset relative logic
8	RW	0x0	resetn_timer2 When high, reset relative logic
7	RW	0x0	resetn_timer1 When high, reset relative logic
6	RW	0x0	resetn_timer0 When high, reset relative logic
5	RW	0x0	presetn_timer When high, reset relative logic
4	RW	0x0	resetn_core_rga When high, reset relative logic
3	RW	0x0	aresetn_rga When high, reset relative logic
2	RW	0x0	hresetn_rga When high, reset relative logic
1	RW	0x0	aresetn_dcf When high, reset relative logic
0	RW	0x0	presetn_dcf When high, reset relative logic

BUSCRU_BUS_SOFTRST_CON03

Address: Operational Base(0x20010000) + offset (0x0A0C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	resetn_spi1 When high, reset relative logic
12	RW	0x0	presetn_spi1 When high, reset relative logic
11	RW	0x0	resetn_spi0 When high, reset relative logic
10	RW	0x0	presetn_spi0 When high, reset relative logic
9	RW	0x0	resetn_i2c5 When high, reset relative logic
8	RW	0x0	presetn_i2c5 When high, reset relative logic
7	RW	0x0	resetn_i2c4 When high, reset relative logic
6	RW	0x0	presetn_i2c4 When high, reset relative logic
5	RW	0x0	resetn_i2c3 When high, reset relative logic

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Bit	Attr	Reset Value	Description
4	RW	0x0	presetn_i2c3 When high, reset relative logic
3	RW	0x0	resetn_i2c1 When high, reset relative logic
2	RW	0x0	presetn_i2c1 When high, reset relative logic
1	RW	0x0	resetn_i2c0 When high, reset relative logic
0	RW	0x0	presetn_i2c0 When high, reset relative logic

BUSCRU_BUS_SOFTRST_CON04

Address: Operational Base(0x20010000) + offset (0x0A10)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	resetn_pwm3 When high, reset relative logic
8	RW	0x0	presetn_pwm3 When high, reset relative logic
7:6	RO	0x0	reserved
5	RW	0x0	resetn_pwm2 When high, reset relative logic
4	RW	0x0	presetn_pwm2 When high, reset relative logic
3:2	RO	0x0	reserved
1	RW	0x0	resetn_pwm0 When high, reset relative logic
0	RW	0x0	presetn_pwm0 When high, reset relative logic

BUSCRU_BUS_SOFTRST_CON05

Address: Operational Base(0x20010000) + offset (0x0A14)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	sresetn_uart7 When high, reset relative logic
12	RW	0x0	presetn_uart7 When high, reset relative logic
11	RW	0x0	sresetn_uart6 When high, reset relative logic
10	RW	0x0	presetn_uart6 When high, reset relative logic
9	RW	0x0	sresetn_uart5 When high, reset relative logic
8	RW	0x0	presetn_uart5 When high, reset relative logic

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Bit	Attr	Reset Value	Description
7	RW	0x0	sresetn_uart4 When high, reset relative logic
6	RW	0x0	presetn_uart4 When high, reset relative logic
5	RW	0x0	sresetn_uart3 When high, reset relative logic
4	RW	0x0	presetn_uart3 When high, reset relative logic
3	RW	0x0	sresetn_uart2 When high, reset relative logic
2	RW	0x0	presetn_uart2 When high, reset relative logic
1	RW	0x0	sresetn_uart1 When high, reset relative logic
0	RW	0x0	presetn_uart1 When high, reset relative logic

BUSCRU_BUS_SOFTRST_CON06
Address: Operational Base(0x20010000) + offset (0x0A18)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	resetn_pdm When high, reset relative logic
11	RW	0x0	mresetn_pdm When high, reset relative logic
10	RW	0x0	hresetn_pdm When high, reset relative logic
9	RW	0x0	mresetn_rkdsm When high, reset relative logic
8	RW	0x0	hresetn_rkdsm When high, reset relative logic
7	RW	0x0	mresetn_sai2 When high, reset relative logic
6	RW	0x0	hresetn_sai2 When high, reset relative logic
5	RW	0x0	mresetn_sai1 When high, reset relative logic
4	RW	0x0	hresetn_sai1 When high, reset relative logic
3	RW	0x0	mresetn_sai0 When high, reset relative logic
2	RW	0x0	hresetn_sai0 When high, reset relative logic
1	RW	0x0	resetn_tsadc When high, reset relative logic
0	RW	0x0	presetn_tsadc When high, reset relative logic

BUSCRU_BUS_SOFTRST_CON07
Address: Operational Base(0x20010000) + offset (0x0A1C)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	presetn_otp_mask When high, reset relative logic
11	RW	0x0	resetn_otpc_arb When high, reset relative logic
10	RW	0x0	resetn_user_otpc_ns When high, reset relative logic
9	RW	0x0	resetn_sbpi_otpc_ns When high, reset relative logic
8	RW	0x0	presetn_otpc_ns When high, reset relative logic
7	RW	0x0	hresetn_ns_rkce When high, reset relative logic
6	RW	0x0	presetn_rkce When high, reset relative logic
5	RW	0x0	mresetn_audio_adc_bus When high, reset relative logic
4	RW	0x0	presetn_audio_adc_bus When high, reset relative logic
3	RW	0x0	resetn_asrc1 When high, reset relative logic
2	RW	0x0	hresetn_asrc1 When high, reset relative logic
1	RW	0x0	resetn_asrc0 When high, reset relative logic
0	RW	0x0	hresetn_asrc0 When high, reset relative logic

2.4.3 PERICRU

2.4.3.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

2.4.3.2 Registers Summary

Name	Offset	Size	Reset Value	Description
PERICRU_CRU_CPLL_CON0	0x0000	W	0x0000307D	PLL configuration register0
PERICRU_CRU_CPLL_CON1	0x0004	W	0x00001041	PLL configuration register1
PERICRU_CRU_CPLL_CON2	0x0008	W	0x00000000	PLL configuration register2
PERICRU_CRU_CPLL_CON3	0x000C	W	0x00000007	PLL configuration register3
PERICRU_CRU_CPLL_CON4	0x0010	W	0x00007F00	PLL configuration register4
PERICRU_PERI_CLKSEL_CON00	0x0300	W	0x00000071	Internal clock select and division register 0
PERICRU_PERI_CLKSEL_CON01	0x0304	W	0x00000009	Internal clock select and division register 1
PERICRU_PERI_GATE_CON00	0x0800	W	0x00008000	Internal clock gate and division register 0
PERICRU_PERI_GATE_CON01	0x0804	W	0x00002800	Internal clock gate and division register 1

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Name	Offset	Size	Reset Value	Description
PERICRU_PERI_SOFTRST_CON00	0x0A00	W	0x00000000	Internal clock reset register 0
PERICRU_PERI_SOFTRST_CON01	0x0A04	W	0x00000000	Internal clock reset register 1

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

2.4.3.3 Detail Registers Description

PERICRU_CRU_CPLL_CON0

Address: Operational Base(0x20020000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	bypass PLL Bypass. FREF bypasses PLL to FOUTPOSTDIV 1'b0: No bypass 1'b1: Bypass
14:12	RW	0x3	postdiv1 First Post Divide Value, (1-7)
11:0	RW	0x07d	fbdiv Feedback Divide Value, valid divider settings are: [16, 2500] in integer mode [20, 500] in fractional mode Tips: No plus one operation

PERICRU_CRU_CPLL_CON1

Address: Operational Base(0x20020000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pllpdsel PLL global power down source selection If pllpdsel == 1, PLL can be power down only by pllpd1, otherwise pll is power down when any one of refdiv/fbdiv/fracdiv is changed or pllpd0 is asserted
14	RW	0x0	pllpd1 PLL global power down request 1'b0: No power down 1'b1: Power down
13	RW	0x0	pllpd0 PLL global power down request 1'b0: No power down 1'b1: Power down
12	RW	0x1	dsmpd PLL delta sigma modulator enable 1'b0: Modulator is enable 1'b1: Modulator is disabled
11	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
10	RW	0x0	pll_lock PLL lock status 1'b0: Unlock 1'b1: Lock
9	RO	0x0	reserved
8:6	RW	0x1	postdiv2 Second Post Divide Value, (1-7)
5:0	RW	0x01	refdiv Reference Clock Divide Value, (1-63)

PERICRU_CRU_CPLL_CON2

Address: Operational Base(0x20020000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	fout4phasepd Power down 4-phase clocks and 2X, 3X, 4X clocks 1'b0: No power down 1'b1: Power down
26	RW	0x0	foutvcopd Power down buffered VCO clock 1'b0: No power down 1'b1: Power down
25	RW	0x0	foutpostdivpd Power down all outputs except for buffered VCO clock 1'b0: No power down 1'b1: Power down
24	RW	0x0	dacpd Power down quantization noise cancellation DAC 1'b0: No power down 1'b1: Power down
23:0	RW	0x000000	fracdiv Fractional part of feedback divide (fraction = FRAC/2^24)

PERICRU_CRU_CPLL_CON3

Address: Operational Base(0x20020000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x00	ssmod_spread spread amplitude % = 0.1 * SPREAD[4: 0]
7:4	RW	0x0	ssmod_divval Divider required to set the modulation frequency
3	RW	0x0	ssmod_downspread Selects center spread or downs pread 1'b0: Center spread 1'b1: Down spread
2	RW	0x1	ssmod_reset Reset modulator state 1'b0: No reset 1'b1: Reset

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Bit	Attr	Reset Value	Description
1	RW	0x1	ssmod_disable_sscg Bypass SSMOD by module 1'b0: No bypass 1'b1: Bypass
0	RW	0x1	ssmod_bp Bypass SSMOD by integration 1'b0: No bypass 1'b1: Bypass

PERICRU_CRU_CPLL_CON4
Address: Operational Base(0x20020000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x7f	ssmod_ext_maxaddr External wave table data inputs (0-255)
7:1	RO	0x00	reserved
0	RW	0x0	ssmod_sel_ext_wave select external wave 1'b0: No select ext_wave 1'b1: Select ext_wave

PERICRU_PERI_CLKSEL_CON00
Address: Operational Base(0x20020000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:10	RW	0x0	clk_testout_peri_sel clk_testout_peri clock mux. 4'b0000: aclk_peri_root 4'b0001: pclk_peri_root 4'b0010: pclk_rtc_root 4'b0011: cclk_emmc 4'b0100: sclk_2x_fspi0 4'b0101: clk_utmi_usb2phy_otg_io 4'b0110: clk_utmi_usb2phy_host_io 4'b0111: clk48_utmi_usb2phy_io 4'b1000: clk_pipe_pipephy_io
9:8	RO	0x0	reserved
7:4	RW	0x7	clk_testout_peri_div Divide clk_testout_peri by (div_con + 1).
3:2	RO	0x0	reserved
1:0	RW	0x1	pclk_rtc_root_div Divide pclk_rtc_root by (div_con + 1).

PERICRU_PERI_CLKSEL_CON01
Address: Operational Base(0x20020000) + offset (0x0304)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	clk_ref_pipephy_sel clk_ref_pipephy clock mux. 1'b0: clk_ref_pipephy_cpll_src 1'b1: xin_osc0_ref_pipephy
11:6	RO	0x00	reserved
5:0	RW	0x09	clk_ref_pipephy_cpll_src_div Divide clk_ref_pipephy_cpll_src by (div_con + 1).

PERICRU_PERI_GATE_CON00

Address: Operational Base(0x20020000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	clk_testout_peri_en clk_testout_peri clock gating control. When high, disable clock
14	RO	0x0	reserved
13	RW	0x0	pclk_rtc_test_en pclk_rtc_test clock gating control. When high, disable clock
12	RW	0x0	hclk_arb_usb2host_en hclk_arb_usb2host clock gating control. When high, disable clock
11	RW	0x0	hclk_usb2host_en hclk_usb2host clock gating control. When high, disable clock
10	RW	0x0	clk_suspend_usb3drd_en clk_suspend_usb3drd clock gating control. When high, disable clock
9	RW	0x0	clk_ref_usb3drd_en clk_ref_usb3drd clock gating control. When high, disable clock
8	RW	0x0	aclk_usb3drd_en aclk_usb3drd clock gating control. When high, disable clock
7	RW	0x0	pclk_ioc_vccio1_en pclk_ioc_vccio1 clock gating control. When high, disable clock
6	RW	0x0	dbclk_gpio1_en dbclk_gpio1 clock gating control. When high, disable clock
5	RW	0x0	pclk_gpio1_en pclk_gpio1 clock gating control. When high, disable clock
4	RW	0x0	pclk_peri_grf_en pclk_peri_grf clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
3	RW	0x0	pclk_cru_peri_en pclk_cru_peri clock gating control. When high, disable clock
2	RW	0x0	pclk_rtc_biu_en pclk_rtc_biu clock gating control. When high, disable clock
1	RW	0x0	pclk_peri_biu_en pclk_peri_biu clock gating control. When high, disable clock
0	RW	0x0	aclk_peri_biu_en aclk_peri_biu clock gating control. When high, disable clock

PERICRU_PERI_GATE_CON01

Address: Operational Base(0x20020000) + offset (0x0804)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	clk_ref_pipephy_cpll_src_en clk_ref_pipephy_cpll_src clock gating control. When high, disable clock
13	RW	0x1	clk_cpll_pmu_src_en clk_cpll_pmu_src clock gating control. When high, disable clock
12	RO	0x0	reserved
11	RW	0x1	clk_emmc_delay_line_test_en clk_emmc_delay_line_test clock gating control. When high, disable clock
10	RW	0x0	pclk_usb2phy_en pclk_usb2phy clock gating control. When high, disable clock
9	RW	0x0	pclk_pipephy_grf_en pclk_pipephy_grf clock gating control. When high, disable clock
8	RW	0x0	pclk_pipephy_en pclk_pipephy clock gating control. When high, disable clock
7	RO	0x0	reserved
6	RW	0x0	clk48_utmi_usb2host_dft_en clk48_utmi_usb2host_dft clock gating control. When high, disable clock
5	RW	0x0	clk_utmi_usb2host_dft_en clk_utmi_usb2host_dft clock gating control. When high, disable clock
4	RW	0x0	clk_pipe_usb3drd_dft_en clk_pipe_usb3drd_dft clock gating control. When high, disable clock
3	RW	0x0	clk_utmi_usb3drd_dft_en clk_utmi_usb3drd_dft clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
2	RW	0x0	hclk_xip_fspi0_en hclk_xip_fspi0 clock gating control. When high, disable clock
1	RW	0x0	hclk_fspi0_en hclk_fspi0 clock gating control. When high, disable clock
0	RW	0x0	hclk_emmc_en hclk_emmc clock gating control. When high, disable clock

PERICRU_PERI_SOFTRST_CON00

Address: Operational Base(0x20020000) + offset (0x0A00)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	presetn_rtc_test When high, reset relative logic
12	RW	0x0	hresetn_arb_usb2host When high, reset relative logic
11	RW	0x0	hresetn_usb2host When high, reset relative logic
10:9	RO	0x0	reserved
8	RW	0x0	aresetn_usb3drd When high, reset relative logic
7	RW	0x0	presetn_ioc_vccio1 When high, reset relative logic
6	RW	0x0	dbresetn_gpio1 When high, reset relative logic
5	RW	0x0	presetn_gpio1 When high, reset relative logic
4	RW	0x0	presetn_peri_grf When high, reset relative logic
3	RW	0x0	presetn_cru_peri When high, reset relative logic
2	RW	0x0	presetn_rtc_biu When high, reset relative logic
1	RW	0x0	presetn_peri_biu When high, reset relative logic
0	RW	0x0	aresetn_peri_biu When high, reset relative logic

PERICRU_PERI_SOFTRST_CON01

Address: Operational Base(0x20020000) + offset (0x0A04)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	resetn_host_usb2phy When high, reset relative logic

Bit	Attr	Reset Value	Description
12	RW	0x0	resetn_otg_usb2phy When high, reset relative logic
11	RW	0x0	resetn_por_usb2phy When high, reset relative logic
10	RW	0x0	presetn_usb2phy When high, reset relative logic
9	RW	0x0	presetn_pipephy_grf When high, reset relative logic
8	RW	0x0	presetn_pipephy When high, reset relative logic
7	RW	0x0	resetn_ref_pipephy When high, reset relative logic
6	RO	0x0	reserved
5	RW	0x0	resetn_utmi_usb2host When high, reset relative logic
4	RO	0x0	reserved
3	RW	0x0	sresetn_2x_fspi0 When high, reset relative logic
2	RW	0x0	hresetn_xip_fspi0 When high, reset relative logic
1	RW	0x0	hresetn_fspi0 When high, reset relative logic
0	RW	0x0	hresetn_emmc When high, reset relative logic

2.4.4 CORECRU

2.4.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

2.4.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
CORECRU_CORE_CLKSEL_CON00	0x0300	W	0x00000170	Internal clock select and division register 0
CORECRU_CORE_CLKSEL_CON01	0x0304	W	0x00000701	Internal clock select and division register 1
CORECRU_CORE_CLKSEL_CON02	0x0308	W	0x00000701	Internal clock select and division register 2
CORECRU_CORE_GATE_CON00	0x0800	W	0x00008000	Internal clock gate and division register 0
CORECRU_CORE_GATE_CON01	0x0804	W	0x00000000	Internal clock gate and division register 1
CORECRU_CORE_SOFTRST_CON00	0x0A00	W	0x00000000	Internal clock reset register 0
CORECRU_CORE_SOFTRST_CON01	0x0A04	W	0x00000020	Internal clock reset register 1
CORECRU_AUTOCS_CLK_SRC_CON0	0x0D00	W	0x00A00047	bus clock auto clock swith control 0
CORECRU_AUTOCS_CLK_SRC_CON1	0x0D04	W	0x00000000	bus clock auto clock swith control 1

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

2.4.4.3 Detail Registers Description

CORECRU_CORE_CLKSEL_CON00

Address: Operational Base(0x20030000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:10	RW	0x0	clk_testout_core_sel clk_testout_core clock mux. 3'b000: clk_core_root 3'b001: aclk_core_root 3'b010: pclk_core_root 3'b011: hclk_core_biu 3'b100: test_clkout_core_pvtpll 3'b101: swclktck_io 3'b110: 1'b0 3'b111: 1'b0
9	RO	0x0	reserved
8:4	RW	0x17	clk_testout_core_div Divide clk_testout_core by (div_con + 1).
3:2	RO	0x0	reserved
1	RW	0x0	clk_core_src_sel clk_core_src clock mux. 1'b0: clk_core_pll_src 1'b1: clk_core_pvtpll_src
0	RW	0x0	clk_core_pvtpll_src_sel clk_core_pvtpll_src clock mux. 1'b0: clk_deepslow 1'b1: clk_core_pvtpll

CORECRU_CORE_CLKSEL_CON01

Address: Operational Base(0x20030000) + offset (0x0304)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	mbist_clk_a53_ndft_sel mbist_clk_a53_ndft clock mux. 1'b0: mbist_clk_core 1'b1: clk_core_pvtpll_src
14:13	RO	0x0	reserved
12:8	RW	0x07	clk_scanhs_clk_core_div8_div Divide clk_scanhs_clk_core_div8 by (div_con + 1).
7:5	RO	0x0	reserved
4:0	RW	0x01	clk_scanhs_clk_core_div2_div Divide clk_scanhs_clk_core_div2 by (div_con + 1).

CORECRU_CORE_CLKSEL_CON02

Address: Operational Base(0x20030000) + offset (0x0308)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12:8	RW	0x07	pclk_core_root_div Divide pclk_core_root by (div_con + 1).
7:5	RO	0x0	reserved
4:0	RW	0x01	aclk_core_root_div Divide aclk_core_root by (div_con + 1).

CORECRU_CORE_GATE_CON00

Address: Operational Base(0x20030000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	clk_testout_core_en clk_testout_core clock gating control. When high, disable clock
14:11	RO	0x0	reserved
10	RW	0x0	pclk_dbg_en pclk_dbg clock gating control. When high, disable clock
9	RO	0x0	reserved
8	RW	0x0	pclk_core_biu_en pclk_core_biu clock gating control. When high, disable clock
7	RW	0x0	aclk_core_biu_en aclk_core_biu clock gating control. When high, disable clock
6	RW	0x0	pclk_core_root_en pclk_core_root clock gating control. When high, disable clock
5	RW	0x0	aclk_core_root_en aclk_core_root clock gating control. When high, disable clock
4	RW	0x0	clk_core_en clk_core clock gating control. When high, disable clock
3	RW	0x0	clk_core_root_en clk_core_root clock gating control. When high, disable clock
2:1	RO	0x0	reserved
0	RW	0x0	clk_ref_pvtpll_core_en clk_ref_pvtpll_core clock gating control. When high, disable clock

CORECRU_CORE_GATE_CON01

Address: Operational Base(0x20030000) + offset (0x0804)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_scanhs_clk_core_en clk_scanhs_clk_core clock gating control. When high, disable clock
14:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12	RW	0x0	swclktck_dft_en swclktck_dft clock gating control. When high, disable clock
11:5	RO	0x00	reserved
4	RW	0x0	pclk_dft2apb_en pclk_dft2apb clock gating control. When high, disable clock
3	RO	0x0	reserved
2	RW	0x0	pclk_core_grf_en pclk_core_grf clock gating control. When high, disable clock
1	RW	0x0	pclk_cru_core_en pclk_cru_core clock gating control. When high, disable clock
0	RW	0x0	pclk_core_pvtpll_en pclk_core_pvtpll clock gating control. When high, disable clock

CORECRU_CORE_SOFTRST_CON00

Address: Operational Base(0x20030000) + offset (0x0A00)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10	RW	0x0	nl2reset When high, reset relative logic
9	RW	0x0	ndbgreset When high, reset relative logic
8	RW	0x0	ncoreset3 When high, reset relative logic
7	RW	0x0	ncoreporeset3 When high, reset relative logic
6	RW	0x0	ncoreset2 When high, reset relative logic
5	RW	0x0	ncoreporeset2 When high, reset relative logic
4	RW	0x0	ncoreset1 When high, reset relative logic
3	RW	0x0	ncoreporeset1 When high, reset relative logic
2	RW	0x0	ncoreset0 When high, reset relative logic
1	RW	0x0	ncoreporeset0 When high, reset relative logic
0	RW	0x0	resetn_ref_pvtpll_core When high, reset relative logic

CORECRU_CORE_SOFTRST_CON01

Address: Operational Base(0x20030000) + offset (0x0A04)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10	RW	0x0	presetn_dft2apb When high, reset relative logic
9	RO	0x0	reserved
8	RW	0x0	presetn_core_grf When high, reset relative logic
7	RW	0x0	presetn_cru_core When high, reset relative logic
6	RW	0x0	presetn_core_pvtpll When high, reset relative logic
5	RW	0x1	ntresetn_dbg When high, reset relative logic
4	RW	0x0	potresetn_dbg When high, reset relative logic
3	RW	0x0	presetn_dbg When high, reset relative logic
2	RW	0x0	hresetn_core_biu When high, reset relative logic
1	RW	0x0	presetn_core_biu When high, reset relative logic
0	RW	0x0	aresetn_core_biu When high, reset relative logic

CORECRU_AUTOCS_CLK_SRC_CON0

Address: Operational Base(0x20030000) + offset (0x0D00)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original clk
15:0	RW	0x0047	idle_th idle time threshold, measured by original clk

CORECRU_AUTOCS_CLK_SRC_CON1

Address: Operational Base(0x20030000) + offset (0x0D04)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	autocs_select auto switch clock selection 2'b00: div16 of original clk 2'b01: div8 of original clk 2'b10: div4 of original clk 2'b11: div2 of original clk
13	RO	0x0	reserved
12	RW	0x0	autocs_en 1'b1: enable the autocs function 1'b0: disable

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Bit	Attr	Reset Value	Description
11:0	RW	0x000	autocs_ctrl The autocs ctrl enable for internal hardware signal b0 : =0, disable ; =1, enable the signal ~(grf_st_standbywfi[0] | grf_st_standbywfe[0]) b1 : =0, disable ; =1, enable the signal ~(grf_st_standbywfi[1] | grf_st_standbywfe[1]) b2 : =0, disable ; =1, enable the signal ~(grf_st_standbywfi[2] | grf_st_standbywfe[2]) b3 : =0, disable ; =1, enable the signal ~(grf_st_standbywfi[3] | grf_st_standbywfe[3]) b4 : =0, disable ; =1, enable the signal ~(grf_st_standbywfil2) b5 : =0, disable ; =1, enable the signal ~(~noc_slave_active_pdcore) b6 : =0, disable ; =1, enable the signal ~(&{gic_nirqcpu_core,gic_nfiqcpu_core,gic_nvfiqcpu_core,gic_nvirqcpu_core}) Other bits reserved.

2.4.5 PMUCRU

2.4.5.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

2.4.5.2 Registers Summary

Name	Offset	Size	Reset Value	Description
PMUCRU_PMU_CLKSEL_CON00	0x0300	W	0x00000000	Internal clock select and division register 0
PMUCRU_PMU_CLKSEL_CON01	0x0304	W	0x00002000	Internal clock select and division register 1
PMUCRU_PMU_CLKSEL_CON02	0x0308	W	0x00000000	Internal clock select and division register 2
PMUCRU_PMU_CLKSEL_CON03	0x030C	W	0x00000000	Internal clock select and division register 3
PMUCRU_PMU_CLKSEL_CON08	0x0320	W	0x0040B71B	Internal clock select and division register 8
PMUCRU_PMU_GATE_CON00	0x0800	W	0x0000C000	Internal clock gate and division register 0
PMUCRU_PMU_GATE_CON01	0x0804	W	0x00000000	Internal clock gate and division register 1
PMUCRU_PMU_GATE_CON02	0x0808	W	0x00000040	Internal clock gate and division register 2
PMUCRU_PMU_GATE_CON03	0x080C	W	0x00000000	Internal clock gate and division register 3
PMUCRU_PMU_SOFTRST_CON00	0x0A00	W	0x00000000	Internal clock reset register 0
PMUCRU_PMU_SOFTRST_CON01	0x0A04	W	0x00000000	Internal clock reset register 1
PMUCRU_PMU_SOFTRST_CON02	0x0A08	W	0x00000000	Internal clock reset register 2
PMUCRU_PMU_SOFTRST_CON03	0x0A0C	W	0x0000003C	Internal clock reset register 3
PMUCRU_AUTOCS_BUSCLK_MUX_CON0	0x0D00	W	0x00A00047	bus clock auto clock swith control 0
PMUCRU_AUTOCS_BUSCLK_MUX_CON1	0x0D04	W	0x00000000	bus clock auto clock swith control 1

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits)

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access, **DW**-Double WORD (64 bits) access

2.4.5.3 Detail Registers Description

PMUCRU_PMU_CLKSEL_CON00

Address: Operational Base(0x20040000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:10	RW	0x00	clk_testout_pmu_sel clk_testout_pmu clock mux. 5'b00000: xin_osc0_func 5'b00001: clk_deepslow 5'b00010: clk_refout 5'b00011: busclk_pmu_root 5'b00100: clk_pmu 5'b00101: clk_pmu_hp_timer 5'b00110: clk_pmu_hp_timer_xin_pll 5'b00111: tclk_wdt_lpmcu 5'b01000: clk_pwm1 5'b01001: sclk_uart0 5'b01010: clk_i2c2 5'b01011: clk_32k_rtc 5'b01100: clk_32k_io 5'b01101: sclk_spi2ahb_io 5'b01110: clk_lpmcu_jtag_io 5'b01111: sclk_in_audio_adc 5'b10000: sclk_out_audio_adc 5'b10001: clk_rcosc_io 5'b10010: clk_rcosc_div2_io 5'b10011: clk_rcosc_div3_io 5'b10100: clk_rcosc_div4_io 5'b10101: clk_rc_400k 5'b10110: 1'b0 5'b10111: 1'b0 5'b11000: 1'b0 5'b11001: 1'b0 5'b11010: 1'b0 5'b11011: 1'b0 5'b11100: 1'b0 5'b11101: 1'b0 5'b11110: 1'b0 5'b11111: 1'b0
9:7	RO	0x0	reserved
6:4	RW	0x0	clk_testout_pmu_div Divide clk_testout_pmu by (div_con + 1).

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	clk_testout_out_sel clk_testout_out clock mux. 4'b0000: clk_testout_pmu 4'b0001: clk_testout_top 4'b0010: clk_testout_core 4'b0011: clk_testout_npu 4'b0100: clk_testout_vi 4'b0101: clk_testout_vepu 4'b0110: clk_testout_vdo 4'b0111: clk_testout_ddr 4'b1000: clk_testout_bus 4'b1001: clk_testout_peri 4'b1010: clk_testout_vcp 4'b1011: 1'b0 4'b1100: 1'b0 4'b1101: 1'b0 4'b1110: 1'b0 4'b1111: 1'b0

PMUCRU_PMU_CLKSEL_CON01
Address: Operational Base(0x20040000) + offset (0x0304)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x1	clk_pmu_hp_timer_xin_pll_sel clk_pmu_hp_timer_xin_pll clock mux. 1'b0: clk_cpll_pmu_src 1'b1: xin_osc0_func
12:8	RW	0x00	clk_pmu_hp_timer_xin_pll_div Divide clk_pmu_hp_timer_xin_pll by (div_con + 1).
7:6	RO	0x0	reserved
5:4	RW	0x0	busclk_pmu_mux_div Divide busclk_pmu_mux by (div_con + 1).
3	RW	0x0	busclk_pmu_mux_sel busclk_pmu_mux clock mux. 1'b0: busclk_pmu_32k 1'b1: clk_rcosc_src
2:0	RW	0x0	clk_rcosc_src_sel clk_rcosc_src clock mux. 3'b000: xin_osc0_func 3'b001: clk_rcosc_io 3'b010: clk_rcosc_div2_io 3'b011: clk_rcosc_div3_io 3'b100: clk_rcosc_div4_io

PMUCRU_PMU_CLKSEL_CON02
Address: Operational Base(0x20040000) + offset (0x0308)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:14	RW	0x0	clk_i2c2_sel clk_i2c2 clock mux. 2'b00: xin_osc0_func 2'b01: clk_rcosc_src 2'b10: busclk_pmu_src
13:12	RW	0x0	clk_i2c2_div Divide clk_i2c2 by (div_con + 1).
11:10	RO	0x0	reserved
9:8	RW	0x0	clk_pwm1_sel clk_pwm1 clock mux. 2'b00: xin_osc0_func 2'b01: clk_rcosc_src 2'b10: busclk_pmu_src
7:6	RW	0x0	clk_pwm1_div Divide clk_pwm1 by (div_con + 1).
5	RO	0x0	reserved
4	RW	0x0	dbclk_pmu_gpio0_sel dbclk_pmu_gpio0 clock mux. 1'b0: xin_osc0_func 1'b1: clk_deepslow
3	RO	0x0	reserved
2:1	RW	0x0	clk_deepslow_sel clk_deepslow clock mux. 2'b00: clk_xin_rc_div 2'b01: clk_32k_rtc 2'b10: clk_32k_io
0	RW	0x0	clk_xin_rc_div_sel clk_xin_rc_div clock mux. 1'b0: xin_osc0_func 1'b1: clk_rcosc_src

PMUCRU_PMU_CLKSEL_CON03

Address: Operational Base(0x20040000) + offset (0x030C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:6	RW	0x0	tclk_wdt_lpmcu_sel tclk_wdt_lpmcu clock mux. 2'b00: xin_osc0_func 2'b01: clk_rcosc_src 2'b10: busclk_pmu_src 2'b11: clk_deepslow
5:3	RO	0x0	reserved
2	RW	0x0	clk_osc_rcosc_ctrl_sel clk_osc_rcosc_ctrl clock mux. 1'b0: clk_rcosc_src 1'b1: clk_testout_out
1:0	RW	0x0	sclk_uart0_sel sclk_uart0 clock mux. 2'b00: sclk_uart0_src 2'b01: xin_osc0_func 2'b10: clk_rcosc_src

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PMUCRU_PMU_CLKSEL_CON08
Address: Operational Base(0x20040000) + offset (0x0320)

Bit	Attr	Reset Value	Description
31:0	RW	0x0040b71b	clk_xin_rc_div_div clk_xin_rc_div fraction division register. High 16-bit for numerator Low 16-bit for denominator

PMUCRU_PMU_GATE_CON00
Address: Operational Base(0x20040000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	clk_testout_pmu_en clk_testout_pmu clock gating control. When high, disable clock
14	RW	0x1	clk_testout_out_en clk_testout_out clock gating control. When high, disable clock
13	RW	0x0	clk_pmu_32k_hp_timer_en clk_pmu_32k_hp_timer clock gating control. When high, disable clock
12	RW	0x0	clk_pmu_hp_timer_en clk_pmu_hp_timer clock gating control. When high, disable clock
11	RW	0x0	clk_pmu_hp_timer_xin_pll_en clk_pmu_hp_timer_xin_pll clock gating control. When high, disable clock
10	RW	0x0	pclk_pmu_hp_timer_en pclk_pmu_hp_timer clock gating control. When high, disable clock
9	RO	0x0	reserved
8	RW	0x0	dbclk_pmu_gpio0_en dbclk_pmu_gpio0 clock gating control. When high, disable clock
7	RW	0x0	pclk_pmu_gpio0_en pclk_pmu_gpio0 clock gating control. When high, disable clock
6	RW	0x0	pclk_pmu_en pclk_pmu clock gating control. When high, disable clock
5	RW	0x0	clk_pmu_en clk_pmu clock gating control. When high, disable clock
4	RO	0x0	reserved
3	RW	0x0	hclk_pmu_biu_en hclk_pmu_biu clock gating control. When high, disable clock
2	RO	0x0	reserved
1	RW	0x0	busclk_pmu_root_en busclk_pmu_root clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
0	RW	0x0	clk_rcosc_src_en clk_rcosc_src clock gating control. When high, disable clock

PMUCRU_PMU_GATE_CON01

Address: Operational Base(0x20040000) + offset (0x0804)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	sclk_uart0_en sclk_uart0 clock gating control. When high, disable clock
10:9	RO	0x0	reserved
8	RW	0x0	pclk_uart0_en pclk_uart0 clock gating control. When high, disable clock
7	RW	0x0	clk_i2c2_en clk_i2c2 clock gating control. When high, disable clock
6	RW	0x0	pclk_i2c2_en pclk_i2c2 clock gating control. When high, disable clock
5	RW	0x0	clk_counter_pwm1_en clk_counter_pwm1 clock gating control. When high, disable clock
4	RW	0x0	clk_freq_pwm1_en clk_freq_pwm1 clock gating control. When high, disable clock
3	RW	0x0	clk_rc_pwm1_en clk_rc_pwm1 clock gating control. When high, disable clock
2	RW	0x0	clk_osc_pwm1_en clk_osc_pwm1 clock gating control. When high, disable clock
1	RW	0x0	clk_pwm1_en clk_pwm1 clock gating control. When high, disable clock
0	RW	0x0	pclk_pwm1_en pclk_pwm1 clock gating control. When high, disable clock

PMUCRU_PMU_GATE_CON02

Address: Operational Base(0x20040000) + offset (0x0808)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	hclk_pmu_sram_en hclk_pmu_sram clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
8	RW	0x0	clk_preroll_32k_en clk_preroll_32k clock gating control. When high, disable clock
7	RW	0x0	clk_preroll_en clk_preroll clock gating control. When high, disable clock
6	RW	0x1	clk_refout_en clk_refout clock gating control. When high, disable clock
5	RW	0x0	pclk_pmu_grf_en pclk_pmu_grf clock gating control. When high, disable clock
4	RW	0x0	pclk_cru_pmu_en pclk_cru_pmu clock gating control. When high, disable clock
3	RW	0x0	pclk_ioc_pmuio0_en pclk_ioc_pmuio0 clock gating control. When high, disable clock
2	RW	0x0	clk_ref_rcosc_ctrl_en clk_ref_rcosc_ctrl clock gating control. When high, disable clock
1	RW	0x0	clk_osc_rcosc_ctrl_en clk_osc_rcosc_ctrl clock gating control. When high, disable clock
0	RW	0x0	pclk_rcosc_ctrl_en pclk_rcosc_ctrl clock gating control. When high, disable clock

PMUCRU_PMU_GATE_CON03

Address: Operational Base(0x20040000) + offset (0x080C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	clk_lpmcu_jtag_dft_en clk_lpmcu_jtag_dft clock gating control. When high, disable clock
13:12	RO	0x0	reserved
11	RW	0x0	busclk_pmu1_root_en busclk_pmu1_root clock gating control. When high, disable clock
10:5	RO	0x00	reserved
4	RW	0x0	pclk_lpmcu_mailbox_en pclk_lpmcu_mailbox clock gating control. When high, disable clock
3	RW	0x0	clk_lpmcu_rtc_en clk_lpmcu_rtc clock gating control. When high, disable clock
2	RW	0x0	clk_lpmcu_en clk_lpmcu clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
1	RW	0x0	tclk_wdt_lpmcu_en tclk_wdt_lpmcu clock gating control. When high, disable clock
0	RW	0x0	pclk_wdt_lpmcu_en pclk_wdt_lpmcu clock gating control. When high, disable clock

PMUCRU_PMU_SOFTRST_CON00
Address: Operational Base(0x20040000) + offset (0x0A00)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	resetn_pmu_32k_hp_timer When high, reset relative logic
11	RW	0x0	resetn_pmu_hp_timer When high, reset relative logic
10	RW	0x0	presetn_pmu_hp_timer When high, reset relative logic
9	RO	0x0	reserved
8	RW	0x0	dbresetn_pmu_gpio0 When high, reset relative logic
7	RW	0x0	presetn_pmu_gpio0 When high, reset relative logic
6:1	RO	0x00	reserved
0	RW	0x0	hresetn_pmu_biu When high, reset relative logic

PMUCRU_PMU_SOFTRST_CON01
Address: Operational Base(0x20040000) + offset (0x0A04)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	sresetn_uart0 When high, reset relative logic
4	RW	0x0	presetn_uart0 When high, reset relative logic
3	RW	0x0	resetn_i2c2 When high, reset relative logic
2	RW	0x0	presetn_i2c2 When high, reset relative logic
1	RW	0x0	resetn_pwm1 When high, reset relative logic
0	RW	0x0	presetn_pwm1 When high, reset relative logic

PMUCRU_PMU_SOFTRST_CON02
Address: Operational Base(0x20040000) + offset (0x0A08)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	hresetn_pmu_sram When high, reset relative logic
8	RW	0x0	resetn_preroll_32k When high, reset relative logic
7	RW	0x0	resetn_preroll When high, reset relative logic
6	RO	0x0	reserved
5	RW	0x0	presetn_pmu_grf When high, reset relative logic
4	RW	0x0	presetn_cru_pmu When high, reset relative logic
3	RW	0x0	presetn_ioc_pmuio0 When high, reset relative logic
2	RW	0x0	resetn_ref_rcosc_ctrl When high, reset relative logic
1	RO	0x0	reserved
0	RW	0x0	presetn_rcosc_ctrl When high, reset relative logic

PMUCRU_PMU_SOFTRST_CON03

Address: Operational Base(0x20040000) + offset (0x0A0C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	presetn_lpmcu_mailbox When high, reset relative logic
5	RW	0x1	tresetn_lpmcu_jtag When high, reset relative logic
4	RW	0x1	resetn_lpmcu_only_core When high, reset relative logic
3	RW	0x1	resetn_lpmcu_pwup When high, reset relative logic
2	RW	0x1	resetn_lpmcu_full_cluster When high, reset relative logic
1	RW	0x0	tresetn_wdt_lpmcu When high, reset relative logic
0	RW	0x0	presetn_wdt_lpmcu When high, reset relative logic

PMUCRU_AUTOCS_BUSCLK_MUX_CON0

Address: Operational Base(0x20040000) + offset (0x0D00)

Bit	Attr	Reset Value	Description
31:16	RW	0x00a0	wait_th wait time threshold, measured by original clk
15:0	RW	0x0047	idle_th idle time threshold, measured by original clk

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PMUCRU_AUTOCS_BUSCLK_MUX_CON1
Address: Operational Base(0x20040000) + offset (0x0D04)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	autocs_select auto switch clock selection 2'b00: div16 of original clk 2'b01: div8 of original clk 2'b10: div4 of original clk 2'b11: div2 of original clk
13	RO	0x0	reserved
12	RW	0x0	autocs_en 1'b1: enable the autocs function 1'b0: disable
11:0	RW	0x000	autocs_ctrl The autocs ctrl enable for internal hardware signal b0: =0, disable ; =1, enable the signal dtp_pmuLKdr_pwrDiscTarg_vcpLKpmPwrActive Other bits reserved.

2.4.6 PMU1CRU

2.4.6.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

2.4.6.2 Registers Summary

Name	Offset	Size	Reset Value	Description
PMU1CRU_PMU1_CLKSEL_CON00	0x0300	W	0x00000002	Internal clock select and division register 0
PMU1CRU_PMU1_GATE_CON00	0x0800	W	0x00000000	Internal clock gate and division register 0
PMU1CRU_PMU1_GATE_CON01	0x0804	W	0x00000000	Internal clock gate and division register 1
PMU1CRU_PMU1_SOFTRST_CON00	0x0A00	W	0x00000000	Internal clock reset register 0
PMU1CRU_PMU1_SOFTRST_CON01	0x0A04	W	0x00000000	Internal clock reset register 1

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

2.4.6.3 Detail Registers Description

PMU1CRU_PMU1_CLKSEL_CON00
Address: Operational Base(0x20050000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x00	mclk_lpsai_div Divide mclk_lpsai by (div_con + 1).

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Bit	Attr	Reset Value	Description
7:6	RW	0x0	mclk_lpsai_sel mclk_lpsai clock mux. 2'b00: xin_osc0_func 2'b01: clk_rcosc_src 2'b10: busclk_pmu_src
5	RO	0x0	reserved
4:2	RW	0x0	sclk_1x_fspi1_div Divide sclk_1x_fspi1 by (div_con + 1).
1:0	RW	0x2	sclk_1x_fspi1_sel sclk_1x_fspi1 clock mux. 2'b00: xin_osc0_func 2'b01: clk_rcosc_src 2'b10: busclk_pmu_src

PMU1CRU_PMU1_GATE_CON00

Address: Operational Base(0x20050000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10	RW	0x0	hclk_pmu1_biu_en hclk_pmu1_biu clock gating control. When high, disable clock
9	RW	0x0	mclk_audio_adc_pmu_en mclk_audio_adc_pmu clock gating control. When high, disable clock
8	RW	0x0	pclk_audio_adc_pmu_en pclk_audio_adc_pmu clock gating control. When high, disable clock
7	RO	0x0	reserved
6	RW	0x0	pclk_cru_pmu1_en pclk_cru_pmu1 clock gating control. When high, disable clock
5	RW	0x0	pclk_ioc_pmuio1_en pclk_ioc_pmuio1 clock gating control. When high, disable clock
4	RW	0x0	sclk_1x_fspi1_en sclk_1x_fspi1 clock gating control. When high, disable clock
3	RW	0x0	hclk_xip_fspi1_en hclk_xip_fspi1 clock gating control. When high, disable clock
2	RW	0x0	hclk_fspi1_en hclk_fspi1 clock gating control. When high, disable clock
1	RW	0x0	hclk_spi2ahb_en hclk_spi2ahb clock gating control. When high, disable clock
0	RW	0x0	pclk_spi2ahb_en pclk_spi2ahb clock gating control. When high, disable clock

PMU1CRU_PMU1_GATE_CON01

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Address: Operational Base(0x20050000) + offset (0x0804)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	hclk_aoa_sram_en hclk_aoa_sram clock gating control. When high, disable clock
6:5	RO	0x0	reserved
4	RW	0x0	pclk_aoa_en pclk_aoa clock gating control. When high, disable clock
3	RW	0x0	mclk_lpsai_en mclk_lpsai clock gating control. When high, disable clock
2	RW	0x0	hclk_sai0_en hclk_lpsai clock gating control. When high, disable clock
1	RW	0x0	aclk_lpdma_en aclk_lpdma clock gating control. When high, disable clock
0	RW	0x0	pclk_lpdma_en pclk_lpdma clock gating control. When high, disable clock

PMU1CRU_PMU1_SOFTRST_CON00

Address: Operational Base(0x20050000) + offset (0x0A00)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	hresetn_pmu1_biu When high, reset relative logic
8	RW	0x0	mresetn_audio_adc_pmu When high, reset relative logic
7	RW	0x0	presetn_audio_adc_pmu When high, reset relative logic
6	RW	0x0	presetn_cru_pmu1 When high, reset relative logic
5	RW	0x0	presetn_ioc_pmuio1 When high, reset relative logic
4	RW	0x0	sresetn_1x_fspi1 When high, reset relative logic
3	RW	0x0	hresetn_xip_fspi1 When high, reset relative logic
2	RW	0x0	hresetn_fspi1 When high, reset relative logic
1	RW	0x0	hresetn_spi2ahb When high, reset relative logic
0	RW	0x0	presetn_spi2ahb When high, reset relative logic

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PMU1CRU_PMU1_SOFTRST_CON01
Address: Operational Base(0x20050000) + offset (0x0A04)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	presetn_aoa_sram When high, reset relative logic
7	RW	0x0	presetn_aoa_apb When high, reset relative logic
6	RW	0x0	presetn_aoa_aad When high, reset relative logic
5	RW	0x0	presetn_aoa_fe When high, reset relative logic
4	RW	0x0	presetn_aoa_tdd When high, reset relative logic
3	RW	0x0	mresetn_lpsai When high, reset relative logic
2	RW	0x0	hresetn_lpsai When high, reset relative logic
1	RW	0x0	aresetn_lpdma When high, reset relative logic
0	RW	0x0	presetn_lpdma When high, reset relative logic

2.4.7 DDRCRU

2.4.7.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

2.4.7.2 Registers Summary

Name	Offset	Size	Reset Value	Description
DDRCRU_DDR_CLKSEL_CON00	0x0300	W	0x000000F0	Internal clock select and division register 0
DDRCRU_DDR_GATE_CON00	0x0800	W	0x00008000	Internal clock gate and division register 0
DDRCRU_DDR_SOFTRST_CON00	0x0A00	W	0x00000000	Internal clock reset register 0

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

2.4.7.3 Detail Registers Description

DDRCRU_DDR_CLKSEL_CON00
Address: Operational Base(0x20060000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:10	RW	0x0	clk_testout_ddr_sel clk_testout_ddr clock mux. 2'b00: clk1x_ddr_root 2'b01: pclk_ddr_root 2'b10: aclk_sysmem_root

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Bit	Attr	Reset Value	Description
9:8	RO	0x0	reserved
7:4	RW	0xf	clk_testout_ddr_div Divide clk_testout_ddr by (div_con + 1).
3:0	RO	0x0	reserved

DDRCRU_DDR_GATE_CON00
Address: Operational Base(0x20060000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	clk_testout_ddr_en clk_testout_ddr clock gating control. When high, disable clock
14:10	RO	0x00	reserved
9	RW	0x0	pclk_dma2ddr_en pclk_dma2ddr clock gating control. When high, disable clock
8	RW	0x0	pclk_ddrphy_en pclk_ddrphy clock gating control. When high, disable clock
7	RW	0x0	pclk_cru_ddr_en pclk_cru_ddr clock gating control. When high, disable clock
6	RW	0x0	pclk_ddr_grf_en pclk_ddr_grf clock gating control. When high, disable clock
5	RW	0x0	pclk_dfictrl_en pclk_dfictrl clock gating control. When high, disable clock
4	RW	0x0	clk_timer_ddrmon_en clk_timer_ddrmon clock gating control. When high, disable clock
3	RW	0x0	pclk_ddrmon_en pclk_ddrmon clock gating control. When high, disable clock
2	RW	0x0	pclk_ddrc_en pclk_ddrc clock gating control. When high, disable clock
1	RW	0x0	pclk_ddr_biu_en pclk_ddr_biu clock gating control. When high, disable clock
0	RO	0x0	reserved

DDRCRU_DDR_SOFTRST_CON00
Address: Operational Base(0x20060000) + offset (0x0A00)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	presetn_dma2ddr When high, reset relative logic

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Bit	Attr	Reset Value	Description
8	RW	0x0	presetn_ddrphy When high, reset relative logic
7	RW	0x0	presetn_cru_ddr When high, reset relative logic
6	RW	0x0	presetn_ddr_grf When high, reset relative logic
5	RW	0x0	presetn_dfictrl When high, reset relative logic
4	RW	0x0	resetn_timer_ddrmon When high, reset relative logic
3	RW	0x0	presetn_ddrmon When high, reset relative logic
2	RW	0x0	presetn_ddrc When high, reset relative logic
1	RW	0x0	presetn_ddr_biu When high, reset relative logic
0	RO	0x0	reserved

2.4.8 SUBDDRCRU

2.4.8.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

2.4.8.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SUBDDRCRU_CRU_DPLL_CON0	0x0000	W	0x000030AF	PLL configuration register0
SUBDDRCRU_CRU_DPLL_CON1	0x0004	W	0x00001042	PLL configuration register1
SUBDDRCRU_CRU_DPLL_CON2	0x0008	W	0x00000000	PLL configuration register2
SUBDDRCRU_CRU_DPLL_CON3	0x000C	W	0x00000007	PLL configuration register3
SUBDDRCRU_CRU_DPLL_CON4	0x0010	W	0x00007F00	PLL configuration register4
SUBDDRCRU_SUBDDR_CLKSEL_CON00	0x0300	W	0x00000000	Internal clock select and division register 0
SUBDDRCRU_SUBDDR_GATE_CON00	0x0800	W	0x00008000	Internal clock gate and division register 0
SUBDDRCRU_SUBDDR_SOFTRST_CON00	0x0A00	W	0x00000000	Internal clock reset register 0

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

2.4.8.3 Detail Registers Description

SUBDDRCRU_CRU_DPLL_CON0

Address: Operational Base(0x20068000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	bypass PLL Bypass. FREF bypasses PLL to FOUTPOSTDIV 1'b0: No bypass 1'b1: Bypass

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Bit	Attr	Reset Value	Description
14:12	RW	0x3	postdiv1 First Post Divide Value, (1-7)
11:0	RW	0x0af	fbdiv Feedback Divide Value, valid divider settings are: [16, 2500] in integer mode [20, 500] in fractional mode Tips: No plus one operation

SUBDDRCRU_CRU_DPLL_CON1
Address: Operational Base(0x20068000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pllpdsel PLL global power down source selection If pllpdsel == 1, PLL can be power down only by pllpd1, otherwise pll is power down when any one of refdiv/fbdiv/fracdiv is changed or pllpd0 is asserted
14	RW	0x0	pllpd1 PLL global power down request 1'b0: No power down 1'b1: Power down
13	RW	0x0	pllpd0 PLL global power down request 1'b0: No power down 1'b1: Power down
12	RW	0x1	dsmpd PLL delta sigma modulator enable 1'b0: Modulator is enable 1'b1: Modulator is disabled
11	RO	0x0	reserved
10	RW	0x0	pll_lock PLL lock status 1'b0: Unlock 1'b1: Lock
9	RO	0x0	reserved
8:6	RW	0x1	postdiv2 Second Post Divide Value, (1-7)
5:0	RW	0x02	refdiv Reference Clock Divide Value, (1-63)

SUBDDRCRU_CRU_DPLL_CON2
Address: Operational Base(0x20068000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	fout4phasepd Power down 4-phase clocks and 2X, 3X, 4X clocks 1'b0: No power down 1'b1: Power down
26	RW	0x0	foutvcopd Power down buffered VCO clock 1'b0: No power down 1'b1: Power down

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Bit	Attr	Reset Value	Description
25	RW	0x0	foutpostdivpd Power down all outputs except for buffered VCO clock 1'b0: No power down 1'b1: Power down
24	RW	0x0	dacpd Power down quantization noise cancellation DAC 1'b0: No power down 1'b1: Power down
23:0	RW	0x000000	fracdiv Fractional part of feedback divide (fraction = FRAC/2^24)

SUBDDRCRU_CRU_DPLL_CON3
Address: Operational Base(0x20068000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x00	ssmod_spread spread amplitude % = 0.1 * SPREAD[4: 0]
7:4	RW	0x0	ssmod_divval Divider required to set the modulation frequency
3	RW	0x0	ssmod_downspread Selects center spread or downs pread 1'b0: Center spread 1'b1: Down spread
2	RW	0x1	ssmod_reset Reset modulator state 1'b0: No reset 1'b1: Reset
1	RW	0x1	ssmod_disable_sscg Bypass SSMOD by module 1'b0: No bypass 1'b1: Bypass
0	RW	0x1	ssmod_bp Bypass SSMOD by integration 1'b0: No bypass 1'b1: Bypass

SUBDDRCRU_CRU_DPLL_CON4
Address: Operational Base(0x20068000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x7f	ssmod_ext_maxaddr External wave table data inputs (0-255)
7:1	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	ssmod_sel_ext_wave select external wave 1'b0: No select ext_wave 1'b1: Select ext_wave

SUBDDRCRU_SUBDDR_CLKSEL_CON00
Address: Operational Base(0x20068000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	clk1x_pll_root_sel clk1x_pll_root clock mux. 1'b0: clk_dpll 1'b1: aclk_sysmem_src
0	RO	0x0	reserved

SUBDDRCRU_SUBDDR_GATE_CON00
Address: Operational Base(0x20068000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	clk_dplltest_en clk_dplltest clock gating control. When high, disable clock
14	RW	0x0	clk1x_ddr_src_en clk1x_ddr_src clock gating control. When high, disable clock
13	RW	0x0	clk1x_ddrphy_en clk1x_ddrphy clock gating control. When high, disable clock
12	RW	0x0	aclk_dma2ddr_en aclk_dma2ddr clock gating control. When high, disable clock
11	RW	0x0	clk1x_rs_en clk1x_rs clock gating control. When high, disable clock
10	RO	0x0	reserved
9	RW	0x0	clk_dfictrl_en clk_dfictrl clock gating control. When high, disable clock
8	RW	0x0	clk_ddrmon_en clk_ddrmon clock gating control. When high, disable clock
7	RW	0x0	clk_core_ddrc_en clk_core_ddrc clock gating control. When high, disable clock
6	RW	0x0	aclk_ddrsch3_vi_en aclk_ddrsch3_vi clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
5	RW	0x0	aclk_ddrsch2_poe_en aclk_ddrsch2_poe clock gating control. When high, disable clock
4	RW	0x0	aclk_ddrsch1_npu_en aclk_ddrsch1_npu clock gating control. When high, disable clock
3	RW	0x0	aclk_ddrsch0_cpu_en aclk_ddrsch0_cpu clock gating control. When high, disable clock
2	RW	0x0	aclk_ddr_biu_en aclk_ddr_biu clock gating control. When high, disable clock
1	RW	0x0	aclk_sysmem_en aclk_sysmem clock gating control. When high, disable clock
0	RW	0x0	aclk_sysmem_biu_en aclk_sysmem_biu clock gating control. When high, disable clock

SUBDDRCRU_SUBDDR_SOFTRST_CON00

Address: Operational Base(0x20068000) + offset (0x0A00)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	resetn_ddrphy When high, reset relative logic
12	RW	0x0	aresetn_dma2ddr When high, reset relative logic
11	RW	0x0	resetn_rs When high, reset relative logic
10	RO	0x0	reserved
9	RW	0x0	resetn_dfictrl When high, reset relative logic
8	RW	0x0	resetn_ddrmon When high, reset relative logic
7	RW	0x0	resetn_core_ddrc When high, reset relative logic
6	RW	0x0	aresetn_ddrsch3_vi When high, reset relative logic
5	RW	0x0	aresetn_ddrsch2_poe When high, reset relative logic
4	RW	0x0	aresetn_ddrsch1_npu When high, reset relative logic
3	RW	0x0	aresetn_ddrsch0_cpu When high, reset relative logic
2	RW	0x0	aresetn_ddr_biu When high, reset relative logic
1	RW	0x0	aresetn_sysmem When high, reset relative logic
0	RW	0x0	aresetn_sysmem_biu When high, reset relative logic

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2.4.9 VICRU

2.4.9.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

2.4.9.2 Registers Summary

Name	Offset	Size	Reset Value	Description
VICRU_VI_CLKSEL_CON00	0x0300	W	0x00000090	Internal clock select and division register 0
VICRU_VI_CLKSEL_CON01	0x0304	W	0x00000000	Internal clock select and division register 1
VICRU_VI_GATE_CON00	0x0800	W	0x00008000	Internal clock gate and division register 0
VICRU_VI_GATE_CON01	0x0804	W	0x00000000	Internal clock gate and division register 1
VICRU_VI_GATE_CON02	0x0808	W	0x00000000	Internal clock gate and division register 2
VICRU_VI_GATE_CON03	0x080C	W	0x00000000	Internal clock gate and division register 3
VICRU_VI_GATE_CON04	0x0810	W	0x000001F0	Internal clock gate and division register 4
VICRU_VI_SOFTRST_CON00	0x0A00	W	0x00000000	Internal clock reset register 0
VICRU_VI_SOFTRST_CON01	0x0A04	W	0x00000000	Internal clock reset register 1
VICRU_VI_SOFTRST_CON02	0x0A08	W	0x00000000	Internal clock reset register 2
VICRU_VI_SOFTRST_CON03	0x0A0C	W	0x00000002	Internal clock reset register 3

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

2.4.9.3 Detail Registers Description

VICRU_VI_CLKSEL_CON00

Address: Operational Base(0x20070000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	mbist_clk_pvtpll_vi_sel mbist_clk_pvtpll_vi clock mux. 1'b0: mbist_clk_isp 1'b1: clk_isp_pvtpll_src
14	RW	0x0	clk_gmac_ptp_ref_sel clk_gmac_ptp_ref clock mux. 1'b0: clk_gmac_ptp_ref_src 1'b1: clk_gmac_ptp_from_io
13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:8	RW	0x00	clk_testout_vi_sel clk_testout_vi clock mux. 5'b00000: aclk_vi_root 5'b00001: hclk_vi_root 5'b00010: pclk_vi_root 5'b00011: aclk_gmac_root 5'b00100: clk_core_isp_root 5'b00101: dclk_vicap_root 5'b00110: clk_gmac_ptp_ref 5'b00111: clk_gmac_125m_matrix 5'b01000: test_clkout_vi_pvtpll 5'b01001: cclk_sdmmc0 5'b01010: clk_sys_dsmc 5'b01011: clk_can0 5'b01100: clk_can1 5'b01101: clk_saradc1_src 5'b01110: clk_saradc2_src 5'b01111: clk_saradc1_rcosc_io 5'b10000: clk_saradc2_rcosc_io 5'b10001: test_clk_out_macphy_io 5'b10010: test_clk_rmii_macphy_io 5'b10011: clk_rmii_from_iomux_m0 5'b10100: clk_rmii_from_iomux_m1 5'b10101: clk_rmii_from_macphy 5'b10110: clk_rxbyteclkhs_0_io 5'b10111: clk_rxbyteclkhs_1_io 5'b11000: clk_rxbyteclkhs_2_io 5'b11001: clk_rxbyteclkhs_3_io 5'b11010: pclkin_vicap_cif_iobuf 5'b11011: clk_gmac_ptp_from_io 5'b11100: 1'b0 5'b11101: 1'b0 5'b11110: 1'b0 5'b11111: 1'b0
7:4	RW	0x9	clk_testout_vi_div Divide clk_testout_vi by (div_con + 1).
3	RW	0x0	clk_saradc2_sel clk_saradc2 clock mux. 1'b0: clk_saradc2_src 1'b1: clk_saradc2_rcosc_io
2	RW	0x0	clk_saradc1_sel clk_saradc1 clock mux. 1'b0: clk_saradc1_src 1'b1: clk_saradc1_rcosc_io
1	RW	0x0	clk_core_isp_root_sel clk_core_isp_root clock mux. 1'b0: clk_isp_pll_src 1'b1: clk_isp_pvtpll_src
0	RW	0x0	clk_isp_pvtpll_src_sel clk_isp_pvtpll_src clock mux. 1'b0: clk_deepslow 1'b1: clksp_pvtpll

VICRU_VI_CLKSEL_CON01
Address: Operational Base(0x20070000) + offset (0x0304)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	clk_in_macphy_sel clk_in_macphy clock mux. 1'b0: xin_osc0_ref_macphy 1'b1: clk_in_50m_macphy
0	RW	0x0	clk_in_50m_macphy_sel clk_in_50m_macphy clock mux. 1'b0: clk_matrix_50m_vi 1'b1: xin_osc0_func

VICRU_VI_GATE_CON00

Address: Operational Base(0x20070000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	clk_testout_vi_en clk_testout_vi clock gating control. When high, disable clock
14	RW	0x0	clk_rmii_macphy_cru_en clk_rmii_macphy_cru clock gating control. When high, disable clock
13	RW	0x0	clk_rmii_macphy_io_en clk_rmii_macphy_io clock gating control. When high, disable clock
12	RW	0x0	clk_in_50m_macphy_en clk_in_50m_macphy clock gating control. When high, disable clock
11	RW	0x0	hclk_can1_en hclk_can1 clock gating control. When high, disable clock
10	RW	0x0	hclk_can0_en hclk_can0 clock gating control. When high, disable clock
9	RW	0x0	aclk_dsmc_en aclk_dsmc clock gating control. When high, disable clock
8	RW	0x0	pclk_dsmc_en pclk_dsmc clock gating control. When high, disable clock
7	RW	0x0	pclk_vi_pvtpll_en pclk_vi_pvtpll clock gating control. When high, disable clock
6	RW	0x0	pclk_vi_grf_en pclk_vi_grf clock gating control. When high, disable clock
5	RW	0x0	pclk_cru_vi_en pclk_cru_vi clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
4	RW	0x0	pclk_vi_biu_en pclk_vi_biu clock gating control. When high, disable clock
3	RW	0x0	hclk_vi_biu_en hclk_vi_biu clock gating control. When high, disable clock
2	RW	0x0	aclk_vi_biu_en aclk_vi_biu clock gating control. When high, disable clock
1	RW	0x0	aclk_gmac_biu_en aclk_gmac_biu clock gating control. When high, disable clock
0	RW	0x0	clk_ref_pvtpll_isp_en clk_ref_pvtpll_isp clock gating control. When high, disable clock

VICRU_VI_GATE_CON01

Address: Operational Base(0x20070000) + offset (0x0804)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	pclk_ioc_vccio7_en pclk_ioc_vccio7 clock gating control. When high, disable clock
13	RW	0x0	pclk_ioc_vccio6_en pclk_ioc_vccio6 clock gating control. When high, disable clock
12	RW	0x0	pclk_ioc_vccio5_en pclk_ioc_vccio5 clock gating control. When high, disable clock
11	RW	0x0	pclk_ioc_vccio4_en pclk_ioc_vccio4 clock gating control. When high, disable clock
10	RW	0x0	pclk_ioc_vccio2_en pclk_ioc_vccio2 clock gating control. When high, disable clock
9	RW	0x0	dbclk_gpio7_en dbclk_gpio7 clock gating control. When high, disable clock
8	RW	0x0	pclk_gpio7_en pclk_gpio7 clock gating control. When high, disable clock
7	RW	0x0	dbclk_gpio6_en dbclk_gpio6 clock gating control. When high, disable clock
6	RW	0x0	pclk_gpio6_en pclk_gpio6 clock gating control. When high, disable clock
5	RW	0x0	dbclk_gpio5_en dbclk_gpio5 clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
4	RW	0x0	pclk_gpio5_en pclk_gpio5 clock gating control. When high, disable clock
3	RW	0x0	dbclk_gpio4_en dbclk_gpio4 clock gating control. When high, disable clock
2	RW	0x0	pclk_gpio4_en pclk_gpio4 clock gating control. When high, disable clock
1	RW	0x0	dbclk_gpio2_en dbclk_gpio2 clock gating control. When high, disable clock
0	RW	0x0	pclk_gpio2_en pclk_gpio2 clock gating control. When high, disable clock

VICRU_VI_GATE_CON02

Address: Operational Base(0x20070000) + offset (0x0808)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12	RW	0x0	clk_core_vpsl_en clk_core_vpsl clock gating control. When high, disable clock
11	RW	0x0	aclk_vpsl_en aclk_vpsl clock gating control. When high, disable clock
10	RW	0x0	hclk_vpsl_en hclk_vpsl clock gating control. When high, disable clock
9	RW	0x0	clk_core_vpss_en clk_core_vpss clock gating control. When high, disable clock
8	RW	0x0	aclk_vpss_en aclk_vpss clock gating control. When high, disable clock
7	RW	0x0	hclk_vpss_en hclk_vpss clock gating control. When high, disable clock
6	RW	0x0	isp0clk_vicap_en isp0clk_vicap clock gating control. When high, disable clock
5	RW	0x0	dclk_vicap_en dclk_vicap clock gating control. When high, disable clock
4	RW	0x0	aclk_vicap_en aclk_vicap clock gating control. When high, disable clock
3	RW	0x0	hclk_vicap_en hclk_vicap clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
2	RW	0x0	clk_core_isp_en clk_core_isp clock gating control. When high, disable clock
1	RW	0x0	aclk_isp_en aclk_isp clock gating control. When high, disable clock
0	RW	0x0	hclk_isp_en hclk_isp clock gating control. When high, disable clock

VICRU_VI_GATE_CON03

Address: Operational Base(0x20070000) + offset (0x080C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	clk_50m_gmac_iobuf_en clk_50m_gmac_iobuf clock gating control. When high, disable clock
13	RW	0x0	pclk_macphy_en pclk_macphy clock gating control. When high, disable clock
12	RW	0x0	pclk_csiphy1_en pclk_csiphy1 clock gating control. When high, disable clock
11	RW	0x0	pclk_csiphy0_en pclk_csiphy0 clock gating control. When high, disable clock
10	RW	0x0	pclk_gmac_en pclk_gmac clock gating control. When high, disable clock
9	RW	0x0	aclk_gmac_en aclk_gmac clock gating control. When high, disable clock
8	RW	0x0	hclk_sdmmc0_en hclk_sdmmc0 clock gating control. When high, disable clock
7	RW	0x0	dclk_csi2host3_en dclk_csi2host3 clock gating control. When high, disable clock
6	RW	0x0	pclk_csi2host3_en pclk_csi2host3 clock gating control. When high, disable clock
5	RW	0x0	dclk_csi2host2_en dclk_csi2host2 clock gating control. When high, disable clock
4	RW	0x0	pclk_csi2host2_en pclk_csi2host2 clock gating control. When high, disable clock
3	RW	0x0	dclk_csi2host1_en dclk_csi2host1 clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
2	RW	0x0	pclk_csi2host1_en pclk_csi2host1 clock gating control. When high, disable clock
1	RW	0x0	dclk_csi2host0_en dclk_csi2host0 clock gating control. When high, disable clock
0	RW	0x0	pclk_csi2host0_en pclk_csi2host0 clock gating control. When high, disable clock

VICRU_VI_GATE_CON04

Address: Operational Base(0x20070000) + offset (0x0810)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	pclkin_vicap_cif_dft_en pclkin_vicap_cif_dft clock gating control. When high, disable clock
14	RW	0x0	clk_rxbyteclkhs_3_dft_en clk_rxbyteclkhs_3_dft clock gating control. When high, disable clock
13	RW	0x0	clk_rxbyteclkhs_2_dft_en clk_rxbyteclkhs_2_dft clock gating control. When high, disable clock
12	RW	0x0	clk_rxbyteclkhs_1_dft_en clk_rxbyteclkhs_1_dft clock gating control. When high, disable clock
11	RW	0x0	clk_rxbyteclkhs_0_dft_en clk_rxbyteclkhs_0_dft clock gating control. When high, disable clock
10	RW	0x0	rx3pclk_vicap_lvds_dft_en rx3pclk_vicap_lvds_dft clock gating control. When high, disable clock
9	RW	0x0	rx2pclk_vicap_lvds_dft_en rx2pclk_vicap_lvds_dft clock gating control. When high, disable clock
8	RW	0x1	clk_vop_delay_line_test_en clk_vop_delay_line_test clock gating control. When high, disable clock
7	RW	0x1	clk_dsmc_delay_line_test_en clk_dsmc_delay_line_test clock gating control. When high, disable clock
6	RW	0x1	clk_sdmmc0_delay_line_test_en clk_sdmmc0_delay_line_test clock gating control. When high, disable clock
5	RW	0x1	clk_cif_delay_line_test_m1_en clk_cif_delay_line_test_m1 clock gating control. When high, disable clock
4	RW	0x1	clk_cif_delay_line_test_m0_en clk_cif_delay_line_test_m0 clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
3	RW	0x0	rx1pclk_vicap_lvds_dft_en rx1pclk_vicap_lvds_dft clock gating control. When high, disable clock
2	RW	0x0	pclk_saradc2_en pclk_saradc2 clock gating control. When high, disable clock
1	RW	0x0	rx0pclk_vicap_lvds_dft_en rx0pclk_vicap_lvds_dft clock gating control. When high, disable clock
0	RW	0x0	pclk_saradc1_en pclk_saradc1 clock gating control. When high, disable clock

VICRU_VI_SOFTRST_CON00
Address: Operational Base(0x20070000) + offset (0x0A00)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	resetn_can1 When high, reset relative logic
12	RW	0x0	hresetn_can1 When high, reset relative logic
11	RW	0x0	resetn_can0 When high, reset relative logic
10	RW	0x0	hresetn_can0 When high, reset relative logic
9	RW	0x0	aresetn_dsmc When high, reset relative logic
8	RW	0x0	presetn_dsmc When high, reset relative logic
7	RW	0x0	presetn_vi_pvtpll When high, reset relative logic
6	RW	0x0	presetn_vi_grf When high, reset relative logic
5	RW	0x0	presetn_cru_vi When high, reset relative logic
4	RW	0x0	presetn_vi_biu When high, reset relative logic
3	RW	0x0	hresetn_vi_biu When high, reset relative logic
2	RW	0x0	aresetn_vi_biu When high, reset relative logic
1	RW	0x0	aresetn_gmac_biu When high, reset relative logic
0	RW	0x0	resetn_ref_pvtpll_isp When high, reset relative logic

VICRU_VI_SOFTRST_CON01
Address: Operational Base(0x20070000) + offset (0x0A04)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	presetn_ioc_vccio7 When high, reset relative logic
13	RW	0x0	presetn_ioc_vccio6 When high, reset relative logic
12	RW	0x0	presetn_ioc_vccio5 When high, reset relative logic
11	RW	0x0	presetn_ioc_vccio4 When high, reset relative logic
10	RW	0x0	presetn_ioc_vccio2 When high, reset relative logic
9	RW	0x0	dbresetn_gpio7 When high, reset relative logic
8	RW	0x0	presetn_gpio7 When high, reset relative logic
7	RW	0x0	dbresetn_gpio6 When high, reset relative logic
6	RW	0x0	presetn_gpio6 When high, reset relative logic
5	RW	0x0	dbresetn_gpio5 When high, reset relative logic
4	RW	0x0	presetn_gpio5 When high, reset relative logic
3	RW	0x0	dbresetn_gpio4 When high, reset relative logic
2	RW	0x0	presetn_gpio4 When high, reset relative logic
1	RW	0x0	dbresetn_gpio2 When high, reset relative logic
0	RW	0x0	presetn_gpio2 When high, reset relative logic

VICRU_VI_SOFTRST_CON02

Address: Operational Base(0x20070000) + offset (0x0A08)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	presetn_csiphy1 When high, reset relative logic
13	RW	0x0	presetn_csiphy0 When high, reset relative logic
12	RW	0x0	aresetn_gmac When high, reset relative logic
11	RW	0x0	hresetn_sdmmc0 When high, reset relative logic
10	RW	0x0	presetn_csi2host3 When high, reset relative logic

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Bit	Attr	Reset Value	Description
9	RW	0x0	presetn_csi2host2 When high, reset relative logic
8	RW	0x0	presetn_csi2host1 When high, reset relative logic
7	RW	0x0	presetn_csi2host0 When high, reset relative logic
6	RW	0x0	resetn_core_vpsl When high, reset relative logic
5	RW	0x0	resetn_core_vpss When high, reset relative logic
4	RW	0x0	isp0resetn_vicap When high, reset relative logic
3	RW	0x0	dresetn_vicap When high, reset relative logic
2	RW	0x0	aresetn_vicap When high, reset relative logic
1	RW	0x0	hresetn_vicap When high, reset relative logic
0	RW	0x0	resetn_core_isp When high, reset relative logic

VICRU_VI_SOFTRST_CON03
Address: Operational Base(0x20070000) + offset (0x0A0C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	resetn_saradc2 When high, reset relative logic
5	RW	0x0	presetn_saradc2 When high, reset relative logic
4	RO	0x0	reserved
3	RW	0x0	resetn_saradc1 When high, reset relative logic
2	RW	0x0	presetn_saradc1 When high, reset relative logic
1	RW	0x1	resetn_macphy When high, reset relative logic
0	RW	0x0	presetn_macphy When high, reset relative logic

2.4.10 VEPUCRU

2.4.10.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

2.4.10.2 Registers Summary

Name	Offset	Size	Reset Value	Description
VEPUCRU_VEPU_CLKSEL_CON00	0x0300	W	0x00000070	Internal clock select and division register 0
VEPUCRU_VEPU_GATE_CON00	0x0800	W	0x00008000	Internal clock gate and division register 0

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Name	Offset	Size	Reset Value	Description
VEPUCRU_VEPU_GATE_CON01	0x0804	W	0x00000010	Internal clock gate and division register 1
VEPUCRU_VEPU_SOFTRST_CON00	0x0A00	W	0x00000000	Internal clock reset register 0
VEPUCRU_VEPU_SOFTRST_CON01	0x0A04	W	0x00000000	Internal clock reset register 1

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

2.4.10.3 Detail Registers Description

VEPUCRU_VEPU_CLKSEL_CON00

Address: Operational Base(0x20080000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	mbist_clk_pvtpll_vepu_sel mbist_clk_pvtpll_vepu clock mux. 1'b0: mbist_clk_vepu 1'b1: clk_vepu_pvtpll_src
14:13	RO	0x0	reserved
12:10	RW	0x0	clk_testout_vepu_sel clk_testout_vepu clock mux. 3'b000: aclk_vepu_root 3'b001: hclk_vepu_root 3'b010: pclk_vepu_root 3'b011: clk_core_vepu 3'b100: test_clkout_vepu_pvtpll 3'b101: cclk_sdmmc1 3'b110: clk_saradc0_src 3'b111: clk_saradc0_rcosc_io
9	RO	0x0	reserved
8:4	RW	0x07	clk_testout_vepu_div Divide clk_testout_vepu by (div_con + 1).
3	RO	0x0	reserved
2	RW	0x0	clk_saradc0_sel clk_saradc0 clock mux. 1'b0: clk_saradc0_src 1'b1: clk_saradc0_rcosc_io
1	RW	0x0	clk_core_vepu_occmux_sel clk_core_vepu_occmux clock mux. 1'b0: clk_vepu_pll_src 1'b1: clk_vepu_pvtpll_src
0	RW	0x0	clk_vepu_pvtpll_src_sel clk_vepu_pvtpll_src clock mux. 1'b0: clk_deepslow 1'b1: clk_vepu_pvtpll

VEPUCRU_VEPU_GATE_CON00

Address: Operational Base(0x20080000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15	RW	0x1	clk_testout_vepu_en clk_testout_vepu clock gating control. When high, disable clock
14:13	RO	0x0	reserved
12	RW	0x0	hclk_sdmmc1_en hclk_sdmmc1 clock gating control. When high, disable clock
11	RO	0x0	reserved
10	RW	0x0	pclk_saradc0_en pclk_saradc0 clock gating control. When high, disable clock
9	RW	0x0	pclk_ioc_vccio3_en pclk_ioc_vccio3 clock gating control. When high, disable clock
8	RW	0x0	dbclk_gpio3_en dbclk_gpio3 clock gating control. When high, disable clock
7	RW	0x0	pclk_gpio3_en pclk_gpio3 clock gating control. When high, disable clock
6	RO	0x0	reserved
5	RW	0x0	pclk_vepu_grf_en pclk_vepu_grf clock gating control. When high, disable clock
4	RW	0x0	pclk_cru_vepu_en pclk_cru_vepu clock gating control. When high, disable clock
3	RW	0x0	pclk_vepu_biu_en pclk_vepu_biu clock gating control. When high, disable clock
2	RW	0x0	hclk_vepu_biu_en hclk_vepu_biu clock gating control. When high, disable clock
1	RW	0x0	aclk_vepu_biu_en aclk_vepu_biu clock gating control. When high, disable clock
0	RW	0x0	clk_ref_pvtpll_vepu_en clk_ref_pvtpll_vepu clock gating control. When high, disable clock

VEPUCRU_VEPU_GATE_CON01

Address: Operational Base(0x20080000) + offset (0x0804)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x1	clk_sdmmc1_delay_line_test_en clk_sdmmc1_delay_line_test clock gating control. When high, disable clock
3	RW	0x0	clk_core_vepu_en clk_core_vepu clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
2	RW	0x0	aclk_vepu_en aclk_vepu clock gating control. When high, disable clock
1	RW	0x0	hclk_vepu_en hclk_vepu clock gating control. When high, disable clock
0	RW	0x0	pclk_vepu_pvtpll_en pclk_vepu_pvtpll clock gating control. When high, disable clock

VEPUCRU_VEPU_SOFTRST_CON00

Address: Operational Base(0x20080000) + offset (0x0A00)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	hresetn_sdmmc1 When high, reset relative logic
12	RO	0x0	reserved
11	RW	0x0	resetn_saradc0 When high, reset relative logic
10	RW	0x0	presetn_saradc0 When high, reset relative logic
9	RW	0x0	presetn_ioc_vccio3 When high, reset relative logic
8	RW	0x0	dbresetn_gpio3 When high, reset relative logic
7	RW	0x0	presetn_gpio3 When high, reset relative logic
6	RO	0x0	reserved
5	RW	0x0	presetn_vepu_grf When high, reset relative logic
4	RW	0x0	presetn_cru_vepu When high, reset relative logic
3	RW	0x0	presetn_vepu_biu When high, reset relative logic
2	RW	0x0	hresetn_vepu_biu When high, reset relative logic
1	RW	0x0	aresetn_vepu_biu When high, reset relative logic
0	RW	0x0	resetn_ref_pvtpll_vepu When high, reset relative logic

VEPUCRU_VEPU_SOFTRST_CON01

Address: Operational Base(0x20080000) + offset (0x0A04)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	resetn_core_vepu When high, reset relative logic

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Bit	Attr	Reset Value	Description
2	RW	0x0	aresetn_vepu When high, reset relative logic
1	RW	0x0	hresetn_vepu When high, reset relative logic
0	RW	0x0	presetn_vepu_pvtpll When high, reset relative logic

2.4.11 NPUCRU

2.4.11.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

2.4.11.2 Registers Summary

Name	Offset	Size	Reset Value	Description
NPUCRU_NPU_CLKSEL_CON00	0x0300	W	0x000000F0	Internal clock select and division register 0
NPUCRU_NPU_GATE_CON00	0x0800	W	0x00008000	Internal clock gate and division register 0
NPUCRU_NPU_SOFTRST_CON00	0x0A00	W	0x00000000	Internal clock reset register 0

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

2.4.11.3 Detail Registers Description

NPUCRU_NPU_CLKSEL_CON00

Address: Operational Base(0x20090000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	mbist_clk_pvtpll_npu_sel mbist_clk_pvtpll_npu clock mux. 1'b0: mbist_clk_npu 1'b1: clk_npu_pvtpll_src
14:12	RO	0x0	reserved
11:10	RW	0x0	clk_testout_npu_sel clk_testout_npu clock mux. 2'b00: aclk_npu_root 2'b01: hclk_npu_root 2'b10: pclk_npu_root 2'b11: test_clkout_npu_pvtpll
9	RO	0x0	reserved
8:4	RW	0x0f	clk_testout_npu_div Divide clk_testout_npu by (div_con + 1).
3:2	RO	0x0	reserved
1	RW	0x0	aclk_npu_root_sel aclk_npu_root clock mux. 1'b0: clk_npu_pll_src 1'b1: clk_npu_pvtpll_src
0	RW	0x0	clk_npu_pvtpll_src_sel clk_npu_pvtpll_src clock mux. 1'b0: clk_deepslow 1'b1: clk_npu_pvtpll

NPUCRU_NPU_GATE_CON00

Address: Operational Base(0x20090000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	clk_testout_npu_en clk_testout_npu clock gating control. When high, disable clock
14:11	RO	0x0	reserved
10	RW	0x0	aclk_rknn_en aclk_rknn clock gating control. When high, disable clock
9	RW	0x0	hclk_rknn_en hclk_rknn clock gating control. When high, disable clock
8	RW	0x0	pclk_npu_pvtpll_en pclk_npu_pvtpll clock gating control. When high, disable clock
7	RO	0x0	reserved
6	RW	0x0	pclk_npu_grf_en pclk_npu_grf clock gating control. When high, disable clock
5	RW	0x0	pclk_cru_npu_en pclk_cru_npu clock gating control. When high, disable clock
4	RW	0x0	pclk_npu_biu_en pclk_npu_biu clock gating control. When high, disable clock
3	RW	0x0	hclk_npu_biu_en hclk_npu_biu clock gating control. When high, disable clock
2	RW	0x0	aclk_npu_biu_en aclk_npu_biu clock gating control. When high, disable clock
1	RO	0x0	reserved
0	RW	0x0	clk_ref_pvtpll_npu_en clk_ref_pvtpll_npu clock gating control. When high, disable clock

NPUCRU_NPU_SOFTRST_CON00

Address: Operational Base(0x20090000) + offset (0x0A00)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10	RW	0x0	aresetn_rknn When high, reset relative logic
9	RW	0x0	hresetn_rknn When high, reset relative logic
8	RW	0x0	presetn_npu_pvtpll When high, reset relative logic
7	RO	0x0	reserved
6	RW	0x0	presetn_npu_grf When high, reset relative logic

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Bit	Attr	Reset Value	Description
5	RW	0x0	presetn_cru_npu When high, reset relative logic
4	RW	0x0	presetn_npu_biu When high, reset relative logic
3	RW	0x0	hresetn_npu_biu When high, reset relative logic
2	RW	0x0	aresetn_npu_biu When high, reset relative logic
1	RO	0x0	reserved
0	RW	0x0	resetn_ref_pvtpll_npu When high, reset relative logic

2.4.12 VDOCRU

2.4.12.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

2.4.12.2 Registers Summary

Name	Offset	Size	Reset Value	Description
VDOCRU_VDO_CLKSEL_CON00	0x0300	W	0x00000070	Internal clock select and division register 0
VDOCRU_VDO_GATE_CON00	0x0800	W	0x00008000	Internal clock gate and division register 0
VDOCRU_VDO_GATE_CON01	0x0804	W	0x00000000	Internal clock gate and division register 1
VDOCRU_VDO_GATE_CON02	0x0808	W	0x00000000	Internal clock gate and division register 2
VDOCRU_VDO_SOFTRST_CON00	0x0A00	W	0x00000000	Internal clock reset register 0
VDOCRU_VDO_SOFTRST_CON01	0x0A04	W	0x00000000	Internal clock reset register 1

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

2.4.12.3 Detail Registers Description

VDOCRU_VDO_CLKSEL_CON00

Address: Operational Base(0x200A0000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:10	RW	0x0	clk_testout_vdo_sel clk_testout_vdo clock mux. 4'b0000: aclk_vdo_root 4'b0001: aclk_rkvdec_root 4'b0010: hclk_vdo_root 4'b0011: pclk_vdo_root 4'b0100: clk_hevc_ca_rkvdec 4'b0101: dclk_vop 4'b0110: dclk_ooc 4'b0111: dclk_decom 4'b1000: clk_txbyteclkhs_io 4'b1001: clk_rxclkesc_io 4'b1010: 1'b0 4'b1011: 1'b0 4'b1100: 1'b0 4'b1101: 1'b0 4'b1110: 1'b0 4'b1111: 1'b0
9:8	RO	0x0	reserved
7:4	RW	0x7	clk_testout_vdo_div Divide clk_testout_vdo by (div_con + 1).
3:0	RO	0x0	reserved

VDOCRU_VDO_GATE_CON00

Address: Operational Base(0x200A0000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	clk_testout_vdo_en clk_testout_vdo clock gating control. When high, disable clock
14	RW	0x0	hclk_ooc_en hclk_ooc clock gating control. When high, disable clock
13	RW	0x0	aclk_ooc_en aclk_ooc clock gating control. When high, disable clock
12	RO	0x0	reserved
11	RW	0x0	hclk_vop_en hclk_vop clock gating control. When high, disable clock
10	RW	0x0	aclk_vop_en aclk_vop clock gating control. When high, disable clock
9	RW	0x0	clk_hevc_ca_rkvdec_en clk_hevc_ca_rkvdec clock gating control. When high, disable clock
8	RW	0x0	hclk_rkvdec_en hclk_rkvdec clock gating control. When high, disable clock
7	RW	0x0	aclk_rkvdec_en aclk_rkvdec clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
6	RW	0x0	pclk_vdo_grf_en pclk_vdo_grf clock gating control. When high, disable clock
5	RW	0x0	pclk_cru_vdo_en pclk_cru_vdo clock gating control. When high, disable clock
4	RW	0x0	pclk_vdo_biu_en pclk_vdo_biu clock gating control. When high, disable clock
3	RW	0x0	hclk_vdo_biu_en hclk_vdo_biu clock gating control. When high, disable clock
2	RO	0x0	reserved
1	RW	0x0	aclk_vdo_biu_en aclk_vdo_biu clock gating control. When high, disable clock
0	RW	0x0	aclk_rkvdec_biu_en aclk_rkvdec_biu clock gating control. When high, disable clock

VDOCRU_VDO_GATE_CON01

Address: Operational Base(0x200A0000) + offset (0x0804)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	pclk_dsiphy_en pclk_dsiphy clock gating control. When high, disable clock
12	RW	0x0	pclk_mipi_dsi_en pclk_mipi_dsi clock gating control. When high, disable clock
11	RO	0x0	reserved
10	RW	0x0	pclk_decom_en pclk_decom clock gating control. When high, disable clock
9	RW	0x0	aclk_decom_en aclk_decom clock gating control. When high, disable clock
8	RW	0x0	dclk_decom_en dclk_decom clock gating control. When high, disable clock
7	RO	0x0	reserved
6	RW	0x0	hclk_rkmmu_decom_en hclk_rkmmu_decom clock gating control. When high, disable clock
5	RW	0x0	aclk_rkmmu_decom_en aclk_rkmmu_decom clock gating control. When high, disable clock
4	RW	0x0	aclk_rkjpeg_en aclk_rkjpeg clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
3	RW	0x0	hclk_rkjpeg_en hclk_rkjpeg clock gating control. When high, disable clock
2:0	RO	0x0	reserved

VDOCRU_VDO_GATE_CON02

Address: Operational Base(0x200A0000) + offset (0x0808)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	clk_rxclkesc_dft_en clk_rxclkesc_dft clock gating control. When high, disable clock
0	RW	0x0	clk_txbyteclkhs_dft_en clk_txbyteclkhs_dft clock gating control. When high, disable clock

VDOCRU_VDO_SOFTRST_CON00

Address: Operational Base(0x200A0000) + offset (0x0A00)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	dresetn_ooc When high, reset relative logic
14	RW	0x0	hresetn_ooc When high, reset relative logic
13	RW	0x0	aresetn_ooc When high, reset relative logic
12	RW	0x0	dresetn_vop When high, reset relative logic
11	RW	0x0	hresetn_vop When high, reset relative logic
10	RW	0x0	aresetn_vop When high, reset relative logic
9	RW	0x0	resetn_hevc_ca_rkvdec When high, reset relative logic
8	RW	0x0	hresetn_rkvdec When high, reset relative logic
7	RW	0x0	aresetn_rkvdec When high, reset relative logic
6	RW	0x0	presetn_vdo_grf When high, reset relative logic
5	RW	0x0	presetn_cru_vdo When high, reset relative logic
4	RW	0x0	presetn_vdo_biu When high, reset relative logic
3	RW	0x0	hresetn_vdo_biu When high, reset relative logic
2	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x0	aresetn_vdo_biu When high, reset relative logic
0	RW	0x0	aresetn_rkvdec_biu When high, reset relative logic

VDOCRU_VDO_SOFTRST_CON01
Address: Operational Base(0x200A0000) + offset (0x0A04)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	presetn_dsiphy When high, reset relative logic
12	RW	0x0	presetn_mipi_dsi When high, reset relative logic
11	RO	0x0	reserved
10	RW	0x0	presetn_decom When high, reset relative logic
9	RW	0x0	aresetn_decom When high, reset relative logic
8	RW	0x0	dresetn_decom When high, reset relative logic
7	RO	0x0	reserved
6	RW	0x0	hresetn_rkmmu_decom When high, reset relative logic
5	RW	0x0	aresetn_rkmmu_decom When high, reset relative logic
4	RW	0x0	aresetn_rkjpeg When high, reset relative logic
3	RW	0x0	hresetn_rkjpeg When high, reset relative logic
2:0	RO	0x0	reserved

2.4.13 VCPCRU

2.4.13.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

2.4.13.2 Registers Summary

Name	Offset	Size	Reset Value	Description
VCPCRU_VCP_CLKSEL_CON00	0x0300	W	0x00000070	Internal clock select and division register 0
VCPCRU_VCP_GATE_CON00	0x0800	W	0x00008000	Internal clock gate and division register 0
VCPCRU_VCP_GATE_CON01	0x0804	W	0x00000000	Internal clock gate and division register 1
VCPCRU_VCP_SOFTRST_CON00	0x0A00	W	0x00000000	Internal clock reset register 0
VCPCRU_VCP_SOFTRST_CON01	0x0A04	W	0x00000000	Internal clock reset register 1

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

2.4.13.3 Detail Registers Description

VCPCRU_VCP_CLKSEL_CON00
Address: Operational Base(0x200B0000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	clk_core_aiisp_sel clk_core_aiisp clock mux. 1'b0: clk_aiisp_pll_src 1'b1: clk_vcp_pvtpll_src
14	RO	0x0	reserved
13	RW	0x0	clk_core_fec_sel clk_core_fec clock mux. 1'b0: clk_core_fec_src 1'b1: clk_vcp_pvtpll_src
12:10	RW	0x0	clk_testout_vcp_sel clk_testout_vcp clock mux. 3'b000: aclk_vcp_root 3'b001: hclk_vcp_root 3'b010: pclk_vcp_root 3'b011: clk_core_fec 3'b100: 1'b0 3'b101: clk_core_aiisp 3'b110: 1'b0 3'b111: test_clkout_vcp_pvtpll
9	RO	0x0	reserved
8:4	RW	0x07	clk_testout_vcp_div Divide clk_testout_vcp by (div_con + 1).
3	RO	0x0	reserved
2	RW	0x0	mbist_clk_pvtpll_aiisp_sel mbist_clk_pvtpll_aiisp clock mux. 1'b0: mbist_clk_aiisp 1'b1: clk_vcp_pvtpll_src
1	RW	0x0	mbist_clk_pvtpll_vcp_sel mbist_clk_pvtpll_vcp clock mux. 1'b0: mbist_clk_500m 1'b1: clk_vcp_pvtpll_src
0	RW	0x0	clk_vcp_pvtpll_src_sel clk_vcp_pvtpll_src clock mux. 1'b0: clk_deepslow 1'b1: clk_vcp_pvtpll

VCPCRU_VCP_GATE_CON00

Address: Operational Base(0x200B0000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	clk_testout_vcp_en clk_testout_vcp clock gating control. When high, disable clock
14	RO	0x0	reserved
13	RW	0x0	clk_core_aiisp_en clk_core_aiisp clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
12	RW	0x0	aclk_aiisp_en aclk_aiisp clock gating control. When high, disable clock
11	RW	0x0	hclk_aiisp_en hclk_aiisp clock gating control. When high, disable clock
10	RO	0x0	reserved
9	RW	0x0	hclk_aiisp_biu_en hclk_aiisp_biu clock gating control. When high, disable clock
8	RW	0x0	aclk_aiisp_biu_en aclk_aiisp_biu clock gating control. When high, disable clock
7	RW	0x0	pclk_vcp_pvtpll_en pclk_vcp_pvtpll clock gating control. When high, disable clock
6	RO	0x0	reserved
5	RW	0x0	pclk_vcp_grf_en pclk_vcp_grf clock gating control. When high, disable clock
4	RW	0x0	pclk_cru_vcp_en pclk_cru_vcp clock gating control. When high, disable clock
3	RW	0x0	pclk_vcp_biu_en pclk_vcp_biu clock gating control. When high, disable clock
2	RW	0x0	hclk_vcp_biu_en hclk_vcp_biu clock gating control. When high, disable clock
1	RW	0x0	aclk_vcp_biu_en aclk_vcp_biu clock gating control. When high, disable clock
0	RW	0x0	clk_ref_pvtpll_vcp_en clk_ref_pvtpll_vcp clock gating control. When high, disable clock

VCPCRU_VCP_GATE_CON01

Address: Operational Base(0x200B0000) + offset (0x0804)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x0	aclk_avsp_en aclk_avsp clock gating control. When high, disable clock
3	RW	0x0	hclk_avsp_en hclk_avsp clock gating control. When high, disable clock
2	RW	0x0	clk_core_fec_en clk_core_fec clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
1	RW	0x0	aclk_fec_en aclk_fec clock gating control. When high, disable clock
0	RW	0x0	hclk_fec_en hclk_fec clock gating control. When high, disable clock

VCPCRU_VCP_SOFTRST_CON00

Address: Operational Base(0x200B0000) + offset (0x0A00)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	resetn_core_aiisp When high, reset relative logic
12:10	RO	0x0	reserved
9	RW	0x0	hresetn_aiisp_biu When high, reset relative logic
8	RW	0x0	aresetn_aiisp_biu When high, reset relative logic
7	RW	0x0	presetn_vcp_pvtpll When high, reset relative logic
6	RO	0x0	reserved
5	RW	0x0	presetn_vcp_grf When high, reset relative logic
4	RW	0x0	presetn_cru_vcp When high, reset relative logic
3	RW	0x0	presetn_vcp_biu When high, reset relative logic
2	RW	0x0	hresetn_vcp_biu When high, reset relative logic
1	RW	0x0	aresetn_vcp_biu When high, reset relative logic
0	RW	0x0	resetn_ref_pvtpll_vcp When high, reset relative logic

VCPCRU_VCP_SOFTRST_CON01

Address: Operational Base(0x200B0000) + offset (0x0A04)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x0	aresetn_avsp When high, reset relative logic
3	RW	0x0	hresetn_avsp When high, reset relative logic
2	RW	0x0	resetn_core_fec When high, reset relative logic
1	RW	0x0	aresetn_fec When high, reset relative logic

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Bit	Attr	Reset Value	Description
0	RW	0x0	hresetn_fec When high, reset relative logic

2.4.14 SBUSCRU

2.4.14.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

2.4.14.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SBUSCRU_SBUS_CLKSEL_CON02	0x0308	W	0x00001000	Internal clock select and division register 2
SBUSCRU_SBUS_GATE_CON00	0x0800	W	0x00000000	Internal clock gate and division register 0
SBUSCRU_SBUS_GATE_CON02	0x0808	W	0x00000000	Internal clock gate and division register 2
SBUSCRU_SBUS_SOFTRST_CON00	0x0A00	W	0x00000000	Internal clock reset register 0
SBUSCRU_SBUS_SOFTRST_CON02	0x0A08	W	0x00000000	Internal clock reset register 2

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

2.4.14.3 Detail Registers Description

SBUSCRU_SBUS_CLKSEL_CON02

Address: Operational Base(0x20200000) + offset (0x0308)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x1	clk_user_otpc_s_div Divide clk_user_otpc_s by (div_con + 1).
11:0	RO	0x000	reserved

SBUSCRU_SBUS_GATE_CON00

Address: Operational Base(0x20200000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	pclk_key_reader_en pclk_key_reader clock gating control. When high, disable clock
12	RW	0x0	clk_user_otpc_s_en clk_user_otpc_s clock gating control. When high, disable clock
11	RW	0x0	clk_sbpi_otpc_s_en clk_sbpi_otpc_s clock gating control. When high, disable clock
10	RW	0x0	pclk_otpc_s_en pclk_otpc_s clock gating control. When high, disable clock

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Bit	Attr	Reset Value	Description
9	RW	0x0	hclk_kl_rkce_en hclk_kl_rkce clock gating control. When high, disable clock
8	RW	0x0	hclk_s_rkce_en hclk_s_rkce clock gating control. When high, disable clock
7	RW	0x0	tclk_wdt_s_en tclk_wdt_s clock gating control. When high, disable clock
6	RW	0x0	pclk_wdt_s_en pclk_wdt_s clock gating control. When high, disable clock
5	RW	0x0	clk_stimer1_en clk_stimer1 clock gating control. When high, disable clock
4	RW	0x0	clk_stimer0_en clk_stimer0 clock gating control. When high, disable clock
3	RW	0x0	pclk_stimer_en pclk_stimer clock gating control. When high, disable clock
2	RW	0x0	pclk_sys_sgrf_en pclk_sys_sgrf clock gating control. When high, disable clock
1	RW	0x0	pclk_cru_sbus_en pclk_cru_sbus clock gating control. When high, disable clock
0	RO	0x0	reserved

SBUSCRU_SBUS_GATE_CON02

Address: Operational Base(0x20200000) + offset (0x0808)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	hclk_rkrng_s_en hclk_rkrng_s_scru clock gating control. When high, disable clock
13	RW	0x0	clk_pka_rkce_en clk_pka_srkce clock gating control. When high, disable clock
12	RW	0x0	aclk_rkce_en aclk_srkce clock gating control. When high, disable clock
11:0	RO	0x000	reserved

SBUSCRU_SBUS_SOFTRST_CON00

Address: Operational Base(0x20200000) + offset (0x0A00)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:14	RO	0x0	reserved
13	RW	0x0	presetn_key_reader When high, reset relative logic
12	RW	0x0	resetn_user_otpc_s When high, reset relative logic
11	RW	0x0	resetn_sbpi_otpc_s When high, reset relative logic
10	RW	0x0	presetn_otpc_s When high, reset relative logic
9	RW	0x0	hresetn_kl_rkce When high, reset relative logic
8	RW	0x0	hresetn_s_rkce When high, reset relative logic
7	RW	0x0	tresetn_wdt_s When high, reset relative logic
6	RW	0x0	presetn_wdt_s When high, reset relative logic
5	RW	0x0	resetn_stimer1 When high, reset relative logic
4	RW	0x0	resetn_stimer0 When high, reset relative logic
3	RW	0x0	presetn_stimer When high, reset relative logic
2	RW	0x0	presetn_sys_sgrf When high, reset relative logic
1	RW	0x0	presetn_cru_sbus When high, reset relative logic
0	RO	0x0	reserved

SBUSCRU_SBUS_SOFTRST_CON02

Address: Operational Base(0x20200000) + offset (0x0A08)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	hresetn_rkrng_s When high, reset relative logic
13	RW	0x0	resetn_pka_rkce When high, reset relative logic
12	RW	0x0	aresetn_rkce When high, reset relative logic
11:0	RO	0x000	reserved

2.4.15 SPMUCRU

2.4.15.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

2.4.15.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SPMUCRU_SPMU_GATE_CON00	0x0800	W	0x00000000	Internal clock gate and division register 0

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Name	Offset	Size	Reset Value	Description
SPMUCRU_SPMU_SOFTRST_CON00	0x0A00	W	0x00000000	Internal clock reset register 0

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

2.4.15.3 Detail Registers Description

SPMUCRU_SPMU_GATE_CON00

Address: Operational Base(0x20210000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	pclk_pmu_sgrf_en pclk_pmu_sgrf clock gating control. When high, disable clock
0	RW	0x0	pclk_cru_spmu_en pclk_cru_spmu clock gating control. When high, disable clock

SPMUCRU_SPMU_SOFTRST_CON00

Address: Operational Base(0x20210000) + offset (0x0A00)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2	RW	0x0	presetn_pmu_sgrf_remap When high, reset relative logic
1	RW	0x0	presetn_pmu_sgrf When high, reset relative logic
0	RW	0x0	presetn_cru_spmu When high, reset relative logic

2.5 Application Notes

2.5.1 Fractional PLL Usage

2.5.1.1 PLL Frequency Configuration

FBDIV, POSTDIV1, BYPASS can be configured by programming CRU_xPLL_CON0.
DSMPD, REFDIV, POSTDIV2 can be configured by programming CRU_xPLL_CON1.
FRAC can be configured by programming CRU_xPLL_CON2.

If DSMPD = 1 (DSM is disabled, “integer mode”)
FOUTVCO = (FREF / REFDIV) * FBDIV
FOUTPOSTDIV = FOUTVCO / (POSTDIV1*POSTDIV2)
When FREF is 24MHz, and if 700MHz FOUTPOSTDIV is needed. The configuration can be:

DSMPD = 1
REFDIV = 6
FBDIV = 175
POSTDIV1=1
POSTDIV2=1

And then
FOUTVCO = (FREF / REFDIV) * FBDIV = 24/6*175 = 700
FOUTPOSTDIV = FOUTVCO / (POSTDIV1*POSTDIV2) = 700/1/1 = 700

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If DSMPD = 0 (DSM is enabled, "fractional mode")
FOUTVCO = (FREF / REFDIV) * (FBDIV + FRAC / (2^24))
FOUTPOSTDIV = FOUTVCO / (POSTDIV1*POSTDIV2)
When FREF is 24MHz, and if 491.52MHz FOUTPOSTDIV is needed. The configuration can be:

DSMPD = 0
REFDIV = 1
FBDIV = 40
FRAC = 24'hf5c28f
POSTDIV1=2
POSTDIV2=1

And then
FOUTVCO = (FREF / REFDIV) * (FBDIV + FRAC / (2^24)) = 983.04
FOUTPOSTDIV = FOUTVCO / (POSTDIV1*POSTDIV2) = 983.04 / (2*1) =491.52
POSTDIV1=0, POSTDIV2=0 are unused. We should make sure that POSTDIV1>=POSTDIV2.

2.5.1.2 PLL Setting Consideration

- If the POSTDIV value is changed during operation, a short pulse (glitch) may occur on FOUTPOSTDIV. The minimum width of the short pulse will be equal to twice the period of the VCO. Therefore, if the circuitry clocked by the PLL is sensitive to short pulses, the new divide value should be re-timed so that it is synchronous with the rising edge of the output clock (FOUTPOSTDIV). Glitches cannot occur on any of the other outputs.
- For lowest power operation, the minimum VCO and FREF frequencies should be used. For minimum jitter operation, the highest VCO and FREF frequencies should be used. The normal operating range for the VCO is described above in.
- The supply rejection will be worse at the low end of the VCO range so care should be taken to keep the supply clean for low power applications.
- The feedback divider is not capable of dividing by all possible settings due to the use of a power-saving architecture. The following settings are valid for FBDIV:
  - DSMPD=1 (Integer Mode)
  - DSMPD=0 (Fractional Mode)
- The PD input places the PLL into the lowest power mode. In this case, all analog circuits are turned off and FREF will be "ignored". The FOUTPOSTDIV and FOUTVCO pins are forced to logic low (0V).
- The BYPASS pin controls FREF to be passed to the FOUTPOSTDIV when active high. However, the PLL continues to run as it normally would if bypass were low. This is a useful feature for PLL testing since the clock path can be verified without the PLL being required to work. Also, the effect that the PLL induced supply noise has on the output buffering can be evaluated. It is not recommended to switch between BYPASS mode and normal mode for regular chip operation since this may result in a glitch. Also, FOUTPOSTDIVPD should be set low if the PLL is to be used in BYPASS mode.

2.5.1.3 PLL Frequency Change and Lock Check

PLL lock state can be checked in CRU_xPLL_CON1[10] register. The lock state is high when both original hardware PLL lock and PLL counter lock are high.
The max delay time is 500*REFDIV/FREF.
PLL locking consists of three phases.

- Phase 1 is control voltage slewing. During this phase one of the clocks (reference or divide) is much faster than the other, and the PLL frequency adjusts almost continuously. When locking from power down, the divide clock is initially very slow and steadily increases frequency. It will take slightly longer for faster VCO settings when locking from power down, since the PLL must slew further.
- Phase 2 is small signal phase acquisition. During this phase, the internal up/down signals alternate semi-chaotically as the phase slowly adjusts until the two signals are aligned. The duration of this phase depends on the loop bandwidth and is faster with higher bandwidth. Bandwidth can be estimated as FREF / REFDIV / 20 for integer mode and FREF /REFDIV / 40 for fractional mode. The duration of small signal locking is about 1/Bandwidth.

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- Phase 3 is the digital cycle count. After the last cycle slip is detected, an internal counter waits 128 FREF / REFDIV cycles before the lock signal goes high. This is frequently the dominant factor in lock time – especially for slower reference clock signals or large reference divide settings. This time can be calculated as 128*REFDIV/FREF.

2.5.2 Integer PLL Usage

2.5.2.1 PLL Frequency Configuration

FBDIV, POSTDIV1, BYPASS can be configured by programming CRU_xPLL_CON0.
DSMPD, REFDIV, POSTDIV2 can be configured by programming CRU_xPLL_CON1.
DSMPD should always be set to 1 (CLKSSCG is power down), and REFDIV can only be 1 or 2.
FOUTVCO = (FREF / REFDIV) * FBDIV
FOUTPOSTDIV = FOUTVCO / (POSTDIV1*POSTDIV2)
POSTDIV1=0, POSTDIV2=0 are unused. We should make sure that POSTDIV1>=POSTDIV2.

2.5.2.2 PLL Frequency Change and Lock Check

The PLL programming supports changed on-the-fly and the PLL will simply slew to the new frequency.
PLL lock state can be checked in CRU_xPLL_CON1[10] register. The lock state is high when both original hardware PLL lock and PLL counter lock are high.
The max delay time is 1500*REFDIV/FREF.

2.5.3 Divider Usage

2.5.3.1 Fractional Divider Usage

To get specific frequency, clocks of 32k source UART and SAI can be generated by fractional divider. Generally, you should set that denominator 20 times larger than numerator to generate precise clock frequency. So the fractional divider applies only to generate low frequency clock. For implementation issue, the input source clocks of fractional divider should limit to less than 1200MHz.

2.5.3.2 Divfree50 Divider Usage

Some modules like EMMC, SDMMC, FSPI need clock of 50% duty cycle, divfree_duty50 can generate clock of 50% duty cycle even in odd value divisor.

2.5.4 Global Software Reset

Two global software resets are designed, you can program CRU_GLB_SRST_FST_VALUE[15:0] as 0xfdb9 to assert the first global software reset glb_srstn_1 and program CRU_GLB_SRST_SND_VALUE[15:0] as 0xeca8 to assert the second global software reset glb_srstn_2. These two software resets are self-de-asserted by hardware. Resetting hold timing of global software reset (glb_srstn_1, glb_srstn_2, wdt_rstn, tsadc_rstn) can be programed up to 1ms.
glb_srstn_1 resets almost all logic except some registers just supporting hardware reset.
glb_srstn_2 resets almost all logic except GRFs, IOCs, GPIOs.
Reset for IP in PD_PMU can be hold if its reset_hold_enable in PMUGRF_SOC_CON4/5/6/7 is high even if glb_srstn_1 or glb_srstn_2 active.

2.5.5 SSCG Usage

There are some scenes where SSCG should be enabled. One scene is in communication where a fixed frequency is required. Another scene is a system requiring a clock with low long-term jitter. When SSCG is used, the PLL should be configured to fractional mode firstly for spread spectrum capability.

2.5.5.1 SSCG Use Internal Point Table

User can use SSCG with internal point table as following steps:

- Setting ssmod_spread (CRU_xPLL_CON3[12:8]) and ssmod_downspread (CRU_xPLL_CON3[3])
  The modulation amplitude is controlled by the value of ssmod_spread. A ssmod_spread value of5'd0 turns off the modulation. A ssmod_spread value of 5'd31 (5'b11111) gives maximum modulation while a value of 5'd1gives minimum modulation.
  The modulation amplitude can be calculated from the value of modulation by:
  Modulation Amplitude = ±5'd (ssmod_spread) * 0.1%
  The modulation direction is determined by the ssmod_downspread bit.

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- ssmod_downspread=1'b1, down spread mode is used. If ssmod_spread = 5'd29, the maximum PLL frequency is the nominally programmed value F_{NOM}, and the minimum value is given by F_{NOM} * (1–0.029).
- ssmod_downspread=1'b0, center spread mode is used. If ssmod_spread = 5'd29, the maximum PLL frequency would be determined by F_{NOM}*(1+0.029) and the minimum frequency by F_{NOM} * (1–0.029).
  Setting the style of modulation (center versus down) and the modulation amplitude depend on the amount of EMI reduction desired and the timing margin for circuits running on the spread clock domain. The larger the spread value, the greater the reduction in EMI amplitude. However, the larger the spread value, the more timing margin needed for correct circuit operation.
- Setting ssmod_sel_ext_wave (CRU_xPLL_CON4[0]) = 1'b0
  When use internal point table, the frequency will change as following during 128 point:
- Change from minimum value to maximum value uniformly within 64 points
- Change from maximum value to minimum value uniformly within 64 points
  Spread spectrum modulator is implemented by repeating as above.
- Setting ssmod_divval (CRU_xPLL_CON3[7:4])
  The frequency of modulation FMOD= FREF / (Point number * REFDIV * ssmod_divval). The FMOD is typically set above 32KHz and below the maximum frequency for modulation fidelity, which isdetermined by the PLL bandwidth. The maximum modulation frequency is conservatively set at FREF/(200*REFDIV).
  When FREF=24MHz and REFDIV= 1, the value of ssmod_divval can be 5, then the FMOD is 37.5KHz.
- Setting ssmod_bp (CRU_xPLL_CON3[0]) = 1'b0
- Setting ssmod_disable_sscg (CRU_xPLL_CON3[1]) = 1'b0
- Setting ssmod_reset (CRU_xPLL_CON3[2]) = 1'b0

2.5.5.2 SSCG Use External Point Table

In addition to the internal shape table, an external shape table can be used.
This enables customization tables in both shape and the number of sample points for the envelope wave form up to 128 data points. The external table of 128 data points can be configured from CRU_SSCGTBL_CON0~CRU_SSCGTBL_CON31.
User can use SSMOD with external point table as following steps:

- Setting ssmod_spread (CRU_xPLL_CON3[12:8]) and ssmod_downspread (CRU_xPLL_CON3[3]), same with internal point table usage.
- Setting ssmod_sel_ext_wave (CRU_xPLL_CON4[0]) = 1'b1
- Setting ssmod_ext_maxaddr (CRU_xPLL_CON4[15:8]) and table0~table127(CRU_SSCGTBL_CON0~CRU_SSCGTBL_CON31)
  ssmod_ext_maxaddr is the maximum table address. For example, if the number of points describing the envelope shape is 128, the ssmod_ext_maxaddr should be configured to 127. The table address circulates over the range 0 to 127.
  The table0~table127 must be 8 bit numbers in the form of sign and magnitude.
- 1.00 is represented by 8'b01111111, it is corresponded to maximum frequency.
- -1.00 is represented in the table by8'b11111111, it is corresponded to minimum frequency.
- 0.5 is represented in the table by 8'b00111111.
- -0.5 is represented in the table by 8'b10111111.
  The frequency will change base table0~table127 within 128 points, and then repeat.
- Setting ssmod_divval (CRU_xPLL_CON3[7:4])
  The frequency of modulation FMOD= FREF / (Point number * REFDIV * ssmod_divval). The point number equals to ssmod_ext_maxaddr+1.
- Setting ssmod_bp (CRU_xPLL_CON3[0]) = 1'b0
- Setting ssmod_disable_sscg (CRU_xPLL_CON3[1]) = 1'b0
- Setting ssmod_reset (CRU_xPLL_CON3[2]) = 1'b0.
  Attention: xPLL means AUPLL/CPLL/DPLL/GPLL.

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Chapter 3 CPU (Cortex-A53)

3.1 Overview

The RV1126B has a quad-core Cortex-A53 cluster with 512K L2 memory. Cortex-A53 processor, which is a mid-range, low-power processor that implements the ARMv8-A architecture.
The Cortex-A53 processor includes following features:

- Full implementation of the ARMv8-A architecture instruction set
- Support for both AArch32 and AArch64 Execution status.
- Support for all exception levels, EL0, EL1, EL2, and EL3, in each execution states.
- Support A32 instruction set, previously called the ARM instruction set.
- Support T32 instruction set, previously called the Thumb instruction set.
- Support A64 instruction set.
- In-order pipeline with symmetric dual-issue of most instructions.
- Harvard Level 1(L1) memory system with a Memory Management Unit (MMU).
- Level 2(L2) memory system providing cluster memory coherency, with L2 cache.
- Support advanced SIMD and Floating-point Extension for integer and floating-point vector operations.
- Support ARMv8 Cryptography Extensions.
- Support AMBA 4 ACE bus architecture.

The configuration details of little cluster and big cluster are shown in following tables

Table 3-1 CPU Configuration

Number of CPU	4
L1 I cache size	32K
L1 D cache size	32K
L2 cache size	512K
L2 data RAM output latency	2 cycles
L2 data RAM input latency	2 cycles
CPU cache protection	No
SCU L2 cache protection	No
BUS master interface	ACE
NEON and floating point support	Yes
Cryptography extension	Yes

3.2 Block Diagram

The Cortex-A53 sub system is shown in Fig. 3-1 Block Diagram.
The Cortex-A53 is connected with system counter, which can run under a constant frequency clock, for PPI interrupt generation.

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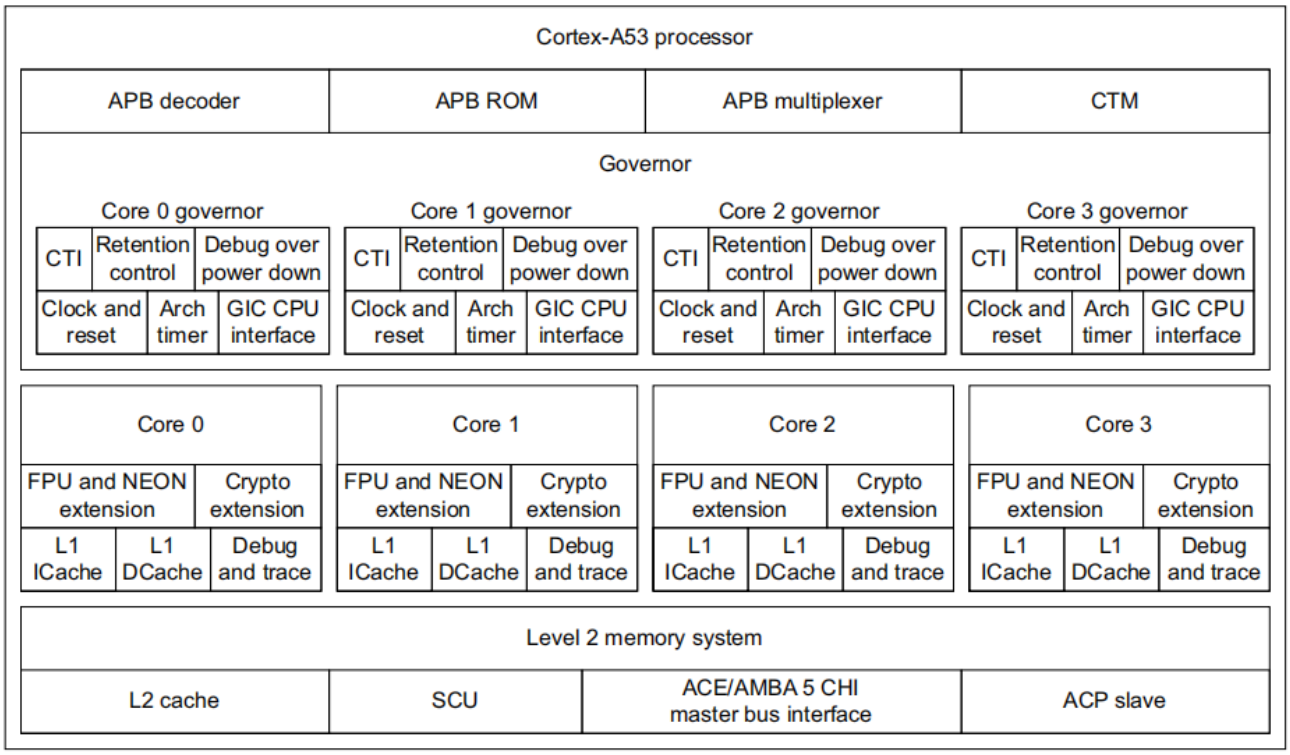

Fig. 3-1 Block Diagram

3.3 Function Description

Please refer to the document cortex_a53_r0p4_trm.pdf for the detail function description.

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Chapter 4 General Register Files (GRF)

4.1 Overview

The general register file will be used to do static setting by software, which is composed of many registers for system control. The GRF is located at several addresses.

4.2 Function Description

The function of general register file is：

- Common system control
- Record the system state

Table 4-1GRF Adress Mapping Table

No	Name	Address Base
1	SYS_GRF	0X20100000
2	PERI_GRF	0X20110000
3	USB3 PHY_GRF	0X20118000
4	CPU_GRF	0X20120000
5	PMU_GRF	0X20130000
6	DDR_GRF	0X20140000
7	VI_GRF	0X20150000
8	VEPU_GRF	0X20160000
9	NPU_GRF	0X20170000
10	VDO_GRF	0x20180000
11	VCP_GRF	0x20190000

4.3 SYS GRF Register Description

4.3.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

4.3.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SYS_GRF_MEM_GRF_SPRA	0x0000	W	0x00000021	PERI single memory configuration register
SYS_GRF_MEM_GRF_DPRA	0x0004	W	0x00000000	PERI dual-port memory config register
SYS_GRF_MEM_GRF_ROM	0x0008	W	0x00000155	Peripheral system memory control register
SYS_GRF_BUS_GRF_MISC	0x000C	W	0x00000000	Peripheral system control register 2
SYS_GRF_MEM_CON_GATE	0x0010	W	0x00000000	Peripheral system memory control register
SYS_GRF_BUS_GRF_HPROT_STALL	0x0014	W	0x00000000	Peripheral BufferAble HProt2 Signal Register
SYS_GRF_HPMCU_CACHE_MISC	0x0018	W	0x00000000	Hpmcu cache misc register
SYS_GRF_HPMCU_CACHE_ADDR_START	0x001C	W	0x00000000	Cache addr start register
SYS_GRF_HPMCU_CACHE_ADDR_END	0x0020	W	0x00000000	Cache addr end register
SYS_GRF_HPMCU_CODE_ADDR_START	0x0024	W	0x00000000	Hpmcu code addr start register

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Name	Offset	Size	Reset Value	Description
SYS_GRF_HPMCU_SRAM_ADDR_START	0x0028	W	0x00000000	Hpmcu sram addr start register
SYS_GRF_HPMCU_EXSRAM_ADDR_START	0x002C	W	0x00000000	Hpmcu exsram addr start register
SYS_GRF_BIU_CON0	0x0030	W	0x00000000	BIU control register 0
SYS_GRF_BIU_CON1	0x0034	W	0x00000000	BIU control register 0
SYS_GRF_UART_GRF_RTS_CTS	0x0038	W	0x00000000	Peripheral system control register 0
SYS_GRF_UART_GRF_DMA_BYPASS	0x003C	W	0x00000000	Peripheral system control register 0
SYS_GRF_AUDIO_CON0	0x0040	W	0x00000000	Peripheral audio control register 0
SYS_GRF_AUDIO_CON2	0x0048	W	0x00000000	Peripheral audio control register 1
SYS_GRF_OTP_CON	0x004C	W	0x00000000	OTP controller lock configuration register
SYS_GRF_TSADC_GRF_CON0	0x0050	W	0x00000000	Tsadc register
SYS_GRF_TSADC_GRF_CON1	0x0054	W	0x00000000	Tsadc register
SYS_GRF_TSADC_GRF_CON2	0x0058	W	0x00000000	Tsadc register
SYS_GRF_TSADC_GRF_CON3	0x005C	W	0x00000000	Tsadc register
SYS_GRF_TSADC_GRF_CON4	0x0060	W	0x00000000	Tsadc register
SYS_GRF_TSADC_GRF_CON5	0x0064	W	0x00000000	Tsadc register
SYS_GRF_TSADC_GRF_CON6	0x0068	W	0x00000000	Tsadc register
SYS_GRF_BIU_STATUS0	0x0100	W	0x00000000	BIU status register 0
SYS_GRF_BIU_STATUS1	0x0104	W	0x00000000	BIU status register 0
SYS_GRF_BIU_STATUS2	0x0108	W	0x00000000	BIU status register 0
SYS_GRF_HPMCU_CACHE_STATUS	0x010C	W	0x00000000	Hpmcu cache status register
SYS_GRF_TSADC_GRF_STATUS0	0x0110	W	0x00000000	
SYS_GRF_TSADC_GRF_STATUS1	0x0114	W	0x00000000	BIU status register 0
SYS_GRF_SYS_STATUS	0x0118	W	0x00000000	Peripheral system status register
SYS_GRF_CHIP_ID	0x0800	W	0x1126000B	Chip Id register
SYS_GRF_CHIP_VERSION	0x0804	W	0x00000001	Chip Version register

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

4.3.3 Detail Registers Description

SYS_GRF_MEM_GRF_SPRA

Address: Operational Base(0x20100000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bit, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:10	RW	0x0	wtsel_hvt_mux4 Configuration for wtsel mux4 type for memory for PERI.
9:8	RW	0x0	rtsel_hvt_mux4 Configuration for rtsel mux4 type for memory for PERI.
7:6	RW	0x0	wtsel_hvt_mux1ormux2 Configuration for wtsel mux1ormux2 mem type for memory for PERI.

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Bit	Attr	Reset Value	Description
5:4	RW	0x2	rtsel_hvt_mux1ormux2 Configuration for wtsel mux1ormux2 mem type for memory for PERI.
3:2	RW	0x0	wtsel_svt Configuration for rtsel mux1ormux2 mem type for memory for PERI. We only use the hvt.
1:0	RW	0x1	rtsel_svt Configuration for rtsel mux1ormux2 mem type for memory for PERI. We only use the hvt.

SYS_GRF_MEM_GRF_DPRA

Address: Operational Base(0x20100000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5:4	RW	0x0	rtsel PERI memory configuration. 2'b00: Recommended setting with the optimized read margin. 2'b01: Relaxed read margin setting, used for debugging purpose. 2'b10: More relaxed read margin setting, used for debugging purpose. 2'b11: Most relaxed read margin setting, used for debugging purpose.
3:2	RW	0x0	wtsel PERI memory configuration. 2'b00: Recommended setting with the optimized write margin. 2'b01: Relaxed write margin setting, used for debugging purpose. 2'b10: More relaxed write margin setting, used for debugging purpose. 2'b11: Most relaxed write margin setting, used for debugging purpose.
1:0	RW	0x0	ptsel PERI memory configuration. Setting for internal clock skew of port A/B with the optimized design margin and timming. 2'b00: Recommended value. 2'b01: Relaxed setting for internal clock skew of port A/B used for debugging purpose. 2'b10: More Relaxed setting for internal clock skew of port A/B used for debugging purpose. 2'b11: Most Relaxed setting for internal clock skew of port A/B used for debugging purpose.

SYS_GRF_MEM_GRF_ROM

Address: Operational Base(0x20100000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0155	peri_mem_cfg_rom Configuration for PERI ROM memory timing . [1:0]: PTSEL [3:2]: RTSEL [5:4]: TRB

SYS_GRF_BUS_GRF_MISC

Address: Operational Base(0x20100000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	grf_con_usbphy_hostport_wakeup_irq_en grf_con_usbphy_hostport_wakeup_irq enable controll. 1'b0: Disable. irq_host0_linestate and irq_host0_disconnect source is disable for wakeup_usbdev. 1'b1: Enable. irq_host0_linestate and irq_host0_disconnect source is enable for wakeup_usbdev.
14	RW	0x0	grf_con_usbphy_lfps_beacon_irq_en grf_con_usbphy_lfps_beacon_irq enable controll. 1'b0: Disable. irq_lfps_beacon source is disable for wakeup_usbdev. 1'b1: Enable. irq_lfps_beacon source is enable for wakeup_usbdev.
13:12	RW	0x0	grf_con_wdt_pmu_glb_reset_en No-secure WDT global reset enable. 1'b0: Disable. No-secure WDT reset output cannot reset SoC system. 1'b1: Enable. No-secure WDT reset output will reset SoC system.
11	RW	0x0	grf_con_wdt_s_pause_speedup speedup enable 1: enable 0:disable
10	RW	0x0	grf_con_wdt_s_pause pause enable. 1:enable 0:disable
9	RW	0x0	grf_con_hpmcu_wdt_s_speedup speedup enable 1: enable 0:disable
8	RW	0x0	grf_con_hpmcu_wdt_s_pause pause enable. 1:enable 0:disable
7:0	RO	0x00	reserved

SYS_GRF_MEM_CON_GATE

Address: Operational Base(0x20100000) + offset (0x0010)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	grf_con_mem_gat_en_rkce memory gate control for this ip. 1'b0: Disable 1'b1: Enable
2	RW	0x0	grf_con_ck_gating_audio_adc memory gate control for this ip. 1'b0: Disable 1'b1: Enable
1	RW	0x0	grf_con_ck_gating_asrc memory gate control for this ip. 1'b0: Disable 1'b1: Enable
0	RW	0x0	grf_con_mem_gat_en_rkcache memory gate control for this ip. 1'b0: Disable 1'b1: Enable

SYS_GRF_BUS_GRF_HPROT_STALL

Address: Operational Base(0x20100000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits. each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	grf_con_ddr2aiisp_pwr_stall 1'b0: Access to the ddr2aiisp path idle power domain will be response error. 1'b1: Access to theddr2aiisp path idle power domain will be stalled.
14:1	RO	0x0000	reserved
0	RW	0x0	grf_con_bufferable_hprot2_hpmcu The ahb mater is hpmcu. 1'b1: set 1 for ahb master hprot bit2 field , this means enable the ahb master access is bufferable. 1'b0: set 0 for ahb master hprot bit2 field , this means enable the ahb master access is bufferable.

SYS_GRF_HPMCU_CACHE_MISC

Address: Operational Base(0x20100000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	cache_maintain_exram_en cache_maintain_exram_en
5	RW	0x0	cache_maintain_sram_en cache_maintain_sram_en

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Bit	Attr	Reset Value	Description
4	RW	0x0	cache_maintain_code_en cache_maintain_code_en
3	RW	0x0	scr1_soft_irq mcu software irq
2:1	RW	0x0	cache_slv_memattr cache slave memory attribute
0	RW	0x0	cache_flush_req cache flush request

SYS_GRF_HPMCU_CACHE_ADDR_START
Address: Operational Base(0x20100000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	peri_addr_start Cache periphral high 20-bit base address, the address should be put in low 20-bit when configure this reg

SYS_GRF_HPMCU_CACHE_ADDR_END
Address: Operational Base(0x20100000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	periphral_addr_end Cache periphral high 20-bit end address, the address should be put in low 20-bit when configure this reg

SYS_GRF_HPMCU_CODE_ADDR_START
Address: Operational Base(0x20100000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	hpmcu_code_addr_start Hpmcu code region high 20-bit base address, the address should be put in low 20-bit when configure this reg

SYS_GRF_HPMCU_SRAM_ADDR_START
Address: Operational Base(0x20100000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	hpmcu_sram_addr_start Hpmcu sram region high 20-bit end address, the address should be put in low 20-bit when configure this reg

SYS_GRF_HPMCU_EXSRAM_ADDR_START
Address: Operational Base(0x20100000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	hpmcu_exsram_addr_start Hpmcu exsram region high 20-bit end address, the address should be put in low 20-bit when configure this reg

SYS_GRF_BIU_CON0
Address: Operational Base(0x20100000) + offset (0x0030)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:0	RW	0x0000	biu_stall_ctrl0 biu_stall_ctrl The value description: 1'b0: Access to the idle power domain will be response error. 1'b1: Access to the idle power domain will be stalled. The bit field description: Bit0 : aiisp_fwd_vcp ; Bit1 : bus_fwd_cru ; Bit2 : bus_fwd_ddr ; Bit3 : bus_fwd_cfgddr ; Bit4 : bus_fwd_vepu ; Bit5 : bus_fwd_vi ; Bit6 : bus_fwd_npu ; Bit7 : bus_fwd_vdo ; Bit8 : bus_fwd_vcp ; Bit9 : bus_fwd_ddr ; Bit10 : cfgddr_fwd_ddrfw ; Bit11 : cpu_fwd_bus ; Bit12 : cpu_fwd_ddr ; Bit13 : npu_fwd_ddr ; Bit14 : peri_fwd_vcp ; Bit15 : pmu1_fwd_pmu ;

SYS_GRF_BIU_CON1

Address: Operational Base(0x20100000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved

Bit	Attr	Reset Value	Description
14:0	RW	0x0000	biu_stall_ctrl1 biu_stall_ctrl The value description: 1'b0: Access to the idle power domain will be response error. 1'b1: Access to the idle power domain will be stalled. The bit field description: Bit0 : pmu_fwd_vcp ; Bit1 : pmu_fwd_pmu1 ; Bit2 : subddr_fwd_cpu ; Bit3 : subddr_fwd_npu ; Bit4 : subddr_fwd_poe ; Bit5 : subddr_fwd_vi ; Bit6 : vcp_fwd_aiisp ; Bit7 : vcp_fwd_ddr ; Bit8 : vcp_fwd_peri ; Bit9 : vcp_fwd_pmu ; Bit10 : vdo_fwd_bus ; Bit11 : vepu_fwd_ddr ; Bit12 : vepu_fwd_npu ; Bit13 : vi_fwd_bus ; Bit14 : vi_fwd_npu ; Bit15 : ddr_fwd_dma2ddr ;

SYS_GRF_UART_GRF_RTS_CTS

Address: Operational Base(0x20100000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	uart7_cts_inv Polarity selection for uart_cts. 1'b0: Low active 1'b1: High active
14	RW	0x0	uart6_cts_inv Polarity selection for uart_cts. 1'b0: Low active 1'b1: High active
13	RW	0x0	uart5_cts_inv Polarity selection for uart_cts. 1'b0: Low active 1'b1: High active
12	RW	0x0	uart4_cts_inv Polarity selection for uart_cts. 1'b0: Low active 1'b1: High active
11	RW	0x0	uart3_cts_inv Polarity selection for uart_cts. 1'b0: Low active 1'b1: High active
10	RW	0x0	uart2_cts_inv Polarity selection for uart_cts. 1'b0: Low active 1'b1: High active

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Bit	Attr	Reset Value	Description
9	RW	0x0	uart1_cts_inv Polarity selection for uart_cts. 1'b0: Low active 1'b1: High active
8	RO	0x0	reserved
7	RW	0x0	uart7_rts_inv Polarity selection for uart_rts. 1'b0: Low active 1'b1: High active
6	RW	0x0	uart6_rts_inv Polarity selection for uart_rts. 1'b0: Low active 1'b1: High active
5	RW	0x0	uart5_rts_inv Polarity selection for uart_rts. 1'b0: Low active 1'b1: High active
4	RW	0x0	uart4_rts_inv Polarity selection for uart_rts. 1'b0: Low active 1'b1: High active
3	RW	0x0	uart3_rts_inv Polarity selection for uart_rts. 1'b0: Low active 1'b1: High active
2	RW	0x0	uart2_rts_inv Polarity selection for uart_rts. 1'b0: Low active 1'b1: High active
1	RW	0x0	uart1_rts_inv Polarity selection for uart1_rts. 1'b0: Low active 1'b1: High active
0	RO	0x0	reserved

SYS_GRF_UART_GRF_DMA_BYPASS

Address: Operational Base(0x20100000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	uart7_dma_rx_single_bypass uart single transfer for dma 1'b0: Enable 1'b1: Disable
6	RW	0x0	uart6_dma_rx_single_bypass uart single transfer for dma 1'b0: Enable 1'b1: Disable
5	RW	0x0	uart5_dma_rx_single_bypass uart single transfer for dma 1'b0: Enable 1'b1: Disable

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Bit	Attr	Reset Value	Description
4	RW	0x0	uart4_dma_rx_single_bypass uart single transfer for dma 1'b0: Enable 1'b1: Disable
3	RW	0x0	uart3_dma_rx_single_bypass uart single transfer for dma 1'b0: Enable 1'b1: Disable
2	RW	0x0	uart2_dma_rx_single_bypass uart single transfer for dma 1'b0: Enable 1'b1: Disable
1	RW	0x0	uart1_dma_rx_single_bypass uart single transfer for dma 1'b0: Enable 1'b1: Disable
0	RO	0x0	reserved

SYS_GRF_AUDIO_CON0

Address: Operational Base(0x20100000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	grf_con_dsm_en It is dsm ip for sai2 or not function. 1'b1: select dsm for sai2, enable sai2_sdo to dsm. 1'b0: not select it, disable sai2_sdo to dsm. Tips: The older name is grf_con_dsm_sel. When enable or disable the bit, it does not affect the path from sai2 to io.
14:12	RO	0x0	reserved
11	RW	0x0	grf_con_sai2_sdi1_sel It is audio_adc enable function. 1'b1: from ADC1, select audio adc . 1'b0: from IO , not select it. Tips: The older name is grf_con_audio_adc_en.
10:8	RO	0x0	reserved
7	RW	0x0	grf_con_sai2_sdi0_sel It is sai2 ip from pmu or Top io function. 1'b1: from ADC0(LP) ,select pmu for sai2. 1'b0: from IO, select main for sai2. Tips: The older name is grf_con_sai2_pmu_en.
6	RO	0x0	reserved
5:4	RW	0x0	grf_con_sai2_series_sel The select control bits to sai2 ip from sai0 or sai1 2'b00: sel from sai0. 2'b01: sel from sai1. others: tie 0.
3:2	RW	0x0	grf_con_sai1_series_sel The select control bits to sai1 ip from sai0 or sai2 2'b00: sel from sai0. 2'b10: sel from sai2. others: tie 0.

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	grf_con_sai0_series_sel The select control bits to sai0 ip from sai1 or sai2 2'b01: sel from sai1. 2'b10: sel from sai2. others: tie 0.

SYS_GRF_AUDIO_CON2

Address: Operational Base(0x20100000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2	RW	0x0	grf_sai2_mclk_ioe_ 1'b0: select sai mclk out. 1'b1: mclk in.
1	RW	0x0	grf_sai1_mclk_ioe_ 1'b0: select sai mclk out. 1'b1: mclk in.
0	RW	0x0	grf_sai0_mclk_ioe_ 1'b0: select sai mclk out. 1'b1: mclk in.

SYS_GRF_OTP_CON

Address: Operational Base(0x20100000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bit, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2	RW	0x0	otp_pmc_cke otp_pmc_clk enable 1'b1: Enable 1'b0: Disable
1	RW	0x0	otpc_s_lock GRF control OTP secure controller lock. This is controlled by VOSGRF_OTPC_CON[0]. 1'b1: Lock 1'b0: Not lock
0	RW	0x0	otpc_ns_lock GRF control OTP none secure controller lock. This is controlled by VOSGRF_OTPC_CON[0]. 1'b1: Lock 1'b0: Not lock

SYS_GRF_TSADC_GRF_CON0

Address: Operational Base(0x20100000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bit, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15	RW	0x0	grf_con_tsadc_ctrl_software rk tsadc controll by software 1'b1: by software. 1'b0: by hardware.
14:13	RO	0x0	reserved
12	RW	0x0	grf_con_tsadc_rstn rk tsadc sofware resetn 1'b1: release reset. 1'b0: keep reset.
11:7	RO	0x00	reserved
6:4	RW	0x0	grf_con_sample_mode rk tsadc sample mode Bit4: 1 means only enable the current ch. 0 disable. Bit5: 1 means conitnue sample mode , 0 disable Bit6: 1 only ennable the ch when cal, 0 disable. Bit7: Reserved
3	RW	0x0	grf_con_sample_en rk tsadc sample enable When this Register Bit 15 is 1 . The value is from Bit3 1'b1: sample enable. 1'b0: disable.
2:0	RW	0x0	grf_con_tclk_chsel rk tsadc temperature detect channel select. When this Register Bit 15 is 1 . The value is from Bit2:0 Store the select channel value for temperature detect, active when bit15 is 1.

SYS_GRF_TSADC_GRF_CON1

Address: Operational Base(0x20100000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bit, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	grf_con_tclk_chsel rk tsadc register con 1 Bit14-12:debug mux select. BIt 8: 1'b1 means unlock. 1'b0: lock. Bit7-0: store the unlock value.

SYS_GRF_TSADC_GRF_CON2

Address: Operational Base(0x20100000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bit, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	grf_tsadc_otp_threshold. Bit15:0 Store the otp threshold. otp is the over temperature protect state.

SYS_GRF_TSADC_GRF_CON3

Address: Operational Base(0x20100000) + offset (0x005C)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bit, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	grf_tsadc_ota_threshold. Bit15:0 Store the ota threshold. otp is the over temperature alarm state.

SYS_GRF_TSADC_GRF_CON4
Address: Operational Base(0x20100000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bit, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	grf_tsadc_offset Bit15:0 Store the temperatore offset value for rk tsasc .

SYS_GRF_TSADC_GRF_CON5
Address: Operational Base(0x20100000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bit, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	grf_tsadc_otp_coefficient Bit15:0 Store the rk tsadc temperature coefficient value.

SYS_GRF_TSADC_GRF_CON6
Address: Operational Base(0x20100000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bit, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RW	0x00	grf_tsadc_tclk_chen Store the Soc channel enable bits. Every channel every bit.
7:6	RO	0x0	reserved
5:0	RW	0x00	grf_tsadc_tosc_ibj_adj Bit6:0 :Store the bias current for rk tsadc phy.

SYS_GRF_BIU_STATUS0
Address: Operational Base(0x20100000) + offset (0x0100)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	nopendingtrans1 No pending transfer status. The value description: 1'b0: Inactive 1'b1: Active The bit field description: Bit 0: aad_m_I_mainNoPendingTrans ; Bit 1: afe_m_I_mainNoPendingTrans ; Bit 2: aiisp_m_I_mainNoPendingTrans ; Bit 3: atdd_m_I_mainNoPendingTrans ; Bit 4: avsp_ro_m_I_mainNoPendingTrans ; Bit 5: avsp_wo_m_I_mainNoPendingTrans ; Bit 6: cpu_m_I_mainNoPendingTrans ; Bit 7: dcf_m_I_mainNoPendingTrans ; Bit 8: decom_m_I_mainNoPendingTrans ; Bit 9: dft2apb_m_I_mainNoPendingTrans ; Bit10: dma2ddr_m_I_mainNoPendingTrans ; Bit11: emmc_m_I_mainNoPendingTrans ; Bit12: fec_ro_m_I_mainNoPendingTrans ; Bit13: fec_wo_m_I_mainNoPendingTrans ; Bit14: fspi0_m_I_mainNoPendingTrans ; Bit15: fspi1_m_I_mainNoPendingTrans ; Bit16: gmac_m_I_mainNoPendingTrans ; Bit17: isp_m_I_mainNoPendingTrans ; Bit18: lpdma_m_I_mainNoPendingTrans ; Bit19: lpmcu_m_I_mainNoPendingTrans ; Bit20: mcu_m_I_mainNoPendingTrans ; Bit21: npu_m_I_mainNoPendingTrans ; Bit22: ooc_m_I_mainNoPendingTrans ; Bit23: rga_m_I_mainNoPendingTrans ; Bit24: rkcan0_m_I_mainNoPendingTrans ; Bit25: rkcan1_m_I_mainNoPendingTrans ; Bit26: rkce_m_I_mainNoPendingTrans ; Bit27: rkdma_m_I_mainNoPendingTrans ; Bit28: rkjpeg_m_I_mainNoPendingTrans ; Bit29: rkvdec_m_I_mainNoPendingTrans ; Bit30: rkvenc_m_I_mainNoPendingTrans ; Bit31: saradc0_apb_m_I_mainNoPendingTrans ;

SYS_GRF_BIU_STATUS1
Address: Operational Base(0x20100000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	nopendingtrans2 No pending transfer status. The value description: 1'b0: Inactive 1'b1: Active The bit field description: Bit 0: saradc1_apb_m_I_mainNoPendingTrans ; Bit 1: saradc2_apb_m_I_mainNoPendingTrans ; Bit 2: sdmmc0_m_I_mainNoPendingTrans ; Bit 3: sdmmc1_m_I_mainNoPendingTrans ; Bit 4: spi2ahb_m_I_mainNoPendingTrans ; Bit 5: usb2host_m_I_mainNoPendingTrans ; Bit 6: usb3drd_m_I_mainNoPendingTrans ; Bit 7: vicap_m_I_mainNoPendingTrans ; Bit 8: vop_m_I_mainNoPendingTrans ; Bit 9: vpsl_m_I_mainNoPendingTrans ; Bit10: vpss_m_I_mainNoPendingTrans ; Bit11: 1'b0 ; Bit12: 1'b0 ; Bit13: 1'b0 ; Bit14: 1'b0 ; Bit15: 1'b0 ; Bit16: 1'b0 ; Bit17: 1'b0 ; Bit18: 1'b0 ; Bit19: 1'b0 ; Bit20: 1'b0 ; Bit21: 1'b0 ; Bit22: 1'b0 ; Bit23: 1'b0 ; Bit24: 1'b0 ; Bit25: 1'b0 ; Bit26: 1'b0 ; Bit27: 1'b0 ; Bit28: 1'b0 ; Bit29: 1'b0 ; Bit30: 1'b0 ; This Bit31 is power Active signal. Bit31: dtp_subddrLKaiisp_pwrDiscTarg_aiispLKmemPwrActive ;

SYS_GRF_BIU_STATUS2
Address: Operational Base(0x20100000) + offset (0x0108)

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Bit	Attr	Reset Value	Description

31:0	RO	0x00000000	PwrActive Power Active Status. The value description: 1'b0: Inactive 1'b1: Active The bit field description: Bit 0 : dtp_aiispLKdr_pwrDiscTarg_vcpLKaiPwrActive ; Bit 1 : dtp_busLKcs_pwrDiscTarg_cruLKsvPwrActive ; Bit 2 : dtp_busLKdr_pwrDiscTarg_ddrLKbsPwrActive ; Bit 3 : dtp_busLKds_pwrDiscTarg_cfgddrLKsvPwrActive ; Bit 4 : dtp_busLKes_pwrDiscTarg_vepuLKsvPwrActive ; Bit 5 : dtp_busLKis_pwrDiscTarg_viLKsvPwrActive ; Bit 6 : dtp_busLKns_pwrDiscTarg_npuLKsvPwrActive ; Bit 7 : dtp_busLKos_pwrDiscTarg_vdoLKsvPwrActive ; Bit 8 : dtp_busLKpp_pwrDiscTarg_vcpLKsvPwrActive ; Bit 9 : dtp_busLKvibrgout_pwrDiscTarg_ddrLKviPwrActive ; Bit10 : dtp_cfgddrLKfw_pwrDiscTarg_ddrfwLKdcPwrActive ; Bit11 : dtp_cpuLKbs_pwrDiscTarg_busLKcoPwrActive ; Bit12 : dtp_cpuLKdr_pwrDiscTarg_ddrLKcoPwrActive ; Bit13 : dtp_npuLKdr_pwrDiscTarg_ddrLKnnPwrActive ; Bit14 : dtp_periLKdr_pwrDiscTarg_vcpLKprPwrActive ; Bit15 : dtp_pmu1LKpmdr_pwrDiscTarg_pmuLKpm1drPwrActive ; Bit16 : dtp_pmuLKdr_pwrDiscTarg_vcpLKpmPwrActive ; Bit17 : dtp_pmuLKpm1sv_pwrDiscTarg_pmu1LKsvPwrActive ; Bit18 : dtp_subddrLKcpu_pwrDiscTarg_cpu_probe_linkPwrActive ; Bit19 : dtp_subddrLKnpu_pwrDiscTarg_npu_probe_linkPwrActive ; Bit20 : dtp_subddrLKpoe_pwrDiscTarg_poe_probe_linkPwrActive ; Bit21 : dtp_subddrLKvi_pwrDiscTarg_vi_probe_linkPwrActive ; Bit22 : dtp_vcpLKaisv_pwrDiscTarg_aiispLksvPwrActive ; Bit23 : dtp_vcpLKdr_pwrDiscTarg_ddrLKvcpPwrActive ; Bit24 : dtp_vcpLKps_pwrDiscTarg_periLKsvPwrActive ; Bit25 : dtp_vcpLKus_pwrDiscTarg_pmuLKsvPwrActive ;

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Bit	Attr	Reset Value	Description
			Bit26 : dtp_vdoLKdr_pwrDiscTarg_busLKvoPwrActive ; Bit27 : dtp_vepuLKdr_pwrDiscTarg_ddrLKvePwrActive ; Bit28 : dtp_vepuLKnn_pwrDiscTarg_npuLKvepuPwrActive ; Bit29 : dtp_viLKdr_pwrDiscTarg_busLKvibrginPwrActive ; Bit30 : dtp_viLKnn_pwrDiscTarg_npuLKviPwrActive ; Bit31 : srv_ddrSWservice_pwrDiscTarg_dma2ddr_m_IPwrActive ;

SYS_GRF_HPMCU_CACHE_STATUS

Address: Operational Base(0x20100000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	ndm_rst_n_out Non-debug module reset output
2	RW	0x0	wfi_halted mcu is in wfi state.
1	RW	0x0	cache_flush_ack cache flush ack
0	RW	0x0	cache_idle cache is in idle state, high active

SYS_GRF_TSADC_GRF_STATUS0

Address: Operational Base(0x20100000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RW	0x0	grf_tsadc_temperature_cch Return the channel for rk tsadc phy. channel 0 is master tsadc phy. channel1 is slave tsadc phy.
19	RO	0x0	reserved
18	RW	0x0	grf_tsadc_eoc Return the eoc from tsadc phy.
17	RW	0x0	grf_tsadc_ota_state Return the ota_state from rk tsadc phy. ota state is over temperature alarm state.
16	RW	0x0	grf_tsadc_otp_state Return the otp_state from rk tsadc phy. otp state is over temperature protect state.
15:0	RO	0x0000	grf_tsadc_temperature Return the temperature from tsadc phy.

SYS_GRF_TSADC_GRF_STATUS1

Address: Operational Base(0x20100000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	grf_tsadc_hi_width Return the hi_width for rk tsadc phy.
15:0	RO	0x0000	grf_tsadc_lo_width Return the lo_width for rk tsadc phy.

SYS_GRF_SYS_STATUS

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Address: Operational Base(0x20100000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RW	0x0	topcs_user_busy 1'b0: not busy. 1'b1: otpc secure module user is busy
24	RW	0x0	topcs_sbpi_busy 1'b0: not busy. 1'b1: otpc secure module sbpi is busy
23	RW	0x0	topcns_user_busy 1'b0: not busy. 1'b1: otpc no secure module user is busy
22	RW	0x0	topcns_sbpi_busy Power on reset when low, reset deassert when high.
21:8	RO	0x0000	reserved
7	RO	0x0	stimer1_en_status Secure TIMER1 active status. 1'b0: Inactive 1'b1: Active
6	RO	0x0	stimer0_en_status Secure TIMER0 active status. 1'b0: Inactive 1'b1: Active
5	RO	0x0	timer5_en_status TIMER5 active status. 1'b0: Inactive 1'b1: Active
4	RO	0x0	timer4_en_status TIMER4 active status. 1'b0: Inactive 1'b1: Active
3	RO	0x0	timer3_en_status TIMER3 active status. 1'b0: Inactive 1'b1: Active
2	RO	0x0	timer2_en_status TIMER2 active status. 1'b0: Inactive 1'b1: Active
1	RO	0x0	timer1_en_status TIMER1 active status. 1'b0: Inactive 1'b1: Active
0	RO	0x0	timer0_en_status TIMER0 active status. 1'b0: Inactive 1'b1: Active

SYS_GRF_CHIP_ID

Address: Operational Base(0x20100000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:0	RW	0x1126000b	chip_id Store the chip id.

SYS_GRF_CHIP_VERSION

Address: Operational Base(0x20100000) + offset (0x0804)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000001	chip_version Store the chip version.

4.4 PERI GRF Register Description

4.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

4.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
PERI_GRF_MEM_GRF_SPRA	0x0000	W	0x00000021	PERI single memory configuration
PERI_GRF_MEM_GRF_DPRA	0x0004	W	0x00000000	PERI dual-port memory config register
PERI_GRF_USB3DRD_GRF_CON_PENDING	0x000C	W	0x000001F4	USB3DRD_GRF pending controller register
PERI_GRF_MEM_GATE_GRF_CON	0x0014	W	0x00000000	PERI Memory Gating Grf Controller Register
PERI_GRF_HPROT_GRF_CON	0x0018	W	0x00000000	GRF AHB Prot Register
PERI_GRF_USB2HOSTPHY_CON0	0x001C	W	0x00008DD2	USB2HOSTPHY controller register0
PERI_GRF_USB3DRDPHY_CON0	0x0020	W	0x00008C52	USBDRDPHY controller register0
PERI_GRF_USB3DRDPHY_CON1	0x0024	W	0x00000000	USBDRDPHY controller register1
PERI_GRF_USB3DRDPHY_CON2	0x0028	W	0x00000000	USBDRDPHY controller register2
PERI_GRF_USB3DRDPHY_CON3	0x002C	W	0x00000000	USBDRDPHY controller register3
PERI_GRF_USB2HOST_CON0	0x0030	W	0x00000820	USB2HOST controller register0
PERI_GRF_USB2HOST_CON1	0x0034	W	0x000004BC	USB2HOST controller register1
PERI_GRF_USB3DRD_CON0	0x0038	W	0x00002000	USB3DRD control register0
PERI_GRF_USB3DRD_CON1	0x003C	W	0x00000000	USB3DRD control register1
PERI_GRF_USB3DRDPHY_INT_EN	0x0074	W	0x00000000	USB3DRDPHY interrupt enable register
PERI_GRF_USB3DRDPHY_INT_ST	0x0078	W	0x00000000	USB3DRDPHY interrupt status register
PERI_GRF_USB3DRDPHY_INT_ST_CLR	0x007C	W	0x00000000	USB3DRDPHY interrupt clear register
PERI_GRF_USB3DRDPHY_LS_CON	0x0080	W	0x00030100	USB3DRDPHY linestate filter controller register
PERI_GRF_USB3DRDPHY_DIS_CON	0x0084	W	0x00030100	USB3DRDPHY disconnect filter controller register

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Name	Offset	Size	Reset Value	Description
PERI_GRF_USB3DRDPHY_BVALID_CON	0x0088	W	0x00030100	USB3DRDPHY bvalid filter controller register
PERI_GRF_USB3DRDPHY_ID_CON	0x008C	W	0x00030100	USB3DRDPHY_ID controller register
PERI_GRF_USB2HOSTPHY_INT_EN	0x0090	W	0x00000000	USB2HOSTPHY interrupt enable register
PERI_GRF_USB2HOSTPHY_INT_ST	0x0094	W	0x00000000	USB2HOSTPHY interrupt status register
PERI_GRF_USB2HOSTPHY_INT_ST_CLR	0x0098	W	0x00000000	USB2HOSTPHY interrupt status clear register
PERI_GRF_USB2HOSTPHY_LS_CON	0x009C	W	0x00030100	USB2HOSTPHY linestate filter controller register
PERI_GRF_USB2HOSTPHY_DIS_CON	0x00A0	W	0x00030100	USB2HOSTPHY disconnect filter controller register
PERI_GRF_USB2HOSTPHY_BVALID_CON	0x00A4	W	0x00030100	USB2HOSTPHY bvalid detect controller register
PERI_GRF_USB2HOSTPHY_ID_CON	0x00A8	W	0x00030100	USB2HOSTPHY id detect controller register
PERI_GRF_USB3DRD_STATUS	0x0100	W	0x00000000	USB3DRD status register
PERI_GRF_USB3DRD_STATUS_CB	0x0104	W	0x00000000	USB3DRD status register current belt
PERI_GRF_USB3DRD_STATUS_LAT0	0x0108	W	0x00000000	USB3DRD status logic analyzer trace register 0
PERI_GRF_USB3DRD_STATUS_LAT1	0x010C	W	0x00000000	USB3DRD status logic analyzer trace register 1
PERI_GRF_USBPHY_ST	0x0110	W	0x00000000	USBPHY status register
PERI_GRF_USB2HOST_ST	0x0114	W	0x00000000	USB2HOST status register
PERI_GRF_USBPHY_UTMI_ST	0x0118	W	0x00000000	USBPHY utmi status register
PERI_GRF_RTC_GRF_ST	0x011C	W	0x00000000	RTC GRF status register

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

4.4.3 Detail Registers Description

PERI_GRF_MEM_GRF_SPRA

Address: Operational Base(0x20110000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bit, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:10	RW	0x0	wtsel_hvt_mux4 Configuration for wtsel mux4 type for memory for VEPU.
9:8	RW	0x0	rtsel_hvt_mux4 Configuration for rtsel mux4 type for memory for VEPU.
7:6	RW	0x0	wtsel_hvt_mux1ormux2 Configuration for wtsel mux1ormux2 mem type for memory for VEPU.
5:4	RW	0x2	rtsel_hvt_mux1ormux2 Configuration for wtsel mux1ormux2 mem type for memory for VEPU.
3:2	RW	0x0	wtsel_svt Configuration for rtsel mux1ormux2 mem type for memory for VEPU. We only use the hvt.
1:0	RW	0x1	rtsel_svt Configuration for rtsel mux1ormux2 mem type for memory for VEPU. We only use the hvt.

PERI_GRF_MEM_GRF_DPRA

Address: Operational Base(0x20110000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5:4	RW	0x0	rtsel VEPU memory configuration. 2'b00: Recommended setting with the optimized read margin. 2'b01: Relaxed read margin setting, used for debugging purpose. 2'b10: More relaxed read margin setting, used for debugging purpose. 2'b11: Most relaxed read margin setting, used for debugging purpose.
3:2	RW	0x0	wtsel VEPU memory configuration. 2'b00: Recommended setting with the optimized write margin. 2'b01: Relaxed write margin setting, used for debugging purpose. 2'b10: More relaxed write margin setting, used for debugging purpose. 2'b11: Most relaxed write margin setting, used for debugging purpose.
1:0	RW	0x0	ptsel VEPU memory configuration. Setting for internal clock skew of port A/B with the optimized design margin and timming. 2'b00: Recommended value. 2'b01: Relaxed setting for internal clock skew of port A/B used for debugging purpose. 2'b10: More Relaxed setting for internal clock skew of port A/B used for debugging purpose. 2'b11: Most Relaxed setting for internal clock skew of port A/B used for debugging purpose.

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PERI_GRF_USB3DRD_GRF_CON_PENDING
Address: Operational Base(0x20110000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:0	RW	0x1f4	grf_con_u3_pending_hp_max The pending hp time value for USB3DRD as the usb3.2 spec test.

PERI_GRF_MEM_GATE_GRF_CON
Address: Operational Base(0x20110000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	grf_con_mem_gat_en_usb3_mem_gate memory gate control for usb3_mem_gate 1'b0: Disable 1'b1: Enable
6	RW	0x0	grf_con_mem_gat_en_usb2host memory gate control for usb2host 1'b0: Disable 1'b1: Enable
5:0	RO	0x00	reserved

PERI_GRF_HPROT_GRF_CON
Address: Operational Base(0x20110000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	grf_con_bufferable_hprot2_fspi0 The ahb mater is fspi0. 1'b1: set 1 for ahb master hprot bit2 field , this means enable the ahb master access is bufferable. 1'b0: set 0 for ahb master hprot bit2 field , this means enable the ahb master access is bufferable.
8	RW	0x0	grf_con_bufferable_hprot2_emmc The ahb mater is emmc. 1'b1: set 1 for ahb master hprot bit2 field , this means enable the ahb master access is bufferable. 1'b0: set 0 for ahb master hprot bit2 field , this means enable the ahb master access is bufferable.
7:0	RO	0x00	reserved

PERI_GRF_USB2HOSTPHY_CON0
Address: Operational Base(0x20110000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:9	RW	0x46	reserve
8	RW	0x1	dmpulldown When soft_con_sel is 1'b1, dmpulldown is controlled by soft_utmi_dmpulldown.

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Bit	Attr	Reset Value	Description
7	RW	0x1	dppulldwon When soft_con_sel is 1'b1, dppulldown is controlled by soft_utmi_dppulldown.
6	RW	0x1	termsel When soft_con_sel is 1'b1, termselect is controlled by soft_utmi_termselect.
5:4	RW	0x1	xcvr When soft_con_sel is 1'b1, xcvrselect is controlled by soft_utmi_xcvrselect.
3:2	RW	0x0	opmode When soft_con_sel is 1'b1, opmode is controlled by soft_utmi_opmode.
1	RW	0x1	suspend When soft_con_sel is 1'b1, suspendn is controlled by soft_utmi_suspendn.
0	RW	0x0	grf_sel Soft control select Bit. 1'b1: Use grf 1'b0: Use controller.

PERI_GRF_USB3DRDPHY_CON0
Address: Operational Base(0x20110000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	bvalid When soft_vbus_sel is 1'b1, vbusvalid and bvalid is controlled by soft_vbus.
14	RW	0x0	bvalid_sel VBUS software control select.
13:12	RO	0x0	reserved
11	RW	0x1	reserve
10	RW	0x1	idpullup Pull-up enable control for IDDIG pin. High valid.
9	RW	0x0	iddig_sel IDDIG select 1'b0: Select iddig output from PHY. 1'b1: Select soft_utmi_iddig.
8	RW	0x0	dmpulldown When soft_con_sel is 1'b1, dmpulldown is controlled by soft_utmi_dmpulldown.
7	RW	0x0	dppulldown When soft_con_sel is 1'b1, dppulldown is controlled by soft_utmi_dppulldown.
6	RW	0x1	termsel When soft_con_sel is 1'b1, termselect is controlled by soft_utmi_termselect.
5:4	RW	0x1	xcvr When soft_con_sel is 1'b1, xcvrselect is controlled by soft_utmi_xcvrselect.

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	opmode When soft_con_sel is 1'b1, opmode is controlled by soft_utmi_opmode.
1	RW	0x1	suspend When soft_con_sel is 1'b1, suspendn is controlled by soft_utmi_suspendn.
0	RW	0x0	soft_sel_con Soft control select Bit. 1'b1: Use grf 1'b0: Use controller.

PERI_GRF_USB3DRDPHY_CON1

Address: Operational Base(0x20110000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6:4	RW	0x0	grf_con_usb3drd_utmi_suspend_n This function active when grf_usbphy_usb3drd_con0 bit 0 is 0 value. 3'b001: the signal "usb3drd_utmi_suspend_n_i" is 0 3'b101: the signal "usb3drd_utmi_suspend_n_i" is 1 3'b011: the signal "usb3drd_utmi_suspend_n_i" is "usb3drd_utmi_suspend_n & usb3drd_utmi_l1_suspend_n" 3'b111: the signal "usb3drd_utmi_suspend_n_i" is "usb3drd_utmi_suspend_n & usb3drd_utmi_l1_suspend_n" 3'bXX0: the signal "usb3drd_utmi_suspend_n_i" is "~usb3drd_utmi_suspend_com_n & ~usb3drd_utmi_l1_suspend_com_n".
3:0	RO	0x0	reserved

PERI_GRF_USB3DRDPHY_CON2

Address: Operational Base(0x20110000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	utmi_dischrgvbus store the utmi disconnect charge vbus value.
7	RW	0x0	utmi_chrgvbus store the utmi charge vbus value
6	RO	0x0	reserved
5	RW	0x0	utmi_drvvbus_val store the utmi drvvbus value
4	RW	0x0	utmi_drvvbus_sel 1'b0: choose usb3drd utmi drvvbus hardware 1'b1: choose grf value,the value is store in bit5

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Bit	Attr	Reset Value	Description
3	RW	0x0	usbphy_commononn configure PLL clock output in suspend mode 1'b0:480MHz clock always on 1'b1:480MHz clock will turn off when both ports suspend asserted. If the supsend of any port deassert, it will wait 1ms to make 480MHz clock stable.
2	RW	0x0	bypasssel_usb3drd bypass select usb3drd
1	RW	0x0	bypassdmen_usb3drd bypass dm enable

PERI_GRF_USB3DRDPHY_CON3

Address: Operational Base(0x20110000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	weakpulldown_tune enable dp/dm weakpulldown
13:12	RW	0x0	weakpullup_tune enable dp/dm weakpulldown
11	RW	0x0	weakpulldown_en enable dp/dm weakpulldown
10	RW	0x0	weakpullup_en enable dp/dm weakpullup
9	RW	0x0	dcp_det force dcp_detected high
8	RW	0x0	cp_det force cp_detected high
7	RW	0x0	dp_attached force dp_attached high
6	RW	0x0	charge_det_byp bypass charging detect module
5	RW	0x0	vdm_src_en open dm voltage source
4	RW	0x0	vdp_src_en open dp voltage source
3	RW	0x0	rdm_pdwn_en open dm pull down resistor
2	RW	0x0	idp_src_en open dp source current
1	RW	0x0	idm_sink_en open dm sink current
0	RW	0x0	idp_sink_en open dp sink current

PERI_GRF_USB2HOST_CON0

Address: Operational Base(0x20110000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:6	RW	0x20	fladj_val_common This feature adjusts any offset from the clock source that drives the macro-SOF counter. The macro-SOF cycle time (number of macro-SOF counter clock periods to generate a macro-SOF microframe length) is equal to 59488 plus this value. The default value is decimal 32, which gives an SOF cycle time of 60000 (each microframe has 60000 bit times). Frame Length (decimal) FLADJ Value (decimal) 59488 0 (0x00) 59504 1 (0x01) 59520 2 (0x02) ... ... 59984 31 (0x1F) 60000 32 (0x20) 60496 63 (0x3F)
5:0	RW	0x20	fladj_val USBHOST fladj bit control. This feature adjusts the frame length of the microframe per port. This value must be the same as that of host0_fladj_val_common, or the EHCI yields undefined results.

PERI_GRF_USB2HOST_CON1

Address: Operational Base(0x20110000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	arb_pause USBHOST ehci/ohci arbiter pause control. 1'b0: Disable 1'b1: Enable
12	RW	0x0	ohci_susp_lgcy OHCI Clock control signal This is a static strap signal. When tied HIGH and the USB port is owned by OHCI, the signal utmi_suspend_o_n reflects the status of the USB port. (suspend or not suspend).
11	RW	0x0	ohci_cntsel Count Select Selects the counter value for simulation or real time for 1 ms. 1'b0: Count full 1 ms 1'b1: Simulation time
10	RW	0x1	clkcktrst Clear Clock Reset Initial reset signal for the Digital Phase-Locked Loop (DPLL) block. This is needed only for simulation and can be tied to inactive in the real netlist. The duration of the reset in simulation must be the same as hreset_n.

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Bit	Attr	Reset Value	Description
9	RW	0x0	app_prt_ovrcur Port Overcurrent Indication from Application When asserted by the application, the corresponding port enters Disable state. This signal controls both EHCI and OHCI controller port state machines. Depending on ownership of the port, the corresponding EHCI or OHCI controller generates an Overcurrent Detect interrupt.
8	RW	0x0	autoppd_on_overcur_en Auto Port Power Disable on Overcurrent This strap signal enables automatic port power disable in the host controller. When this signal is active, if an over-current condition is detected on a powered port and PPC is 1, the PP bit in each affected port is automatically transitioned by the host controller from a 1 to 0, removing power from the port.
7	RW	0x1	word_if Word Interface Selects the data width of the UTMI PHY interface. 1'b1: 16bit interface 1'b0: 8bit interface Only 16bit used in this application.
6	RW	0x0	sim_mode USB HOST0 simulation mode bit control Not used in application.
5	RW	0x1	incrx_en Burst Alignment Enable Forces AHB master to start INCR4/8/16 busts only on burst boundaries. AHB requires that double word width burst be addressed aligned only to the double-word boundary. 1'b1: Start INCRX burst only on burst x-aligned addresses. 1'b0: Normal AHB operation; start bursts on any double word boundary. Note: When this function is enabled, the burst is started only when the lowest bits of haddr are: INCR4: haddr[3:0] == 4'b0000 INCR8: haddr[4:0] == 5'b00000 INCR16: haddr[5:0] == 6'b000000
4	RW	0x1	incr8_en AHB Burst Type INCR8 Enable Enables the AHB master interface to utilize burst INCR8 when appropriate. 1'b1: Use INCR8 when appropriate. 1'b0: Do not use INCR8; use other enabled INCRX bursts or unspecified length burst INCR.
3	RW	0x1	incr4_en AHB Burst Type INCR4 Enable Enables the AHB master interface to utilize burst INCR4 when appropriate. 1'b1: Use INCR4 when appropriate. 1'b0: Do not use INCR4; use other enabled INCRX bursts or unspecified length burst INCR.

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Bit	Attr	Reset Value	Description
2	RW	0x1	incr16_en AHB Burst Type INCR16 Enable Enables the AHB master interface to utilize burst INCR16 when appropriate. 1'b1: Use INCR16 when appropriate. 1'b0: Do not use INCR16; use other enabled INCRX bursts or unspecified length burst INCR.
1	RW	0x0	hubsetup_min Some FS devices down the hub do not recover properly after a pre-amble packet, directed at other LS device, if the hub setup time is four FS clocks. Four FS clocks just meet the specification. By adding one extra clock, these FS devices are made to work better. This strap selects four or five FS clocks as hub setup time for interoperability with the various devices. It is recommended to tie low, that is, for five FS clocks.
0	RW	0x0	app_start_clk OHCI Clock control signal This is an asynchronous primary input to the host core. When the OHCI clocks are suspended, the system has to assert this signal to start the clocks (12 and 48 MHz). This should be de-asserted after the clocks are started and before the host is suspended again. (Host is suspended means HCFS = SUSPEND or all the OHCI ports are suspended).

PERI_GRF_USB3DRD_CON0

Address: Operational Base(0x20110000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	usb3drd_host_u2_port_disable USB2.0 Port Disable control. 1'b0: Port Enabled 1'b1: Port Disabled When 1, this signal stops reporting connect/disconnect events the port and keeps the port in disabled state.
14	RW	0x0	usb3drd_host_port_power_control_present This indicates whether the host controller implementation includes port power control. 1'b0: Indicates that the port does not have port power switches 1'b1: Indicates that the port has port power switches

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Bit	Attr	Reset Value	Description
13:8	RW	0x20	usb3drd_fladj_30mhz_reg HS Jitter Adjustment. Indicates the correction required to accommodate mac3 clock and utmi clock jitter to measure 125 's duration. With fladj_30mhz_reg tied to zero, the high speed 125us micro-frame is counted for 123933ns. You must program the value in terms of high speed bit times in a 30 MHz cycle. The default value that must be driven is 32 (assuming 30 MHz perfect clock). Fladj_30mhz_reg connects to the FLADJ register defined in the xHCI spec in the PCI configuration space. Each count is equal to 16 high speed bit times. By default, when this register is set to 32, it gives a 125us interval. Now, based the clock accuracy you can decrement the count or increment the count to get the 125 us uSOF window. For non-PCI systems, it is recommended that this strap is connected to a register that can be controlled by software. This strap is used in device mode also. If device only mode is implemented, it is recommended to tie this input to 'd32.
7:6	RW	0x0	usb3drd_hub_port_perm_attach Indicates if the device attached to a downstream port is permanently attached or not. 1'b0: Not permanently attached 1'b1: Permanently attached Bit0 is for USB2.0 port and bit1 are for USB 3.0 SS port
5:4	RW	0x0	usb3drd_hub_port_overcurrent This is the per port Overcurrent indication of the root-hub ports: 1'b0: No Overcurrent 1'b1: Overcurrent Bit0 is for USB 2.0 port and bit1 are for USB 3.0 SS port
3:0	RW	0x0	usb3drd_bus_filter_bypass It is expected that this signal is set or reset at power-on reset and is not changed during the normal operation of the core. The function of each bit is: bus_filter_bypass[3]: Bypass the filter for utmiusb3drd_iddig bus_filter_bypass[2]: Bypass the filters for utmisrp_bvalid and utmisrp_sessend bus_filter_bypass[1]: Bypass the filter for pipe3_PowerPresent all U3 ports bus_filter_bypass[0]: Bypass the filter for utmiusb3drd_vbusvalid all U2 ports In non-USB3DRD Host-only mode, internal bus filters are not needed. Values: 1'b0: Bus filter(s) enabled 1'b1: Bus filter(s) disabled (bypassed)

PERI_GRF_USB3DRD_CON1

Address: Operational Base(0x20110000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	usb3drd_host_num_u3_port xHCI usb3 port number, default as 1.

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Bit	Attr	Reset Value	Description
11:8	RW	0x0	usb3drd_host_num_u2_port xHCI host USB2 Port number, default as 1.
7	RW	0x0	usb3drd_pipe_clk_sel usb3drd1_pipe3_rx_pclk/tx_pclk input source clk select. 1'b0: Select clk_usb3drd_pipe for source clock 1'b1: Select clk_usb3drd_utmi for source clock
6	RW	0x0	usb3drd_mem_gate_en 1'b1: Enanle memory auto clock gating 1'b0: Disable memory auto clock gating
5	RW	0x0	usb3drd_host_legacy_smi_bar Use this register to support SMI on BAR defined in xHCI spec. Software must set this register, then clear this register to indicate Base Address Register written.
4	RW	0x0	usb3drd_host_legacy_smi_pci_cmd Use this register to support SMI on PCI Command defined in xHCI spec. Software must set this register, then clear this register to indicate PCI command register written.
3:2	RW	0x0	usb3drd_phystatus_con Grf controll usb pipe phystatus. 2'b00: Select phystatus form phy. 2'b10: Set phystatus to 0. Others: Reserved
1	RW	0x0	usb3drd_pme_en Enable signal for the pme_generation. Enable the core to assert pme_generation. If not use set this bit to 1'b1.
0	RW	0x0	usb3drd_host_u3_port_disable USB 3.0 SS Port Disable control. 1'b0: Port Enabled 1'b1: Port Disabled

PERI_GRF_USB3DRDPHY_INT_EN

Address: Operational Base(0x20110000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:6	RW	0x0	disconnect_irq_en disconnect_irq edge status enable 2'bx1: Disconnect rising edge irq status enable 2'b1x: Disconnect falling edge irq status enable
5:4	RW	0x0	id_irq_en id edge status enable 2'bx1: ID rising edge irq status enable 2'b1x: ID falling edge irq status enable
3:2	RW	0x0	bvalid_irq_en bvalid edge status irq enable 2'bx1: Bvalid rising edge irq status enable 2'b1x: Bvalid falling edge irq status enable
1	RO	0x0	reserved
0	RW	0x0	linestate_irq_en linestate change status irq enable High valid.

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PERI_GRF_USB3DRDPHY_INT_ST
Address: Operational Base(0x20110000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	disconnect_irq disconnect_irq edge status 2'bx1: Disconnect rising edge irq status 2'b1x: Disconnect falling edge irq status
5:4	RW	0x0	id_irq id edge status 2'bx1: ID rising edge irq status 2'b1x: ID falling edge irq status
3:2	RW	0x0	bvalid_irq bvalid edge status irq status 2'bx1: Bvalid rising edge irq status 2'b1x: Bvalid falling edge irq status
1	RO	0x0	reserved
0	RW	0x0	linestate_irq linestate change status irq status

PERI_GRF_USB3DRDPHY_INT_ST_CLR
Address: Operational Base(0x20110000) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:6	RW	0x0	disconnect_irq_clr disconnect_irq edge status clear, write 1 to clear irq status 2'bx1: Disconnect rising edge irq status clear, write 1 to clear irq status 2'b1x: Disconnect falling edge irq status clear, write 1 to clear irq status
5:4	RW	0x0	id_irq_clr id edge status clear, write 1 to clear irq status 2'bx1: ID rising edge irq status clear, write 1 to clear irq status 2'b1x: ID falling edge irq status clear, write 1 to clear irq status
3:2	RW	0x0	bvalid_irq_clr bvalid edge status irq status clear, write 1 to clear irq status 2'bx1: Bvalid rising edge irq status clear, write 1 to clear irq status 2'b1x: Bvalid falling edge irq status clear, write 1 to clear irq status
1	RO	0x0	reserved
0	RW	0x0	linestate_irq_clr linestate change status irq status clear, write 1 to clear irq status

PERI_GRF_USB3DRDPHY_LS_CON
Address: Operational Base(0x20110000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x30100	linestate_filter_con host/usb3drd port linestate filter time control register. Unit:PCLK

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PERI_GRF_USB3DRDPHY_DIS_CON
Address: Operational Base(0x20110000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x30100	disconnect_filter_con host/usb3drd port hostdisconnect filter time control register. Unit:PCLK

PERI_GRF_USB3DRDPHY_BVALID_CON
Address: Operational Base(0x20110000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x30100	bvalid_filter_con usb3drd port bvalid filter time control register. Unit:PCLK

PERI_GRF_USB3DRDPHY_ID_CON
Address: Operational Base(0x20110000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0030100	id_filter_con usb3drd ID port filter time control register. Unit:PCLK

PERI_GRF_USB2HOSTPHY_INT_EN
Address: Operational Base(0x20110000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:6	RW	0x0	disconnect_irq_en disconnect_irq edge status enable 2'bx1: Disconnect rising edge irq status enable 2'b1x: Disconnect falling edge irq status enable
5:1	RO	0x00	reserved
0	RW	0x0	linestate_irq_en linestate change status irq enable High valid.

PERI_GRF_USB2HOSTPHY_INT_ST
Address: Operational Base(0x20110000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	disconnect_irq disconnect_irq edge status 2'bx1: Disconnect rising edge irq status 2'b1x: Disconnect falling edge irq status
5:1	RO	0x00	reserved
0	RW	0x0	linestate_irq linestate change status irq status

PERI_GRF_USB2HOSTPHY_INT_ST_CLR
Address: Operational Base(0x20110000) + offset (0x0098)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:6	RW	0x0	disconnect_irq_clr disconnect_irq edge status clear, write 1 to clear irq status 2'bx1: Disconnect rising edge irq status clear, write 1 to clear irq status 2'b1x: Disconnect falling edge irq status clear, write 1 to clear irq status
5:1	RO	0x00	reserved
0	RW	0x0	linestate_irq_clr linestate change status irq status clear, write 1 to clear irq status

PERI_GRF_USB2HOSTPHY_LS_CON

Address: Operational Base(0x20110000) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x30100	linestate_filter_con host/usb3drd port linestate filter time control register. Unit:PCLK

PERI_GRF_USB2HOSTPHY_DIS_CON

Address: Operational Base(0x20110000) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x30100	disconnect_filter_con host/usb3drd port hostdisconnect filter time control register. Unit:PCLK

PERI_GRF_USB2HOSTPHY_BVALID_CON

Address: Operational Base(0x20110000) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x30100	bvalid_detect_con host/usb3drd port bvalid detect time control register. Unit:PCLK

PERI_GRF_USB2HOSTPHY_ID_CON

Address: Operational Base(0x20110000) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x30100	usb3drd_id_detect_con host/usb3drd port id detect time control register. Unit:PCLK

PERI_GRF_USB3DRD_STATUS

Address: Operational Base(0x20110000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
1	RO	0x0	usb3drd_pme_generation PME Generation. This signal is used to generate a PME# (Power Management Event). When the Run/Stop bit of the USB Command Register is cleared during USB suspend mode, the core cannot generate an event and cannot assert a regular interrupt. In this case, the core asserts a pme_generation signal to report any wakeup condition if pme_en is high. If the system does not support PCI-like PME interface, then it must not clear the Run/Stop bit during USB suspend mode. In this case, the core generates an event and asserts an interrupt when there is any wakeup event.
0	RO	0x0	usb3drd_host_sys_err Host System Error. This signal indicates that a Host System Error has occurred as reflected in the USBSTS.HSE field. This signal is asserted only if the USBCMD.HSEE field is set to '1'. It can occur when the host controller encounters an 'Error' response in the AHB, the AXI, or the Native Master Bus. When the USBSTS.HSE field is cleared by software, this signal is deasserted unless the master continues to assert its bus error output. The typical software response to an HSE is to reset the core. For more details, refer to section 4.10.2.6 of the xHCI 1.0 specification.

PERI_GRF_USB3DRD_STATUS_CB

Address: Operational Base(0x20110000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	usb3drd_host_current_belt[11:0] usb3drd_host_current_belt[11:0] bit status. Current BELT Value. This signal indicates the minimum value of all received BELT values and the BELT that is set by the Set LTV command. This signal is valid only in Host mode.

PERI_GRF_USB3DRD_STATUS_LAT0

Address: Operational Base(0x20110000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	usb3drd_logic_analyzer_trace0 usb3drd_logic_analyzer_trace[31:0] bit status. Logic Analyzer Trace. These are internal design signals that you can use for debug purposes. Some of the signals are interface signals like PIPE, UTMI, ULPI, AXI, and AHB, and others are internal state machines and status information signals. During chip bring-up, to debug functional issues, you can probe the interface signals for additional visibility.

PERI_GRF_USB3DRD_STATUS_LAT1

Address: Operational Base(0x20110000) + offset (0x010C)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	usb3drd_logic_analyzer_trace1 usb3drd_logic_analyzer_trace[63:32] bit status. Logic Analyzer Trace. These are internal design signals that you can use for debug purposes. Some of the signals are interface signals like PIPE, UTMI, ULPI, AXI, and AHB, and others are internal state machines and status information signals. During chip bring-up, to debug functional issues, you can probe the interface signals for additional visibility.

PERI_GRF_USBPHY_ST

Address: Operational Base(0x20110000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	dp_attached assert dp pin connect successfully
19	RW	0x0	cp_detect charging port detected successfully
18	RW	0x0	dcp_detect dp_float detected
17	RW	0x0	dp_flaotdet dp_float detected
16	RW	0x0	dm_floatdet dm_float detected
15	RW	0x0	host_hostdisconnect Host Disconnect status 1'b0: connect 1'b1: disconnect
14	RW	0x0	host_iddig IDDIG status. 1'b0: Host 1'b1: Device
13:12	RW	0x0	host_linestate Line State Indicator This controller bus reflects the state of the single-ended receivers. In Suspend or Sleep mode, this bus is a combinatorial output (directly reflecting the current state of D- and D+, respectively). 11: SE1 (D+ high, D- high) 10: K state for high-speed and full-speed USB traffic; J state for low-speed USB traffic (D+ low, D- high) 01: J state for high-speed and full-speed USB traffic; K state for low-speed USB traffic (D+ high, D- low) 00: SE0 (D+ low, D- low)
11	RW	0x0	host_sessend USB3DRD Device Session Valid Indicator (Low Voltage) This controller signal is output from the USB 2.0 PHY's Session Valid comparator and indicates whether the voltage on VBUS is below the USB3DRD Device Session Valid threshold. 1'b1: The voltage on VBUS is above the USB3DRD Device Session Valid threshold. 1'b0: The voltage on VBUS is below the USB3DRD Device Session Valid threshold.
10	RW	0x0	host_vbusvalid VBUS valid status.

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Bit	Attr	Reset Value	Description
9	RW	0x0	host_avalid VBUS avalid status.
8	RW	0x0	host_bvalid VBUS bvalid status.
7	RW	0x0	usb3drd_hostdisconnect Host Disconnect status 1'b0: connect 1'b1: disconnect
6	RW	0x0	usb3drd_iddig IDDIG status. 1'b0: Host 1'b1: Device
5:4	RW	0x0	usb3drd_linestate Line State Indicator This controller bus reflects the state of the single-ended receivers. In Suspend or Sleep mode, this bus is a combinatorial output (directly reflecting the current state of D- and D+, respectively). 11: SE1 (D+ high, D- high) 10: K state for high-speed and full-speed USB traffic; J state for low-speed USB traffic (D+ low, D- high) 01: J state for high-speed and full-speed USB traffic; K state for low-speed USB traffic (D+ high, D- low) 00: SE0 (D+ low, D- low)
3	RW	0x0	usb3drd_sessend USB3DRD Device Session Valid Indicator (Low Voltage) This controller signal is output from the USB 2.0 PHY's Session Valid comparator and indicates whether the voltage on VBUS is below the USB3DRD Device Session Valid threshold. 1'b1: The voltage on VBUS is above the USB3DRD Device Session Valid threshold. 1'b0: The voltage on VBUS is below the USB3DRD Device Session Valid threshold.
2	RW	0x0	usb3drd_vbusvalid VBUS valid status.
1	RW	0x0	usb3drd_avalid VBUS avalid status.
0	RW	0x0	usb3drd_bvalid VBUS bvalid status.

PERI_GRF_USB2HOST_ST

Address: Operational Base(0x20110000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	ehci_power_state_ack Power State ACK This signal indicates the power state change acknowledgement from the EHCI to the PCI for PCI power management.
29	RO	0x0	ehci_pme_status PME Status This signal displays the PME status. This value is updated in the PCI PMCSR's pme_status bit.

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Bit	Attr	Reset Value	Description
28	RO	0x0	ehci_bufacc EHCI Buffer Access Level signal that is asserted whenever the host controller does a data read/write transfer. If this signal is de-asserted while the AHB is active, the host controller is performing a descriptor read/write. This signal can be used to support Big Endian operation.
27	RO	0x0	ehci_xfer_prdc Transfer Periodic Indicates that the current transfer of the EHCI master on the AHB bus belongs to periodic descriptor/data.
26	RO	0x0	ohci_ccs Current Connect Status of Each Port When set, this bit indicates that the port state machine is in a connected state. If the bit is cleared, the port state machine is in either a disconnected or powered-off state.
25	RO	0x0	ohci_rwe Remote Wake Up Enable This bit reflects the HcControl.RWE bit. This is brought out as a status signal and can be ignored by the application for normal host controller operation.
24	RO	0x0	ohci_drwe Device Remote Wake-Up Enable This signal reflects the HcRhStatus.DRWE bit. When active, it causes the host controller to treat a connect or disconnect event as a remote wake-up, which in turn causes the host controller to enter the Global Resume state from the Global Suspend state. If this bit is cleared, a connect or disconnect event is not treated as a remote wake-up event.
23	RO	0x0	ohci_globalsuspend Host Controller is in Global Suspend State This signal is asserted 5 ms after the host controller enters the USB Suspend state, and is asserted as long as the host controller remains in this state. The host controller enters the USB Suspend state when the Host Controller Driver forces it by writing to the HcControl.HCFS bits. The host controller exits this state when either the Host Controller Driver moves it to USB Reset (Global USB Reset) or USB Resume (Global Resume) or when a remote wake-up event is seen at one of the downstream USB ports.
22	RO	0x0	ohci_bufacc Host Controller Buffer Access Indicator When active, this signal indicates that the host controller is currently accessing the data buffer indicated by the TD. This is simply a status signal to let the application know whether the host controller is reading from or writing to the data buffer indicated by TD, or reading from or writing to the ED, TD descriptor, etc. If this is set (1) during the cycle on the HCI master bus, it indicates buffer fetch and if reset (0), all other transfers (such as ED, TD fetch, and Status Writeback). This is a status signal; the application need not take any action when it is asserted.
21	RO	0x0	ohci_rmtwkp Remote Wakeup Status See the HCI_MRmtWkp signal description in the USB 1.1 OHCI Host Controller Family Databook.

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Bit	Attr	Reset Value	Description
20:17	RO	0x0	ehci_lpsmc_state LPSMC State This signal indicates the state of the LPSMC module. It is used only for debugging.
16:11	RO	0x00	ehci_usbsts USB Status EHCI USBSTS register[5:0] bits. This signal indicates pending interrupts and various host controller statuses. These 6 bits reflect the value in the USBSTS[5:0] register. Active High.
10:0	RO	0x000	ehci_xfer_cnt Transfer Count Transfer byte count from the EHCI master of the current AHB transaction. This is a constant signal and its value is valid when the EHCI starts its AHB address phase. The host controller aborts an AHB transfer before completing the transactions specified in ehci_xfer_cnt when a data read transaction is in progress and both these conditions are true: 1. There is insufficient time to complete the USB transfer. 2. The Root Hub detects an underrun condition.

PERI_GRF_USBPHY_UTMI_ST
Address: Operational Base(0x20110000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	usbhost_utmi_vbusvalid return the usbhost_utmi_vbusvalid value.
6	RO	0x0	usbhost_utmi_bvalid return the usbhost utmi bvalid value.
5	RO	0x0	usbhost_utmi_avalid return the usbhost_utmi_avalid value.
4	RO	0x0	usbhost_utmi_sessend return the usbhost_utmi_sessend value.
3	RO	0x0	usbhost_utmi_iddig return the usbhost_utmi_iddig value.
2	RO	0x0	usb3drd_utmi_avalid return the usb3drd_utmi_avalid value.
1	RO	0x0	usb3drd_utmi_sessend return the usb3drd_utmi_sessend value.
0	RO	0x0	usb3drd_utmi_iddig return the usb3drd_utmi_iddig value.

PERI_GRF_RTC_GRF_ST
Address: Operational Base(0x20110000) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	external_off_o Indicates the chip power off,high active
0	RO	0x0	dig_ldo_rdy Power on reset when low, reset deassert when high.

4.5 USB3 PHY GRF Register Description

4.5.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

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4.5.2 Registers Summary

Name	Offset	Size	Reset Value	Description
USB3_PHY_GRF_PIPE_CON0	0x0000	W	0x00000110	PIPE Combo PHY Configuration Register 0
USB3_PHY_GRF_PIPE_CON1	0x0004	W	0x00000000	PIPE Combo PHY Configuration Register 1
USB3_PHY_GRF_PIPE_CON2	0x0008	W	0x00009401	PIPE Combo PHY Configuration Register 2
USB3_PHY_GRF_PIPE_CON3	0x000C	W	0x00000002	PIPE Combo PHY Configuration Register 3
USB3_PHY_GRF_PIPE_CON4	0x0010	W	0x00000000	PIPE Combo PHY Configuration Register 4
USB3_PHY_GRF_PIPE_STATUS1	0x0034	W	0x000000C0	PIPE Combo PHY Status Register1
USB3_PHY_GRF_LFPS_DET_CON	0x0080	W	0x00000009	PIPE Combo PHY LFPS Detect Control Register
USB3_PHY_GRF_PHY_INT_EN	0x00A0	W	0x00000000	PIPE Combo PHY Interrupt Signal Enable
USB3_PHY_GRF_PHY_INT_STATUS	0x00A4	W	0x00000000	PIPE Combo PHY Interrupt Status

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

4.5.3 Detail Registers Description

USB3_PHY_GRF_PIPE_CON0

Address: Operational Base(0x20118000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	pipe_rxstandby SATA mode Controls whether the PHY RX is active when the PHY is in any power state with PCLK on. RX_STANDBY is ignored when the PHY is in any power state where the high-speed receiver is always off. 1'b0: Active 1'b1: Standby PCIe mode Controls whether the PHY RX is active when the PHY is in P0 or P0s. RX_STANDBY is ignored when the PHY is in P1 or P2 1'b0: Active 1'b1: Standby Only used in SATA and PCIe mode. USB3.0 mode should be tied to 1'b0. The value when override enable is selected.
13	RW	0x0	pipe_rxelecidle_disable RX electrical idle detect disable. The value when override enable is selected. 1'b0: Idle detect enable 1'b1: Idle detect disable

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Bit	Attr	Reset Value	Description
12	RW	0x0	pipe_rxterm Control presence of receiver terminations. The value when override enable is selected. 1'b0: Termination removed 1'b1: Termination present Only used in USB3.0 mode, PCIe and SATA mode should be tied to 1'b1.
11	RW	0x0	pipe_bypass_codec PCIe mode, USB mode, and SATA mode. The value when override enable is selected. Controls whether the PHY performs 8b/10b encode and decode. 1'b0: 8b/10b encode/decode performed normally by the PHY 1'b1: 8b/10b encode/decode bypassed, 20bit 8b/10b encode/decode bypass mode works only when BUS_WIDTH=2'b01 It should be tie to 1'b1 in SATA low latency and SERDES mode.
10	RW	0x0	pipe_ebuffmode RX Elasticity Buffer operating mode selection. The value when override enable is selected. 1'b0: Nominal half-full buffer mode 1'b1: Nominal empty buffer mode In SATA and USB3.0 mode, when RX elastic buffer is operating at nominal empty buffer mode, RX_DATA_VALID is de-asserted which means elastic buffer is empty and no data is available. In PCIe mode, only nominal half-full Elasticity Buffer mode is supported.
9	RW	0x0	pipe_l1sub_entreq In PCIe mode L1 sub-state entry request signal in PCIe mode. When set to high, it instructs PHY to do power transition to L1 sub-state. In SATA Mode When set to high, it will be power down PLL. This signal could be connected to the L1 sub-state enable/request signal from controller Only used in PCIe and SATA mode, USB mode should be tied to 1'b0. The value when override enable is selected. Reserved for current chip.
8	RW	0x1	pipe_mac_pclkreq_n PCIe common clock request signal in PCIe mode. The signal shall be low and CKREF_SRC[1:0] is set to 2'b10 when CKREFP/N and PCI_100M_CLK output from PHY is used for PCIe system with common clock Note: Details refer to CKREFP/N and PCI_100M_CLK. Only used in PCIe mode, USB and SATA mode should be tied to 1'b1. This bit is a override bit for input CLKREQ for PHY when override selection enable.

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Bit	Attr	Reset Value	Description
7:6	RW	0x0	pipe_powerdown Power up or power down status control of Transceiver. If PIPE PHY support PIPE4.3, the powerdown is 4-bit, PIPE4.2 or below 2-bit. This filed is powerdown [1:0], powerdown[3:2] is controlled by pipe_powerdown_4p3. The value when override enable is selected. In PCIe mode 4'h0: P0, normal mode 4'h1: P0s, low recovery time latency, power saving state 4'h2: P1, longer recovery time latency, lower power saving 4'h3: P2, lowest power state 4'h4: P1.CPM 4'h5: P1.1 4'hc: P1.2 Others: Reserved In USB3.0 mode 4'h0: P0, normal mode 4'h1: P1, low recovery time latency, power saving state 4'h2: P2, longer recovery time latency, lower power saving 4'h3: P3, lowest power state Others: Reserved In SATA and Serdes mode 4'h0: POWER_STATE_0 operational state, PHY normal operation 4'h1: PCLK on, TX common mode on 4'h3: PCLK on, TX common mode off 4'h5: PCLK off, TX common mode on 4'h7: PCLK off, TX common mode off Others: Reserved
5:4	RW	0x1	pipe_rate Combo PHY link signaling rate. The value when override enable is selected. In PCIe mode 2'b00: 2.5GT/s 2'b01: 5.0GT/s Others: Reserved In USB3.0 mode 2'b00: 5GT/s Others: Reserved In SATA mode 2'b00: 1.5GT/s 2'b01: 3.0GT/s 2'b10: 6.0GT/s 2'b11: Reserved In SERDES(QSGMII/SGMII) mode 2'b00: 1.25Gbps 2'b01: Reserved 2'b10: 5.0Gbps 2'b11: Reserved

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	pipe_phymode Combo PHY mode. 2'b00: PCIe 2'b01: USB3 2'b10: SATA 2'b11: Serdes In RK3588 Combo PHY PIPE4.3. The PHY and controller usage list below when each PHY mode is set to PCIe: 1L0 connects to Combo PHY1, when pcie1l0_sel is set to 1'b1. 1L1 connects to Combo PHY2, when pcie1l1_sel is set to 1'b1. 1L2 connects to Combo PHY0.
1:0	RW	0x0	pipe_databuswidth Combo PHY PIPE data bus width. The value when override enable is selected. 2'b00: 32-bit, PCIe and USB3 only support 32-bit 2'b01: 16-bit, SATA only support 16-bit 2'b10: Reserved 2'b11: Reserved

USB3_PHY_GRF_PIPE_CON1

Address: Operational Base(0x20118000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:13	RW	0x0	phy_clk_sel Combo Phy PIPE reference clock frequency selection. 2'b00: 24M 2'b01: 25M 2'b10: 100M 2'b11: Reserved
12:11	RW	0x0	pipe_txpattern_sata Controls which pattern the PHY sends at the Gen 1 rate when sending OOB or initialization signaling. The PHY transmits this pattern at the Gen 1 rate regardless of what rate the PHY is configured at. Used in SATA mode only. The value when override enable is selected. 2'b00: C ALIGN 2'b01: C D24.3 2'b10: C D10.2 2'b11: C Reserved
10:8	RW	0x0	pipe_txmargin Transmit margin control, combined with txswing to control TX output amplitude. The value when override enable is selected.
7:6	RW	0x0	pipe_txdeemph Transmitter de-emphasis level configuration. The value when override enable is selected. 2'b00: -6dB 2'b01: -3.5dB 2'b10: No de-emphasis 2'b11: Reserved

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Bit	Attr	Reset Value	Description
5	RW	0x0	pipe_txswing Control transmitter voltage swing level. The value when override enable is selected. 1'b0: Full swing 1'b1: Low swing
4	RW	0x0	pipe_txcompliance Set the running disparity to negative. Only used in PCIe mode, USB and SATA mode should be tied to 1'b0. The value when override enable is selected.
3	RW	0x0	pipe_txcommonmode_disable TX Common mode Control. 1'b0: Enable 1'b1: Disable The value when override enable is selected.
2	RW	0x0	pipe_txoneszeros This signal is used in USB3.0 mode for transmitting compliance pattern CP7 and CP8. When set to high, it causes the transmitter to transmit an alternating sequence of 0s and 1s, regardless the states of TX_DATA. Only used in USB mode, PCIE and SATA mode should be tied to 1'b0. The value when override enable is selected.
1	RW	0x0	pipe_txelecidle Forces TX output to electrical idle when asserted except in loopback, refer to PIPE spec for details on control signal usage. When asserted with TX_COMPLIANCE high, the PHY is fully powered off. Shall be kept high when SATA mode that is not in P0. The value when override enable is selected.
0	RW	0x0	pipe_txdectrx_loopback Used to tell the PHY to begin a receiver detection operation or to begin loopback. Refer to s PIPE spec for detail description. This signal shall be set to low when SATA mode that is not in P0. The value when override enable is selected.

USB3_PHY_GRF_PIPE_CON2

Address: Operational Base(0x20118000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x1	sel_pipe_txcompliance pipe_txcompliance selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
14	RW	0x0	sel_pipe_txcommonmode_disable pipe_txcommonmode_disable selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF

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Bit	Attr	Reset Value	Description
13	RW	0x0	sel_pipe_txoneszeros pipe_txoneszeros selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
12	RW	0x1	sel_pipe_txelecidle pipe_txelecidle selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
11	RW	0x0	sel_pipe_txdectrx_loopback pipe_txdectrx_loopback selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
10	RW	0x1	sel_pipe_rxstandby sel_pipe_rxstandby selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
9	RW	0x0	sel_pipe_rxelecidle_disable pipe_rxelecidle_disable selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
8	RW	0x0	sel_pipe_rxterm pipe_rxterm selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
7	RW	0x0	sel_pipe_bypass_codec pipe_bypass_codec selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
6	RW	0x0	sel_pipe_ebuffmode pipe_ebuffmode selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
5	RW	0x0	sel_pipe_l1sub_entreq pipe_l1sub_entreq selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
4	RW	0x0	sel_pipe_powerdown pipe_powerdown selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
3	RW	0x0	sel_pipe_mac_pclkreq_n pipe_mac_pclkreq_n selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF

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Bit	Attr	Reset Value	Description
2	RW	0x0	sel_pipe_rate pipe_rate selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
1	RW	0x0	sel_pipe_phymode pipe_phymode selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF Reserved for RK3588
0	RW	0x1	sel_pipe_databuswidth pipe_databuswidth selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF

USB3_PHY_GRF_PIPE_CON3

Address: Operational Base(0x20118000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	qsgm_mode QSGMII mode enable. 1'b0: Other mode 1'b1: QSGMII/SGMII mode Reserved in this chip
14:13	RW	0x0	pipe_sel Control the PD PIPE interface source selection, it's used for RK356X Combo PIPE4.2 PHY only. For Combo PIPE PHY0 2'b01: Connect to USB3 Controller 0 2'b10: Connect to SATA Port 0 Others: Reserved For Combo PIPE PHY1 2'b01: Connect to USB3 Controller 1 2'b10: Connect to SATA Port 1 2'b11: Connect to QSGMII Controller Others: Reserved For Combo PIPE PHY2 2'b00: Connect to PCIe2.0 Controller 2'b10: Connect to SATA Port 2 2'b11: Connect to QSGMII Controller Others: Reserved Reserved in this chip.
12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11	RW	0x0	sel_clkreq CLKREQ for PIPE PHY source selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side(Controller/Constant/PD GRF/PHY GRF) 1'b1: From GPIO mux for CLKREQ_N Because the CLKREQ is valid when high, so the pipe_mac_pclkreq_n should set to "0" when sel_pipe_mac_pclkreq_n is set to "1".
10	RW	0x0	sel_rxelecidle Rxelecidle to controller source selection. Override value is selected for PIPE PHY interface. 1'b0: From PIPE PHY 1'b1: When rxelecidle_disable is high, rxelecidle return "1" to controller
9:8	RW	0x0	phy_clk_ref_src Combo PHY PIPE reference clock source selection. 2'b00: Use PLL_CKREF_INNER as reference clock source, CKREFP/N is not active, the PAD can be floating 2'b01: Use CKREFP/N as input reference clock source 2'b10: Use PLL_CKREF_INNER (From SoC CRU) as reference clock source, Use CKREFP/N as output clock to provide a differential 100M reference clock in PCIe mode while PIPE PHY CLKREQ is high. 2'b11: Not allowed
7:4	RO	0x0	reserved
3	RW	0x0	sel_pipe_txpattern_sata pipe_txpattern_sata selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
2	RW	0x0	sel_pipe_txmargin pipe_txmargin selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
1	RW	0x1	sel_pipe_txdeemph pipe_txdeemph selection. Override value is selected for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF
0	RW	0x0	sel_pipe_txswing pipe_txswing selection. Override value is selected select for PIPE PHY interface. 1'b0: From controller side (Controller/Constant/PD GRF) 1'b1: From PHY GRF

USB3_PHY_GRF_PIPE_CON4

Address: Operational Base(0x20118000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
8	RW	0x0	pipe_txdeemph_ext Extra direct control the txdeemph bit3. Reserved in RK356X.
7:4	RW	0x0	bist_mode BIST mode test in normal operation. 4'h0: PHY Normal operation, default value of BIST_MODE 4'h8: PHY external BIST from TXP/TXN to RXP/RXN 4'h9: PHY internal BIST 4'ha: PHY send 1'b0 on TXP and 1'b1 on TXN (only for VOL test) 4'hc: PHY send 1'b1 on TXP and 1'b0 on TXN (only for VOH test) 4'he: PHY send D10.2 (only for Eye-Diagram test) Others: Reserved Reserved in RK356X.
3:2	RW	0x0	serdes_arch This signal indicates whether Serdes architecture and SATA low latency is enabled. 2'b00: PCIe/USB/SATA normal working 2'b01: Used for SATA SAPIS compliant controller, that bypass PHY elastic buffer to reduce latency, RX_DATA is the result of comma align. 2'b10: General serdes mode and RX_DATA is the result of CDR in PMA 2'b11: General serdes mode and RX_DATA is the result of comma align Reserved in RK356X.
1:0	RW	0x0	pipe_powerdown_4p3 For PIPE4.3 interface, the powerdown are 4 bit, the field is for powerdown[3:2]. Override value when override enable is selected. Reserved in RK356X.

USB3_PHY_GRF_PIPE_STATUS1

Address: Operational Base(0x20118000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RO	0x0	pipe_clkreq_n Indicates that the PHY is in corresponding state to L1-sub-state in PCIE mode, during which PHY reference clock could be turned off. This signal could connect to corresponding signal in controller IP, if applicable.
8	RO	0x0	pipe_power_presetn Reserved
7	RO	0x1	pipe_rxelecidle_o Indicates receiver detection of an electrical idle. When de-asserted with the PHY in P2 (PCIE Mode), indicates a detection of beacon, while indicate exit from electrical idle in other power states in PCIe mode. In USB3.0 mode, it indicates the detection of LFPS. In SATA mode, it indicates if there is no data/OOB received.
6	RO	0x1	pipe_phystatus_o Used to communicate completion of several PHY functions including power management state transitions, rate change and receiver detection.

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Bit	Attr	Reset Value	Description
5:3	RO	0x0	pipe_rxstatus_o PIPE PHY receiver status. Encode receiver status and error codes for the received data stream when receiving data. 3'b000: Received data OK 3'b001: PCIe mode, 1 SKP added; USB mode: 1 SKP added; SATA mode: 1 ALIGN added Asseted width first byte of Align that was added 3'b010: PCIe mode: 1 SKP Ordered set removed; 1 SKP Ordered Set removed; SATA mode: 1 or more ALIGNs 3'b011: PCIe and USB mode: Receiver detected 3'b100: 8B/10B decode error 3'b101: Elastic buffer overflow 3'b110: Elastic buffer under flow, this error code is not used if the elastic buffer is operating in the nominal buffer empty mode 3'b111: Receive disparity error, overwritten by decode error
2:0	RO	0x0	reserved

USB3_PHY_GRF_LFPS_DET_CON

Address: Operational Base(0x20118000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x09	lfps_detect_con LFPS Detect Count Filter Control. This counter determines whether a rxelecidle (high pulse) is valid or not. The counter is based on Combo PIPE PHY APB PCLK.

USB3_PHY_GRF_PHY_INT_EN

Address: Operational Base(0x20118000) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	rxelecidle_l1_fall_irq_en rxelecidle_l1_fall irq enable. 1'b0: IRQ disable 1'b1: IRQ enable Reserved for current PHY.
1:0	RW	0x0	rxelecidle_l0_fall_irq_en rxelecidle_l0_fall irq enable. 1'b0: IRQ disable 1'b1: IRQ enable

USB3_PHY_GRF_PHY_INT_STATUS

Address: Operational Base(0x20118000) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	W1C	0x0	rxelecidle_l1_fall_irq_st rxelecidle_l1_fall irq status. 1'b0: Interrupt inactive 1'b1: Interrupt active Reserved for current PHY.
0	W1C	0x0	rxelecidle_l0_fall_irq_st rxelecidle_l0_fall irq status. 1'b0: Interrupt inactive 1'b1: Interrupt active

4.6 CPU GRF Register Description

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4.6.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

4.6.2 Registers Summary

Name	Offset	Size	Reset Value	Description
CPU_GRF_CON0	0x0000	W	0x00008000	CPU control register0
CPU_GRF_CON1	0x0004	W	0x00000848	CPU control register1
CPU_GRF_MEM_CFG_UHDSPRA	0x0008	W	0x00000021	CPU UHDSPRA memory configuration
CPU_GRF_STATUS0	0x000C	W	0x00000000	CPU status register0
CPU_GRF_STATUS1	0x0010	W	0x00000003	CPU status register1

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

4.6.3 Detail Registers Description

CPU_GRF_CON0

Address: Operational Base(0x20130000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable. 1'b1: Write access enable.
15	RW	0x1	sysbardisable Disable broadcasting of barriers onto the system bus: 1'b0: Barriers are broadcast onto the system bus. This requires an AMBA4 ACE, or AMBA5 CHI, interconnect. 1'b1: Barriers are not broadcast onto the system bus. This is compatible with an AXI3 interconnect and most AMBA4 interconnects. This pin is sampled only during reset of the Cortex-A53 processor.
14	RW	0x0	broadcastouter Enable broadcasting of outer shareable transactions: 1'b0: Outer Shareable transactions are not broadcast externally. 1'b1: Outer Shareable transactions are broadcast externally. This pin is sampled only during reset of the Cortex-A53 processor.
13	RW	0x0	broadcastinner Enable broadcasting of Inner Shareable transactions: 1'b0: Inner Shareable transactions are not broadcast externally. 1'b1: Inner Shareable transactions are broadcast externally. If BROADCASTINNER is tied HIGH, you must also tie BROADCASTOUTER HIGH. This pin is sampled only during reset of the Cortex-A53 processor.
12	RW	0x0	broadcastcachemaint Enable broadcasting of cache maintenance operations to downstream caches: 1'b0: Cache maintenance operations are not broadcast to downstream caches. 1'b1: Cache maintenance operations are broadcast to downstream caches. This pin is sampled only during reset of the Cortex-A53 processor.
11	RW	0x0	evento_clear Clear the output of active events that execute SEV instruction.

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Bit	Attr	Reset Value	Description
10	RW	0x0	eventi Event input for processor wake-up from WFE low-power state.
9	RW	0x0	clrexmonreq Clearing of the external global exclusive monitor request. When this signal is asserted, it acts as a WFE wake-up event to all the cores in the MPCore device.
8	RW	0x0	l2rstdisable Disable automatic L2 cache invalidate at reset: 0 Hardware resets L2 cache. 1 Hardware does not reset L2 cache.
7:4	RW	0x0	cfgte Enable T32 exceptions. It sets the initial value of the TE bit in the CP15 SCTLR register: 1'b0: TE bit is LOW. 1'b1: TE bit is HIGH. This pin is sampled only during reset of the processor.
3:0	RW	0x0	cfgend Endianness configuration at reset. It sets the initial value of the EE bits in the CP15 SCTLR_EL3 and SCTR_S registers: 1'b0: EE bit is LOW. 1'b1: EE bit is HIGH. This pin is sampled only during reset of the processor.

CPU_GRF_CON1

Address: Operational Base(0x20130000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable. 1'b1: Write access enable.
15	RO	0x0	reserved
14	RW	0x0	dbgl1rstdisable Disable L1 data cache automatic invalidate on reset functionality: 1'b0: Enable automatic invalidation of L1 data cache on reset. 1'b1: Disable automatic invalidation of L1 data cache on reset. This pin is sampled only during reset of the processor.
13:0	RW	0x0848	periphbase Specifies the bits [31:18] of base address for the GIC registers. This value is sampled into the CP15 Configuration Base Address Register (CBAR) at reset.

CPU_GRF_MEM_CFG_UHDSPRA

Address: Operational Base(0x20130000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	W1C	0x021	mem_cfg_uhdspra UHDSPRA memory configuration.

CPU_GRF_STATUS0

Address: Operational Base(0x20130000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	wrmemattr Write request memory attributes.

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Bit	Attr	Reset Value	Description
23:16	RO	0x00	rdmemattr Read request memory attributes.
15	RO	0x0	evento Event output. Active when a SEV instruction is executed.
14	RO	0x0	eventi_ack Event input ack for processor wake-up from WFE state.
13	RO	0x0	clrexmonack Clearing of the external global exclusive monitor acknowledge.
12:9	RO	0x0	smpen Indicates whether a core is taking part in coherency.
8	RO	0x0	standbywfil2 Indicates whether the L2 memory system is in WFI low-power state. This signal is activewhen the following conditions are met: All cores are in WFI low-power state, held in reset, or nL2RESET is asserted LOW. In an ACE configuration, ACINACTM is asserted HIGH. In a CHI configuration, SINACT is asserted HIGH. If ACP has been configured, AINACTS is asserted HIGH. L2 memory system is idle.
7:4	RO	0x0	standbywfi Indicates if a processor is in WFI low-power state: 1'b0 : Processor not in WFI low-power state. 1'b1 : Processor in WFI low-power state.
3:0	RO	0x0	standbywfe Indicates if a processor is in WFE low-power state: 1'b0 : Processor not in WFE low-power state. 1'b1 : Processor in WFE low-power state.

CPU_GRF_STATUS1

Address: Operational Base(0x20130000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x1	st_jtagtop Indicates the state of the JTAG-DP TAP controller. These states are: Test-Logic-Reset Run-Test/Idle Select-DR-Scan Select-IR-Scan
0	RO	0x1	st_jtagnsw The SWJ-DP contains a mode status output: 1'b1 : The SWJ-DP is in JTAG mode. 1'b0 : The SWJ-DP is in LOW when in SWD mode.

4.7 PMU GRF Register Description

4.7.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

4.7.2 Registers Summary

Name	Offset	Size	Reset Value	Description
PMU_GRF_SOC_CON0	0x0000	W	0x00000200	System control register 0
PMU_GRF_SOC_CON1	0x0004	W	0x00000908	System control register 1

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Name	Offset	Size	Reset Value	Description
PMU_GRF_SOC_CON2	0x0008	W	0x00000080	System control register 2
PMU_GRF_SOC_CON3	0x000C	W	0x00002EE0	System control register 3
PMU_GRF_SOC_CON4	0x0010	W	0x00000000	System control register 4
PMU_GRF_SOC_CON5	0x0014	W	0x00000000	System control register 5
PMU_GRF_SOC_CON6	0x0018	W	0x00000000	System control register 6
PMU_GRF_SOC_CON7	0x001C	W	0x00000000	System control register 7
PMU_GRF_SOC_CON8	0x0020	W	0x0000001F	System control register 8
PMU_GRF_SOC_CON9	0x0024	W	0xFFFFFFFF	System control register 9
PMU_GRF_SOC_CON10	0x0028	W	0x00000000	System control register 10
PMU_GRF_SOC_CON11	0x002C	W	0x00000000	System control register 11
PMU_GRF_SOC_CON12	0x0030	W	0x00000000	System control register 12
PMU_GRF_SOC_CON13	0x0034	W	0x00000000	System control register 13
PMU_GRF_SOC_CON14	0x0038	W	0x00000000	System control register 14
PMU_GRF_SOC_CON15	0x003C	W	0x00000000	System control register 15
PMU_GRF_AAD_CON0	0x0080	W	0x00000000	AAD control register 0
PMU_GRF_MEN_CON0	0x0140	W	0x00000000	Memory control register 0
PMU_GRF_MEN_CON1	0x0144	W	0x00000021	Memory control register 1
PMU_GRF_MEN_CON2	0x0148	W	0x00000155	Memory control register 2
PMU_GRF_SOC_SPECIAL0	0x0150	W	0x00000001	System control special0 register
PMU_GRF_SOC_AOV_INT_CON	0x0160	W	0x00000000	AOV interrupt control register
PMU_GRF_SOC_STATUS0	0x0170	W	0x00003000	System status register 0
PMU_GRF_SOC_STATUS1	0x0174	W	0x00000000	System status register 1
PMU_GRF_SOC_STATUS2	0x0178	W	0x00000000	System status register 2
PMU_GRF_OS_REG0	0x0200	W	0x00000000	PMU GRF OS register0
PMU_GRF_OS_REG1	0x0204	W	0x00000000	PMU GRF OS register1
PMU_GRF_OS_REG2	0x0208	W	0x00000000	PMU GRF OS register2
PMU_GRF_OS_REG3	0x020C	W	0x00000000	PMU GRF OS register3
PMU_GRF_OS_REG4	0x0210	W	0x00000000	PMU GRF OS register4
PMU_GRF_OS_REG5	0x0214	W	0x00000000	PMU GRF OS register5
PMU_GRF_OS_REG6	0x0218	W	0x00000000	PMU GRF OS register6
PMU_GRF_OS_REG7	0x021C	W	0x00000000	PMU GRF OS register7
PMU_GRF_OS_REG8	0x0220	W	0x00000000	PMU GRF OS register8

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Name	Offset	Size	Reset Value	Description
PMU_GRF_OS_REG9	0x0224	W	0x00000000	PMU GRF OS register9
PMU_GRF_OS_REG10	0x0228	W	0x00000000	PMU GRF OS register10
PMU_GRF_OS_REG11	0x022C	W	0x00000000	PMU GRF OS register11
PMU_GRF_RESET_FUNCTION_STATUS	0x0230	W	0x00000000	system reset status register
PMU_GRF_RESET_FUNCTION_CLR	0x0234	W	0x00000000	system reset status clear register
PMU_GRF_SIG_DETECT_CON	0x0380	W	0x00000000	sdmmc detect control reg
PMU_GRF_SIG_DETECT_STATUS	0x0390	W	0x00000000	sdmmc detect status reg
PMU_GRF_SIG_DETECT_STATUS_CLEAR	0x03A0	W	0x00000000	sdmmc irq clear reg
PMU_GRF_SDMMC_DET_COUNTER	0x03B0	W	0x000003E8	sdmmc detect counter reg

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

4.7.3 Detail Registers Description

PMU_GRF_SOC_CON0

Address: Operational Base(0x20130000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	grf_con_rtc_clamp_en RTC_32k clock clamp enable. Default value is 1'b0, means clamp enable. 1'b0: Clamp Enable 1'b1: Clamp Disable
14	RW	0x0	grf_con_usb_clamp_en USB3PHY clamp enable. Default value is 1'b0, means clamp enable. 1'b0: Clamp Enable 1'b1: Clamp Disable
13	RO	0x0	reserved
12	RW	0x0	grf_con_pwm_clk_gate_pll_sel PMU can gate pwm clock from pll source. 1'b0: Disable 1'b1: Enable
11	RW	0x0	grf_con_pwm_clk_gate_osc_sel PMU can gate pwm clock from osc source. 1'b0: Disable 1'b1: Enable
10	RW	0x0	grf_con_ddrphy_bufferen_core 1'b0: Enable ddrphy io retention 1'b1: Disable ddrphy io retention
9	RW	0x1	grf_con_ddrphy_bufferen_sel 1'b0: Ddrphy_bufferen from pmu and ddr_fail_safe 1'b1: Ddrphy_bufferen from grf_con_ddrphy_bufferen_core. Default value is 1'b1, so ddr_io_ret is enable.
8:4	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
3	RW	0x0	grf_con_pmic_sleep2_pol Select polarity of IO_PWRctrl2 1'b0: High active. 1'b1: Low active.
2:0	RW	0x0	grf_con_pmic_sleep2_sel IO_PWRctrl2 function selection 3'b000: From pmu block, indicate the VDD_LOGIC power off state 3'b001: From reset pulse generator, can reset external PMIC 3'b010: From pmu block, indicate the VDD_CORE power off state 3'b011: From pmu block, indicate the VDD_NPU power off state 3'b100: From pmu block, indicate the pd_pmu1 power off state

PMU_GRF_SOC_CON1

Address: Operational Base(0x20130000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	grf_con_fspi1_clk_ioen Psram_spi_clk oen 1'b0: Output enable 1'b1: Output disable
14	RW	0x0	grf_con_pmumcu_soft_irq LPMCU software interrupt 1'b0: Disable 1'b1: Enable
13	RW	0x0	grf_con_pwm1_switch_ena Pwm1 switch enable 1'b0: Disable 1'b1: Enable
12	RW	0x0	grf_con_pwm0_switch_ena Pwm0 switch enable 1'b0: Disable 1'b1: Enable
11	RW	0x1	grf_con_uart0_dma_rx_single_bypass uart2 dma_rx single mode bypass 1'b0: Bypass 1'b1: Not bypass
10	RW	0x0	grf_con_uart0_rts_inv uart2_rtsn invert enable 1'b0: Disable 1'b1: Enable
9	RW	0x0	grf_con_uart0_cts_inv uart2_ctsn invert enable 1'b0: Disable 1'b1: Enable
8	RW	0x1	grf_con_clk_32_ioen IO_clk_32k oen 1'b0: Output enable 1'b1: Output disable

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Bit	Attr	Reset Value	Description
7	RW	0x0	grf_con_pmic_sleep1_pol Select polarity of IO_PWRctrl1 1'b0: High active. 1'b1: Low active.
6:4	RW	0x0	grf_con_sleep1_src_sel IO_PWRctrl1 function selection 3'b000: From pmu block, indicate the VDD_LOGIC power off state 3'b001: From reset pulse generator, can reset external PMIC 3'b010: From pmu block, indicate the VDD_CORE power off state 3'b011: From pmu block, indicate the VDD_NPU power off state 3'b100: From pmu block, indicate the pd_pmu1 power off state
3	RW	0x1	grf_con_pmic_sleep0_pol Select polarity of IO_PWRctrl0 1'b0: High active. 1'b1: Low active.
2:0	RW	0x0	grf_con_sleep0_src_sel IO_PWRctrl0 function selection 3'b000: From pmu block, indicate the VDD_LOGIC power off state 3'b001: From reset pulse generator, can reset external PMIC 3'b010: From pmu block, indicate the VDD_CORE power off state 3'b011: From pmu block, indicate the VDD_NPU power off state 3'b100: From pmu block, indicate the pd_pmu1 power off state

PMU_GRF_SOC_CON2

Address: Operational Base(0x20130000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	grf_con_sdmmc0_detn_pol Select polarity of sdmmc0_detn_masked_pin 1'b0: Low active. 1'b1: High active.
13:12	RW	0x0	grf_con_wdt_ns_pmu_pause_speed WDT_PMU pause enable 1'b0: Disable 1'b1: Enable
11	RW	0x0	grf_con_lpmcu_hprot2 hprot[2] of LPMCU AHB master.
10	RW	0x0	grf_con_bufferable_hprot2_fspi1 hprot[2] of FSPI1 bufferable AHB master.
9	RW	0x0	grf_con_spi2ahb_hprot2 hprot[2] of SPI2AHB AHB master.
8	RW	0x0	grf_con_pwr_ctrl0_ioen Output enable of power_ctrl0. 1'b0: Output enable 1'b1: Output disable

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Bit	Attr	Reset Value	Description
7	RW	0x1	grf_con_lpsai_sel 1'b0: audioadc receive data from SAI2 1'b1: audioadc receive data from SAI_lP
6	RO	0x0	reserved
5	RW	0x0	grf_con_pmu1_power_gating_mask PD_PMU1 power gate mask. 1'b0: mask disable 1'b1: mask enable
4	RW	0x0	grf_con_pmumem_clkgat_disable Pmu Sram clockgating disable 1'b0: Disable 1'b1: Enable
3	RW	0x0	grf_con_aoamem_clkgat_disable AOA Sram clockgating disable 1'b0: Disable 1'b1: Enable
2	RW	0x0	grf_con_adcmem_auto_gating_en ADCMEM clock auto gating 1'b0: Disable 1'b1: Enable
1	RW	0x0	grf_con_ldo_leakage_en LDO33V09 leakage enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	grf_con_ldo_leakage_sel LDO33V09 leakage enable select 1'b0: pmu_sleep from PMU 1'b1: grf_con_ldo_leakage_en

PMU_GRF_SOC_CON3

Address: Operational Base(0x20130000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:0	RW	0x2ee0	npor_out2chip_pulse_width Pulse width of triggered NPOR output. Multiplied with XIN_OSC clock period. The default value is 500us.

PMU_GRF_SOC_CON4

Address: Operational Base(0x20130000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	pmucru_softrst_hold0 Each bit has a reset hold. [0]: dbresetn_pmu_gpio0 [1]: hresetn_pmu_biu [2]: hresetn_pmu_sram [3]: presetn_cru_pmu [4]: presetn_i2c2 [5]: presetn_ioc_pmuio0 [6]: presetn_lpmcu_mailbox [7]: presetn_pmu_gpio0 [8]: presetn_pmu_grf [9]: presetn_pmu_hp_timer [10]: presetn_pwm1 [11]: presetn_rcosc_ctrl [12]: presetn_uart0 [13]: presetn_wdt_lpmcu [14]: resetn_i2c2 [15]: resetn_lpmcu_full_cluster

PMU_GRF_SOC_CON5

Address: Operational Base(0x20130000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	pmucru_softrst_hold1 Each bit has a reset hold. [0]: resetn_lpmcu_only_core [1]: resetn_lpmcu_pwup [2]: resetn_pmu_32k_hp_timer [3]: resetn_pmu_hp_timer [4]: resetn_preroll_32k [5]: resetn_preroll [6]: resetn_pwm1 [7]: resetn_ref_rcosc_ctrl [8]: sresetn_uart0 [9]: tresetn_lpmcu_ijtag [10]: tresetn_wdt_lpmcu [11]: NA [12]: NA [13]: presetn_cru_spmu [14]: presetn_pmu_sgrf_remap [15]: presetn_pmu_sgrf

PMU_GRF_SOC_CON6

Address: Operational Base(0x20130000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	pmucru_softrst_hold2 Each bit has a reset hold. [0]: aresetn_lpdma [1]: hresetn_fspi1 [2]: hresetn_lpsai [3]: hresetn_pmu1_biu [4]: hresetn_spi2ahb [5]: hresetn_xip_fspi1 [6]: mresetn_audio_adc_pmu [7]: mresetn_lpsai [8]: presetn_aoa_aad [9]: presetn_aoa_apb [10]: presetn_aoa_fe [11]: presetn_aoa_sram [12]: presetn_aoa_tdd [13]: presetn_audio_adc_pmu [14]: presetn_cru_pmu1 [15]: presetn_ioc_pmuio1

PMU_GRF_SOC_CON7

Address: Operational Base(0x20130000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	pmucru_softrst_hold3 Each bit has a reset hold. [0]: presetn_lpdma [1]: presetn_spi2ahb [2]: sresetn_1x_fspi1 [3]: chiprstn_pd_pmu1

PMU_GRF_SOC_CON8

Address: Operational Base(0x20130000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x0000001f	grf_con_pmuio1_pwr_up_cnt_thresh PMUIO1 power_on timer counter. Multiplied with RC_OSC_div clock period.

PMU_GRF_SOC_CON9

Address: Operational Base(0x20130000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RW	0xffffffff	grf_con_aov_on_timeout_thresh AOV_on_timeout_thresh. Multiplied with RC_OSC_div clock period.

PMU_GRF_SOC_CON10

Address: Operational Base(0x20130000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	grf_con_aov_off_timeout_thresh AOV_off_timeout_thresh. Multiplied with 32K clock period.

PMU_GRF_SOC_CON11

Address: Operational Base(0x20130000) + offset (0x002C)

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Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	grf_con_aov_ldo_stable_cnt_threth LDO stable counter thresh. Multiplied with RC_OSC_div clock period.

PMU_GRF_SOC_CON12

Address: Operational Base(0x20130000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10	RW	0x0	grf_con_aov_info_tx_soft_en Enable AOV debug software information. 1'b0: Disable 1'b1: Enable
9	RW	0x0	grf_con_aov_info_tx_soft_sel Enable AOV debug information select. 1'b0: Preroll state 1'b1: Software state
8	RW	0x0	grf_con_aov_info_tx_en Enable AOV debug information transition. 1'b0: Disable 1'b1: Enable
7:0	RW	0x00	grf_con_aov_info_tx_intv_time The interval time between the bytes of AOV debug information.

PMU_GRF_SOC_CON13

Address: Operational Base(0x20130000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	grf_con_aov_info_tx_sft_con AOV debug software information

PMU_GRF_SOC_CON14

Address: Operational Base(0x20130000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	grf_con_aov_pmu1_pwr_ack_sel pd_pmu1_dwn_ack source selection when power down PD_PMU1 in AOV Mode. 1'b0: ACK from power switch 1'b1: ACK from pd_pmu1_dwn_req
14	RW	0x0	grf_con_aov_pmu1_noc_auto_con PD_PMU1 bus clock gating mask enable in AOV Mode. 1'b0: disable 1'b1: enable
13	RW	0x0	grf_con_aov_pmu1_bus_idle_sftcon PD_PMU1 bus idle enable in AOV Mode by software. 1'b0: disable 1'b1: enable

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Bit	Attr	Reset Value	Description
12	RW	0x0	grf_con_aov_pmu1_bus_idle_con PD_PMU1 bus idle enable in AOV Mode. 1'b0: disable 1'b1: enable
11	RW	0x0	grf_con_aov_pmu1_pwr_gate_sftcon Power down PD_PMU1 in AOV Mode by software. 1'b0: disable 1'b1: enable
10	RW	0x0	grf_con_aov_off_counter_start_sel 1'b0: AOV OFF counter start from fspi1_idle 1'b1: AOV OFF counter start from spi2ahb_idle
9	RW	0x0	grf_con_aov_off_counter_clr AOV OFF counter clear 1'b0: Disable 1'b1: Enable
8	RW	0x0	grf_con_aov_on_timeout_clr AOV ON state timeout clear 1'b0: Disable 1'b1: Enable
7	RW	0x0	grf_con_aov_st_idle_fspi1_bypass AOV_STATE wait idle_fspi1 bypass 1'b0: Disable 1'b1: Enable
6	RW	0x0	grf_con_aov_st_idle_spi2ahb_bypass AOV_STATE wait idle_spi2ahb bypass 1'b0: Disable 1'b1: Enable
5	RW	0x0	grf_con_aov_st_csn_spi2ahb_bypass AOV_STATE wait csn_spi2ahb bypass 1'b0: Disable 1'b1: Enable
4	RW	0x0	grf_con_aov_pmuio1_pwrdn_bypass AOV_STATE pmuio1 power down bypass 1'b0: Disable 1'b1: Enable
3	RW	0x0	grf_con_aov_pmu1_pwrdn_bypass AOV_STATE pd_pmu1 power down bypass 1'b0: Disable 1'b1: Enable
2	RW	0x0	grf_con_aov_pmu1_bus_idle_bypass AOV_STATE pd_pmu1 bus idle bypass 1'b0: Disable 1'b1: Enable
1	RW	0x0	grf_con_aov_mode AOV Mode. When enable, 1) The power down/up of pd_pmu1 will be controlled by AOV Mode, 2) IO_PWRctrl0 indicates pmuio1_pwr_up when output and indicates wifi_wakeup when input. 1'b0: Disable 1'b1: Enable
0	RW	0x0	grf_con_aov_en AOV Mode start enable 1'b0: Disable 1'b1: Enable

PMU_GRF_SOC_CON15

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Address: Operational Base(0x20130000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	grf_con_aov_on_timeout_check_en AOV ON timeout check enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	grf_con_aov_ldo_bypass AOV_STATE wait LDO stable bypass 1'b0: Disable 1'b1: Enable

PMU_GRF_AAD_CON0

Address: Operational Base(0x20130000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	grf_con_afe_mem_gate_en AFEMEM clock auto gating 1'b0: Disable 1'b1: Enable
0	RW	0x0	grf_con_aad_mem_gate_en AADMEM clock auto gating 1'b0: Disable 1'b1: Enable

PMU_GRF_MEN_CON0

Address: Operational Base(0x20130000) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:0	RW	0x000	grf_con_pmu_mem_cfg_sdp Pmu_mem SDP configuration.

PMU_GRF_MEN_CON1

Address: Operational Base(0x20130000) + offset (0x0144)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:0	RW	0x021	grf_con_adc_mem_cfg_sp ADC_mem SP configuration.

PMU_GRF_MEN_CON2

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Address: Operational Base(0x20130000) + offset (0x0148)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:0	RW	0x155	grf_con_adc_mem_cfg_rom ADC_mem ROM configuration.

PMU_GRF_SOC_SPECIAL0

Address: Operational Base(0x20130000) + offset (0x0150)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x1	grf_con_soc_test_mode_en soc_test_mode enable. Should be disabled when function mode and reset by NPOR. 1'b0: Disable 1'b1: Enable

PMU_GRF_SOC_AOV_INT_CON

Address: Operational Base(0x20130000) + offset (0x0160)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	int_aov_on_timeout_en AOV ON timeout interrupt enable 1'b0: Disable 1'b1: Enable
5	RW	0x0	int_aov_off_en AOV OFF interrupt enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	int_aov_on_en AOV ON interrupt enable 1'b0: Disable 1'b1: Enable
3	RO	0x0	reserved
2	RW	0x0	int_aov_on_timeout_clr AOV ON_Timeout interrupt clear bit 1'b0: Disable 1'b1: Enable
1	RW	0x0	int_aov_off_clr AOV OFF interrupt clear bit 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
0	RW	0x0	int_aov_on_clr AOV ON interrupt clear bit 1'b0: Disable 1'b1: Enable

PMU_GRF_SOC_STATUS0

Address: Operational Base(0x20130000) + offset (0x0170)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	pmu1_pwr_idle
29	RW	0x0	pmu1_pwr_idleack
28	RO	0x0	grf_st_standbywfil2 L2WFI status of CPU. 1'b0: Not WFI 1'b1: WFI
27:24	RO	0x0	grf_st_standbywfe WFE status of core. 1'b0: Not WFE 1'b1: WFE
23:20	RO	0x0	grf_st_standbywfi WFI status of core. 1'b0: Not WFI 1'b1: WFI
19:16	RO	0x0	grf_st_aov_state AOV state 4'b0000: IDLE state 4'b0001: AOV_ON state 4'b0010: WAIT_SPI2AHB_IDLE state 4'b0011: WAIT_FSPI1_IDLE state 4'b0100: POWER_DOWN_PD_PMU1 state 4'b0101: POWER_DOWN_PMUIO1 state 4'b0110: AOV_OFF state 4'b0111: POWER_UP_PMUIO1 state 4'b1000: POWER_UP_PD_PMU1 state
15	RW	0x0	pmuio1_pwr_down
14	RW	0x0	pd_pmu1_dwn_ack
13	RO	0x1	fspi1_idle IDLE statu of fspi1 1'b0: Busy 1'b1: IDLE
12	RO	0x1	spi2ahb_idle IDLE statu of spi2ahb 1'b0: Busy 1'b1: IDLE
11:10	RO	0x0	reserved
9	RO	0x0	grf_st_pmu_mcu_wfi_halted Indicates that the processor is in debug state. HALTED remains asserted for as long as the processor remains in debug state.
8	RO	0x0	grf_st_pmu_mcu_rst_n_out Indicates the Reset signal for system controlled by Debug Module
7	RO	0x0	reserved
6	RO	0x0	grf_st_aov_on_timeout Indicates that the AOV mode ON_status timeout

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Bit	Attr	Reset Value	Description
5	RO	0x0	grf_st_aov_off Indicates that the AOV mode is OFF_status
4	RO	0x0	grf_st_aov_on Indicates that the AOV mode is ON_status
3:1	RO	0x0	reserved
0	RO	0x0	rknpor_powergood rknpor_powergood status

PMU_GRF_SOC_STATUS1
Address: Operational Base(0x20130000) + offset (0x0174)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	grf_st_aov_on_timer_cnt AOV ON timer counter.

PMU_GRF_SOC_STATUS2
Address: Operational Base(0x20130000) + offset (0x0178)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	grf_st_aov_off_timer_cnt AOV OFF timer counter.

PMU_GRF_OS_REG0
Address: Operational Base(0x20130000) + offset (0x0200)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_os_reg0 OS register

PMU_GRF_OS_REG1
Address: Operational Base(0x20130000) + offset (0x0204)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_os_reg1 OS register

PMU_GRF_OS_REG2
Address: Operational Base(0x20130000) + offset (0x0208)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_os_reg2 OS register

PMU_GRF_OS_REG3
Address: Operational Base(0x20130000) + offset (0x020C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_os_reg3 OS register

PMU_GRF_OS_REG4
Address: Operational Base(0x20130000) + offset (0x0210)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_os_reg4 OS register

PMU_GRF_OS_REG5
Address: Operational Base(0x20130000) + offset (0x0214)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_os_reg5 OS register

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PMU_GRF_OS_REG6
Address: Operational Base(0x20130000) + offset (0x0218)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_os_reg6 OS register

PMU_GRF_OS_REG7
Address: Operational Base(0x20130000) + offset (0x021C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_os_reg7 OS register

PMU_GRF_OS_REG8
Address: Operational Base(0x20130000) + offset (0x0220)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_os_reg8 OS register, once this reg is wrotten, it can't be reset

PMU_GRF_OS_REG9
Address: Operational Base(0x20130000) + offset (0x0224)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_os_reg9 OS register, once this reg is wrotten, it can't be reset

PMU_GRF_OS_REG10
Address: Operational Base(0x20130000) + offset (0x0228)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_os_reg10 OS register, once this reg is wrotten, it can't be reset

PMU_GRF_OS_REG11
Address: Operational Base(0x20130000) + offset (0x022C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_os_reg11 OS register, once this reg is wrotten, it can't be reset

PMU_GRF_RESET_FUNCTION_STATUS
Address: Operational Base(0x20130000) + offset (0x0230)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RO	0x0	tsadc_shut_reset_src Reset by tsadc shut trigger
1	RO	0x0	wdt_reset_src Reset by wdt trigger
0	RO	0x0	first_reset_src Reset by first reset trigger

PMU_GRF_RESET_FUNCTION_CLR
Address: Operational Base(0x20130000) + offset (0x0234)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	WO	0x0	tsadc_shut_reset_src_clr Clear bit for reset by tsadc shut trigger 1'b1: Clear enable 1'b0: Clear disable

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Bit	Attr	Reset Value	Description
1	WO	0x0	wdt_reset_src_clr Clear bit for reset by wdt trigger 1'b1: Clear enable 1'b0: Clear disable
0	WO	0x0	first_reset_src_clr Clear bit for reset by first reset trigger 1'b1: Clear enable 1'b0: Clear disable

PMU_GRF_SIG_DETECT_CON

Address: Operational Base(0x20130000) + offset (0x0380)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0:Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	sdmmc0_detectn_neg_irq_msk Enable sdmmc0 detectn negedge irq 1'b0: Disable 1'b1: Enable
0	RW	0x0	sdmmc0_detectn_pos_irq_msk Enable sdmmc0 detectn posedge irq 1'b0: Disable 1'b1: Enable

PMU_GRF_SIG_DETECT_STATUS

Address: Operational Base(0x20130000) + offset (0x0390)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	sdmmc0_detectn_neg_irq 1'b1: Irq asserted; 1'b0: No irq
0	RO	0x0	sdmmc0_detectn_pos_irq 1'b1: Irq asserted; 1'b0: No irq

PMU_GRF_SIG_DETECT_STATUS_CLEAR

Address: Operational Base(0x20130000) + offset (0x03A0)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	WO	0x0	sdmmc0_detectn_neg_irq_clr 1'b1: Clear irq
0	WO	0x0	sdmmc0_detectn_pos_irq_clr 1'b1: Clear irq

PMU_GRF_SDMMC_DET_COUNTER

Address: Operational Base(0x20130000) + offset (0x03B0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x003e8	sdmmc_detectn_count sdmmc_detectn_count bit register

4.8 DDR GRF Register Description

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4.8.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

4.8.2 Registers Summary

Name	Offset	Size	Reset Value	Description
DDR_GRF_CON0	0x0000	W	0x00000000	DDR Control Register0
DDR_GRF_CON1	0x0004	W	0x00000600	DDR Control Register1
DDR_GRF_CON4	0x0010	W	0x00000000	DDR Control Register4
DDR_GRF_CON12	0x0030	W	0x00000000	DDR Control Register12
DDR_GRF_CON13	0x0034	W	0x00000000	DDR Control Register13
DDR_GRF_CON14	0x0038	W	0x00000000	DDR Control Register14
DDR_GRF_CON15	0x003C	W	0x00000000	DDR Control Register15
DDR_GRF_CON16	0x0040	W	0x00000000	DDR Control Register16
DDR_GRF_CON17	0x0044	W	0x00000000	DDR Control Register17
DDR_GRF_CON18	0x0048	W	0x00000000	DDR Control Register18
DDR_GRF_CON20	0x0050	W	0x00000400	DDR Control Register20
DDR_GRF_CON21	0x0054	W	0x00000000	DDR Control Register21
DDR_GRF_CON22	0x0058	W	0x00000390	DDR Control Register22
DDR_GRF_CON23	0x005C	W	0x00000000	DDR Control Register23
DDR_GRF_PROBE_CTRL	0x0080	W	0x00000000	PROBE Control Register
DDR_GRF_STATUS0	0x0100	W	0x00000000	DDR Status Register0
DDR_GRF_STATUS1	0x0104	W	0x00000000	DDR Status Register1
DDR_GRF_STATUS2	0x0108	W	0x00000000	DDR Status Register2
DDR_GRF_STATUS3	0x010C	W	0x00000000	DDR Status Register3
DDR_GRF_STATUS4	0x0110	W	0x00000000	DDR Status Register4
DDR_GRF_STATUS5	0x0114	W	0x00000000	DDR Status Register5
DDR_GRF_STATUS6	0x0118	W	0x00000000	DDR Status Register6
DDR_GRF_STATUS7	0x011C	W	0x00000000	DDR Status Register7
DDR_GRF_STATUS8	0x0120	W	0x00000000	DDR Status Register8
DDR_GRF_STATUS9	0x0124	W	0x00000000	DDR Status Register9
DDR_GRF_STATUS10	0x0128	W	0x00000000	DDR Status Register10
DDR_GRF_STATUS11	0x012C	W	0x00000000	DDR Status Register11
DDR_GRF_STATUS12	0x0130	W	0x00000000	DDR Status Register12
DDR_GRF_STATUS13	0x0134	W	0x00000000	DDR Status Register13
DDR_GRF_STATUS14	0x0138	W	0x00000000	DDR Status Register14
DDR_GRF_STATUS15	0x013C	W	0x00000000	DDR Status Register15
DDR_GRF_STATUS16	0x0140	W	0x0FF007FB	DDR Status Register16
DDR_GRF_STATUS17	0x0144	W	0x00401F21	DDR Status Register17
DDR_GRF_STATUS19	0x014C	W	0x00000000	DDR Status Register19
DDR_GRF_STATUS30	0x0178	W	0x00000000	DDR Status Register30

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

4.8.3 Detail Registers Description

DDR_GRF_CON0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:8	RW	0x0	ddrctl_axi_cg_en DDRCTL AXI port 0~3 aclk gate enable. Bit 0 is for DDRCTL AXI port 0, bit 1 is for DDRCTL AXI port 1 and so on. 1'b0: Disable 1'b1: Enable DDRCTL AXI auto gate
7:4	RO	0x0	reserved
3	RW	0x0	dfi_init_complete Value of dfi_init_complete
2	RW	0x0	dfi_init_complete_sel DDRCTL dfi_init_complete select 1'b0: DDRCTL dfi_init_complete is driven by DDRPHY 1'b1: DDRCTL dfi_init_complete is driven by DDR_GRF
1	RW	0x0	dfi_init_start Value of dfi_init_start
0	RW	0x0	dfi_init_start_sel DDRPHY dfi_init_start select 1'b0: DDRPHY dfi_init_start is driven by DDRCTL 1'b1: DDRPHY dfi_init_start is driven by DDR_GRF

DDR_GRF_CON1

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	ddrctl_apb_pclk_cg_en DDRCTL APB interface pclk clock gate enable 1'b0: Disable 1'b1: Enable
14:12	RO	0x0	reserved
11:8	RW	0x6	auto_sr_dly When SDRAM is in self-refresh state indicated by selfref_type2_en, the core clk of DDRCTL will be gated after auto_sr_dly clocks.
7	RO	0x0	reserved
6	RW	0x0	ddrctl_mem_cg_en DDRCTL memory clock gate enable 1'b0: Disable 1'b1: Enable
5	RO	0x0	reserved
4	RW	0x0	ddrctl_syscreq_cg_en DDRCTL core clock gate enable during SR-PD 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3	RW	0x0	selfref_type2_en DDRCTL self-refresh type for auto gate 1'b0: SDRAM is in SR-Powerdown (LPDDR4/5), which was caused by automatic self refresh only. If retry is enabled, this guarantees SRE command is executed correctly without parity error. 1'b1: SDRAM is in SR-Powerdown (LPDDR4/5), which was not caused solely under automatic self refresh control. It could have been caused by hardware low power interface and/or software (PWRCTL.selfref_sw). If retry is enabled, this guarantees SRE command is executed correctly without parity error.
2	RW	0x0	ddrctl_core_cg_en DDRCTL core clock gate enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	ddrctl_apb_cg_en DDRCTL AXI port 0~3 aclk gate enable mode. This register is valid only when ddrctl_axi_cg_en is none zero. 1'b0: The DDRCTL AXI port aclk will be gated and ignores the status of DDRCTL APB slave interface. 1'b1: The DDRCTL AXI port aclk will be ungated when the APB slave interface of DDRCTL is active.
0	RO	0x0	reserved

DDR_GRF_CON4

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	awpoison DDRCTL AXI port 0~3 write address poison. Bit 0 is for DDRCTL AXI port 0, bit 1 is for DDRCTL AXI port 1 and so on. 1'b0: Disable 1'b1: Enable poison on write command
23:20	RO	0x0	reserved
19:16	RW	0x0	arpoison DDRCTL AXI port 0~3 read address poison. Bit 0 is for DDRCTL AXI port 0, bit 1 is for DDRCTL AXI port 1 and so on. 1'b0: Disable 1'b1: Enable poison on read command
15:12	RO	0x0	reserved
11:8	RW	0x0	awautopre DDRCTL AXI port 0~3 auto-precharge signal for write command. This register should be keep 1'b0 for each AXI port. Bit 0 is for DDRCTL AXI port 0, bit 1 is for DDRCTL AXI port 1 and so on.
7:4	RO	0x0	reserved
3:0	RW	0x0	arautopre DDRCTL AXI port 0~3 auto-precharge signal for read command. This register should be keep 1'b0 for each AXI port. Bit 0 is for DDRCTL AXI port 0, bit 1 is for DDRCTL AXI port 1 and so on.

DDR_GRF_CON12

Address: Operational Base + offset (0x0030)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x00	hpr_entry_num The HPR entry numbers that used to make write command go to critical when wr_mask_by_hpr is set to 1'b1. If wr_mask_by_hpr is set to 1'b0, hpr_entry_num is not used.
7:5	RO	0x0	reserved
4	RW	0x0	wr_mask_by_hpr If set to 1, when the HPR is not empty, it will prevents awurgent from triggering go2critical_wr. Thus the HPR requests are less likely to be blocked by write requests.
3	RW	0x0	rrbtoken_empty2critical 1'b0: The DDRCTL read CAM will not go to critical state when rrb token is empty. When the RRB token is empty, the PA cannot arbitrate to the read request, and the priority mechanism of the read request may be invalidated. 1'b1: The DDRCTL read CAM will go to critical state when rrb read token is empty. So that the read CAM is prioritized for scheduling, and the PA recovers the arbitration ability of read requests as soon as possible.
2	RW	0x0	wr_full2critical 1'b0: The DDRCTL WR CAM will go to critical state when awurgent assert. 1'b1: The DDRCTL WR CAM will go to critical state when awurgent assert and WR credits are empty simultaneously.
1	RW	0x0	hpr_full2critical 1'b0: The DDRCTL HPR will go to critical state when arurgent assert. 1'b1: The DDRCTL HPR will go to critical state when arurgent assert and HPR credits are empty simultaneously. It is strongly recommended to set hpr_full2critical=0, otherwise unexpected situations may occur.
0	RW	0x0	lpr_full2critical 1'b0: The DDRCTL LPR will go to critical state when arurgent assert. 1'b1: The DDRCTL LPR will go to critical state when arurgent assert and LPR credits are empty simultaneously.

DDR_GRF_CON13

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:8	RW	0x0	awqos_urgent_en Enable the urgent mechanism of DDRCTL's AXI write port 0~3 according to the Awqos. Each bit is corresponding to DDRCTL's AXI write port 0~3 respectively. For example, awqos_urgent_en[0] is used to enable AXI write port 0, awqos_urgent_en[1] is used to enable AXI write port 1 and so on. 1'b0: Disable 1'b1: Enable
7:4	RO	0x0	reserved
3:0	RW	0x0	arqos_urgent_en Enable the urgent mechanism of DDRCTL's AXI read port 0~3 according to the Arqos. Each bit is corresponding to DDRCTL's AXI read port 0~3 respectively. For example, arqos_urgent_en[0] is used to enable AXI read port 0, arqos_urgent_en[1] is used to enable AXI read port 1 and so on. 1'b0: Disable 1'b1: Enable

DDR_GRF_CON14

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	press_aw_th Qos/Press threshold for wite requests. The awugent may assert only when press (qos) > grf_press_aw_th. The press_aw_th[2:0] set the threshold for AXI write port 0. The press_aw_th[5:3] set the threshold for AXI write port 1, and so on.
15:0	RW	0x0000	press_ar_th Qos/Press threshold for read requests. The arugent may assert only when press (qos) > grf_press_ar_th. The press_ar_th[2:0] set the threshold for AXI read port 0. The press_ar_th[5:3] set the threshold for AXI read port 1, and so on.

DDR_GRF_CON15

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	press_en_aw Hold the awurguent always active when press[2:0] >= 3'h6, high active. Each bit is corresponding to DDRCTL's AXI port 0~3 respectively.
11:8	RW	0x0	press_cg_en Clock gate enable of DDRCTL's urgent control module. Each bit is corresponding to DDRCTL's AXI port 0~3 respectively. 1'b0: Disable 1'b1: Enable If the DDRCTL's urgent control module is not used, please set press_cg_en[4:0] to 5'h1f to save power.

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	press_en_ar Hold the arurguent always active when press[2:0] >= 3'h6, high active. Each bit is corresponding to DDRCTL's AXI port 0~3 respectively.
3:0	RW	0x0	press_en Urgent control function enable for DDRCTL's AXI port 0~3. Each bit is corresponding to DDRCTL's AXI port 0~3 respectively. For example, press_en[0] is used to control AXI port 0, press_en[1] is used to control AXI port 1 and so on. 1'b0: Disable 1'b1: Enable

DDR_GRF_CON16

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:8	RW	0x0	press_rdwr_order Read/write order enable of DDRCTL's urgent control module. Each bit is corresponding to DDRCTL's AXI port 0~3 respectively. For example, press_rdwr_order[0] is used to control AXI port 0, press_rdwr_order[1] is used to control AXI port 1 and so on.
7	RO	0x0	reserved
6:2	RW	0x00	press_queue_wait_limit The QOS may trigger urgent only when the request with high QOS in the queue is not poped for press_queue_wait_limit*4 cycles.
1:0	RW	0x0	press_policy Bit[0]: 1'b0: The arurgent and awurgent will not assert simultaneously. 1'b1: The arurgent and awurgent may assert simultaneously. Bit[1]: 1'b0: The QOS queue pops once when the queue in DDRCTL pops. 1'b1: The QOS queue pops once when the queue in DDRCTL pops and is arbitrated by the PA.

DDR_GRF_CON17

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	pa_rmask_en The DDRCTL's PA(Port Arbitar) read mask enable. Only even bits are used, odd bits are ignored. For example, pa_rmask_en[0]/[2]/[4]/[6]/[8] is used to control DDRCTL AXI read port 0/1/2/3/4. If enabled, read commands from that AXI read port are not arbitared and are blocked in read address FIFO. 1'b0: Disable 1'b1: Enable

DDR_GRF_CON18

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3:0	RW	0x0	pa_wmask_en The DDRCTL's PA(Port Arbitar) write mask enable. Each bit is corresponding to DDRCTL's AXI write port 0~3. For example, pa_wmask_en[0] is used to enable the write port mask function for DDRCTL's AXI write port 0. 1'b0: Disable 1'b1: Enable

DDR_GRF_CON20

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10	RW	0x1	dfi_clk_gate_en_mask dfi clk auto gate mask. 1'b0: dfi clock auto gating enable; 1'b1: dfi clock auto gating disable.
9	RW	0x0	ddrctl_aclk_auto_gate_enable ddrc aclk auto gate by noc signal.
8	RW	0x0	dfi_phymstr_state_sel dfi phymaster state sel
7:6	RW	0x0	dfi_phymstr_type dfi phymaster type
5:4	RW	0x0	dfi_phymstr_cs_state dfi phymaster cs state
3:2	RO	0x0	reserved
1	RW	0x0	ddrmon_external_trigger_en 1'b0: Disable 1'b1: Enable
0	RW	0x0	ddrctl_slverr_enable DDRCTL slave APB error response enable 1'b0: Disable DDRCTL from responding error 1'b1: Enable DDRCTL from responding error

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DDR_GRF_CON21
Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	noc_axi_rddata_sel 1'b0: AXI rdata channel pipe added between NOC and DDRC; 1'b1: AXI rdata send to NOC from DDRC directely.
12	RW	0x0	csysreq_ddrc_pmu 1'b0: The hardware low power request signal of ddrc, cysreq_ddrc, is not related to PMU. 1'b1: The hardware low power request signal of ddrc, cysreq_ddrc, can be generated by PMU.
11	RW	0x0	csysreq_aclk_ddrsh3_vi_grf Select AXI port3 csysreq signal source from GRF or masked. 1'b0: GRF csysreq aclk masked; 1'b1: GRF csysreq aclk selected;
10	RW	0x0	csysreq_aclk_ddrsh2_poe_grf Select AXI port2 csysreq signal source from GRF or masked. 1'b0: GRF csysreq aclk masked; 1'b1: GRF csysreq aclk selected;
9	RW	0x0	csysreq_aclk_ddrsh1_npu_grf Select AXI port1 csysreq signal source from GRF or masked. 1'b0: GRF csysreq aclk masked; 1'b1: GRF csysreq aclk selected;
8	RW	0x0	csysreq_aclk_ddrsh0_cpu_grf Select AXI port0 csysreq signal source from GRF or masked. 1'b0: GRF csysreq aclk masked; 1'b1: GRF csysreq aclk selected;
7	RW	0x0	csysreq_aclk_ddrsh3_vi_pmu Select AXI port3 csysreq signal source from PMU or masked. 1'b0: PMU csysreq aclk masked; 1'b1: PMU csysreq aclk selected;
6	RW	0x0	csysreq_aclk_ddrsh2_poe_pmu Select AXI port2 csysreq signal source from PMU or masked. 1'b0: PMU csysreq aclk masked; 1'b1: PMU csysreq aclk selected;
5	RW	0x0	csysreq_aclk_ddrsh1_npu_pmu Select AXI port1 csysreq signal source from PMU or masked. 1'b0: PMU csysreq aclk masked; 1'b1: PMU csysreq aclk selected;
4	RW	0x0	csysreq_aclk_ddrsh0_cpu_pmu Select AXI port0 csysreq signal source from PMU or masked. 1'b0: PMU csysreq aclk masked; 1'b1: PMU csysreq aclk selected;
3	RW	0x0	csysreq_aclk_ddrsh3_vi As one of csysreq_aclk_ddrsh3_vi source, when select csysreq aclk control from DDR_GRF.
2	RW	0x0	csysreq_aclk_ddrsh2_poe As one of csysreq_aclk_ddrsh2_poe source, when select csysreq aclk control from DDR_GRF.

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Bit	Attr	Reset Value	Description
1	RW	0x0	csysreq_aclk_ddrsh1_npu As one of csysreq_aclk_ddrsh1_npu source, when select csysreq aclk control from DDR_GRF.
0	RW	0x0	csysreq_aclk_ddrsh0_cpu As one of csysreq_aclk_ddrsh0_cpu source, when select csysreq aclk control from DDR_GRF.

DDR_GRF_CON22

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9:8	RW	0x3	dq_swap_sel3 The 4*N+3 byte swap select
7:6	RW	0x2	dq_swap_sel2 The 4*N+2 byte swap select
5:4	RW	0x1	dq_swap_sel1 The 4*N+1 byte swap select
3:2	RW	0x0	dq_swap_sel0 The 4*N byte swap select
1	RO	0x0	reserved
0	RW	0x0	dq_swap_en dq swap enable

DDR_GRF_CON23

Address: Operational Base + offset (0x005C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	sys_mem_cfg system mem cfg

DDR_GRF_PROBE_CTRL

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	vi_port3_probe vi port3 probe mainstatsuspend.
2	RW	0x0	poe_port2_probe poe port2 probe mainstatsuspend.
1	RW	0x0	npu_port1_probe npu port1 probe mainstatsuspend.
0	RW	0x0	cpu_port0_probe cpu port0 probe mainstatsuspend.

DDR_GRF_STATUS0

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Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	st_mrr_data0_32 MRR data from DDRCTL

DDR_GRF_STATUS1

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	st_mrr_data0_64 MRR data from DDRCTL

DDR_GRF_STATUS2

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	st_mrr_data0_96 MRR data from DDRCTL

DDR_GRF_STATUS3

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	st_mrr_data0_128 MRR data from DDRCTL

DDR_GRF_STATUS4

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	st_mrr_data1_32 MRR data from DDRCTL

DDR_GRF_STATUS5

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	st_mrr_data1_64 MRR data from DDRCTL

DDR_GRF_STATUS6

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	st_mrr_data1_96 MRR data from DDRCTL

DDR_GRF_STATUS7

Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	st_mrr_data1_128 MRR data from DDRCTL

DDR_GRF_STATUS8

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	st_mrr_data2_32 MRR data from DDRCTL

DDR_GRF_STATUS9

Address: Operational Base + offset (0x0124)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	st_mrr_data2_64 MRR data from DDRCTL

DDR_GRF_STATUS10
Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	st_mrr_data2_96 MRR data from DDRCTL

DDR_GRF_STATUS11
Address: Operational Base + offset (0x012C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	st_mrr_data2_128 MRR data from DDRCTL

DDR_GRF_STATUS12
Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	st_mrr_data3_32 MRR data from DDRCTL

DDR_GRF_STATUS13
Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	st_mrr_data3_64 MRR data from DDRCTL

DDR_GRF_STATUS14
Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	st_mrr_data3_96 MRR data from DDRCTL

DDR_GRF_STATUS15
Address: Operational Base + offset (0x013C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	st_mrr_data3_128 MRR data from DDRCTL

DDR_GRF_STATUS16
Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RO	0x1	bready_3 bready_3 signal status of DDRCTL AXI write port 3.
26	RO	0x1	bready_2 bready_2 signal status of DDRCTL AXI write port 2.
25	RO	0x1	bready_1 bready_1 signal status of DDRCTL AXI write port 1.
24	RO	0x1	bready_0 bready_0 signal status of DDRCTL AXI write port 0.
23	RO	0x1	rready_3 rready_3 signal status of DDRCTL AXI read port 3.
22	RO	0x1	rready_2 rready_2 signal status of DDRCTL AXI read port 2.

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Bit	Attr	Reset Value	Description
21	RO	0x1	rready_1 rready_1 signal status of DDRCTL AXI read port 1.
20	RO	0x1	rready_0 rready_0 signal status of DDRCTL AXI read port 0.
19:18	RO	0x0	st_stat_ddrc_reg_selfref_type DDRCTL selfrefresh type status Flags if SR-Powerdown is entered and if it was under automatic self refresh control only or not. 2'b00: SDRAM is not in SR-Powerdown. 2'b01: SDRAM is in self refresh, which was caused by PHY master request. 2'b10: SDRAM is in SR-Powerdown, which was not caused solely under automatic self refresh control. 2'b11: SDRAM is in SR-Powerdown, which was caused by automatic self refresh only.
17:15	RO	0x0	reserved
14:11	RO	0x0	st_cactive_aclk DDRCTL aclk cactive status. Bit 0 is corresponding to AXI port 0, bit 1 is corresponding to AXI port 1 and so on. 1'b0: Not active 1'b1: Active
10:7	RO	0xf	st_csysack_aclk DDRCTL aclk csysack status. Bit 0 is corresponding to AXI port 0, bit 1 is corresponding to AXI port 1 and so on. 1'b0: Low power request is acknowledged. 1'b1: Low power request is not acknowledged.
6:3	RO	0xf	st_csysreq_aclk DDRCTL aclk csysreq status. Bit 0 is corresponding to AXI port 0, bit 1 is corresponding to AXI port 1 and so on. 1'b0: Low power request 1'b1: No low power request
2	RO	0x0	st_cactive_ddrc DDRCTL core cactive status 1'b0: Not active 1'b1: Active
1	RO	0x1	st_csysack_ddrc DDRCTL core low power ack status 1'b0: Low power request is acknowledged. 1'b1: Low power request is not acknowledged.
0	RO	0x1	st_csysreq_ddrc DDRCTL core low power request status 1'b0: Low power request. 1'b1: No low power request.

DDR_GRF_STATUS17

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:16	RO	0x40	st_wr_credit_cnt DDRCTL wr credit count
15	RO	0x0	reserved
14:8	RO	0x1f	st_hpr_credit_cnt DDRCTL hpr credit count
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:0	RO	0x21	st_lpr_credit_cnt DDRCTL lpr credit count

DDR_GRF_STATUS19
Address: Operational Base + offset (0x014C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x0	st_derate_temp_limit_intr_fault This signal is the derate temperature limit fault. This is a version of derate_temp_limit_intr, which can not be disabled or forced via a register. It is a 2-bit antivalent signal with encoding as follows: 2'b01: No Fault 2'b10: Fault Detected
7:6	RO	0x0	reserved
5:0	RO	0x00	st_hif_refresh_req_bank This signal indicates the next bank that is refreshed; for multi-rank configurations, the bank number is reported independently for each rank, and the information for all ranks is concatenated to form this signal.

DDR_GRF_STATUS30
Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	dfi_clk_gate_en dfi clock auto gating en, generate by DDRC
14	RO	0x0	vi_port3_probe_linkPwrActive dtp_subddrLKvi_pwrDiscTarg_vi_probe_linkPwrActive
13	RO	0x0	poe_port2_probe_linkPwrActive dtp_subddrLKpoe_pwrDiscTarg_poe_probe_linkPwrActive
12	RO	0x0	npu_port1_probe_linkPwrActive dtp_subddrLKnpu_pwrDiscTarg_npu_probe_linkPwrActive
11	RO	0x0	cpu_port0_probe_linkPwrActive dtp_subddrLKcpu_pwrDiscTarg_cpu_probe_linkPwrActive
10	RO	0x0	vi_port3_probe_mainTraceAlarm vi_port3_probe_mainTraceAlarm
9	RO	0x0	vi_port3_probe_mainStatAlarm vi_port3_probe_mainStatAlarm
8	RO	0x0	poe_port2_probe_mainTraceAlarm poe_port2_probe_mainTraceAlarm
7	RO	0x0	poe_port2_probe_mainStatAlarm poe_port2_probe_mainStatAlarm
6	RO	0x0	npu_port1_probe_mainTraceAlarm npu_port1_probe_mainTraceAlarm
5	RO	0x0	npu_port1_probe_mainStatAlarm npu_port1_probe_mainStatAlarm
4	RO	0x0	cpu_port0_probe_mainTraceAlarm cpu_port0_probe_mainTraceAlarm
3	RO	0x0	cpu_port0_probe_mainStatAlarm cpu_port0_probe_mainStatAlarm
2	RO	0x0	dtp_ddrfwLKdcPwrActive dtp_cfgddrLKfw_pwrDiscTarg_ddrfwLKdcPwrActive
1	RO	0x0	ddrctl_idle ddr controller idle state

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Bit	Attr	Reset Value	Description
0	RO	0x0	ddrphy_pll_lock ddrphy pll lock

4.9 VI GRF Register Description

4.9.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

4.9.2 Registers Summary

Name	Offset	Size	Reset Value	Description
VI_GRF_MEM_CON_SPRA	0x0000	W	0x00000021	VI single memory configuration
VI_GRF_MEM_CON_DPRA	0x0004	W	0x00000000	VI dual-port memory config register
VI_GRF_VI_GRF_STATUS	0x0008	W	0x000003F8	VI status register
VI_GRF_CSIPHY0_GRF_CON	0x0010	W	0x00000000	VI csiphy0 config register
VI_GRF_CSIPHY1_GRF_CON	0x0014	W	0x00000000	VI csiphy1 config register
VI_GRF_CSIPHY0_GRF_STATUS	0x0018	W	0x00000000	VI csiphy0 status register
VI_GRF_CSIPHY1_GRF_STATUS	0x001C	W	0x00000000	VI csiphy1 status register
VI_GRF_MISC_GRF_CON	0x0020	W	0x00000000	VI misc control register
VI_GRF_GMAC_GRF_CON0	0x0050	W	0x00000000	VI gmac config register 0
VI_GRF_GMAC_DMA_ACK	0x0054	W	0x00000000	VI gmac dma ack register
VI_GRF_GMAC_GRF_STATUS0	0x0060	W	0x00000000	VI gmac status register0
VI_GRF_GMAC_GRF_STATUS1	0x0064	W	0x00000000	VI gmac status register1
VI_GRF_GMAC_GRF_STATUS2	0x0068	W	0x00000000	VI gmac status register2
VI_GRF_SARADC1_GRF_CON0	0x0080	W	0x00000031	VI saradc1 config register 0
VI_GRF_SARADC1_GRF_CON1	0x0084	W	0x00000000	VI saradc1 config register 1
VI_GRF_SARADC1_GRF_CON2	0x0088	W	0x0000052F	VI saradc1 config register 2
VI_GRF_SARADC2_GRF_CON0	0x0090	W	0x00000031	VI saradc2 config register 0
VI_GRF_SARADC2_GRF_CON1	0x0094	W	0x00000000	VI saradc2 config register 1
VI_GRF_SARADC2_GRF_CON2	0x0098	W	0x0000052F	VI saradc2 config register 2
VI_GRF_RKMACPHY_GRF_CON0	0x00B4	W	0x00000000	VI rkmacphy config register 0
VI_GRF_RKMACPHY_GRF_CON1	0x00B8	W	0x00000000	VI rkmacphy config register 1
VI_GRF_RKMACPHY_GRF_CON2	0x00BC	W	0x00000000	VI rkmacphy config register 2
VI_GRF_RKMACPHY_GRF_STATUS	0x00C0	W	0x00000000	VI rkmacphy status register
VI_GRF_RKMACPHY_CALIB_CON	0x00C4	W	0x00000000	VI rkmacphy calib config register

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

4.9.3 Detail Registers Description

VI_GRF_MEM_CON_SPRA

Address: Operational Base(0x20150000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bit, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:10	RW	0x0	wtsel_hvt_mux4 Configuration for wtsel mux4 type for memory for VI.
9:8	RW	0x0	rtsel_hvt_mux4 Configuration for rtsel mux4 type for memory for VI.

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Bit	Attr	Reset Value	Description
7:6	RW	0x0	wtsel_hvt_mux1ormux2 Configuration for wtsel mux1ormux2 mem type for memory for VI.
5:4	RW	0x2	rtsel_hvt_mux1ormux2 Configuration for wtsel mux1ormux2 mem type for memory for VI.
3:2	RW	0x0	wtsel_svt Configuration for rtsel mux1ormux2 mem type for memory for VI. We only use the hvt.
1:0	RW	0x1	rtsel_svt Configuration for rtsel mux1ormux2 mem type for memory for VI. We only use the hvt.

VI_GRF_MEM_CON_DPRA

Address: Operational Base(0x20150000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5:4	RW	0x0	rtsel VI memory configuration. 2'b00: Recommended setting with the optimized read margin. 2'b01: Relaxed read margin setting, used for debugging purpose. 2'b10: More relaxed read margin setting, used for debugging purpose. 2'b11: Most relaxed read margin setting, used for debugging purpose.
3:2	RW	0x0	wtsel VI memory configuration. 2'b00: Recommended setting with the optimized write margin. 2'b01: Relaxed write margin setting, used for debugging purpose. 2'b10: More relaxed write margin setting, used for debugging purpose. 2'b11: Most relaxed write margin setting, used for debugging purpose.
1:0	RW	0x0	ptsel VI memory configuration. Setting for internal clock skew of port A/B with the optimized design margin and timming. 2'b00: Recommended value. 2'b01: Relaxed setting for internal clock skew of port A/B used for debugging purpose. 2'b10: More Relaxed setting for internal clock skew of port A/B used for debugging purpose. 2'b11: Most Relaxed setting for internal clock skew of port A/B used for debugging purpose.

VI_GRF_VI_GRF_STATUS

Address: Operational Base(0x20150000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RO	0x1	vicap_a_idle vicap idle state, idle in aclk
8	RO	0x1	vicap_isp_c_idle vicap idle state, idle in isp0_clk
7	RO	0x1	vpsl_a_idle vpsl idle state, idle in aclk
6	RO	0x1	vpss_a_idle vpss idle state, idle in aclk
5	RO	0x1	vpss_c_idle vpss idle state, idle in core_clk
4	RO	0x1	isp_a_idle isp idle state, idle in aclk
3	RO	0x1	isp_c_idle isp idle state, idle in core_clk
2	RO	0x0	isp_flash_trig Hold signal for flash light
1	RO	0x0	isp_prelight_trig Hold signal for prelight
0	RO	0x0	reserved

VI_GRF_CSIPHY0_GRF_CON

Address: Operational Base(0x20150000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	rxbyteclkhs_1_inv_sel It is used to select invert rxbyteclkhs_1.
10	RW	0x0	enable_ck_1 D-PHY clk lane1 enable signal
9	RW	0x0	rxbyteclkhs_0_inv_sel It is used to select invert rxbyteclkhs.
8	RW	0x0	enable_ck D-PHY clk lane enable signal, high active
7:4	RW	0x0	lane_enable Enable lane module, This active high signal forces the lane module out of shutdown.
3:0	RW	0x0	force_rx_mode Force lane module into receive mode/wait for stop state.

VI_GRF_CSIPHY1_GRF_CON

Address: Operational Base(0x20150000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	rxbyteclkhs_1_inv_sel It is used to select invert rxbyteclkhs_1.
10	RW	0x0	enable_ck_1 D-PHY clk lane1 enable signal

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Bit	Attr	Reset Value	Description
9	RW	0x0	rxbyteclkhs_0_inv_sel It is used to select invert rxbyteclkhs.
8	RW	0x0	enable_ck D-PHY clk lane enable signal, high active
7:4	RW	0x0	lane_enable Enable lane module, This active high signal forces the lane module out of shutdown.
3:0	RW	0x0	force_rx_mode Force lane module into receive mode/wait for stop state.

VI_GRF_CSIPHY0_GRF_STATUS

Address: Operational Base(0x20150000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:19	RO	0x0	csiphy_err_control Contorl error This active high signal is asserted when an incorrect line state sequence is detected. For example, if a turnaround request or escape mode request is immediately followed by a Stop state instead of the required Bridge state, this signal is asserted and remains asserted until the next change in line state
18	RO	0x0	csiphy_direction Transmit/Receive direction This signal is used to indicate the current direction of the Lane interconnects. When pin_direction =0, the Lane is in transmit mode. When pin_direction =1, the Lane is in receive mode
17	RO	0x0	csiphy_ulpsactivenotclk_1 ULP state(not) active This active low signal is asserted to indicate that the Lane is in ULP state
16	RO	0x0	csiphy_ulpsactivenotclk ULP state(not) active This active low signal is asserted to indicate that the Lane is in ULP state
15	RO	0x0	csiphy_errcontentionlp1_3 LP1 contention error This active high signal is asserted when the Lane Module detects a contention situation on a line while trying to drive the line low
14	RO	0x0	csiphy_errcontentionlp0_3 LP0 contention error This active high signal is asserted when the Lane Module detects a contention situation on a line while trying to drive the line low
13	RO	0x0	csiphy_errcontentionlp1_2 LP1 contention error This active high signal is asserted when the Lane Module detects a contention situation on a line while trying to drive the line low
12	RO	0x0	csiphy_errcontentionlp0_2 LP0 contention error This active high signal is asserted when the Lane Module detects a contention situation on a line while trying to drive the line low
11	RO	0x0	csiphy_errcontentionlp1_1 LP1 contention error This active high signal is asserted when the Lane Module detects a contention situation on a line while trying to drive the line low

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Bit	Attr	Reset Value	Description
10	RO	0x0	csiphy_errcontentionlp0_1 LP0 contention error This active high signal is asserted when the Lane Module detects a contention situation on a line while trying to drive the line low
9	RO	0x0	csiphy_errcontentionlp1_0 LP1 contention error This active high signal is asserted when the Lane Module detects a contention situation on a line while trying to drive the line low
8	RO	0x0	csiphy_errcontentionlp0_0 LP0 contention error This active high signal is asserted when the Lane Module detects a contention situation on a line while trying to drive the line low
7:4	RO	0x0	csiphy_rxskewcalhs High speed receive skew calibration This optional active high signal indicates that the high speed deskew burst is being received
3:0	RO	0x0	csiphy_ulpsactivenot ULP state(not) active This active low signal is asserted to indicate that the lane is in ULP state

VI_GRF_CSIPHY1_GRF_STATUS
Address: Operational Base(0x20150000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:19	RO	0x0	csiphy_err_control Contorl error This active high signal is asserted when an incorrect line state sequence is detected. For example, if a turnaround request or escape mode request is immediately followed by a Stop state instead of the required Bridge state, this signal is asserted and remains asserted until the next change in line state
18	RO	0x0	csiphy_direction Transmit/Receive direction This signal is used to indicate the current direction of the Lane interconnects. When pin_direction =0, the Lane is in transmit mode. When pin_direction =1, the Lane is in receive mode
17	RO	0x0	csiphy_ulpsactivenotclk_1 ULP state(not) active This active low signal is asserted to indicate that the Lane is in ULP state
16	RO	0x0	csiphy_ulpsactivenotclk ULP state(not) active This active low signal is asserted to indicate that the Lane is in ULP state
15	RO	0x0	csiphy_errcontentionlp1_3 LP1 contention error This active high signal is asserted when the Lane Module detects a contention situation on a line while trying to drive the line low
14	RO	0x0	csiphy_errcontentionlp0_3 LP0 contention error This active high signal is asserted when the Lane Module detects a contention situation on a line while trying to drive the line low

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Bit	Attr	Reset Value	Description
13	RO	0x0	csiphy_errcontentionlp1_2 LP1 contention error This active high signal is asserted when the Lane Module detects a contention situation on a line while trying to drive the line low
12	RO	0x0	csiphy_errcontentionlp0_2 LP0 contention error This active high signal is asserted when the Lane Module detects a contention situation on a line while trying to drive the line low
11	RO	0x0	csiphy_errcontentionlp1_1 LP1 contention error This active high signal is asserted when the Lane Module detects a contention situation on a line while trying to drive the line low
10	RO	0x0	csiphy_errcontentionlp0_1 LP0 contention error This active high signal is asserted when the Lane Module detects a contention situation on a line while trying to drive the line low
9	RO	0x0	csiphy_errcontentionlp1_0 LP1 contention error This active high signal is asserted when the Lane Module detects a contention situation on a line while trying to drive the line low
8	RO	0x0	csiphy_errcontentionlp0_0 LP0 contention error This active high signal is asserted when the Lane Module detects a contention situation on a line while trying to drive the line low
7:4	RO	0x0	csiphy_rxskewcalhs High speed receive skew calibration This optional active high signal indicates that the high speed deskew burst is being received
3:0	RO	0x0	csiphy_ulpsactivenot ULP state(not) active This active low signal is asserted to indicate that the lane is in ULP state

VI_GRF_MISC_GRF_CON

Address: Operational Base(0x20150000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	grf_isp_rd_hurry_thr isp read hurry threshold.
11:9	RW	0x0	grf_isp_wr_hurry_thr isp write hurry threshold.
8	RW	0x0	grf_isp_shaping_npu_en Use the isp hurry signal to control the npu's shaping value. 1'b1: enable. 1'b0: disable.
7	RW	0x0	grf_con_dsmc_mem_gate_en dsmc memory clock auto gating. 1'b1: enable auto gating. 1'b0: disable auto gating.

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Bit	Attr	Reset Value	Description
6	RW	0x0	grf_con_rkcan1_mem_gate_en rkcan1 memory clock auto gating. 1'b1: enable auto gating. 1'b0: disable auto gating.
5	RW	0x0	grf_con_rkcan0_mem_gate_en rkcan0 memory clock auto gating. 1'b1: enable auto gating. 1'b0: disable auto gating.
4	RW	0x0	grf_con_bufferable_hprot2_rkcan1 The ahb mater is rkcan1. 1'b1: set 1 for ahb master hprot bit2 field , this means enable the ahb master access is bufferable. 1'b0: set 0 for ahb master hprot bit2 field , this means enable the ahb master access is bufferable.
3	RW	0x0	grf_con_bufferable_hprot2_rkcan0 The ahb mater is rkcan0. 1'b1: set 1 for ahb master hprot bit2 field , this means enable the ahb master access is bufferable. 1'b0: set 0 for ahb master hprot bit2 field , this means enable the ahb master access is bufferable.
2	RW	0x0	grf_con_bufferable_hprot2_sdmmc0 The ahb mater is sdmmc0. 1'b1: set 1 for ahb master hprot bit2 field , this means enable the ahb master access is bufferable. 1'b0: set 0 for ahb master hprot bit2 field , this means enable the ahb master access is bufferable.
1	RW	0x0	csi2host1_ppi_sel_2lane Csi2host1 ppi select the lane0 and lane1.
0	RW	0x0	csi2host0_ppi_sel_2lane Csi2host0 ppi select the lane0 and lane1.

VI_GRF_GMAC_GRF_CON0

Address: Operational Base(0x20150000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	rkmacphy_en RKMACPHY Enable 1'b0:Disable 1'b1:Enable
14:12	RO	0x0	reserved
11	RW	0x0	gmac_ptp_aux_ts_trig Auxiliary Time Stamp Trigger. This signal is asserted to take an auxiliary snapshot of the time and store it in the auxiliary time stamp FIFO. A rising edge on this port is used to trigger the auxiliary snapshot.
10	RW	0x0	gmac_ptp_aux_ts_trig_sel Auxiliary Time Stamp Trigger Select 1'b0: from IO 1'b1: from grf gmac_ptp_aux_ts_trig
9	RW	0x0	gmac_mcg_pst_trig Trigger Input to the DUT to capture presentation time.

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Bit	Attr	Reset Value	Description
8	RW	0x0	gmac_mcg_pst_trig_sel Trigger Input to the DUT to capture presentation time. From IO or software. 1'b1: From IO 1'b0: From gmac0_mcg_pst_trig.
7:3	RW	0x00	gmac_clk_con GMAC cru configuration. Bit[3]: RMII mode. Bit[4]: Gate RMII 50MHz clock, active high. Bit[6:5]: GMAC controller txclk divider sel. In RMII mode : 2'b0: 25Mhz 2'b1: 2.5Mhz In RGMII mode : 2'b10: 2.5Mhz 2'b11: 25Mhz other: 125Mhz Bit[7]: GMAC txclk select control. 1'b1: Select clock form CRU 1'b0: Select clock form IO
2:1	RW	0x0	gnac_sbd_flowctrl Sideband Flow Control. When set high, instructs the MAC to transmit Pause frames in Full-duplex mode. In half-duplex mode, the MAC enables the Back-pressure function until this signal is made low again.
0	RW	0x0	gmac_clk_gating_en GMAC memory clock gate enable, active high.

VI_GRF_GMAC_DMA_ACK

Address: Operational Base(0x20150000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	gmac_mcgr_dma_ack_cmd This signal indicate that the request indicated by mcgr_dma_req_o is accepted by the application. active high.

VI_GRF_GMAC_GRF_STATUS0

Address: Operational Base(0x20150000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RO	0x0	grf_sbd_tx_clk_gating_ctrl_o GMAC LPI Tx Clock Gating Control. This signal is high after the MAC enters the Tx LPI (low power idle) mode. You can use this signal to control the Tx clock gating.
4:2	RO	0x0	reserved
1:0	RO	0x0	grf_gmac_speed_o Mac Speed indication/status. 2'b00:1000Mbps(GMII) 2'b01:2500Mbps(GMII) 2'b10:10Mbps(MII) 2'b11:100Mbps(MII).

VI_GRF_GMAC_GRF_STATUS1

Address: Operational Base(0x20150000) + offset (0x0064)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	gmac_timestamp_0 GMAC ptp timestamp[31:0] Reference Time Output. This bus provides the System Time output when it is generated internally.

VI_GRF_GMAC_GRF_STATUS2

Address: Operational Base(0x20150000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	gmac_timestamp_1 GMAC ptp timestamp[63:32] Reference Time Output. This bus provides the System Time output when it is generated internally.

VI_GRF_SARADC1_GRF_CON0

Address: Operational Base(0x20150000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	saradc_en_val Save the value when saradc power down signal is controlled by grf_con.
14	RW	0x0	saradc_en_sel 1'b1: the saradc_power down signal is controlled by "grf_saradc_en_val". 1'b0: the saradc_power down signal is controlled by ip.
13:10	RO	0x0	reserved
9:8	RW	0x0	saradc_itest_sel Internal test selection.
7	RW	0x0	saradc_itest_en Internal test enable.
6:4	RW	0x3	saradc_ibp_adj Control the bias current of the preamplifier in the SARADC. The value is the bias current.
3:1	RO	0x0	reserved
0	RW	0x1	saradc_clk_sel 1'b0: use rc oscillator clock. 1'b1: use cru clock.

VI_GRF_SARADC1_GRF_CON1

Address: Operational Base(0x20150000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	saradc_cal_mode set the cal mode for saradc phy, Enter calibration mode: RCOSC frequency calibration.
7:0	RW	0x00	saradc_offset_sel Bit7-Bit0: Store the offset cal value for saradc phy.

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VI_GRF_SARADC1_GRF_CON2
Address: Operational Base(0x20150000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:8	RW	0x5	saradc_rcosc_coarse set the rocsc_coarse value for saradc phy.
7:0	RW	0x2f	saradc_rcosc_fine Bit7-Bit0: Store the rcosc fine value for saradc phy. Fine-tuning of the internal RC oscillator frequency is configured by a register.

VI_GRF_SARADC2_GRF_CON0
Address: Operational Base(0x20150000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	saradc_en_val Save the value when saradc power down signal is controlled by grf_con.
14	RW	0x0	saradc_en_sel 1'b1: the saradc_power down signal is controlled by "grf_saradc_en_val". 1'b0: the saradc_power down signal is controlled by ip.
13:10	RO	0x0	reserved
9:8	RW	0x0	saradc_itest_sel Internal test selection.
7	RW	0x0	saradc_itest_en Internal test enable.
6:4	RW	0x3	saradc_ibp_adj Control the bias current of the preamplifier in the SARADC. The value is the bias current.
3:1	RO	0x0	reserved
0	RW	0x1	saradc_clk_sel 1'b0: use rc oscillator clock. 1'b1: use cru clock.

VI_GRF_SARADC2_GRF_CON1
Address: Operational Base(0x20150000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	saradc_cal_mode set the cal mode for saradc phy, Enter calibration mode: RCOSC frequency calibration.
7:0	RW	0x00	saradc_offset_sel Bit7-Bit0: Store the offset cal value for saradc phy.

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VI_GRF_SARADC2_GRF_CON2
Address: Operational Base(0x20150000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:8	RW	0x5	saradc_rcosc_coarse set the rocsc_coarse value for saradc phy.
7:0	RW	0x2f	saradc_rcosc_fine Bit7-Bit0: Store the rcosc fine value for saradc phy. Fine-tuning of the internal RC oscillator frequency is configured by a register.

VI_GRF_RKMACPHY_GRF_CON0
Address: Operational Base(0x20150000) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:5	RW	0x000000	rkmacphy_cfg_phy_id Assigned to the 3rd through 24th bits of the Organizationally Unique Identifier (OUI), respectively.
4:0	RW	0x00	rkmacphy_cfg_phy_addr PHY Address. The PHY Address is used for the SMI address and for the initialization of the Cipher (Scrambler) key.

VI_GRF_RKMACPHY_GRF_CON1
Address: Operational Base(0x20150000) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31	RW	0x0	rkmacphy_phy_enable PHY enable signal (active high). 1'b0: Enable PHY 1'b1: Disable PHY (Power down analog block, all internal clocks are killed, no access to PHY)
30:23	RO	0x00	reserved
22	RW	0x0	rkmacphy_grf_apb_sel APB selection for the mode of accessing registers. 1'b0: SMI mode 1'b1: APB mode
21:10	RO	0x000	reserved
9:6	RW	0x0	rkmacphy_cfg_rev_nr Manufacturer Revision Number. The Number is used in the MAC address to identify a specific product revision.
5:0	RW	0x00	rkmacphy_cfg_model_nr Manufacturer Model Number. The Number is a unique identifier assigned by the device manufacturer to identify a particular hardware model.

VI_GRF_RKMACPHY_GRF_CON2
Address: Operational Base(0x20150000) + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
13	RW	0x0	rkmacphy_gpio_mode_en GPIO mode enable 1'b0: PHY Enable 1'b1: GPIO Enable
12	RW	0x0	rkmacphy_preamble_bps 10Base-T preamble bypass mode 1'b0: Generating RX_DV with Preamble 1'b1: Generating RX_DV without Preamble
11:9	RW	0x0	rkmacphy_clk_freq_sel Clock frequency selection. 3'b000: 24MHz 3'b100: 50MHz Others: Reserved
8	RW	0x0	rkmacphy_grf_con_extclk_sel External clock model select.
7:0	RW	0x00	rkmacphy_dbg_bp_in Bypass input for debug.

VI_GRF_RKMACPHY_GRF_STATUS

Address: Operational Base(0x20150000) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RO	0x0	rkmacphy_fephy_led_spd FEPHY speed 1'b0: 10 Mbps 1'b1: 100 Mbps
3	RO	0x0	rkmacphy_fephy_led_link PHY link status 1'b0: PHY unlink 1'b1: PHY link
2	RO	0x0	rkmacphy_intreq Interrupt request 1'b0: No interrupt generated 1'b1: Interrupt generated
1	RO	0x0	rkmacphy_powerup_reset Power up reset signal 1'b0: Power up 1'b1: Reset
0	RO	0x0	rkmacphy_fephy_pll_lock PLL lock signal 1'b0: PLL unlock 1'b1: PLL lock

VI_GRF_RKMACPHY_CALIB_CON

Address: Operational Base(0x20150000) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:10	RW	0x0	rx_100btsig_cmp_isel RX 100BT signal detect comp current selection. 2'b00: 150uA 2'b01: 195uA 2'b10: 255uA 2'b11: 300uA
9	RW	0x0	rx_100btsig_trim_vcm_sel RX Squelch comp offset trimming common voltage selection. 1'b0: input signal common mode voltage 1'b1: internal generated common mode voltage
8	RW	0x0	rx_100btsig_trim_ck_sel RX Squelch comp offset trimming clock selection. 1'b0: ref clock 1'b1: ref clock division 4
7:6	RW	0x0	rx_sqcmp_data_ise RX Squelch comp current bias selection. 2'b00: 5uA 2'b01: 10uA 2'b10: 15uA 2'b11: 20uA
5	RW	0x0	rx_sqtrim_vcm_sel RX Squelch comp offset trimming common voltage selection. 1'b0: input signal common mode voltage 1'b1: internal generated common mode voltage
4	RW	0x0	rx_sqtrim_ck_sel RX Squelch comp offset trimming clock selection. 1'b0: ref clock 1'b1: ref clock division 4
3	RW	0x0	tx_calib_halfi_en TX driver bias current decrease half enable.
2	RW	0x0	txrx_rterm_en Enable TX internal term resistance.
1	RO	0x0	reserved
0	RW	0x0	grf_calib_en Calibration enable.

4.10 VEPU GRF Register Description

4.10.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

4.10.2 Registers Summary

Name	Offset	Size	Reset Value	Description
VEPU_GRF_MEM_GRF_SPRA	0x0000	W	0x00000021	VEPU single memory configuration
VEPU_GRF_MEM_GRF_DPRA	0x0004	W	0x00000000	VEPU dual-port memory config register
VEPU_GRF_VEPU_GRF_CON0	0x0008	W	0x00000000	VEPU grf register con0
VEPU_GRF_SARADC0_GRF_CON0	0x000C	W	0x00000031	Saradc0 grf con0 register
VEPU_GRF_SARADC0_GRF_CON1	0x0010	W	0x00000000	Saradc0 grf con1 register
VEPU_GRF_SARADC0_GRF_CON2	0x0014	W	0x0000052F	Saradc0 grf con2 register

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Name	Offset	Size	Reset Value	Description
VEPU_GRF_SDMMC1_DET_CNT	0x0024	W	0x000003E8	SDMMC1 detect counter register
VEPU_GRF_SDMMC1_SIG_DETECT_CON	0x0028	W	0x00000000	Sdmmc1 detect control register
VEPU_GRF_SDMMC1_SIG_DETECT_STATUS	0x002C	W	0x00000000	Sdmmc1 detect status register
VEPU_GRF_SDMMC1_STATUS_CLR	0x0030	W	0x00000000	Sdmmc1 status clear register

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

4.10.3 Detail Registers Description

VEPU_GRF_MEM_GRF_SPRA

Address: Operational Base(0x20160000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bit, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:10	RW	0x0	wtsel_hvt_mux4 Configuration for wtsel mux4 type for memory for VEPU.
9:8	RW	0x0	rtsel_hvt_mux4 Configuration for rtsel mux4 type for memory for VEPU.
7:6	RW	0x0	wtsel_hvt_mux1ormux2 Configuration for wtsel mux1ormux2 mem type for memory for VEPU.
5:4	RW	0x2	rtsel_hvt_mux1ormux2 Configuration for wtsel mux1ormux2 mem type for memory for VEPU.
3:2	RW	0x0	wtsel_svt Configuration for rtsel mux1ormux2 mem type for memory for VEPU. We only use the hvt.
1:0	RW	0x1	rtsel_svt Configuration for rtsel mux1ormux2 mem type for memory for VEPU. We only use the hvt.

VEPU_GRF_MEM_GRF_DPRA

Address: Operational Base(0x20160000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5:4	RW	0x0	rtsel VEPU memory configuration. 2'b00: Recommended setting with the optimized read margin. 2'b01: Relaxed read margin setting, used for debugging purpose. 2'b10: More relaxed read margin setting, used for debugging purpose. 2'b11: Most relaxed read margin setting, used for debugging purpose.

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	wtsel VEPU memory configuration. 2'b00: Recommended setting with the optimized write margin. 2'b01: Relaxed write margin setting, used for debugging purpose. 2'b10: More relaxed write margin setting, used for debugging purpose. 2'b11: Most relaxed write margin setting, used for debugging purpose.
1:0	RW	0x0	ptsel VEPU memory configuration. Setting for internal clock skew of port A/B with the optimized design margin and timming. 2'b00: Recommended value. 2'b01: Relaxed setting for internal clock skew of port A/B used for debugging purpose. 2'b10: More Relaxed setting for internal clock skew of port A/B used for debugging purpose. 2'b11: Most Relaxed setting for internal clock skew of port A/B used for debugging purpose.

VEPU_GRF_VEPU_GRF_CON0

Address: Operational Base(0x20160000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	grf_con_vepu_rf_mem_ckg vepu noc reorder bufffer memory clock auto gating. 1'b1: enable auto gating. 1'b0: disable auto gating.
14:1	RO	0x0000	reserved
0	RW	0x0	grf_con_bufferable_hprot2_sdmmc1 The ahb mater is hpmcu. 1'b1: set 1 for ahb master hprot bit2 field , this means enable the ahb master access is bufferable. 1'b0: set 0 for ahb master hprot bit2 field , this means enable the ahb master access is bufferable.

VEPU_GRF_SARADC0_GRF_CON0

Address: Operational Base(0x20160000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	grf_con_saradc_en_val Save the value when saradc power down signal is controlled by grf_con.
14	RW	0x0	grf_con_saradc_en_sel 1'b1: the saradc_power down signal is controlled by "grf_saradc_en_val". 1'b0: the saradc_power down signal is controlled by ip.
13:10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9:8	RW	0x0	grf_con_itest_sel Internal test selection.
7	RW	0x0	grf_con_itest_en Internal test enable.
6:4	RW	0x3	grf_con_ibj_adj Control the bias current of the preamplifier in the SARADC. The value is the bias current.
3:1	RO	0x0	reserved
0	RW	0x1	grf_con_clk_sel 1'b0: use rc oscillator clock. 1'b1: use cru clock .

VEPU_GRF_SARADC0_GRF_CON1
Address: Operational Base(0x20160000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	grf_cal_mode set the cal mode for saradc phy, Enter calibration mode: RCOSC frequency calibration.
7:0	RW	0x00	grf_offset_cal Bit7-Bit0: Store the offset cal value for saradc phy.

VEPU_GRF_SARADC0_GRF_CON2
Address: Operational Base(0x20160000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:8	RW	0x5	grf_rcosc_coarse set the rocsc_coarse value for saradc phy.
7:0	RW	0x2f	grf_rcosc_fine Bit7-Bit0: Store the rcosc fine value for saradc phy. Fine-tuning of the internal RC oscillator frequency is configured by a register.

VEPU_GRF_SDMMC1_DET_CNT
Address: Operational Base(0x20160000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x0003e8	detect_cnt SDMMC detect pin filter counter, in the unit of pclk default value is 1000, equal with 0x3e8

VEPU_GRF_SDMMC1_SIG_DETECT_CON
Address: Operational Base(0x20160000) + offset (0x0028)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	sig_detect_fall_en Enable SDMMC detect pin falling edge irq 1'b0: Disable 1'b1: Enable
0	RW	0x0	sig_detect_rise_en Enable SDMMC detect pin rising edge irq 1'b0: Disable 1'b1: Enable

VEPU_GRF_SDMMC1_SIG_DETECT_STATUS
Address: Operational Base(0x20160000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	sig_detect_fall_irq SDMMC detect pin falling edge irq status 1'b0: Not active 1'b1: Active
0	RW	0x0	sig_detect_rise_irq SDMMC detect pin rising edge irq status 1'b0: Not active 1'b1: Active

VEPU_GRF_SDMMC1_STATUS_CLR
Address: Operational Base(0x20160000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
1	W1C	0x0	sig_detect_fall_clr SDMMC detect pin falling edge irq clear 1'b0: Disable 1'b1: Enable
0	W1C	0x0	sig_detect_rise_clr SDMMC detect pin rising edge irq clear 1'b0: Disable 1'b1: Enable

4.11 NPU GRF Register Description

4.11.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

4.11.2 Registers Summary

Name	Offset	Size	Reset Value	Description
NPU_GRF_MEM_GRF_SPRA	0x0000	W	0x00000021	NPU memory configuration
NPU_GRF_MEM_GRF_DPRA	0x0004	W	0x00000000	NPU dual-port memory config register

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Name	Offset	Size	Reset Value	Description
NPU_GRF_NPU_GRF_CBUF_MEM_SOFT_GATE	0x0008	W	0x00000000	npu cbuf mem soft gate
NPU_GRF_NPU_GRF_CFG_NSP_SLV_ADDR	0x000C	W	0x00000000	NPU grf configuration nsp slave address register
NPU_GRF_NPU_GRF_NSP_MEM_SOFT_GATE	0x0010	W	0x00000000	NPU grf nsp memory software gate register
NPU_GRF_NPU_GRF_CFG_USE_NSP	0x0014	W	0x00000000	NPU grf configuration use nsp register
NPU_GRF_NPU_GRF_SHAPE	0x0018	W	0x00000000	NPU grf shape register

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

4.11.3 Detail Registers Description

NPU_GRF_MEM_GRF_SPRA

Address: Operational Base(0x20170000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bit, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:10	RW	0x0	wtsel_hvt_mux4 Configuration for wtsel mux4 type for memory for RKNN.
9:8	RW	0x0	rtsel_hvt_mux4 Configuration for rtsel mux4 type for memory for RKNN.
7:6	RW	0x0	wtsel_hvt_mux1ormux2 Configuration for wtsel mux1ormux2 mem type for memory for RKNN.
5:4	RW	0x2	rtsel_hvt_mux1ormux2 Configuration for rtsel mux1ormux2 mem type for memory for RKNN.
3:2	RW	0x0	wtsel_svt Configuration for wtsel mux1ormux2 mem type for memory for RKNN.
1:0	RW	0x1	rtsel_svt Configuration for rtsel mux1ormux2 mem type for memory for RKNN.

NPU_GRF_MEM_GRF_DPRA

Address: Operational Base(0x20170000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
5:4	RW	0x0	rtsel NPU memory configuration. 2'b00: Recommended setting with the optimized read margin. 2'b01: Relaxed read margin setting, used for debugging purpose. 2'b10: More relaxed read margin setting, used for debugging purpose. 2'b11: Most relaxed read margin setting, used for debugging purpose.
3:2	RW	0x0	wtsel NPU memory configuration. 2'b00: Recommended setting with the optimized write margin. 2'b01: Relaxed write margin setting, used for debugging purpose. 2'b10: More relaxed write margin setting, used for debugging purpose. 2'b11: Most relaxed write margin setting, used for debugging purpose.
1:0	RW	0x0	ptsel NPU memory configuration. Setting for internal clock skew of port A/B with the optimized design margin and timming. 2'b00: Recommended value. 2'b01: Relaxed setting for internal clock skew of port A/B used for debugging purpose. 2'b10: More Relaxed setting for internal clock skew of port A/B used for debugging purpose. 2'b11: Most Relaxed setting for internal clock skew of port A/B used for debugging purpose.

NPU_GRF_NPU_GRF_CBUF_MEM_SOFT_GATE
Address: Operational Base(0x20170000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cbuf_mem_soft_gate NPU configuration clock gating for cbuf memory.

NPU_GRF_NPU_GRF_CFG_NSP_SLV_ADDR
Address: Operational Base(0x20170000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cfg_nsp_slv_addr NPU configuration nsp slv address .

NPU_GRF_NPU_GRF_NSP_MEM_SOFT_GATE
Address: Operational Base(0x20170000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	nsp_mem_soft_gate NPU configuration clock gating for nsp mem .

NPU_GRF_NPU_GRF_CFG_USE_NSP
Address: Operational Base(0x20170000) + offset (0x0014)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	cfg_use_nsp when use_nsp is 1 , then set nsp slave to configure npu. or ahb bus configure npu.

NPU_GRF_NPU_GRF_SHAPE
Address: Operational Base(0x20170000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:0	RW	0x00	grf_isp_shape_npu_val Store the isp shape npu value.

4.12 VDO GRF Register Description

4.12.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

4.12.2 Registers Summary

Name	Offset	Size	Reset Value	Description
VDO_GRF_MEM_GRF_SPRA	0x0000	W	0x00000021	VEPU single memory configuration
VDO_GRF_MEM_GRF_DPRA	0x0004	W	0x00000000	VEPU dual-port memory config register
VDO_GRF_MEM_GATE_GRF_CON	0x0008	W	0x00000000	Memory gate grf con register
VDO_GRF_DSI_GRF_CON	0x000C	W	0x00000000	DSI grf con register
VDO_GRF_DSIPHY_GRF_CON	0x0010	W	0x00000000	DSIPHY grf con register
VDO_GRF_RKMMU_GRF_CON	0x0014	W	0x00000001	RKMMU grf con register
VDO_GRF_VDO_GRF_STATUS0	0x0050	W	0x00000000	VDO grf status0 register
VDO_GRF_VDO_GRF_STATUS1	0x0054	W	0x00000000	VDO grf status1 register

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

4.12.3 Detail Registers Description

VDO_GRF_MEM_GRF_SPRA
Address: Operational Base(0x20180000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bit, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:10	RW	0x0	wtsel_hvt_mux4 Configuration for wtsel mux4 type for memory for VEPU.
9:8	RW	0x0	rtsel_hvt_mux4 Configuration for rtsel mux4 type for memory for VEPU.
7:6	RW	0x0	wtsel_hvt_mux1ormux2 Configuration for wtsel mux1ormux2 mem type for memory for VEPU.
5:4	RW	0x2	rtsel_hvt_mux1ormux2 Configuration for wtsel mux1ormux2 mem type for memory for VEPU.

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	wtsel_svt Configuration for rtsel mux1ormux2 mem type for memory for VEPU. We only use the hvt.
1:0	RW	0x1	rtsel_svt Configuration for rtsel mux1ormux2 mem type for memory for VEPU. We only use the hvt.

VDO_GRF_MEM_GRF_DPRA

Address: Operational Base(0x20180000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5:4	RW	0x0	rtsel VEPU memory configuration. 2'b00: Recommended setting with the optimized read margin. 2'b01: Relaxed read margin setting, used for debugging purpose. 2'b10: More relaxed read margin setting, used for debugging purpose. 2'b11: Most relaxed read margin setting, used for debugging purpose.
3:2	RW	0x0	wtsel VEPU memory configuration. 2'b00: Recommended setting with the optimized write margin. 2'b01: Relaxed write margin setting, used for debugging purpose. 2'b10: More relaxed write margin setting, used for debugging purpose. 2'b11: Most relaxed write margin setting, used for debugging purpose.
1:0	RW	0x0	ptsel VEPU memory configuration. Setting for internal clock skew of port A/B with the optimized design margin and timming. 2'b00: Recommended value. 2'b01: Relaxed setting for internal clock skew of port A/B used for debugging purpose. 2'b10: More Relaxed setting for internal clock skew of port A/B used for debugging purpose. 2'b11: Most Relaxed setting for internal clock skew of port A/B used for debugging purpose.

VDO_GRF_MEM_GATE_GRF_CON

Address: Operational Base(0x20180000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	grf_con_mem_gat_en_decom memory gate control for decom 1'b0: Disable 1'b1: Enable

VDO_GRF_DSI_GRF_CON

Address: Operational Base(0x20180000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	dsi_grf_con_dpiupdatecfg 1'b1: dpiupdatecfg. 1'b0: not active.
2	RO	0x0	reserved
1	RW	0x0	dsi_grf_con_dpicolorm 1'b1: dpicolorm. 1'b0: not active.
0	RW	0x0	dsi_grf_con_shutdn 1'b1: shutdown 1'b0: not active.

VDO_GRF_DSIPHY_GRF_CON

Address: Operational Base(0x20180000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	dsi_grf_phy_con Bit[0] : 1 active grf_con_dsiphy_forcerxmode , 0 not active . Bit[1] : 1 active grf_con_dsiphy_lvds_mode , 0 not active . Bit[2] : 1 active grf_con_dsiphy_lane0_turndisable , 0 not active . Bit[4] : 1 active grf_con_dsiphy_lane0_frctxstpm , 0 not active . Bit[5] : 1 active grf_con_dsiphy_lane1_frctxstpm , 0 not active . Bit[6] : 1 active grf_con_dsiphy_lane2_frctxstpm , 0 not active . Bit[7] : 1 active grf_con_dsiphy_lane3_frctxstpm , 0 not active . Bit[11] : 1 active grf_con_dsiphy_txskewcalhs_ck , 0 not active . Bit[12] : 1 active grf_con_dsiphy_txskewcalhs_0 , 0 not active . Bit[13] : 1 active grf_con_dsiphy_txskewcalhs_1 , 0 not active . Bit[14] : 1 active grf_con_dsiphy_txskewcalhs_2 , 0 not active . Bit[15] : 1 active grf_con_dsiphy_txskewcalhs_3 , 0 not active .

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VDO_GRF_RKMMU_GRF_CON
Address: Operational Base(0x20180000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	grf_con_dbg_err_clr 1'b0: not clr the debug cnt for rkmmu. 1'b1: clr the debug cnt for rkmmu.
7:4	RO	0x0	reserved
3	RW	0x0	grf_con_mem_gat_en_rkmmu memory gate control for rkmmu_deom 1'b0: Disable 1'b1: Enable
2:1	RO	0x0	reserved
0	RW	0x1	grf_con_bypass_rkmmu 1'b1: bypass rkmmu, this means disable rkmmu for decom ip. 1'b0: not bypass rkmmu, If you want to use rkmmu func. you must first set 1 before enable decom.

VDO_GRF_VDO_GRF_STATUS0
Address: Operational Base(0x20180000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	grf_st_rkmmu_pte_tag_hits 1'b1: means rkmmu PteTagHits err. 1'b0: normal status.
1	RW	0x0	grf_st_rkmmu_dte_tag_hits 1'b1: means rkmmu DteTagHits err. 1'b0: normal status.
0	RO	0x0	reserved

VDO_GRF_VDO_GRF_STATUS1
Address: Operational Base(0x20180000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	grf_st1_mmu Bit[7:0]: Return the External Rx AXI Command Counter Value. Bit[15:8]: Return the External Tx AXI Command Counter Value. Bit[23:16]: Return the AXI Page Read Data Channel Counter Value. Bit[31:24]: Return the AXI Page Address Read Channel Counter Value.

4.13 VCP GRF Register Description

4.13.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

4.13.2 Registers Summary

Name	Offset	Size	Reset Value	Description
VCP_GRF_MEM_GRF_SPRA	0x0000	W	0x00000021	VEPU single memory configuration
VCP_GRF_MEM_GRF_DPRA	0x0004	W	0x00000000	VEPU dual-port memory config register

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Name	Offset	Size	Reset Value	Description
VCP_GRF_VCP_GRF_AIISP_SHAPING_CON	0x0008	W	0x00000000	VEPU AIISP SHAPING Con Register

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

4.13.3 Detail Registers Description

VCP_GRF_MEM_GRF_SPRA

Address: Operational Base(0x20190000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bit, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:10	RW	0x0	wtsel_hvt_mux4 Configuration for wtsel mux4 type for memory for VEPU.
9:8	RW	0x0	rtsel_hvt_mux4 Configuration for rtsel mux4 type for memory for VEPU.
7:6	RW	0x0	wtsel_hvt_mux1ormux2 Configuration for wtsel mux1ormux2 mem type for memory for VEPU.
5:4	RW	0x2	rtsel_hvt_mux1ormux2 Configuration for wtsel mux1ormux2 mem type for memory for VEPU.
3:2	RW	0x0	wtsel_svt Configuration for rtsel mux1ormux2 mem type for memory for VEPU. We only use the hvt.
1:0	RW	0x1	rtsel_svt Configuration for rtsel mux1ormux2 mem type for memory for VEPU. We only use the hvt.

VCP_GRF_MEM_GRF_DPRA

Address: Operational Base(0x20190000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5:4	RW	0x0	rtsel VEPU memory configuration. 2'b00: Recommended setting with the optimized read margin. 2'b01: Relaxed read margin setting, used for debugging purpose. 2'b10: More relaxed read margin setting, used for debugging purpose. 2'b11: Most relaxed read margin setting, used for debugging purpose.

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	wtsel VEPU memory configuration. 2'b00: Recommended setting with the optimized write margin. 2'b01: Relaxed write margin setting, used for debugging purpose. 2'b10: More relaxed write margin setting, used for debugging purpose. 2'b11: Most relaxed write margin setting, used for debugging purpose.
1:0	RW	0x0	ptsel VEPU memory configuration. Setting for internal clock skew of port A/B with the optimized design margin and timming. 2'b00: Recommended value. 2'b01: Relaxed setting for internal clock skew of port A/B used for debugging purpose. 2'b10: More Relaxed setting for internal clock skew of port A/B used for debugging purpose. 2'b11: Most Relaxed setting for internal clock skew of port A/B used for debugging purpose.

VCP_GRF_VCP_GRF_AIISP_SHAPING_CON

Address: Operational Base(0x20190000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:12	RW	0x0	grf_aiisp_rd_hurry_thr Store the aiisp read hurry threshold value.
11	RO	0x0	reserved
10:8	RW	0x0	grf_aiisp_wr_hurry_thr Store the aiisp wr hurry threshold value.
7	RW	0x0	grf_aiisp_shaping_npu_en 1'b0: Disable the aiisp shaping npu function. 1'b1: Enable the aiisp shaping npu function.
6:0	RO	0x00	reserved

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Chapter 5 Power Management Unit (PMU)

5.1 Overview

In order to meet low power requirements, a power management unit (PMU) is designed for controlling power resources in the chip. The PMU is dedicated for managing the power of the whole chip.

PMU supports the following features:

- Support multi voltage domains: VD_PMU/VD_CORE/VD_NPU/VD_RTC/VD_LOGIC
- Support multi power domains in VD_PMU: PD_PMU1
- Support multi power domains in VD_LOGIC: PD_VDO/PD_AIISP
- Support multi power domains in VD_CORE: PD_A53_2/PD_A53_3
- Support BIU idle operations: BIU_PMU1/BIU_CORE/BIU_NPU/BIU_BUS/BIU_DDR/BIU_PERI/BIU_VI/BIU_VCP/BIU_VDO/BIU_AIISP
- Support SCU/CPU auto power down
- Support power down/up all power domains by software or hardware
- Support power down/up all voltage domains by software or hardware
- Support clock gating mask for each domain
- Support auto clock gating domain: PERI/VEPU/VCP/VI/NPU/VDO/AIISP/CORE/DDR/BUS
- Support to send idle request to each BIU
- Support global interrupt disable in low power mode
- Support low frequency clock source from IO/RTC/RC_OSC
- Support PMU clock switch to low frequency clock in low power mode
- Support PLL(DPLL/GPLL/PPLL/CPLL) power down/up by hardware in low power mode
- Support OSC enable/disable request in low power mode
- Support to clamp all VD_PMU input before power off VD_LOGIC in low power mode
- Support wake-up reset control in power off mode
- Support DDR self-refresh in low power mode
- Support DDR controller clock auto gating in low power mode
- Support varies configurable wake-up source for low power mode
- Support sending PMU debug information to IO
- Support sending AOV debug information to IO
- Support sending PMU sleep signals to IO
- Support PWM auto switch to GPIO during power down
- Support configurable counters: PLL lock/SCU stable/OSC stable/PWM switch/PMU sleep counter, etc.

5.2 Block Diagram

The following figure is the PMU block diagram. The PMU includes the 3 following sections:

- APB Interface and Register: Provide AMBA APB interface for register read and write
- System Power State Control: Provide power management for various low power modes
- Power Gating Control: Provide power gating control for power domains

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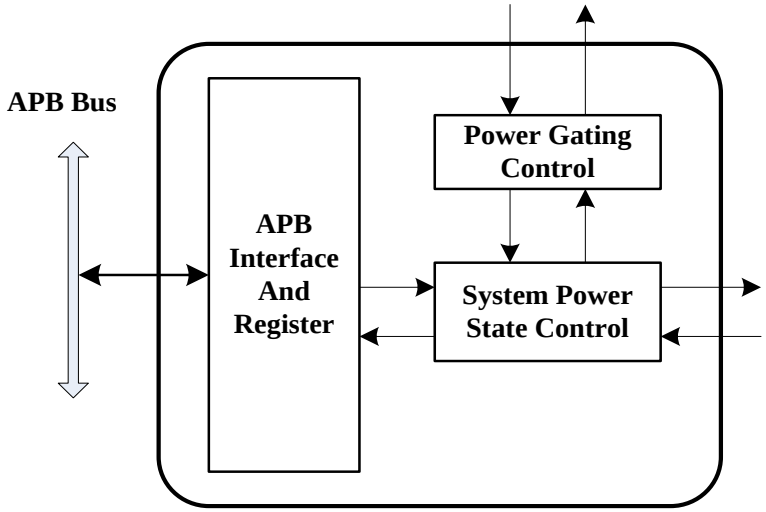

Fig.5-1 PMU Bock Diagram

5.3 Function Description

5.3.1 Domain Partition

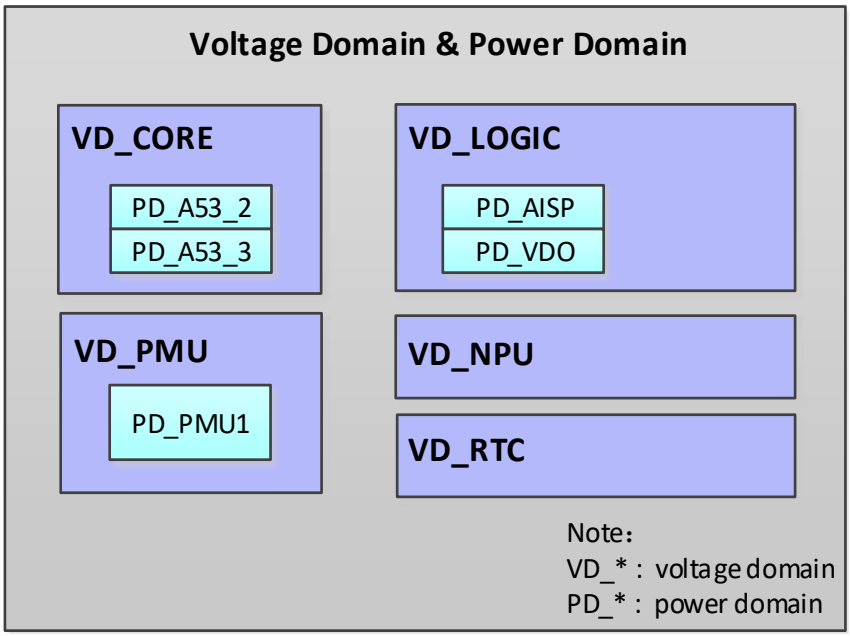

Fig.5-2 Voltage Domain and Power Domain Partition

The above diagram describes the power domain and voltage domain partition, and the following table lists IPs in every power domain.

Table 5-1 Voltage Domain and Power Domain Summary

Voltage Domain	Power Domain	Description
VD_PMU	PD_PMU1	SPI2AHB/FSPI1/LPDMA/LPSAI/LPADC AOA_CTRL/AOA_MEM/PMUIO1_IOC/PMU1_CRU
	ALIVE	I2C2/PWM1/GPIO0/UART0/HPTIMER PMU_MAILBOX/PMU_WDT/LPMCU/PMUMEM PMU/AOV_CTRL/RKNPOR/LDO/RCOSC PMUIO0_IOC/PMU_CRU/PMU_GRF
VD_CORE	PD_A53_2	A53_CORE2
	PD_A53_3	A53_CORE3
	ALIVE	A53_CORE0/A53_CORE1/L1/L2/DAPLITE GRF_CORE/CRU_CORE/PVTPLL_CORE
VD_NPU	NA	RKNN/GRF_NPU/CRU_NPU/PVTPLL_NPU
VD_RTC	NA	RTCPHY
VD_LOGIC	PD_AIISP	AIISP

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Voltage Domain	Power Domain	Description
	PD_VDO	VOP/RKVDEC/RKJPEGD/DECOM MIPI_DSI_PHY/DSI_TX/VDO_CRU/VDO_GRF
	ALIVE	VOP/DSI/MIPI_DSIPHY/OCC/RGA2P5/RKVDEC RKJPEGD/FEC/AVSP/ISP/CSI_RX/MIPI_CSIPHY VICAP/VPSS/VPSL/TSADC/BOOTROM/PDM ASRC/GMAC/RKFEPHY/DCF/DECOM/CAN DDRC/DDRPHY/DFIMONITOR/DMA2DDR RKDMA/HPMCU/SDMMC/EMMC CRU/GRF/BIU/PLL RKMMU_DECOM/WDTS/WDTNS TIMERS/TIMERNS/OTPC/OTPCMASK RKCE/RKRNG/KEYREADER/DFT2APB/PWM USBHOST2/USB2PHY/USBOTG3/USB3PHY PVTPLL_ISP/PVTPLL_VENC SYS_SRAM/GIC400/SPINLOCK/MAILBOX_HP DSMC/FSPI0/GPIO/UART/SPI/I2C

5.3.2 Operation Mode

First of all, we define two operation modes of PMU, normal mode and low power mode.
When operating at normal mode, that means software can manage power sources directly by accessing PMU registers.
When operating at low power mode, software manages power sources indirectly through FSM (Finite States Machine) in PMU and those settings always not take effect immediately. That means software also can configure PMU registers to power down/up some power resources, but these setting will not be executed immediately after configuration. They will be delayed to execute after FSM running in particular phase.
To enter low power mode, after setting some power configurations, the PMU1_PWR_CON1[0] bit must be set 1 to enable PMU FSM. Then CPU needs to execute a WFI command to perform ready signal. After PMU detects all CPUs in WFI status, the FSM will be fetched. And the specific power sources will be controlled during specific status in FSM. So, the low power mode is a "delay affect" way to handle power sources inside the chip.

5.3.3 Low Power Mode

There are 2 low power modes defined for the chip: Power mode 0, Power mode 1.
Power mode 0: Ultra low power mode. In this power mode, all logic except ALIVE in VD_PMU can be power off or power down. Chip can be waked up by GPIO interrupt triggered by IO in PMUIO0 domain.
Power mode 1: Low power mode. In this power mode, all logic except ALIVE and PD_PMU1 in VD_PMU can be power off or power down. Chip can be waked up by GPIO interrupt triggered by IO in PMUIO0 and PMUIO1 domain or other wake up source from PD_PMU1 when in hardware power mode, or wake up by LPMCU_PMU when in hardware power mode.

5.4 Register Description

PMU registers are divided into 3 parts for flexible applications:

- Offset = 0x0000~0x3FFF: registers defined in PMU0;
- Offset = 0x4000~0x7FFF: registers defined in PMU1;
- Offset = 0x8000~0xBFFF: registers defined in PMU2.

5.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PMU0_PWR_CON0	0x0000	W	0x00000000	PMU power control 0 register
PMU0_PMIC_STABLE_CNT_P0	0x0010	W	0x000FFFFF	PMU wake up interrupt status register for power mode 0

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Name	Offset	Size	Reset Value	Description
PMU0_INFO_TX_CON	0x0030	W	0x00000000	PMU debug information transmit control register
PMU0_INFO_TX_SOFT_CON	0x0034	W	0x00000000	PMU debug information transmit control software register
PMU0_PWR_ACK_SEL_CON	0x0040	W	0x00000000	PMU acknowledge selection control register
PMU0_BUS_IDLE_ACK	0x0044	W	0x00000000	BIU idle acknowledge status register
PMU0_BUS_IDLE_ST	0x0048	W	0x00000000	BIU idle status register
PMU1_VERSION	0x0000	W	0x00001126	PMU version register
PMU1_PWR_CON1	0x0004	W	0x00000000	PMU power control 1 register
PMU1_GLB_POWER_STS	0x0008	W	0x00000000	PMU global power status register
PMU1_INT_MASK_CON	0x000C	W	0x00000000	PMU interrupt mask control register
PMU1_WAKEUP_INT_CON	0x0010	W	0x00000000	PMU wake up interrupt control register
PMU1_WAKEUP_INT_STS	0x0014	W	0x00000000	PMU wake up interrupt status register
PMU1_WAKEUP_EDGE_CON	0x0018	W	0x00000000	PMU wake up edge control register
PMU1_WAKEUP_EDGE_ST	0x001C	W	0x00000000	PMU wake up edge status register
PMU1_WAKEUP_TIMEOUT_CNT_STATUS	0x0020	W	0x00000000	PMU wakeup timeout counter register
PMU1_DDR_CH0_PWR_CON	0x0100	W	0x00000000	DDR channel 0 hardware power control register
PMU1_DDR_CH0_PWR_SFTCON	0x0110	W	0x00000000	DDR channel 0 software power control register
PMU1_DDR_AXIPWR_CON0	0x0120	W	0x00000000	DDR axi-clock domain hardware power control register 0
PMU1_DDR_AXIPWR_SFTCON0	0x0130	W	0x00000000	DDR axi-clock domain software power control register 0
PMU1_DDR_AXIPWR_SFTCON1	0x0134	W	0x00000000	DDR axi-clock domain software power control register 1
PMU1_DDR_AXIPWR_SFTCON2	0x0138	W	0x00000000	DDR axi-clock domain software power control register 2
PMU1_DDR_POWER_STS	0x0140	W	0x00000000	DDR power state register
PMU1_DDR_STS	0x0144	W	0x00000000	DDR state register
PMU1_DDR_AXI_STS	0x0148	W	0x00000000	DDR axi-clock domain state register

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Name	Offset	Size	Reset Value	Description
PMU1_CRU_PWR_CON0	0x0200	W	0x00000000	Clock and reset hardware power control register0
PMU1_CRU_PWR_CON1	0x0204	W	0x00000000	Clock and reset hardware power control register1
PMU1_CRU_PWR_SFTCON	0x0208	W	0x00000000	Clock and reset software power control register
PMU1_CRU_PWR_SFTCON1	0x020C	W	0x00000000	Clock and reset hardware power control register 1
PMU1_CRU_POWER_STS	0x0210	W	0x00000000	Clock and reset power state register
PMU1_PLLPD_CON0	0x0220	W	0x00000000	PLL hardware power control register 0
PMU1_PLLPD_SFTCON0	0x0228	W	0x00000000	PLL software power control register 0
PMU1_PMIC_STABLE_CNT	0x0300	W	0x000FFFFF	PMIC stable count register
PMU1_OSC_STABLE_CNT	0x0304	W	0x000FFFFF	Oscillator stable count register
PMU1_WAKEUP_RST_CLR_CNT	0x0308	W	0x000FFFFF	Wake up reset clear count register
PMU1_PLL_LOCK_CNT	0x030C	W	0x000FFFFF	PLL lock count register
PMU1_WAKEUP_TIMEOUT_CNT	0x0310	W	0x00005DC0	PMU wake up timeout count register
PMU1_PWM_SWITCH_CNT	0x0314	W	0x000FFFFF	PWM switch stable count register
PMU1_SLEEP_CNT	0x0318	W	0x00000000	PMU sleep count register
PMU2_SCU_PWR_CON0	0x0000	W	0x00000200	SCU power control register
PMU2_SCU_PWR_SFTCON	0x0004	W	0x00000000	SCU power control software register
PMU2_SCU_AUTO_PWR_CON	0x0008	W	0x00000000	SCU auto power control register
PMU2_SCU_PWR_STATE	0x000C	W	0x00000000	SCU power status register
PMU2_DBG_PWR_CON	0x0018	W	0x00000000	CPU debug power control register
PMU2_CLUSTER_PWR_ST	0x001C	W	0x00000000	CLUSTER status register
PMU2_CLUSTER_IDLE_CON	0x0020	W	0x00000000	ClUSTER idle control register
PMU2_CLUSTER_IDLE_SFTCON	0x0024	W	0x00000000	ClUSTER idle control software register
PMU2_CLUSTER_IDLE_ACK	0x0028	W	0x00000000	Cluster idle acknowledge register
PMU2_CLUSTER_IDLE_ST	0x002C	W	0x00000000	Cluster idle state register
PMU2_SCU_PWRUP_CNT	0x0040	W	0x00005DC0	SCU power up stable counter
PMU2_SCU_PWRDN_CNT	0x0044	W	0x00005DC0	SCU power down stable counter

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Name	Offset	Size	Reset Value	Description
PMU2_SCU_STABLE_CNT	0x0048	W	0x000FFFFF	SCU power stable counter
PMU2_CPU_AUTO_PWR_CON0	0x0080	W	0x00000000	CPU0 auto power control register
PMU2_CPU_AUTO_PWR_CON1	0x0084	W	0x00000000	CPU1 auto power control register
PMU2_CPU_AUTO_PWR_CON2	0x0088	W	0x00000000	CPU2 auto power control register
PMU2_CPU_AUTO_PWR_CON3	0x008C	W	0x00000000	CPU3 auto power control register
PMU2_CPU_PWR_SFTCON0	0x00A0	W	0x00000000	CPU0 power control software register
PMU2_CPU_PWR_SFTCON1	0x00A4	W	0x00000000	CPU1 power control software register
PMU2_CPU_PWR_SFTCON2	0x00A8	W	0x00000000	CPU2 power control software register
PMU2_CPU_PWR_SFTCON3	0x00AC	W	0x00000000	CPU3 power control software register
PMU2_BIU_IDLE_CON0	0x0100	W	0x00000000	BIU idle request hardware control register 0
PMU2_BIU_IDLE_SFTCON0	0x0110	W	0x00000000	BIU idle request software control register 0
PMU2_BIU_IDLE_ACK_STS0	0x0120	W	0x00000000	BIU idle acknowledge status register 0
PMU2_BIU_IDLE_STS0	0x0128	W	0x00000000	BIU idle status register 0
PMU2_BIU_GATEMASK_CON0	0x0130	W	0x00000000	BIU automatic clock gating control register 0
PMU2_BIU_GATEMASK_SFTCON0	0x0140	W	0x00000000	BIU software clock gating control register 0
PMU2_PWR_GATE_CON0	0x0200	W	0x00000000	Power domain hardware power control register 0
PMU2_PWR_GATE_SFTCON0	0x0210	W	0x00000001	Power domain software power control register 0
PMU2_VOL_GATE_CON0	0x0220	W	0x00000000	Voltage domain hardware power control register 0
PMU2_PWR_GATE_STS	0x0230	W	0x00000000	Power domain power status register
PMU2_PWR_GATE_POWER_STS	0x0238	W	0x00000000	Power gating status register
PMU2_PWR_DWN_ACK_STS0	0x0240	W	0x00000000	Power chain 0 power status register 0
PMU2_PWR_C0_ACK_SEL_CON0	0x0380	W	0x00000000	Power chain 0 acknowledge selection control register 0

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

5.4.2 Detail Registers Description

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PMU0_PWR_CON0
Address: Operational Base(0x20830000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	biu_auto_pmu1 When perform idle operation, BIU_PMU1 corresponding clock can be opened or gated automatically. 1'b0: Disable 1'b1: Enable
12	RW	0x0	pmu1_bus_idle_sftena Enable sending idle request to BIU_PMU1 by software. 1'b0: Disable 1'b1: Enable
11	RW	0x0	pmu1_bus_idle_ena Enable sending idle request to BIU_PMU1 by hardware. 1'b0: Disable 1'b1: Enable
10	RO	0x0	reserved
9	RW	0x0	pmu1_pwr_gate_sftena Enable power down PD_PMU1 by software. 1'b0: Disable 1'b1: Enable
8	RW	0x0	pmu1_pwr_gate_ena Enable power down PD_PMU1 by hardware. 1'b0: Disable 1'b1: Enable
7:5	RO	0x0	reserved
4	RW	0x0	pmic_stable_bypass Bypass waiting for PMIC stability in power mode 0 procedure. If asserted, the FSM will enter next state without waiting until PMIC is stable. 1'b0: Disable 1'b1: Enable
3	RO	0x0	reserved
2	RW	0x0	pmu1_bus_bypass Bypass BIU_PMU1 idle flow in power mode 0 procedure. 1'b0: Disable 1'b1: Enable
1	RW	0x0	pmu1_pwr_bypass Bypass PD_PMU1 power gating flow in power mode 0 procedure. If asserted, PD_PMU1 is not power down or power up during power mode 0 procedure. 1'b0: Disable 1'b1: Enable
0	R/WSC	0x0	powermode0_en Power mode 0 (minimal power status) enable. When controller enters power mode 0 procedure, this bit is automatically cleared. 1'b0: Disable 1'b1: Enable

PMU0_PMIC_STABLE_CNT_P0
Address: Operational Base(0x20830000) + offset (0x0010)

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Bit	Attr	Reset Value	Description
31:0	RO	0x000fffff	pmic_stable_cnt PMIC stable count for power mode 0 procedure. Number of clk_pmu used by counter logic.

PMU0_INFO_TX_CON

Address: Operational Base(0x20830000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10	RW	0x0	info_tx_sft_en Enable PMU debug information set by software. 1'b0: Disable 1'b1: Enable
9	RW	0x0	info_tx_sft_sel PMU debug information selection. 1'b0: PMU power state 1'b1: software debug information
8	RW	0x0	info_tx_en Enable PMU debug information transition. 1'b0: Disable 1'b1: Enable
7:0	RW	0x00	info_tx_intv_time The interval time between the bytes of PMU debug information.

PMU0_INFO_TX_SOFT_CON

Address: Operational Base(0x20830000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	info_tx_soft_con software debug information.

PMU0_PWR_ACK_SEL_CON

Address: Operational Base(0x20830000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	pmu_pwr_ack_sel pd_pmu1_dwn_ack source selection when power down PD_PMU1 in Power mode 0. 1'b0: ACK from power switch 1'b1: ACK from pd_pmu1_dwn_req

PMU0_BUS_IDLE_ACK

Address: Operational Base(0x20830000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
0	RO	0x0	idle_ack_pmu1 BIU_PMU1 idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge

PMU0_BUS_IDLE_ST

Address: Operational Base(0x20830000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	idle_pmu1 BIU_PMU1 idle state. 1'b0: Not idle 1'b1: Idle

PMU1_VERSION

Address: Operational Base(0x20834000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RO	0x00001126	version PMU version

PMU1_PWR_CON1

Address: Operational Base(0x20834000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14	RW	0x0	wakeup_pmu_sft_con Wake up PMU sleep by software. 1'b0: Disable 1'b1: Enable
13	RW	0x0	sleep_cnt_en Enable sleep_cnt in power mode 1 procedure when PMU is in ST_SLEEP. 1'b0: Disable 1'b1: Enable
12	RW	0x0	wfi_bypass Bypass WFI in power mode 1 procedure. If asserted, PMU FSM does not need to wait for CPU standbywfi state before entering low power flow. 1'b0: Disable 1'b1: Enable
11:10	RO	0x0	reserved
9	RW	0x0	pdpmu1_bypass Bypass pd_pmu1 low power flow in power mode 1 procedure. 1'b0: Disable 1'b1: Enable
8	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
7	RW	0x0	cru_bypass Bypass clock and reset low power flow in power mode 1 procedure. If asserted, PMU_CRU_PWR_CON cannot take effect for clock and reset low power flow. If you want to execute clock and reset low power flow, you can program PMU_CRU_PWR_SFTCON through software flow. 1'b0: Disable 1'b1: Enable
6	RW	0x0	pwrgate_bypass Bypass power gating flow in power mode 1 procedure. If asserted, PMU_PWR_GATE_CON0/1/2 cannot take effect for power gating flow. If you want to execute power gating flow, you can program PMU_PWR_GATE_SFTCON0/1/2 through software flow. 1'b0: Disable 1'b1: Enable
5	RW	0x0	ddr_bypass Bypass DDR low power flow in power mode 1 procedure. If asserted, PMU_DDR_CH0/1/2/3_PWR_CON cannot take effect for DDR low power flow. If you want to execute DDR low power flow, you can program PMU_DDR_CH0/1/2/3_PWR_SFTCON through software flow. 1'b0: Disable 1'b1: Enable
4	RW	0x0	bus_bypass Bypass BIU idle request in power mode 1 procedure. If asserted, PMU_BIU_IDLE_CON0/1/2 cannot take effect for BIU idle request. If you want to execute BIU idle request, you can program PMU_BIU_IDLE_SFTCON0/1/2 through software flow. 1'b0: Disable 1'b1: Enable
3:2	RO	0x0	reserved
1	RW	0x0	scu_bypass Bypass SCU low power flow in power mode 1 procedure. 1'b0: Disable 1'b1: Enable
0	R/WSC	0x0	powermode1_en Power mode 1 enable. When controller enters power mode 1 procedure. It is automatically cleared after PMU enters power mode 1 procedure. 1'b0: Disable 1'b1: Enable

PMU1_GLB_POWER_STS

Address: Operational Base(0x20834000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
3:0	RO	0x0	power_state PMU1 global power state. 4'h0: Normal state 4'h1: SCU low power state 4'h2: Q-Channel low power state 4'h3: Bus low power state 4'h4: DDR low power state 4'h5: Power gating low power state 4'h6: Clock and reset low power state 4'h7: PD_PMU1 low power state 4'h8: Sleep state 4'h9: PD_PMU1 active state 4'ha: Clock and reset active state 4'hb: Power gating active state 4'hc: DDR active state 4'hd: Bus active state 4'he: Q-Channel active state 4'hf: SCU active state

PMU1_INT_MASK_CON

Address: Operational Base(0x20834000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	R/WSC	0x0	glb_int_mask Global interrupt mask during SCU sleep state. Cleared when SCU is active. 1'b0: Interrupt is not mask 1'b1: Interrupt is mask

PMU1_WAKEUP_INT_CON

Address: Operational Base(0x20834000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	wakeup_timeout_en Enable PMU wake up timeout as wake up source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
16	RW	0x0	wakeup_aad_en Enable AAD interrupt as wake up source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
15	RW	0x0	wakeup_aov_en Enable AOV interrupt as wake up source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
14	RW	0x0	wakeup_sys_int_en Enable system interrupt as wake up source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
13	RW	0x0	wakeup_hptimer_int_en Enable PMU_HPTIMER interrupt as wake up source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
12	RW	0x0	wakeup_timer_int_en Enable TIMER0 interrupt as wake up source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
11	RW	0x0	wakeup_pwm1_int_en Enable PWM1 interrupt as wake up source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
10	RW	0x0	wakeup_uart0_int_en Enable UART0 interrupt as wake up source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
9	RW	0x0	wakeup_i2c2_int_en Enable I2C2 interrupt as wake up source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
8	RW	0x0	wakeup_usb_int_en Enable USB detect interrupt as wake up source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
7	RW	0x0	wakeup_sdio_int_en Enable SDIO interrupt as wake up source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
6	RW	0x0	wakeup_sdmmc1_int_en Enable SDMMC1 detect interrupt as wake up source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
5	RW	0x0	wakeup_sdmmc0_int_en Enable SDMMC0 detect interrupt as wake up source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
4	RW	0x0	wakeup_gpio0_int_en Enable GPIO0 interrupt as wake up source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3	RW	0x0	wakeup_cpu3_int_en Enable CPU3 interrupt as wakeup source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
2	RW	0x0	wakeup_cpu2_int_en Enable CPU2 interrupt as wakeup source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
1	RW	0x0	wakeup_cpu1_int_en Enable CPU1 interrupt as wakeup source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable
0	RW	0x0	wakeup_cpu0_int_en Enable CPU0 interrupt as wakeup source to exit power mode 1 procedure. 1'b0: Disable 1'b1: Enable

PMU1_WAKEUP_INT_STS

Address: Operational Base(0x20834000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RO	0x0	wakeup_timeout_st Wake up timeout as wake up source status. 1'b0: Inactive 1'b1: Active
16	RW	0x0	wakeup_aad_st AAD interrupt as wake up source status. 1'b0: Inactive 1'b1: Active
15	RW	0x0	wakeup_aov_st AOV interrupt as wake up source status. 1'b0: Inactive 1'b1: Active
14	RO	0x0	wakeup_sys_int_st System interrupt as wake up source status. 1'b0: Inactive 1'b1: Active
13	RO	0x0	wakeup_hptimer_int_st PMU_HPTIMER interrupt as wake up source status. 1'b0: Inactive 1'b1: Active
12	RO	0x0	wakeup_timer_int_st TIMER0 interrupt as wake up source status. 1'b0: Inactive 1'b1: Active
11	RO	0x0	wakeup_pwm1_int_st PWM1 interrupt as wake up source status. 1'b0: Inactive 1'b1: Active

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Bit	Attr	Reset Value	Description
10	RO	0x0	wakeup_uart0_int_st UART0 interrupt as wake up source status. 1'b0: Inactive 1'b1: Active
9	RW	0x0	wakeup_i2c2_int_st I2C2 interrupt as wake up source status. 1'b0: Inactive 1'b1: Active
8	RO	0x0	wakeup_usb_int_st USB interrupt as wake up source status. 1'b0: Inactive 1'b1: Active
7	RO	0x0	wakeup_sdio_int_st SDIO interrupt as wake up source status. 1'b0: Inactive 1'b1: Active
6	RW	0x0	wakeup_sdmmc1_int_st SDMMC1 interrupt as wake up source status. 1'b0: Inactive 1'b1: Active
5	RO	0x0	wakeup_sdmmc0_int_st SDMMC0 interrupt as wake up source status. 1'b0: Inactive 1'b1: Active
4	RO	0x0	wakeup_gpio0_int_st GPIO0 interrupt as wake up source status. 1'b0: Inactive 1'b1: Active
3	RW	0x0	wakeup_cpu3_int_st CPU3 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
2	RW	0x0	wakeup_cpu2_int_st CPU2 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
1	RW	0x0	wakeup_cpu1_int_st CPU1 interrupt as wakeup source status. 1'b0: Inactive 1'b1: Active
0	RW	0x0	wakeup_cpu0_int_st CPU0 interrupt as wake up source status. 1'b0: Inactive 1'b1: Active

PMU1_WAKEUP_EDGE_CON

Address: Operational Base(0x20834000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	edge_wakeup_en Enable both posedge and negedge of GPIO0 pins as wakeup source. Each pin has independent control bit. 1'b0: Disable 1'b1: Enable

PMU1_WAKEUP_EDGE_ST

Address: Operational Base(0x20834000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	edge_status Edge interrupt wakeup status. Each pin has independent control bit. 1'b0: Inactive 1'b1: Active

PMU1_WAKEUP_TIMEOUT_CNT_STATUS

Address: Operational Base(0x20834000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	wakeup_timeout_counter_status wakeup timeout counter can be checked by this register.

PMU1_DDR_CH0_PWR_CON

Address: Operational Base(0x20834000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	ddrphy_auto_gating_ena Enable DDRPHY auto clock gating. DDRPHY's clock can be gated when in sleep mode. 1'b0: Disable 1'b1: Enable
5	RW	0x0	ddrctl_c_auto_gating_ena Enable DDRCTRL's core-clock auto clock gating. Core-clock can be gated when in self-refresh mode. 1'b0: Disable 1'b1: Enable
4	RW	0x0	ddrio_rstiov_exit_ena Enable DDR exits retention mode through RST_IOV by hardware. 1'b0: Disable 1'b1: Enable
3	RW	0x0	ddrio_rstiov_enter_ena Enable DDR enters retention mode through RST_IOV by hardware. 1'b0: Disable 1'b1: Enable
2	RW	0x0	ddrio_reton_exit_ena Enable DDR exits retention mode through RETON/RETOFF by hardware. 1'b0: Disable 1'b1: Enable
1	RW	0x0	ddrio_reton_enter_ena Enable DDR enters retention mode through RETON/RETOFF by hardware. 1'b0: Disable 1'b1: Enable
0	RW	0x0	ddr_sref_c_ena Enable DDR self-refresh mode for core-clock domain by hardware. 1'b0: Disable 1'b1: Enable

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PMU1_DDR_CH0_PWR_SFTCON
Address: Operational Base(0x20834000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	ddrctl_c_active_wait_enter 1'b0: Not need to wait for ddrctl_c_active low before FSM enter self-refresh state 1'b1: Need to wait for ddrctl_c_active low before FSM enter self-refresh state
5	RW	0x0	ddrctl_c_active_wait_exit 1'b0: Not need to wait for ddrctl_c_active high before FSM exit self-refresh state 1'b1: Need to wait for ddrctl_c_active high before FSM exit self-refresh state
4	R/WSC	0x0	ddrio_rstiov_exit_sftena Enable DDR exits retention mode through RST_IOV by software. It is auto cleared after DDR exits retention mode. 1'b0: Disable 1'b1: Enable
3	RW	0x0	ddrio_rstiov_enter_sftena Enable DDR enters retention mode through RST_IOV by software. 1'b0: Disable 1'b1: Enable
2	R/WSC	0x0	ddrio_reton_exit_sftena Enable DDR exits retention mode through RETON/RETOFF by software. It is auto cleared after DDR exits retention mode. 1'b0: Disable 1'b1: Enable
1	RW	0x0	ddrio_reton_enter_sftena Enable DDR enters retention mode through RETON/RETOFF by software. 1'b0: Disable 1'b1: Enable
0	RW	0x0	ddr_sref_c_sftena Enable DDR self-refresh mode for core-clock domain by software. 1'b0: Disable 1'b1: Enable

PMU1_DDR_AXIPWR_CON0
Address: Operational Base(0x20834000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	ddr_sref_a_ena Enable DDR self-refresh mode for AXI-clock domain by hardware. Bit[i] used for AXI-clock channel i, i=0~3. 1'b0: Disable 1'b1: Enable

PMU1_DDR_AXIPWR_SFTCON0

Address: Operational Base(0x20834000) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3:0	RW	0x0	ddr_sref_a_sftena Enable DDR self-refresh mode for AXI-clock domain by software. Bit[i] used for AXI-clock channel i, i=0~3. 1'b0: Disable 1'b1: Enable

PMU1_DDR_AXIPWR_SFTCON1

Address: Operational Base(0x20834000) + offset (0x0134)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3:0	RW	0x0	ddrctl_a_active_wait_enter Bit[i] used for AXI-clock channel i, i=0~3. 1'b0: Not need to wait for ddrctl_a_active low before FSM enter self-refresh state 1'b1: Need to wait for ddrctl_a_active low before FSM enter self-refresh state

PMU1_DDR_AXIPWR_SFTCON2

Address: Operational Base(0x20834000) + offset (0x0138)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3:0	RW	0x0	ddrctl_a_active_wait_exit Bit[i] used for AXI-clock channel i, i=0~3. 1'b0: Not need to wait for ddrctl_a_active high before FSM exit self-refresh state 1'b1: Need to wait for ddrctl_a_active high before FSM exit self-refresh state

PMU1_DDR_POWER_STS

Address: Operational Base(0x20834000) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
3:0	RO	0x0	ddr_power_state DDR power state. 4'h0: Normal state 4'h1: Enter self-refresh mode for AXI-clock state 4'h2: Enter self-refresh mode core-clock state 4'h3: Enter retention mode through RETON/RETOFF state 4'h4: Enter retention mode through RST_IOV state 4'h5: Sleep state 4'h6: Exit retention mode through RST_IOV state 4'h7: Exit retention mode through RETON/RETOFF state 4'h8: Exit self-refresh mode for core-clock state 4'h9: Exit self-refresh mode for AXI-clock state Others: Reserved

PMU1_DDR_STS

Address: Operational Base(0x20834000) + offset (0x0144)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RO	0x0	ddrctrl_c_sysactive_ch0 DDRC hardware low-power clock active for channel 0. 1'b0: Inactive 1'b1: Active
2	RO	0x0	ddrctrl_c_sysack_ch0 DDRC hardware low-power request acknowledge for channel 0. 1'b0: Inactive 1'b1: Active
1	RO	0x0	ddr_io_rstiov_ch0 DDR RST_IOV state for channel 0. 1'b0: Inactive 1'b1: Active
0	RO	0x0	ddr_io_reton_ch0 DDR RETON/RETOFF state for channel 0. 1'b0: Inactive 1'b1: Active

PMU1_DDR_AXI_STS

Address: Operational Base(0x20834000) + offset (0x0148)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	ddrctrl_a_sysactive_ch3 DDRC AXI clock active for channel 3. 1'b0: Inactive 1'b1: Active
6	RO	0x0	ddrctrl_a_sysack_ch3 DDRC AXI hardware low-power request acknowledge for channel 3. 1'b0: Inactive 1'b1: Active
5	RO	0x0	ddrctrl_a_sysactive_ch2 DDRC AXI clock active for channel 2. 1'b0: Inactive 1'b1: Active

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Bit	Attr	Reset Value	Description
4	RO	0x0	ddrctrl_a_sysack_ch2 DDRC AXI hardware low-power request acknowledge for channel 2. 1'b0: Inactive 1'b1: Active
3	RO	0x0	ddrctrl_a_sysactive_ch1 DDRC AXI clock active for channel 1. 1'b0: Inactive 1'b1: Active
2	RO	0x0	ddrctrl_a_sysack_ch1 DDRC AXI hardware low-power request acknowledge for channel 1. 1'b0: Inactive 1'b1: Active
1	RO	0x0	ddrctrl_a_sysactive_ch0 DDRC AXI clock active for channel 0. 1'b0: Inactive 1'b1: Active
0	RO	0x0	ddrctrl_a_sysack_ch0 DDRC AXI hardware low-power request acknowledge for channel 0. 1'b0: Inactive 1'b1: Active

PMU1_CRU_PWR_CON0

Address: Operational Base(0x20834000) + offset (0x0200)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	pwm_clk_gate_ena Enable clock gating when pwm_switch. 1'b0: Disable 1'b1: Enable
8	RW	0x0	pwm_switch_iout PWM output. 1'b0: Disable 1'b1: Enable
7	RW	0x0	pwm_gpio_ioe_ena PWM output enable. 1'b0: Disable 1'b1: Enable
6	RW	0x0	pwm_switch_ena PWM switch enable. 1'b0: Disable 1'b1: Enable
5	RW	0x0	power_off_ena Enable chip power off by hardware. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
4	RW	0x0	alive_osc_ena Enable clk_pmu/hclk_pmu/pclk_pmu switch to oscillator by hardware. When alive_32k_ena is asserted, this bit is ignored. 1'b0: Disable 1'b1: Enable
3	RW	0x0	input_clamp_ena Enable VD_PMU input clamped by hardware. 1'b0: Disable 1'b1: Enable
2	RW	0x0	wakeup_rst_ena Enable wake up reset by hardware. If asserted, all registers without reset hold will be reset after chip wake up. 1'b0: Disable 1'b1: Enable
1	RW	0x0	osc_dis_ena Disable oscillator by hardware. 1'b0: Enable 1'b1: Disable
0	RW	0x0	alive_32k_ena Enable pclk_pmu and clk_pmu switch to 32KHz clock by hardware. 1'b0: Disable 1'b1: Enable

PMU1_CRU_PWR_CON1

Address: Operational Base(0x20834000) + offset (0x0204)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	pd_bus_clk_src_gate_ena Gating BIU_BUS's clock source during clock low power mode. 1'b0: Disable 1'b1: Enable
8	RW	0x0	pd_ddr_clk_src_gate_ena Gating BIU_DDR's clock source during clock low power mode. 1'b0: Disable 1'b1: Enable
7	RW	0x0	pd_core_clk_src_gate_ena Gating BIU_CORE's clock source during clock low power mode. 1'b0: Disable 1'b1: Enable
6	RW	0x0	pd_aiisp_clk_src_gate_ena Gating BIU_AIISP's clock source during clock low power mode. 1'b0: Disable 1'b1: Enable
5	RW	0x0	pd_vdo_clk_src_gate_ena Gating BIU_VDO's clock source during clock low power mode. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
4	RW	0x0	pd_npu_clk_src_gate_ena Gating BIU_NPU's clock source during clock low power mode. 1'b0: Disable 1'b1: Enable
3	RW	0x0	pd_vi_clk_src_gate_ena Gating BIU_VI's clock source during clock low power mode. 1'b0: Disable 1'b1: Enable
2	RW	0x0	pd_vcp_clk_src_gate_ena Gating BIU_VCP's clock source during clock low power mode. 1'b0: Disable 1'b1: Enable
1	RW	0x0	pd_vepu_clk_src_gate_ena Gating BIU_VEPU's clock source during clock low power mode. 1'b0: Disable 1'b1: Enable
0	RW	0x0	pd_peri_clk_src_gate_ena Gating BIU_PERI's clock source during clock low power mode. 1'b0: Disable 1'b1: Enable

PMU1_CRU_PWR_SFTCON

Address: Operational Base(0x20834000) + offset (0x0208)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	power_off_sftena Enable chip power off by software. 1'b0: Disable 1'b1: Enable
4	RW	0x0	alive_osc_sftena Enable clk_pmu/hclk_pmu/pclk_pmu switch to oscillator by software. When alive_32k_ena is asserted, this bit is ignored. 1'b0: Disable 1'b1: Enable
3	RW	0x0	input_clamp_sftena Enable VD_PMU input clamp by software. 1'b0: Disable 1'b1: Enable
2	RW	0x0	wakeup_rst_sftena Enable wake up reset by software. If asserted, all digital except IP with reset hold will be reset. 1'b0: Disable 1'b1: Enable
1	RW	0x0	osc_dis_sftena Disable oscillator by software. 1'b0: Enable 1'b1: Disable

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Bit	Attr	Reset Value	Description
0	RW	0x0	alive_32k_sftena Enable pclk_pmu and clk_pmu switch to 32KHz clock by software. 1'b0: Disable 1'b1: Enable

PMU1_CRU_PWR_SFTCON1

Address: Operational Base(0x20834000) + offset (0x020C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	pd_bus_clk_src_gate_sftena Gating BIU_BUS's clock source by software. 1'b0: Disable 1'b1: Enable
8	RW	0x0	pd_ddr_clk_src_gate_sftena Gating BIU_DDR's clock source by software. 1'b0: Disable 1'b1: Enable
7	RW	0x0	pd_core_clk_src_gate_sftena Gating BIU_CORE's clock source by software. 1'b0: Disable 1'b1: Enable
6	RW	0x0	pd_aiisp_clk_src_gate_sftena Gating BIU_AIISP's clock source by software. 1'b0: Disable 1'b1: Enable
5	RW	0x0	pd_vdo_clk_src_gate_sftena Gating BIU_VDO's clock source by software. 1'b0: Disable 1'b1: Enable
4	RW	0x0	pd_npu_clk_src_gate_sftena Gating BIU_NPU's clock source by software. 1'b0: Disable 1'b1: Enable
3	RW	0x0	pd_vi_clk_src_gate_sftena Gating BIU_VI's clock source by software. 1'b0: Disable 1'b1: Enable
2	RW	0x0	pd_vcp_clk_src_gate_sftena Gating BIU_VCP's clock source by software. 1'b0: Disable 1'b1: Enable
1	RW	0x0	pd_vepu_clk_src_gate_sftena Gating BIU_VEPU's clock source by software. 1'b0: Disable 1'b1: Enable
0	RW	0x0	pd_peri_clk_src_gate_sftena Gating BIU_PERI's clock source by software. 1'b0: Disable 1'b1: Enable

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PMU1_CRU_POWER_STS
Address: Operational Base(0x20834000) + offset (0x0210)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RO	0x0	cru_power_state Clock and reset power state. 4'h0: Normal state 4'h1: Clock low frequency state 4'h2: PLL power down state 4'h3: IO sleep state 4'h4: Input clamp state 4'h5: Oscillator disable state 4'h6: Sleep state 4'h7: Wake up state 4'h8: Oscillator enable state 4'h9: Input clamp release state 4'ha: Clock high frequency state 4'hb: Wake up reset clear state 4'hc: IO wake up state 4'hd: GPIO switch state 4'he: PLL power up state 4'hf: PWM switch state Others: Reserved

PMU1_PLLPD_CON0
Address: Operational Base(0x20834000) + offset (0x0220)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	ppll_pd_ena Enable power down PPLL by hardware. 1'b0: Disable 1'b1: Enable
2	RW	0x0	cpll_pd_ena Enable power down CPLL by hardware. 1'b0: Disable 1'b1: Enable
1	RW	0x0	dpll_pd_ena Enable power down DPLL by hardware. 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpll_pd_ena Enable power down GPLL by hardware. 1'b0: Disable 1'b1: Enable

PMU1_PLLPD_SFTCON0
Address: Operational Base(0x20834000) + offset (0x0228)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
3	RW	0x0	ppll_pd_sftena Enable power down PPLL by software. 1'b0: Disable 1'b1: Enable
2	RW	0x0	cpll_pd_sftena Enable power down CPLL by software. 1'b0: Disable 1'b1: Enable
1	RW	0x0	dpll_pd_sftena Enable power down DPLL by software. 1'b0: Disable 1'b1: Enable
0	RW	0x0	gpll_pd_sftena Enable power down GPLL by software. 1'b0: Disable 1'b1: Enable

PMU1_PMIC_STABLE_CNT

Address: Operational Base(0x20834000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	pmic_stable_cnt PMIC stable count for mode 1 procedure. Number of clk_pmu used by counter logic.

PMU1_OSC_STABLE_CNT

Address: Operational Base(0x20834000) + offset (0x0304)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	osc_stable_cnt Oscillator stable count for mode 1 procedure. Number of clk_pmu used by counter logic.

PMU1_WAKEUP_RST_CLR_CNT

Address: Operational Base(0x20834000) + offset (0x0308)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	wakeup_rst_clr_cnt Wake up reset clear count for mode 1 procedure. Number of clk_pmu used by counter logic.

PMU1_PLL_LOCK_CNT

Address: Operational Base(0x20834000) + offset (0x030C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	pll_lock_cnt Count for PLL from power up to lock. Number of clk_pmu used by counter logic.

PMU1_WAKEUP_TIMEOUT_CNT

Address: Operational Base(0x20834000) + offset (0x0310)

Bit	Attr	Reset Value	Description
31:0	RW	0x00005dc0	wakeup_timeout_cnt Wake up timeout count. Number of clk_pmu used by counter logic.

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PMU1_PWM_SWITCH_CNT
Address: Operational Base(0x20834000) + offset (0x0314)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	pwm_switch_cnt PWM switch count. Number of clk_pmu used by counter logic.

PMU1_SLEEP_CNT
Address: Operational Base(0x20834000) + offset (0x0318)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sleep_cnt_thresh PMU sleep counter thresh. Number of clk_pmu used by counter logic. The counter start counting when PMU is in ST_SLEEP and sleep_cnt_en is enable. After counter equal to counter thresh, PMU can be waked up by wakeup_source.

PMU2_SCU_PWR_CON0
Address: Operational Base(0x20838000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x1	standbywfil2_bypass_ena L2 standbywfi bypass enable for SCU enter low power mode. 1'b0: Disable 1'b1: Enable. SCU not needs wait for L2 standbywfi state before execute low power procedure.
8	RW	0x0	standbywfi_bypass_ena CPU standbywfi bypass enable for SCU enter low power mode. 1'b0: Disable 1'b1: Enable. SCU not needs wait for CPU standbywfi state before execute low power procedure.
7:6	RO	0x0	reserved
5	RW	0x0	cluster_cpu_pwrdn_ena Enable all cpu power down by hardware. 1'b0: Disable 1'b1: Enable
4	RO	0x0	reserved
3	RW	0x0	scu_pwroff_ena Enable SCU power off by hardware. Indicate the PMIC to cut off the scu power. 1'b0: Disable 1'b1: Enable
2	RW	0x0	scu_pwrdn_ena Enable SCU power down by hardware. 1'b0: Disable 1'b1: Enable
1	RW	0x0	l2_idle_ena Enable sending l2 idle request by hardware. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
0	RW	0x0	l2_flush_ena Enable sending l2 flush request by hardware. 1'b0: Disable 1'b1: Enable

PMU2_SCU_PWR_SFTCON

Address: Operational Base(0x20838000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	RW	0x0	pd_scu_dwn_ack_sel pd_scu_dwn_ack source selection. 1'b0: pd_scu_dwn_ack is from power switch. 1'b1: pd_scu_dwn_ack is generated by PMU.
5	RW	0x0	scu_vol_gate_sftcon Indicate that SCU is acting as a VD and also a PD. 1'b0: pd_scu_dwn_ack_clamp_n is not used. 1'b1: pd_scu_dwn_ack_clamp_n is equal to pd_scu_dwn_clamp_n
4	RO	0x0	reserved
3	RW	0x0	scu_pwroff_cfg Enable SCU power off by software. 1'b0: Disable 1'b1: Enable
2	RW	0x0	scu_pwrdn_req_cfg Enable SCU power down by software. 1'b0: Disable 1'b1: Enable
1	RW	0x0	acinactm_cluster_cfg Enable sending l2 idle request by software. 1'b0: Disable 1'b1: Enable
0	RW	0x0	l2flushreq_cluster_cfg Enable sending l2 flush request by software. 1'b0: Disable 1'b1: Enable

PMU2_SCU_AUTO_PWR_CON

Address: Operational Base(0x20838000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	scu_sft_wakeup_cluster_ena SCU software wakeup enable. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
2	RW	0x0	scu_int_mask_ena SCU interrupt mask enable. 1'b0: Disable 1'b1: Enable
1	RW	0x0	scu_int_wakeup_cluster_ena SCU interrupt wakeup enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	scu_lp_en Enable SCU low-power procedure by hardware. Start when all core enter WFI, Cleared when SCU wakeup. 1'b0: Disable 1'b1: Enable

PMU2_SCU_PWR_STATE

Address: Operational Base(0x20838000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RO	0x0	scu_power_state SCU power state. 4'h0: SCU normal state 4'h1: CPU power down state 4'h2: L2 flush state 4'h3: L2 idle state 4'h4: Cluster transfer idle state 4'h5: SCU power down state 4'h6: SCU sleep state 4'h7: SCU wakeup state 4'h8: SCU power up state 4'h9: Cluster transfer resume state 4'ha: CPU power up state Others: Reserved

PMU2_DBG_PWR_CON

Address: Operational Base(0x20838000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	cpu3_dbgnopwrdwn_ena CPU3 dbgnopwrdwn check enable. 1'b0: Disable 1'b1: Enable
6	RW	0x0	cpu3_dbgpwrupreq_ena CPU3 dbgpwrupreq check enable. 1'b0: Disable 1'b1: Enable
5	RW	0x0	cpu2_dbgnopwrdwn_ena CPU2 dbgnopwrdwn check enable. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
4	RW	0x0	cpu2_dbgpwrupreq_ena CPU2 dbgpwrupreq check enable. 1'b0: Disable 1'b1: Enable
3	RW	0x0	cpu1_dbgnopwrdwn_ena CPU1 dbgnopwrdwn check enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	cpu1_dbgpwrupreq_ena CPU1 dbgpwrupreq check enable. 1'b0: Disable 1'b1: Enable
1	RW	0x0	cpu0_dbgnopwrdwn_ena CPU0 dbgnopwrdwn check enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	cpu0_dbgpwrupreq_ena CPU0 dbgpwrupreq check enable. 1'b0: Disable 1'b1: Enable

PMU2_CLUSTER_PWR_ST

Address: Operational Base(0x20838000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RO	0x0	scu_dwn_state SCU power down state. 1'b0: Inactive 1'b1: Active
11	RW	0x0	cpu3_dwn_state CPU3 power down state. 1'b0: Inactive 1'b1: Active
10	RW	0x0	cpu2_dwn_state CPU2 power down state. 1'b0: Inactive 1'b1: Active
9	RW	0x0	cpu1_dwn_state CPU1 power down state. 1'b0: Inactive 1'b1: Active
8	RO	0x0	cpu0_dwn_state CPU0 power down state. 1'b0: Inactive 1'b1: Active
7:6	RO	0x0	reserved
5	RO	0x0	l2flushdone L2 flushdone state. 1'b0: Inactive 1'b1: Active
4	RO	0x0	standbywfil2 L2 STANDBYWFI state. 1'b0: Inactive 1'b1: Active

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Bit	Attr	Reset Value	Description
3	RO	0x0	cpu3_standbywfi CPU3 STANDBYWFI state. 1'b0: Inactive 1'b1: Active
2	RO	0x0	cpu2_standbywfi CPU2 STANDBYWFI state. 1'b0: Inactive 1'b1: Active
1	RO	0x0	cpu1_standbywfi CPU1 STANDBYWFI state. 1'b0: Inactive 1'b1: Active
0	RO	0x0	cpu0_standbywfi CPU0 STANDBYWFI state. 1'b0: Inactive 1'b1: Active

PMU2_CLUSTER_IDLE_CON

Address: Operational Base(0x20838000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	core_gate_mask_ena Enable sending clock gating mask to BIU_CPU by PMU. 1'b0: Disable 1'b1: Enable
2	RW	0x0	idle_req_cpu Enable sending bus idle request to BIU_CPU by PMU. 1'b0: Disable 1'b1: Enable
1:0	RO	0x0	reserved

PMU2_CLUSTER_IDLE_SFTCON

Address: Operational Base(0x20838000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	cpu_gate_mask_ena Enable sending clock gating mask to BIU_CPU by software. 1'b0: Disable 1'b1: Enable
2	RW	0x0	idle_req_cpu Enable sending bus idle request to BIU_CPU by software. 1'b0: Disable 1'b1: Enable
1:0	RO	0x0	reserved

PMU2_CLUSTER_IDLE_ACK

Address: Operational Base(0x20838000) + offset (0x0028)

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Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	cluster_biu_idle_ack BIU_CORE idle acknowledge state. 1'b0: Inactive 1'b1: Active

PMU2_CLUSTER_IDLE_ST

Address: Operational Base(0x20838000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	cluster_biu_idle BIU_CORE idle state. 1'b0: Inactive 1'b1: Active

PMU2_SCU_PWRUP_CNT

Address: Operational Base(0x20838000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x05dc0	stable_cnt SCU power up stable counter, reflect on the falling time of pd_scu_dwn_ack.

PMU2_SCU_PWRDN_CNT

Address: Operational Base(0x20838000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x05dc0	stable_cnt SCU power down stable counter, reflect on the rising time of pd_scu_dwn_ack.

PMU2_SCU_STABLE_CNT

Address: Operational Base(0x20838000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	stable_cnt SCU power stable counter for SCU from power off to wakeup.

PMU2_CPU_AUTO_PWR_CON0

Address: Operational Base(0x20838000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	cpu0_cluster_wakeup_ena 1'b0: CPU wakeup by interrupt 1'b1: CPU wakeup when SCU_LP state entering CPU power up state
4	RW	0x0	cpu0_auto_pwrdn_mode 1'b0: CPU is power down after CPU enter WFI 1'b1: CPU is power down after CPU exit WFI

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Bit	Attr	Reset Value	Description
3	RW	0x0	cpu0_sft_wakeup_cluster_ena CPU0 software wakeup enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	cpu0_int_mask_ena CPU0 interrupt mask enable. 1'b0: Disable 1'b1: Enable
1	RW	0x0	cpu0_int_wakeup_ena CPU0 interrupt wakeup enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	cpu0_auto_pwrdn_ena CPU0 auto power down enable. 1'b0: Disable 1'b1: Enable

PMU2_CPU_AUTO_PWR_CON1
Address: Operational Base(0x20838000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	cpu1_cluster_wakeup_ena 1'b0: CPU wakeup by interrupt 1'b1: CPU wakeup when SCU_LP state entering CPU power up state
4	RW	0x0	cpu1_auto_pwrdn_mode 1'b0: CPU is power down after CPU enter WFI 1'b1: CPU is power down after CPU exit WFI
3	RW	0x0	cpu1_sft_wakeup_cluster_ena CPU1 software wakeup enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	cpu1_int_mask_ena CPU1 interrupt mask enable. 1'b0: Disable 1'b1: Enable
1	RW	0x0	cpu1_int_wakeup_ena CPU1 interrupt wakeup enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	cpu1_auto_pwrdn_ena CPU1 auto power down enable. 1'b0: Disable 1'b1: Enable

PMU2_CPU_AUTO_PWR_CON2
Address: Operational Base(0x20838000) + offset (0x0088)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	cpu2_cluster_wakeup_ena 1'b0: CPU wakeup by interrupt 1'b1: CPU wakeup when SCU_LP state entering CPU power up state
4	RW	0x0	cpu2_auto_pwrdn_mode 1'b0: CPU is power down after CPU enter WFI 1'b1: CPU is power down after CPU exit WFI
3	RW	0x0	cpu2_sft_wakeup_cluster_ena CPU2 software wakeup enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	cpu2_int_mask_ena CPU2 interrupt mask enable. 1'b0: Disable 1'b1: Enable
1	RW	0x0	cpu2_int_wakeup_ena CPU2 interrupt wakeup enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	cpu2_auto_pwrdn_ena CPU2 auto power down enable. 1'b0: Disable 1'b1: Enable

PMU2_CPU_AUTO_PWR_CON3

Address: Operational Base(0x20838000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	cpu3_cluster_wakeup_ena 1'b0: CPU wakeup by interrupt 1'b1: CPU wakeup when SCU_LP state entering CPU power up state
4	RW	0x0	cpu3_auto_pwrdn_mode 1'b0: CPU is power down after CPU enter WFI 1'b1: CPU is power down after CPU exit WFI
3	RW	0x0	cpu3_sft_wakeup_cluster_ena CPU3 software wakeup enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	cpu3_int_mask_ena CPU3 interrupt mask enable. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
1	RW	0x0	cpu3_int_wakeup_ena CPU3 interrupt wakeup enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	cpu3_auto_pwrdn_ena CPU3 auto power down enable. 1'b0: Disable 1'b1: Enable

PMU2_CPU_PWR_SFTCON0
Address: Operational Base(0x20838000) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	cpu0_sft_pwrdn_ena CPU0 software power down enable. 1'b0: Disable 1'b1: Enable

PMU2_CPU_PWR_SFTCON1
Address: Operational Base(0x20838000) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	cpu1_sft_pwrdn_ena CPU1 software power down enable. 1'b0: Disable 1'b1: Enable

PMU2_CPU_PWR_SFTCON2
Address: Operational Base(0x20838000) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	cpu2_sft_pwrdn_ena CPU2 software power down enable. 1'b0: Disable 1'b1: Enable

PMU2_CPU_PWR_SFTCON3
Address: Operational Base(0x20838000) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:1	RO	0x0000	reserved
0	RW	0x0	cpu3_sft_pwrdn_ena CPU3 software power down enable. 1'b0: Disable 1'b1: Enable

PMU2_BIU_IDLE_CON0

Address: Operational Base(0x20838000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	idle_req_bus_ena Enable sending idle request to BIU_BUS by hardware. 1'b0: Disable 1'b1: Enable
10	RW	0x0	idle_req_aiisp_ena Enable sending idle request to BIU_AIISP by hardware. 1'b0: Disable 1'b1: Enable
9	RW	0x0	idle_req_vdo_ena Enable sending idle request to BIU_VDO by hardware. 1'b0: Disable 1'b1: Enable
8	RW	0x0	idle_req_npu_ena Enable sending idle request to BIU_NPU by hardware. 1'b0: Disable 1'b1: Enable
7	RW	0x0	idle_req_cru_ena Enable sending idle request to BIU_CRU by hardware. 1'b0: Disable 1'b1: Enable
6	RW	0x0	idle_req_vi_ena Enable sending idle request to BIU_VI by hardware. 1'b0: Disable 1'b1: Enable
5	RW	0x0	idle_req_vcp_ena Enable sending idle request to BIU_VCP by hardware. 1'b0: Disable 1'b1: Enable
4	RW	0x0	idle_req_vepu_ena Enable sending idle request to BIU_VEPU by hardware. 1'b0: Disable 1'b1: Enable
3	RW	0x0	idle_req_peri_ena Enable sending idle request to BIU_PERI by hardware. 1'b0: Disable 1'b1: Enable
2	RW	0x0	idle_req_cfgddr_ena Enable sending idle request to BIU_CFGDDR by hardware. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
1	RW	0x0	idle_req_subddr_ena Enable sending idle request to BIU_SUBDDR by hardware. 1'b0: Disable 1'b1: Enable
0	RW	0x0	idle_req_ddr_ena Enable sending idle request to BIU_DDR by hardware. 1'b0: Disable 1'b1: Enable

PMU2_BIU_IDLE_SFTCON0

Address: Operational Base(0x20838000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	idle_req_bus_sftena Enable sending idle request to BIU_BUS by software. 1'b0: Disable 1'b1: Enable
10	RW	0x0	idle_req_aiisp_sftena Enable sending idle request to BIU_AIISP by software. 1'b0: Disable 1'b1: Enable
9	RW	0x0	idle_req_vdo_sftena Enable sending idle request to BIU_VDO by software. 1'b0: Disable 1'b1: Enable
8	RW	0x0	idle_req_npu_sftena Enable sending idle request to BIU_NPU by software. 1'b0: Disable 1'b1: Enable
7	RW	0x0	idle_req_cru_sftena Enable sending idle request to BIU_CRU by software. 1'b0: Disable 1'b1: Enable
6	RW	0x0	idle_req_vi_sftena Enable sending idle request to BIU_VI by software. 1'b0: Disable 1'b1: Enable
5	RW	0x0	idle_req_vcp_sftena Enable sending idle request to BIU_VCP by software. 1'b0: Disable 1'b1: Enable
4	RW	0x0	idle_req_vepu_sftena Enable sending idle request to BIU_VEPU by software. 1'b0: Disable 1'b1: Enable
3	RW	0x0	idle_req_peri_sftena Enable sending idle request to BIU_PERI by software. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
2	RW	0x0	idle_req_cfgddr_sftena Enable sending idle request to BIU_CFGDDR by software. 1'b0: Disable 1'b1: Enable
1	RW	0x0	idle_req_subddr_sftena Enable sending idle request to BIU_SUBDDR by software. 1'b0: Disable 1'b1: Enable
0	RW	0x0	idle_req_ddr_sftena Enable sending idle request to BIU_DDR by software. 1'b0: Disable 1'b1: Enable

PMU2_BIU_IDLE_ACK_STS0

Address: Operational Base(0x20838000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RW	0x0	idle_ack_bus BIU_BUS idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
10	RW	0x0	idle_ack_aiisp BIU_AIISP idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
9	RW	0x0	idle_ack_vdo BIU_VDO idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
8	RW	0x0	idle_ack_npu BIU_NPU idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
7	RW	0x0	idle_ack_cru BIU_CRU idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
6	RW	0x0	idle_ack_vi BIU_VI idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
5	RO	0x0	idle_ack_vcp BIU_VCP idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
4	RO	0x0	idle_ack_vepu BIU_VEPU idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
3	RO	0x0	idle_ack_peri BIU_PERI idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge

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Bit	Attr	Reset Value	Description
2	RO	0x0	idle_ack_cfgddr BIU_CFGDDR idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
1	RO	0x0	idle_ack_subddr BIU_SUBDDR idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge
0	RO	0x0	idle_ack_ddr BIU_DDR idle acknowledge state. 1'b0: Not acknowledge 1'b1: Acknowledge

PMU2_BIU_IDLE_STS0

Address: Operational Base(0x20838000) + offset (0x0128)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RW	0x0	idle_bus BIU_BUS idle state. 1'b0: Not idle 1'b1: Idle
10	RW	0x0	idle_aiisp BIU_AIISP idle state. 1'b0: Not idle 1'b1: Idle
9	RW	0x0	idle_vdo BIU_VDO idle state. 1'b0: Not idle 1'b1: Idle
8	RW	0x0	idle_npu BIU_NPU idle state. 1'b0: Not idle 1'b1: Idle
7	RW	0x0	idle_cru BIU_CRU idle state. 1'b0: Not idle 1'b1: Idle
6	RW	0x0	idle_vi BIU_VI idle state. 1'b0: Not idle 1'b1: Idle
5	RO	0x0	idle_vcp BIU_VCP idle state. 1'b0: Not idle 1'b1: Idle
4	RO	0x0	idle_vepu BIU_VEPU idle state. 1'b0: Not idle 1'b1: Idle
3	RO	0x0	idle_peri BIU_PERI idle state. 1'b0: Not idle 1'b1: Idle

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Bit	Attr	Reset Value	Description
2	RO	0x0	idle_cfgddr BIU_CFGDDR idle state. 1'b0: Not idle 1'b1: Idle
1	RO	0x0	idle_subddr BIU_SUBDDR idle state. 1'b0: Not idle 1'b1: Idle
0	RO	0x0	idle_ddr BIU_DDR idle state. 1'b0: Not idle 1'b1: Idle

PMU2_BIU_GATEMASK_CON0

Address: Operational Base(0x20838000) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	biu_auto_bus_ena If enable, BIU_BUS corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
10	RW	0x0	biu_auto_aiisp_ena If enable, BIU_AIISP corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
9	RW	0x0	biu_auto_vdo_ena If enable, BIU_VDO corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
8	RW	0x0	biu_auto_npu_ena If enable, BIU_NPU corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
7	RW	0x0	biu_auto_cru_ena If enable, BIU_CRU corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
6	RW	0x0	biu_auto_vi_ena If enable, BIU_VI corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
5	RW	0x0	biu_auto_vcp_ena If enable, BIU_VCP corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
4	RW	0x0	biu_auto_vepu_ena If enable, BIU_VEPU corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
3	RW	0x0	biu_auto_peri_ena If enable, BIU_PERI corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
2	RW	0x0	biu_auto_cfgddr_ena If enable, BIU_CFGDDR corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
1	RW	0x0	biu_auto_subddr_ena If enable, BIU_SUBDDR corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable
0	RW	0x0	biu_auto_ddr_ena If enable, BIU_DDR corresponding clock can be opened or gated automatically when idle operation. 1'b0: Disable 1'b1: Enable

PMU2_BIU_GATEMASK_SFTCON0

Address: Operational Base(0x20838000) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	biu_bus_sftena If enable, BIU_BUS corresponding clock can not be gated. 1'b0: Disable 1'b1: Enable
10	RW	0x0	biu_aiisp_sftena If enable, BIU_AIISP corresponding clock can not be gated. 1'b0: Disable 1'b1: Enable
9	RW	0x0	biu_vdo_sftena If enable, BIU_VDO corresponding clock can not be gated. 1'b0: Disable 1'b1: Enable
8	RW	0x0	biu_npu_sftena If enable, BIU_NPU corresponding clock can not be gated. 1'b0: Disable 1'b1: Enable
7	RW	0x0	biu_cru_sftena If enable, BIU_CRU corresponding clock can not be gated. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
6	RW	0x0	biu_vi_sftena If enable, BIU_VI corresponding clock can not be gated. 1'b0: Disable 1'b1: Enable
5	RW	0x0	biu_vcp_sftena If enable, BIU_VCP corresponding clock can not be gated. 1'b0: Disable 1'b1: Enable
4	RW	0x0	biu_vepu_sftena If enable, BIU_VEPU corresponding clock can not be gated. 1'b0: Disable 1'b1: Enable
3	RW	0x0	biu_peri_sftena If enable, BIU_PERI corresponding clock can not be gated. 1'b0: Disable 1'b1: Enable
2	RW	0x0	biu_cfgddr_sftena If enable, BIU_CFGDDR corresponding clock can not be gated. 1'b0: Disable 1'b1: Enable
1	RW	0x0	biu_subddr_sftena If enable, BIU_SUBDDR corresponding clock can not be gated. 1'b0: Disable 1'b1: Enable
0	RW	0x0	biu_ddr_sftena If enable, BIU_DDR corresponding clock can not be gated. 1'b0: Disable 1'b1: Enable

PMU2_PWR_GATE_CON0
Address: Operational Base(0x20838000) + offset (0x0200)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2	RW	0x0	pd_aiisp_dwn_ena Enable power down PD_AIISP by hardware. 1'b0: Disable 1'b1: Enable
1	RW	0x0	pd_vdo_dwn_ena Enable power down PD_VDO by hardware. 1'b0: Disable 1'b1: Enable
0	RW	0x0	pd_npu_dwn_ena Enable power down VD_NPU by hardware. 1'b0: Disable 1'b1: Enable

PMU2_PWR_GATE_SFTCON0
Address: Operational Base(0x20838000) + offset (0x0210)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:3	RO	0x0000	reserved
2	RW	0x0	pd_aiisp_dwn_sftena Enable power down PD_AIISP by software. 1'b0: Disable 1'b1: Enable
1	RW	0x0	pd_vdo_dwn_sftena Enable power down PD_VDO by software. 1'b0: Disable 1'b1: Enable
0	RW	0x1	pd_npu_dwn_sftena Enable power down VD_NPU by software. 1'b0: Disable 1'b1: Enable

PMU2_VOL_GATE_CON0

Address: Operational Base(0x20838000) + offset (0x0220)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	vd_npu_dwn_ena Enable power off VD_NPU by hardware. 1'b0: Disable 1'b1: Enable

PMU2_PWR_GATE_STS

Address: Operational Base(0x20838000) + offset (0x0230)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RO	0x0	pd_aiisp_dwn_stat The power state of PD_AIISP. 1'b0: Power up 1'b1: Power down
1	RO	0x0	pd_vdo_dwn_stat The power state of PD_VDO. 1'b0: Power up 1'b1: Power down
0	RO	0x0	pd_npu_dwn_stat The power state of VD_NPU. 1'b0: Power up 1'b1: Power down

PMU2_PWR_GATE_POWER_STS

Address: Operational Base(0x20838000) + offset (0x0238)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
2:0	RO	0x0	power_gate_state Power gating state. 3'h0: Normal state 3'h1: Power down start state 3'h2: Power down running state 3'h3: Wait for power up state 3'h4: Power up start state 3'h5: Power up running state Others: Reserved

PMU2_PWR_DWN_ACK_STS0

Address: Operational Base(0x20838000) + offset (0x0240)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	pd_scu_dwn_ack The dwn_ack state of VD_SCU. 1'b0: Power up 1'b1: Power down
6	RO	0x0	pd_cpu3_dwn_ack The dwn_ack state of PD_CPU3. 1'b0: Power up 1'b1: Power down
5	RO	0x0	pd_cpu2_dwn_ack The dwn_ack state of PD_CPU2. 1'b0: Power up 1'b1: Power down
4	RO	0x0	pd_cpu1_dwn_ack The dwn_ack state of PD_CPU1. 1'b0: Power up 1'b1: Power down
3	RO	0x0	pd_cpu0_dwn_ack The dwn_ack state of PD_CPU0. 1'b0: Power up 1'b1: Power down
2	RO	0x0	pd_aiisp_dwn_ack The dwn_ack state of PD_AIISP. 1'b0: Power up 1'b1: Power down
1	RO	0x0	pd_vdo_dwn_ack The dwn_ack state of PD_VDO. 1'b0: Power up 1'b1: Power down
0	RO	0x0	pd_npu_dwn_ack The dwn_ack state of VD_NPU. 1'b0: Power up 1'b1: Power down

PMU2_PWR_C0_ACK_SEL_CON0

Address: Operational Base(0x20838000) + offset (0x0380)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
7	RW	0x0	pd_scu_dwn_c0_ack_sel PD_SCU power chain 0 acknowledge signal selection. 1'b0: From power chain 0 output 1'b1: From power chain 0 request signal
6	RW	0x0	pd_cpu3_dwn_c0_ack_sel PD_CPU3 power chain 0 acknowledge signal selection. 1'b0: From power chain 0 output 1'b1: From power chain 0 request signal
5	RW	0x0	pd_cpu2_dwn_c0_ack_sel PD_CPU2 power chain 0 acknowledge signal selection. 1'b0: From power chain 0 output 1'b1: From power chain 0 request signal
4	RW	0x0	pd_cpu1_dwn_c0_ack_sel PD_CPU1 power chain 0 acknowledge signal selection. 1'b0: From power chain 0 output 1'b1: From power chain 0 request signal
3	RW	0x0	pd_cpu0_dwn_c0_ack_sel PD_CPU0 power chain 0 acknowledge signal selection. 1'b0: From power chain 0 output 1'b1: From power chain 0 request signal
2	RW	0x0	pd_aiisp_dwn_c0_ack_sel PD_AIISP power chain 0 acknowledge signal selection. 1'b0: From power chain 0 output 1'b1: From power chain 0 request signal
1	RW	0x0	pd_vdo_dwn_c0_ack_sel PD_VDO power chain 0 acknowledge signal selection. 1'b0: From power chain 0 output 1'b1: From power chain 0 request signal
0	RW	0x0	pd_npu_dwn_c0_ack_sel PD_NPU power chain 0 acknowledge signal selection. 1'b0: From power chain 0 output 1'b1: From power chain 0 request signal

5.5 Application Notes

5.5.1 Low Power Mode

PMU can work in the power mode 1 by setting bit[0] of PMU1_PWR_CON1 register. After setting this bit and all CPUs enter standby states, PMU low power FSM will start to run. In this low power mode, PMU will manage power resources by hardware or software, such as send idle request or resume transfer to specified BIU interface, power down or power up the specified power domain, DDR enters or exits retention mode, shut down or power up PLL, disable or enable oscillator, and so on. All of above are configurable by setting corresponding registers.

PMU can work in power mode 0 by setting bit[0] in PMU0_PWR_CON0 register. After setting this bit, PMU power mode 0 FSM will start to run. In this low power mode, PMU will manage PD_PMU1 power resource. All of above are configurable by setting corresponding registers.

5.5.2 Always on Video Low Power Mode

There is a Always on Video(AOV) Mode Sub-System in PMU. The chip can accept image data from an external camera and transmit it to the PSRAM outside the chip when in Power-Off Mode(which means that the VDD_LOGIC is power down). After each frame is transmitted, the AOV controls the chip to enter a Deep-Power-Off Mode. In this mode, PD_PMU1 will be power down. After the time set by the counter, the AOV wakes up PD_PMU1 to prepare for receiving the next frame of data. The following figure describes the AOV Mode configuration and operational workflow.

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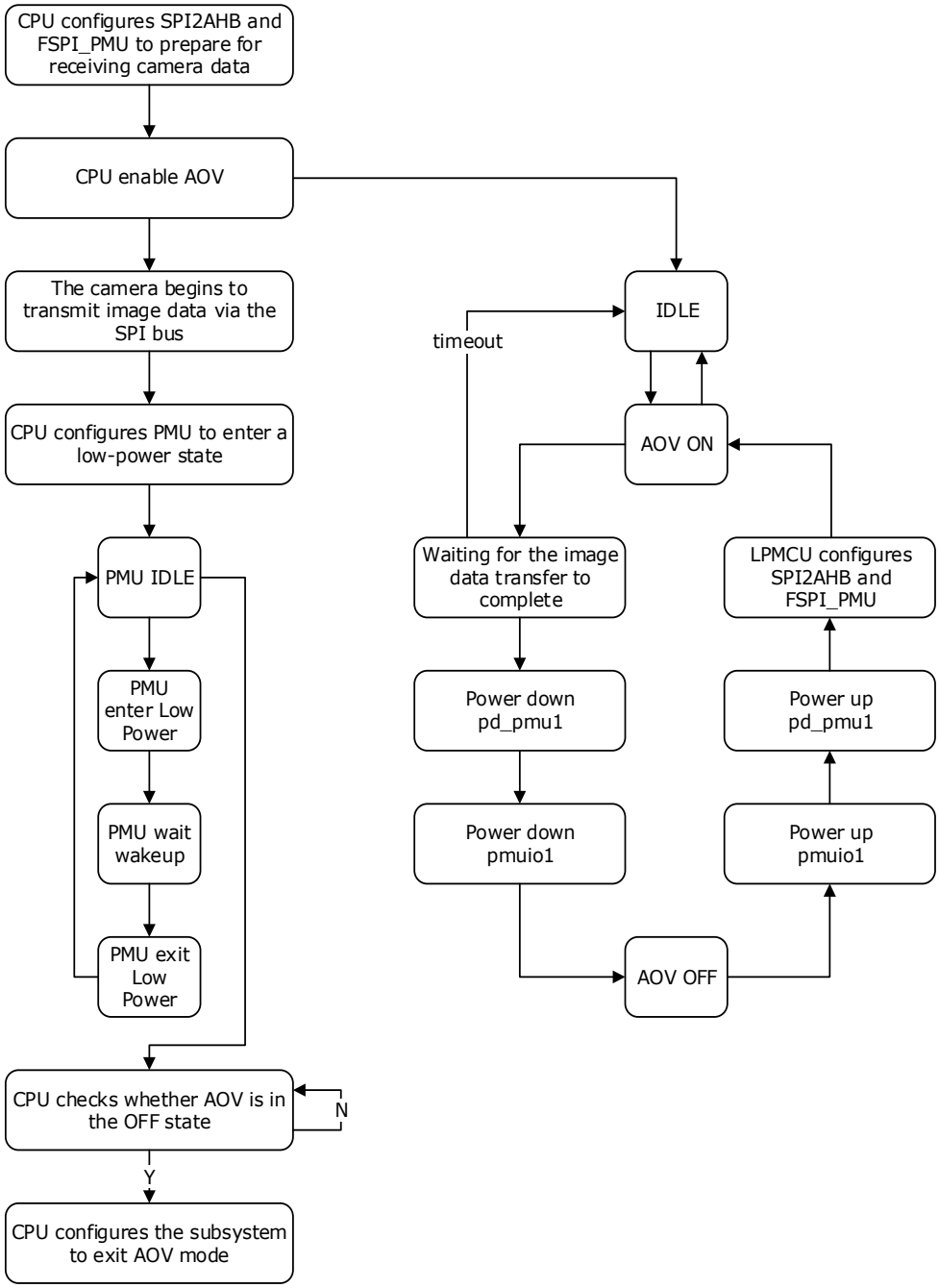

Fig.5-3 The AOV Mode configuration and operational workflow

5.5.3 Power Management IO Usage

There are independent power supplies for different voltage domain. You can communicate with external PMIC (Power Management Integrated Circuits) through I2C interface, or through IO interface.

There are 3 IOs designed for purpose, corresponding Module Pin names are pwr_ctrl0_iout ~ pwr_ctrl2_iout. The IO interface configuration is as below.

Table 5-2 Power Management IO Interface

Module Pin	Direction	Pin Name	IOMUX Setting
pwr_ctrl0_iout	O	GPIO0_A3	PMU_IOC_GPIO0A_IOMUX_SEL_L[15:12]=1
pwr_ctrl1_iout	O	GPIO0_A4	PMU_IOC_GPIO0A_IOMUX_SEL_H[3:0]=1
pwr_ctrl2_iout	O	GPIO0_C1	PMU_IOC_GPIO0C_IOMUX_SEL_L[7:4]=3

Each pwr_ctrl IO has multi power off requests and you can only choose one at a time. Detail refers to PMUGRF_SOC_CON0/1.

5.5.4 Debug IO

ALL FSM power states could be monitored through IO. Chip also provides PMU Debug IO for FSM observation in UART signal mode.

Table 5-3 Debug IO for PMU FSM state

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Module Pin	Direction	Pin Name	IOMUX Setting
pmu_debug_tx	O	GPIO0_A2	PMU_IOC_GPIO0A_IOMUX_SEL_L[11:8]=3
aov_debug_tx	O	GPIO0_B3	PMU_IOC_GPIO0B_IOMUX_SEL_L[15:12]=5

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Chapter 6 HPMCU Subsystem

6.1 Overview

The High Performance MCU (HPMCU) Subsystem embedded one MCU processor (RISCV Architecture), a 16KB unified I/D cache and interrupt multiplexer (INTMUX). It allowed fast & efficient data exchange. And the Level 1 Instruction/Data Cache designed for HPMCU can improve the memory access performance significantly.
The following features may or may not be present in the actual product. Please contact Rockchip for the actual feature configurations and the third-party licensing requirements.
The HPMCU features and benefits are:

- One MCU processor
- Machine privilege level
- 32 32-bit general purpose integer registers
- Instruction set is RV32I with M and C extensions
- 3 stage pipeline implementations
- 3 embedded 64bit performance counters
  Real time clock
  Cycle counter
  Instructions-retired counter
- Optional debug support
  - Two hardware breakpoints
  - Support Serial Wire debug connection
- Interrupt multiplexer (INTMUX)
  - Multiplexer 8 interrupts from 256 interrupt sources using round-robin algorithm
  - Each 32 adjacent interrupts are seen as a group which share same INTMUX_INT_ENABLE_GROUPx and INTMUX_INT_FLAG_GROUPx register
    In addition, 8 interrupts come from 8 interrupt sources in a direct connection manner.
- 16KB unified I/D Cache
  - Support 2-way set-associative with 32Byte cache line size
  - Support one 64bit AHB-Lite bus master interface to SoC interconnect
  - Support memory cacheable access and peripheral bypass access
  - Support Write-Through with No-Write-Allocate and Read-Allocate
  - Support Write-Back with Write-Allocate and Read-Allocate
  - Support cache maintenance operations (clean/invalidate/clean & invalidate) by address
  - Support cache invalidate/clean & invalidate operations for all cache lines
  - Support cache initialization by software configuration
  - Support RAM debug mode for tag RAM and data RAM
  - Support one interrupt source

The main configurations of HPMCU as shown below.

Table 6-1 HPMCU Subsystem Configurations

	HPMCU
CACHE	16KB
IRQ_NUM	16
INTMUX	YES

6.2 Block Diagram

The Int_in[255:0] will connect with all interrupt source, and please refer to "Chapter System Overview" for the detail interrupt number. HPMCU Subsystem are shown below.

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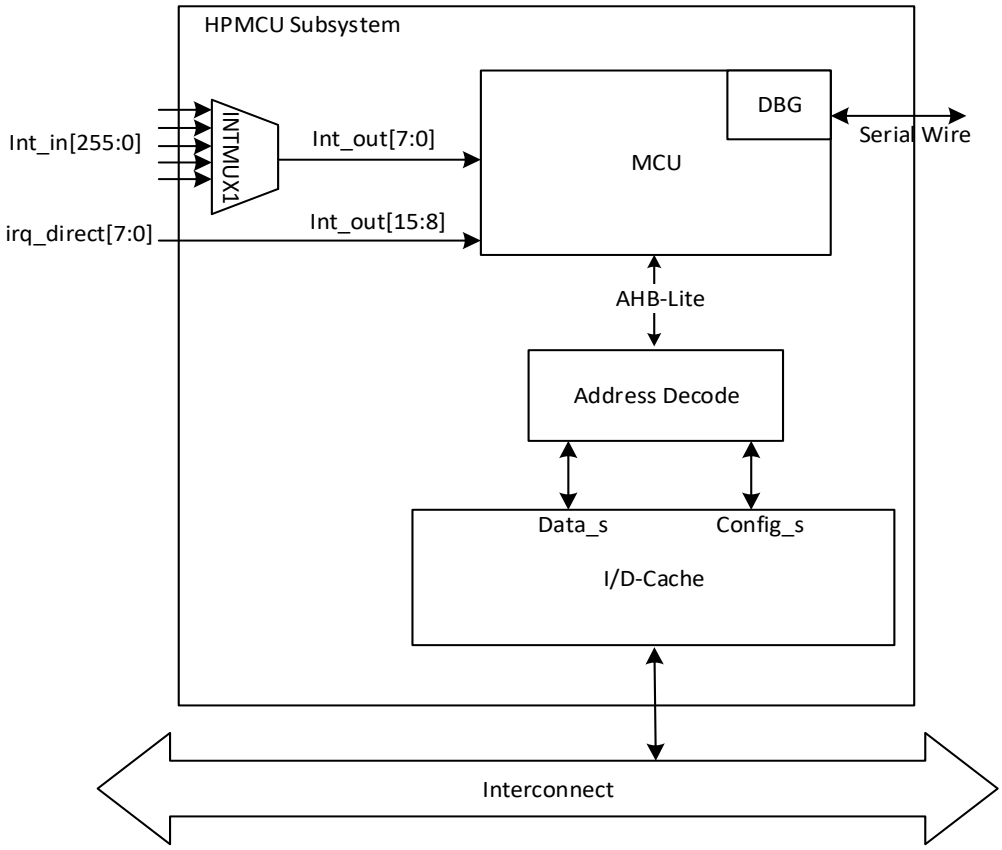

Fig. 6-1 Block Diagram of HPMCU Subsystem

6.3 CACHE Register Description

6.3.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

6.3.2 Registers Summary

Name	Offset	Size	Reset Value	Description
CACHE_CACHE_CTRL	0x0000	W	0x0000002D	Cache control register
CACHE_CACHE_MAINTAIN0	0x0004	W	0x00000000	Cache maintain register0
CACHE_CACHE_MAINTAIN1	0x0008	W	0x00000000	Cache maintain register1
CACHE_STB_TIMEOUT_CTRL	0x000C	W	0x00000000	Store buffer timeout control register
CACHE_CACHE_INT_EN	0x0020	W	0x00000000	Cache interrupt enable register
CACHE_CACHE_INT_ST	0x0024	W	0x00000000	Interrupt status register
CACHE_CACHE_ERR_HADDR	0x0028	W	0x00000000	Address record when ahb error response on ahb master interface
CACHE_CACHE_STATUS	0x0030	W	0x00000000	Cache status register
CACHE_PMU_RD_NUM_CNT	0x0040	W	0x00000000	PMU read number counter status
CACHE_PMU_WR_NUM_CNT	0x0044	W	0x00000000	PMU write number counter status
CACHE_PMU_SRAM_RD_HIT_CNT	0x0048	W	0x00000000	PMU SRAM hit counter status
CACHE_PMU_HB_RD_HIT_CNT	0x004C	W	0x00000000	PMU hot buffer hit status

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Name	Offset	Size	Reset Value	Description
CACHE_PMU_STB_RD_HIT_CNT	0x0050	W	0x00000000	PMU store buffer hit status
CACHE_PMU_RD_HIT_CNT	0x0054	W	0x00000000	PMU read hit counter status
CACHE_PMU_WR_HIT_CNT	0x0058	W	0x00000000	PMU write hit counter status
CACHE_PMU_RD_MISS_PENALTY_CNT	0x005C	W	0x00000000	PMU read miss penalty counter status
CACHE_PMU_WR_MISS_PENALTY_CNT	0x0060	W	0x00000000	PMU write miss penalty counter status
CACHE_PMU_RD_LAT_CNT	0x0064	W	0x00000000	PMU read latency status
CACHE_PMU_WR_LAT_CNT	0x0068	W	0x00000000	PMU write latency status
CACHE_REVISION	0x00F0	W	0x00000100	Cache desgin revision register

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

6.3.3 Detail Registers Description

CACHE_CACHE_CTRL

Address: Operational Base(0x209D0000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	cache_mpu_mode cortex-m4 mpu mode support 1'b0: not support mpu mode 1'b1: support mpu mode, the cache controller will cache the request if bothe hprot[3] and memattr[0] is high on ahb slave bus, or will bypass the request.
11	RO	0x0	reserved
10:8	RW	0x0	cache_entry_thresh Cache store buffer entry threshold control register, when data entrys are more than threshhold value, the wirte data will be write to Cache RAM
7	RW	0x0	stb_timeout_en Store buffer time out enable, when this bit is set enable, the data in store buffer must be flushed to Cache RAM. 1'b0: Disable 1'b1: Enable
6	RW	0x0	cache_bypass Cache bypass controler register, when this bit is set high, data will bypass the AHB interface. 1'b0: Disable 1'b1: Enable
5	RW	0x1	cache_pmu_en Cache performance monitor enable register 1'b0: Disable 1'b1: Enable
4	RW	0x0	cache_flush Cache flush enable, when this bit is set enable, the dirty data is flushed to external memory and the cache line are set invalid 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3	RW	0x1	cache_stb_en Cache store buffer enable register 1'b0: Disable 1'b1: Enable This bit must be disable when write through mode is selected
2	RW	0x1	cache_hb_en Cache hot buffer enable register 1'b0: Disable 1'b1: Enable
1	RW	0x0	cache_wt_en Cache mode control register 1'b0: write back 1'b1: write through
0	RW	0x1	cache_en Cache enable bit 1'b0: Disable 1'b1: Enable

CACHE_CACHE_MAINTAIN0

Address: Operational Base(0x209D0000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:5	RW	0x0000000	cache_m_addr Cache maintain start address
4:3	RO	0x0	reserved
2:1	RW	0x0	cache_m_cmd Cache maintain command register 2'b00: Cache clean 2'b01: Cache invalid 2'b10: Cache clean and invalid 2'b11: Cache invalid all
0	RW	0x0	cache_m_valid Cache maintain valid register, the cache_m_cmd will be valid only this bit is set high.

CACHE_CACHE_MAINTAIN1

Address: Operational Base(0x209D0000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	cache_m_offset Cache maintain offset address, the maintain address scope is from cache_m_addr to cache_m_addr + cache_m_offset

CACHE_STB_TIMEOUT_CTRL

Address: Operational Base(0x209D0000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RW	0x00000	stb_timeout_value store buffer timeout counter value

CACHE_CACHE_INT_EN

Address: Operational Base(0x209D0000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	err_record_en ahb master bus error record enable 1'b0: Disable 1'b1: Enable

CACHE_CACHE_INT_ST
Address: Operational Base(0x209D0000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	ahb_error_status Error status bit on ahb master bus

CACHE_CACHE_ERR_HADDR
Address: Operational Base(0x209D0000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	status_haddr address information when ahb bus error

CACHE_CACHE_STATUS
Address: Operational Base(0x209D0000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RO	0x0	cache_flush_done Cache flush finish status register
1	RO	0x0	cache_m_busy Cache maintain busy status register
0	RO	0x0	cache_init_finish Cache initialization finish status register

CACHE_PMU_RD_NUM_CNT
Address: Operational Base(0x209D0000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pmu_rd_num_cnt Performance monitor read nunber register

CACHE_PMU_WR_NUM_CNT
Address: Operational Base(0x209D0000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pmu_wr_num_cnt Performance monitor write number register

CACHE_PMU_SRAM_RD_HIT_CNT
Address: Operational Base(0x209D0000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pmu_sram_rd_hit_cnt Performance monitor SRAM hit counter register

CACHE_PMU_HB_RD_HIT_CNT
Address: Operational Base(0x209D0000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pmu_hb_rd_hit_cnt Performance monitor hot buffer hit counter register

CACHE_PMU_STB_RD_HIT_CNT

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Address: Operational Base(0x209D0000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_stb_rd_hit_cnt Performance monitor store buffer hit counter register

CACHE_PMU_RD_HIT_CNT

Address: Operational Base(0x209D0000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pmu_rd_hit_cnt Performance monitor read hit counter register

CACHE_PMU_WR_HIT_CNT

Address: Operational Base(0x209D0000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pmu_wr_hit_cnt Performance monitor write hit register

CACHE_PMU_RD_MISS_PENALTY_CNT

Address: Operational Base(0x209D0000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pmu_rd_miss_penalty_cnt Performance monitor read miss penalty count register

CACHE_PMU_WR_MISS_PENALTY_CNT

Address: Operational Base(0x209D0000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pmu_wr_miss_penalty_cnt Performance monitor write miss penalty register

CACHE_PMU_RD_LAT_CNT

Address: Operational Base(0x209D0000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pmu_rd_lat_cnt Performance monitor read latency register

CACHE_PMU_WR_LAT_CNT

Address: Operational Base(0x209D0000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pmu_rd_lat_cnt Performance monitor write latency register

CACHE_REVISION

Address: Operational Base(0x209D0000) + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000100	revision Design revision

6.4 INTMUX Registers Summary

6.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

6.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
INTMUX_INT_ENABLE_GROUP0	0x0000	W	0x00000000	Interrupt Group0 Enable Register

Name	Offset	Size	Reset Value	Description
INTMUX_INT_ENABLE_GROUP1	0x0004	W	0x00000000	Interrupt Group1 Enable Register
INTMUX_INT_ENABLE_GROUP2	0x0008	W	0x00000000	Interrupt Group2 Enable Register
INTMUX_INT_ENABLE_GROUP3	0x000C	W	0x00000000	Interrupt Group3 Enable Register
INTMUX_INT_ENABLE_GROUP4	0x0010	W	0x00000000	Interrupt Group4 Enable Register
INTMUX_INT_ENABLE_GROUP5	0x0014	W	0x00000000	Interrupt Group5 Enable Register
INTMUX_INT_ENABLE_GROUP6	0x0018	W	0x00000000	Interrupt Group6 Enable Register
INTMUX_INT_ENABLE_GROUP7	0x001C	W	0x00000000	Interrupt Group7 Enable Register
INTMUX_INT_FLAG_GROUP0	0x0080	W	0x00000000	Interrupt Group0 Flag Register
INTMUX_INT_FLAG_GROUP1	0x0084	W	0x00000000	Interrupt Group1 Flag Register
INTMUX_INT_FLAG_GROUP2	0x0088	W	0x00000000	Interrupt Group2 Flag Register
INTMUX_INT_FLAG_GROUP3	0x008C	W	0x00000000	Interrupt Group3 Flag Register
INTMUX_INT_FLAG_GROUP4	0x0090	W	0x00000000	Interrupt Group4 Flag Register
INTMUX_INT_FLAG_GROUP5	0x0094	W	0x00000000	Interrupt Group5 Flag Register
INTMUX_INT_FLAG_GROUP6	0x0098	W	0x00000000	Interrupt Group6 Flag Register
INTMUX_INT_FLAG_GROUP7	0x009C	W	0x00000000	Interrupt Group7 Flag Register

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

6.4.3 Detail Registers Description

INTMUX_INT_ENABLE_GROUP0

Address: Operational Base(0x20B40000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disable 1'b1: Interrupt enable

INTMUX_INT_ENABLE_GROUP1

Address: Operational Base(0x20B40000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disable 1'b1: Interrupt enable

INTMUX_INT_ENABLE_GROUP2

Address: Operational Base(0x20B40000) + offset (0x0008)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disable 1'b1: Interrupt enable

INTMUX_INT_ENABLE_GROUP3
Address: Operational Base(0x20B40000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disable 1'b1: Interrupt enable

INTMUX_INT_ENABLE_GROUP4
Address: Operational Base(0x20B40000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disable 1'b1: Interrupt enable

INTMUX_INT_ENABLE_GROUP5
Address: Operational Base(0x20B40000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disable 1'b1: Interrupt enable

INTMUX_INT_ENABLE_GROUP6
Address: Operational Base(0x20B40000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disable 1'b1: Interrupt enable

INTMUX_INT_ENABLE_GROUP7
Address: Operational Base(0x20B40000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	enable Each bit represents one interrupt enable bit. 1'b0: Interrupt disable 1'b1: Interrupt enable

INTMUX_INT_FLAG_GROUP0
Address: Operational Base(0x20B40000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP1
Address: Operational Base(0x20B40000) + offset (0x0084)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP2
Address: Operational Base(0x20B40000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP3
Address: Operational Base(0x20B40000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP4
Address: Operational Base(0x20B40000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP5
Address: Operational Base(0x20B40000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP6
Address: Operational Base(0x20B40000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

INTMUX_INT_FLAG_GROUP7
Address: Operational Base(0x20B40000) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	flag Each bit represents one interrupt is in service. 1'b0: Interrupt in service 1'b1: Interrupt out of service

6.5 Interface Description

There are three sets of serial debug interface for the HPMCU. When we debug using serial

wire, not only set IOMUX, but also configure the bit[2:1] of IOC_GRF_JTAG_CON0 to select the HPMCU. Note that, you shall also configure the bit[7] of SYS_SGRF_CON2 in SYS_SGRF to enable debug for HPMCU.

Table 6-2 MCU Serial Wire Debug Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
mcujtag_tckm0	I	GPIO0_B3	GPIO0B_IOMUX_SEL_0[15:12]=4'h4
mcujtag_tmsm0	I/O	GPIO0_B4	GPIO0B_IOMUX_SEL_1[3:0]=4'h4
mcujtag_tckm1	I	GPIO2_A2	GPIO2A_IOMUX_SEL_0[11:8]=4'h4
mcujtag_tmsm1	I/O	GPIO2_A3	GPIO2A_IOMUX_SEL_0[15:12]=4'h4
mcujtag_tckm2	I	GPIO5_D6	GPIO5D_IOMUX_SEL_1[11:8]=4'h2
mcujtag_tmsm2	I/O	GPIO5_D7	GPIO5D_IOMUX_SEL_1[15:12]=4'h2

Notes: I=input, O=output, I/O=input/output, bidirectional

6.6 Application Notes

6.6.1 Clock and Reset Generation

Please refer to "Chapter CRU" for more detailed information.

6.6.2 Interrupt for HPMCU

The Int_in[255:0] are part of system interrupts and each 32 interrupts will multiplexed into one interrupt. Please refer to "Chapter System Overview" for the detail interrupt number

Table 6-3 HPMCU Intmux Interrupt

IRQ ID	IRQ Source
0	Int_in[31:0] mux 1
1	Int_in[63:32] mux 1
2	Int_in[95:64] mux 1
3	Int_in[127:96] mux 1
4	Int_in[159:128] mux 1
5	Int_in[191:160] mux 1
6	Int_in[223:192] mux 1
7	Int_in[255:224] mux 1

The irq_direct[7:0] are part of system interrupts. Please refer to "Chapter System Overview" for the detail interrupt number.

Table 6-4 HPMCU Direct Interrupt

IRQ ID	IRQ Source
0	irq_gpio1[0]
1	irq_hpmcu_mailbox_ap[0]
2	irq_stimer0
3	irq_spi0
4	irq_rkdma
5	irq_uart1
6	irq_pwm0[0]
7	irq_saradc0

6.6.3 Cache Initialization

The Cache is bypassed after reset and need to be initialized by the HPMCU. The basic initialization flow is:

1. Configure to Write-Back or Write-Through mode by setting CACHE_CTRL.cache_wt_en and start initialization by configuring CACHE_CTRL.cache_en to high while keeping the Cache in bypass mode (CACHE_CTRL.cache_bypass is high). The store buffer must and only can be enabled for Write-Back mode, so you must disable the store buffer when Write-Through mode is selected. You can also enable the hot buffer for better performance. It is recommended that configure the I-Cache to Write-Through mode and configure the D-Cache to Write-Back mode.
2. Wait for cache initialization to be finished by polling CACHE_STATUS.cache_init_finish.

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3. Disable cache bypass mode by configuring CACHE_CTRL.cache_bypass to low. Now that the Cache is enabled.
4. Simply configure CACHE_CTRL.cache_bypass to bypass or enable the Cache again after the initialization flow.

6.6.4 Cache Maintenance

The Cache Controller support the following cache maintenance operations:

1. Clean by address: push the specified cache line data to external memory if it is valid and dirty.
2. Invalidate by address: unconditionally clear the valid and dirty data of the specified cache lines.
3. Clean and invalidate by address: clean and then invalidate the specified cache lines.
4. Invalidate all: unconditionally clear the valid and dirty data for all the cache lines.
5. Clean and invalidate all (Flush): clean and then invalidate all the cache lines.
   For the operation of cache clean and invalidate all, configure CACHE_CTRL.cache_flush to high first, and then wait for flush to be done by polling CACHE_STATUS.cache_flush_done. Finally, if the flush is done, you should configure CACHE_CTRL.cache_flush to low.

   For the other four maintenance operations, you should set the maintenance command and the address range of the cache lines by configuring CACHE_MAINTAIN0 and CACHE_MAINTAIN1, then start by configuring CACHE_MAINTAIN0.cache_m_valid to high. When the operation is finished, CACHE_MAINTAIN0.cache_m_valid will be automatically cleared to low. You can also poll CACHE_STATUS.cache_m_busy to judge whether the operation is done.

6.6.5 Cache RAM Debug Mode

When the Cache is enabled and not in the bypass mode, you can enter the cache RAM debug mode by configuring CACHE_RAM_DEBUG.ram_debug_en to high. In the RAM debug mode, the cache RAM can be accessed directly by the specific address, and all the other cacheable memory accesses are bypassed because the cache core is disabled.

The following table shows the address map for the cache RAM debug.

Table 6-4 Address Map for the Cache RAM Debug

RAM Access Type	RAM Access Size	Address Range for Cache RAM Debug
Reserved	7KB	0x209E6400 ~ 0x209E7FFF
TAG RAM1	1KB	0x209E6000 ~ 0x209E63FF
Reserved	7KB	0x209E4400 ~ 0x209E5FFF
TAG RAMCU	1KB	0x209E4000 ~ 0x209E43FF
DATA RAM1	8KB	0x209E2000 ~ 0x209E3FFF
DATA RAMCU	8KB	0x209E0000 ~ 0x209E1FFF

As shown in the above table, there are 2 ways for each cache, and the size of one DATA RAM is 8KB.

The following explanation may help you use the RAM debug method:

1. Using the word-aligned address to access the TAG RAM.
2. The bits[9:2] of the TAG RAM address are acted as the bits[12:5] of the corresponding memory address.
3. Only the bits[20:0] of the TAG RAM data are available, and the bits[31:21] are always zero.
- The bit[20] is the valid flag bit.
- The bit[19] is the dirty flag bit.
- The bits[18:0] are acted as the bits[31:13] of the corresponding memory address.

4. The bits[12:0] of the DATA RAM address are acted as the bits[12:0] of the corresponding memory address.
5. In order to get the cache line data at the wanted address, you should read both of the TAG RAMs to find the matched address, and then read data from the corresponding DATA RAM.
6. If write data to the DATA RAM, 8 copies of the 32bit data on the AHB bus will be written to the 32Byte cache line.

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6.6.6 Other Hints

1. One interrupt request source is supported for the I/D-Cache, so you can query the interrupt register in the ISR if it is enabled. When CACHE_INT_EN.err_record_en is high, the Cache will generate a bus error interrupt if access to a wrong address. You can read CACHE_INT_ST.ahb_error_status for the cache interrupt status and get the recent error address information from CACHE_ERR_HADDR.status_haddr.
2. The non-cacheable space of cache can be configured by GRF, please refer to Chapter GRF for more detail.

Table 6-5 Configuration of Cache Peripheral Space

MCU Type	Begin Address	End Address
HPMCU	PERI_GRF_MCU_CACHE_PERI_START_ADDR	PERI_GRF_MCU_CACHE_PERI_END_ADDR

6.6.7 How to boot

Currently, the HPMCU core boot address is configurable, with the default value is 32'h4012_0000, and the default value of trap vector base address is 32'h0010_01c0, you can configure PERI_SGRF_MCU_BOOT_ADDR of PERI_SGRF related to HPMCU before de-assert its reset. If you change the boot address, don't forget to configure the MCU_CSR_MTVEC register by system instructions.

6.6.8 Debug clk enable

When using JTAG interface to access the debug function of HPMCU, clk_hpmcu, and clk_hpmcu_rtc need to be all turned on.

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Chapter 7 LPMCU Subsystem

7.1 Overview

The Low Performance MCU (LPMCU) Subsystem embedded one MCU processor(RISCV Architecture).

The following features may or may not be present in the actual product. Please contact Rockchip for the actual feature configurations and the third-party licensing requirements.

The LPMCU features and benefits are:

- One MCU processor
- Machine privilege level
- 32 32-bit general purpose integer registers
- Instruction set is RV32I with M and C extensions
- 3 stage pipeline implementations
- 3 embedded 64bit performance counters
- Real time clock
- Cycle counter
- Instructions-retired counter
- Optional debug support
  - Two hardware breakpoints
  - Support Serial Wire debug connection

The main configurations of LPMCU as shown below.

Table 7-1 LPMCU Subsystem Configurations

	LPMCU
CACHE	NA
IRQ_NUM	16
INTMUX	NA

7.2 Block Diagram

The Int_in[15:0] will connect with some PMU interrupt source, and please refer to "Chapter System Overview" for the detail interrupt number. LPMCU Subsystem are shown below.

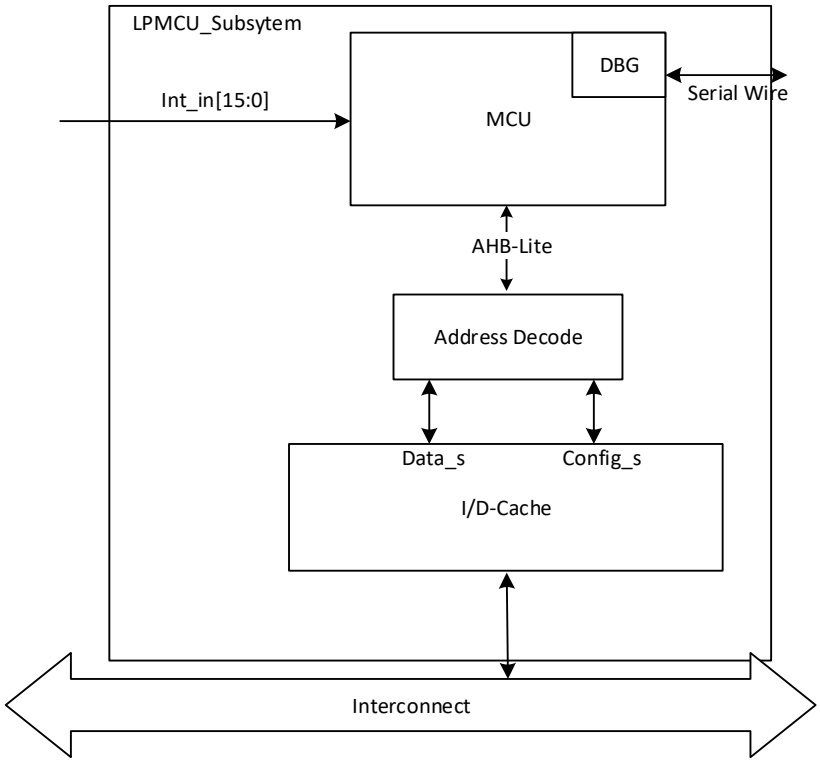

Fig. 7-1 Block Diagram of LPMCU Subsystem

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7.3 Interface Description

There are three sets of serial debug interface for the LPMCU. When we debug using serial wire, not only set IOMUX, but also configure the bit[2:1] of IOC_GRF_JTAG_CON0 to select the LPMCU.

Table 7-2 MCU Serial Wire Debug Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
mcujtag_tckm0	I	GPIO0_B3	GPIO0B_IOMUX_SEL_0[15:12]=4'h4
mcujtag_tmsm0	I/O	GPIO0_B4	GPIO0B_IOMUX_SEL_1[3:0]=4'h4
mcujtag_tckm1	I	GPIO2_A2	GPIO2A_IOMUX_SEL_0[11:8]=4'h4
mcujtag_tmsm1	I/O	GPIO2_A3	GPIO2A_IOMUX_SEL_0[15:12]=4'h4
mcujtag_tckm2	I	GPIO5_D6	GPIO5D_IOMUX_SEL_1[11:8]=4'h2
mcujtag_tmsm2	I/O	GPIO5_D7	GPIO5D_IOMUX_SEL_1[15:12]=4'h2

Notes: I=input, O=output, I/O=input/output, bidirectional

7.4 Application Notes

7.4.1 Clock and Reset Generation

Please refer to "Chapter CRU" for more detailed information.

7.4.2 Interrupt for LPMCU

The Int_in[15:0] are part of system interrupts. Please refer to "Chapter System Overview" for the detail interrupt number

Table 7-3 LPMCU Interrupt

IRQ ID	IRQ Source	IRQ ID	IRQ Source
0	irq_gpio_pmu	8	irq_fspi_pmu
1	irq_hptimer_pmu	9	irq_pwm1_pmu
2	irq_uart0_pmu	10	irq_preroll_on
3	irq_i2c2_pmu	11	irq_preroll_off
4	irq_wdt_pmu	12	intmux_int16out_mux
5	irq_mailbox_ap_pmu	13	irq_rtcphy
6	irq_lpsai	14	irq_aad
7	irq_spi2ahb	15	irq_lpdmac

7.4.3 How to boot

Currently, the LPMCU core boot address is configurable, with the default value is 32'h3ff1_e000, and the default value of trap vector base address is 32'h0010_01c0, you can configure PMU_SGRF_PMUMCU_BOOT_ADDR of PMU_SGRF related to LPMCU before de-assert its reset. If you change the boot address, don't forget to configure the MCU_CSR_MTVEC register by system instructions.

7.4.4 Debug clk enable

When using JTAG interface to access the debug function of LPMCU, clk_lpmcu, and clk_lpmcu_rtc need to be all turned on.

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Chapter 8 System Debug

8.1 Overview

The chip uses the DAPLITE Technology to support real-time debug.

8.1.1 Features

- Invasive debug with core halted
- SW-DP

8.1.2 Debug Components Address Map

The following table shows the debug components address in memory map:

Module	Base Address
DAP_ROM	0x22400000

8.2 Block Diagram

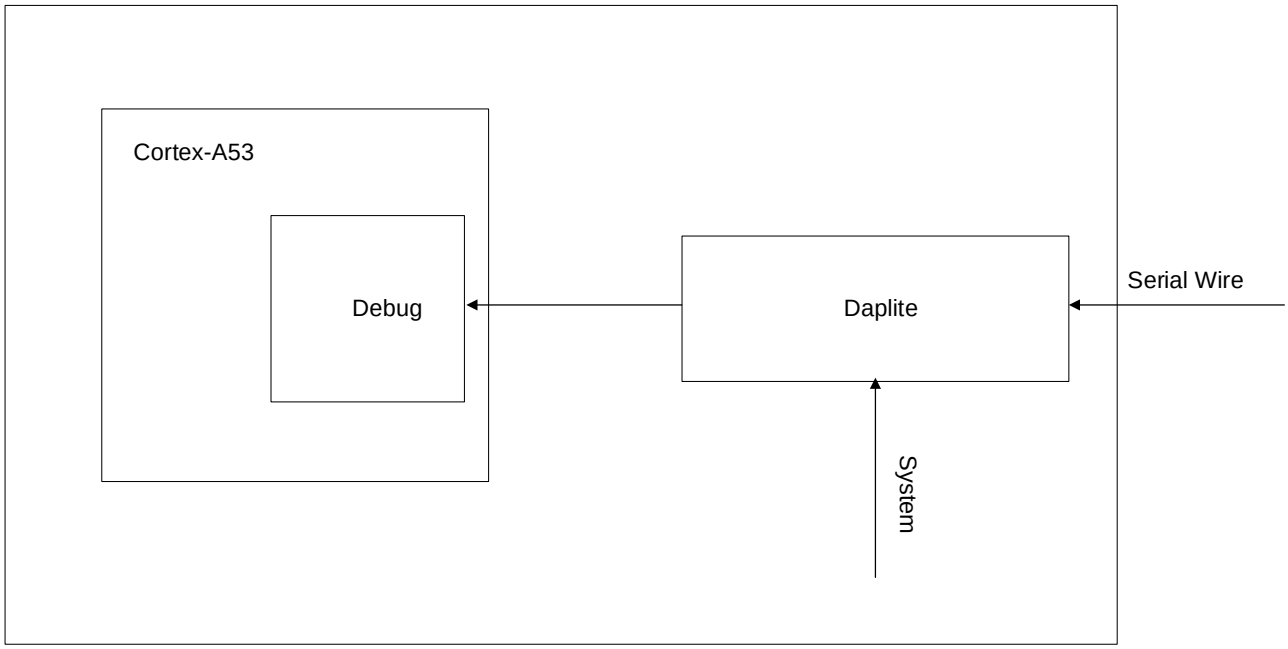

Fig. 8-1 Debug system structure

8.3 Function Description

8.3.1 DAP

The DAP has following components:

- Serial Wire JTAG Debug Port (SWJ-DP)
- APB Access Port (APB-AP)
- ROM table

The debug port is the host tools interface to access the DAP-Lite. This interface controls any access ports provided within the DAP-Lite. The DAP-Lite supports a combined debug port which includes both JTAG and Serial Wire Debug (SWD), with a mechanism that supports switching between them.

The APB-AP acts as a bridge between SWJ-DP and APB bus which translate the Debug request to APB bus.

The DAP provides an internal ROM table connected to the master Debug APB port of the APB-Mux. The Debug ROM table is loaded at address 0x00000000 and 0x80000000 of this bus and is accessible from both APB-AP and the system APB input. Bit[31] of the address bus is not connected to the ROM Table, ensuring that both views read the same value. The ROM table stores the locations of the components on the Debug APB.

More information please refer to the document CoreSight_DAPLite_TRM.pdf for the debug detail description.

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8.4 Register Description

8.4.1 Internal Address Mapping

Please refer to the document CoreSight_DAPLite_TRM.pdf for the debug detail description.

8.5 Interface Description

8.5.1 DAP SWJ-DP Interface

The following figure is the DAP SWJ-DP interface, the SWJ-DP is a combined JTAG-DP and SW-DP that enable you connect either a Serial Wire Debug (SWJ) to JTAG probe to a target.

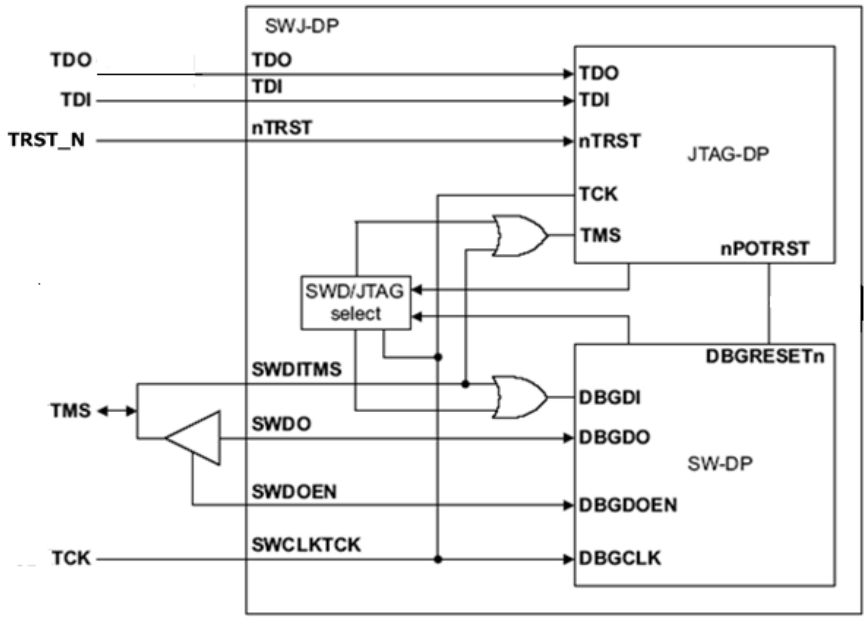

Fig. 8-2 DAP SWJ interface

8.5.2 DAP SWJ-DP Interface

This implementation is taken from ADIv5.1 and operates with a synchronous serial interface. This uses a single bidirectional data signal, and a clock signal.

The figure below describes the interaction between the timing of transactions on the serial wire interface, and the DAP internal bus transfers. It shows when the target responds with a WAIT acknowledgement.

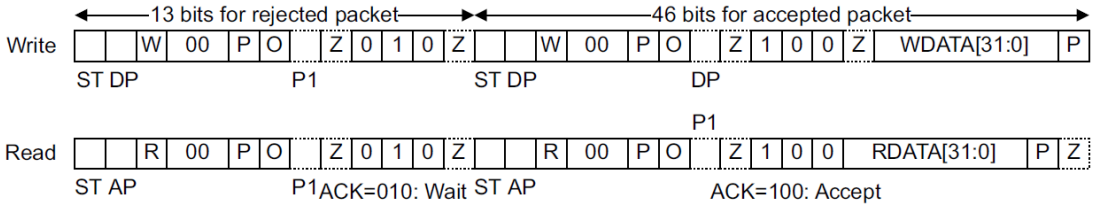

Fig. 8-3 SW-DP acknowledgement timing

There are three sets of serial debug interface for the Cortex-A53. When we debug using serial wire, not only set IOMUX, but also configure the bit[0] of IOC_GRF_JTAG_CON0 to select the Cortex-A53.

Table 8-1 DAP-Lite Interface Description

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Module Pin	Direction	Pad Name	IOMUX Setting
jtag_tckm0	I	GPIO0_B3	PMUIO0_IOC_GPIO0B_IOMUX_SEL_0 [15:12] = 4'h4
jtag_tmsm0	I/O	GPIO0_B4	PMUIO0_IOC_GPIO0B_IOMUX_SEL_1 [3:0] = 4'h4
jtag_tckm1	I	GPIO2_A2	VCCIO2_IOC_GPIO2A_IOMUX_SEL_0 [11:8] = 4'h4
jtag_tmsm1	I/O	GPIO2_A3	VCCIO2_IOC_GPIO2A_IOMUX_SEL_0 [15:12] = 4'h4
jtag_tckm2	I	GPIO5_D6	VCCIO5_IOC_GPIO5D_IOMUX_SEL_1 [11:8] = 4'h2
jtag_tmsm2	I/O	GPIO5_D7	VCCIO5_IOC_GPIO5D_IOMUX_SEL_1 [15:12] = 4'h2

By default, jtag_tckm0 and jtag_tmsm0 are forced to connect to corresponding io pad, we don't need to set IOMUX again.

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Chapter 9 SYSMEM

9.1 Overview

System Memory is a non-coherence SRAM of SOC. System MEM supports 1-set of AXI4 interface for masters to access a shared normal space constructed by SRAM. System MEM exchanges data between SRAM and AXI bus and transforms AXI read-write operations to SRAM read-write operations. All masters connected to the System MEM can share the SRAM fairly.

System MEM supports the following features:

- Interface Type
  - Support AXI4 interface
  - Support 1-set AXI4 interface
  - Support 16-bit address width(64KB address space)
  - Support 128-bit data width
- Operation Type
  - Support FIXED, INCR and WRAP operation type
  - Support all AxSize less than data width
  - Support AxLen inside {[0:15]} for FIXED, {[0:255]} for INCR and {1,3,7,15} for WRAP
  - Support outstanding read-write operation(max 4 deep)
  - Support sequential execution and response in read and write channel
  - Support read-write data consistence
- SRAM specification
  - Support 64KB size of SRAM
  - Support 1-block and 2-bank per block SRAM for high bandwidth

9.2 Block Diagram

System MEM comprises with:

- AXI Slave: AXI Slave Interface and AXI to SRAM operation transform
- ARBITER : Arbiter a operation to SRAM between all read-write channel
- SRAM : storage space of BUS MEM

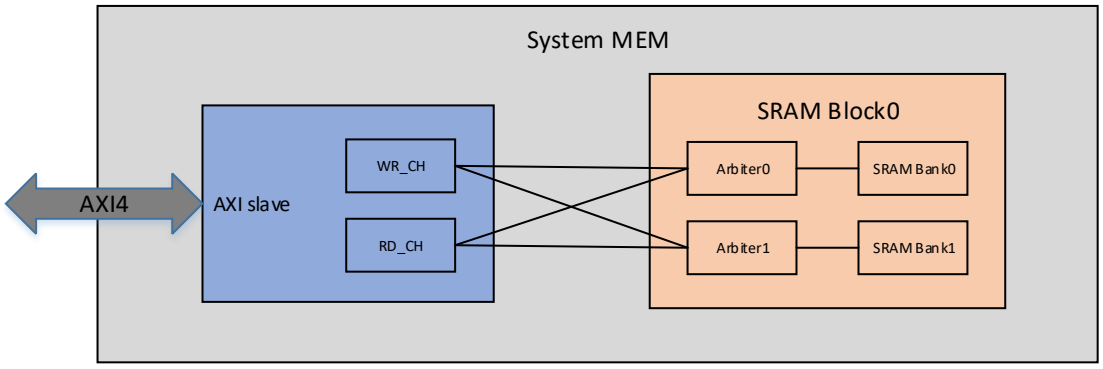

Fig. 9-1 System MEM Block Diagram

9.3 Function Description

9.3.1 AXI Slave

AXI Slave supports a AXI4 slave interface to connect the AXI4 master and receives the read-write operations from master. AXI Slave use CMD FIFO to buffer the read-write operations from master and then transform the AXI4 operation to SRAM operation orderly. Before a read operation pushed into CMD FIFO, AXI Slave will check all address space of write operation unfinished in CMD FIFO. If there is no address conflict, AXI Slave will push the read operation into CMD FIFO, otherwise AXI Slave will block the read channel until conflict release.

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9.3.2 Arbiter

Arbiter supports read-write channel of all AXI Slaves asking request to SRAM simultaneously. Arbiter use Round Robin method to grant a channel while other channel wait until it is granted. Arbiter choose the granted address and data and send to SRAM.

9.3.3 SRAM

SRAM uses multi blocks and multi banks construction to improve bandwidth and reduce address conflict. The higher bit of address will use to choose the block of SRAM, and the lower bit of address will use to choose the bank of SRAM.

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Chapter 10 DMAC

10.1 Overview

DMAC receives software control and peripheral request signals to realize data transmission between SoC modules; DMAC dynamically controls the binding and release of logical channels and physical channels to reduce power consumption and area; DMAC realizes data transmission through AXI interface, logical channel and physical channel.

DMAC supports the following features:

- Clock Domain
  - There are two asynchronous clocks: dmac_pclk, dmac_aclk
  - APB3 slave logic and all logical channels use dmac_pclk
  - AXI3 master logic and all physical channels use dmac_aclk
- Reset
  - There are two asynchronous resets: dmac_prstn, dmac_arstn
  - Independent reset for APB, logical channels, physical channels, DMAC Core
  - Support software reset for DMAC APB, DMAC Core, DMAC channels
- Overall Features
  - Supports 48 logical channels, and 2 physical channels
  - Supports 39 groups of peripheral request interfaces
  - Support dynamic binding and static binding
  - Supports software memory structure based on CMD Entry and LLI
  - Supports three transfer levels: dma transfer level, block level, and transaction level
  - Supports DMAC as flow controller
  - Supports little endian format
- DMAC Logical Channel (LCH)
  - Supports DMA kill/resume/flush
  - Supports three DMA transfer types: M2M, M2P, P2M
  - Supports three kinds of multi-block transfer: contiguous, reload, link list
  - Supports dynamic expansion of link list
  - Supports three stride transfer mode
  - Supports independent configuration of src/dst multi-block type
  - Supports single transaction (one axi req with AxLEN=0)
  - Supports burst transaction (MSIZE: one or more axi req with AxLEN≥0)
- DMAC Physical Channel (PCH)
  - Each physical channel is occupied by only one logical channel at the same time, and automatically initiates channel release operation
  - Responsible for reading, parsing and updating CMD Entry
  - Independent internal data buffer
  - Automatically packaging/unpacking operations
- DMAC Slave Interface
  - APB3 protocol
  - Supports 32-bit data width
- DMAC Master Interface
  - AMBA3 AXI protocol
  - Supports 32-bit address width, and 128-bit data width
  - Configurable AXI burst size, maximum is 16 bytes
  - Configurable AXI burst length, maximum is 16 beats
  - Supports FIXED, INC burst type, not support WRAP
  - Supports AXI read/write outstanding, maximum is 16 for each PCH
  - Supports OKAY, SLVERR, DECERR response type
  - Supports AXI read data reorder for different ID, and AXI read data inorder for the same id
  - Configurable AXI control signals, shared by all channels: cache/protection/lock
  - Supports WLAST output and RLAST input
  - Supports read data interleaving
  - Not support WID, and write data interleaving

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- Not support AXI unaligned transfers
- DMAC BIND Arbiter
- Supports Dynamic bind and static bind
- Supports round robin polling for 16 input requests and authorizations
- DMAC AXI Arbiter
- Supports round robin polling for 16 input requests and authorizations
- Interrupt
- Supports global interrupt output and per-channel interrupt output
- Supports interrupt enable and clear
- Supports multiple interrupt types: dma transfer complete interrupt, block transfer complete interrupt, burst transaction complete interrupt, error interrupt

10.2 Block Diagram

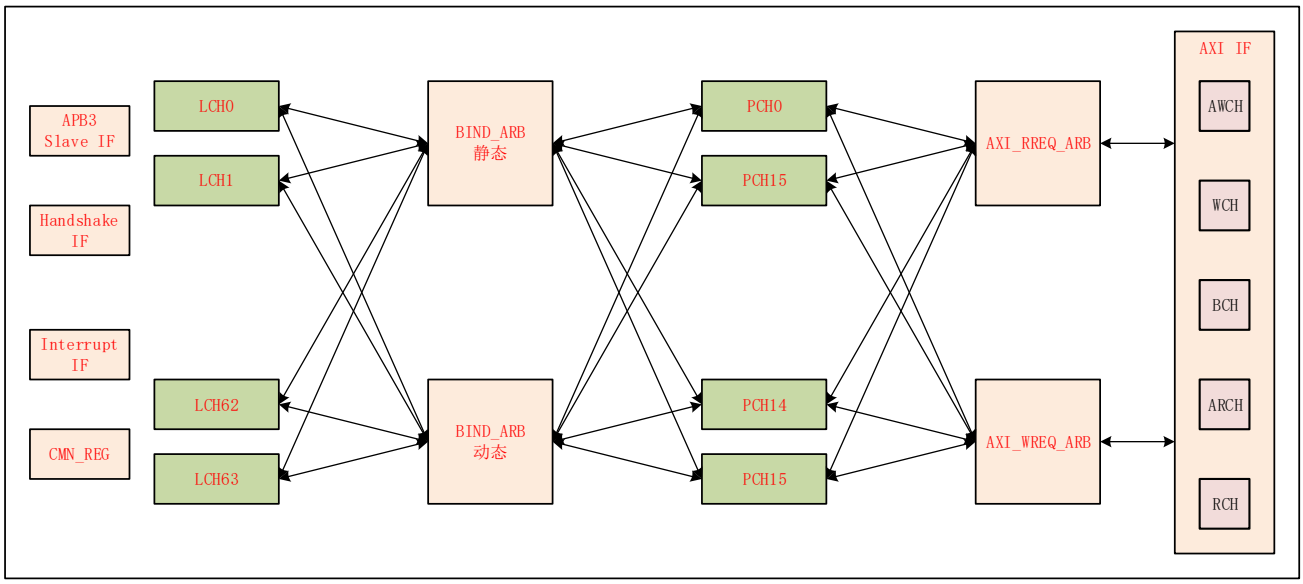

Figure 10-1 DMAC Top Structure

DMAC top-level modules are as follows:

- APB3 Slave IF:
  Responsible for the read/write access of DMAC internal registers
- AXI IF:
  Responsible for CMD/LLI read, CMD write back, SRC/DST data transmission
- Handshake IF:
  Including all groups of peripheral handshake signals
- Interrupt IF:
  Including global interrupt, logic channel interrupt
- CMN_REG:
  Common register group, used for controller enable, interrupt enable, software reset, etc
- LCH:
  Cooperate with PCH to realize data transmission
- PCH:
  Responsible for CMD/LLI reading, CMD write back, and data packaging, staging, and unpacking
- BIND_ARB:
  Responsible for dynamic binding and static binding
- AXI_*REQ_ARB:
  AXI access arbiter, which enables PCHs to access AXI master if

10.3 Function Description

10.3.1 DMAC Peripheral Interconnection

Table 10-1 DMAC Peripheral Interconnection

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DMAC Channel	Peripheral	TX/RX/M	Support Single
0	DMA_PERI_UART0_RX	RX/M	Y
1	DMA_PERI_UART0_TX	TX/M	N
2	DMA_PERI_UART1_RX	RX/M	Y
3	DMA_PERI_UART1_TX	TX/M	N
4	DMA_PERI_UART2_RX	RX/M	Y
5	DMA_PERI_UART2_TX	TX/M	N
6	DMA_PERI_UART3_RX	RX/M	Y
7	DMA_PERI_UART3_TX	TX/M	N
8	DMA_PERI_UART4_RX	RX/M	Y
9	DMA_PERI_UART4_TX	TX/M	N
10	DMA_PERI_UART5_RX	RX/M	Y
11	DMA_PERI_UART5_TX	TX/M	N
12	DMA_PERI_UART6_RX	RX/M	Y
13	DMA_PERI_UART6_TX	TX/M	N
14	DMA_PERI_UART7_RX	RX/M	Y
15	DMA_PERI_UART7_TX	TX/M	N
16	DMA_PERI_SAI0_RX	RX/M	N
17	DMA_PERI_SAI0_TX	TX/M	N
18	DMA_PERI_SAI1_RX	RX/M	N
19	DMA_PERI_SAI1_TX	TX/M	N
20	DMA_PERI_SAI2_RX	RX/M	N
21	DMA_PERI_SAI2_TX	TX/M	N
22	DMA_PERI_ASRC0_RX	RX/M	N
23	DMA_PERI_ASRC0_TX	TX/M	N
24	DMA_PERI_ASRC1_RX	RX/M	N
25	DMA_PERI_ASRC1_TX	TX/M	N
26	DMA_PERI_PDM_RX	RX/M	N
27	RSV	M	N
28	RSV	M	N
29	RSV	M	N
30	DMA_PERI_I2C1_RX	RX/M	Y
31	DMA_PERI_I2C1_TX	TX/M	N
32	RSV	M	N
33	RSV	M	N
34	DMA_PERI_I2C3_RX	RX/M	Y
35	DMA_PERI_I2C3_TX	TX/M	N
36	RSV	M	N
37	RSV	M	N
38	RSV	M	N
39	RSV	M	N
40	DMA_PERI_SPI0_RX	RX/M	Y
41	DMA_PERI_SPI0_TX	TX/M	N
42	DMA_PERI_SPI1_RX	RX/M	Y
43	DMA_PERI_SPI1_TX	TX/M	N
44	DMA_PERI_CAN0_RX	RX/M	N
45	DMA_PERI_CAN1_RX	RX/M	N
46	DMA_PERI_DSMC0	RX/TX/M	N
47	DMA_PERI_DSMC1	RX/TX/M	N

Notes:TX/RX/M:**TX**-Memory to Peripheral, **RX**-Peripheral to Memory, **M**-Memory to Memory

10.3.2 DMAC Peripheral Handshake Interface

DMAC peripheral handshake interface only supports DMAC as flow controller, and does not

support peripheral as flow controller.
The following figure shows the interaction module:

- PERI Side:
  The peripheral initiates peri_req/peri_single and receives peri_ack;
  peri-req/peri_single is a mutually exclusive relationship;
- DMA Side:
  Receive mutually exclusive req/single and return ack.

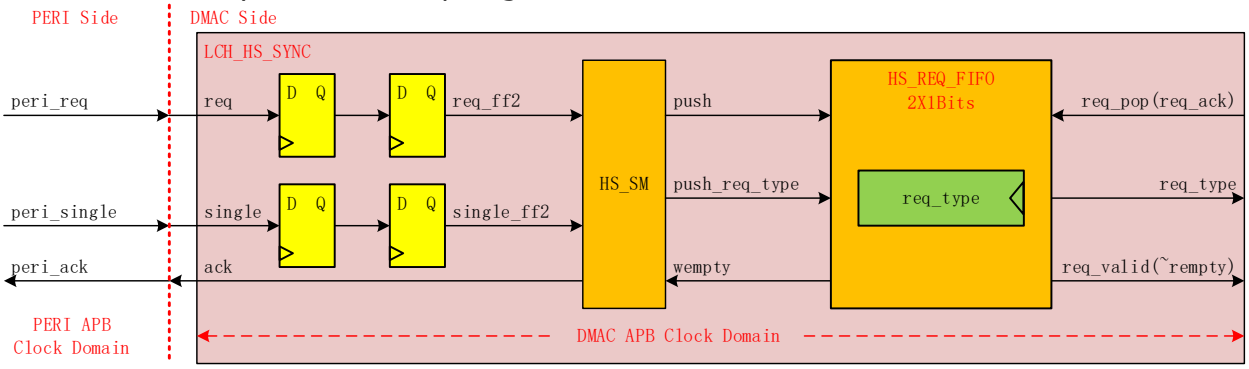

Figure 10-2 Peripheral Handshake Interface

The workflow of the interaction module is as follows:

1. no peripheral request is being processed, and HS_SM waits for req/single to be valid:
a) req=1: HS_SM generates a burst transaction request
b) single=1: HS_SM generates a single transaction request
c) req=0 & single=0: HS_SM waits for req/single to be valid
2. HS_SM writes the generated transaction request into HS_REQ_FIFO:
a) req_type=0, indicating a single transaction request
b) req_type=1, indicating a burst transaction request
3. HS_SM keeps waiting for wempty to be valid:
a) The assertion of wempty means DMAC has completed the current transaction transfer
4. DMAC executes the transaction transfer, then asserts req_pop to pop HS_REQ_FIFO:
a) After req_pop is valid, HS_REQ_FIFO becomes empty, and wempty asserted
5. HS_SM detects that wempty is valid and generates ack;
6. HS_SM generates ack, and continues to wait for req=0 & single=0, then return to idle state.

10.3.2.1 PERI_RX-DMAC Handshake Interface

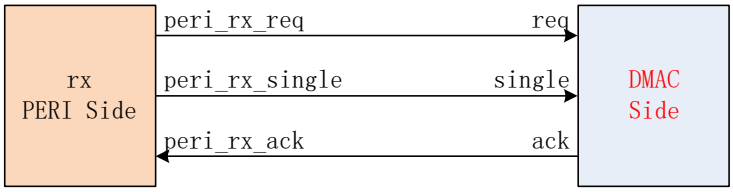

Figure 10-3 PERI_RX-DMAC Handshake Interface

- peri_rx_req:
a) Peripheral asserts peri_rx_req, indicating that a source burst transaction transfer can be executed
b) As long as RX FIFO entry is greater than RX FIFO threshold, peri_rx_req will be raised, and the rising edge will trigger a burst request
c) After peri_rx_req is raised, it needs to remain valid until peri_rx_ack asserted
- peri_rx_single:
a) Peripheral asserts peri_rx_single, indicating that a source single transaction transfer can be executed
b) Only when the peripheral RX FIFO is not empty and after timeout, the dma_ src_single can be raised, and the rising edge triggers a single request
c) After the peri_rx_single asserted, it needs to remain valid until the peri_rx_ack asserted

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d) After timeout, peri_rx_req/peri_rx_single can be valid at the same time; dmac handles peripheral requests according to peri_rx_req->peri_rx_single priority order, and the first in first service order

- peri_rx_ack:

a) DMAC asserts peri_rx_ack, indicating that the execution of the current transaction transfer is completed
b) When peripheral samples peri_rx_ack to be asserted, it pulls down the peri_rx_req, peri_rx_single
c) Then the peripheral asserts peri_rx_req, peri_rx_single according to the RX FIFO entry and timeout status

10.3.2.2 PERI_TX-DMAC Handshake Interface

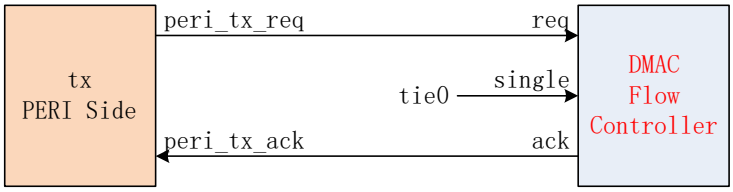

Figure 10-4 PERI_TX-DMAC Handshake Interface

- peri_tx_req:

a) Peripheral asserts peri_tx_req, indicating that a destination burst transaction transfer can be executed
b) As long as TX FIFO entry is less than TX FIFO threshold, peri_tx_req will be raised, and the rising edge will trigger a burst request
c) After peri_tx_req is raised, it needs to remain valid until peri_tx_ack asserted

- peri_tx_single:

a) Peripheral asserts peri_tx_single, indicating that a destination single transaction transfer can be executed
b) As long as TX FIFO is not full, peri_tx_single will be raised, and the rising edge will trigger a single request
c) DMAC don't use this signal

- peri_tx_ack:

a) DMAC asserts peri_tx_ack, indicating that the current transaction transfer completed
b) When peripheral samples peri_tx_ack to be asserted, it pulls down the peri_tx_req, peri_tx_single

10.3.3 DMAC Interrupt

10.3.3.1 Interrupt Interface

DMAC interrupt interface is divided into two types:

- dmac_intr: Global interrupt status, generated by all LCH interrupts
- dmac_lch_intr[*]: Per-channel interrupt status

10.3.3.2 Interrupt Types

LCH interrupt types refer to LCH_IS register, mainly including:

- Channel status interrupt
- LLI status interrupt
- Data transfer interrupt
- AXI master response interrupt

10.3.3.3 Interrupt Structure

Interrupt registers are divided into interrupt status registers and interrupt enable registers. After the interrupt source is triggered, the corresponding interrupt status register is set; The interrupt status will be output to the DMAC interrupt interface only when the corresponding interrupt enable register is valid.

DMAC_CFG.DMAC_IE is the global interrupt enable register, which controls whether all interrupt status can output to the interrupt interface.

The logic of interrupt sources, interrupt registers and interrupt interfaces is shown in the figure below.

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```
拼接DMAC_IS0/1寄存器为DMAC_IS:
    CMN.DMAC_IS = {CMN.DMAC_IS1, CMN.DMAC_IS0};

每个逻辑通道内部的中断组合:
    lch_intr[k] = | (LCH[k].LCH_IS & LCH[k].LCH_IE);

DMAC_IS的逻辑:
    CMN.DMAC_IS[k] = lch_intr[k] ? 1'b1 : CMN.DMAC_IS[k];

最终，per-channel中断输出逻辑为:
    dmac_ch_intr[k] = DMAC_CFG.DMAC_IE & lch_intr[k];

最终，全局中断输出逻辑为:
    dmac_intr = DMAC_CFG.DMAC_IE & ( | CMN.DMAC_IS);
```

Figure 10-5 DMAC Interrupt Structure

10.3.4 Arbitration Scheme

10.3.4.1 BIND_ARB allocates PCH

BIND_ARB is divided into dynamic arbiter(DYN_ARB) and static arbiter(STA_ARB).

On the one hand, DYN_ARB receives 64 LCH dynamic binding requests and outputs grant signals; On the other hand, it receives 16 PCH dynamic idle flags, and decodes the next available PCH index; When there is no free PCHs, the arbiter stops working.

On the one hand, STA_ARB receives 64 LCH static binding requests and outputs grant signals; On the other hand, it receives 16 PCH static idle flags; When there is no free PCHs, the arbiter stops working.

The structure of BIND_ARB, LCH and PCH is shown in the figure.

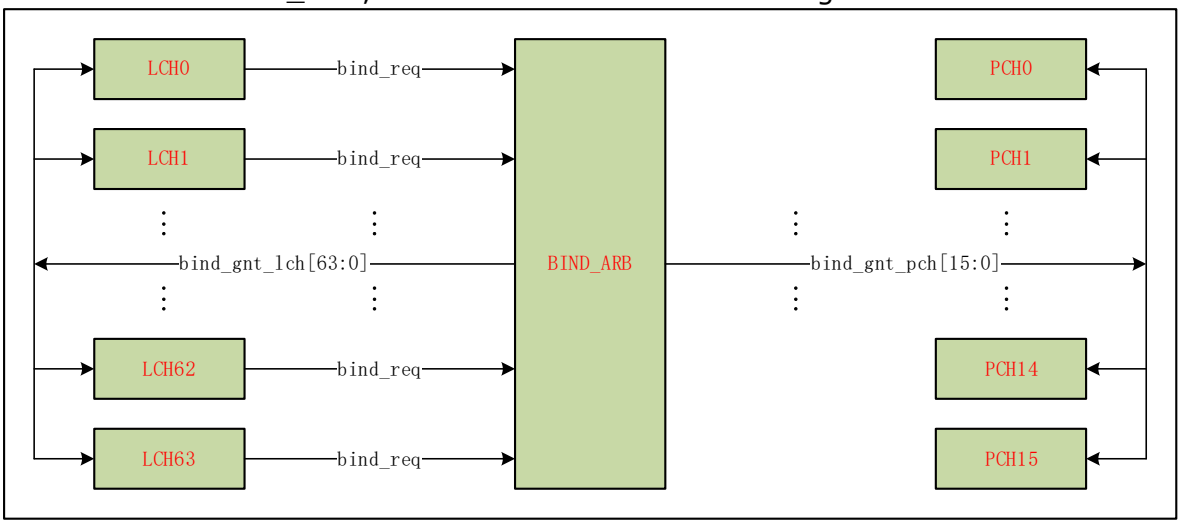

Figure 10-6 BIND_ARB Request and Grant Waveform

10.3.4.2 REL_ARB releases PCH

REL_ARB receives 16 PCH request signals REL_REQ and outputs grant signals REL_GNT_LCH/REL_GNT_PCH.

The structure of REL_ARB, LCH and PCH is shown in the figure.

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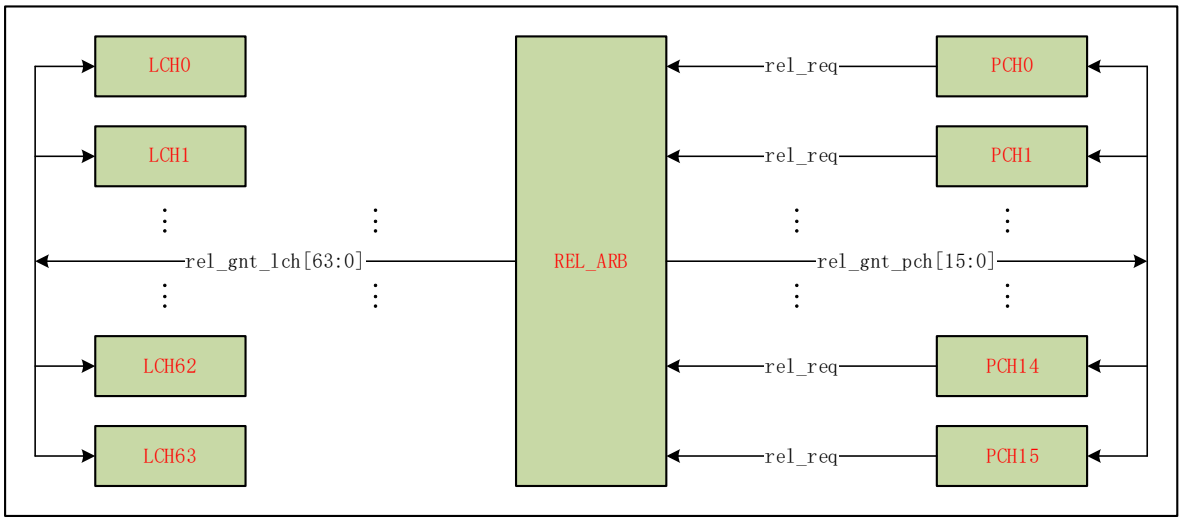

Figure 10-7 BIND_ARB Request and Grant Waveform

10.3.4.3 SEV_ARB generates trigger event

On the one hand, SEV_ARB receives 64 logic channel request signals SEV_REQ/SEV_REQ_ID and outputs grant signals WFE_TRG/WFE_TRG_ID.

WFE_TRG/WFE_TRG_ID is sent to all LCHs. Each LCH uses its own WFE_ID to compare with WFE_TRG_ID. If it is equal, the LCH is triggered and the corresponding transmission is executed.

The structure of SEV_ARB and LCH is shown in the figure.

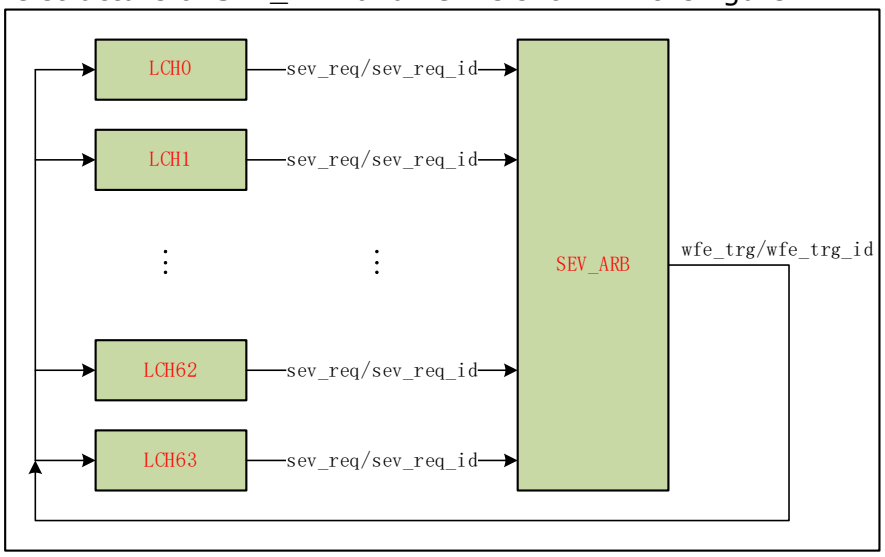

Figure 10-8 BIND_ARB Request and Grant Waveform

10.3.4.4 AXI_ARB allocates AXI Interface

AXI_REQ_ARB is divided into AXI_WREQ_ARB, AXI_RREQ_ARB, which controls PCHs to access axi write/read interface.

AXI_WREQ_ARB receives all DMA write requests, and selects one to access AXI write interface according to round-robin.
AXI_RREQ_ARB receives all DMA read requests, and selects one to access AXI read interface according to round-robin.

Access Type Priority:

- Access type priority of different channels:
  For read: CMD read=LLI read=AXI data read
  For write: CMD write=AXI data write
- Access type priority of the same channel:
  Different types of read requests occur sequentially: CMD read → LLI read → AXI data

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read
Different types of write requests occur sequentially: AXI data write → CMD write

10.3.5 DMAC Register Structure

10.3.5.1 APB Interface Structure

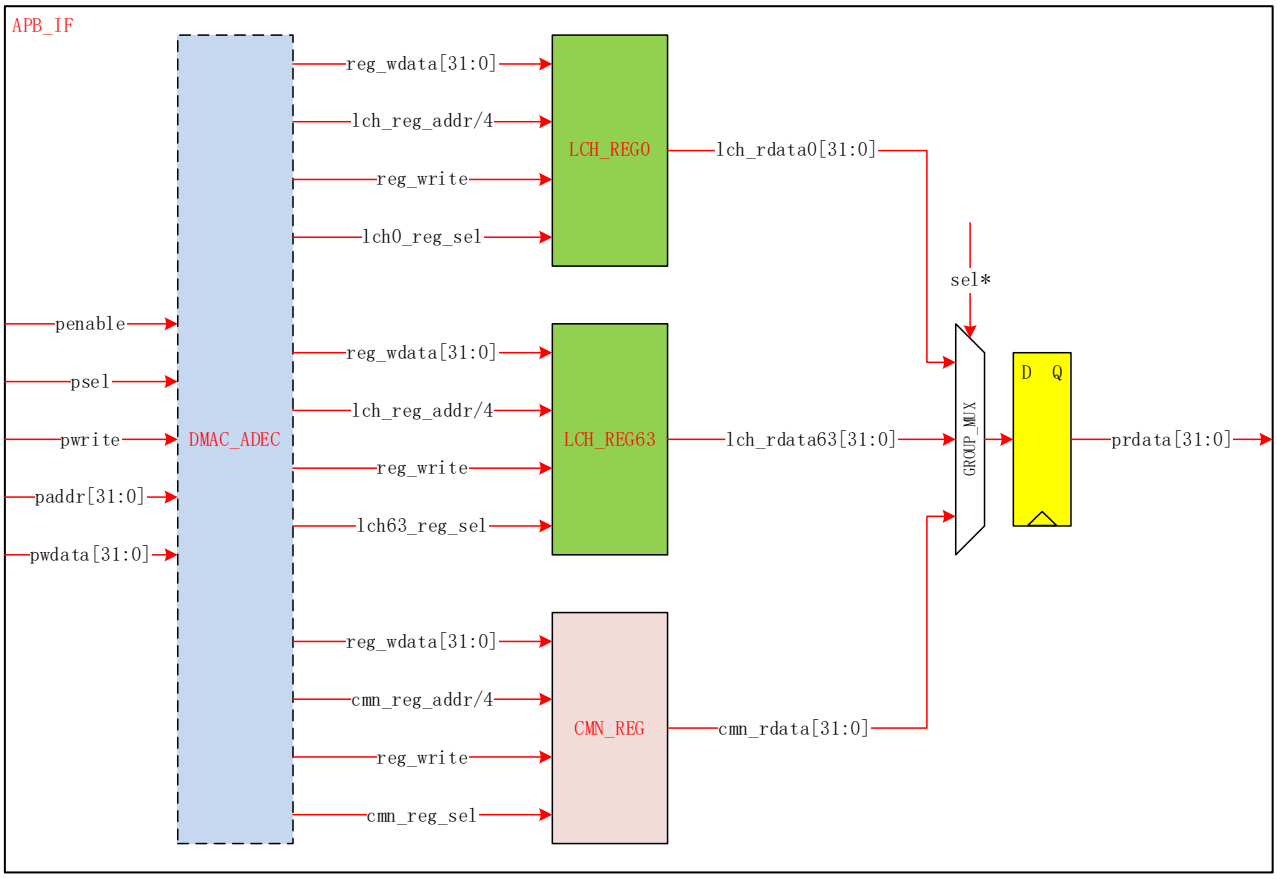

Figure 10-9 APB Interface Structure

10.3.5.2 Register Map

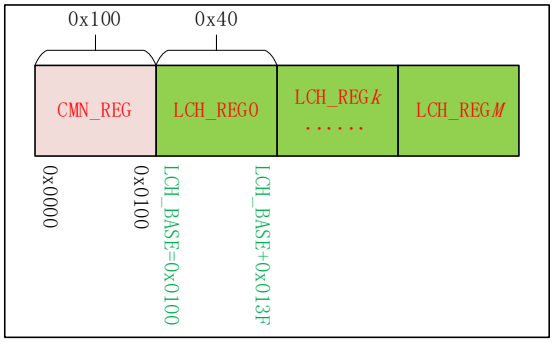

Figure 10-10 DMAC Register Map

The registers are organized as follows:

- CMN_REG: 0x00--0xFF
- LCH_REG: 0x00--0x3F for each, LCH_BASE=0x0100
- The overall address space size depends on LCH_NUM

10.3.6 DMAC Memory Structure

10.3.6.1 CMD Entry Structure

DMAC uses CMD Entry and link list as the interface between software and hardware. The software packages DMA transmission parameters into CMD Entry and link list and writes them into memory.

Then the software writes the CMD Entry base address to the LCH and starts DMA transfer; DMAC is responsible for reading CMD Entry and link list, executing data transfer, and

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updating DMA transfer status back to CMD Entry.

The software can then read the CMD Entry to obtain DMA transfer status, block transfer status and other information.

The CMD Entry structure is shown in the figure below:

- TFR_CTL0: MSIZE, LLI and Interrupt Control
- TFR_CTL1: DMA Source and Destination Transfer Control
- SAR: Source Address Low of DMA Transfer
- DAR: Destination Address Low of DMA Transfer
- BLOCK_TS: Total Block Transfer Size in Bytes
- LLP_NXT: Starting Address Low in Memory of Next LLI
- SAR_HIGH: Source Address High of DMA Transfer
- DAR_HIGH: Destination Address High of DMA Transfer
- LLP_NXT_HIGH: Starting Address High in Memory of Next LLI
- LLI_IDX: Current LLI Tag
- TFR_CFG: DMA Transfer Configuration Information
- BLOCK_CS: Completed Block Transfer Size in Bytes
- SAR_RLD: Initial Source Address Low for Auto-Reload
- DAR_RLD: Initial Destination Address Low for Auto-Reload
- SAR_RLD_HIGH: Initial Source Address High for Auto-Reload
- DAR_RLD_HIGH: Initial Destination Address High for Auto-Reload
- CH_NUM: The ch number in one frame
- CH_SIZE: The ch size
- STRIDE_INC: Stride Transfer Address Increament

CMD Entry contains the entire LLI structure (0x00-0x1F), Used to temporarily save the LLI currently being processed; Each binding operation will trigger the PCH to read the CMD Entry and LLI, and the writeback operation will write the LLI currently being processed back to the CMD Entry (0x00-0x1F), The next LLI will be read only when the current LLI transfer is completed.

The “RSV” fields must be initialized to 0. Otherwise, unexpected behavior may occur.

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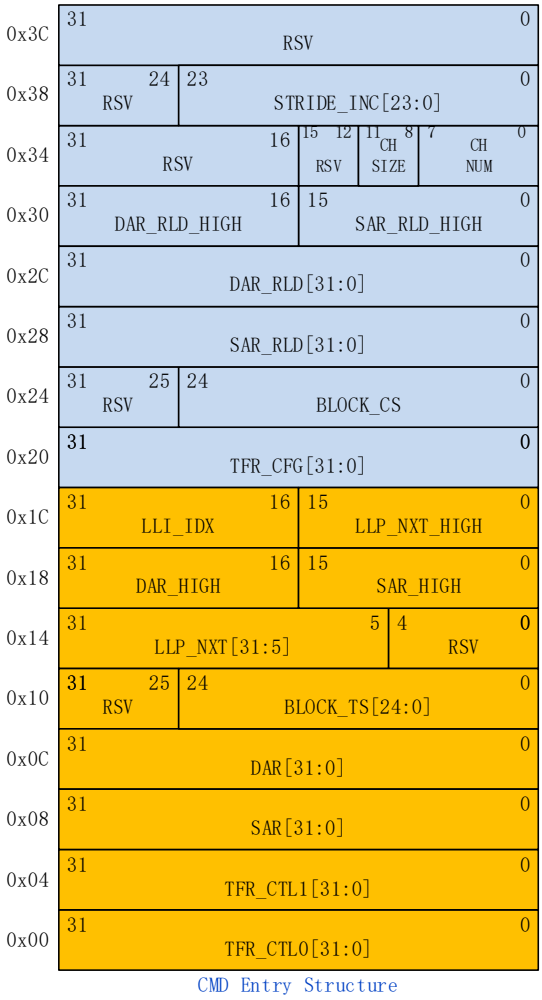

Figure 10-11 CMD Entry Structure

10.3.6.2 LLI Structure

Link List Item (LLI) structure is shown in the figure below:

- TFR_CTL0: MSIZE, LLI and Interrupt Control
- TFR_CTL1: DMA Source and Destination Transfer Control
- SAR: Source Address Low of DMA Transfer
- DAR: Destination Address Low of DMA Transfer
- BLOCK_TS: Total Block Transfer Size in Bytes
- LLP_NXT: Starting Address Low in Memory of Next LLI
- SAR_HIGH: Source Address High of DMA Transfer
- DAR_HIGH: Destination Address High of DMA Transfer
- LLP_NXT_HIGH: Starting Address High in Memory of Next LLI
- LLI_IDX: Current LLI Tag

The “RSV” fields must be initialized to 0. Otherwise, unexpected behavior may occur.

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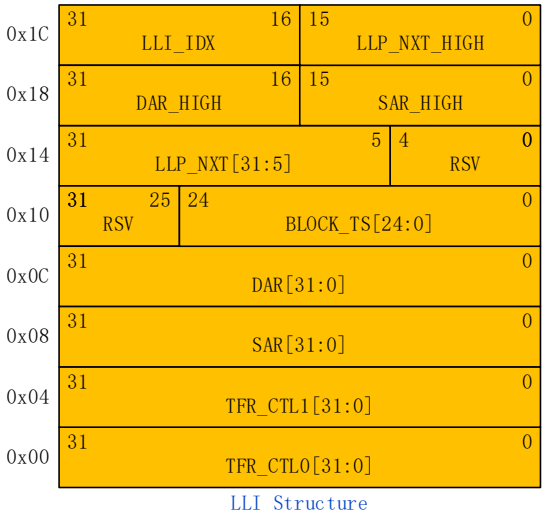

Figure 10-12 LLI Structure

10.3.6.3 Detail Fields Description

Register	Offset	Description
TFR_CTL0	0x00	DMA Transfer Control Register 0
TFR_CTL1	0x04	DMA Transfer Control Register 1
SAR	0x08	DMA Transfer Source Address Register, low 32 bits
DAR	0x0C	DMA Transfer Destination Address Register, low 32 bits
BLOCK_ON BLOCK_TS	0x10	Block Transfer in Progress Indication DMA Transfer Block Size in Bytes
LLP_NXT	0x14	DMA Next LLI Pointer Register, low 32 bits
DAR_HIGH SAR_HIGH	0x18	DMA Transfer Destination Address Register, high 16 bits DMA Transfer Source Address Register, high 16 bits
LLI_IDX LLP_NXT_HIGH	0x1C	LLI Index Tag DMA Next LLI Pointer Register, high 16 bits
TFR_CFG	0x20	DMA Transfer Configuration Register
BLOCK_CS	0x24	DMA Transfer completed Block Size in Bytes
SAR_RLD	0x28	DMA Initial Source Address for Auto-Reload, low 32 bits
DAR_RLD	0x2C	DMA Initial Destination Address for Auto-Reload, low 32 bits
DAR_RLD_HIGH SAR_RLD_HIGH	0x30	DMA Initial Destination Address for Auto-Reload, high 16 bits DMA Initial Source Address for Auto-Reload, high 16 bits
STRIDE_CH_SIZE STRIDE_CH_NUM	0x34	DMA Stride Transfer byte number in one channel DMA Stride Transfer channel num in one frame
STRIDE_INC	0x38	Stride Transfer Address Increament
RSV	0x3C	RSV

0x00-TFR_CTL0

Bits	Name	Attr	Reset Value	Description
31:15	MSIZE	R	0	Burst Transaction Length Number of bytes to be read/written from/to the source/destination every time a burst

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				transaction request is made from the corresponding hardware handshaking interface. Burst Transaction Length=(MSIZE) Bytes **Note:** This field is not applicable when servicing a single transaction request. In this case, the AXI burst length is forced to 0.
14:5	RSV	R	0	Reserved
4	CNT_CLR	R	0	Clear LLI_CNT in LCH On completion of Block Transfer Values: - 1: Clear LLI_CNT - 0: Not clear LLI_CNT
3	IOC	R	0	Interrupt On completion of Block Transfer This bit is used to control the BLOCK_DONE_IS interrupt generation on a block by block basis. Values: - 1: Enables LCH_IS.BLOCK_DONE_IS field - 0: Disables LCH_IS.BLOCK_DONE_IS field **Note:** This field is only applicable for Link List based Multi-Block types of any transfer type.
2	LLI_WAIT	R	0	LLI Wait Indicates whether fetches the next LLI automatically from the memory once the current block completed. Values: - 0: Automatically fetches the next LLI - 1: Logic Channel Stalls and Waits Resume
1	LLI_LAST	R	0	LLI Last Indicates whether the LLI fetched from the memory is the last one. Values: - 0: Not last LLI - 1: Last LLI **LLI based Multi-Block Transfer:** DMAC Channel uses this bit to decide if another LLI fetch is needed in the current DMA Transfer. - If this bit is 0, DMAC Channel fetches the next LLI from the address pointed out by LLP_NXT field in the current LLI. - If this bit is 1, DMAC Channel understands that current block is the final block in the DMA Transfer and ends the DMA Transfer once the AMBA transfer corresponding to the current block completes.
0	LLI_VALID	R	0	LLI Valid Indicates whether the content of the LLI fetched from the memory is valid. Values: - 0: LLI is invalid - 1: LLI is valid **LLI based Multi-Block Transfer:** This field is loaded from the LLI. On noticing this bit as 0, DMAC Channel discards the LLI and asserts the LLI_INVALID_IS.

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				This error condition causes the DMAC Channel to halt the corresponding channel gracefully. DMAC Channel waits until software writes 1 to LCH_TFR_CMD.DMA_RESUME to indicate valid LLI availability before attempting another LLI read operation.

0x04-TFR_CTL1

Bits	Name	Attr	Reset Value	Description
31	RSV	R	0	Reserved
30:27	AWOSR	R	0	Destination Burst Outstanding Number
26:21	AWLEN	R	0	Destination Burst Length AXI burst length used for destination data transfer. The specified burst length is used for destination data transfer till the extent possible; remaining transfers use maximum possible value. Burst Length=(AWLEN+1) Beats
20:18	AWSIZE	R	0	Destination Burst Size Values: - 0: Destination Transfer width is 1 byte - 1: Destination Transfer width is 2 bytes - 2: Destination Transfer width is 4 bytes - 3: Destination Transfer width is 8 bytes - 4: Destination Transfer width is 16 bytes
17	RSV	R	0	Reserved
16	AWBURST	R	0	Destination Burst Type Indicates whether to increment the destination address on every destination transfer. Values: - 0: FIXED - 1: INCR
15	RSV	R	0	Reserved
14:11	AROSR	R	0	Source Burst Outstanding Number
10:5	ARLEN	R	0	Source Burst Length AXI burst length used for source data transfer. The specified burst length is used for source data transfer till the extent possible; remaining transfers use maximum possible value. Burst Length=(ARLEN+1) Beats
4:2	ARSIZE	R	0	Source Burst Size Values: - 0: Source Transfer width is 1 byte - 1: Source Transfer width is 2 bytes - 2: Source Transfer width is 4 bytes - 3: Source Transfer width is 8 bytes - 4: Source Transfer width is 16 bytes
1	RSV	R	0	Reserved
0	ARBURST	R	0	Source Burst Type Indicates whether to increment the source address on every source transfer. Values: - 0: FIXED

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				- 1: INCR

0x08-SAR

Bits	Name	Attr	Reset Value	Description
31:0	SAR	R	0	Current Source Address of DMA Transfer, low 32 bits Updated after each source transfer. The ARBURST fields in the CMD/LLI determines whether the address increments or is left unchanged on every source transfer throughout the Block Transfer.

0x0C-DAR

Bits	Name	Attr	Reset Value	Description
31:0	DAR	R	0	Current Destination Address of DMA Transfer, low 32 bits Updated after each destination transfer. The AWBURST fields in the CMD/LLI determines whether the address increments or is left unchanged on every destination transfer throughout the Block Transfer.

0x10-BLOCK_TS

Bits	Name	Attr	Reset Value	Description
31:25	RSV	R	0	Reserved
24:0	BLOCK_TS	R	0	Block Transfer Size The number programmed into BLOCK_TS field indicates the total number of bytes to be transferred in a DMA Block Transfer. Block Transfer Size=(BLOCK_TS) Bytes

0x14-LLP_NXT

Bits	Name	Attr	Reset Value	Description
31:5	LLP_NXT	R	0	Starting Address [31:5] of Next LLI, low 32 bits Starting Address in Memory of next LLI if block chaining is enabled. The five LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-byte boundary. LLI access always uses the burst size (arsize/awsize) that is same as the data bus width and cannot be changed or programmed to anything other than this. DMAC Channel will fetch the entire LLI (32 bytes) in one AXI burst.
4:0	RSV	R	0	Reserved

0x18-DAR_HIGH/SAR_HIGH

Bits	Name	Attr	Reset Value	Description
31:16	DAR_HIGH	R	0	Current Destination Address of DMA Transfer,

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				high 16 bits Updated after each destination transfer. The AWBURST fields in the CMD/LLI determines whether the address increments or is left unchanged on every destination transfer throughout the Block Transfer.
15:0	SAR_HIGH	R	0	Current Source Address of DMA Transfer, high 16 bits Updated after each source transfer. The ARBURST fields in the CMD/LLI determines whether the address increments or is left unchanged on every source transfer throughout the Block Transfer.

0x1C-LLI_IDX/LLP_NXT_HIGH

Bits	Name	Attr	Reset Value	Description
31:16	LLI_IDX	R	0	Current LLI Index Tag
15:0	LLP_NXT_HIGH	R	0	Starting Address [31:5] of Next LLI, high 16 bits Starting Address in Memory of next LLI if block chaining is enabled. The five LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-byte boundary. LLI access always uses the burst size (arsize/awsize) that is same as the data bus width and cannot be changed or programmed to anything other than this. DMAC Channel will fetch the entire LLI (32 bytes) in one AXI burst.

0x20-TFR_CFG

Bits	Name	Attr	Reset Value	Description
31:15	RSV	R	0	Reserved
14:13	STRIDE_MODE	R	0	Stride Transfer Mode Used only for memory access of M2M or M2P or P2M transfer type, and valid for the whole DMA Transfer hierarchy. Values: - 0: Stride Transaction Mode - 1: Stride SRC Mode - 2: Stride DST Mode
12	STRIDE_EN	R	0	Stride Transfer Enable Used only for memory access of M2M or M2P or P2M transfer type, and valid for the whole DMA Transfer hierarchy.
11:10	RSV	R	0	Reserved
9:8	TT_FC	R	0	Transfer Type and Flow Control Values: - 0: Transfer Type is memory to memory - 1: Transfer Type is memory to peripheral - 2: Transfer Type is peripheral to memory - 3: Transfer Type is peripheral to peripheral
7:6	RSV	R	0	Reserved

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5:4	DST_MT	R	0	Destination Multi-BlockTransfer Type These bits define the type of Multi-Block Transfer used for destination peripheral. Values: - 0: Contiguous - 1: Auto Reload - 2: Link List - 3: Reserved
3:2	RSV	R	0	Reserved
1:0	SRC_MT	R	0	Source Multi-BlockTransfer Type These bits define the type of Multi-Block Transfer used for source peripheral. Values: - 0: Contiguous - 1: Auto Reload - 2: Link List - 3: Reserved

0x24-BLOCK_CS

Bits	Name	Attr	Reset Value	Description
31:25	RSV	R	0	Reserved
24:0	BLOCK_CS	R	0	Completed Block Transfer Size This field indicates the completed number of bytes to be transferred in a DMA Block Transfer. Completed Block Transfer Size=(BLOCK_CS) Bytes

0x28-SAR_RLD

Bits	Name	Attr	Reset Value	Description
31:0	SAR_RLD	R	0	Reload Source Address of Block Transfer, low 32 bits

0x2C-DAR_RLD

Bits	Name	Attr	Reset Value	Description
31:0	DAR_RLD	R	0	Reload Destination Address of Block Transfer, low 32 bits

0x30-DAR_RLD_HIGH/SAR_RLD_HIGH

Bits	Name	Attr	Reset Value	Description
31:16	DAR_RLD_HIGH	R	0	Reload Destination Address of Block Transfer, high 16 bits
15:0	SAR_RLD_HIGH	R	0	Reload Source Address of Block Transfer, high 16 bits

0x34-STRIDE_ADDR_HIGH/STRIDE_CH_SIZE/NUM

Bits	Name	Attr	Reset Value	Description
31:12	RSV	R	0	Reserved
11:8	STRIDE_CH_SIZE	R	0	DMA Stride Transfer Byte Number in one channel
7:0	STRIDE_CH_NUM	R	0	DMA Stride Transfer Channel Number in one

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				frame

0x38-STRIDE_INC

Bits	Name	Attr	Reset Value	Description
31:24	RSV	R	0	Reserved
23:0	STRIDE_INC	R	0	Stride Transfer Address Increament When enabled, except for the native address increament, the address will have an additional increament after each burst Transaction Transfer. Used only for memory access of M2M or M2P or P2M transfer type, and valid for the whole DMA Transfer process. This field must be aligned to ARSIZE or AWSIZE of memory access. Stride Increament=(STRIDE_INC) Bytes

0x3C-RSV

Bits	Name	Attr	Reset Value	Description
31:0	RSV	R	0	Reserved

10.3.7 DMAC Block Transfer

10.3.7.1 Single Block Transfer

The software initiates a DMA transfer, including only one block; After the block transfer is completed, DMA transfer automatically ends, and the software does not need to initiate DMA resume; Simultaneous setting BLOCK_DONE_IS, DMA_DONE_IS.

The software configures SRC/DST_MT=2'b00 to initiate single block transfer.

10.3.7.2 Multiple Block Transfer

The software initiates a DMA transfer, including multiple block transfers; After each block transfer is completed, BLOCK_DONE_IS will assert; DMA transfer ends after the last block transfer is completed; When DMA Transfer ends, BLOCK_DONE_IS, DMA_DONE_IS will assert.

DMAC uses the following mechanisms to achieve multi-block transfer:

- Contiguous address
- Auto reload
- Link list

Contiguous Address:
Next Block Start Address=Previous Block End Address + 1

Auto Reload:
Next Block Start Address=Previous Block Start Address

Link List:
Next Block Start Address=Reload from Next LLI
After the block transfer is completed, DMAC reads the next LLI, and the block start address uses LLI.SAR, LLI.DAR.

The way to end multi block transfer depends on the selected multi block transfer type:

- If at least one of the source and destination uses the link list, then LLI_LAST=1 indicates that the current block is the last block; DMA transfer ends after the current block transfer ends.

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- If the source and destination do not use the link list, SRC/DST_MT=0 indicates that previous block is the last block and DMA transfer ends.

SRC_MT, DST_MT is independently configured by software, so multiple multi block types can be combined; The parameter register update mode depends on the combination mode, as shown in the following table.

Table 10-2 Multi-Block Type Combination

MB_TYPE		Register Update Method				No	Remarks
SRC_MT	DST_MT	SAR	DAR	TFR_CTL0 TFR_CTL1	BLOCK_TS		
00	00	No update	No update	No update	No update	1	Single block or last block of Multi-Block
00	01	Contiguous	Reloaded from initial value	Reloaded from initial value	Reloaded from initial value	2	-
00	10	Contiguous	Loaded from next LLI	Loaded from next LLI	Loaded from next LLI	3	-
01	00	Reloaded from initial value	Contiguous	Reloaded from initial value	Reloaded from initial value	4	-
01	01	Reloaded from initial value	Reloaded from initial value	Reloaded from initial value	Reloaded from initial value	5	-
01	10	Reloaded from initial value	Loaded from next LLI	Loaded from next LLI	Loaded from next LLI	6	-
10	00	Loaded from next LLI	Contiguous	Loaded from next LLI	Loaded from next LLI	7	-
10	01	Loaded from next LLI	Reloaded from initial value	Loaded from next LLI	Loaded from next LLI	8	-
10	10	Loaded from next LLI	Loaded from next LLI	Loaded from next LLI	Loaded from next LLI	9	-

10.4 Register Description

10.4.1 Common Registers

10.4.1.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

10.4.1.2 Registers Summary

Name	Offset	Size	Reset Value	Description
RKDMA_CMN_REG_DMAC_VER	0x0000	W	0x00010001	DMAC ID and Version Register
RKDMA_CMN_REG_DMAC_CFG	0x0004	W	0x00000000	DMAC Configuration Register
RKDMA_CMN_REG_DMAC_CTL0	0x0008	W	0x00000000	DMAC Control Register 0
RKDMA_CMN_REG_DMAC_CTL1	0x000C	W	0x00000000	DMAC Control Register 1
RKDMA_CMN_REG_DMAC_AXICTL	0x0010	W	0x00000000	DMAC AXI Control Register
RKDMA_CMN_REG_DMAC_DYNCTL	0x0014	W	0x00000000	DMAC Dynamic Clock Control Register
RKDMA_CMN_REG_DMAC_IS0	0x0018	W	0x00000000	DMAC Interrupt Status Register 0
RKDMA_CMN_REG_DMAC_IS1	0x001C	W	0x00000000	DMAC Interrupt Status Register 1
RKDMA_CMN_REG_DMAC_CAP0	0x0030	W	0x0FFDF06F	DMAC Capability Register 0
RKDMA_CMN_REG_DMAC_CAP1	0x0034	W	0x0078D87C	DMAC Capability Register 1
RKDMA_CMN_REG_DMAC_PCH_EN	0x0040	W	0x00000000	DMAC Physical Channel Enable

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Name	Offset	Size	Reset Value	Description
RKDMA_CMN_REG_DMAC_PCH_SEN	0x0044	W	0x00000000	DMAC Physical Channel Bind Static Enable

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

10.4.1.3 Detail Registers Description

RKDMA_CMN_REG_DMAC_VER

Address: Operational Base(0x20B80000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0001	DMAC_MAJVER DMAC Major Version Number
15:0	RO	0x0001	DMAC_MINVER DMAC Minor Version Number

RKDMA_CMN_REG_DMAC_CFG

Address: Operational Base(0x20B80000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	WE Write Enable Bit
15:3	RO	0x0000	reserved
2	RW	0x0	DMAC_IE This bit is used to globally enable the interrupt generation Values: - 0: DMAC interrupt logic is disabled - 1: DMAC interrupt logic is enabled
1	RW	0x0	DMAC_SRST DMAC Reset Request bit Values: - 0: DMAC software reset is not in progress - 1: DMAC software reset is initiated or in progress Software writes 1 to this bit to reset the DMAC and polls this bit to zero to return to normal state. When asserted, DMAC resets all the modules except this register.
0	RW	0x0	DMAC_EN This bit is used to enable the DMAC Values: - 0: DMAC disabled - 1: DMAC enabled Software sets this bit to 1 before any other operation of DMAC. When cleared to zero, DMAC resets all the modules except this register.

RKDMA_CMN_REG_DMAC_CTL0

Address: Operational Base(0x20B80000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RSV This bit is used to enable the address 40h align function Values: - 0: 40h align disabled - 1: 40h align enabled

RKDMA_CMN_REG_DMAC_CTL1

Address: Operational Base(0x20B80000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RSV Reserved

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RKDMA_CMN_REG_DMAC_AXICTL
Address: Operational Base(0x20B80000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:22	RW	0x0	ARPROT AXI ARPROT These bits form the arprot output of AXI3 master interface.
21:18	RW	0x0	ARCACHE AXI ARCACHE These bits form the arcache output of AXI3 master interface.
17:16	RW	0x0	ARLOCK AXI ARLOCK These bits form the arlock output of AXI3 master interface.
15:9	RO	0x00	reserved
8:6	RW	0x0	AWPROT AXI AWPROT These bits form the awprot output of AXI3 master interface.
5:2	RW	0x0	AWCACHE AXI AWCACHE These bits form the awcache output of AXI3 master interface.
1:0	RW	0x0	AWLOCK AXI AWLOCK These bits form the awlock output of AXI3 master interface.

RKDMA_CMN_REG_DMAC_DYNCTL
Address: Operational Base(0x20B80000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	MEM_DYNEN Memory Dynamic Clock Enable Values: - 0: Clock is in free running state - 1: Clock is in dynamic gating state
3	RW	0x0	ARB_DYNEN AXI Read Request Arbitration Dynamic Clock Enable Values: - 0: Clock is in free running state - 1: Clock is in dynamic gating state
2	RW	0x0	AXI_DYNEN AXI Interface Dynamic Clock Enable This bit controls all the channels in AXI interface. Values: - 0: Clock is in free running state - 1: Clock is in dynamic gating state
1	RW	0x0	PCH_DYNEN Physical Channel Dynamic Clock Enable This bit controls all the physical channels in DMAC. Values: - 0: Clock is in free running state - 1: Clock is in dynamic gating state

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Bit	Attr	Reset Value	Description
0	RW	0x0	LCH_DYNEN Logical Channel Dynamic Clock Enable This bit controls all the logical channels in DMAC. Values: - 0: Clock is in free running state - 1: Clock is in dynamic gating state

RKDMA_CMN_REG_DMAC_IS0
Address: Operational Base(0x20B80000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	W1C	0x00000000	IS Bit k: Logic Channel (k) Interrupt Status Bit

RKDMA_CMN_REG_DMAC_IS1
Address: Operational Base(0x20B80000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	W1C	0x00000000	IS Bit k: Logic Channel (k+32) Interrupt Status Bit

RKDMA_CMN_REG_DMAC_CAP0
Address: Operational Base(0x20B80000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:21	RO	0x07f	DMAC_BUF_DEPTH Buffer Depth = (DMAC_BUF_DEPTH+1)
20:18	RO	0x7	DMAC_MB_SUP DMAC Multi-Block Type Support Bit 0: CONT Bit 1: RELOAD Bit 2: LLI
17:14	RO	0x7	DMAC_TT_SUP DMAC Transfer Type Support Bit 0: M2M Bit 1: M2P Bit 2: P2M Bit 3: P2P
13	RO	0x1	DMAC_STRIDE_SUP DMAC Stride Transfer Support
12	RO	0x1	DMAC_STATIC_SUP DMAC Static Bind Support
11:6	RO	0x01	DMAC_PCH_NUM DMAC Physical Channel Number Channel Number = (DMAC_PCH_NUM+1)
5:0	RO	0x2f	DMAC_LCH_NUM DMAC Logic Channel Number Channel Number = (DMAC_LCH_NUM+1)

RKDMA_CMN_REG_DMAC_CAP1
Address: Operational Base(0x20B80000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:19	RO	0x0f	DMAC_AXOSR_SUP DMAC AXI Max Outstanding Number Support Max Outstanding Number = (DMAC_AXOSR_SUP +1)

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Bit	Attr	Reset Value	Description
18:14	RO	0x03	DMAC_AXADDR_WIDTH DMAC AXI Address Width Address Width = (32+DMAC_AXADDR_WIDTH-3) bits
13:11	RO	0x3	DMAC_AXBURST_SUP DMAC AXI Burst Support Bit 0: FIX Bit 1: INC Bit 2: WRAP
10:3	RO	0x0f	DMAC_AXLEN_SUP DMAC AXI Length Support Burst Length = (DMAC_AXLEN_SUP+1) beats
2:0	RO	0x4	DMAC_AXSIZE_SUP DMAC AXI Size Support AXI Size = (2^DMAC_AXSIZE_SUP) bytes

RKDMA_CMN_REG_DMAC_PCH_EN
Address: Operational Base(0x20B80000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	WE Write Enable Bit
15:0	RW	0x0000	PCH_EN Physical Channel Enable Request Values: - 0: Physical channel is in idle state, and channel logic is in reset state. - 1: Physical channel is in active state. Software sets this bit to 1 before any other operation to physical channel.

RKDMA_CMN_REG_DMAC_PCH_SEN
Address: Operational Base(0x20B80000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	WE Write Enable Bit
15:0	RW	0x0000	PCH_EN Physical Channel Enable Request Values: - 0: Physical channel is in idle state, and channel logic is in reset state. - 1: Physical channel is in active state. Software sets this bit to 1 before any other operation to physical channel.

10.4.2 Logic Channel Registers

10.4.2.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
RKDMA_LCH0_REG	0x20B80100
RKDMA_LCH1_REG	0x20B80140
RKDMA_LCH2_REG	0x20B80180
RKDMA_LCH3_REG	0x20B801C0
RKDMA_LCH4_REG	0x20B80200
RKDMA_LCH5_REG	0x20B80240

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Name	Base Address
RKDMA_LCH6_REG	0x20B80280
RKDMA_LCH7_REG	0x20B802C0
RKDMA_LCH8_REG	0x20B80300
RKDMA_LCH9_REG	0x20B80340
RKDMA_LCH10_REG	0x20B80380
RKDMA_LCH11_REG	0x20B803C0
RKDMA_LCH12_REG	0x20B80400
RKDMA_LCH13_REG	0x20B80440
RKDMA_LCH14_REG	0x20B80480
RKDMA_LCH15_REG	0x20B804C0
RKDMA_LCH16_REG	0x20B80500
RKDMA_LCH17_REG	0x20B80540
RKDMA_LCH18_REG	0x20B80580
RKDMA_LCH19_REG	0x20B805C0
RKDMA_LCH20_REG	0x20B80600
RKDMA_LCH21_REG	0x20B80640
RKDMA_LCH22_REG	0x20B80680
RKDMA_LCH23_REG	0x20B806C0
RKDMA_LCH24_REG	0x20B80700
RKDMA_LCH25_REG	0x20B80740
RKDMA_LCH26_REG	0x20B80780
RKDMA_LCH27_REG	0x20B807C0
RKDMA_LCH28_REG	0x20B80800
RKDMA_LCH29_REG	0x20B80840
RKDMA_LCH30_REG	0x20B80880
RKDMA_LCH31_REG	0x20B808C0
RKDMA_LCH32_REG	0x20B80900
RKDMA_LCH33_REG	0x20B80940
RKDMA_LCH34_REG	0x20B80980
RKDMA_LCH35_REG	0x20B809C0
RKDMA_LCH36_REG	0x20B80A00
RKDMA_LCH37_REG	0x20B80A40
RKDMA_LCH38_REG	0x20B80A80
RKDMA_LCH39_REG	0x20B80AC0
RKDMA_LCH40_REG	0x20B80B00
RKDMA_LCH41_REG	0x20B80B40
RKDMA_LCH42_REG	0x20B80B80
RKDMA_LCH43_REG	0x20B80BC0
RKDMA_LCH44_REG	0x20B80C00
RKDMA_LCH45_REG	0x20B80C40
RKDMA_LCH46_REG	0x20B80C80
RKDMA_LCH47_REG	0x20B80CC0

10.4.2.2 Registers Summary

Name	Offset	Size	Reset Value	Description
RKDMA_LCH_REG_LCH_CTL0	0x0000	W	0x00000000	Channel Control Register 0
RKDMA_LCH_REG_LCH_CTL1	0x0004	W	0x00000000	Channel Control Register 1
RKDMA_LCH_REG_LCH_CMDBA	0x0008	W	0x00000000	Channel CMD Entry Base Address Register
RKDMA_LCH_REG_LCH_TFR_CMD	0x000C	W	0x00000000	Channel Transfer Command Register

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Name	Offset	Size	Reset Value	Description
RKDMA_LCH_REG_LCH_CMDBA_HIGH	0x0010	W	0x00000000	Channel CMD Entry Base Address High Register
RKDMA_LCH_REG_LCH_IS	0x0014	W	0x00000000	Channel Interrupt Status Register
RKDMA_LCH_REG_LCH_IE	0x0018	W	0x00000000	Channel Interrupt Enable Register
RKDMA_LCH_REG_LCH_DBGS0	0x001C	W	0x00000000	Channel Debug Status 0 Register
RKDMA_LCH_REG_LCH_DBGC0	0x0020	W	0x00000000	Channel Debug Control 0 Register
RKDMA_LCH_REG_LCH_LLI_CNT	0x0030	W	0x00000000	Channel LLI Completed Number

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

10.4.2.3 Detail Registers Description

RKDMA_LCH_REG_LCH_CTL0

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	CH_EN Logic Channel Enable Request Values: - 0: Logic channel is in idle state, and channel logic is in reset state. - 1: Logic channel is in active state. Software sets this bit to 1 before any other operation to logic channel.

RKDMA_LCH_REG_LCH_CTL1

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RW	0x0	BIND_SEN Logic Channel Bind Static Enable
25	RW	0x0	SEV_EN Logic Channel DMASEV Enable Register When enabled, current channel will initiate one trigger event after each Block Transfer. The trigger event will be kept internally until target channel into WFE state. Values: - 0: disable DMASEV function - 1: enable DMASEV function
24	RW	0x0	WFE_EN Logic Channel DMAWFE Enable Register When enabled, current channel will wait one trigger event before each Block Transfer. Values: - 0: disable DMAWFE function - 1: enable DMAWFE function
23:20	RO	0x0	reserved
19:16	RW	0x0	BIND_PIDX_S Logic Channel Bind Static Peer Index Physical Channel Index of Logic Channel in Bind Static. Valid only when BIND_SEN is 1.

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Bit	Attr	Reset Value	Description
15:12	RO	0x0	reserved
11:6	RW	0x00	SEV_ID Logic Channel DMASEV ID Register
5:0	RW	0x00	WFE_ID Logic Channel DMAWFE ID Register

RKDMA_LCH_REG_LCH_CMDBA

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	CMDBA Starting Address [31:x] of CMD Entry(x>=6) Starting Address in Memory of CMD Entry. The x LSBs of the starting address are not stored because the address is assumed to be aligned to a (2^x)B boundary. CMD Entry access always uses the burst size (arsize/awsize)='h3. DMAC Channel will fetch the entire CMD Entry (64 bytes) in one AXI burst. This field is programmable before channel started.
5:0	RO	0x00	reserved

RKDMA_LCH_REG_LCH_TFR_CMD

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	WE Write Enable bit
15:14	RW	0x0	TT_FC Transfer Type and Flow Control Values: - 0: Transfer Type is memory to memory - 1: Transfer Type is memory to peripheral - 2: Transfer Type is peripheral to memory - 3: Reserved
13:12	RW	0x0	DST_MT Destination Multi-BlockTransfer Type These bits define the type of Multi-Block Transfer used for destination peripheral. Values: - 0: Contiguous - 1: Auto Reload - 2: Link List - 3: Reserved
11:10	RW	0x0	SRC_MT Source Multi-BlockTransfer Type These bits define the type of Multi-Block Transfer used for source peripheral. Values: - 0: Contiguous - 1: Auto Reload - 2: Link List - 3: Reserved
9:4	RO	0x00	reserved
3	RW	0x0	DMA_FLUSH DMAC Transfer Flush Request This bit is auto-cleared by hardware after flush done.

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Bit	Attr	Reset Value	Description
2	RW	0x0	DMA_RESUME DMAC Transfer Resume Request This bit is auto-cleared by hardware after 1T.
1	RW	0x0	DMA_KILL DMAC Transfer Kill Request This bit is auto-cleared by hardware after 1T.
0	RW	0x0	DMA_START DMAC Transfer Start Request This bit is auto-cleared by hardware after 1T.

RKDMA_LCH_REG_LCH_CMDBA_HIGH

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	CMDBA_HIGH Base Address High of CMD Entry This field is reserved when dmac is in 32-bit configuration. CMDBA_HIGH[x-1:0]: x=1 when ADDR_WIDTH=33 x=2 when ADDR_WIDTH=34 ... x=15 when ADDR_WIDTH=47 x=16 when ADDR_WIDTH=48

RKDMA_LCH_REG_LCH_IS

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	W1C	0x0	LLI_WAIT_IS LLI Wait Event Occurred This event occurs if LCH_TRF_CTL.LLI_WAIT bit is seen to be 1 once DMAC channel completes current block transfer. This event condition causes the DMAC to halt the corresponding channel gracefully; The channel waits till software writes LCH_TRF_CMD.DMA_RESUME to indicate valid LLI availability. Event Interrupt is generated if the corresponding bit in LCH_IE is enabled. Values: - 1: LLI Wait event detected - 0: No LLI Wait events
11	W1C	0x0	LLI_INVALID_IS LLI Invalid Error This error occurs if LCH_TRF_CTL.LLI_VALID bit is seen to be 0 during DMAC channel LLI fetch phase. This error condition causes the DMAC to halt the corresponding channel gracefully; The channel waits till software writes LCH_TRF_CMD.DMA_RESUME to indicate valid LLI availability. Error Interrupt is generated if the corresponding bit in LCH_IE is enabled. Values: - 1: LLI Invalid error detected - 0: No LLI Invalid errors

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Bit	Attr	Reset Value	Description
10	W1C	0x0	LLI_RD_ERR_IS LLI Read Response Error Response Error detected by master interface during LLI read operation. Error Interrupt is generated if the corresponding bit in LCH_IE is enabled. Values: - 1: LLI Read Response Errors detected - 0: No LLI Read Response Errors
9	W1C	0x0	CMD_WR_ERR_IS CMD Write Response Error Response Error detected by master interface during CMD Entry write operation. Error Interrupt is generated if the corresponding bit in LCH_IE is enabled. Values: - 1: CMD Write Response Errors detected - 0: No CMD Write Response Errors
8	W1C	0x0	CMD_RD_ERR_IS CMD Read Response Error Response Error detected by master interface during CMD Entry read operation. Error Interrupt is generated if the corresponding bit in LCH_IE is enabled. Values: - 1: CMD Read Response Errors detected - 0: No CMD Read Response Errors
7	W1C	0x0	DST_WR_ERR_IS Destination Write Response Error Response Error detected by master interface during destination data transfer. Error Interrupt is generated if the corresponding bit in LCH_IE is enabled. Values: - 1: Destination Response Errors Detected - 0: No Destination Response Errors
6	W1C	0x0	SRC_RD_ERR_IS Source Response Error Response Error detected by master interface during source data transfer. Error Interrupt is generated if the corresponding bit in LCH_IE is enabled. Values: - 1: Source Response Errors Detected - 0: No Source Response Errors
5	W1C	0x0	DST_STRANS_DONE_IS Destination Single Transaction Done Values: - 1: Destination single transaction completed - 0: Destination single transaction not completed
4	W1C	0x0	SRC_STRANS_DONE_IS Source Single Transaction Done Values: - 1: Source single transaction completed - 0: Source single transation not completed

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Bit	Attr	Reset Value	Description
3	W1C	0x0	DST_BTRANS_DONE_IS Destination Burst Transaction Done Values: - 1: Destination burst transaction completed - 0: Destination burst transaction not completed
2	W1C	0x0	SRC_BTRANS_DONE_IS Source Burst Transaction Done Values: - 1: Source burst transaction completed - 0: Source burst transation not completed
1	W1C	0x0	BLOCK_DONE_IS Block Transfer Done This indicates to the software that the DMAC channel has completed the requested Block Transfer. The DMAC channel sets this bit to 1 when the transfer is successfully completed. Values: - 1: Block Transfer completed - 0: Block Transfer not completed
0	W1C	0x0	DMA_DONE_IS DMA Transfer Done This indicates to the software that the DMAC channel has completed the requested DMA Transfer. The DMAC channel sets this bit to 1 along with setting LCH_IS.BLOCK_DONE_IS bit to 1 when the last Block Transfer is completed. Values: - 1: DMA Transfer completed - 0: DMA Transfer not complete

RKDMA_LCH_REG_LCH_IE

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	LLI_WAIT_IE LLI Wait Event Occurred Interrupt Enable Bit
11	RW	0x0	LLI_INVALID_IE LLI Invalid Error Interrupt Enable Bit
10	RW	0x0	LLI_RD_ERR_IE LLI Read Response Error Interrupt Enable Bit
9	RW	0x0	CMD_WR_ERR_IE CMD Write Response Error Interrupt Enable Bit
8	RW	0x0	CMD_RD_ERR_IE CMD Read Response Error Interrupt Enable Bit
7	RW	0x0	DST_WR_ERR_IE Destination Write Response Error Interrupt Enable Bit
6	RW	0x0	SRC_RD_ERR_IE Source Read Response Error Interrupt Enable Bit
5	RW	0x0	DST_STRANS_DONE_IE Destination Single Transaction Done Interrupt Enable Bit
4	RW	0x0	SRC_STRANS_DONE_IE Source Single Transaction Done Interrupt Enable Bit
3	RW	0x0	DST_BTRANS_DONE_IE Destination Burst Transaction Done Interrupt Enable Bit

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Bit	Attr	Reset Value	Description
2	RW	0x0	SRC_BTRANS_DONE_IE Source Burst Transaction Done Interrupt Enable Bit
1	RW	0x0	BLOCK_DONE_IE Block Transfer Done Interrupt Enable Bit
0	RW	0x0	DMA_DONE_IE DMA Transfer Done Interrupt Enable Bit

RKDMA_LCH_REG_LCH_DBGS0

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	BIND_PIDX Logic Channel Bind Physical Channel Index Status Valid only when BIND_VLD is 1.
11	RO	0x0	BIND_VLD Logic Channel Bind Valid Status Values: - 0: Logic Channel is not in bind state - 1: Logic Channel is in bind state
10:4	RO	0x00	reserved
3:0	RO	0x0	DMA_CS DMA State Machine Values: - 0: DMA_IDLE - 1: DMA_WFE - 2: DMA_BLK_START - 3: DMA_PERI_WAIT - 4: DMA_BIND - 5: DMA_TRANS - 6: DMA_REL - 7: DMA_PERI_ACK - 8: DMA_PERI_FNSH - 9: DMA_SEV - 10: DMA_BLK_DONE - 11: DMA_SUSPD - 12: DMA_ERR - 13: DMA_DONE

RKDMA_LCH_REG_LCH_DBGC0

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	WO	0x0	SOFT_SEV Channel Software WFE Trigger Register Setting this bit will trigger current channel to exit from WFE state, and to start one Block Transfer. The software trigger event will be kept internally until current channel into WFE state. This bit is auto-cleared by hardware after 1T.
23:13	RO	0x000	reserved
12:0	WO	0x0000	SOFT_IS Channel Software Trigger Interrupt Register Each bit corresponds to each bit in the LCH_IS register. Each bit is auto-cleared by hardware after 1T.

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RKDMA_LCH_REG_LCH_LLI_CNT
Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	W1C	0x0000	LLI_CNT This counter increments by one each time the DMAC channel completes one Block Transfer.

10.5 Application Notes

10.5.1 DMAC Software Flow

The software configures the CMN_REG, LCH_REG to control the behavior of DMAC. The following describes the functions of DMAC and the software control flow.

10.5.1.1 DMAC Initialization

1) Enable DMAC:
   DMAC_CFG.DMAC_EN=1
2) Initiate software reset:
   DMAC_CFG.DMAC_SRST=1
3) Wait software reset completed by polling:
   Wait DMAC_CFG.DMAC_SRST=0
4) Clear interrupt status:
   LCH_REG*k*.LCH_IS=0xFFFFFFFF
   DMAC_IS0=0xFFFFFFFF, DMAC_IS1=0xFFFFFFFF
5) Enable LCH interrupt:
   LCH_REG*k*.LCH_IE=0xFFFFFFFF
6) Enable global interrupt:
   DMAC_CFG.DMAC_IE=1
7) Enable PCH*j*, to participate in the binding process:
   CMN_REG.PCH_EN=(0x1<<(16+*j*)) | (0x1<<*j*), disabled by default

10.5.1.2 DMAC Software Reset

1) Initiate software reset:
   DMAC_CFG.DMAC_SRST=1
2) Wait software reset completed by polling:
   Wait DMAC_CFG.DMAC_SRST=0
3) DMAC software reset completed.

10.5.1.3 Channel DMA Start

1) DMA start is only used to triger DMA transfer to be started; and it does not work when DMA transfer is in progress;
2) Software initiates DMA start:
   LCH_TFR_CMD.DMA_START=1
   LCH_TFR_CMD.TT_FC/SRC_MT/DST_MT are the start parameters of dma transfer

10.5.1.4 Channel DMA Kill

1) DMA kill is only used to stop the current dma transfer when a response error occurs; In other cases, it does not work;
2) After receiving the response error interrupt, the software first initiates a DMA kill:
   LCH_TFR_CMD.DMA_KILL=1
   DMA kill operation will cause DMA_DONE_IS interrupt
3) After that, the software clears the interrupt status and performs error handling;
4) The software clears LCH_CTL.CH_EN to release LCH.

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10.5.1.5 Channel DMA Resume

1) DMA resume is only used to wake up the current DMA transfer from the DMA suspend state; In other cases, it does not work;
2) Software initiates DMA resume:
   LCH_TFR_CMD.DMA_RESUME=1
3) The software waits for the completion of the current block transfer or DMA transfer.

10.5.1.6 Channel DMA Flush

1) Software initiates DMA flush, which is only applicable to P2M transfer:
   LCH_TFR_CMD.DMA_FLUSH=1
2) DMA_DONE_IS interrupt is generated after flush operation is completed;
3) Software waits for LCH_ IS.DMA_DONE_IS, and performs interrupt handling:
   The software reads the CMD Entry to obtain the status of the data transmission
4) After the flush process, LCH_TFR_CMD.DMA_FLUSH reset automatically;
5) DMA transfer ends directly after the flush process:
   The remaining data of the current block transfer will not be transferred
   The remaining blocks of the current DMA transfer will not be transferred
6) The software clears LCH_CTL.CH_EN to release LCH.

10.5.1.7 Channel DMA SEV

1) The software configures LCH_CTL1 to enable the DMASEV function:
   LCH_CTL1.SEV_EN = 1
   LCH_CTL1.SEV_ID = 6'hx
2) After the current LCH finishes Block Transfer, an event with the index of SEV_ID=x will be triggered:
   The event will be sent to all other LCHs and the trigger status will be recorded
3) Other LCHs(WFE_EN=1) will detect the trigger status:
   If the trigger status is valid, execute Block Transfer once
   If the trigger status is invalid, wait for the event, and then execute Block Transfer onc

10.5.1.8 Channel DMA WFE

1) Software configuration LCH_CTL1 enables DMAWFE function:
   LCH_CTL1.WFE_EN = 1
   LCH_CTL1.WFE_ID = 6'hx
2) The current LCH waits for the event SEV_ID=x before Block Transfer:
   After receiving the event, the current LCH will record the trigger status
3) Before the next Block Transfer, detects the trigger status:
   If the trigger status is valid, execute Block Transfer once
   If the trigger status is invalid, wait for the event, and then execute Block Transfer once

10.5.1.9 Channel Static Bind

1) The software configures LCH*k* to use static binding:
   LCH_REG*k*.LCH_CTL1.BIND_SEN=1, LCH static binding enabled
   LCH_REG*k*.LCH_CTL1.BIND_PIDX_S=*j*, *j* is the static binding PCH's index
2) Software configuration PCH*j* is in static state:
   CMN_REG.DMAC_PCH_SEN=(0x1<<(16+*j*)) | (0x1<<*j*), PCH static binding enable
3) The software continues to configure other LCH and PCH static binding registers:
   It is necessary to ensure that each static LCH has a corresponding static PCH
4) Static binding supports the following configurations:
   One LCH can only be statically bound to one PCH
   It can support the static binding of one or more LCHs to one PCH

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It also supports static binding of multiple LCHs to multiple PCHs

10.5.1.10 Link List Wait

1) Add LLI_WAIT to avoid conflicts between LLI fetch and LLI software construction;
2) DMAC reads LLI, parses LLI fields, and executes block transfer;
3) DMAC queries LLI_WAIT after block transfer done (LLI_VALID=1 implicitly):

If LLI_WAIT=0, LLI_LAST=0, DMAC reads the next LLI immediately

If LLI_WAIT=1, LLI_LAST=0, DMAC generates LLI_WAIT interrupt, and waits for the software resume before reading the next LLI

If LLI_LAST=1, DMAC asserts DMA_DONE_IS, and DMA transfer ends

10.5.1.11 DMAC Error Handling

DMAC can receive CMD-Read/LLI-Read/AXI Data-Read/AXI Data-Write/CMD-Write response errors; If an error occurs:

- The current PCH will not send new read/write requests
- The current PCH waits for the end of all outstanding requests
- The current PCH is released, and the remaining FIFO data becomes invalid:
  Software can read the CMD Entry to continue data transmission from the error point
- The current logic channel error interrupt status is set;
- If interrupt is enabled, DMAC outputs interrupt signal and CPU executes interrupt routine;
- Interrupt routine:
  Firstly, initiate DMA kill and stop the DMA transfer, which trigers DMA_DONE_IS interrupt
  Then clear the interrupt status, and finally execute error processing
- If an error occurs when accessing non-memory peripheral, the CPU needs to reconfigure the peripheral after detecting an interrupt.

10.5.1.12 Stride Transaction Transfer

DMAC supports three stride modes, where mode0 is Stride Transaction Transfer.

For Stride Transaction Transfer:

Every time a Peripheral Transaction Transfer is completed, the memory access address is incremented additionally.

Support: M2P & (ARBURST=INC)、P2M & (AWBURST=INC).

The following figure shows the transmission of P2M in Stride Transaction mode.

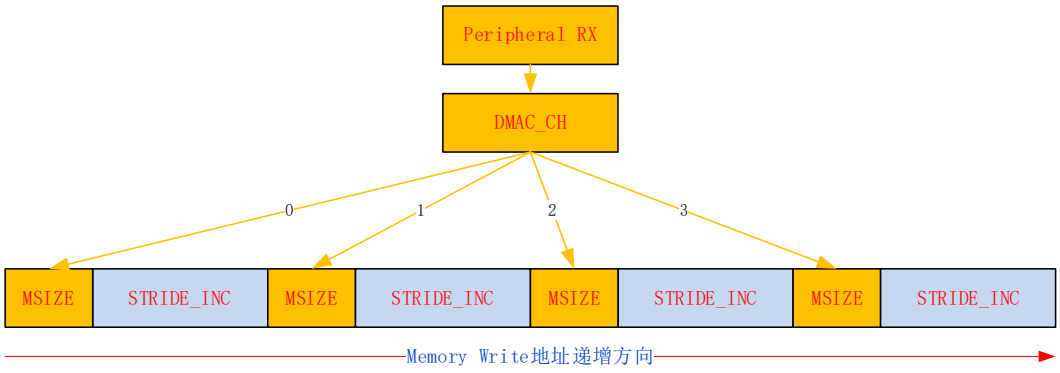

Figure 10-13 P2M in Stride Transaction mode

The following figure shows the transmission of M2P in Stride Transaction mode.

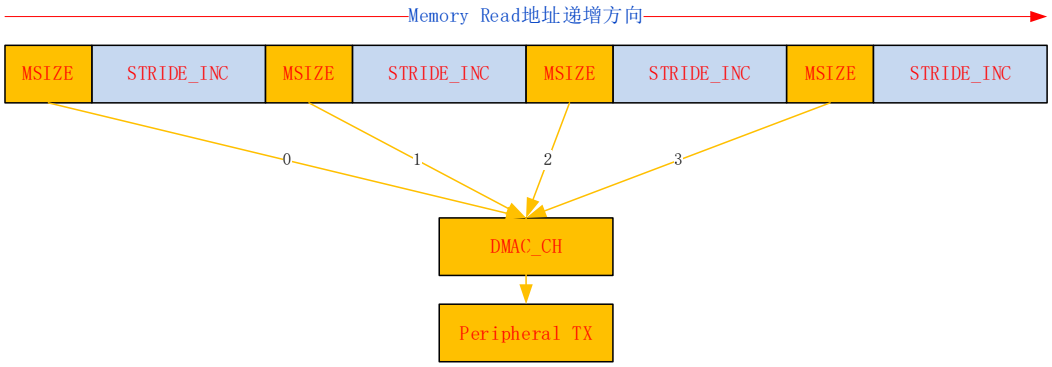

Figure 10-14 M2P in Stride Transaction mode

Stride Transaction Transfer configuration:

1) Stride transfer enable:
   CMD.TFR_CFG.STRIDE_EN=1
2) Select Stride Mode:
   CMD.TFR_CFG.STRIDE_MODE=STRIDE_TRANS
3) Configure Stride Increment:
   CMD.TFR_CFG.STRIDE_INC=24'hxxxxx
4) Execute M2P/P2M transmission:
   For M2P, hardware increments SAR
   For P2M, hardware increments DAR

10.5.1.13 Stride SRC/DST Transfer

DMAC supports three Stride Modes, where mode1/2 are Stride SRC/DST Transfer.

For Stride SRC Transfer:
Each time frame.ch Transfer is completed, SAR is incremented additionally;

Support: M2M & (ARBURST=INC)、M2P & (ARBURST=INC)、P2M & (ARBURST=INC).

For Stride DST Transfer:
For every frame.ch Transfer completed, DAR will increase additionally;

Support: M2M & (AWBURST=INC)、M2P & (AWBURST=INC)、P2M & (AWBURST=INC).

For M2M transmission, the relationship between Block, frame and ch is as follows:

- Block = H * frame, (H>=1, and is an integer)
- frame = N * ch, (N>=1, and is an integer)

For M2P/P2M transmission, the relationship between Block, MSIZE, frame and ch is as follows:

- One peripheral burst request, and the data byte number is MSIZE
- Block = H * MSIZE, (H>=1, and is an integer)
- MSIZE = M * frame, (M>=1, which is an integer)
- frame = N * ch, (N>=1, and is an integer)

The following figure shows the transmission of M2P in Stride SRC mode.

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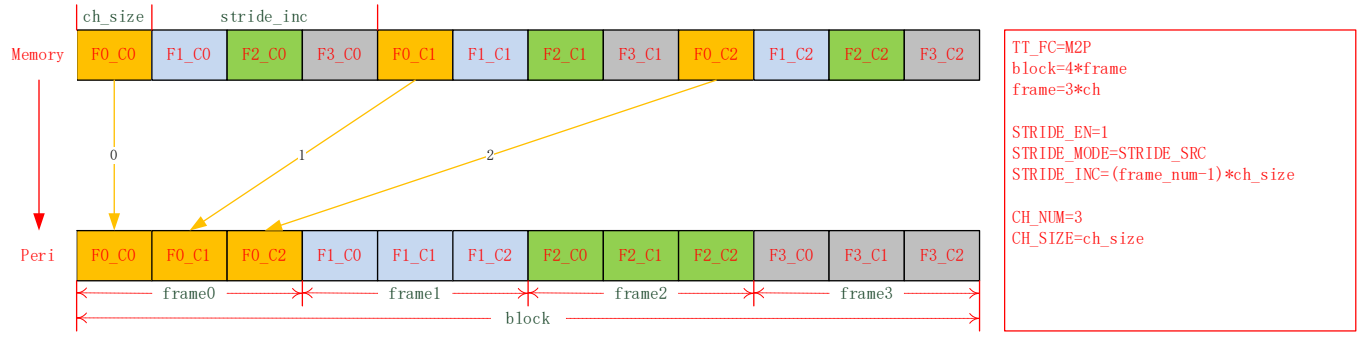

Figure 10-15 M2P in Stride SRC mode

The following figure shows the transmission of P2M in Stride DST mode.

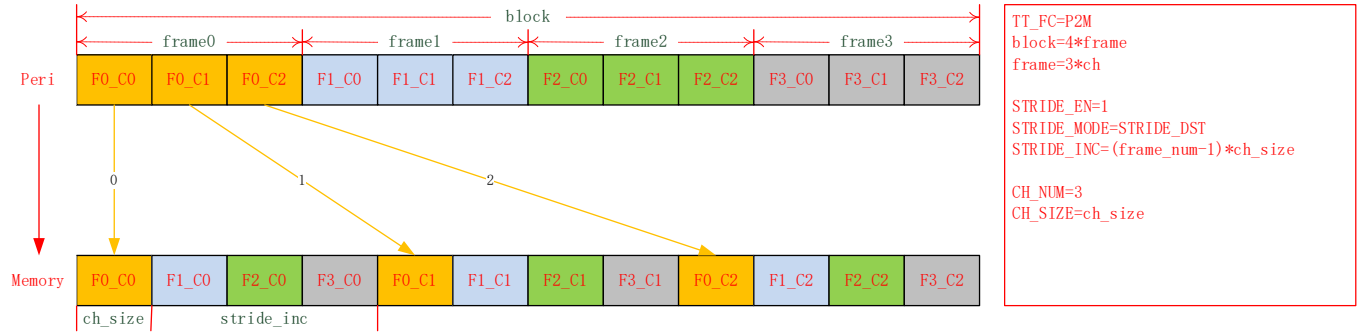

Figure 10-16 P2M in Stride DST mode

Stride SRC/DST Transfer configuration:

1) Stride transfer enable:
   CMD.TFR_CFG.STRIDE_EN=1
2) Select Stride Mode:
   CMD.TFR_CFG.STRIDE_MODE=STRIDE_SRC/DST
3) Configure Stride Increment:
   CMD.TFR_CFG.STRIDE_INC=24'hxxxxx
4) Execute M2M/M2P/P2M transmission:
   M2M & (ARBURST=INC) & (STRIDE_SRC): hardware increments SAR
   M2M & (AWBURST=INC) & (STRIDE_DST): hardware increments DAR

   M2P & (ARBURST=INC) & (STRIDE_SRC): hardware increments SAR
   M2P & (AWBURST=INC) & (STRIDE_DST): hardware increments DAR

   P2M & (ARBURST=INC) & (STRIDE_SRC): hardware increments SAR
   P2M & (AWBURST=INC) & (STRIDE_DST): hardware increments DAR

10.5.1.14 Single Block Transfer

The steps of single block transfer are as follows:

1) Select the LCH when the software detects the transmission demand;
2) Software configures LCH_ CTL.CH_EN=1 to enable the LCH;
3) The software constructs a CMD Entry to set dma transfer parameters:
   CMD.TT_FC=M2M/M2P/P2M
   CMD.SRC/DST_MT=2'b00/2'b00
   CMD Entry other fields
4) Software writes the CMD Entry base address to LCH_CMDBA;
5) Software configures LCH_TFR_CMD.DMA_START=1 to start data transmission:
   LCH_TFR_CMD.TT_FC=CMD.TT_FC

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LCH_TFR_CMD.SRC_MT/DST_MT=CMD.SRC/DST_MT

6) According to LCH_TFR_CMD.TT_FC, the LCH determines when to ask for the PCH:
   M2M: The LCH immediately asks for the PCH
   M2P/P2M: The LCH waits for the peripheral request to be valid before asking for the PCH
7) The PCH initiates a CMD read request to parse and update the parameter registers;
8) DMAC performs data transfer:
   M2M: After the whole block data transmission is completed, the block transfer ends
   M2P/P2M: When a burst transaction is completed, an acknowledge is returned until the end of block transfer
9) After block transfer, if LCH_TFR_CMD.SRC/DST_MT=2'b00/2'b00, DMA transfer will end automatically;
10) Software wait/query interrupt status:
    DMA/BLOCK_DONE_IS asserted: Software reads relevant registers and processes block data
11) After DMA transfer, the software releases memory space and clears LCH_CTL.CH_EN, and the LCH enters the idle state.

When BLOCK_TS is not an integer multiple of (ARLEN+1)*2^ARSIZE or (AWLEN+1)*2^AWSIZE, the last remaining data will use the largest possible burst length, and the unaligned part will be indicated by byte enable.

For example, BLOCK_TS=104h, SAR=000h/ARLEN=7h/ARSIZE=3h, DAR=400h/AWLEN=7h/AWSIZE=2h, then:

- The last read request is SAR=100h/ARLEN=0h/ARSIZE=3h (High 32bit dropped);
- The last write request is DAR=500h/AWLEN=0h/AWSIZE=2h/WSTRB=0Fh (High 32bit dropped).

10.5.1.15 Link List Based Multi-Block Transfer

Link list based multi block transfer steps are as follows:

1) Select the LCH when the software detects the transmission demand;
2) Software configures LCH_ CTL.CH_ EN=1 to enable the LCH;
3) The software constructs a CMD Entry to set dma transfer parameters:
   CMD.TT_FC=M2M/M2P/P2M
   CMD.SRC/DST_MT=2'bxx/2’bxx (At least one party equals 2’b10)
   CMD.LLP_NXT
   CMD Entry other fields
4) The software constructs one or more LLIs and writes them to memory:
   The first LLI base address needs to be written to CMD.LLP_NXT
   The software can construct all LLIs in advance, or dynamically expand the link list
   Link list dynamic expansion function can be controlled by LLI_VALID/LLI_WAIT/LLI_LAST
5) Software writes the CMD Entry base address to LCH_CMDBA;
6) Software configures LCH_TFR_CMD.DMA_START=1 to start data transmission:
   LCH_TFR_CMD.TT_FC=CMD.TT_FC
   LCH_TFR_CMD.SRC_MT/DST_MT=CMD.SRC/DST_MT
7) According to LCH_TFR_CMD.TT_FC, the LCH determines when to ask for the PCH:
   M2M: The LCH immediately asks for the PCH
   M2P/P2M: The LCH waits for the peripheral request to be valid before asking for the PCH

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8) The PCH initiates a CMD read request to parse and update the parameter registers;
9) According to SRC/DST_MT, the PCH initiates a LLI read request to parse and update the parameter register;
10) If LLI_VALID=1, the PCH performs the current LLI data transmission:
    M2M: Transmit the whole block at one time
    M2P/P2M: Transmit one transaction at a time and return one acknowledge
11) If LLI_VALID=0, PCH releases:
    The LCH enters the SUSPD state, and the LLI_INVALID_IS is raised and wait for DMA resume
12) After the current transmission is completed, the PCH is released:
    M2M: After the current block transfer is completed, write back the CMD Entry and release the PCH
    M2P/P2M: After the current transaction transfer is completed, write back the CMD Entry and release the PCH
13) The LCH receives the PCH release signal, sets the interrupt status, and waits for the next transmission:
    M2M: Assert BLOCK_DONE_IS, and go to 14)
    M2P/P2M: Assert *TRANS_DONE_IS; If block transfer ends and LLI_LAST=1, go to 14); Otherwise, go to 7)
14) After block transfer ends, BLOCK_DONE_IS asserted:
    If LLI_LAST=1, DMA transfer ends, the LCH enters the END state, and the DMA_DONE_IS is set
    If LLI_LAST=0 & LLI_WAIT=1, the LCH enters the SUSPD state, LLI_WAIT_IS is set, and waits DMA resume
    If LLI_LAST=0 & LLI_WAIT=0, the LCH enters the BLOCK_START state, and continues to transfer
15) After DMA transfer, the software releases memory space and clears LCH_CTL.CH_EN, the LCH enters the idle state.

When BLOCK_TS is not an integer multiple of (ARLEN+1)*2^ARSIZE or (AWLEN+1)*2^AWSIZE, the last remaining data will use the largest possible burst length, and the unaligned part will be indicated by byte enable.

If LLI_INVALID/LLI_WAIT interrupt asserted, the following resume steps need to be performed:
1) Software clears the interrupt status register;
2) Software constructs LLI for the next block;
3) Software sets LCH_TFR_CMD.DMA_RESUME to initiate DMA resume.

10.5.1.16 Auto Reload Based Multi-Block Transfer

Auto reload based multi block transfer steps are as follows:
1) Select the LCH when the software detects the transmission demand;
2) Software configures LCH_ CTL.CH_ EN=1 to enable the LCH;
3) Software writes the CMD Entry base address to LCH_CMDBA;
4) Software configures LCH_TFR_CMD.DMA_START=1 to start data transmission:
    LCH_TFR_CMD.TT_FC=CMD.TT_FC
    LCH_TFR_CMD.SRC_MT/DST_MT=CMD.SRC/DST_MT
5) According to LCH_TFR_CMD.TT_FC, the LCH determines when to ask for the PCH:
    M2M: The LCH immediately asks for the PCH
    M2P/P2M: The LCH waits for the peripheral request to be valid before asking for the

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PCH

6) The PCH initiates a CMD read request to parse and update the parameter registers;
7) The PCH performs data transmission:
   M2M: Transmit the whole block at one time
   M2P/P2M: Transmit one transaction at a time and return one acknowledge
8) After the current transmission is completed, the PCH is released:
   M2M: After the current block transfer is completed, write back the CMD Entry and release the PCH
   M2P/P2M: After the current transaction transfer is completed, write back the CMD Entry and release the PCH
9) The LCH receives the PCH release signal, sets the interrupt status, and waits for the next transmission:
   M2M: Assert BLOCK_DONE_IS, and go to 10)
   M2P/P2M: Assert *TRANS_DONE_IS; If block transfer ends, go to 10); Otherwise, go to 5)
10) After block transfer ends, BLOCK_DONE_IS asserted:
   The LCH enters SUSPD state, and the software can configure LCH_TFR_CMD. SRC_MT/DST_MT, and then initiate DMA resume
11) The LCH waits for DMA resume when in the SUSPD state:
   If the next block needs to be transmitted, keep SRC/DST_MT remains unchanged, and the software initiates DMA resume
   Otherwise, set SRC/DST_MT=2'b00/2'b00, and the software initiates DMA resume
12) DMA Resume received by LCH:
   If SRC_MT=0 & DST_MT=0, the LCH enters the END state, and DMA_DONE_IS is set
   If SRC_MT!=0 | DST_MT!=0, the LCH transmits the next block again
13) After DMA transfer, the software releases memory space and clears LCH_CTL.CH_EN, the LCH enters the idle state.

When BLOCK_TS is not an integer multiple of (ARLEN+1)*2^ARSIZE or (AWLEN+1)*2^AWSIZE, the last remaining data will use the largest possible burst length, and the unaligned part will be indicated by byte enable.

10.5.1.17 Contiguous Based Multi-Block Transfer

SRC/DST_MT=2'b00/2'b00 is a single block indication, or is a last block indication of multi-block. Contiguous based multi-block transfer can be implemented indirectly using link list.

Next LLI.LCH_SAR=Previous Block Source End Address + 1;
Next LLI.LCH_DAR=Previous Block Destination End Address + 1.

When BLOCK_TS is not an integer multiple of (ARLEN+1)*2^ARSIZE or (AWLEN+1)*2^AWSIZE, the last remaining data will use the largest possible burst length, and the unaligned part will be indicated by byte enable.

10.5.2 DMAC Programming Requirements

10.5.2.1 Hardware Handshake

- Only support dma_req, dma_single, dma_ack
- Peripheral is not supported as a flow controller

10.5.2.2 AXI Master

- AWLEN/ARLEN range:
  [4'b0000, 4'b1111], maximum is 16 beats
- AWSIZE/ARSIZE range:

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[3'b000, 3'b100] for DATA_WIDTH=128
[2'b00, 2'b10] for DATA_WIDTH=64

- ARBURST/AWBURST:
  Only support FIXED, INC, not support WRAP
- AWID/WID/BID, ARID/RID width:
  4bits, indicating PCH id
- Only support OKAY, SLVERR, DECERR response type
- Only support little-endian format

10.5.2.3 M2M Transfer Type

SRC AXI Transfer Byte Num = (ARLEN+1)*2^ARSIZE Bytes
DST AXI Transfer Byte Num = (AWLEN+1)*2^AWSIZE Bytes

SRC/DST are memory, and the AXI transfer is the transmission unit.

About SRC/DST parameter configuration:

- BLOCK_TS, SRC/DST AXI transfer byte num don't have constraint relationship
- The last remaining data will use the largest possible burst length, and the unaligned part will be indicated by byte enable, and size remains unchanged:
  For example: block=70B, src_burst=20B, dst_burst=30B

About PCH release:

- M2M release hierarchy support block transfer level only;
- Release granularity is fixed as block.

10.5.2.4 M2P Transfer Type

SRC AXI Transfer Byte Num = (ARLEN+1)*2^ARSIZE Bytes
DST AXI Transfer Byte Num = (AWLEN+1)*2^AWSIZE Bytes
DST Burst Transaction Byte Num = (MSIZE) Bytes
DST Single Transaction Byte Num = (2^AWSIZE) Bytes

SRC is memory, with AXI transfer as the transmission unit.
DST is non memory, and takes transaction as the transmission unit. A transaction can be composed of one or more AXI transfers.

About SRC/DST parameter configuration:

- BLOCK_TS and MSIZE do not need to be integer multiples:

1) BLOCK_TS≥MSIZE: The non integral multiple part is transmitted by changing AXLEN/WSTRB (42h≥20h)
2) BLOCK_TS≤MSIZE: The non integral multiple part is transmitted by changing AXLEN/WSTRB (12h≤20h)

- MSIZE, DST AXI transfer byte num do not need to be integer multiples:

1) MSIZE≥DST AXI transfer byte num: The non integral multiple part is transmitted by changing AXLEN/WSTRB (42h≥20h)
2) MSIZE≤DST AXI transfer byte num: The non integral multiple part is transmitted by changing AXLEN/WSTRB (12h≤20h)

- DST and SRC transmission parameters have no constraint relationship;
- SRC uses AXI non-fix type to access memory, SAR and ARSIZE can be unaligned:

1) DMAC automatically calculates the current ARSIZE according to the current SAR internally to ensure address alignment
2) The ARSIZE configuration value determines the upper limit of the actual ARSIZE value

- DST uses AXI fix type to access peripherals, and needs to ensure the following alignment:

1) BLOCK_TS needs to be aligned with AWSIZE
2) MSIZE needs to be aligned with AWSIZE
3) DAR needs to be aligned with AWSIZE

About PCH release:

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- M2P release hierarchy support transaction level only:
  Release will be issued after each transaction transmission is completed
- The release granularity is fixed as transaction.

10.5.2.5 P2M Transfer Type

SRC AXI Transfer Byte Num = (ARLEN+1)*2^ARSIZE Bytes;
SRC Burst Transaction Byte Num = (MSIZE) Bytes;
SRC Single Transaction Byte Num = (2^ARSIZE) Bytes;
DST AXI Transfer Byte Num = (AWLEN+1)*2^AWSIZE Bytes;

SRC is non memory, and takes transaction as the transmission unit. A transaction can be composed of one or more AXI transfers.
DST is memory, with AXI transfer as the transmission unit.

About SRC/DST parameter configuration:

- BLOCK_TS and MSIZE do not need to be integer multiples:

1) BLOCK_TS≥MSIZE: The non integral multiple part is transmitted by changing AXLEN/WSTRB (42h≥20h)
2) BLOCK_TS≤MSIZE: The non integral multiple part is transmitted by changing AXLEN/WSTRB (12h≤20h)

- MSIZE, DST AXI transfer byte num do not need to be integer multiples:

1) MSIZE≥DST AXI transfer byte num: The non integral multiple part is transmitted by changing AXLEN/WSTRB (42h≥20h)
2) MSIZE≤DST AXI transfer byte num: The non integral multiple part is transmitted by changing AXLEN/WSTRB (12h≤20h)

- DST and SRC transmission parameters have no constraint relationship;
- SRC uses AXI fix type to access peripherals, and needs to ensure the following alignment:

1) BLOCK_TS needs to be aligned with ARSIZE
2) MSIZE needs to be aligned with ARSIZE
3) SAR needs to be aligned with ARSIZE

- DST uses AXI non-fix type to access memory, DAR and AWSIZE can be unaligned:

1) DMAC automatically calculates the current AWSIZE according to the current DAR internally to ensure address alignment
2) The AWSIZE configuration value determines the upper limit of the actual AWSIZE value

About PCH release:

- P2M release hierarchy support transaction level only:
  Release will be issued after each transaction transmission is completed
- The release granularity is fixed as transaction.

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Chapter 11 DMA2DDR_LITE

11.1 Overview

As an external memory, DDR plays an important role on SOC system. Testing DDR device, determine the DDR grain yield, to eliminate errors in data transmission is very important. Through this module mainly realize the DDR memory test, it still supports memory copy and eye diagram scanning function.

11.1.1 Features

The DMA2DDR_LITE supports the following features:

- Supports one AXI master and a 32bits APB slave interface
- The AXI master only supports 128 bits transmission width
- The AXI master only supports INCR16 transmission length
- Supports data transfer complete interrupt, data error interrupt and AXI bus error response interrupt
- Supports test data value configurable, the length of test data is 8 word
- Supports comparison data configuration, and comparison data location configurable
- Supports 2 transmission modes configurable: WW mode and RC mode
- Supports reporting error status after the interruption of data error such as error address, error data and error byte/word counter

11.2 Architecture

This section descripts the functions and behavior under various conditions.

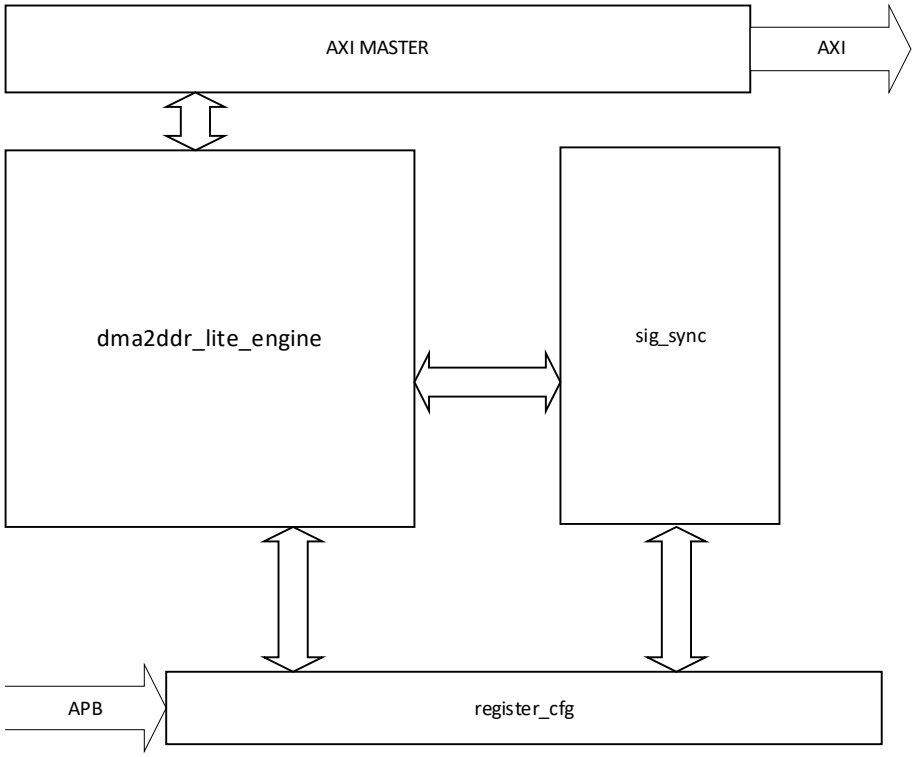

Fig. 11-1 DMA2DDR_LITE architecture

11.2.1 Block Diagram

The DMA2DDR_LITE comprises with:

- DMA2DDR_LITE register configuration block
- DMA2DDR_LITE engine block
- DMA2DDR_LITE sig_sync block
- DMA2DDR_LITE axi_master block

11.2.2 Block Descriptions

DMA2DDR_LITE register configuration block

DMA2DDR_LITE register configuration block is used to configure the parameters of dma2ddr_lite. This module includes all the registers which are necessary for dma2ddr_lite working.

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DMA2DDR_LITE engine block
DMA2DDR_lite engine block is the main block of DMA2DDR_LITE module. According to the configured message, this module makes the corresponding data processing which test needed, it has write, read and compare functions of data process.
DMA2DDR_LITE sig_sync block
The sig_sync block is used to handle the signals from different clock domains.
DMA2DDR_LITE axi_master block
The axi_master block is used to implement the functions of the AXI master and communicate with engine block.

11.3 Register description

11.3.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

11.3.2 Registers Summary

Name	Offset	Size	Reset Value	Description
DMA2DDR_LITE_TMODE	0x0000	W	0x00000000	Test Mode Register
DMA2DDR_LITE_TIADDR0	0x0004	W	0x00000000	Address Register 00
DMA2DDR_LITE_TIADDR1	0x0008	W	0x00000000	Address Register 01
DMA2DDR_LITE_TLENGTH0	0x000C	W	0x00000000	Length Register 0
DMA2DDR_LITE_TLENGTH1	0x0010	W	0x00000000	Length Register 1
DMA2DDR_LITE_EDFLAG	0x0018	W	0x00000000	Error Location Register
DMA2DDR_LITE_EADDR0	0x001C	W	0x00000000	Current Address Register 0
DMA2DDR_LITE_EADDR1	0x0020	W	0x00000000	Current Address Register 1
DMA2DDR_LITE_EDATA0	0x0030	W	0x00000000	Current Data Register 0
DMA2DDR_LITE_EDATA1	0x0034	W	0x00000000	Current Data Register 1
DMA2DDR_LITE_EDATA2	0x0038	W	0x00000000	Current Data Register 2
DMA2DDR_LITE_EDATA3	0x003C	W	0x00000000	Current Data Register 3
DMA2DDR_LITE_INTEN	0x0050	W	0x00000000	Interrupt Enable Register
DMA2DDR_LITE_INTST	0x0054	W	0x00000000	Interrupt Status Register
DMA2DDR_LITE_INTCL	0x0058	W	0x00000000	Interrupt Clear Register
DMA2DDR_LITE_TDATA00	0x0060	W	0x00000000	Input Data Register 00
DMA2DDR_LITE_TDATA01	0x0064	W	0x00000000	Input Data Register 01
DMA2DDR_LITE_TDATA02	0x0068	W	0x00000000	Input Data Register 02
DMA2DDR_LITE_TDATA03	0x006C	W	0x00000000	Input Data Register 03
DMA2DDR_LITE_TDATA10	0x0070	W	0x00000000	Input Data Register 10
DMA2DDR_LITE_TDATA11	0x0074	W	0x00000000	Input Data Register 11
DMA2DDR_LITE_TDATA12	0x0078	W	0x00000000	Input Data Register 12
DMA2DDR_LITE_TDATA13	0x007C	W	0x00000000	Input Data Register 13
DMA2DDR_LITE_TRCDATA00	0x00A0	W	0x00000000	Background Data Register 00
DMA2DDR_LITE_TRCDATA01	0x00A4	W	0x00000000	Background Data Register 01
DMA2DDR_LITE_TRCDATA02	0x00A8	W	0x00000000	Background Data Register 02
DMA2DDR_LITE_TRCDATA03	0x00AC	W	0x00000000	Background Data Register 03
DMA2DDR_LITE_TRCDATA10	0x00B0	W	0x00000000	Background Data Register 10
DMA2DDR_LITE_TRCDATA11	0x00B4	W	0x00000000	Background Data Register 11
DMA2DDR_LITE_TRCDATA12	0x00B8	W	0x00000000	Background Data Register 12
DMA2DDR_LITE_TRCDATA13	0x00BC	W	0x00000000	Background Data Register 13
DMA2DDR_LITE_TDMAST	0x00E0	W	0x00000000	Status Register
DMA2DDR_LITE_TEN	0x00E4	W	0x00000000	Enable Register
DMA2DDR_LITE_EDBCNT	0x00E8	W	0x00000000	Data Byte Counter Register
DMA2DDR_LITE_EDBFLAG	0x00EC	W	0x00000000	Data Flag Register 0
DMA2DDR_LITE_EWCNT	0x00F0	W	0x00000000	Data Word Counter Register
DMA2DDR_LITE_EDWFLAG	0x00F4	W	0x00000000	Data Flag Register 1

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Name	Offset	Size	Reset Value	Description
DMA2DDR_LITE_TRCDATA00M	0x0120	W	0x00000000	Background Data Location Register 00
DMA2DDR_LITE_TRCDATA01M	0x0124	W	0x00000000	Background Data Location Register 01
DMA2DDR_LITE_TRCDATA02M	0x0128	W	0x00000000	Background Data Location Register 02
DMA2DDR_LITE_TRCDATA03M	0x012C	W	0x00000000	Background Data Location Register 03
DMA2DDR_LITE_TRCDATA10M	0x0130	W	0x00000000	Background Data Location Register 10
DMA2DDR_LITE_TRCDATA11M	0x0134	W	0x00000000	Background Data Location Register 11
DMA2DDR_LITE_TRCDATA12M	0x0138	W	0x00000000	Background Data Location Register 12
DMA2DDR_LITE_TRCDATA13M	0x013C	W	0x00000000	Background Data Location Register 13
DMA2DDR_LITE_VER	0x0200	W	0x00000100	Version Register

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

11.3.3 Detail Registers Description

DMA2DDR_LITE_TMODE

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	tmode Test mode selection 1'b0: WW mode 1'b1: RC mode

DMA2DDR_LITE_TIADDR0

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	iaddr0 Initial address low 32 bits for DMA2DDR_LITE, this address is used for all the test modes.

DMA2DDR_LITE_TIADDR1

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	iaddr1 Initial address high 3 bits for DMA2DDR_LITE, this address is used for all the test modes.

DMA2DDR_LITE_TLENGTH0

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tlengh0 The low 32 bits of test length. The unit is word.

DMA2DDR_LITE_TLENGTH1

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	tlength1 The high 2 bits of test length. The unit is word.

DMA2DDR_LITE_EDFLAG

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	eflag Indicate error data location in the burst. 16'h1: Error in the first beat in this burst 16'h2: Error in the second beat in this burst 16'h4: Error in the third beat in this burst 16'h8: Error in the fourth beat in this burst 16'h10: Error in the fifth beat in this burst 16'h20: Error in the sixth beat in this burst 16'h40: Error in the seventh beat in this burst 16'h80: Error in the eighth beat in this burst 16'h100: Error in the ninth beat in this burst 16'h200: Error in the tenth beat in this burst 16'h400: Error in the eleventh beat in this burst 16'h800: Error in the twelfth beat in this burst 16'h1000: Error in the thirteenth beat in this burst 16'h2000: Error in the fourteenth beat in this burst 16'h4000: Error in the fifteenth beat in this burst 16'h8000: Error in the sixteenth beat in this burst

DMA2DDR_LITE_EADDR0

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	eaddr0 Current address[31:0] for the first data error detected.

DMA2DDR_LITE_EADDR1

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RO	0x0	eaddr1 Current address[34:32] for the first data error detected.

DMA2DDR_LITE_EDATA0

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	edata0 Detected error data[31:0]

DMA2DDR_LITE_EDATA1

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	edata1 Detected error data[63:32]

DMA2DDR_LITE_EDATA2

Address: Operational Base + offset (0x0038)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	edata2 Detected error data[95:64]

DMA2DDR_LITE_EDATA3

Address: Operational Base + offset (0x003C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	edata3 Detected error data[127:96]

DMA2DDR_LITE_INTEN

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	cpinten Completed interrupt enable. 1'b0: Disable the interrupt 1'b1: Enable the interrupt
1	RW	0x0	reinten Error response interrupt enable. 1'b0: Disable the interrupt 1'b1: Enable the interrupt
0	RW	0x0	deinten Data error interrupt enable. 1'b0: Disable the interrupt 1'b1: Enable the interrupt

DMA2DDR_LITE_INTST

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RO	0x0	cpintst Completed interrupt status. 1'b0: Interrupt is inactive. 1'b1: Interrupt is active.
1	RO	0x0	reintst Error response interrupt status. 1'b0: Interrupt is inactive. 1'b1: Interrupt is active.
0	RO	0x0	deintst Data error interrupt status. 1'b0: Interrupt is inactive. 1'b1: Interrupt is active.

DMA2DDR_LITE_INTCL

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	W1C	0x0	cpintcl Completed interrupt clear, write 1'b1 clear 1'b0.
1	W1C	0x0	reintcl Error response interrupt clear, write 1'b1 clear 1'b0.
0	W1C	0x0	deintcl Data error interrupt clear, write 1'b1 clear 1'b0.

DMA2DDR_LITE_TDATA00

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Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tdata00 Input data0 bits [31:0] for DMA2DDR_LITE test in WW modes.

DMA2DDR_LITE_TDATA01

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tdata01 Input data0 bits [63:32] for DMA2DDR_LITE test in WW modes.

DMA2DDR_LITE_TDATA02

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tdata02 Input data0 bits [95:64] for DMA2DDR_LITE test in WW modes.

DMA2DDR_LITE_TDATA03

Address: Operational Base + offset (0x006C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tdata03 Input data0 bits [127:96] for DMA2DDR_LITE test in WW modes.

DMA2DDR_LITE_TDATA10

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tdata10 Input data1 bits [31:0] for DMA2DDR_LITE test in WW modes.

DMA2DDR_LITE_TDATA11

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tdata11 Input data1 bits [63:32] for DMA2DDR_LITE test in WW modes.

DMA2DDR_LITE_TDATA12

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tdata12 Input data1 bits [95:64] for DMA2DDR_LITE test in WW modes.

DMA2DDR_LITE_TDATA13

Address: Operational Base + offset (0x007C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tdata13 Input data0 bits [127:96] for DMA2DDR_LITE test in WW modes.

DMA2DDR_LITE_TRCDATA00

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata00 Background data0 bits [31:0] for RC operation in RC modes.

DMA2DDR_LITE_TRCDATA01

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Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata01 Background data0 bits [63:32] for RC operation in RC modes.

DMA2DDR_LITE_TRCDATA02

Address: Operational Base + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata02 Background data0 bits [95:64] for RC operation in RC modes.

DMA2DDR_LITE_TRCDATA03

Address: Operational Base + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata03 Background data0 bits [127:96] for RC operation in RC modes.

DMA2DDR_LITE_TRCDATA10

Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata10 Background data1 bits [31:0] for RC operation in RC modes.

DMA2DDR_LITE_TRCDATA11

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata11 Background data1 bits [63:32] for RC operation in RC modes.

DMA2DDR_LITE_TRCDATA12

Address: Operational Base + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata12 Background data1 bits [95:64] for RC operation in RC modes.

DMA2DDR_LITE_TRCDATA13

Address: Operational Base + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata13 Background data0 bits [127:96] for RC operation in RC modes.

DMA2DDR_LITE_TDMAST

Address: Operational Base + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	workst DMA2DDR_LITE current work status. 1'b0: DMA2DDR_LITE is idle. 1'b1: DMA2DDR_LITE is busy.

DMA2DDR_LITE_TEN

Address: Operational Base + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
0	R/WSC	0x0	ten DMA2DDR_LITE work enable bit. This bit should be configurable at last. It means all the registers should be configured before this bit is set. 1'b0: Disable 1'b1: Enable

DMA2DDR_LITE_EDBCNT

Address: Operational Base + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ebcnt Indicated error data byte cnt in the whole transmission.

DMA2DDR_LITE_EDBFLAG

Address: Operational Base + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	ebfalg Indicates data flag which right or wrong in byte unit in the whole transmission. 1'b1: Data is wrong in this byte. 1'b0: Data is right in this byte.

DMA2DDR_LITE_EWCNT

Address: Operational Base + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ewcnt Indicated error data word cnt in the whole transmission.

DMA2DDR_LITE_EDWFLAG

Address: Operational Base + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RO	0x0	ewflag Indicates data flag which right or wrong in word unit in the whole transmission. 1'b1: Data is wrong in this word. 1'b0: Data is right in this word.

DMA2DDR_LITE_TRCDATA00M

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata00m Background data0 rc location enable bits [31:0] for RC operation in RC modes.

DMA2DDR_LITE_TRCDATA01M

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata01m Background data0 rc location enable bits [63:32] for RC operation in RC modes.

DMA2DDR_LITE_TRCDATA02M

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata02m Background data0 rc location enable bits [95:64] for RC operation in RC modes.

DMA2DDR_LITE_TRCDATA03M

Address: Operational Base + offset (0x012C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata03m Background data0 rc location enable bits [127:96] for RC operation in RC modes.

DMA2DDR_LITE_TRCDATA10M

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata10m Background data1 rc location enable bits [31:0] for RC operation in RC modes.

DMA2DDR_LITE_TRCDATA11M

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata11m Background data1 rc location enable bits [63:32] for RC operation in RC modes.

DMA2DDR_LITE_TRCDATA12M

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata12m Background data1 rc location enable bits [95:64] for RC operation in RC modes.

DMA2DDR_LITE_TRCDATA13M

Address: Operational Base + offset (0x013C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trcdata13m Background data1 rc location enable bits [127:96] for RC operation in RC modes.

DMA2DDR_LITE_VER

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000100	version Version of DMA2DDR_LITE

11.4 Application Notes

Register configuration should follow:

(1) DMA2DDR_TEN should be configured in the end.

(2) When you use different test modes, the need for a particular configuration register is important, especially DMA2DDR_TCTL register. Inappropriate configuration will lead to the transmission error, you can reference DMA2DDR instruction when using it in different test mode.

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Chapter 12 DCF

12.1 Overview

DCF is used to implement register automatic configuration without the participation of CPU. DCF is connected to SOC through an AXI Master and an APB Slave, with a DMAC and instruction buffer inside. Beforehand, software puts into SRAM formulary pieces of instructions which consist of all the register-related configurations in the process of frequency conversion. When started-up, DCF automatically reads instructions to the inside buffer by means of DMA, and implement register configuration after analysis. A done signal will be provided for CPU after all the instructions are analyzed.

DCF supports the following features:

- AMBA 32-bit AXI compliant
- Support DMA operation from SRAM to buffer
  - Support burst8 only
  - LLP not supported
- Support 2 internal instruction registers : r0 & r1
- Support following software instructions:
  - IDL (delay)
  - LDR (read register)
  - STR (write register)
  - ISB (write with flush)
  - Bitwise AND
  - Bitwise OR
  - Bitwise INV
  - LSR (left shift)
  - RSR (right shift)
  - ADD
  - SUB
  - POLLEQ (poll a register until the value match)
  - POLLNEQ (poll a register until the value mismatch)
  - CMPEQ (compare if equal)
  - CMPNEQ (compare if unequal)
  - BL (jump upwards or downwards, 8bytes align)
- Support following program functions through combination of basic instructions
  - If-else
  - while
  - loop
  - for

12.2 Block Diagram

DCF comprises with:

- An AXI Master Interface
- An APB Slave Interface
- A DMA controller
- An Instruction Buffer
- Instruction analyzer

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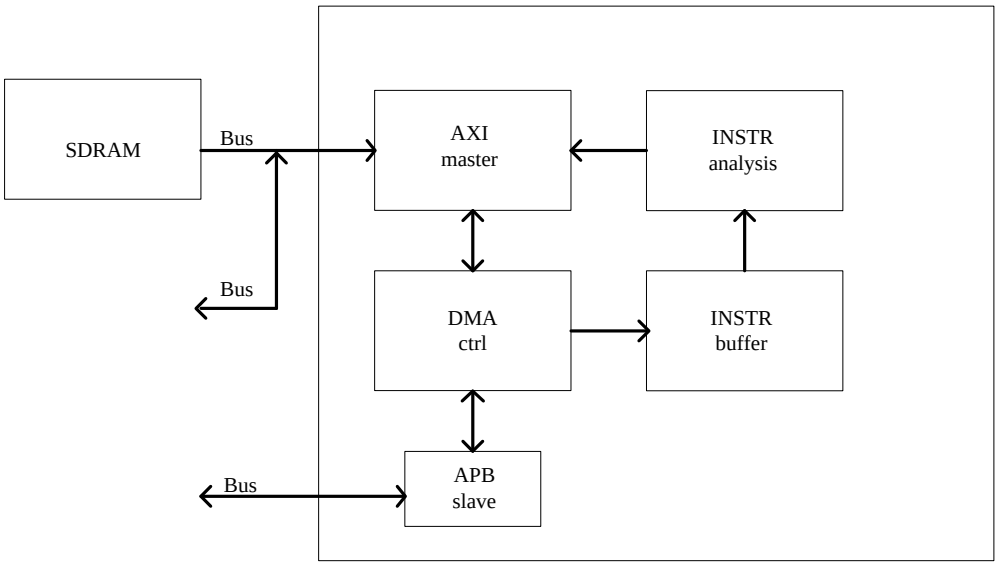

Fig.12-1DCF Block Diagram

12.3 Register Description

12.3.1 Registers Summary

Name	Offset	Size	Reset Value	Description
DCF_CTRL	0x0000	W	0x00000000	DCF Control Register
DCF_STATUS	0x0004	W	0x00000001	DCF Internal Status Register
DCF_ADDR	0x0008	W	0x00000000	DCF Instruction Start Address Register
DCF_ISR	0x000C	W	0x00000000	DCF Interrupt Status Register
DCF_TIMEOUT_CYC	0x0014	W	0xFFFFFFFF	DCF Instruction Timeout Cycle Register
DCF_CURR_R0	0x0020	W	0x00000000	Current Internal R0 Value Register
DCF_CURR_R1	0x0024	W	0x00000000	Current Internal R1 Value Register
DCF_CMD_COUNTER	0x0028	W	0x00000000	Current Command Counter Value Register
DCF_LAST_ADDR1	0x0030	W	0x00000000	Last 1 Instruction Address Register
DCF_LAST_ADDR2	0x0034	W	0x00000000	Last 2 Instruction Address Register
DCF_LAST_ADDR3	0x0038	W	0x00000000	Last 3 Instruction Address Register
DCF_LAST_ADDR4	0x003C	W	0x00000000	Last 4 Instruction Address Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

12.3.2 Detail Registers Description

DCF_CTRL

Address: Operational Base(0x20B70000) + offset (0x0000)

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Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	R/WSC	0x0	timeout_en 1'b1: Enable 1'b0: Disable
0	R/WSC	0x0	start This bit will be auto cleared when DCF is done. 1'b1: Start DCF 1'b0: Stop DCF

DCF_STATUS

Address: Operational Base(0x20B70000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	W1C	0x0	dma_done_st 1'b1: DCF has fetched all the instructions.
6	W1C	0x0	instr_done_st 1'b1: DCF has done all the instructions analysis.
5	W1C	0x0	dma_error_st 1'b1 : Error response received when DCF is fetching instructions.
4	W1C	0x0	instr_error_st 1'b1 : Error response received when DCF is handling instructions.
3	W1C	0x0	dcf_timeout_st 1'b1: DCF timeout
2:1	RO	0x0	reserved
0	RO	0x1	dcf_idle_st 1'b1 : DCF is idle 1'b0 : DCF is busy

DCF_ADDR

Address: Operational Base(0x20B70000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	addr DCF instruction fetch start address

DCF_ISR

Address: Operational Base(0x20B70000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	W1C	0x0	dcf_error 1'b1: Error response or timeout during DDR change frequency.

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Bit	Attr	Reset Value	Description
0	W1C	0x0	dcf_done 1'b1: DDR change frequency completed. 1'b0: DDR change frequency not completed.

DCF_TIMEOUT_CYC

Address: Operational Base(0x20B70000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0xffffffff	timeout Calculated by aclk

DCF_CURR_R0

Address: Operational Base(0x20B70000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	curr_r0 R0 value is sampled when dcf_done or dcf_error occurs.

DCF_CURR_R1

Address: Operational Base(0x20B70000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	curr_r1 R1 value is sampled when dcf_done or dcf_error occurs.

DCF_CMD_COUNTER

Address: Operational Base(0x20B70000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	cmd_counter cmd_counter value is sampled when dcf_done or dcf_error occurs. it records the number of pieces of instructions among DCF.

DCF_LAST_ADDR1

Address: Operational Base(0x20B70000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	last_addr1 Value is sampled when dcf_done or dcf_error occurs. it records the last 1 instruction address.

DCF_LAST_ADDR2

Address: Operational Base(0x20B70000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	last_addr2 Value is sampled when dcf_done or dcf_error occurs. it records the last 2 instruction address.

DCF_LAST_ADDR3

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Address: Operational Base(0x20B70000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	last_addr3 Value is sampled when dcf_done or dcf_error occurs. it records the last 3 instruction address.

DCF_LAST_ADDR4

Address: Operational Base(0x20B70000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	last_addr4 Value is sampled when dcf_done or dcf_error occurs. it records the last 4 instruction address.

12.4 Application Notes

12.4.1 DCF Work Flow

1. Software needs to open up a separate space in SRAM and loads a series of instructions in advance.
2. Software configure DCF, notifying the start_addr, and then start DCF.
3. DCF will transfer instruction data through DMA from SRAM to an internal buffer.
4. In the meanwhile, An instruction analysis module will read these instructions from buffer, and transform them to corresponding bus-relative operations, including Write & Read registers, delay some clock cycles, arithmetic operation and so on.
5. DCF will recognize the last command, and generate a dcf_done interrupt for CPU.

12.4.2 Instruction Format

One piece of instruction, which is 64bit, should consist of the information of:

63:59	58	57:34	33:32	31:0
cmd[4:0]	dst flag	addr[25:2]	(r1,r0)	data

The overall principle of instruction information is:

- address[31:27] is reserved for 5bit command, which represents the corresponding operation.
- address[1:0] is used to indicate operation of r0 or r1.
- address[25:2] is the real bus address. If 0, it means no bus operation; if not 0, it means a combination of 2 instructions with a bus operation ahead and an arithmetic c operation followed in order to improve efficiency.

The following table lists all the supported command

INSTR	cmd[4:0]	addr[25:2]	R1	R0	Data[31:0]	
IDLE	5'h00	NA	NA	NA	#data	IDL #data
AND	5'h01	#addr	0	0	NA	ldr #addr r0 ; ldr #addr r1
			0	1	#data	ldr #addr r0 ; AND r0 #data
			1	0	#data	ldr #addr r1 ; AND r1 #data
			1	1	NA	ldr #addr r1 ; AND r1 r0
		All 0	0	0	NA	mov r0 r0 ; mov r1 r1
			0	1	#data	AND r0 #data

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INSTR	cmd[4:0]	addr[25:2]	R1	R0	Data[31:0]	
			1	0	#data	AND r1 #data
			1	1	NA	AND r1 r0
OR	5'h02	#addr	0	0	NA	ldr #addr r0 ; ldr #addr r1
			0	1	#data	ldr #addr r0 ; OR r0 #data
			1	0	#data	ldr #addr r1 ; OR r1 #data
			1	1	NA	ldr #addr r1 ; OR r1 r0
		All 0	0	0	NA	mov r0 r0 ; mov r1 r1
			0	1	#data	OR r0 #data
			1	0	#data	OR r1 #data
			1	1	NA	OR r1 r0
INV	5'h03	#addr	0	0	NA	ldr #addr r0 ; ldr #addr r1
			0	1	#data	ldr #addr r0 ; XOR r0 ^#data
			1	0	#data	ldr #addr r1 ; XOR r1 ^#data
			1	1	#data	ldr #addr r1 ; XOR r1 ^r0
		All 0	0	0	NA	mov r0 r0 ; mov r1 r1
			0	1	NA	INV r0
			1	0	NA	INV R1
			1	1	NA	SWP r0 r1
LSR	5'h04	#addr	0	0	NA	ldr #addr r0 ; ldr #addr r1
			0	1	#data	ldr #addr r0 ; LSR r0 #data
			1	0	#data	ldr #addr r1 ; LSR r1 #data
			1	1	NA	ldr #addr r1 ; LSR r1 r0
		All 0	0	0	NA	mov r0 r0 ; mov r1 r1
			0	1	#data	LSR r0 #data
			1	0	#data	LSR r1 #data
			1	1	NA	LSR r1 r0
RSR	5'h05	#addr	0	0	NA	ldr #addr r0 ; ldr #addr r1
			0	1	#data	ldr #addr r0 ; RSR r0 #data
			1	0	#data	ldr #addr r1 ; RSR r1 #data
			1	1	NA	ldr #addr r1 ; RSR r1 r0
		All 0	0	0	NA	mov r0 r0 ; mov r1 r1
			0	1	#data	RSR r0 #data
			1	0	#data	RSR r1 #data
			1	1	NA	RSR r1 r0
CMPEQ	5'h06	#addr	0	0	NA	ldr #addr r0 ; ldr #addr r1
			0	1	#data	ldr #addr r0 ; CMPEQ r0 #data,flag
			1	0	#data	ldr #addr r0 ; CMPEQ r1 #data,flag
			1	1	NA	ldr #addr r0 ; CMPEQ r1 r0,flag
		All 0	0	0	NA	mov r0 r0 ; mov r1 r1
			0	1	#data	CMPEQ r0 #data, flag
			1	0	#data	CMPEQ r1 #data, flag

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INSTR	cmd[4:0]	addr[25:2]	R1	R0	Data[31:0]	
			1	1	NA	CMPEQ r1 r0, flag
CMPNE	5'h07	#addr	0	0	NA	ldr #addr r0 ; ldr #addr r1
			0	1	#data	ldr #addr r0 ; CMPNE r0 #data,flag
			1	0	#data	ldr #addr r1 ; CMPNE r1 #data,flag
			1	1	NA	ldr #addr r1 ; CMPNE r1 r0,flag
		All 0	0	0	NA	mov r0 r0 ; mov r1 r1
			0	1	#data	CMPNE r0 #data, flag
			1	0	#data	CMPNE r1 #data, flag
			1	1	NA	CMPNE r1 r0, flag
ADD	5'h08	#addr	0	0	NA	ldr #addr r0 ; ldr #addr r1
			0	1	#data	ldr #addr r0 ; ADD r0 #data
			1	0	#data	ldr #addr r0 ; ADD r1 #data
			1	1	NA	ldr #addr r0 ; ADD r1 r0
		All 0	0	0	NA	mov r0 r0 ; mov r1 r1
			0	1	#data	ADD r0 #data
			1	0	#data	ADD r1 #data
			1	1	NA	ADD r1 r0
SUB	5'h09	#addr	0	0	NA	ldr #addr r0 ; ldr #addr r1
			0	1	#data	ldr #addr r0 ; SUB r0 #data
			1	0	#data	ldr #addr r0 ; SUB r1 #data
			1	1	NA	ldr #addr r0 ; SUB r1 r0
		All 0	0	0	NA	mov r0 r0 ; mov r1 r1
			0	1	#data	SUB r0 #data
			1	0	#data	SUB r1 #data
			1	1	NA	SUB r1 r0
STR	5'h0a	#addr	0	0	#data	STR #addr #data
			0	1	NA	STR #ADDR r0
			1	0	NA	STR #ADDR r1
			1	1	#data	STR #addr #data
ISB	5'h0b	#addr	0	0	#data	STR #addr #data
			0	1	NA	STR #ADDR r0
			1	0	NA	STR #ADDR r1
			1	1	#data	STR #addr #data
POLEQ	5'h0c	NA	0	1	#data	poll r0=#data,repeat last command
			1	0	#data	poll r1=#data,repeat last command
			1	1	NA	poll r1=r0,repeat last command
POLNEQ	5'h0d	NA	0	1	#data	poll r0!=#data,repeat last command

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INSTR	cmd[4:0]	addr[25:2]	R1	R0	Data[31:0]	
			1	0	#data	poll r1!=#data,repeat last command
			1	1	NA	poll r1!=r0,repeat last command
BL_U	5'h0e	ALL 0	NA	NA	#data	brr #data,?flag (upwards)
			0	1	NA	brr r0, ?flag
			1	0	NA	brr r1, ?flag
		ALL 1	NA	NA	#data	brr #data (upwards)
			0	1	NA	brr r0
			1	0	NA	brr r1
BL_D	5'h0f	ALL 0	NA	NA	#data	brr #data,?flag (downwards)
			0	1	NA	brr r0, ?flag
			1	0	NA	brr r1, ?flag
		ALL 1	NA	NA	#data	brr #data (downwards)
			0	1	NA	brr r0
			1	0	NA	brr r1
DMA_S	5'h10	NA	NA	NA	#data	set dma_start_addr = #data
DMA_D	5'h11	NA	NA	NA	#data	set dma_end_addr = #data
DMA_DO	5'h12	NA	NA	NA	#data	set dma_length = #data (byte) dma_start
END	5'h13	NA	NA	NA	NA	End of instruction

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Chapter 13 Generic Interrupt Controller (GIC)

13.1 Overview

There is a generic interrupt controller (GIC400) in RV1126B which generates physical interrupts to Cortex-A53. It has two interfaces, the distributor interface connects to the interrupt source, and the CPU interface connects to Cortex-A53. The details of CPU interface connectivity are shown in the following table.

Table 13-1 CPU Interface Connectivity

CPU Interface Number	Connectivity
CPU interface 0	CPU0
CPU interface 1	CPU1
CPU interface 2	CPU2
CPU interface 3	CPU3

It supports the following features:

- Support 256 hardware interrupt inputs
- Support masking of any interrupts
- Support interrupts prioritization
- Support distribution of the interrupts to the target Cortex-A53 processor(s)
- Support generation of interrupts by software
- Support security extensions
- Support virtual extension

13.2 Block Diagram

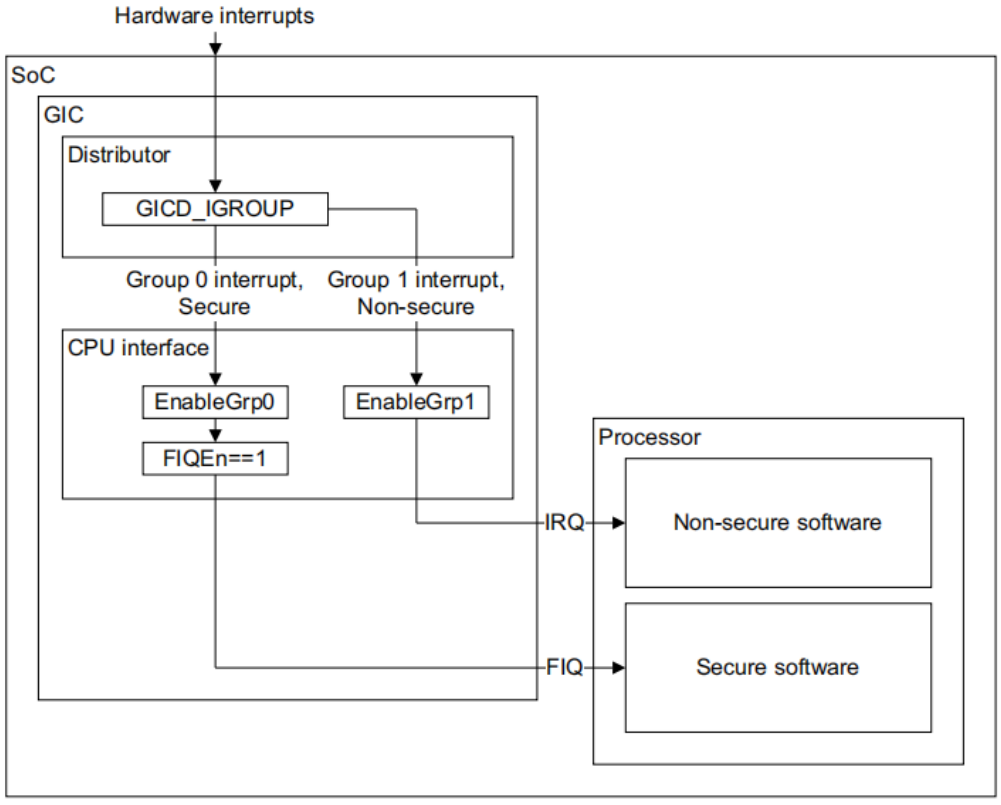

Fig. 13-1 GIC Block Diagram

13.3 Function Description

Please refer to the document IHI0048B_gic_architecture_specification.pdf and GIC400_Technical_Reference_Manual.pdf for the detail function description.

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Chapter 14 TIMER

14.1 Overview

TIMER is a programmable timer peripheral. It is usually used for generating a timing interrupt. There are two types of TIMER which are different in channel number. Both of them can be configured as a count-up or count-down timer.

TIMER supports the following features:

- Support two timer mode: free-running and user-defined
- Support two count mode: count-up and count-down
- Support configuration of loading count value
- Support configuration of initial count value
- Support mask interrupt

14.2 Block Diagram

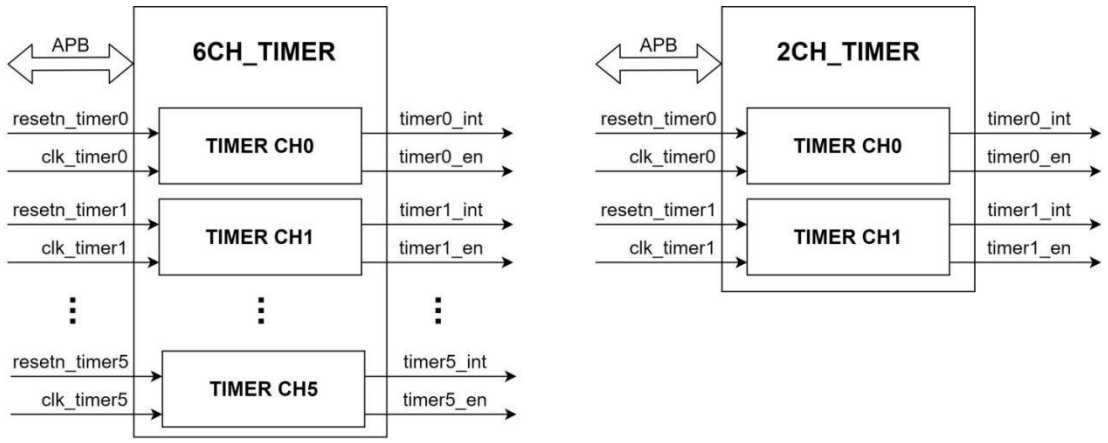

Fig. 14-1 TIMER Block Diagram

The figure above shows the block diagram of TIMER.

14.3 Function Description

14.3.1 TIMER Clock

The frequency of counting clock can be chosen from 24MHz and 100MHz clock.

14.3.2 TIMER Mode

- **User-defined Count Mode**

TIMER loads TIMER_TIMERn_LOAD_COUNT1 and TIMER_TIMERn_ LOAD_ COUNT0 registers (for count-down TIMER) or TIMER_TIMERn_INIT_COUNT1 and TIMER_ TIMERn_INIT_COUNT0 registers (for count-up TIMER) as initial value. When the TIMER counts down to 0 (for count-down TIMER) or counts up to the value in TIMER_TIMERn _LOAD_COUNT1 and TIMER_TIMERn_LOAD_COUNT0 (for count-up TIMER), it will not automatically reload the count value register. User need to disable timer firstly and follow the programming sequence to make timer work again.

- **Free-running Count Mode**

TIMER loads the TIMER_TIMERn_LOAD_COUNT1 and TIMER_ TIMERn_LOAD_COUNT0 (for count-down TIMER) or TIMER_TIMERn_INIT_COUNT1 and TIMER_ TIMERn_INIT_COUNT0 (for count-up TIMER) register as initial value. TIMER will automatically reload the count value register, when timer counts down to 0 (for count-down TIMER) or counts up to the value in TIMER_TIMERn_LOAD_ COUNT1 and TIMER_TIMERn_LOAD_COUNT0 (for count-up TIMER).

14.4 Register Description

14.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

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Operational Base

Name	Base Address
TIMER_6CH-CH0	0x20C00000
TIMER_6CH-CH1	0x20C10000
TIMER_6CH-CH2	0x20C20000
TIMER_6CH-CH3	0x20C30000
TIMER_6CH-CH4	0x20C40000
TIMER_6CH-CH5	0x20C50000

Operational Base

Name	Base Address
TIMER_2CH-CH0	0x20A00000
TIMER_2CH-CH1	0x20A10000

14.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
TIMER_TIMERn_LOAD_COUNT0	0x0000	W	0x00000000	Low 32 bits value to be loaded into Timer0
TIMER_TIMERn_LOAD_COUNT1	0x0004	W	0x00000000	High 32 bits value to be loaded into Timer0
TIMER_TIMERn_CURR_VALUE0	0x0008	W	0x00000000	Low 32 bits of current value of Timer0
TIMER_TIMERn_CURR_VALUE1	0x000C	W	0x00000000	High 32 bits of current value of Timer0
TIMER_TIMERn_CONTROL	0x0010	W	0x00000000	Timer Control Register
TIMER_TIMERn_INTSTATUS	0x0018	W	0x00000000	Timer Interrupt Status Register
TIMER_TIMERn_REVISION	0x001C	W	0x3AEE0000	Timer Version Register
TIMER_TIMERn_INIT_COUNT0	0x0020	W	0x00000000	Low 32 bits value to be initial into Timer0
TIMER_TIMERn_INIT_COUNT1	0x0024	W	0x00000000	High 32 bits value to be initial into Timer0

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

14.4.3 Detail Registers Description

TIMER_TIMERn_LOAD_COUNT0

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	count0 Load count low bits

TIMER_TIMERn_LOAD_COUNT1

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	count1 Load count high bits

TIMER_TIMERn_CURR_VALUE0

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	current_value0 Current_cnt_low bits

TIMER_TIMERn_CURR_VALUE1

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Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	current_value1 Current_cnt_high bits

TIMER_TIMERn_CONTROL

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	count_mode Count mode 1'b0: Count up counter 1'b1: Count down counter
2	RW	0x0	int_en Timer interrupt enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	timer_mode Timer mode 1'b0: Free-running mode 1'b1: User-defined count mode
0	RW	0x0	timer_en Timer enable 1'b0: Disable 1'b1: Enable

TIMER_TIMERn_INTSTATUS

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	int_pd This register contains the interrupt status for Timer. Write 1 to this register will clear the interrupt.

TIMER_TIMERn_REVISION

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RO	0x3aee	svn_revision SVN revision.
15:9	RO	0x00	reserved
8	RO	0x0	ch_type Indicate the timer count mode 1'b0: Count up counter 1'b1: Count down counter
7:0	RO	0x00	reserved

TIMER_TIMERn_INIT_COUNT0

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	count0 Iintial count low bits

TIMER_TIMERn_INIT_COUNT1

Address: **Operational Base** + offset (0x0024)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	count1 Initial count high bits

14.5 Application Notes

14.5.1 Clock and Reset

There are two different clock domain in TIMER: clk_timern and pclk. The frequency of these clocks are as below:

Table 14-1 Clock Source and Frequency

Module	Clock Name	Clock Source	Frequency
RKTIMER_6CH	pclk	clk_matrix_100m	100M
	clk_timern(n=0-5)	clk_matrix_100m /xin_osc0	100M/24M
RKTIMER_2CH	pclk	clk_matrix_100m	100M
	clk_timern(n=0-1)	clk_matrix_100m /xin_osc0	100M/24M

When user disables the timer enables bit (bit 0 of TIMER_TIMERn_CONTROL), the timer_en output signal is de-asserted, and timer_clk will stop. When user enables the timer, the timer_en signal is asserted and timer_clk will start running.
The application is only allowed to re-configure registers when timer_en is low.

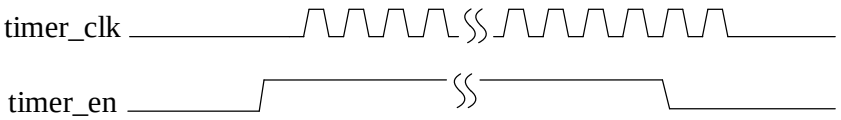

Fig. 14-2 Timing between timer_en and timer_clk

14.5.2 Programming Flow

- Initialize the TIMER by the TIMER_TIMERn_CONTROL register:
  - Disable the timer by writing a "0" to the timer enable bit (bit 0). Accordingly, the timer_en output signal is de-asserted.
  - Program the timer mode—free-running or user-defined—by writing a "0" or "1" respectively, to the timer mode bit (bit 1).
  - Program the counting mode—count-up or count-down—by writing a "0" or "1" respectively to the count mode bit (bit 3).
  - Set the interrupt mask as either masked or not masked by writing a "0" or "1" respectively, to the timer interrupt mask bit (bit 2).
- Initial the timer count value into the TIMER_TIMERn_INIT_COUNT1 and TIMER_TIMERn_INIT_COUNT0 register.
- Load the timer count value into the TIMER_TIMERn_LOAD_COUNT1 and TIMER_TIMERn_LOAD_COUNT0 register.
- Enable the TIMER by writing a "1" to bit 0 of TIMER_TIMERn_CONTROL.

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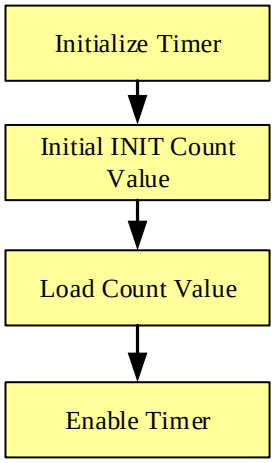

Fig. 14-3 Timer Usage Flow

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Chapter 15 Watchdog Timer (WDT)

15.1 Overview

Watchdog Timer (WDT) is an APB slave peripheral that can be used to prevent system lockup that caused by conflicting parts or programs in a SOC. The WDT would generate interrupt or reset signal when its counter reaches zero, then a reset controller would reset the system.

WDT supports the following features:

- 32 bits APB bus width
- WDT counter's clock can be chosen from 24MHz and 100MHz clock
- 32 bits WDT counter width
- Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
- WDT can perform two types of operations when timeout occurs:
  - Generate a system reset
  - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
- Programmable reset pulse length
- Total 16 defined ranges of main timeout period
- There are 4 WDTs: WDT_LP, WDT_HP, WDT_S, WDT_NS
- WDT_S, WDT_NS can drive CRU to generate global software reset, and WDT_HP can generate HPMCU reset, correspondingly, WDT_LP can reset PMU_MCU

15.2 Block Diagram

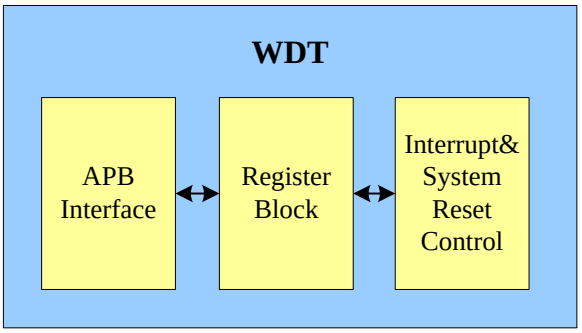

Fig. 15-1 WDT Block Diagram

WDT comprises with:

- APB Interface

The APB Interface implements the APB slave operation. Its data bus width is 32 bits.

- Register Block

A register block that read coherence for the current count register.

- Interrupt & System Reset Control

An interrupt/system reset generation block is comprised of a decrementing counter and control logic.

15.3 Function Description

15.3.1 Operation

Counter

The WDT counts from a preset (timeout) value in descending order to zero. When the counter reaches zero, depending on the output response mode selected, either a system reset or an interrupt occurs. When the counter reaches zero, it wraps to the selected timeout value and continues decrementing. The user can restart the counter to its initial value. This is programmed by writing to the restart register at any time. The process of restarting the watchdog counter is sometimes referred as kicking the dog. As a safety feature to prevent accidental restarts, the value 0x76 must be written to the Current Counter Value Register (WDT_CRR).

Interrupts

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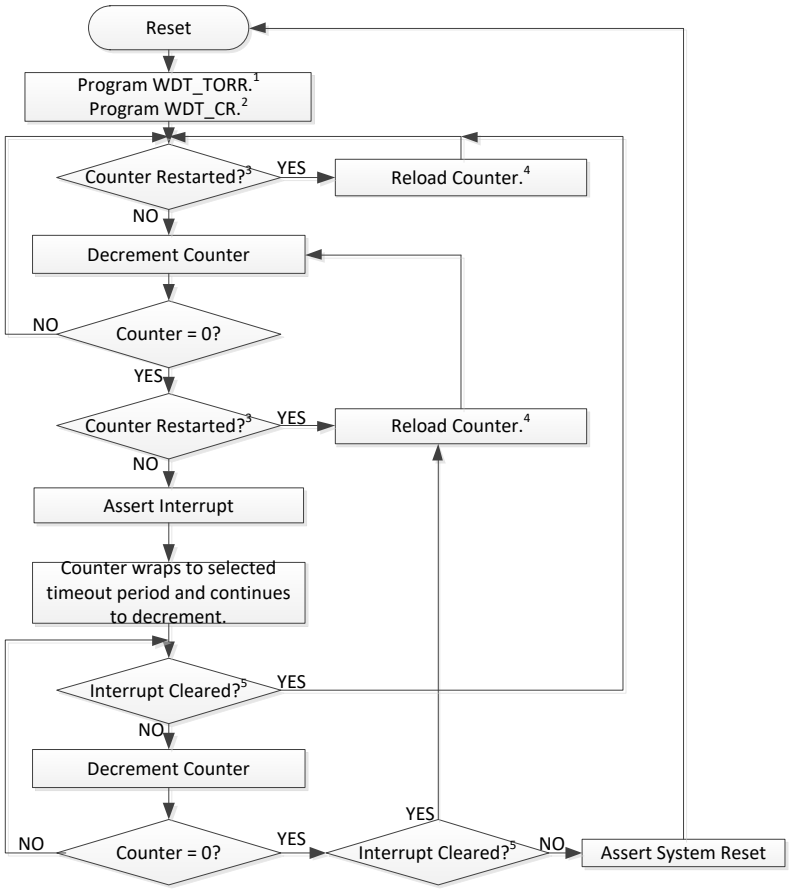
The WDT can be programmed to generate an interrupt (and then a system reset) when a timeout occurs. When a 1 is written to the response mode field (RMOD, bit 1) of the Watchdog Timer Control Register (WDT_CR), the WDT generates an interrupt. If it is not cleared by the time a second timeout occurs, then it generates a system reset. If a restart occurs at the same time the watchdog counter reaches zero, an interrupt is not generated.

System Resets
When a 0 is written to the output response mode field (RMOD, bit 1) of the Watchdog Timer Control Register (WDT_CR), the WDT generates a system reset when a timeout occurs.

Reset Pulse Length
The reset pulse length is the number of pclk cycles for which a system reset is asserted. When a system reset is generated, it remains asserted for the number of cycles specified by the reset pulse length or until the system is reset. A counter restart has no effect on the system reset once it has been asserted.

15.3.2 Programming Sequence



1. Select required timeout period.
2. Set reset pulse length, response mode, and enable WDT.
3. Write 0x76 to WDT_CRR.
4. Starts back to selected timeout period.
5. Can clear by reading WDT_EOI or restarting (kicking) the counter by writing 0x76 to WDT_CRR.

Fig. 15-2 WDT Operation Flow (RMOD=1)

15.4 Register Description

15.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
WDT_LP	0x20850000

Name	Base Address
WDT_S	0x20B00000
WDT_HP	0x20B50000
WDT_NS	0x20B60000

15.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
WDT_CR	0x0000	W	0x00000008	Control Register
WDT_TORR	0x0004	W	0x00000000	Timeout Range Register
WDT_CCVR	0x0008	W	0x0000FFFF	Current Counter Value Register
WDT_CRR	0x000C	W	0x00000000	Counter Restart Register
WDT_STAT	0x0010	W	0x00000000	Interrupt Status Register
WDT_EOI	0x0014	W	0x00000000	Interrupt Clear Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

15.4.3 Detail Registers Description

WDT_CR

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:2	RW	0x2	rst_pluse_length This is used to select the number of pclk cycles for which the system reset stays asserted. 3'b000: 2 pclk cycles 3'b001: 4 pclk cycles 3'b010: 8 pclk cycles 3'b011: 16 pclk cycles 3'b100: 32 pclk cycles 3'b101: 64 pclk cycles 3'b110: 128 pclk cycles 3'b111: 256 pclk cycles
1	RW	0x0	resp_mode Selects the output response generated to a timeout. 1'b0: Generate a system reset 1'b1: First generate an interrupt and if it is not cleared by the time a second timeout occurs then generate a system reset
0	RW	0x0	en This bit is used to enable and disable the WDT. When disabled, the counter dose not decrement .Thus, no interrupt or system reset are generated. Once this bit has been enabled, it can be cleared only by a system reset. 1'b0: WDT disabled 1'b1: WDT enabled

WDT_TORR

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	timeout_period This field is used to select the timeout period from which the watchdog counter restarts. A change of the timeout period takes effect only after the next counter restart (kick). The range of values available for a 32-bit watchdog counter are: 4'b0000: 0x0000ffff 4'b0001: 0x0001ffff 4'b0010: 0x0003ffff 4'b0011: 0x0007ffff 4'b0100: 0x000fffff 4'b0101: 0x001fffff 4'b0110: 0x003fffff 4'b0111: 0x007fffff 4'b1000: 0x00ffffff 4'b1001: 0x01ffffff 4'b1010: 0x03ffffff 4'b1011: 0x07ffffff 4'b1100: 0x0fffffff 4'b1101: 0x1fffffff 4'b1110: 0x3fffffff 4'b1111: 0x7fffffff

WDT_CCVR

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RO	0x0000ffff	cur_cnt This register, when read, is the current value of the internal counter. This value is read coherently whenever it is read.

WDT_CRR

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	WO	0x00	cnt_restart This register is used to restart the WDT counter. As a safety feature to prevent accidental restarts, the value 0x76 must be written. A restart also clears the WDT interrupt. Reading this register returns zero.

WDT_STAT

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	status This register shows the interrupt status of the WDT. 1'b1: Interrupt is active regardless of polarity 1'b0: Interrupt is inactive

WDT_EOI

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	int_clr This can be used to clear the interrupt without restarting the watchdog counter.

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Chapter 16 HPTIMER

16.1 Overview

HPTIMER is a programmable timer peripheral, which has special calibration function. This component is an APB slave device, and can provide count value for CPU directly.

HPTIMER supports the following features:

- Support three timer mode: normal mode, hardware adjust mode and software adjust mode
- Support two counting mode at normal mode: free-running and user-defined
- Support configuration of loading count value at normal mode
- Support low-speed counter configurate of initial count value
- Support several mask interrupts at different timer mode
- Support calibrate back to exact count value without software calculation in Hardware adjust mode
- Support calibrate back to exact count value with software-aided calculation in Software adjust mode
- Support common multiple configuration of slow and fast clock period
- Support providing count value for CPU use

16.2 Block Diagram

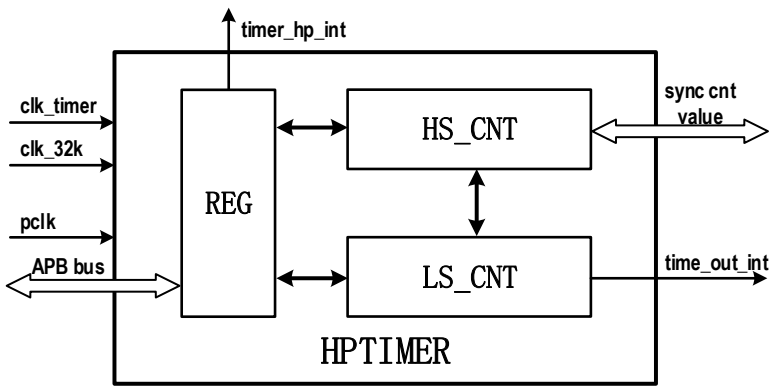

Fig. 16-1 HPTIMER Block Diagram

The figure above shows the block diagram of HPTIMER.

Register Block(REG)

This block contains several registers which are used for timer configuration, status checking and interrupt generation.

High-Speed Counter(HS_CNT)

This block contains two main counters which are working at high speed clock rate, one is used for record the current counter value that can update to CPU, the other is used to generate timing interrupt.

Low-Speed Counter(LS_CNT)

This block also contains two main counters, the different is that these counters are working at low speed clock rate, one counter is used to record the current counter value at low power mode, the other one is used as a reference counter for anti-attack.

16.3 Function Description

16.3.1 TIMER Clock

The clock frequency of clk_32k is 32KHz, and the clock frequency of clk_timer can be switched among 1GHz, 24MHz and 32KHz.

16.3.2 Timer Mode

- **Normal mode**

At this mode, HPTIMER works as a normal incremental timer. After configuration of load count, interrupt enable, and control bit. The counter will counts from 0 to load count value step by step, and generate an interrupt when the counter value reaches the load count

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value. If the count mode is configured as free-running, then the counter will reload to zero, after reaching the load count, and begin a new counting loop.

- **Hardware adjust mode**

At this mode, HPTIMER works as a special incremental timer with automatic calibration by hardware.
When system is working at normal mode, the counter in high clock domain(hs_cnt) will count up normally. And the counter in low clock domain(ls_cnt) will count plus T24_GCD every T32_GCD low clock period. Since that, the hs_cnt and the ls_cnt will represent the same counter value at every T32_GCD low clock period.
When system enter low power mode, the clock frequency of hs_cnt will also switch to low frequency, but thanks to the ls_cnt, the counter value of current time will not lost. And after system recover from low power mode, the counter value of ls_cnt will automatic calibrate to hs_cnt.

- **Software adjust mode**

At this mode, HPTIMER works as a special incremental timer with calibration by software. Which means software can calibrate the counter value as you wish. The hardware will record the counter value when system enter to and recover from low power mode. And software should get this two begin and end counter values to calculate the lost time during the low power mode, and make a compensation to get the correct system time.

16.4 Register Description

16.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

16.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
HPTIMER_REVISION	0x0000	W	0x3AEE0201	HPTIMER Version Register
HPTIMER_CTRL	0x0004	W	0x00000000	HPTIMER Control Register
HPTIMER_INTR_EN	0x0008	W	0x00000000	Interrupt Mask Register
HPTIMER_T24_GCD	0x000C	W	0x00000000	Common Multiple Divide 24MHz
HPTIMER_T32_GCD	0x0010	W	0x00000000	Common Multiple Divide 32KHz
HPTIMER_LOAD_COUNT0	0x0014	W	0x00000000	Low 32bits of load count value
HPTIMER_LOAD_COUNT1	0x0018	W	0x00000000	High 32bits of load count value
HPTIMER_T24_DELAT_COUNT0	0x001C	W	0x00000000	Low 32bits of 24MHz clock delay time count value
HPTIMER_T24_DELAT_COUNT1	0x0020	W	0x00000000	High 32bits of 24MHz clock delay time count value
HPTIMER_CURR_32K_VALUE0	0x0024	W	0x00000000	Low 32bits of current ls_cnt value
HPTIMER_CURR_32K_VALUE1	0x0028	W	0x00000000	High 32bits of current ls_cnt value
HPTIMER_CURR_TIMER_VALUE0	0x002C	W	0x00000000	Low 32bits of current hs_cnt value
HPTIMER_CURR_TIMER_VALUE1	0x0030	W	0x00000000	High 32bits of current hs_cnt value

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Name	Offset	Size	Reset Value	Description
HPTIMER_T24_32BEGIN0	0x0034	W	0x00000000	Low 32 bits of low power begin counter value
HPTIMER_T24_32BEGIN1	0x0038	W	0x00000000	High 32 bits of low power begin counter value
HPTIMER_T32_24END0	0x003C	W	0x00000000	Low 32 bits of low power end counter value
HPTIMER_T32_24END1	0x0040	W	0x00000000	High 32 bits of low power end counter value
HPTIMER_RECORD_VALUE_VALID	0x0044	W	0x00000000	Record count value valid
HPTIMER_SYNC_REQ	0x0048	W	0x00000000	Synchronize request control
HPTIMER_INTR_STATUS	0x004C	W	0x00000000	Interrupt Status Register
HPTIMER_CURR_ATATK_32K_VALUE0	0x0054	W	0x00000000	Low 32bits of current ATATK counter value
HPTIMER_CURR_ATATK_32K_VALUE1	0x0058	W	0x00000000	High 32bits of current ATATK counter value
HPTIMER_LOAD_COUNT0_32K	0x005C	W	0x00000000	Low 32bits of load count 32k value
HPTIMER_LOAD_COUNT1_32K	0x0060	W	0x00000000	High 32bits of load count 32k value
HPTIMER_CURR_COMP_H_VALUE0	0x0064	W	0x00000000	Low 32bits of hs_cnt value when hardware synchronization enable
HPTIMER_CURR_COMP_H_VALUE1	0x0068	W	0x00000000	High 32bits of hs_cnt value when hardware synchronization enable
HPTIMER_CURR_COMP_L_VALUE0	0x006C	W	0x00000000	Low 32bits of ls_cnt value when hardware synchronization enable
HPTIMER_CURR_COMP_L_VALUE1	0x0070	W	0x00000000	High 32bits of ls_cnt value when hardware synchronization enable
HPTIMER_CURR_COMP_H_32K_VALUE0	0x0074	W	0x00000000	Low 32bits of hs_cnt value when compensation enable
HPTIMER_CURR_COMP_H_32K_VALUE1	0x0078	W	0x00000000	High 32bits of hs_cnt value when compensation enable
HPTIMER_CURR_COMP_L_32K_VALUE0	0x007C	W	0x00000000	Low 32bits of ls_cnt value when compensation enable
HPTIMER_CURR_COMP_L_32K_VALUE1	0x0080	W	0x00000000	High 32bits of ls_cnt value when compensation enable
HPTIMER_INIT_COUNT0_32K	0x0084	W	0x00000000	Low 32bits of initial count 32k value
HPTIMER_INIT_COUNT1_32K	0x008C	W	0x00000000	High 32bits of initial count 32k value

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*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

16.4.3 Detail Registers Description

HPTIMER_REVISION

Address: Operational Base(0x20820000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RO	0x3aee	svn_revision SVN revision
15:10	RO	0x00	reserved
9:8	RO	0x2	ch_type Channel 0 is a low power recovery self-correction count up counter.
7:0	RO	0x01	ip_function IP function. 16'd1

HPTIMER_CTRL

Address: Operational Base(0x20820000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable of the lower 16bit 1'b0: Disable 1'b1: Enable
15:8	RO	0x00	reserved
7	RW	0x0	hs_cnt_auto_hold Auto hold the hs_cnt at hard ware adjust mode when system enter low power mode 1'b0: Disable auto hold 1'b1: Enable auto hold
6	RW	0x0	hp_init_mode Control the hs_cnt initial mode 1'b0: hs_cnt will begin count together with ls_cnt 1'b1: hs_cnt will not wait for ls_cnt
5	RW	0x0	extra_cnt_ctrl Control the extra counter 1'b0: Disable 1'b1: Enable
4	RW	0x0	atatk_cnt_ctrl Control the anti-attack counter 1'b0: Enable 1'b1: Disable
3	RW	0x0	count_mode Timer count mode 1'b0: Free-running mode 1'b1: User-defined count mode
2:1	RW	0x0	timer_mode Select timer as which timer mode 2'b00: Normal timer 2'b01: Adjust timer with hardware adjust 2'b10: Adjust timer with software adjust
0	RW	0x0	timer_en Timer enable 1'b0: Disable 1'b1: Enable

HPTIMER_INTR_EN

Address: Operational Base(0x20820000) + offset (0x0008)

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Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	extra_count_reach_intr_en Extra timer count reach load_count interrupt enable 1'b0: Disable 1'b1: Enable
3	RW	0x0	count_reach_32k_intr_en Low speed count reach interrupt enable 1'b0: Disable 1'b1: Enable
2	RW	0x0	sync_done_intr_en Synchronization done interrupt enable 1'b0: Disable 1'b1: Enable
1	RO	0x0	reserved
0	RW	0x0	count_reach_intr_en High speed count reach load_count interrupt enable 1'b0: Disable 1'b1: Enable

HPTIMER_T24_GCD

Address: Operational Base(0x20820000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	t24_gcd The least common multiple of 24MHz (100MHz) and 32KHz clock cycles divided by 24MHz (100MHz) clock cycles.

HPTIMER_T32_GCD

Address: Operational Base(0x20820000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	t32_gcd The least common multiple of 24MHz (100MHz) and 32KHz clock cycles divided by 32KHz clock cycles.

HPTIMER_LOAD_COUNT0

Address: Operational Base(0x20820000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	load_count0 Low 32bits of load count value.

HPTIMER_LOAD_COUNT1

Address: Operational Base(0x20820000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	load_count1 High 32bits of load count value.

HPTIMER_T24_DELAT_COUNT0

Address: Operational Base(0x20820000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	t24_delay_time_count0 Low 32bits of 24MHz clock delay time count value.

HPTIMER_T24_DELAT_COUNT1

Address: Operational Base(0x20820000) + offset (0x0020)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	t24_delay_time_count1 High 32bits of 24MHz clock delay time count value.

HPTIMER_CURR_32K_VALUE0

Address: Operational Base(0x20820000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	current_32k_value0 Low 32bits of current ls_cnt value.

HPTIMER_CURR_32K_VALUE1

Address: Operational Base(0x20820000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	current_32k_value1 High 32bits of current ls_cnt value.

HPTIMER_CURR_TIMER_VALUE0

Address: Operational Base(0x20820000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	current_value0 Low 32bits of current hs_cnt value.

HPTIMER_CURR_TIMER_VALUE1

Address: Operational Base(0x20820000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	current_value1 High 32bits of current hs_cnt value.

HPTIMER_T24_32BEGIN0

Address: Operational Base(0x20820000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	t24_32begin0 Low 32 bits of hs_cnt value when 24MHz (100MHz) clock switches to 32KHz clock.

HPTIMER_T24_32BEGIN1

Address: Operational Base(0x20820000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	t24_32begin1 High 32 bits of hs_cnt value when 24MHz (100MHz) clock switches to 32KHz clock.

HPTIMER_T32_24END0

Address: Operational Base(0x20820000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	t32_24end0 Low 32 bits of hs_cnt value when 32KHz clock switches to 24MHz (100MHz) clock.

HPTIMER_T32_24END1

Address: Operational Base(0x20820000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	t32_24end1 High 32 bits of hs_cnt value when 32KHz clock switches to 24MHz (100MHz) clock.

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HPTIMER_RECORD_VALUE_VALID

Address: Operational Base(0x20820000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	W1C	0x0	curr_comp_value_32k_valid CURR_COMP_*_32K_VALUE valid 1'b0: Invalid 1'b1: Valid
2	W1C	0x0	curr_comp_value_valid CURR_COMP_*_VALUE valid 1'b0: Invalid 1'b1: Valid
1	W1C	0x0	t32_24end_valid T32_24END value valid 1'b0: Invalid 1'b1: Valid
0	W1C	0x0	t24_32begin_valid T24_32BEGIN value valid 1'b0: Invalid 1'b1: Valid

HPTIMER_SYNC_REQ

Address: Operational Base(0x20820000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable of the lower 16bit 1'b0: Disable 1'b1: Enable
15:10	RO	0x00	reserved
9	RW	0x0	hw_sync_disable 1'b0: Enable synchronization 1'b1: Disable synchronization When this bit is set to 1'b1, then no matter the value of hs_cnt and ls_cnt, the synchronization will not be executed.
8	RW	0x0	hw_sync_en Control the sync logic of hs_cnt 1'b0: Disable 1'b1: Enable When enable this bit, hardware will record the value of hs_cnt and ls_cnt at the time that a hw_sync_req occurs. And if the value of hs_cnt is larger than ls_cnt, then the synchronization to hs_cnt will not be executed.
7	RO	0x0	reserved
6	RW	0x0	hw_sync_compensation_en Enable the compensation to ls_cnt after a hw_sync_req occurs, the hardware will compare the value of hs_cnt and ls_cnt, if hs_cnt is larger than ls_cnt, then the different will be compensated to ls_cnt. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
5	RW	0x0	low_power_compensation_en Enable the compensation to ls_cnt at the time that system enter the low power state, the hardware will compare the value of hs_cnt and ls_cnt, if hs_cnt is larger than ls_cnt, then the different will be compensated to ls_cnt. 1'b0: Disable 1'b1: Enable
4	RW	0x0	compensation_en Control the compensation logic of ls_cnt 1'b0: Disable 1'b1: Enable When enable this bit, hardware will record the value of hs_cnt and ls_cnt at the time that system enter low power state.
3:2	RO	0x0	reserved
1	R/WSC	0x0	hw_sync_req Hs_cnt synchronize request by hardware, which means synchronize hs_cnt by ls_cnt value
0	R/WSC	0x0	sw_sync_req Hs_cnt synchronize request by software, which means directly compensate T24_DELAT_COUNT to hs_cnt

HPTIMER_INTR_STATUS

Address: Operational Base(0x20820000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	W1C	0x0	extra_count_reach Extra cnt reach the load count value
3	W1C	0x0	count_reach_32k Ls_cnt counter value is more than load_count_32k-t24_gcd, and less than load_count_32k
2	W1C	0x0	sync_done hs_cnt synchronization done
1	RO	0x0	reserved
0	W1C	0x0	count_reach Normal counter: hs_cnt reach load_count value

HPTIMER_CURR_ATATK_32K_VALUE0

Address: Operational Base(0x20820000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	current_atatk_32k_value0 Low 32bits of current atatk_cnt_32k value.

HPTIMER_CURR_ATATK_32K_VALUE1

Address: Operational Base(0x20820000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	current_atatk_32k_value1 High 32bits of current atatk_cnt_32k value.

HPTIMER_LOAD_COUNT0_32K

Address: Operational Base(0x20820000) + offset (0x005C)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	load_count0_32k Low 32bits of load count 32k value.

HPTIMER_LOAD_COUNT1_32K

Address: Operational Base(0x20820000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	load_count1_32k High 32bits of load count 32k value.

HPTIMER_CURR_COMP_H_VALUE0

Address: Operational Base(0x20820000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	curr_comp_h_value0 Low 32bits of curr_comp_h_value, which indicate the record value of hs_cnt when a hw_sync_req occurs.

HPTIMER_CURR_COMP_H_VALUE1

Address: Operational Base(0x20820000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	curr_comp_h_value1 High 32bits of curr_comp_h_value, which indicate the record value of hs_cnt when a hw_sync_req occurs.

HPTIMER_CURR_COMP_L_VALUE0

Address: Operational Base(0x20820000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	curr_comp_l_value0 Low 32bits of curr_comp_l_value, which indicate the record value of ls_cnt when a hw_sync_req occurs.

HPTIMER_CURR_COMP_L_VALUE1

Address: Operational Base(0x20820000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	curr_comp_l_value1 High 32bits of curr_comp_l_value, which indicate the record value of ls_cnt when a hw_sync_req occurs.

HPTIMER_CURR_COMP_H_32K_VALUE0

Address: Operational Base(0x20820000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	curr_comp_h_32k_value0 Low 32bits of curr_comp_h_32k_value, which indicate the record value of hs_cnt when system enter the low power state.

HPTIMER_CURR_COMP_H_32K_VALUE1

Address: Operational Base(0x20820000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	curr_comp_h_32k_value1 High 32bits of curr_comp_h_32k_value, which indicate the record value of hs_cnt when system enter the low power state.

HPTIMER_CURR_COMP_L_32K_VALUE0

Address: Operational Base(0x20820000) + offset (0x007C)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	curr_comp_l_32k_value0 Low 32bits of curr_comp_l_32k_value, which indicate the record value of ls_cnt when system enter the low power state.

HPTIMER_CURR_COMP_L_32K_VALUE1

Address: Operational Base(0x20820000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	curr_comp_l_32k_value1 High 32bits of curr_comp_l_32k_value, which indicate the record value of ls_cnt when system enter the low power state.

HPTIMER_INIT_COUNT0_32K

Address: Operational Base(0x20820000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	load_count0_32k Low 32bits of initial count 32k value.

HPTIMER_INIT_COUNT1_32K

Address: Operational Base(0x20820000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	load_count1_32k High 32bits of initial count 32k value.

16.5 Application Notes

16.5.1 Clock and Reset

There are two different clock domains in HPTIMER: clk_timer, clk_32k. The frequency of these clocks are as below:

Table 16-1 Clock Frequency

Clock Name	Clock Source
clk_timer	1G/24M/32K
clk_32k	32K

The clock clk_timer can switch to three different frequencies according to different mode. In normal working mode, HPTIMER is working at 24M or 1G. In low power mode, HPTIMER is working at 32K. And xin_pll_sel is clock control bit to switch between 24M and 1G, which is related to PMU_CRU_CLKSEL_CON01. lp_ena is clock control bit to switch between xin_osc0_func clock and 32K, which is related to PMU_SGRF_SOC_CON0.

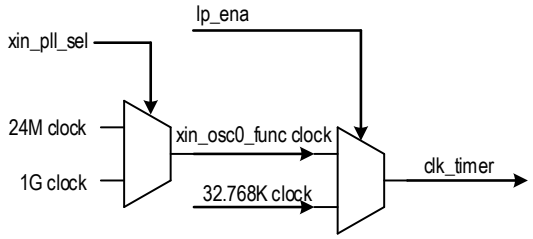

Fig. 16-2 Clock Selection of clk_timer

Please refer to chapter CRU and GRF for detail.

16.5.2 Programming Flow

- **Normal mode**

1. Initialize the HPTIMER by the HPTIMER_CTRL register:

(1) Disable the HPTIMER by writing a '0' to the timer enable bit (bit 0). Accordingly, the timer_hp_en output signal is de-asserted.

(2) Program the timer mode, normal mode by writing a 0x0 to the timer mode bits (bit 1 to bit 2).

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(3) Program the count mode, free-running or user-defined by writing a '0' or '1' to the count mode bit (bit 3).
2. Load the HPTIMER count value into the HPTIMER_LOAD_COUNT1 and HPTIMER_LOAD_ COUNT0 register.
3. Enable the HPTIMER by writing a '1' to bit 0 of HPTIMER_CTRL.

If you want to do another count, repeat steps 1 to 3.

- **Hardware adjust mode**

1. Initialize the HPTIMER by the HPTIMER_CTRL register:
(1) Disable the HPTIMER by writing a '0' to the timer enable bit (bit 0). Accordingly, the timer_hp_en output signal is de-asserted.
(2) Program the timer mode, normal mode by writing a 0x1 to the timer mode bits (bit 1 to bit 2).
(3) Program the count mode, free-running or user-defined by writing a '0' or '1' to the count mode bit (bit 3).
2. Initialize the HPTIMER by the HPTIMER_INTR_STATUS register. Write 0x5 to HPTIMER_ INTR_STATUS register to clear HPTIMER_INTR_STATUS register.
3. Configure the HPTIMER GCD register.
(1) Divide the least common multiple of clk_timer and clk_32k clock cycle by clk_timer clock cycle and configure it in HPTIMER_T24_GCD register.
(2) Divide the least common multiple of clk_timer and clk_32k clock cycle by clk_32k clock cycle and configure it in HPTIMER_T32_GCD register.
4. Enable the HPTIMER by writing a '1' to bit 0 of HPTIMER_CTRL.
5. Configure the PMU_SGRF_SOC_CON0 to assert lp_ena before the chip enters low power consumption mode.
6. The chip enters and exits the low power consumption mode at any time in between.
7. Configure the PMU_SGRF_SOC_CON0 to de-assert lp_ena after the chip exits low power consumption mode.
8. Read out the INTR_STATUS register until the sync_done bit segment (bit 2) is '1', indicating that the HPTIMER count is adjusted.
9. Write 0x4 to HPTIMER_ INTR_STATUS register to clear HPTIMER_INTR_STATUS register.

If the chip enters and exits the low power consumption mode again, repeat steps 6 to 9.

- **Software adjust mode**

1. Initialize the HPTIMER by the HPTIMER_CTRL register:
(1) Disable the HPTIMER by writing a '0' to the timer enable bit (bit 0). Accordingly, the timer_hp_en output signal is de-asserted.
(2) Program the timer mode, normal mode by writing a 0x2 to the timer mode bits (bit 1 to bit 2).
(3) Program the count mode, free-running or user-defined by writing a '0' or '1' to the count mode bit (bit 3).
2. Initialize the HPTIMER by the HPTIMER_INTR_STATUS and BEGIN_END_VALID register. Write 0x5 to HPTIMER_ INTR_STATUS register to clear HPTIMER_INTR_STATUS register. write 0x3 to RECORD_VALUE_VALID register to clear RECORD_VALUE_VALID register.
3. Enable the HPTIMER by writing a '1' to bit 0 of HPTIMER_CTRL.
4. Configure the PMU_SGRF_SOC_CON0 to assert lp_ena before the chip enters low power consumption mode.
5. The chip enters and exits the low power consumption mode at any time in between.
6. Configure the PMU_SGRF_SOC_CON0 to deassert lp_ena after the chip exits low power consumption mode.
7. Read out RECORD_VALUE_VALID register until the value of it is 0x3, which indicates that the chip has entered and exited the low power consumption mode, then you can adjust the timer count value. Then write 0x3 to RECORD_VALUE_VALID register to clear the register.
8. The count value of HPTIMER compensation.
(1) Read out HPTIMER_T24_32BEGIN1, TIMER_ HP_T24_32BEGIN0, HPTIMER_T32_ 24END1 and HPTIMER_T32_24END0 register.

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(2) configure HPTIMER_T24_DELAT_COUNT1 and HPTIMER_T24_DELAT_COUNT0 registers to compensate for the count values according to the values of these registers read out above.
(3) Write 0x1 to HPTIMER_SYNC_REQ register to start compensation counting.
(4) Read out the INTR_STATUS register until the sync_done bit segment (bit 2) is '1', indicating that the compensation count is completed.
9. Write 0x5 to HPTIMER_ INTR_STATUS register to clear HPTIMER_INTR_STATUS register.

If the chip enters and exits the low power consumption mode again, repeat steps 5 to 8.

- **Hardware compensation configuration**

The hardware compensation configurations are all related to the HPTIMER_SYNC_REQ register.

1. When compensation_en(bit 4) of HPTIMER_SYNC_REQ is asserted, then the hardware will record the value of hs_cnt and ls_cnt at the time that system enters low power mode, and the record value will be stored at HPTIMER_CURR_COMP_*_32K_VALUE.
2. When low_power_compensation_en(bit 5) of HPTIMER_SYNC_REQ is asserted, then the hardware will compare the value of hs_cnt and ls_cnt at the time that system enters low power mode. And if hs_cnt is greater than ls_cnt at this time, the different will be compensated to ls_cnt.
3. When hw_sync_compensation_en(bit 6) of HPTIMER_SYNC_REQ is asserted, then the hardware will compare the value of hs_cnt and ls_cnt at the time that hardware synchronization occurs. And if hs_cnt is larger than ls_cnt at this time, the different will be compensated to ls_cnt.
4. When hw_sync_en(bit 7) of TIMRE_HP_SYNC_REQ is asserted, then the hardware will record the value of hs_cnt and ls_cnt at the time that hardware synchronization occurs, and the record value will be stored at HPTIMER_CURR_COMP_*_VALUE. The other hand, if the value of hs_cnt is greater than ls_cnt，then the synchronization to hs_cnt will not be executed.
5. When hw_sync_disable(bit 8) of HPTIMER_SYNC_REQ is asserted, then no matter the value of hs_cnt and ls_cnt, the synchronization will not be executed.

- **Low power mode wakeup**

This function is used at hardware adjust mode, the programing flow is mainly as hardware adjust mode.

1. Configure HPTIMER to hardware adjust mode.
2. Configure the HPTIMER GCD register.
3. Enable the HPTIMER by writing a '1' to bit 0 of HPTIMER_CTRL.
4. Prepare to enter low power mode:

(1) Configure PMU to set HPTIMER as wake up source.
(2) Configure the bit 3 of HPTIMER_INTR_EN to set count reach interrupt enable at 32K.
(3) Configure the HPTIMER_LOAD_COUNT1_32K and HPTIMER_LOAD_COUNT0_32K to set the wake up time. (note that user must configure HPTIMER_LOAD_COUNT0_32K at last)

5. Configure the PMU_SGRF_SOC_CON0 to assert lp_ena before the chip enters low power consumption mode.
6. Wait for HPTIMER to wake up system.
7. Configure the PMU_SGRF_SOC_CON0 to de-assert lp_ena after the chip exits low power consumption mode.
8. Read out the INTR_STATUS register and write 0x8 to HPTIMER_INTR_STATUS register to clear count reach 32k interrupt.
9. Read out the INTR_STATUS register until the sync_done bit segment (bit 2) is '1', indicating that the HPTIMER count is adjusted.
10. Write 0x4 to HPTIMER_ INTR_STATUS register to clear HPTIMER_INTR_STATUS register.

If the chip enters and exits the low power consumption mode again, repeat steps 4 to 10.

- **High performance timing interrupt**

HPTIMER provides a 32-bits High performance counter to generate timing interrupt at hardware adjust mode.

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1. Configure HPTIMER to hardware adjust mode.
2. Configure the HPTIMER_LOAD_COUNT0 to set the load count.
3. Configure bit 4 of HPTIMER_INTR_EN to enable interrupt.
4. Configure bit 5 of HPTIMER_CTRL to enable the hyper performance counter to work.
5. Wait for the interrupt generate.
6. Write '1' to bit 4 of HPTIMER_INTR_STATUS to clear the interrupt status.

When the count mode of timer is configured to free-running, then the interrupt will assert every load count time, otherwise the interrupt will generate only one time.

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Chapter 17 Real Time Clock (RTC)

17.1 Overview

The main function of a real-time clock (RTC) is to keep track of the current time of computer. The main characteristics of RTC are listed below:

- Support battery voltage detect.
- Support RTC external power off indication.
- Support 32.768 kHz clock self-detect.
- Provides year, month, day, weekday, hours, minutes, and seconds based on a 32.768 kHz crystal oscillator.
- Support compensation for the second and hour count.
- BCD representation of time, calendar and alarm.
- 12- or 24-hour clock with AM and PM in 12-hour mode.
- APB interface with 8bit data bus width.
- Bus-compatible interrupt signals (IRQ)
- Interrupts are separately software maskable:
  - Alarm interrupt
  - Periodic interrupt
  - Chip power off interrupt
  - Battery power atypical interrupt

17.2 Block Diagram

Fig. 17-1 RTC Block Diagram

System Interface
The system interface implements the APB slave operation. Rtc_test and RTC use the common APBus address decoder, the common control bus and data bus.
rtc_test
rtc 32k clock test module, test the 32k clock accuracy.
rtc_analog
Battery power domain, support power and generate 32k clock for RTC digital, and some detect function, such as external power off and battery voltage atypical.
rtc_timer
Include npor, clock_gen, irq_gen, timer and reg_file, the main function is to keep track of the current time, alarm, and some control registers for RTC Analog.

17.3 Function Description

17.3.1 APB Interface

There is an APB slave interface in RTC. It is responsible for accessing registers.

17.3.2 Alarm interrupt

Alarm interrupt generate from the real-time, the alarm time, and the alarm_irq_mask bit.
alarm_irq_mask[0]: 1'b0: fix alarm second, 1'b1: every second.
alarm_irq_mask[1]: 1'b0: fix alarm minute, 1'b1: every minute.
alarm_irq_mask[2]: 1'b0: fix alarm hour, 1'b1: every hour.
alarm_irq_mask[3]: 1'b0: fix alarm day, 1'b1: every day.
alarm_irq_mask[4]: 1'b0: fix alarm month, 1'b1: every month.
alarm_irq_mask[5]: 1'b0: fix alarm year
when alarm_irq_mask = 6'h3, means every hour fix min and fix second alarm.
When alarm_irq_mask = 6'b101011, fix year, every month, fix day every hour fix min and fix second alarm.

17.3.3 RTC 32k clock test

Due to the analog generator 32k clock affected by temperature, voltage, clock precision need test with the environment change. In rtc test, use 24M clock as reference clock to

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measure the 32k clock. Before start test 32k clock, we should configure test length, when rtc test done(0x78[2]), latch the 24M clock domain counter, and read out the counter from rtc_test registers(0x80~0x8c) via apb bus.

17.3.4 Compensation

In RTC digital design, we set three level compensation, the compensation value due to the RTC 32k clock test result, and if we need compensation, we need configure the compensation enable bit.

Compensation every hour, compensation at last minute every hour, and support add time and sub time by the MSB bit.

Compensation every day, compensation at last minute in last hour every day, and support add time and sub time by the MSB bit.

Compensation every month, compensation at last minute in last hour in last day every month, and support add time and sub time by the MSB bit.

17.4 Register Description

17.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

17.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
RTC_SET_SECONDS	0x0000	W	0x00000000	Seconds
RTC_SET_MINUTES	0x0004	W	0x00000000	Minutes
RTC_SET_HOURS	0x0008	W	0x00000000	Hours
RTC_SET_DAYS	0x000C	W	0x00000000	Days
RTC_SET_MONTHS	0x0010	W	0x00000000	Months
RTC_SET_YEARSL	0x0014	W	0x00000000	Years (LSB)
RTC_SET_YEARSH	0x0018	W	0x00000000	Years (MSB)
RTC_SET_WEEKS	0x001C	W	0x00000000	Weeks
RTC_ALARM_SECONDS	0x0020	W	0x00000000	Alarm seconds
RTC_ALARM_MINUTES	0x0024	W	0x00000000	Alarm minutes
RTC_ALARM_HOURS	0x0028	W	0x00000000	Alarm hours
RTC_ALARM_DAYS	0x002C	W	0x00000000	Alarm days
RTC_ALARM_MONTHS	0x0030	W	0x00000000	Alarm months
RTC_ALARM_YEARSL	0x0034	W	0x00000000	Alarm years (LSB)
RTC_ALARM_YEARSH	0x0038	W	0x00000000	Alarm years (MSB)
RTC_CTRL	0x003C	W	0x00000000	RTC controll registers
RTC_STATUS0	0x0040	W	0x00000000	RTC statues registers
RTC_STATUS1	0x0044	W	0x00000000	RTC statues registers
RTC_INT0_EN	0x0048	W	0x00000000	RTC interrupt enable registers
RTC_INT1_EN	0x004C	W	0x00000000	RTC interrupt enable registers
RTC_MSEC_CTRL	0x0050	W	0x00000000	Millisecond control
RTC_MSEC_CNT	0x0054	W	0x00000000	Millisecond periodic count
RTC_COMP_H	0x0058	W	0x00000000	Hour compensation registers
RTC_COMP_D	0x005C	W	0x00000000	Day compensation registers
RTC_COMP_M	0x0060	W	0x00000000	Month compensation registers
RTC_XO_TRIM0	0x0064	W	0x00000000	XO trim registers
RTC_XO_TRIM1	0x0068	W	0x00000000	XO trim registers
RTC_TEST_SEL	0x006C	W	0x00000000	Analog test
RTC_LDO_CTRL	0x0070	W	0x00000000	LDO control
RTC_ANALOG_EN	0x0074	W	0x00000000	Analog config
RTC_TEST_ST	0x0078	W	0x00000000	Test 32k clock start and status
RTC_TEST_LEN	0x007C	W	0x00000000	Test 32k clock length, unit second.

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Name	Offset	Size	Reset Value	Description
RTC_CNT_0	0x0080	W	0x00000000	24M clock counter[7:0]
RTC_CNT_1	0x0084	W	0x00000000	24M clock counter[15:8]
RTC_CNT_2	0x0088	W	0x00000000	24M clock counter[23:16]
RTC_CNT_3	0x008C	W	0x00000000	24M clock counter[31:24]

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

17.4.3 Detail Registers Description

RTC_SET_SECONDS

Address: Operational Base(0x21280000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:4	RW	0x0	SEC1 Set the second digit of the RTC seconds (0-5).
3:0	RW	0x0	SEC0 Set the first digit of the RTC seconds (0-9).

RTC_SET_MINUTES

Address: Operational Base(0x21280000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:4	RW	0x0	MIN1 Set the second digit of the RTC minutes (0-5).
3:0	RW	0x0	MIN0 Set the first digit of the RTC minutes (0-9).

RTC_SET_HOURS

Address: Operational Base(0x21280000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	AMPM Only used in PM-AM mode 1'b1: PM 1'b0: AM.
6	RO	0x0	reserved
5:4	RW	0x0	HOUR1 Set the second digit of the RTC hours.
3:0	RW	0x0	HOUR0 Set the first digit of the RTC hours.

RTC_SET_DAYS

Address: Operational Base(0x21280000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:4	RW	0x0	DAY1 Set the second digit of the RTC days.
3:0	RW	0x0	DAY0 Set the first digit of the RTC days.

RTC_SET_MONTHS

Address: Operational Base(0x21280000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	MONTH1 Set the second digit of the RTC months.

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	MONTH0 Set the first digit of the RTC months.

RTC_SET_YEARSL

Address: Operational Base(0x21280000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	YEAR1 Set the second digit of the RTC years.
3:0	RW	0x0	YEAR0 Set the first digit of the RTC years.

RTC_SET_YEARSH

Address: Operational Base(0x21280000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	YEAR3 Set the 3th digit of the RTC years.
3:0	RW	0x0	YEAR2 Set the second digit of the RTC years.

RTC_SET_WEEKS

Address: Operational Base(0x21280000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:0	RW	0x0	WEEK Set the second digit of the RTC weeks. configure value: 1~7.

RTC_ALARM_SECONDS

Address: Operational Base(0x21280000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:4	RW	0x0	ALARM_SEC1 Set the second digit of the RTC alarm seconds.
3:0	RW	0x0	ALARM_SEC0 Set the first digit of the RTC alarm seconds.

RTC_ALARM_MINUTES

Address: Operational Base(0x21280000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:4	RW	0x0	ALARM_MIN1 Set the second digit of the RTC alarm minutes.
3:0	RW	0x0	ALARM_MIN0 Set the first digit of the RTC alarm minutes.

RTC_ALARM_HOURS

Address: Operational Base(0x21280000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ALARM_PM_AM Set alarm PM or AM: only used in PM-AM mode. 1'b1: PM 1'b0: AM.

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Bit	Attr	Reset Value	Description
6	RO	0x0	reserved
5:4	RW	0x0	ALARM_HOUR1 Set the second digit of the RTC alarm hours.
3:0	RW	0x0	ALARM_HOUR0 Set the first digit of the RTC alarm hours.

RTC_ALARM_DAYS

Address: Operational Base(0x21280000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:4	RW	0x0	ALARM_DAY1 Set the second digit of the RTC alarm days.
3:0	RW	0x0	ALARM_DAY0 Set the first digit of the RTC alarm days.

RTC_ALARM_MONTHS

Address: Operational Base(0x21280000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	ALARM_MONTH1 Set the second digit of the RTC alarm months.
3:0	RW	0x0	ALARM_MONTH0 Set the first digit of the RTC alarm months.

RTC_ALARM_YEARSL

Address: Operational Base(0x21280000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	ALARM_YEAR1 Set the second digit of the RTC alarm years.
3:0	RW	0x0	ALARM_YEAR0 Set the first digit of the RTC alarm years.

RTC_ALARM_YEARSH

Address: Operational Base(0x21280000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	ALARM_YEAR3 Set the 3th digit of the RTC alarm years.
3:0	RW	0x0	ALARM_YEAR2 Set the second digit of the RTC alarm years.

RTC_CTRL

Address: Operational Base(0x21280000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	RTC_READ_SEL Reserved
6	RW	0x0	GET_TIME Reserved
5	RO	0x0	reserved
4	RW	0x0	COMP_MODE Error compensation mode bit

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Bit	Attr	Reset Value	Description
3	RW	0x0	AMPM_MODE AMPM mode set. 1'b0: 24 hours mode 1'b1: 12 hours mode.
2	RW	0x0	COMP_EN Auto compensation enabile bit. 1'b0: No auto compensation 1'b1: Auto compensation enabled.
1	RW	0x0	PSEL_SEL Psel select bit. 1'b0: psel 1'b1: psel & sys_npor
0	RW	0x0	START_RTC RTC trigger bit. 1'b0: RTC stop 1'b1: RTC start. Note: RTC_time(SET_SECONDS/MINUTES/HOURS/DAYS/MONTHS/YEARS) can only be changed during RTC stop.

RTC_STATUS0

Address: Operational Base(0x21280000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	MSEC_ST milisec periodic interrupt occurred.
5	RO	0x0	reserved
4	RW	0x0	ALARM Indicates that an alarm interrupt has been generated.
3	RW	0x0	EVENT_1D One day has occurred.
2	RW	0x0	EVENT_1H One hour has occurred.
1	RW	0x0	EVENT_1M One minutes has occurred.
0	RW	0x0	EVENT_1S One second has occurred.

RTC_STATUS1

Address: Operational Base(0x21280000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RO	0x0	EXT_OFF RTC external power detect status. 1'b0: external power on 1'b1: external power off.
2	RO	0x0	BAT_DET Battery voltage detect status. 1'b0: battery voltage in typical range 1'b1: battery voltage lower.
1	RO	0x0	SYS_INT Reserved

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Bit	Attr	Reset Value	Description
0	RO	0x0	RUN_ST 1'b0: RTC is frozen. 1'b1: RTC is running. Note: This bit shows the real state of the RTC.

RTC_INT0_EN

Address: Operational Base(0x21280000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	ALARM_IRQ_EN Alarm interrupt output enable bit. 1'b1: enable 1'b0: disable. include external power on or off.
6	RW	0x0	ALARM_IRQ_EN_PD Alarm interrupt output enable bit(only asserted when external power down). 1'b1: enable 1'b0: disable. not need config ALARM_IRQ_EN.
5:0	RW	0x00	ALARM_IRQ_MASK Alarm irq mask: alarm irq mask[0]: second alarm alarm irq mask[1]: minute alarm alarm irq mask[2]: hour alarm alarm irq mask[3]: day alarm alarm irq mask[4]: month alarm alarm irq mask[5]: year alarm if mask bit equal 1'b1, means that fix point, if mask bit equal 1'b0, means every. example: if configure ALARM_IRQ_MASK = 6'h01, configure RTC_ALARM_SECONDS = 8'h03, every minute, if second == 8'h03, alarm active; if configure ALARM_IRQ_MASK = 6'h17, configure RTC_ALARM_SECONDS = 8'h30: configure RTC_ALARM_MINUTES = 8'h30: configure RTC_ALARM_HOURS = 8'h8 (24hour mode): configure RTC_ALARM_MONTH=8'h2. every day in February, when Am 8:30:30 (H:M:S), alarm active.

RTC_INT1_EN

Address: Operational Base(0x21280000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	MSEC_IRQ_EN Milisecond interrupt output enable bit. 1'b0: Disable 1'b1: Enable
6	RW	0x0	EXT_IRQ_EN External power off interrupt output enable bit. 1'b0: disable 1'b1: Enable.

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Bit	Attr	Reset Value	Description
5	RW	0x0	BAT_IRQ_EN Detect battery voltage lower interrupt output enable bit. 1'b0: Disable 1'b1: Enable.
4	RW	0x0	SYS_IRQ_MASK System interrupt mask bit. 1'b0: Normal mode, no system interrupt masked 1'b1: system interrupt masked, no system interrupt output.
3	RW	0x0	PER_PD_MASK_EN Periodic interrupt output enable bit, when RTC external power down. 1'b1: Mask periodic interrupt while the external power down 1'b0: Normal mode, no periodic interrupt masked when external power down Need config PER_TIMER_EN enable.
2	RW	0x0	PER_TIMER_EN Periodic interrupt output enable bit. 1'b0: Disable 1'b1: Enable.
1:0	RW	0x0	EVERY_TYPE_SEL Periodic interrupt type select. 2'b00: Every second 2'b01: Every minute 2'b10: Every hour 2'b11: Every day.

RTC_MSEC_CTRL

Address: Operational Base(0x21280000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2:1	RW	0x0	MSEC_SEL Milisec periodic clock select. 2'b00: 8hz 2'b01: 128hz 2'b10: 1khz 2'b11: 32khz.
0	RW	0x0	MSEC_EN Milisec periodic function enable.

RTC_MSEC_CNT

Address: Operational Base(0x21280000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	MSEC_CNT Number of milisec periodic interrupt interval clock.

RTC_COMP_H

Address: Operational Base(0x21280000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	COMP_H_DIR Compensation direction every hour. 1'b1: Add second 1'b0: Sub second.

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Bit	Attr	Reset Value	Description
6:0	RW	0x00	COMP_HOUR This register contains the number of second periods to be added/sub every hour. the 7bit value need 8421BCD code.

RTC_COMP_D

Address: Operational Base(0x21280000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	COMP_D_DIR compensation direction every day. 1'b1: Add second 1'b0: Sub second.
6:0	RW	0x00	COMP_DAY This register contains the number of second periods to be added/sub every day. the 7bit value need 8421BCD code.

RTC_COMP_M

Address: Operational Base(0x21280000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	COMP_M_DIR Compensation direction every month. 1'b1: Add second 1'b0: Sub second.
6:0	RW	0x00	COMP_MONTH This register contains the number of second periods to be added/sub every month. the 7bit value need 8421BCD code.

RTC_XO_TRIM0

Address: Operational Base(0x21280000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:3	RW	0x0	D2A_XO_XOUT_CAP_SEL Capacitance compensation for xo load. 3'b000: 0pf 3'b001: 1pf 3'b010: 2pf 3'b011: 3pf
2:1	RW	0x0	D2A_XO_XIN_CAP_SEL Capacitance compensation for xo load. 3'b000: 0pf 3'b001: 1pf 3'b010: 2pf 3'b011: 3pf
0	RW	0x0	D2A_XO_EN XO enable bit. 1'b0: Disable 1'b1: Enable configure 1'b1 for rtc analog 32k generate.

RTC_XO_TRIM1

Address: Operational Base(0x21280000) + offset (0x0068)

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Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:3	RW	0x0	D2A_XO_GM_SEL Reserved
2:0	RW	0x0	D2A_XO_CUR_SEL Reserved

RTC_TEST_SEL

Address: Operational Base(0x21280000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:4	RW	0x0	D2A_AVDD_SEL XO LDO output voltage adjust
3:0	RW	0x0	D2A_TEST_SEL Reserved

RTC_LDO_CTRL

Address: Operational Base(0x21280000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:4	RW	0x0	D2A_RESERVE D2A_RESERVE[0]: d2a_por_ref_sel[1] D2A_RESERVE[1]: clk_32k_h gating enable bit
3:1	RW	0x0	D2A_DVDD_SEL DIG LDO output voltage adjust
0	RW	0x0	D2A_DVDD_TEST_SEL DIG LDO test path enable signal

RTC_ANALOG_EN

Address: Operational Base(0x21280000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	D2A_CLK_OUT_EN XO clock output enable bit. 1'b0: Disable 1'b1: Enable. configure d2a_clk_out_en 1'b1 after d2a_xo_en, about 500ms.
2	RW	0x0	D2A_BAT_DET_EN battery voltage detect enable bit. 1'b0: Disable 1'b1: Enable.
1	RW	0x0	D2A_VDET_SEL Reserved
0	RW	0x0	D2A_CLK_BYPS_EN 32K clock input from XIN pin. 1'b0: Disable 1'b1: Enable.

RTC_TEST_ST

Address: Operational Base(0x21280000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RO	0x0	TEST_DONE 32K clock test status. 1'b0: Test idle or in test. 1'b1: Test done.

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Bit	Attr	Reset Value	Description
1	RO	0x0	TEST_START_ST Test clk32k status. 1'b0: Idle 1'b1: In test.
0	RW	0x0	TEST_START Test clk32k start. 1'b0: Stop 1'b1: Start.

RTC_TEST_LEN

Address: Operational Base(0x21280000) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	TEST_LENGTH Test length, unit second.

RTC_CNT_0

Address: Operational Base(0x21280000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	CLK24M_CNT_0 Count[7:0]

RTC_CNT_1

Address: Operational Base(0x21280000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	CLK24M_CNT_1 Count[15:8]

RTC_CNT_2

Address: Operational Base(0x21280000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	CLK24M_CNT_2 Count[23:16]

RTC_CNT_3

Address: Operational Base(0x21280000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	CLK24M_CNT_3 Count[31:24]

17.5 Application Notes

1) APB configuration operation:
   pwdata[31:8] == 24'hc45229, pwdata[7:0] store the configure value.
2) If enable AMPM mode, AMPM mode need set before real time set.
3) If update real time, need stop RTC first, and then set real time registers and start RTC.
4) RTC work sequence:
   Wait ldo rdy;
   APB cfg D2A_XO_EN: 0x64[0] = 1
   Wait 200ms for xo 32k clock stable;

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APB cfg D2A_CLK_OUT_EN: 0x74[3] = 1
APB cfg real time: 0x00~0x1c;
APB cfg alarm time: 0x20~0x38;
APB cfg interrupt enable: 0x48, 0x4c;
APB cfg millisecond register: 0x50, 0x54;
APB cfg compensation register: 0x58, 0x5c, 0x60;
Set START_RTC, 0x3c[0] = 1
Read RUN_ST, 0x44[0], check rtc status.

5) Read time: Read time from: 0x00~0x1c
   Due to shadow registers delete, read time maybe not all right, need read at least three times: time0, time1, time2(need in 1 second).
   If time0, time1, time2 all different, the right time is the time2;
   If time0, time1, time2 have two or three the same, the right time is the same time.
6) Stop RTC: APB cfg 0x3c[0]=0; read RUN_ST check RTC stop.

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Chapter 18 RC oscillator Controller (RCOSC_CTRL)

18.1 Overview

The RC oscillator Controller (RCOSC_CTRL) is used to control the output frequency of RC oscillator (RCOSC). data transmission from host to flash device or from flash device to host. RCOSC_CTRL is connected to APB BUS through an APB Slave.
RCOSC_CTRL supports the following features:

- Support RCOSC output frequency detection
- Support software to manually adjust RCOSC frequency
- Support hardware to automatically adjust RCOSC frequency
- Support automatic frequency adjustment abnormal frequency detection (greater than the maximum output frequency supported by RCOSC or less than the minimum output frequency supported by RCOSC)
- Interrupts are separately software maskable:
- Manually adjust the frequency of RCOSC to complete the interrupt
- Automatically adjust the frequency of RCOSC upward to complete interrupt
- Automatic downward adjustment of RCOSC frequency completes interrupt
- Abnormal higher frequency detection of RCOSC frequency interrupt
- Abnormal lower frequency detection of RCOSC frequency interrupt

18.2 Block Diagram

RCOSC_CTRL comprises with:

- rcosc_ctrl_adj: Automatically adjust the frequency of RCOSC according to the calculation result of freq_cal module.
- freq_adj: Frequency calculation module

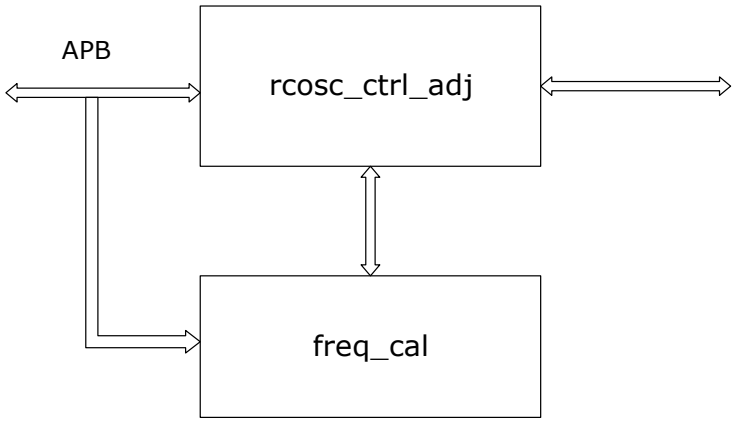

Fig. 18-1 RCOSC_CTRL Block Diagram

18.3 Function Description

18.3.1 APB Interface

There is an APB slave interface in RTC. It is responsible for accessing registers.

18.3.2 Automatic adjustment of RCOSC frequency

According to the target frequency, RCOSC_CTRL can automatically adjust the parameters of RCOSC up or down to the target frequency. When the frequency adjustment is completed, the completion interrupt indication in different adjustment directions will be given. If abnormal higher frequency or abnormal lower frequency is detected in the frequency adjustment process, the frequency adjustment will be terminated and an interrupt will be reported.

18.3.3 Frequency calculation

The time-counter is used to measure the frequency of RCOSC, and the time-counter uses reference clock as counting clock. RCOSC_CTRL generates a signal for frequency stabilization by comparing the count values of RCOSC frequency and the count of reference clock in the same time period.

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The measurement precision is configured through the APB interface. At the end of each measurement period, the count measured is equivalent to the frequency of RCOSC frequency.

18.4 Register Description

18.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

18.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
RCOSC_CTRL_CTRL	0x0000	W	0x00000000	RCOSC_CTRL Control Registers
RCOSC_CTRL_CAL_CNT	0x0004	W	0x00000000	Frequency Calculation Accuracy
RCOSC_CTRL_FREQ_MANUAL	0x0008	W	0x00000000	Frequency Value of Manual
RCOSC_CTRL_FREQ_AUTO_UP	0x000C	W	0x00000000	Frequency Value of Automatic Upward
RCOSC_CTRL_FREQ_AUTO_DOWN	0x0010	W	0x00000000	Frequency Value of Automatic Downward
RCOSC_CTRL_FREQ_TARGET	0x0014	W	0x00000000	Target Frequency Value
RCOSC_CTRL_INT_EN	0x0018	W	0x00000000	Interrupt Enable Register
RCOSC_CTRL_INT_STATUS	0x001C	W	0x00000000	Interrupt State Register
RCOSC_CTRL_STATUS	0x0020	W	0x00000000	RCOSC_CTRL Status Registers

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

18.4.3 Detail Registers Description

RCOSC_CTRL_CTRL

Address: Operational Base(0x20860000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:10	RW	0x00	trim_fine_manual RCOSC trim_fine value of manual frequency adjustment.
9:7	RW	0x0	trim_coarse_manual RCOSC trim_coarse value of manual frequency adjustment.
6	RW	0x0	rcosc_trim_pwm reserved The lowest bit of the frequency configuration of RCOSC is reserved for PWM or DSM to adjust the frequency of RCOSC more finely.
5	RW	0x0	rcosc_sm_en The working mode of voltage comparator in RCOSC. 1'b0: Conventional inverter mode 1'b1: Schmidt inverter mode
4	RW	0x0	rcosc_en RCOSC enable bit. 1'b0: enable 1'b1: disable
3	RW	0x0	auto_down_en RCOSC automatic downward frequency adjustment enable signal. 1'b0: disable 1'b1: enable

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Bit	Attr	Reset Value	Description
2	RW	0x0	auto_up_en RCOSC automatic upward frequency adjustment enable signal. 1'b0: disable 1'b1: enable
1	RW	0x0	auto_manual_en Automatic or maunal frequency adjustment enable. 1'b0: manual 1'b1: automatic
0	RW	0x0	freq_cal_start Frequency measurement and frequency compare module enable signal. 1'b0: disable 1'b1: enable

RCOSC_CTRL_CAL_CNT

Address: Operational Base(0x20860000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cal_cnt Used to configure the measurement period of the frequency measurement module.

RCOSC_CTRL_FREQ_MANUAL

Address: Operational Base(0x20860000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	freq_manual Measured frequency value of maunal adjustment.

RCOSC_CTRL_FREQ_AUTO_UP

Address: Operational Base(0x20860000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	freq_auto_up Measured frequency value of automatic upward adjustment.

RCOSC_CTRL_FREQ_AUTO_DOWN

Address: Operational Base(0x20860000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	freq_auto_down Measured frequency value of automatic downward adjustment.

RCOSC_CTRL_FREQ_TARGET

Address: Operational Base(0x20860000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	freq_target Target frequency value of hardware automatic frequency modulation.

RCOSC_CTRL_INT_EN

Address: Operational Base(0x20860000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	freq_less_int_en Interrupt enable when the target frequency is lower than the low-frequency limit of rcosc. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3	RW	0x0	freq_over_int_en Interrupt enable when the target frequency is higher than the high-frequency limit of rcosc. 1'b0: Disable 1'b1: Enable
2	RW	0x0	auto_down_done_int_en Automatic downward frequency adjustment done interrupt enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	auto_up_done_int_en Automatic upward frequency adjustment done interrupt enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	manual_done_int_en Maunal frequency adjustment done interrupt enable 1'b0: Disable 1'b1: Enable

RCOSC_CTRL_INT_STATUS

Address: Operational Base(0x20860000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	freq_less_int Interrupt when the target frequency is lower than the RCOSC low-frequency limit. 1'b0: None 1'b1: Interrupt when the target frequency is lower than the RCOSC low-frequency limit.
3	RW	0x0	freq_over_int Interrupt when the target frequency is higher than the RCOSC high-frequency limit. 1'b0: None 1'b1: Interrupt when the target frequency is higher than the RCOSC high-frequency limit.
2	RW	0x0	auto_down_done_int Automatic downward frequency adjustment done interrupt 1'b0: None 1'b1: Indicates that automatic downward frequency adjustment done interrupt.
1	RW	0x0	auto_up_done_int Automatic upward frequency adjustment done interrupt 1'b0: None 1'b1: Indicates that automatic upward frequency adjustment done interrupt.
0	RW	0x0	manual_done_int Maunal frequency adjustment done interrupt 1'b0: None 1'b1: Indicates that maunal frequency adjustment done interrupt.

RCOSC_CTRL_STATUS

Address: Operational Base(0x20860000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
22:15	RO	0x00	trim_fine_down RCOSC trim_fine value of automatic downward frequency adjustment.
14:12	RO	0x0	trim_coarse_down RCOSC trim_coarse value of automatic downward frequency adjustment.
11:4	RO	0x00	trim_fine_up RCOSC trim_fine value of automatic upward frequency adjustment.
3:1	RO	0x0	trim_coarse_up RCOSC trim_coarse value of automatic upward frequency adjustment.
0	RO	0x0	freq_valid Measurement of the valid signal indication of the RCOSC output frequency. 1'b0: Invalid 1'b1: Valid

18.5 Application Notes

18.5.1 Manual frequency adjustment mode

APB configures RCOSC_CTRL_CAL_CNT register to set the measurement accuracy of frequency calculation module.
APB configures the RCOSC_CTRL_INT_EN register to enable the interrupt enable signal to be completed by manually adjusting the frequency of RCOSC.
APB configures RCOSC_CTRL_CTRL register to enable manual adjustment mode, trim_coarse and trim_fine parameters of RCOSC adjustment frequency, RCOSC enable signal rcosc_en, and start signal of frequency calculation module.

18.5.2 Automatic upward adjustment frequency mode

APB configures RCOSC_CTRL_CAL_CNT register to set the measurement accuracy of frequency calculation module.
APB configures the RCOSC_CTRL_INT_EN register to enable the interrupt enable signal to automatically adjust the frequency of RCOSC upward.
APB configuration RCOSC_CTRL_FREQ_TARGET register is used to configure the target frequency.
APB configures RCOSC_CTRL_CTRL register to enable automatic adjustment mode, RCOSC enable signal rcosc_en, and frequency calculation module start signal.

18.5.3 Automatic downward adjustment frequency mode

APB configures RCOSC_CTRL_CAL_CNT register to set the measurement accuracy of frequency calculation module.
APB configures the RCOSC_CTRL_INT_EN register to enable the interrupt enable signal to automatically adjust the RCOSC frequency downward.
APB configuration RCOSC_CTRL_FREQ_TARGET register is used to configure the target frequency.
APB configures RCOSC_CTRL_CTRL register to enable automatic adjustment mode, RCOSC enable signal rcosc_en, and frequency calculation module start signal.

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Chapter 19 Mailbox

19.1 Overview

The Mailbox module is a simple APB peripheral that allows CPU and MCU core to communicate with each other by writing operation to generate interrupt. The registers are accessible via APB interface.

The Mailbox has the following main features:

- Support APB interface
- Support 4 mailbox groups, each group includes one data word, one command word register and one flag bit that can represent one interrupt
- Support interrupts to CPU and MCU core
- Support two type of interrupt: TX done and RX done
- Support two trigger mode for TX done interrupt

19.2 Block Diagram

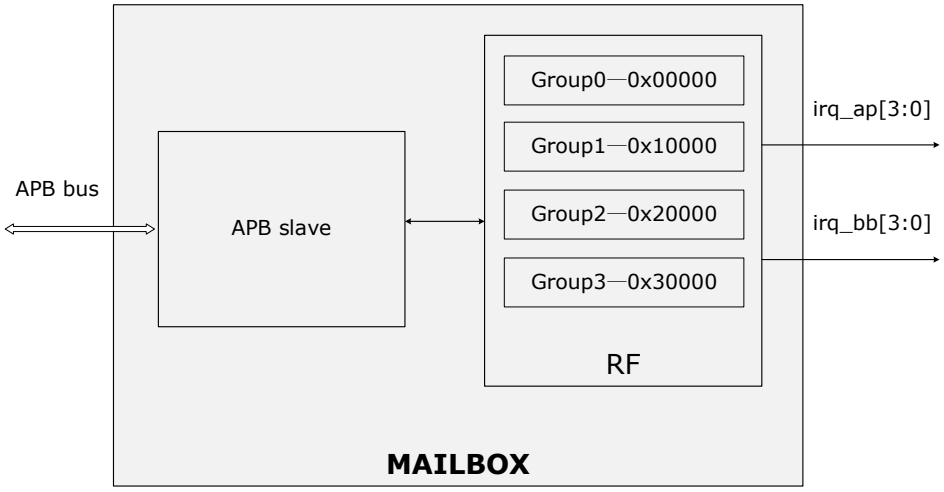

Fig. 19-1 Mailbox Block Diagram

19.3 Function Description

19.3.1 TX Done Interrupt

- Regard CPU as the "AP" side of the Mailbox. The 4 groups TX done interrupt to CPU is:
  - Enabled when MAILBOX_B2A_INTEN.b2a_tx_done_inten is set to 1 and the corresponding IRQs is enabled in GIC.
  - Generated when
    - there are writing operation to corresponding MAILBOX_B2A_CMD_i and MAILBOX_B2A_DAT_i orderly in normal mode.
    - there are writing operation to corresponding MAILBOX_B2A_CMD_i in fast trigger mode.
  - Cleared when writing 1 to corresponding MAILBOX_B2A_STATUS.b2a_tx_done_int.
- Regard MCU core as the "BB" side of the Mailbox. The 4 groups TX done interrupt to MCU core is:
  - Enabled when MAILBOX_A2B_INTEN.a2b_tx_done_inten is set to 1 and the corresponding IRQs is enabled in LP_MCU or the INTC of HP_MCU.
  - Generated when
    - there are writing operation to corresponding MAILBOX_A2B_CMD_i and MAILBOX_A2B_DAT_i orderly.
    - there are writing operation to corresponding MAILBOX_A2B_CMD_i in fast trigger mode.
  - Cleared when writing 1 to corresponding MAILBOX_A2B_STATUS.a2b_tx_done_int.

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19.3.2 RX Done Interrupt

- Regard CPU as the "AP" side of the Mailbox. The 4 groups RX done interrupt to CPU is:
  - Enabled when MAILBOX_B2A_INTEN.b2a_rx_done_inten is set to 1 and the corresponding IRQs is enabled in GIC.
  - Generated when "BB" side clear the corresponding TX done interrupt by write 1 to MAILBOX_A2B_STATUS.a2b_tx_done_int.
  - Cleared when writing 1 to the corresponding MAILBOX_B2A_STATUS.b2a_rx_done_int.
- Regard MCU core as the "BB" side of the Mailbox. The 4 groups RX done interrupt to MCU core is:
  - Enabled when MAILBOX_A2B_INTEN.a2b_rx_done_inten is set to 1 and the corresponding IRQs is enabled in LP_MCU or the INTC of HP_MCU.
  - Generated when "AP" side clear the corresponding TX done interrupt by write 1 to MAILBOX_B2A_STATUS.b2a_tx_done_int.
  - Cleared when writing 1 to the corresponding MAILBOX_A2B_STATUS.a2b_rx_done_int.

- You can also regard CPU as the "BB" side of the Mailbox and regard MCU core as the "AP" side of the Mailbox. The configuration flow is similar.

19.4 Register Description

19.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
HPMCU_MAILBOX	0x20D00000
LPMCU_MAILBOX	0x20500000

19.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
MAILBOX_A2B_INTEN	0x0000	W	0x00000100	AP to BB Interrupt Enable Register for Groupx
MAILBOX_A2B_STATUS	0x0004	W	0x00000000	AP to BB Interrupt Status Register for Groupx
MAILBOX_A2B_CMD	0x0008	W	0x00000000	AP to BB Command x Register
MAILBOX_A2B_DATA	0x000C	W	0x00000000	AP to BB Data x Register
MAILBOX_B2A_INTEN	0x0010	W	0x00000100	BB to AP Interrupt Enable Register for Groupx
MAILBOX_B2A_STATUS	0x0014	W	0x00000000	BB to AP Interrupt Status Register for Groupx
MAILBOX_B2A_CMD	0x0018	W	0x00000000	BB to AP Command x Register
MAILBOX_B2A_DATA	0x001C	W	0x00000000	BB to AP Data x Register

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

19.4.3 Detail Registers Description

MAILBOX_A2B_INTEN

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for low bit 1'b0: Disable 1'b1: Enable
15:9	RO	0x00	reserved
8	RW	0x1	a2b_trig_modex Interrupt trigger mode for groupx a2b int 1'b0: Write CMD then generate interrupt 1'b1: Write CMD firstly, then Write DAT, and then generate interrupt

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Bit	Attr	Reset Value	Description
7:2	RO	0x00	reserved
1	RW	0x0	a2b_rx_done_inten Interrupt enable for a2b rx_done int of groupx. 1'b0: Disable 1'b1: Enable
0	RW	0x0	a2b_tx_done_inten Interrupt enable for a2b tx_done int of groupx. 1'b0: Disable 1'b1: Enable

MAILBOX_A2B_STATUS

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	W1C	0x0	a2b_rx_done_int Interrupt status for a2b rx_done int of groupx. This interrupt will be set when ap clear the b2a_tx_done_int. Clear the interrupt by writing 1 to this bit. 1'b0: Interrupt is inactive 1'b1: Interrupt is active
0	W1C	0x0	a2b_tx_done_int Interrupt status for a2b tx_done int of groupx. This interrupt will be set when ap write to a2b cmd/data. Clear the interrupt by writing 1 to this bit. 1'b0: Interrupt is inactive 1'b1: Interrupt is active

MAILBOX_A2B_CMD

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	command Command x register

MAILBOX_A2B_DATA

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	data Data x register

MAILBOX_B2A_INTEN

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for low bit 1'b0: Disable 1'b1: Enable
15:9	RO	0x00	reserved
8	RW	0x1	b2a_trig_modex Interrupt trigger mode for groupx b2a int 1'b0: Write CMD then generate interrupt 1'b1: Write CMD firstly, then Write DAT, and then generate interrupt
7:2	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x0	b2a_rx_done_inten Interrupt enable for b2a rx_done int of groupx. 1'b0: Disable 1'b1: Enable
0	RW	0x0	b2a_tx_done_inten Interrupt enable for b2a tx_done int of groupx. 1'b0: Disable 1'b1: Enable

MAILBOX_B2A_STATUS
Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	W1C	0x0	b2a_rx_done_int Interrupt status for b2a rx_done int of groupx. This interrupt will be set when bb clear the a2b_tx_done_int. Clear the interrupt by writing 1 to this bit. 1'b0: Interrupt is inactive 1'b1: Interrupt is active
0	W1C	0x0	b2a_tx_done_int Interrupt status for b2a tx_done int of groupx. This interrupt will be set when bb write to b2a cmd/data. Clear the interrupt by writing 1 to this bit. 1'b0: Interrupt is inactive 1'b1: Interrupt is active

MAILBOX_B2A_CMD
Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	command Command x register

MAILBOX_B2A_DATA
Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	data Data x register

19.5 Application Notes

- TX done interrupt is usually used to inform the receiver that the CMD and DATA is ready. It supports two trigger mode:

■ Normal mode

1. Configure bit 8 of MAILBOX_*_INTEN to ‘1’(* stands for "A2B" or "B2A")
2. Configure bit 0 of MAILBOX_*_INTEN to ‘1’
3. Write the MAILBOX_*_CMD firstly
4. Then write the MAILBOX_*_DATA
5. And then generate a TX done interrupt

Write to the MAILBOX_*_CMD register before writing to the MAILBOX_*_DATA register. If wrong order is used, then the interrupt cannot be generated successfully.

■ Fast trigger mode

1. Configure bit 8 of MAILBOX_*_INTEN to ‘0’
2. Configure bit 0 of MAILBOX_*_INTEN to ‘1’

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3. Write the MAILBOX_*_CMD
4. And then generate a TX done interrupt

- If you want to clear the interrupt, you can read out the MAILBOX_*_STATUS register and writing 1 to corresponding bit.

- RX done interrupt is usually used to inform the sender that the receiver has read out the CMD and DATA. It is triggered when the receiver has cleared the corresponding TX done interrupt:

- AP to BB (assume TX done interrupt is set to normal mode)

1. AP configure bit 1 of MAILBOX_B2A_INTEN to '1'
2. BB configure bit 8 of MAILBOX_A2B_INTEN to '1'
3. BB configure bit 0 of MAILBOX_A2B_INTEN to '1'
4. AP write the MAILBOX_A2B_CMD
5. AP write the MAILBOX_A2B_DATA
6. Bit 0 of MAILBOX_A2B_STATUS is automatically set to '1' and TX done interrupt to BB is generated
7. BB receive the TX done interrupt and read out the message
8. BB write '1' to bit 0 of MAILBOX_A2B_STATUS
9. And then bit 1 of MAILBOX_B2A_STATUS is automatically set to '1' and RX done interrupt to AP is generated
10. AP receive the RX done interrupt which indicate BB has read out the message
11. AP write '1' to bit 1 of MAILBOX_B2A_STATUS
12. AP can start a new transfer

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Chapter 20 SARADC

20.1 Overview

This is an 8-channel, 13-bit analog-to-digital converter (ADC) designed using the TSMC 22nm ULP process. The device is powered by dual supply voltages of 1.8V/0.9V and supports a maximum conversion rate of 2 MS/s. It features an 8-to-1 analog input and a 13-bit successive approximation ADC, complete with an onboard clock generator and a digital interface with level shifting. It converts analog input signals into 13-bit digital output codes. The input range is 0 to 1.8V.

SARADC controller supports the following features:

- Support single mode and series conversion mode
- In single mode, the conversion operates once each software is accessed
- In series conversion, the controller samples each channel then loops until the software stops conversion
- High/low threshold can be set, higher/lower/between high-low-threshold interrupt can be enabled
- Support APB master interface to record the ADC conversion result code
- Support to calculate the conversion results for a configurable number of times to obtain a more accurate code

20.2 Block Diagram

SARADC block is shown in Figure below. This includes:

- APB Interface
- Control FSM
- SARADC PHY

The software can configure the SARADC controller by APB interface, then the inter FSM will communicate with SARADC PHY for limited timing requests.

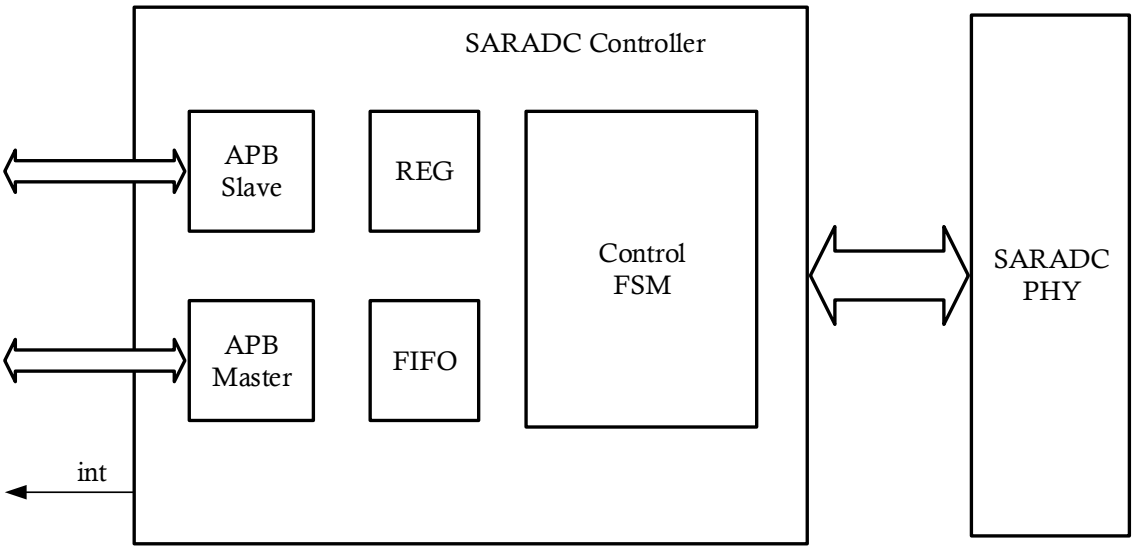

Fig. 20-1 SARADC Block Diagram

20.3 Function Description

SARADC block includes controller and PHY, user cannot directly access SARADC PHY. Software access the SARADC through SARADC controller by APB interface. SARADC controller will sample the conversion result from SARADC PHY.
If the APB master interface is configured enabled, the SARADC could write the conversion result code to the SRAM memory, and the SRAM base address is also configurable.

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20.4 Register Description

20.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
SARADC0	0x21F10000
SARADC1	0x21CB0000
SARADC2	0x21CC0000

20.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SARADC_CONV_CON	0x0000	W	0x00000000	Conversion control
SARADC_T_PD_SOC	0x0004	W	0x00000013	Timing control for PD to SOC
SARADC_T_AS_SOC	0x0008	W	0x00000001	Timing control for assert SOC
SARADC_T_DAS_SOC	0x000C	W	0x00000007	Timing control from dis-assert SOC to change channel
SARADC_T_SEL_SOC	0x0010	W	0x00000003	Timing control from change channel select to assert SOC
SARADC_HIGH_COMP0	0x0014	W	0x00000000	High threshold for ADC output data
SARADC_HIGH_COMP1	0x0018	W	0x00000000	High threshold for ADC output data
SARADC_HIGH_COMP2	0x001C	W	0x00000000	High threshold for ADC output data
SARADC_HIGH_COMP3	0x0020	W	0x00000000	High threshold for ADC output data
SARADC_HIGH_COMP4	0x0024	W	0x00000000	High threshold for ADC output data
SARADC_HIGH_COMP5	0x0028	W	0x00000000	High threshold for ADC output data
SARADC_HIGH_COMP6	0x002C	W	0x00000000	High threshold for ADC output data
SARADC_HIGH_COMP7	0x0030	W	0x00000000	High threshold for ADC output data
SARADC_LOW_COMP0	0x0054	W	0x00000000	Low threshold for ADC output data
SARADC_LOW_COMP1	0x0058	W	0x00000000	Low threshold for ADC output data
SARADC_LOW_COMP2	0x005C	W	0x00000000	Low threshold for ADC output data
SARADC_LOW_COMP3	0x0060	W	0x00000000	Low threshold for ADC output data
SARADC_LOW_COMP4	0x0064	W	0x00000000	Low threshold for ADC output data
SARADC_LOW_COMP5	0x0068	W	0x00000000	Low threshold for ADC output data
SARADC_LOW_COMP6	0x006C	W	0x00000000	Low threshold for ADC output data
SARADC_LOW_COMP7	0x0070	W	0x00000000	Low threshold for ADC output data
SARADC_DEBOUNCE	0x0094	W	0x00000003	Threshold debounce
SARADC_HT_INT_EN	0x0098	W	0x00000000	High threshold interrupt enable
SARADC_LT_INT_EN	0x009C	W	0x00000000	Low threshold interrupt enable

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Name	Offset	Size	Reset Value	Description
SARADC_MT_INT_EN	0x0100	W	0x00000000	Middle threshold interrupt enable
SARADC_END_INT_EN	0x0104	W	0x00000000	End conversion interrupt enable
SARADC_STATUS	0x010C	W	0x00000002	ADC status
SARADC_END_INT_ST	0x0110	W	0x00000000	End conversion interrupt state
SARADC_HT_INT_ST	0x0114	W	0x00000000	High threshold interrupt state
SARADC_LT_INT_ST	0x0118	W	0x00000000	Low threshold interrupt state
SARADC_MT_INT_ST	0x011C	W	0x00000000	Middle threshold interrupt state
SARADC_DATA0	0x0120	W	0x00000000	ADC output data
SARADC_DATA1	0x0124	W	0x00000000	ADC output data
SARADC_DATA2	0x0128	W	0x00000000	ADC output data
SARADC_DATA3	0x012C	W	0x00000000	ADC output data
SARADC_DATA4	0x0130	W	0x00000000	ADC output data
SARADC_DATA5	0x0134	W	0x00000000	ADC output data
SARADC_DATA6	0x0138	W	0x00000000	ADC output data
SARADC_DATA7	0x013C	W	0x00000000	ADC output data
SARADC_AUTO_CH_EN	0x0160	W	0x00000000	Channel enable in auto channel mode
SARADC_AVG_TIME_CH0	0x0164	W	0x00000000	Average for ADC result
SARADC_AVG_TIME_CH1	0x0168	W	0x00000000	Average for ADC result
SARADC_AVG_TIME_CH2	0x016C	W	0x00000000	Average for ADC result
SARADC_AVG_TIME_CH3	0x0170	W	0x00000000	Average for ADC result
SARADC_AVG_TIME_CH4	0x0174	W	0x00000000	Average for ADC result
SARADC_AVG_TIME_CH5	0x0178	W	0x00000000	Average for ADC result
SARADC_AVG_TIME_CH6	0x017C	W	0x00000000	Average for ADC result
SARADC_AVG_TIME_CH7	0x0180	W	0x00000000	Average for ADC result
SARADC_ROUND_MAX	0x0184	W	0x00000005	Round interrupt counter number
SARADC_TIMEOUT_T	0x0188	W	0x00000006	FIFO full interrupt counter number
SARADC_FIFO_CON	0x018C	W	0x00000000	FIFO configuration register
SARADC_PADDR_BASE_H	0x0190	W	0x00000000	APB interface base address
SARADC_PADDR_BASE_L	0x0194	W	0x00000000	APB interface base address
SARADC_PADDR_OFFSET_MAX	0x0198	W	0x00000111	APB interface max offset address
SARADC_PADDR_OFFSET_WK	0x0200	W	0x00000110	APB interface watermark address

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

20.4.3 Detail Registers Description

SARADC_CONV_CON

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
10	RW	0x0	pu_he_mode This bit is power up high efficiency mode. The SARADC PHY will be powered up continuously when this bit is asserted. 1'b0: Disable 1'b1: Enable
9	RW	0x0	int_lock This is used to lock the sample data when interrupt happened. 1'b0: Disable lock 1'b1: Enable lock
8	RW	0x0	as_pd_mode If this bit is set to 1'b1, each time conversion ends, PD will be asserts. Then next time conversion starts, PD will be set to low auto automatically. This is not used in signal mode.
7	W1C	0x0	end_conv End conversion, this is not used when CONV_CON[5] is set to 1'b1. If this bit set to 1'b1, PD will set to 1'b1 after the last conversion and this bit will be cleared to 1'b0.
6	RW	0x0	auto_channel_mode Auto channel mode. If this is enable, channel will be round auto according which is set in AUTO_CH_EN.
5	RW	0x0	single_pd_mode Single conversion mode. If this bit is set to 1, conversion only operate once, then PD single will be set to 1.
4	W1C	0x0	start_adc Enable ADC, if this bit set to one, conversion will start. Then this bit will be clear to 0.
3:0	RW	0x0	channel_sel Channel for SARADC, 16 channel is supported. This field is not used when CONV_CON[6] is set to 1. 4'd0: select channel 0 4'd1: select channel 1 4'd2: select channel 2 4'd3: select channel 3 4'd4: select channel 4 4'd5: select channel 5 4'd6: select channel 6 4'd7: select channel 7

SARADC_T_PD_SOC

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000013	t_pd_soc Timing control between power up to start-of-conversion.

SARADC_T_AS_SOC

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000001	t_as_soc Timing control for assert SOC signal.

SARADC_T_DAS_SOC

Address: **Operational Base** + offset (0x000C)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000007	t_das_soc Timing from dis-assert SOC to channel select change.

SARADC_T_SEL_SOC

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0003	t_sel_soc Timing from channel load to SOC assert.

SARADC_HIGH_COMP0

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	high_comp0 High threshold for ADC output data for channel 0.

SARADC_HIGH_COMP1

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	high_comp1 High threshold for ADC output data for channel 1.

SARADC_HIGH_COMP2

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	high_comp2 High threshold for ADC output data for channel 2.

SARADC_HIGH_COMP3

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	high_comp3 High threshold for ADC output data for channel 3.

SARADC_HIGH_COMP4

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	high_comp4 High threshold for ADC output data for channel 4.

SARADC_HIGH_COMP5

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	high_comp5 High threshold for ADC output data for channel 5.

SARADC_HIGH_COMP6

Address: **Operational Base** + offset (0x002C)

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Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	high_comp6 High threshold for ADC output data for channel 6.

SARADC_HIGH_COMP7

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	high_comp7 High threshold for ADC output data for channel 7.

SARADC_LOW_COMP0

Address: **Operational Base** + offset (0x0054)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	low_comp0 Low threshold for ADC output data for channel 0.

SARADC_LOW_COMP1

Address: **Operational Base** + offset (0x0058)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	low_comp1 Low threshold for ADC output data for channel 1.

SARADC_LOW_COMP2

Address: **Operational Base** + offset (0x005C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	low_comp2 Low threshold for ADC output data for channel 2.

SARADC_LOW_COMP3

Address: **Operational Base** + offset (0x0060)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	low_comp3 Low threshold for ADC output data for channel 3.

SARADC_LOW_COMP4

Address: **Operational Base** + offset (0x0064)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	low_comp4 Low threshold for ADC output data for channel 4.

SARADC_LOW_COMP5

Address: **Operational Base** + offset (0x0068)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	low_comp5 Low threshold for ADC output data for channel 5.

SARADC_LOW_COMP6

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Address: **Operational Base** + offset (0x006C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	low_comp6 Low threshold for ADC output data for channel 6.

SARADC_LOW_COMP7

Address: **Operational Base** + offset (0x0070)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	low_comp7 Low threshold for ADC output data for channel 7.

SARADC_DEBOUNCE

Address: **Operational Base** + offset (0x0094)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x03	debounce ADC controller will only generate interrupt data is higher/lower/between setting threshold for "debounce" times.

SARADC_HT_INT_EN

Address: **Operational Base** + offset (0x0098)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	ht_int_en7 High threshold interrupt for channel7. 1'b0: Disable interrupt. 1'b1: Enable interrupt.t.
6	RW	0x0	ht_int_en6 High threshold interrupt for channel6. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
5	RW	0x0	ht_int_en5 High threshold interrupt for channel5. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
4	RW	0x0	ht_int_en4 High threshold interrupt for channel4. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
3	RW	0x0	ht_int_en3 High threshold interrupt for channel3. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
2	RW	0x0	ht_int_en2 High threshold interrupt for channel2. 1'b0: Disable interrupt. 1'b1: Enable interrupt.

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Bit	Attr	Reset Value	Description
1	RW	0x0	ht_int_en1 High threshold interrupt for channel1. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
0	RW	0x0	ht_int_en0 High threshold interrupt for channel0. 1'b0: Disable interrupt. 1'b1: Enable interrupt.

SARADC_LT_INT_EN

Address: **Operational Base** + offset (0x009C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	lt_int_en7 Low threshold interrupt for channel7. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
6	RW	0x0	lt_int_en6 Low threshold interrupt for channel6. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
5	RW	0x0	lt_int_en5 Low threshold interrupt for channel5. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
4	RW	0x0	lt_int_en4 Low threshold interrupt for channel4. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
3	RW	0x0	lt_int_en3 Low threshold interrupt for channel3. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
2	RW	0x0	lt_int_en2 Low threshold interrupt for channel2. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
1	RW	0x0	lt_int_en1 Low threshold interrupt for channel1. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
0	RW	0x0	lt_int_en0 Low threshold interrupt for channel0. 1'b0: Disable interrupt. 1'b1: Enable interrupt.

SARADC_MT_INT_EN

Address: **Operational Base** + offset (0x0100)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	mt_int_en7 Middle threshold interrupt for channel7. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
6	RW	0x0	mt_int_en6 Middle threshold interrupt for channel6. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
5	RW	0x0	mt_int_en5 Middle threshold interrupt for channel5. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
4	RW	0x0	mt_int_en4 Middle threshold interrupt for channel4. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
3	RW	0x0	mt_int_en3 Middle threshold interrupt for channel3. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
2	RW	0x0	mt_int_en2 Middle threshold interrupt for channel2. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
1	RW	0x0	mt_int_en1 Middle threshold interrupt for channel1. 1'b0: Disable interrupt. 1'b1: Enable interrupt.
0	RW	0x0	mt_int_en0 Middle threshold interrupt for channel0. 1'b0: Disable interrupt. 1'b1: Enable interrupt.

SARADC_END_INT_EN

Address: **Operational Base** + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	wr_err_en This enables a interrupt when APB master error. 1'b0: Disable 1'b1: Enabler
4	RW	0x0	paddr_watermark_int_en This enables a interrupt when APB master address meet watermark address. 1'b0: Disable 1'b1: Enabler

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Bit	Attr	Reset Value	Description
3	RW	0x0	paddr_max_int_en This enables a interrupt when APB master address meet max address. 1'b0: Disable 1'b1: Enabler
2	RW	0x0	timeout_int_en If APB Mater cannot write for long time, an interrupt can set. 1'b0: Disable 1'b1: Enabler
1	RW	0x0	round_int_en Some round for all channel done, an interrupt can be set. 1'b0: Disable 1'b1: Enabler
0	RW	0x0	end_int_en End of conversion interrupt. 1'b0: Disable end conversion interrupt. 1'b1: Enable end conversion interrupt.

SARADC_STATUS

Address: **Operational Base** + offset (0x010C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:2	RO	0x0	sel ADC channel select.
1	RO	0x1	pd 1'b1: ADC is power down. 1'b0: ADC is power up and in conversion.
0	RO	0x0	conv_st Conversion status 1'b1: ADC controller FSM is busy. 1'b0: ADC controller FSM is idle.

SARADC_END_INT_ST

Address: **Operational Base** + offset (0x0110)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	wr_err_st ADC APB master error status. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
4	RW	0x0	paddr_watermark_int_st ADC APB master meet watermark address status. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
3	RW	0x0	paddr_max_int_st ADC APB master meet max address status. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
2	RW	0x0	timeout_int_st ADC APB master write timeout interrupt status. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.

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Bit	Attr	Reset Value	Description
1	RW	0x0	roun_int_st ADC all channel end conversion interrupt status. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
0	W1C	0x0	end_int_st ADC end conversion interrupt status. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.

SARADC_HT_INT_ST

Address: **Operational Base** + offset (0x0114)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	W1C	0x0	ht_int_st7 High threshold interrupt state for channel7. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
6	W1C	0x0	ht_int_st6 High threshold interrupt state for channel6. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
5	W1C	0x0	ht_int_st5 High threshold interrupt state for channel5. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
4	W1C	0x0	ht_int_st4 High threshold interrupt state for channel4. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
3	W1C	0x0	ht_int_st3 High threshold interrupt state for channel3. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
2	W1C	0x0	ht_int_st2 High threshold interrupt state for channel2. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
1	W1C	0x0	ht_int_st1 High threshold interrupt state for channel1. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
0	W1C	0x0	ht_int_st0 High threshold interrupt state for channel0. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.

SARADC_LT_INT_ST

Address: **Operational Base** + offset (0x0118)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	W1C	0x0	lt_int_st7 Low threshold interrupt state for channel7. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.

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Bit	Attr	Reset Value	Description
6	W1C	0x0	lt_int_st6 Low threshold interrupt state for channel6. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
5	W1C	0x0	lt_int_st5 Low threshold interrupt state for channel5. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
4	W1C	0x0	lt_int_st4 Low threshold interrupt state for channel4. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
3	W1C	0x0	lt_int_st3 Low threshold interrupt state for channel3. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
2	W1C	0x0	lt_int_st2 Low threshold interrupt state for channel2. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
1	W1C	0x0	lt_int_st1 Low threshold interrupt state for channel1. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
0	W1C	0x0	lt_int_st0 Low threshold interrupt state for channel0. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.

SARADC_MT_INT_ST

Address: **Operational Base** + offset (0x011C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	W1C	0x0	mt_int_st7 Between high and low threshold interrupt state for channel7. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
6	W1C	0x0	mt_int_st6 Between high and low threshold interrupt state for channel6. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
5	W1C	0x0	mt_int_st5 Between high and low threshold interrupt state for channel5. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
4	W1C	0x0	mt_int_st4 Between high and low threshold interrupt state for channel4. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
3	W1C	0x0	mt_int_st3 Between high and low threshold interrupt state for channel3. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.

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Bit	Attr	Reset Value	Description
2	W1C	0x0	mt_int_st2 Between high and low threshold interrupt state for channel2. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
1	W1C	0x0	mt_int_st1 Between high and low threshold interrupt state for channel1. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.
0	W1C	0x0	mt_int_st0 Between high and low threshold interrupt state for channel0. 1'b0: Interrupt not happened. 1'b1: Interrupt happened.

SARADC_DATA0

Address: **Operational Base** + offset (0x0120)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RO	0x0000	data0 ADC channel 0 data.

SARADC_DATA1

Address: **Operational Base** + offset (0x0124)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RO	0x0000	data1 ADC channel 1 data.

SARADC_DATA2

Address: **Operational Base** + offset (0x0128)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RO	0x0000	data2 ADC channel 2 data.

SARADC_DATA3

Address: **Operational Base** + offset (0x012C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RO	0x0000	data3 ADC channel 3 data.

SARADC_DATA4

Address: **Operational Base** + offset (0x0130)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RO	0x0000	data4 ADC channel 4 data.

SARADC_DATA5

Address: **Operational Base** + offset (0x0134)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RO	0x0000	data5 ADC channel 5 data.

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SARADC_DATA6

Address: **Operational Base** + offset (0x0138)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RO	0x0000	data6 ADC channel 6 data.

SARADC_DATA7

Address: **Operational Base** + offset (0x013C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RO	0x0000	data7 ADC channel 7 data.

SARADC_AUTO_CH_EN

Address: **Operational Base** + offset (0x0160)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	auto_ch_en Enable channel in auto channel mode. Each bit can enable for one channel.

SARADC_AVG_TIME_CH0

Address: **Operational Base** + offset (0x0164)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	avg_time_ch0 The times for ADC output which will be add and get average value. 8'h0: No average 8'h1: 2 times 8'h3: 4 times 8'h7: 8 times 8'h15: 16 times 8'h31: 32 times 8'h63: 64 times 8'h127: 128 times 8'h255: 256 times Other value is not enable.

SARADC_AVG_TIME_CH1

Address: **Operational Base** + offset (0x0168)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	avg_time_ch1 The times for ADC output which will be add and get average value. 8'h0: No average 8'h1: 2 times 8'h3: 4 times 8'h7: 8 times 8'h15: 16 times 8'h31: 32 times 8'h63: 64 times 8'h127: 128 times 8'h255: 256 times Other value is not enable.

SARADC_AVG_TIME_CH2

Address: **Operational Base** + offset (0x016C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	avg_time_ch2 The times for ADC output which will be add and get average value. 8'h0: No average 8'h1: 2 times 8'h3: 4 times 8'h7: 8 times 8'h15: 16 times 8'h31: 32 times 8'h63: 64 times 8'h127: 128 times 8'h255: 256 times Other value is not enable.

SARADC_AVG_TIME_CH3

Address: **Operational Base** + offset (0x0170)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	avg_time_ch3 The times for ADC output which will be add and get average value. 8'h0: No average 8'h1: 2 times 8'h3: 4 times 8'h7: 8 times 8'h15: 16 times 8'h31: 32 times 8'h63: 64 times 8'h127: 128 times 8'h255: 256 times Other value is not enable.

SARADC_AVG_TIME_CH4

Address: **Operational Base** + offset (0x0174)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	avg_time_ch4 The times for ADC output which will be add and get average value. 8'h0: No average 8'h1: 2 times 8'h3: 4 times 8'h7: 8 times 8'h15: 16 times 8'h31: 32 times 8'h63: 64 times 8'h127: 128 times 8'h255: 256 times Other value is not enable.

SARADC_AVG_TIME_CH5

Address: **Operational Base** + offset (0x0178)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	avg_time_ch5 The times for ADC output which will be add and get average value. 8'h0: No average 8'h1: 2 times 8'h3: 4 times 8'h7: 8 times 8'h15: 16 times 8'h31: 32 times 8'h63: 64 times 8'h127: 128 times 8'h255: 256 times Other value is not enable.

SARADC_AVG_TIME_CH6

Address: **Operational Base** + offset (0x017C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	avg_time_ch6 The times for ADC output which will be add and get average value. 8'h0: No average 8'h1: 2 times 8'h3: 4 times 8'h7: 8 times 8'h15: 16 times 8'h31: 32 times 8'h63: 64 times 8'h127: 128 times 8'h255: 256 times Other value is not enable.

SARADC_AVG_TIME_CH7

Address: **Operational Base** + offset (0x0180)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	avg_time_ch7 The times for ADC output which will be add and get average value. 8'h0: No average 8'h1: 2 times 8'h3: 4 times 8'h7: 8 times 8'h15: 16 times 8'h31: 32 times 8'h63: 64 times 8'h127: 128 times 8'h255: 256 times Other value is not enable.

SARADC_ROUND_MAX

Address: **Operational Base** + offset (0x0184)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x005	round_max This use for round_interrupt. If enable round_interrupt, all channel done once, a counter will add. If the counter meets the max value, a interrupt will be generate.

SARADC_TIMEOUT_T

Address: **Operational Base** + offset (0x0188)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x006	fifo_timeout_t This used for timeout interrupt. If FIFO is full and APB master can not write, one conversion end and a counter will add. If counter meet this value, an interrupt will generate.

SARADC_FIFO_CON

Address: **Operational Base** + offset (0x018C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	W1C	0x0	fifo_clr Clear FIFO.
3	RW	0x0	pmaster_en Enanle APB master.
2	RW	0x0	fifo_ch_en This enable channel number addr to the bit[31:28] in pwdata.
1	RW	0x0	full_lock_en This bit used for FIFO full. When this set, new conversion data will be abandon when FIFO is full and the channel number before full will be recorded. If FIFO have space, when channel meet the channel order, the data will be push to FIFO.

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Bit	Attr	Reset Value	Description
0	RW	0x0	fifo_cover_en This bit used for FIFO full. When this set, new conversion data will be abandon when FIFO is full. If FOFO have space, the ADC latest data will be pushed to FIFO. So the channel in FIFO is not sort.

SARADC_PADDR_BASE_H

Address: **Operational Base** + offset (0x0190)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	paddr_base_h Paddr address[39:34].

SARADC_PADDR_BASE_L

Address: **Operational Base** + offset (0x0194)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	paddr_base_l Paddr address[33:2].

SARADC_PADDR_OFFSET_MAX

Address: **Operational Base** + offset (0x0198)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0111	paddr_offset_max Max word for APB address space.

SARADC_PADDR_OFFSET_WK

Address: **Operational Base** + offset (0x0200)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0110	paddr_offset_watermark WaterMark for APB word address.

20.5 Application Notes

20.5.1 Series Conversion Mode

Steps of ADC conversion in series conversion mode:

- Decide which channel should be used and whether auto_channel mode should be set. In auto_channel mode, the channel will be changed from 0-3 then to 0. Please refer to the SARADC_CONV_CON register.
- Set SARADC_CONV_CON[4] to 1'b1, then the conversion will start.
- If conversion wants to be ended, set SARADC_CONV_CON[7] to 1'b1.
- Conversion could be read from SARADC_DATAn (n is from 0-3).
- If threshold compare interrupt wants to be used, high/low threshold could be set, and interrupt should be set as an application.
- If auto_channel mode is not set, you could set the channel as an application.

20.5.2 Single Mode

Steps of ADC conversion in single mode:

- Decide which channel should be used and set SARADC_CONV_CON[3:0].
- Set SARADC_CONV_CON[5] to 1'b1.
- Set SARADC_CONV_CON[4] to 1'b1, then the conversion will start.
- The conversion only operates once then ends. PD will be asserted and PD status could be got by reading SARADC_STATUS.

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- Conversion could be read from SARADC_DATAn (n is from 0-3).

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Chapter 21 Temperature-Sensor ADC (TSADC)

21.1 Overview

TSADC controller is used to control and get the temperature information. TSADC will convert for each enabled channel in loop after the initial setting and can be stopped by software. If you find that the temperature is high in a period of time, an interrupt is generated to the processor down-measures taken; if the temperature over a period of time High, the resulting TSHUT gave CRU module, let it reset the entire chip, or via GPIO give PMIC. Also, if you find that the temperature low in a period of time, an interrupt can be generated.

TSADC controller supports the following features:
- The temperature for high and low interrupt can be configured
- The temperature of system reset can be configured
- The time interval of temperature detection can be configured
- When detecting a high temperature, the time interval of temperature detection can be configured
- High temperature debounce can be configured
- An interrupt can be generated after TSADC converts all setting channel

21.2 Block Diagram

TSADC controller comprises with:
- APB Interface
- TSADC control logic

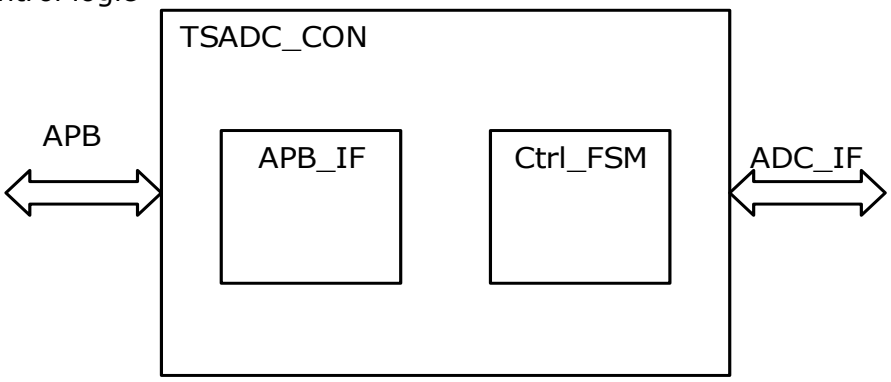

Fig. 21-1 TSADC Controller Block Diagram

21.3 Function Description

21.3.1 APB Interface

There is an APB Slave interface in TSADC controller, which is used to configure the TSADC controller registers and look up the temperature from the temperature sensor.

21.3.2 TSADC Controller

This block is used to control the TSADC PHY to meet the conversion timing and receive the temperature information from TSADC PHY.

21.4 Register Description

21.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
TSADC_USER_CON	0x0000	W	0x00000000	User control
TSADC_AUTO_CON	0x0004	W	0x00000000	Auto control
TSADC_AUTO_STATUS	0x0008	W	0x00000000	Status used in auto mode
TSADC_AUTO_SRC	0x000C	W	0x00000000	Channel select for TSADC in auto mode
TSADC_LT_EN	0x0010	W	0x00000000	Low temperature check logic enable

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Name	Offset	Size	Reset Value	Description
TSADC_HT_INT_EN	0x0014	W	0x00000000	High temperature interrupt enable
TSADC_GPIO_EN	0x0018	W	0x00000000	Temperature violation to GPIO enable
TSADC_CRU_EN	0x001C	W	0x00000000	Temperature violation to cru enable
TSADC_LT_INT_EN	0x0020	W	0x00000000	Low temperature interrupt enable
TSADC_HLT_INT_PD	0x0024	W	0x00000000	High and low temperature interrupt status
TSADC_EOC_HSHUT_PD	0x0028	W	0x00000000	High temperature shut and round interrupt status
TSADC_DATA0	0x002C	W	0x00000000	Channel0 data
TSADC_DATA1	0x0030	W	0x00000000	Channel1 data
TSADC_COMP0_INT	0x006C	W	0x00000000	High temperature interrupt threshold for channel0
TSADC_COMP1_INT	0x0070	W	0x00000000	High temperature interrupt threshold for channel1
TSADC_COMP0_SHUT	0x010C	W	0x00000000	High temperature shut threshold for channel0
TSADC_COMP1_SHUT	0x0110	W	0x00000000	High temperature shut threshold for channel1
TSADC_HIGH_INT_DEBOUNCE	0x014C	W	0x00000003	High interrupt debounce
TSADC_HIGH_TSHUT_DEBOUNCE	0x0150	W	0x00000003	High shut debounce
TSADC_AUTO_PERIOD	0x0154	W	0x00010000	Auto conversion period
TSADC_AUTO_PERIOD_HT	0x0158	W	0x00010000	Auto conversion period for high temperature
TSADC_COMP0_LOW_INT	0x015C	W	0x00000000	Low temperature threshold for channel0
TSADC_COMP1_LOW_INT	0x0160	W	0x00000000	Low temperature threshold for channel1
TSADC_Q_MAX	0x0210	W	0x00000000	Max data used for data inversion

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

21.4.2 Detail Registers Description

TSADC_USER_CON

Address: Operational Base(0x20BB0000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b1: Write access enable 1'b0: Write access disable
15:9	RO	0x00	reserved
8	RO	0x0	adc_status 1'b0: ADC stop 1'b1: Conversion in progress
7	R/WSC	0x0	start When software write 1 to this bit, start-of-conversion will be assert. This bit will be cleared after TSADC access finishing. Only when TSADC_USER_CON[5] = 1'b1, this bit takes effect.

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Bit	Attr	Reset Value	Description
6	RW	0x0	eoc_inten Enable end of conversion interrupt for each conversion. 1'b0 : Disable 1'b1 : Enable
5	RW	0x0	start_mode Start mode. 1'b0: TSADC controller will assert start_of_conversion after power up. 1'b1: The start_of_conversion will be controlled by TSADC_USER_CON[7].
4	RW	0x0	power_control ADC power control 1'b0: Power down 1'b1: Power up This bit is not enable when TSADC_AUTO_CON[0] is set to 1.
3:0	RW	0x0	input_src_sel ADC input source select in user mode. Can be changed from 0 - 15.

TSADC_AUTO_CON

Address: Operational Base(0x20BB0000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b1: Write access enable 1'b0: Write access disable
15:9	RO	0x00	reserved
8	RW	0x0	tshut_polarity This bit is used to control the output signal polarity to gpio when the temperature is higher than threshold. 1'b0: Low active 1'b1: High active
7:3	RO	0x00	reserved
2	RW	0x0	round_int_en Interrupt enable for round model. Used for auto model all channel set is sampled. 1'b1: Enable 1'b0: Disable
1	RW	0x0	q_sel 1'b0: Use tsadc_q as output (positive temperature coefficient) 1'b1: Use (q_max - tsadc_q) as output (negative temperature coefficient)
0	RW	0x0	auto_en Auto conversion enable 1'b0: TSADC controller works at user-define mode 1'b1: TSADC controller works at auto mode

TSADC_AUTO_STATUS

Address: Operational Base(0x20BB0000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
3	RW	0x0	ht_wram High temperature status 1'b0: TSADC data is not higher than the shut temperature 1'b1: TSADC data is higher than the shut temperature
2	RW	0x0	auto_status TSADC auto mode status 1'b0: Auto mode stop 1'b1: Auto mode in progress
1	W1C	0x0	last_tshut_cru Status for cru reset latest temperature shut, write 1 to clear.
0	W1C	0x0	last_tshut_gpio Status for GPIO latest temperature shut, write 1 to clear.

TSADC_AUTO_SRC

Address: Operational Base(0x20BB0000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b1: Write access enable 1'b0: Write access disable
15:0	RW	0x0000	auto_src Enable channel for TSADC in auto mode. Each bit can enable for one channel.

TSADC_LT_EN

Address: Operational Base(0x20BB0000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b1: Write access enable 1'b0: Write access disable
15:0	RW	0x0000	low_temperature_vio_en Low temperature violation logic enable, each bit enables one channel. 1'b1: Enable 1'b0: Disable

TSADC_HT_INT_EN

Address: Operational Base(0x20BB0000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b1: Write access enable 1'b0: Write access disable
15:0	RW	0x0000	high_temperature_int_en High temperature interrupt enable, each bit enables one channel. 1'b1: Enable 1'b0: Disable

TSADC_GPIO_EN

Address: Operational Base(0x20BB0000) + offset (0x0018)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b1: Write access enable 1'b0: Write access disable
15:0	RW	0x0000	gpio_en Temperature violation to GPIO enable, each bit enables one channel. 1'b1: Enable 1'b0: Disable

TSADC_CRU_EN

Address: Operational Base(0x20BB0000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b1: Write access enable 1'b0: Write access disable
15:0	RW	0x0000	cru_en Temperature violation to cru reset enable, each bit enables one channel. 1'b1: Enable 1'b0: Disable

TSADC_LT_INT_EN

Address: Operational Base(0x20BB0000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b1: Write access enable 1'b0: Write access disable
15:0	RW	0x0000	low_tempeture_int_en Low temperature interrupt enable, each bit enables one channel. 1'b1: Enable 1'b0: Disable

TSADC_HLT_INT_PD

Address: Operational Base(0x20BB0000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	W1C	0x0000	lt_int_status Low temperature interrupt status for each channel.
15:0	W1C	0x0000	ht_int_status High temperature interrupt status for each channel.

TSADC_EOC_HSHUT_PD

Address: Operational Base(0x20BB0000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	W1C	0x0	round_int_pd Auto model interrupt for each round of all set channel.
16	W1C	0x0	usr_eoc_irq_pd User model end interrupt status.
15:0	W1C	0x0000	ht_shut_pd High temperature shut down status for each channel.

TSADC_DATA0

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Address: Operational Base(0x20BB0000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RO	0x00000	adc_data A/D value of the channel 0 last conversion.

TSADC_DATA1

Address: Operational Base(0x20BB0000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RO	0x00000	adc_data A/D value of the channel 1 last conversion.

TSADC_COMP0_INT

Address: Operational Base(0x20BB0000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RW	0x00000	tsadc_h_int_comp_src0 TSADC high temperature level. TSADC output is bigger than or equal to tsadc_comp, means the temperature is high. TSADC_INT will be valid.

TSADC_COMP1_INT

Address: Operational Base(0x20BB0000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RW	0x00000	tsadc_h_int_comp_src1 TSADC high temperature level. TSADC output is bigger than or equal to tsadc_comp, means the temperature is high. TSADC_INT will be valid.

TSADC_COMP0_SHUT

Address: Operational Base(0x20BB0000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RW	0x00000	tsadc_shut_comp_src0 TSADC high temperature level. TSADC output is bigger than or equal to tsadc_comp, means the temperature is too high. TSHUT will be valid.

TSADC_COMP1_SHUT

Address: Operational Base(0x20BB0000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RW	0x00000	tsadc_shut_comp_src1 TSADC high temperature level. TSADC output is bigger than or equal to tsadc_comp, means the temperature is too high. TSHUT will be valid.

TSADC_HIGH_INT_DEBOUNCE

Address: Operational Base(0x20BB0000) + offset (0x014C)

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Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x03	debounce TSADC controller will only generate interrupt when temperature is higher than or equal to COMP_INT for "debounce" times.

TSADC_HIGH_TSHUT_DEBOUNCE

Address: Operational Base(0x20BB0000) + offset (0x0150)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x03	debounce TSADC controller will only generate TSHUT when temperature is higher than or equal to COMP_SHUT for "debounce" times.

TSADC_AUTO_PERIOD

Address: Operational Base(0x20BB0000) + offset (0x0154)

Bit	Attr	Reset Value	Description
31:0	RW	0x00010000	auto_period When auto mode is enabled, this register controls the interleave between every conversion for all channel enabled of TSADC.

TSADC_AUTO_PERIOD_HT

Address: Operational Base(0x20BB0000) + offset (0x0158)

Bit	Attr	Reset Value	Description
31:0	RW	0x00010000	auto_period This register controls the interleave between every conversion for all channel enabled of TSADC after the temperature is higher than COMP_SHUT or COMP_INT.

TSADC_COMP0_LOW_INT

Address: Operational Base(0x20BB0000) + offset (0x015C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RW	0x00000	tsadc_l_int_comp_src0 TSADC low temperature level. TSADC output is lower than tsadc_comp, means the temperature is low. TSADC_LOW_INT will be valid.

TSADC_COMP1_LOW_INT

Address: Operational Base(0x20BB0000) + offset (0x0160)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RW	0x00000	tsadc_l_int_comp_src1 TSADC low temperature level. TSADC output is lower than tsadc_comp, means the temperature is low. TSADC_LOW_INT will be valid.

TSADC_Q_MAX

Address: Operational Base(0x20BB0000) + offset (0x0210)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:0	RW	0x00000	q_max This register used for TSADC_AUTO_CON[1] for conversion output data.

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21.5 Interface Description

Table 21-1 TSADC Rockchip Matrix IO Interface Description

Module Pin	Dir	Pad Name	IOMUX Setting
IOMUX0			
tsadc_tshut	O	FSPI1_D3_M0/PWM1_CH1_M0/TSADC_SHUT/TSADC_SHUTORG/GPIO0_A1	GPIO0A_IOMUX_SEL_0[7:4]=3
tsadc_tshutorg		FSPI1_D3_M0/PWM1_CH1_M0/TSADC_SHUT/TSADC_SHUTORG/GPIO0_A1	GPIO0A_IOMUX_SEL_0[7:4]=4

Notes: I=input, O=output, I/O=input/output. For the configuration of RM_IO, please refer to chapter "Rockchip Matrix IO".

21.6 Application Notes

21.6.1 Conversion Flow

The system works as follows:

1) Temperature violation and other configurations may be set.
2) Select TSADC channel 0.
3) Set the bit[0] in register TSADC_AUTO_CON, then TSADC will work.
4) Then temperature information can be read from the APB interface.
5) If TSADC needs to be closed, set bit[0] in register TSADC_AUTO_CON to 1'b0.
6) The temperature equals to the reading code divided by 100.

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Chapter 22 SPINLOCK

22.1 Overview

The hardware spinlock is used for spinlock status storage. All the CPU can access spinlock to get the lock status.

22.2 Block Diagram

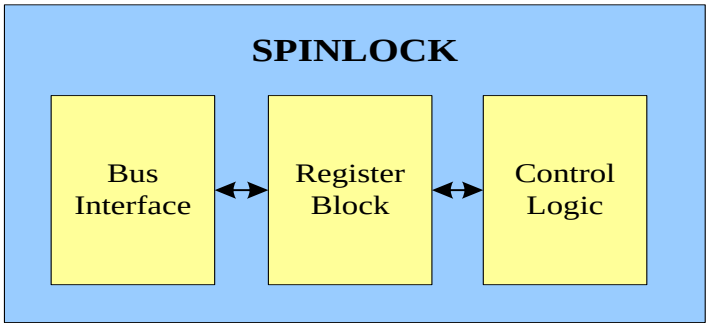

Fig. 22-1 Spinlock Block Diagram

- Bus Interface

The Bus Interface implements the bus slave operation.

- Register Block

The Register block includes the lock status registers.

- Control Logic

The control logic implemented the spinlock function.

22.3 Function Description

The SPINLOCK includes 64 lock-status register groups. Each lock-status register has 4bits, which corresponding to the lock status.
When 4bits spinlock_status is not zero, this lock-status register cannot be written.
When write data is 4'h0, 4bits spinlock_status registers clean to all zero.
If write data is 4'h0, that means unlock process.
If write data is 4bits ID, that means lock process. If read back value is equal to write data ID, that means lock successfully.

22.4 Register Description

22.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

22.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SPINLOCK_status_n (range of n is 0~63)	0x0+4*n	W	0x00000000	Spinlock Status Controller Register_n

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access

22.4.3 Detail Register Description

SPINLOCK_status_n

Address: Operational Base(0x21210000) + offset (0x0000+4*n)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved reserved

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	spinlock_status When 4bits is 0, 4bits can be written with new value. When 4bits is not 0, 4bits cannot be written. When write data is 4'h0, 4bits clean to 0.

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Chapter 23 IO Controller (IOC)

23.1 Overview

The IO Controller (IOC) will be used by the software to do some static settings related to IOs.

23.2 Function Description

The functions of the IO Controller (IOC) are as follows:

- GPIO IOMUX control
- GPIO PAD pull-up/pull-down, drive strength, power supply voltage and other configurations

Table 23-1 GRF Adress Mapping Table

No	Name	Address Base
1	GPIO0_IOC	0X201A0000
2	GPIO1_IOC	0X201B0000
3	GPIO2_IOC	0X201B8000
4	GPIO3_IOC	0X201C0000
5	GPIO4_IOC	0X201C8000
6	GPIO5_IOC	0X201D0000
7	GPIO6_IOC	0X201D8000
8	GPIO7_IOC	0x201E0000

23.3 GPIO0_IOC Register Description

23.3.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

23.3.2 Registers Summary

Name	Offset	Size	Reset Value	Description
GPIO0_IOC_GPIO0A_IOMUX_SEL_0	0x0000	W	0x00000030	GPIO0A IOMUX Select Register 0
GPIO0_IOC_GPIO0A_IOMUX_SEL_1	0x0004	W	0x00000000	GPIO0A IOMUX Select Register 1
GPIO0_IOC_GPIO0B_IOMUX_SEL_0	0x0008	W	0x00000000	GPIO0B IOMUX Select Register 0
GPIO0_IOC_GPIO0B_IOMUX_SEL_1	0x000C	W	0x00000000	GPIO0B IOMUX Select Register 1
GPIO0_IOC_GPIO0C_IOMUX_SEL_0	0x8010	W	0x00000000	GPIO0C IOMUX Select Register 0
GPIO0_IOC_GPIO0C_IOMUX_SEL_1	0x8014	W	0x00000000	GPIO0C IOMUX Select Register 1
GPIO0_IOC_GPIO0D_IOMUX_SEL_0	0x8018	W	0x00000000	GPIO0D IOMUX Select Register 0
GPIO0_IOC_GPIO0A_DS_0	0x0100	W	0x00000F0F	GPIO0A driver strength 0 register
GPIO0_IOC_GPIO0A_DS_1	0x0104	W	0x00000B0B	GPIO0A driver strength 1 register
GPIO0_IOC_GPIO0A_DS_2	0x0108	W	0x00000B0B	GPIO0A driver strength 2 register
GPIO0_IOC_GPIO0A_DS_3	0x010C	W	0x00000F0F	GPIO0A driver strength 3 register
GPIO0_IOC_GPIO0B_DS_0	0x0110	W	0x00000F0F	GPIO0B driver strength 0 register

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Name	Offset	Size	Reset Value	Description
GPIO0_IOC_GPIO0B_DS_1	0x0114	W	0x00000B0F	GPIO0B driver strength 1 register
GPIO0_IOC_GPIO0B_DS_2	0x0118	W	0x0000000B	GPIO0B driver strength 2 register
GPIO0_IOC_GPIO0C_DS_0	0x8120	W	0x00000909	GPIO0C driver strength 0 register
GPIO0_IOC_GPIO0C_DS_1	0x8124	W	0x00000909	GPIO0C driver strength 1 register
GPIO0_IOC_GPIO0C_DS_2	0x8128	W	0x00000909	GPIO0C driver strength 2 register
GPIO0_IOC_GPIO0C_DS_3	0x812C	W	0x00000909	GPIO0C driver strength 3 register
GPIO0_IOC_GPIO0D_DS_0	0x8130	W	0x00000909	GPIO0D driver strength 0 register
GPIO0_IOC_GPIO0A_PULL	0x0300	W	0x00005640	GPIO0A pull register
GPIO0_IOC_GPIO0B_PULL	0x0304	W	0x0000016A	GPIO0B pull register
GPIO0_IOC_GPIO0C_PULL	0x8308	W	0x0000AA5A	GPIO0C pull register
GPIO0_IOC_GPIO0D_PULL	0x830C	W	0x0000000A	GPIO0D pull register
GPIO0_IOC_GPIO0A_IE	0x0400	W	0x000000FF	GPIO0A input enable register
GPIO0_IOC_GPIO0B_IE	0x0404	W	0x0000001F	GPIO0B input enable register
GPIO0_IOC_GPIO0C_IE	0x8408	W	0x000000FF	GPIO0C input enable register
GPIO0_IOC_GPIO0D_IE	0x840C	W	0x00000003	GPIO0D input enable register
GPIO0_IOC_GPIO0A_SMT	0x0500	W	0x000000FF	GPIO0A receiver enable for schmitter trigger register
GPIO0_IOC_GPIO0B_SMT	0x0504	W	0x0000001F	GPIO0B receiver enable for schmitter trigger register
GPIO0_IOC_GPIO0C_SMT	0x8508	W	0x000000FF	GPIO0C receiver enable for schmitter trigger register
GPIO0_IOC_GPIO0D_SMT	0x850C	W	0x00000003	GPIO0D receiver enable for schmitter trigger register
GPIO0_IOC_GPIO0A_SUS	0x0600	W	0x00000000	GPIO0A enable weak pull keeper register
GPIO0_IOC_GPIO0B_SUS	0x0604	W	0x00000000	GPIO0B enable weak pull keeper register
GPIO0_IOC_GPIO0C_SUS	0x8608	W	0x00000000	GPIO0C enable weak pull keeper register
GPIO0_IOC_GPIO0D_SUS	0x860C	W	0x00000000	GPIO0D enable weak pull keeper register
GPIO0_IOC_GPIO0A_SL	0x0700	W	0x00000000	GPIO0A slew rate control register
GPIO0_IOC_GPIO0B_SL	0x0704	W	0x00000000	GPIO0B slew rate control register
GPIO0_IOC_GPIO0C_SL	0x8708	W	0x00000000	GPIO0C slew rate control register
GPIO0_IOC_GPIO0D_SL	0x870C	W	0x00000000	GPIO0D slew rate control register

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Name	Offset	Size	Reset Value	Description
GPIO0_IOC_GPIO0A_OD	0x0800	W	0x00000000	GPIO0A open drain register
GPIO0_IOC_GPIO0B_OD	0x0804	W	0x00000000	GPIO0B open drain register
GPIO0_IOC_GPIO0C_OD	0x8808	W	0x00000000	GPIO0C open drain register
GPIO0_IOC_GPIO0D_OD	0x880C	W	0x00000000	GPIO0D open drain register
GPIO0_IOC_IO_VSEL_PMUIO0	0x0900	W	0x00000000	PMUIO0 iddq register
GPIO0_IOC_IO_VSEL_PMUIO1	0x8900	W	0x00000000	PMUIO1 iddq register
GPIO0_IOC_GRF_JTAG_CON0	0x0904	W	0x00000009	JTAG control register0
GPIO0_IOC_GRF_JTAG_CON1	0x0908	W	0x016E3600	JTAG control register1
GPIO0_IOC_XIN_CON	0x0910	W	0x0000000F	XIN con register
GPIO0_IOC_GRF_GPIO0_FILTER_CON0	0x0C00	W	0x00000000	GPIO0 filter config register 0
GPIO0_IOC_GRF_GPIO0_FILTER_CON1	0x0C04	W	0x00000000	GPIO0 filter config register 1
GPIO0_IOC_GRF_GPIO0_FILTER_CON2	0x0C08	W	0x00000000	GPIO0 filter config register 2
GPIO0_IOC_GRF_GPIO0_FILTER_CON3	0x0C0C	W	0x00000000	GPIO0 filter config register 3
GPIO0_IOC_GRF_GPIO0_FILTER_CON4	0x0C10	W	0x00000000	GPIO0 filter config register 4
GPIO0_IOC_GRF_GPIO0_FILTER_CON5	0x0C14	W	0x00000000	GPIO0 filter config register 5

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

23.3.3 Detail Registers Description

GPIO0_IOC_GPIO0A_IOMUX_SEL_0

Address: Operational Base(0x201A0000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio0a3_sel 4'h0: GPIO0_A3 4'h1: PWR_CTRL0
11:8	RW	0x0	gpio0a2_sel 4'h0: GPIO0_A2 4'h1: RTC_32K_OUT 4'h2: CLK_32K 4'h3: PMU_DBG
7:4	RW	0x3	gpio0a1_sel 4'h0: GPIO0_A1 4'h1: FSPI1_D3_M0 4'h2: PWM1_CH1_M0 4'h3: TSADC_SHUT 4'h4: TSADC_SHUTORG
3:0	RW	0x0	gpio0a0_sel 4'h0: GPIO0_A0 4'h1: REF_CLK0_OUT 4'h2: TEST_CLK0_OUT

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GPIO0_IOC_GPIO0A_IOMUX_SEL_1

Address: Operational Base(0x201A0000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio0a7_sel 4'h0: GPIO0_A7 4'h1: FSPI1_CSN0_M0 4'h2: SPI0_CSN0_M0
11:8	RW	0x0	gpio0a6_sel 4'h0: GPIO0_A6 4'h1: FSPI1_D2_M0 4'h2: SPI0_CSN1_M0
7:4	RW	0x0	gpio0a5_sel 4'h0: GPIO0_A5 4'h1: SDMMC0_DETN 4'h2: PWM1_CH0_M0
3:0	RW	0x0	gpio0a4_sel 4'h0: GPIO0_A4 4'h1: PWR_CTRL1

GPIO0_IOC_GPIO0B_IOMUX_SEL_0

Address: Operational Base(0x201A0000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio0b3_sel 4'h0: GPIO0_B3 4'h1: UART0_TX_M2 4'h2: PWM1_CH2_M0 4'h3: I2C1_SCL_M0 4'h4: JTAG_TCK_M0 4'h5: PREROLL_DBG
11:8	RW	0x0	gpio0b2_sel 4'h0: GPIO0_B2 4'h1: FSPI1_CLK_M0 4'h2: SPI0_CLK_M0
7:4	RW	0x0	gpio0b1_sel 4'h0: GPIO0_B1 4'h1: FSPI1_D1_M0 4'h2: SPI0_MISO_M0
3:0	RW	0x0	gpio0b0_sel 4'h0: GPIO0_B0 4'h1: FSPI1_D0_M0 4'h2: SPI0_MOSI_M0

GPIO0_IOC_GPIO0B_IOMUX_SEL_1

Address: Operational Base(0x201A0000) + offset (0x000C)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3:0	RW	0x0	gpio0b4_sel 4'h0: GPIO0_B4 4'h1: UART0_RX_M2 4'h2: PWM1_CH3_M0 4'h3: I2C1_SDA_M0 4'h4: JTAG_TMS_M0

GPIO0_IOC_GPIO0C_IOMUX_SEL_0

Address: Operational Base(0x201A0000) + offset (0x8010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio0c3_sel 4'h0: GPIO0_C3 4'h1: SPI2AHB_CLK 4'h4: I2C0_SDA_M0
11:8	RW	0x0	gpio0c2_sel 4'h0: GPIO0_C2 4'h1: SPI2AHB_CSN0 4'h4: I2C0_SCL_M0
7:4	RW	0x0	gpio0c1_sel 4'h0: GPIO0_C1 4'h1: I2C3_SDA_M0 4'h2: PWM0_CH6_M0 4'h3: PWR_CTRL2
3:0	RW	0x0	gpio0c0_sel 4'h0: GPIO0_C0 4'h1: I2C3_SCL_M0 4'h2: PWM0_CH7_M0

GPIO0_IOC_GPIO0C_IOMUX_SEL_1

Address: Operational Base(0x201A0000) + offset (0x8014)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio0c7_sel 4'h0: GPIO0_C7 4'h1: SPI2AHB_D0 4'h2: PWM0_CH3_M0 4'h3: UART1_CTSN_M0 4'h4: FSPI1_TESTDATA_OUT

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Bit	Attr	Reset Value	Description
11:8	RW	0x0	gpio0c6_sel 4'h0: GPIO0_C6 4'h1: SPI2AHB_D1 4'h2: PWM0_CH2_M0 4'h3: UART1_RTSN_M0 4'h4: FSPI1_TESTCLK_OUT
7:4	RW	0x0	gpio0c5_sel 4'h0: GPIO0_C5 4'h1: SPI2AHB_D2 4'h2: PWM0_CH1_M0 4'h3: UART1_RX_M0 4'h4: I2C5_SDA_M0
3:0	RW	0x0	gpio0c4_sel 4'h0: GPIO0_C4 4'h1: SPI2AHB_D3 4'h2: PWM0_CH0_M0 4'h3: UART1_TX_M0 4'h4: I2C5_SCL_M0

GPIO0_IOC_GPIO0D_IOMUX_SEL_0

Address: Operational Base(0x201A0000) + offset (0x8018)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:4	RW	0x0	gpio0d1_sel 4'h0: GPIO0_D1 4'h1: I2C2_SDA_M0 4'h2: PWM0_CH5_M0
3:0	RW	0x0	gpio0d0_sel 4'h0: GPIO0_D0 4'h1: I2C2_SCL_M0 4'h2: PWM0_CH4_M0

GPIO0_IOC_GPIO0A_DS_0

Address: Operational Base(0x201A0000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio0a1_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

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Bit	Attr	Reset Value	Description
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio0a0_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO0_IOC_GPIO0A_DS_1

Address: Operational Base(0x201A0000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0b	gpio0a3_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0b	gpio0a2_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO0_IOC_GPIO0A_DS_2

Address: Operational Base(0x201A0000) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x0b	gpio0a5_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0b	gpio0a4_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO0_IOC_GPIO0A_DS_3

Address: Operational Base(0x201A0000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio0a7_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x0f	gpio0a6_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO0_IOC_GPIO0B_DS_0

Address: Operational Base(0x201A0000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio0b1_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio0b0_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO0_IOC_GPIO0B_DS_1

Address: Operational Base(0x201A0000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:8	RW	0x0b	gpio0b3_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio0b2_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO0_IOC_GPIO0B_DS_2

Address: Operational Base(0x201A0000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5:0	RW	0x0b	gpio0b4_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO0_IOC_GPIO0C_DS_0

Address: Operational Base(0x201A0000) + offset (0x8120)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:8	RW	0x09	gpio0c1_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x09	gpio0c0_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO0_IOC_GPIO0C_DS_1

Address: Operational Base(0x201A0000) + offset (0x8124)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x09	gpio0c3_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x09	gpio0c2_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO0_IOC_GPIO0C_DS_2

Address: Operational Base(0x201A0000) + offset (0x8128)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x09	gpio0c5_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x09	gpio0c4_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO0_IOC_GPIO0C_DS_3

Address: Operational Base(0x201A0000) + offset (0x812C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x09	gpio0c7_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x09	gpio0c6_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO0_IOC_GPIO0D_DS_0

Address: Operational Base(0x201A0000) + offset (0x8130)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x09	gpio0d1_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x09	gpio0d0_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO0_IOC_GPIO0A_PULL

Address: Operational Base(0x201A0000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	gpio0a7_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
13:12	RW	0x1	gpio0a6_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
11:10	RW	0x1	gpio0a5_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
9:8	RW	0x2	gpio0a4_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
7:6	RW	0x1	gpio0a3_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
5:4	RW	0x0	gpio0a2_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	gpio0a1_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
1:0	RW	0x0	gpio0a0_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

GPIO0_IOC_GPIO0B_PULL

Address: Operational Base(0x201A0000) + offset (0x0304)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9:8	RW	0x1	gpio0b4_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
7:6	RW	0x1	gpio0b3_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
5:4	RW	0x2	gpio0b2_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
3:2	RW	0x2	gpio0b1_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
1:0	RW	0x2	gpio0b0_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

GPIO0_IOC_GPIO0C_PULL

Address: Operational Base(0x201A0000) + offset (0x8308)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	gpio0c7_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
13:12	RW	0x2	gpio0c6_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
11:10	RW	0x2	gpio0c5_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
9:8	RW	0x2	gpio0c4_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
7:6	RW	0x1	gpio0c3_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
5:4	RW	0x1	gpio0c2_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
3:2	RW	0x2	gpio0c1_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
1:0	RW	0x2	gpio0c0_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

GPIO0_IOC_GPIO0D_PULL

Address: Operational Base(0x201A0000) + offset (0x830C)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3:2	RW	0x2	gpio0d1_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
1:0	RW	0x2	gpio0d0_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

GPIO0_IOC_GPIO0A_IE

Address: Operational Base(0x201A0000) + offset (0x0400)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio0a7_ie Receiver enable 1'b0: N 1'b1: Y
6	RW	0x1	gpio0a6_ie Receiver enable 1'b0: N 1'b1: Y
5	RW	0x1	gpio0a5_ie Receiver enable 1'b0: N 1'b1: Y
4	RW	0x1	gpio0a4_ie Receiver enable 1'b0: N 1'b1: Y
3	RW	0x1	gpio0a3_ie Receiver enable 1'b0: N 1'b1: Y
2	RW	0x1	gpio0a2_ie Receiver enable 1'b0: N 1'b1: Y
1	RW	0x1	gpio0a1_ie Receiver enable 1'b0: N 1'b1: Y

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Bit	Attr	Reset Value	Description
0	RW	0x1	gpio0a0_ie Receiver enable 1'b0: N 1'b1: Y

GPIO0_IOC_GPIO0B_IE

Address: Operational Base(0x201A0000) + offset (0x0404)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x1	gpio0b4_ie Receiver enable 1'b0: N 1'b1: Y
3	RW	0x1	gpio0b3_ie Receiver enable 1'b0: N 1'b1: Y
2	RW	0x1	gpio0b2_ie Receiver enable 1'b0: N 1'b1: Y
1	RW	0x1	gpio0b1_ie Receiver enable 1'b0: N 1'b1: Y
0	RW	0x1	gpio0b0_ie Receiver enable 1'b0: N 1'b1: Y

GPIO0_IOC_GPIO0C_IE

Address: Operational Base(0x201A0000) + offset (0x8408)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio0c7_ie Receiver enable 1'b0: N 1'b1: Y
6	RW	0x1	gpio0c6_ie Receiver enable 1'b0: N 1'b1: Y
5	RW	0x1	gpio0c5_ie Receiver enable 1'b0: N 1'b1: Y

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Bit	Attr	Reset Value	Description
4	RW	0x1	gpio0c4_ie Receiver enable 1'b0: N 1'b1: Y
3	RW	0x1	gpio0c3_ie Receiver enable 1'b0: N 1'b1: Y
2	RW	0x1	gpio0c2_ie Receiver enable 1'b0: N 1'b1: Y
1	RW	0x1	gpio0c1_ie Receiver enable 1'b0: N 1'b1: Y
0	RW	0x1	gpio0c0_ie Receiver enable 1'b0: N 1'b1: Y

GPIO0_IOC_GPIO0D_IE

Address: Operational Base(0x201A0000) + offset (0x840C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x1	gpio0d1_ie Receiver enable 1'b0: N 1'b1: Y
0	RW	0x1	gpio0d0_ie Receiver enable 1'b0: N 1'b1: Y

GPIO0_IOC_GPIO0A_SMT

Address: Operational Base(0x201A0000) + offset (0x0500)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio0a7_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
6	RW	0x1	gpio0a6_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y

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Bit	Attr	Reset Value	Description
5	RW	0x1	gpio0a5_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
4	RW	0x1	gpio0a4_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
3	RW	0x1	gpio0a3_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
2	RW	0x1	gpio0a2_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
1	RW	0x1	gpio0a1_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
0	RW	0x1	gpio0a0_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y

GPIO0_IOC_GPIO0B_SMT

Address: Operational Base(0x201A0000) + offset (0x0504)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x1	gpio0b4_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
3	RW	0x1	gpio0b3_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
2	RW	0x1	gpio0b2_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
1	RW	0x1	gpio0b1_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
0	RW	0x1	gpio0b0_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y

GPIO0_IOC_GPIO0C_SMT

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Address: Operational Base(0x201A0000) + offset (0x8508)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio0c7_smt
6	RW	0x1	gpio0c6_smt
5	RW	0x1	gpio0c5_smt
4	RW	0x1	gpio0c4_smt
3	RW	0x1	gpio0c3_smt
2	RW	0x1	gpio0c2_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
1	RW	0x1	gpio0c1_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
0	RW	0x1	gpio0c0_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y

GPIO0_IOC_GPIO0D_SMT

Address: Operational Base(0x201A0000) + offset (0x850C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x1	gpio0d1_smt
0	RW	0x1	gpio0d0_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y

GPIO0_IOC_GPIO0A_SUS

Address: Operational Base(0x201A0000) + offset (0x0600)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio0a7_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
6	RW	0x0	gpio0a6_sus Weak pull keeper for pad 1'b0: N 1'b1: Y

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Bit	Attr	Reset Value	Description
5	RW	0x0	gpio0a5_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
4	RW	0x0	gpio0a4_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
3	RW	0x0	gpio0a3_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
2	RW	0x0	gpio0a2_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
1	RW	0x0	gpio0a1_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
0	RW	0x0	gpio0a0_sus Weak pull keeper for pad 1'b0: N 1'b1: Y

GPIO0_IOC_GPIO0B_SUS

Address: Operational Base(0x201A0000) + offset (0x0604)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x0	gpio0b4_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
3	RW	0x0	gpio0b3_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
2	RW	0x0	gpio0b2_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
1	RW	0x0	gpio0b1_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
0	RW	0x0	gpio0b0_sus Weak pull keeper for pad 1'b0: N 1'b1: Y

GPIO0_IOC_GPIO0C_SUS

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Address: Operational Base(0x201A0000) + offset (0x8608)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio0c7_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
6	RW	0x0	gpio0c6_sus
5	RW	0x0	gpio0c5_sus
4	RW	0x0	gpio0c4_sus
3	RW	0x0	gpio0c3_sus
2	RW	0x0	gpio0c2_sus
1	RW	0x0	gpio0c1_sus
0	RW	0x0	gpio0c0_sus

GPIO0_IOC_GPIO0D_SUS

Address: Operational Base(0x201A0000) + offset (0x860C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	gpio0d1_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
0	RW	0x0	gpio0d0_sus Weak pull keeper for pad 1'b0: N 1'b1: Y

GPIO0_IOC_GPIO0A_SL

Address: Operational Base(0x201A0000) + offset (0x0700)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio0a7_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
13:12	RW	0x0	gpio0a6_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y

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Bit	Attr	Reset Value	Description
11:10	RW	0x0	gpio0a5_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
9:8	RW	0x0	gpio0a4_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
7:6	RW	0x0	gpio0a3_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
5:4	RW	0x0	gpio0a2_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
3:2	RW	0x0	gpio0a1_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
1:0	RW	0x0	gpio0a0_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y

GPIO0_IOC_GPIO0B_SL

Address: Operational Base(0x201A0000) + offset (0x0704)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9:8	RW	0x0	gpio0b4_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y

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Bit	Attr	Reset Value	Description
7:6	RW	0x0	gpio0b3_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
5:4	RW	0x0	gpio0b2_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
3:2	RW	0x0	gpio0b1_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
1:0	RW	0x0	gpio0b0_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y

GPIO0_IOC_GPIO0C_SL

Address: Operational Base(0x201A0000) + offset (0x8708)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio0c7_sl
13:12	RW	0x0	gpio0c6_sl
11:10	RW	0x0	gpio0c5_sl
9:8	RW	0x0	gpio0c4_sl
7:6	RW	0x0	gpio0c3_sl
5:4	RW	0x0	gpio0c2_sl
3:2	RW	0x0	gpio0c1_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
1:0	RW	0x0	gpio0c0_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y

GPIO0_IOC_GPIO0D_SL

Address: Operational Base(0x201A0000) + offset (0x870C)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3:2	RW	0x0	gpio0d1_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
1:0	RW	0x0	gpio0d0_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y

GPIO0_IOC_GPIO0A_OD

Address: Operational Base(0x201A0000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio0a7_od For open drain functionality 1'b0: N 1'b1: Y
6	RW	0x0	gpio0a6_od For open drain functionality 1'b0: N 1'b1: Y
5	RW	0x0	gpio0a5_od For open drain functionality 1'b0: N 1'b1: Y
4	RW	0x0	gpio0a4_od For open drain functionality 1'b0: N 1'b1: Y
3	RW	0x0	gpio0a3_od For open drain functionality 1'b0: N 1'b1: Y
2	RW	0x0	gpio0a2_od For open drain functionality 1'b0: N 1'b1: Y
1	RW	0x0	gpio0a1_od For open drain functionality 1'b0: N 1'b1: Y

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Bit	Attr	Reset Value	Description
0	RW	0x0	gpio0a0_od For open drain functionality 1'b0: N 1'b1: Y

GPIO0_IOC_GPIO0B_OD

Address: Operational Base(0x201A0000) + offset (0x0804)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:5	RO	0x000	reserved
4	RW	0x0	gpio0b4_od For open drain functionality 1'b0: N 1'b1: Y
3	RW	0x0	gpio0b3_od For open drain functionality 1'b0: N 1'b1: Y
2	RW	0x0	gpio0b2_od For open drain functionality 1'b0: N 1'b1: Y
1	RW	0x0	gpio0b1_od For open drain functionality 1'b0: N 1'b1: Y
0	RW	0x0	gpio0b0_od For open drain functionality 1'b0: N 1'b1: Y

GPIO0_IOC_GPIO0C_OD

Address: Operational Base(0x201A0000) + offset (0x8808)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio0c7_od
6	RW	0x0	gpio0c6_od
5	RW	0x0	gpio0c5_od
4	RW	0x0	gpio0c4_od
3	RW	0x0	gpio0c3_od
2	RW	0x0	gpio0c2_od
1	RW	0x0	gpio0c1_od
0	RW	0x0	gpio0c0_od

GPIO0_IOC_GPIO0D_OD

Address: Operational Base(0x201A0000) + offset (0x880C)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	gpio0d1_od
0	RW	0x0	gpio0d0_od

GPIO0_IOC_IO_VSEL_PMUIO0

Address: Operational Base(0x201A0000) + offset (0x0900)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	poc_pmuio0_iddq PMUIO0 iddq control 1'b0: Disable 1'b1: Enable

GPIO0_IOC_IO_VSEL_PMUIO1

Address: Operational Base(0x201A0000) + offset (0x8900)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	poc_pmuio1_vd
14:1	RO	0x0000	reserved
0	RW	0x0	poc_pmuio1_iddq

GPIO0_IOC_GRF_JTAG_CON0

Address: Operational Base(0x201A0000) + offset (0x0904)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x1	grf_con_force_jtag_uart_rx_m2 Enable GPIO0b3 and GPIO0b4 switch to JTAG function if uart0_rx low last for a specified period of time. 1'b0: Disable 1'b1: Enable
2:0	RW	0x1	grf_con_jtag_sel Switch source to JTAG function. 3'b000: reserved 3'b001: connect to CPU 3'b010: connect to HPMCU 3'b100: connect to LPMCU

GPIO0_IOC_GRF_JTAG_CON1

Address: Operational Base(0x201A0000) + offset (0x0908)

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Bit	Attr	Reset Value	Description
31:0	RW	0x016e3600	uart0_m2_rx_low_dly uart0_rx low delay count by 24M. The default value means 1 second.

GPIO0_IOC_XIN_CON

Address: Operational Base(0x201A0000) + offset (0x0910)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3:0	RW	0xf	xin_con_ds The drive strength of OSC_24M.

GPIO0_IOC_GRF_GPIO0_FILTER_CON0

Address: Operational Base(0x201A0000) + offset (0x0C00)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14:10	RW	0x00	grf_gpio0_filter_sel1 GPIO select to go through first filter logic 5'h00: GPIOxA0 5'h01: GPIOxA1 5'h02: GPIOxA2 5'h03: GPIOxA3 5'h04: GPIOxA4 5'h05: GPIOxA5 5'h06: GPIOxA6 5'h07: GPIOxA7 5'h08: GPIOxB0 5'h09: GPIOxB1 5'h0a: GPIOxB2 5'h0b: GPIOxB3 5'h0c: GPIOxB4 5'h0d: GPIOxB5 5'h0e: GPIOxB6 5'h0f: GPIOxB7 5'h10: GPIOxC0 5'h11: GPIOxC1 5'h12: GPIOxC2 5'h13: GPIOxC3 5'h14: GPIOxC4 5'h15: GPIOxC5 5'h16: GPIOxC6 5'h17: GPIOxC7 5'h18: GPIOxD0 5'h19: GPIOxD1 5'h1a: GPIOxD2 5'h1b: GPIOxD3 5'h1c: GPIOxD4 5'h1d: GPIOxD5 5'h1e: GPIOxD6 5'h1f: GPIOxD7
9	RO	0x0	reserved
8:4	RW	0x00	grf_gpio0_filter_sel0 GPIO select to go through first filter logic 5'h00: GPIOxA0 5'h01: GPIOxA1 5'h02: GPIOxA2 5'h03: GPIOxA3 5'h04: GPIOxA4 5'h05: GPIOxA5 5'h06: GPIOxA6 5'h07: GPIOxA7 5'h08: GPIOxB0 5'h09: GPIOxB1 5'h0a: GPIOxB2 5'h0b: GPIOxB3 5'h0c: GPIOxB4 5'h0d: GPIOxB5 5'h0e: GPIOxB6 5'h0f: GPIOxB7 5'h10: GPIOxC0 5'h11: GPIOxC1 5'h12: GPIOxC2

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Bit	Attr	Reset Value	Description
			5'h13: GPIOxC3 5'h14: GPIOxC4 5'h15: GPIOxC5 5'h16: GPIOxC6 5'h17: GPIOxC7 5'h18: GPIOxD0 5'h19: GPIOxD1 5'h1a: GPIOxD2 5'h1b: GPIOxD3 5'h1c: GPIOxD4 5'h1d: GPIOxD5 5'h1e: GPIOxD6 5'h1f: GPIOxD7
3:0	RW	0x0	grf_gpio0_filter_en There are four filter circuits for pad in GPIOx, each bit controls the enable of one filter.

GPIO0_IOC_GRF_GPIO0_FILTER_CON1

Address: Operational Base(0x201A0000) + offset (0x0C04)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:10	RW	0x00	grf_gpio0_filter_sel3 GPIO select to go through first filter logic 5'h00: GPIOxA0 5'h01: GPIOxA1 5'h02: GPIOxA2 5'h03: GPIOxA3 5'h04: GPIOxA4 5'h05: GPIOxA5 5'h06: GPIOxA6 5'h07: GPIOxA7 5'h08: GPIOxB0 5'h09: GPIOxB1 5'h0a: GPIOxB2 5'h0b: GPIOxB3 5'h0c: GPIOxB4 5'h0d: GPIOxB5 5'h0e: GPIOxB6 5'h0f: GPIOxB7 5'h10: GPIOxC0 5'h11: GPIOxC1 5'h12: GPIOxC2 5'h13: GPIOxC3 5'h14: GPIOxC4 5'h15: GPIOxC5 5'h16: GPIOxC6 5'h17: GPIOxC7 5'h18: GPIOxD0 5'h19: GPIOxD1 5'h1a: GPIOxD2 5'h1b: GPIOxD3 5'h1c: GPIOxD4

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Bit	Attr	Reset Value	Description
			5'h1d: GPIOxD5 5'h1e: GPIOxD6 5'h1f: GPIOxD7
9	RO	0x0	reserved
8:4	RW	0x00	grf_gpio0_filter_sel2 GPIO select to go through first filter logic 5'h00: GPIOxA0 5'h01: GPIOxA1 5'h02: GPIOxA2 5'h03: GPIOxA3 5'h04: GPIOxA4 5'h05: GPIOxA5 5'h06: GPIOxA6 5'h07: GPIOxA7 5'h08: GPIOxB0 5'h09: GPIOxB1 5'h0a: GPIOxB2 5'h0b: GPIOxB3 5'h0c: GPIOxB4 5'h0d: GPIOxB5 5'h0e: GPIOxB6 5'h0f: GPIOxB7 5'h10: GPIOxC0 5'h11: GPIOxC1 5'h12: GPIOxC2 5'h13: GPIOxC3 5'h14: GPIOxC4 5'h15: GPIOxC5 5'h16: GPIOxC6 5'h17: GPIOxC7 5'h18: GPIOxD0 5'h19: GPIOxD1 5'h1a: GPIOxD2 5'h1b: GPIOxD3 5'h1c: GPIOxD4 5'h1d: GPIOxD5 5'h1e: GPIOxD6 5'h1f: GPIOxD7
3:0	RO	0x0	reserved

GPIO0_IOC_GRF_GPIO0_FILTER_CON2

Address: Operational Base(0x201A0000) + offset (0x0C08)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio0_filter_count0 Filter counter for first filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

GPIO0_IOC_GRF_GPIO0_FILTER_CON3

Address: Operational Base(0x201A0000) + offset (0x0C0C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio0_filter_count1 Filter counter for second filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

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GPIO0_IOC_GRF_GPIO0_FILTER_CON4

Address: Operational Base(0x201A0000) + offset (0x0C10)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio0_filter_count2 Filter counter for third filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

GPIO0_IOC_GRF_GPIO0_FILTER_CON5

Address: Operational Base(0x201A0000) + offset (0x0C14)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio0_filter_count3 Filter counter for fouth filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

23.4 GPIO1_IOC Register Description

23.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

23.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
GPIO1_IOC_GPIO1A_IOMUX_SEL_0	0x0020	W	0x00000000	GPIO1A IOMUX Select Register 0
GPIO1_IOC_GPIO1A_IOMUX_SEL_1	0x0024	W	0x00000000	GPIO1A IOMUX Select Register 1
GPIO1_IOC_GPIO1B_IOMUX_SEL_0	0x0028	W	0x00000000	GPIO1B IOMUX Select Register 0
GPIO1_IOC_GPIO1B_IOMUX_SEL_1	0x002C	W	0x00000000	GPIO1B IOMUX Select Register 1
GPIO1_IOC_GPIO1A_DS_0	0x0140	W	0x00000F0F	GPIO1A driver strength register 0
GPIO1_IOC_GPIO1A_DS_1	0x0144	W	0x00000F0F	GPIO1A driver strength register 1
GPIO1_IOC_GPIO1A_DS_2	0x0148	W	0x00000F0F	GPIO1A driver strength register 2
GPIO1_IOC_GPIO1A_DS_3	0x014C	W	0x00000F0F	GPIO1A driver strength register 3
GPIO1_IOC_GPIO1B_DS_0	0x0150	W	0x00000F0F	GPIO1B driver strength register 0
GPIO1_IOC_GPIO1B_DS_1	0x0154	W	0x00000F0F	GPIO1B driver strength register 1
GPIO1_IOC_GPIO1B_DS_2	0x0158	W	0x00000F0F	GPIO1B driver strength register 2
GPIO1_IOC_GPIO1B_DS_3	0x015C	W	0x00000F0F	GPIO1B driver strength register 3
GPIO1_IOC_GPIO1A_PULL	0x0310	W	0x00000000	GPIO1A pull register
GPIO1_IOC_GPIO1B_PULL	0x0314	W	0x00000000	GPIO1B pull register
GPIO1_IOC_GPIO1A_IE	0x0410	W	0x000000FF	GPIO1A input enable register
GPIO1_IOC_GPIO1B_IE	0x0414	W	0x000000FF	GPIO1B input enable register

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Name	Offset	Size	Reset Value	Description
GPIO1_IOC_GPIO1A_SMT	0x0510	W	0x00000000	GPIO1A receiver enable for schmitter trigger register
GPIO1_IOC_GPIO1B_SMT	0x0514	W	0x00000000	GPIO1B receiver enable for schmitter trigger register
GPIO1_IOC_GPIO1A_SUS	0x0610	W	0x00000000	GPIO1A enable weak pull keeper register
GPIO1_IOC_GPIO1B_SUS	0x0614	W	0x00000000	GPIO1B enable weak pull keeper register
GPIO1_IOC_GPIO1A_SL	0x0710	W	0x00000000	GPIO1A slew rate control register
GPIO1_IOC_GPIO1B_SL	0x0714	W	0x00000000	GPIO1B slew rate control register
GPIO1_IOC_GPIO1A_OD	0x0810	W	0x00000000	GPIO1A open drain register
GPIO1_IOC_GPIO1B_OD	0x0814	W	0x00000000	GPIO1B open drain register
GPIO1_IOC_IO1_VSEL	0x0908	W	0x00000000	IO1 iddq register
GPIO1_IOC_IOC_MISC_CON0	0x0A00	W	0x00000000	IOC_MISC_CON0 register
GPIO1_IOC_GRF_GPIO1_FILTER_CON0	0x0A04	W	0x00000000	GPIO1 filter config register 0
GPIO1_IOC_GRF_GPIO1_FILTER_CON1	0x0A08	W	0x00000000	GPIO1 filter config register 1
GPIO1_IOC_GRF_GPIO1_FILTER_CON2	0x0A0C	W	0x00000000	GPIO1 filter config register 2
GPIO1_IOC_GRF_GPIO1_FILTER_CON3	0x0A10	W	0x00000000	GPIO1 filter config register 3
GPIO1_IOC_GRF_GPIO1_FILTER_CON4	0x0A14	W	0x00000000	GPIO1 filter config register 4
GPIO1_IOC_GRF_GPIO1_FILTER_CON5	0x0A18	W	0x00000000	GPIO1 filter config register 5

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

23.4.3 Detail Registers Description

GPIO1_IOC_GPIO1A_IOMUX_SEL_0

Address: Operational Base(0x201B0000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio1a3_sel 4'h0: GPIO1_A3 4'h1: EMMC_D3 4'h2: FSPI1_D3_M1 4'h3: PWM3_CH3_M0
11:8	RW	0x0	gpio1a2_sel 4'h0: GPIO1_A2 4'h1: EMMC_D2 4'h2: FSPI1_D2_M1 4'h3: PWM3_CH2_M0

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	gpio1a1_sel 4'h0: GPIO1_A1 4'h1: EMMC_D1 4'h2: FSPI1_D1_M1 4'h3: PWM3_CH1_M0
3:0	RW	0x0	gpio1a0_sel 4'h0: GPIO1_A0 4'h1: EMMC_D0 4'h2: FSPI1_D0_M1 4'h3: PWM3_CH0_M0

GPIO1_IOC_GPIO1A_IOMUX_SEL_1

Address: Operational Base(0x201B0000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio1a7_sel 4'h0: GPIO1_A7 4'h1: EMMC_D7 4'h3: PWM3_CH7_M0
11:8	RW	0x0	gpio1a6_sel 4'h0: GPIO1_A6 4'h1: EMMC_D6 4'h3: PWM3_CH6_M0
7:4	RW	0x0	gpio1a5_sel 4'h0: GPIO1_A5 4'h1: EMMC_D5 4'h2: FSPI0_CSN1 4'h3: PWM3_CH5_M0
3:0	RW	0x0	gpio1a4_sel 4'h0: GPIO1_A4 4'h1: EMMC_D4 4'h3: PWM3_CH4_M0

GPIO1_IOC_GPIO1B_IOMUX_SEL_0

Address: Operational Base(0x201B0000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio1b3_sel 4'h0: GPIO1_B3 4'h1: EMMC_CLK 4'h2: FSPI1_CLK_M1
11:8	RW	0x0	gpio1b2_sel 4'h0: GPIO1_B2 4'h1: FSPI0_D2 4'h2: SAI1_SDO_M0
7:4	RW	0x0	gpio1b1_sel 4'h0: GPIO1_B1 4'h1: EMMC_CMD 4'h2: FSPI1_CSN0_M1

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	gpio1b0_sel 4'h0: GPIO1_B0 4'h1: FSPI0_CSN0 4'h2: SAI1_MCLK_M0 4'h3: SDMMC0_TESTDATA_OUT

GPIO1_IOC_GPIO1B_IOMUX_SEL_1

Address: Operational Base(0x201B0000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio1b7_sel 4'h0: GPIO1_B7 4'h1: FSPI0_CLK 4'h3: SDMMC0_TESTCLK_OUT
11:8	RW	0x0	gpio1b6_sel 4'h0: GPIO1_B6 4'h1: FSPI0_D3 4'h2: SAI1_SDI_M0
7:4	RW	0x0	gpio1b5_sel 4'h0: GPIO1_B5 4'h1: FSPI0_D1 4'h2: SAI1_SCLK_M0
3:0	RW	0x0	gpio1b4_sel 4'h0: GPIO1_B4 4'h1: FSPI0_D0 4'h2: SAI1_LRCK_M0

GPIO1_IOC_GPIO1A_DS_0

Address: Operational Base(0x201B0000) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio1a1_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x0f	gpio1a0_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO1_IOC_GPIO1A_DS_1

Address: Operational Base(0x201B0000) + offset (0x0144)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio1a3_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio1a2_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO1_IOC_GPIO1A_DS_2

Address: Operational Base(0x201B0000) + offset (0x0148)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x0f	gpio1a5_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio1a4_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO1_IOC_GPIO1A_DS_3

Address: Operational Base(0x201B0000) + offset (0x014C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio1a7_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x0f	gpio1a6_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO1_IOC_GPIO1B_DS_0

Address: Operational Base(0x201B0000) + offset (0x0150)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio1b1_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio1b0_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO1_IOC_GPIO1B_DS_1

Address: Operational Base(0x201B0000) + offset (0x0154)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x0f	gpio1b3_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio1b2_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO1_IOC_GPIO1B_DS_2

Address: Operational Base(0x201B0000) + offset (0x0158)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio1b5_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio1b4_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA)

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Bit	Attr	Reset Value	Description
			6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO1_IOC_GPIO1B_DS_3

Address: Operational Base(0x201B0000) + offset (0x015C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio1b7_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio1b6_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO1_IOC_GPIO1A_PULL

Address: Operational Base(0x201B0000) + offset (0x0310)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio1a7_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

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Bit	Attr	Reset Value	Description
13:12	RW	0x0	gpio1a6_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
11:10	RW	0x0	gpio1a5_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
9:8	RW	0x0	gpio1a4_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
7:6	RW	0x0	gpio1a3_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
5:4	RW	0x0	gpio1a2_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
3:2	RW	0x0	gpio1a1_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
1:0	RW	0x0	gpio1a0_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

GPIO1_IOC_GPIO1B_PULL

Address: Operational Base(0x201B0000) + offset (0x0314)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio1b7_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

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Bit	Attr	Reset Value	Description
13:12	RW	0x0	gpio1b6_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
11:10	RW	0x0	gpio1b5_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
9:8	RW	0x0	gpio1b4_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
7:6	RW	0x0	gpio1b3_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
5:4	RW	0x0	gpio1b2_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
3:2	RW	0x0	gpio1b1_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
1:0	RW	0x0	gpio1b0_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

GPIO1_IOC_GPIO1A_IE

Address: Operational Base(0x201B0000) + offset (0x0410)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio1a7_ie Receiver enable 1'b0: N 1'b1: Y

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Bit	Attr	Reset Value	Description
6	RW	0x1	gpio1a6_ie Receiver enable 1'b0: N 1'b1: Y
5	RW	0x1	gpio1a5_ie Receiver enable 1'b0: N 1'b1: Y
4	RW	0x1	gpio1a4_ie Receiver enable 1'b0: N 1'b1: Y
3	RW	0x1	gpio1a3_ie Receiver enable 1'b0: N 1'b1: Y
2	RW	0x1	gpio1a2_ie Receiver enable 1'b0: N 1'b1: Y
1	RW	0x1	gpio1a1_ie Receiver enable 1'b0: N 1'b1: Y
0	RW	0x1	gpio1a0_ie Receiver enable 1'b0: N 1'b1: Y

GPIO1_IOC_GPIO1B_IE

Address: Operational Base(0x201B0000) + offset (0x0414)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio1b7_ie Receiver enable 1'b0: N 1'b1: Y
6	RW	0x1	gpio1b6_ie Receiver enable 1'b0: N 1'b1: Y
5	RW	0x1	gpio1b5_ie Receiver enable 1'b0: N 1'b1: Y
4	RW	0x1	gpio1b4_ie Receiver enable 1'b0: N 1'b1: Y

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Bit	Attr	Reset Value	Description
3	RW	0x1	gpio1b3_ie Receiver enable 1'b0: N 1'b1: Y
2	RW	0x1	gpio1b2_ie Receiver enable 1'b0: N 1'b1: Y
1	RW	0x1	gpio1b1_ie Receiver enable 1'b0: N 1'b1: Y
0	RW	0x1	gpio1b0_ie Receiver enable 1'b0: N 1'b1: Y

GPIO1_IOC_GPIO1A_SMT

Address: Operational Base(0x201B0000) + offset (0x0510)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio1a7_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
6	RW	0x0	gpio1a6_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
5	RW	0x0	gpio1a5_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
4	RW	0x0	gpio1a4_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
3	RW	0x0	gpio1a3_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
2	RW	0x0	gpio1a2_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
1	RW	0x0	gpio1a1_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y

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Bit	Attr	Reset Value	Description
0	RW	0x0	gpio1a0_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y

GPIO1_IOC_GPIO1B_SMT

Address: Operational Base(0x201B0000) + offset (0x0514)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio1b7_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
6	RW	0x0	gpio1b6_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
5	RW	0x0	gpio1b5_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
4	RW	0x0	gpio1b4_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
3	RW	0x0	gpio1b3_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
2	RW	0x0	gpio1b2_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
1	RW	0x0	gpio1b1_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
0	RW	0x0	gpio1b0_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y

GPIO1_IOC_GPIO1A_SUS

Address: Operational Base(0x201B0000) + offset (0x0610)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
7	RW	0x0	gpio1a7_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
6	RW	0x0	gpio1a6_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
5	RW	0x0	gpio1a5_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
4	RW	0x0	gpio1a4_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
3	RW	0x0	gpio1a3_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
2	RW	0x0	gpio1a2_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
1	RW	0x0	gpio1a1_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
0	RW	0x0	gpio1a0_sus Weak pull keeper for pad 1'b0: N 1'b1: Y

GPIO1_IOC_GPIO1B_SUS

Address: Operational Base(0x201B0000) + offset (0x0614)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio1b7_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
6	RW	0x0	gpio1b6_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
5	RW	0x0	gpio1b5_sus Weak pull keeper for pad 1'b0: N 1'b1: Y

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Bit	Attr	Reset Value	Description
4	RW	0x0	gpio1b4_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
3	RW	0x0	gpio1b3_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
2	RW	0x0	gpio1b2_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
1	RW	0x0	gpio1b1_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
0	RW	0x0	gpio1b0_sus Weak pull keeper for pad 1'b0: N 1'b1: Y

GPIO1_IOC_GPIO1A_SL

Address: Operational Base(0x201B0000) + offset (0x0710)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio1a7_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
13:12	RW	0x0	gpio1a6_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
11:10	RW	0x0	gpio1a5_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
9:8	RW	0x0	gpio1a4_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y

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Bit	Attr	Reset Value	Description
7:6	RW	0x0	gpio1a3_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
5:4	RW	0x0	gpio1a2_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
3:2	RW	0x0	gpio1a1_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
1:0	RW	0x0	gpio1a0_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y

GPIO1_IOC_GPIO1B_SL

Address: Operational Base(0x201B0000) + offset (0x0714)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio1b7_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
13:12	RW	0x0	gpio1b6_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
11:10	RW	0x0	gpio1b5_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
9:8	RW	0x0	gpio1b4_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y

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Bit	Attr	Reset Value	Description
7:6	RW	0x0	gpio1b3_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
5:4	RW	0x0	gpio1b2_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
3:2	RW	0x0	gpio1b1_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
1:0	RW	0x0	gpio1b0_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y

GPIO1_IOC_GPIO1A_OD

Address: Operational Base(0x201B0000) + offset (0x0810)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio1a7_od For open drain functionality 1'b0: N 1'b1: Y
6	RW	0x0	gpio1a6_od For open drain functionality 1'b0: N 1'b1: Y
5	RW	0x0	gpio1a5_od For open drain functionality 1'b0: N 1'b1: Y
4	RW	0x0	gpio1a4_od For open drain functionality 1'b0: N 1'b1: Y
3	RW	0x0	gpio1a3_od For open drain functionality 1'b0: N 1'b1: Y

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Bit	Attr	Reset Value	Description
2	RW	0x0	gpio1a2_od For open drain functionality 1'b0: N 1'b1: Y
1	RW	0x0	gpio1a1_od For open drain functionality 1'b0: N 1'b1: Y
0	RW	0x0	gpio1a0_od For open drain functionality 1'b0: N 1'b1: Y

GPIO1_IOC_GPIO1B_OD

Address: Operational Base(0x201B0000) + offset (0x0814)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio1b7_od For open drain functionality 1'b0: N 1'b1: Y
6	RW	0x0	gpio1b6_od For open drain functionality 1'b0: N 1'b1: Y
5	RW	0x0	gpio1b5_od For open drain functionality 1'b0: N 1'b1: Y
4	RW	0x0	gpio1b4_od For open drain functionality 1'b0: N 1'b1: Y
3	RW	0x0	gpio1b3_od For open drain functionality 1'b0: N 1'b1: Y
2	RW	0x0	gpio1b2_od For open drain functionality 1'b0: N 1'b1: Y
1	RW	0x0	gpio1b1_od For open drain functionality 1'b0: N 1'b1: Y
0	RW	0x0	gpio1b0_od For open drain functionality 1'b0: N 1'b1: Y

GPIO1_IOC_IO1_VSEL

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Address: Operational Base(0x201B0000) + offset (0x0908)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	vccio1_vd VCCIO hardware voltage status 1'b0: 1.8V 1'b1: 3.3V
14:1	RO	0x0000	reserved
0	RW	0x0	poc_vccio1_iddq VCCIO1 iddq control 1'b0: Disable 1'b1: Enable

GPIO1_IOC_IOC_MISC_CON0

Address: Operational Base(0x201B0000) + offset (0x0A00)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	fspi0_clk_ioe_ FSPI clk pad output enable, 1'b0: means enable fspi output enable. 1'b1: means disable fspi output enable.

GPIO1_IOC_GRF_GPIO1_FILTER_CON0

Address: Operational Base(0x201B0000) + offset (0x0A04)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14:10	RW	0x00	grf_gpio1_filter_sel1 5'h00: GPIO1A0 5'h01: GPIO1A1 5'h02: GPIO1A2 5'h03: GPIO1A3 5'h04: GPIO1A4 5'h05: GPIO1A5 5'h06: GPIO1A6 5'h07: GPIO1A7 5'h08: GPIO1B0 5'h09: GPIO1B1 5'h0a: GPIO1B2 5'h0b: GPIO1B3 5'h0c: GPIO1B4 5'h0d: GPIO1B5 5'h0e: GPIO1B6 5'h0f: GPIO1B7 5'h10: 0 5'h11: 0 5'h12: 0 5'h13: 0 5'h14: 0 5'h15: 0 5'h16: 0 5'h17: 0 5'h18: 0
9	RO	0x0	reserved
8:4	RW	0x00	grf_gpio1_filter_sel0 5'h00: GPIO1A0 5'h01: GPIO1A1 5'h02: GPIO1A2 5'h03: GPIO1A3 5'h04: GPIO1A4 5'h05: GPIO1A5 5'h06: GPIO1A6 5'h07: GPIO1A7 5'h08: GPIO1B0 5'h09: GPIO1B1 5'h0a: GPIO1B2 5'h0b: GPIO1B3 5'h0c: GPIO1B4 5'h0d: GPIO1B5 5'h0e: GPIO1B6 5'h0f: GPIO1B7 5'h10: 0 5'h11: 0 5'h12: 0 5'h13: 0 5'h14: 0 5'h15: 0 5'h16: 0 5'h17: 0 5'h18: 0
3:0	RW	0x0	grf_gpio1_filter_en There are 4 filter circuits for pad in GPIO1, each bit controls the enable of one filter.

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GPIO1_IOC_GRF_GPIO1_FILTER_CON1

Address: Operational Base(0x201B0000) + offset (0x0A08)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:10	RW	0x00	grf_gpio1_filter_sel3 5'h00: GPIO1A0 5'h01: GPIO1A1 5'h02: GPIO1A2 5'h03: GPIO1A3 5'h04: GPIO1A4 5'h05: GPIO1A5 5'h06: GPIO1A6 5'h07: GPIO1A7 5'h08: GPIO1B0 5'h09: GPIO1B1 5'h0a: GPIO1B2 5'h0b: GPIO1B3 5'h0c: GPIO1B4 5'h0d: GPIO1B5 5'h0e: GPIO1B6 5'h0f: GPIO1B7 5'h10: 0 5'h11: 0 5'h12: 0 5'h13: 0 5'h14: 0 5'h15: 0 5'h16: 0 5'h17: 0 5'h18: 0
9	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
8:4	RW	0x00	grf_gpio1_filter_sel2 5'h00: GPIO1A0 5'h01: GPIO1A1 5'h02: GPIO1A2 5'h03: GPIO1A3 5'h04: GPIO1A4 5'h05: GPIO1A5 5'h06: GPIO1A6 5'h07: GPIO1A7 5'h08: GPIO1B0 5'h09: GPIO1B1 5'h0a: GPIO1B2 5'h0b: GPIO1B3 5'h0c: GPIO1B4 5'h0d: GPIO1B5 5'h0e: GPIO1B6 5'h0f: GPIO1B7 5'h10: 0 5'h11: 0 5'h12: 0 5'h13: 0 5'h14: 0 5'h15: 0 5'h16: 0 5'h17: 0 5'h18: 0
3:0	RO	0x0	reserved

GPIO1_IOC_GRF_GPIO1_FILTER_CON2

Address: Operational Base(0x201B0000) + offset (0x0A0C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio1_filter_count0 Filter counter for first filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

GPIO1_IOC_GRF_GPIO1_FILTER_CON3

Address: Operational Base(0x201B0000) + offset (0x0A10)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio1_filter_count1 Filter counter for first filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

GPIO1_IOC_GRF_GPIO1_FILTER_CON4

Address: Operational Base(0x201B0000) + offset (0x0A14)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio1_filter_count2 Filter counter for first filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

GPIO1_IOC_GRF_GPIO1_FILTER_CON5

Address: Operational Base(0x201B0000) + offset (0x0A18)

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Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio1_filter_count3 Filter counter for first filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

23.5 GPIO2_IOC Register Description

23.5.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

23.5.2 Registers Summary

Name	Offset	Size	Reset Value	Description
GPIO2_IOC_GPIO2A_IOMUX_SEL_0	0x0040	W	0x00004400	GPIO2A IOMUX Select Register 0
GPIO2_IOC_GPIO2A_IOMUX_SEL_1	0x0044	W	0x00000000	GPIO2A IOMUX Select Register 1
GPIO2_IOC_GPIO2A_DS_0	0x0180	W	0x00000F0F	GPIO2A driver strength register 0
GPIO2_IOC_GPIO2A_DS_1	0x0184	W	0x00000F0F	GPIO2A driver strength register 1
GPIO2_IOC_GPIO2A_DS_2	0x0188	W	0x00000F0F	GPIO2A driver strength register 2
GPIO2_IOC_GPIO2A_PULL	0x0320	W	0x00000AAA	GPIO2A pull register
GPIO2_IOC_GPIO2A_IE	0x0420	W	0x0000003F	GPIO2A input enable register
GPIO2_IOC_GPIO2A_SMT	0x0520	W	0x0000003F	GPIO2A receiver enable for schmitter trigger register
GPIO2_IOC_GPIO2A_SUS	0x0620	W	0x00000000	GPIO2A enable weak pull keeper register
GPIO2_IOC_GPIO2A_SL	0x0720	W	0x00000000	GPIO2A slew rate control register
GPIO2_IOC_GPIO2A_OD	0x0820	W	0x00000000	GPIO2A open drain register
GPIO2_IOC_IO_VSEL	0x090C	W	0x00000000	IO iddq register
GPIO2_IOC_GRF_SDDET_DLY_CON	0x0B8C	W	0x0003A980	sdcard detect delay con register
GPIO2_IOC_GRF_JTAG_CON	0x0B90	W	0x00000001	jtag con register
GPIO2_IOC_GRF_GPIO2_FILTER_CON0	0x0C00	W	0x00000000	GPIO2 filter config register 0
GPIO2_IOC_GRF_GPIO2_FILTER_CON1	0x0C04	W	0x00000000	GPIO2 filter config register 1
GPIO2_IOC_GRF_GPIO2_FILTER_CON2	0x0C08	W	0x00000000	GPIO2 filter config register 2
GPIO2_IOC_GRF_GPIO2_FILTER_CON3	0x0C0C	W	0x00000000	GPIO2 filter config register 3
GPIO2_IOC_GRF_GPIO2_FILTER_CON4	0x0C10	W	0x00000000	GPIO2 filter config register 4
GPIO2_IOC_GRF_GPIO2_FILTER_CON5	0x0C14	W	0x00000000	GPIO2 filter config register 5

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

23.5.3 Detail Registers Description

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GPIO2_IOC_GPIO2A_IOMUX_SEL_0

Address: Operational Base(0x201B8000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x4	gpio2a3_sel 4'h0: GPIO2_A3 4'h1: SDMMC0_D3 4'h2: UART3_TX_M0 4'h3: UART4_CTSN_M3 4'h4: JTAG_TMS_M1 4'h5: EMMC_TESTDATA_OUT
11:8	RW	0x4	gpio2a2_sel 4'h0: GPIO2_A2 4'h1: SDMMC0_D2 4'h2: UART3_RX_M0 4'h3: UART4_RTSN_M3 4'h4: JTAG_TCK_M1 4'h5: EMMC_TESTCLK_OUT 4'h6: TEST_CLK1_OUT
7:4	RW	0x0	gpio2a1_sel 4'h0: GPIO2_A1 4'h1: SDMMC0_D1 4'h2: UART0_TX_M0 4'h3: I2C0_SCL_M1 4'h4: FSPI0_TESTDATA_OUT
3:0	RW	0x0	gpio2a0_sel 4'h0: GPIO2_A0 4'h1: SDMMC0_D0 4'h2: UART0_RX_M0 4'h3: I2C0_SDA_M1 4'h4: FSPI0_TESTCLK_OUT

GPIO2_IOC_GPIO2A_IOMUX_SEL_1

Address: Operational Base(0x201B8000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:4	RW	0x0	gpio2a5_sel 4'h0: GPIO2_A5 4'h1: SDMMC0_CMD 4'h2: UART3_CTSN_M0 4'h3: UART4_TX_M3
3:0	RW	0x0	gpio2a4_sel 4'h0: GPIO2_A4 4'h1: SDMMC0_CLK 4'h2: UART3_RTSN_M0 4'h3: UART4_RX_M3

GPIO2_IOC_GPIO2A_DS_0

Address: Operational Base(0x201B8000) + offset (0x0180)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio2a1_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio2a0_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO2_IOC_GPIO2A_DS_1

Address: Operational Base(0x201B8000) + offset (0x0184)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio2a3_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x0f	gpio2a2_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO2_IOC_GPIO2A_DS_2

Address: Operational Base(0x201B8000) + offset (0x0188)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio2a5_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio2a4_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO2_IOC_GPIO2A_PULL

Address: Operational Base(0x201B8000) + offset (0x0320)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:10	RW	0x2	gpio2a5_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
9:8	RW	0x2	gpio2a4_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
7:6	RW	0x2	gpio2a3_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
5:4	RW	0x2	gpio2a2_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
3:2	RW	0x2	gpio2a1_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
1:0	RW	0x2	gpio2a0_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

GPIO2_IOC_GPIO2A_IE

Address: Operational Base(0x201B8000) + offset (0x0420)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x1	gpio2a5_ie Receiver enable 1'b0: N 1'b1: Y
4	RW	0x1	gpio2a4_ie Receiver enable 1'b0: N 1'b1: Y

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Bit	Attr	Reset Value	Description
3	RW	0x1	gpio2a3_ie Receiver enable 1'b0: N 1'b1: Y
2	RW	0x1	gpio2a2_ie Receiver enable 1'b0: N 1'b1: Y
1	RW	0x1	gpio2a1_ie Receiver enable 1'b0: N 1'b1: Y
0	RW	0x1	gpio2a0_ie Receiver enable 1'b0: N 1'b1: Y

GPIO2_IOC_GPIO2A_SMT

Address: Operational Base(0x201B8000) + offset (0x0520)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x1	gpio2a5_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
4	RW	0x1	gpio2a4_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
3	RW	0x1	gpio2a3_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
2	RW	0x1	gpio2a2_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
1	RW	0x1	gpio2a1_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
0	RW	0x1	gpio2a0_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y

GPIO2_IOC_GPIO2A_SUS

Address: Operational Base(0x201B8000) + offset (0x0620)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	gpio2a5_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
4	RW	0x0	gpio2a4_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
3	RW	0x0	gpio2a3_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
2	RW	0x0	gpio2a2_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
1	RW	0x0	gpio2a1_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
0	RW	0x0	gpio2a0_sus Weak pull keeper for pad 1'b0: N 1'b1: Y

GPIO2_IOC_GPIO2A_SL

Address: Operational Base(0x201B8000) + offset (0x0720)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11:10	RW	0x0	gpio2a5_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
9:8	RW	0x0	gpio2a4_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y

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Bit	Attr	Reset Value	Description
7:6	RW	0x0	gpio2a3_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
5:4	RW	0x0	gpio2a2_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
3:2	RW	0x0	gpio2a1_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
1:0	RW	0x0	gpio2a0_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y

GPIO2_IOC_GPIO2A_OD

Address: Operational Base(0x201B8000) + offset (0x0820)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved
5	RW	0x0	gpio2a5_od For open drain functionality 1'b0: N 1'b1: Y
4	RW	0x0	gpio2a4_od For open drain functionality 1'b0: N 1'b1: Y
3	RW	0x0	gpio2a3_od For open drain functionality 1'b0: N 1'b1: Y
2	RW	0x0	gpio2a2_od For open drain functionality 1'b0: N 1'b1: Y
1	RW	0x0	gpio2a1_od For open drain functionality 1'b0: N 1'b1: Y

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Bit	Attr	Reset Value	Description
0	RW	0x0	gpio2a0_od For open drain functionality 1'b0: N 1'b1: Y

GPIO2_IOC_IO_VSEL

Address: Operational Base(0x201B8000) + offset (0x090C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	vccio2_vd vccio2_vd
14:1	RO	0x0000	reserved
0	RW	0x0	poc_vccio2_iddq VCCIO2 iddq control 1'b0: Disable 1'b1: Enable

GPIO2_IOC_GRF_SDDET_DLY_CON

Address: Operational Base(0x201B8000) + offset (0x0B8C)

Bit	Attr	Reset Value	Description
31:0	RW	0x0003a980	grf_con_sdmmc0_dectn_dly grf_con_sdmmc0_dectn_dly

GPIO2_IOC_GRF_JTAG_CON

Address: Operational Base(0x201B8000) + offset (0x0B90)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x1	grf_sdmmc0_jtag_con sdmmc0 jtag control 1'b0: Disable 1'b1: Enable

GPIO2_IOC_GRF_GPIO2_FILTER_CON0

Address: Operational Base(0x201B8000) + offset (0x0C00)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14:10	RW	0x00	grf_gpio2_filter_sel1 GPIO select to go through first filter logic 5'h00: GPIOxA0 5'h01: GPIOxA1 5'h02: GPIOxA2 5'h03: GPIOxA3 5'h04: GPIOxA4 5'h05: GPIOxA5 5'h06: GPIOxA6 5'h07: GPIOxA7 5'h08: GPIOxB0 5'h09: GPIOxB1 5'h0a: GPIOxB2 5'h0b: GPIOxB3 5'h0c: GPIOxB4 5'h0d: GPIOxB5 5'h0e: GPIOxB6 5'h0f: GPIOxB7 5'h10: GPIOxC0 5'h11: GPIOxC1 5'h12: GPIOxC2 5'h13: GPIOxC3 5'h14: GPIOxC4 5'h15: GPIOxC5 5'h16: GPIOxC6 5'h17: GPIOxC7 5'h18: GPIOxD0 5'h19: GPIOxD1 5'h1a: GPIOxD2 5'h1b: GPIOxD3 5'h1c: GPIOxD4 5'h1d: GPIOxD5 5'h1e: GPIOxD6 5'h1f: GPIOxD7
9	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
8:4	RW	0x00	grf_gpio2_filter_sel0 GPIO select to go through first filter logic 5'h00: GPIOxA0 5'h01: GPIOxA1 5'h02: GPIOxA2 5'h03: GPIOxA3 5'h04: GPIOxA4 5'h05: GPIOxA5 5'h06: GPIOxA6 5'h07: GPIOxA7 5'h08: GPIOxB0 5'h09: GPIOxB1 5'h0a: GPIOxB2 5'h0b: GPIOxB3 5'h0c: GPIOxB4 5'h0d: GPIOxB5 5'h0e: GPIOxB6 5'h0f: GPIOxB7 5'h10: GPIOxC0 5'h11: GPIOxC1 5'h12: GPIOxC2 5'h13: GPIOxC3 5'h14: GPIOxC4 5'h15: GPIOxC5 5'h16: GPIOxC6 5'h17: GPIOxC7 5'h18: GPIOxD0 5'h19: GPIOxD1 5'h1a: GPIOxD2 5'h1b: GPIOxD3 5'h1c: GPIOxD4 5'h1d: GPIOxD5 5'h1e: GPIOxD6 5'h1f: GPIOxD7
3:0	RW	0x0	grf_gpio2_filter_en There are four filter circuits for pad in GPIOx, each bit controls the enable of one filter.

GPIO2_IOC_GRF_GPIO2_FILTER_CON1

Address: Operational Base(0x201B8000) + offset (0x0C04)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14:10	RW	0x00	grf_gpio2_filter_sel3 GPIO select to go through first filter logic 5'h00: GPIOxA0 5'h01: GPIOxA1 5'h02: GPIOxA2 5'h03: GPIOxA3 5'h04: GPIOxA4 5'h05: GPIOxA5 5'h06: GPIOxA6 5'h07: GPIOxA7 5'h08: GPIOxB0 5'h09: GPIOxB1 5'h0a: GPIOxB2 5'h0b: GPIOxB3 5'h0c: GPIOxB4 5'h0d: GPIOxB5 5'h0e: GPIOxB6 5'h0f: GPIOxB7 5'h10: GPIOxC0 5'h11: GPIOxC1 5'h12: GPIOxC2 5'h13: GPIOxC3 5'h14: GPIOxC4 5'h15: GPIOxC5 5'h16: GPIOxC6 5'h17: GPIOxC7 5'h18: GPIOxD0 5'h19: GPIOxD1 5'h1a: GPIOxD2 5'h1b: GPIOxD3 5'h1c: GPIOxD4 5'h1d: GPIOxD5 5'h1e: GPIOxD6 5'h1f: GPIOxD7
9	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
8:4	RW	0x00	grf_gpio2_filter_sel2 GPIO select to go through first filter logic 5'h00: GPIOxA0 5'h01: GPIOxA1 5'h02: GPIOxA2 5'h03: GPIOxA3 5'h04: GPIOxA4 5'h05: GPIOxA5 5'h06: GPIOxA6 5'h07: GPIOxA7 5'h08: GPIOxB0 5'h09: GPIOxB1 5'h0a: GPIOxB2 5'h0b: GPIOxB3 5'h0c: GPIOxB4 5'h0d: GPIOxB5 5'h0e: GPIOxB6 5'h0f: GPIOxB7 5'h10: GPIOxC0 5'h11: GPIOxC1 5'h12: GPIOxC2 5'h13: GPIOxC3 5'h14: GPIOxC4 5'h15: GPIOxC5 5'h16: GPIOxC6 5'h17: GPIOxC7 5'h18: GPIOxD0 5'h19: GPIOxD1 5'h1a: GPIOxD2 5'h1b: GPIOxD3 5'h1c: GPIOxD4 5'h1d: GPIOxD5 5'h1e: GPIOxD6 5'h1f: GPIOxD7
3:0	RO	0x0	reserved

GPIO2_IOC_GRF_GPIO2_FILTER_CON2

Address: Operational Base(0x201B8000) + offset (0x0C08)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio2_filter_count0 Filter counter for first filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

GPIO2_IOC_GRF_GPIO2_FILTER_CON3

Address: Operational Base(0x201B8000) + offset (0x0C0C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio2_filter_count1 Filter counter for second filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

GPIO2_IOC_GRF_GPIO2_FILTER_CON4

Address: Operational Base(0x201B8000) + offset (0x0C10)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
19:0	RW	0x00000	grf_gpio2_filter_count2 Filter counter for third filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

GPIO2_IOC_GRF_GPIO2_FILTER_CON5

Address: Operational Base(0x201B8000) + offset (0x0C14)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio2_filter_count3 Filter counter for fouth filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

23.6 GPIO3_IOC Register Description

23.6.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

23.6.2 Registers Summary

Name	Offset	Size	Reset Value	Description
GPIO3_IOC_GPIO3A_IOMUX_SEL_0	0x0060	W	0x00000000	GPIO3A IOMUX Select Register 0
GPIO3_IOC_GPIO3A_IOMUX_SEL_1	0x0064	W	0x00000000	GPIO3A IOMUX Select Register 1
GPIO3_IOC_GPIO3B_IOMUX_SEL_0	0x0068	W	0x00000000	GPIO3B IOMUX Select Register 0
GPIO3_IOC_GPIO3B_IOMUX_SEL_1	0x006C	W	0x00000000	GPIO3B IOMUX Select Register 1
GPIO3_IOC_GPIO3A_DS_0	0x01C0	W	0x00000F0F	GPIO3A driver strength register 0
GPIO3_IOC_GPIO3A_DS_1	0x01C4	W	0x00000F0F	GPIO3A driver strength register 1
GPIO3_IOC_GPIO3A_DS_2	0x01C8	W	0x00000F0F	GPIO3A driver strength register 2
GPIO3_IOC_GPIO3A_DS_3	0x01CC	W	0x00000F0F	GPIO3A driver strength register 3
GPIO3_IOC_GPIO3B_DS_0	0x01D0	W	0x00000F0F	GPIO3B driver strength register 0
GPIO3_IOC_GPIO3B_DS_1	0x01D4	W	0x00000F0F	GPIO3B driver strength register 1
GPIO3_IOC_GPIO3B_DS_2	0x01D8	W	0x00000F0F	GPIO3B driver strength register 2
GPIO3_IOC_GPIO3B_DS_3	0x01DC	W	0x00000F0F	GPIO3B driver strength register 3
GPIO3_IOC_GPIO3A_PULL	0x0330	W	0x00000000	GPIO3A pull register
GPIO3_IOC_GPIO3B_PULL	0x0334	W	0x00000000	GPIO3B pull register
GPIO3_IOC_GPIO3A_IE	0x0430	W	0x000000FF	GPIO3A input enable register
GPIO3_IOC_GPIO3B_IE	0x0434	W	0x000000FF	GPIO3B input enable register
GPIO3_IOC_GPIO3A_SMT	0x0530	W	0x00000000	GPIO3A receiver enable for schmitter trigger register

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Name	Offset	Size	Reset Value	Description
GPIO3_IOC_GPIO3B_SMT	0x0534	W	0x00000000	GPIO3B receiver enable for schmitter trigger register
GPIO3_IOC_GPIO3A_SUS	0x0630	W	0x00000000	GPIO3A enable weak pull keeper register
GPIO3_IOC_GPIO3B_SUS	0x0634	W	0x00000000	GPIO3B enable weak pull keeper register
GPIO3_IOC_GPIO3A_SL	0x0730	W	0x00000000	GPIO3A slew rate control register
GPIO3_IOC_GPIO3B_SL	0x0734	W	0x00000000	GPIO3B slew rate control register
GPIO3_IOC_GPIO3A_OD	0x0830	W	0x00000000	GPIO3A open drain register
GPIO3_IOC_GPIO3B_OD	0x0834	W	0x00000000	GPIO3B open drain register
GPIO3_IOC_IO3_VSEL	0x0910	W	0x00000000	IO3 iddq register
GPIO3_IOC_IOC_MISC_CON0	0x0A00	W	0x00000000	IOC misc con register 0
GPIO3_IOC_GRF_GPIO3_FILTER_CON0	0x0A04	W	0x00000000	GPIO3 filter config register 0
GPIO3_IOC_GRF_GPIO3_FILTER_CON1	0x0A08	W	0x00000000	GPIO3 filter config register 1
GPIO3_IOC_GRF_GPIO3_FILTER_CON2	0x0A0C	W	0x00000000	GPIO3 filter config register 2
GPIO3_IOC_GRF_GPIO3_FILTER_CON3	0x0A10	W	0x00000000	GPIO3 filter config register 3
GPIO3_IOC_GRF_GPIO3_FILTER_CON4	0x0A14	W	0x00000000	GPIO3 filter config register 4
GPIO3_IOC_GRF_GPIO3_FILTER_CON5	0x0A18	W	0x00000000	GPIO3 filter config register 5

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

23.6.3 Detail Registers Description

GPIO3_IOC_GPIO3A_IOMUX_SEL_0

Address: Operational Base(0x201C0000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio3a3_sel 4'h0: GPIO3_A3 4'h1: SDMMC1_D1 4'h2: I2C1_SDA_M1
11:8	RW	0x0	gpio3a2_sel 4'h0: GPIO3_A2 4'h1: SDMMC1_D0 4'h2: I2C1_SCL_M1
7:4	RW	0x0	gpio3a1_sel 4'h0: GPIO3_A1 4'h1: SDMMC1_CMD
3:0	RW	0x0	gpio3a0_sel 4'h0: GPIO3_A0 4'h1: SDMMC1_CLK

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GPIO3_IOC_GPIO3A_IOMUX_SEL_1

Address: Operational Base(0x201C0000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio3a7_sel 4'h0: GPIO3_A7 4'h4: UART2_CTSN_M0 4'h6: SDMMC1_TESTDATA_OUT
11:8	RW	0x0	gpio3a6_sel 4'h0: GPIO3_A6 4'h4: UART2_RTSN_M0 4'h6: SDMMC1_TESTCLK_OUT
7:4	RW	0x0	gpio3a5_sel 4'h0: GPIO3_A5 4'h1: SDMMC1_D3
3:0	RW	0x0	gpio3a4_sel 4'h0: GPIO3_A4 4'h1: SDMMC1_D2

GPIO3_IOC_GPIO3B_IOMUX_SEL_0

Address: Operational Base(0x201C0000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio3b3_sel 4'h0: GPIO3_B3 4'h1: SPI1_MISO_M1 4'h2: SAI2_SDI0_M0 4'h3: PWM2_CH1_M0 4'h6: PRELIGHT_TRIG_OUT
11:8	RW	0x0	gpio3b2_sel 4'h0: GPIO3_B2 4'h1: SPI1_MOSI_M1 4'h2: SAI2_SDO_M0 4'h3: PWM2_CH0_M0 4'h6: FLASH_TRIG_OUT
7:4	RW	0x0	gpio3b1_sel 4'h0: GPIO3_B1 4'h2: SAI2_SDI2_M0 4'h4: UART2_TX_M0
3:0	RW	0x0	gpio3b0_sel 4'h0: GPIO3_B0 4'h4: UART2_RX_M0

GPIO3_IOC_GPIO3B_IOMUX_SEL_1

Address: Operational Base(0x201C0000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:12	RW	0x0	gpio3b7_sel 4'h0: GPIO3_B7 4'h2: SAI2_SDI1_M0 4'h4: UART1_RX_M1 4'h5: I2C5_SDA_M1
11:8	RW	0x0	gpio3b6_sel 4'h0: GPIO3_B6 4'h1: SPI1_CSN1_M1 4'h2: SAI2_MCLK_M0 4'h3: SDMMC1_DETN 4'h4: UART1_TX_M1 4'h5: I2C5_SCL_M1
7:4	RW	0x0	gpio3b5_sel 4'h0: GPIO3_B5 4'h1: SPI1_CSN0_M1 4'h2: SAI2_LRCK_M0 4'h3: PWM2_CH3_M0 4'h4: UART1_CTSN_M1 4'h5: I2C4_SDA_M0 4'h6: FEPHY_LEDSPD_M0
3:0	RW	0x0	gpio3b4_sel 4'h0: GPIO3_B4 4'h1: SPI1_CLK_M1 4'h2: SAI2_SCLK_M0 4'h3: PWM2_CH2_M0 4'h4: UART1_RTSN_M1 4'h5: I2C4_SCL_M0 4'h6: FEPHY_LEDLINK_M0

GPIO3_IOC_GPIO3A_DS_0

Address: Operational Base(0x201C0000) + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio3a1_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x0f	gpio3a0_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO3_IOC_GPIO3A_DS_1

Address: Operational Base(0x201C0000) + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio3a3_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio3a2_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO3_IOC_GPIO3A_DS_2

Address: Operational Base(0x201C0000) + offset (0x01C8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x0f	gpio3a5_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio3a4_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO3_IOC_GPIO3A_DS_3

Address: Operational Base(0x201C0000) + offset (0x01CC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio3a7_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x0f	gpio3a6_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO3_IOC_GPIO3B_DS_0

Address: Operational Base(0x201C0000) + offset (0x01D0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio3b1_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio3b0_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO3_IOC_GPIO3B_DS_1

Address: Operational Base(0x201C0000) + offset (0x01D4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x0f	gpio3b3_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio3b2_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO3_IOC_GPIO3B_DS_2

Address: Operational Base(0x201C0000) + offset (0x01D8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio3b5_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x0f	gpio3b4_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO3_IOC_GPIO3B_DS_3

Address: Operational Base(0x201C0000) + offset (0x01DC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio3b7_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio3b6_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO3_IOC_GPIO3A_PULL

Address: Operational Base(0x201C0000) + offset (0x0330)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:14	RW	0x0	gpio3a7_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
13:12	RW	0x0	gpio3a6_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
11:10	RW	0x0	gpio3a5_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
9:8	RW	0x0	gpio3a4_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
7:6	RW	0x0	gpio3a3_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
5:4	RW	0x0	gpio3a2_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
3:2	RW	0x0	gpio3a1_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
1:0	RW	0x0	gpio3a0_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

GPIO3_IOC_GPIO3B_PULL

Address: Operational Base(0x201C0000) + offset (0x0334)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:14	RW	0x0	gpio3b7_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
13:12	RW	0x0	gpio3b6_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
11:10	RW	0x0	gpio3b5_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
9:8	RW	0x0	gpio3b4_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
7:6	RW	0x0	gpio3b3_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
5:4	RW	0x0	gpio3b2_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
3:2	RW	0x0	gpio3b1_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
1:0	RW	0x0	gpio3b0_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

GPIO3_IOC_GPIO3A_IE

Address: Operational Base(0x201C0000) + offset (0x0430)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

Bit	Attr	Reset Value	Description
15:8	RO	0x00	reserved
7	RW	0x1	gpio3a7_ie Receiver enable 1'b0: N 1'b1: Y
6	RW	0x1	gpio3a6_ie Receiver enable 1'b0: N 1'b1: Y
5	RW	0x1	gpio3a5_ie Receiver enable 1'b0: N 1'b1: Y
4	RW	0x1	gpio3a4_ie Receiver enable 1'b0: N 1'b1: Y
3	RW	0x1	gpio3a3_ie Receiver enable 1'b0: N 1'b1: Y
2	RW	0x1	gpio3a2_ie Receiver enable 1'b0: N 1'b1: Y
1	RW	0x1	gpio3a1_ie Receiver enable 1'b0: N 1'b1: Y
0	RW	0x1	gpio3a0_ie Receiver enable 1'b0: N 1'b1: Y

GPIO3_IOC_GPIO3B_IE

Address: Operational Base(0x201C0000) + offset (0x0434)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio3b7_ie Receiver enable 1'b0: N 1'b1: Y
6	RW	0x1	gpio3b6_ie Receiver enable 1'b0: N 1'b1: Y
5	RW	0x1	gpio3b5_ie Receiver enable 1'b0: N 1'b1: Y

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Bit	Attr	Reset Value	Description
4	RW	0x1	gpio3b4_ie Receiver enable 1'b0: N 1'b1: Y
3	RW	0x1	gpio3b3_ie Receiver enable 1'b0: N 1'b1: Y
2	RW	0x1	gpio3b2_ie Receiver enable 1'b0: N 1'b1: Y
1	RW	0x1	gpio3b1_ie Receiver enable 1'b0: N 1'b1: Y
0	RW	0x1	gpio3b0_ie Receiver enable 1'b0: N 1'b1: Y

GPIO3_IOC_GPIO3A_SMT

Address: Operational Base(0x201C0000) + offset (0x0530)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio3a7_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
6	RW	0x0	gpio3a6_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
5	RW	0x0	gpio3a5_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
4	RW	0x0	gpio3a4_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
3	RW	0x0	gpio3a3_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
2	RW	0x0	gpio3a2_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y

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Bit	Attr	Reset Value	Description
1	RW	0x0	gpio3a1_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
0	RW	0x0	gpio3a0_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y

GPIO3_IOC_GPIO3B_SMT

Address: Operational Base(0x201C0000) + offset (0x0534)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio3b7_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
6	RW	0x0	gpio3b6_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
5	RW	0x0	gpio3b5_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
4	RW	0x0	gpio3b4_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
3	RW	0x0	gpio3b3_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
2	RW	0x0	gpio3b2_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
1	RW	0x0	gpio3b1_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
0	RW	0x0	gpio3b0_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y

GPIO3_IOC_GPIO3A_SUS

Address: Operational Base(0x201C0000) + offset (0x0630)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio3a7_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
6	RW	0x0	gpio3a6_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
5	RW	0x0	gpio3a5_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
4	RW	0x0	gpio3a4_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
3	RW	0x0	gpio3a3_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
2	RW	0x0	gpio3a2_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
1	RW	0x0	gpio3a1_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
0	RW	0x0	gpio3a0_sus Weak pull keeper for pad 1'b0: N 1'b1: Y

GPIO3_IOC_GPIO3B_SUS

Address: Operational Base(0x201C0000) + offset (0x0634)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio3b7_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
6	RW	0x0	gpio3b6_sus Weak pull keeper for pad 1'b0: N 1'b1: Y

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Bit	Attr	Reset Value	Description
5	RW	0x0	gpio3b5_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
4	RW	0x0	gpio3b4_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
3	RW	0x0	gpio3b3_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
2	RW	0x0	gpio3b2_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
1	RW	0x0	gpio3b1_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
0	RW	0x0	gpio3b0_sus Weak pull keeper for pad 1'b0: N 1'b1: Y

GPIO3_IOC_GPIO3A_SL

Address: Operational Base(0x201C0000) + offset (0x0730)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio3a7_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
13:12	RW	0x0	gpio3a6_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
11:10	RW	0x0	gpio3a5_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
9:8	RW	0x0	gpio3a4_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y

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Bit	Attr	Reset Value	Description
7:6	RW	0x0	gpio3a3_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
5:4	RW	0x0	gpio3a2_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
3:2	RW	0x0	gpio3a1_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
1:0	RW	0x0	gpio3a0_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y

GPIO3_IOC_GPIO3B_SL

Address: Operational Base(0x201C0000) + offset (0x0734)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio3b7_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
13:12	RW	0x0	gpio3b6_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
11:10	RW	0x0	gpio3b5_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
9:8	RW	0x0	gpio3b4_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y

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Bit	Attr	Reset Value	Description
7:6	RW	0x0	gpio3b3_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
5:4	RW	0x0	gpio3b2_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
3:2	RW	0x0	gpio3b1_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
1:0	RW	0x0	gpio3b0_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y

GPIO3_IOC_GPIO3A_OD

Address: Operational Base(0x201C0000) + offset (0x0830)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio3a7_od For open drain functionality 1'b0: N 1'b1: Y
6	RW	0x0	gpio3a6_od For open drain functionality 1'b0: N 1'b1: Y
5	RW	0x0	gpio3a5_od For open drain functionality 1'b0: N 1'b1: Y
4	RW	0x0	gpio3a4_od For open drain functionality 1'b0: N 1'b1: Y
3	RW	0x0	gpio3a3_od For open drain functionality 1'b0: N 1'b1: Y

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Bit	Attr	Reset Value	Description
2	RW	0x0	gpio3a2_od For open drain functionality 1'b0: N 1'b1: Y
1	RW	0x0	gpio3a1_od For open drain functionality 1'b0: N 1'b1: Y
0	RW	0x0	gpio3a0_od For open drain functionality 1'b0: N 1'b1: Y

GPIO3_IOC_GPIO3B_OD

Address: Operational Base(0x201C0000) + offset (0x0834)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio3b7_od For open drain functionality 1'b0: N 1'b1: Y
6	RW	0x0	gpio3b6_od For open drain functionality 1'b0: N 1'b1: Y
5	RW	0x0	gpio3b5_od For open drain functionality 1'b0: N 1'b1: Y
4	RW	0x0	gpio3b4_od For open drain functionality 1'b0: N 1'b1: Y
3	RW	0x0	gpio3b3_od For open drain functionality 1'b0: N 1'b1: Y
2	RW	0x0	gpio3b2_od For open drain functionality 1'b0: N 1'b1: Y
1	RW	0x0	gpio3b1_od For open drain functionality 1'b0: N 1'b1: Y
0	RW	0x0	gpio3b0_od For open drain functionality 1'b0: N 1'b1: Y

GPIO3_IOC_IO3_VSEL

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Address: Operational Base(0x201C0000) + offset (0x0910)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	vccio3_vd VCCIO hardware voltage status 1'b0: 1.8V 1'b1: 3.3V
14:1	RO	0x0000	reserved
0	RW	0x0	poc_vccio3_iddq VCCIO3 iddq control 1'b0: Disable 1'b1: Enable

GPIO3_IOC_IOC_MISC_CON0

Address: Operational Base(0x201C0000) + offset (0x0A00)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	grf_sdmmc1_detn_masked_pin_pol sdmmc1 masked pin input pol. 1'b0: polarity orignal. 1'b1: polarity opposite
0	RW	0x0	grf_sdmmc1_detn_enable sdmmc1 detectn enable 1'b1: enable 1'b0: disable

GPIO3_IOC_GRF_GPIO3_FILTER_CON0

Address: Operational Base(0x201C0000) + offset (0x0A04)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14:10	RW	0x00	grf_gpio3_filter_sel1 5'h00: gpio3A0 5'h01: gpio3A1 5'h02: gpio3A2 5'h03: gpio3A3 5'h04: gpio3A4 5'h05: gpio3A5 5'h06: gpio3A6 5'h07: gpio3A7 5'h08: gpio3B0 5'h09: gpio3B1 5'h0a: gpio3B2 5'h0b: gpio3B3 5'h0c: gpio3B4 5'h0d: gpio3B5 5'h0e: gpio3B6 5'h0f: gpio3B7 5'h10: 0 5'h11: 0 5'h12: 0 5'h13: 0 5'h14: 0 5'h15: 0 5'h16: 0 5'h17: 0 5'h18: 0
9	RO	0x0	reserved
8:4	RW	0x00	grf_gpio3_filter_sel0 5'h00: gpio3A0 5'h01: gpio3A1 5'h02: gpio3A2 5'h03: gpio3A3 5'h04: gpio3A4 5'h05: gpio3A5 5'h06: gpio3A6 5'h07: gpio3A7 5'h08: gpio3B0 5'h09: gpio3B1 5'h0a: gpio3B2 5'h0b: gpio3B3 5'h0c: gpio3B4 5'h0d: gpio3B5 5'h0e: gpio3B6 5'h0f: gpio3B7 5'h10: 0 5'h11: 0 5'h12: 0 5'h13: 0 5'h14: 0 5'h15: 0 5'h16: 0 5'h17: 0 5'h18: 0
3:0	RW	0x0	grf_gpio3_filter_en There are 4 filter circuits for pad in gpio3, each bit controls the enable of one filter.

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GPIO3_IOC_GRF_GPIO3_FILTER_CON1

Address: Operational Base(0x201C0000) + offset (0x0A08)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:10	RW	0x00	grf_gpio3_filter_sel3 5'h00: gpio3A0 5'h01: gpio3A1 5'h02: gpio3A2 5'h03: gpio3A3 5'h04: gpio3A4 5'h05: gpio3A5 5'h06: gpio3A6 5'h07: gpio3A7 5'h08: gpio3B0 5'h09: gpio3B1 5'h0a: gpio3B2 5'h0b: gpio3B3 5'h0c: gpio3B4 5'h0d: gpio3B5 5'h0e: gpio3B6 5'h0f: gpio3B7 5'h10: 0 5'h11: 0 5'h12: 0 5'h13: 0 5'h14: 0 5'h15: 0 5'h16: 0 5'h17: 0 5'h18: 0
9	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
8:4	RW	0x00	grf_gpio3_filter_sel2 5'h00: gpio3A0 5'h01: gpio3A1 5'h02: gpio3A2 5'h03: gpio3A3 5'h04: gpio3A4 5'h05: gpio3A5 5'h06: gpio3A6 5'h07: gpio3A7 5'h08: gpio3B0 5'h09: gpio3B1 5'h0a: gpio3B2 5'h0b: gpio3B3 5'h0c: gpio3B4 5'h0d: gpio3B5 5'h0e: gpio3B6 5'h0f: gpio3B7 5'h10: 0 5'h11: 0 5'h12: 0 5'h13: 0 5'h14: 0 5'h15: 0 5'h16: 0 5'h17: 0 5'h18: 0
3:0	RO	0x0	reserved

GPIO3_IOC_GRF_GPIO3_FILTER_CON2

Address: Operational Base(0x201C0000) + offset (0x0A0C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio3_filter_count0 Filter counter for first filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

GPIO3_IOC_GRF_GPIO3_FILTER_CON3

Address: Operational Base(0x201C0000) + offset (0x0A10)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio3_filter_count1 Filter counter for first filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

GPIO3_IOC_GRF_GPIO3_FILTER_CON4

Address: Operational Base(0x201C0000) + offset (0x0A14)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio3_filter_count2 Filter counter for first filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

GPIO3_IOC_GRF_GPIO3_FILTER_CON5

Address: Operational Base(0x201C0000) + offset (0x0A18)

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Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio3_filter_count3 Filter counter for first filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

23.7 GPIO4_IOC Register Description

23.7.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

23.7.2 Registers Summary

Name	Offset	Size	Reset Value	Description
GPIO4_IOC_GPIO4A_IOMUX_SEL_0	0x0080	W	0x00000000	GPIO4A IOMUX Select Register 0
GPIO4_IOC_GPIO4A_IOMUX_SEL_1	0x0084	W	0x00000000	GPIO4A IOMUX Select Register 1
GPIO4_IOC_GPIO4B_IOMUX_SEL_0	0x0088	W	0x00000000	GPIO4B IOMUX Select Register 0
GPIO4_IOC_GPIO4A_DS_0	0x0200	W	0x00000F0F	GPIO4A driver strength register 0
GPIO4_IOC_GPIO4A_DS_1	0x0204	W	0x00000F0F	GPIO4A driver strength register 1
GPIO4_IOC_GPIO4A_DS_2	0x0208	W	0x00000F0F	GPIO4A driver strength register 2
GPIO4_IOC_GPIO4A_DS_3	0x020C	W	0x00000F0F	GPIO4A driver strength register 3
GPIO4_IOC_GPIO4B_DS_0	0x0210	W	0x00000F0F	GPIO4B driver strength register 0
GPIO4_IOC_GPIO4A_PULL	0x0340	W	0x0000AAA5	GPIO4A pull register
GPIO4_IOC_GPIO4B_PULL	0x0344	W	0x0000000A	GPIO4B pull register
GPIO4_IOC_GPIO4A_IE	0x0440	W	0x000000FF	GPIO4A input enable register
GPIO4_IOC_GPIO4B_IE	0x0444	W	0x00000003	GPIO4B input enable register
GPIO4_IOC_GPIO4A_SMT	0x0540	W	0x000000FF	GPIO4A receiver enable for schmitter trigger register
GPIO4_IOC_GPIO4B_SMT	0x0544	W	0x00000003	GPIO4B receiver enable for schmitter trigger register
GPIO4_IOC_GPIO4A_SUS	0x0640	W	0x00000000	GPIO4A enable weak pull keeper register
GPIO4_IOC_GPIO4B_SUS	0x0644	W	0x00000000	GPIO4B enable weak pull keeper register
GPIO4_IOC_GPIO4A_SL	0x0740	W	0x00000000	GPIO4A slew rate control register
GPIO4_IOC_GPIO4B_SL	0x0744	W	0x00000000	GPIO4B slew rate control register
GPIO4_IOC_GPIO4A_OD	0x0840	W	0x00000000	GPIO4A open drain register
GPIO4_IOC_GPIO4B_OD	0x0844	W	0x00000000	GPIO4B open drain register
GPIO4_IOC_IO_VSEL	0x0914	W	0x00000000	IO iddq register

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Name	Offset	Size	Reset Value	Description
GPIO4_IOC_GRF_GPIO4_FILTER_CON0	0x0C20	W	0x00000000	GPIO4 filter config register 0
GPIO4_IOC_GRF_GPIO4_FILTER_CON1	0x0C24	W	0x00000000	GPIO4 filter config register 1
GPIO4_IOC_GRF_GPIO4_FILTER_CON2	0x0C28	W	0x00000000	GPIO4 filter config register 2
GPIO4_IOC_GRF_GPIO4_FILTER_CON3	0x0C2C	W	0x00000000	GPIO4 filter config register 3
GPIO4_IOC_GRF_GPIO4_FILTER_CON4	0x0C30	W	0x00000000	GPIO4 filter config register 4
GPIO4_IOC_GRF_GPIO4_FILTER_CON5	0x0C34	W	0x00000000	GPIO4 filter config register 5

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

23.7.3 Detail Registers Description

GPIO4_IOC_GPIO4A_IOMUX_SEL_0

Address: Operational Base(0x201C8000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio4a3_sel 4'h0: GPIO4_A3 4'h1: SPI0_CSN1_M1 4'h2: SAI1_MCLK_M1 4'h4: PWM0_CH5_M1 4'h5: UART4_TX_M0
11:8	RW	0x0	gpio4a2_sel 4'h0: GPIO4_A2 4'h4: PWM0_CH4_M1 4'h5: UART4_RX_M0
7:4	RW	0x0	gpio4a1_sel 4'h0: GPIO4_A1 4'h3: CAM_CLK2_OUT 4'h5: UART4_CTSN_M0 4'h6: I2C1_SCL_M2
3:0	RW	0x0	gpio4a0_sel 4'h0: GPIO4_A0 4'h3: CAM_CLK3_OUT 4'h5: UART4_RTSN_M0 4'h6: I2C1_SDA_M2

GPIO4_IOC_GPIO4A_IOMUX_SEL_1

Address: Operational Base(0x201C8000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:12	RW	0x0	gpio4a7_sel 4'h0: GPIO4_A7 4'h1: SPI0_CLK_M1 4'h2: SAI1_SDO_M1 4'h4: PWM0_CH7_M1 4'h5: UART5_RX_M0 4'h6: I2C4_SCL_M2
11:8	RW	0x0	gpio4a6_sel 4'h0: GPIO4_A6 4'h1: SPI0_CSN0_M1 4'h2: SAI1_SDI_M1 4'h4: PWM0_CH6_M1 4'h5: UART5_TX_M0 4'h6: I2C4_SDA_M2
7:4	RW	0x0	gpio4a5_sel 4'h0: GPIO4_A5 4'h1: SPI0_MISO_M1 4'h2: SAI1_LRCK_M1 4'h6: I2C3_SDA_M1
3:0	RW	0x0	gpio4a4_sel 4'h0: GPIO4_A4 4'h1: SPI0_MOSI_M1 4'h2: SAI1_SCLK_M1 4'h6: I2C3_SCL_M1

GPIO4_IOC_GPIO4B_IOMUX_SEL_0

Address: Operational Base(0x201C8000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:4	RW	0x0	gpio4b1_sel 4'h0: GPIO4_B1 4'h3: CAM_CLK0_OUT 4'h5: UART5_CTSN_M0
3:0	RW	0x0	gpio4b0_sel 4'h0: GPIO4_B0 4'h3: CAM_CLK1_OUT 4'h5: UART5_RTSN_M0

GPIO4_IOC_GPIO4A_DS_0

Address: Operational Base(0x201C8000) + offset (0x0200)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x0f	gpio4a1_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio4a0_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO4_IOC_GPIO4A_DS_1

Address: Operational Base(0x201C8000) + offset (0x0204)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio4a3_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x0f	gpio4a2_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO4_IOC_GPIO4A_DS_2

Address: Operational Base(0x201C8000) + offset (0x0208)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio4a5_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio4a4_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO4_IOC_GPIO4A_DS_3

Address: Operational Base(0x201C8000) + offset (0x020C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:8	RW	0x0f	gpio4a7_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio4a6_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO4_IOC_GPIO4B_DS_0

Address: Operational Base(0x201C8000) + offset (0x0210)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio4b1_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x0f	gpio4b0_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO4_IOC_GPIO4A_PULL

Address: Operational Base(0x201C8000) + offset (0x0340)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	gpio4a7_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
13:12	RW	0x2	gpio4a6_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
11:10	RW	0x2	gpio4a5_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
9:8	RW	0x2	gpio4a4_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
7:6	RW	0x2	gpio4a3_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
5:4	RW	0x2	gpio4a2_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

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Bit	Attr	Reset Value	Description
3:2	RW	0x1	gpio4a1_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
1:0	RW	0x1	gpio4a0_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

GPIO4_IOC_GPIO4B_PULL

Address: Operational Base(0x201C8000) + offset (0x0344)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3:2	RW	0x2	gpio4b1_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
1:0	RW	0x2	gpio4b0_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

GPIO4_IOC_GPIO4A_IE

Address: Operational Base(0x201C8000) + offset (0x0440)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio4a7_ie Receiver enable 1'b0: N 1'b1: Y
6	RW	0x1	gpio4a6_ie Receiver enable 1'b0: N 1'b1: Y
5	RW	0x1	gpio4a5_ie Receiver enable 1'b0: N 1'b1: Y

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Bit	Attr	Reset Value	Description
4	RW	0x1	gpio4a4_ie Receiver enable 1'b0: N 1'b1: Y
3	RW	0x1	gpio4a3_ie Receiver enable 1'b0: N 1'b1: Y
2	RW	0x1	gpio4a2_ie Receiver enable 1'b0: N 1'b1: Y
1	RW	0x1	gpio4a1_ie Receiver enable 1'b0: N 1'b1: Y
0	RW	0x1	gpio4a0_ie Receiver enable 1'b0: N 1'b1: Y

GPIO4_IOC_GPIO4B_IE

Address: Operational Base(0x201C8000) + offset (0x0444)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x1	gpio4b1_ie Receiver enable 1'b0: N 1'b1: Y
0	RW	0x1	gpio4b0_ie Receiver enable 1'b0: N 1'b1: Y

GPIO4_IOC_GPIO4A_SMT

Address: Operational Base(0x201C8000) + offset (0x0540)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio4a7_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
6	RW	0x1	gpio4a6_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y

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Bit	Attr	Reset Value	Description
5	RW	0x1	gpio4a5_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
4	RW	0x1	gpio4a4_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
3	RW	0x1	gpio4a3_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
2	RW	0x1	gpio4a2_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
1	RW	0x1	gpio4a1_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
0	RW	0x1	gpio4a0_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y

GPIO4_IOC_GPIO4B_SMT

Address: Operational Base(0x201C8000) + offset (0x0544)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x1	gpio4b1_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
0	RW	0x1	gpio4b0_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y

GPIO4_IOC_GPIO4A_SUS

Address: Operational Base(0x201C8000) + offset (0x0640)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio4a7_sus Weak pull keeper for pad 1'b0: N 1'b1: Y

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Bit	Attr	Reset Value	Description
6	RW	0x0	gpio4a6_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
5	RW	0x0	gpio4a5_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
4	RW	0x0	gpio4a4_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
3	RW	0x0	gpio4a3_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
2	RW	0x0	gpio4a2_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
1	RW	0x0	gpio4a1_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
0	RW	0x0	gpio4a0_sus Weak pull keeper for pad 1'b0: N 1'b1: Y

GPIO4_IOC_GPIO4B_SUS

Address: Operational Base(0x201C8000) + offset (0x0644)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	gpio4b1_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
0	RW	0x0	gpio4b0_sus Weak pull keeper for pad 1'b0: N 1'b1: Y

GPIO4_IOC_GPIO4A_SL

Address: Operational Base(0x201C8000) + offset (0x0740)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:14	RW	0x0	gpio4a7_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
13:12	RW	0x0	gpio4a6_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
11:10	RW	0x0	gpio4a5_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
9:8	RW	0x0	gpio4a4_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
7:6	RW	0x0	gpio4a3_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
5:4	RW	0x0	gpio4a2_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
3:2	RW	0x0	gpio4a1_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
1:0	RW	0x0	gpio4a0_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y

GPIO4_IOC_GPIO4B_SL

Address: Operational Base(0x201C8000) + offset (0x0744)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:4	RO	0x000	reserved
3:2	RW	0x0	gpio4b1_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
1:0	RW	0x0	gpio4b0_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y

GPIO4_IOC_GPIO4A_OD

Address: Operational Base(0x201C8000) + offset (0x0840)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio4a7_od For open drain functionality 1'b0: N 1'b1: Y
6	RW	0x0	gpio4a6_od For open drain functionality 1'b0: N 1'b1: Y
5	RW	0x0	gpio4a5_od For open drain functionality 1'b0: N 1'b1: Y
4	RW	0x0	gpio4a4_od For open drain functionality 1'b0: N 1'b1: Y
3	RW	0x0	gpio4a3_od For open drain functionality 1'b0: N 1'b1: Y
2	RW	0x0	gpio4a2_od For open drain functionality 1'b0: N 1'b1: Y
1	RW	0x0	gpio4a1_od For open drain functionality 1'b0: N 1'b1: Y
0	RW	0x0	gpio4a0_od For open drain functionality 1'b0: N 1'b1: Y

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GPIO4_IOC_GPIO4B_OD

Address: Operational Base(0x201C8000) + offset (0x0844)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	gpio4b1_od For open drain functionality 1'b0: N 1'b1: Y
0	RW	0x0	gpio4b0_od For open drain functionality 1'b0: N 1'b1: Y

GPIO4_IOC_IO_VSEL

Address: Operational Base(0x201C8000) + offset (0x0914)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	vccio4_vd vccio4_vd
14:1	RO	0x0000	reserved
0	RW	0x0	poc_vccio4_iddq VCCIO4 iddq control 1'b0: Disable 1'b1: Enable

GPIO4_IOC_GRF_GPIO4_FILTER_CON0

Address: Operational Base(0x201C8000) + offset (0x0C20)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14:10	RW	0x00	grf_gpio4_filter_sel1 GPIO select to go through first filter logic 5'h00: GPIOxA0 5'h01: GPIOxA1 5'h02: GPIOxA2 5'h03: GPIOxA3 5'h04: GPIOxA4 5'h05: GPIOxA5 5'h06: GPIOxA6 5'h07: GPIOxA7 5'h08: GPIOxB0 5'h09: GPIOxB1 5'h0a: GPIOxB2 5'h0b: GPIOxB3 5'h0c: GPIOxB4 5'h0d: GPIOxB5 5'h0e: GPIOxB6 5'h0f: GPIOxB7 5'h10: GPIOxC0 5'h11: GPIOxC1 5'h12: GPIOxC2 5'h13: GPIOxC3 5'h14: GPIOxC4 5'h15: GPIOxC5 5'h16: GPIOxC6 5'h17: GPIOxC7 5'h18: GPIOxD0 5'h19: GPIOxD1 5'h1a: GPIOxD2 5'h1b: GPIOxD3 5'h1c: GPIOxD4 5'h1d: GPIOxD5 5'h1e: GPIOxD6 5'h1f: GPIOxD7
9	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
8:4	RW	0x00	grf_gpio4_filter_sel0 GPIO select to go through first filter logic 5'h00: GPIOxA0 5'h01: GPIOxA1 5'h02: GPIOxA2 5'h03: GPIOxA3 5'h04: GPIOxA4 5'h05: GPIOxA5 5'h06: GPIOxA6 5'h07: GPIOxA7 5'h08: GPIOxB0 5'h09: GPIOxB1 5'h0a: GPIOxB2 5'h0b: GPIOxB3 5'h0c: GPIOxB4 5'h0d: GPIOxB5 5'h0e: GPIOxB6 5'h0f: GPIOxB7 5'h10: GPIOxC0 5'h11: GPIOxC1 5'h12: GPIOxC2 5'h13: GPIOxC3 5'h14: GPIOxC4 5'h15: GPIOxC5 5'h16: GPIOxC6 5'h17: GPIOxC7 5'h18: GPIOxD0 5'h19: GPIOxD1 5'h1a: GPIOxD2 5'h1b: GPIOxD3 5'h1c: GPIOxD4 5'h1d: GPIOxD5 5'h1e: GPIOxD6 5'h1f: GPIOxD7
3:0	RW	0x0	grf_gpio4_filter_en There are four filter circuits for pad in GPIOx, each bit controls the enable of one filter.

GPIO4_IOC_GRF_GPIO4_FILTER_CON1

Address: Operational Base(0x201C8000) + offset (0x0C24)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14:10	RW	0x00	grf_gpio4_filter_sel3 GPIO select to go through first filter logic 5'h00: GPIOxA0 5'h01: GPIOxA1 5'h02: GPIOxA2 5'h03: GPIOxA3 5'h04: GPIOxA4 5'h05: GPIOxA5 5'h06: GPIOxA6 5'h07: GPIOxA7 5'h08: GPIOxB0 5'h09: GPIOxB1 5'h0a: GPIOxB2 5'h0b: GPIOxB3 5'h0c: GPIOxB4 5'h0d: GPIOxB5 5'h0e: GPIOxB6 5'h0f: GPIOxB7 5'h10: GPIOxC0 5'h11: GPIOxC1 5'h12: GPIOxC2 5'h13: GPIOxC3 5'h14: GPIOxC4 5'h15: GPIOxC5 5'h16: GPIOxC6 5'h17: GPIOxC7 5'h18: GPIOxD0 5'h19: GPIOxD1 5'h1a: GPIOxD2 5'h1b: GPIOxD3 5'h1c: GPIOxD4 5'h1d: GPIOxD5 5'h1e: GPIOxD6 5'h1f: GPIOxD7
9	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
8:4	RW	0x00	grf_gpio4_filter_sel2 GPIO select to go through first filter logic 5'h00: GPIOxA0 5'h01: GPIOxA1 5'h02: GPIOxA2 5'h03: GPIOxA3 5'h04: GPIOxA4 5'h05: GPIOxA5 5'h06: GPIOxA6 5'h07: GPIOxA7 5'h08: GPIOxB0 5'h09: GPIOxB1 5'h0a: GPIOxB2 5'h0b: GPIOxB3 5'h0c: GPIOxB4 5'h0d: GPIOxB5 5'h0e: GPIOxB6 5'h0f: GPIOxB7 5'h10: GPIOxC0 5'h11: GPIOxC1 5'h12: GPIOxC2 5'h13: GPIOxC3 5'h14: GPIOxC4 5'h15: GPIOxC5 5'h16: GPIOxC6 5'h17: GPIOxC7 5'h18: GPIOxD0 5'h19: GPIOxD1 5'h1a: GPIOxD2 5'h1b: GPIOxD3 5'h1c: GPIOxD4 5'h1d: GPIOxD5 5'h1e: GPIOxD6 5'h1f: GPIOxD7
3:0	RO	0x0	reserved

GPIO4_IOC_GRF_GPIO4_FILTER_CON2

Address: Operational Base(0x201C8000) + offset (0x0C28)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio4_filter_count0 Filter counter for first filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

GPIO4_IOC_GRF_GPIO4_FILTER_CON3

Address: Operational Base(0x201C8000) + offset (0x0C2C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio4_filter_count1 Filter counter for second filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

GPIO4_IOC_GRF_GPIO4_FILTER_CON4

Address: Operational Base(0x201C8000) + offset (0x0C30)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
19:0	RW	0x00000	grf_gpio4_filter_count2 Filter counter for third filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

GPIO4_IOC_GRF_GPIO4_FILTER_CON5

Address: Operational Base(0x201C8000) + offset (0x0C34)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio4_filter_count3 Filter counter for fouth filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

23.8 GPIO5_IOC Register Description

23.8.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

23.8.2 Registers Summary

Name	Offset	Size	Reset Value	Description
GPIO5_IOC_GPIO5A_IOMUX_SEL_0	0x00A0	W	0x00000000	GPIO5A IOMUX Select Register 0
GPIO5_IOC_GPIO5A_IOMUX_SEL_1	0x00A4	W	0x00000000	GPIO5A IOMUX Select Register 1
GPIO5_IOC_GPIO5B_IOMUX_SEL_0	0x00A8	W	0x00000000	GPIO5B IOMUX Select Register 0
GPIO5_IOC_GPIO5B_IOMUX_SEL_1	0x00AC	W	0x00000000	GPIO5B IOMUX Select Register 1
GPIO5_IOC_GPIO5C_IOMUX_SEL_0	0x00B0	W	0x00000000	GPIO5C IOMUX Select Register 0
GPIO5_IOC_GPIO5C_IOMUX_SEL_1	0x00B4	W	0x00000000	GPIO5C IOMUX Select Register 1
GPIO5_IOC_GPIO5D_IOMUX_SEL_0	0x00B8	W	0x00000000	GPIO5D IOMUX Select Register 0
GPIO5_IOC_GPIO5D_IOMUX_SEL_1	0x00BC	W	0x00000000	GPIO5D IOMUX Select Register 1
GPIO5_IOC_GPIO5A_DS_0	0x0240	W	0x00000F0F	GPIO5A driver strength register 0
GPIO5_IOC_GPIO5A_DS_1	0x0244	W	0x00000F0F	GPIO5A driver strength register 1
GPIO5_IOC_GPIO5A_DS_2	0x0248	W	0x00000F0F	GPIO5A driver strength register 2
GPIO5_IOC_GPIO5A_DS_3	0x024C	W	0x00000F0F	GPIO5A driver strength register 3
GPIO5_IOC_GPIO5B_DS_0	0x0250	W	0x00000F0F	GPIO5B driver strength register 0
GPIO5_IOC_GPIO5B_DS_1	0x0254	W	0x00000F0F	GPIO5B driver strength register 1
GPIO5_IOC_GPIO5B_DS_2	0x0258	W	0x00000F0F	GPIO5B driver strength register 2
GPIO5_IOC_GPIO5B_DS_3	0x025C	W	0x00000F0F	GPIO5B driver strength register 3
GPIO5_IOC_GPIO5C_DS_0	0x0260	W	0x00000F0F	GPIO5C driver strength register 0

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Name	Offset	Size	Reset Value	Description
GPIO5_IOC_GPIO5C_DS_1	0x0264	W	0x00000F0F	GPIO5C driver strength register 1
GPIO5_IOC_GPIO5C_DS_2	0x0268	W	0x00000F0F	GPIO5C driver strength register 2
GPIO5_IOC_GPIO5C_DS_3	0x026C	W	0x00000F0F	GPIO5C driver strength register 3
GPIO5_IOC_GPIO5D_DS_0	0x0270	W	0x00000F0F	GPIO5D driver strength register 0
GPIO5_IOC_GPIO5D_DS_1	0x0274	W	0x00000F0F	GPIO5D driver strength register 1
GPIO5_IOC_GPIO5D_DS_2	0x0278	W	0x00000F0F	GPIO5D driver strength register 2
GPIO5_IOC_GPIO5D_DS_3	0x027C	W	0x00000F0F	GPIO5D driver strength register 3
GPIO5_IOC_GPIO5A_PULL	0x0350	W	0x0000AAAA	GPIO5A pull register
GPIO5_IOC_GPIO5B_PULL	0x0354	W	0x0000AAAA	GPIO5B pull register
GPIO5_IOC_GPIO5C_PULL	0x0358	W	0x0000AAAA	GPIO5C pull register
GPIO5_IOC_GPIO5D_PULL	0x035C	W	0x000055AA	GPIO5D pull register
GPIO5_IOC_GPIO5A_IE	0x0450	W	0x000000FF	GPIO5A input enable register
GPIO5_IOC_GPIO5B_IE	0x0454	W	0x000000FF	GPIO5B input enable register
GPIO5_IOC_GPIO5C_IE	0x0458	W	0x000000FF	GPIO5C input enable register
GPIO5_IOC_GPIO5D_IE	0x045C	W	0x000000FF	GPIO5D input enable register
GPIO5_IOC_GPIO5A_SMT	0x0550	W	0x000000FF	GPIO5A receiver enable for schmitter trigger register
GPIO5_IOC_GPIO5B_SMT	0x0554	W	0x000000FF	GPIO5B receiver enable for schmitter trigger register
GPIO5_IOC_GPIO5C_SMT	0x0558	W	0x000000FF	GPIO5C receiver enable for schmitter trigger register
GPIO5_IOC_GPIO5D_SMT	0x055C	W	0x000000FF	GPIO5D receiver enable for schmitter trigger register
GPIO5_IOC_GPIO5A_SUS	0x0650	W	0x00000000	GPIO5A enable weak pull keeper register
GPIO5_IOC_GPIO5B_SUS	0x0654	W	0x00000000	GPIO5B enable weak pull keeper register
GPIO5_IOC_GPIO5C_SUS	0x0658	W	0x00000000	GPIO5C enable weak pull keeper register
GPIO5_IOC_GPIO5D_SUS	0x065C	W	0x00000000	GPIO5D enable weak pull keeper register
GPIO5_IOC_GPIO5A_SL	0x0750	W	0x00000000	GPIO5A slew rate control register
GPIO5_IOC_GPIO5B_SL	0x0754	W	0x00000000	GPIO5B slew rate control register
GPIO5_IOC_GPIO5C_SL	0x0758	W	0x00000000	GPIO5C slew rate control register
GPIO5_IOC_GPIO5D_SL	0x075C	W	0x00000000	GPIO5D slew rate control register

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Name	Offset	Size	Reset Value	Description
GPIO5_IOC_GPIO5A_OD	0x0850	W	0x00000000	GPIO5A open drain register
GPIO5_IOC_GPIO5B_OD	0x0854	W	0x00000000	GPIO5B open drain register
GPIO5_IOC_GPIO5C_OD	0x0858	W	0x00000000	GPIO5C open drain register
GPIO5_IOC_GPIO5D_OD	0x085C	W	0x00000000	GPIO5D open drain register
GPIO5_IOC_IO_VSEL	0x0918	W	0x00000000	IO iddq register
GPIO5_IOC_GRF_VICIF_M1_CON	0x0B98	W	0x00000000	vi cif m1 con register
GPIO5_IOC_GRF_VOP_LCDC_CON	0x0B9C	W	0x00000000	vop lcdc con register
GPIO5_IOC_GRF_GMACIO_M1_CON0	0x0BA8	W	0x00000000	gmacio m1 con0 register
GPIO5_IOC_GRF_GMACIO_M1_CON1	0x0BAC	W	0x00000000	gmacio m1 con1 register
GPIO5_IOC_GRF_UART0_DLY_CON	0x0BB0	W	0x0003A980	uart0 delay con register
GPIO5_IOC_GRF_UART_JTAG_CON	0x0BB4	W	0x00000000	uart jtag con register
GPIO5_IOC_GRF_GPIO5_FILTER_CON0	0x0C40	W	0x00000000	GPIO5 filter config register 0
GPIO5_IOC_GRF_GPIO5_FILTER_CON1	0x0C44	W	0x00000000	GPIO5 filter config register 1
GPIO5_IOC_GRF_GPIO5_FILTER_CON2	0x0C48	W	0x00000000	GPIO5 filter config register 2
GPIO5_IOC_GRF_GPIO5_FILTER_CON3	0x0C4C	W	0x00000000	GPIO5 filter config register 3
GPIO5_IOC_GRF_GPIO5_FILTER_CON4	0x0C50	W	0x00000000	GPIO5 filter config register 4
GPIO5_IOC_GRF_GPIO5_FILTER_CON5	0x0C54	W	0x00000000	GPIO5 filter config register 5

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

23.8.3 Detail Registers Description

GPIO5_IOC_GPIO5A_IOMUX_SEL_0

Address: Operational Base(0x201D0000) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio5a3_sel 4'h0: GPIO5_A3 4'h1: VO_LCDC_D3 4'h2: SPI0_CSN0_M2 4'h4: DSMC_D14 4'h5: SAI2_MCLK_M1 4'h7: PWM0_CH4_M2 4'h8: UART4_RX_M1

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Bit	Attr	Reset Value	Description
11:8	RW	0x0	gpio5a2_sel 4'h0: GPIO5_A2 4'h1: VO_LCDC_D2 4'h2: ETH_PPSCLK_M1 4'h3: VI_CIF_D2_M1 4'h4: DSMC_D15 4'h5: SAI2_SDI1_M1 4'h7: PWM0_CH5_M2 4'h8: UART4_TX_M1
7:4	RW	0x0	gpio5a1_sel 4'h0: GPIO5_A1 4'h1: VO_LCDC_D1 4'h2: I2C5_SCL_M2 4'h3: VI_CIF_D1_M1 4'h4: DSMC_DQS1 4'h5: SAI2_SDI2_M1 4'h6: IR_FPA_SDA1 4'h7: PWM2_CH5_M0 4'h8: UART4_CTSN_M1
3:0	RW	0x0	gpio5a0_sel 4'h0: GPIO5_A0 4'h1: VO_LCDC_D0 4'h2: ETH_TXD3_M1 4'h3: VI_CIF_D0_M1 4'h4: DSMC_CSN1 4'h6: IR_FPA_SDA0 4'h7: PWM2_CH4_M0 4'h8: UART4_RTSN_M1

GPIO5_IOC_GPIO5A_IOMUX_SEL_1

Address: Operational Base(0x201D0000) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio5a7_sel 4'h0: GPIO5_A7 4'h1: VO_LCDC_D7 4'h2: SPI0_CSN1_M2 4'h3: VI_CIF_D3_M1 4'h4: DSMC_D10 4'h5: SAI2_LRCK_M1 4'h6: I2C5_SDA_M2 4'h7: PWM0_CH0_M1 4'h8: UART5_CTSN_M1
11:8	RW	0x0	gpio5a6_sel 4'h0: GPIO5_A6 4'h1: VO_LCDC_D6 4'h2: SPI0_CLK_M2 4'h4: DSMC_D11 4'h5: SAI2_SDI0_M1 4'h7: PWM0_CH1_M1 4'h8: UART5_RTSN_M1

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	gpio5a5_sel 4'h0: GPIO5_A5 4'h1: VO_LCDC_D5 4'h2: SPI0_MISO_M2 4'h4: DSMC_D12 4'h5: SAI2_SCLK_M1 4'h7: PWM0_CH2_M1 4'h8: UART5_RX_M1
3:0	RW	0x0	gpio5a4_sel 4'h0: GPIO5_A4 4'h1: VO_LCDC_D4 4'h2: SPI0_MOSI_M2 4'h4: DSMC_D13 4'h5: SAI2_SDO_M1 4'h7: PWM0_CH3_M1 4'h8: UART5_TX_M1

GPIO5_IOC_GPIO5B_IOMUX_SEL_0

Address: Operational Base(0x201D0000) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio5b3_sel 4'h0: GPIO5_B3 4'h1: VO_LCDC_D11 4'h2: ETH_MCLK_M1 4'h3: VI_CIF_D7_M1 4'h4: DSMC_RDYN 4'h7: PWM2_CH1_M1 4'h8: UART6_CTSN_M0
11:8	RW	0x0	gpio5b2_sel 4'h0: GPIO5_B2 4'h1: VO_LCDC_D10 4'h2: ETH_RXD1_M1 4'h3: VI_CIF_D6_M1 4'h4: DSMC_RESETN 4'h5: DSMC_INT1 4'h7: PWM2_CH0_M1 4'h8: UART6_RTSN_M0
7:4	RW	0x0	gpio5b1_sel 4'h0: GPIO5_B1 4'h1: VO_LCDC_D9 4'h2: ETH_RXD0_M1 4'h3: VI_CIF_D5_M1 4'h4: DSMC_D8 4'h6: IR_FPA_SDA3 4'h8: UART6_RX_M0

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	gpio5b0_sel 4'h0: GPIO5_B0 4'h1: VO_LCDC_D8 4'h2: ETH_RXCTL_M1 4'h3: VI_CIF_D4_M1 4'h4: DSMC_D9 4'h6: IR_FPA_SDA2 4'h8: UART6_TX_M0

GPIO5_IOC_GPIO5B_IOMUX_SEL_1

Address: Operational Base(0x201D0000) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio5b7_sel 4'h0: GPIO5_B7 4'h1: VO_LCDC_D15 4'h2: ETH_TXD0_M1 4'h3: VI_CIF_D11_M1 4'h4: DSMC_CLKP 4'h7: PWM2_CH3_M1 4'h8: UART7_CTSN_M0
11:8	RW	0x0	gpio5b6_sel 4'h0: GPIO5_B6 4'h1: VO_LCDC_D14 4'h2: ETH_MDC_M1 4'h3: VI_CIF_D10_M1 4'h4: DSMC_CLKN 4'h5: DSMC_INT0 4'h6: ETH_TESTRXCLK_OUT_M0 4'h7: PWM2_CH2_M1 4'h8: UART7_RTSN_M0
7:4	RW	0x0	gpio5b5_sel 4'h0: GPIO5_B5 4'h1: VO_LCDC_D13 4'h2: ETH_MDIO_M1 4'h3: VI_CIF_D9_M1 4'h4: DSMC_DQS0 4'h6: ETH_TESTRXD_OUT_M0 4'h8: UART7_RX_M0
3:0	RW	0x0	gpio5b4_sel 4'h0: GPIO5_B4 4'h1: VO_LCDC_D12 4'h3: VI_CIF_D8_M1 4'h4: DSMC_CSN0 4'h8: UART7_TX_M0

GPIO5_IOC_GPIO5C_IOMUX_SEL_0

Address: Operational Base(0x201D0000) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:12	RW	0x0	gpio5c3_sel 4'h0: GPIO5_C3 4'h1: VO_LCDC_D19 4'h2: ETH_RXD2_M1 4'h3: VI_CIF_D15_M1 4'h4: DSMC_D4 4'h5: SAI1_MCLK_M2 4'h7: PWM3_CH3_M1
11:8	RW	0x0	gpio5c2_sel 4'h0: GPIO5_C2 4'h1: VO_LCDC_D18 4'h2: ETH_TXCTL_M1 4'h3: VI_CIF_D14_M1 4'h4: DSMC_D5 4'h6: IR_FPA_SDA6 4'h7: PWM3_CH2_M1
7:4	RW	0x0	gpio5c1_sel 4'h0: GPIO5_C1 4'h1: VO_LCDC_D17 4'h2: ETH_CLK_25M_OUT_M1 4'h3: VI_CIF_D13_M1 4'h4: DSMC_D6 4'h6: IR_FPA_SDA5 4'h7: PWM3_CH1_M1
3:0	RW	0x0	gpio5c0_sel 4'h0: GPIO5_C0 4'h1: VO_LCDC_D16 4'h2: ETH_TXD1_M1 4'h3: VI_CIF_D12_M1 4'h4: DSMC_D7 4'h6: IR_FPA_SDA4 4'h7: PWM3_CH0_M1

GPIO5_IOC_GPIO5C_IOMUX_SEL_1

Address: Operational Base(0x201D0000) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio5c7_sel 4'h0: GPIO5_C7 4'h1: VO_LCDC_D23 4'h2: ETH_RXCLK_M1 4'h3: VI_CIF_HSYNC_M1 4'h4: DSMC_D0 4'h5: SAI1_SDI_M2 4'h7: PWM3_CH7_M1
11:8	RW	0x0	gpio5c6_sel 4'h0: GPIO5_C6 4'h1: VO_LCDC_D22 4'h2: ETH_TXCLK_M1 4'h3: VI_CIF_CLKIN_M1 4'h4: DSMC_D1 4'h5: SAI1_LRCK_M2 4'h7: PWM3_CH6_M1

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	gpio5c5_sel 4'h0: GPIO5_C5 4'h1: VO_LCDC_D21 4'h2: ETH_TXD2_M1 4'h3: VI_CIF_CLKOUT_M1 4'h4: DSMC_D2 4'h5: SAI1_SCLK_M2 4'h7: PWM3_CH5_M1
3:0	RW	0x0	gpio5c4_sel 4'h0: GPIO5_C4 4'h1: VO_LCDC_D20 4'h2: ETH_RXD3_M1 4'h3: VI_CIF_VSYNC_M1 4'h4: DSMC_D3 4'h5: SAI1_SDO_M2 4'h7: PWM3_CH4_M1

GPIO5_IOC_GPIO5D_IOMUX_SEL_0

Address: Operational Base(0x201D0000) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio5d3_sel 4'h0: GPIO5_D3 4'h1: VO_LCDC_CLK 4'h2: SPI1_MISO_M2 4'h4: DSMC_INT2 4'h7: PWM1_CH0_M1 4'h8: UART3_CTSN_M1
11:8	RW	0x0	gpio5d2_sel 4'h0: GPIO5_D2 4'h1: VO_LCDC_VSYNC 4'h2: SPI1_MOSI_M2 4'h4: DSMC_INT3 4'h7: PWM1_CH1_M1 4'h8: UART3_RTSN_M1
7:4	RW	0x0	gpio5d1_sel 4'h0: GPIO5_D1 4'h1: VO_LCDC_HSYNC 4'h2: SPI1_CLK_M2 4'h3: ETH_PPSTRIG_M1 4'h4: DSMC_CSN2 4'h6: I2C3_SDA_M2 4'h7: PWM1_CH2_M1
3:0	RW	0x0	gpio5d0_sel 4'h0: GPIO5_D0 4'h1: VO_LCDC_DEN 4'h2: SPI1_CSN0_M2 4'h3: ETH_PTP_REFCLK_M1 4'h4: DSMC_CSN3 4'h6: I2C3_SCL_M2 4'h7: PWM0_CH6_M2

GPIO5_IOC_GPIO5D_IOMUX_SEL_1

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Address: Operational Base(0x201D0000) + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio5d7_sel 4'h0: GPIO5_D7 4'h1: UART0_RX_M1 4'h2: JTAG_TMS_M2 4'h3: CAN1_TXD_M0 4'h7: PWM2_CH7_M0
11:8	RW	0x0	gpio5d6_sel 4'h0: GPIO5_D6 4'h1: UART0_TX_M1 4'h2: JTAG_TCK_M2 4'h3: CAN1_RXD_M0 4'h7: PWM2_CH6_M0
7:4	RW	0x0	gpio5d5_sel 4'h0: GPIO5_D5 4'h1: FEPHY_LEDSPD_M1 4'h3: CAN0_TXD_M0 4'h5: IR_FPA_MCLK 4'h6: I2C2_SDA_M1 4'h7: PWM1_CH3_M1 4'h8: UART3_RX_M1
3:0	RW	0x0	gpio5d4_sel 4'h0: GPIO5_D4 4'h1: FEPHY_LEDLINK_M1 4'h2: SPI1_CSN1_M2 4'h3: CAN0_RXD_M0 4'h5: IR_FPA_FSYNC 4'h6: I2C2_SCL_M1 4'h7: PWM0_CH7_M2 4'h8: UART3_TX_M1

GPIO5_IOC_GPIO5A_DS_0

Address: Operational Base(0x201D0000) + offset (0x0240)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio5a1_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x0f	gpio5a0_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO5_IOC_GPIO5A_DS_1

Address: Operational Base(0x201D0000) + offset (0x0244)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio5a3_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio5a2_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO5_IOC_GPIO5A_DS_2

Address: Operational Base(0x201D0000) + offset (0x0248)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:8	RW	0x0f	gpio5a5_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio5a4_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO5_IOC_GPIO5A_DS_3

Address: Operational Base(0x201D0000) + offset (0x024C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio5a7_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x0f	gpio5a6_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO5_IOC_GPIO5B_DS_0

Address: Operational Base(0x201D0000) + offset (0x0250)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio5b1_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio5b0_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO5_IOC_GPIO5B_DS_1

Address: Operational Base(0x201D0000) + offset (0x0254)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x0f	gpio5b3_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio5b2_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO5_IOC_GPIO5B_DS_2

Address: Operational Base(0x201D0000) + offset (0x0258)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio5b5_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x0f	gpio5b4_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO5_IOC_GPIO5B_DS_3

Address: Operational Base(0x201D0000) + offset (0x025C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio5b7_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio5b6_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO5_IOC_GPIO5C_DS_0

Address: Operational Base(0x201D0000) + offset (0x0260)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x0f	gpio5c1_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio5c0_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO5_IOC_GPIO5C_DS_1

Address: Operational Base(0x201D0000) + offset (0x0264)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio5c3_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x0f	gpio5c2_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO5_IOC_GPIO5C_DS_2

Address: Operational Base(0x201D0000) + offset (0x0268)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio5c5_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio5c4_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO5_IOC_GPIO5C_DS_3

Address: Operational Base(0x201D0000) + offset (0x026C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:8	RW	0x0f	gpio5c7_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio5c6_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO5_IOC_GPIO5D_DS_0

Address: Operational Base(0x201D0000) + offset (0x0270)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio5d1_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x0f	gpio5d0_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO5_IOC_GPIO5D_DS_1

Address: Operational Base(0x201D0000) + offset (0x0274)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio5d3_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio5d2_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO5_IOC_GPIO5D_DS_2

Address: Operational Base(0x201D0000) + offset (0x0278)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x0f	gpio5d5_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio5d4_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO5_IOC_GPIO5D_DS_3

Address: Operational Base(0x201D0000) + offset (0x027C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio5d7_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x0f	gpio5d6_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO5_IOC_GPIO5A_PULL

Address: Operational Base(0x201D0000) + offset (0x0350)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	gpio5a7_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
13:12	RW	0x2	gpio5a6_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
11:10	RW	0x2	gpio5a5_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
9:8	RW	0x2	gpio5a4_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
7:6	RW	0x2	gpio5a3_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
5:4	RW	0x2	gpio5a2_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

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Bit	Attr	Reset Value	Description
3:2	RW	0x2	gpio5a1_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
1:0	RW	0x2	gpio5a0_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

GPIO5_IOC_GPIO5B_PULL

Address: Operational Base(0x201D0000) + offset (0x0354)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	gpio5b7_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
13:12	RW	0x2	gpio5b6_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
11:10	RW	0x2	gpio5b5_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
9:8	RW	0x2	gpio5b4_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
7:6	RW	0x2	gpio5b3_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
5:4	RW	0x2	gpio5b2_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

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Bit	Attr	Reset Value	Description
3:2	RW	0x2	gpio5b1_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
1:0	RW	0x2	gpio5b0_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

GPIO5_IOC_GPIO5C_PULL

Address: Operational Base(0x201D0000) + offset (0x0358)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	gpio5c7_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
13:12	RW	0x2	gpio5c6_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
11:10	RW	0x2	gpio5c5_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
9:8	RW	0x2	gpio5c4_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
7:6	RW	0x2	gpio5c3_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
5:4	RW	0x2	gpio5c2_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

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Bit	Attr	Reset Value	Description
3:2	RW	0x2	gpio5c1_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
1:0	RW	0x2	gpio5c0_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

GPIO5_IOC_GPIO5D_PULL

Address: Operational Base(0x201D0000) + offset (0x035C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x1	gpio5d7_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
13:12	RW	0x1	gpio5d6_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
11:10	RW	0x1	gpio5d5_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
9:8	RW	0x1	gpio5d4_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
7:6	RW	0x2	gpio5d3_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
5:4	RW	0x2	gpio5d2_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

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Bit	Attr	Reset Value	Description
3:2	RW	0x2	gpio5d1_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
1:0	RW	0x2	gpio5d0_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

GPIO5_IOC_GPIO5A_IE

Address: Operational Base(0x201D0000) + offset (0x0450)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio5a7_ie Receiver enable 1'b0: N 1'b1: Y
6	RW	0x1	gpio5a6_ie Receiver enable 1'b0: N 1'b1: Y
5	RW	0x1	gpio5a5_ie Receiver enable 1'b0: N 1'b1: Y
4	RW	0x1	gpio5a4_ie Receiver enable 1'b0: N 1'b1: Y
3	RW	0x1	gpio5a3_ie Receiver enable 1'b0: N 1'b1: Y
2	RW	0x1	gpio5a2_ie Receiver enable 1'b0: N 1'b1: Y
1	RW	0x1	gpio5a1_ie Receiver enable 1'b0: N 1'b1: Y
0	RW	0x1	gpio5a0_ie Receiver enable 1'b0: N 1'b1: Y

GPIO5_IOC_GPIO5B_IE

Address: Operational Base(0x201D0000) + offset (0x0454)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio5b7_ie Receiver enable 1'b0: N 1'b1: Y
6	RW	0x1	gpio5b6_ie Receiver enable 1'b0: N 1'b1: Y
5	RW	0x1	gpio5b5_ie Receiver enable 1'b0: N 1'b1: Y
4	RW	0x1	gpio5b4_ie Receiver enable 1'b0: N 1'b1: Y
3	RW	0x1	gpio5b3_ie Receiver enable 1'b0: N 1'b1: Y
2	RW	0x1	gpio5b2_ie Receiver enable 1'b0: N 1'b1: Y
1	RW	0x1	gpio5b1_ie Receiver enable 1'b0: N 1'b1: Y
0	RW	0x1	gpio5b0_ie Receiver enable 1'b0: N 1'b1: Y

GPIO5_IOC_GPIO5C_IE

Address: Operational Base(0x201D0000) + offset (0x0458)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio5c7_ie Receiver enable 1'b0: N 1'b1: Y
6	RW	0x1	gpio5c6_ie Receiver enable 1'b0: N 1'b1: Y

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Bit	Attr	Reset Value	Description
5	RW	0x1	gpio5c5_ie Receiver enable 1'b0: N 1'b1: Y
4	RW	0x1	gpio5c4_ie Receiver enable 1'b0: N 1'b1: Y
3	RW	0x1	gpio5c3_ie Receiver enable 1'b0: N 1'b1: Y
2	RW	0x1	gpio5c2_ie Receiver enable 1'b0: N 1'b1: Y
1	RW	0x1	gpio5c1_ie Receiver enable 1'b0: N 1'b1: Y
0	RW	0x1	gpio5c0_ie Receiver enable 1'b0: N 1'b1: Y

GPIO5_IOC_GPIO5D_IE

Address: Operational Base(0x201D0000) + offset (0x045C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio5d7_ie Receiver enable 1'b0: N 1'b1: Y
6	RW	0x1	gpio5d6_ie Receiver enable 1'b0: N 1'b1: Y
5	RW	0x1	gpio5d5_ie Receiver enable 1'b0: N 1'b1: Y
4	RW	0x1	gpio5d4_ie Receiver enable 1'b0: N 1'b1: Y
3	RW	0x1	gpio5d3_ie Receiver enable 1'b0: N 1'b1: Y

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Bit	Attr	Reset Value	Description
2	RW	0x1	gpio5d2_ie Receiver enable 1'b0: N 1'b1: Y
1	RW	0x1	gpio5d1_ie Receiver enable 1'b0: N 1'b1: Y
0	RW	0x1	gpio5d0_ie Receiver enable 1'b0: N 1'b1: Y

GPIO5_IOC_GPIO5A_SMT

Address: Operational Base(0x201D0000) + offset (0x0550)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio5a7_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
6	RW	0x1	gpio5a6_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
5	RW	0x1	gpio5a5_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
4	RW	0x1	gpio5a4_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
3	RW	0x1	gpio5a3_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
2	RW	0x1	gpio5a2_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
1	RW	0x1	gpio5a1_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
0	RW	0x1	gpio5a0_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y

GPIO5_IOC_GPIO5B_SMT

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Address: Operational Base(0x201D0000) + offset (0x0554)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio5b7_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
6	RW	0x1	gpio5b6_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
5	RW	0x1	gpio5b5_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
4	RW	0x1	gpio5b4_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
3	RW	0x1	gpio5b3_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
2	RW	0x1	gpio5b2_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
1	RW	0x1	gpio5b1_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
0	RW	0x1	gpio5b0_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y

GPIO5_IOC_GPIO5C_SMT

Address: Operational Base(0x201D0000) + offset (0x0558)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio5c7_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
6	RW	0x1	gpio5c6_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y

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Bit	Attr	Reset Value	Description
5	RW	0x1	gpio5c5_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
4	RW	0x1	gpio5c4_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
3	RW	0x1	gpio5c3_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
2	RW	0x1	gpio5c2_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
1	RW	0x1	gpio5c1_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
0	RW	0x1	gpio5c0_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y

GPIO5_IOC_GPIO5D_SMT

Address: Operational Base(0x201D0000) + offset (0x055C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio5d7_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
6	RW	0x1	gpio5d6_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
5	RW	0x1	gpio5d5_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
4	RW	0x1	gpio5d4_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
3	RW	0x1	gpio5d3_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y

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Bit	Attr	Reset Value	Description
2	RW	0x1	gpio5d2_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
1	RW	0x1	gpio5d1_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
0	RW	0x1	gpio5d0_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y

GPIO5_IOC_GPIO5A_SUS

Address: Operational Base(0x201D0000) + offset (0x0650)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio5a7_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
6	RW	0x0	gpio5a6_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
5	RW	0x0	gpio5a5_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
4	RW	0x0	gpio5a4_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
3	RW	0x0	gpio5a3_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
2	RW	0x0	gpio5a2_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
1	RW	0x0	gpio5a1_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
0	RW	0x0	gpio5a0_sus Weak pull keeper for pad 1'b0: N 1'b1: Y

GPIO5_IOC_GPIO5B_SUS

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Address: Operational Base(0x201D0000) + offset (0x0654)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio5b7_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
6	RW	0x0	gpio5b6_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
5	RW	0x0	gpio5b5_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
4	RW	0x0	gpio5b4_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
3	RW	0x0	gpio5b3_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
2	RW	0x0	gpio5b2_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
1	RW	0x0	gpio5b1_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
0	RW	0x0	gpio5b0_sus Weak pull keeper for pad 1'b0: N 1'b1: Y

GPIO5_IOC_GPIO5C_SUS

Address: Operational Base(0x201D0000) + offset (0x0658)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio5c7_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
6	RW	0x0	gpio5c6_sus Weak pull keeper for pad 1'b0: N 1'b1: Y

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Bit	Attr	Reset Value	Description
5	RW	0x0	gpio5c5_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
4	RW	0x0	gpio5c4_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
3	RW	0x0	gpio5c3_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
2	RW	0x0	gpio5c2_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
1	RW	0x0	gpio5c1_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
0	RW	0x0	gpio5c0_sus Weak pull keeper for pad 1'b0: N 1'b1: Y

GPIO5_IOC_GPIO5D_SUS

Address: Operational Base(0x201D0000) + offset (0x065C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio5d7_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
6	RW	0x0	gpio5d6_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
5	RW	0x0	gpio5d5_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
4	RW	0x0	gpio5d4_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
3	RW	0x0	gpio5d3_sus Weak pull keeper for pad 1'b0: N 1'b1: Y

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Bit	Attr	Reset Value	Description
2	RW	0x0	gpio5d2_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
1	RW	0x0	gpio5d1_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
0	RW	0x0	gpio5d0_sus Weak pull keeper for pad 1'b0: N 1'b1: Y

GPIO5_IOC_GPIO5A_SL

Address: Operational Base(0x201D0000) + offset (0x0750)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio5a7_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
13:12	RW	0x0	gpio5a6_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
11:10	RW	0x0	gpio5a5_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
9:8	RW	0x0	gpio5a4_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
7:6	RW	0x0	gpio5a3_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
5:4	RW	0x0	gpio5a2_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	gpio5a1_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
1:0	RW	0x0	gpio5a0_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y

GPIO5_IOC_GPIO5B_SL

Address: Operational Base(0x201D0000) + offset (0x0754)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio5b7_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
13:12	RW	0x0	gpio5b6_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
11:10	RW	0x0	gpio5b5_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
9:8	RW	0x0	gpio5b4_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
7:6	RW	0x0	gpio5b3_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
5:4	RW	0x0	gpio5b2_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	gpio5b1_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
1:0	RW	0x0	gpio5b0_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y

GPIO5_IOC_GPIO5C_SL

Address: Operational Base(0x201D0000) + offset (0x0758)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio5c7_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
13:12	RW	0x0	gpio5c6_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
11:10	RW	0x0	gpio5c5_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
9:8	RW	0x0	gpio5c4_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
7:6	RW	0x0	gpio5c3_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
5:4	RW	0x0	gpio5c2_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	gpio5c1_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
1:0	RW	0x0	gpio5c0_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y

GPIO5_IOC_GPIO5D_SL

Address: Operational Base(0x201D0000) + offset (0x075C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio5d7_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
13:12	RW	0x0	gpio5d6_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
11:10	RW	0x0	gpio5d5_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
9:8	RW	0x0	gpio5d4_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
7:6	RW	0x0	gpio5d3_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
5:4	RW	0x0	gpio5d2_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	gpio5d1_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
1:0	RW	0x0	gpio5d0_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y

GPIO5_IOC_GPIO5A_OD

Address: Operational Base(0x201D0000) + offset (0x0850)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio5a7_od For open drain functionality 1'b0: N 1'b1: Y
6	RW	0x0	gpio5a6_od For open drain functionality 1'b0: N 1'b1: Y
5	RW	0x0	gpio5a5_od For open drain functionality 1'b0: N 1'b1: Y
4	RW	0x0	gpio5a4_od For open drain functionality 1'b0: N 1'b1: Y
3	RW	0x0	gpio5a3_od For open drain functionality 1'b0: N 1'b1: Y
2	RW	0x0	gpio5a2_od For open drain functionality 1'b0: N 1'b1: Y
1	RW	0x0	gpio5a1_od For open drain functionality 1'b0: N 1'b1: Y
0	RW	0x0	gpio5a0_od For open drain functionality 1'b0: N 1'b1: Y

GPIO5_IOC_GPIO5B_OD

Address: Operational Base(0x201D0000) + offset (0x0854)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio5b7_od For open drain functionality 1'b0: N 1'b1: Y
6	RW	0x0	gpio5b6_od For open drain functionality 1'b0: N 1'b1: Y
5	RW	0x0	gpio5b5_od For open drain functionality 1'b0: N 1'b1: Y
4	RW	0x0	gpio5b4_od For open drain functionality 1'b0: N 1'b1: Y
3	RW	0x0	gpio5b3_od For open drain functionality 1'b0: N 1'b1: Y
2	RW	0x0	gpio5b2_od For open drain functionality 1'b0: N 1'b1: Y
1	RW	0x0	gpio5b1_od For open drain functionality 1'b0: N 1'b1: Y
0	RW	0x0	gpio5b0_od For open drain functionality 1'b0: N 1'b1: Y

GPIO5_IOC_GPIO5C_OD

Address: Operational Base(0x201D0000) + offset (0x0858)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio5c7_od For open drain functionality 1'b0: N 1'b1: Y
6	RW	0x0	gpio5c6_od For open drain functionality 1'b0: N 1'b1: Y

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Bit	Attr	Reset Value	Description
5	RW	0x0	gpio5c5_od For open drain functionality 1'b0: N 1'b1: Y
4	RW	0x0	gpio5c4_od For open drain functionality 1'b0: N 1'b1: Y
3	RW	0x0	gpio5c3_od For open drain functionality 1'b0: N 1'b1: Y
2	RW	0x0	gpio5c2_od For open drain functionality 1'b0: N 1'b1: Y
1	RW	0x0	gpio5c1_od For open drain functionality 1'b0: N 1'b1: Y
0	RW	0x0	gpio5c0_od For open drain functionality 1'b0: N 1'b1: Y

GPIO5_IOC_GPIO5D_OD

Address: Operational Base(0x201D0000) + offset (0x085C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio5d7_od For open drain functionality 1'b0: N 1'b1: Y
6	RW	0x0	gpio5d6_od For open drain functionality 1'b0: N 1'b1: Y
5	RW	0x0	gpio5d5_od For open drain functionality 1'b0: N 1'b1: Y
4	RW	0x0	gpio5d4_od For open drain functionality 1'b0: N 1'b1: Y
3	RW	0x0	gpio5d3_od For open drain functionality 1'b0: N 1'b1: Y

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Bit	Attr	Reset Value	Description
2	RW	0x0	gpio5d2_od For open drain functionality 1'b0: N 1'b1: Y
1	RW	0x0	gpio5d1_od For open drain functionality 1'b0: N 1'b1: Y
0	RW	0x0	gpio5d0_od For open drain functionality 1'b0: N 1'b1: Y

GPIO5_IOC_IO_VSEL

Address: Operational Base(0x201D0000) + offset (0x0918)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	vccio5_vd vccio5_vd
14:1	RO	0x0000	reserved
0	RW	0x0	poc_vccio5_iddq VCCIO5 iddq control 1'b0: Disable 1'b1: Enable

GPIO5_IOC_GRF_VICIF_M1_CON

Address: Operational Base(0x201D0000) + offset (0x0B98)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	cif_m1_datapath grf_vicif_m0_con
8	RW	0x0	cif_m1_clk_inv_sel grf_vicif_m0_con
7	RO	0x0	reserved
6:0	RW	0x00	cif_m1_clk_delay_num grf_vicif_m0_con

GPIO5_IOC_GRF_VOP_LCDC_CON

Address: Operational Base(0x201D0000) + offset (0x0B9C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	lcdc_mcu_sel grf_vop_lcdc_con
14:8	RW	0x00	lcdc_dclk_dll_num grf_vop_lcdc_con

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Bit	Attr	Reset Value	Description
7:2	RO	0x00	reserved
1	RW	0x0	lcdc_dclk_dll_sel grf_vop_lcdc_con
0	RW	0x0	lcdc_dclk_inv_sel grf_vop_lcdc_con

GPIO5_IOC_GRF_GMACIO_M1_CON0

Address: Operational Base(0x201D0000) + offset (0x0BA8)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:8	RW	0x00	gmacio_m1_clk_rx_dl_cfg grf_gmacio_m1_con0
7	RO	0x0	reserved
6:0	RW	0x00	gmacio_m1_clk_tx_dl_cfg grf_gmacio_m1_con0

GPIO5_IOC_GRF_GMACIO_M1_CON1

Address: Operational Base(0x201D0000) + offset (0x0BAC)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x00	gmacio_m1_rgmii_debug_io grf_gmacio_m1_con1
7:2	RO	0x00	reserved
1	RW	0x0	gmacio_m1_rxclk_dly_ena grf_gmacio_m1_con1
0	RW	0x0	gmacio_m1_txclk_dly_ena grf_gmacio_m1_con1

GPIO5_IOC_GRF_UART0_DLY_CON

Address: Operational Base(0x201D0000) + offset (0x0BB0)

Bit	Attr	Reset Value	Description
31:0	RW	0x0003a980	grf_con_uart0_rx_low_dly grf_con_uart0_rx_low_dly

GPIO5_IOC_GRF_UART_JTAG_CON

Address: Operational Base(0x201D0000) + offset (0x0BB4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	grf_uart0_jtag_con uart0 jtag control 1'b0: Disable 1'b1: Enable

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GPIO5_IOC_GRF_GPIO5_FILTER_CON0

Address: Operational Base(0x201D0000) + offset (0x0C40)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:10	RW	0x00	grf_gpio5_filter_sel1 GPIO select to go through first filter logic 5'h00: GPIOxA0 5'h01: GPIOxA1 5'h02: GPIOxA2 5'h03: GPIOxA3 5'h04: GPIOxA4 5'h05: GPIOxA5 5'h06: GPIOxA6 5'h07: GPIOxA7 5'h08: GPIOxB0 5'h09: GPIOxB1 5'h0a: GPIOxB2 5'h0b: GPIOxB3 5'h0c: GPIOxB4 5'h0d: GPIOxB5 5'h0e: GPIOxB6 5'h0f: GPIOxB7 5'h10: GPIOxC0 5'h11: GPIOxC1 5'h12: GPIOxC2 5'h13: GPIOxC3 5'h14: GPIOxC4 5'h15: GPIOxC5 5'h16: GPIOxC6 5'h17: GPIOxC7 5'h18: GPIOxD0 5'h19: GPIOxD1 5'h1a: GPIOxD2 5'h1b: GPIOxD3 5'h1c: GPIOxD4 5'h1d: GPIOxD5 5'h1e: GPIOxD6 5'h1f: GPIOxD7
9	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
8:4	RW	0x00	grf_gpio5_filter_sel0 GPIO select to go through first filter logic 5'h00: GPIOxA0 5'h01: GPIOxA1 5'h02: GPIOxA2 5'h03: GPIOxA3 5'h04: GPIOxA4 5'h05: GPIOxA5 5'h06: GPIOxA6 5'h07: GPIOxA7 5'h08: GPIOxB0 5'h09: GPIOxB1 5'h0a: GPIOxB2 5'h0b: GPIOxB3 5'h0c: GPIOxB4 5'h0d: GPIOxB5 5'h0e: GPIOxB6 5'h0f: GPIOxB7 5'h10: GPIOxC0 5'h11: GPIOxC1 5'h12: GPIOxC2 5'h13: GPIOxC3 5'h14: GPIOxC4 5'h15: GPIOxC5 5'h16: GPIOxC6 5'h17: GPIOxC7 5'h18: GPIOxD0 5'h19: GPIOxD1 5'h1a: GPIOxD2 5'h1b: GPIOxD3 5'h1c: GPIOxD4 5'h1d: GPIOxD5 5'h1e: GPIOxD6 5'h1f: GPIOxD7
3:0	RW	0x0	grf_gpio5_filter_en There are four filter circuits for pad in GPIOx, each bit controls the enable of one filter.

GPIO5_IOC_GRF_GPIO5_FILTER_CON1

Address: Operational Base(0x201D0000) + offset (0x0C44)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14:10	RW	0x00	grf_gpio5_filter_sel3 GPIO select to go through first filter logic 5'h00: GPIOxA0 5'h01: GPIOxA1 5'h02: GPIOxA2 5'h03: GPIOxA3 5'h04: GPIOxA4 5'h05: GPIOxA5 5'h06: GPIOxA6 5'h07: GPIOxA7 5'h08: GPIOxB0 5'h09: GPIOxB1 5'h0a: GPIOxB2 5'h0b: GPIOxB3 5'h0c: GPIOxB4 5'h0d: GPIOxB5 5'h0e: GPIOxB6 5'h0f: GPIOxB7 5'h10: GPIOxC0 5'h11: GPIOxC1 5'h12: GPIOxC2 5'h13: GPIOxC3 5'h14: GPIOxC4 5'h15: GPIOxC5 5'h16: GPIOxC6 5'h17: GPIOxC7 5'h18: GPIOxD0 5'h19: GPIOxD1 5'h1a: GPIOxD2 5'h1b: GPIOxD3 5'h1c: GPIOxD4 5'h1d: GPIOxD5 5'h1e: GPIOxD6 5'h1f: GPIOxD7
9	RO	0x0	reserved
8:4	RW	0x00	grf_gpio5_filter_sel2 GPIO select to go through first filter logic 5'h00: GPIOxA0 5'h01: GPIOxA1 5'h02: GPIOxA2 5'h03: GPIOxA3 5'h04: GPIOxA4 5'h05: GPIOxA5 5'h06: GPIOxA6 5'h07: GPIOxA7 5'h08: GPIOxB0 5'h09: GPIOxB1 5'h0a: GPIOxB2 5'h0b: GPIOxB3 5'h0c: GPIOxB4 5'h0d: GPIOxB5 5'h0e: GPIOxB6 5'h0f: GPIOxB7 5'h10: GPIOxC0 5'h11: GPIOxC1 5'h12: GPIOxC2

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Bit	Attr	Reset Value	Description
			5'h13: GPIOxC3 5'h14: GPIOxC4 5'h15: GPIOxC5 5'h16: GPIOxC6 5'h17: GPIOxC7 5'h18: GPIOxD0 5'h19: GPIOxD1 5'h1a: GPIOxD2 5'h1b: GPIOxD3 5'h1c: GPIOxD4 5'h1d: GPIOxD5 5'h1e: GPIOxD6 5'h1f: GPIOxD7
3:0	RO	0x0	reserved

GPIO5_IOC_GRF_GPIO5_FILTER_CON2

Address: Operational Base(0x201D0000) + offset (0x0C48)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio5_filter_count0 Filter counter for first filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

GPIO5_IOC_GRF_GPIO5_FILTER_CON3

Address: Operational Base(0x201D0000) + offset (0x0C4C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio5_filter_count1 Filter counter for second filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

GPIO5_IOC_GRF_GPIO5_FILTER_CON4

Address: Operational Base(0x201D0000) + offset (0x0C50)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio5_filter_count2 Filter counter for third filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

GPIO5_IOC_GRF_GPIO5_FILTER_CON5

Address: Operational Base(0x201D0000) + offset (0x0C54)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio5_filter_count3 Filter counter for fouth filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

23.9 GPIO6_IOC Register Description

23.9.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

23.9.2 Registers Summary

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Name	Offset	Size	Reset Value	Description
GPIO6_IOC_GPIO6A_IOMUX_SEL_0	0x00C0	W	0x00000000	GPIO6A IOMUX Select Register 0
GPIO6_IOC_GPIO6A_IOMUX_SEL_1	0x00C4	W	0x00000000	GPIO6A IOMUX Select Register 1
GPIO6_IOC_GPIO6B_IOMUX_SEL_0	0x00C8	W	0x00000000	GPIO6B IOMUX Select Register 0
GPIO6_IOC_GPIO6B_IOMUX_SEL_1	0x00CC	W	0x00000000	GPIO6B IOMUX Select Register 1
GPIO6_IOC_GPIO6C_IOMUX_SEL_0	0x00D0	W	0x00000000	GPIO6C IOMUX Select Register 0
GPIO6_IOC_GPIO6A_DS_0	0x0280	W	0x00000F0F	GPIO6A driver strength register 0
GPIO6_IOC_GPIO6A_DS_1	0x0284	W	0x00000F0F	GPIO6A driver strength register 1
GPIO6_IOC_GPIO6A_DS_2	0x0288	W	0x00000F0F	GPIO6A driver strength register 2
GPIO6_IOC_GPIO6A_DS_3	0x028C	W	0x00000F0F	GPIO6A driver strength register 3
GPIO6_IOC_GPIO6B_DS_0	0x0290	W	0x00000F0F	GPIO6B driver strength register 0
GPIO6_IOC_GPIO6B_DS_1	0x0294	W	0x00000F0F	GPIO6B driver strength register 1
GPIO6_IOC_GPIO6B_DS_2	0x0298	W	0x00000F0F	GPIO6B driver strength register 2
GPIO6_IOC_GPIO6B_DS_3	0x029C	W	0x00000F0F	GPIO6B driver strength register 3
GPIO6_IOC_GPIO6C_DS_0	0x02A0	W	0x00000F0F	GPIO6C driver strength register 0
GPIO6_IOC_GPIO6C_DS_1	0x02A4	W	0x00000F0F	GPIO6C driver strength register 1
GPIO6_IOC_GPIO6A_PULL	0x0360	W	0x0000AAAA	GPIO6A pull register
GPIO6_IOC_GPIO6B_PULL	0x0364	W	0x0000AAAA	GPIO6B pull register
GPIO6_IOC_GPIO6C_PULL	0x0368	W	0x000000AA	GPIO6C pull register
GPIO6_IOC_GPIO6A_IE	0x0460	W	0x000000FF	GPIO6A input enable register
GPIO6_IOC_GPIO6B_IE	0x0464	W	0x000000FF	GPIO6B input enable register
GPIO6_IOC_GPIO6C_IE	0x0468	W	0x0000000F	GPIO6C input enable register
GPIO6_IOC_GPIO6A_SMT	0x0560	W	0x000000FF	GPIO6A receiver enable for schmitter trigger register
GPIO6_IOC_GPIO6B_SMT	0x0564	W	0x000000FF	GPIO6B receiver enable for schmitter trigger register
GPIO6_IOC_GPIO6C_SMT	0x0568	W	0x0000000F	GPIO6C receiver enable for schmitter trigger register
GPIO6_IOC_GPIO6A_SUS	0x0660	W	0x00000000	GPIO6A enable weak pull keeper register
GPIO6_IOC_GPIO6B_SUS	0x0664	W	0x00000000	GPIO6B enable weak pull keeper register
GPIO6_IOC_GPIO6C_SUS	0x0668	W	0x00000000	GPIO6C enable weak pull keeper register

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Name	Offset	Size	Reset Value	Description
GPIO6_IOC_GPIO6A_SL	0x0760	W	0x00000000	GPIO6A slew rate control register
GPIO6_IOC_GPIO6B_SL	0x0764	W	0x00000000	GPIO6B slew rate control register
GPIO6_IOC_GPIO6C_SL	0x0768	W	0x00000000	GPIO6C slew rate control register
GPIO6_IOC_GPIO6A_OD	0x0860	W	0x00000000	GPIO6A open drain register
GPIO6_IOC_GPIO6B_OD	0x0864	W	0x00000000	GPIO6B open drain register
GPIO6_IOC_GPIO6C_OD	0x0868	W	0x00000000	GPIO6C open drain register
GPIO6_IOC_IO_VSEL	0x091C	W	0x00000000	IO iddq register
GPIO6_IOC_GRF_VICIF_M0_CON	0x0B94	W	0x00000000	vicif m0 con register
GPIO6_IOC_GRF_GMACIO_M0_CON0	0x0BA0	W	0x00000000	gmacio m0 con0 register
GPIO6_IOC_GRF_GMACIO_M0_CON1	0x0BA4	W	0x00000000	gmacio m0 con1 register
GPIO6_IOC_GRF_GPIO6_FILTER_CON0	0x0C60	W	0x00000000	GPIO6 filter config register 0
GPIO6_IOC_GRF_GPIO6_FILTER_CON1	0x0C64	W	0x00000000	GPIO6 filter config register 1
GPIO6_IOC_GRF_GPIO6_FILTER_CON2	0x0C68	W	0x00000000	GPIO6 filter config register 2
GPIO6_IOC_GRF_GPIO6_FILTER_CON3	0x0C6C	W	0x00000000	GPIO6 filter config register 3
GPIO6_IOC_GRF_GPIO6_FILTER_CON4	0x0C70	W	0x00000000	GPIO6 filter config register 4
GPIO6_IOC_GRF_GPIO6_FILTER_CON5	0x0C74	W	0x00000000	GPIO6 filter config register 5

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

23.9.3 Detail Registers Description

GPIO6_IOC_GPIO6A_IOMUX_SEL_0

Address: Operational Base(0x201D8000) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio6a3_sel 4'h0: GPIO6_A3 4'h1: VI_CIF_D3_M0 4'h2: ETH_RXD2_M0 4'h3: CAN1_TXD_M1 4'h4: SAI0_SDI0_M1 4'h5: PWM1_CH3_M2 4'h6: UART5_RX_M2 4'h7: I2C4_SDA_M1

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Bit	Attr	Reset Value	Description
11:8	RW	0x0	gpio6a2_sel 4'h0: GPIO6_A2 4'h1: VI_CIF_D2_M0 4'h2: ETH_PPSCLK_M0 4'h3: CAN1_RXD_M1 4'h4: SAI0_SDO0_M1 4'h5: PWM1_CH2_M2 4'h6: UART5_TX_M2 4'h7: I2C4_SCL_M1
7:4	RW	0x0	gpio6a1_sel 4'h0: GPIO6_A1 4'h1: VI_CIF_D1_M0 4'h2: ETH_PTP_REFCLK_M0 4'h3: CAN0_TXD_M1 4'h4: SAI0_LRCK_M1 4'h5: PWM1_CH1_M2 4'h6: UART4_RX_M2 4'h7: I2C3_SDA_M3 4'h8: TEST_FEPHY_RMII_RXD1
3:0	RW	0x0	gpio6a0_sel 4'h0: GPIO6_A0 4'h1: VI_CIF_D0_M0 4'h2: ETH_PPSTRIG_M0 4'h3: CAN0_RXD_M1 4'h4: SAI0_SCLK_M1 4'h5: PWM1_CH0_M2 4'h6: UART4_TX_M2 4'h7: I2C3_SCL_M3 4'h8: TEST_FEPHY_RMII_RXD0

GPIO6_IOC_GPIO6A_IOMUX_SEL_1

Address: Operational Base(0x201D8000) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio6a7_sel 4'h0: GPIO6_A7 4'h1: VI_CIF_D7_M0 4'h2: ETH_TXD0_M0 4'h3: PWM2_CH3_M2 4'h4: SAI0_SDI3_M1 4'h5: SAI0_SDO1_M1 4'h6: UART4_CTSN_M2 4'h8: FEPHY_TESTDATA3_OUT
11:8	RW	0x0	gpio6a6_sel 4'h0: GPIO6_A6 4'h1: VI_CIF_D6_M0 4'h2: ETH_TXD3_M0 4'h5: PWM2_CH2_M2 4'h6: UART4_RTSN_M2 4'h8: FEPHY_TESTDATA2_OUT

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	gpio6a5_sel 4'h0: GPIO6_A5 4'h1: VI_CIF_D5_M0 4'h2: ETH_TXD2_M0 4'h5: PWM2_CH1_M2 4'h6: UART5_CTSN_M2 4'h8: FEPHY_TESTDATA1_OUT
3:0	RW	0x0	gpio6a4_sel 4'h0: GPIO6_A4 4'h1: VI_CIF_D4_M0 4'h2: ETH_RXD3_M0 4'h4: SAI0_MCLK_M1 4'h5: PWM2_CH0_M2 4'h6: UART5_RTSN_M2 4'h8: FEPHY_TESTDATA0_OUT

GPIO6_IOC_GPIO6B_IOMUX_SEL_0

Address: Operational Base(0x201D8000) + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio6b3_sel 4'h0: GPIO6_B3 4'h1: VI_CIF_D11_M0 4'h2: ETH_RXD1_M0 4'h3: SPI1_MISO_M0 4'h5: PDM_SDI3_M1 4'h6: UART6_CTSN_M1 4'h8: FEPHY_TESTDATA7_OUT
11:8	RW	0x0	gpio6b2_sel 4'h0: GPIO6_B2 4'h1: VI_CIF_D10_M0 4'h2: ETH_RXD0_M0 4'h3: SPI1_MOSI_M0 4'h5: PDM_SDI2_M1 4'h6: UART6_RTSN_M1 4'h8: FEPHY_TESTDATA6_OUT
7:4	RW	0x0	gpio6b1_sel 4'h0: GPIO6_B1 4'h1: VI_CIF_D9_M0 4'h2: ETH_TXCTL_M0 4'h3: SPI1_CSN0_M0 4'h4: SAI0_SDI1_M1 4'h5: SAI0_SDO3_M1 4'h6: UART6_RX_M1 4'h8: FEPHY_TESTDATA5_OUT

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	gpio6b0_sel 4'h0: GPIO6_B0 4'h1: VI_CIF_D8_M0 4'h2: ETH_TXD1_M0 4'h3: SPI1_CSN1_M0 4'h4: SAI0_SDI2_M1 4'h5: SAI0_SDO2_M1 4'h6: UART6_TX_M1 4'h8: FEPHY_TESTDATA4_OUT

GPIO6_IOC_GPIO6B_IOMUX_SEL_1

Address: Operational Base(0x201D8000) + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio6b7_sel 4'h0: GPIO6_B7 4'h1: VI_CIF_D15_M0 4'h2: ETH_MDIO_M0 4'h3: ETH_TESTRXD_OUT_M1 4'h5: PDM_CLK1_M1 4'h6: UART7_CTSN_M1 4'h8: FEPHY_TESTCLK_OUT
11:8	RW	0x0	gpio6b6_sel 4'h0: GPIO6_B6 4'h1: VI_CIF_D14_M0 4'h5: PDM_SDI1_M1 4'h6: UART7_RTSN_M1 4'h8: TEST_FEPHY_RMII_DVCRS
7:4	RW	0x0	gpio6b5_sel 4'h0: GPIO6_B5 4'h1: VI_CIF_D13_M0 4'h2: ETH_RXCTL_M0 4'h5: PDM_SDI0_M1 4'h6: UART7_RX_M1 4'h8: TEST_FEPHY_RMII_RXER
3:0	RW	0x0	gpio6b4_sel 4'h0: GPIO6_B4 4'h1: VI_CIF_D12_M0 4'h2: ETH_MCLK_M0 4'h3: SPI1_CLK_M0 4'h5: PDM_CLK0_M1 4'h6: UART7_TX_M1 4'h8: TEST_FEPHY_RMII_CLK

GPIO6_IOC_GPIO6C_IOMUX_SEL_0

Address: Operational Base(0x201D8000) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:12	RW	0x0	gpio6c3_sel 4'h0: GPIO6_C3 4'h1: VI_CIF_HSYNC_M0 4'h2: ETH_RXCLK_M0 4'h3: FEPHY_LEDSPD_M2 4'h5: PWM0_CH3_M2 4'h6: UART3_RX_M2 4'h7: I2C2_SDA_M2 4'h8: DSMC_TESTDATA_OUT
11:8	RW	0x0	gpio6c2_sel 4'h0: GPIO6_C2 4'h1: VI_CIF_CLKOUT_M0 4'h2: ETH_TXCLK_M0 4'h3: FEPHY_LEDLINK_M2 4'h5: PWM0_CH2_M2 4'h6: UART3_TX_M2 4'h8: DSMC_TESTCLK_OUT
7:4	RW	0x0	gpio6c1_sel 4'h0: GPIO6_C1 4'h1: VI_CIF_CLKIN_M0 4'h2: ETH_CLK_25M_OUT_M0 4'h5: PWM0_CH1_M2 4'h6: UART3_CTSN_M2
3:0	RW	0x0	gpio6c0_sel 4'h0: GPIO6_C0 4'h1: VI_CIF_VSYNC_M0 4'h2: ETH_MDC_M0 4'h3: ETH_TESTRXCLK_OUT_M1 4'h5: PWM0_CH0_M2 4'h6: UART3_RTSN_M2 4'h7: I2C2_SCL_M2

GPIO6_IOC_GPIO6A_DS_0

Address: Operational Base(0x201D8000) + offset (0x0280)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio6a1_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x0f	gpio6a0_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO6_IOC_GPIO6A_DS_1

Address: Operational Base(0x201D8000) + offset (0x0284)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio6a3_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio6a2_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO6_IOC_GPIO6A_DS_2

Address: Operational Base(0x201D8000) + offset (0x0288)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:8	RW	0x0f	gpio6a5_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio6a4_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO6_IOC_GPIO6A_DS_3

Address: Operational Base(0x201D8000) + offset (0x028C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio6a7_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x0f	gpio6a6_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO6_IOC_GPIO6B_DS_0

Address: Operational Base(0x201D8000) + offset (0x0290)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio6b1_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio6b0_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO6_IOC_GPIO6B_DS_1

Address: Operational Base(0x201D8000) + offset (0x0294)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x0f	gpio6b3_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio6b2_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO6_IOC_GPIO6B_DS_2

Address: Operational Base(0x201D8000) + offset (0x0298)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio6b5_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x0f	gpio6b4_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO6_IOC_GPIO6B_DS_3

Address: Operational Base(0x201D8000) + offset (0x029C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio6b7_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio6b6_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO6_IOC_GPIO6C_DS_0

Address: Operational Base(0x201D8000) + offset (0x02A0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:8	RW	0x0f	gpio6c1_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio6c0_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO6_IOC_GPIO6C_DS_1

Address: Operational Base(0x201D8000) + offset (0x02A4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio6c3_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x0f	gpio6c2_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO6_IOC_GPIO6A_PULL

Address: Operational Base(0x201D8000) + offset (0x0360)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	gpio6a7_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
13:12	RW	0x2	gpio6a6_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
11:10	RW	0x2	gpio6a5_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
9:8	RW	0x2	gpio6a4_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
7:6	RW	0x2	gpio6a3_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
5:4	RW	0x2	gpio6a2_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

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Bit	Attr	Reset Value	Description
3:2	RW	0x2	gpio6a1_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
1:0	RW	0x2	gpio6a0_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

GPIO6_IOC_GPIO6B_PULL

Address: Operational Base(0x201D8000) + offset (0x0364)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	gpio6b7_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
13:12	RW	0x2	gpio6b6_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
11:10	RW	0x2	gpio6b5_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
9:8	RW	0x2	gpio6b4_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
7:6	RW	0x2	gpio6b3_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
5:4	RW	0x2	gpio6b2_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

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Bit	Attr	Reset Value	Description
3:2	RW	0x2	gpio6b1_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
1:0	RW	0x2	gpio6b0_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

GPIO6_IOC_GPIO6C_PULL

Address: Operational Base(0x201D8000) + offset (0x0368)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:6	RW	0x2	gpio6c3_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
5:4	RW	0x2	gpio6c2_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
3:2	RW	0x2	gpio6c1_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
1:0	RW	0x2	gpio6c0_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

GPIO6_IOC_GPIO6A_IE

Address: Operational Base(0x201D8000) + offset (0x0460)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
7	RW	0x1	gpio6a7_ie Receiver enable 1'b0: N 1'b1: Y
6	RW	0x1	gpio6a6_ie Receiver enable 1'b0: N 1'b1: Y
5	RW	0x1	gpio6a5_ie Receiver enable 1'b0: N 1'b1: Y
4	RW	0x1	gpio6a4_ie Receiver enable 1'b0: N 1'b1: Y
3	RW	0x1	gpio6a3_ie Receiver enable 1'b0: N 1'b1: Y
2	RW	0x1	gpio6a2_ie Receiver enable 1'b0: N 1'b1: Y
1	RW	0x1	gpio6a1_ie Receiver enable 1'b0: N 1'b1: Y
0	RW	0x1	gpio6a0_ie Receiver enable 1'b0: N 1'b1: Y

GPIO6_IOC_GPIO6B_IE

Address: Operational Base(0x201D8000) + offset (0x0464)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio6b7_ie Receiver enable 1'b0: N 1'b1: Y
6	RW	0x1	gpio6b6_ie Receiver enable 1'b0: N 1'b1: Y
5	RW	0x1	gpio6b5_ie Receiver enable 1'b0: N 1'b1: Y

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Bit	Attr	Reset Value	Description
4	RW	0x1	gpio6b4_ie Receiver enable 1'b0: N 1'b1: Y
3	RW	0x1	gpio6b3_ie Receiver enable 1'b0: N 1'b1: Y
2	RW	0x1	gpio6b2_ie Receiver enable 1'b0: N 1'b1: Y
1	RW	0x1	gpio6b1_ie Receiver enable 1'b0: N 1'b1: Y
0	RW	0x1	gpio6b0_ie Receiver enable 1'b0: N 1'b1: Y

GPIO6_IOC_GPIO6C_IE

Address: Operational Base(0x201D8000) + offset (0x0468)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x1	gpio6c3_ie Receiver enable 1'b0: N 1'b1: Y
2	RW	0x1	gpio6c2_ie Receiver enable 1'b0: N 1'b1: Y
1	RW	0x1	gpio6c1_ie Receiver enable 1'b0: N 1'b1: Y
0	RW	0x1	gpio6c0_ie Receiver enable 1'b0: N 1'b1: Y

GPIO6_IOC_GPIO6A_SMT

Address: Operational Base(0x201D8000) + offset (0x0560)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
7	RW	0x1	gpio6a7_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
6	RW	0x1	gpio6a6_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
5	RW	0x1	gpio6a5_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
4	RW	0x1	gpio6a4_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
3	RW	0x1	gpio6a3_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
2	RW	0x1	gpio6a2_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
1	RW	0x1	gpio6a1_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
0	RW	0x1	gpio6a0_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y

GPIO6_IOC_GPIO6B_SMT

Address: Operational Base(0x201D8000) + offset (0x0564)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio6b7_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
6	RW	0x1	gpio6b6_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
5	RW	0x1	gpio6b5_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y

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Bit	Attr	Reset Value	Description
4	RW	0x1	gpio6b4_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
3	RW	0x1	gpio6b3_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
2	RW	0x1	gpio6b2_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
1	RW	0x1	gpio6b1_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
0	RW	0x1	gpio6b0_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y

GPIO6_IOC_GPIO6C_SMT

Address: Operational Base(0x201D8000) + offset (0x0568)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x1	gpio6c3_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
2	RW	0x1	gpio6c2_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
1	RW	0x1	gpio6c1_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
0	RW	0x1	gpio6c0_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y

GPIO6_IOC_GPIO6A_SUS

Address: Operational Base(0x201D8000) + offset (0x0660)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
7	RW	0x0	gpio6a7_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
6	RW	0x0	gpio6a6_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
5	RW	0x0	gpio6a5_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
4	RW	0x0	gpio6a4_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
3	RW	0x0	gpio6a3_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
2	RW	0x0	gpio6a2_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
1	RW	0x0	gpio6a1_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
0	RW	0x0	gpio6a0_sus Weak pull keeper for pad 1'b0: N 1'b1: Y

GPIO6_IOC_GPIO6B_SUS

Address: Operational Base(0x201D8000) + offset (0x0664)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio6b7_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
6	RW	0x0	gpio6b6_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
5	RW	0x0	gpio6b5_sus Weak pull keeper for pad 1'b0: N 1'b1: Y

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Bit	Attr	Reset Value	Description
4	RW	0x0	gpio6b4_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
3	RW	0x0	gpio6b3_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
2	RW	0x0	gpio6b2_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
1	RW	0x0	gpio6b1_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
0	RW	0x0	gpio6b0_sus Weak pull keeper for pad 1'b0: N 1'b1: Y

GPIO6_IOC_GPIO6C_SUS

Address: Operational Base(0x201D8000) + offset (0x0668)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	gpio6c3_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
2	RW	0x0	gpio6c2_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
1	RW	0x0	gpio6c1_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
0	RW	0x0	gpio6c0_sus Weak pull keeper for pad 1'b0: N 1'b1: Y

GPIO6_IOC_GPIO6A_SL

Address: Operational Base(0x201D8000) + offset (0x0760)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:14	RW	0x0	gpio6a7_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
13:12	RW	0x0	gpio6a6_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
11:10	RW	0x0	gpio6a5_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
9:8	RW	0x0	gpio6a4_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
7:6	RW	0x0	gpio6a3_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
5:4	RW	0x0	gpio6a2_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
3:2	RW	0x0	gpio6a1_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
1:0	RW	0x0	gpio6a0_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y

GPIO6_IOC_GPIO6B_SL

Address: Operational Base(0x201D8000) + offset (0x0764)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:14	RW	0x0	gpio6b7_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
13:12	RW	0x0	gpio6b6_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
11:10	RW	0x0	gpio6b5_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
9:8	RW	0x0	gpio6b4_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
7:6	RW	0x0	gpio6b3_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
5:4	RW	0x0	gpio6b2_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
3:2	RW	0x0	gpio6b1_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
1:0	RW	0x0	gpio6b0_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y

GPIO6_IOC_GPIO6C_SL

Address: Operational Base(0x201D8000) + offset (0x0768)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:8	RO	0x00	reserved
7:6	RW	0x0	gpio6c3_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
5:4	RW	0x0	gpio6c2_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
3:2	RW	0x0	gpio6c1_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
1:0	RW	0x0	gpio6c0_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y

GPIO6_IOC_GPIO6A_OD

Address: Operational Base(0x201D8000) + offset (0x0860)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio6a7_od For open drain functionality 1'b0: N 1'b1: Y
6	RW	0x0	gpio6a6_od For open drain functionality 1'b0: N 1'b1: Y
5	RW	0x0	gpio6a5_od For open drain functionality 1'b0: N 1'b1: Y
4	RW	0x0	gpio6a4_od For open drain functionality 1'b0: N 1'b1: Y
3	RW	0x0	gpio6a3_od For open drain functionality 1'b0: N 1'b1: Y

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Bit	Attr	Reset Value	Description
2	RW	0x0	gpio6a2_od For open drain functionality 1'b0: N 1'b1: Y
1	RW	0x0	gpio6a1_od For open drain functionality 1'b0: N 1'b1: Y
0	RW	0x0	gpio6a0_od For open drain functionality 1'b0: N 1'b1: Y

GPIO6_IOC_GPIO6B_OD

Address: Operational Base(0x201D8000) + offset (0x0864)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio6b7_od For open drain functionality 1'b0: N 1'b1: Y
6	RW	0x0	gpio6b6_od For open drain functionality 1'b0: N 1'b1: Y
5	RW	0x0	gpio6b5_od For open drain functionality 1'b0: N 1'b1: Y
4	RW	0x0	gpio6b4_od For open drain functionality 1'b0: N 1'b1: Y
3	RW	0x0	gpio6b3_od For open drain functionality 1'b0: N 1'b1: Y
2	RW	0x0	gpio6b2_od For open drain functionality 1'b0: N 1'b1: Y
1	RW	0x0	gpio6b1_od For open drain functionality 1'b0: N 1'b1: Y
0	RW	0x0	gpio6b0_od For open drain functionality 1'b0: N 1'b1: Y

GPIO6_IOC_GPIO6C_OD

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Address: Operational Base(0x201D8000) + offset (0x0868)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	gpio6c3_od For open drain functionality 1'b0: N 1'b1: Y
2	RW	0x0	gpio6c2_od For open drain functionality 1'b0: N 1'b1: Y
1	RW	0x0	gpio6c1_od For open drain functionality 1'b0: N 1'b1: Y
0	RW	0x0	gpio6c0_od For open drain functionality 1'b0: N 1'b1: Y

GPIO6_IOC_IO_VSEL

Address: Operational Base(0x201D8000) + offset (0x091C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	vccio6_vd vccio6_vd
14	RO	0x0	rkmacphy_voldet
13:2	RO	0x000	reserved
1:0	RW	0x0	poc_vccio6_iddq VCCIO6 iddq control 1'b0: Disable 1'b1: Enable

GPIO6_IOC_GRF_VICIF_M0_CON

Address: Operational Base(0x201D8000) + offset (0x0B94)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	cif_m0_datapath grf_vicif_m0_con
8	RW	0x0	cif_m0_clk_inv_sel grf_vicif_m0_con
7	RO	0x0	reserved
6:0	RW	0x00	cif_m0_clk_delay_num grf_vicif_m0_con

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GPIO6_IOC_GRF_GMACIO_M0_CON0

Address: Operational Base(0x201D8000) + offset (0x0BA0)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:8	RW	0x00	gmacio_m0_clk_rx_dl_cfg grf_gmacio_m1_con0
7	RO	0x0	reserved
6:0	RW	0x00	gmacio_m0_clk_tx_dl_cfg grf_gmacio_m1_con0

GPIO6_IOC_GRF_GMACIO_M0_CON1

Address: Operational Base(0x201D8000) + offset (0x0BA4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:13	RO	0x0	reserved
12:8	RW	0x00	gmacio_m0_rgmii_debug_io grf_gmacio_m1_con1
7:2	RO	0x00	reserved
1	RW	0x0	gmacio_m0_rxclk_dly_ena grf_gmacio_m1_con1
0	RW	0x0	gmacio_m0_txclk_dly_ena grf_gmacio_m1_con1

GPIO6_IOC_GRF_GPIO6_FILTER_CON0

Address: Operational Base(0x201D8000) + offset (0x0C60)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14:10	RW	0x00	grf_gpio6_filter_sel1 GPIO select to go through first filter logic 5'h00: GPIOxA0 5'h01: GPIOxA1 5'h02: GPIOxA2 5'h03: GPIOxA3 5'h04: GPIOxA4 5'h05: GPIOxA5 5'h06: GPIOxA6 5'h07: GPIOxA7 5'h08: GPIOxB0 5'h09: GPIOxB1 5'h0a: GPIOxB2 5'h0b: GPIOxB3 5'h0c: GPIOxB4 5'h0d: GPIOxB5 5'h0e: GPIOxB6 5'h0f: GPIOxB7 5'h10: GPIOxC0 5'h11: GPIOxC1 5'h12: GPIOxC2 5'h13: GPIOxC3 5'h14: GPIOxC4 5'h15: GPIOxC5 5'h16: GPIOxC6 5'h17: GPIOxC7 5'h18: GPIOxD0 5'h19: GPIOxD1 5'h1a: GPIOxD2 5'h1b: GPIOxD3 5'h1c: GPIOxD4 5'h1d: GPIOxD5 5'h1e: GPIOxD6 5'h1f: GPIOxD7
9	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
8:4	RW	0x00	grf_gpio6_filter_sel0 GPIO select to go through first filter logic 5'h00: GPIOxA0 5'h01: GPIOxA1 5'h02: GPIOxA2 5'h03: GPIOxA3 5'h04: GPIOxA4 5'h05: GPIOxA5 5'h06: GPIOxA6 5'h07: GPIOxA7 5'h08: GPIOxB0 5'h09: GPIOxB1 5'h0a: GPIOxB2 5'h0b: GPIOxB3 5'h0c: GPIOxB4 5'h0d: GPIOxB5 5'h0e: GPIOxB6 5'h0f: GPIOxB7 5'h10: GPIOxC0 5'h11: GPIOxC1 5'h12: GPIOxC2 5'h13: GPIOxC3 5'h14: GPIOxC4 5'h15: GPIOxC5 5'h16: GPIOxC6 5'h17: GPIOxC7 5'h18: GPIOxD0 5'h19: GPIOxD1 5'h1a: GPIOxD2 5'h1b: GPIOxD3 5'h1c: GPIOxD4 5'h1d: GPIOxD5 5'h1e: GPIOxD6 5'h1f: GPIOxD7
3:0	RW	0x0	grf_gpio6_filter_en There are four filter circuits for pad in GPIOx, each bit controls the enable of one filter.

GPIO6_IOC_GRF_GPIO6_FILTER_CON1

Address: Operational Base(0x201D8000) + offset (0x0C64)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:10	RW	0x00	grf_gpio6_filter_sel3 GPIO select to go through first filter logic 5'h00: GPIOxA0 5'h01: GPIOxA1 5'h02: GPIOxA2 5'h03: GPIOxA3 5'h04: GPIOxA4 5'h05: GPIOxA5 5'h06: GPIOxA6 5'h07: GPIOxA7

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Bit	Attr	Reset Value	Description
			5'h08: GPIOxB0 5'h09: GPIOxB1 5'h0a: GPIOxB2 5'h0b: GPIOxB3 5'h0c: GPIOxB4 5'h0d: GPIOxB5 5'h0e: GPIOxB6 5'h0f: GPIOxB7 5'h10: GPIOxC0 5'h11: GPIOxC1 5'h12: GPIOxC2 5'h13: GPIOxC3 5'h14: GPIOxC4 5'h15: GPIOxC5 5'h16: GPIOxC6 5'h17: GPIOxC7 5'h18: GPIOxD0 5'h19: GPIOxD1 5'h1a: GPIOxD2 5'h1b: GPIOxD3 5'h1c: GPIOxD4 5'h1d: GPIOxD5 5'h1e: GPIOxD6 5'h1f: GPIOxD7
9	RO	0x0	reserved
8:4	RW	0x00	grf_gpio6_filter_sel2 GPIO select to go through first filter logic 5'h00: GPIOxA0 5'h01: GPIOxA1 5'h02: GPIOxA2 5'h03: GPIOxA3 5'h04: GPIOxA4 5'h05: GPIOxA5 5'h06: GPIOxA6 5'h07: GPIOxA7 5'h08: GPIOxB0 5'h09: GPIOxB1 5'h0a: GPIOxB2 5'h0b: GPIOxB3 5'h0c: GPIOxB4 5'h0d: GPIOxB5 5'h0e: GPIOxB6 5'h0f: GPIOxB7 5'h10: GPIOxC0 5'h11: GPIOxC1 5'h12: GPIOxC2 5'h13: GPIOxC3 5'h14: GPIOxC4 5'h15: GPIOxC5 5'h16: GPIOxC6 5'h17: GPIOxC7 5'h18: GPIOxD0 5'h19: GPIOxD1 5'h1a: GPIOxD2 5'h1b: GPIOxD3 5'h1c: GPIOxD4

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Bit	Attr	Reset Value	Description
			5'h1d: GPIOxD5 5'h1e: GPIOxD6 5'h1f: GPIOxD7
3:0	RO	0x0	reserved

GPIO6_IOC_GRF_GPIO6_FILTER_CON2

Address: Operational Base(0x201D8000) + offset (0x0C68)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio6_filter_count0 Filter counter for first filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

GPIO6_IOC_GRF_GPIO6_FILTER_CON3

Address: Operational Base(0x201D8000) + offset (0x0C6C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio6_filter_count1 Filter counter for second filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

GPIO6_IOC_GRF_GPIO6_FILTER_CON4

Address: Operational Base(0x201D8000) + offset (0x0C70)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio6_filter_count2 Filter counter for third filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

GPIO6_IOC_GRF_GPIO6_FILTER_CON5

Address: Operational Base(0x201D8000) + offset (0x0C74)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio6_filter_count3 Filter counter for fouth filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

23.10 GPIO7_IOC Register Description

23.10.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

23.10.2 Registers Summary

Name	Offset	Size	Reset Value	Description
GPIO7_IOC_GPIO7A_IOMUX_SEL_0	0x00E0	W	0x00000000	GPIO7A IOMUX Select Register 0
GPIO7_IOC_GPIO7A_IOMUX_SEL_1	0x00E4	W	0x00000000	GPIO7A IOMUX Select Register 1
GPIO7_IOC_GPIO7B_IOMUX_SEL_0	0x00E8	W	0x00000000	GPIO7B IOMUX Select Register 0
GPIO7_IOC_GPIO7A_DS_0	0x02C0	W	0x00000F0F	GPIO7A driver strength register 0

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Name	Offset	Size	Reset Value	Description
GPIO7_IOC_GPIO7A_DS_1	0x02C4	W	0x00000F0F	GPIO7A driver strength register 1
GPIO7_IOC_GPIO7A_DS_2	0x02C8	W	0x00000F0F	GPIO7A driver strength register 2
GPIO7_IOC_GPIO7A_DS_3	0x02CC	W	0x00000F0F	GPIO7A driver strength register 3
GPIO7_IOC_GPIO7B_DS_0	0x02D0	W	0x00000F0F	GPIO7B driver strength register 0
GPIO7_IOC_GPIO7A_PULL	0x0370	W	0x0000AAAA	GPIO7A pull register
GPIO7_IOC_GPIO7B_PULL	0x0374	W	0x0000000A	GPIO7B pull register
GPIO7_IOC_GPIO7A_IE	0x0470	W	0x000000FF	GPIO7A input enable register
GPIO7_IOC_GPIO7B_IE	0x0474	W	0x00000003	GPIO7B input enable register
GPIO7_IOC_GPIO7A_SMT	0x0570	W	0x000000FF	GPIO7A receiver enable for schmitter trigger register
GPIO7_IOC_GPIO7B_SMT	0x0574	W	0x00000003	GPIO7B receiver enable for schmitter trigger register
GPIO7_IOC_GPIO7A_SUS	0x0670	W	0x00000000	GPIO7A enable weak pull keeper register
GPIO7_IOC_GPIO7B_SUS	0x0674	W	0x00000000	GPIO7B enable weak pull keeper register
GPIO7_IOC_GPIO7A_SL	0x0770	W	0x00000000	GPIO7A slew rate control register
GPIO7_IOC_GPIO7B_SL	0x0774	W	0x00000000	GPIO7B slew rate control register
GPIO7_IOC_GPIO7A_OD	0x0870	W	0x00000000	GPIO7A open drain register
GPIO7_IOC_GPIO7B_OD	0x0874	W	0x00000000	GPIO7B open drain register
GPIO7_IOC_IO_VSEL	0x0920	W	0x00000000	IO iddq register
GPIO7_IOC_GRF_GPIO7_FILTER_CON0	0x0C80	W	0x00000000	GPIO7 filter config register 0
GPIO7_IOC_GRF_GPIO7_FILTER_CON1	0x0C84	W	0x00000000	GPIO7 filter config register 1
GPIO7_IOC_GRF_GPIO7_FILTER_CON2	0x0C88	W	0x00000000	GPIO6 filter config register 2
GPIO7_IOC_GRF_GPIO7_FILTER_CON3	0x0C8C	W	0x00000000	GPIO7 filter config register 3
GPIO7_IOC_GRF_GPIO7_FILTER_CON4	0x0C90	W	0x00000000	GPIO7 filter config register 4
GPIO7_IOC_GRF_GPIO7_FILTER_CON5	0x0C94	W	0x00000000	GPIO7 filter config register 5
GPIO7_IOC_GRF_DSM_IOC_CON	0x0CA0	W	0x00000000	DSM_IOC con regiseter

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

23.10.3 Detail Registers Description

GPIO7_IOC_GPIO7A_IOMUX_SEL_0

Address: Operational Base(0x201E0000) + offset (0x00E0)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio7a3_sel 4'h0: GPIO7_A3 4'h1: SAI0_LRCK_M0 4'h4: DSM_AUD_LN 4'h5: PWM2_CH7_M1
11:8	RW	0x0	gpio7a2_sel 4'h0: GPIO7_A2 4'h1: SAI0_MCLK_M0 4'h5: PWM2_CH6_M1
7:4	RW	0x0	gpio7a1_sel 4'h0: GPIO7_A1 4'h1: AUPLL_CLK_IN 4'h3: PDM_CLK1_M0 4'h5: PWM2_CH5_M1
3:0	RW	0x0	gpio7a0_sel 4'h0: GPIO7_A0 4'h1: SAI0_SCLK_M0 4'h5: PWM2_CH4_M1

GPIO7_IOC_GPIO7A_IOMUX_SEL_1

Address: Operational Base(0x201E0000) + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RW	0x0	gpio7a7_sel 4'h0: GPIO7_A7 4'h1: SAI0_SDI3_M0 4'h2: SAI0_SDO1_M0 4'h3: PDM_SDI3_M0 4'h6: UART2_RTSN_M1
11:8	RW	0x0	gpio7a6_sel 4'h0: GPIO7_A6 4'h1: SAI0_SDI0_M0 4'h3: PDM_SDI0_M0
7:4	RW	0x0	gpio7a5_sel 4'h0: GPIO7_A5 4'h1: SAI0_SDO0_M0 4'h4: DSM_AUD_LP
3:0	RW	0x0	gpio7a4_sel 4'h0: GPIO7_A4 4'h3: PDM_CLK0_M0 4'h6: UART2_CTSN_M1

GPIO7_IOC_GPIO7B_IOMUX_SEL_0

Address: Operational Base(0x201E0000) + offset (0x00E8)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7:4	RW	0x0	gpio7b1_sel 4'h0: GPIO7_B1 4'h1: SAI0_SDI1_M0 4'h2: SAI0_SDO3_M0 4'h3: PDM_SDI1_M0 4'h4: DSM_AUD_RP 4'h5: I2C1_SDA_M3 4'h6: UART2_TX_M1
3:0	RW	0x0	gpio7b0_sel 4'h0: GPIO7_B0 4'h1: SAI0_SDI2_M0 4'h2: SAI0_SDO2_M0 4'h3: PDM_SDI2_M0 4'h4: DSM_AUD_RN 4'h5: I2C1_SCL_M3 4'h6: UART2_RX_M1

GPIO7_IOC_GPIO7A_DS_0

Address: Operational Base(0x201E0000) + offset (0x02C0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio7a1_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio7a0_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

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GPIO7_IOC_GPIO7A_DS_1

Address: Operational Base(0x201E0000) + offset (0x02C4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio7a3_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio7a2_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO7_IOC_GPIO7A_DS_2

Address: Operational Base(0x201E0000) + offset (0x02C8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio7a5_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x0f	gpio7a4_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO7_IOC_GPIO7A_DS_3

Address: Operational Base(0x201E0000) + offset (0x02CC)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13:8	RW	0x0f	gpio7a7_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio7a6_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO7_IOC_GPIO7B_DS_0

Address: Operational Base(0x201E0000) + offset (0x02D0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x0f	gpio7b1_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)
7:6	RO	0x0	reserved
5:0	RW	0x0f	gpio7b0_ds The drive strength of IO which can be programmed from 0.5mA to 11.5mA, bit0~bit5 controls 0.5/1/2/2/2/4mA of driving ability. The weakest setting is 6'b000001 and the strongest setting is 6'b111111. 6'b000000: Disable 6'b000001: Level0(0.5mA) 6'b000011: Level1(1.5mA) 6'b000111: Level2(3.5mA) 6'b001111: Level3(5.5mA) 6'b011111: Level4(7.5mA) 6'b111111: Level5(11.5mA)

GPIO7_IOC_GPIO7A_PULL

Address: Operational Base(0x201E0000) + offset (0x0370)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x2	gpio7a7_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
13:12	RW	0x2	gpio7a6_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
11:10	RW	0x2	gpio7a5_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

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Bit	Attr	Reset Value	Description
9:8	RW	0x2	gpio7a4_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
7:6	RW	0x2	gpio7a3_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
5:4	RW	0x2	gpio7a2_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
3:2	RW	0x2	gpio7a1_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
1:0	RW	0x2	gpio7a0_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

GPIO7_IOC_GPIO7B_PULL

Address: Operational Base(0x201E0000) + offset (0x0374)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3:2	RW	0x2	gpio7b1_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal
1:0	RW	0x2	gpio7b0_pull Weak pull down/up for pad 2'b00: z 2'b01: up 2'b10: down 2'b11: illegal

GPIO7_IOC_GPIO7A_IE

Address: Operational Base(0x201E0000) + offset (0x0470)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio7a7_ie Receiver enable 1'b0: N 1'b1: Y
6	RW	0x1	gpio7a6_ie Receiver enable 1'b0: N 1'b1: Y
5	RW	0x1	gpio7a5_ie Receiver enable 1'b0: N 1'b1: Y
4	RW	0x1	gpio7a4_ie Receiver enable 1'b0: N 1'b1: Y
3	RW	0x1	gpio7a3_ie Receiver enable 1'b0: N 1'b1: Y
2	RW	0x1	gpio7a2_ie Receiver enable 1'b0: N 1'b1: Y
1	RW	0x1	gpio7a1_ie Receiver enable 1'b0: N 1'b1: Y
0	RW	0x1	gpio7a0_ie Receiver enable 1'b0: N 1'b1: Y

GPIO7_IOC_GPIO7B_IE

Address: Operational Base(0x201E0000) + offset (0x0474)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x1	gpio7b1_ie Receiver enable 1'b0: N 1'b1: Y
0	RW	0x1	gpio7b0_ie Receiver enable 1'b0: N 1'b1: Y

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GPIO7_IOC_GPIO7A_SMT

Address: Operational Base(0x201E0000) + offset (0x0570)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x1	gpio7a7_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
6	RW	0x1	gpio7a6_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
5	RW	0x1	gpio7a5_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
4	RW	0x1	gpio7a4_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
3	RW	0x1	gpio7a3_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
2	RW	0x1	gpio7a2_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
1	RW	0x1	gpio7a1_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y
0	RW	0x1	gpio7a0_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y

GPIO7_IOC_GPIO7B_SMT

Address: Operational Base(0x201E0000) + offset (0x0574)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x1	gpio7b1_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y

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Bit	Attr	Reset Value	Description
0	RW	0x1	gpio7b0_smt Receiver enable for schmitt trigger 1'b0: N 1'b1: Y

GPIO7_IOC_GPIO7A_SUS

Address: Operational Base(0x201E0000) + offset (0x0670)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio7a7_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
6	RW	0x0	gpio7a6_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
5	RW	0x0	gpio7a5_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
4	RW	0x0	gpio7a4_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
3	RW	0x0	gpio7a3_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
2	RW	0x0	gpio7a2_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
1	RW	0x0	gpio7a1_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
0	RW	0x0	gpio7a0_sus Weak pull keeper for pad 1'b0: N 1'b1: Y

GPIO7_IOC_GPIO7B_SUS

Address: Operational Base(0x201E0000) + offset (0x0674)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x0	gpio7b1_sus Weak pull keeper for pad 1'b0: N 1'b1: Y
0	RW	0x0	gpio7b0_sus Weak pull keeper for pad 1'b0: N 1'b1: Y

GPIO7_IOC_GPIO7A_SL

Address: Operational Base(0x201E0000) + offset (0x0770)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RW	0x0	gpio7a7_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
13:12	RW	0x0	gpio7a6_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
11:10	RW	0x0	gpio7a5_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
9:8	RW	0x0	gpio7a4_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
7:6	RW	0x0	gpio7a3_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
5:4	RW	0x0	gpio7a2_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	gpio7a1_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
1:0	RW	0x0	gpio7a0_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y

GPIO7_IOC_GPIO7B_SL

Address: Operational Base(0x201E0000) + offset (0x0774)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3:2	RW	0x0	gpio7b1_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y
1:0	RW	0x0	gpio7b0_sl Slew rate control for the driver section, while driving pad, 2'b11 is fastest and 2'b00 is slowest. Always set to 2'b11 in normal operation. 2'b00: N 2'b11: Y

GPIO7_IOC_GPIO7A_OD

Address: Operational Base(0x201E0000) + offset (0x0870)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:8	RO	0x00	reserved
7	RW	0x0	gpio7a7_od For open drain functionality 1'b0: N 1'b1: Y
6	RW	0x0	gpio7a6_od For open drain functionality 1'b0: N 1'b1: Y
5	RW	0x0	gpio7a5_od For open drain functionality 1'b0: N 1'b1: Y

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Bit	Attr	Reset Value	Description
4	RW	0x0	gpio7a4_od For open drain functionality 1'b0: N 1'b1: Y
3	RW	0x0	gpio7a3_od For open drain functionality 1'b0: N 1'b1: Y
2	RW	0x0	gpio7a2_od For open drain functionality 1'b0: N 1'b1: Y
1	RW	0x0	gpio7a1_od For open drain functionality 1'b0: N 1'b1: Y
0	RW	0x0	gpio7a0_od For open drain functionality 1'b0: N 1'b1: Y

GPIO7_IOC_GPIO7B_OD

Address: Operational Base(0x201E0000) + offset (0x0874)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	RW	0x0	gpio7b1_od For open drain functionality 1'b0: N 1'b1: Y
0	RW	0x0	gpio7b0_od For open drain functionality 1'b0: N 1'b1: Y

GPIO7_IOC_IO_VSEL

Address: Operational Base(0x201E0000) + offset (0x0920)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	vccio7_vd vccio7_vd
14:1	RO	0x0000	reserved
0	RW	0x0	poc_vccio7_iddq VCCIO7 iddq control 1'b0: Disable 1'b1: Enable

GPIO7_IOC_GRF_GPIO7_FILTER_CON0

Address: Operational Base(0x201E0000) + offset (0x0C80)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:10	RW	0x00	grf_gpio7_filter_sel1 GPIO select to go through first filter logic 5'h00: GPIOxA0 5'h01: GPIOxA1 5'h02: GPIOxA2 5'h03: GPIOxA3 5'h04: GPIOxA4 5'h05: GPIOxA5 5'h06: GPIOxA6 5'h07: GPIOxA7 5'h08: GPIOxB0 5'h09: GPIOxB1 5'h0a: GPIOxB2 5'h0b: GPIOxB3 5'h0c: GPIOxB4 5'h0d: GPIOxB5 5'h0e: GPIOxB6 5'h0f: GPIOxB7 5'h10: GPIOxC0 5'h11: GPIOxC1 5'h12: GPIOxC2 5'h13: GPIOxC3 5'h14: GPIOxC4 5'h15: GPIOxC5 5'h16: GPIOxC6 5'h17: GPIOxC7 5'h18: GPIOxD0 5'h19: GPIOxD1 5'h1a: GPIOxD2 5'h1b: GPIOxD3 5'h1c: GPIOxD4 5'h1d: GPIOxD5 5'h1e: GPIOxD6 5'h1f: GPIOxD7
9	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
8:4	RW	0x00	grf_gpio7_filter_sel0 GPIO select to go through first filter logic 5'h00: GPIOxA0 5'h01: GPIOxA1 5'h02: GPIOxA2 5'h03: GPIOxA3 5'h04: GPIOxA4 5'h05: GPIOxA5 5'h06: GPIOxA6 5'h07: GPIOxA7 5'h08: GPIOxB0 5'h09: GPIOxB1 5'h0a: GPIOxB2 5'h0b: GPIOxB3 5'h0c: GPIOxB4 5'h0d: GPIOxB5 5'h0e: GPIOxB6 5'h0f: GPIOxB7 5'h10: GPIOxC0 5'h11: GPIOxC1 5'h12: GPIOxC2 5'h13: GPIOxC3 5'h14: GPIOxC4 5'h15: GPIOxC5 5'h16: GPIOxC6 5'h17: GPIOxC7 5'h18: GPIOxD0 5'h19: GPIOxD1 5'h1a: GPIOxD2 5'h1b: GPIOxD3 5'h1c: GPIOxD4 5'h1d: GPIOxD5 5'h1e: GPIOxD6 5'h1f: GPIOxD7
3:0	RW	0x0	grf_gpio7_filter_en There are four filter circuits for pad in GPIOx, each bit controls the enable of one filter.

GPIO7_IOC_GRF_GPIO7_FILTER_CON1

Address: Operational Base(0x201E0000) + offset (0x0C84)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:10	RW	0x00	grf_gpio7_filter_sel3 GPIO select to go through first filter logic 5'h00: GPIOxA0 5'h01: GPIOxA1 5'h02: GPIOxA2 5'h03: GPIOxA3 5'h04: GPIOxA4 5'h05: GPIOxA5 5'h06: GPIOxA6 5'h07: GPIOxA7

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Bit	Attr	Reset Value	Description
			5'h08: GPIOxB0 5'h09: GPIOxB1 5'h0a: GPIOxB2 5'h0b: GPIOxB3 5'h0c: GPIOxB4 5'h0d: GPIOxB5 5'h0e: GPIOxB6 5'h0f: GPIOxB7 5'h10: GPIOxC0 5'h11: GPIOxC1 5'h12: GPIOxC2 5'h13: GPIOxC3 5'h14: GPIOxC4 5'h15: GPIOxC5 5'h16: GPIOxC6 5'h17: GPIOxC7 5'h18: GPIOxD0 5'h19: GPIOxD1 5'h1a: GPIOxD2 5'h1b: GPIOxD3 5'h1c: GPIOxD4 5'h1d: GPIOxD5 5'h1e: GPIOxD6 5'h1f: GPIOxD7
9	RO	0x0	reserved
8:4	RW	0x00	grf_gpio7_filter_sel2 GPIO select to go through first filter logic 5'h00: GPIOxA0 5'h01: GPIOxA1 5'h02: GPIOxA2 5'h03: GPIOxA3 5'h04: GPIOxA4 5'h05: GPIOxA5 5'h06: GPIOxA6 5'h07: GPIOxA7 5'h08: GPIOxB0 5'h09: GPIOxB1 5'h0a: GPIOxB2 5'h0b: GPIOxB3 5'h0c: GPIOxB4 5'h0d: GPIOxB5 5'h0e: GPIOxB6 5'h0f: GPIOxB7 5'h10: GPIOxC0 5'h11: GPIOxC1 5'h12: GPIOxC2 5'h13: GPIOxC3 5'h14: GPIOxC4 5'h15: GPIOxC5 5'h16: GPIOxC6 5'h17: GPIOxC7 5'h18: GPIOxD0 5'h19: GPIOxD1 5'h1a: GPIOxD2 5'h1b: GPIOxD3 5'h1c: GPIOxD4

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Bit	Attr	Reset Value	Description
			5'h1d: GPIOxD5 5'h1e: GPIOxD6 5'h1f: GPIOxD7
3:0	RO	0x0	reserved

GPIO7_IOC_GRF_GPIO7_FILTER_CON2

Address: Operational Base(0x201E0000) + offset (0x0C88)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio7_filter_count0 Filter counter for first filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

GPIO7_IOC_GRF_GPIO7_FILTER_CON3

Address: Operational Base(0x201E0000) + offset (0x0C8C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio7_filter_count1 Filter counter for second filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

GPIO7_IOC_GRF_GPIO7_FILTER_CON4

Address: Operational Base(0x201E0000) + offset (0x0C90)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio7_filter_count2 Filter counter for third filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

GPIO7_IOC_GRF_GPIO7_FILTER_CON5

Address: Operational Base(0x201E0000) + offset (0x0C94)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	grf_gpio7_filter_count3 Filter counter for fouth filter logic. When this value is n, it will filter pulse which width is n+1 oscillator clock cycle.

GPIO7_IOC_GRF_DSM_IOC_CON

Address: Operational Base(0x201E0000) + offset (0x0CA0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	grf_dsm_aud_rp_ioe_ dsm audio right p ouput enable 1'b0: enable. 1'b1: disable. It is active only "grf_dsm_r_mode is 0"
14	RW	0x0	grf_dsm_aud_rn_ioe_ dsm audio right n ouput enable 1'b0: enable. 1'b1: disable. It is active only "grf_dsm_r_mode is 0"

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Bit	Attr	Reset Value	Description
13	RW	0x0	grf_dsm_aud_lp_ioe_ dsm audio left p ouput enable 1'b0: enable. 1'b1: disable. It is active only "grf_dsm_l_mode is 0"
12	RW	0x0	grf_dsm_aud_ln_ioe_ dsm audio left n ouput enable 1'b0: enable. 1'b1: disable. It is active only "grf_dsm_l_mode is 0"
11	RW	0x0	grf_dsm_r_oe_n dsm right ouput enable 1'b0: enable. 1'b1: disable.
10	RO	0x0	reserved
9	RW	0x0	grf_dsm_r_pu dsm right pull up . 1'b0: not active 1'b1: active
8	RW	0x0	grf_dsm_r_pd dsm right pull down . 1'b0: not active 1'b1: active
7	RW	0x0	grf_dsm_l_oe_n dsm left ouput enable 1'b0: enable. 1'b1: disable.
6	RO	0x0	reserved
5	RW	0x0	grf_dsm_l_pu dsm left pull up . 1'b0: not active 1'b1: active
4	RW	0x0	grf_dsm_l_pd dsm left pull down . 1'b0: not active 1'b1: active
3	RW	0x0	grf_dsm_rpn_pol_swap grf_dsm right port polarity swap 1'b0: not swap. 1'b1: swap the polarity.
2	RW	0x0	grf_dsm_lpn_pol_swap grf_dsm left port polarity swap 1'b0: not swap. 1'b1: swap the polarity.
1	RW	0x0	grf_dsm_r_mode dsm io right audio side mode 1'b0: not use 1'b1: use for dsm right audio side mode
0	RW	0x0	grf_dsm_l_mode dsm io left audio side mode 1'b0: not use 1'b1: use for dsm left audio side mode

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23.11 Application Notes

IOC is usually connected to a functional IP in the following ways (take input as an example):

1) As shown in the Figure 23-1, the IO PAD connects directly to the function IP through IOC, and IOC_IOMUX_SEL controls which IP the signal is input to.

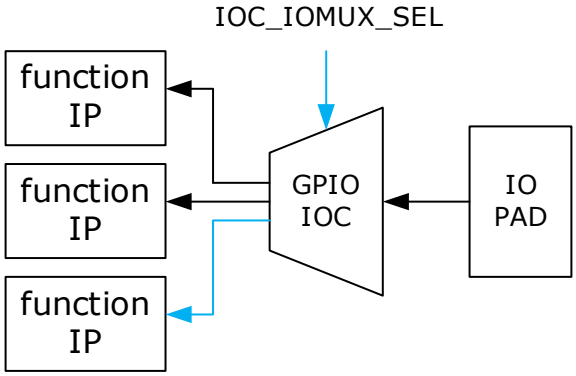

Figure 23-1 Connect directly from IOC to function IP

2) As shown in the Figure 23-2, some IP will be connected to the IO PAD via RMIO and IOC. In this case, you need to configure IOC_IOMUX_SEL to select RMIO and then configure RMIO FUNC_SEL so that one of the IP in the orange box is selected to complete stroking with the IO PAD.

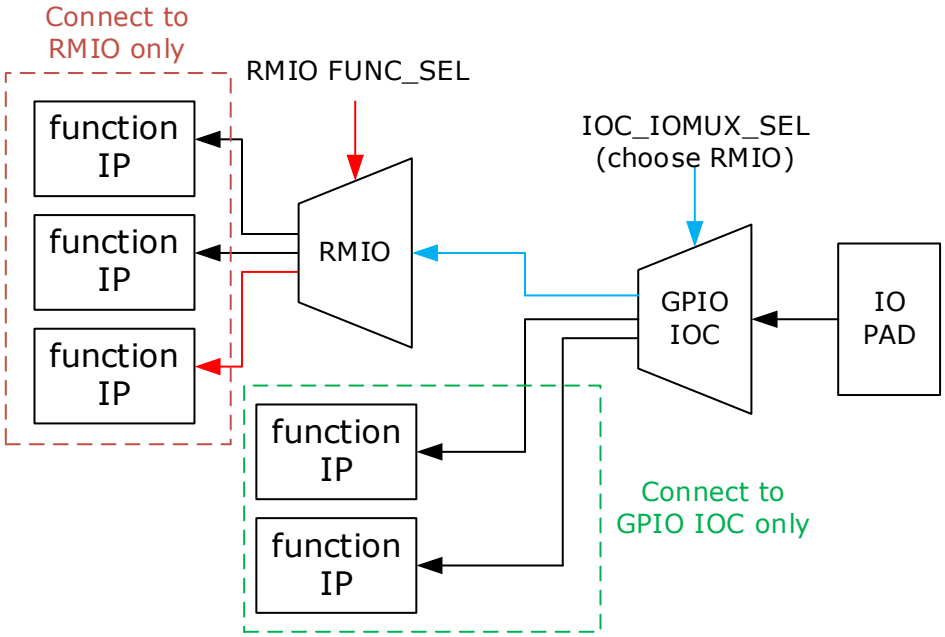

Figure 23-2 Some IPs are connected to the IO PAD through RMIO and IOC

3) As shown in the Figure 23-3, the IP can be connected to the IO PAD only through IOC, or through RMIO+IOC. In addition, this IP can be connected to the IO PAD via different RMIOs (for example, RM0 and RM1). In this case, you need to configure GRF_FUNC_SEL, RMIO_FUNC_SEL, and IOC_IOMUX_SEL to select one of the paths.

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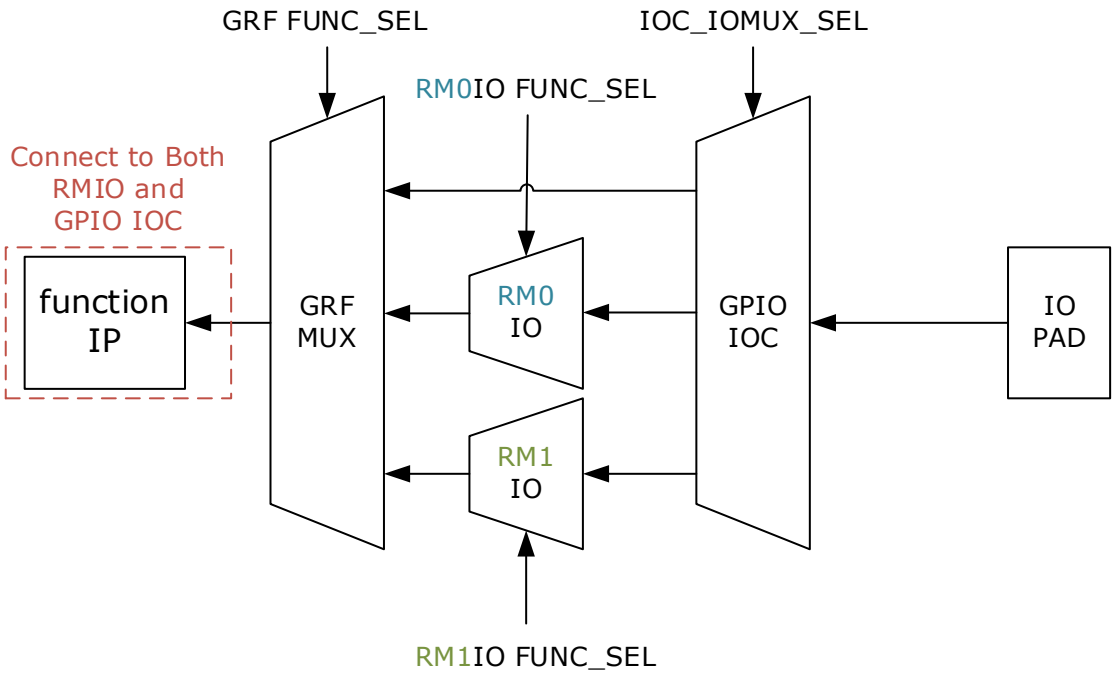

Figure 23-3 IP which has multiple paths connecting to the I/O PAD

If a signal can be connected to the PAD via either RMIO or IOC, you are advised to configure the signal to be routed from IOC.

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Chapter 24 GPIO

24.1 Overview

GPIO is a programmable General Purpose Programming I/O peripheral. This component is an APB slave device. GPIO controls the output data and direction of external I/O pads. It can also read back the data on external pads using memory-mapped registers.
GPIO supports the following features:

- 32 bits APB data bus width
- Up to 32 independently configurable signals
- Software control registers with write mask for each bit of each signal
- Configurable debounce logic with a slow clock to debounce interrupts
- Configurable interrupt mode
- Four virtual OS with independent control registers can be supported
- In virtual OS mode, each OS has independent interrupt

24.2 Block Diagram

GPIO is comprised of:

- APB Interface

The APB Interface implements the APB slave operation. Its data bus width is 32 bits.

- I/O Port Interface

External data interface to or from I/O pads.

- Interrupt Detection

Interrupt interface to or from interrupt controller.

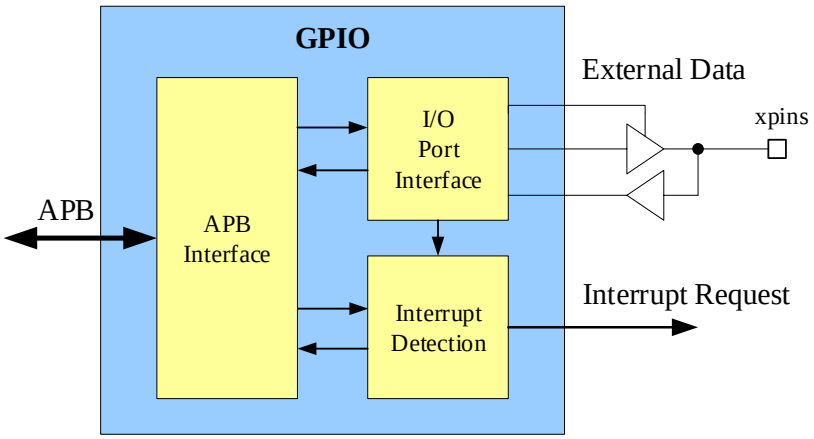

Fig. 24-1 GPIO Block Diagram

24.3 Function Description

24.3.1 Data Control

Under software control, the data and direction control for the signal are sourced from the port data registers (GPIO_SWPORT_DR_L/GPIO_SWPORT_DR_H) and direction control registers (GPIO_SWPORT_DDR_L/GPIO_SWPORT_DRR_H). The direction of the external I/O pad is controlled by the value of the port data direction registers. The data written to these memory-mapped registers gets mapped onto an output signal (gpio_port_ddr) of the GPIO peripheral. This output signal controls the direction of an external I/O pad. The default data direction is Input. The data written to the port data registers drives the output buffer (gpio_port_dr) of the I/O pad.

External data are input on the external data signal (gpio_ext_port). Reading the external signal register (GPIO_EXT_PORT) shows the value of this signal, regardless of the direction. This register is read-only, meaning that it cannot be written from the APB software interface.

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24.3.2 Interrupts

I/O port can be programmed to accept external signals as interrupt sources on any of the bits of the signal. The type of interrupt is programmable with one of the following settings:

- Active-high and level
- Active-low and level
- Rising edge
- Falling edge
- Both the rising edge and the falling edge

The interrupts can be masked by programming the GPIO_INT_MASK_L/GPIO_INT_MASK_H registers. The interrupt status can be read before masking (GPIO_INT_RAWSTATUS) and after masking (GPIO_INT_STATUS).

For edge-sensitive interrupts, the Interrupt Service Routine (ISR) can clear the interrupt by writing a 1'b1 to the corresponding bit of the GPIO_PORT_EOI_L/GPIO_PORT_EOI_H registers. This write operation also clears the interrupt status and raw status registers. Writing to the interrupt clear registers has no effect on level-sensitive interrupts. If level-sensitive interrupts cause the processor to interrupt, then the ISR can poll the interrupt raw status register until the interrupt source disappears, or it can write to the interrupt mask register to mask the interrupt before exiting the ISR. If the ISR exits without masking or disabling the interrupt prior to exiting, then the level-sensitive interrupt repeatedly requests an interrupt until the interrupt is cleared at the source.

The interrupts are combined into an active-high interrupt output signal. In order to mask the combined interrupt, all individual interrupts have to be masked. The single combined interrupt does not have its own mask bit.

Whenever I/O port is configured for interrupts, the data direction must be set to Input. If the data direction is reprogrammed to Output, then any pending edge-sensitive interrupts are not lost. However, no new interrupts are generated, and level-sensitive interrupts are lost.

Interrupt signals are internally synchronized to a system clock pclk_intr, which is connected to the APB bus clock pclk. Therefore, the pclk needs to be running for interrupt detection.

24.3.3 Debounce Operation

The external signal can be debounced to remove any spurious glitches that are less than half period of the external debouncing clock.

When an input interrupt signal is debounced using a slow debounce clock (external input clock dbclk or internal divided clock dbclk_div), the signal must be active for a minimum of one cycle of the debounce clock to guarantee that it is registered. Any input pulse widths less than half debounce clock period are bounced. A pulse width between half and one debounce clock width may or may not propagate, depending on its phase relationship to the debounce clock. If the input pulse spans rising edges and falling edge of the debounce clock, it is registered. If it spans only one edge, it is not registered.

The debounce function can be controlled by programming the debounce enable registers (GPIO_DEBOUNCE_L/GPIO_DEBOUNCE_H), debounce clock divide enable registers (GPIO_DBCLK_DIV_EN_L/GPIO_DBCLK_DIV_EN_H) and debounce clock divide control register (GPIO_DBCLK_DIV_CON).

24.3.4 Four OS Operation and Four Interrupts

To select this mode, virtual enable register should be set (GPIO_VIRTUAL_EN). Then all the configurations can be allotted to four OS (for example OS_A, OS_B, OS_C, OS_D). OS_A will use the original address offset, OS_B will use the offset + 0x1000, OS_C will use the offset + 0x2000, OS_D will use the offset + 0x3000. The 32 bit I/O port should also be allotted to the OS by setting reg group registers (GPIO_REG_GROUP_L and GPIO_REG_GROUP_H). Once reg group is set, the I/O operation can only be used by the

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setting address offset. Each OS has its own interrupt for I/O port, this is depended on reg group.
If virtual enable register is disabled, the reg group can also be used to allocate I/O interrupts. These four independent interrupts may be used for priority interrupt setting.

24.4 Register Description

24.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
GPIO0	0x20600000
GPIO1	0x21300000
GPIO2	0x21700000
GPIO3	0x21E00000
GPIO4	0x21800000
GPIO5	0x21900000
GPIO6	0x21A00000
GPIO7	0x21B00000

24.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
GPIO_SWPORT_DR_L	0x0000	W	0x00000000	Port Data Register (Low)
GPIO_SWPORT_DR_H	0x0004	W	0x00000000	Port Data Register (High)
GPIO_SWPORT_DDR_L	0x0008	W	0x00000000	Port Data Direction Register (Low)
GPIO_SWPORT_DDR_H	0x000C	W	0x00000000	Port Data Direction Register (High)
GPIO_INT_EN_L	0x0010	W	0x00000000	Interrupt Enable Register (Low)
GPIO_INT_EN_H	0x0014	W	0x00000000	Interrupt Enable Register (High)
GPIO_INT_MASK_L	0x0018	W	0x00000000	Interrupt Mask Register (Low)
GPIO_INT_MASK_H	0x001C	W	0x00000000	Interrupt Mask Register (High)
GPIO_INT_TYPE_L	0x0020	W	0x00000000	Interrupt Level Register (Low)
GPIO_INT_TYPE_H	0x0024	W	0x00000000	Interrupt Level Register (High)
GPIO_INT_POLARITY_L	0x0028	W	0x00000000	Interrupt Polarity Register (Low)
GPIO_INT_POLARITY_H	0x002C	W	0x00000000	Interrupt Polarity Register (High)
GPIO_INT_BOTHEDGE_L	0x0030	W	0x00000000	Interrupt Both Edge Type Register (Low)
GPIO_INT_BOTHEDGE_H	0x0034	W	0x00000000	Interrupt Both Edge Type Register (High)
GPIO_DEBOUNCE_L	0x0038	W	0x00000000	Debounce Enable Register (Low)
GPIO_DEBOUNCE_H	0x003C	W	0x00000000	Debounce Enable Register (High)
GPIO_DBCLK_DIV_EN_L	0x0040	W	0x00000000	DBCLK Divide Enable Register (Low)
GPIO_DBCLK_DIV_EN_H	0x0044	W	0x00000000	DBCLK Divide Enable Register (High)
GPIO_DBCLK_DIV_CON	0x0048	W	0x00000001	DBCLK Divide Control Register
GPIO_INT_STATUS	0x0050	W	0x00000000	Interrupt Status Register
GPIO_INT_RAWSTATUS	0x0058	W	0x00000000	Interrupt Raw Status Register
GPIO_PORT_EOI_L	0x0060	W	0x00000000	Interrupt Clear Register (Low)
GPIO_PORT_EOI_H	0x0064	W	0x00000000	Interrupt Clear Register (High)
GPIO_EXT_PORT	0x0070	W	0x00000000	External Port Data Register
GPIO_FLOW_CTRL	0x0074	W	0x00000000	Flow Control Backdoor Register
GPIO_VER_ID	0x0078	W	0x01063F6E	Version ID Register

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Name	Offset	Size	Reset Value	Description
GPIO_STORE_ST_L	0x0080	W	0x00000000	Status Store Register (Low)
GPIO_STORE_ST_H	0x0084	W	0x00000000	Status Store Register (High)
GPIO_GPIO_VIRTUAL_EN	0x0108	W	0x00000000	GPIO Virtual Enable

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

24.4.3 Detail Registers Description

GPIO_SWPORT_DR_L

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	swport_dr_low Output data for the lower 16 bits of I/O Port, each bit is individual. 1'b0: Low 1'b1: High Values written to this register are output on the I/O signals for the lower 16 bits of I/O Port if the corresponding data direction bits for I/O Port are set to Output mode. The value read back is equal to the last value written to this register.

GPIO_SWPORT_DR_H

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	swport_dr_high Output data for the upper 16 bits of I/O Port, each bit is individual. 1'b0: Low 1'b1: High Values written to this register are output on the I/O signals for the upper 16 bits of I/O Port if the corresponding data direction bits for I/O Port are set to Output mode. The value read back is equal to the last value written to this register.

GPIO_SWPORT_DDR_L

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	swport_ddr_low Data direction for the lower 16 bits of I/O Port, each bit is individual. 1'b0: Input 1'b1: Output Values written to this register independently control the direction of the corresponding data bit in the lower 16 bits of I/O Port.

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GPIO_SWPORT_DDR_H

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	swport_ddr_high Data direction for the upper 16 bits of I/O Port, each bit is individual. 1'b0: Input 1'b1: Output Values written to this register independently control the direction of the corresponding data bit in the upper 16 bits of I/O Port.

GPIO_INT_EN_L

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_en_low Allows each bit of the lower 16 bits of I/O Port to be configured for interrupts. 1'b0: Interrupt is disabled 1'b1: Interrupt is enabled Whenever a 1 is written to a bit of this register, it configures the corresponding bit on I/O Port to become an interrupt source; otherwise, I/O Port operates as a normal GPIO signal. Interrupts are disabled on the corresponding bits of I/O Port if the corresponding data direction register is set to Output.

GPIO_INT_EN_H

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_en_high Allows each bit of the upper 16 bits of I/O Port to be configured for interrupts. 1'b0: Interrupt is disabled 1'b1: Interrupt is enabled Whenever a 1 is written to a bit of this register, it configures the corresponding bit on I/O Port to become an interrupt source; otherwise, I/O Port operates as a normal GPIO signal. Interrupts are disabled on the corresponding bits of I/O Port if the corresponding data direction register is set to Output.

GPIO_INT_MASK_L

Address: **Operational Base** + offset (0x0018)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_mask_low Controls whether an interrupt on the lower 16 bits of I/O Port can create an interrupt for the interrupt controller by not masking it. 1'b0: Interrupt is unmasked 1'b1: Interrupt is masked Whenever a 1 is written to a bit in this register, it masks the interrupt generation capability for this signal; otherwise interrupts are allowed through.

GPIO_INT_MASK_H

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_mask_high Controls whether an interrupt on the upper 16 bits of I/O Port can create an interrupt for the interrupt controller by not masking it. 1'b0: Interrupt is unmasked 1'b1: Interrupt is masked Whenever a 1 is written to a bit in this register, it masks the interrupt generation capability for this signal; otherwise interrupts are allowed through.

GPIO_INT_TYPE_L

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_type_low Controls the type of interrupt that can occur on the lower 16 bits of I/O Port. 1'b0: Level-sensitive 1'b1: Edge-sensitive Whenever a 1 is written to a bit of this register, it configures the interrupt type to be edge-sensitive; otherwise, it is level-sensitive.

GPIO_INT_TYPE_H

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	int_type_high Controls the type of interrupt that can occur on the upper 16 bits of I/O Port. 1'b0: Level-sensitive 1'b1: Edge-sensitive Whenever a 1 is written to a bit of this register, it configures the interrupt type to be edge-sensitive; otherwise, it is level-sensitive.

GPIO_INT_POLARITY_L

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_polarity_low Controls the polarity of edge or level sensitivity that can occur on the lower 16 bits of I/O Port. 1'b0: Active-low 1'b1: Active-high Whenever a 1 is written to a bit of this register, it configures the interrupt type to rising-edge or active-high sensitive; otherwise, it is falling-edge or active-low sensitive.

GPIO_INT_POLARITY_H

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_polarity_high Controls the polarity of edge or level sensitivity that can occur on the upper 16 bits of I/O Port. 1'b0: Active-low 1'b1: Active-high Whenever a 1 is written to a bit of this register, it configures the interrupt type to rising-edge or active-high sensitive; otherwise, it is falling-edge or active-low sensitive.

GPIO_INT_BOTHEDGE_L

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	int_bothedge_low Controls the edge type of interrupt that can occur on the lower 16 bits of I/O Port. 1'b0: Disable both-edge detection 1'b1: Enable both-edge detection Whenever a particular bit is programmed to 1, it enables the generation of interrupts on both the rising edge and the falling edge of an external input signal corresponding to that bit on I/O Port. The values programmed in the registers int_type_low and int_polarity_low for this particular bit are not considered when the corresponding bit of this register is set to 1. Whenever a particular bit is programmed to 0, the interrupt type depends on the value of the corresponding bits in the int_type_low and int_polarity_low registers.

GPIO_INT_BOTHEDGE_H

Address: **Operational Base** + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	int_bothedge_high Controls the edge type of interrupt that can occur on the upper 16 bits of I/O Port. 1'b0: Disable both-edge detection 1'b1: Enable both-edge detection Whenever a particular bit is programmed to 1, it enables the generation of interrupts on both the rising edge and the falling edge of an external input signal corresponding to that bit on I/O Port. The values programmed in the registers int_type_high and int_polarity_high for this particular bit are not considered when the corresponding bit of this register is set to 1. Whenever a particular bit is programmed to 0, the interrupt type depends on the value of the corresponding bits in the int_type_high and int_polarity_high registers.

GPIO_DEBOUNCE_L

Address: **Operational Base** + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	debounce_low Controls whether an external signal of the lower 16 bits of I/O Port that is the source of an interrupt needs to be debounced to remove any spurious glitches. 1'b0: Disable debounce 1'b1: Enable debounce Writing a 1 to a bit in this register enables the debouncing circuitry. A signal must be valid for two periods of an external clock before it is internally processed.

GPIO_DEBOUNCE_H

Address: **Operational Base** + offset (0x003C)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	debounce_high Controls whether an external signal of the lower 16 bits of I/O Port that is the source of an interrupt needs to be debounced to remove any spurious glitches. 1'b0: Disable debounce 1'b1: Enable debounce Writing a 1 to a bit in this register enables the debouncing circuitry. A signal must be valid for two periods of an external clock before it is internally processed.

GPIO_DBCLK_DIV_EN_L

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	dbclk_div_en_low Controls whether to use the internal divided clock when debounce function is enabled for an external signal of the lower 16 bits of I/O Port. 1'b0: Disable divider for debounce clock 1'b1: Enable divider for debounce clock Whenever a 1 is written to a bit of this register, the clock divided from dbclk is used as debounce clock; otherwise, the original dbclk is used. The clock divide factor depends on the register dbclk_div_con. The values programmed in this register for this particular bit are not considered when the corresponding bit of the register debounce_low is set to 0.

GPIO_DBCLK_DIV_EN_H

Address: **Operational Base** + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	dbclk_div_en_high Controls whether to use the internal divided clock when debounce function is enabled for an external signal of the upper 16 bits of I/O Port. 1'b0: Disable divider for debounce clock 1'b1: Enable divider for debounce clock Whenever a 1 is written to a bit of this register, the clock divided from dbclk is used as debounce clock; otherwise, the original dbclk is used. The clock divide factor depends on the register dbclk_div_con. The values programmed in this register for this particular bit are not considered when the corresponding bit of the register debounce_high is set to 0.

GPIO_DBCLK_DIV_CON

Address: **Operational Base** + offset (0x0048)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000001	dbclk_div_con dbclk_div = dbclk / (dbclk_div_con + 1)

GPIO_INT_STATUS

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	int_status Interrupt status of I/O Port.

GPIO_INT_RAWSTATUS

Address: **Operational Base** + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	int_rawstatus Interrupt raw status of I/O Port (premasking bits).

GPIO_PORT_EOI_L

Address: **Operational Base** + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	R/WSC	0x0000	port_eoi_low Controls the clearing of edge type interrupts from the lower 16 bits of I/O Port. 1'b0: Nothing 1'b1: Clear edge-sensitive interrupt When a 1 is written into a corresponding bit of this register, the interrupt is cleared and the bit is self cleared at once. Writing to this register has no effect on level-sensitive interrupts. All interrupts are cleared when I/O Port is not configured for interrupts.

GPIO_PORT_EOI_H

Address: **Operational Base** + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	R/WSC	0x0000	port_eoi_high Controls the clearing of edge type interrupts from the upper 16 bits of I/O Port. 1'b0: Nothing 1'b1: Clear edge-sensitive interrupt When a 1 is written into a corresponding bit of this register, the interrupt is cleared and the bit is self cleared at once. Writing to this register has no effect on level-sensitive interrupts. All interrupts are cleared when I/O Port is not configured for interrupts.

GPIO_EXT_PORT

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Address: **Operational Base** + offset (0x0070)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ext_port This register always reflects the value of the signals on the external I/O Port.

GPIO_FLOW_CTRL

Address: **Operational Base** + offset (0x0074)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RO	0x0000	reserved

GPIO_VER_ID

Address: **Operational Base** + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RO	0x01063f6e	ver_id Version ID.

GPIO_STORE_ST_L

Address: **Operational Base** + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	store_st_l This reigister can store the state for each GPIO by user writting to this register.

GPIO_STORE_ST_H

Address: **Operational Base** + offset (0x0084)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	store_st_h This reigister can store the state for each GPIO by user writting to this register.

GPIO_GPIO_VIRTUAL_EN

Address: **Operational Base** + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:1	RO	0x0000	reserved
0	RW	0x0	gpio_virtual_en 1'b1: Enable virtual, four OS supported 1'b0: Disable virtual. Only in GROUP0 with offset 0x0000.

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24.5 Interface Description

Table 24-1 GPIO Interface Description

Module Pin	Pad Name	IOMUX Setting
GPIO0 Interface		
gpio0_port[0]	GPIO0_A0	GPIO0A_IOMUX_SEL_0 [3:0]=4'h0
gpio0_port[1]	GPIO0_A1	GPIO0A_IOMUX_SEL_0 [7:4]=4'h0
gpio0_port[2]	GPIO0_A2	GPIO0A_IOMUX_SEL_0 [11:8]=4'h0
gpio0_port[3]	GPIO0_A3	GPIO0A_IOMUX_SEL_0 [15:12]=4'h0
gpio0_port[4]	GPIO0_A4	GPIO0A_IOMUX_SEL_1[3:0]=4'h0
gpio0_port[5]	GPIO0_A5	GPIO0A_IOMUX_SEL_1 [7:4]=4'h0
gpio0_port[6]	GPIO0_A6	GPIO0A_IOMUX_SEL_1 [11:8]=4'h0
gpio0_port[7]	GPIO0_A7	GPIO0A_IOMUX_SEL_1 [15:11]=4'h0
gpio0_port[8]	GPIO0_B0	GPIO0B_IOMUX_SEL_0 [3:0]=4'h0
gpio0_port[9]	GPIO0_B1	GPIO0B_IOMUX_SEL_0 [7:4]=4'h0
gpio0_port[10]	GPIO0_B2	GPIO0B_IOMUX_SEL_0 [11:8]=4'h0
gpio0_port[11]	GPIO0_B3	GPIO0B_IOMUX_SEL_0 [15:12]=4'h0
gpio0_port[12]	GPIO0_B4	GPIO0B_IOMUX_SEL_1 [3:0]=4'h0
gpio0_port[15:13]		Not used
gpio0_port[16]	GPIO0_C0	GPIO0C_IOMUX_SEL_0 [3:0]=4'h0
gpio0_port[17]	GPIO0_C1	GPIO0C_IOMUX_SEL_0 [7:4]=4'h0
gpio0_port[18]	GPIO0_C2	GPIO0C_IOMUX_SEL_0 [11:8]=4'h0
gpio0_port[19]	GPIO0_C3	GPIO0C_IOMUX_SEL_0 [15:12]=4'h0
gpio0_port[20]	GPIO0_C4	GPIO0C_IOMUX_SEL_1 [3:0]=4'h0
gpio0_port[21]	GPIO0_C5	GPIO0C_IOMUX_SEL_1 [7:4]=4'h0
gpio0_port[22]	GPIO0_C6	GPIO0C_IOMUX_SEL_1 [11:8]=4'h0
gpio0_port[23]	GPIO0_C7	GPIO0C_IOMUX_SEL_1 [15:12]=4'h0
gpio0_port[24]	GPIO0_D0	GPIO0D_IOMUX_SEL_0 [3:0]=4'h0
gpio0_port[25]	GPIO0_D1	GPIO0D_IOMUX_SEL_0 [7:4]=4'h0
gpio0_port[31:26]		Not used
GPIO1 Interface		
gpio1_port[0]	GPIO1_A0	GPIO1A_IOMUX_SEL_0 [3:0]=4'h0
gpio1_port[1]	GPIO1_A1	GPIO1A_IOMUX_SEL_0 [7:4]=4'h0
gpio1_port[2]	GPIO1_A2	GPIO1A_IOMUX_SEL_0 [11:8]=4'h0
gpio1_port[3]	GPIO1_A3	GPIO1A_IOMUX_SEL_0 [15:12]=4'h0
gpio1_port[4]	GPIO1_A4	GPIO1A_IOMUX_SEL_1[3:0]=4'h0
gpio1_port[5]	GPIO1_A5	GPIO1A_IOMUX_SEL_1 [7:4]=4'h0
gpio1_port[6]	GPIO1_A6	GPIO1A_IOMUX_SEL_1 [11:8]=4'h0
gpio1_port[7]	GPIO1_A7	GPIO1A_IOMUX_SEL_1 [15:11]=4'h0
gpio1_port[8]	GPIO1_B0	GPIO1B_IOMUX_SEL_0 [3:0]=4'h0
gpio1_port[9]	GPIO1_B1	GPIO1B_IOMUX_SEL_0 [7:4]=4'h0
gpio1_port[10]	GPIO1_B2	GPIO1B_IOMUX_SEL_0 [11:8]=4'h0
gpio1_port[11]	GPIO1_B3	GPIO1B_IOMUX_SEL_0 [15:12]=4'h0
gpio1_port[12]	GPIO1_B4	GPIO1B_IOMUX_SEL_1 [3:0]=4'h0
gpio1_port[13]	GPIO1_B5	GPIO1B_IOMUX_SEL_1 [7:4]=4'h0
gpio1_port[14]	GPIO1_B6	GPIO1B_IOMUX_SEL_1 [11:8]=4'h0
gpio1_port[15]	GPIO1_B7	GPIO1B_IOMUX_SEL_1 [15:11]=4'h0
gpio1_port[31:16]		Not used
GPIO2 Interface		
gpio2_port[0]	GPIO2_A0	GPIO2A_IOMUX_SEL_0 [3:0]=4'h0
gpio2_port[1]	GPIO2_A1	GPIO2A_IOMUX_SEL_0 [7:4]=4'h0
gpio2_port[2]	GPIO2_A2	GPIO2A_IOMUX_SEL_0 [11:8]=4'h0
gpio2_port[3]	GPIO2_A3	GPIO2A_IOMUX_SEL_0 [15:12]=4'h0
gpio2_port[4]	GPIO2_A4	GPIO2A_IOMUX_SEL_1[3:0]=4'h0

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Module Pin	Pad Name	IOMUX Setting
gpio2_port[5]	GPIO2_A5	GPIO2A_IOMUX_SEL_1 [7:4]=4'h0
gpio2_port[31:6]		Not used
GPIO3 Interface		
gpio3_port[0]	GPIO3_A0	GPIO3A_IOMUX_SEL_0 [3:0]=4'h0
gpio3_port[1]	GPIO3_A1	GPIO3A_IOMUX_SEL_0 [7:4]=4'h0
gpio3_port[2]	GPIO3_A2	GPIO3A_IOMUX_SEL_0 [11:8]=4'h0
gpio3_port[3]	GPIO3_A3	GPIO3A_IOMUX_SEL_0 [15:12]=4'h0
gpio3_port[4]	GPIO3_A4	GPIO3A_IOMUX_SEL_1[3:0]=4'h0
gpio3_port[5]	GPIO3_A5	GPIO3A_IOMUX_SEL_1 [7:4]=4'h0
gpio3_port[6]	GPIO3_A6	GPIO3A_IOMUX_SEL_1 [11:8]=4'h0
gpio3_port[7]	GPIO3_A7	GPIO3A_IOMUX_SEL_1 [15:11]=4'h0
gpio3_port[8]	GPIO3_B0	GPIO3B_IOMUX_SEL_0 [3:0]=4'h0
gpio3_port[9]	GPIO3_B1	GPIO3B_IOMUX_SEL_0 [7:4]=4'h0
gpio3_port[10]	GPIO3_B2	GPIO3B_IOMUX_SEL_0 [11:8]=4'h0
gpio3_port[11]	GPIO3_B3	GPIO3B_IOMUX_SEL_0 [15:12]=4'h0
gpio3_port[12]	GPIO3_B4	GPIO3B_IOMUX_SEL_1 [3:0]=4'h0
gpio3_port[13]	GPIO3_B5	GPIO3B_IOMUX_SEL_1 [7:4]=4'h0
gpio3_port[14]	GPIO3_B6	GPIO3B_IOMUX_SEL_1 [11:8]=4'h0
gpio3_port[15]	GPIO3_B7	GPIO3B_IOMUX_SEL_1 [15:11]=4'h0
gpio3_port[31:16]		Not used
GPIO4 Interface		
gpio4_port[0]	GPIO4_A0	GPIO4A_IOMUX_SEL_0 [3:0]=4'h0
gpio4_port[1]	GPIO4_A1	GPIO4A_IOMUX_SEL_0 [7:4]=4'h0
gpio4_port[2]	GPIO4_A2	GPIO4A_IOMUX_SEL_0 [11:8]=4'h0
gpio4_port[3]	GPIO4_A3	GPIO4A_IOMUX_SEL_0 [15:12]=4'h0
gpio4_port[4]	GPIO4_A4	GPIO4A_IOMUX_SEL_1[3:0]=4'h0
gpio4_port[5]	GPIO4_A5	GPIO4A_IOMUX_SEL_1 [7:4]=4'h0
gpio4_port[6]	GPIO4_A6	GPIO4A_IOMUX_SEL_1 [11:8]=4'h0
gpio4_port[7]	GPIO4_A7	GPIO4A_IOMUX_SEL_1 [15:11]=4'h0
gpio4_port[8]	GPIO4_B0	GPIO4B_IOMUX_SEL_0 [3:0]=4'h0
gpio4_port[9]	GPIO4_B1	GPIO4B_IOMUX_SEL_0 [7:4]=4'h0
gpio4_port[31:10]		Not used
GPIO5 Interface		
gpio5_port[0]	GPIO5_A0	GPIO5A_IOMUX_SEL_0 [3:0]=4'h0
gpio5_port[1]	GPIO5_A1	GPIO5A_IOMUX_SEL_0 [7:4]=4'h0
gpio5_port[2]	GPIO5_A2	GPIO5A_IOMUX_SEL_0 [11:8]=4'h0
gpio5_port[3]	GPIO5_A3	GPIO5A_IOMUX_SEL_0 [15:12]=4'h0
gpio5_port[4]	GPIO5_A4	GPIO5A_IOMUX_SEL_1[3:0]=4'h0
gpio5_port[5]	GPIO5_A5	GPIO5A_IOMUX_SEL_1 [7:4]=4'h0
gpio5_port[6]	GPIO5_A6	GPIO5A_IOMUX_SEL_1 [11:8]=4'h0
gpio5_port[7]	GPIO5_A7	GPIO5A_IOMUX_SEL_1 [15:11]=4'h0
gpio5_port[8]	GPIO5_B0	GPIO5B_IOMUX_SEL_0 [3:0]=4'h0
gpio5_port[9]	GPIO5_B1	GPIO5B_IOMUX_SEL_0 [7:4]=4'h0
gpio5_port[10]	GPIO5_B2	GPIO5B_IOMUX_SEL_0 [11:8]=4'h0
gpio5_port[11]	GPIO5_B3	GPIO5B_IOMUX_SEL_0 [15:12]=4'h0
gpio5_port[12]	GPIO5_B4	GPIO5B_IOMUX_SEL_1 [3:0]=4'h0
gpio5_port[13]	GPIO5_B5	GPIO5B_IOMUX_SEL_1 [7:4]=4'h0
gpio5_port[14]	GPIO5_B6	GPIO5B_IOMUX_SEL_1 [11:8]=4'h0
gpio5_port[15]	GPIO5_B7	GPIO5B_IOMUX_SEL_1 [15:11]=4'h0
gpio5_port[16]	GPIO5_C0	GPIO5C_IOMUX_SEL_0 [3:0]=4'h0
gpio5_port[17]	GPIO5_C1	GPIO5C_IOMUX_SEL_0 [7:4]=4'h0
gpio5_port[18]	GPIO5_C2	GPIO5C_IOMUX_SEL_0 [11:8]=4'h0
gpio5_port[19]	GPIO5_C3	GPIO5C_IOMUX_SEL_0 [15:12]=4'h0
gpio5_port[20]	GPIO5_C4	GPIO5C_IOMUX_SEL_1 [3:0]=4'h0

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Module Pin	Pad Name	IOMUX Setting
gpio5_port[21]	GPIO5_C5	GPIO5C_IOMUX_SEL_1 [7:4]=4'h0
gpio5_port[22]	GPIO5_C6	GPIO5C_IOMUX_SEL_1 [11:8]=4'h0
gpio5_port[23]	GPIO5_C7	GPIO5C_IOMUX_SEL_1 [15:12]=4'h0
gpio5_port[24]	GPIO5_D0	GPIO5D_IOMUX_SEL_0 [3:0]=4'h0
gpio5_port[25]	GPIO5_D1	GPIO5D_IOMUX_SEL_0 [7:4]=4'h0
gpio5_port[26]	GPIO5_D2	GPIO5D_IOMUX_SEL_0 [11:8]=4'h0
gpio5_port[27]	GPIO5_D3	GPIO5D_IOMUX_SEL_0 [15:12]=4'h0
gpio5_port[28]	GPIO5_D4	GPIO5D_IOMUX_SEL_1 [3:0]=4'h0
gpio5_port[29]	GPIO5_D5	GPIO5D_IOMUX_SEL_1 [7:4]=4'h0
gpio5_port[30]	GPIO5_D6	GPIO5D_IOMUX_SEL_1 [11:8]=4'h0
gpio5_port[31]	GPIO5_D7	GPIO5D_IOMUX_SEL_1 [15:12]=4'h0
GPIO6 Interface		
gpio6_port[0]	GPIO6_A0	GPIO6A_IOMUX_SEL_0 [3:0]=4'h0
gpio6_port[1]	GPIO6_A1	GPIO6A_IOMUX_SEL_0 [7:4]=4'h0
gpio6_port[2]	GPIO6_A2	GPIO6A_IOMUX_SEL_0 [11:8]=4'h0
gpio6_port[3]	GPIO6_A3	GPIO6A_IOMUX_SEL_0 [15:12]=4'h0
gpio6_port[4]	GPIO6_A4	GPIO6A_IOMUX_SEL_1[3:0]=4'h0
gpio6_port[5]	GPIO6_A5	GPIO6A_IOMUX_SEL_1 [7:4]=4'h0
gpio6_port[6]	GPIO6_A6	GPIO6A_IOMUX_SEL_1 [11:8]=4'h0
gpio6_port[7]	GPIO6_A7	GPIO6A_IOMUX_SEL_1 [15:11]=4'h0
gpio6_port[8]	GPIO6_B0	GPIO6B_IOMUX_SEL_0 [3:0]=4'h0
gpio6_port[9]	GPIO6_B1	GPIO6B_IOMUX_SEL_0 [7:4]=4'h0
gpio6_port[10]	GPIO6_B2	GPIO6B_IOMUX_SEL_0 [11:8]=4'h0
gpio6_port[11]	GPIO6_B3	GPIO6B_IOMUX_SEL_0 [15:12]=4'h0
gpio6_port[12]	GPIO6_B4	GPIO6B_IOMUX_SEL_1 [3:0]=4'h0
gpio6_port[13]	GPIO6_B5	GPIO6B_IOMUX_SEL_1 [7:4]=4'h0
gpio6_port[14]	GPIO6_B6	GPIO6B_IOMUX_SEL_1 [11:8]=4'h0
gpio6_port[15]	GPIO6_B7	GPIO6B_IOMUX_SEL_1 [15:11]=4'h0
gpio6_port[16]	GPIO6_C0	GPIO6C_IOMUX_SEL_0 [3:0]=4'h0
gpio6_port[17]	GPIO6_C1	GPIO6C_IOMUX_SEL_0 [7:4]=4'h0
gpio6_port[18]	GPIO6_C2	GPIO6C_IOMUX_SEL_0 [11:8]=4'h0
gpio6_port[19]	GPIO6_C3	GPIO6C_IOMUX_SEL_0 [15:12]=4'h0
gpio6_port[31:20]		Not used
GPIO7 Interface		
gpio7_port[0]	GPIO7_A0	GPIO7A_IOMUX_SEL_0 [3:0]=4'h0
gpio7_port[1]	GPIO7_A1	GPIO7A_IOMUX_SEL_0 [7:4]=4'h0
gpio7_port[2]	GPIO7_A2	GPIO7A_IOMUX_SEL_0 [11:8]=4'h0
gpio7_port[3]	GPIO7_A3	GPIO7A_IOMUX_SEL_0 [15:12]=4'h0
gpio7_port[4]	GPIO7_A4	GPIO7A_IOMUX_SEL_1[3:0]=4'h0
gpio7_port[5]	GPIO7_A5	GPIO7A_IOMUX_SEL_1 [7:4]=4'h0
gpio7_port[6]	GPIO7_A6	GPIO7A_IOMUX_SEL_1 [11:8]=4'h0
gpio7_port[7]	GPIO7_A7	GPIO7A_IOMUX_SEL_1 [15:11]=4'h0
gpio7_port[8]	GPIO7_B0	GPIO7B_IOMUX_SEL_0 [3:0]=4'h0
gpio7_port[9]	GPIO7_B1	GPIO7B_IOMUX_SEL_0 [7:4]=4'h0
gpio7_port[31:10]		Not used

Notes: Unused Module Pin is tied to zero!
Notes: I=input, O=output, I/O=input/output, bidirectional

24.6 Application Notes

- Reading from an unused location or unused bits in a particular register always returns zeros. There is no error mechanism in the APB.
- Programming the GPIO registers for interrupt detection should be completed prior to enabling the interrupts in order to prevent spurious glitches on the interrupt output signal to the interrupt controller.

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Chapter 25 Audio ADC

25.1 Overview

Audio ADC is a 24-bit digital audio decoder which supports multiple sample rates. The function of Audio ADC is to convert external MIC input analog signal to I2S/PCM format audio data through a series of filters and volume control. The coding process of Audio ADC is controlled by the register through the APB Bus.

Audio ADC supports the following features.

- Support APB bus slave interface
- Support Analog gain between 0~48dB with 3db/step
- Support 1-channel Differential-mode/Single-mode/Pseudo-differential mode ADC
- Support I2S/PCM master and slave mode
- Support I2S normal, left and right justified mode serial audio data transfer
- Support PCM early, late1, late2, late3 mode serial audio data transfer
- Support MSB or LSB first serial audio data transfer
- Support 16 ~32bit sample resolution
- Support sample rate: 8kHz, 16kHz, 32kHz, 64kHz, 128kHz, 11.025kHz, 22.05kHz, 44.1kHz, 88.2kHz, 176.4kHz, 12kHz, 24kHz, 48kHz, 96kHz, 192kHz
- The passband of filters is 0.45625*fs
- Support passband ripple within +/-0.1dB
- The stopband of filters is 0.5*fs
- Support stopband attenuation at least 60dB
- Support Digital Audio ADC volume control
- Support programmable negative volume gain and positive volume gain

25.2 Block Diagram

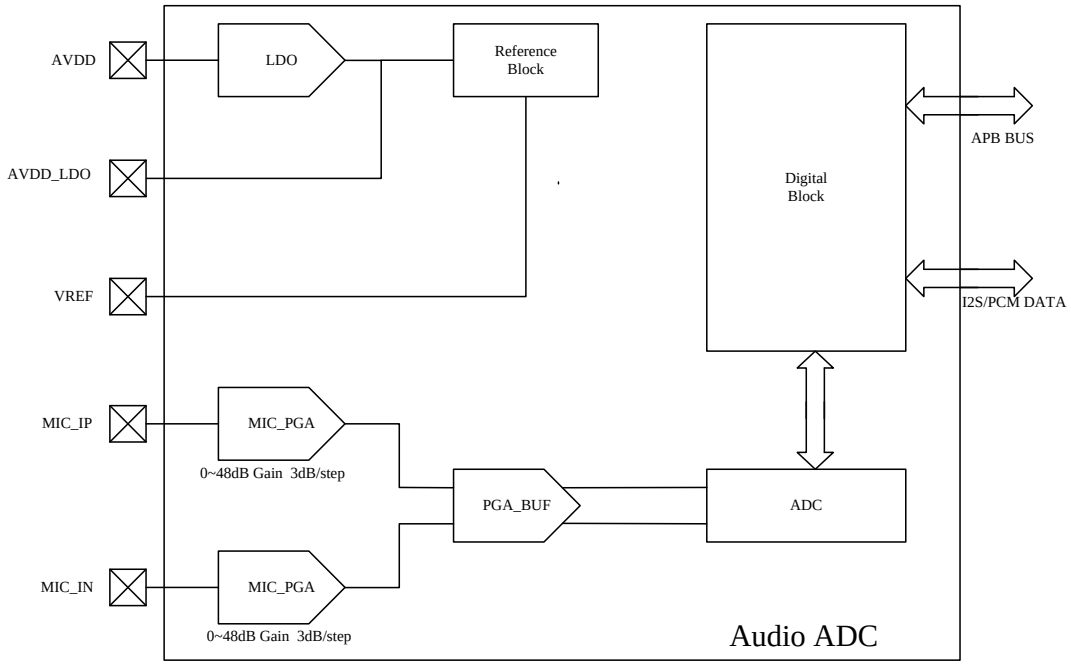

Fig. 25-1 Audio ADC Block Diagram

25.3 Function Description

25.3.1 I2S normal mode

This is the waveform of I2S normal mode. For LRCK (i2s_lrck_tx) signal, it goes low to indicate left channel and high to right channel. For SD (i2s_sdo) signal, it starts sending the first bit (MSB or LSB) one SCLK clock cycle after LRCK changes. The range of SD signal width is from 16 to 32bits. The left and right channels transmit the same data.

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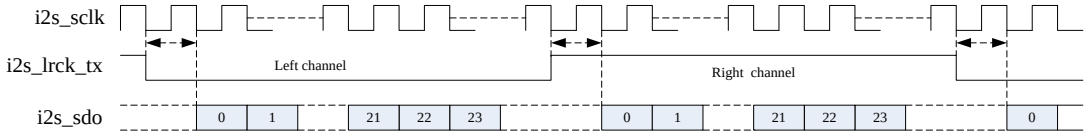

Fig. 25-2 I2S Normal Mode Timing Format

25.3.2 I2S left justified mode

This is the waveform of I2S left justified mode. For LRCK (i2s_lrck_tx) signal, it goes high to indicate left channel and low to right channel. For SD (i2s_sdo) signal, it starts sending the first bit (MSB or LSB) at the same time when LRCK changes. The range of SD signal width is from 16 to 32bits. The left and right channels transmit the same data.

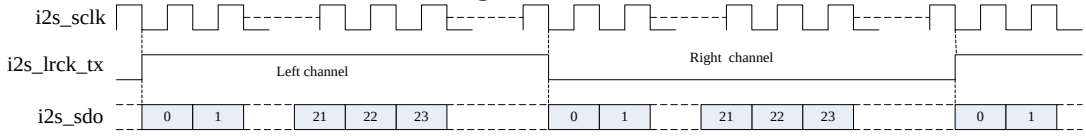

Fig. 25-3 I2S Left Justified Mode Timing Format

25.3.3 I2S right justified mode

This is the waveform of I2S right justified mode. For LRCK (i2s_lrck_tx) signal, it goes high to indicate left channel and low to right channel. For SD (i2s_sdo) signal, it transfers MSB or LSB first; but what is different from I2S normal or left justified mode, the last bit of the transferred data is aligned to the transition edge of the LRCK signal while one bit is transferred at one SCLK cycle. The range of SD signal width is from 16 to 32bits. The left and right channels transmit the same data.

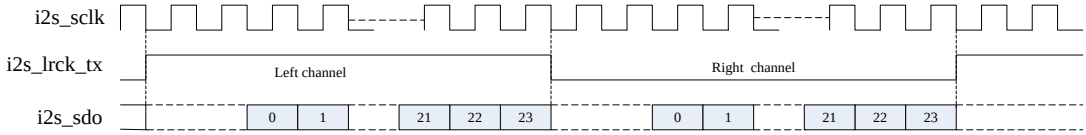

Fig. 25-4 I2S Right Justified Mode Timing Format

25.3.4 PCM early mode

This is the waveform of PCM early mode. For LRCK (i2s_lrck_tx) signal, it goes high to indicate the start of a group of audio channels. For SD (i2s_sdo) signal, it sends the first bit (MSB or LSB) at the same time when LRCK goes high. The range of SD signal width is from 16 to 32bits. The left and right channels transmit the same data.

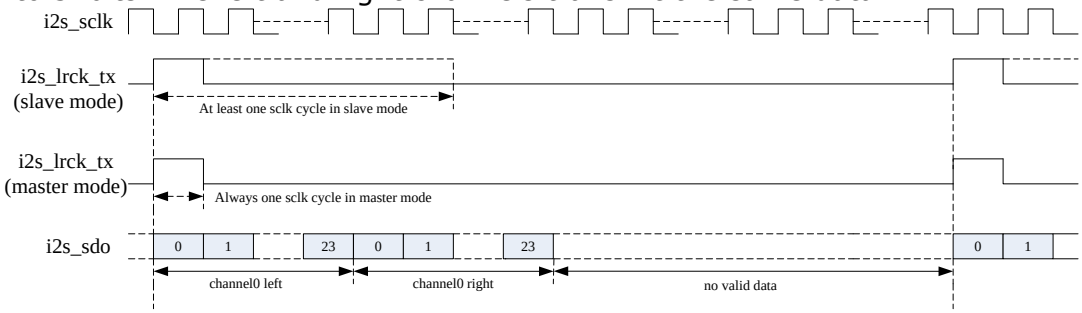

Fig. 25-5 PCM Early Mode Timing Format

25.3.5 PCM late1 mode

This is the waveform of PCM late1 mode. For LRCK (i2s_lrck_tx) signal, it goes high to indicate the start of a group of audio channels. For SD (i2s_sdo) signal, it sends the first bit (MSB or LSB) one SCLK clock cycle after LRCK goes high. The range of SD signal width is from 16 to 32bits. The left and right channels transmit the same data.

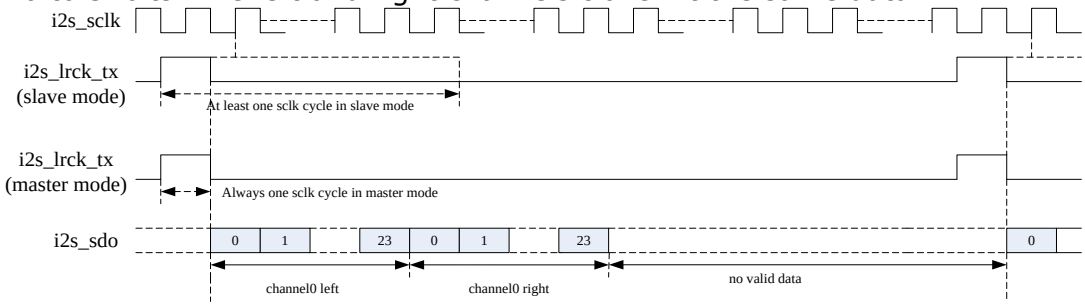

Fig. 25-6 PCM Late1 Mode Timing Format

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25.3.6 PCM late2 mode

This is the waveform of PCM late2 mode. For LRCK (i2s_lrck_tx) signal, it goes high to indicate the start of a group of audio channels. For SD (i2s_sdo) signal, it sends the first bit (MSB or LSB) two SCLK clock cycles after LRCK goes high. The range of SD signal width is from 16 to 32bits. The left and right channels transmit the same data.

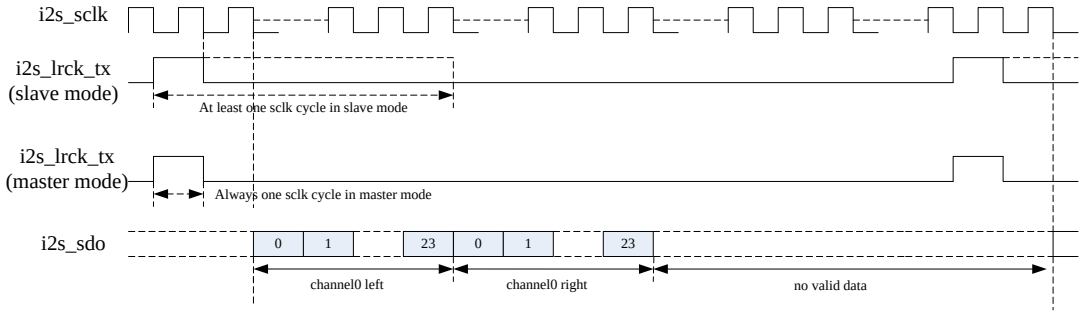

Fig. 25-7 PCM Late2 Mode Timing Format

25.3.7 PCM late3 mode

This is the waveform of PCM late3 mode. For LRCK (i2s_lrck_tx) signal, it goes high to indicate the start of a group of audio channels. For SD (i2s_sdo) signal, it sends the first bit (MSB or LSB) three SCLK clock cycles after LRCK goes high. The range of SD signal width is from 16 to 32bits. The left and right channels transmit the same data.

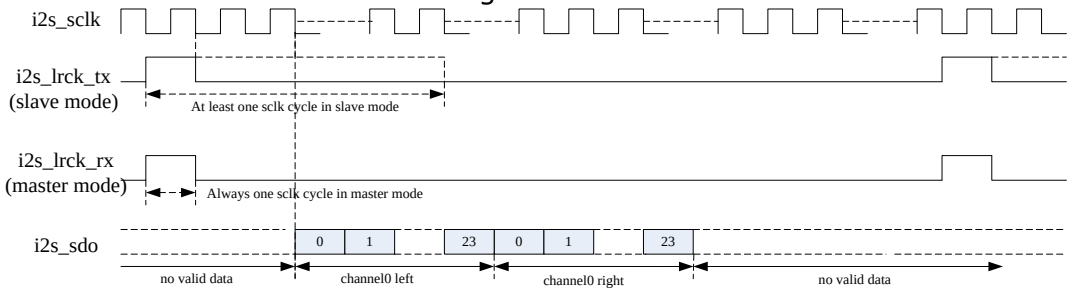

Fig. 25-8 PCM Late3 Mode Timing Format

25.3.8 Digital Filters

In order to achieve PCM format audio data from input 1-bit data stream, a total of 5 filters are embedded in ADC module. It includes a CIC decimation filter, a compensation filter, 2 half-band filters and a high pass filter.

The CIC decimation filter achieves 8-timse or 16-times or 32-times or 64-times or 128-times decimation. Which decimation rate is selected depends on the sample rate. For example, in order to output a 12K sample rate signal, 128-times decimation rate need to be selected.

Compensation filter is connected in series following CIC filter. Its function is to reduce the ripple of CIC filter output. It can be software enabled or disabled. It is valid only when CIC decimation filter works in 32-times or 64-times decimation.

The 2 half-band filters each perform 2-times decimation.

The high pass filter is used to filter DC components in audio data stream. The result of high pass filter is sent to the volume control.

25.3.9 Volume Control

The PCM format data output from the high pass filter are fed into the volume control. It can be digitally attenuated over a range of -95.625dB~0dB in 0.375dB/step for negative gain. The ADC IP has an 8-bit register for volume control. For negative gain, 0xff corresponds to digital mute while 0x00 corresponds to 0dB.

25.3.10 Frequency Configuration

ACDC_CLK is the input clock of Audio ADC. All internal clocks are generated by ACDC_CLK if the I2S module acts as a master. ACDC_CLK must be homologous to the operation clock of I2S master when the I2S module of Audio ADC acts as a slave. There is another clock named ADC_CLK acting as sample clock generated from ACDC_CLK and sent out to the Analogy Audio ADC. The relationship of ACDC_CLK, ADC_CLK and sample rates is as follows where the ACDC_CLK is 8 times of ADC_CLK. Make sure that the frequency of ACDC_CLK is at least 8 times of ADC_CLK.

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Table 25-1 Relationship of ACDC_CLK, ADC_CLK and Sample Rates in Normal Mode

ACDC_CLK	ADC_CLK	Sample rate supported
49.152MHz	6.144MHz	12k/24k/48k/96k/192k
45.1584 MHz	5.6448 MHz	11.025k/22.05k/44.1k/88.2k/176.4k
32.768MHz	4.096MHz	8k/16k/32k/64k/128k

25.4 Register Description

25.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
Audio ADC BUS	0x20BF0000
Audio ADC LP	0x20890000

25.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
Audio_ADC_ADC_0	0x0008	W	0x00000001	Main ADC Function Setting Register 0
Audio_ADC_ADC_1	0x000C	W	0x00000021	Main ADC Function Setting Register 1
Audio_ADC_ADC_2	0x0010	W	0x00000002	Main ADC Function Setting Register 2
Audio_ADC_MIC_PGA_0	0x0014	W	0x00000001	MIC_PGA Block Setting Register 0
Audio_ADC_MIC_PGA_1	0x0018	W	0x00000000	MIC_PGA Block Setting Register 1
Audio_ADC_MIC_PGA_2	0x001C	W	0x00000000	MIC_PGA Block Setting Register 2
Audio_ADC_ADC_LDO	0x0020	W	0x00000008	ADC LDO Setting Register
Audio_ADC_ADC_HK_0	0x0024	W	0x00000000	ADC Housekeeping Block Setting Register 0
Audio_ADC_ADC_HK_1	0x0028	W	0x00000000	ADC Housekeeping Block Setting Register 1
Audio_ADC_DIG_CLKEN	0x002C	W	0x00000000	Digital Enable and Clock Control Register
Audio_ADC_VOL_CTL	0x0030	W	0x00000000	Volume of Digital ADC Configure Register
Audio_ADC_ADC_AGC0	0x0034	W	0x00000002	Digital AGC Configure Register 0
Audio_ADC_ADC_AGC1	0x0038	W	0x00000000	Digital AGC Configure Register 1
Audio_ADC_ADC_AGC2	0x003C	W	0x00000070	Digital AGC Configure Register 2
Audio_ADC_ADC_AGC3	0x0040	W	0x00000006	Digital AGC Configure Register 3
Audio_ADC_ADC_AGC4	0x0044	W	0x00000060	Digital AGC Configure Register 4
Audio_ADC_ADC_AGC5	0x0048	W	0x00000007	Digital AGC Configure Register 5
Audio_ADC_ADC_AGC6	0x004C	W	0x0000005A	Digital AGC Configure Register 6
Audio_ADC_ADC_AGC7	0x0050	W	0x00000004	Digital AGC Configure Register 7
Audio_ADC_ADC_AGC8	0x0054	W	0x00000066	Digital AGC Configure Register 8
Audio_ADC_ADC_STATUS0	0x0058	W	0x00000000	ADC Status Register 0
Audio_ADC_ADC_STATUS1	0x005C	W	0x00000000	ADC Status Register 1
Audio_ADC_ADC_FILTER	0x0060	W	0x0000000B	Digital Filter Configure Register
Audio_ADC_I2S_CKM	0x0064	W	0x00000001	I2S Clock Control Register
Audio_ADC_I2S_TXCR0	0x0068	W	0x000000B8	I2S TX Control Register 0
Audio_ADC_I2S_TXCR1	0x006C	W	0x00000000	I2S TX Control Register 1

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Name	Offset	Size	Reset Value	Description
Audio_ADC_I2S_TXCMD	0x0070	W	0x00000000	I2S TX Command Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

25.4.3 Detail Registers Description

Audio_ADC_ADC_0

Address: Operational Base(0xFF4F8000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	adc_delay_clksel ADC sample clock delay control 2'b00: Delay 100% 2'b01: Delay 75% 2'b10: Delay 50% 2'b11: Delay 25%
5:4	RW	0x0	adc_delay_intsel Internal ADC delay control 2'b00: Delay 100% 2'b01: Delay 75% 2'b10: Delay 50% 2'b11: Delay 25%
3:2	RW	0x0	adc_meth_ctrl Meth code select 2'b00: Thermometer code 2'b01: Normal math code 2'b10: One-direction math code 2'b11: Dual-direction math code
1	RW	0x0	adc_zero ADC integrator reset 1'b0: ADC working 1'b1: ADC reset to zero
0	RW	0x1	adc_pwd Analog ADC power down configure 1'b0: Power on 1'b1: Power down

Audio_ADC_ADC_1

Address: Operational Base(0xFF4F8000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	adc_stop_rtz Turn off the RTZ function 1'b0: RTZ on 1'b1: RTZ off
6:4	RW	0x2	adc_ibctrl ADC ibias control 3'b000: 133% 3'b001: 114% 3'b010: 100% 3'b011: 89% 3'b100: 80% 3'b101: 73% 3'b110: 67% 3'b111: 62%

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Bit	Attr	Reset Value	Description
3	RW	0x0	adc_ibop3_inc Increasing ibias of the 3rd integrator 1'b0: 100% 1'b1: 150%
2	RW	0x0	adc_ibop2_inc Increasing ibias of the 2nd integrator 1'b0: 100% 1'b1: 200%
1:0	RW	0x1	adc_ibop1_ctrl Ibias of the 1st integrator control 2'b00: 50% 2'b01: 100% 2'b10: 150% 2'b11: 200%

Audio_ADC_ADC_2

Address: Operational Base(0xFF4F8000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	adc_out_sel ADC output data select 1'b0: Select SDM output as output data 1'b1: Select one clock as output data
5	RW	0x0	adc_chop_sel ADC chop frequency control 1'b0: High speed 1'b1: Low speed
4	RW	0x0	adc_chop_en ADC chop enable 1'b0: Chop on 1'b1: Chop off
3	RW	0x0	adc_eld_off ADC ELD disable control 1'b0: ELD on 1'b1: ELD off
2:0	RW	0x2	adc_captrim Integrator cap calibration control 3'b000: 80% 3'b001: 90% 3'b010: 100% 3'b011: 110% 3'b100: 120% 3'b101: 130% 3'b110: 140% 3'b111: 150%

Audio_ADC_MIC_PGA_0

Address: Operational Base(0xFF4F8000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:3	RW	0x00	mic_pga_gain mic_pga output gain increase 5'h00: 0dB 5'h10: 3dB 5'h11: 6dB

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Bit	Attr	Reset Value	Description
			5'h12: 9dB 5'h13: 12dB 5'h14: 15dB 5'h15: 18dB 5'h16: 21dB 5'h17: 24dB 5'h18: 27dB 5'h19: 30dB 5'h1A: 33dB 5'h1B: 36dB 5'h1C: 39dB 5'h1D: 42dB 5'h1E: 45dB 5'h1F: 48dB others: 0dB
2:1	RW	0x0	mic_pga_input_dec mic_pga input gain decrease 2'b00: -1.34dB 2'b01: -4.34dB 2'b10: -7.34dB 2'b11: -10.34dB
0	RW	0x1	mic_pga_pwd mic_pga and pga_buf power down 1'b0: mic_pga and pga_buf enable 1'b1: mic_pga and pga_buf disable

Audio_ADC_MIC_PGA_1

Address: Operational Base(0xFF4F8000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:2	RW	0x0	mic_pga_ibias_ctrl mic_pga ibias ctrl 2'b00: 100% (default) 2'b01: 67% 2'b10: 133% 2'b11: 167%
1:0	RW	0x0	mic_pga_chop_sel mic_pga chop clock select 2'b00: No chop (default) 2'b01: fchop=200K 2'b10: fchop=400K 2'b11: fchop=800K

Audio_ADC_MIC_PGA_2

Address: Operational Base(0xFF4F8000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:3	RW	0x0	pga_buf_chop_sel pga_buf chop clock select 2'b00: No chop 2'b01: fchop=200K 2'b10: fchop=400K 2'b11: fchop=800K

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Bit	Attr	Reset Value	Description
2:1	RW	0x0	pga_buf_ib_sel mic_pga ibias ctrl 2'b00: 100% 2'b01: 67% 2'b10: 133% 2'b11: 167%
0	RW	0x0	pga_buf_gain_sel pga_buf gain select 1'b0: 0dB for differential mod 1'b1: 6dB for single mod

Audio_ADC_ADC_LDO

Address: Operational Base(0xFF4F8000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	adc_ip_en ADC enable 1'b0: Disable 1'b1: Enable
6:4	RO	0x0	reserved
3:2	RW	0x2	ldo_vsel LDO 1P6V output voltage select 2'b00: 1.5V 2'b01: 1.55V 2'b10: 1.6V 2'b11: 1.65V
1	RW	0x0	ldo_bypass_en LDO_1P6V bypass mode control. 1'b0: Off 1'b1: On
0	RO	0x0	reserved

Audio_ADC_ADC_HK_0

Address: Operational Base(0xFF4F8000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	hk_ibias_sel hk_ibias_current control: 4'h0: 100% 4'h1: 80% 4'h2: 66% 4'h7: 36% 4'h8: 200% 4'h9: 160% 4'hA 133% 4'hB: 114%
3	RW	0x0	hk_adc_buf_en adc_buf enable control 1'b0: Disable 1'b1: Enable
2	RW	0x0	hk_vag_buf_en vag_buf enable control 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
1	RW	0x0	hk_half_adc_buf adc_buf_bias_half enable control 1'b0: Disable 1'b1: Enable
0	RW	0x0	hk_half_vag_buf vag_buf_bias_half enable control 1'b0: Disable 1'b1: Enable

Audio_ADC_ADC_HK_1

Address: Operational Base(0xFF4F8000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:2	RW	0x0	hk_vag_cur_sel hk_vag_buf_cur_sel control 2'b00: 6uA 2'b01: 4uA 2'b10: 3uA 2'b11: 1uA
1:0	RW	0x0	hk_vref_1p2v_sel hk_vref_1p2v_sel<1:0>: 2'b00: normal (default=1.2) 2'b01: normal - 10m 2'b10: normal + 10m 2'b11: normal - 20m

Audio_ADC_DIG_CLKEN

Address: Operational Base(0xFF4F8000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	adc_cke ADC clock enable. 1'b0: Disable 1'b1: Enable
6	RW	0x0	i2stx_cke Clock enable of internal I2S TX channel. 1'b0: Disable 1'b1: Enable
5	RW	0x0	adc_en ADC channel enable. 1'b0: Disable 1'b1: Enable
4	RW	0x0	i2stx_en I2S TX channel enable. 1'b0: Disable 1'b1: Enable
3	RW	0x0	srst Soft reset, write 1 to reset all registers to default value. 1'b0: Not reset 1'b1: Reset

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Bit	Attr	Reset Value	Description
2:0	RW	0x0	adcsrt Selects which kind of sample rate. 3'b000: 12kHz/11.025kHz/8kHz 3'b001: 24kHz/22.05kHz/16kHz 3'b010: 48kHz/44.1kHz/32kHz 3'b011: 96kHz/88.2kHz/64kHz 3'b100~3'b111: 192kHz/176.4kHz/128kHz

Audio_ADC_VOL_CTL

Address: Operational Base(0xFF4F8000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	adc_volume ADC path Digital Volume Register. 0dB~-95.625dB, -0.375dB/step. 8'h0: 0dB 8'h1: -0.375dB 8'h2: -0.75dB 8'h3: -1.125dB ... 8'hFF: -95.625dB

Audio_ADC_ADC_AGC0

Address: Operational Base(0xFF4F8000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	adc_agc_offset LSB 4bits of adc_agc_offset; adc_agc_offset: Adjust calculated received signal power in dB, it is represented by two's complement with 1 sign bit, 4 integer bits, 4 fractional bits. 9'h000: 0 dB 9'h001: 0.0625 dB 9'h002: 0.125 dB 9'h003: 0.1875 dB 9'h004: 0.25 dB ... 9'h0FF: 15.9375 dB 9'h100: -16 dB 9'h101: -15.9375 dB 9'h102: -15.875 dB ... 9'h1FF: -0.0625 dB
3	RW	0x0	adc_byps ADC volume control bypass. 1'b0: ADC volume control enable 1'b1: ADC volume control bypass
2	RW	0x0	agc_zerocren Gain adjusting at zero-crossing enable. 1'b0: Disable 1'b1: Enable
1	RW	0x1	adc_ng_mode_en Noise gate enable. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
0	RW	0x0	adc_agc_ena Automatic Gain control enable. 1'b0: Disable 1'b1: Enable

Audio_ADC_ADC_AGC1

Address: Operational Base(0xFF4F8000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x00	adc_agc_offset MSB 5bits of adc_agc_offset; adc_agc_offset: Adjust calculated received signal power in dB, it is represented by two's complement with 1 sign bit, 4 integer bits, 4 fractional bits. 9'h000: 0 dB 9'h001: 0.0625 dB 9'h002: 0.125 dB 9'h003: 0.1875 dB 9'h004: 0.25 dB ... 9'h0FF: 15.9375 dB 9'h100: -16 dB 9'h101: -15.9375 dB 9'h102: -15.875 dB ... 9'h1FF: -0.0625 dB

Audio_ADC_ADC_AGC2

Address: Operational Base(0xFF4F8000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x70	adc_ng_rssi_db LSB 8bits of adc_ng_rssi_db; adc_ng_rssi_db: noise gate threshold in dB, it is represented by two's complement with 1 sign bit, 7 integer bits, 3 fractional bits. 11'h000: 0 dB 11'h001: 0.125 dB 11'h002: 0.25 dB ... 11'h400: -128 dB 11'h401: -127.875 dB 11'h402: -127.75 dB ... 11'h7FF: -0.125 dB

Audio_ADC_ADC_AGC3

Address: Operational Base(0xFF4F8000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:3	RW	0x00	adc_ng_pga_gain Analog ADC PGA gain configure when in noise gate mode. 5'h00: 0dB 5'h10: 3dB 5'h11: 6dB 5'h12: 9dB 5'h13: 12dB 5'h14: 15dB 5'h15: 18dB 5'h16: 21dB 5'h17: 24dB 5'h18: 27dB 5'h19: 30dB 5'h1A: 33dB 5'h1B: 36dB 5'h1C: 39dB 5'h1D: 42dB 5'h1E: 45dB 5'h1F: 48dB others: 0dB
2:0	RW	0x6	adc_ng_rssi_db MSB 3bits of adc_ng_rssi_db; adc_ng_rssi_db: noise gate threshold in dB, it is represented by two's complement with 1 sign bit, 7 integer bits, 3 fractional bits. 11'h000: 0 dB 11'h001: 0.125 dB 11'h002: 0.25 dB ... 11'h400: -128 dB 11'h401: -127.875 dB 11'h402: -127.75 dB ... 11'h7FF: -0.125 dB

Audio_ADC_ADC_AGC4

Address: Operational Base(0xFF4F8000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x60	adc_tar_db LSB 8bits of adc_tar_db; adc_tar_db: target output signal power in dB, it is represented by two's complement with 1 sign bit, 7 integer bits, 3 fractional bits. 11'h000: 0 dB 11'h001: 0.125 dB 11'h002: 0.25 dB ... 11'h400: -128 dB 11'h401: -127.875 dB 11'h402: -127.75 dB ... 11'h7FF: -0.125 dB

Audio_ADC_ADC_AGC5

Address: Operational Base(0xFF4F8000) + offset (0x0048)

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Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:3	RW	0x00	adc_ini_pga_gain Initial Analog ADC PGA gain configure when AGC enable. 5'h00: 0dB 5'h10: 3dB 5'h11: 6dB 5'h12: 9dB 5'h13: 12dB 5'h14: 15dB 5'h15: 18dB 5'h16: 21dB 5'h17: 24dB 5'h18: 27dB 5'h19: 30dB 5'h1A: 33dB 5'h1B: 36dB 5'h1C: 39dB 5'h1D: 42dB 5'h1E: 45dB 5'h1F: 48dB others: 0dB
2:0	RW	0x7	adc_tar_db MSB 3bits of adc_tar_db; adc_tar_db: target output signal power in dB, it is represented by two's complement with 1 sign bit, 7 integer bits, 3 fractional bits. 11'h000: 0 dB 11'h001: 0.125 dB 11'h002: 0.25 dB ... 11'h400: -128 dB 11'h401: -127.875 dB 11'h402: -127.75 dB ... 11'h7FF: -0.125 dB

Audio_ADC_ADC_AGC6

Address: Operational Base(0xFF4F8000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x5a	adc_ng_vol_ctrl Digital volume configure when in noise gate mode. 0dB~-96dB, -0.375dB/step. 8'h0: 0dB 8'h1: -0.375dB 8'h2: -0.75dB 8'h3: -1.125dB ... 8'hFF: -95.625dB

Audio_ADC_ADC_AGC7

Address: Operational Base(0xFF4F8000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x04	adc_ini_vol_ctrl Initial Digital volume configure when AGC enable. 0dB~-96dB, -0.375dB/step. 8'h0: 0dB 8'h1: -0.375dB 8'h2: -0.75dB 8'h3: -1.125dB ... 8'hFF: -95.625dB

Audio_ADC_ADC_AGC8

Address: Operational Base(0xFF4F8000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x6	adc_prattrate_win Attack/release rate = 2^adc_prattrate_win.
3:0	RW	0x6	adc_powdet_win AGC power detect length = 2^adc_powdet_win.

Audio_ADC_ADC_STATUS0

Address: Operational Base(0xFF4F8000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	adcrlv ADC internal volume.

Audio_ADC_ADC_STATUS1

Address: Operational Base(0xFF4F8000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RO	0x0	adc_ngvalid Noise gates valid status. 1'b0: Not in NG status 1'b1: Now in NG status
4:0	RO	0x00	adc_pga_gain_r Gain of ADC PGA block.

Audio_ADC_ADC_FILTER

Address: Operational Base(0xFF4F8000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	hpf_cf HPF Cut Frequency Select. 2'b00: 3.79HZ 2'b01: 60HZ 2'b10: 243HZ 2'b11: 493HZ
5	RO	0x0	reserved
4	RW	0x0	hpfl Digital ADC High Pass Filter Enable. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3:2	RW	0x2	ciccomp_cf CIC Compensation Filter Output Scale Coefficient. 2'b00: 3/8 2'b01: 6/8 2'b10, 2'b11: 1
1	RW	0x1	ciccomp_ena64 CIC compensation filter enable, valid when sample rate is 24kHz/22.05kHz/16kHz. 1'b0: Disable 1'b1: Enable
0	RW	0x1	ciccomp_ena32 CIC compensation filter enable, valid when sample rate is 24kHz/22.05kHz/16kHz. 1'b0: Disable 1'b1: Enable

Audio_ADC_I2S_CKM

Address: Operational Base(0xFF4F8000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	sck_div Interger clock divider to generate sclk when I2S TX works in master mode. It is ignored when in slave mode. sck_div = F(mclk2x)/F(sclk) - 1
3	RO	0x0	reserved
2	RW	0x0	sck_en SCLK clock enable, active in master mode. 1'b0: Disable 1'b1: Enable
1	RW	0x0	sck_p SCLK polarity. 1'b0: Normal 1'b1: Inverted
0	RW	0x1	i2s_mst I2S TX acts as master or slave. 1'b0: Slave mode 1'b1: Master mode

Audio_ADC_I2S_TXCR0

Address: Operational Base(0xFF4F8000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:3	RW	0x17	vdw_tx I2S TX valid data width. 5'h00000-5'h01110: reserved 5'h0f: 16bit 5'h10: 17bit 5'h11: 18bit 5'h12: 19bit ... 5'h17: 24bit 5'h18: 25bit 5'h19: 26bit 5'h1A: 27bit 5'h1B: 28bit

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Bit	Attr	Reset Value	Description
			5'h1C: 29bit 5'h1D: 30bit 5'h1E: 31bit 5'h1F: 32bit
2:1	RW	0x0	sckd_tx Sclk divider for tx_lrck generator. 2'b00: 64 2'b01: 128 2'b10~2'b11: 256 2'b01 valid only if LRCK <= 96k, 2'b10 valid only if LRCK <= 48k
0	RW	0x0	txrl_p I2S TX LRCK polarity. 1'b0: Normal 1'b1: Inverted

Audio_ADC_I2S_TXCR1

Address: Operational Base(0xFF4F8000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	tfs_tx I2S TX transfer mode. 1'b0: I2S 1'b1: PCM
5:4	RW	0x0	pbm_tx I2S TX PCM bus mode. 2'b00: PCM early mode 2'b01: PCM late 1 mode 2'b10: PCM late 2 mode 2'b11: PCM late 3 mode
3:2	RW	0x0	ibm_tx I2S TX bus mode. 2'b00: Normal 2'b01: Left 2'b10: Right
1	RW	0x0	exrl_tx Exchange right/left channel for I2S TX 1'b0: Normal 1'b1: Exchange right and left channel
0	RW	0x0	lsb_tx I2S TX MSB/LSB send first. 1'b0: MSB send first 1'b1: LSB send first

Audio_ADC_I2S_TXCMD

Address: Operational Base(0xFF4F8000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	txs I2S TX transfer start. 1'b0: Stop I2S TX transfer 1'b1: Start I2S TX transfer

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Bit	Attr	Reset Value	Description
6	RW	0x0	txc This is a self-cleared bit. Write 1 to clear all I2S TX transmit logic. 1'b0: No clean the I2STX transmit logic 1'b1: Clean the I2STX transmit logic
5:0	RW	0x00	rcnt_tx Right justified counter for I2S right justified slave mode only.

25.5 Application Notes

25.5.1 Hardware Application Notes:

1. Put the LDO filter cap close to the output Pin of ADC_LDO.
2. Give a Clean ground to the LDO filter cap and AVSS.

25.5.2 Software Application Notes

Steps to configure Audio ADC operates in I2S mode are as follows.

1. Program Audio_ADC_ADC_LDO to power up the HK circuit and LDO circuit.
2. Program the gain of PGA_Block and PGA_Buffer by Audio_ADC_MIC_PGA_0, Audio_ADC_MIC_PGA_1, Audio_ADC_MIC_PGA_2.
3. Program Audio_ADC_DIG_CLKEN to enable operation clocks of I2S module and ADC.
4. Program Audio_ADC_I2S_CKM to select sample rate.
5. Program Audio_ADC_ADC_0 to power up the analog ADC circuit.
6. Enable high pass filter if necessary by Programming Audio_ADC_ADC_FILTER.

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Chapter 26 Audio DSM

26.1 Overview

Audio DSM is a 16-bit digital audio encoder which supports multiple sample rates. It is mainly composed of digital DAC. The aim of digital DAC is to process the data received from I2S/PCM interface through filters, volume control and modulation.
The RK DSM supports the following features.

- Support 8-bit APB and AHB bus slave interface
- Support 2-channel digital DAC
- Support I2S/PCM interface
- Support I2S/PCM master and slave mode
- Support 2-channel audio receiving in I2S mode
- Support 2-channel audio receiving in PCM mode
- Support I2S normal, left and right justified mode serial audio data transfer
- Support PCM early, late1, late2, late3 mode serial audio data transfer
- Support MSB or LSB first serial audio data transfer
- Support configurable SCLK and LRCK polarity
- Support 16 bit sample resolution
- Support programmable left and right channel exchangeable in I2S mode and PCM mode
- Support three modes of mixing for every digital DAC channel
- Support volume control
- Support programmable negative and positive volume gain

26.2 Block Diagram

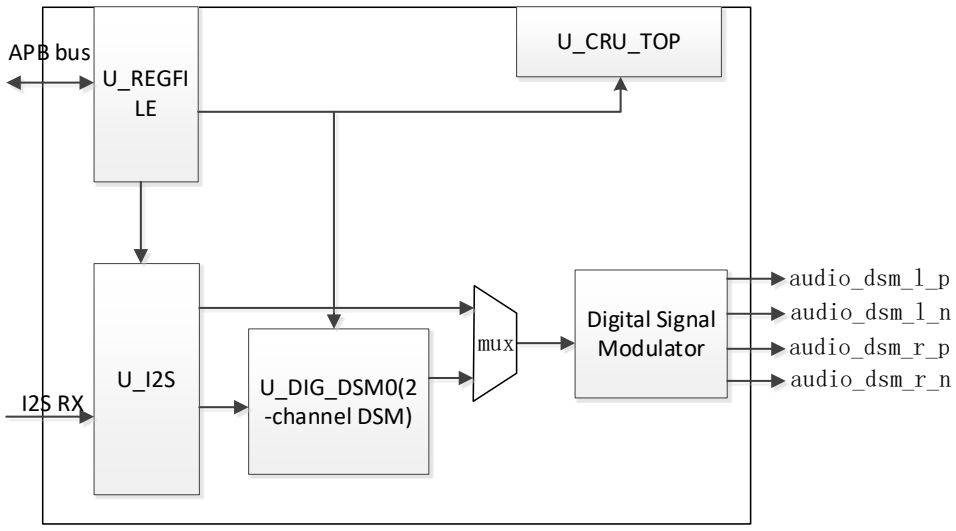

Fig.26-1 RK DSM Block Diagram

RK DSM_RF
The RK DSM_RF implements the 8-bit APB/AHB slave operation through APB/AHB bus. It is responsible for configuring the operation registers of other modules.
RK DSM_CRU
The RK DSM_CRU implements clock and reset generation function. It is responsible for generating sample clock, digital DAC operation clock and I2S operation clock.
RK DSM
There are 2 digital DAC channels. The digital DAC receives audio data from ACDC_I2S module. It includes one CIC filter, one high-pass filter, several low-pass decimation filters and other audio signal processing related modules. The output of digital DAC is sent to DSM modular before transmitting outside.
RK DSM_I2S
The I2S/PCM audio interface can be configured to master mode or slave mode. In Master Mode, SCLK and LRCK are configured as output. In slave mode, SCLK and LRCK are

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configured as input. The RK DSM_I2S module can only operate in RX mode. When in RX mode, it receives audio data from I2S RX interface and sends it to digital DAC.

DSM Modulator

It is a modulator that converts 16 bits audio sample data to 1 bit audio data.

26.3 Function description

The I2S/PCM interface of Digital Audio Codec is connected to the I2S1 controller. Please refer to the I2S chapter for detailed information about I2S and PCM format that Digital Audio Codec supports.

26.3.1 Filters of Digital DAC

I2S module receives two-channel audio data from I2S RX interface and drives it to the digital DAC which supports mixing function or directly to the DSM modulator. How to pour 2-channel audio data into 2-channel digital DAC can be achieved by programming mixing mode.

The 2-channel digital DAC includes a high-pass filter and a maximum of 5 half-band filters. The high-pass filter is used to filter DC components in audio data stream. Result of high-pass filter is sent to the digital DAC volume control module. The input of 5 half-band filters comes from output of volume control module with each perform 2-times interpolation. But not all of them are working all the time. How many of them are needed to work depends on the sample rate of digital DAC. The result of half-band filters is sent to a modulator.

26.3.2 Volume Control

For digital DAC, output of high-pass filters is fed into volume control module. The volume control module inside digital DAC contains several sub-modules such as peak detect, frequency cross zero detect, LIMITER and digital gain control. It can be digitally attenuated over a range of -96dB~0dB in 0.375dB/step for negative gain and amplified over a range of 0dB~96dB in 0.375dB/step for positive gain. Whether is attenuated or amplified can be software programmed.

26.4 Register Description

26.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

26.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
RKDSM_DSMVUCTL	0x0000	W	0x00000001	DAC Volume Control Register
RKDSM_DSMVUCTIME	0x0004	W	0x00000000	DAC Volume Control Time Limit Register
RKDSM_DSMDIGEN	0x0008	W	0x00000000	DAC Digital Enable Register
RKDSM_DSMCLKCTRL	0x000C	W	0x00000000	DAC Clock Control Register
RKDSM_DSMINTMOD_DIV	0x0014	W	0x00000007	DAC Integer Clock Divider Register
RKDSM_DSMINTSCLK_DIV	0x0020	W	0x0000001F	I2S SCLK RX Integer Divider Register
RKDSM_DSM_DIV	0x0024	W	0x00000003	DSM Mode Integer Divider Register
RKDSM_DSM_CTRL	0x0028	W	0x00000000	DSM Mode Control Register
RKDSM_DSMCFG1	0x0044	W	0x00000004	DAC Configure Register 1
RKDSM_DSMMUTE	0x0048	W	0x00000000	DAC Mute Control Register
RKDSM_DSMMUTEST	0x004C	W	0x00000000	DAC Mute Status Register
RKDSM_DSMVOLL0	0x0050	W	0x00000000	Volume of DAC Left Channel 0 Register
RKDSM_DSMVOLL1	0x0054	W	0x00000000	Volume of DAC Left Channel 0 Register

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Name	Offset	Size	Reset Value	Description
RKDSM_DSMVOLL2	0x0058	W	0x00000000	Volume of DAC Left Channel 0 Register
RKDSM_DSMVOLL3	0x005C	W	0x00000000	Volume of DAC Left Channel 0 Register
RKDSM_DSMVOLR0	0x0060	W	0x00000000	Volume of DAC right Channel 1 Register
RKDSM_DSMVOLR1	0x0064	W	0x00000000	Volume of DAC right Channel 1 Register
RKDSM_DSMVOLR2	0x0068	W	0x00000000	Volume of DAC right Channel 1 Register
RKDSM_DSMVOLR3	0x006C	W	0x00000000	Volume of DAC right Channel 1 Register
RKDSM_DSMVOGP	0x0070	W	0x00000000	DAC Volume Gain Polarity Register
RKDSM_DSMRVOLL0	0x0074	W	0x000000FF	Internal Volume of DAC Left Channel 0 Register
RKDSM_DSMRVOLL1	0x0078	W	0x00000000	Internal Volume of DAC Left Channel 0 Register
RKDSM_DSMRVOLL2	0x007C	W	0x00000000	Internal Volume of DAC Left Channel 0 Register
RKDSM_DSMRVOLL3	0x0080	W	0x00000000	Internal Volume of DAC Left Channel 0 Register
RKDSM_DSMRVOLR0	0x0084	W	0x000000FF	Internal Volume of DAC right Channel 1 Register
RKDSM_DSMRVOLR1	0x0088	W	0x00000000	Internal Volume of DAC right Channel 1 Register
RKDSM_DSMRVOLR2	0x008C	W	0x00000000	Internal Volume of DAC right Channel 1 Register
RKDSM_DSMRVOLR3	0x0090	W	0x00000000	Internal Volume of DAC right Channel 1 Register
RKDSM_DSMLMT0	0x0094	W	0x00000000	DAC Limiter Register 0
RKDSM_DSMLMT1	0x0098	W	0x00000000	DAC Limiter Register 1
RKDSM_DSMLMT2	0x009C	W	0x00000000	DAC Limiter Register 2
RKDSM_DSMMIXCTRLL	0x00A0	W	0x00000000	DAC Mixing Control Register Of Left Channels
RKDSM_DSMMIXCTRLR	0x00A4	W	0x00000000	DAC Mixing Control Register Of right Channels
RKDSM_DSMHPF	0x00A8	W	0x00000000	DAC High-pass Filter Control Register
RKDSM_DSM_I2S_RXCR0	0x010C	W	0x0000000F	Receive Operation Control Register 0
RKDSM_DSM_I2S_RXCR1	0x0110	W	0x00000000	Receive Operation Control Register 1
RKDSM_DSM_I2S_CKR0	0x0114	W	0x00000000	Clock Generation Register 0
RKDSM_DSM_I2S_CKR1	0x0118	W	0x00000000	Clock Generation Register 1
RKDSM_DSM_I2S_XFER	0x011C	W	0x00000000	Transfer Start Register
RKDSM_DSM_I2S_CLR	0x0120	W	0x00000000	SCLK Domain Logic Clear Register
RKDSM_DSM_VERSION	0x0140	W	0x00000010	Version Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

26.4.3 Detail Registers Description

RKDSM_DSMVUCTL

Address: Operational Base(0xFF4B0000) + offset (0x0000)

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Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	dac_byps Digital DAC volume control bypass. 1'b0: Digital DAC volume control enable 1'b1: Digital DAC volume control bypass
1	RW	0x0	dacfade Digital DAC volume adjust mode. 1'b0: Update to new volume immediately. 1'b1: Update volume as daczdt field describes.
0	RW	0x1	daczdt Digital DAC volume cross zero detect enable. It works when dac_byps is 1'b0 and dacfade is 1'b1. 1'b0: Volume adjusts every sample. 1'b1: Volume adjusts only when audio waveform crosses zero or volume-control time-limit condition meets.

RKDSM_DSMVUCTIME

Address: Operational Base(0xFF4B0000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	dacvuct Volume control time limit, valid only in fade cross zero mode. Time limit = dacvuct*(1/sample rate) Unit: Sample rate

RKDSM_DSMDIGEN

Address: Operational Base(0xFF4B0000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	dacglben Global enable of all Digital DAC channels. Only when dacglben and the enable signal corresponding to each Digital DAC channel is valid before starting work. 1'b0: Disable 1'b1: Enable
3:1	RO	0x0	reserved
0	RW	0x0	dacen_l0r1 Digital DAC left channel 0 and right channel 1 enable. 1'b0: Disable 1'b1: Enable

RKDSM_DSMCLKCTRL

Address: Operational Base(0xFF4B0000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	dac_cke Digital DAC operation clock enable. 1'b0: Disable 1'b1: Enable
4	RW	0x0	i2srx_cke Clock enable of internal I2S RX channel. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3	RW	0x0	cke_bclkrx Clock enable of sclk_out_rx. 1'b0: Disable 1'b1: Enable
2	RW	0x0	dac_sync_ena Enable of the synchronization signal used internally generated by Digital DAC. 1'b0: Disable 1'b1: Enable
1	RO	0x0	dac_sync_status There is a counter to generate synchronization signal of Digital DAC. In order to ensure the integrity of synchronization signal, it is necessary to read back dac_sync_status to judge whether the counter stops working when dac_sync_ena is set from 1'b1 to 1'b0. If the signal is read back to 1'b0, it means that the counter stops working and the synchronization signal of Digital DAC is complete.
0	RW	0x0	dac_mod_attenu_en When enabled, the input of the Digital DAC modulator is attenuated by 6dB, and the output of the Digital DAC modulator is increased by 6dB. 1'b0: Disable 1'b1: Enable

RKDSM_DSMINTMOD_DIV

Address: Operational Base(0xFF4B0000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x07	int_div_con Integer clock divider to provide 6.144/5.644/4.096MHz sample clock for internal filters. Make sure that int_div_con is an odd number between 7(8 times division) and 15(16 times division).

RKDSM_DSMINTSCLK_DIV

Address: Operational Base(0xFF4B0000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x1f	sckrxdiv Integer clock divider to generate sclk_out_rx when I2S RX works in master mode. It is ignored when in slave mode. Sckrxdiv=((frequency of input operation clock)/(frequency of sclk_out_rx))-1. Sckrxdiv can be any value from 0 to 255.

RKDSM_DSM_DIV

Address: Operational Base(0xFF4B0000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x03	audio_dsm_div DSM mode division of Digital DAC's operation clock. The operation clock frequency of DSM module is equal to the input operation clock frequency of Digital DAC's divided by audio_dsm_div+1. It's recommended that audio_dsm_div is set 8'h3.

RKDSM_DSM_CTRL

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Address: Operational Base(0xFF4B0000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	dsm_mode_cke Clock enable of 1-bit DSM modulator 1'b0: Disable 1'b1: Enable
5:4	RW	0x0	dsm_mode Audio DSM mode selection 2'b01: Audio DSM mode 0. The input of 1-bit DSM modulator is from the last filter of Audio DAC. 2'b10: Audio DSM mode 1. The input of 1-bit DSM modulator is directly from output of I2S RX inside the ACDCDIG. Others: Reserved
3	RW	0x0	dsm_en 1-bit DSM modulator enable 1'b0: Disable 1'b1: Enable
2:0	RW	0x0	dith_sel Dith mode selection of 1-bit DSM modulator.

RKDSM_DSMCFG1

Address: Operational Base(0xFF4B0000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:2	RW	0x1	dacsrt Sample rates of Digital DAC when in audio DSM mode 0. This field is ignored when in audio DSM mode 1. 3'b000: 12kHz/11.024kHz/8kHz 3'b001: 24kHz/22.05kHz/16kHz 3'b010: 32kHz/48kHz/44.1kHz 3'b011: 96kHz/88.2kHz/64kHz 3'b100: 192kHz/176.4kHz/128kHz 3'b101~3'b111: Reserved
1:0	RO	0x0	reserved

RKDSM_DSMMUTE

Address: Operational Base(0xFF4B0000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	dacunmt 1'b0: DAC normal mode 1'b1: DAC unmute mode. In this mode, DAC volume control block will adjust volume to match the value in DACVOLL* and DACVOLR*.
0	RW	0x0	dacmt 1'b0: DAC normal mode 1'b1: DAC mute mode

RKDSM_DSMMUTEST

Address: Operational Base(0xFF4B0000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
4	RO	0x0	unmutest_l0r1 Unmute status for Digital DAC left channel 0 and right channel 1. When unmute is done, it indicates that internal volume is equal to the value programmed in DACVOLL* and DACVOLR*. 1'b0: Unmute not done 1'b1: Unmute done
3:1	RO	0x0	reserved
0	RO	0x0	mutest_l0r1 Mute status for Digital DAC left channel 0 and right channel 1. 1'b0: Not mute 1'b1: Mute

RKDSM_DSMVOLL0

Address: Operational Base(0xFF4B0000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	daclv0 Volume of Digital DAC left channel 0. 0db~-95.625db, 0.375db/step. 8'h0: 0db 8'h1: -0.375db 8'h2: -0.75db 8'h3: -1.125db ..... 8'hff: -95.625db

RKDSM_DSMVOLL1

Address: Operational Base(0xFF4B0000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	daclv1 Volume of Digital DAC left channel 1. 0db~-95.625db, 0.375db/step. 8'h0: 0db 8'h1: -0.375db 8'h2: -0.75db 8'h3: -1.125db ..... 8'hff: -95.625db

RKDSM_DSMVOLL2

Address: Operational Base(0xFF4B0000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	daclv2 Volume of Digital DAC left channel 2. 0db~-95.625db, 0.375db/step. 8'h0: 0db 8'h1: -0.375db 8'h2: -0.75db 8'h3: -1.125db ..... 8'hff: -95.625db

RKDSM_DSMVOLL3

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Address: Operational Base(0xFF4B0000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	daclv3 Volume of Digital DAC left channel 3. 0db~-95.625db, 0.375db/step. 8'h0: 0db 8'h1: -0.375db 8'h2: -0.75db 8'h3: -1.125db ..... 8'hff: -95.625db

RKDSM_DSMVOLR0

Address: Operational Base(0xFF4B0000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	dacrv0 Volume of Digital DAC right channel 0. 0db~-95.625db, 0.375db/step. 8'h0: 0db 8'h1: -0.375db 8'h2: -0.75db 8'h3: -1.125db ..... 8'hff: -95.625db

RKDSM_DSMVOLR1

Address: Operational Base(0xFF4B0000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	dacrv1 Volume of Digital DAC right channel 1. 0db~-95.625db, 0.375db/step. 8'h0: 0db 8'h1: -0.375db 8'h2: -0.75db 8'h3: -1.125db ..... 8'hff: -95.625db

RKDSM_DSMVOLR2

Address: Operational Base(0xFF4B0000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	dacrv2 Volume of Digital DAC right channel 2. 0db~-95.625db, 0.375db/step. 8'h0: 0db 8'h1: -0.375db 8'h2: -0.75db 8'h3: -1.125db ..... 8'hff: -95.625db

RKDSM_DSMVOLR3

Address: Operational Base(0xFF4B0000) + offset (0x006C)

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Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	dacrv3 Volume of Digital DAC right channel 3. 0db~-95.625db, 0.375db/step. 8'h0: 0db 8'h1: -0.375db 8'h2: -0.75db 8'h3: -1.125db ..... 8'hff: -95.625db

RKDSM_DSMVOGP

Address: Operational Base(0xFF4B0000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	volgpr1 Gain polarity for the volume of Digital DAC right channel 1. 1'b0: Negative gain 1'b1: Positive gain
0	RW	0x0	volgpl0 Gain polarity for the volume of Digital DAC left channel 0. 1'b0: Negative gain 1'b1: Positive gain

RKDSM_DSMRVOLL0

Address: Operational Base(0xFF4B0000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0xff	rvoll0 Internal real-time volume of Digital DAC left channel 0.

RKDSM_DSMRVOLL1

Address: Operational Base(0xFF4B0000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	rvoll1 Internal real-time volume of Digital DAC left channel 1.

RKDSM_DSMRVOLL2

Address: Operational Base(0xFF4B0000) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	rvoll2 Internal real-time volume of Digital DAC left channel 2.

RKDSM_DSMRVOLL3

Address: Operational Base(0xFF4B0000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	rvoll3 Internal real-time volume of Digital DAC left channel 3.

RKDSM_DSMRVOLR0

Address: Operational Base(0xFF4B0000) + offset (0x0084)

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Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0xff	rvolr0 Internal real-time volume of Digital DAC right channel 0.

RKDSM_DSMRVOLR1

Address: Operational Base(0xFF4B0000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	rvolr1 Internal real-time volume of Digital DAC right channel 1.

RKDSM_DSMRVOLR2

Address: Operational Base(0xFF4B0000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	rvolr2 Internal real-time volume of Digital DAC right channel 2.

RKDSM_DSMRVOLR3

Address: Operational Base(0xFF4B0000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	rvolr3 Internal real-time volume of Digital DAC right channel 3.

RKDSM_DSMLMT0

Address: Operational Base(0xFF4B0000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	limen LIMITER enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	limdct Limiter detect mode. 1'b0: (Left channel + right channel)/2 1'b0: Left channel or right channel independently

RKDSM_DSMLMT1

Address: Operational Base(0xFF4B0000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	atk_rate LIMITER attack rate=(power(2, atk_rate)*(8*clk)), clk is such as 4.096Mhz, 5.6448Mhz, 6.144Mhz.
3:0	RW	0x0	rls_rate LIMITER release rate=(power(2, rls_rate)*(8*clk)), clk is such as 4.096MHz, 5.6448MHz, 6.144MHz.

RKDSM_DSMLMT2

Address: Operational Base(0xFF4B0000) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
6:4	RW	0x0	max_lilmt The highest threshold of LIMITER. 3'b000~3'b100: 0db~-12db, 3db/step 3'b101~3'b111: -18db~-30db, 6db/step
3	RO	0x0	reserved
2:0	RW	0x0	min_lilmt The lowest threshold of LIMITER. 3'b000~3'b100: 0db~-12db, 3db/step 3'b101~3'b111: -18db~-30db, 6db/step

RKDSM_DSMMIXCTRLL

Address: Operational Base(0xFF4B0000) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	mixmode_l0 Digital DAC left channel 0 mixing mode. 2'b00: Left channel 2'b01: Right channel 2'b10~2'b11: (Left channel + right channel)/2

RKDSM_DSMMIXCTRLR

Address: Operational Base(0xFF4B0000) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	mixmode_r0 Digital DAC right channel 1 mixing mode. 2'b00: Left channel 2'b01: Right channel 2'b10~2'b11: (Left channel + right channel)/2

RKDSM_DSMHPF

Address: Operational Base(0xFF4B0000) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:4	RW	0x0	hpfcf High-pass filter control. 2'b00: 80Hz 2'b01: 100Hz 2'b10: 120Hz 2'b11: 140Hz
3:1	RO	0x0	reserved
0	RW	0x0	hpfen_l0r1 High-pass filter enable for left channel 0 and right channel 1. 1'b0: High-pass filter is disabled. 1'b1: High-pass filter is enabled.

RKDSM_DSM_I2S_RXCR0

Address: Operational Base(0xFF4B0000) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:6	RW	0x0	pbm PCM bus mode 2'b00: PCM no delay mode 2'b01: PCM delay 1 mode 2'b10: PCM delay 2 mode 2'b11: PCM delay 3 mode
5	RW	0x0	tfs Transfer format select 1'b0: I2S format 1'b1: PCM format
4:0	RW	0x0f	vdw Valid data width 5'b00000~5'b01110: Reserved 5'b01111: 16bit 5'b10000: 17bit 5'b10001: 18bit 5'b10010: 19bit ..... 5'b11100: 29bit 5'b11101: 30bit 5'b11110: 31bit 5'b11111: 32bit

RKDSM_DSM_I2S_RXCR1

Address: Operational Base(0xFF4B0000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RW	0x0	rcsr Channel select 2'b00: Two channel Others: Reserved
5	RO	0x0	reserved
4	RW	0x0	cex Exchange left channel and right channel in the every receive line. 1'b0: Not exchange 1'b1: Exchange
3	RO	0x0	reserved
2	RW	0x0	fbm First bit mode 1'b0: MSB 1'b1: LSB
1:0	RW	0x0	ibm I2S bus mode 2'b00: I2S normal 2'b01: I2S Left justified 2'b10: I2S Right justified 2'b11: Reserved

RKDSM_DSM_I2S_CKR0

Address: Operational Base(0xFF4B0000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	rsd I2S rx sclk divider for rx_lrck generator. 2'b00: 64 2'b01: 128 2'b10~2'b11: 256
1:0	RO	0x0	reserved

RKDSM_DSM_I2S_CKR1

Address: Operational Base(0xFF4B0000) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	mss Master/slave mode select 1'b0: Master mode(sclk output) 1'b1: Slave mode(sclk input)
2	RW	0x0	ckp Sclk polarity 1'b0: Sample data at posedge sclk and drive data at negedge sclk. 1'b1: Sample data at negedge sclk and drive data at posedge sclk.
1	RW	0x0	rlp 1'b0: Normal polarity (I2S normal: low for left channel, high for right channel I2S left/right just: high for left channel, low for right channel PCM start signal: high valid) 1'b1: Opposite polarity (I2S normal: high for left channel, low for right channel I2S left/right just: low for left channel, high for right channel PCM start signal: low valid)
0	RO	0x0	reserved

RKDSM_DSM_I2S_XFER

Address: Operational Base(0xFF4B0000) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	rxs 1'b0: Stop RX transfer 1'b1: Start RX transfer
0	RO	0x0	reserved

RKDSM_DSM_I2S_CLR

Address: Operational Base(0xFF4B0000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	rxc This is a self-cleared bit. Write 1'b1 to clear all receive logic. This bit can be set only when rxs is 1'b0. After writing rxc to 1'b1, wait until rxc become 1'b0 by polling rxc.
0	RO	0x0	reserved

RKDSM_DSM_VERSION

Address: Operational Base(0xFF4B0000) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RO	0x10	ver Version of DSM.

26.5 Interface Description

The I2S RX interface of Digital Audio Codec is connected to the TX interface of I2S2 when GRF_AUDIO_CON[15] is set to 1'b1.
When operating in audio DSM mode 0 or 1, Digital Audio Codec outputs two pairs of differential signals encoded in DSM format. The following table shows the RK DSM interface description for audio DSM mode.

Table 26-1 Audio DSM M0 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
AUDIO_DSM_L_P	O	SAI0_SDO0_M0/DSM_AUD_LP/GPIO7_A5	GPIO7A_IOMUX_SEL_1 [7:4]=4
AUDIO_DSM_L_N	O	SAI0_LRCK_M0/DSM_AUD_LN/PWM2_CH7_M1/GPIO7_A3	GPIO7A_IOMUX_SEL_0 [15:12]=4
AUDIO_DSM_R_P	O	SAI0_SDI1_M0/SAI0_SDO3_M0/PDM_SDI1_M0/DSM_AUD_RP/I2C1_SDA_M3/UART2_TX_M1/GPIO7_B1	GPIO7B_IOMUX_SEL_0 [7:4]=4
AUDIO_DSM_R_N	O	SAI0_SDI2_M0/SAI0_SDO2_M0/PDM_SDI2_M0/DSM_AUD_RN/I2C1_SCL_M3/UART2_RX_M1/GPIO7_B0	GPIO7B_IOMUX_SEL_0 [3:0]=4

26.6 Application Notes

26.6.1 Software Application Notes

Steps to configure Digital DAC to work in audio DSM mode 0 are as follows.
1. Program CRU in the SOC system to achieve the operation frequency of Digital DAC.
2. Program DSMINTMOD_DIV to 0x07.
3. Program DSMCLKCTRL to 0x3d.
4. Program DSMINTSCLK_DIV if Digital DAC I2S RX acts as master.
5. Program DSMDSM_CTRL to 0x58.
6. Program DSM_I2S_CKR0 and ACDCDIG_I2S_CKR1 to set I2S RX related registers.
7. Program DSM_I2S_CLR to clear RX logic.
8. Program DSM_I2S_RXCR0 and ACDCDIG_I2S_RXCR1.
9. Program GRF_AUDIO_CON[14] to 1'b1 and program registers of I2S1 that is connected to Digital Audio Codec. Don't start transfer at this time.
10. Program DAC related registers such as DSMHPF, DSMVUCTL and DSMCFG1 to achieve basic configuration.
11. Program ACDCDIG_I2S_XFER to start I2S RX.
12. Program registers of I2S1 outside Digital Audio Codec to start TX.
13. Program DSMDIGEN to enable digital DAC channels. From now on, the Digital Audio Codec begins to work.

Steps to configure Digital Audio Codec to end audio DSM mode 0 transfer are as follows.
1. Program registers of I2S1 to stop TX and ACDCDIG_I2S_XFER to stop RX.
2. Program DSMDSM_CTRL to 0x0.
3. Program DSMDIGEN to disable digital DAC channels.
4. Program DSMCLKCTRL to 0x0. Wait DSMCLKCTRL.dac_sync_status until read back to be 1'b0.

Steps to configure Digital DAC to work in audio DSM mode 1 are as follows.
1. Program CRU in the SOC system to achieve the operation frequency of Digital DAC.
2. Program DSMCLKCTRL to 0x3d.
3. Program DSMSCLKRXINT_DIV if Digital DAC I2S RX acts as master.
4. Program DSMDSM_CTRL to 0x68.
5. Program DSM_I2S_CKR0 and ACDCDIG_I2S_CKR1 to set I2S RX related registers.

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6. Program DSM_I2S_CLR to clear RX logic.
7. Program DSM_I2S_RXCR0 and ACDCDIG_I2S_RXCR1.
8. Program GRF_AUDIO_CON[14] to 1'b1 and program registers of I2S1 to start TX.
9. Program DSM_I2S_XFER to start I2S RX. From now on, the Digital Audio Codec begins to work.

Steps to configure Digital Audio Codec to end audio DSM mode 1 transfer are as follows.

1. Program registers of I2S1 to stop TX and DSM_I2S_XFER to stop RX.
2. Program DSMDSM_CTRL to 0x0.
3. Program DSMCLKCTRL to 0x0. Wait DSMCLKCTRL.dac_sync_status until read back to be 1'b0.

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Chapter 27 Audio Subsystem

27.1 Overview

The audio subsystem is dedicated for managing the audio resources of the whole chip. In RV1126B, the audio subsystem consists of two pieces: BUS_WRAPPER, and PMU_WRAPPER. With the audio subsystem, we can combine audio components and the embedded SOC platform together and provide an audio system solution.

27.2 Block Diagram

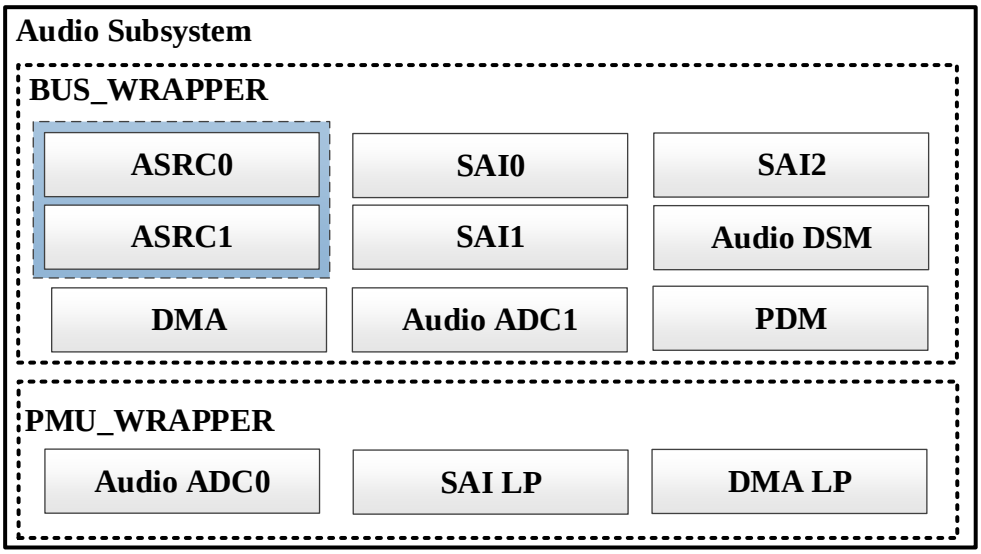

Fig. 27-1 Audio Subsystem Block Diagram

BUS Wrapper

BUS Wrapper consists of audio components shown as follow:

- One PDM
- One Audio DSM, which can be used to play audio data from SAI2
- One Audio ADC, which can be used to play audio data to SAI2
- One SAI0 (4 tx, 4 rx lanes)
- One SAI1 (1 tx, 1 rx lanes)
- One SAI2 (1 tx, 3 rx lanes)
- Two 2 channel ASRC0/1, which can be combined together.
- One DMA, which can be used to transmit audio data.

PMU Wrapper

PMU Wrapper consists of audio components shown as follow:

- One Audio ADC, which can be used to play audio data to SAI_LP or SAI2
- One SAI_LP
- One DMA_LP, which can be used to transmit audio data.

27.3 Function Description

In this chapter, we will only cover the interconnection of two audio components. For the detail of audio components, please refer to the following chapters: Audio DSM, Audio ADC, PDM, Serial Audio Interface (SAI) and Asynchronous Sample Rate Converter (ASRC).

27.3.1 ASRC Series Mode

In series mode, adjacent ASRCs in BUS wrapper can be combined together to enhance throughput. We can appoint the ASRC at the front as master and other ASRCs as slave. In RV1126B, ASRC0 as master and ASRC1 as slave when combined.

In series mode, all combined ASRCs can be viewed as a whole and interact with the outside world using the interface of master ASRC only. We can take MEM2MEM series mode in audio0 wrapper as an example in the following figure.

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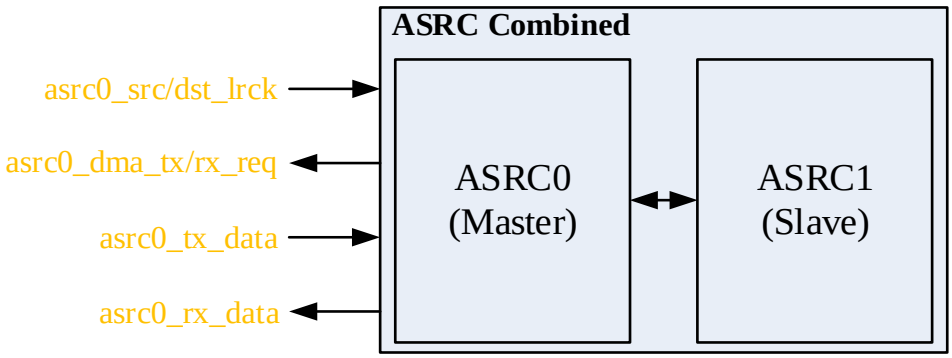

Fig. 27-2 ASRC MEM2MEM Series Mode Structure

In series mode of SAI and ASRC, only the clock source of master is used. Combined SAIs using their own DMA handshake interface and interrupt interface, but only the interface of master ASRC is used when combined.

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Chapter 28 Always-On Audio Subsystem

28.1 Overview

The always-on audio subsystem is dedicated for recording with low power consumption requirements, and in RV1126B, support abnormal sound detection in the subsystem. The always-on audio subsystem includes LPADC, LPSAI, LPDMA, Connect, FSPI1, AOA Controller and AOA Memory.

28.2 Block Diagram

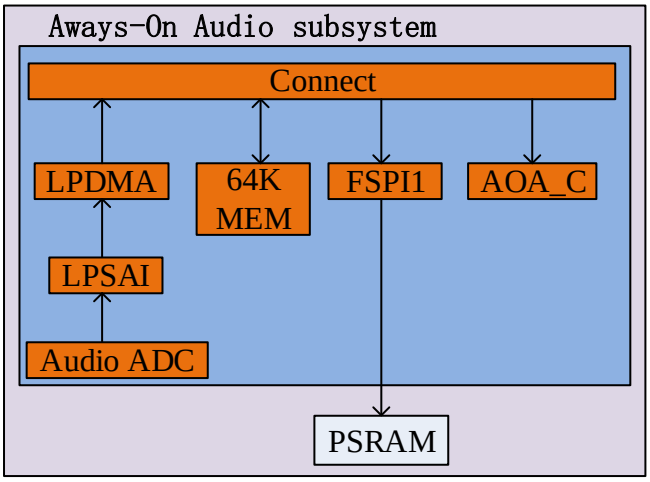

Fig. 28-1 Always-On Audio subsystem Block Diagram

The always-on audio subsystem consists of three parts, as follows:

- Audio input path, Audio ADC → LPSAI.
- Data store path, LPSAI → LPDMA → 64K MEM (and FSPI1 → PSRAM, if the external connected).
- Abnormal sound detection, 64K MEM → AOA_C, if it is necessary to wake up the system when an abnormal sound is detected.

28.3 Function Description

In this chapter, we mainly introduce the functions of AOA system data path. For the module level introduce, you can refer to the other chapters that specifically introduce those modules.

28.3.1 Data Path

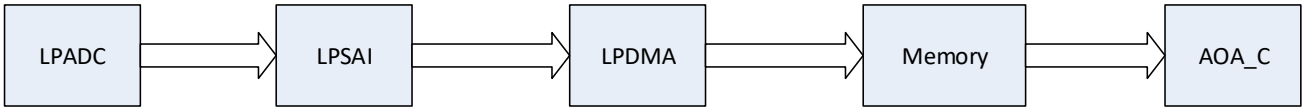

Fig. 28-2 AOA Abnormal Sound Detect Data Path

The Data flow is described as follows:

1. LPADC converts external sound into digital signals and sends to LPSAI
2. LPSAI organizes the audio data and sends requirement to LPDMA
3. LPDMA read data from LPSAI and write to Memory
4. When LPDMA completes one transfer, and gives the frame done to AOA Controller
5. AOA.ATD start work, if enable abnormal sound detect function

28.3.2 LPDMA

LPDMA receives software control and peripheral request signals to realize data transmission between LPSAI, 64K MEM, PMU MEM, FSPI1, and DDR.

28.3.2.1 Features

- Overall Features
  - Supports 4 logical channels, and 1 physical channel
  - Supports 1 group of peripheral request interface
  - Supports 32-bit address width, and 64-bit data width

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- Master Interface
- Configurable AXI burst size, maximum is 8 bytes
- Configurable AXI burst length, maximum is 16 beats

For other features, functions, registers and applications, please refer to "Chapter DMAC".

28.3.2.2 Peripheral Interconnection

Table 70-1 LPDMA Peripheral Interconnection

DMAC Channel	Peripheral	TX/RX/M	Support Single
0	DMA_PERI_LPSAI_RX	RX/M	N
1	RSV	M	N
2	RSV	M	N
3	RSV	M	N

*Notes: TX/RX/M: **TX**-Memory to Peripheral, **RX**-Peripheral to Memory, **M**-Memory to Memory*

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Chapter 29 AOA Controller

29.1 Overview

The AOA Controller is used to detect the abnormal sound, and generate IRQ to wake up system or other events. In the controller, ATD (Audio Time Detect) use the time domain audio data as initial detection part, and if the time audio data meet some conditions, then the AFE (Audio Feature Extract) and AAD (Audio AI Detect) will start working about 100 frames for AI detection, and during the AI detect period, the AAD will generate case interrupt when meet the setting conditions.
The main characteristics of AOA Controller are listed below:

- APB Slave interface with 32bit data bus width
- APB Master interface with 32bit data bus width
- AHB Master interface with 128bit data bus width
- Support Hardware mode
- Interrupts are separately software maskable
- Abnormal sound interrupt
- ATD start interrupt
- ATD done interrupt
- AAD done interrupt
- AAD debug enter interrupt

29.2 Block Diagram

AOA Controller comprises with:

- APB SLV: APB slave interface
- ATD: audio time detect part
- AFE: audio feature generate
- AAD: audio AI detect

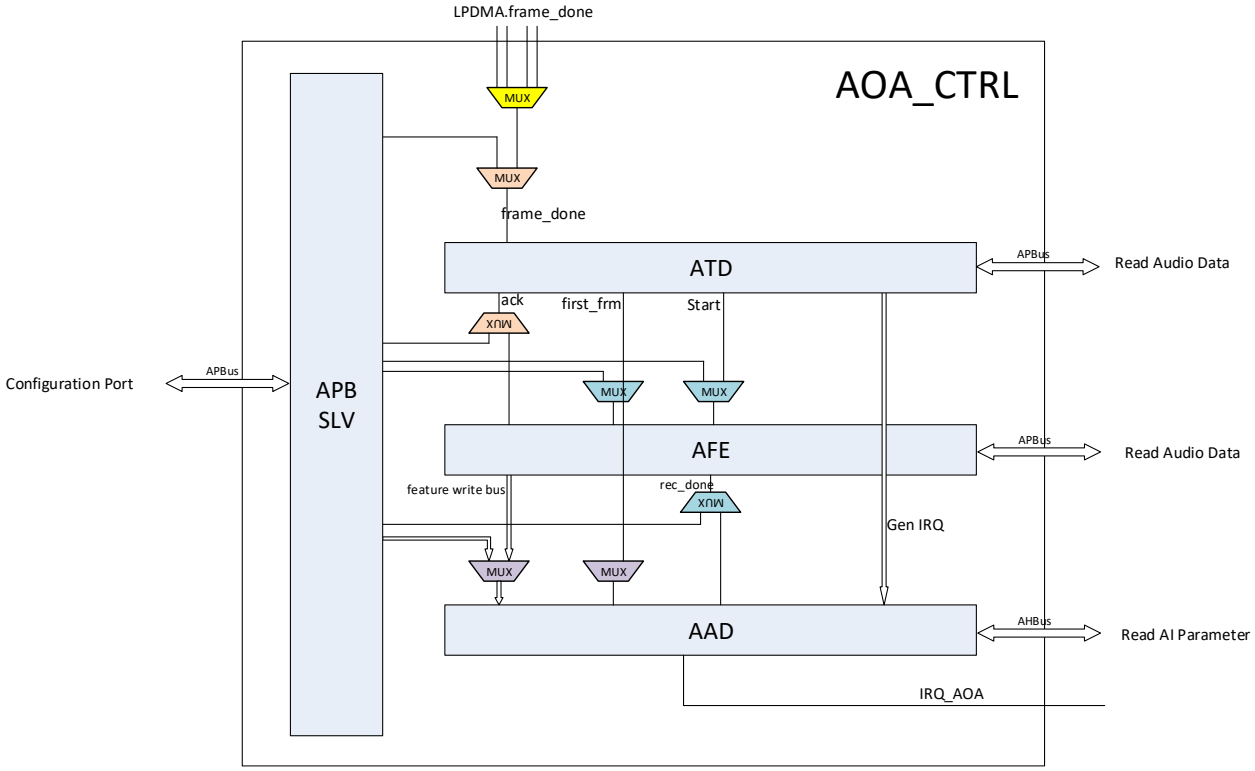

Fig. 29-1 AOA_CTRL Block Diagram

APB Slave interface:
The interface implements the APB slave operation. Data bus width use 32bit, and no ready signal.
APB Master interface in ATD:
The APB master used to fetch the audio data from audio mem for the time detection, only read function, and data width 32bit.

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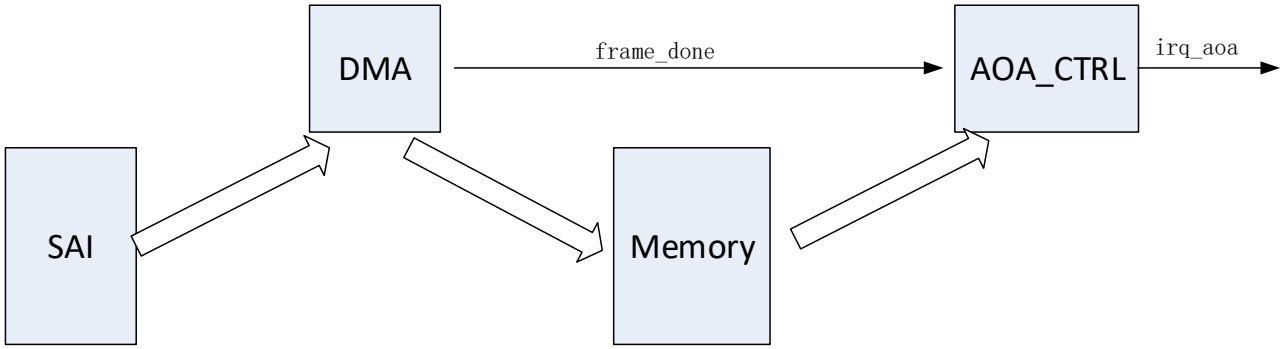
APB Master interface in AFE:
The APB master used to fetch the audio data from audio mem for the feature extract, only read function, and data width 32bit.
AHB Master interface in AAD:
The AHB Master used to fetch AI parameter for the detect, only read function, and data width 128bit.

29.3 Function Description

29.3.1 Data Path



The audio data flow is described as follows:
1. SAI receive audio data from the external environment
2. DMA read data from SAI and write them to Memory
3. When DMA completes one transfer, and give the frame to AOA
4. AOA.ATD start work

Note:
1. DMA one transfer need configure 512byte length
2. The space used to store the audio data must the Nx512Byte

29.3.2 Flow control Description

The ATD, AFE, AAD work about once every 16ms, as shown in the following figure.

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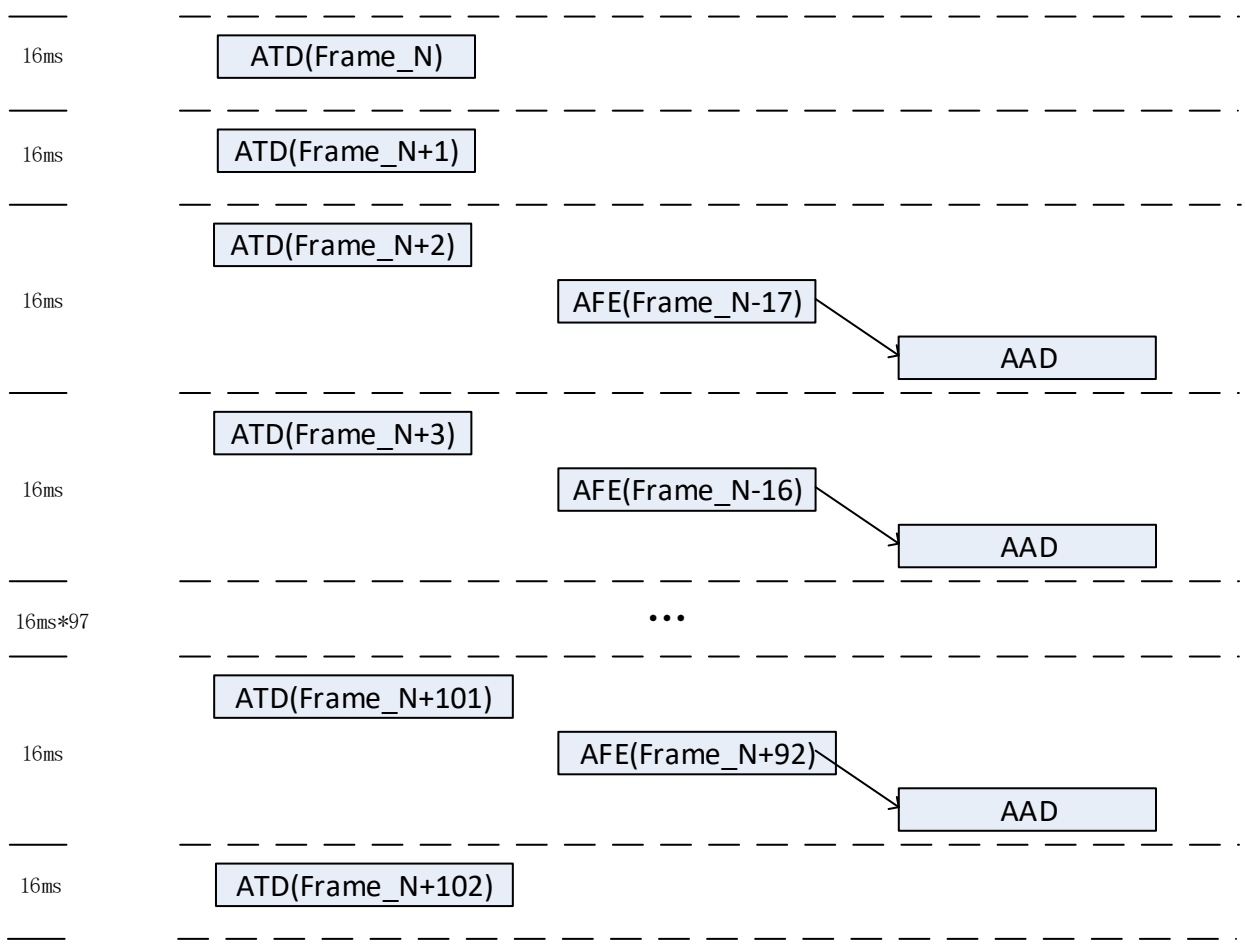

Fig. 29-2 AOA Controller Timing Step

The ATD start work after one frame audio data store done in the 64K memory.
The AFE start work after the ATD detect abnormal sound, and detect the data that 20 frames ahead of the current frame data, and once start, 100 rounds will be detected.
The AAD working start when AFE generate all the feature data done.

29.4 Register Description

29.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

29.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
AOA_CTRL_AUDIO_PARAM0	0x0000	W	0x00000000	Audio Data Param0
AOA_CTRL_AUDIO_PARAM1	0x0004	W	0x00000800	Audio Data Param1
AOA_CTRL_ATD_PARAM_CFG0	0x0010	W	0x00000000	ATD Param Config0
AOA_CTRL_ATD_PARAM_CFG1	0x0014	W	0x00000000	ATD Param Config1
AOA_CTRL_ATD_PARAM_CFG2	0x0018	W	0x00000000	ATD Param Config2
AOA_CTRL_ATD_PARAM_CFG3	0x001C	W	0x00000000	ATD Param Config3
AOA_CTRL_ATD_PARAM_CFG4	0x0020	W	0x00006401	ATD Param Config4
AOA_CTRL_ATD_CTRL	0x0024	W	0x00000000	ATD Control Registers
AOA_CTRL_AAD_FEATURE0	0x0100	W	0x00000000	AAD Feature data0
AOA_CTRL_AAD_FEATURE1	0x0104	W	0x00000000	AAD Feature data1
AOA_CTRL_AAD_FEATURE2	0x0108	W	0x00000000	AAD Feature data2
AOA_CTRL_AAD_FEATURE3	0x010C	W	0x00000000	AAD Feature data3
AOA_CTRL_AAD_FEATURE4	0x0110	W	0x00000000	AAD Feature data4
AOA_CTRL_AAD_FEATURE5	0x0114	W	0x00000000	AAD Feature data5
AOA_CTRL_AAD_FEATURE6	0x0118	W	0x00000000	AAD Feature data6

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Name	Offset	Size	Reset Value	Description
AOA_CTRL_AAD_FEATURE7	0x011C	W	0x00000000	AAD Feature data7
AOA_CTRL_AAD_FEATURE8	0x0120	W	0x00000000	AAD Feature data8
AOA_CTRL_AAD_FEATURE9	0x0124	W	0x00000000	AAD Feature data9
AOA_CTRL_AAD_FEATURE10	0x0128	W	0x00000000	AAD Feature data10
AOA_CTRL_AAD_FEATURE11	0x012C	W	0x00000000	AAD Feature data11
AOA_CTRL_AAD_FEATURE12	0x0130	W	0x00000000	AAD Feature data12
AOA_CTRL_AAD_FEATURE13	0x0134	W	0x00000000	AAD Feature data13
AOA_CTRL_AAD_FEATURE14	0x0138	W	0x00000000	AAD Feature data14
AOA_CTRL_AAD_FEATURE15	0x013C	W	0x00000000	AAD Feature data15
AOA_CTRL_AAD_FEATURE16	0x0140	W	0x00000000	AAD Feature data16
AOA_CTRL_AAD_FEATURE17	0x0144	W	0x00000000	AAD Feature data17
AOA_CTRL_AAD_FEATURE18	0x0148	W	0x00000000	AAD Feature data18
AOA_CTRL_AAD_FEATURE19	0x014C	W	0x00000000	AAD Feature data19
AOA_CTRL_AAD_FEATURE20	0x0150	W	0x00000000	AAD Feature data20
AOA_CTRL_AAD_FEATURE21	0x0154	W	0x00000000	AAD Feature data21
AOA_CTRL_AAD_FEATURE22	0x0158	W	0x00000000	AAD Feature data22
AOA_CTRL_AAD_FEATURE23	0x015C	W	0x00000000	AAD Feature data23
AOA_CTRL_AAD_FEATURE24	0x0160	W	0x00000000	AAD Feature data24
AOA_CTRL_AAD_FEATURE25	0x0164	W	0x00000000	AAD Feature data25
AOA_CTRL_AAD_FEATURE26	0x0168	W	0x00000000	AAD Feature data26
AOA_CTRL_AAD_FEATURE27	0x016C	W	0x00000000	AAD Feature data27
AOA_CTRL_AAD_FEATURE28	0x0170	W	0x00000000	AAD Feature data28
AOA_CTRL_AAD_FEATURE29	0x0174	W	0x00000000	AAD Feature data29
AOA_CTRL_AAD_FEATURE30	0x0178	W	0x00000000	AAD Feature data30
AOA_CTRL_AAD_FEATURE31	0x017C	W	0x00000000	AAD Feature data31
AOA_CTRL_AAD_FEATURE32	0x0180	W	0x00000000	AAD Feature data32
AOA_CTRL_AAD_FEATURE33	0x0184	W	0x00000000	AAD Feature data33
AOA_CTRL_AAD_FEATURE34	0x0188	W	0x00000000	AAD Feature data34
AOA_CTRL_AAD_FEATURE35	0x018C	W	0x00000000	AAD Feature data35
AOA_CTRL_AAD_FEATURE36	0x0190	W	0x00000000	AAD Feature data36
AOA_CTRL_AAD_FEATURE37	0x0194	W	0x00000000	AAD Feature data37
AOA_CTRL_AAD_FEATURE38	0x0198	W	0x00000000	AAD Feature data38
AOA_CTRL_AAD_FEATURE39	0x019C	W	0x00000000	AAD Feature data39
AOA_CTRL_AAD_CTRL	0x01A0	W	0x00000000	AAD Control Registers
AOA_CTRL_AAD_DEBUG_CTRL	0x01A4	W	0x00000000	AAD Debug Control Registers
AOA_CTRL_AAD_IRQ_ST	0x01A8	W	0x00000000	AAD IRQ Status
AOA_CTRL_AAD_IRQ_OUT_EN	0x01AC	W	0x00000000	AAD IRQ Output Enable
AOA_CTRL_AAD_STATUS0	0x01B0	W	0x00000000	AAD Status0 Registers0
AOA_CTRL_AAD_STATUS1	0x01B4	W	0x00000000	AAD Status0 Registers1
AOA_CTRL_AAD_PARAM0	0x01B8	W	0x00000000	AAD Param Config0
AOA_CTRL_AAD_PARAM1	0x01BC	W	0x00000317	AAD Param Config1
AOA_CTRL_AFE_CTL0	0x0200	W	0x00000000	AFE Control Register0
AOA_CTRL_AFE_CTL1	0x0204	W	0x00000000	AFE Control Register1
AOA_CTRL_AFE_CFG0	0x0210	W	0x00004083	AFE Configuration Register0
AOA_CTRL_AFE_CFG1	0x0214	W	0x00000040	AFE Configuration Register0
AOA_CTRL_AFE_DBG_MEMADDR	0x0240	W	0x00000000	AFE Debug Memory Read Control Register
AOA_CTRL_AFE DBG_MEMDATA	0x0244	W	0x00000000	AFE Debug Memory Read Data Register
AOA_CTRL_AFE_DBGSM	0x0250	W	0x00000000	AFE Debug State Machine Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

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29.4.3 Detail Registers Description

AOA_CTRL_AUDIO_PARAM0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	atd_audio_start_addr audio data store base address

AOA_CTRL_AUDIO_PARAM1

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0800	atd_audio_space audio data space, Unit: Byte

AOA_CTRL_ATD_PARAM_CFG0

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	pcm_buff_size pcm buff size
23:16	RW	0x00	frm_ratio_th frm ratio th
15:8	RW	0x00	frm_alpha frm alpha
7:4	RW	0x0	param_qp QP
3:0	RW	0x0	src_shift src_shift = 16-PCM_BIT

AOA_CTRL_ATD_PARAM_CFG1

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	den den
15:0	RW	0x0000	radius radius

AOA_CTRL_ATD_PARAM_CFG2

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	abs_frm_sm_init abs_frm_sm = abs_frm_sm_init * 256

AOA_CTRL_ATD_PARAM_CFG3

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	abs_frm_th abs_frm_th

AOA_CTRL_ATD_PARAM_CFG4

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
17:8	RW	0x064	flag_loop flag loop
7:0	RW	0x01	flag_cnt_th flag_cnt_th

AOA_CTRL_ATD_CTRL

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	sw_ai_start_ack ai start ack software source, write 1 and self auto clear
5	RW	0x0	sw_frame_done frame done software source, write 1 and self auto clear
4	RW	0x0	sw_ctrl_atd Control frame_done and ai_start_ack select hardware or software as audio time detect trigger source. 1'b0: select hardware 1'b1: select software
3:1	RO	0x0	reserved
0	RW	0x0	time_det_en time detect enable bit, high active

AOA_CTRL_AAD_FEATURE0

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data0 feature data0

AOA_CTRL_AAD_FEATURE1

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data1 feature data1

AOA_CTRL_AAD_FEATURE2

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data2 feature data2

AOA_CTRL_AAD_FEATURE3

Address: Operational Base + offset (0x010C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data3 feature data3

AOA_CTRL_AAD_FEATURE4

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	feature_data4 feature data4

AOA_CTRL_AAD_FEATURE5

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data5 feature data5

AOA_CTRL_AAD_FEATURE6

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data6 feature data6

AOA_CTRL_AAD_FEATURE7

Address: Operational Base + offset (0x011C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data7 feature data7

AOA_CTRL_AAD_FEATURE8

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data8 feature data8

AOA_CTRL_AAD_FEATURE9

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data9 feature data9

AOA_CTRL_AAD_FEATURE10

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data10 feature data10

AOA_CTRL_AAD_FEATURE11

Address: Operational Base + offset (0x012C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data11 feature data11

AOA_CTRL_AAD_FEATURE12

Address: Operational Base + offset (0x0130)

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Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data12 feature data12

AOA_CTRL_AAD_FEATURE13

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data13 feature data13

AOA_CTRL_AAD_FEATURE14

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data14 feature data14

AOA_CTRL_AAD_FEATURE15

Address: Operational Base + offset (0x013C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data15 feature data15

AOA_CTRL_AAD_FEATURE16

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data16 feature data16

AOA_CTRL_AAD_FEATURE17

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data17 feature data17

AOA_CTRL_AAD_FEATURE18

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data18 feature data18

AOA_CTRL_AAD_FEATURE19

Address: Operational Base + offset (0x014C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data19 feature data19

AOA_CTRL_AAD_FEATURE20

Address: Operational Base + offset (0x0150)

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Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data20 feature data20

AOA_CTRL_AAD_FEATURE21

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data21 feature data21

AOA_CTRL_AAD_FEATURE22

Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data22 feature data22

AOA_CTRL_AAD_FEATURE23

Address: Operational Base + offset (0x015C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data23 feature data23

AOA_CTRL_AAD_FEATURE24

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data24 feature data24

AOA_CTRL_AAD_FEATURE25

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data25 feature data25

AOA_CTRL_AAD_FEATURE26

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data26 feature data26

AOA_CTRL_AAD_FEATURE27

Address: Operational Base + offset (0x016C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data27 feature data27

AOA_CTRL_AAD_FEATURE28

Address: Operational Base + offset (0x0170)

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Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data28 feature data28

AOA_CTRL_AAD_FEATURE29

Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data29 feature data29

AOA_CTRL_AAD_FEATURE30

Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data30 feature data30

AOA_CTRL_AAD_FEATURE31

Address: Operational Base + offset (0x017C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data31 feature data31

AOA_CTRL_AAD_FEATURE32

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data32 feature data32

AOA_CTRL_AAD_FEATURE33

Address: Operational Base + offset (0x0184)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data33 feature data33

AOA_CTRL_AAD_FEATURE34

Address: Operational Base + offset (0x0188)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data34 feature data34

AOA_CTRL_AAD_FEATURE35

Address: Operational Base + offset (0x018C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data35 feature data35

AOA_CTRL_AAD_FEATURE36

Address: Operational Base + offset (0x0190)

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Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data36 feature data36

AOA_CTRL_AAD_FEATURE37

Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data37 feature data37

AOA_CTRL_AAD_FEATURE38

Address: Operational Base + offset (0x0198)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data38 feature data38

AOA_CTRL_AAD_FEATURE39

Address: Operational Base + offset (0x019C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	feature_data39 feature data39

AOA_CTRL_AAD_CTRL

Address: Operational Base + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	sw_first_frm first frm software source, write 1 and self auto clear
4	RW	0x0	sw_ctrl_aad Control feature data and first frm select hardware or software as audio ai detect trigger source. 1'b0: select hardware 1'b1: select software
3:1	RO	0x0	reserved
0	RW	0x0	aad_en aad enable bit, high active

AOA_CTRL_AAD_DEBUG_CTRL

Address: Operational Base + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:8	RW	0x00	aad_debug_mem_addr internal mem addr space: 0~199 when addr <= 200, means select the debug group, and the module debug signal select as follow: addr[2:0] == 3'h4: step_debug_signal addr[2:0] == 3'h5: conv_debug_signal addr[2:0] == 3'h6: gru_debug_signal addr[2:0] == 3'h7: fc_debug_signal
7:4	RW	0x0	aad_debug_32bit_sel select 32bit location in 320bit
3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2	RW	0x0	aad_debug_mem_rd memory read, write 1 and self auto clear
1	RW	0x0	aad_debug_next_step debug next step, write 1 and self auto clear
0	RW	0x0	aad_debug_en aad debug enable, high active

AOA_CTRL_AAD_IRQ_ST

Address: Operational Base + offset (0x01A8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	W1C	0x0000	irq_st bit7~bit0: AAD model case7~case0 irq bit8: ATD first frm irq bit9: AAD start irq bit10: feature data0 irq bit11: feature data39 irq bit12: debug status enter irq bit13: AAD done irq bit14: ATD done irq bit15: Reserved

AOA_CTRL_AAD_IRQ_OUT_EN

Address: Operational Base + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	irq_output_en irq output enable bit, high active bit7~bit0: ai model case7~case0 irq output enable bit8: ai first frm irq output enable bit9: ai start irq output enable bit10: feature data0 irq output enable bit11: feature data39 irq output enable bit12: debug status enter irq output enable bit13: aad done irq output enable bit14: atd done irq output enable bit15: Reserved

AOA_CTRL_AAD_STATUS0

Address: Operational Base + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RO	0x0	feature_rec_done feature data recieve done flag
1	RO	0x0	aad_debug_st aad in debug status, high active
0	RO	0x0	aad_idle aad idle status, high active

AOA_CTRL_AAD_STATUS1

Address: Operational Base + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	aad_debug_data aad debug data

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AOA_CTRL_AAD_PARAM0

Address: Operational Base + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	aad_param_ba aad parameter store base address

AOA_CTRL_AAD_PARAM1

Address: Operational Base + offset (0x01BC)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x317	aad_param_num aad parameter num. unit: 128bit

AOA_CTRL_AFE_CTL0

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	MEM_DYNEN Memory Dynamic Clock Enable Values: 1'b0: AFE memory clock is in free-running state 1'b1: AFE memory clock is in dynamic-gate state
8	RW	0x0	FUNC_DYNEN Function Dynamic Clock Enable Values: 1'b0: AFE function clock is in free-running state 1'b1: AFE function clock is in dynamic-gate state
7:6	RW	0x0	DBG_MEM_SEL Debug Memory Select Values: 2'h0: Select none 2'h1: Select MEM_WINBUF, size=768X24 2'h2: Select MEM_FREQDATA, size=514X18 2'h3: Select MEM_MEL, size=40X16
5	RW	0x0	DBG_MEM_EN Debug Memory Enable When in debug memory mode, software can read AFE internal memory. Values: 1'b0: AFE is in normal memory mode 1'b1: AFE is in debug memory mode
4	RW	0x0	DBG_RUN_EN AFE Debug Run Mode Enable When in debug run mode, AFE will go into idle state after current frame finished, and AFE_START will be self-cleared. AFE will process next frame until software sets AFE_START=1. Values: 1'b0: AFE is in normal run mode 1'b1: AFE is in debug run mode
3:1	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	AFE_START AFE Start Request When in normal run mode, this bit is not self-cleared when in debug run mode, this bit is self-cleared after current frame finished Values: 1'b0: AFE is in idle state 1'b1: AFE is in working state

AOA_CTRL_AFE_CTL1

Address: Operational Base + offset (0x0204)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	RSV reserved

AOA_CTRL_AFE_CFG0

Address: Operational Base + offset (0x0210)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15	RO	0x0	reserved
14:10	RW	0x10	WAVE_BITS AFE Input PCM Wave Amplitude(FTR_WAV_BIT) Amplitude = -2^(FTR_WAV_BIT-1) --- 2^(FTR_WAV_BIT-1)-1
9	RO	0x0	reserved
8:4	RW	0x08	BANK_SHIFT FTR_Q_BankW This field controls the SHR shift size for st->melout to outmel. outmel = st->melout >>FTR_Q_BankW
3:0	RW	0x3	QLOG2NUM This field controls the feature result precision(FTR_Q_Log2) to AAD, default 1/8 Values: 4'h1: Precision is 1/2 4'h2: Precision is 1/4 4'h3: Precision is 1/8 4'h4: Precision is 1/16 4'h5: Precision is 1/32 4'h6: Precision is 1/64 4'h7: Precision is 1/128 4'h8: Precision is 1/256 Other values not supported

AOA_CTRL_AFE_CFG1

Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0040	GAIN_VAL AFE PCM Input Gain Control This field is 16Q6 format, default value is 1.0

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AOA_CTRL_AFE_DBG_MEMADDR

Address: Operational Base + offset (0x0240)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual 1'b0: Write access disable 1'b1: Write access enable
15	RW	0x0	MEM_RD Memory Read Strobe This bit is self-cleared after 1T.
14:10	RO	0x00	reserved
9:0	RW	0x000	MEM_RADDR Memory Read Address

AOA_CTRL_AFE DBG_MEMDATA

Address: Operational Base + offset (0x0244)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	MEM_RDATA Memory Read Data This field is 32-bit signed int number.

AOA_CTRL_AFE_DBGSM

Address: Operational Base + offset (0x0250)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RO	0x0	CORE_CS CORE_CS Status Values: 4'h0: CORE_IDLE 4'h1: CORE_EMPH 4'h2: CORE_MOVSAVE 4'h3: CORE_WIN 4'h4: CORE_SHF 4'h5: CORE_RNG_MAX 4'h6: CORE_FLY 4'h7: CORE_FREQ 4'h8: CORE_RNG_NMO 4'h9: CORE_MOVBACK 4'ha: CORE_MEL 4'hb: CORE_DONE
3:0	RO	0x0	AFE_CS AFE_CS status Values: 4'h0: AFE_IDLE 4'h1: AFE_TDWAIT 4'h2: AFE_TDACK 4'h3: AFE_BUSR 4'h4: AFE_CORE 4'h5: AFE_MELWAIT 4'h6: AFE_MELOUT 4'h7: AFE_DONE

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29.5 Application Notes

29.5.1 Hardware Mode

1. Initial AAD AI Parameter in the memory
2. Configure the Audio base address (Rx00) and space (Rx04);
3. Configure the ATD parameter (Rx10~Rx20);
4. Configure the AAD AI parameter base address (Rx1b0) and length (Rx1b4);
5. Enable IRQ output enable (Rx1ac);
6. Configure the AFE parameter (Rx210, Rx214);
7. Enable ATD(Rx24[0]) & AFE(Rx200[0]) & AAD(Rx1a0[1]);

29.5.2 Software Mode

1. Initial AAD AI Parameter in the memory
2. Configure the Audio base address (Rx00) and space (Rx04);
3. Configure the ATD parameter (Rx10~Rx20);
4. Configure the AAD AI parameter base address (Rx1b0) and length (Rx1b4);
5. Configure the AFE parameter (Rx210, Rx214);
6. Configure the AFE into debug run mode(Rx210[4]);
7. Enable IRQ output enable (Rx1ac), software mode need enable ATD done and AAD done interrupt output.
8. Start ATD(Rx24[0]) & AAD(Rx1a0[1]) and sw_ctrl_atd(Rx24[4]) and sw_ctrl_aad(Rx1a0[4]);

========== ATD Part ==========

9. Write 1 frame audio data in Memory, use LPDMA or MCU write;
10. Set sw_frame_done(Rx24[5]);
11. Wait AOA IRQ active;
12. Read AOA IRQ Status and check bit8 and bit9;
13. Clear IRQ status;
14. Set sw_ai_start_ack(Rx24[6]);
15. If IRQ status bit9 active, need start AFE and AAD, if bit9==0, jump to step7;

========== AFE Part ==========

16. Start AFE for current frame process (Rx210[0]); After current frame finished, this bit will be self-cleared.

========== AAD Part ==========

17. Set sw_first_frm(Rx1a0[5]) if IRQ status bit8 active;
18. Write Feature data to AOA by MCU(Rx100~Rx19c);
19. Wait AAD done interrupt;
20. Read AOA IRQ status;
21. Clear IRQ status;
22. If IRQ status bit7~bit0 != 8'h0, wakeup system, else jump to step7.

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Chapter 30 Serial Audio Interface (SAI)

30.1 Overview

The SAI controller is designed for interfacing between the AHB bus and the serial audio interface bus. The SAI is a serial link for digital audio data transfer between devices in the system. The SAI interface (Serial Audio Interface) offers a wide set of audio protocols due to its flexibility and wide range of configurations. Many stereo or mono audio applications may be targeted. I2S standards, PCM, and TDM may be addressed.
SAI is widely used in the devices such as ADC, DAC, DSP, CPU, etc. With the SAI interface, we can connect audio devices and the embedded SoC platform together and provide an audio interface solution for the system.

30.1.1 Features

- Support eight internal 32-bit wide and 32-location deep FIFOs, four for transmitting and the other for receiving audio data
- Support AHB bus interface
- Support 8 ~ 32 bits audio data transfer
- Support master and slave mode
- Support DMA handshaking interface and configurable DMA water level
- Support transmit FIFO empty, underflow, receive FIFO full, overflow interrupt and all interrupts can be masked
- Support configurable water level of transmit FIFO empty and receive FIFO full interrupt
- Support combined interrupt output
- Support 8 to 32 bit audio data left or right justified in 32-bit wide FIFO
- Support two 16-bit audio data store together in one 32-bit wide location and support four 8-bit audio data store together in one 32-bit wide location
- Support TX to RX loopback bypass mode
- Support audio protocol: I2S, PCM, TDM
- Support Number of bits by frame can be configurable
- Support First active slot position in the frame is configurable
- Support up to 128 slots available with configurable size
- Support slot length 8 to 32 bits configurable
- Support slot valid data length 8 to 32 bits configurable
- Support Mono audio mode
- Support slot mask configurable
- Support First active bit position in the slot is configurable
- Support MSB or LSB first serial audio data transfer
- Support configurable SCLK and FS polarity
- Support up to four lanes parallel transceivers
- Support SDI,SDO IOMUX

30.2 Block Diagram

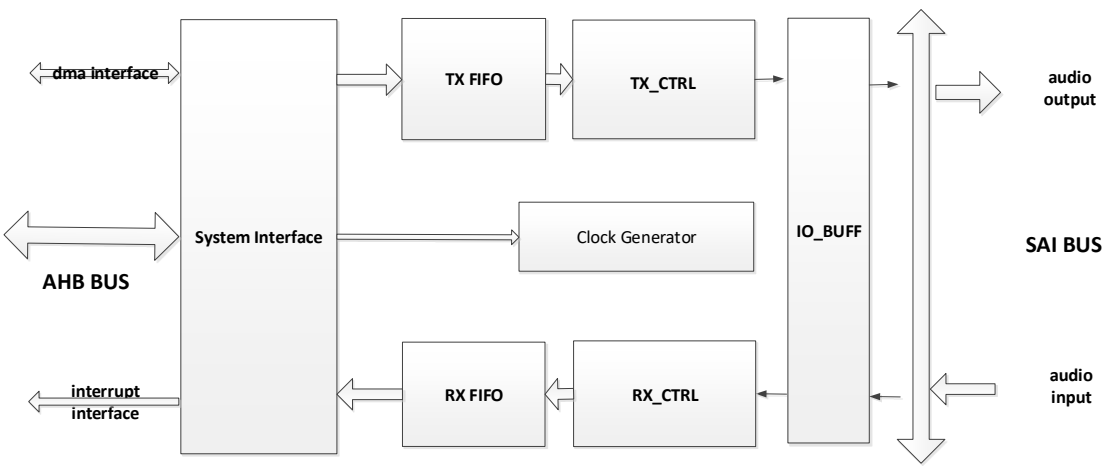

Fig. 30-1 SAI Block Diagram

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System Interface
The system interface implements the AHB slave operation. It contains not only control registers of transmitters and receiver inside but also interrupt and DMA handshaking interface.
Clock Generator
The Clock Generator implements clock generation function. The input source clock to the module is MCLK_SAI, and by the divider of the module, the clock generator generates SCLK and FS to transmitter and receiver.
Transmitters
The Transmitters implement transmission operation. The transmitters can act as either a master or a slave, with I2S, PCM or TDM mode surround serial audio interface.
Receiver
The Receiver implements receive operation. The receiver can act as either a master or a slave, with I2S, PCM or TDM mode stereo serial audio interface.
Transmit FIFO
The Transmit FIFO is the buffer to store transmitted audio data. The size of the FIFO is 32bits x 32.
Receive FIFO
The Receive FIFO is the buffer to store received audio data. The size of the FIFO is 32bits x 32.
IO_BUFF
SDO, SDI, LRCK_IN and LRCK_OUT Register output.

30.3 Function Description

In the SAI controller, there are two types: transmitter-master & receiver-master; transmitter-slave & receiver-slave.
In broadcasting application, the SAI controller is used as a transmitter and external or internal audio CODEC is used as a receiver. In recording application, the SAI controller is used as a receiver and external or internal audio CODEC is used as a transmitter. Either the SAI controller or the audio CODEC can act as a master or a slave, but if one is master, the other must be slave.

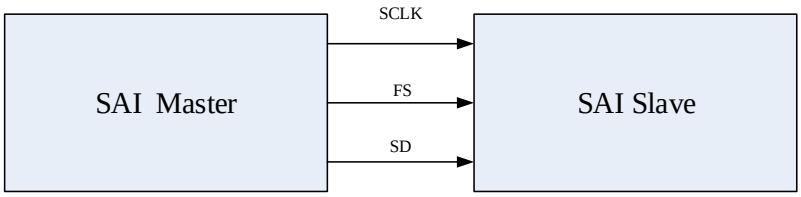

Fig.30-2 SAI transmitter-master & receiver-slave condition

When the transmitter acts as a master, it sends all signals to the receiver (the slave), and CPU controls when to send clock and data to the receiver. When acts as a slave, SD signal still goes from transmitter to receiver, but SCLK and FS signals are from the receiver (the master) to the transmitter. Based on three interface specifications, transmitting data should be ready before transmitter receives SCLK and FS signals. CPU should know when the receiver to initialize a transaction and when the transmitter to send data.
When the receiver acts as a master, it sends SCLK and FS signals to the transmitter (the slave) and receives serial data. So CPU must tell the transmitter when to start a transaction for it to prepare transmitting data then start a transfer and send clock and channel-select signals. When the receiver acts as a slave, CPU should only do initial setting and wait for all signals and then start reading data.
Before transmitting or receiving data, CPU need do initial setting to the SAI register. These includes CPU settings, SAI interface registers settings, and maybe the embedded SoC platform settings. These registers must be set before starting data transfer.
The SAI interface offers a wide set of audio protocols due to its flexibility and wide range of configurations.It can support I2S/PCM/TDM aduio protocol by different configuration.

30.3.1 I2S normal mode

This is the waveform of I2S normal mode. For FS (sai_fs_rx/sai_fs_tx) signal, it goes low

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to indicate left channel and high to right channel. For SD (sai_sdo, sai_sdi) signal, it starts sending the first bit (MSB or LSB) one SCLK clock cycle after FS changes. The range of SD signal width is from 8 to 32bits.

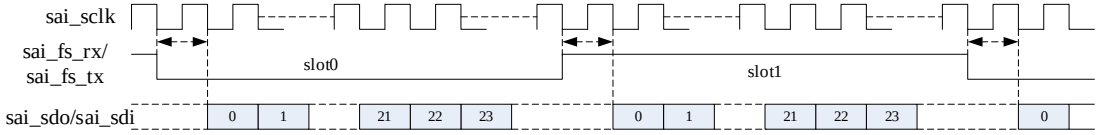

Fig.30-3 I2S Normal Mode Timing Format

30.3.2 I2S left justified mode

This is the waveform of I2S left justified mode. For FS (sai_fs_rx / sai_fs_tx) signal, it goes high to indicate left channel and low to right channel. For SD (sai_sdo, sai_sdi) signal, it starts sending the first bit (MSB or LSB) at the same time when FS changes. The range of SD signal width is from 8 to 32bits.

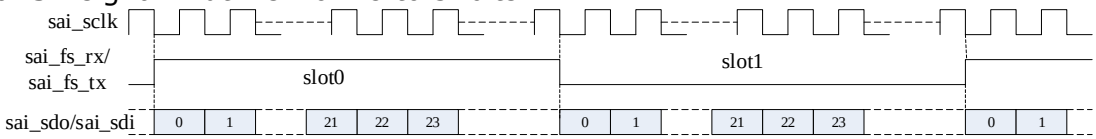

Fig.30-4 I2S Left Justified Mode Timing Format

30.3.3 I2S right justified mode

This is the waveform of I2S right justified mode. For FS (sai_fs_rx / sai_fs_tx) signal, it goes high to indicate left channel and low to right channel. For SD (sai_sdo, sai_sdi) signal, it transfers MSB or LSB first; but what is different from I2S normal or left justified mode, the last bit of the transferred data is aligned to the transition edge of the FS signal while one bit is transferred at one SCLK cycle. The range of SD signal width is from 8 to 32bits.

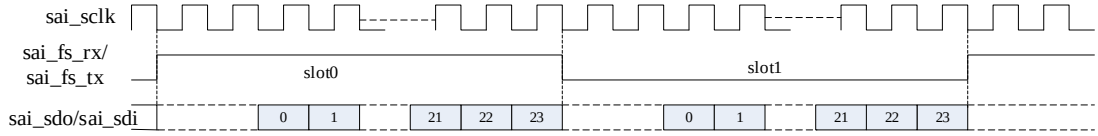

Fig.30-5 I2S Right Justified Mode Timing Format

30.3.4 PCM early mode

This is the waveform of PCM early mode. For FS (sai_fs_rx / sai_fs_tx) signal, it goes high to indicate the start of a group of audio channels. For SD (sai_sdo, sai_sdi) signal, it sends the first bit (MSB or LSB) at the same time when FS goes high. The range of SD signal width is from 8 to 32bits.

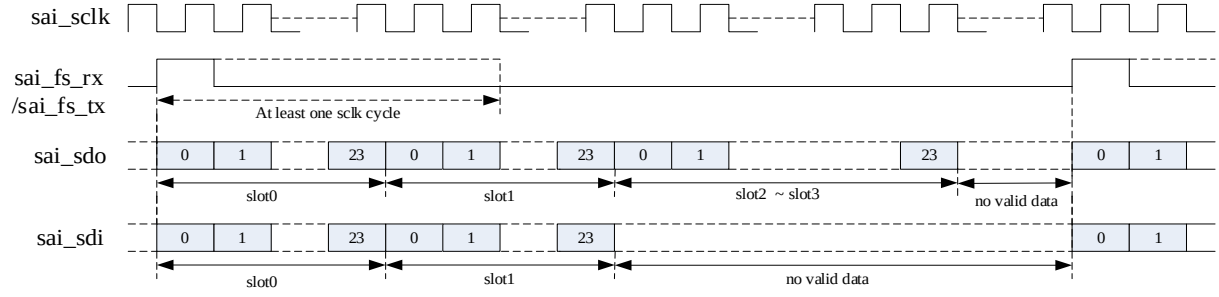

Fig.30-6 PCM Early Mode Timing Format

30.3.5 Flexibility and wide range of configurations

The SAI interface (Serial Audio Interface) offers a wide set of audio protocols due to its flexibility and wide range of configurations.Many stereo or mono audio applications may be targeted. I2S standards, PCM, and TDM may be addressed.

This is the waveform of PCM mode(SBW==VDW,FW >=SBW *SNB). For FS (sai_fs_rx / sai_fs_tx) signal, it goes high to indicate the start of a group of audio data.

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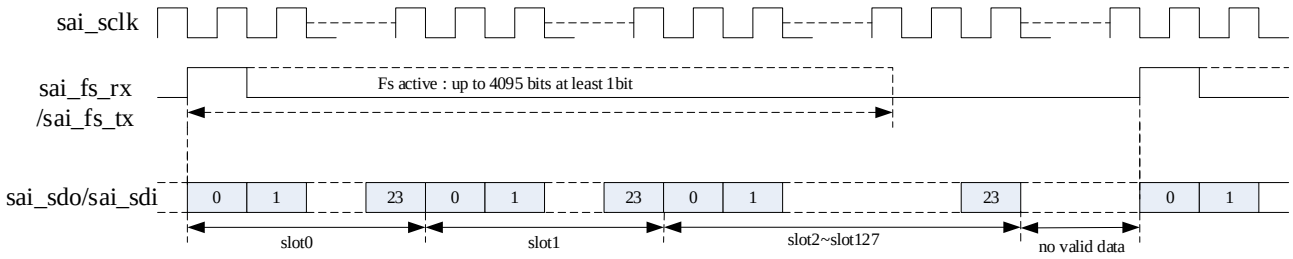

Fig.30-7 SAI PCM mode timing format

This is the waveform of I2S left mode(SBW>=VDW,FW >=SBW *SNB,VDJ==1'b1).

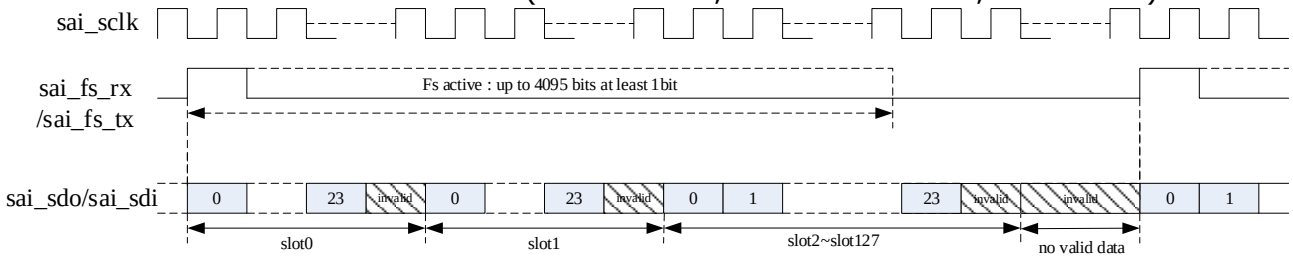

Fig.30-8 SAI I2S left mode timing format

This is the waveform of I2S right mode(SBW>=VDW,FW >=SBW *SNB,VDJ==1'b0).

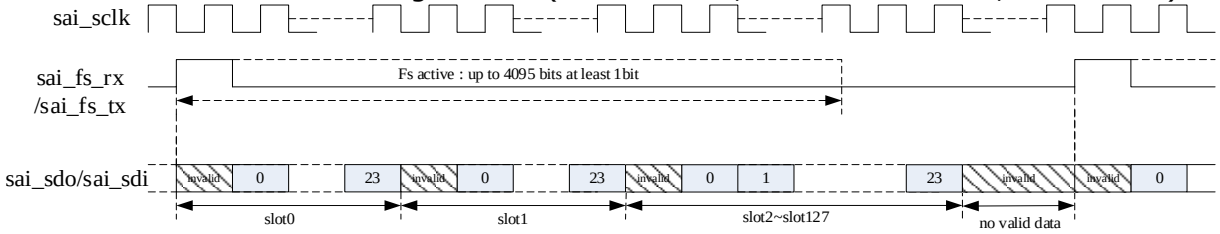

Fig.30-9 SAI I2S right mode timing format

This is the waveform of FS and SD delay time,as the posedge of FS (sai_fs_rx / sai_fs_tx) signal,we can send data at different time ,The time between the FS rise edge and the first valid bit can be configured using the fs_shift register,when fs_shift[0] == 1'b0,data send at posedge of sclk,when fs_shift[0] == 1'b1,data send at negedge of sclk.

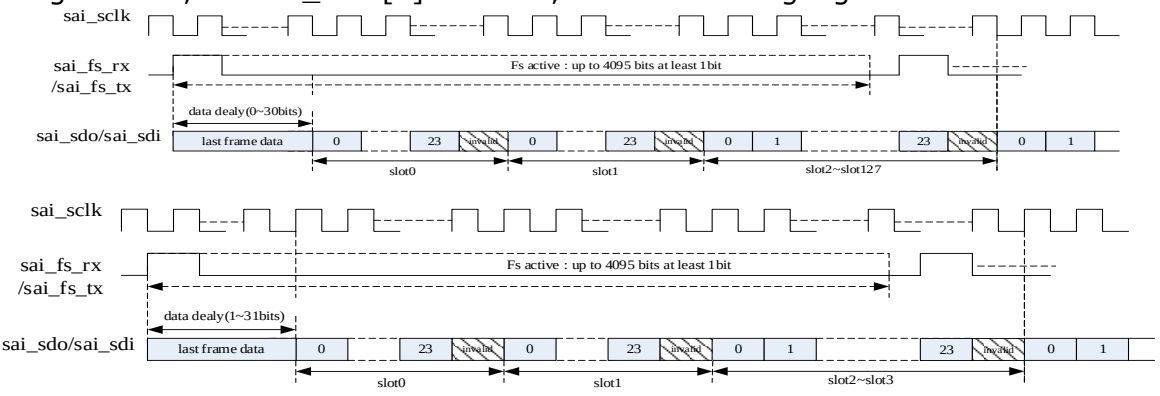

Fig.30-10 fs shift timing format

30.4 Register Description

30.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
SAI0	0x20960000
SAI1	0x20970000
SAI2	0x20980000
SAILP	0x208d0000

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30.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SAI_TXCR	0x0000	W	0x00000FFF	Transmit Control Register
SAI_FSCR	0x0004	W	0x0001F03F	Frame Sync Control Register
SAI_RXCR	0x0008	W	0x00000FFF	Receive Control Register
SAI_MONOCR	0x000C	W	0x00000000	Mono Control Register
SAI_XFER	0x0010	W	0x00000000	Transfer Start Register
SAI_CLR	0x0014	W	0x00000000	Sclk Domain Logic Clear Register
SAI_CKR	0x0018	W	0x00000000	Clock Generation Register
SAI_TXFIFOLR	0x001C	W	0x00000000	Transmit FIFO Level Register
SAI_RXFIFOLR	0x0020	W	0x00000000	Receive FIFO Level Register
SAI_DMACR	0x0024	W	0x00000000	DMA Control Register
SAI_INTCR	0x0028	W	0x00000000	Interrupt Control Register
SAI_INTSR	0x002C	W	0x00000000	Interrupt Status Register
SAI_PATH_SEL	0x0038	W	0x0000E4E4	Path Select Register
SAI_TX_SLOT_MASK0	0x003C	W	0x00000000	Transmit Slot 0~31 Mask
SAI_TX_SLOT_MASK1	0x0040	W	0x00000000	Transmit Slot 32~63 Mask
SAI_TX_SLOT_MASK2	0x0044	W	0x00000000	Transmit Slot 64~95 Mask state
SAI_TX_SLOT_MASK3	0x0048	W	0x00000000	Transmit Slot 96~127 Mask
SAI_RX_SLOT_MASK0	0x004C	W	0x00000000	Receive Slot 0~31 Mask
SAI_RX_SLOT_MASK1	0x0050	W	0x00000000	Receive Slot 32~63 Mask
SAI_RX_SLOT_MASK2	0x0054	W	0x00000000	Receive Slot 64~95 Mask
SAI_RX_SLOT_MASK3	0x0058	W	0x00000000	Receive Slot 96~127 Mask
SAI_TX_DATA_CNT	0x005C	W	0x00000000	Transmit Data Counter Register
SAI_RX_DATA_CNT	0x0060	W	0x00000000	Receive Data Counter Register
SAI_TX_TIMING_SHIFT	0x0064	W	0x00000000	Transmit Timing Shift Register
SAI_RX_TIMING_SHIFT	0x0068	W	0x00000000	Receive Timing Shift Register
SAI_STATUS	0x006C	W	0x00000007	Transfer Status Register
SAI_VERSION	0x0070	W	0x24101126	Version Register
SAI_FSXN	0x0074	W	0x00000000	Frame Sync x N Register
SAI_FS_TIMEOUT	0x0078	W	0x00000000	Frame Sync Timeout Register
SAI_LOOP2	0x007C	W	0x00000000	Tx Loopback Rx Register
SAI_FIFO_CHG	0x0080	W	0x00000000	Fifo Change Register
SAI_TXFLR_SET	0x0084	W	0x00000000	Tx Flr Num Register
SAI_RXFLR_SET	0x0088	W	0x00000000	Rx Flr Num Register
SAI_DEBUG_CTRL	0x008C	W	0x00000000	Debug Ctrl Register
SAI_TXDATA0_DB	0x0090	W	0x00000000	Tx0 Debug Data Register
SAI_TXDATA1_DB	0x0094	W	0x00000000	Tx1 Debug Data Register
SAI_TXDATA2_DB	0x0098	W	0x00000000	Tx2 Debug Data Register
SAI_TXDATA3_DB	0x009C	W	0x00000000	Tx3 Debug Data Register
SAI_RXDATA0_DB	0x00A0	W	0x00000000	Rx0 Debug Data Register
SAI_RXDATA1_DB	0x00A4	W	0x00000000	Rx1 Debug Data Register
SAI_RXDATA2_DB	0x00A8	W	0x00000000	Rx2 Debug Data Register
SAI_RXDATA3_DB	0x00AC	W	0x00000000	Rx3 Debug Data Register
SAI_TXDR	0x0100	W	0x00000000	Transmit FIFO Data Register
SAI_RXDR	0x0104	W	0x00000000	Receive FIFO Data Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

30.4.3 Detail Registers Description

SAI_TXCR

Address: Operational Base(0xFF800000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RW	0x0	flr_cnt_en tx flr cnt enl 1'b0:off 1'b1:on
25	RW	0x0	sync_en lrck sync ctrl 1'b0:off 1'b1:on
24	RW	0x0	lane_only only one path is pass
23	RW	0x0	ctl This bit select which one XFER.txs signal is used to start/stop data transfer. when config in Chained mode, support multiple controllers start/stop at the same time. 1'b0: Standalone, use bit txs in the current controller. 1'b1: Chained, use bit txs in the chained master controller.
22	RW	0x0	dse Data Start Edge Select 1'b0: rising edge 1'b1: falling edge
21:20	RW	0x0	lane Data Lanes Select 2'b00: 1 lane 2'b01: 2 lanes 2'b10: 3 lanes 2'b11: 4 lanes
19	RW	0x0	sjm Store Justified Mode 8bits~32bits DATA stored in 32 bits width FIFO. 1'b0: Right justified 1'b1: Left justified
18	RW	0x0	fbm First Bit Mode 1'b0: MSB 1'b1: LSB
17:11	RW	0x01	snb Slot Number Number of slots in one frame, support max 128 slots per lane. snb = (slots number) - 1. 7'h00: 1 slot 7'h01: 2 slots 7'h02: 3 slots 7'h03: 4 slots ..... 7'h7f: 128 slots
10	RW	0x1	vdj Valid Data Justified 1'b0: Right justified 1'b1: Left justified
9:5	RW	0x1f	sbw Slot Bits Width supports from 8 ~ 32 bits data width. sbw = (width in bits) - 1

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Bit	Attr	Reset Value	Description
4:0	RW	0x1f	vdw Valid Data Width supports from 8 ~ 32 bits data width. vdw = (width in bits) - 1

SAI_FSCR

Address: Operational Base(0xFF800000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	edge 1'b0: rising edge 1'b1: dual edge
23:12	RW	0x01f	fpw Frame Pulse Width fpw = (frame pulse width) - 1, support max 4095 bit pulse width. 12'h000: 1 bit 12'h001: 2 bits 12'h002: 3 bits ..... 12'hffe: 4095 bits 12'hfff: reserved
11:0	RW	0x03f	fw Frame Sync Width fw = (frame width in bits) - 1, support max 4096 bit frame width. 12'h007: 8 bits 12'h008: 9 bits ..... 12'hfff: 4096 bits

SAI_RXCR

Address: Operational Base(0xFF800000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RW	0x0	flr_cnt_en rx flr cnt enl 1'b0:off 1'b1:on
25	RW	0x0	sync_en lrck sync ctrl 1'b0:off 1'b1:on
24	RW	0x0	lane_only only one path is pass
23	RW	0x0	ctl This bit select which one XFER.rxs signal is used to start/stop data receive. when config in Chained mode, support multiple controllers start/stop at the same time. 1'b0: Standalone, use bit rxs in the current controller. 1'b1: Chained, use bit rxs in the chained master controller.

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Bit	Attr	Reset Value	Description
22	RW	0x0	dse Data Start Edge Select 1'b0: rising edge 1'b1: falling edge
21:20	RW	0x0	lane Data Lanes Select 2'b00: 1 lane 2'b01: 2 lanes 2'b10: 3 lanes 2'b11: 4 lanes
19	RW	0x0	sjm Store Justified Mode 8bits~32bits DATA stored in 32 bits width FIFO. 1'b0: Right justified 1'b1: Left justified
18	RW	0x0	fbm First Bit Mode 1'b0: MSB 1'b1: LSB
17:11	RW	0x01	snb Slot Number Number of slots in one frame, support max 128 slots per lane. snb = (slots number) - 1. 7'h00: 1 slot 7'h01: 2 slots 7'h02: 3 slots 7'h03: 4 slots ..... 7'h7f: 128 slots
10	RW	0x1	vdj Valid Data Justified 1'b0: Right justified 1'b1: Left justified
9:5	RW	0x1f	sbw Slot Bits Width supports from 8 ~ 32 bits data width. sbw = (width in bits) - 1
4:0	RW	0x1f	vdw Valid Data Width supports from 8 ~ 32 bits data width. vdw = (width in bits) - 1

SAI_MONOCR

Address: Operational Base(0xFF800000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:2	RW	0x00	rmono_slot Receive Mono Slot Select Choose one slot as the mono data. 7'h00: the first slot 7'h01: the second slot ..... 7'h7f: the 128'th slot

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Bit	Attr	Reset Value	Description
1	RW	0x0	rmono Receive Mono Enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	tmono Transmit Mono Enable 1'b0: Disable 1'b1: Enable

SAI_XFER

Address: Operational Base(0xFF800000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	tx_auto TX Auto Mode used for tx only mode, because controller will auto gates the clk/fsync when tx FIFO empty. 1'b0: stop tx auto mode. 1'b1: start tx auto mode, and controller will auto gates clk/fsync when tx FIFO empty. if this bit enabled, the XFER.fss, XFER.txs, XFER.rxs are ignored. when the tx FIFO empty, will auto gates the clk/fsync, and then user should disable this bits and do CLR.txc, CLR.fsc.
5	RW	0x0	rdc 1'b0: Stop cnt 1'b1: Start cnt
4	RW	0x0	tdc 1'b0: Stop cnt 1'b1: Start cnt
3	RW	0x0	rxs 1'b0: Stop RX transfer 1'b1: Start RX transfer
2	RW	0x0	txs 1'b0: Stop TX transfer 1'b1: Start TX transfer
1	RW	0x0	fss 1'b0: Disable 1'b1: Enable
0	RW	0x0	clk_en reserved

SAI_CLR

Address: Operational Base(0xFF800000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	auto_clr auto clear 1'b0:stop 1'b1:start
3	RW	0x0	fcr This is a self-cleared bit. write 1 to enable clear all for slave mode .

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Bit	Attr	Reset Value	Description
2	W1C	0x0	fsc Frame Sync Clear This is a self-cleared bit. write 1 to clear all receive logic.
1	W1C	0x0	rxc Receive Logic Clear This is a self-cleared bit. write 1 to clear all receive logic.
0	W1C	0x0	txc Transmit Logic Clear This is a self-cleared bit. write 1 to clear all transmit logic.

SAI_CKR

Address: Operational Base(0xFF800000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:3	RW	0x000	mdiv The divider is used to div output sclk from mclk. mdiv = (mclk / sclk) - 1. For example, if clk divider is 3, then the frequency of sclk is clk / 4.
2	RW	0x0	mss Master/Slave Mode Select 1'b0: Master mode 1'b1: Slave mode
1	RW	0x0	ckp Sclk Polarity 1'b0: Sample data at posedge sclk and drive data at negedge sclk 1'b1: Sample data at negedge sclk and drive data at posedge sclk
0	RW	0x0	fsp Frame Sync Polarity 1'b0: Frame sync low active 1'b1: Frame sync high active

SAI_TXFIFOLR

Address: Operational Base(0xFF800000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:18	RO	0x00	tfl3 Transmit FIFO3 Level Contains the number of valid data entries in the transmit fifo3.
17:12	RO	0x00	tfl2 Transmit FIFO2 Level Contains the number of valid data entries in the transmit fifo2.
11:6	RO	0x00	tfl1 Transmit FIFO1 Level Contains the number of valid data entries in the transmit fifo1.
5:0	RO	0x00	tfl0 Transmit FIFO0 Level Contains the number of valid data entries in the transmit fifo0.

SAI_RXFIFOLR

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Address: Operational Base(0xFF800000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:18	RO	0x00	rfl3 Receive FIFO3 Level Contains the number of valid data entries in the receive fifo3.
17:12	RO	0x00	rfl2 Receive FIFO2 Level Contains the number of valid data entries in the receive fifo2.
11:6	RO	0x00	rfl1 Receive FIFO1 Level Contains the number of valid data entries in the receive fifo1.
5:0	RO	0x00	rfl0 Receive FIFO0 Level Contains the number of valid data entries in the receive fifo0.

SAI_DMACR

Address: Operational Base(0xFF800000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	rde Receive DMA Enable 1'b0: Disable 1'b1: Enable
23:21	RO	0x0	reserved
20:16	RW	0x00	rdl Receive Data Level This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above this field value + 1.
15:9	RO	0x00	reserved
8	RW	0x0	tde Transmit DMA Enable 1'b0: Disable 1'b1: Enable
7:5	RO	0x0	reserved
4:0	RW	0x00	tdl Transmit Data Level This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the TX FIFO(TX FIFO0 if CSR=00;TX FIFO1 if CSR=01,TX FIFO2 if CSR=10,TX FIFO3 if CSR=11)is equal to or below this field value.

SAI_INTCR

Address: Operational Base(0xFF800000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28	RW	0x0	fslostc Frame Sync Lost Interrupt Clear Write 1 to clear fs lost interrupt.
27	RW	0x0	fslost Frame Sync Lost Interrupt Enable 1'b0: Disable 1'b1: Enable
26	RW	0x0	fserrc Frame Sync Error Interrupt Clear Write 1 to clear fs err interrupt.
25	RW	0x0	fserr Frame Sync Error Interrupt Enable 1'b0: Disable 1'b1: Enable
24:20	RW	0x00	rft Receive FIFO Threshold When the number of receive fifo entries is more than or equal to this threshold plus 1, the receive fifo full interrupt is triggered.
19	RO	0x0	reserved
18	WO	0x0	rxoic RX Overrun Interrupt Clear Write 1 to clear RX overrun interrupt.
17	RW	0x0	rxoie RX Overrun Interrupt Enable 1'b0: Disable 1'b1: Enable
16	RW	0x0	rxfie RX Full Interrupt Enable 1'b0: Disable 1'b1: Enable
15:13	RO	0x0	reserved
12	RW	0x0	rxflrerrc Rx flr Error Interrupt Enable 1'b0: Disable 1'b1: Enable
11	RW	0x0	rxflrerr Rx flr Error Interrupt Enable 1'b0: Disable 1'b1: Enable
10	RW	0x0	txflrerrc Tx flr Error Interrupt Clear Write 1 to clear fs err interrupt.
9	RW	0x0	txflrerr Tx flr Error Interrupt Enable 1'b0: Disable 1'b1: Enable
8:4	RW	0x00	tft Transmit FIFO Threshold When the number of transmit fifo entries is less than or equal to this threshold, the transmit fifo empty interrupt is triggered.
3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2	W1C	0x0	txuic TX Underrun Interrupt Clear Write 1 to clear TX underrun interrupt.
1	RW	0x0	txuie TX Underrun Interrupt Enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	txeie TX Empty Interrupt Enable 1'b0: Disable 1'b1: Enable

SAI_INTSR

Address: Operational Base(0xFF800000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RW	0x0	rxflrerri Rx flr Error Interrupt Status 1'b0: Inactive 1'b1: Active
20	RW	0x0	txflrerri Tx flr Error Interrupt Status 1'b0: Inactive 1'b1: Active
19	RO	0x0	fslosti Frame Sync Lost Interrupt Status 1'b0: Inactive 1'b1: Active
18	RO	0x0	fserri Frame Sync Error Interrupt Status 1'b0: Inactive 1'b1: Active
17	RO	0x0	rxoi RX Overrun Interrupt Status 1'b0: Inactive 1'b1: Active
16	RO	0x0	rxfi RX Full Interrupt Status 1'b0: Inactive 1'b1: Active
15:2	RO	0x0000	reserved
1	RO	0x0	txui TX Underrun Interrupt Status 1'b0: Inactive 1'b1: Active
0	RO	0x0	txei TX Empty Interrupt Status 1'b0: Inactive 1'b1: Active

SAI_PATH_SEL

Address: Operational Base(0xFF800000) + offset (0x0038)

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Bit	Attr	Reset Value	Description
31	RW	0x0	rx_ch_sel 1'b0: forward 1'b1: reverse
30	RW	0x0	loopback_mode_en 1'b0: Disable 1'b1: Enable
29:22	RW	0x00	loopback_path_sel Loopback Path Sel [23:22]:sdi0 sel sdo0 or sdo1 or sdo2 or sdo3 [25:24]:sdi1 sel sdo0 or sdo1 or sdo2 or sdo3 [27:26]:sdi2 sel sdo0 or sdo1 or sdo2 or sdo3 [29:28]:sdi3 sel sdo0 or sdo1 or sdo2 or sdo3
21:18	RW	0x0	loopback Loopback Control SDO -> SDI [18]:Loopback_en0 [19]:Loopback_en1 [20]:Loopback_en2 [21]:Loopback_en3 1'b0: Disable 1'b1: Enable
17	RW	0x0	sync_out_sel Sync Out Select 1'b0: sclk and fs sync out use out signal 1'b1: sclk and fs sync out use in signal
16	RW	0x0	sync_in_sel Sync In Select 1'b0: sclk and fs use pad signal 1'b1: sclk and fs use sync input port
15:14	RW	0x3	rx_path_select3 RX Path Select3 2'b00: Path3 data from sdi0 2'b01: Path3 data from sdi1 2'b10: Path3 data from sdi2 2'b11: Path3 data from sdi3
13:12	RW	0x2	rx_path_select2 RX Path Select2 2'b00: Path2 data from sdi0 2'b01: Path2 data from sdi1 2'b10: Path2 data from sdi2 2'b11: Path2 data from sdi3
11:10	RW	0x1	rx_path_select1 RX Path Select1 2'b00: Path0 data from sdi0 2'b01: Path0 data from sdi1 2'b10: Path0 data from sdi2 2'b11: Path0 data from sdi3
9:8	RO	0x0	rx_path_select0 RX Path Select0 2'b00: Path0 data from sdi0 2'b01: Path0 data from sdi1 2'b10: Path0 data from sdi2 2'b11: Path0 data from sdi3

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Bit	Attr	Reset Value	Description
7:6	RW	0x3	tx_path_select3 TX Path Select3 2'b00: Sdo3 output data from path0 2'b01: Sdo3 output data from path1 2'b10: Sdo3 output data from path2 2'b11: Sdo3 output data from path3
5:4	RW	0x2	tx_path_select2 TX Path Select2 2'b00: Sdo2 output data from path0 2'b01: Sdo2 output data from path1 2'b10: Sdo2 output data from path2 2'b11: Sdo2 output data from path3
3:2	RW	0x1	tx_path_select1 TX Path Select1 2'b00: Sdo1 output data from path0 2'b01: Sdo1 output data from path1 2'b10: Sdo1 output data from path2 2'b11: Sdo1 output data from path3
1:0	RW	0x0	tx_path_select0 TX Path Select0 2'b00: Sdo0 output data from path0 2'b01: Sdo0 output data from path1 2'b10: Sdo0 output data from path2 2'b11: Sdo0 output data from path3

SAI_TX_SLOT_MASK0

Address: Operational Base(0xFF800000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_slot_mask0 Transmit Slot 0~31 Mask slot 0~31 mask state 1'b0: Slot active 1'b1: Slot mask,data is invalid

SAI_TX_SLOT_MASK1

Address: Operational Base(0xFF800000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_slot_mask1 Transmit Slot 32~63 Mask slot 32~63 mask state 1'b0: Slot active 1'b1: Slot mask,data is invalid

SAI_TX_SLOT_MASK2

Address: Operational Base(0xFF800000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_slot_mask2 Transmit Slot 64~95 Mask slot 64~95 mask state 1'b0: Slot active 1'b1: Slot mask,data is invalid

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SAI_TX_SLOT_MASK3

Address: Operational Base(0xFF800000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_slot_mask3 Transmit Slot 96~127 Mask slot 96~127 mask state 1'b0: Slot active 1'b1: Slot mask,data is invalid

SAI_RX_SLOT_MASK0

Address: Operational Base(0xFF800000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rx_slot_mask0 Receive Slot 0~31 Mask Slot 0~31 mask state 1'b0: Slot active 1'b1: Slot mask,data is invalid

SAI_RX_SLOT_MASK1

Address: Operational Base(0xFF800000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rx_slot_mask1 Receive Slot 32~63 Mask slot 32~63 mask state 1'b0: Slot active 1'b1: Slot mask,data is invalid

SAI_RX_SLOT_MASK2

Address: Operational Base(0xFF800000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rx_slot_mask2 Receive Slot 64~95 Mask slot 64~95 mask state 1'b0: Slot active 1'b1: Slot mask,data is invalid

SAI_RX_SLOT_MASK3

Address: Operational Base(0xFF800000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rx_slot_mask3 Receive Slot 96~127 Mask slot 96~127 mask state 1'b0: Slot active 1'b1: Slot mask,data is invalid

SAI_TX_DATA_CNT

Address: Operational Base(0xFF800000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	tx_data_cnt TX data counter

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SAI_RX_DATA_CNT

Address: Operational Base(0xFF800000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data_cnt RX data counter

SAI_TX_TIMING_SHIFT

Address: Operational Base(0xFF800000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:24	RW	0x0	data_shift_left Transmit Data Shift Left The data is shifted to the left by n/2 sclks relative to the frame sync edge. 2'b00: no shift 2'b01: shift 1/2 sclk left. 2'b10: shift 1 sclk left.
23:0	RW	0x000000	data_shift_right Transmit Data Shift Right The data is shifted to the right by n/2 SCLKs relative to the frame sync edge. 24'h00: no shift 24'h01: 1/2 sclk shift right. 24'h02: 1 sclk shift right. .....

SAI_RX_TIMING_SHIFT

Address: Operational Base(0xFF800000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	data_shift_right Receive Data Shift Right The data is shifted to the right by n/2 SCLKs relative to the frame sync edge. 24'h00: no shift 24'h01: 1/2 sclk shift right. 24'h02: 1 sclk shift right. .....

SAI_STATUS

Address: Operational Base(0xFF800000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x1	rx_idle Receive Logic Idle 1'b0: busy 1'b1: idle
1	RW	0x1	tx_idle Transmit Logic Idle 1'b0: busy 1'b1: idle

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Bit	Attr	Reset Value	Description
0	RW	0x1	fs_idle Frame Sync Idle 1'b0: busy 1'b1: idle

SAI_VERSION

Address: Operational Base(0xFF800000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:0	RO	0x24101126	sai_vertion SAI version

SAI_FSXN

Address: Operational Base(0xFF800000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	fsxn1_shift N1 shift to the left by n N1.fs releative to frame sync edge. 3'h0: 0 fs 3'h1: 1 fs ..... 3'h7: 7fs
28:26	RW	0x0	fsxn0_shift N0 shift to the left by n N0.fs releative to frame sync edge. 3'h0: 0 fs 3'h1: 1 fs ..... 3'h7: 7fs
25:14	RW	0x000	fsxn1_fw Frame Sync x N1 Width 12'h007: 8 bits 12'h008: 9 bits ..... 12'hffe: 4095 bits 12'hfff: 4096 bits
13	RW	0x0	fsxn1_en Frame Sync x N1 Enable 1'b0: Disable 1'b1: Enable
12:1	RW	0x000	fsxn0_fw Frame Sync x N0 Width 12'h007: 8 bits 12'h008: 9 bits ..... 12'hffe: 4095 bits 12'hfff: 4096 bits
0	RW	0x0	fsxn0_en Frame Sync x N0 Enable 1'b0: Disable 1'b1: Enable

SAI_FS_TIMEOUT

Address: Operational Base(0xFF800000) + offset (0x0078)

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Bit	Attr	Reset Value	Description
31:1	RW	0x00000000	timeout_value The timeout value is used with INTCR.fslost to detect whether the external frame sync is lost, when the timeout count done and no frame sync found, the Frame Lost Interrupt is generated.
0	RW	0x0	timeout_en Frame Sync Timeout Enable 1'b0: Disable 1'b1: Enable

SAI_LOOP2

Address: Operational Base(0xFF800000) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	rx_ch_sel [4]:path0 [5]:path1 [6]:path2 [7]:path3 1'b0: forward 1'b1: reverse
3:0	RW	0x0	loopback_mode_en [0]:path0 [1]:path1 [2]:path2 [3]:path3 1'b0: Disable 1'b1: Enable

SAI_FIFO_CHG

Address: Operational Base(0xFF800000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:8	RW	0x00	rx_fifo_chg_num Slot Number Number of slots in one frame, support max 128 slots per lane. snb = (slots number) - 1. 7'h00: 1 slot 7'h01: 2 slots 7'h02: 3 slots 7'h03: 4 slots ..... 7'h7f: 128 slots

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Bit	Attr	Reset Value	Description
7:1	RW	0x00	tx_fifo_chg_num Slot Number Number of slots in one frame, support max 128 slots per lane. snb = (slots number) - 1. 7'h00: 1 slot 7'h01: 2 slots 7'h02: 3 slots 7'h03: 4 slots ..... 7'h7f: 128 slots
0	RW	0x0	fifo_mode fifo change mode 1'b0:off 1'b1:on

SAI_TXFLR_SET

Address: Operational Base(0xFF800000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txflr_cnt_set The timeout value is used with INTCR., when the timeout count done and tx fifo flr not change, the Interrupt is generated.

SAI_RXFLR_SET

Address: Operational Base(0xFF800000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxflr_cnt_set The timeout value is used with INTCR., when the timeout count done and rx fifo flr not change, the Interrupt is generated.

SAI_DEBUG_CTRL

Address: Operational Base(0xFF800000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	debug_en debug data input en 1'b0:off 1'b1:on

SAI_TXDATA0_DB

Address: Operational Base(0xFF800000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	txdata0 debug tx data0

SAI_TXDATA1_DB

Address: Operational Base(0xFF800000) + offset (0x0094)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	txdata1 debug tx data1

SAI_TXDATA2_DB
Address: Operational Base(0xFF800000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	txdata2 debug tx data2

SAI_TXDATA3_DB
Address: Operational Base(0xFF800000) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	txdata3 debug tx data3

SAI_RXDATA0_DB
Address: Operational Base(0xFF800000) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata0 debug rx data0

SAI_RXDATA1_DB
Address: Operational Base(0xFF800000) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata1 debug rx data1

SAI_RXDATA2_DB
Address: Operational Base(0xFF800000) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata2 debug rx data2

SAI_RXDATA3_DB
Address: Operational Base(0xFF800000) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata3 debug rx data3

SAI_TXDR
Address: Operational Base(0xFF800000) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdr Transmit FIFO Data Register When it is written, data are moved into the transmit fifo.

SAI_RXDR

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Address: Operational Base(0xFF800000) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxdr Receive FIFO Data Register When the register is read, data in the receive fifo is accessed.

30.5 Interface Description

The following table shows the SAI0 interface description.

Table 30-1 SAI0 mux0 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
sai0_mclk_m0	I/O	SAI0_MCLK_M0/PWM2_CH6_M1/GPIO7_A2	GPIO7A_IOMUX_SEL_0 [11:8]=1
sai0_sclk_m0	I/O	SAI0_SCLK_M0/PWM2_CH4_M1/GPIO7_A0	GPIO7A_IOMUX_SEL_0 [3:0]=1
sai0_lrck_m0	I/O	SAI0_LRCK_M0/DSM_AUD_LN/PWM2_CH7_M1/GPIO7_A3	GPIO7A_IOMUX_SEL_0 [15:12]=1
sai0_sdo0_m0	O	SAI0_SDO0_M0/DSM_AUD_LP/GPIO7_A5	GPIO7A_IOMUX_SEL_1 [7:4]=1
sai0_sdo1_m0	O	SAI0_SDI3_M0/SAI0_SDO1_M0/PDM_SDI3_M0/UART2_RTSN_M1/GPIO7_A7	GPIO7A_IOMUX_SEL_1 [15:12]=2
sai0_sdo2_m0	O	SAI0_SDI2_M0/SAI0_SDO2_M0/PDM_SDI2_M0/DSM_AUD_RN/I2C1_SCL_M3/UART2_RX_M1/GPIO7_B0	GPIO7B_IOMUX_SEL_0 [3:0]=1
sai0_sdo3_m0	O	SAI0_SDI1_M0/SAI0_SDO3_M0/PDM_SDI1_M0/DSM_AUD_RP/I2C1_SDA_M3/UART2_TX_M1/GPIO7_B1	GPIO7B_IOMUX_SEL_0 [7:4]=2
sai0_sdi0_m0	I	SAI0_SDI0_M0/PDM_SDI0_M0/GPIO7_A6	GPIO7A_IOMUX_SEL_1 [11:8]=1
sai0_sdi1_m0	I	SAI0_SDI1_M0/SAI0_SDO3_M0/PDM_SDI1_M0/DSM_AUD_RP/I2C1_SDA_M3/UART2_TX_M1/GPIO7_B1	GPIO7B_IOMUX_SEL_0 [7:4]=1
sai0_sdi2_m0	I	SAI0_SDI2_M0/SAI0_SDO2_M0/PDM_SDI2_M0/DSM_AUD_RN/I2C1_SCL_M3/UART2_RX_M1/GPIO7_B0	GPIO7B_IOMUX_SEL_0 [3:0]=1
sai0_sdi3_m0	I	SAI0_SDI3_M0/SAI0_SDO1_M0/PDM_SDI3_M0/UART2_RTSN_M1/GPIO7_A7	GPIO7A_IOMUX_SEL_1 [15:12]=1

Table 30-2 SAI0 mux1 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
sai0_mclk_m1	I/O	VI_CIF_D4_M0/ETH_RXD3_M0/SAI0_MCLK_M1/PWM2_CH0_M2/UART5_RTSN_M2/I2C5_SCL_M3/GPIO6_A4	GPIO6A_IOMUX_SEL_1 [3:0]=4
sai0_sclk_m1	I/O	VI_CIF_D0_M0/ETH_PPSTRIG_M0/CAN0_RXD_M1/SAI0_SCLK_M1/PWM1_CH0_M2/UART4_TX_M2/I2C3_SCL_M3/GPIO6_A0	GPIO6A_IOMUX_SEL_0 [3:0]=4
sai0_lrck_m1	I/O	VI_CIF_D1_M0/ETH_PTP_REFCLK_M0/CAN0_TXD_M1/SAI0_LRCK_M1/PWM1_CH1_M2/UART4_RX_M2/I2C3_SDA_M3/GPIO6_A1	GPIO6A_IOMUX_SEL_0 [7:4]=4
sai0_sdo0_m1	O	VI_CIF_D2_M0/ETH_PPSCLK_M0/CAN1_RXD_M1/SAI0_SDO0_M1/PWM1_CH2_M2/UART5_TX_M2/I2C4_SCL_M1/GPIO6_A2	GPIO6A_IOMUX_SEL_0 [11:8]=4

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Module Pin	Direction	Pad Name	IOMUX Setting
sai0_sdo1_m1	O	VI_CIF_D7_M0/ETH_TXD0_M0/PWM2_CH3_M2/SAI0_SDI3_M1/SAI0_SDO1_M1/UART4_CTSN_M2/GPIO6_A7	GPIO6A_IOMUX_SEL_1 [15:12]=5
sai0_sdo2_m1	O	VI_CIF_D8_M0/ETH_TXD1_M0/SPI1_CSN1_M0/SAI0_SDI2_M1/SAI0_SDO2_M1/UART6_TX_M1/GPIO6_B0	GPIO6B_IOMUX_SEL_0 [3:0]=5
sai0_sdo3_m1	O	VI_CIF_D9_M0/ETH_TXCTL_M0/SPI1_CSN0_M0/SAI0_SDI1_M1/SAI0_SDO3_M1/UART6_RX_M1/GPIO6_B1	GPIO6B_IOMUX_SEL_0 [7:4]=5
sai0_sdi0_m1	I	VI_CIF_D3_M0/ETH_RXD2_M0/CAN1_TXD_M1/SAI0_SDI0_M1/PWM1_CH3_M2/UART5_RX_M2/I2C4_SDA_M1/GPIO6_A3	GPIO6A_IOMUX_SEL_0 [15:12]=4
sai0_sdi1_m1	I	VI_CIF_D8_M0/ETH_TXD1_M0/SPI1_CSN1_M0/SAI0_SDI2_M1/SAI0_SDO2_M1/UART6_TX_M1/GPIO6_B0	GPIO6B_IOMUX_SEL_0 [7:4]=4
sai0_sdi2_m1	I	VI_CIF_D8_M0/ETH_TXD1_M0/SPI1_CSN1_M0/SAI0_SDI2_M1/SAI0_SDO2_M1/UART6_TX_M1/GPIO6_B0	GPIO6B_IOMUX_SEL_0 [3:0]=4
sai0_sdi3_m1	I	VI_CIF_D9_M0/ETH_TXCTL_M0/SPI1_CSN0_M0/SAI0_SDI1_M1/SAI0_SDO3_M1/UART6_RX_M1/GPIO6_B1	GPIO6A_IOMUX_SEL_1 [15:12]=4

Table 30-3 SAI1 mux0 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
i2s1_mclk_m0	I/O	FSPI0_CSN0/SAI1_MCLK_M0/SDMMC0_TESTDATA_OUT/GPIO1_B0	GPIO1B_IOMUX_SEL_0 [3:0]=2
i2s1_sclk_m0	I/O	FSPI0_D1/SAI1_SCLK_M0/GPIO1_B5	GPIO1B_IOMUX_SEL_1 [7:4]=2
i2s1_lrck_m0	I/O	FSPI0_D0/SAI1_LRCK_M0/GPIO1_B4	GPIO1B_IOMUX_SEL_1 [3:0]=2
i2s1_sdo0_m0	O	FSPI0_D2/SAI1_SDO_M0/GPIO1_B2	GPIO1B_IOMUX_SEL_0 [11:8]=2
i2s1_sdi0_m0	I	FSPI0_D3/SAI1_SDI_M0/GPIO1_B6	GPIO1B_IOMUX_SEL_1 [11:8]=2

Table 30-4 SAI1 mux1 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
i2s1_mclk_m1	I/O	SPI0_CSN1_M1/SAI1_MCLK_M1/PWM0_CH5_M1/UART4_TX_M0/GPIO4_A3	GPIO4A_IOMUX_SEL_0 [15:12]=2
i2s1_sclk_m1	I/O	SPI0_MOSI_M1/SAI1_SCLK_M1/I2C3_SCL_M1/GPIO4_A4	GPIO4A_IOMUX_SEL_1 [3:0]=2
i2s1_lrck_m1	I/O	SPI0_MISO_M1/SAI1_LRCK_M1/I2C3_SDA_M1/GPIO4_A5	GPIO4A_IOMUX_SEL_1 [7:4]=2
i2s1_sdo0_m1	O	SPI0_CSN0_M1/SAI1_SDI_M1/PWM0_CH6_M1/UART5_TX_M0/I2C4_SDA_M2/GPIO4_A6	GPIO4A_IOMUX_SEL_1 [11:8]=2
i2s1_sdi0_m1	I	SPI0_CLK_M1/SAI1_SDO_M1/PWM0_CH7_M1/UART5_RX_M0/I2C4_SCL_M2/GPIO4_A7	GPIO4A_IOMUX_SEL_1 [15:12]=2

Table 30-5 SAI1 mux2 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
i2s1_mclk_m2	I/O	VO_LCDC_D19/ETH_RXD2_M1/VI_CIF_D15_M1/DSMC_D4/SAI1_MCLK_M2/PWM3_CH3_M1/GPIO5_C3	GPIO5C_IOMUX_SEL_0 [15:12]=5

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Module Pin	Direction	Pad Name	IOMUX Setting
i2s1_sclk_m2	I/O	VO_LCDC_D21/ETH_TXD2_M1/VI_CIF_CLKOUT_M1/DSMC_D2/SAI1_SCLK_M2/PWM3_CH5_M1/GPIO5_C5	GPIO5C_IOMUX_SEL_1 [7:4]=5
i2s1_lrck_m2	I/O	VO_LCDC_D22/ETH_TXCLK_M1/VI_CIF_CLKIN_M1/DSMC_D1/SAI1_LRCK_M2/PWM3_CH6_M1/GPIO5_C6	GPIO5C_IOMUX_SEL_1 [11:8]=5
i2s1_sdo0_m2	O	VO_LCDC_D20/ETH_RXD3_M1/VI_CIF_VSYNC_M1/DSMC_D3/SAI1_SDO_M2/PWM3_CH4_M1/GPIO5_C4	GPIO5C_IOMUX_SEL_1 [3:0]=5
i2s1_sdi0_m2	I	VO_LCDC_D23/ETH_RXCLK_M1/VI_CIF_HSYNC_M1/DSMC_D0/SAI1_SDI_M2/PWM3_CH7_M1/GPIO5_C7	GPIO5C_IOMUX_SEL_1 [15:12]=5

Table 30-6 SAI2 mux0 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
i2s2_mclk_m0	I/O	SPI1_CSN1_M1/SAI2_MCLK_M0/SDMMC1_DETN/UART1_TX_M1/I2C5_SCL_M1/GPIO3_B6	GPIO3B_IOMUX_SEL_1 [11:8]=2
i2s2_sclk_m0	I/O	SPI1_CLK_M1/SAI2_SCLK_M0/PWM2_CH2_M0/UART1_RTSN_M1/I2C4_SCL_M0/FEPHY_LEDLINK_M0/GPIO3_B4	GPIO3B_IOMUX_SEL_1 [3:0]=2
i2s2_lrck_m0	I/O	SPI1_CSN0_M1/SAI2_LRCK_M0/PWM2_CH3_M0/UART1_CTSN_M1/I2C4_SDA_M0/FEPHY_LEDSPD_M0/GPIO3_B5	GPIO3B_IOMUX_SEL_1 [7:4]=2
i2s2_sdo0_m0	O	SPI1_MOSI_M1/SAI2_SDO_M0/PWM2_CH0_M0/FLASH_TRIG_OUT/GPIO3_B2	GPIO3B_IOMUX_SEL_0 [11:8]=2
i2s2_sdi0_m0	I	SPI1_MISO_M1/SAI2_SDI0_M0/PWM2_CH1_M0/PRELIGHT_TRIG_OUT/GPIO3_B3	GPIO3B_IOMUX_SEL_0 [15:12]=2
i2s2_sdi1_m0	I	SAI2_SDI1_M0/UART1_RX_M1/I2C5_SDA_M1/GPIO3_B7	GPIO3B_IOMUX_SEL_1[15:12]=2
i2s2_sdi2_m0	I	SAI2_SDI2_M0/UART2_TX_M0/GPIO3_B1	GPIO3B_IOMUX_SEL_0[7:4]=2

Table 30-7 SAI2 mux1 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
i2s2_mclk_m1	I/O	VO_LCDC_D3/SPI0_CSN0_M2/DSMC_D14/SAI2_MCLK_M1/PWM0_CH4_M2/UART4_RX_M1/GPIO5_A3	GPIO5A_IOMUX_SEL_0 [15:12]=5
i2s2_sclk_m1	I/O	VO_LCDC_D5/SPI0_MISO_M2/DSMC_D12/SAI2_SCLK_M1/PWM0_CH2_M1/UART5_RX_M1/GPIO5_A5	GPIO5A_IOMUX_SEL_1 [7:4]=5
i2s2_lrck_m1	I/O	VO_LCDC_D7/SPI0_CSN1_M2/VI_CIF_D3_M1/DSMC_D10/SAI2_LRCK_M1/I2C5_SDA_M2/PWM0_CH0_M1/UART5_CTSN_M1/GPIO5_A7	GPIO5A_IOMUX_SEL_1 [15:12]=5
i2s2_sdo0_m1	O	VO_LCDC_D4/SPI0_MOSI_M2/DSMC_D13/SAI2_SDO_M1/PWM0_CH3_M1/UART5_TX_M1/GPIO5_A4	GPIO5A_IOMUX_SEL_1 [3:0]=5
i2s2_sdi0_m1	I	VO_LCDC_D6/SPI0_CLK_M2/DSMC_D11/SAI2_SDI0_M1/PWM0_CH1_M1/UART5_RTSN_M1/GPIO5_A6	GPIO5A_IOMUX_SEL_1 [11:8]=5
i2s2_sdi1_m1	I	VO_LCDC_D2/ETH_PPSCLK_M1/VI_CIF_D2_M1/DSMC_D15/SAI2_SDI1_M1/PWM0_CH5_M2/UART4_TX_M1/GPIO5_A2	GPIO5A_IOMUX_SEL_0 [11:8]=5
i2s2_sdi2_m1	I	VO_LCDC_D1/I2C5_SCL_M2/VI_CIF_D1_M1/DSMC_DQS1/SAI2_SDI2_M1/IR_FPA_SDA1/PWM2_CH5_M0/UART4_CTSN_M1/GPIO5_A1	GPIO5A_IOMUX_SEL_0 [7:4]=5

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30.6 Application Notes

30.6.1 Software Application Notes

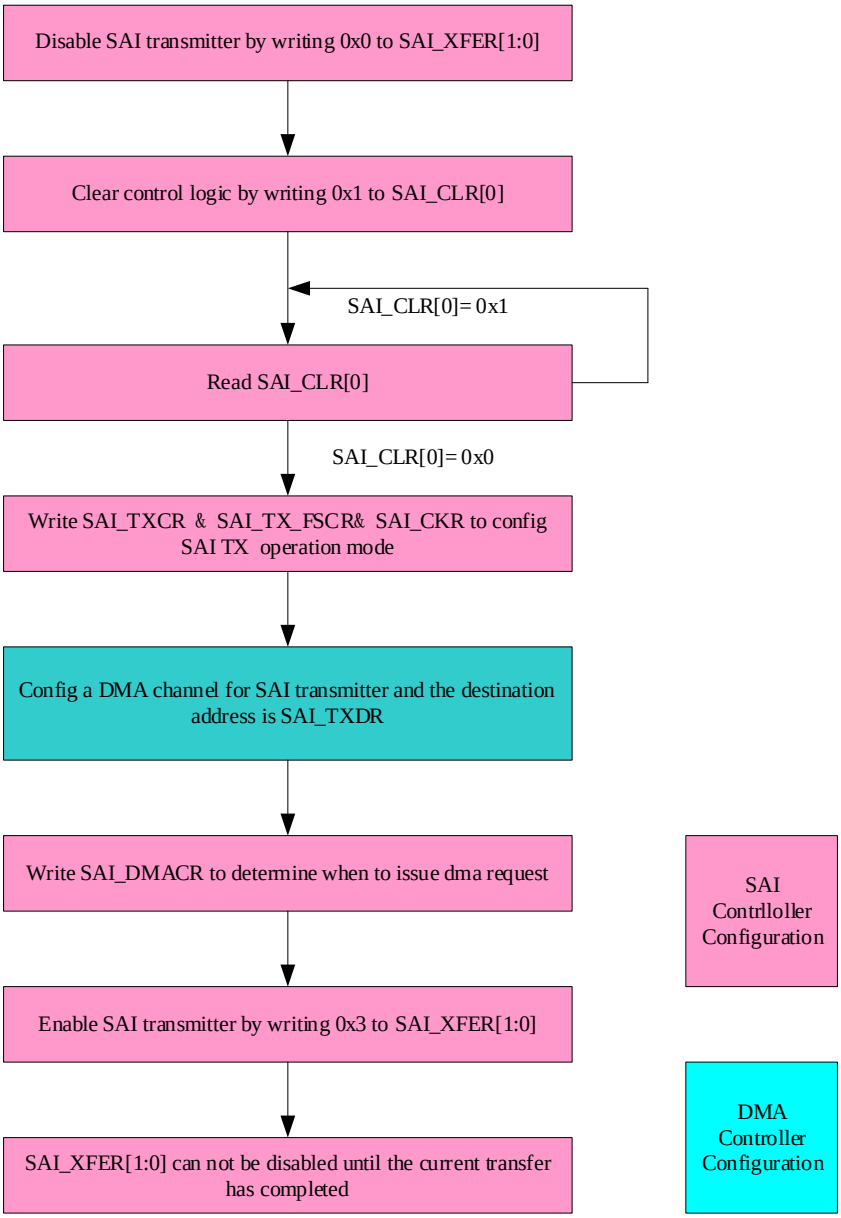

Fig.30-5 SAI controller transmit operation flow chart

Note: User should clear TX/RX logical by CLR[0]/CLR[1] and wait clear operation done before configure the other registers.

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Chapter 31 Pulse Density Modulation (PDM)

31.1 Overview

The Pulse Density Modulation (PDM) is a PDM interface controller that supports mono PDM format. It integrates a clock generator driving the PDM microphone and embeds filters which decimate the incoming bit stream to obtain most common audio rates.
PDM supports the following features:

- Support one internal 32-bit wide and 128-location deep FIFOs for receiving audio data
- Support receive FIFO full, overflow interrupt and all interrupts can be masked
- Support configurable water level of receive FIFO full interrupt
- Support combined interrupt output
- Support AHB bus slave interface
- Support DMA handshaking interface and configurable DMA water level
- Support PDM master receive mode
- Support 4 paths. Each path is composed of two digital microphone channels, the PDM can be used with four stereo or eight mono microphones. Each path is enabled or disabled independently
- Support 16 ~24 bit sample resolution
- Support sample rate:

8KHz, 16KHz, 32KHz, 64KHz, 128KHz, 11.025KHz, 22.05KHz, 44.1KHz, 88.2KHz, 176.4KHz, 12KHz, 24KHz, 48KHz, 96KHz, 192KHz

- Support two 16-bit audio data store together in one 32-bit wide location
- Support 16 to 31 bit audio data left or right justified in 32-bit wide FIFO
- Support programmable data sampling sensibility (rising or falling edge)
- Support mute function
- Support gain control
- Support 2.4MHz pdm clock

31.2 Block Diagram

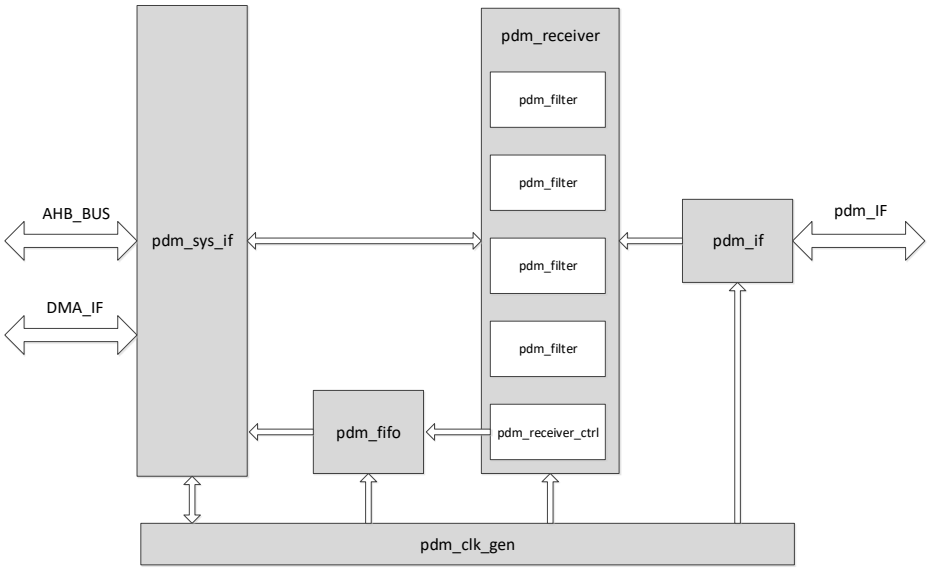

Fig. 31-1 PDM Block Diagram

System Interface
The system interface implements the APB slave operation. It contains not only control registers of receiver inside but also interrupt and DMA handshaking interface.
Receiver
The receiver can act as a decimation filter of PDM. And export PCM format data.
Receive FIFO
The Receive FIFO is the buffer to store received audio data. The size of the FIFO is 32bits x 128.
PDM interface
The PDM interface implements PDM bit streams receive operation.

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31.3 Function Description

31.3.1 AHB Interface

There is an AHB slave interface in PDM. It is responsible for accessing registers and internal memories.

31.3.2 PDM Interface

The PDM interface is a 5-wire interface. The PDM module can support up to four external stereo and eight digital microphones.

The following figures show two cases of use of the PDM, but all configurations are possible with stereo and mono digital microphones.

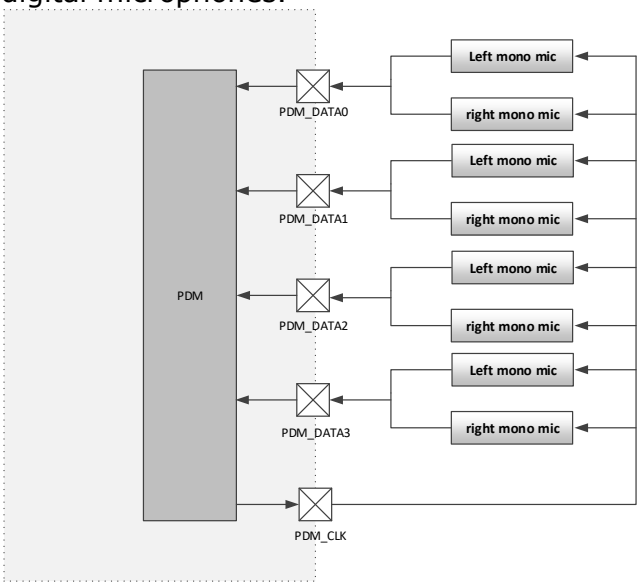

Fig. 31-2 PDM with Eight Mono MIC

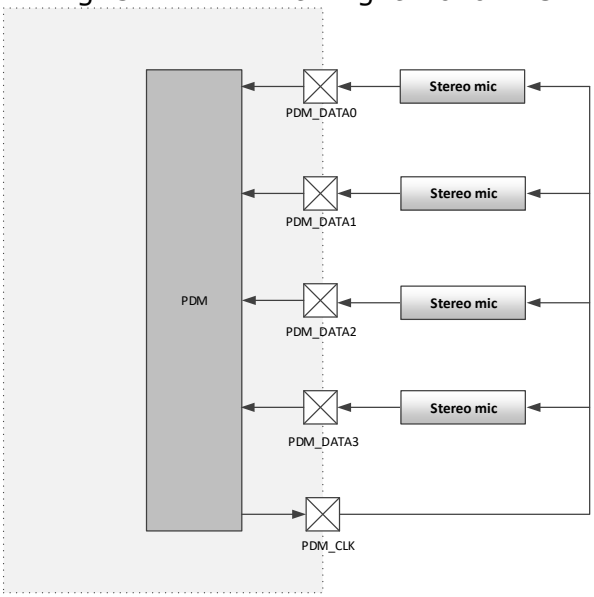

Fig. 31-3 PDM with Four Stereo MIC

The PDM interface consists of a serial-data shift clock output (PDM_CLK) and a serial data input (PDM_DATA). The clock is fanned out to both digital mics, and both digital mics' data (left channel and right channel) outputs share a single signal line. To share a single line, the digital mics tristate their output during one phase of the clock (high or low part of cycle, depending on how they are configured via their L/R input).

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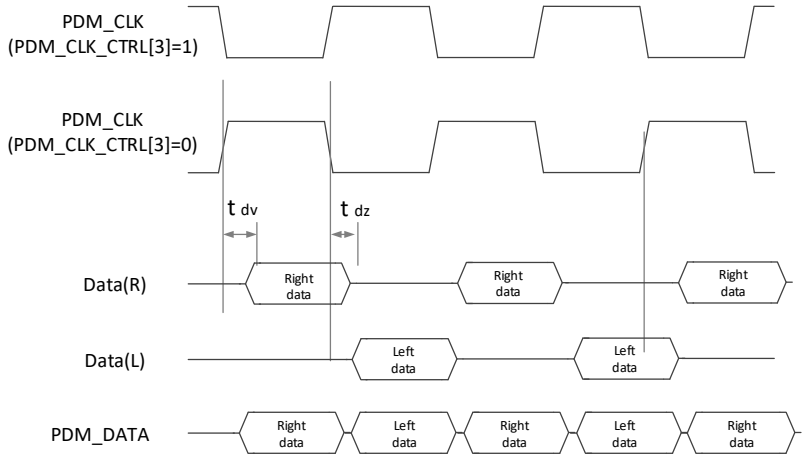

Fig. 31-4 PDM interface diagram with external MIC

31.3.3 Digital Filter

The external PDM generates a PDM stream of bits and transfers it in one period or one half-period of the clock provided by the PDM. The aim of the PDM is to process data from the PDM interface, decimate and filter the data, and store the processed data in the FIFO. The four paths are identical. Each path is composed of a left and a right channel. The PDM interface delivers eight parallel data of 1bit. Each bit goes to a filter. The aim of the filter is to limit the noise and export PCM format audio data.

31.3.4 Clock Configuration

MCLK is the source clock signal. PDM_CLK is the output clocks generated in the PDM and is fed to the external microphones. They are also the internal clock of the external microphones. User must take care about the value of PDM_CLK when selecting the source clock (MCLK).

Table 31-1 Relation between PDM_CLK and sample rate

PDM_CLK	Sample rate
3.072MHz	12KHz,24KHz,48KHz,96KHz,192KHz
2.8224MHz	11.025KHz,22.05KHz,44.1KHz,88.2KHz,176.4KHz
2.048MHz	8KHz,16KHz,32KHz,64KHz,128KHz

MCLK/PDM_CLK is more than 10;

31.4 Register Description

31.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

31.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
PDM_SYSCONFIG	0x0000	W	0x00000002	PDM System Configure Register
PDM_CTRL	0x0004	W	0x001C8797	PDM Control Register
PDM_FILTER_CTRL	0x0008	W	0x00000000	PDM Filter Control Register
PDM_FIFO_CTRL	0x000C	W	0x0003E000	PDM FIFO Control Register
PDM_DATA_VALID	0x0010	W	0x00000000	PDM Path Data Valid Register
PDM_RXFIFO_DATA_REG	0x0014	W	0x00000000	PDM Receive FIFO Data Register
PDM_DATA0R	0x0018	W	0x00000000	PDM Path 0 Right Channel Data Register
PDM_DATA0L	0x001C	W	0x00000000	PDM Path 0 Left Channel Data Register
PDM_DATA1R	0x0020	W	0x00000000	PDM Path 1 Right Channel Data Register
PDM_DATA1L	0x0024	W	0x00000000	PDM Path 1 Left Channel Data Register

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Name	Offset	Size	Reset Value	Description
PDM_DATA2R	0x0028	W	0x00000000	PDM Path 2 Right Channel Data Register
PDM_DATA2L	0x002C	W	0x00000000	PDM Path 2 Left Channel Data Register
PDM_DATA3R	0x0030	W	0x00000000	PDM Path 3 Right Channel Data Register
PDM_DATA3L	0x0034	W	0x00000000	PDM Path 3 Left Channel Data Register
PDM_VERSION	0x0038	W	0x24101126	PDM Version Register
PDM_GAIN_CTRL	0x003C	W	0x00000000	PDM Gain Control Register
PDM_DATA_SHIFT0	0x0040	W	0x00000000	PDM DATA Shift Register0
PDM_DATA_SHIFT1	0x0044	W	0x00000000	PDM DATA Shift Register1
PDM_FILTER_CTRL1	0x0048	W	0x00000000	PDM Filter Control Register1
PDM_INCR_RXDR	0x0400	W	0x00000000	Increment Address Receive FIFO Data Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

31.4.3 Detail Registers Description

PDM_SYSCONFIG

Address: Operational Base(0x404B0000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RW	0x0	dither_bypass 1'b0: data not for bypass 1'b1: data for bypass
12:5	RW	0x00	mute mute[0]: ch0 mute mute[1]: ch1 mute mute[2]: ch2 mute mute[3]: ch3 mute mute[4]: ch4 mute mute[5]: ch5 mute mute[6]: ch6 mute mute[7]: ch7 mute
4	RW	0x0	filter_gate_en Filter gate enable If some filters not work, the filter and its corresponding memory clock will be gated if filter_gate_en is 1'b1, otherwise the clock will be still active.
3	RW	0x0	num_start Software configuration enable bit. This bit only vaild data when num_start = 1'b1.
2	RW	0x0	rx_start RX transfer start bit 1'b0: Stop RX transfer 1'b1: Start RX transfer
1	RW	0x1	mem_gate_en 1'b1: Memory interface clock auto gating enable 1'b0: Memory interface clock auto gating disable

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Bit	Attr	Reset Value	Description
0	RW	0x0	rx_clr PDM RX logic clear This is a self-cleared bit. High active. Write 1'b1: Clear RX logic Write 1'b0: No action Read 1'b1: Clear ongoing Read 1'b0: Clear done

PDM_CTRL

Address: Operational Base(0x404B0000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:27	RW	0x0	path1_ch_sel Left and right channel data sel If path_mode_select = 2'b00 3'b000: path3 left (R ch) and path2 left (L ch) 3'b001: path3 right (R ch) and path2 left (L ch) 3'b010: path3 left (R ch) and path2 right (L ch) 3'b011: path3 right (R ch) and path2 right (L ch) 3'b100: path2 left (R ch) and path3 left (L ch) 3'b101: path2 right (R ch) and path3 left (L ch) 3'b110: path2 left (R ch) and path3 right (L ch) 3'b111: path2 right (R ch) and path3 right (L ch) If path_mode_select = 2'b01 3'b000: path3 left (R ch) and path1 left (L ch) 3'b001: path3 right (R ch) and path1 left (L ch) 3'b010: path3 left (R ch) and path1 right (L ch) 3'b011: path3 right (R ch) and path1 right (L ch) 3'b100: path1 left (R ch) and path3 left (L ch) 3'b101: path1 right (R ch) and path3 left (L ch) 3'b110: path1 left (R ch) and path3 right (L ch) 3'b111: path1 right (R ch) and path3 right (L ch) If path_mode_select = 2'b10 3'b000: path2 left (R ch) and path1 left (L ch) 3'b001: path2 right (R ch) and path1 left (L ch) 3'b010: path2 left (R ch) and path1 right (L ch) 3'b011: path2 right (R ch) and path1 right (L ch) 3'b100: path1 left (R ch) and path2 left (L ch) 3'b101: path1 right (R ch) and path2 left (L ch) 3'b110: path1 left (R ch) and path2 right (L ch) 3'b111: path1 right (R ch) and path2 right (L ch)

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Bit	Attr	Reset Value	Description
26:24	RW	0x0	path0_ch_sel Left and right channel data sel If path_mode_select = 2'b00 3'b000: path1 left (R ch) and path0 left (L ch) 3'b001: path1 right (R ch) and path0 left (L ch) 3'b010: path1 left (R ch) and path0 right (L ch) 3'b011: path1 right (R ch) and path0 right (L ch) 3'b100: path0 left (R ch) and path1 left (L ch) 3'b101: path0 right (R ch) and path1 left (L ch) 3'b110: path0 left (R ch) and path1 right (L ch) 3'b111: path0 right (R ch) and path1 right (L ch) If path_mode_select = 2'b01 3'b000: path2 left (R ch) and path0 left (L ch) 3'b001: path2 right (R ch) and path0 left (L ch) 3'b010: path2 left (R ch) and path0 right (L ch) 3'b011: path2 right (R ch) and path0 right (L ch) 3'b100: path0 left (R ch) and path2 left (L ch) 3'b101: path0 right (R ch) and path2 left (L ch) 3'b110: path0 left (R ch) and path2 right (L ch) 3'b111: path0 right (R ch) and path2 right (L ch) If path_mode_select = 2'b10 3'b000: path3 left (R ch) and path0 left (L ch) 3'b001: path3 right (R ch) and path0 left (L ch) 3'b010: path3 left (R ch) and path0 right (L ch) 3'b011: path3 right (R ch) and path0 right (L ch) 3'b100: path0 left (R ch) and path3 left (L ch) 3'b101: path0 right (R ch) and path3 left (L ch) 3'b110: path0 left (R ch) and path3 right (L ch) 3'b111: path0 right (R ch) and path3 right (L ch)
23:22	RW	0x0	path_mode_select path Select 2'b00: Path0 data and path1 data (path2 data and path3 data) 2'b01: Path0 data and path2 data (path1 data and path3 data) 2'b10: Path0 data and path3 data (path1 data and path2 data)
21	RW	0x0	split_en Split enable 1'b1: Enable 1'b0: Disable
20:19	RW	0x3	rx_path_select3 RX Path Select 2'b00: Path3 data from PDM data0 2'b01: Path3 data from PDM data1 2'b10: Path3 data from PDM data2 2'b11: Path3 data from PDM data3
18:17	RW	0x2	rx_path_select2 RX Path Select 2'b00: Path2 data from PDM data0 2'b01: Path2 data from PDM data1 2'b10: Path2 data from PDM data2 2'b11: Path2 data from PDM data3

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Bit	Attr	Reset Value	Description
16:15	RW	0x1	rx_path_select1 RX Path Select 2'b00: Path1 data from PDM data0 2'b01: Path1 data from PDM data1 2'b10: Path1 data from PDM data2 2'b11: Path1 data from PDM data3
14:13	RW	0x0	rx_path_select0 RX Path Select 2'b00: Path0 data from PDM data0 2'b01: Path0 data from PDM data1 2'b10: Path0 data from PDM data2 2'b11: Path0 data from PDM data3
12	RW	0x0	pdm_ch_ex Left and right channel data exchange 1'b0: Not inverted, if mono_path_en, the output path is the Left path. 1'b1: Inverted, if mono_path_en, the output path is the Right path.
11	RW	0x0	sjm_sel Store justified mode This bit can be written only when SYSCONFIG[2] is 0. 16bit~31bit DATA stored in 32 bits width FIFO. If VDW select 16bit data, this bit is valid only when HWT select 1. Because if HWT is 0, every FIFO unit contains two 16bit data and 32 bit space is full, it is impossible to choose justified mode. 1'b0: Right justified 1'b1: Left justified
10	RW	0x1	path3_en Path 3 enable 1'b1: Enable 1'b0: Disable
9	RW	0x1	path2_en Path 2 enable 1'b1: Enable 1'b0: Disable
8	RW	0x1	path1_en Path 1 enable 1'b1: Enable 1'b0: Disable
7	RW	0x1	path0_en Path 0 enable 1'b1: Enable 1'b0: Disable
6	RW	0x0	hwt_en Halfword word transform Only valid when VDW select 16bit data. 1'b0: 32 bit data valid to AHB/APB bus. Low 16 bit for left channel and high 16 bit for right channel. 1'b1: Low 16bit data valid to AHB/APB bus, high 16 bit data invalid.

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Bit	Attr	Reset Value	Description
5	RW	0x0	mono_path_enable Mono path enable bit. If mono path enable, path0/path1/path2/path3 only one path enable, and the right or left path depended on the lr_ch_ex reg. If data_vld_width cfg right/left data only 16bit, the data write to memory is combined by two data, {L1, L0} or {R1, R0}.
4:0	RW	0x17	data_vld_width Can be written only when SYSCONFIG[2] is 0. Valid Data width 0~14: Reserved 15: 16bit 16: 17bit 17: 18bit 18: 19bit ..... n: (n+1)bit 23: 24bit

PDM_FILTER_CTRL

Address: Operational Base(0x404B0000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:21	RW	0x0	hpf_ctrl High-pass filter configure 4'd0: 0.234Hz 4'd1: 0.468Hz 4'd2: 0.937Hz 4'd3: 1.875Hz 4'd4: 3.75Hz 4'd5: 7.5Hz 4'd6: 15Hz 4'd7: 30Hz 4'd8: 60Hz 4'd9: 122Hz 4'd10: 251Hz 4'd11: 528Hz 4'd12: 1183Hz 4'd13: 3152Hz 4'd14: 23999Hz 4'd15: high frequency
20	RW	0x0	hpf_ctrll High-pass filter enable for left channel 1'b0: High pass filter for left channel is disabled. 1'b1: High pass filter for left channel is enabled.
19	RW	0x0	hpf_ctrlr High-pass filter enable for right channel 1'b0: High pass filter for right channel is disabled. 1'b1: High pass filter for right channel is enabled.
18	RW	0x0	fir_com_bps FIR compensate filter bypass 1'b0: Not bypass 1'b1: Bypass

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Bit	Attr	Reset Value	Description
17	RW	0x0	sig_scale_mode Signal scale mode select 1'b0: CIC outputs the normal latitude. 1'b1: Scale the CIC outputs to half of the normal latitude and scale 2 times after hpf-filter.
16:10	RW	0x00	cic_scale CIC scale bits
9:1	RW	0x000	cic_value CIC filter extract value
0	RW	0x0	filter_en Contrl hb2 filter en 1'b0: Off 1'b1: On

PDM_FIFO_CTRL

Address: Operational Base(0x404B0000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RO	0x0	dma_status 1'b0: idle 1'b1: busy
27:20	RO	0x00	rfl Receive FIFO level Contains the number of valid data entries in the receive FIFO.
19:13	RW	0x1f	rdl Receive data level This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above this field value + 1.
12	RW	0x0	rde Receive DMA enable 1'b0: Receive DMA disabled 1'b1: Receive DMA enabled
11	RO	0x0	rxoi RX overflow interrupt 1'b0: Inactive 1'b1: Active
10	RO	0x0	rxfi RX full interrupt 1'b0: Inactive 1'b1: Active
9	RW	0x0	rxoic RX overflow interrupt clear (high active, auto clear).
8:2	RW	0x00	rft Receive FIFO threshold When the number of receive FIFO entries is more than or equal to this threshold plus 1, the receive FIFO threshold interrupt is triggered.

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Bit	Attr	Reset Value	Description
1	RW	0x0	rxoie RX overflow interrupt enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	rxftie RX full threshold interrupt enable 1'b0: Disable 1'b1: Enable

PDM_DATA_VALID

Address: Operational Base(0x404B0000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RC	0x0	path0_vld 1'b0: DATA0R_REG, DATA0L_REG value is invalid. 1'b1: DATA0R_REG, DATA0L_REG value is valid.
2	RC	0x0	path1_vld 1'b0: DATA1R_REG, DATA1L_REG value is invalid. 1'b1: DAT1R_REG, DATA1L_REG value is valid.
1	RC	0x0	path2_vld 1'b0: DATA2R_REG, DATA2L_REG value is invalid. 1'b1: DATA2R_REG, DATA2L_REG value is valid.
0	RC	0x0	path3_vld 1'b0: DATA3R_REG, DATA3L_REG value is invalid. 1'b1: DATA3R_REG, DATA3L_REG value is valid.

PDM_RXFIFO_DATA_REG

Address: Operational Base(0x404B0000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdr Receive FIFO shadow register When the register is read, data in the receive FIFO is accessed.

PDM_DATA0R

Address: Operational Base(0x404B0000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data0r Data of the path 0 right channel

PDM_DATA0L

Address: Operational Base(0x404B0000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data0l Data of the path 0 left channel

PDM_DATA1R

Address: Operational Base(0x404B0000) + offset (0x0020)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data1r Data of the path 1 right channel

PDM_DATA1L

Address: Operational Base(0x404B0000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data1l Data of the path 1 left channel

PDM_DATA2R

Address: Operational Base(0x404B0000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data2r Data of the path 2 right channel

PDM_DATA2L

Address: Operational Base(0x404B0000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data2l Data of the path 2 left channel

PDM_DATA3R

Address: Operational Base(0x404B0000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data3r Data of the path 3 right channel

PDM_DATA3L

Address: Operational Base(0x404B0000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	data3l Data of the path 3 left channel

PDM_VERSION

Address: Operational Base(0x404B0000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RO	0x24101126	ver PDM version

PDM_GAIN_CTRL

Address: Operational Base(0x404B0000) + offset (0x003C)

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	gain_ctrl3 0: -65.625dB 1: -65.25dB .... 175: 0dB 255: 30dB step:0.375dB
23:16	RW	0x00	gain_ctrl2 0: -65.625dB 1: -65.25dB .... 175: 0dB 255: 30dB step:0.375dB
15:8	RW	0x00	gain_ctrl1 0: -65.625dB 1: -65.25dB .... 175: 0dB 255: 30dB step:0.375dB
7:0	RW	0x00	gain_ctrl0 0: -65.625dB 1: -65.25dB .... 175: 0dB 255: 30dB step:0.375dB

PDM_DATA_SHIFT0

Address: Operational Base(0x404B0000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	right_data1_shift 0: no shift ... 255: shift 255 cycle
23:16	RW	0x00	left_data1_shift 0: no shift ... 255: shift 255 cycle
15:8	RW	0x00	right_data0_shift 0: no shift ... 255: shift 255 cycle
7:0	RW	0x00	left_data0_shift 0: no shift ... 255: shift 255 cycle

PDM_DATA_SHIFT1

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Address: Operational Base(0x404B0000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	right_data3_shift 0: no shift ... 255: shift 255 cycle
23:16	RW	0x00	left_data3_shift 0: no shift ... 255: shift 255 cycle
15:8	RW	0x00	right_data2_shift 0: no shift ... 255: shift 255 cycle
7:0	RW	0x00	left_data2_shift 0: no shift ... 255: shift 255 cycle

PDM_FILTER_CTRL1

Address: Operational Base(0x404B0000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:2	RW	0x0	hpf_ctrl High-pass filter configure 4'd0: 0.234Hz 4'd1: 0.468Hz 4'd2: 0.937Hz 4'd3: 1.875Hz 4'd4: 3.75Hz 4'd5: 7.5Hz 4'd6: 15Hz 4'd7: 30Hz 4'd8: 60Hz 4'd9: 122Hz 4'd10: 251Hz 4'd11: 528Hz 4'd12: 1183Hz 4'd13: 3152Hz 4'd14: 23999Hz 4'd15: high frequency
1	RW	0x0	hpf_ctrlr High-pass filter enable for right channel 1'b0: High pass filter for right channel is disabled. 1'b1: High pass filter for right channel is enabled.
0	RW	0x0	hpf_ctrll High-pass filter enable for left channel 1'b0: High pass filter for left channel is disabled. 1'b1: High pass filter for left channel is enabled.

PDM_INCR_RXDR

Address: Operational Base(0x404B0000) + offset (0x0400)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	receive_fifo_data FIFO data can be read from these registers. This register is used when the access address is increment.

31.5 Interface Description

The following table shows the PDM interface description.

Table 31-2 PDM mux0 Interface Description

Module Pin	Direction	Rockchip IO	IOMUX Setting
O_pdm_clk(0) _m0	O	I2C4_SDA_M3/PDM_CLK0_M0/UART2_CTSN_M1/GPIO7_A4	GPIO7A_IOMUX_SEL_1 [3:0]=3
O_pdm_clk(1) _m0	O	I2C4_SCL_M3/PDM_CLK1_M0/PWM2_CH5_M1/GPIO7_A1	GPIO7A_IOMUX_SEL_0 [7:4]=3
I_pdm_data0_m0	I	SAI0_SDI0_M0/PDM_SDI0_M0/GPIO7_A6	GPIO7A_IOMUX_SEL_1 [11:8]=3
I_pdm_data1_m0	I	SAI0_SDI1_M0/SAI0_SDO3_M0/PDM_SDI1_M0/DSM_AUD_RP/I2C1_SDA_M3/UART2_TX_M1/GPIO7_B1	GPIO7A_IOMUX_SEL_0 [7:4]=3
I_pdm_data2_m0	I	SAI0_SDI2_M0/SAI0_SDO2_M0/PDM_SDI2_M0/DSM_AUD_RN/I2C1_SCL_M3/UART2_RX_M1/GPIO7_B0	GPIO7A_IOMUX_SEL_0 [3:0]=3
I_pdm_data3_m0	I	SAI0_SDI3_M0/SAI0_SDO1_M0/PDM_SDI3_M0/UART2_RTSN_M1/GPIO7_A7	GPIO7A_IOMUX_SEL_1 [15:12]=3

Table 31-3 PDM mux1 Interface Description

Module Pin	Direction	Rockchip IO	IOMUX Setting
O_pdm_clk(0) _m1	O	VI_CIF_D12_M0/ETH_MCLK_M0/SPI1_CLK_M0/PDM_CLK0_M1/UART7_TX_M1/GPIO6_B4	GPIO6B_IOMUX_SEL_1 [3:0]=5
O_pdm_clk(1) _m1	O	VI_CIF_D15_M0/ETH_MDIO_M0/ETH_TESTRXD_OUT_M1/PDM_CLK1_M1/UART7_CTSN_M1/GPIO6_B7	GPIO6B_IOMUX_SEL_1 [15:12]=5
I_pdm_data0_m1	I	VI_CIF_D13_M0/ETH_RXCTL_M0/PDM_SDI0_M1/UART7_RX_M1/GPIO6_B5	GPIO6B_IOMUX_SEL_1 [7:4]=5
I_pdm_data1_m1	I	VI_CIF_D14_M0/PDM_SDI1_M1/UART7_RTSN_M1/GPIO6_B6	GPIO6B_IOMUX_SEL_1 [11:8]=5
I_pdm_data2_m1	I	VI_CIF_D10_M0/ETH_RXD0_M0/SPI1_MOSI_M0/PDM_SDI2_M1/UART6_RTSN_M1/GPIO6_B2	GPIO6B_IOMUX_SEL_0 [11:8]=5
I_pdm_data3_m1	I	VI_CIF_D11_M0/ETH_RXD1_M0/SPI1_MISO_M0/PDM_SDI3_M1/UART6_CTSN_M1/GPIO6_B3	GPIO6B_IOMUX_SEL_0 [15:12]=5

Notes: I=input, O=output, I/O=input/output. For the configuration of RM_IO, please refer to chapter "Rockchip Matrix IO".

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31.6 Application Notes

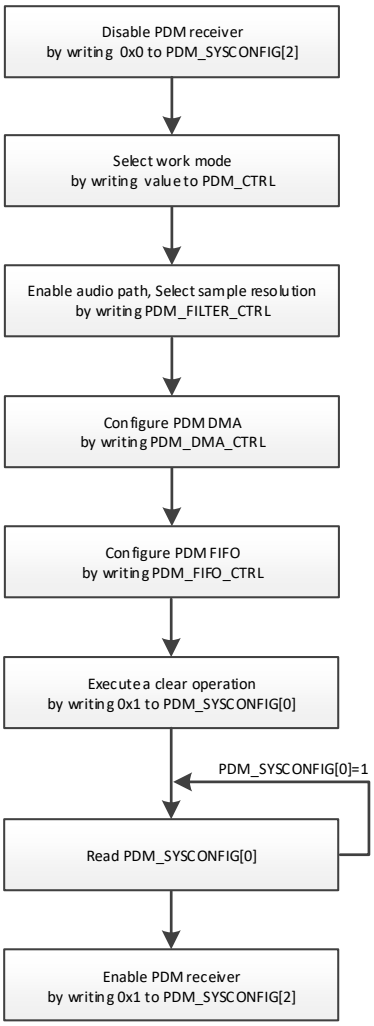

Fig. 31-5 PDM operation flow

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Chapter 32 Asynchronous Sample Rate Converter (ASRC)

32.1 Overview

ASRC converts digital audio data from one sample frequency to another. The input sample frequency can be an arbitrary fraction of the output frequency or the same frequency, but based on different clock sources. ASRC fetches audio data through AHB bus and acts as an intermediary for audio interfaces such as SAI, PDM etc. With the help of ASRC, we can connect audio components with the embedded SOC platform together and provide an audio interface solution for the system.

32.1.1 Features

- Support two 2-channel ASRC0/1
- Support series mode which combines adjacent ASRC (ASRC0~1) into maximum 4-channel
- Support one 32-bit AHB-Lite bus slave interface
- Support DMA handshaking interface and configurable DMA water level
- Support up to 2-channel with same ratio for ASRC0/1
- Support sample rate and resample rate range from 8 to 384KHz, mainly include three typical rate groups:

1) 8KHz, 16KHz, 32KHz, 64KHz, 128KHz
2) 12KHz, 24KHz, 48KHz, 96KHz, 192KHz, 384KHz
3) 11.025KHz, 22.05KHz, 44.1KHz, 88.2KHz, 176.4KHz, 352.8KHz

- Support up-conversion, down-conversion, and 1:1 asynchronous conversion
- Support conversion ratio ranging from 1:8 (down) to 8:1 (up) with 22-bit resolution
- Support low deterministic latency related to ratio
- Support hard mute and soft mute
- Support output dither to reduce harmonic component
- Support typical THD+N -130dB (range from -120dB to -140dB)
- Support real-time transmission mode, which transmits or receives audio data from either audio component or memory with ratio tracking
- Support memory fetch mode, which transmits or receives audio data from memory with manual ratio without tracking
- Support input/output 16/20/24-bit wide audio data transfer, width unaligned conversion is supported
- Support two 16-bit audio data store together in one 32-bit wide location
- Support audio data left or right justified in 32-bit wide FIFO
- Support half channels internal 48-bit wide and 16-location deep FIFOs for transmitting, and half channels 48-bit wide and 64-location deep FIFOs for receiving audio data
- Support fixed and incremental address access to transmit and receive FIFOs
- Support ratio_init/update_done, asrc_out_start, conv_done/error, fifo_in_empty/full, fifo_out_empty/full, ratio/src_lrck/dst_lrck_unlock interrupt, which can be masked
- Support combined interrupt output

32.2 Block Diagram

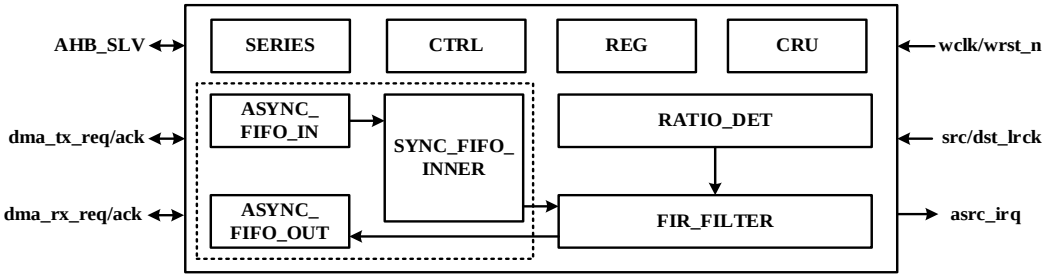

Fig. 32-1 ASRC Block Diagram

System Interface

System interface implements the interactions with SOC platform. It contains not only AHB slave interface which controls registers and audio data transfer, but also LRCK interface,

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DMA handshaking interface and interrupt interface.

Clock Reset Unit (CRU)

Clock reset unit implements inner clock and reset management. The main function is clock frequency divide, the source clock of the divider block are src_lrck and dst_lrck, and by the divider, it generates clocks with the same frequency as sample rate or resample rate.

Register Block (REG)

Register block is responsible for the main ASRC functionality including control, status and interrupt generation.

Controller Block (CTRL)

Controller block is the main control block of variable sampling filter, its main functions include filtering output judgment, coefficient position calculation and interpolation filtering.

Ratio Detector Block (RATIO_DET)

The main function of ratio detector block is to initialize and track ratio related parameters. In the initialization stage, related parameters is fetched directly from register configuration. Then in the tracking stage, ratio tracking is realized through periodic detection of src_lrck and dst_lrck. In the meantime, the water level of output FIFO is monitored for negative feedback adjustment.

FIR Block (FIR_FILTER)

FIR block acts as a poly-phase filter, which interpolates the correct phase and applies the calculated filter coefficients to the set of input samples to form an output sample.

Inner FIFO Block (SYNC_FIFO_INNER)

Inner FIFO block is the buffer to store audio data for FIR Filter. The size is 48bits x 512 and the number is half channels.

Input FIFO Block (ASYNC_FIFO_IN)

Input FIFO block is the buffer to store received audio data. The size is 48bits x 16 and the number is half channels.

Output FIFO Block (ASYNC_FIFO_OUT)

Output FIFO block is the buffer to store transmitted audio data. The size is 48bits x 64 and the number is half channels.

Series Block (SERIES)

Series block implements the interactions with other ASRCs in the SOC platform.

32.3 Function Description

Firstly, we define two basic modes of ASRC, memory fetch mode and real-time transmission mode. Then to enhance throughput, we define an enhancement mode called series mode, which can combine adjacent ASRCs together.

32.3.1 Memory Fetch Mode

In memory fetch mode, ASRC is working based on manual ratio, ratio tracking is disabled, so src_lrck or dst_lrck is unused. ASRC acts as peripheral when transmitting or receiving audio data from memory, so both dma_tx_req and dma_rx_req are started by ASRC. The faster the frequency of working clock, the faster the conversion will be completed.

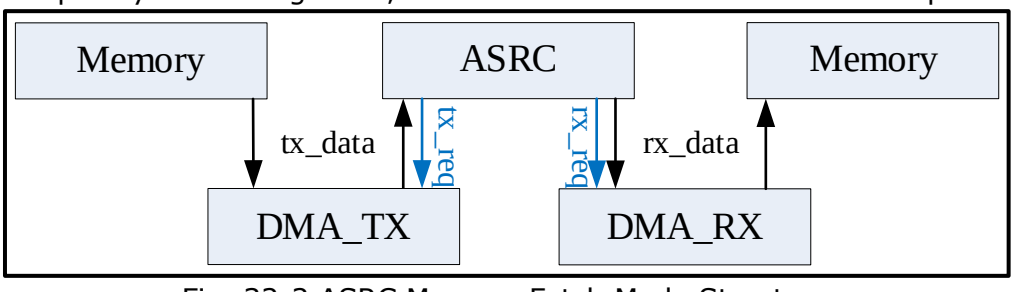

Fig. 32-2 ASRC Memory Fetch Mode Structure

Based on memory fetch mode, we extends a new sub-pattern called loop mode. With loop mode, multiple discrete audio files can be converted by only one configuration, or one continuous audio files can be split into multiple parts and converted by one configuration. The most significant application of loop mode is to convert more channel real-time audio data than ASRC defined by time division multiplexing. Audio data in the middle part of file should be recalled additionally for continuous output.

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32.3.2 Real-time Transmission Mode

In real-time transmission mode, ASRC is working based on both manual ratio and tracking ratio, ratio tracking is enabled, so src_lrck or dst_lrck is needed. The faster the frequency of working clock, the more precise the tracking will be completed. Real-time transmission mode can be divided into four sub-patterns based on the component types at the source and destination ends, called MEM2MEM, MEM2DST, SRC2MEM and SRC2DST for short.

- **MEM2MEM**

In MEM2MEM mode, memory serves as both source and destination component. ASRC acts as peripheral when receiving audio data from memory or transmitting audio data to memory. Hence, both dma_tx_req and dma_rx_req are started by ASRC. Besides, both src_lrck and dst_lrck originate from CRU.

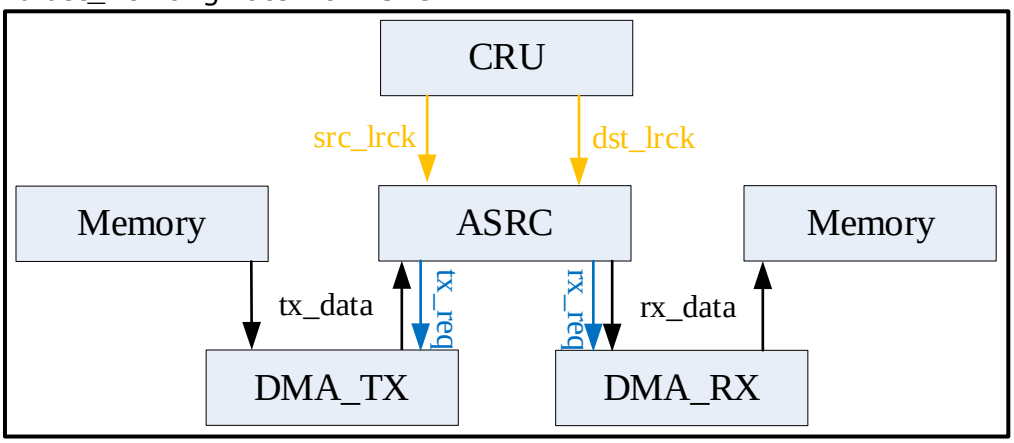

Fig. 32-3 ASRC MEM2MEM Mode Structure

- **MEM2DST**

In MEM2DST mode, memory serves as source component, and audio component serves as destination component. ASRC acts as peripheral when receiving audio data from memory, but as memory when transmitting audio data to peripheral. Hence, dma_tx_req is started by ASRC, but dma_rx_req is started by audio component. Besides, src_lrck originates from CRU, but dst_lrck originates from audio component.

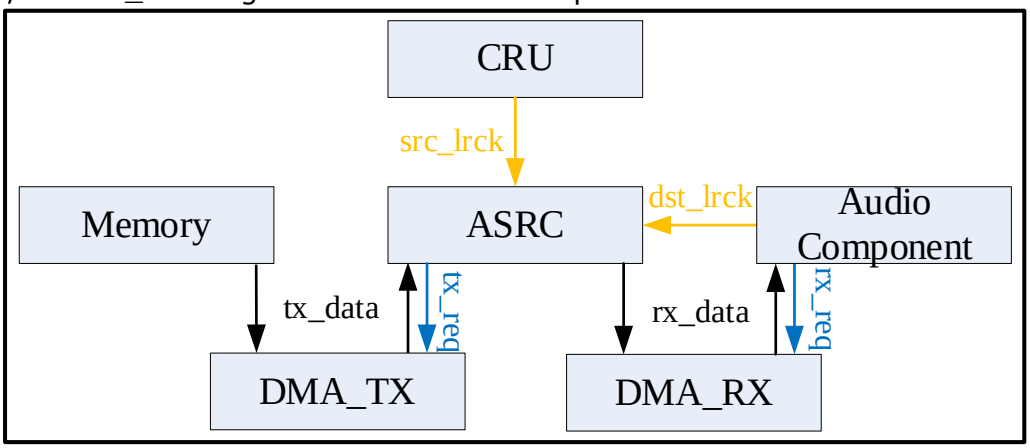

Fig. 32-4 ASRC MEM2DST Mode Structure

- **SRC2MEM**

In SRC2MEM mode, audio component serves as source component, and memory serves as destination component. ASRC acts as memory when receiving audio data from audio component, but as peripheral when transmitting audio data to memory. Hence, dma_tx_req is started by audio component, but dma_rx_req is started by ASRC. Besides, src_lrck originates from audio component, but dst_lrck originates from CRU.

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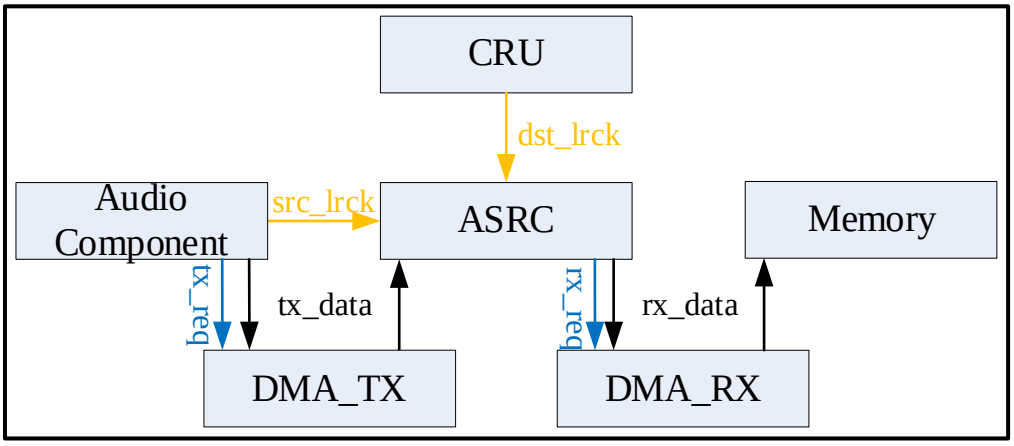

Fig. 32-5 ASRC SRC2MEM Mode Structure

- **SRC2DST**

In SRC2DST mode, audio component serves as both source component and destination component. ASRC acts as memory when receiving audio data from audio component or transmitting audio data to audio component. Hence, both dma_tx_req and dma_rx_req are started by audio component. Besides, both src_lrck and dst_lrck originate from audio component.

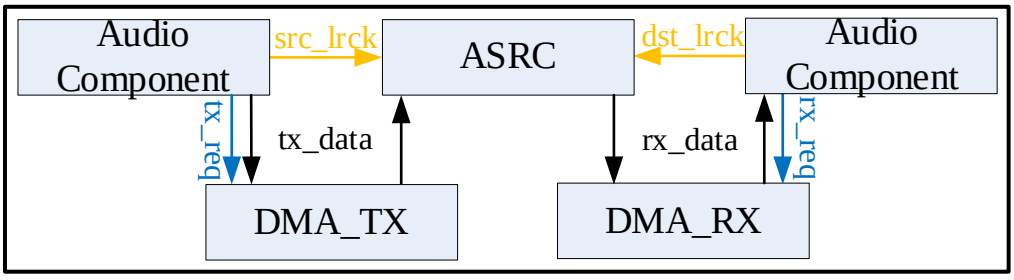

Fig. 32-6 ASRC SRC2DST Mode Structure

32.3.3 Series Mode

In series mode, adjacent ASRCs can be combined together to enhance throughput. We can appoint the ASRC at the front as master and other ASRCs as slave. All combined ASRCs can be viewed as a whole and interact with the outside world using the interface of master only. We can take MEM2MEM series mode as an example in the following figure. Note, the letter M stands for master and the letter S stands for slave.

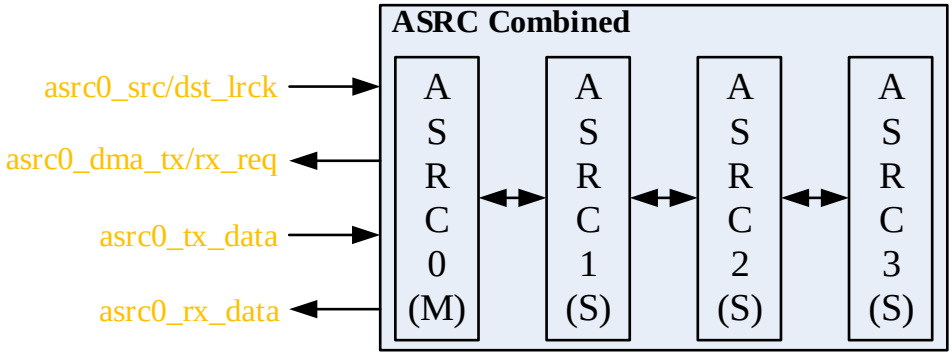

Fig. 32-7 ASRC MEM2MEM Series Mode Structure

In RV1126B, ASRC in the same audio wrapper can be combined together, which means that ASRC0/1 can be combined together into maximum 4-channel.

32.3.4 ASRC Latency

In real-time transmission mode, the latency of ASRC is determined by the phase delay of the FIR filter and fill level of the FIFO. For any given configuration and ratio, the latency of ASRC is fixed as follow:

Latency = phase delay + FIFO delay

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Where phase delay equals 32 input sample periods when ratio is not more than one, or equals (32*ratio) input sample periods otherwise. FIFO delay equals (asrc_in_thresh+1) input sample periods plus (asrc_out_thresh+1) output sample periods.
In memory fetch mode, the conversion will be completed as fast as possible according to working clock only, regardless of src_lrck and dst_lrck, the latency can be ignored.

32.4 Register Description

32.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
ASRC0 base address	0x209B0000
ASRC1 base address	0x209C0000

32.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
ASRC_VERSION	0x0000	W	0x01020000	Version register
ASRC_ASRC_CON	0x0004	W	0x00680030	ASRC control register
ASRC_CLKDIV_CON	0x0008	W	0x00000000	LRCK divider control register
ASRC_DATA_FMT	0x000C	W	0x00000000	Data format register
ASRC_LOOP_CON0	0x0010	W	0x00000000	Loop control register 0
ASRC_LOOP_CON1	0x0014	W	0x00000000	Loop control register 1
ASRC_LOOP_CON2	0x0018	W	0x00000000	Loop control register 2
ASRC_MANUAL_RATIO	0x0020	W	0x00000000	Manual ratio register
ASRC_SAMPLE_RATE	0x0024	W	0x0002EE00	Sample rate register
ASRC_RESAMPLE_RATE	0x0028	W	0x0002EE00	Resample rate register
ASRC_TRACK_PERIOD	0x002C	W	0x000003FF	Track period register
ASRC_RATIO_MARGIN	0x0030	W	0x003FFFFF	Ratio margin register
ASRC_LRCK_MARGIN	0x0034	W	0x007F007F	LRCK margin register
ASRC_TRACK_BIAS	0x0038	W	0x00010002	Track bias register
ASRC_FETCH_LEN	0x0040	W	0x3F000000	Fetch length register
ASRC_DMA_THRESH	0x0050	W	0xEC40B333	DMA thresh register
ASRC_LRCK_THRESH	0x0054	W	0x00000001	LRCK thresh register
ASRC_LRCK_FILT	0x0058	W	0x807F007F	LRCK filter register
ASRC_INT_CON	0x0060	W	0x00000000	Interrupt control register
ASRC_INT_ST	0x0064	W	0x00000000	Interrupt status register
ASRC_ASRC_ST0	0x0070	W	0x00000000	ASRC status register 0
ASRC_ASRC_ST1	0x0074	W	0x00000000	ASRC status register 1
ASRC_RATIO_ST	0x0080	W	0x00000000	Ratio status register
ASRC_RESAMPLE_RATE_ST	0x0084	W	0x00000000	Resample rate status register
ASRC_THETA_CNT_ST	0x0090	W	0x00000000	Theta counter status register
ASRC_DECI_THETA_ACC_ST	0x0094	W	0x00000000	Decimal theta accumulator status register
ASRC_FIFO_IN_WRCNT	0x00A0	W	0x00000000	Input FIFO write counter register

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Name	Offset	Size	Reset Value	Description
ASRC_FIFO_IN_RDCNT	0x00A4	W	0x00000000	Input FIFO read counter register
ASRC_FIFO_OUT_WRCNT	0x00B0	W	0x00000000	Output FIFO write counter register
ASRC_FIFO_OUT_RDCNT	0x00B4	W	0x00000000	Output FIFO read counter register
ASRC_FIFO_IN_FIXED_DR	0x00C0	W	0x00000000	Input FIFO fixed address data register
ASRC_FIFO_OUT_FIXED_DR	0x00C4	W	0x00000000	Output FIFO fixed address data register
ASRC_FIFO_IN_INCR_DR	0x1000	W	0x00000000	Input FIFO increment address data register
ASRC_FIFO_OUT_INCR_DR	00	W	0x00000000	Output FIFO increment address data register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

32.4.3 Detail Registers Description

ASRC_VERSION

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RO	0x01020000	version ASRC version number.

ASRC_ASRC_CON

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	soft_mute_en Soft mute enable. Each lane is controlled independently, bit 0~3 is corresponding to lane 0~3. 1'b0: Disable 1'b1: Enable
27:24	RW	0x0	hard_mute_en Hard mute enable. Each lane is controlled independently, bit 0~3 is corresponding to lane 0~3. 1'b0: Disable 1'b1: Enable
23	RW	0x0	dither_en Dither enable. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
22	RW	0x1	clk_gating_en ASRC clock auto gating enable. 1'b0: Disable 1'b1: Enable
21:20	RW	0x2	ratio_filt_win Ratio filter sliding window select. 2'b00: window width 2 2'b01: window width 4 2'b10: window width 8 2'b11: window width 16
19	RW	0x1	ratio_track_mode Ratio track mode select. 1'b0: Update src_lrck_cnt and dst_lrck_cnt once track period reached 1'b1: Update src_lrck_cnt and dst_lrck_cnt only when track period reached and the value change by more than bias_lrck_step from the previous value
18	RW	0x0	ratio_exc_dis Ratio exceed detect disable. 1'b0: Disable 1'b1: Enable
17	RW	0x0	ratio_filt_dis Ratio track filter disable. This bit works only when ratio_track_dis equal 0. 1'b0: Disable 1'b1: Enable
16	RW	0x0	ratio_track_dis Ratio track disable. 1'b0: Disable 1'b1: Enable
15	RW	0x0	series_rx_apart ASRC series enable but use respective rx request.
14	RW	0x0	series_tx_apart ASRC series enable but use respective tx request.
13:12	RW	0x0	series_en ASRC series enable. 2'b00: series disable 2'b01: serve as series master 2'b10: serve as series slave
11	RW	0x0	series_post_end ASRC series post end flag. This bit works only when asrc_mode equal 1.
10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9	RW	0x0	asrc_out_stop ASRC stop transmitting data to destination component. This bit works only when asrc_mode equal 0. 1'b0: Disable 1'b1: Enable
8	RW	0x0	asrc_in_stop ASRC stop receiving data from source component. This bit works only when asrc_mode equal 0. 1'b0: Disable 1'b1: Enable
7	RO	0x0	reserved
6	RW	0x0	unlock_rst_en ASRC unlock reset enable. Once enable, ASRC auto clear and restart when src_lrck_unlock, dst_lrck_unlock or ratio_unlock happen. 1'b0: Disable 1'b1: Enable
5:4	RW	0x3	chan_num Channel number select. 2'b00: 2 channel used 2'b01: 4 channel used 2'b10: 6 channel used 2'b11: 8 channel used
3:2	RW	0x0	real_time_mode Real-time transmission mode select. This bit works only when asrc_mode equal 0. 2'b00: Memory as both source and destination component 2'b01: Peripheral as source component, Memory as destination component 2'b10: Memory as source component, Peripheral as destination component 2'b11: Peripheral as both source and destination component
1	RW	0x0	asrc_mode ASRC mode select. 1'b0: Real-time transmission mode 1'b1: Memory fetch mode
0	RW	0x0	asrc_en ASRC enable. 1'b0: Disable 1'b1: Enable In loop mode, this bit must be set after loop_en. When asrc_en equal 0, FIFOs in ASRC are self-cleared.

ASRC_CLKDIV_CON

Address: Operational Base + offset (0x0008)

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Bit	Attr	Reset Value	Description
31	RW	0x0	dst_lrck_div_en dst_lrck divider enable. 1'b0: Disable 1'b1: Enable
30:16	RW	0x0000	dst_lrck_div_con dst_lrck divider. dst_lrck_div_con=Fdst_lrck/resample_rate-1.
15	RW	0x0	src_lrck_div_en src_lrck divider enable. 1'b0: Disable 1'b1: Enable
14:0	RW	0x0000	src_lrck_div_con src_lrck divider. src_lrck_div_con=Fsrc_lrck/sample_rate-1.

ASRC_DATA_FMT

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	OSJM Output data store justified mode, which indicate LSB of output data.
23:21	RO	0x0	reserved
20:16	RW	0x00	ISJM Input data store justified mode, which indicate LSB of input data.
15:13	RO	0x0	reserved
12	RW	0x0	OFMT Output data format. 1'b0: low bits data valid to AHB bus, high bits data invalid. 1'b1: 32 bit data valid to AHB bus. Low 16 bit for left channel and high 16 bit for right channel.
11:9	RO	0x0	reserved
8	RW	0x0	IFMT Input data format. 1'b0: low bits data valid from AHB bus, high bits data invalid. 1'b1: 32 bit data valid from AHB bus. Low 16 bit for left channel and high 16 bit for right channel.
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:4	RW	0x0	OWL Output data bit wide. 3'b000: Input 24 bits, Output 24 bits 3'b001: Input 20 bits, Output 20 bits 3'b010: Input 16 bits, Output 16 bits 3'b011: Input 24 bits, Output 16 bits 3'b100: Input 20 bits, Output 16 bits 3'b101: Input 24 bits, Output 20 bits Others: Reserved
3:2	RO	0x0	reserved
1:0	RW	0x0	IWL Input data bit wide. 2'b00: 24 bits 2'b01: 20 bits 2'b10: 16 bits 2'b01: Reserved

ASRC_LOOP_CON0

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	loop_end_con Loop end mode. Each loop is controlled independently, bit 0~7 is corresponding to loop time 0~7. 1'b0: Convert the end part of a file 1'b1: Not convert the end part of a file
7:0	R/WSC	0x00	loop_start_con Loop start mode. Each loop is controlled independently, bit 0~7 is corresponding to loop time 0~7. 1'b0: Convert the start part of a file 1'b1: Not convert the start part of a file

ASRC_LOOP_CON1

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:8	RW	0x0	chan_times Channel times, which means the actual channel to be converted is (chan_times+1) much as (chan_num+1).
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:4	RW	0x0	loop_times Loop times, which means (loop_times+1) conversion is done continuously.
3:1	RO	0x0	reserved
0	R/WSC	0x0	loop_en ASRC loop enable. This bit is automatically cleared when loop conversion done. 1'b0: Disable 1'b1: Enable

ASRC_LOOP_CON2

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	R/WSC	0x0000	loop_gap_thresh ASRC loop gap thresh, which sets the interval between two conversion.

ASRC_MANUAL_RATIO

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:0	RW	0x0000000	manual_ratio Manual ratio with fixed-point 26Q22. High 4 bits shows integer part, low 22 bits shows decimal part. manual_ratio=sample_rate/resample_rate.

ASRC_SAMPLE_RATE

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RW	0x2ee00	sample_rate Sample rate ranges from 8KHz to 384KHz.

ASRC_RESAMPLE_RATE

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RW	0x2ee00	resample_rate Resample rate ranges from 8KHz to 384KHz.

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ASRC_TRACK_PERIOD

Address: Operational Base + offset (0x002C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	ratio_track_div Ratio track divider, which scale down the frequency of src_lrck and dst_lrck for higher precision of ratio tracking.
15:12	RO	0x0	reserved
11:0	RW	0x3ff	ratio_track_period Ratio track period, which means tracking information updates every (ratio_track_period+1)*(ratio_track_div+1) clock.

ASRC_RATIO_MARGIN

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RW	0x3fffff	ratio_margin Ratio margin with fixed-point 22Q22, which shows decimal part of ratio. Ratio unlock occurs when the difference between ratio_st and manual_ratio exceeds ratio_margin.

ASRC_LRCK_MARGIN

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31	RW	0x0	dst_lrck_margin_dis Dst_lrck drift detect disable. 1'b0: Disable 1'b1: Enable
30:16	RW	0x007f	dst_lrck_margin Dst_lrck drift margin. Dst_lrck unlock occurs when the variation of dst_lrck exceeds dst_lrck_margin.
15	RW	0x0	src_lrck_margin_dis Src_lrck drift detect disable. 1'b0: Disable 1'b1: Enable
14:0	RW	0x007f	src_lrck_margin Src_lrck drift margin. Src_lrck unlock occurs when the variation of src_lrck exceeds src_lrck_margin.

ASRC_TRACK_BIAS

Address: Operational Base + offset (0x0038)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x01	bias_ratio_step Bias ratio step. These bits works only when ratio_exc_dis equal 1.
15:8	RO	0x00	reserved
7:0	RW	0x02	bias_lrck_step Bias LRCK step. These bits works only when ratio_track_mode equal 1.

ASRC_FETCH_LEN

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:24	RW	0x3f	mem_fetch_ext_cnt Memory fetch extend counter, is used only when asrc_mode equal 1. It extends the interval of filter operation, which works only when series_en not equal 0.
23:20	RO	0x0	reserved
19:0	RW	0x00000	fetch_length Memory fetch length, is used only when asrc_mode equal 1. It indicates the number of input data per channel. As input data is written by AHB bus in word, if the number written is called INPUT_WORD_NUM, the equation is as follows: fetch_length=INPUT_WORD_NUM*(IFMT+1)/(2*(chan_num+1))

ASRC_DMA_THRESH

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:26	RW	0x3b	asrc_pos_thresh Output FIFO positive thresh, unit channel_num. Exceed positive occurs once the number of valid data entries in the output FIFO is above this field value. Note, asrc_pos_thresh had better be higher than 59.
25:20	RW	0x04	asrc_neg_thresh Output FIFO negative thresh, unit channel_num. Exceed negative occurs once the number of valid data entries in the output FIFO is below this field value. Note, asrc_neg_thresh had better be lower than 4.
19:18	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
17:12	RW	0x0b	asrc_out_thresh ASRC start output thresh, unit channel_num. Output will start once the number of valid data entries in the output FIFO is above this field value. Note, asrc_out_thresh must be higher than dma_rx_thresh.
11:8	RW	0x3	asrc_in_thresh ASRC start conversion thresh, unit channel_num. Conversion will start once the number of valid data entries in the input FIFO is above this field value. Note, asrc_in_thresh must be no more than dma_tx_thresh.
7:4	RW	0x3	dma_rx_thresh DMA rx request thresh, unit channel_num. The watermark level = dma_rx_thresh+1; that is, dma_rx_req is generated when the number of valid data entries in the output FIFO is equal to or above this field value + 1.
3:0	RW	0x3	dma_tx_thresh DMA tx request thresh, unit channel_num. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the input FIFO is equal to or below this field value.

ASRC_LRCK_THRESH

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x001	lrck_thresh Src_lrck thresh, is used to waiting for src_lrck ready.

ASRC_LRCK_FILT

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31	RW	0x1	lrck_filt_en Lrck filt enable. 1'b0: Disable 1'b1: Enable
30:16	RW	0x007f	lrck_spur_margin Lrck spur margin. Lrck unstable occurs when the toggle of lrck within lrck_spur_margin.
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14:0	RW	0x007f	lrck_drift_margin Lrck drift margin. Lrck unstable occurs when the variation of lrck exceeds lrck_drift_margin.

ASRC_INT_CON

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	RW	0x0	dst_lrck_unlock_en Enable dst_lrck unlock interrupt. 1'b0: Disable 1'b1: Enable
11	RW	0x0	src_lrck_unlock_en Enable src_lrck unlock interrupt. 1'b0: Disable 1'b1: Enable
10	RW	0x0	ratio_unlock_en Enable ratio unlock interrupt. 1'b0: Disable 1'b1: Enable
9	RW	0x0	fifo_out_empty_en Enable output FIFO empty interrupt. 1'b0: Disable 1'b1: Enable
8	RW	0x0	fifo_out_full_en Enable output FIFO full interrupt. 1'b0: Disable 1'b1: Enable
7	RW	0x0	fifo_in_empty_en Enable input FIFO empty interrupt. 1'b0: Disable 1'b1: Enable
6	RW	0x0	fifo_in_full_en Enable input FIFO full interrupt. 1'b0: Disable 1'b1: Enable
5	RW	0x0	ratio_update_done_en Enable ratio update done interrupt. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
4	RW	0x0	ratio_change_done_en Enable ratio change done interrupt. 1'b0: Disable 1'b1: Enable
3	RW	0x0	ratio_init_done_en Enable ratio initial done interrupt. 1'b0: Disable 1'b1: Enable
2	RW	0x0	conv_error_en Enable conversion error interrupt. 1'b0: Disable 1'b1: Enable
1	RW	0x0	conv_done_en Enable conversion done interrupt. 1'b0: Disable 1'b1: Enable
0	RW	0x0	asrc_out_start_en Enable ASRC output start interrupt. 1'b0: Disable 1'b1: Enable

ASRC_INT_ST

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12	W1C	0x0	dst_lrck_unlock_st Dst_lrck unlock interrupt status.
11	W1C	0x0	src_lrck_unlock_st Src_lrck unlock interrupt status.
10	W1C	0x0	ratio_unlock_st Ratio unlock interrupt status.
9	W1C	0x0	fifo_out_empty_st Output FIFO empty interrupt status.
8	W1C	0x0	fifo_out_full_st Output FIFO full interrupt status.
7	W1C	0x0	fifo_in_empty_st Input FIFO empty interrupt status.
6	W1C	0x0	fifo_in_full_st Input FIFO full interrupt status.
5	W1C	0x0	ratio_update_done_st Ratio update interrupt status.
4	W1C	0x0	ratio_change_done_st Ratio change interrupt status.

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Bit	Attr	Reset Value	Description
3	RO	0x0	ratio_init_done_st Ratio initial done interrupt status. Level interrupt which can be clear by mask ratio_init_done_en of INT_CON.
2	W1C	0x0	conv_error_st Conversion error interrupt status.
1	RO	0x0	conv_done_st Conversion done interrupt status. Level interrupt which can be clear by mask conv_done_en of INT_CON.
0	RO	0x0	asrc_out_start_st ASRC output start interrupt status. Level interrupt which can be clear by mask asrc_out_start_en of INT_CON.

ASRC_ASRC_ST0

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RO	0x00	chan_num_series Used channel number status in series mode.
7	RO	0x0	dma_rx_ack DMA rx acknowledge status.
6	RO	0x0	dma_rx_req DMA rx request status.
5	RO	0x0	dma_tx_ack DMA tx acknowledge status.
4	RO	0x0	dma_tx_req DMA tx request status.
3	RO	0x0	reserved
2	RO	0x0	filt_delay_done ASRC filter delay done status.
1	RO	0x0	asrc_out_start ASRC out start status.
0	RO	0x0	asrc_in_start ASRC in start status.

ASRC_ASRC_ST1

Address: Operational Base + offset (0x0074)

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Bit	Attr	Reset Value	Description
31:30	RO	0x0	ratio_state Ratio track state. 2'h0: IDLE 2'h1: RATIO_INIT 2'h2: RATIO_TRACK 2'h3: RATIO_STOP
29	RO	0x0	exceed_pos Output FIFO positive exceed status.
28	RO	0x0	exceed_neg Output FIFO negative exceed status.
27:26	RO	0x0	reserved
25:20	RO	0x00	pos_thresh Output FIFO positive thresh status, unit channel_num.
19:18	RO	0x0	reserved
17:12	RO	0x00	neg_thresh Output FIFO negative thresh status, unit channel_num.
11:10	RO	0x0	reserved
9:4	RO	0x00	fifo_out_level Output FIFO level, contains the number of valid data entries in the receive FIFO, unit channel_num.
3:0	RO	0x0	fifo_in_level Input FIFO level, contains the number of valid data entries in the transmit FIFO, unit channel_num.

ASRC_RATIO_ST

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:0	RO	0x0000000	ratio_st Calculate ratio with fixed-point 26Q22. High 4 bits shows integer part, low 22 bits shows decimal part.

ASRC_RESAMPLE_RATE_ST

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RO	0x00000	resample_rate_st Calculate resample rate status.

ASRC_THETA_CNT_ST

Address: Operational Base + offset (0x0090)

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Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:0	RO	0x0000000	theta_cnt_st Theta counter status.

ASRC_DECI_THETA_ACC_ST

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RO	0x00000	deci_theta_acc_st Decimal theta accumulator status.

ASRC_FIFO_IN_WRCNT

Address: Operational Base + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RO	0x00000	fifo_in_wrcnt Input FIFO write counter status, unit channel_num.

ASRC_FIFO_IN_RDCNT

Address: Operational Base + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RO	0x00000	fifo_in_rdcnt Input FIFO read counter status, unit channel_num.

ASRC_FIFO_OUT_WRCNT

Address: Operational Base + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RO	0x00000	fifo_out_wrcnt Output FIFO write counter status, unit channel_num.

ASRC_FIFO_OUT_RDCNT

Address: Operational Base + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RO	0x00000	fifo_out_rdcnt Output FIFO read counter status, unit channel_num.

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ASRC_FIFO_IN_FIXED_DR

Address: Operational Base + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	fifo_in_data Input FIFO fixed address data register.

ASRC_FIFO_OUT_FIXED_DR

Address: Operational Base + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	fifo_out_data Output FIFO fixed address data register.

ASRC_FIFO_IN_INCR_DR

Address: Operational Base + offset (0x1000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	fifo_in_data Input FIFO increment address data register, which ranges from 0x1000 to 0x4FFF.

ASRC_FIFO_OUT_INCR_DR

Address: Operational Base + offset (0x5000)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	fifo_out_data Output FIFO increment address data register, which ranges from 0x5000 to x8FFF.

32.5 Application Notes

32.5.1 LRCK Multiplexing Setting

There are src_lrck and dst_lrck interface which source from audio component or CRU. In real-time transmission mode, the following multiplexing selector need to be set.

Table 32-1 ASRC0 Src_lrck Selector Description

Register Name	MUX Setting	LRCK Source Select
BUSCRU_CLKSEL_CON03	2:0	5'd0: mclk_asrc0 5'd1: mclk_asrc1 5'd2: mclk_asrc2 5'd3: mclk_asrc3 5'd4: sai0_fs 5'd5: sai1_fs 5'd6: sai2_fs 5'd7: clkout_pdm

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Table 32-2 ASRC0 Dst_lrck Selector Description

Register Name	MUX Setting	LRCK Source Select
BUSCRU_CLKSEL_CON03	6:4	5'd0: mclk_asrc0 5'd1: mclk_asrc1 5'd2: mclk_asrc2 5'd3: mclk_asrc3 5'd4: sai0_fs 5'd5: sai1_fs 5'd6: sai2_fs 5'd7: clkout_pdm

Table 32-3 ASRC1 Src_lrck Selector Description

Register Name	MUX Setting	LRCK Source Select
BUSCRU_CLKSEL_CON03	10:8	5'd0: mclk_asrc0 5'd1: mclk_asrc1 5'd2: mclk_asrc2 5'd3: mclk_asrc3 5'd4: sai0_fs 5'd5: sai1_fs 5'd6: sai2_fs 5'd7: clkout_pdm

Table 32-4 ASRC1 Dst_lrck Selector Description

Register Name	MUX Setting	LRCK Source Select
BUSCRU_CLKSEL_CON03	14:12	5'd0: mclk_asrc0 5'd1: mclk_asrc1 5'd2: mclk_asrc2 5'd3: mclk_asrc3 5'd4: sai0_fs 5'd5: sai1_fs 5'd6: sai2_fs 5'd7: clkout_pdm

32.5.2 LRCK Divider Setting

In real-time transmission mode, src_lrck and dst_lrck are treated as data and sampled by working clock to realize periodic detection for ratio tracking. Frequency of src_lrck must be the same as sample rate of audio data, and frequency of dst_lrck must be the same as resample rate of audio data. To guarantee this, two clock dividers are integrating into ASRC. In the following condition, the corresponding divider ought to be set and we ought to wait for the generated clock to stabilize before starting ASRC.

- Using PDM as source component, set src_lrck_div_con to (pdm_oversample_rate-1)

32.5.3 Tracking Period Setting

In real-time transmission mode, ratio tracking is enabled. Tracking period is determined by the value of ratio_track_period and ratio_track_div, which means track information updates every (ratio_track_period+1)*(ratio_track_div+1) working clock. The longer the period, the more precise the tracking. Besides, the following format must be meet to ensure ratio resolution:

(ratio_track_period+1)*(ratio_track_div+1) >=

Twclk*Fsrc_lrck*(1/Resolution+Fsrc_lrck/(Resolution*Fdst_lrck)+1)

Where Twclk is the period of working clock, Resolution is the bit wide of ratio, Fsrc_lrck is the frequency of src_lrck, and Fdst_lrck is the frequency of dst_lrck. Note that the smaller ratio_track_div is, the better, given the equation.

Besides, once lrck sources from CRU for audio component like USB or MAC, the fractional divider in the clock path of src_lrck or dst_lrck ought to be used for seamless switching. In

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this scenario, tracking period must be an integer multiple of the frequency division period, to guarantee ratio tracking accuracy.

32.5.4 DMA Setting

For transmitting data to ASRC and receiving data from ASRC, two DMA channels are need called DMA_TX and DMA_RX here. DMA mode used for various ASRC mode is shown below.

Table 32-5 ASRC DMA Mode Description

ASRC Mode	DMA_TX	DMA_RX
Memory Fetch Mode	M2P	P2M
MEM2MEM	M2P	P2M
MEM2DST	M2P	M2P
SRC2MEM	P2M	P2M
SRC2DST	P2M	M2P

In a word, once interacting with audio component, ASRC acts as memory and audio component issues DMA request, once interacting with memory, ASRC acts as peripheral and issues DMA request according to dma_tx_thresh and dma_rx_thresh.
Both dma_tx_thresh and dma_rx_thresh are in the unit of chan_num. That is, the relation between real DMA burst (called dma_tx/rx_burst) and dma_tx/rx_thresh is shown below:

dma_tx_thresh = dma_tx_burst*(IFMT+1)/(chan_num+1)/2-1
dma_rx_thresh = dma_rx_burst*(OFMT+1)/(chan_num+1)/2-1

32.5.5 Memory Fetch Mode Setting

- **Setting order**
  - Set and start DMA_TX and DMA_RX.
  - Set and start ASRC.
- **ASRC start Flow**
  - Set used channel number, chan_num.
  - Set data format, OFMT, IFMT, OWL, IWL, OSJM and ISJM.
  - Set manual_ratio, sample_rate and resample_rate.
  - Set thresh, dma_rx_thresh, dma_tx_thresh, asrc_out_thresh and asrc_in_thresh;
  - Set asrc_mode to 1.
  - Set conversion length, fetch_length.
  - Set conv_done_en to enable conversion done interrupt.
  - In loop mode, set continuous conversion times (loop_times), file channel number divided by used channel number (chan_times), file type (loop_start/end_mode) and conversion interval (loop_gap_thresh), then enable loop_en.
  - Set asrc_en to enable ASRC.
- **ASRC end Flow**
  - Wait for conv_done and DMA_RX done interrupt.
  - Set asrc_en to disable ASRC.

32.5.6 Real-time Transmission Mode Setting

- **Setting order**
  - Set the source of src_lrck and dst_lrck.
  - Set src_lrck_div_con, src_lrck_div_en, dst_lrck_div_con, dst_lrck_div_en if needed.
  - Set and start DMA_TX and DMA_RX.
  - Set and start ASRC; ASRC must be set before source and destination component to make sure audio data is aligned by channel.
  - Set and start source component in the mode SRC2MEM or SRC2DST.
  - Set mem2asrc_ready when source data ready in the mode MEM2MEM or MEM2DST.
  - Set and start destination component in the mode MEM2DST or SRC2DST.

Destination component had better start when asrc_out_start interrupt assert which means destination data is ready.

- **ASRC start Flow**
  - Set used channel number, chan_num.
  - Set data format, OFMT, IFMT, OWL, IWL, OSJM and ISJM.
  - Set manual_ratio, sample_rate and resample_rate.
  - Set thresh, dma_rx_thresh, dma_tx_thresh, asrc_out_thresh and asrc_in_thresh.

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- Set asrc_mode to 0; set real_time_mode.
- Set ratio_track_period and ratio_track_div.
- Set ratio_track_dis to disable ratio tracking, ratio_filt_dis to disable ratio tracking filter, or ratio_exc_dis to disable ratio tracking feedback if needed.
- Set conv_done_en to enable conversion done interrupt.
- **ASRC end Flow**
- Set asrc_in_stop to end conversion if source component stop.
- Set asrc_out_stop to end conversion if destination component stop.
- Wait for conv_done and DMA_RX done interrupt.
- Set asrc_en to disable ASRC.

32.5.7 Series Mode Setting

In series mode, we can set each ASRC as mentioned above. Several additional setting is needed shown as follow:

- Set series_en to appoint master and slave; Note that series_en can't be set if series mode is disabled.
- In series mode, thresh like dma_rx_thresh, dma_tx_thresh, asrc_out_thresh or asrc_in_thresh needs to be set to the same value.
- Set series_post_end to appoint the last slave if memory fetch mode is selected.
- Set asrc_en of the series master at the end after all other configurations are set.

The following table shows all the cascading combinations in RV1126B. Note, the letter M stands for master and the letter S stands for slave.

Table 32-6 Audio0 Wrapper ASRC Series Description

Series Setting	Series Combination
ASRC0_ASRC_CON[13:12]=2'h1 ASRC1_ASRC_CON[13:12]=2'h2	ASRC0(M), ASRC1(S)

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Chapter 33 Flexible Serial Peripheral Interface (FSPI)

33.1 Overview

The FSPI is a flexible serial peripheral interface host controller to interface with external device.

The FSPI supports the following features:

- Support various vendor devices with flexible command sequencer engine
  - Serial NOR Flash
  - Serial NAND Flash
  - Serial pSRAM
  - Serial SRAM
- Support 2 independent FSPI: FSPI0~1
- FSPI0 Support SDR mode and x4 DDR mode, FSPI1 Support SDR mode
- Support Single/Dual/Quad IO mode
- Support a 32-bit AHB slave to read and write controller register bank and initiate command sequence, including transfer data from/to external device indirectly
- Support a 32-bit AHB master with embedded DMA engine to transfer data from/to external device indirectly
- Support a 128-bit AHB slave to transfer data from/to external device indirectly
- Support independent clock for system bus HCLK and controller core SCLK
- Support maskable interrupts generation
- Support sampling clock with optionally configurable delay line
- FSPI0 Support 2 CS# operation, FSPI1 Support 1 CS# operation

33.2 Block Diagram

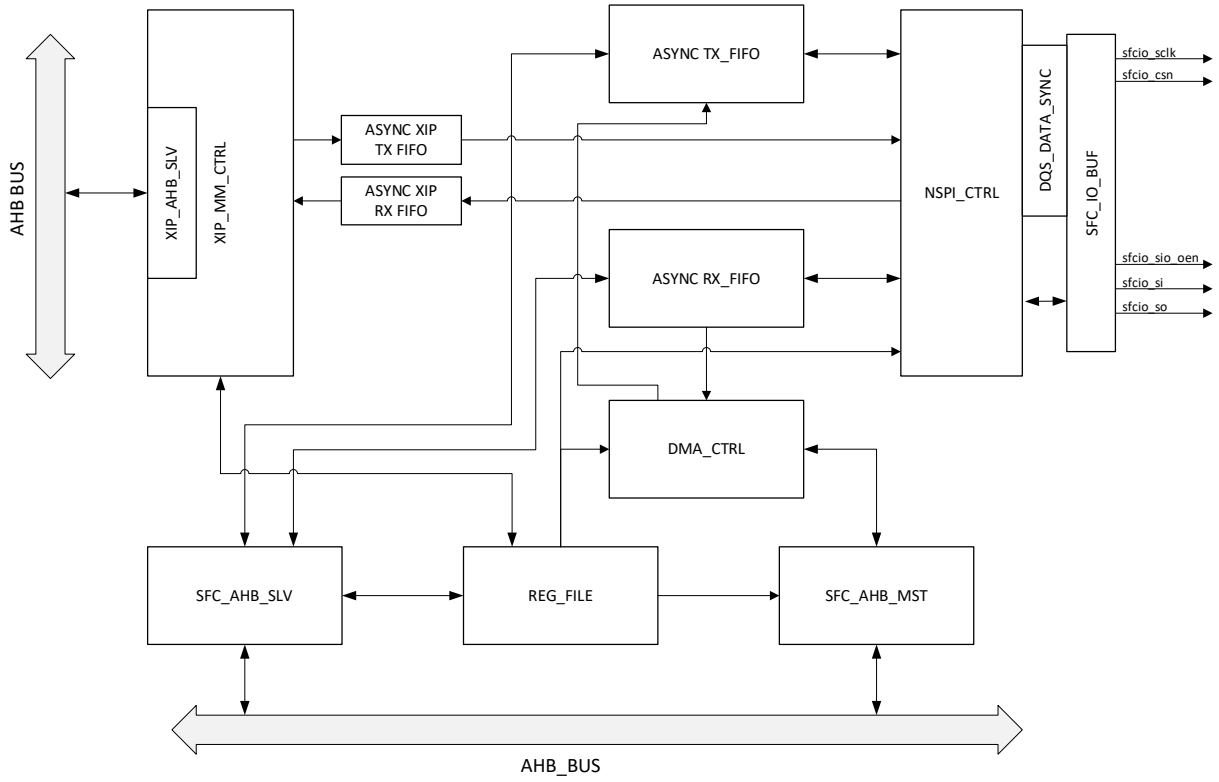

Fig. 33-1 FSPI Architecture

Memory-Mapped AHB slave is available when XIP feature is present.

33.3 Function Description

33.3.1 AHB Slave

The AHB slave block is used to configure the register of controller to generate flexible command sequence, process the interrupt exception, target various device feature and AC timing specification. It is also used to write CMD/ADDR/DATA to TX FIFO and read DATA from RX FIFO which buffer the DATA from external device.

33.3.2 AHB Master

When the embedded DMA CTRL is used to transfer DATA, the AHB master is used to transfer data to other system region, such as internal SRAM, peripheral, external DRAM.

33.3.3 XIP MM CTRL

When the XIP port is used to transfer DATA, the XIP_MM_CTRL is used to transfer data to other system region.

33.3.4 REG File

The REG File is configurable register bank to control the store the static configuration and dynamic status of controller.

33.3.5 DMA CTRL

A block takes responsible for splitting a long length transfer trans into AHB bus transaction and interfacing with ASYNC TX or RX FIFO.

33.3.6 FIFO

There are four FIFO in the FSPI controller. ASYNC TX FIFO and ASYNC RX FIFO is for normal transaction that initiated by command sequence driver. The ASYNC MM (Memory-Mapped) TX FIFO and ASYNC MM (Memory-Mapped) RX FIFO is only used to buffer DATA from or to external device initiated by system bus master directly.

33.3.7 NSPI CTRL

Sequence decode engine which generates specialized timing sequence for various device. The NSPI decode the transaction from TX FIFO and Memory-Mapped Controller and convert it to relative CMD/ADDR/DATA frame based on the configuration.

33.4 Register Description

33.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
FSPI0	0x21460000
FSPI1	0x208C0000

33.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
FSPI_CTRL0	0x0000	W	0x00000000	Control Register for CS0 Device
FSPI_IMR	0x0004	W	0x00000FFF	Interrupt Mask Register
FSPI_ICLR	0x0008	W	0x00000000	Interrupt Clear Register
FSPI_FTLR	0x000C	W	0x00001010	FIFO Threshold Level Register
FSPI_RCVR	0x0010	W	0x00000000	FSPI Recover Register
FSPI_AX0	0x0014	W	0x00000000	FSPI Auxiliary Data Value for CS0 Device
FSPI_ABIT0	0x0018	W	0x00000000	Extend Address Bits for CS0 Device
FSPI_ISR	0x001C	W	0x00000000	Interrupt Status
FSPI_FSR	0x0020	W	0x00000001	FIFO Status Register
FSPI_SR	0x0024	W	0x00000000	FSPI Status Register
FSPI_RISR	0x0028	W	0x00000000	Raw Interrupt Status Register

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Name	Offset	Size	Reset Value	Description
FSPI_VER	0x002C	W	0x00030010	Version Register
FSPI_QOP	0x0030	W	0x00000000	Quad Line Operation IO Level Pre-set Register
FSPI_EXT_CTRL	0x0034	W	0x00004023	Extend Control Register
FSPI_DLL_CTRL0	0x003C	W	0x00000001	Delay Line Control Register for CS0 Device
FSPI_HRDYMASK	0x0040	W	0x00000000	AMBA HREADY Mask Control Register
FSPI_EXT_AX	0x0044	W	0x0000F0FF	Extend Auxiliary Data Control Register
FSPI_SCLK_INATM_CNT	0x0048	W	0xFFFFFFFF	SCLK Inactive Timeout Counter
FSPI_XMMC_WCMD0	0x0050	W	0x00000000	Memory Mapped Control Write Command Register for CS0 Device
FSPI_XMMC_RCMD0	0x0054	W	0x00000000	Memory Mapped Control Read Command Register for CS0 Device
FSPI_XMMC_CTRL	0x0058	W	0x000072E0	Memory Mapped Control Register
FSPI_MODE	0x005C	W	0x00000000	Controller Working Mode Register
FSPI_DEVRGN	0x0060	W	0x00000017	Device Region Size Register
FSPI_DEVSIZE0	0x0064	W	0x00000012	Device Size Register for CS0 Device
FSPI_TME0	0x0068	W	0x00000000	Timeout Enable Control Register for CS0 Device
FSPI_POLLDLY_CTRL	0x006C	W	0x0003FFFF	Polling Delay Control Register
FSPI_RX_FULL_WTMRK	0x0070	W	0x00010002	Receiver FIFO Water Mark Register
FSPI_DUMM_CTRL	0x0074	W	0x00000000	Dummy Cycle Control Register
FSPI_CMD_EXT	0x0078	W	0x00000000	Command Extend Register
FSPI_TRC_CTRL	0x007C	W	0x00000000	TRC Cycle Control Register
FSPI_DMATR	0x0080	W	0x00000000	DMA Trigger Register
FSPI_DMAADDR	0x0084	W	0x00000000	DMA Address Register
FSPI_LEN_CTRL	0x0088	W	0x00000000	Length Control Register
FSPI_LEN_EXT	0x008C	W	0x00000000	Length Extended Register
FSPI_XMMCSR	0x0094	W	0x00000000	Memory Mapped Status Register
FSPI_HYPER_RSVD_ADDR	0x0098	W	0x00000000	Hyperbus Reserved Address Bit
FSPI_VDMC0	0x009C	W	0x00000000	Vendor Device Mode Control Register
FSPI_DBG_IO_CTRL	0x00A0	W	0x00000000	Debug IO Control
FSPI_DEV_RSTN	0x00A4	W	0x0000000F	Device Reset_n
FSPI_SLF_DQS_CTRL	0x00A8	W	0x00000000	Self DQS Control
FSPI_TRNS_TR_CTRL	0x00AC	W	0x00000000	Transfer Trigger Control
FSPI_TRNS_TR	0x00B0	W	0x00000000	Transfer Trigger
FSPI_DMA_CHAIN_TR	0x00B4	W	0x00000000	DMA Chain Trigger
FSPI_DMA_HEAD_ADDR	0x00B8	W	0x00000000	DMA Chain Head Node Address
FSPI_DMA_CTRL	0x00BC	W	0x00000000	DMA AHB Burst Type Control
FSPI_FSPI_IDLE	0x00C0	W	0x00000000	FSPI IDLE State
FSPI_TX_DLL_CTRL0	0x00C4	W	0x00000001	TX SCLK Delay Line Control Register for CS0 Device
FSPI_CMD	0x0100	W	0x00000000	Indirect Command Register

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Name	Offset	Size	Reset Value	Description
FSPI_ADDR	0x0104	W	0x00000000	Address Register
FSPI_DATA	0x0108	W	0x00000000	Data Register
FSPI_CTRL1	0x0200	W	0x00000000	Control Register for CS1 Device
FSPI_AX1	0x0214	W	0x00000000	FSPI Auxiliary Data Value for CS1 Device
FSPI_ABIT1	0x0218	W	0x00000000	Extend Address Bits for CS1 Device
FSPI_DLL_CTRL1	0x023C	W	0x00000001	Delay Line Control Register for CS1 Device
FSPI_XMMC_WCMD1	0x0250	W	0x00000000	Memory Mapped Control Write Command Register for CS1 Device
FSPI_XMMC_RCMD1	0x0254	W	0x00000000	Memory-Mapped Command Control Register for CS1 Device
FSPI_DEVSIZE1	0x0264	W	0x00000012	Device Size Register for CS1 Device
FSPI_TME1	0x0268	W	0x00000000	Timeout Enable Control Register for CS1 Device
FSPI_VDMC1	0x029C	W	0x00000000	Special device information
FSPI_TX_DLL_CTRL1	0x02C4	W	0x00000000	TX SCLK Delay Line Control Register for CS1 Device

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

33.4.3 Detail Registers Description

FSPI_CTRL0

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	WP_EN WP# Port Enable 1'b0: Disable 1'b1: Enable. The WP# port will always be driven by QOP[SO123] when QOP[SO123BP] is set to disable.
28:27	RW	0x0	CMD_CTRL Indirect Command Field Controll 2'b00: Command controlled by CMD[CMD] 2'b01: Command controlled by CMD[CMD] and combine with 8 bit address 2'b10: Command controlled by CMD_EXT/XMMC_WCMD/XMMC_RCMD[CMDF_EXT] according to different mode. Command length is 16 bits 2'b11: Reserved
26	RW	0x0	HYPER_RSVD_EN Hyperbus Reserved Address Bit Enable 1'b0: Disable 1'b1: Enable
25	RW	0x0	HYPER_ADDR_EN Address Remap in Hyperbus Mode 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
24	RW	0x0	INTRNL_CLK_MODE Internal Clock Mode 1'b0: Use the IOBUF CORE_CLK to Sample the Data 1'b1: Use the Sclk from IOPAD to Sample the Data.
23:22	RW	0x0	DUMM_OVLP Dummy Phase Overlap with Address Phase. 3'd0: Dummy phase will start after address phase 3'd1: Dummy phase will overlap a cycle with address phase 3'd2: Dummy phase will overlap 2 cycles with address phase 3'd3: Dummy phase will overlap 3 cycles with address phase To set the overlap cycles between dummy phase and address phase.
21	RW	0x0	DBL_DUMM_CTRL Double dummy cycle controller 1'b0: dummy cycle always equal to CMD[DUMM] 1'b1: dummy cycle will be twice of CMD[DUMM] when dqs is high
20	RW	0x0	ADDR_STR Cmd phase work in STR mode in DTR mode. 1'b0: Disable 1'b1: Enable. The CTRL0/1[DTR_MODE] must set to 1'b1
19	RW	0x0	CMD_STR Cmd phase work in STR mode in DTR mode. 1'b0: Disable 1'b1: Enable. The CTRL0/1[DTR_MODE] must set to 1
18	RW	0x0	DTR_RDC_SEL Read Clk Select in DTR Mode 1'b0: Use external synchronous clock to sample the data. Quad DTR mode does not support this mode 1'b1: Use internal clk to sample the data
17	RW	0x0	DQS_MODE DQS MODE 1'b0: DQS can be driven by controller and device 1'b1: DQS is always driven by device
16	RW	0x0	DATAB16 16 Bit Data Line Width. 1'b0: Data Line Width controlled by CTRL0[DATB] 1'b1: 16 bits, x16 mode
15	RW	0x0	ADRB16 16 Bit Address Line Width. 1'b0: Address Line Width controlled by CTRL0[ADRB] 1'b1: 16 bits, x16 mode
14	RW	0x0	CMDB16 16 Bit Command Line Width. 1'b0: Command Line Width controlled by CTRL0[CMDB] 1'b1: 16 bits, x16 mode
13:12	RW	0x0	DATB Data Line Width 2'b00: 1 bit, x1 mode 2'b01: 2 bits, x2 mode 2'b10: 4 bits, x4 mode 2'b11: 8 bits, x8 mode Set this DATB to match the CMD sequence before doing indirect access mode and memory mapped access mode.

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Bit	Attr	Reset Value	Description
11:10	RW	0x0	ADRB Address Line Width 2'b00: 1 bit, x1 mode 2'b01: 2 bits, x2 mode 2'b10: 4 bits, x4 mode 2'b11: 8 bits, x8 mode Set this ADRB to match the CMD sequence before doing indirect access mode and memory mapped access mode.
9:8	RW	0x0	CMDB Command Line Width 2'b00: 1 bit, x1 mode 2'b01: 2 bits, x2 mode 2'b10: 4 bits, x4 mode 2'b11: 8 bits, x8 mode Set this CMDB to match the CMD sequence before doing indirect access mode and memory mapped access mode.
7:4	RW	0x0	IDLE_CYCLE Idle Cycles When Switching IO from Output to Input 4'h0: Idle hold is disable 4'h1: Hold the SCLK in idle for 2 cycles when switch to shift in ... 4'hf: Hold the SCLK in idle for 16 cycles when switch to shift in To improve the transform IO timing, the application can set this register to hold the SCLK in low state or high state.
3	RW	0x0	DAT_ORDER The Order of Data in a Cycle 1'b0: Date in a cycle is from low byte to high byte 1'b1: Date in a cycle is from high byte to low byte
2	RW	0x0	DTR_MODE DTR mode enable 1'b0: STR mode 1'b1: DTR mode
1	RW	0x0	SHIFTPHASE Shift Phase of Data Input in Controller 1'b0: Shift input data at posedge SCLK 1'b1: Shift input data at negedge SCLK The application can select the input data captured by posedge of SCLK when "0" or negedge of SCLK when "1".
0	RW	0x0	SPIM Serial Peripheral Interface Mode 1'b0: Mode 0 1'b1: Mode 3 SPIM is used to control the serial mode (CPOL and CPHA). CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

FSPI_IMR

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
11	RW	0x1	CHAINM Chain Finish Interrupt Mask 1'b0: Chain finish interrupt is not masked 1'b1: Chain finish interrupt is masked Only valid in indirect access mode.
10	RW	0x1	NODE_ILLGLM Chain Node Illegal Interrupt Mask 1'b0: Chain Node Illegal Interrupt is not masked 1'b1: Chain Node Illegal Interrupt is masked
9	RW	0x1	ILLGL_WRM Illegal Register Write Interrupt Mask 1'b0: Illegal register write interrupt is not masked 1'b1: Illegal register write interrupt is masked Only valid when IP support the Secure Function.
8	RO	0x0	reserved
7	RW	0x1	DMAM DMA Finish Interrupt Mask 1'b0: DMA finish interrupt is not masked 1'b1: DMA finish interrupt is masked Only valid in indirect access mode.
6	RW	0x1	NSPIM NSPI Interrupt Mask 1'b0: NSPI interrupt is not masked 1'b1: NSPI interrupt is masked Valid in indirect access mode and memory mapped mode.
5	RW	0x1	AHBM AMBA AHB Error Interrupt Mask 1'b0: AMBA AHB Error interrupt is not masked 1'b1: AMBA AHB Error interrupt is masked Only valid in indirect access mode.
4	RW	0x1	TRANSM Transfer Finish Interrupt Mask 1'b0: Transfer finish interrupt is not masked 1'b1: Transfer finish interrupt is masked Only valid in indirect access mode.
3	RW	0x1	TXEM Transmit FIFO Empty Interrupt Mask 1'b0: Transmit FIFO empty interrupt is not masked 1'b1: Transmit FIFO empty interrupt is masked Only valid in indirect access mode.
2	RW	0x1	TXOM Transmit FIFO Overflow Interrupt Mask 1'b0: Transmit FIFO overflow interrupt is not masked 1'b1: Transmit FIFO overflow interrupt is masked Only valid in indirect access mode.
1	RW	0x1	RXUM Receive FIFO Underflow Interrupt Mask 1'b0: Receive FIFO underflow interrupt is not masked 1'b1: Receive FIFO underflow interrupt is masked Only valid in indirect access mode.
0	RW	0x1	RXFM Receive FIFO Full Interrupt Mask 1'b0: Receive FIFO full interrupt is not masked 1'b1: Receive FIFO full interrupt is masked Only valid in indirect access mode.

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FSPI_ICLR

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RW	0x0	CHAINC Chain Finish Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the CHAINS
10	RW	0x0	NODE_ILLGLM Chain Node Illegal Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the NODE_ILLGLS
9	W1C	0x0	ILLGL_WRC Illegal Register Write Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the ILLGL_WRS.
8	RO	0x0	reserved
7	W1C	0x0	DMAC DMA Finish Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the DMAS
6	W1C	0x0	NSPIC NSPI Error Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the NSPIS.
5	W1C	0x0	AHBC AMBA AHB Error Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the AHBS.
4	W1C	0x0	TRANSC Transfer Finish Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the TRANSS.
3	W1C	0x0	TXEC Transmit FIFO Empty Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the TXES.
2	W1C	0x0	TXOC Transmit FIFO Overflow Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the TXOS.
1	W1C	0x0	RXUC Receive FIFO Underflow Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the RXUS.

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Bit	Attr	Reset Value	Description
0	W1C	0x0	RXFC Receive FIFO Full Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the RXFS.

FSPI_FTLR

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x10	RXFTLR Receive FIFO Threshold Level 8'h0: 0 entry level 8'h1: 1 entry level ... 8'h10: 16 entry level(default) ... When the number of receive FIFO entries is bigger than or equal to this value, the receive FIFO full interrupt is triggered.
7:0	RW	0x10	TXFTLR Transmit FIFO Threshold Level 8'h0: 0 entry level 8'h1: 1 entry level ... 8'h10: 16 entry level(default) ... When the number of transmit FIFO entries is less than or equal to this value, the transmit FIFO empty interrupt is triggered.

FSPI_RCVR

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	R/WSC	0x0	RCVR FSPI Recover Write any values to trigger the recovery of SMC NSPI state machine, FIFO state and other logic state.

FSPI_AX0

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	AX Auxiliary Data The AX value when doing the continuous read (enhance mode or XIP mode). That is M7-M0 in "Continuous Read Mode".

FSPI_ABIT0

Address: **Operational Base** + offset (0x0018)

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Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	ABIT Address Bits Extend 6'h0: 1 bit 6'h1: 2 bits ... 6'h3f: 64 bits When ADDRB have no option for address bits number, use this field to set the right address bits number. Only valid when ADDRB is set to 2'b11.

FSPI_ISR

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RW	0x0	CHAINS Chain Finish Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
10	RW	0x0	NODE_ILLGLS Chain Node Illegal Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
9:8	RO	0x0	reserved
7	RO	0x0	DMAS DMA Finish Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
6	RO	0x0	NSPIS NSPI Transaction Decode Error Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
5	RO	0x0	AHBS AMBA AHB Error Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
4	RO	0x0	TRANSS Transfer Finish Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
3	RO	0x0	TXES Transmit FIFO Empty Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
2	RO	0x0	TXOS Transmit FIFO Overflow Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
1	RO	0x0	RXUS Receive FIFO Underflow Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated

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Bit	Attr	Reset Value	Description
0	RW	0x0	RXFS Receive FIFO Full Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated

FSPI_FSR

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:16	RW	0x00	RXWLVL RX FIFO Water Level 5'h0: FIFO is empty 5'h1: 1 entry is taken ... 5'h10: 16 entry is taken, FIFO is full
15	RO	0x0	reserved
14:8	RO	0x00	TXWLVL TX FIFO Water Level 7'h0: FIFO is full 7'h1: 1 entry is left ... 7'h10: 16 entry is left ...
7:4	RO	0x0	reserved
3	RO	0x0	RXFS Receive FIFO Full Status 1'b0: RX FIFO is not full 1'b1: RX FIFO is full
2	RO	0x0	RXES Receive FIFO Empty Status 1'b0: RX FIFO is not empty 1'b1: RX FIFO is empty
1	RO	0x0	TXES Transmit FIFO Empty Status 1'b0: TX FIFO is not empty 1'b1: TX FIFO is empty
0	RO	0x1	TXFS Transmit FIFO Full Status 1'b0: TX FIFO is not full 1'b1: TX FIFO is full

FSPI_SR

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
0	RO	0x0	SR Status Register 1'b0: NSPI Controller is idle 1'b1: NSPI Controller is busy When controller is busy, don't change the setting of control register. When NSPI is idle, the software can initiate new transaction to external device.

FSPI_RISR

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	ILLGL_WRS Illegal Register Write Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
8	RO	0x0	reserved
7	RO	0x0	DMAS DMA Finish Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
6	RO	0x0	NSPIS NSPI Error Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
5	RO	0x0	AHBS AMBA AHB Error Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
4	RO	0x0	TRANSS Transfer Finish Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
3	RO	0x0	TXES Transmit FIFO Empty Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.

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Bit	Attr	Reset Value	Description
2	RO	0x0	TXOS Transmit FIFO Overflow Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
1	RO	0x0	RXUS Receive FIFO Underflow Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
0	RO	0x0	RXFS Receive FIFO Full Interrupt Status 1'b0: No active raw interrupt 1'b1: Active raw interrupt is generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.

FSPI_VER

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RO	0x0	DDR_UNSPPT The DDR CAP of FSPI 1'b0: Supported 1'b1: Unspported
19	RO	0x0	X16_CAP The X16 CAP of FSPI 1'b0: Unsupported 1'b1: Supported
18	RO	0x0	X8_CAP The X8 CAP of FSPI 1'b0: Unsupported 1'b1: Supported
17	RO	0x1	X4_CAP The X4 CAP of FSPI 1'b0: Unsupported 1'b1: Supported
16	RO	0x1	RSVD Reserved Bit
15:0	RO	0x0010	VER The Version ID of FSPI

FSPI_QOP

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x0	SO123BP SO123 Bypass Mode 1'b0: Disable bypass 1'b1: Enable bypass Default is enabled.
0	RW	0x0	SO123 D1/D2/D3 Data Value During Inactive When CS is Active 1'b0: Set to "0" 1'b1: Set to "1" The value of SO1, SO2 and SO3 during command and address bits input.

FSPI_EXT_CTRL

Address: **Operational Base** + offset (0x0034)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	SCLK_X2_BYPASS Bypass the SCLK_X2 as CORE_SCLK 1'b0: Use the SCLK_X2 div 2 as CORE_SCLK 1'b1: Use the SCLK_X2 as CORE_SCLK
23:22	RO	0x0	reserved
21:20	RW	0x0	DQS_SMP_MODE In Register Input Mode, the dqin data will be registered and then written to the FIFO, and the CS will be pulled up when the number of read data satisfy the requirement of the burst, and the dqin FIFO need be reset asynchronously. In Direct Input Mode, the dqin data will be input directly to the FIFO, and also the CS will be pulled up when the CK counter end. In CK Plus One Mode, the dqin data will be registered and then written to the FIFO, and also the CS will be pulled up when the CK+1 counter end. In Async Rst Mode, the dqin data will be input directly to the FIFO, and also the CS will be pulled up when the CK counter end, but the dqin FIFO will also be reset asynchronously. 2'b00: Register Input Mode 2'b01: Direct Input Mode 2'b10: CK Plus One Mode 2'b11: Async Rst Mode
19	RW	0x0	CSH_CLK_EN SCLK Toggle Enable when CS is HIGH 1'b0: SCLK will hold when CS is HIGH 1'b1: SCLK will toggle when CS is HIGH
18	RO	0x0	reserved
17:16	RW	0x0	CSH_EXT Chip Select Hold Time Extend: 1'h0: Default mode 1'h1: Extend 1 cycle 1'h2: Extend 2 cycle 1'h3: Extend 3 cycle To improve the transform IO timing, the application can set this field to extend chip select hold time.

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Bit	Attr	Reset Value	Description
15	RW	0x0	CSS_EXT Chip Select Setup Time Extend: 1'h0: Default mode 1'h1: Extend 1 cycle To improve the transform IO timing, the application can set this field to extend chip select setup time.
14	RW	0x1	SR_GEN_MODE Status Register Generation Mode 1'b0: Compatible mode with old controller 1'b1: Robust generation to indicates the status of controller If set to "1", the controller will only clear the SR bit after operation sequence done and CS is high.
13	RW	0x0	TRANS_INT_MODE Transmit Done Interrupt Generation Mode 1'b0: Trigger NSPI end in data done 1'b1: Trigger NSPI end in CS inactive Default Generation is compatible with old controller.
12	RO	0x0	reserved
11:8	RW	0x0	SWITCH_IO_O2I_CNT Switch IO Attribute Cycles in O2I Idle Phase 4'h0: 1st cycle 4'h1: 2nd cycle 4'h2: 3rd cycle 4'h3: 4th cycle ... 4'hf: 16th cycle The target cycle when switching from output to input in O2I idle phase.
7:4	RW	0x2	SWITCH_IO_DUMM_CNT Switch IO Attribute Cycles in Dummy Phase 4'h0: 1st cycle 4'h1: 2nd cycle 4'h2: 3rd cycle 4'h3: 4th cycle ... 4'hf: 16th cycle The target cycle when switching from output to input in Dummy data phase.
3:0	RW	0x3	CS_DESEL_CTRL CS Inactive Control 4'h0: 1 cycle 4'h1: 2 cycles 4'h2: 3 cycles 4'h3: 4 cycles ... 4'hf: 16 cycles The target cycles to hold CS inactive after de-assert the CS. Default value are 4 SCLK cycles that is enough for normal device.

FSPI_DLL_CTRL0

Address: **Operational Base** + offset (0x003C)

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Bit	Attr	Reset Value	Description
31	RW	0x0	DQS1_SMP_SEL DQS1 Sampling Selection 1'b0: Bypass DLL 1'b1: From DLL The sampling DQS1 source selection.
30:25	RO	0x00	reserved
24:16	RW	0x000	DQS1_DLL_CFG DQS1 Delay Line Configuration 9'h0: 1 DLL element cell 9'h1: 1 DLL element cell 9'h2: 2 DLL element cells ... 9'h1ff: 511 DLL element cells This register to control the sampling delay line cell used. The maximum DLL element cells is decided by process.
15	RW	0x0	SCLK_SMP_SEL SCLK Sampling Selection 1'b0: Bypass DLL 1'b1: From DLL The sampling SCLK source selection.
14:9	RO	0x00	reserved
8:0	RW	0x001	SMP_DLL_CFG Sample Delay Line Configuration 9'h0: 1 DLL element cell 9'h1: 1 DLL element cell 9'h2: 2 DLL element cells ... 9'h1ff: 511 DLL element cells This register to control the sampling delay line cell used. The maximum DLL element cells is decided by process.

FSPI_HRDYMASK

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	RO	0x0	XIP_HUP_STATE Memory Mapped Mode Hang up State 1'b0: Memory Mapped Mode is working 1'b1: Memory Mapped Mode is Hanging up
17	W1C	0x0	XIP_HUP_RLS_REQ Memory Mapped Mode Hang up State Release Request 1'b1: Release Memory Mapped Mode Hang up state
16	W1C	0x0	XIP_HUP_REQ Memory Mapped Mode Hang up Request 1'b1: request Memory Mapped Mode Hang up
15:0	RO	0x0000	reserved

FSPI_EXT_AX

Address: **Operational Base** + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15:8	RW	0xf0	AX_SETUP_PAT Auxiliary Setup Data Pattern The AX data pattern that setup the continuous/enhance/XIP read mode
7:0	RW	0xff	AX_CANCEL_PAT Auxiliary Cancel Data Pattern The AX data pattern that cancel the continuous/enhance/XIP read mode.

FSPI_SCLK_INATM_CNT

Address: **Operational Base** + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RW	0xffffffff	SCLK_INATM_CNT SCLK Inactive Timeout Counter When CS is active and SCLK is hold in high or low due to TX FIFO is empty or RX FIFO is full, if SCLK_INATM_EN is enabled, and timeout occurs, the controller will go back to idle and RX FIFO is flushed.

FSPI_XMMC_WCMD0

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	CMDF_EXT Command Command data in memory mapped access mode when command length is 16 bits.
15:14	WO	0x0	ADDRB Address Bits 2'b00: 0 bit 2'b01: 24 bits 2'b10: 32 bits 2'b11: From the ABIT register Address bits number select in memory mapped mode, if there is not address command to send, set to zero.
13	WO	0x0	CONT Continuous 1'b0: Disable continuous mode 1'b1: Enable continuous mode AX mode or Continuous mode or XIP mode for device which begins with address.
12	RO	0x0	reserved
11:8	WO	0x0	DUMM Dummy Cycles 4'h0: No dummy cycle ... 4'h8: 8 cycles ... Dummy bit cycles in memory mapped mode.
7:0	WO	0x00	CMD Command Command data in memory mapped access mode.

FSPI_XMMC_RCMD0

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Address: **Operational Base** + offset (0x0054)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	CMDF_EXT Command Command data in memory mapped access mode when command length is 16 bits.
15:14	WO	0x0	ADDRB Address Bits 2'b00: 0 bit 2'b01: 24 bits 2'b10: 32 bits 2'b11: From the ABIT register Address bits number select in memory mapped mode, if there is not address command to send, set to zero.
13	WO	0x0	CONT Continuous 1'b0: Disable continuous mode 1'b1: Enable continuous mode AX mode or Continuous mode or XIP mode for device which begins with address.
12	RO	0x0	reserved
11:8	WO	0x0	DUMM Dummy Cycles 4'h0: No dummy cycle ... 4'h8: 8 cycles ... Dummy bit cycles in memory mapped mode.
7:0	WO	0x00	CMD Command Command data in memory mapped access mode.

FSPI_XMMC_CTRL

Address: **Operational Base** + offset (0x0058)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x1	PFT_EN Prefetch Enable 1'b0: Disable 1'b1: Enable Should disable prefetch if controller communicate with pSRAM which need refresh.
5	RW	0x1	DEV_HWEN Device AMBA AHB HWRITE Enable 1'b0: Disable 1'b1: Enable
4:0	RO	0x00	reserved

FSPI_MODE

Address: **Operational Base** + offset (0x005C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	XMMC_MODE_EN Memory Mapped Mode Enable 1'b0: Disable, indirect access mode 1'b1: Enable, Memory-Mapped mode Before switching from indirect access mode to Memory-Mapped mode, the application should make sure the controller is in idle state and no pending transaction. If switch from Memory-Mapped to indirect access mode, software should initiate a dummy read by CPU before that.

FSPI_DEVRGN

Address: **Operational Base** + offset (0x0060)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RW	0x0	DEC_CTRL Decode Control 2'b00: 1 CS# 2'b01: 2 CS# 2'b10: 4 CS# 2'b11: Reserved Only valid in XMMC mode.
7:5	RO	0x0	reserved
4:0	RW	0x17	RSIZE Region Size 5'd0: 1 byte 5'd1: 2 bytes 5'd2: 4 bytes ..... 5'd10: 1K bytes ..... 5'd20: 1M bytes ..... 5'd31: 4G bytes In Memory-Mapped mode, the CS is controlled by AHB address bus, region size is used to generate CS.

FSPI_DEVSIZE0

Address: **Operational Base** + offset (0x0064)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x12	DSIZE Device Size 5'd0: 1 byte 5'd1: 2 bytes 5'd2: 4 bytes ..... 5'd10: 1K bytes ..... 5'd20: 1M bytes ..... 5'd31: 4G byte Device size is used to generate slop over status.

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FSPI_TME0

Address: **Operational Base** + offset (0x0068)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	SCLK_INATM_EN SCLK Inactive Timeout Enable 1'b0: Disable 1'b1: Enable
0	RO	0x0	reserved

FSPI_POLLDLY_CTRL

Address: **Operational Base** + offset (0x006C)

Bit	Attr	Reset Value	Description
31	RW	0x0	POLLDLY_IP Polling Delay in Progress 1'b0: No action 1'b1: Polling mode delay is in progress The application writes "1" to this bit to trigger the delay counter, when delay time elapsed, this bit is de-asserted.
30:0	RW	0x0003ffff	CNT Counter The target delay counter to trigger the polling command. The unit is based on HCLK.

FSPI_RX_FULL_WTMRK

Address: **Operational Base** + offset (0x0070)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x01	INDRT_RX_FULL_WTMRK Indirect Access Mode Receiver FIFO Water Mark. Default is enough.
15:8	RO	0x00	reserved
7:0	RW	0x02	XIP_RX_FULL_WTMRK Memory Mapped Mode Receiver FIFO Water Mark. Default is enough.

FSPI_DUMM_CTRL

Address: **Operational Base** + offset (0x0074)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:1	RW	0x00	DUMM_EXT Dummy Cycles 7'h0: No dummy cycle ... 7'h8: 8 cycles ... 7'h127: 127 cycles Dummy bit cycles in indirect access mode.
0	RW	0x0	DUMM_SEL Dummy Cycle Control Selection 1'b0: Dummy Cycle controlled by CMD[DUMM] 1'b1: Dummy Cycle controlled by DUMM_EXT

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FSPI_CMD_EXT

Address: **Operational Base** + offset (0x0078)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	CMDF_EXT Command Command data in indirect access mode when command length is 16 bits.

FSPI_TRC_CTRL

Address: **Operational Base** + offset (0x007C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:1	RW	0x0000	TRC_CYCLE The minimum transfer cycle 16'd0: 1 Cycle 16'd1: 2 Cycles ..... 16'd100: 101 Cycles ..... The target cycles to hold the controller in working state in a transfer.
0	RW	0x0	TRC_EN The minimum cycle in a transfer enable 1'b0: disable 1'b1: enable

FSPI_DMATR

Address: **Operational Base** + offset (0x0080)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1C	0x0	DMATR DMA Trigger Write "1" to start the DMA transfer.

FSPI_DMAADDR

Address: **Operational Base** + offset (0x0084)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMAADDR DMA Address The destination or source data address in current system.

FSPI_LEN_CTRL

Address: **Operational Base** + offset (0x0088)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	TRB_SEL Total Transfer Bytes Selection 1'b0: TRB controlled by CMD[TRB] 1'b1: TRB controlled by LEN_EXT

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FSPI_LEN_EXT
Address: **Operational Base** + offset (0x008C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TRB_EXT Total Transfer Bytes Extended 32'd0: No data 32'd1: 1 Byte 32'd2: 2 Bytes ... Total data bytes number that will write to /read from the device.

FSPI_XMMCSR
Address: **Operational Base** + offset (0x0094)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	R/WSC	0x0	SLOPOVER1 Slop Over Register for CS1 1'b0: Normal state 1'b1: Address slop over When the access address in memory map mode is bigger than DEVSIZE, this bit will be set. Write "1" to clear this bit.
0	R/WSC	0x0	SLOPOVER0 Slop Over Register for CS0 1'b0: Normal state 1'b1: Address slop over When the access address in memory map mode is bigger than DEVSIZE, this bit will be set. Write "1" to clear this bit.

FSPI_HYPER_RSVD_ADDR
Address: **Operational Base** + offset (0x0098)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	HYPER_RSVD_ADDR Hyperbus Reserved Address Bit

FSPI_VDMC0
Address: **Operational Base** + offset (0x009C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	MID MID 4'h1: Infineon/Cypress 4'h3: ISSI 4'h6: Winbond 4'hd: APM Others: Reserved

FSPI_DBG_IO_CTRL
Address: **Operational Base** + offset (0x00A0)

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Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	DLL_DBG_EN Delayline IO Debug Enable 1'b0 : Disable 1'b1 : Enable
15:4	RO	0x000	reserved
3:2	RW	0x0	DBG_OUT1_MUX Debug IO0 Output Mux 2'b00 : Output Data[2] 2'b01 : Output Data[3] 2'b10 : Output Clock
1:0	RW	0x0	DBG_OUT0_MUX Debug IO0 Output Mux 2'b00 : Output Data[0] 2'b01 : Output Data[1] 2'b10 : Output Clock

FSPI_DEV_RSTN

Address: **Operational Base** + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0xf	DEV_RSTN The RESET# Control Signal DEV_RSTN[0] : CS0 RESET# Control Signal ; DEV_RSTN[1] : CS1 RESET# Control Signal ; DEV_RSTN[2] : CS2 RESET# Control Signal ; DEV_RSTN[3] : CS3 RESET# Control Signal ;

FSPI_SLF_DQS_CTRL

Address: **Operational Base** + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	SLF_BLD_DQS_EN1 CS1 Self-build DQS Enable 1'b0 : Use Device DQS to sample the data 1'b1 : Use Self-build DQS to sample the data
15:1	RO	0x0000	reserved
0	RW	0x0	SLF_BLD_DQS_EN0 CS0 Self-build DQS Enable 1'b0 : Use Device DQS to sample the data 1'b1 : Use Self-build DQS to sample the data

FSPI_TRNS_TR_CTRL

Address: **Operational Base** + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
14:8	RO	0x00	TX_FIFO_DNUM TX FIFO Data Number 7'h0: FIFO is empty 7'h1: 1 entry is taken ... 7'h10: 16 entry is taken ...
7:1	RO	0x00	reserved
0	RW	0x0	TRNS_TR_MODE Transfer Trigger Mode 1'b0: Use CMD register writing to trigger the transfer; 1'b1: Use TRNS_TR register writing to trigger the transfer.

FSPI_TRNS_TR

Address: **Operational Base** + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1C	0x0	TRNS_TR Transfer Trigger Write "1" to start the transfer, when set TRNS_TR_CTRL[TRNS_MODE] to 1.

FSPI_DMA_CHAIN_TR

Address: **Operational Base** + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	DMA_CHAIN_TR DMA Chain Trigger Write "1" to start the DMA Chain transfer. When read this register, it can show the state of chain work state.

FSPI_DMA_HEAD_ADDR

Address: **Operational Base** + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMA_HEAD_ADDR DMA Chain Head Node Address

FSPI_DMA_CTRL

Address: **Operational Base** + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	DMA_BURST_TYPE DMA AHB Burst Type 2'b00: INCR4 2'b01: INCR8 2'b10: INCR16 (RX is not supported this Type)

FSPI_FSPI_IDLE

Address: **Operational Base** + offset (0x00C0)

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Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	FSPI_IDLE FSPI IDLE State 1'b0: FSPI is working 1'b1: FSPI is IDLE

FSPI_TX_DLL_CTRL0

Address: **Operational Base** + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	TX_DLL_SEL TX SCLK Delayline Selection 1'b0: Bypass DLL 1'b1: From DLL The TX SCLK source selection.
15:6	RO	0x000	reserved
5:0	RW	0x01	TX_DLL_CFG TX Delay Line Configuration 6'h0: 1 DLL element cell 6'h1: 1 DLL element cell 6'h2: 2 DLL element cells ... 6'h3f: 63 DLL element cells This register to control the TX SCLK delay line cell used. The maximum DLL element cells is decided by process.

FSPI_CMD

Address: **Operational Base** + offset (0x0100)

Bit	Attr	Reset Value	Description
31:30	WO	0x0	CS Device Chip Select. 2'b00: Chip select 0 2'b01: Chip select 1 2'b10: Reserved 2'b11: Reserved
29:16	WO	0x0000	TRB Total Transfer Bytes 14'd0: No data 14'd1: 1 Byte 14'd2: 2 Bytes ... Total data bytes number that will write to or read from the device.
15:14	WO	0x0	ADDRB Address Bits 2'b00: 0 bit 2'b01: 24 bits 2'b10: 32 bits 2'b11: From the ABIT register Address bits number select in indirect access mode. If there is not address command to send, set to zero.

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Bit	Attr	Reset Value	Description
13	WO	0x0	CONT Continuous 1'b0: Disable continuous mode 1'b1: Enable continuous mode AX mode or Continuous mode or XIP mode for device which begins with address.
12	WO	0x0	WR Write or Read 1'b0: Read 1'b1: Write
11:8	WO	0x0	DUMM Dummy Cycles 4'h0: No dummy cycle ... 4'h8: 8 cycles ... Dummy bit cycles in indirect access mode.
7:0	WO	0x00	CMD Command Command data in indirect access mode.

FSPI_ADDR

Address: **Operational Base** + offset (0x0104)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	ADDR Address Register Indirect access start address data for current command sequence.

FSPI_DATA

Address: **Operational Base** + offset (0x0108)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DATA Data Register Device data read or write from/to device.

FSPI_CTRL1

Address: **Operational Base** + offset (0x0200)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	WP_EN WP# Port Enable 1'b0: Disable 1'b1: Enable. The WP# port will always be driven by QOP[SO123] when QOP[SO123BP] is set to disable.

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Bit	Attr	Reset Value	Description
28:27	RW	0x0	CMD_CTRL Indirect Command Field Controll 2'b00: Command controlled by CMD[CMD] 2'b01: Command controlled by CMD[CMD] and combine with 8 bit address 2'b10: Command controlled by CMD_EXT/XMMC_WCMD/XMMC_RCMD[CMDF_EXT] according to different mode. Command length is 16 bit 2'b11: Reserved
26	RW	0x0	HYPER_RSVD_EN Hyperbus Reserved Address Bit Enable 1'b0: Disable 1'b1: Enable
25	RW	0x0	HYPER_ADDR_EN Address Remap in Hyperbus Mode 1'b0: Disable 1'b1: Enable
24	RW	0x0	INTRNL_CLK_MODE Internal Clock Mode 1'b0: Use the IOBUF CORE_CLK to Sample the Data 1'b1: Use the SCLK from IOPAD to Sample the Data
23:22	RW	0x0	DUMM_OVLP Dummy Phase Overlap with Address Phase. 3'd0: Dummy phase will start after address phase 3'd1: Dummy phase will overlap a cycle with address phase 3'd2: Dummy phase will overlap 2 cycles with address phase 3'd2: Dummy phase will overlap 3 cycles with address phase To set the overlap cycles between dummy phase and address phase.
21	RW	0x0	DBL_DUMM_CTRL Double dummy cycle controller 1'b0: dummy cycle always equal to CMD[DUMM] 1'b1: dummy cycle will be twice of CMD[DUMM] when dqs is high
20	RW	0x0	ADDR_STR Cmd phase work in STR mode in DTR mode. 1'b0: Disable 1'b1: Enable. The CTRL0/1[DTR_MODE] must set to 1'b1
19	RW	0x0	CMD_STR Cmd phase work in STR mode in DTR mode. 1'b0: Disable 1'b1: Enable. The CTRL0/1[DTR_MODE] must set to 1
18	RW	0x0	DTR_RDC_SEL Read Clock Select in DTR Mode 1'b0: use DQS to sample the data 1'b1: use SCLK to sample the data
17	RW	0x0	DQS_MODE DQS MODE 1'b0: DQS can be driven by controller and device 1'b1: DQS is always driven by device
16	RW	0x0	DATAB16 16 Bit Data Line Width. 1'b0: Data Line Width controlled by CTRL0[DATB] 1'b1: 16 bits, x16 mode

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Bit	Attr	Reset Value	Description
15	RW	0x0	ADRB16 16 Bit Address Line Width. 1'b0: Address Line Width controlled by CTRL0[ADRB] 1'b1: 16 bits, x16 mode
14	RW	0x0	CMDB16 16 Bit Command Line Width. 1'b0: Command Line Width controlled by CTRL0[CMDB] 1'b1: 16 bits, x16 mode
13:12	RW	0x0	DATB Data Line Width 2'b00: 1 bit, x1 mode 2'b01: 2 bits, x2 mode 2'b10: 4 bits, x4 mode 2'b11: Reserved Set this DATB to match the CMD sequence before doing indirect access mode and memory mapped access mode.
11:10	RW	0x0	ADRB Address Line Width 2'b00: 1 bit, x1 mode 2'b01: 2 bits, x2 mode 2'b10: 4 bits, x4 mode 2'b11: Reserved Set this ADRB to match the CMD sequence before doing indirect access mode and memory mapped access mode.
9:8	RW	0x0	CMDB Command Line Width 2'b00: 1 bit, x1 mode 2'b01: 2 bits, x2 mode 2'b10: 4 bits, x4 mode 2'b11: Reserved Set this CMDB to match the CMD sequence before doing indirect access mode and memory mapped access mode.
7:4	RW	0x0	IDLE_CYCLE Idle Cycles When Switching IO from Output to Input 4'h0: Idle hold is disable 4'h1: Hold the SCLK in idle for 2 cycles when switch to shift in ... 4'hf: Hold the SCLK in idle for 16 cycles when switch to shift in To improve the transform IO timing, the application can set this register to hold the SCLK in low state or high state.
3	RW	0x0	DAT_ORDER The Order of Data in a Cycle 1'b0: Date in a cycle is from low byte to high byte 1'b1: Date in a cycle is from high byte to low byte
2	RW	0x0	DTR_MODE DTR mode enable 1'b0: STR mode 1'b1: DTR mode
1	RW	0x0	SHIFTPHASE Shift Phase of Data Input in Controller 1'b0: Shift input data at posedge SCLK 1'b1: Shift input data at negedge SCLK The application can select the input data captured by posedge of SCLK when "0" or negedge of SCLK when "1".

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Bit	Attr	Reset Value	Description
0	RW	0x0	SPIM Serial Peripheral Interface Mode 1'b0: Mode 0 1'b1: Mode 3 SPIM is used to control the serial mode (CPOL and CPHA). CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

FSPI_AX1

Address: **Operational Base** + offset (0x0214)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	AX Auxiliary Data The AX value when doing the continuous read (enhance mode or XIP mode). That is M7-M0 in "Continuous Read Mode".

FSPI_ABIT1

Address: **Operational Base** + offset (0x0218)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	ABIT Address Bits Extend 6'h0: 1 bit 6'h1: 2 bits ... 6'h3f: 64 bits When ADDRB have no option for address bits number, use this field to set the right address bits number. Only valid when ADDRB is set to 2'b11.

FSPI_DLL_CTRL1

Address: **Operational Base** + offset (0x023C)

Bit	Attr	Reset Value	Description
31	RW	0x0	DQS1_SMP_SEL DQS1 Sampling Selection 1'b0: Bypass DLL 1'b1: From DLL The sampling DQS1 source selection.
30:25	RO	0x00	reserved
24:16	RW	0x000	DQS1_DLL_CFG DQS1 Delay Line Configuration 9'h0: 1 DLL element cell 9'h1: 1 DLL element cell 9'h2: 2 DLL element cells ... 9'h1ff: 511 DLL element cells This register to control the sampling delay line cell used. The maximum DLL element cells is decided by process.

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Bit	Attr	Reset Value	Description
15	RW	0x0	SCLK_SMP_SEL SCLK sampling selection 1'b0: Bypass DLL 1'b1: From DLL The sampling SCLK source selection.
14:9	RO	0x00	reserved
8:0	RW	0x001	SMP_DLL_CFG Sample Delay Line Configuration 9'h0: 1 DLL element cell 9'h1: 1 DLL element cell 9'h2: 2 DLL element cells ... 9'h1ff: 511 DLL element cells This register to control the sampling delay line cell used. The maximum DLL element cells is decided by process.

FSPI_XMMC_WCMD1

Address: **Operational Base** + offset (0x0250)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	CMDF_EXT Command Command data in memory mapped access mode when command length is 16 bits.
15:14	WO	0x0	ADDRB Address Bits 2'b00: 0 bit 2'b01: 24 bits 2'b10: 32 bits 2'b11: From the ABIT register Address bits number select in memory mapped mode, if there is not address command to send, set to zero.
13	WO	0x0	CONT Continuous 1'b0: Disable continuous mode 1'b1: Enable continuous mode AX mode or Continuous mode or XIP mode for device which begins with address.
12	RO	0x0	reserved
11:8	WO	0x0	DUMM Dummy Cycles 4'h0: No dummy cycle ... 4'h8: 8 cycles ... Dummy bit cycles in memory mapped mode.
7:0	WO	0x00	CMD Command Command data in memory mapped access mode.

FSPI_XMMC_RCMD1

Address: **Operational Base** + offset (0x0254)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	CMDF_EXT Command Command data in memory mapped access mode when command length is 16 bits.
15:14	WO	0x0	ADDRB Address Bits 2'b00: 0 bit 2'b01: 24 bits 2'b10: 32 bits 2'b11: From the ABIT register Address bits number select in memory mapped mode, if there is not address command to send, set to zero.
13	WO	0x0	CONT Continuous 1'b0: Disable continuous mode 1'b1: Enable continuous mode AX mode or Continuous mode or XIP mode for device which begins with address.
12	RO	0x0	reserved
11:8	WO	0x0	DUMM Dummy Cycles 4'h0: No dummy cycle ... 4'h8: 8 cycles ... Dummy bit cycles in memory mapped mode.
7:0	WO	0x00	CMD Command Command data in memory mapped access mode.

FSPI_DEVSIZE1

Address: **Operational Base** + offset (0x0264)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x12	DSIZE Device Size 5'd0: 1 byte 5'd1: 2 bytes 5'd2: 4 bytes ..... 5'd10: 1K bytes ..... 5'd20: 1M bytes ..... 5'd31: 4G bytes Device size is used to generate slop over status.

FSPI_TME1

Address: **Operational Base** + offset (0x0268)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x0	SCLK_INATM_EN SCLK Inactive Timeout Enable 1'b0: Disable 1'b1: Enable
0	RO	0x0	reserved

FSPI_VDMC1

Address: **Operational Base** + offset (0x029C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	MID MID 4'h1: Infineon/Cypress 4'h3: ISSI 4'h6: Winbond 4'hd: APM Others: Reserved

FSPI_TX_DLL_CTRL1

Address: **Operational Base** + offset (0x02C4)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	TX_DLL_SEL TX SCLK Delayline Selection 1'b0: Bypass DLL 1'b1: From DLL The TX SCLK source selection.
15:6	RO	0x000	reserved
5:0	RW	0x00	TX_DLL_CFG TX Delay Line Configuration 6'h0: 1 DLL element cell 6'h1: 1 DLL element cell 6'h2: 2 DLL element cells ... 6'h3f: 63 DLL element cells This register to control the TX SCLK delay line cell used. The maximum DLL element cells is decided by process.

33.5 Interface Description

Table 33-1 FSPI0 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
sfc_sclk	O	GPIO1_B7	GPIO1B_IOMUX_SEL_1[15:12]=4'h1
sfc_csn0	O	GPIO1_B0	GPIO1B_IOMUX_SEL_0[3:0]=4'h1
sfc_csn1	O	GPIO1_A5	GPIO1A_IOMUX_SEL_1[7:4]=4'h2
sfc_sio0	I/O	GPIO1_B4	GPIO1B_IOMUX_SEL_1[3:0]=4'h1
sfc_sio1	I/O	GPIO1_B5	GPIO1B_IOMUX_SEL_1[7:4]=4'h1
sfc_sio2	I/O	GPIO1_B2	GPIO1B_IOMUX_SEL_0[11:8]=4'h1
sfc_sio3	I/O	GPIO1_B6	GPIO1B_IOMUX_SEL_1[11:8]=4'h1

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Table 33-2 FSPI1 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
IOMUX0			
sfc_sclk	O	GPIO0_B2	GPIO0B_IOMUX_SEL_0[11:8]=4'h1
sfc_csn	O	GPIO0_A7	GPIO0A_IOMUX_SEL_1[15:12]=4'h1
sfc_sio0	I/O	GPIO0_B0	GPIO0B_IOMUX_SEL_0[3:0]=4'h1
sfc_sio1	I/O	GPIO0_B1	GPIO0B_IOMUX_SEL_0[7:4]=4'h1
sfc_sio2	I/O	GPIO0_A6	GPIO0A_IOMUX_SEL_1[11:8]=4'h1
sfc_sio3	I/O	GPIO0_A1	GPIO0A_IOMUX_SEL_0[7:4]=4'h1
IOMUX1			
sfc_sclk	O	GPIO1_B3	GPIO1B_IOMUX_SEL_0[15:12]=4'h2
sfc_csn	O	GPIO1_B1	GPIO1B_IOMUX_SEL_0[7:4]=4'h2
sfc_sio0	I/O	GPIO1_A0	GPIO1A_IOMUX_SEL_0[3:0]=4'h2
sfc_sio1	I/O	GPIO1_A1	GPIO1A_IOMUX_SEL_0[7:4]=4'h2
sfc_sio2	I/O	GPIO1_A2	GPIO1A_IOMUX_SEL_0[11:8]=4'h2
sfc_sio3	I/O	GPIO1_A3	GPIO1A_IOMUX_SEL_0[15:12]=4'h2

Notes: I=input, O=output, I/O=input/output, bidirectional

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33.6 Application Notes

33.6.1 Typical Program Flow Without DMA

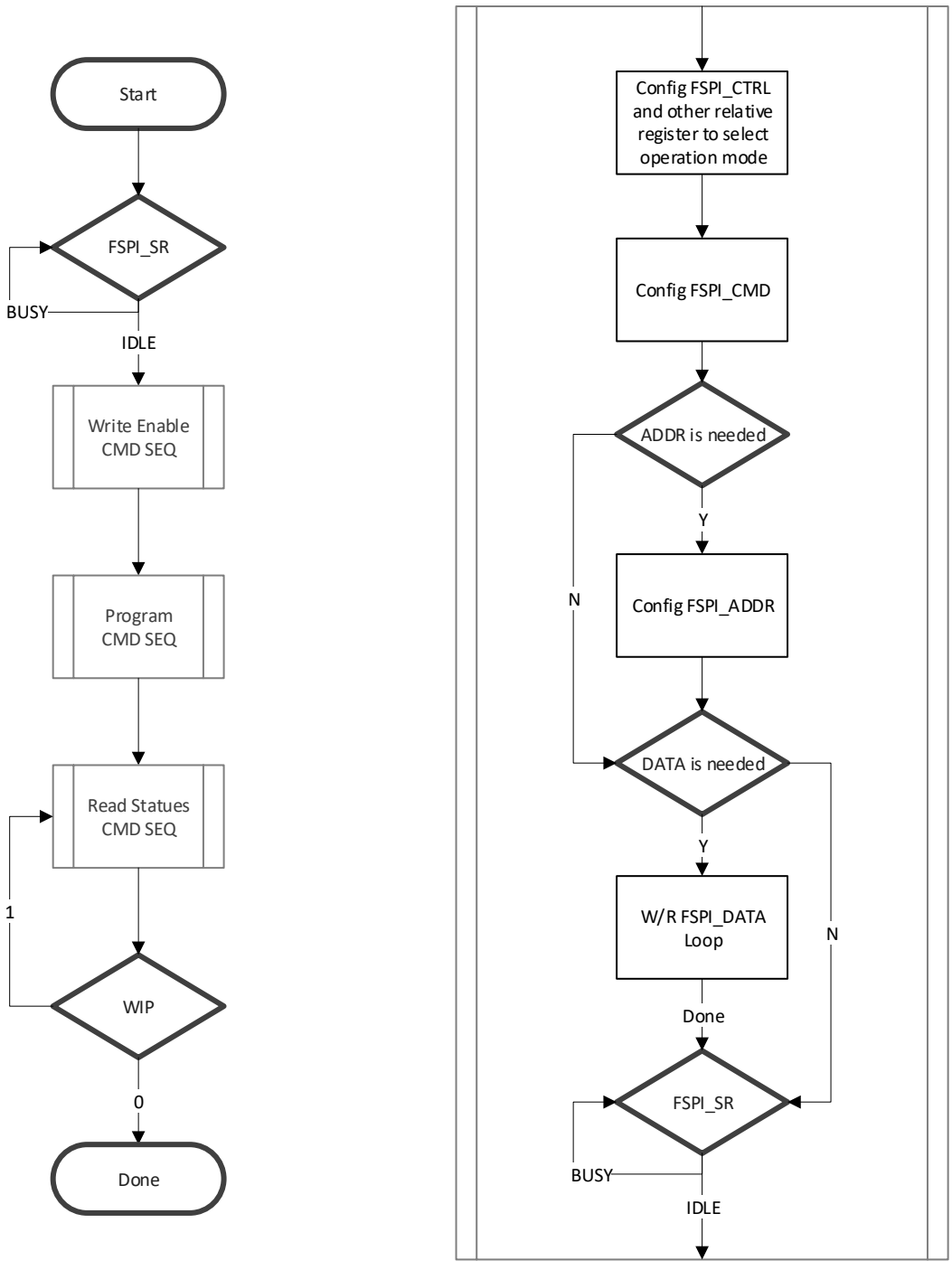

Fig. 33-2 Program Flow

All the AHB bus write data to FSPI_CMD, FSPI_ADDR and FSPI_DATA will be marked with different header and then pushed into transmit FIFO by writing order.

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33.6.2 Typical READ Flow Without DMA

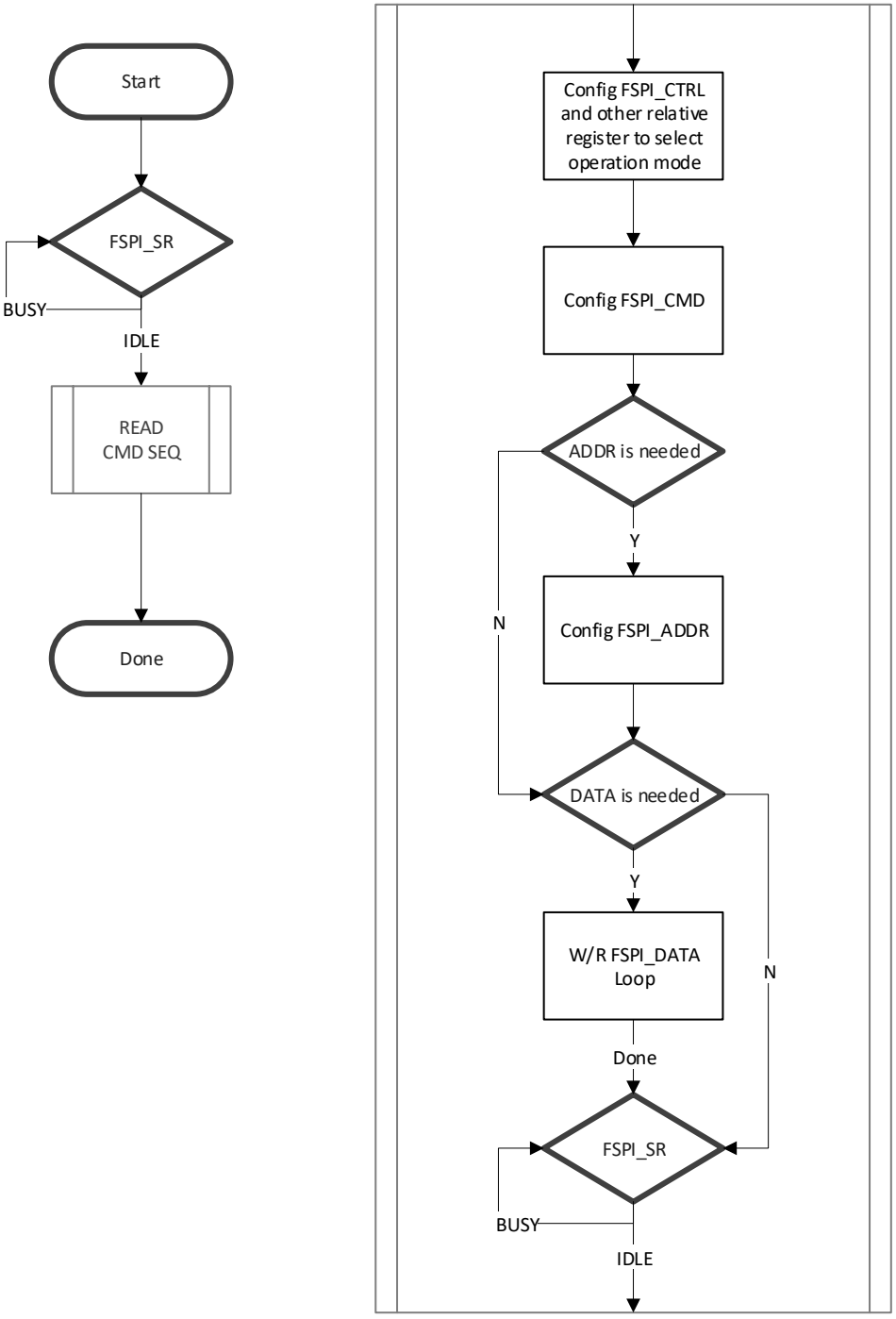

Fig. 33-3 Read Flow

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33.6.3 Command Flow with DMA

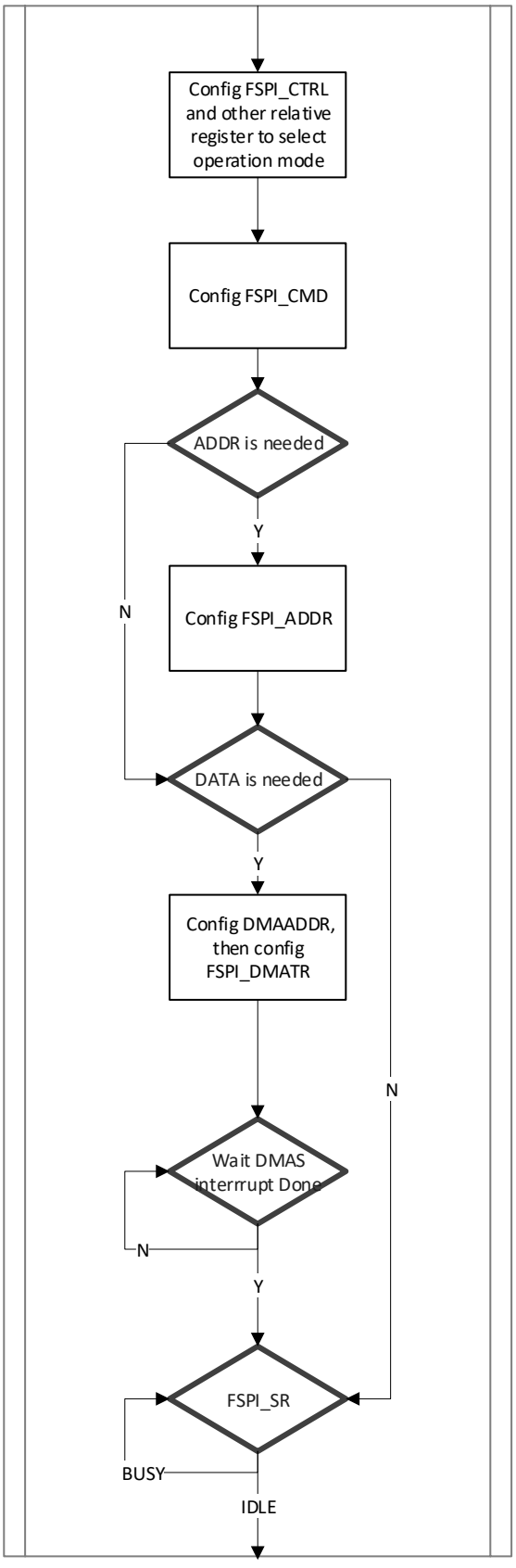

Fig. 33-4 Command with DMA Flow

The total transfer bytes is decided by TRB register in FSPI_CMD and must be aligned to 2 bytes.

33.6.4 SPI Mode and Sampling Phase Control

The register SPIM in FSPI_CTRL will decide the default value of SCLK when CS# is inactive. When SPIM=0, the default value is 0, means Mode 0. When SPIM=1, the default

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value is 1, means SPI Mode 3.

The register SHIFTPAHSE in FSPI_CTRL will decide when to sample the SIO data. If SHIFTPAHSE=0, it will sample the data at the posedge of SCLK sampling clock. If SHIFTPHASE=1, it will sample the data at the negedge of SCLK sampling. The phase delay of sampling clock SCLK is configurable by SMP_DLL_CFG. It is strongly recommended that the SMP_DLL_CFG is set to 1 when SCLK_SMP_SEL is in bypass mode.

Individual FSPI_DLL_CTRL[n] allows flexibly control the DLL for each CSn channel, and the DLL is switched dynamically when the CSn is in operation.

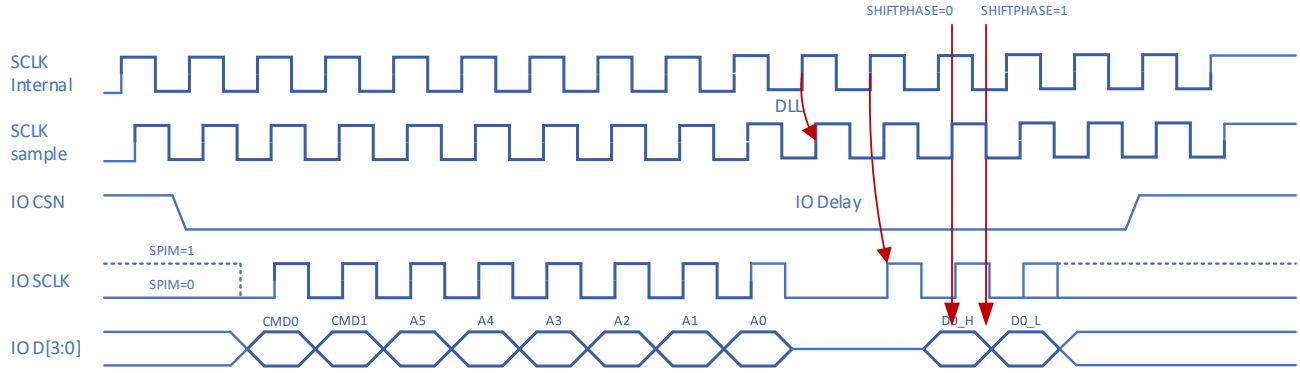

Fig. 33-5 SPI mode

33.6.5 Idle Cycles

The FSPI_CTRL register is a global control register, when the controller is in busy state (FSPI_SR), FSPI_CTRL cannot be set. The field IDLE_CYCLE (FSPI_CTRL[7:4]) of this register are used to configure the idle level cycles of FSPI core clock (SCLK) before reading the first bit of the read command.

Like the following picture shows, the highlighted line of the SCLK is the idle cycles, during these cycles, the chip pad is switched to output. When IDLE_CYCLE=0, it means there will be no idle level cycles.

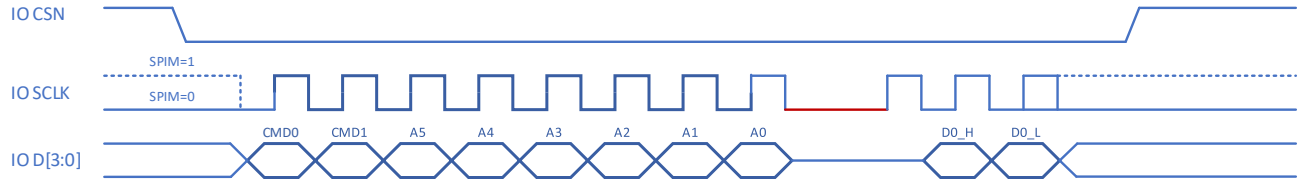

Fig. 33-6 Idle cycles

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Chapter 34 Serial Peripheral Interface (SPI)

34.1 Overview

The serial peripheral interface is an APB slave device. There are four possible combinations for the serial clock phase and polarity. The clock phase (SCPH) determines whether the serial transfer begins with the falling edge of slave select signals or the first edge of the serial clock. The slave select line is held high when the SPI is idle or disabled. This SPI controller can work as either master or slave mode.

SPI Controller supports the following features:

- Support 2 independent SPI: SPI0~1
- Support Motorola SPI, TI Synchronous Serial Protocol and National Semiconductor Micro wire interface
- Support 32-bit APB bus
- Support two internal 16-bit wide and 64-location deep FIFOs, one for transmitting and the other for receiving serial data
- Support two chip select signals in master mode
- Support 4,8,16 bit serial data transfer
- Support configurable interrupt polarity
- Support asynchronous APB bus and SPI clock
- Support master and slave mode
- Support DMA handshake interface and configurable DMA water level
- Support transmit FIFO empty, underflow, receive FIFO full, overflow, interrupt and all interrupts can be masked
- Support configurable water level of transmit FIFO empty and receive FIFO full interrupt
- Support combining interrupt output
- Support up to half of SPI clock frequency transfer in master mode and one quarter of SPI clock frequency transfer in slave mode
- Support full and half duplex mode transfer
- Support one shared I/O for TX or RX transmision in half-duplex mode, MOSI for master mode and MISO for slave mode
- Stop transmitting SCLK if transmit FIFO is empty or receive FIFO is full in master mode
- Support configurable delay from chip select active to SCLK active in master mode
- Support configurable period of chip select inactive between two parallel data in master mode
- Support big and little endian, MSB and LSB first transfer
- Support two 8-bit audio data store together in one 16-bit wide location
- Support sample MISO 0~3 SPI clock cycles later
- Support configurable SCLK polarity and phase
- Support fix and incremental address access to transmit and receive FIFO
- Support timeout mechanism in slave mode
- Support BYPASS slave mode, in which MISO and MOSI logic is drive by sclk_in directly instead of spi_clk

34.2 Block Diagram

The SPI Controller comprises with:

- AMBA APB interface and DMA Controller Interface
- Transmit and receive FIFO controllers and an FSM controller
- Register block
- Shift control and interrupt

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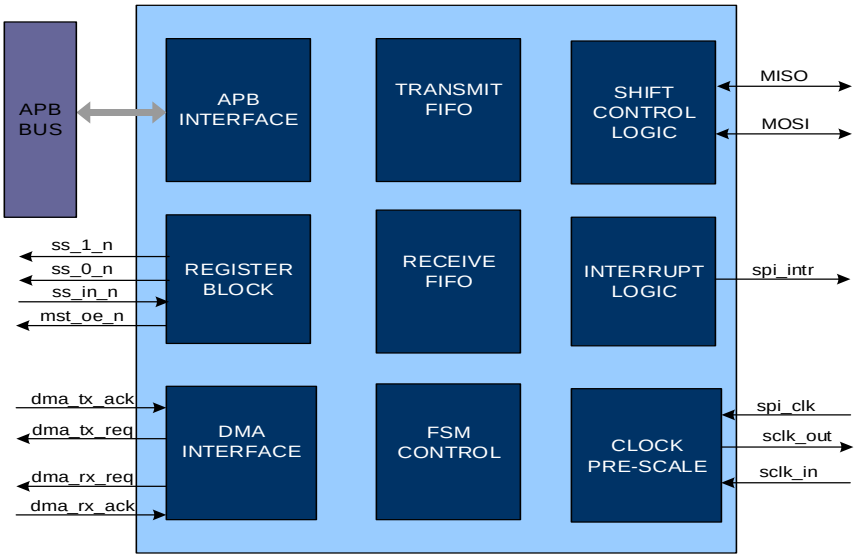

Fig. 34-1 SPI Controller Block Diagram

APB INTERFACE

The host processor accesses data, control, and status information on the SPI through the APB interface. The SPI supports APB data bus widths of 32 bits and 8 or 16 bits when reading or writing internal FIFO if data frame size (SPI_CTRL0[1:0]) is set to 8 bits.

DMA INTERFACE

This block has a handshaking interface to a DMA Controller to request and control transfers. The APB bus is used to perform the data transfer to or from the DMA Controller.

FIFO LOGIC

For transmit and receive transfers, data transmitted from the SPI to the external serial device is written into the transmit FIFO. Data received from the external serial device into the SPI is pushed into the receive FIFO. Both FIFOs are 64x16bits.

FSM CONTROL

Control the state’s transformation of the design.

REGISTER BLOCK

All registers in the SPI are addressed at 32-bit boundaries to remain consistent with the APB bus. Where the physical size of any register is less than 32-bits wide, the upper unused bits of the 32-bit boundary are reserved. Writing to these bits has no effect; reading from these bits returns 0.

SHIFT CONTROL

Shift control logic shift the data from the transmit FIFO or to the receive FIFO. This logic automatically right-justifies receive data in the receive FIFO buffer.

INTERRUPT CONTROL

The SPI supports combined and individual interrupt requests, each of which can be masked. The combined interrupt request is the OR relationship between all other SPI interrupts after masking.

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34.3 Function Description

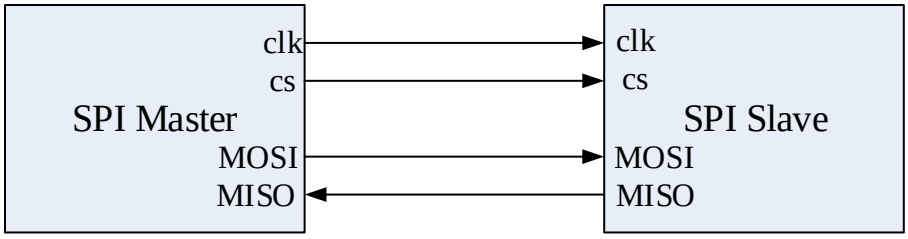

Fig. 34-2 SPI Master and Slave Interconnection

The SPI controller supports dynamic switching between master and slave in a system. The diagram shows how the SPI controller connects with other SPI devices.

Operation Modes

The SPI can be configured in the following two fundamental modes of operation: Master Mode when SPI_CTRLR0 [20] is 1'b0, Slave Mode when SPI_CTRLR0 [20] is 1'b1.

Transfer Modes

The SPI operates in the following three modes when transferring data on the serial bus.
1). Transmit and Receive
When SPI_CTRLR0 [19:18] == 2'b00, both transmit and receive logic are valid.
2). Transmit Only
When SPI_CTRLR0 [19:18] == 2'b01, the receive data are invalid and should not be stored in the receive FIFO.
3). Receive Only
When SPI_CTRLR0 [19:18] == 2'b10, the transmit data are invalid.

Clock Ratios

A summary of the frequency ratio restrictions between the bit-rate clock (sclk_out/sclk_in) and the SPI peripheral clock (spi_clk) are described as:
When SPI Controller works as master, the F_{spi_clk}>= 2 × (maximum F_{sclk_out})
When SPI Controller works as slave, the F_{spi_clk}>= 4 × (maximum F_{sclk_in})

With the SPI, the clock polarity (SCPOL) configuration parameter determines whether the inactive state of the serial clock is high or low. To transmit data, both SPI peripherals must have identical serial clock phase (SCPH) and clock polarity (SCPOL) values. The data frame can be 4/8/16 bits in length.

When the configuration parameter SCPH = 0, data transmission begins on the falling edge of the slave select signal. The first data bit is captured by the master and slave peripherals on the first edge of the serial clock; therefore, valid data must be present on the MISO and MOSI lines prior to the first serial clock edge. The following two figures show a timing diagram for a single SPI data transfer with SCPH = 0. The serial clock is shown for configuration parameters SCPOL = 0 and SCPOL = 1.

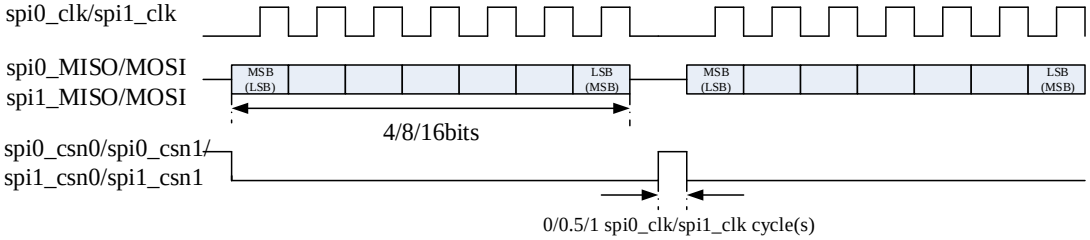

Fig. 34-3 SPI Format (SCPH=0 SCPOL=0)

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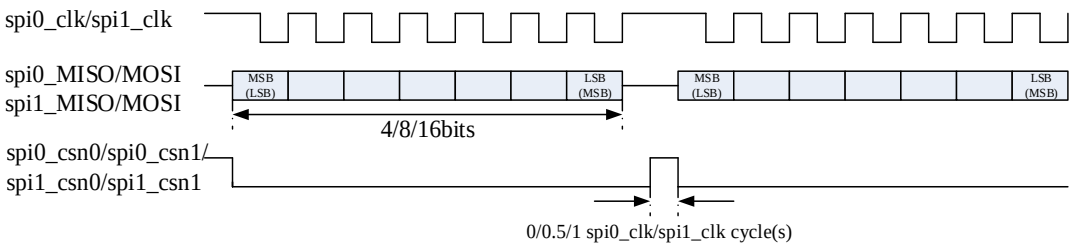

Fig. 34-4 SPI Format (SCPH=0 SCPOL=1)

When the configuration parameter SCPH = 1, both master and slave peripherals begin transmitting data on the first serial clock edge after the slave select line is activated. The first data bit is captured on the second (trailing) serial clock edge. Data are propagated by the master and slave peripherals on the leading edge of the serial clock. During continuous data frame transfers, the slave select line may be held active-low until the last bit of the last frame has been captured. The following two figures show the timing diagram for the SPI format when the configuration parameter SCPH = 1.

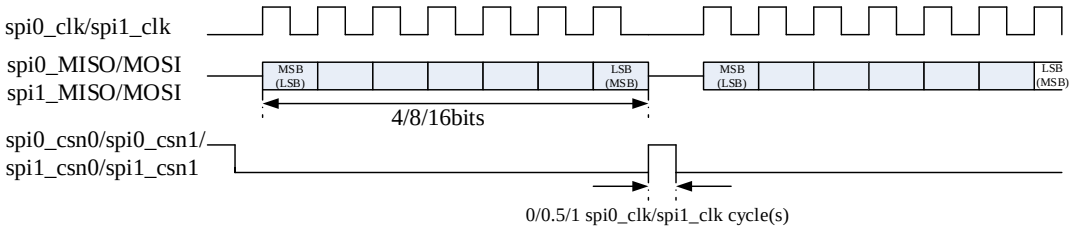

Fig. 34-5 SPI Format (SCPH=1 SCPOL=0)

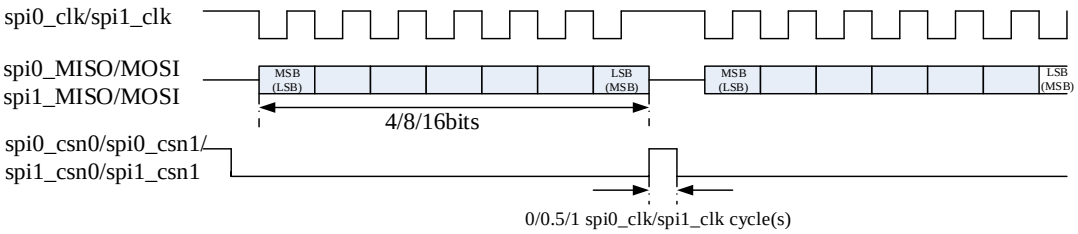

Fig. 34-6 SPI Format (SCPH=1 SCPOL=1)

34.4 Register Description

34.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
SPI0	0x211E0000
SPI1	0x211F0000

34.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SPI_CTRLR0	0x0000	W	0x00000002	Control Register 0
SPI_CTRLR1	0x0004	W	0x00000000	Control Register 1
SPI_ENR	0x0008	W	0x00000000	SPI Enable Register
SPI_SER	0x000C	W	0x00000000	Slave Enable Register
SPI_BAUDR	0x0010	W	0x00000000	Baud Rate Select
SPI_TXFTLR	0x0014	W	0x00000000	Transmit FIFO Threshold Level
SPI_RXFTLR	0x0018	W	0x00000000	Receive FIFO Threshold Level
SPI_TXFLR	0x001C	W	0x00000000	Transmit FIFO Level
SPI_RXFLR	0x0020	W	0x00000000	Receive FIFO Level
SPI_SR	0x0024	W	0x0000004C	SPI Status

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Name	Offset	Size	Reset Value	Description
SPI_IPR	0x0028	W	0x00000000	Interrupt Polarity
SPI_IMR	0x002C	W	0x00000000	Interrupt Mask
SPI_ISR	0x0030	W	0x00000000	Interrupt Status
SPI_RISR	0x0034	W	0x00000001	Raw Interrupt Status
SPI_ICR	0x0038	W	0x00000000	Interrupt Clear
SPI_DMACR	0x003C	W	0x00000000	DMA Control
SPI_DMATDLR	0x0040	W	0x00000000	DMA Transmit Data Level
SPI_DMARDLR	0x0044	W	0x00000000	DMA Receive Data Level
SPI_VERSION	0x0048	W	0x03120003	IP Version
SPI_TIMEOUT	0x004C	W	0x00000000	Timeout Control Register
SPI_BYPASS	0x0050	W	0x00000000	Bypass Control Register
SPI_BPENR	0x0054	W	0x00000000	SPI Bypass Enable Register
SPI_TXDR	0x0400	W	0x00000000	Transmit FIFO Data
SPI_RXDR	0x0800	W	0x00000000	Receive FIFO Data

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

34.4.3 Detail Registers Description

SPI_CTRLR0

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RW	0x0	fdoen Output enables for TX-RX full-duplex capability. 1'b0: Full-duplex 1'b1: Half-duplex. When SPI works in master mode, half-duplex IO is MOSI pad. When SPI works in slave mode, half-duplex IO is MISO pad.
25	RW	0x0	lbk Loop back mode select. 1'b0: Normal mode 1'b1: Loop back mode, rxd is connected to txd.
24:23	RW	0x0	soi Port ss_n output inverted. 1'b0: Corresponding bit of ss_in is not inverted 1'b1: Corresponding bit of ss_in is inverted
22	RW	0x0	sm Port sclk_in is masked by SS_N or not. When configured csm and scpol, disable this configuration. 1'b0: sclk_in is masked 1'b1: sclk_in is not masked
21	RW	0x0	mtm Valid when frame format is set to National Semiconductors Microwire. 1'b0: Non-sequential transfer 1'b1: Sequential transfer
20	RW	0x0	opm Master and slave mode select. 1'b0: Master mode 1'b1: Slave mode

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Bit	Attr	Reset Value	Description
19:18	RW	0x0	xfm Transmit and receive mode select. 2'b00: Transmit & Receive 2'b01: Transmit only 2'b10: Receive only 2'b11: Reserved
17:16	RW	0x0	frf 2'b00: Motorola SPI 2'b01: Texas Instruments SSP 2'b10: National Semiconductors Microwire 2'b11: Reserved
15:14	RW	0x0	rsd When SPI is configured as a master, if the rxd data cannot be sampled by the sclk_out edge at the right time, this register should be configured to define the number of the spi_clk cycles after the active sclk_out edge to sample rxd data later when SPI works at high frequency. 2'b00: Do not delay 2'b01: 1 cycle delay 2'b10: 2 cycles delay 2'b11: 3 cycles delay
13	RW	0x0	bht Valid when data frame size is 8bit. 1'b0: APB 16bit write/read, SPI 8bit write/read 1'b1: APB 8bit write/read, SPI 8bit write/read
12	RW	0x0	fbm 1'b0: First bit is MSB 1'b1: First bit is LSB
11	RW	0x0	em Serial endian mode can be configured by this bit. APB endian mode is always little endian. 1'b0: Little endian 1'b1: Big endian
10	RW	0x0	ssd Valid when the frame format is set to Motorola SPI and SPI used as a master. 1'b0: The period between ss_n active and sclk_out active is half sclk_out cycles 1'b1: The period between ss_n active and sclk_out active is one sclk_out cycle
9:8	RW	0x0	csm Valid when the frame format is set to Motorola SPI and SPI used as a master. 2'b00: ss_n keep low after every frame data is transferred 2'b01: ss_n be high for half sclk_out cycles after every frame data is transferred 2'b10: ss_n be high for one sclk_out cycle after every frame data is transferred 2'b11: Reserved
7	RW	0x0	scpol Valid when the frame format is set to Motorola SPI. 1'b0: Inactive state of serial clock is low 1'b1: Inactive state of serial clock is high

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Bit	Attr	Reset Value	Description
6	RW	0x0	scph Valid when the frame format is set to Motorola SPI. 1'b0: Serial clock toggles in middle of first data bit 1'b1: Serial clock toggles at start of first data bit
5:2	RW	0x0	cfs Selects the length of the control word for the Microwire frame format. 4'b0000~0010: Reserved 4'b0011: 4-bit serial data transfer 4'b0100: 5-bit serial data transfer 4'b0101: 6-bit serial data transfer 4'b0110: 7-bit serial data transfer 4'b0111: 8-bit serial data transfer 4'b1000: 9-bit serial data transfer 4'b1001: 10-bit serial data transfer 4'b1010: 11-bit serial data transfer 4'b1011: 12-bit serial data transfer 4'b1100: 13-bit serial data transfer 4'b1101: 14-bit serial data transfer 4'b1110: 15-bit serial data transfer 4'b1111: 16-bit serial data transfer
1:0	RW	0x2	dfs Selects the data frame length. Therein, The slave bypass mode does not support the 4bits data length. 2'b00: 4bit data 2'b01: 8bit data 2'b10: 16bit data 2'b11: Reserved

SPI_CTRLR1

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ndm When Transfer Mode is received only, this register field sets the number of data frames to be continuously received by the SPI. The SPI continues to receive serial data until the number of data frames received is equal to this register value plus 1, which enables you to receive up to 4GB of data in a continuous transfer.

SPI_ENR

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	enr Enables and disables all SPI operations. Transmit and receive FIFO buffers are cleared when the device is disabled.

SPI_SER

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	ser Slave enable register. The register enables the individual slave select output lines, 2 slave-select output pins are available.This register is valid only when SPI is configured as a master device.

SPI_BAUDR

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	baudr SPI Clock Divider. This register is valid only when the SPI is configured as a master device. The LSB for this field is always set to 0 and is unaffected by a write operation, which ensures an even value is held in this register. If the value is 0, the serial output clock (sclk_out) is disabled. The frequency of the sclk_out is derived from the following equation: Fsclk_out = Fspi_clk/SCKDV Where SCKDV is any even value between 2 and 65534. For example: for Fspi_clk = 3.6864MHz and SCKDV =2 Fsclk_out = 3.6864/2= 1.8432MHz

SPI_TXFTLR

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	txftlr When the number of transmit FIFO entries is less than or equal to this value, the transmit FIFO empty interrupt is triggered.

SPI_RXFTLR

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	rxftlr When the number of receive FIFO entries is greater than or equal to this value + 1, the receive FIFO full interrupt is triggered.

SPI_TXFLR

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RO	0x00	txflr Contains the number of valid data entries in the transmit FIFO. (Note: When the bypass slave scph is 1, the master cannot provide redundant clocks according to the SPI protocol. Therefore, The actual value is the read value minus one.)

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SPI_RXFLR

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RO	0x00	rxflr Contains the number of valid data entries in the receive FIFO.

SPI_SR

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RO	0x1	ssi 1'b0: ss_in_n is low 1'b1: ss_in_n is high
5	RO	0x0	stb 1'b0: Slave tx not busy 1'b1: Slave tx busy
4	RO	0x0	rff 1'b0: Receive FIFO is not full 1'b1: Receive FIFO is full
3	RO	0x1	rfe 1'b0: Receive FIFO is not empty 1'b1: Receive FIFO is empty
2	RO	0x1	tfe 1'b0: Transmit FIFO is not empty 1'b1: Transmit FIFO is empty
1	RO	0x0	tff 1'b0: Transmit FIFO is not full 1'b1: Transmit FIFO is full
0	RO	0x0	bsf When set, indicates that a serial transfer is in progress; when cleared, indicates that the SPI is idle or disabled. 1'b0: SPI is idle or disabled 1'b1: SPI is actively transferring data

SPI_IPR

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	ipr Interrupt Polarity Register. 1'b0: Active Interrupt Polarity Level is HIGH 1'b1: Active Interrupt Polarity Level is LOW

SPI_IMR

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	txfim 1'b0: TX finish interrupt is masked 1'b1: TX finish interrupt is not masked

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Bit	Attr	Reset Value	Description
6	RW	0x0	sspim 1'b0: ss_in_n posedge interrupt is masked 1'b1: ss_in_n posedge interrupt is not masked
5	RW	0x0	toim 1'b0: SPI timeout interrupt is masked 1'b1: SPI timeout interrupt is not masked
4	RW	0x0	rffim 1'b0: spi_rxf_intr interrupt is masked 1'b1: spi_rxf_intr interrupt is not masked
3	RW	0x0	rfoim 1'b0: spi_rxo_intr interrupt is masked 1'b1: spi_rxo_intr interrupt is not masked
2	RW	0x0	rfuim 1'b0: spi_rxu_intr interrupt is masked 1'b1: spi_rxu_intr interrupt is not masked
1	RW	0x0	tfoim 1'b0: spi_txo_intr interrupt is masked 1'b1: spi_txo_intr interrupt is not masked
0	RW	0x0	tfeim 1'b0: spi_txe_intr interrupt is masked 1'b1: spi_txe_intr interrupt is not masked

SPI_ISR

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	txfis 1'b0: TX finish interrupt is not active after masking 1'b1: TX finish interrupt is active after masking
6	RW	0x0	sspis 1'b0: ss_in_n posedge interrupt is not active after masking 1'b1: ss_in_n posedge interrupt is active after masking
5	RW	0x0	tois 1'b0: spi timeout interrupt is not active after masking 1'b1: spi timeout interrupt is active after masking
4	RO	0x0	rffis 1'b0: spi_rxf_intr interrupt is not active after masking 1'b1: spi_rxf_intr interrupt is full after masking
3	RO	0x0	rfois 1'b0: spi_rxo_intr interrupt is not active after masking 1'b1: spi_rxo_intr interrupt is active after masking
2	RO	0x0	rfuis 1'b0: spi_rxu_intr interrupt is not active after masking 1'b1: spi_rxu_intr interrupt is active after masking
1	RO	0x0	tfois 1'b0: spi_txo_intr interrupt is not active after masking 1'b1: spi_txo_intr interrupt is active after masking
0	RO	0x0	tfeis 1'b0: spi_txe_intr interrupt is not active after masking 1'b1: spi_txe_intr interrupt is active after masking

SPI_RISR

Address: **Operational Base** + offset (0x0034)

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Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	txfris 1'b0: TX finish interrupt is not active prior to masking 1'b1: TX finish interrupt is active prior to masking
6	RW	0x0	sspris 1'b0: ss_in_n posedge interrupt is not active prior to masking 1'b1: ss_in_n posedge interrupt is active prior to masking
5	RW	0x0	toris 1'b0: spi_timeout interrupt is not active prior to masking 1'b1: spi_timeout interrupt is active prior to masking
4	RO	0x0	rffris 1'b0: spi_rxf_intr interrupt is not active prior to masking 1'b1: spi_rxf_intr interrupt is full prior to masking
3	RO	0x0	rforis 1'b0: spi_rxo_intr interrupt is not active prior to masking 1'b1: spi_rxo_intr interrupt is active prior to masking
2	RO	0x0	rfuris 1'b0: spi_rxu_intr interrupt is not active prior to masking 1'b1: spi_rxu_intr interrupt is active prior to masking
1	RO	0x0	tforis 1'b0: spi_txo_intr interrupt is not active prior to masking 1'b1: spi_txo_intr interrupt is active prior to masking
0	RO	0x1	tferis 1'b0: spi_txe_intr interrupt is not active prior to masking 1'b1: spi_txe_intr interrupt is active prior to masking

SPI_ICR

Address: **Operational Base** + offset (0x0038)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	WO	0x0	ctxfi Write 1 to Clear tx finish Interrupt.
5	WO	0x0	csspi Write 1 to Clear ss_in_n posedge Interrupt.
4	WO	0x0	ctoi Write 1 to Clear Timeout Interrupt.
3	WO	0x0	ctfoi Write 1 to Clear Transmit FIFO Overflow Interrupt.
2	WO	0x0	crfoi Write 1 to Clear Receive FIFO Overflow Interrupt.
1	WO	0x0	crfui Write 1 to Clear Receive FIFO Underflow Interrupt.
0	WO	0x0	cci Write 1 to Clear Combined Interrupt.

SPI_DMACR

Address: **Operational Base** + offset (0x003C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	tde 1'b0: Transmit DMA disabled 1'b1: Transmit DMA enabled

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Bit	Attr	Reset Value	Description
0	RW	0x0	rde 1'b0: Receive DMA disabled 1'b1: Receive DMA enabled

SPI_DMATDLR

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	tdl This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and transmit DMA is enabled (DMACR[1] = 1).

SPI_DMARDLR

Address: **Operational Base** + offset (0x0044)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	rdl This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above this field value + 1, and receive DMA is enabled(DMACR[0]=1).

SPI_VERSION

Address: **Operational Base** + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RO	0x03120003	version IP Version

SPI_TIMEOUT

Address: **Operational Base** + offset (0x004C)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	RW	0x0	dtsr DMA Timeout single request enable. 1'b0: DMA Timeout single request disable 1'b1: DMA Timeout single request enable
17	RW	0x0	tsb Timeout Sclkcnt Bypass 1'b0: Timeout counter will be active after the first rising edge of sclk_in 1'b1: Timeout counter will be active after the first rising edge of pclk

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Bit	Attr	Reset Value	Description
16	RW	0x0	toe Timeout Enable. 1'b0: Timeout counter is inactive 1'b1: Timeout counter will be active after the first rising edge of sclk_in
15:0	RW	0x0000	tov Timeout Threshold Value. If sclk_in keep inactive for a threshold time , timeout interrupt will be triggered .The timeout threshold time is TOV*pclk_period*16.

SPI_BYPASS

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:2	RW	0x0	ckgen Clock Gating Enable. 2'b00: no gating works 2'b01: gating sclk for bypass module, when work at normal mode 2'b10: gating spi_clk, when work at bypass mode 2'b11: gating sclk and spi_clk, when spi is idle
1	RW	0x0	txfie Bypass Slave TX Finish Interrupt Enable 1'b0: TX finish interrupt disable 1'b1: TX finish interrupt enable
0	RW	0x0	byen Bypass Enable. 1'b0: Normal mode 1'b1: Bypass mode, SPI serial/parallel convert logic is driven by SCLK

SPI_BPENR

Address: **Operational Base** + offset (0x0054)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	bpenr Enables and disables all SPI operations at bypass mode. Transmit and receive FIFO buffers are cleared when the device is disabled.

SPI_TXDR

Address: **Operational Base** + offset (0x0400)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	WO	0x0000	txdr When it is written to, data are moved into the transmit FIFO.

SPI_RXDR

Address: **Operational Base** + offset (0x0800)

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Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	rxdr When the register is read, data in the receive FIFO is accessed.

34.5 Interface Description

Table 34-1 SPI0 Interface Description

Module Pin	Dir	Pad Name	IOMUX Setting
IOMUX0			
spi_sclk	I/O	GPIO0_B2	GPIO0B_IOMUX_SEL_0[11:8]=4'h2
spi_mosi	I/O	GPIO0_B0	GPIO0B_IOMUX_SEL_0[3:0]=4'h2
spi_miso	I/O	GPIO0_B1	GPIO0B_IOMUX_SEL_0[7:4]=4'h2
spi_csn0	I/O	GPIO0_A7	GPIO0A_IOMUX_SEL_1[15:12]=4'h2
spi_csn1	O	GPIO0_A6	GPIO0A_IOMUX_SEL_1[11:8]=4'h2
IOMUX1			
spi_sclk	I/O	GPIO4_A7	GPIO4A_IOMUX_SEL_1[15:12]=4'h1
spi_mosi	I/O	GPIO4_A4	GPIO4A_IOMUX_SEL_1[3:0]=4'h1
spi_miso	I/O	GPIO4_A5	GPIO4A_IOMUX_SEL_1[7:4]=4'h1
spi_csn0	I/O	GPIO4_A6	GPIO4A_IOMUX_SEL_1[11:8]=4'h1
spi_csn1	O	GPIO4_A3	GPIO4A_IOMUX_SEL_0[15:12]=4'h1
IOMUX2			
spi_sclk	I/O	GPIO5_A6	GPIO5A_IOMUX_SEL_1[11:8]=4'h2
spi_mosi	I/O	GPIO5_A4	GPIO5A_IOMUX_SEL_1[3:0]=4'h2
spi_miso	I/O	GPIO5_A5	GPIO5A_IOMUX_SEL_1[7:4]=4'h2
spi_csn0	I/O	GPIO5_A3	GPIO5A_IOMUX_SEL_0[15:12]=4'h2
spi_csn1	O	GPIO5_A7	GPIO5A_IOMUX_SEL_1[15:12]=4'h2

Table 34-2 SPI1 Interface Description

Module Pin	Dir	Pad Name	IOMUX Setting
IOMUX0			
spi_sclk	I/O	GPIO6_B4	GPIO6B_IOMUX_SEL_1[3:0]=4'h3
spi_mosi	I/O	GPIO6_B2	GPIO6B_IOMUX_SEL_0[11:8]=4'h3
spi_miso	I/O	GPIO6_B3	GPIO6B_IOMUX_SEL_0[15:12]=4'h3
spi_csn0	I/O	GPIO6_B1	GPIO6B_IOMUX_SEL_0[7:4]=4'h3
spi_csn1	O	GPIO6_B0	GPIO6B_IOMUX_SEL_0[3:0]=4'h3
IOMUX1			
spi_sclk	I/O	GPIO3_B4	GPIO3B_IOMUX_SEL_1[3:0]=4'h1
spi_mosi	I/O	GPIO3_B2	GPIO3B_IOMUX_SEL_0[11:8]=4'h1
spi_miso	I/O	GPIO3_B3	GPIO3B_IOMUX_SEL_0[15:12]=4'h1
spi_csn0	I/O	GPIO3_B5	GPIO3B_IOMUX_SEL_1[7:4]=4'h1
spi_csn1	O	GPIO3_B6	GPIO3B_IOMUX_SEL_1[11:8]=4'h1
IOMUX2			
spi_sclk	I/O	GPIO5_D1	GPIO5D_IOMUX_SEL_0[7:4]=4'h2
spi_mosi	I/O	GPIO5_D2	GPIO5D_IOMUX_SEL_0[11:8]=4'h2
spi_miso	I/O	GPIO5_D3	GPIO5D_IOMUX_SEL_0[15:12]=4'h2
spi_csn0	I/O	GPIO5_D0	GPIO5D_IOMUX_SEL_0[3:0]=4'h2
spi_csn1	O	GPIO5_D4	GPIO5D_IOMUX_SEL_1[3:0]=4'h2

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34.6 Application Notes

Clock Ratios

A summary of the frequency ratio restrictions between the bit-rate clock (sclk_out/sclk_in) and the SPI peripheral clock (spi_clk) are described as:

When SPI Controller works as master, the F_{spi_clk}>= 2 × (maximum F_{sclk_out})

When SPI Controller works as slave, the F_{spi_clk}>= 4 × (maximum F_{sclk_in})

Master Transfer Flow

When configured as a serial-master device, the SPI initiates and controls all serial transfers. The serial bit-rate clock, generated and controlled by the SPI, is driven out on the sclk_out line. When the SPI is disabled (SPI_ENR = 0), no serial transfers can occur and sclk_out is held in "inactive" state, as defined by the serial protocol under which it operates.

Slave Transfer Flow

When the SPI is configured as a slave device, all serial transfers are initiated and controlled by the serial bus master.

When the SPI serial slave is selected during configuration, it enables its transmit data onto the serial bus. All data transfers to and from the serial slave are regulated on the serial clock line (sclk_in), driven from the serial-master device. Data are propagated from the serial slave on one edge of the serial clock line and sampled on the opposite edge.

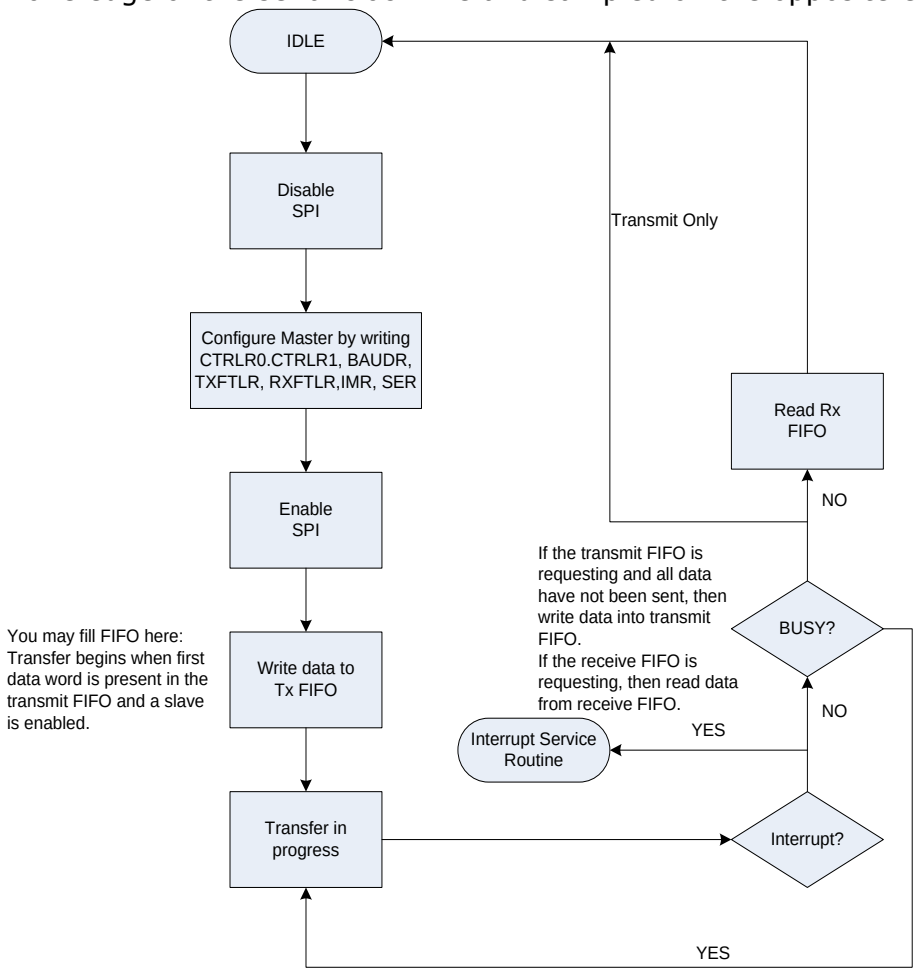

Fig. 34-7 SPI Master Transfer Flow Diagram

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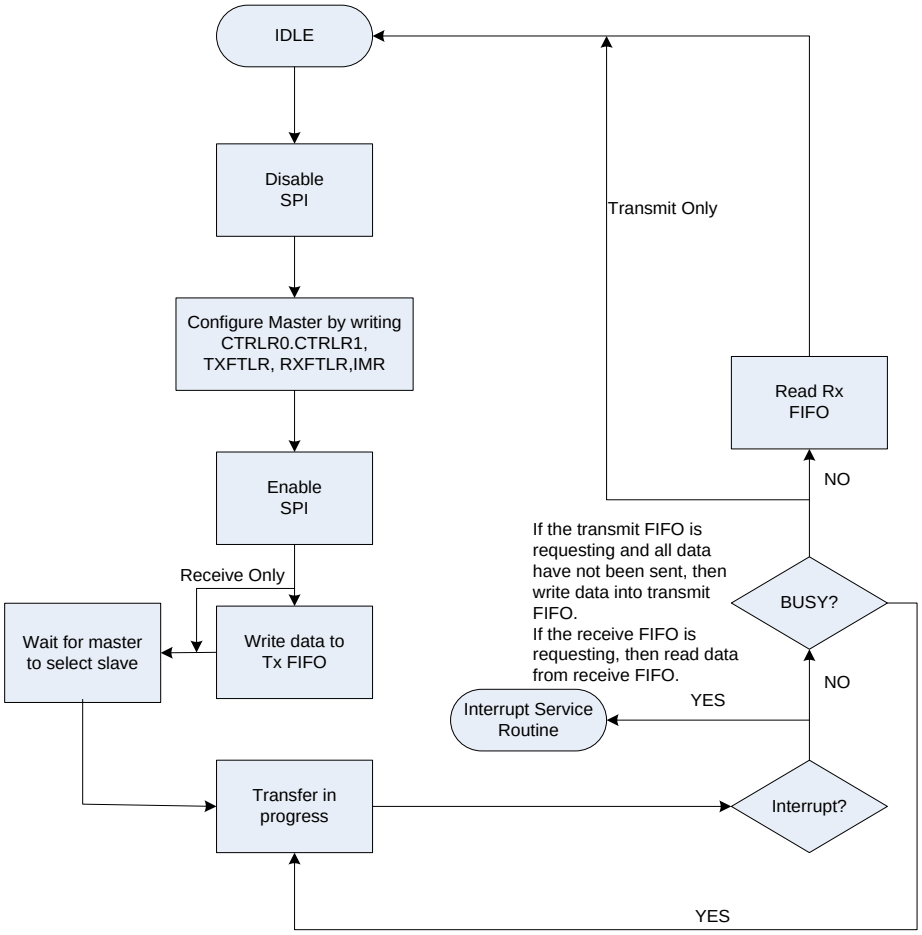

Fig. 34-8 SPI Slave Transfer Flow Diagram

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Chapter 35 SPI2AHB

35.1 Overview

The SPI2AHB is an SPI slave IP configured with APB slave. It is designed for pre-roll applications, connected to external camera sensors. External camera sensors and SPI2AHB use the xSPI protocol for data exchange. SPI2AHB send data to the next level device through the AHB 128bit channel.

The SPI2AHB supports the following features:

- Support 32-bit APB bus to read and write controller register
- Support 128bit AHB Master bus for sending data to PSRAM/DDR
- Support an SPI interface for receiving image data signals transmitted from cameras
- Support Single/Dual/Quad IO mode
- Support SDR (x1, x2, x4), DDR (x2, x4) IO mode
- Support AHB master burst Type: INCR4 INCR8 INCR16
- Support maskable interrupts generation
- Support APB configuration soft reset

35.2 Block Diagram

The SPI2AHB interface comprises with:

- AMBA APB slave interface
- AMBA AHB master interface
- SPI interface

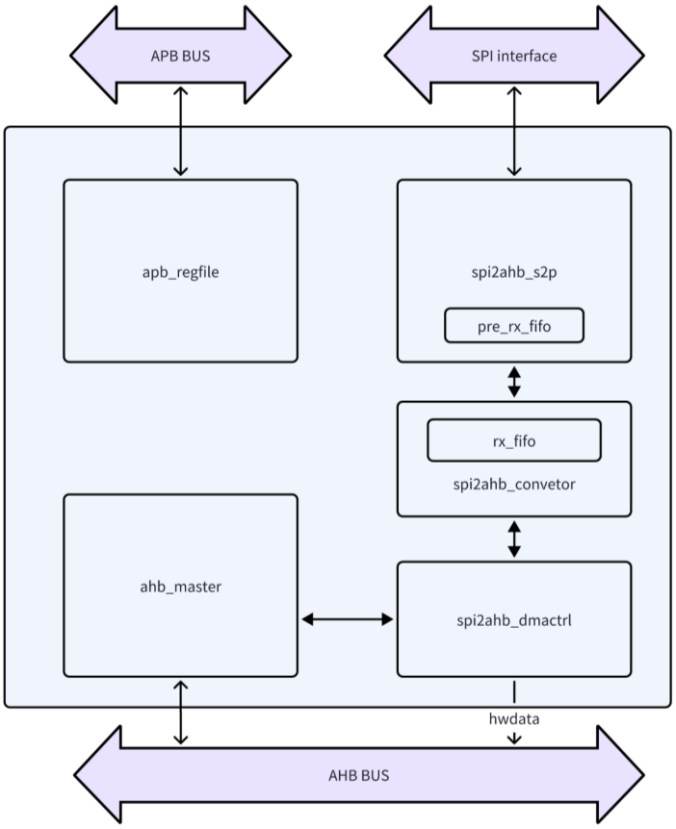

Fig. 35-1 SPI2AHB Block Diagram

35.3 Function Description

35.3.1 SPI2AHB_S2P

SPI2AHB_S2P is used for serial to parallel conversion of sampled data. There is no TX scene, only RX scene. When the data sample reaches 128bit, it starts pushing into RX_FIFO.

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35.3.2 SPI2AHB_CONVETOR

SPI2AHB_CONVETOR is used to process data between PRE_RX_FIFO and RX_FIFO. It reads out 1 byte of data, concatenates it into 16 bytes, and stores it in RX_FIFO. If the data of a frame cannot be matched to 16 bytes, it will be forcibly stored in RX_FIFO at the end of the frame, with 0 bits filled in.

35.3.3 SPI2AHB_DMACTRL

A block takes responsible for splitting a long length transfer trans into AHB bus transaction.

35.3.4 AHB_MASTER

The AHB_MASTER is used to transfer data to other system region, such as PSRAM, DDR.

35.3.5 APB_REGFILE

The host processor accesses data, control, and status information on the SPI2AHB through the APB interface.

35.4 Register Description

35.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

35.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SPI2AHB_SPI_CTRL	0x0000	W	0x00000000	Control Register for the Transmission Mode of the SPI
SPI2AHB_DMA_CTRL	0x0004	W	0x00000000	Control Register for the Burst Type of AHB
SPI2AHB_SPI_EN	0x000C	W	0x00000000	SPI Enable
SPI2AHB_FRAME_ADDR	0x0010	W	0x00000000	Configure Frame Address in PSRAM
SPI2AHB_FRAME_BNUM	0x0014	W	0x00000000	Configure Frame Byte Number
SPI2AHB_FRAME_TME_EN	0x0028	W	0x00000000	RX Timeout Enable Register
SPI2AHB_FRAME_TME	0x002C	W	0x00000000	Timeout Value of Frame Timer
SPI2AHB_SW_RST	0x0030	W	0x00000000	Software Reset Register
SPI2AHB_CSN	0x0038	W	0x00000001	Chip Select State
SPI2AHB_IMR	0x0040	W	0x00000000	Interrupt Mask Register
SPI2AHB_ICLR	0x0044	W	0x00000000	Interrupt Clear Register
SPI2AHB_ISR	0x0048	W	0x00000000	
SPI2AHB_RISR	0x004C	W	0x00000000	Interrupt Status
SPI2AHB_VER	0x0050	W	0x00000001	The Version ID
SPI2AHB_MONITOR	0x0054	W	0x00000001	State Monitor Register
SPI2AHB_FRAME_CNT_MONITOR	0x0058	W	0x00000000	Frame Byte Number Counter Monitor

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

35.4.3 Detail Registers Description

SPI2AHB_SPI_CTRL

Address: Operational Base(0x208A0000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved

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Bit	Attr	Reset Value	Description
5:4	RW	0x0	DATB Data Line Width 2'b00: 1 bit, x1 mode 2'b01: 2 bits, x2 mode 2'b10: 4 bits, x4 mode
3	RW	0x0	SPIM Serial Peripheral Interface Mode 1'b0: Mode 0 1'b1: Mode 3 SPIM is used to control the serial mode (CPOL and CPHA). CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.
2	RW	0x0	CS_MODE Chip Sel Active Mode 1'b0: CS is active when signal is low 1'b1: CS is active when signal is high
1	RW	0x0	DDR_EN DDR mode enable 1'b0: SDR mode 1'b1: DDR mode
0	RW	0x0	FBM 1'b0: first bit is LSB 1'b1: first bit is MSB

SPI2AHB_DMA_CTRL

Address: Operational Base(0x208A0000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	BURST_TYPE DMA AHB Burst Type 2'b00: INCR16 HSIZE4 2'b01: INCR8 HSIZE4 2'b10: INCR4 HSIZE4

SPI2AHB_SPI_EN

Address: Operational Base(0x208A0000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	SPI_EN SPI Enable 1'b0: SPI2AHB disable 1'b1: SPI2AHB enable

SPI2AHB_FRAME_ADDR

Address: Operational Base(0x208A0000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	FRAME_ADDR Frame Address in PSRAM This address should align to AHB Burst Type

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SPI2AHB_FRAME_BNUM

Address: Operational Base(0x208A0000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	FRAME_BNUM Frame Byte number

SPI2AHB_FRAME_TME_EN

Address: Operational Base(0x208A0000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	FRAME_TME_EN RX Timeout Enable 1'b0: Disable 1'b1: Enable

SPI2AHB_FRAME_TME

Address: Operational Base(0x208A0000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	FRAME_TME Timeout value of Frame Timer. The Timer will active when chip_sel is active but no data received.

SPI2AHB_SW_RST

Address: Operational Base(0x208A0000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	W1C	0x0	SW_RST Software reset

SPI2AHB_CSN

Address: Operational Base(0x208A0000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	CSN_SRC The Source of Chip Select State. 1'b0: The source of chip select is low 1'b1: The source of chip select is high
0	RO	0x1	CSN The State of Chip Select. 1'b0: Chip Select is active. 1'b1: Chip Select is inactive.

SPI2AHB_IMR

Address: Operational Base(0x208A0000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7	RW	0x0	TIMEOUTM Timeout Interrupt Mask 1'b0: interrupt is not masked 1'b1: interrupt is masked
6	RW	0x0	FRAME_MISM Frame Data Size Mismatch Interrupt Mask 1'b0: interrupt is not masked 1'b1: interrupt is masked
5	RW	0x0	DMA_ERRM DMA Error Interrupt Mask 1'b0: interrupt is not masked 1'b1: interrupt is masked
4	RW	0x0	FRAME_ERRM Frame Error Interrupt Mask 1'b0: interrupt is not masked 1'b1: interrupt is masked
3	RW	0x0	RFIFO_FWM RX-FIFO Write Error Interrupt Mask 1'b0: interrupt is not masked 1'b1: interrupt is masked
2	RW	0x0	RFIFO_ERM RX-FIFO Read Error Interrupt Mask 1'b0: interrupt is not masked 1'b1: interrupt is masked
1	RW	0x0	PFIFO_ERM Pre-FIFO Read Error Interrupt Mask 1'b0: interrupt is not masked 1'b1: interrupt is masked
0	RW	0x0	FRAME_ENDM Frame End Interrupt Mask 1'b0: interrupt is not masked 1'b1: interrupt is masked

SPI2AHB_ICLR

Address: Operational Base(0x208A0000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	W1C	0x0	TIMEOUTC Timeout Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the TIMEOUTM.
6	W1C	0x0	FRAME_MISC Frame Data Size Mismatch Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the FRAME_MISM.
5	W1C	0x0	DMA_ERRC DMA Error Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the DMA_ERRS.

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Bit	Attr	Reset Value	Description
4	W1C	0x0	FRAME_ERRC Frame Error Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the FRAME_ERRS.
3	W1C	0x0	RFIFO_FWC RX-FIFO Write Error Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the RFIFO_FWS.
2	W1C	0x0	RFIFO_ERC RX-FIFO Read Error Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the RFIFO_ERS.
1	W1C	0x0	PFIFO_ERC Pre-FIFO Read Error Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the PFIFO_ERS.
0	W1C	0x0	FRAME_ENDC Frame End Interrupt Clear 1'b0: No action 1'b1: Clear interrupt Write "1" to clear the FRAME_ENDS.

SPI2AHB_ISR

Address: Operational Base(0x208A0000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	TIMEOUTS Timeout Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
6	RO	0x0	FRAME_MISS Frame Data Size Mismatch Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
5	RO	0x0	DMA_ERRS DMA Error Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
4	RO	0x0	FRAME_ERRS Frame Error Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
3	RO	0x0	RFIFO_FWS RX-FIFO Write Error Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
2	RO	0x0	RFIFO_ERS RX-FIFO Read Error Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated

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Bit	Attr	Reset Value	Description
1	RO	0x0	PFIFO_ERS Pre-FIFO Read Error Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated
0	RO	0x0	FRAME_ENDS Frame End Interrupt Status 1'b0: No interrupt 1'b1: Active interrupt generated

SPI2AHB_RISR

Address: Operational Base(0x208A0000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	TIMEOUTS Timeout Interrupt Status 1'b0: No interrupt 1'b1: Active raw interrupt generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
6	RO	0x0	FRAME_MISS Frame Data Size Mismatch Interrupt Status 1'b0: No interrupt 1'b1: Active raw interrupt generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
5	RO	0x0	DMA_ERRS DMA Error Interrupt Status 1'b0: No interrupt 1'b1: Active raw interrupt generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
4	RO	0x0	FRAME_ERRS Frame Error Interrupt Status 1'b0: No interrupt 1'b1: Active raw interrupt generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
3	RO	0x0	RFIFO_FWS RX-FIFO Write Error Interrupt Status 1'b0: No interrupt 1'b1: Active raw interrupt generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
2	RO	0x0	RFIFO_ERS RX-FIFO Read Error Interrupt Status 1'b0: No interrupt 1'b1: Active raw interrupt generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.

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Bit	Attr	Reset Value	Description
1	RO	0x0	PFIFO_ERS Pre-FIFO Read Error Interrupt Status 1'b0: No interrupt 1'b1: Active raw interrupt generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.
0	RO	0x0	FRAME_ENDS Frame End Interrupt Status 1'b0: No interrupt 1'b1: Active raw interrupt generated Cleared by writing corresponding ICLR bit to clear raw interrupt status.

SPI2AHB_VER

Address: Operational Base(0x208A0000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0001	VER The Version ID

SPI2AHB_MONITOR

Address: Operational Base(0x208A0000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x0	IDLE_STATE SPI2AHB IDLE State 1'b0: SPI2AHB is working 1'b1: SPI2AHB is IDLE
7:6	RO	0x0	reserved
5:4	RO	0x0	FSM_STATE AHB FSM State 2'b00: IDLE 2'b01: CMD_ST 2'b10: DATA_ST
3:2	RO	0x0	reserved
1	RO	0x0	SCLK_CNT_STATE Sclk Counter State 1'b0: Sclk counter equal 0 1'b1: Sclk counter does not equal 0
0	RO	0x1	RX_FIFO_EMPTY RX FIFO Empty State 1'b0: RX FIFO is not empty 1'b1: RX FIFO is empty

SPI2AHB_FRAME_CNT_MONITOR

Address: Operational Base(0x208A0000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	FRAME_CNT_MONITOR Frame Byte Number Counter Monitor.

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35.5 Interface Description

Table 35-1 SPI2AHB interface description

Module Pin	Dir	Pad Name	IOMUX Setting
IOMUX0			
spi2ahb_sclk	I	GPIO0_C3	GPIO0C_IOMUX_SEL_0 [15:12]=4'h1
spi2ahb_rxd_d0	I	GPIO0_C7	GPIO0C_IOMUX_SEL_1 [15:12]=4'h1
spi2ahb_rxd_d1	I	GPIO0_C6	GPIO0C_IOMUX_SEL_1 [11:8]=4'h1
spi2ahb_rxd_d2	I	GPIO0_C5	GPIO0C_IOMUX_SEL_1 [7:4]=4'h1
spi2ahb_rxd_d3	I	GPIO0_C4	GPIO0C_IOMUX_SEL_1 [3:0]=4'h1
spi2ahb_csn	I	GPIO0_C2	GPIO0C_IOMUX_SEL_0 [11:8]=4'h1

35.6 Application Notes

35.6.1 Software Program Flow

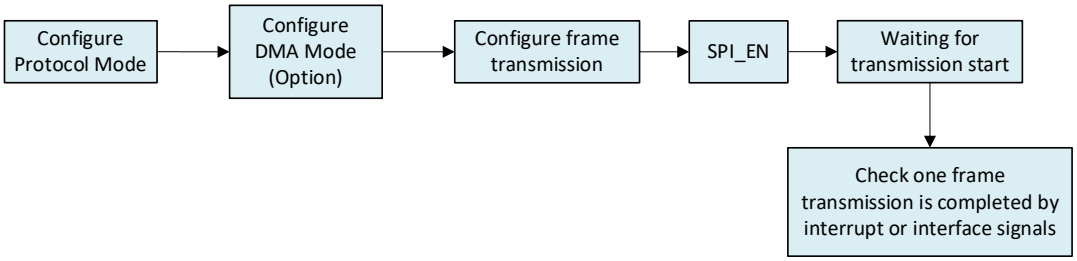

Fig. 35-2 SPI2AHB Software Program Flow

Because there are various forms of interaction between sensors, such as chip_select high effective or low effective, in order to avoid false start due to effective signal switching during the configuration process, register SPI_EN is to control whether the IP enters the working state. Therefore, IP configuration needs to be completed before SPI_EN, and transmission needs to start after SPI_EN.

Configure Protocol Mode

Configure SPI_CTRL (0x0) register.

Note: Only x2 and x4 mode have DDR mode.

Configure Protocol Mode (Option)

Configure DMA_CTRL (0x4) register.

Default DMA BURST is INCR16 HSIZE4. Can be configured as INCR8 HSIZE4 or INCR4 HSIZE4.The subsequent frame addresses require the burst mode selected by DMA.

Configure frame transmission

1.Configure the first address of the frame storage location (Frame-ADDR 0x10), and note that this address needs to be aligned with a burst transmission byte in the configured DMA mode.

INCR16 HSIZE4: Address alignment to 256 bytes;

INCR8 HSIZE4: Address alignment to 128 bytes;

INCR4 HSIZE4: Address alignment to 64 bytes;

Due to this alignment requirement, there may be storage bubbles between frames. These bubbles are filled with 0 every time they are transmitted.

2.Configure the data size (in bytes) for each frame of data (Frame_BNUM 0x14).

SPI_EN

IP working enable (SPI_EN 0x0c), only after completing this configuration can data transmission be received normally.

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35.6.2 Exception handling Flow

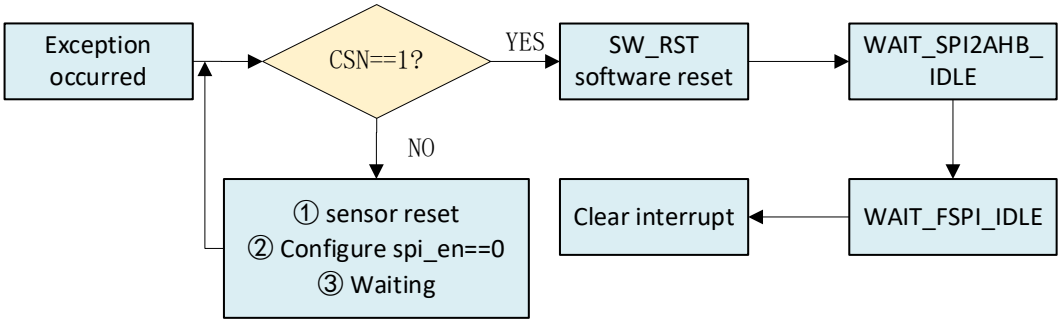

Fig. 35-3 SPI2AHB Exception handling Flow

Some additional explanations about the process shown in the above diagram:

1.When an exception occurs, it is necessary to first confirm the status of the CSN (0x38) register. If the CSN is still in a valid state, a soft reset cannot be performed. Otherwise, after a soft reset, the internal control logic counter will reset and continue to work, making it impossible to truly reset. The CSN register uses the signal after effective polarity conversion, and regardless of the polarity of the input cs, this read-only register is in the IDLE state with 1 and the ACTIVE state with 0.

2.If CSN does not return to idle state, there are three ways to handle CSN:

① Sensor reset. Reset the master to return to IDLE state

② Configure the SPI_EN register to 0. It can force block the input of CSN(not recommended, SCLK may still be toggled, master is not set and cannot start the next transmission)

③ Waiting, wait for master to complete this erroneous transmission (loop reading CSN register), this situation mainly occurs when the actual transmitted data volume is greater than the preset data volume

3. After start a soft reset, SPI2AHB may not immediately return to the control IDLE state. Due to bus integrity design, AHB BURST that has initiated a request must be completed before returning to IDLE. So after resetting, a waiting IDLE process needs to be performed.

4. Finally, clear the abnormal interrupt.

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Chapter 36 Inter-Integrated Circuit (I2C)

36.1 Overview

The Inter-Integrated Circuit (I2C) is a two wired (SCL and SDA), bi-directional serial bus that provides an efficient and simple method of information exchange between devices. This I2C bus controller supports master mode acting as a bridge between AMBA protocol and generic I2C bus system.

I2C Controller supports the following features:

- Support 5 independent I2C: I2C0~5
- Item Compatible with I2C-bus
- AMBA APB slave interface
- Supports master mode of I2C bus
- I2C1 and I2C3 support sending TX data by CPU or DMA, while other I2C support sending TX data only by CPU. When by DMA, can separate configuration data and address
- I2C1 and I2C3 support moving RX data by CPU or DMA, while other I2C support moving RX data only by CPU
- Software programmable clock frequency and transfer rate up to 400Kbit/sec
- Supports 7 bits and 10 bits addressing modes
- Interrupt or polling driven multiple bytes data transfer
- Clock stretching and wait state generation
- Filter out glitch on SCL and SDA

36.2 Block Diagram

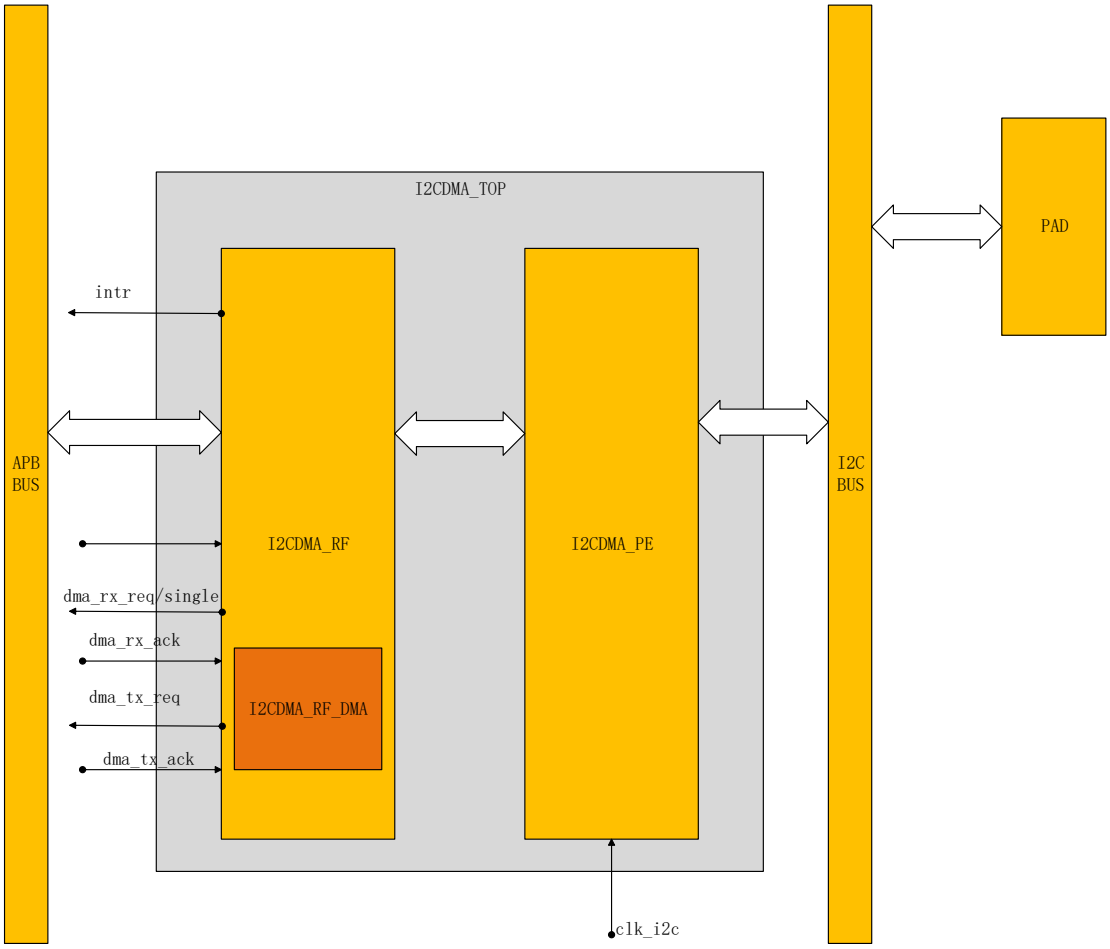

Fig. 36-1 I2C architecture

36.2.1 I2C_RF

I2C_RF module is used to control the I2C controller operation by the host with APB interface. It implements the register set and the interrupt functionality. The I2C_RF component operates synchronously with the pclk.

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36.2.2 I2C_PE

I2C_PE module implements the I2C master operation for transmit data to and receive data from other I2C devices. The I2C master controller operates synchronously with the clk_i2c.

36.2.3 I2C_TOP

I2C_TOP module is the top module of the I2C controller.

36.3 Function Description

This chapter provides a description about the functions and behavior under various conditions.

The I2C controller supports only Master function. It supports the 7-bits/10-bits addressing mode and support general call address. The maximum clock frequency and transfer rate can be up to 400Kbit/sec.

The operation of I2C controller is divided to 2 parts and described separately: initialization and master mode programming.

36.3.1 Initialization

The I2C controller is based on AMBA APB bus architecture and usually is part of a SOC. So before I2C operates, some system setting and configuration must be conformed, which includes:

- I2C interrupt connection type: CPU interrupt scheme should be considered. If the I2C interrupt is connected to extra Interrupt Controller module, we need decide the INTC vector.
- I2C Clock Rate: The I2C controller uses the APB clock to configure controller and uses clk_i2c as the working clock. The correct register setting is subject to the system requirement.

36.3.2 Master Mode Programming

- SCL Clock

When the I2C controller is programmed in Master mode, the SCL frequency is determined by I2C_CLKDIV register. The SCL frequency is calculated by the following formula:

SCL Divisor = 8*(CLKDIVL + 1 + CLKDIVH + 1); clk_i2c = 100MHz~200MHz.

SCL = clk_i2c/ SCLK Divisor.

- Data Receiver Register Access without DMA

When the I2C controller received MRXCNT bytes data, CPU can get the data through register RXDATA0 ~ RXDATA7. The controller can receive up to 32 bytes' data in one transaction.

When MRXCNT register is written, the I2C controller will start to drive SCL to receive data.

- Transmit Transmitter Register without DMA

Data to transmit are written to TXDATA0~7 by CPU. The controller can transmit up to 32 bytes' data in one transaction. The lower byte will be transmitted first.

When MTXCNT register is written, the I2C controller will start to transmit data.

- Data Receiver Register Access with DMA

You can set 1 to DMACONF.rxdma_use_enable to enable DMA RX function.

When the I2C controller received 4 words data every time, it will rise rx_dma_src_request to DMA and then DMA can read data from RXDMA register. When the I2C controller received MRXCNT bytes data and the DMA support single_request function, for the left RX bytes which are less than 4 words, the I2C controller will rise rx_dma_src_single to DMA. However if the DMA does not support single_request function, the I2C controller will still rise rx_dma_src_request to DMA for the left rxdata.

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- Transmit Transmitter Register with DMA

You can set 1 to DMACONF.txdma_use_enable to enable DMA TX function.
TXADDR which includes slave's address and slave's register address are written to DMA_SADDR2 and DMA_SADDR by CPU before configuring MTXCNT.
When there exists 4 words space and the number of data that has been written to TXDMA FIFO is less than MTXCNT, the controller can rise tx_dma_dst_request to DMA to request 4 words once time. For the last request, DMA will bring in the data to make up the MTXCNT.
The lower byte will be transmitted first.
When MTXCNT register is written, the I2C controller will start to transmit data.

- Start Command

Write 1 to I2C_CON[3], the controller will send I2C start command.

- Stop Command

Write 1 to I2C_CON[4], the controller will send I2C stop command.

- I2C Operation mode

There are four i2c operation modes.

- When I2C_CON[2:1] is 2'b00, the controller will transmit all valid data in TXDATA0~TXDATA7 byte by byte. The controller will transmit lower byte first.
- When I2C_CON[2:1] is 2'b01, the controller will transmit device address in MRXADDR first (Write/Read bit = 0) and then transmit device register address in MRXRADDR. After that, the controller will assert restart signal and resend MRXADDR (Write/Read bit = 1). At last, the controller enters receive mode.
- When I2C_CON[2:1] is 2'b10, the controller is in receive mode, it will trigger clock to read MRXCNT byte data.
- When I2C_CON[2:1] is 2'b11, the controller will transmit device address in MRXADDR first (Write/Read bit = 1) and then transmit device register address in MRXRADDR. After that, the controller will assert restart signal and resend MRXADDR (Write/Read bit = 1). At last, the controller enters receive mode.

- Read/Write Command

- When I2C_OPMODE(I2C_CON[2:1]) is 2'b01 or 2'b11, the Read/Write command bit is decided by controller itself.
- In RX only mode (I2C_CON[2:1] is 2'b10), the Read/Write command bit is decided by MRXADDR[0].
- In TX only mode (I2C_CON[[2:1] is 2'b00), the Read/Write command bit is decided by TXDATA[0].

- Master Interrupt Condition

There are 9 interrupt bits in I2C_ISR register related to master mode.

- Byte transmitted finish interrupt (Bit 0): The bit is asserted when Master completed transmitting a byte.
- Byte received finish interrupt (Bit 1): The bit is asserted when Master completed receiving a byte.
- MTXCNT bytes data transmitted finish interrupt (Bit 2): The bit is asserted when Master completed transmitting MTXCNT bytes.
- MRXCNT bytes data received finish interrupt (Bit 3): The bit is asserted when Master completed receiving MRXCNT bytes.
- Start interrupt (Bit 4): The bit is asserted when Master finished asserting start command to I2C bus.
- Stop interrupt (Bit 5): The bit is asserted when Master finished asserting stop command to I2C bus.
- NAK received interrupt (Bit 6): The bit is asserted when Master received a NAK

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handshake.
- SLAVE hold SCL interrupt (Bit 7): The bit is asserted when Slave hold SCL over scl_oe_db's cycles.
- SLAVE hold SDA interrupt (Bit 8): The bit is asserted when SDA on line is different from what MASTER wants, which means Slave drive SDA when MASTER send data.

If enable DMA, there still exists two interrupts:
- DMA RX finish (Bit 10): The bit is asserted when all RX data had been received by DMA.
- DMA TX finish (Bit 11): The bit is asserted when all TX data had been sent to i2c_master by DMA.

- Last byte acknowledge control
- If I2C_CON[5] is 1, the I2C controller will transmit NAK handshake to slave when the last byte received in RX only mode.
- If I2C_CON[5] is 0, the I2C controller will transmit ACK handshake to slave when the last byte received in RX only mode.

- How to handle NAK handshake received
- If I2C_CON[6] is 1, the I2C controller will stop all transactions when NAK handshake received. And the software should take responsibility to handle the problem.
- If I2C_CON[6] is 0, the I2C controller will ignore all NAK handshake received.

- I2C controller data transfer waveform
- Bit transferring

◆ Data Validity

The SDA line must be stable during the high period of SCL, and the data on SDA line can only be changed when SCL is in low state.

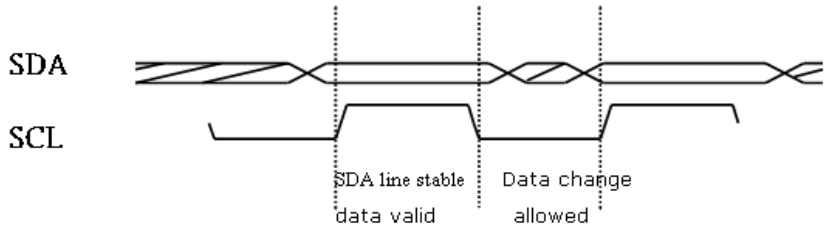

Fig. 36-2 I2C DATA Validity

◆ START and STOP conditions

START condition occurs when SDA goes low while SCL is in high period. STOP condition is generated when SDA line goes high while SCL is in high state.

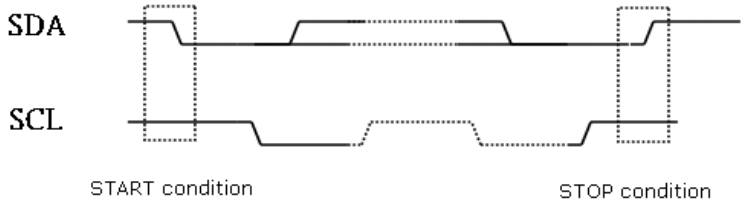

Fig. 36-3 I2C Start and stop conditions

◆ Data transfer

➢ Acknowledge

After a byte of data transferring (clocks labeled as 1~8), in 9th clock the receiver must assert an ACK signal on SDA line, if the receiver pulls SDA line to low, it means "ACK", on

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the contrary, it's "NOT ACK".

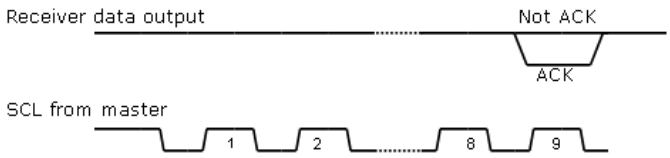

Fig. 36-4 I2C Acknowledge

- Byte transfer

The master own I2C bus might initiate multi byte to transfer to a slave. The transfer starts from a "START" command and ends in a "STOP" command. After every byte transfer, the receiver must reply an ACK to transmitter.

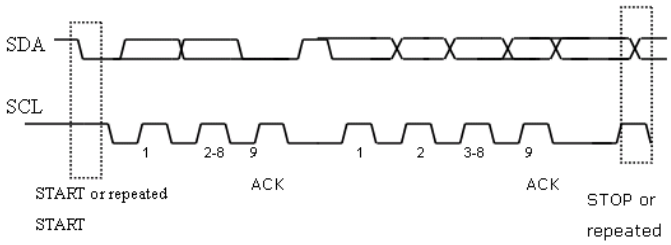

Fig. 36-5 I2C byte transfer

36.4 Register Description

36.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
RKI2C0	0x21100000
RKI2C1	0x21110000
RKI2C2	0x20800000
RKI2C3	0x21120000
RKI2C4	0x21130000
RKI2C5	0x21140000

36.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
RKI2C_CON	0x0000	W	0x00070000	Control register
RKI2C_CLKDIV	0x0004	W	0x00000001	Clock divider register I2C CLK = PCLK / (16*CLKDIV)
RKI2C_MRXADDR	0x0008	W	0x00000000	The slave address accessed for master rx mode
RKI2C_MRXRADDR	0x000C	W	0x00000000	The slave register address accessed for master rx mode
RKI2C_MTXCNT	0x0010	W	0x00000000	Master transmit count, specify the total bytes to be transmit (0~32)
RKI2C_MRXCNT	0x0014	W	0x00000000	Master rx count, specify the total bytes to be recieved(0~32)
RKI2C_IEN	0x0018	W	0x00000000	Interrupt enable register
RKI2C_IPD	0x001C	W	0x00000000	Interrupt pending register

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Name	Offset	Size	Reset Value	Description
RKI2C_FCNT	0x0020	W	0x00000000	Finished count: the count of data which has been transmitted or received for debug purpose
RKI2C_SCL_OE_DB	0x0024	W	0x00000020	Slave hold debounce configure register
RKI2C_DMA_SADDR	0x0080	W	0x00000000	Slave device address for TX when use DMA
RKI2C_DMA_SADDR2	0x0084	W	0x00000000	Slave extern visit address for TX when use DMA
RKI2C_TXDMA	0x0088	W	0x00000000	I2C tx data when use DMA
RKI2C_RXDMA	0x008C	W	0x00000000	I2C rx data when use DMA
RKI2C_DMA_CONF	0x0090	W	0x00000004	DMA related configuration register
RKI2C_DMA_ST	0x0094	W	0x00000000	Status of DMA FIFO
RKI2C_DMA_TXCNT_ST	0x0098	W	0x00000000	Number of TX data when use DMA
RKI2C_DMX_RXCNT_ST	0x009C	W	0x00000000	Number of RX data when use DMA
RKI2C_TXDATA0	0x0100	W	0x00000000	I2C tx data register 0
RKI2C_TXDATA1	0x0104	W	0x00000000	I2C tx data register 1
RKI2C_TXDATA2	0x0108	W	0x00000000	I2C tx data register 2
RKI2C_TXDATA3	0x010C	W	0x00000000	I2C tx data register 3
RKI2C_TXDATA4	0x0110	W	0x00000000	I2C tx data register 4
RKI2C_TXDATA5	0x0114	W	0x00000000	I2C tx data register 5
RKI2C_TXDATA6	0x0118	W	0x00000000	I2C tx data register 6
RKI2C_TXDATA7	0x011C	W	0x00000000	I2C tx data register 7
RKI2C_RXDATA0	0x0200	W	0x00000000	I2C rx data register 0
RKI2C_RXDATA1	0x0204	W	0x00000000	I2C rx data register 1
RKI2C_RXDATA2	0x0208	W	0x00000000	I2C rx data register 2
RKI2C_RXDATA3	0x020C	W	0x00000000	I2C rx data register 3
RKI2C_RXDATA4	0x0210	W	0x00000000	I2C rx data register 4
RKI2C_RXDATA5	0x0214	W	0x00000000	I2C rx data register 5
RKI2C_RXDATA6	0x0218	W	0x00000000	I2C rx data register 6
RKI2C_RXDATA7	0x021C	W	0x00000000	I2C rx data register 7
RKI2C_ST	0x0220	W	0x00000000	Status debug register
RKI2C_DBGCTRL	0x0224	W	0x00000000	Debug config register
RKI2C_CON1	0x0228	W	0x00000000	Control register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

36.4.3 Detail Registers Description

RKI2C_CON

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0007	version Rki2c version information.
15:14	RW	0x0	stop_setup Stop setup config. TSU;sto = (stop_setup + 1) * T(SCL_HIGH) + Tclk_i2c.

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Bit	Attr	Reset Value	Description
13:12	RW	0x0	start_setup Start setup config. TSU;sta = (start_setup + 1) * T(SCL_HIGH) + Tclk_i2c. THD;sta = (start_setup + 2) * T(SCL_HIGH) - Tclk_i2c.
11:8	RW	0x0	data_upd_st SDA update point config. Used to config sda change state when scl is low, used to adjust setup/hold time. 4'bn: Thold = (n + 1) /8*T(SCL_LOW). Note: 0 <= n <= 5
7	RW	0x0	flush_dmaen At the time of writing 1 to this bit, DMA_CONF.bit[2:0] will clear to 3'b100. It is self-clear.
6	RW	0x0	act2nak Operation when NAK handshake is received. 1'b0: Ignored. 1'b1: Stop transaction.
5	RW	0x0	ack Last byte acknowledge control in master receive mode. 1'b0: ACK 1'b1: NAK
4	RW	0x0	stop Stop enable, when this bit is written to 1, I2C will generate stop signal.
3	RW	0x0	start Start enable, when this bit is written to 1, I2C will generate start signal.
2:1	RW	0x0	i2c_mode I2c mode select. 2'b00: Transmit only. 2'b01: Transmit address (device + register address) --> Restart --> Transmit address -> Receive only. 2'b10: Receive only. 2'b11: Transmit address (device + register address, write/read bit is 1) --> Restart --> Transmit address (device address) --> Receive data.
0	RW	0x0	i2c_en I2c module enable. 1'b0: Disable 1'b1: Enable

RKI2C_CLKDIV

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	CLKDIVH SCL high level clock count. T(SCL_HIGH) = Tclk_i2c * (CLKDIVH + 1) * 8.
15:0	RW	0x0001	CLKDIVL SCL low level clock count. T(SCL_LOW) = Tclk_i2c * (CLKDIVL + 1) * 8.

RKI2C_MRXADDR

Address: **Operational Base** + offset (0x0008)

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Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RW	0x0	addhvld Address high byte valid. 1'b0: Invalid 1'b1: Valid
25	RW	0x0	addmvld Address middle byte valid. 1'b0: Invalid 1'b1: Valid
24	RW	0x0	addlvld Address low byte valid. 1'b0: Invalid 1'b1: Valid
23:0	RW	0x000000	saddr Master address register. The lowest bit indicate write or read. 24 bits address register.

RKI2C_MRXRADDR

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RW	0x0	sraddhvld Address high byte valid. 1'b0: Invalid 1'b1: Valid
25	RW	0x0	sraddmvld Address middle byte valid. 1'b0: Invalid 1'b1: Valid
24	RW	0x0	sraddlvld Address low byte valid. 1'b0: Invalid 1'b1: Valid
23:0	RW	0x000000	sraddr Slave register address accessed. 24 bits register address

RKI2C_MTXCNT

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	mtxcnt Master transmit count. 20 bits counter

RKI2C_MRXCNT

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
19:0	RW	0x00000	mrxcnt Master rx count. 20 bits counter

RKI2C_IEN

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RW	0x0	txenden All TX data had been sent to i2c_master by DMA 1'b0: Disable 1'b1: Enable
10	RW	0x0	rxenden All RX data had been received by DMA 1'b0: Disable 1'b1: Enable
9	RO	0x0	reserved
8	RW	0x0	slavehdsdaen Slave hold sda interrupt enable. 1'b0: Disable 1'b1: Enable
7	RW	0x0	slavehdsclen Slave hold scl interrupt enable. 1'b0: Disable 1'b1: Enable
6	RW	0x0	nakrcvien NAK handshake received interrupt enable. 1'b0: Disable 1'b1: Enable
5	RW	0x0	stopien Stop operation finished interrupt enable. 1'b0: Disable 1'b1: Enable
4	RW	0x0	startien Start operation finished interrupt enable. 1'b0: Disable 1'b1: Enable
3	RW	0x0	mbrfien MRXCNT data received finished interrupt enable. 1'b0: Disable 1'b1: Enable
2	RW	0x0	mbtfien MTXCNT data transfer finished interrupt enable. 1'b0: Disable 1'b1: Enable
1	RW	0x0	brfien Byte rx finished interrupt enable. 1'b0: Disable 1'b1: Enable
0	RW	0x0	btfien Byte tx finished interrupt enable. 1'b0: Disable 1'b1: Enable

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RKI2C_IPD

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	W1C	0x0	txendipd All word have been sent to TXFIFO by DMA.
10	W1C	0x0	rxendipd All word have been read by DMA.
9	RO	0x0	reserved
8	W1C	0x0	slavehdsdaipd Slave hold sda interrupt pending bit. 1'b0: No interrupt available. 1'b1: Slave hold sda interrupt appear, write 1 to clear.
7	W1C	0x0	slavehdsclipd Slave hold scl interrupt pending bit. 1'b0: No interrupt available. 1'b1: Slave hold scl interrupt appear, write 1 to clear.
6	W1C	0x0	nakrcvipd NAK handshake received interrupt pending bit. 1'b0: No interrupt available. 1'b1: NAK handshake received interrupt appear, write 1 to clear.
5	W1C	0x0	stopipd Stop operation finished interrupt pending bit. 1'b0: No interrupt available. 1'b1: Stop operation finished interrupt appear, write 1 to clear.
4	W1C	0x0	startipd Start operation finished interrupt pending bit. 1'b0: No interrupt available. 1'b1: Start operation finished interrupt appear, write 1 to clear.
3	W1C	0x0	mbrfipd MRXCNT data received finished interrupt pending bit. 1'b0: No interrupt available. 1'b1: MRXCNT data received finished interrupt appear, write 1 to clear.
2	W1C	0x0	mbtfipd MTXCNT data transfer finished interrupt pending bit. 1'b0: No interrupt available. 1'b1: MTXCNT data transfer finished interrupt appear, write 1 to clear.
1	W1C	0x0	brfipd Byte rx finished interrupt pending bit. 1'b0: No interrupt available. 1'b1: Byte rx finished interrupt appear, write 1 to clear.
0	W1C	0x0	btfipd Byte tx finished interrupt pending bit. 1'b0: No interrupt available. 1'b1: Byte tx finished interrupt appear, write 1 to clear.

RKI2C_FCNT

Address: **Operational Base** + offset (0x0020)

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Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RO	0x00000	fcnt The count of data which has been transmitted or received for debug purpose.

RKI2C_SCL_OE_DB

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000020	scl_oe_db Slave hold scl debounce. Cycles for debounce (unit: Tclk_i2c).

RKI2C_DMA_SADDR

Address: **Operational Base** + offset (0x0080)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RW	0x0	slave_regaddr3_valid 1'b1: means DMA_SADDR2's bit[31:24]'s slave_addr is valid This bit need user to set 0 to clear or be cleared by DMA_CONF.flush_txrx.
20	RW	0x0	slave_regaddr2_valid 1'b1: means DMA_SADDR2's bit[23:16]'s slave_addr is valid This bit need user to set 0 to clear or be cleared by DMA_CONF.flush_txrx.
19	RW	0x0	slave_regaddr1_valid 1'b1: means DMA_SADDR2's bit[15:8]'s slave_addr is valid This bit need user to set 0 to clear or be cleared by DMA_CONF.flush_txrx.
18	RW	0x0	slave_regaddr0_valid 1'b1: means DMA_SADDR2's bit[7:0]'s slave_addr is valid This bit need user to set 0 to clear or be cleared by DMA_CONF.flush_txrx.
17	RW	0x0	slave_addr1_valid 1'b1: means DMA_SADDR's bit[15:7]'s slave_addr is valid This bit need user to set 0 to clear or be cleared by DMA_CONF.flush_txrx.
16	RW	0x0	slave_addr_valid 1'b1: means DMA_SADDR's bit[7:0]'s slave_addr is valid This bit need user to set 0 to clear or be cleared by DMA_CONF.flush_txrx.
15:8	RW	0x00	slave_tx_slvaddr1 When DMA only transmits real txdata without including slave's address and slave's register address, write slave's device address to these bits. This will be sent after bit[7:0]. If DMA transmit slave's register address and real txdata together, you do not need this register. If you need this register, must config it before you config MTXCNT.

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	slave_tx_slvaddr When DMA only transmits real txdata without including slave's address and slave's register address, write slave's device address to these bits. If DMA transmit slave's address and real txdata together, you do not need this register. If you need this register, must config it before you config MTXCNT.

RKI2C_DMA_SADDR2

Address: **Operational Base** + offset (0x0084)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	slave_regaddr_3 when DMA only transmits real txdata without including slave's address and slave's register address, write slave's register address to these bits. These bits will be sent after DMA_SADDR2's bit[23:16]. If DMA transmit slave's register address and real txdata together, you do not need this register. If you need this register, must config it before you config MTXCNT and DMA_SADDR.
23:16	RW	0x00	slave_regaddr_2 when DMA only transmits real txdata without including slave's address and slave's register address, write slave's register address to these bits. These bits will be sent after DMA_SADDR2's bit[15:8]. If DMA transmit slave's register address and real txdata together, you do not need this register. If you need this register, must config it before you config MTXCNT and DMA_SADDR.
15:8	RW	0x00	slave_regaddr_1 when DMA only transmits real txdata without including slave's address and slave's register address, write slave's register address to these bits. These bits will be sent after DMA_SADDR2's bit[7:0]. If DMA transmit slave's register address and real txdata together, you do not need this register. If you need this register, must config it before you config MTXCNT and DMA_SADDR.
7:0	RW	0x00	slave_regaddr_0 when DMA only transmits real txdata without including slave's address and slave's register address, write slave's register address to these bits. These bits will be sent after DMA_SADDR's bits. If DMA transmit slave's register address and real txdata together, you do not need this register. If you need this register, must config it before you config MTXCNT and DMA_SADDR.

RKI2C_TXDMA

Address: **Operational Base** + offset (0x0088)

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Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	txdata Data to be transmitted that written by dma. Transfer 4 words at once, except for the last time. FIFO depth is 8.

RKI2C_RXDMA

Address: **Operational Base** + offset (0x008C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata Data received to be read by dma. Transfer 4 words at once, except for the last time. FIFO depth is 8.

RKI2C_DMA_CONF

Address: **Operational Base** + offset (0x0090)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:16	WO	0x00	mask
15:5	RO	0x000	reserved
4	WO	0x0	flush_txrx flush TXDMA/RXDMA fifo pointer and other related signals It will self-clear.
3	RO	0x0	reserved
2	RW	0x1	rkdma_choice_en 1'b0: use normal dma, without single requset 1'b1: use rkdma, with single request
1	RW	0x0	rxdma_use_enable 1'b0: disable 1'b1: enable
0	RW	0x0	txdma_use_enable 1'b0: disable 1'b1: enable

RKI2C_DMA_ST

Address: **Operational Base** + offset (0x0094)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RO	0x0	tx_second4_empty 1'b1: from txdata4 to txdata7 is empty.
2	RO	0x0	tx_first4_empty 1'b1: from txdata0 to txdata3 is empty.
1	RO	0x0	rx_second4_full 1'b1: from rxdata4 to rxdata7 is full.
0	RO	0x0	rx_first4_full 1'b1: from rxdata0 to rxdata3 is full.

RKI2C_DMA_TXCNT_ST

Address: **Operational Base** + offset (0x0098)

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Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RO	0x00000	dma_txcnt_st the num of word that DMA has sent to this i2c controller This can only be cleared by DMA_CONF.flush_txrx

RKI2C_DMX_RXCNT_ST

Address: **Operational Base** + offset (0x009C)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:0	RO	0x00000	dma_rxcnt_st the num of word that DMA have received from this i2c controller This can only be cleared by DMA_CONF.flush_txrx

RKI2C_TXDATA0

Address: **Operational Base** + offset (0x0100)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata0 Data0 to be transmitted. 32 bits data

RKI2C_TXDATA1

Address: **Operational Base** + offset (0x0104)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata1 Data1 to be transmitted. 32 bits data

RKI2C_TXDATA2

Address: **Operational Base** + offset (0x0108)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata2 Data2 to be transmitted. 32 bits data

RKI2C_TXDATA3

Address: **Operational Base** + offset (0x010C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata3 Data3 to be transmitted. 32 bits data

RKI2C_TXDATA4

Address: **Operational Base** + offset (0x0110)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata4 Data4 to be transmitted. 32 bits data

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RKI2C_TXDATA5

Address: **Operational Base** + offset (0x0114)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata5 Data5 to be transmitted. 32 bits data

RKI2C_TXDATA6

Address: **Operational Base** + offset (0x0118)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata6 Data6 to be transmitted. 32 bits data

RKI2C_TXDATA7

Address: **Operational Base** + offset (0x011C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata7 Data7 to be transmitted. 32 bits data

RKI2C_RXDATA0

Address: **Operational Base** + offset (0x0200)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata0 Data0 received. 32 bits data

RKI2C_RXDATA1

Address: **Operational Base** + offset (0x0204)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata1 Data1 received. 32 bits data

RKI2C_RXDATA2

Address: **Operational Base** + offset (0x0208)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata2 Data2 received. 32 bits data

RKI2C_RXDATA3

Address: **Operational Base** + offset (0x020C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata3 Data3 received. 32 bits data

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RKI2C_RXDATA4

Address: **Operational Base** + offset (0x0210)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata4 Data4 received. 32 bits data

RKI2C_RXDATA5

Address: **Operational Base** + offset (0x0214)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata5 Data5 received. 32 bits data

RKI2C_RXDATA6

Address: **Operational Base** + offset (0x0218)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata6 Data6 received. 32 bits data

RKI2C_RXDATA7

Address: **Operational Base** + offset (0x021C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata7 Data7 received. 32 bits data

RKI2C_ST

Address: **Operational Base** + offset (0x0220)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	scl_st SCL status. 1'b0: SCL status low. 1'b0: SCL status high.
0	RO	0x0	sda_st SDA status. 1'b0: SDA status low. 1'b0: SDA status high.

RKI2C_DBGCTRL

Address: **Operational Base** + offset (0x0224)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
14	RW	0x0	h0_check_scl 1'b0: Check if scl been pull down by slave at the whole SCL_HIGH. 1'b1: Check if scl been pull down by slave only at the h0 of SCL_HIGH(SCL_HIGH including h0~h7).
13	RW	0x0	nak_release_scl 1'b0: Hold scl as low when recieved nack. 1'b1: Release scl as high when recieved nack.
12	RW	0x0	flt_en SCL edage glitch filter enable. 1'b0: Disable 1'b1: Enable
11:8	RW	0x0	slv_hold_scl_th Slave hold scl threshold = slv_hold_scl_db * Tclk_i2c.
7:4	RW	0x0	flt_r Filter scl rising edge glitches of width less than flt_r * Tclk_i2c.
3:0	RW	0x0	flt_f Filter scl falling edge glitches of width less than flt_f * Tclk_i2c.

RKI2C_CON1

Address: **Operational Base** + offset (0x0228)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	auto_stop_nak Auto stop when i2c master recieved nak from slave. Work when CON1[0]=1'b1. 1'b0: Do not auto stop when recieved nak. 1'b1: Auto stop when recieved nak.
1	RW	0x0	auto_stop_tx_end Auto stop when i2c master tx end. Work when CON1[0]=1'b1. 1'b0: Do not auto stop when tx end. 1'b1: Auto stop when tx end.
0	RW	0x0	auto_stop Auto stop when i2c master recieved nak from slave or tx end. 1'b0: Do not auto stop when recieved nak or tx end. 1'b1: Auto stop when recieved nak or tx end.

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36.5 Interface Description

Table 36-1 I2C Interface Description

Module pin	Pad Name	IOMUX Setting
I2C0_SCL_M0	GPIO0_C2	GPIO0C_IOMUX_SEL_0[11:8] = 4'h4
I2C0_SCL_M1	GPIO2_A1	GPIO2A_IOMUX_SEL_0[7:4] = 4'h3
I2C0_SDA_M0	GPIO0_C3	GPIO0C_IOMUX_SEL_0[15:12] = 4'h4
I2C0_SDA_M1	GPIO2_A0	GPIO2A_IOMUX_SEL_0[3:0] = 4'h3
I2C1_SCL_M0	GPIO0_B3	GPIO0B_IOMUX_SEL_0[15:12] = 4'h3
I2C1_SCL_M1	GPIO3_A2	GPIO3A_IOMUX_SEL_0[11:8] = 4'h2
I2C1_SCL_M2	GPIO4_A1	GPIO4A_IOMUX_SEL_0[7:4] = 4'h6
I2C1_SCL_M3	GPIO7_B0	GPIO7B_IOMUX_SEL_0[3:0] = 4'h5
I2C1_SDA_M0	GPIO0_B4	GPIO0B_IOMUX_SEL_1[3:0] = 4'h3
I2C1_SDA_M1	GPIO3_A3	GPIO3A_IOMUX_SEL_0[15:12] = 4'h2
I2C1_SDA_M2	GPIO4_A0	GPIO4A_IOMUX_SEL_0[3:0] = 4'h6
I2C1_SDA_M3	GPIO7_B1	GPIO7B_IOMUX_SEL_0[7:4] = 4'h5
I2C2_SCL_M0	GPIO0_D0	GPIO0D_IOMUX_SEL_0[3:0] = 4'h1
I2C2_SCL_M1	GPIO5_D4	GPIO5D_IOMUX_SEL_1[3:0] = 4'h6
I2C2_SCL_M2	GPIO6_C0	GPIO6C_IOMUX_SEL_0[3:0] = 4'h7
I2C2_SDA_M0	GPIO0_D1	GPIO0D_IOMUX_SEL_0[7:4] = 4'h1
I2C2_SDA_M1	GPIO5_D5	GPIO5D_IOMUX_SEL_1[7:4] = 4'h6
I2C2_SDA_M2	GPIO6_C3	GPIO6C_IOMUX_SEL_0[15:12] = 4'h7
I2C3_SCL_M0	GPIO0_C0	GPIO0C_IOMUX_SEL_0[3:0] = 4'h1
I2C3_SCL_M1	GPIO4_A4	GPIO4A_IOMUX_SEL_1[3:0] = 4'h6
I2C3_SCL_M2	GPIO5_D0	GPIO5D_IOMUX_SEL_0[3:0] = 4'h6
I2C3_SCL_M3	GPIO6_A0	GPIO6A_IOMUX_SEL_0[3:0] = 4'h7
I2C3_SDA_M0	GPIO0_C1	GPIO0C_IOMUX_SEL_0[7:4] = 4'h1
I2C3_SDA_M1	GPIO4_A5	GPIO4A_IOMUX_SEL_1[7:4] = 4'h6
I2C3_SDA_M2	GPIO5_D1	GPIO5D_IOMUX_SEL_0[7:4] = 4'h6
I2C3_SDA_M3	GPIO6_A1	GPIO6A_IOMUX_SEL_0[7:4] = 4'h7
I2C4_SCL_M0	GPIO3_B4	GPIO3B_IOMUX_SEL_1[3:0] = 4'h5
I2C4_SCL_M1	GPIO6_A2	GPIO6A_IOMUX_SEL_0[11:8] = 4'h7
I2C4_SCL_M2	GPIO4_A7	GPIO4A_IOMUX_SEL_1[15:12] = 4'h6

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Module pin	Pad Name	IOMUX Setting
I2C4_SCL_M3	GPIO7_A1	GPIO7A_IOMUX_SEL_0[7:4] = 4'h2
I2C4_SDA_M0	GPIO3_B5	GPIO3B_IOMUX_SEL_1[7:4] = 4'h5
I2C4_SDA_M1	GPIO6_A3	GPIO6A_IOMUX_SEL_0[15:12] = 4'h7
I2C4_SDA_M2	GPIO4_A6	GPIO4A_IOMUX_SEL_1[11:8] = 4'h6
I2C4_SDA_M3	GPIO7_A4	GPIO7A_IOMUX_SEL_1[3:0] = 4'h2
I2C5_SCL_M0	GPIO0_C4	GPIO0C_IOMUX_SEL_1[3:0] = 4'h4
I2C5_SCL_M1	GPIO3_B6	GPIO3B_IOMUX_SEL_1[11:8] = 4'h5
I2C5_SCL_M2	GPIO5_A1	GPIO5A_IOMUX_SEL_0[7:4] = 4'h2
I2C5_SCL_M3	GPIO6_A4	GPIO6A_IOMUX_SEL_1[3:0] = 4'h7
I2C5_SDA_M0	GPIO0_C5	GPIO0C_IOMUX_SEL_1[7:4] = 4'h4
I2C5_SDA_M1	GPIO3_B7	GPIO3B_IOMUX_SEL_1[15:12] = 4'h5
I2C5_SDA_M2	GPIO5_A7	GPIO5A_IOMUX_SEL_1[15:12] = 4'h6
I2C5_SDA_M3	GPIO6_A5	GPIO6A_IOMUX_SEL_1[7:4] = 4'h7

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36.6 Application Notes

The I2C controller core operation flow chart below is to describe how the software configures and performs an I2C transaction through this I2C controller core. Descriptions are divided into 3 sections, transmit only mode, receive only mode, and mix mode. Users are strongly advised to follow:

- Transmit only mode (I2C_CON[1:0]=2'b00)

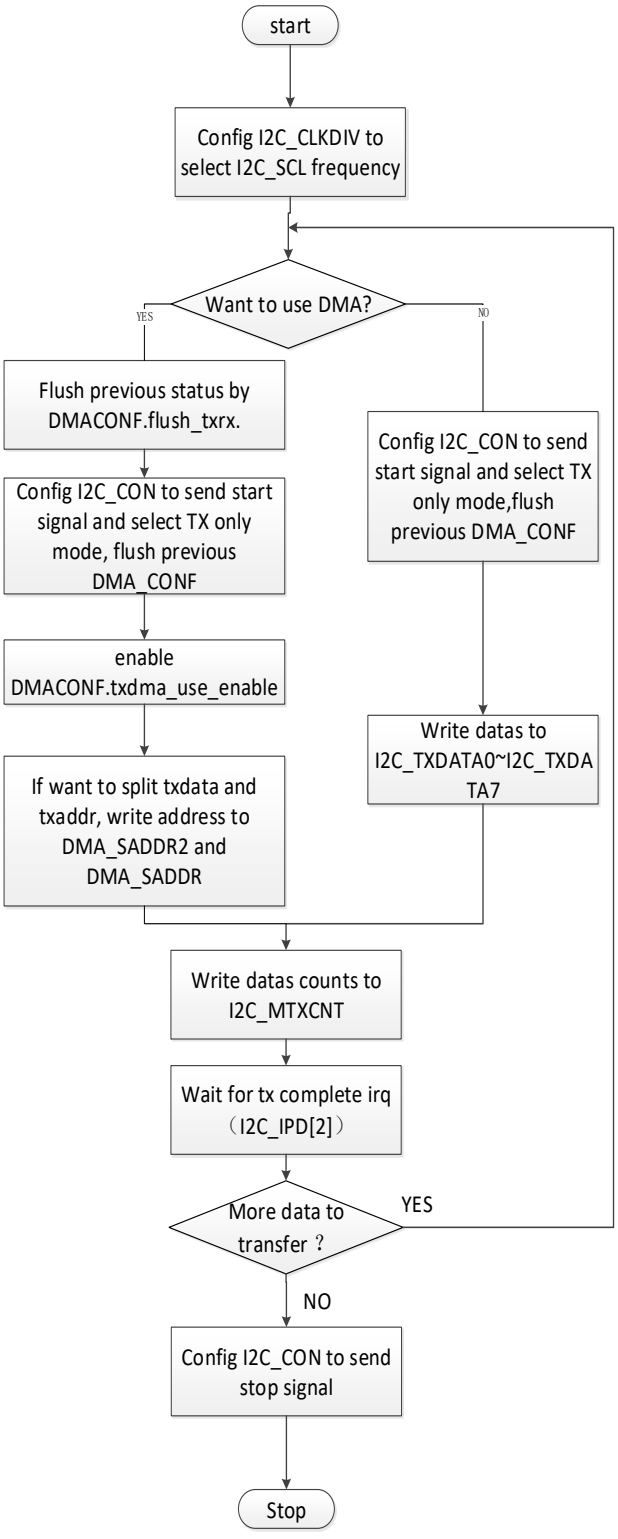

Fig.36-6 I2C Flow chat for transmit only mode

- Receive only mode (I2C_CON[1:0]=2'b10)

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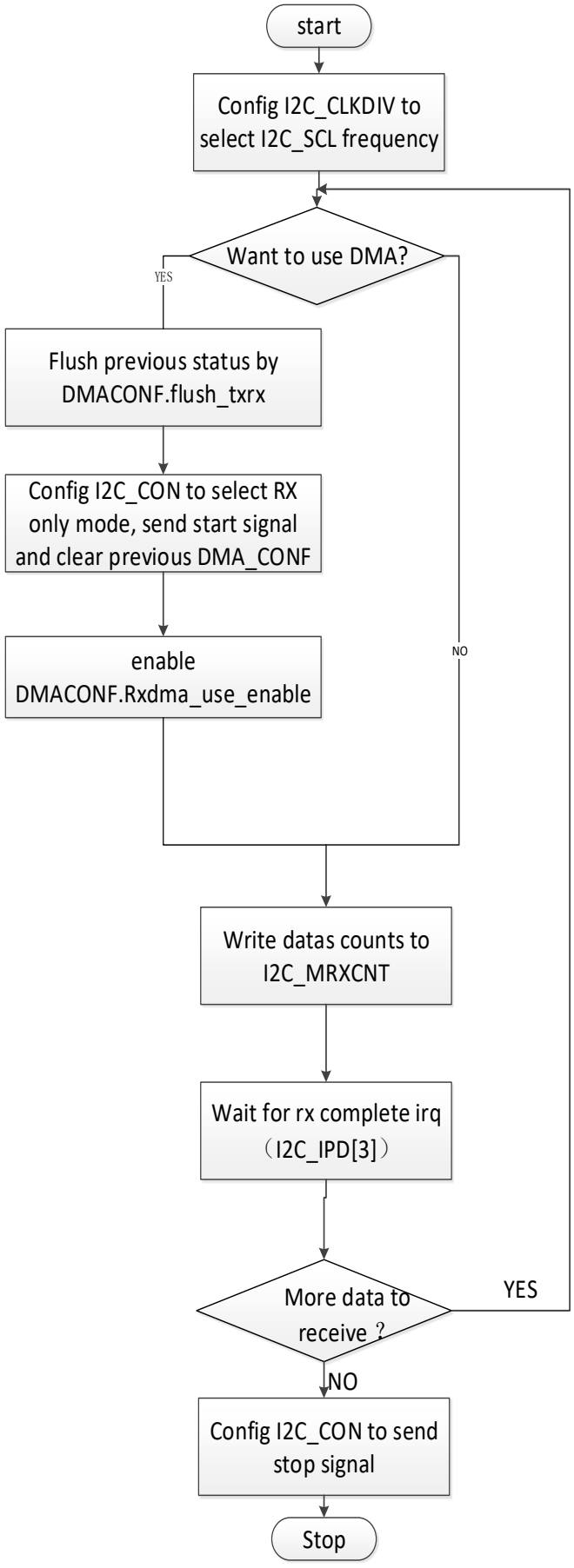

Fig.36-7 I2C Flow chat for receive only mode

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- Mix mode (I2C_CON[1:0]=2'b01 or I2C_CON[1:0]=2'b11)

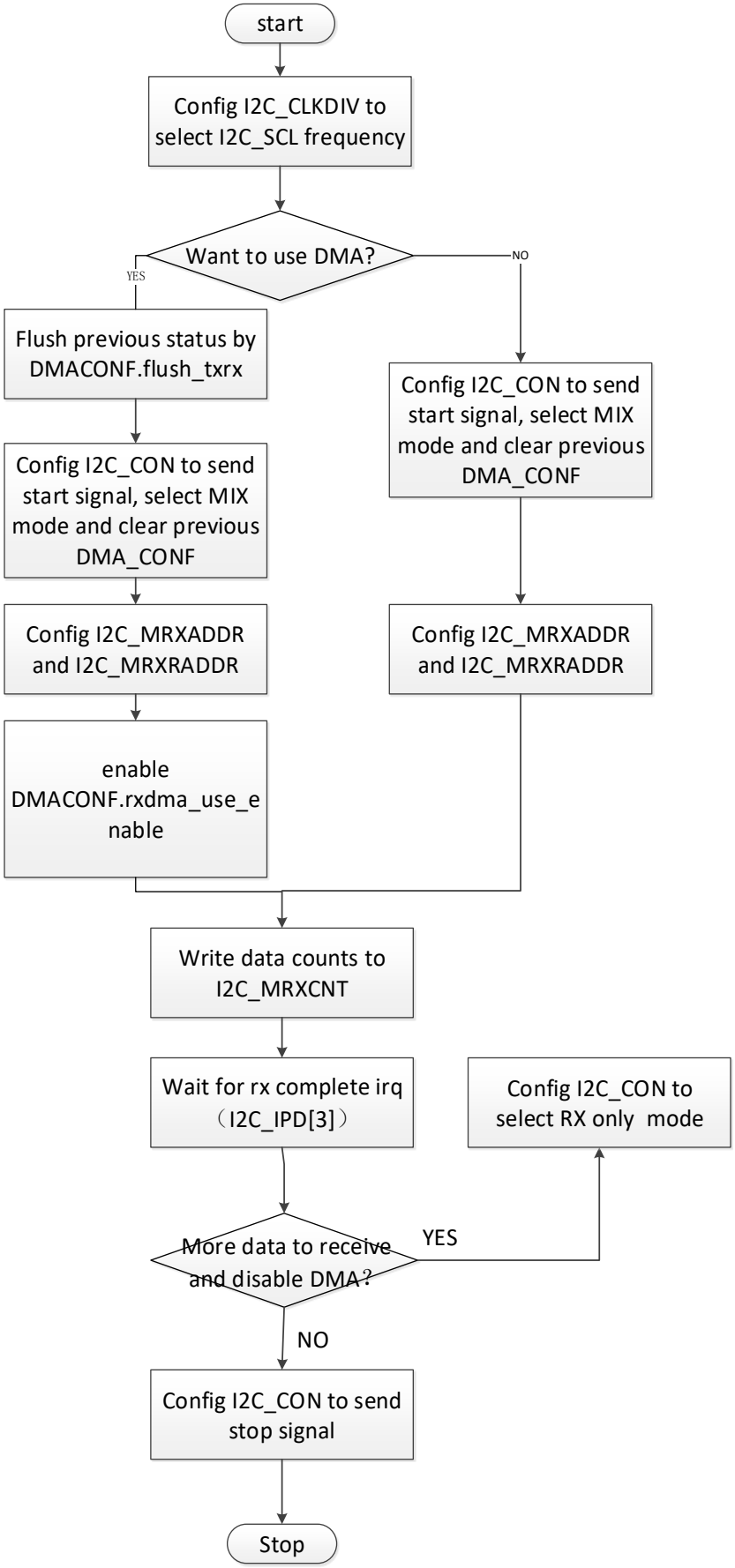

Fig.36-8 I2C Flow chat for mix mode

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Chapter 37 UART

37.1 Overview

The Universal Asynchronous Receiver/Transmitter (UART) is used for serial communication with a peripheral, modem (data carrier equipment, DCE) or data set. Data is written from a master (CPU) over the APB bus to the UART and it is converted to serial form and transmitted to the destination device. Serial data is also received by the UART and stored for the master (CPU) to read back.

UART Controller supports the following features:

- Support 8 independent UART controller: UART0-UART7
- All contain two 64 Bytes FIFOs for data receive and transmit
- UART1-UART7 support auto flow-control
- UART1-UART7 support RS485 function
- Support bit rates 115.2Kbps, 460.8Kbps, 921.6Kbps, 1.5Mbps, 3Mbps, 4Mbps
- Support programmable baud rates, even with non-integer clock divider
- Standard asynchronous communication bits (start, stop and parity)
- Support interrupt-based or DMA-based mode
- Support 5-8 bits width transfer
- Support RKDMA receive single request function. When the timeout signal is high, one single burst data is transmitted from receive FIFO

37.2 Block Diagram

This section provides a description about the functions and behavior under various conditions. The UART Controller comprises with:

- AMBA APB interface
- FIFO controllers
- Register block
- Modem synchronization block and baud clock generation block
- Serial receiver and serial transmitter

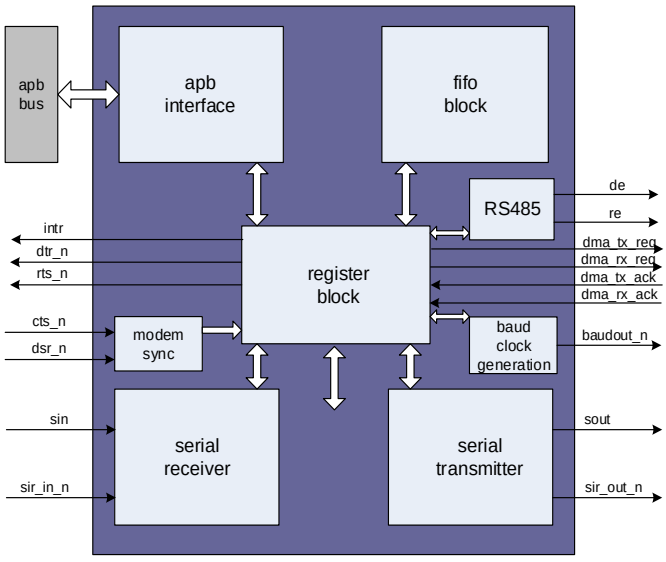

Fig. 37-1 UART Architecture

APB interface

The host processor accesses data, control, and status information on the UART through the APB interface. The UART supports APB data bus widths of 8, 16, and 32 bits.

Register block

Be responsible for the main UART functionality including control, status and interrupt generation.

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Modem Synchronization block
Synchronizes the modem input signal.

FIFO block
Be responsible for FIFO control and storage (when using internal RAM) or signaling to control external RAM (when used).

Baud Clock Generator
Generates the transmitter and receiver baud clock along with the output reference clock signal (baudout_n).

Serial Transmitter
Converts the parallel data, written to the UART, into serial form and adds all additional bits, as specified by the control register, for transmission.

Serial Receiver
Converts the serial data character (as specified by the control register) received to parallel form. Parity error detection, framing error detection and line break detection is carried out in this block.

37.3 Function Description

UART Serial Protocol
Because the serial communication is asynchronous, additional bits (start and stop) are added to the serial data to indicate the beginning and end. An additional parity bit may be added to the serial character. This bit appears after the last data bit and before the stop bit(s) in the character structure to perform simple error checking on the received data, as shown in Figure.

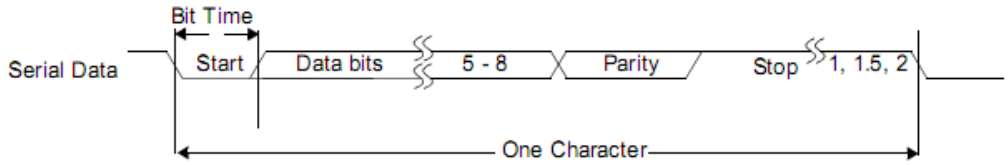

Fig. 37-2 UART Serial protocol

Baud Clock
The baud rate is controlled by the serial clock (sclk or pclk in a single clock implementation) and the Divisor Latch Register (DLH and DLL). As the exact number of baud clocks that each bit was transmitted for is known, calculating the mid-point for sampling is not difficult, that is every 16 baud clocks after the mid-point sample of the start bit.

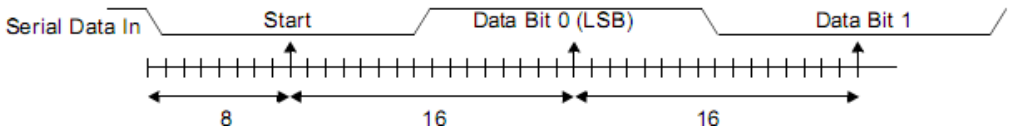

Fig. 37-3 UART baud rate

FIFO Support
1. NONE FIFO MODE
If FIFO support is not selected, then no FIFOs are implemented and only a single receive data byte and transmit data byte can be stored at a time in the RBR and THR.

2. FIFO MODE
The FIFO depth of is 64bytes. The FIFO mode of all the UART is enabled by register FCR[0].

Interrupts
The following interrupt types can be enabled with the IER register.

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- Receiver Error
- Receiver Data Available
- Character Timeout (in FIFO mode only)
- Transmitter Holding Register Empty at/below threshold (in Programmable THRE Interrupt mode)
- Modem Status

DMA Support

The UART supports DMA signaling with the use of two output signals (dma_tx_req_n and dma_rx_req_n) to indicate when data is ready to be read or when the transmit FIFO is empty.

The dma_tx_req_n signal is asserted under the following conditions:

- When the Transmitter Holding Register is empty in non-FIFO mode.
- When the transmitter FIFO is empty in FIFO mode with Programmable THRE interrupt mode disabled.
- When the transmitter FIFO is at, or below the programmed threshold with Programmable THRE interrupt mode enabled.

The dma_rx_req_n signal is asserted under the following conditions:

- When there is a single character available in the Receive Buffer Register in non-FIFO mode.
- When the Receiver FIFO is at or above the programmed trigger level in FIFO mode.

Auto Flow Control

The UART can be configured to have a 16750-compatible Auto RTS and Auto CTS serial data flow control mode available. If FIFOs are not implemented, then this mode cannot be selected. When Auto Flow Control mode has been selected, it can be enabled with the Modem Control Register (MCR[5]). Following figure shows a block diagram of the Auto Flow Control functionality.

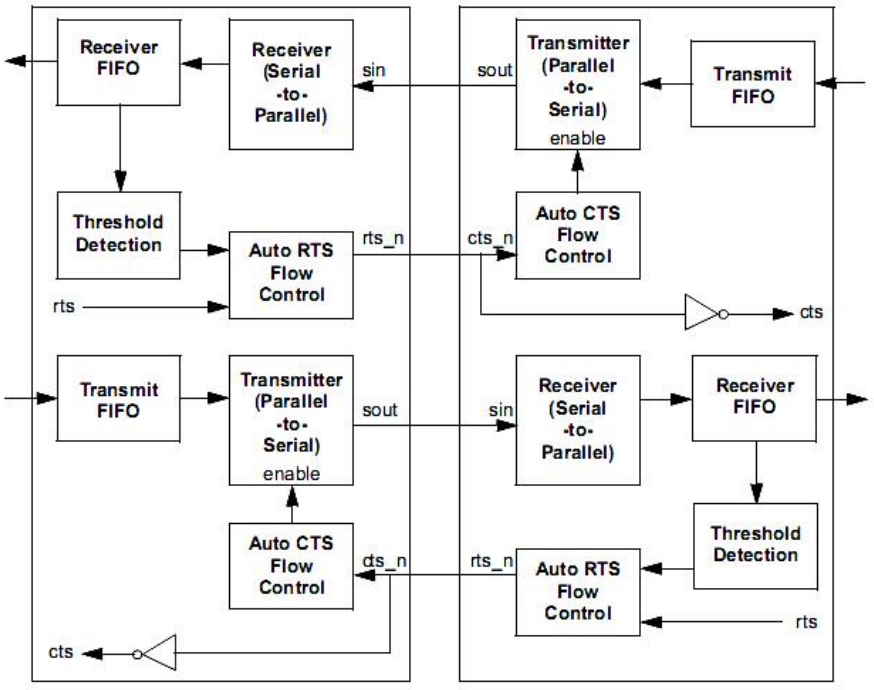

Fig. 37-4 UART Auto flow control block diagram

Auto RTS – Becomes active when the following occurs:

- Auto Flow Control is selected during configuration
- FIFOs are implemented
- RTS (MCR[1] bit and MCR[5]bit are both set)
- FIFOs are enabled (FCR[0]) bit is set)
- SIR mode is disabled (MCR[6] bit is not set)

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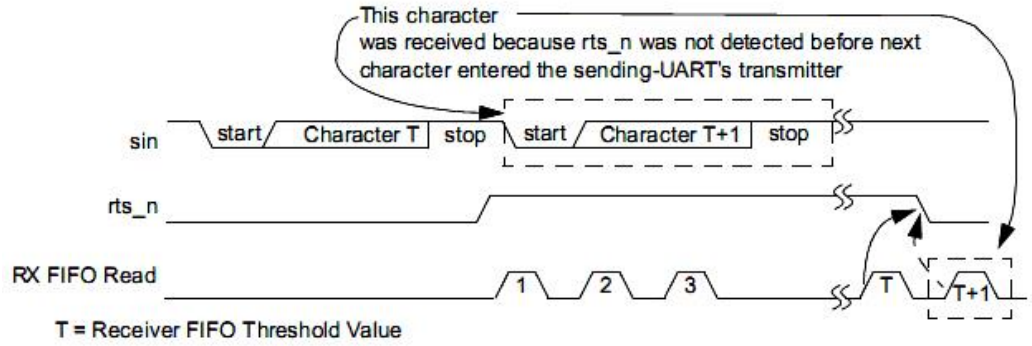

Fig. 37-5 UART AUTO RTS TIMING

Auto CTS – becomes active when the following occurs:

- Auto Flow Control is selected during configuration
- FIFOs are implemented
- AFCE (MCR[5] bit is set)
- FIFOs are enabled through FIFO Control Register FCR[0] bit
- SIR mode is disabled (MCR[6] bit is not set)

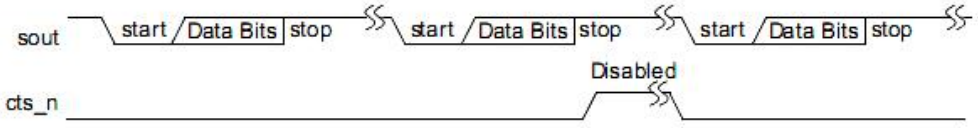

Fig. 37-6 UART AUTO CTS TIMING

RS485 Mode

The RS485 standard supports serial communication over a twisted pair configuration. The difference between the RS232 and RS485 standards is its use of a balanced line for transmission. This usage is also known as the differential format that sends the same signal on two separate lines with phase delay and then compares the signals at the end, subtracts any noise, and adds them to regain signal strength. This process allows the RS485 standard to be viable over significantly longer distances than its short range RS232 counterpart.

UART supports hardware mode and software mode.

- Hardware mode, DE and RE are mutually exclusive. By default 'de' and 're' will be disabled. When at user mode, user should program the DE to active the 'de', while at auto mode, DE will assert when transfer starts. Once the TX FIFO becomes empty and the stop bit be sampled, 're' signal gets enabled and 'de' signal will be disabled, automatically. In this mode, hardware will consider the de-inactive timing and turn around timing, which are programmed in the DET and TAT register, respectively. When 'de' is valid, it is useless to configure RE, and vice versa.
- Software mode, transmit and receive can happen simultaneously. The user can enable DE, RE at any point of time. Turn around timing as programmed in the TAT register and de-inactive timing as programmed in the DET are not applicable in this mode.

37.4 Register Description

37.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
UART0	0x20810000
UART1	0x21160000
UART2	0x21170000
UART3	0x21180000
UART4	0x21190000

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Name	Base Address
UART5	0x211A0000
UART6	0x211B0000
UART7	0x211C0000

37.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
UART_RBR	0x0000	W	0x00000000	Receive Buffer Register
UART_DLL	0x0000	W	0x00000000	Divisor Latch Low
UART_THR	0x0000	W	0x00000000	Transmit Buffer Register
UART_DLH	0x0004	W	0x00000000	Divisor Latch High
UART_IER	0x0004	W	0x00000000	Interrupt Enable Register
UART_FCR	0x0008	W	0x00000000	FIFO Enable
UART_IIR	0x0008	W	0x00000001	Interrupt Identity Register
UART_LCR	0x000C	W	0x00000000	Line Control Register
UART_MCR	0x0010	W	0x00000000	Modem Control Register
UART_LSR	0x0014	W	0x00000060	Line Status Register
UART_MSR	0x0018	W	0x00000000	Modem Status Register
UART_SCR	0x001C	W	0x00000000	Scratchpad Register
UART_SRBR	0x0030	W	0x00000000	Shadow Receive Buffer Register
UART_STHR	0x0030	W	0x00000000	Shadow Transmit Holding Register
UART_FAR	0x0070	W	0x00000000	FIFO Access Register
UART_TFR	0x0074	W	0x00000000	Transmit FIFO Read
UART_RFW	0x0078	W	0x00000000	Receive FIFO write
UART_USR	0x007C	W	0x00000006	UART Status Register
UART_TFL	0x0080	W	0x00000000	Transmit FIFO level
UART_RFL	0x0084	W	0x00000000	Receive FIFO level
UART_SRR	0x0088	W	0x00000000	Software Reset Register
UART_SRTS	0x008C	W	0x00000000	Shadow Request to Send
UART_SBCR	0x0090	W	0x00000000	Shadow Break Control Register
UART_SDMAM	0x0094	W	0x00000000	Shadow DMA Mode
UART_SFE	0x0098	W	0x00000000	Shadow FIFO enable
UART_SRT	0x009C	W	0x00000000	Shadow RCVR Trigger
UART_STET	0x00A0	W	0x00000000	Shadow TX Empty Trigger
UART_HTX	0x00A4	W	0x00000000	Halt TX
UART_DMASA	0x00A8	W	0x00000000	DMA Software Acknowledge
UART_TCR	0x00AC	W	0x00000000	Transceiver Control Register
UART_DE	0x00B0	W	0x00000000	Driver Output Enable Register
UART_RE	0x00B4	W	0x00000000	Receiver Output Enable Register
UART_DET	0x00B8	W	0x00000000	Driver Output Enable Timing Register
UART_TAT	0x00BC	W	0x00000000	Turn Around Timing Register
UART_CPR	0x00F4	W	0x00043FF2	Component Parameter Register
UART_UCV	0x00F8	W	0x3430322A	UART Component Version
UART_CTR	0x00FC	W	0x44570110	Component Type Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

37.4.3 Detail Registers Description

UART_RBR

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RO	0x00	data_input Data byte received on the serial input port (sin) in UART mode, or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line Status Register (LCR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an over-run error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO is preserved, but any incoming data are lost and an over-run error occurs.

UART_DLL

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	baud_rate_divisor_l Lower 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate is equal to the serial clock (pclk if one clock design, sclk if two clock design (CLOCK_MODE == Enabled)) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLL is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

UART_THR

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	WO	0x00	data_output Data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If in non-FIFO mode or FIFOs are disabled (FCR[0] = 0) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If in FIFO mode and FIFOs are enabled (FCR[0] = 1) and THRE is set, 64 characters of data may be written to the THR before the FIFO is full.. Any attempt to write data when the FIFO is full results in the write data being lost.

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UART_DLH

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	baud_rate_divisor_h Upper 8-bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero). The output baud rate is equal to the serial clock (pclk if one clock design, sclk if two clock design CLOCK_MODE == Enabled)) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLH is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

UART_IER

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	prog_thre_int_en Programmable THRE Interrupt Mode Enable that can be written to only when THRE_MODE_USER == Enabled, always readable. This is used to enable/disable the generation of THRE Interrupt. 1'b0: Disabled 1'b1: Enabled
6:4	RO	0x0	reserved
3	RW	0x0	modem_status_int_en Enable Modem Status Interrupt. This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt. 1'b0: Disabled 1'b1: Enabled
2	RW	0x0	receive_line_status_int_en Enable Receiver Line Status Interrupt. This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 1'b0: Disabled 1'b1: Enabled
1	RW	0x0	trans_hold_empty_int_en Enable Transmit Holding Register Empty Interrupt. This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. 1'b0: Disabled 1'b1: Enabled

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Bit	Attr	Reset Value	Description
0	RW	0x0	receive_data_available_int_en Enable Received Data Available Interrupt. This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second highest priority interrupts. 1'b0: Disabled 1'b1: Enabled

UART_FCR

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	WO	0x0	rcvr_trigger at which the Received Data Available Interrupt is generated. In auto flow control mode it is used to determine when the rts_n signal is de-asserted. It also determines when the dma_rx_req_n signal is asserted in certain modes of operation. For details on DMA support, refer to "DMA Support". The following trigger levels are supported: 2'b00: 1 character in the FIFO 2'b01: FIFO 1/4 full 2'b10: FIFO 1/2 full 2'b11: FIFO 2 less than full
5:4	WO	0x0	tx_empty_trigger TX Empty Trigger. Writes have no effect when THRE_MODE_USER == Disabled. This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. It also determines when the dma_tx_req_n signal is asserted when in certain modes of operation. For details on DMA support, refer to " DMA Support". The following trigger levels are supported: 2'b00: FIFO empty 2'b01: 2 characters in the FIFO 2'b10: FIFO 1/4 full 2'b11: FIFO 1/2 full
3	WO	0x0	dma_mode DMA Mode. This determines the DMA signalling mode used for the dma_tx_req_n and dma_rx_req_n output signals when additional DMA handshaking signals are not selected (DMA_EXTRA == No). For details on DMA support, refer to DMA Support. 1'b0: Mode 0 1'b1: Mode 1
2	WO	0x0	xmit_fifo_reset XMIT FIFO Reset. This resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit.

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Bit	Attr	Reset Value	Description
1	WO	0x0	rcvr_fifo_reset RCVR FIFO Reset. This resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
0	WO	0x0	fifo_en FIFO Enable. This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFOs is reset.

UART_IIR

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:6	RO	0x0	fifos_en FIFOs Enabled. This is used to indicate whether the FIFOs are enabled or disabled. 2'b00: Disabled 2'b11: Enabled
5:4	RO	0x0	reserved
3:0	RO	0x1	int_id Interrupt ID. This indicates the highest priority pending interrupt which can be one of the following types: 4'b0000: Modem status 4'b0001: No interrupt pending 4'b0010: THR empty 4'b0100: Received data available 4'b0110: Receiver line status 4'b0111: Busy detect 4'b1100: Character timeout The interrupt priorities are split into four levels that are detailed in Table X. Bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt.

UART_LCR

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	div_lat_access Divisor Latch Access Bit.Writeable only when UART is not busy (USR[0] is zero), always readable. This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers.

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Bit	Attr	Reset Value	Description
6	RW	0x0	break_ctrl Break Control Bit.This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.
5	RW	0x0	stick_parity If UART_16550_COMPATIBLE = NO, then writeable only when UART is not busy (USR[0] is 0); otherwise always writable and always readable. This bit is used to force parity value. When PEN, EPS and Stick Parity are set to 1, the parity bit is transmitted and checked as logic 0. If PEN and Stick Parity are set to 1 and EPS is a logic 0, then parity bit is transmitted and checked as a logic 1. If this bit is set to 0, Stick Parity is disabled.
4	RW	0x0	even_parity_sel Even Parity Select. Writeable only when UART is not busy (USR[0] is zero), always readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). If set to one, an even number of logic 1s is transmitted or checked. If set to zero, an odd number of logic 1s is transmitted or checked.
3	RW	0x0	parity_en Parity Enable. Writeable only when UART is not busy (USR[0] is zero), always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively. 1'b0: Parity disabled 1'b1: Parity enabled
2	RW	0x0	stop_bits_num Number of stop bits. Writeable only when UART is not busy (USR[0] is zero), always readable. This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. 1'b0: 1 stop bit. 1'b1: 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit.

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	data_length_sel Data Length Select. Writeable only when UART is not busy (USR[0] is zero), always readable. This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows: 2'b00: 5 bits 2'b01: 6 bits 2'b10: 7 bits 2'b11: 8 bits

UART_MCR

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	sir_mode_en SIR Mode Enable. Writeable only when SIR_MODE == Enabled, always readable. This is used to enable/disable the IrDA SIR Mode features as described in "IrDA 1.0 SIR Protocol". 1'b0: IrDA SIR Mode disabled 1'b1: IrDA SIR Mode enabled
5	RW	0x0	auto_flow_ctrl_en Auto Flow Control Enable. Writeable only when AFCE_MODE == Enabled, always readable. When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled as described in "Auto Flow Control". 1'b0: Auto Flow Control Mode disabled 1'b1: Auto Flow Control Mode enabled
4	RW	0x0	loopback LoopBack Bit. This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled or not active, MCR[6] set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, MCR[6] set to one), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line.
3	RW	0x0	out2 OUT2. This is used to directly control the user-designated Output2 (out2_n) output. The value written to this location is inverted and driven out on out2_n, that is: 1'b0: Out2_n de-asserted (logic 1) 1'b1: Out2_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the out2_n output is held inactive high while the value of this location is internally looped back to an input.

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Bit	Attr	Reset Value	Description
2	RW	0x0	out1 OUT1. This is used to directly control the user-designated Output1 (out1_n) output. The value written to this location is inverted and driven out on out1_n, that is: 1'b0: Out1_n de-asserted (logic 1) 1'b1: Out1_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the out1_n output is held inactive high while the value of this location is internally looped back to an input.
1	RW	0x0	req_to_send Request to Send. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high.In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFOs enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low. Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input.
0	RW	0x0	data_terminal_ready Data Terminal Ready. This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n, that is: 1'b0: dtr_n de-asserted (logic 1) 1'b1: dtr_n asserted (logic 0) The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive

UART_LSR

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	receiver_fifo_error Receiver FIFO Error bit. This bit is only relevant when FIFO_MODE != NONE AND FIFOs are enabled (FCR[0] set to one). This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO. 1'b0: No error in RX FIFO 1'b1: Error in RX FIFO This bit is cleared when the LSR is read and the character with the error is at the top of the receiver FIFO and there are no subsequent errors in the FIFO.

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Bit	Attr	Reset Value	Description
6	RO	0x1	trans_empty Transmitter Empty bit. If in FIFO mode (FIFO_MODE != NONE) and FIFOs enabled (FCR[0] set to one), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If in non-FIFO mode or FIFOs are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty.
5	RO	0x1	trans_hold_reg_empty Transmit Holding Register Empty bit. If THRE_MODE_USER == Disabled or THRE mode is disabled (IER[7] set to zero) and regardless of FIFO's being implemented/enabled or not, this bit indicates that the THR or TX FIFO is empty. This bit is set whenever data is transferred from the THR or TX FIFO to the transmitter shift register and no new data has been written to the THR or TX FIFO. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled. If THRE_MODE_USER == Enabled AND FIFO_MODE != NONE and both modes are active (IER[7] set to one and FCR[0] set to one respectively), the functionality is switched to indicate the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the FCR[5:4] threshold setting.
4	RO	0x0	break_int Break Interrupt bit. This is used to indicate the detection of a break sequence on the serial input data. If in UART mode (SIR_MODE == Disabled), it is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. If in infrared mode (SIR_MODE == Enabled), it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read.
3	RO	0x0	framing_error Framing Error bit. This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 1'b0: No framing error 1'b1: Framing error Reading the LSR clears the FE bit.

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Bit	Attr	Reset Value	Description
2	RO	0x0	parity_error Parity Error bit. This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 1'b0: No parity error 1'b1: Parity error Reading the LSR clears the PE bit.
1	RO	0x0	overrun_error Overrun error bit. This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. 1'b0: No overrun error 1'b1: Overrun error Reading the LSR clears the OE bit.
0	RO	0x0	data_ready Data Ready bit. This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. 1'b0: No data ready 1'b1: Data ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode.

UART_MSR

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	data_carrier_detect Data Carrier Detect. This is used to indicate the current state of the modem control line dcd_n. This bit is the complement of dcd_n. When the Data Carrier Detect input (dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set. 1'b0: dcd_n input is de-asserted (logic 1) 1'b1: dcd_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DCD is the same as MCR[3] (Out2).

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Bit	Attr	Reset Value	Description
6	RO	0x0	ring_indicator Ring Indicator. This is used to indicate the current state of the modem control line ri_n. This bit is the complement of ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. 1'b0: ri_n input is de-asserted (logic 1) 1'b1: ri_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), RI is the same as MCR[2] (Out1).
5	RO	0x0	data_set_ready Data Set Ready. This is used to indicate the current state of the modem control line dsr_n. This bit is the complement of dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with the UART. 1'b0: dsr_n input is de-asserted (logic 1) 1'b1: dsr_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR).
4	RO	0x0	clear_to_send Clear to Send. This is used to indicate the current state of the modem control line cts_n. This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with the UART. 1'b0: cts_n input is de-asserted (logic 1) 1'b1: cts_n input is asserted (logic 0) In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS).
3	RO	0x0	delta_data_carrier_detect Delta Data Carrier Detect. This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. 1'b0: No change on dcd_n since last read of MSR 1'b1: Change on dcd_n since last read of MSR Reading the MSR clears the DDCD bit. In Loopback Mode (MCR[4] = 1), DDCD reflects changes on MCR[3] (Out2). Note, if the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit is set when the reset is removed if the dcd_n signal remains asserted.
2	RO	0x0	trailing_edge_ring_indicator Trailing Edge of Ring Indicator. This is used to indicate that a change on the input ri_n (from an active-low to an inactive-high state) has occurred since the last time the MSR was read. 1'b0: No change on ri_n since last read of MSR 1'b1: Change on ri_n since last read of MSR Reading the MSR clears the TERI bit. In Loopback Mode (MCR[4] = 1), TERI reflects when MCR[2] (Out1) has changed state from a high to a low.

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Bit	Attr	Reset Value	Description
1	RO	0x0	delta_data_set_ready Delta Data Set Ready. This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. 1'b0: No change on dsr_n since last read of MSR 1'b1: Change on dsr_n since last read of MSR Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] = 1), DDSR reflects changes on MCR[0] (DTR). Note, if the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit is set when the reset is removed if the dsr_n signal remains asserted.
0	RO	0x0	delta_clear_to_send Delta Clear to Send. This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. 1'b0: No change on ctsdsr_n since last read of MSR 1'b1: Change on ctsdsr_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS). Note, if the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit is set when the reset is removed if the cts_n signal remains asserted.

UART_SCR

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	temp_store_space Scratchpad register.This register is for programmers to use as a temporary storage space. It has no defined purpose in the UART.

UART_SRBR

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RO	0x00	shadow_rbr This is a shadow register for the RBR and has been allocated sixteen 32-bit locations (0x30-0x6c) so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If in non-FIFO mode (FIFO_MODE == NONE) or FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If in FIFO mode (FIFO_MODE != NONE) and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs.

UART_STHR

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	WO	0x00	shadow_thr This is a shadow register for the THR and has been allocated sixteen 32-bit locations(0x30-0x6c) so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If in non-FIFO mode or FIFOs are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If in FIFO mode and FIFOs are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.

UART_FAR

Address: **Operational Base** + offset (0x0070)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	fifo_access_test_en Writes have no effect when FIFO_ACCESS == No, always readable. This register is use to enable a FIFO access mode for testing, so that the receive FIFO can be written by the master and the transmit FIFO can be read by the master when FIFOs are implemented and enabled. When FIFOs are not implemented or not enabled it allows the RBR to be written by the master and the THR to be read by the master. 1'b0: FIFO access mode disabled 1'b1: FIFO access mode enabled Note, that when the FIFO access mode is enabled/disabled, the control portion of the receive FIFO and transmit FIFO is reset and the FIFOs are treated as empty.

UART_TFR

Address: **Operational Base** + offset (0x0074)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	trans_fifo_read Transmit FIFO Read. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, reading this register gives the data at the top of the transmit FIFO. Each consecutive read pops the transmit FIFO and gives the next data value that is currently at the top of the FIFO. When FIFOs are not implemented or not enabled, reading this register gives the data in the THR.

UART_RFW

Address: **Operational Base** + offset (0x0078)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	WO	0x0	receive_fifo_framing_error Receive FIFO Framing Error. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, this bit is used to write framing error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write framing error detection information to the RBR.
8	WO	0x0	receive_fifo_parity_error Receive FIFO Parity Error. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, this bit is used to write parity error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write parity error detection information to the RBR.

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Bit	Attr	Reset Value	Description
7:0	WO	0x00	receive_fifo_write Receive FIFO Write Data. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, the data that is written to the RFWD is pushed into the receive FIFO. Each consecutive write pushes the new data to the next write location in the receive FIFO. When FIFOs are not implemented or not enabled, the data that is written to the RFWD is pushed into the RBR.

UART_USR

Address: **Operational Base** + offset (0x007C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RO	0x0	receive_fifo_full Receive FIFO Full. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO is completely full. 1'b0: Receive FIFO not full 1'b1: Receive FIFO Full This bit is cleared when the RX FIFO is no longer full.
3	RO	0x0	receive_fifo_not_empty Receive FIFO Not Empty. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the receive FIFO contains one or more entries. 1'b0: Receive FIFO is empty 1'b1: Receive FIFO is not empty This bit is cleared when the RX FIFO is empty.
2	RO	0x1	trasn_fifo_empty Transmit FIFO Empty. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO is completely empty. 1'b0: Transmit FIFO is not empty 1'b1: Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty.
1	RO	0x1	trans_fifo_not_full Transmit FIFO Not Full. This bit is only valid when FIFO_STAT == YES. This is used to indicate that the transmit FIFO in not full. 1'b0: Transmit FIFO is full 1'b1: Transmit FIFO is not full This bit is cleared when the TX FIFO is full.

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Bit	Attr	Reset Value	Description
0	RO	0x0	uart_busy UART Busy. This is indicates that a serial transfer is in progress, when cleared indicates that the UART is idle or inactive. 1'b0: UART is idle or inactive 1'b1: UART is busy (actively transferring data) Note that it is possible for the UART Busy bit to be cleared even though a new character may have been sent from another device. That is, if the UART has no data in THR and RBR and there is no transmission in progress and a start bit of a new character has just reached the UART. This is due to the fact that a valid start is not seen until the middle of the bit period and this duration is dependent on the baud divisor that has been programmed. If a second system clock has been implemented (CLOCK_MODE == Enabled), the assertion of this bit is also delayed by several cycles of the slower clock.

UART_TFL

Address: **Operational Base** + offset (0x0080)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RO	0x00	trans_fifo_level Transmit FIFO Level. This is indicates the number of data entries in the transmit FIFO.

UART_RFL

Address: **Operational Base** + offset (0x0084)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RO	0x00	receive_fifo_level Receive FIFO Level. This is indicates the number of data entries in the receive FIFO.

UART_SRR

Address: **Operational Base** + offset (0x0088)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	WO	0x0	xmit_fifo_reset XMIT FIFO Reset. This is a shadow register for the XMIT FIFO Reset bit (FCR[2]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the transmit FIFO. This resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit.

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Bit	Attr	Reset Value	Description
1	WO	0x0	rcvr_fifo_reset RCVR FIFO Reset. This is a shadow register for the RCVR FIFO Reset bit (FCR[1]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the receive FIFO This resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request and single signals when additional DMA handshaking signals are selected (DMA_EXTRA == YES). Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
0	WO	0x0	uart_reset UART Reset. This asynchronously resets the UART and synchronously removes the reset assertion. For a two clock implementation both pclk and sclk domains are reset.

UART_SRTS

Address: **Operational Base** + offset (0x008C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	shadow_req_to_send Shadow Request to Send. This is a shadow register for the RTS bit (MCR[1]), this can be used to remove the burden of having to performing a read-modify-write on the MCR. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] = 0), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] = 1) and FIFOs enable (FCR[0] = 1), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). Note that in Loopback mode (MCR[4] = 1), the rts_n output is held inactive-high while the value of this location is internally looped back to an input.

UART_SBCR

Address: **Operational Base** + offset (0x0090)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	shadow_break_ctrl Shadow Break Control Bit. This is a shadow register for the Break bit (LCR[6]), this can be used to remove the burden of having to performing a read modify write on the LCR. This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] = 1) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver.

UART_SDMAM

Address: **Operational Base** + offset (0x0094)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	shadow_dma_mode Shadow DMA Mode. This is a shadow register for the DMA mode bit (FCR[3]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the DMA Mode bit gets updated. This determines the DMA signalling mode used for the dma_tx_req_n and dma_rx_req_n output signals when additional DMA handshaking signals are not selected (DMA_EXTRA == NO). 1'b0: Mode 0 1'b1: Mode 1

UART_SFE

Address: **Operational Base** + offset (0x0098)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	shadow_fifo_en Shadow FIFO Enable. This is a shadow register for the FIFO enable bit (FCR[0]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the FIFO enable bit gets updated.This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. If this bit is set to zero (disabled) after being enabled then both the XMIT and RCVR controller portion of FIFOs are reset.

UART_SRT

Address: **Operational Base** + offset (0x009C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	shadow_rcvr_trigger Shadow RCVR Trigger. This is a shadow register for the RCVR trigger bits (FCR[7:6]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask thisvalue so that only the RCVR trigger bit gets updated.This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. It also determines when the dma_rx_req_n signal is asserted when DMA Mode (FCR[3]) = 1. The following trigger levels are supported: 2'b00: 1 character in the FIFO 2'b01: FIFO 1/4 full 2'b10: FIFO 1/2 full 2'b11: FIFO 2 less than full

UART_STET

Address: **Operational Base** + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	shadow_tx_empty_trigger Shadow TX Empty Trigger. This is a shadow register for the TX empty trigger bits (FCR[5:4]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the TX empty trigger bit gets updated.This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. The following trigger levels are supported: 2'b00: FIFO empty 2'b01: 2 characters in the FIFO 2'b10: FIFO 1/4 full 2'b11: FIFO 1/2 full

UART_HTX

Address: **Operational Base** + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	halt_tx_en This register is use to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFOs are implemented and enabled. 1'b0: Halt TX disabled 1'b1: Halt TX enabled Note, if FIFOs are implemented and not enabled, the setting of the halt TX register has no effect on operation.

UART_DMASA

Address: **Operational Base** + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
0	WO	0x0	dma_software_ack This register is use to perform a DMA software acknowledge if a transfer needs to be terminated due to an error condition. For example, if the DMA disables the channel, then the UART should clear its request. This causes the TX request, TX single, RX request and RX single signals to de-assert. Note that this bit is 'self-clearing'. It is not necessary to clear this bit.

UART_TCR

Address: **Operational Base** + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	auto_de Assert DE Automatically Enable. When data is written to the TXFIFO, the DE will automatically asserted, meanwhile, the RE will automatically de-asserted. 1'b0: Disable. 1'b1: Enable.
4	RW	0x0	re_pol Receiver Enable Polarity. 1'b0: re signal is active low. 1'b1: re signal is active high.
3	RW	0x0	de_pol Driver Enable Polarity. 1'b0: de signal is active high. 1'b1: de signal is active low.
2	RW	0x0	xfer_mode Transfer Mode. 1'b0: Hardware mode, DE and RE are mutually exclusive. By default 'de' and 're' will be disabled. User should program the DE to active the 'de'. Once the TX FIFO becomes empty and the stop bit be sampled, 're' signal gets enabled and 'de' signal will be disabled, automatically. In this mode, hardware will consider the de-inactive timing and turn around timing (applied for 4 wire mode only), which are programmed in the DET and TAT register, respectively. When 'de' is valid, it is useless to configure RE, and vice versa. 1'b1: Software mode, transmit and receive can happen simultaneously. The user can enable DE, RE at any point of time. Turn around timing as programmed in the TAT register and de-inactive timing as programmed in the DET are not applicable in this mode.
1	RW	0x0	re_en Receiver Enable. 1'b0: RE signal disable, DE control both transmit and receive process. Correspondingly, assert DE for transmit state, while de-assert DE for receive state. In this scenario, RE-associated logics and TAT register will hold constant for lower power consumption. 1'b1: RE signal enable, DE control the transmit process, and RE control the receive process.

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Bit	Attr	Reset Value	Description
0	RW	0x0	rs485_en RS485 Enable. 1'b0: In this mode, the transfers are still in the RS232 mode. The registers of DE, RE, DET and TAT are reserved. 1'b1: In this mode, the transfers will happen in RS485 mode.

UART_DE

Address: **Operational Base** + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	de The 'de' register bit is used to control assertion and de-assertion of 'de' signal. 1'b0: De-assert 'de' signal. 1'b1: Assert 'de' signal.

UART_RE

Address: **Operational Base** + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	re The 're' register bit is used to control assertion and de-assertion of 're' signal. 1'b0: De-assert 're' signal. 1'b1: Assert 're' signal.

UART_DET

Address: **Operational Base** + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	de_inact_time This field controls the amount of time (in terms of number of pclk periods) between the finish flag after the sampling point of the stop bit on the sout to the falling edge of Driver output enable signal. Note that, the mentioned finish flag, i.e. the actual starting effective point of the count, is located at the position of (DLL+1) sclk periods before the full stop bit ends, followed by 3~4 synchronization pclk periods. The actual time is the programmed value + 1.

UART_TAT

Address: **Operational Base** + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	de2re_time Turn around time (in terms of pclk) for DE De-assertion to RE assertion. The actual time is the programmed value + 1.

UART_CPR

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Address: **Operational Base** + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x04	fifo_mode 8'h4 means FIFO mode is 64.
15:14	RO	0x0	reserved
13	RO	0x1	dma_extra 1'b1 means DMA_EXTRA enabled.
12	RO	0x1	uart_add_encoded_params 1'b1 means UART_ADD_ENCODED_PARAMS enabled.
11	RO	0x1	shadow 1'b1 means SHADOW mode enabled.
10	RO	0x1	fifo_stat 1'b1 means FIFO_STAT enabled.
9	RO	0x1	fifo_access 1'b1 means FIFO ACCESS enabled.
8	RO	0x1	new_feat 1'b1 means Additional features enabled.
7	RO	0x1	sir_lp_mode 1'b1 means SIR_LP mode enabled.
6	RO	0x1	sir_mode 1'b1 means SIR mode enabled.
5	RO	0x1	thre_mode 1'b1 means THRE mode enabled.
4	RO	0x1	afce_mode 1'b1 means AFCE mode enabled.
3:2	RO	0x0	reserved
1:0	RO	0x2	apb_data_width 2'b10 means APB data width is 32bit.

UART_UCV

Address: **Operational Base** + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:0	RO	0x3430322a	ver ASCII value for each number in the version.

UART_CTR

Address: **Operational Base** + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:0	RO	0x44570110	peripheral_id This register contains the peripherals identification code.

37.4.4 Internal Address Mapping

37.5 Interface Description

Table 37-1 UART0 Interface Description

Module Pin	Dir	Pad Name	IOMUX Setting
IOMUX0			
uart_rx	I	GPIO2_A0	GPIO2A_IOMUX_SEL_0[3:0]=4'h2
uart_tx	O	GPIO2_A1	GPIO2A_IOMUX_SEL_0[3:0]=4'h2

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IOMUX1			
uart_rx	I	GPIO5_D7	GPIO5D_IOMUX_SEL_1[15:12]=4'h1
uart_tx	O	GPIO5_D6	GPIO5D_IOMUX_SEL_1[11:8]=4'h1
IOMUX2			
uart_rx	I	GPIO0_B4	GPIO0B_IOMUX_SEL_1[3:0]=4'h1
uart_tx	O	GPIO0_B3	GPIO0B_IOMUX_SEL_1[15:12]=4'h1

Table 37-2 UART1 Interface Description

Module Pin	Dir	Pad Name	IOMUX Setting
IOMUX0			
uart_rx	I	GPIO0_C5	GPIO0C_IOMUX_SEL_1[7:4]=4'h3
uart_tx	O	GPIO0_C4	GPIO0C_IOMUX_SEL_1[3:0]=4'h3
uart_cts_n	I	GPIO0_C7	GPIO0C_IOMUX_SEL_1[15:12]=4'h3
uart_re	O		
uart_rts_n	O	GPIO0_C6	GPIO0C_IOMUX_SEL_1[11:8]=4'h3
uart_de	O		
IOMUX1			
uart_rx	I	GPIO3_B7	GPIO3B_IOMUX_SEL_1[15:12]=4'h4
uart_tx	O	GPIO3_B6	GPIO3B_IOMUX_SEL_1[11:8]=4'h4
uart_cts_n	I	GPIO3_B5	GPIO3B_IOMUX_SEL_1[7:4]=4'h4
uart_re	O		
uart_rts_n	O	GPIO3_B4	GPIO3B_IOMUX_SEL_1[3:0]=4'h4
uart_de	O		

Table 37-3 UART2 Interface Description

Module Pin	Dir	Pad Name	IOMUX Setting
IOMUX0			
uart_rx	I	GPIO3_B0	GPIO3B_IOMUX_SEL_0[3:0]=4'h4
uart_tx	O	GPIO3_B1	GPIO3B_IOMUX_SEL_0[7:4]=4'h4
uart_cts_n	I	GPIO3_A7	GPIO3A_IOMUX_SEL_1[15:12]=4'h4
uart_re	O		
uart_rts_n	O	GPIO3_A6	GPIO3A_IOMUX_SEL_1[11:8]=4'h4
uart_de	O		
IOMUX1			
uart_rx	I	GPIO7_B0	GPIO7B_IOMUX_SEL_0[3:0]=4'h6
uart_tx	O	GPIO7_B1	GPIO7B_IOMUX_SEL_0[7:4]=4'h6

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uart_cts_n	I	GPIO7_A4	GPIO7A_IOMUX_SEL_1[3:0]=4'h6
uart_re	O		
uart_rts_n	O	GPIO7_A7	GPIO7A_IOMUX_SEL_0[15:12]=4'h6
uart_de	O		

Table 37-4 UART3 Interface Description

Module Pin	Dir	Pad Name	IOMUX Setting
IOMUX0			
uart_rx	I	GPIO2_A2	GPIO2A_IOMUX_SEL_0[11:8]=4'h2
uart_tx	O	GPIO2_A3	GPIO2A_IOMUX_SEL_0[15:12]=4'h2
uart_cts_n	I	GPIO2_A5	GPIO2A_IOMUX_SEL_0[7:4]=4'h2
uart_re	O		
uart_rts_n	O	GPIO2_A4	GPIO2A_IOMUX_SEL_1[3:0]=4'h2
uart_de	O		
IOMUX1			
uart_rx	I	GPIO5_D5	GPIO5D_IOMUX_SEL_1[7:4]=4'h8
uart_tx	O	GPIO5_D4	GPIO5D_IOMUX_SEL_1[3:0]=4'h8
uart_cts_n	I	GPIO5_D3	GPIO5D_IOMUX_SEL_0[15:12]=4'h8
uart_re	O		
uart_rts_n	O	GPIO5_D2	GPIO5D_IOMUX_SEL_0[11:8]=4'h8
uart_de	O		
IOMUX2			
uart_rx	I	GPIO6_C3	GPIO6C_IOMUX_SEL_0[15:12]=4'h6
uart_tx	O	GPIO6_C2	GPIO6C_IOMUX_SEL_0[11:8]=4'h6
uart_cts_n	I	GPIO6_C1	GPIO6C_IOMUX_SEL_0[7:4]=4'h6
uart_re	O		
uart_rts_n	O	GPIO6_C0	GPIO6C_IOMUX_SEL_0[3:0]=4'h6
uart_de	O		

Table 37-5 UART4 Interface Description

Module Pin	Dir	Pad Name	IOMUX Setting
IOMUX0			

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uart_rx	I	GPIO4_A2	GPIO4A_IOMUX_SEL_0[11:8]=4'h5
uart_tx	O	GPIO4_A3	GPIO4A_IOMUX_SEL_0[15:12]=4'h5
uart_cts_n	I	GPIO4_A1	GPIO4A_IOMUX_SEL_0[7:4]=4'h5
uart_re	O		
uart_rts_n	O	GPIO4_A0	GPIO4A_IOMUX_SEL_0[3:0]=4'h5
uart_de	O		
IOMUX1			
uart_rx	I	GPIO5_A3	GPIO5A_IOMUX_SEL_0[15:12]=4'h8
uart_tx	O	GPIO5_A2	GPIO5A_IOMUX_SEL_0[11:8]=4'h8
uart_cts_n	I	GPIO5_A1	GPIO5A_IOMUX_SEL_0[7:4]=4'h8
uart_re	O		
uart_rts_n	O	GPIO5_A0	GPIO5A_IOMUX_SEL_0[3:0]=4'h8
uart_de	O		
IOMUX2			
uart_rx	I	GPIO6_A1	GPIO6A_IOMUX_SEL_0[7:4]=4'h6
uart_tx	O	GPIO6_A0	GPIO6A_IOMUX_SEL_0[3:0]=4'h6
uart_cts_n	I	GPIO6_A7	GPIO6A_IOMUX_SEL_1[15:12]=4'h6
uart_re	O		
uart_rts_n	O	GPIO6_A6	GPIO6A_IOMUX_SEL_1[11:8]=4'h6
uart_de	O		
IOMUX3			
uart_rx	I	GPIO2_A4	GPIO2A_IOMUX_SEL_1[3:0]=4'h3
uart_tx	O	GPIO2_A5	GPIO2A_IOMUX_SEL_1[7:4]=4'h3
uart_cts_n	I	GPIO2_A3	GPIO2A_IOMUX_SEL_0[15:12]=4'h3
uart_re	O		
uart_rts_n	O	GPIO2_A2	GPIO2A_IOMUX_SEL_0[11:8]=4'h3
uart_de	O		

Table 37-6 UART5 Interface Description

Module Pin	Dir	Pad Name	IOMUX Setting
IOMUX0			

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uart_rx	I	GPIO4_A7	GPIO4A_IOMUX_SEL_1[15:12]=4'h5
uart_tx	O	GPIO4_A6	GPIO4A_IOMUX_SEL_1[11:8]=4'h5
uart_cts_n	I	GPIO4_B1	GPIO4B_IOMUX_SEL_0[7:4]=4'h5
uart_re	O		
uart_rts_n	O	GPIO4_B0	GPIO4B_IOMUX_SEL_0[3:0]=4'h5
uart_de	O		
IOMUX1			
uart_rx	I	GPIO5_A5	GPIO5A_IOMUX_SEL_1[7:4]=4'h8
uart_tx	O	GPIO5_A4	GPIO5A_IOMUX_SEL_1[3:0]=4'h8
uart_cts_n	I	GPIO5_A7	GPIO5A_IOMUX_SEL_1[15:12]=4'h8
uart_re	O		
uart_rts_n	O	GPIO5_A6	GPIO5A_IOMUX_SEL_1[11:8]=4'h8
uart_de	O		
IOMUX2			
uart_rx	I	GPIO6_A3	GPIO6A_IOMUX_SEL_0[15:12]=4'h6
uart_tx	O	GPIO6_A2	GPIO6A_IOMUX_SEL_0[11:8]=4'h6
uart_cts_n	I	GPIO6_A5	GPIO6A_IOMUX_SEL_1[7:4]=4'h6
uart_re	O		
uart_rts_n	O	GPIO6_A4	GPIO6A_IOMUX_SEL_1[3:0]=4'h6
uart_de	O		

Table 37-7 UART6 Interface Description

Module Pin	Dir	Pad Name	IOMUX Setting
IOMUX0			
uart_rx	I	GPIO5_B1	GPIO5B_IOMUX_SEL_0[7:4]=4'h8
uart_tx	O	GPIO5_B0	GPIO5B_IOMUX_SEL_0[3:0]=4'h8
uart_cts_n	I	GPIO5_B3	GPIO5B_IOMUX_SEL_0[15:12]=4'h8
uart_re	O		
uart_rts_n	O	GPIO5_B2	GPIO5B_IOMUX_SEL_0[11:8]=4'h8
uart_de	O		
IOMUX1			

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uart_rx	I	GPIO6_B1	GPIO6B_IOMUX_SEL_0[7:4]=4'h6
uart_tx	O	GPIO6_B0	GPIO6B_IOMUX_SEL_0[3:0]=4'h6
uart_cts_n	I	GPIO6_B3	GPIO6B_IOMUX_SEL_0[15:12]=4'h6
uart_re	O		
uart_rts_n	O	GPIO6_B2	GPIO6B_IOMUX_SEL_0[11:8]=4'h6
uart_de	O		

Table 37-8 UART7 Interface Description

Module Pin	Dir	Pad Name	IOMUX Setting
IOMUX0			
uart_rx	I	GPIO5_B5	GPIO5B_IOMUX_SEL_1[7:4]=4'h8
uart_tx	O	GPIO5_B4	GPIO5B_IOMUX_SEL_1[3:0]=4'h8
uart_cts_n	I	GPIO5_B7	GPIO5B_IOMUX_SEL_1[15:12]=4'h8
uart_re	O		
uart_rts_n	O	GPIO5_B6	GPIO5B_IOMUX_SEL_1[11:8]=4'h8
uart_de	O		
IOMUX1			
uart_rx	I	GPIO6_B5	GPIO6B_IOMUX_SEL_1[7:4]=4'h6
uart_tx	O	GPIO6_B4	GPIO6B_IOMUX_SEL_1[3:0]=4'h6
uart_cts_n	I	GPIO6_B7	GPIO6B_IOMUX_SEL_1[15:12]=4'h6
uart_re	O		
uart_rts_n	O	GPIO6_B6	GPIO6B_IOMUX_SEL_1[11:8]=4'h6
uart_de	O		

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37.6 Application Notes

37.6.1 No FIFO Mode Transfer Flow

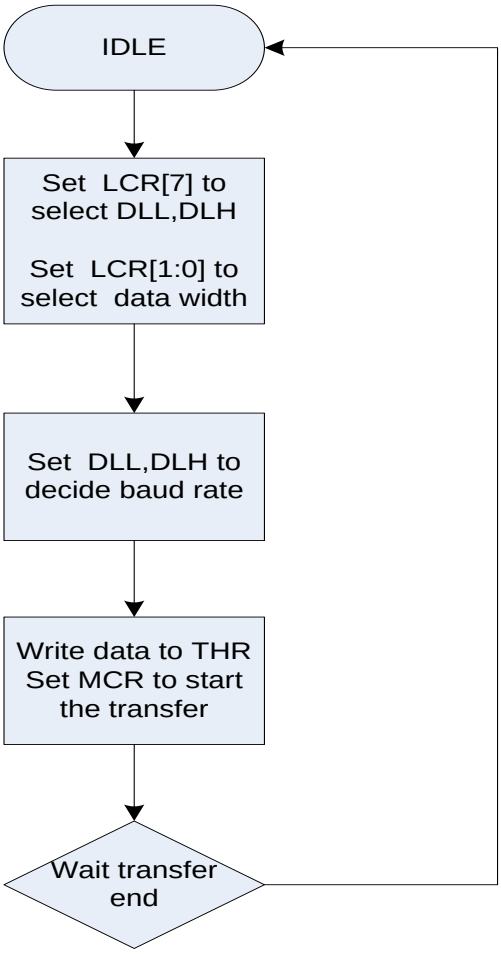

Fig. 37-7 UART None FIFO mode

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37.6.2 FIFO Mode Transfer Flow

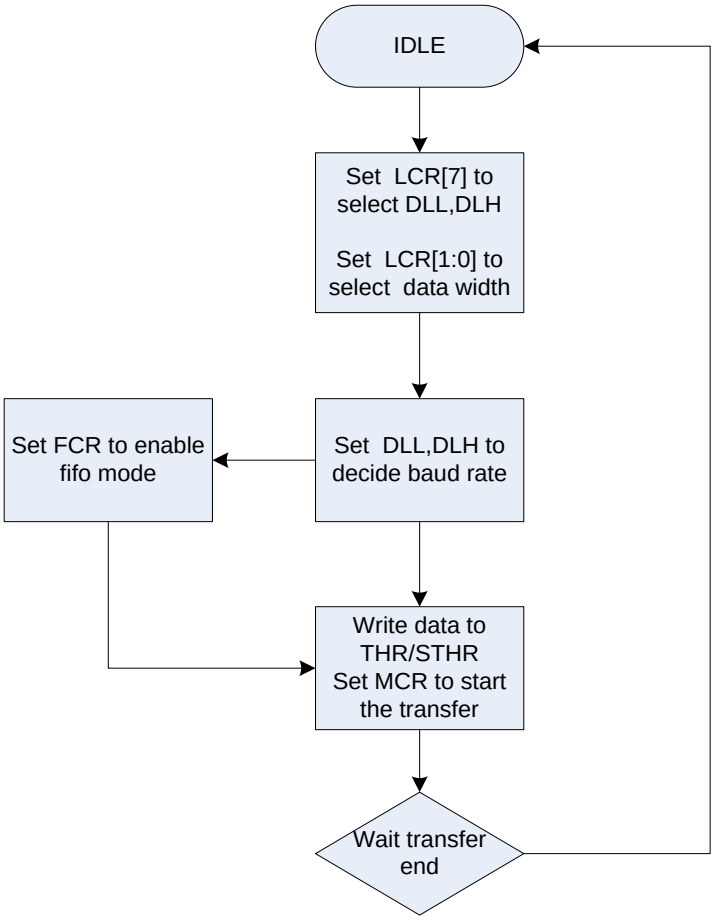

Fig. 37-8 UART FIFO mode

The UART is an APB slave performing:
Serial-to-parallel conversion on data received from a peripheral device. Parallel-to-serial conversion on data transmitted to the peripheral device. The CPU reads and writes data and control/status information through the APB interface. The transmitting and receiving paths are buffered with internal FIFO memories enabling up to 64-bytes to be stored independently in both transmit and receive modes. A baud rate generator can generate a common transmit and receive internal clock input. The baud rates will depend on the internal clock frequency. The UART will also provide transmit, receive and exception interrupts to system. A DMA interface is implemented for improving the system performance.

37.6.3 Baud Rate Calculation

UART clock generation

UARTs source clocks (SCLK) can be selected from different PLL outputs, or from XIN24M. SCLK can be divided to different frequency, please refer to CRU chapter.

UART baud rate configuration

The following table provides some reference configuration for different UART baud rates.

Table 37-9 UART Baud Rate Configuration

Baud Rate	Reference Configuration
115.2 Kbps	Configure PLL to get 1.188GHz clock output; Divide 1.188GHz clock by 16 to get 74.25MHz clock; Divide 74.25MHz clock by 32/20625 to get 115.2KHz clock;
460.8 Kbps	Configure PLL to get 1.188GHz clock output; Divide 1.188GHz clock by 16 to get 74.25MHz clock; Divide 74.25MHz clock by 128/20625 to get 460.8KHz clock;
921.6 Kbps	Configure PLL to get 1.188GHz clock output; Divide 1.188GHz clock by

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	16 to get 74.25MHz clock; Divide 74.25MHz clock by 256/20625 to get 921.6KHz clock;
1.5 Mbps	Choose default 24M clock; Divide 24M clock by 16 to get 1.5MHz clock;
3 Mbps	Configure PLL to get 1.188GHz clock output; Divide 1.188GHz clock by 16 to get 74.25MHz clock; Divide 74.25MHz clock by 4/99 to get 3MHz clock;
4 Mbps	Configure PLL to get 1.188GHz clock output; Divide 1.188GHz clock by 16 to get 74.25MHz clock; Divide 74.25MHz clock by 16/297 to get 4MHz clock;

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Chapter 38 Pulse Width Modulation (PWM)

38.1 Overview

The Pulse-Width Modulator (PWM) provides a way to generate a pulse periodic waveform for motor control, it can also act as a digital-to-analog converter with some external components.

The PWM Module supports the following common features:

- Support input capture mode
  - Support measures the high/low polarity effective cycles of input waveform
  - Support generates an interrupt at the transition of input waveform polarity
  - Support a 32-bits high polarity capture counter
  - Support a 32-bits low polarity capture counter
  - Support an input filter to remove glitch
- Support continuous mode and one-shot output mode
  - Support a 32-bits period counter
  - Support a 32-bits duty counter
  - Support configures the polarity in inactive state and duty cycle
  - Support center or left aligned mode
  - Support a 16-bit first dimensional repeat counter and an interrupt for reload operation
  - Support a 16-bit second dimensional repeat counter and an interrupt for one-shot operation
  - Support global synchronization of various channels
- Supports two-stage frequency division of working clock

RV1126B support 4 PWM controllers, they support some individual feature as following:

- PWM0
  - Support 8 channels
  - Support biphasic counter
- PWM1
  - Support 4 channels
  - Support power key capture mode
  - Support clock frequency meter
  - Support clock counter
- PWM2
  - Support 8 channels
  - Support biphasic counter
  - Support generates waveform through lookup table
- PWM3
  - Support 8 channels
  - Support biphasic counter

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38.2 Block Diagram

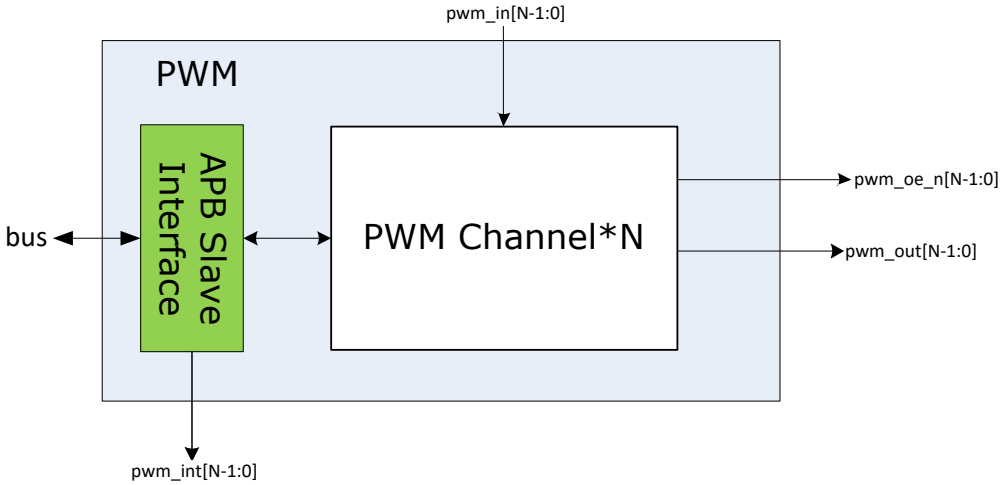

Fig. 38-1 PWM Block Diagram

The host processor gets access to PWM register through the APB slave interface with 32-bit bus width. PWM controller support 1~8 channels, and the offset address of each channel is 4k-byte as interval. PWM supports one interrupt for each channel, user shouldrefer to interrupt register to know the raw interrupt status when an interrupt is asserted.

38.3 Function Description

The PWM supports three operation modes: capture mode, one-shot mode and continuous mode. For the one-shot mode and the continuous mode, the PWM output can be configured as the left-aligned mode or the center-aligned mode.

PWM also supports some additional function, such as clock counter, clock frequency meter and biphasic Counter.

38.3.1 Capture mode

The capture mode is used to measure the PWM channel input waveform high/low effective cycles with the PWM channel clock and asserts an interrupt when the polarity of the input waveform changes. The number of the high effective cycles is recorded in the PWM_HPC register, while the number of the low effective cycles is recorded in the PWM_LPC register.

Notes: the PWM input waveform is doubled buffered when the PWM channel is working in order to filter unexpected shot-time polarity transition, and therefore the interrupt is asserted several cycles after the input waveform polarity changes, and so does the change of the values of PWM_HPC and PWM_LPC.

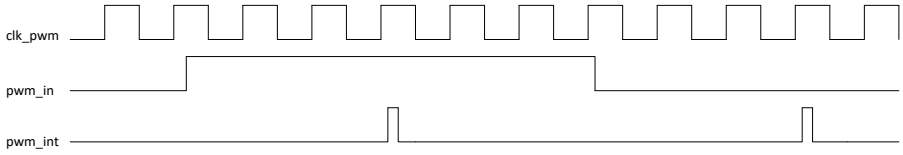

Fig. 38-2 PWMCapture Mode

The PWM support 32-bits power key capture mode. User can configure 16 power keys to match, the interrupt will be asserted when the capture value matches any one.

38.3.2 Continuous mode

In continuous mode, the PWM channel generates a series of the pulses continuously as expected once the channel is enabled. It supports left-aligned mode or center-aligned mode.

For the left-aligned output mode, the PWM channel firstly starts the duty cycle with the configured duty polarity (PWM_CTRL.duty_pol). Once duty cycle number (PWM_DUTY) is reached, the output is switched to the opposite polarity. After the period number (PWM_PERIOD) is reached, the output is again switched to the opposite polarity to start another period of desired pulse.

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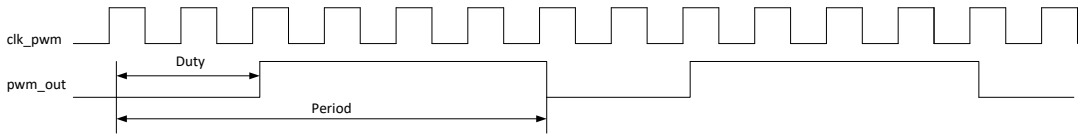

Fig. 38-3 PWM Continuous Left-aligned Output Mode

For the center-aligned output mode, the PWM channel firstly starts the duty cycle with the configured duty polarity (PWM_CTRL.duty_pol). Once one half of duty cycle number (PWM_DUTY) is reached, the output is switched to the opposite polarity. Then if there is one half of duty cycle left for the whole period, the output is again switched to the opposite polarity. Finally, after the period number (PWM_PERIOD) is reached, the output starts another period of desired pulse.

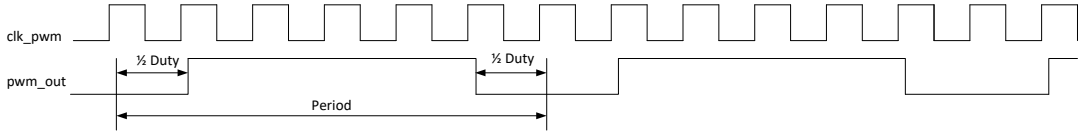

Fig. 38-4 PWM Continuous Center-aligned Output Mode

PWM support a 16 bits first dimensional repeat counter. An reload interrupt is generated every N+1 periods of the waveform when PWM_RPT.rpt_first_dimensional is configured to N. User can update the duty and period configuration for next N+1 periods when receive the interrupt.

Continuous mode will generate the waveform continuously until disabled by user. It's will fix to inactive polarity (PWM_CTRL.inactive_pol) when it's disabled.

38.3.3 One-shot mode

In one-shot mode, the PWM channel generates limited periods of waveforms.

In addition to the first dimensional repeat counter, it also supports a 16 bits second dimensional repeat counter.PWM channel will stop and assert an interrupt after second dimensional counter reach M+1 when PWM_RPT.rpt_second_dimensional is configured to M. The total waveform periods are (N + 1) multi by (M + 1).

The reload interrupt and lookup table is also supported in one-shot mode.

The left-aligned and the center-aligned is also supported in one-shot mode.

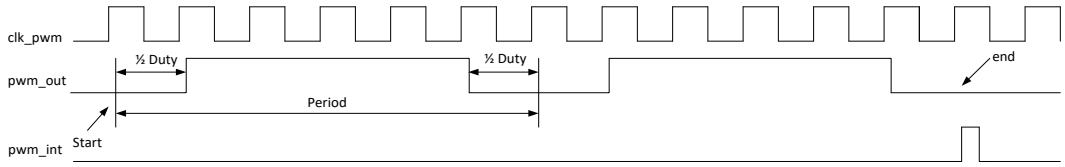

Fig. 38-5 PWM One-shot Center-aligned Output Mode

38.3.4 Generates Waveform Through Lookup Table

PWM1 support generates waveform through lookup table. The depth of the lookup table is 512 and the bit width is 8. The duty and period can be updated by lookup table automatic as needed.

38.3.5 Clock Counter

PWM support a 64-bits counter which clock can select from any PWM channel input and a clock from system CRU.

38.3.6 Clock frequency meter

PWM support a 32-bits frequency meter which clock can select from any PWM channel input and a clock from system CRU. It supports a reference clock and timer to schedule a period time, user can calculate the frequency by gets the counter value that counted by the measured clock in the period time.

38.3.7 Biphasic Counter

PWM0/2/3 support biphasic counter which uses two channels to compose an A/B phase channel. The biphasic counter register is only located at A channel, User only needs to configure the IOMUX of B channel.

PWM0/2/3 controller support 4 biphasic counters: Channel 0 and Channel 4 compose an A/B phase bidirectional counter. Channel 1 and Channel 5 compose an A/B phase bidirectional counter. Channel 2 and Channel 6 compose an A/B phase bidirectional

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counter. Channel 3 and Channel 7 compose an A/B phase bidirectional counter.
Biphasic counter support 5 mode as following:

- Mode 0: Single phase increase mode with A-phase.

When A-phase input is OFF->ON, the count increases by 1.In this mode, it can be used as clock frequency meter or clock counter.

- Mode 1: Single phase increase/decrease mode with A-phase.

When the B-phase input is OFF and the A-phase input is OFF->ON, the count increases by 1.
When the B-phase input is ON and the A-phase input is OFF->ON, the count decreases by 1

- Mode 2: Dual phase with A/B-phase mode.

When the A-phase input is ON and the B-phase input is OFF->ON, the count increases by 1.
When the A-phase input is ON and the B-phase input is ON->OFF, the count decreases by 1

- Mode 3: Dual phase with A/B-phase 2 times frequency mode.

When the A-phase input is ON and the B-phase input is OFF->ON, the count increases by 1;
When the A-phase input is OFF and the B-phase input is ON->OFF, the count increases by 1.
When the A-phase input is ON and the B-phase input is ON->OFF, the count decreases by 1;
When the A-phase input is OFF and the B-phase input is OFF ->ON, the count decreases by 1.

- Mode 4: Dual phase with A/B-phase 4 times frequency mode.

When the input of phase B is OFF and phase A is OFF->ON, the count increases by 1.
When the A-phase input is ON and the B-phase input is OFF->ON, the count increases by 1.
When the input of phase B is ON and phase A is ON->OFF, the count increases by 1.
When the A-phase input is OFF and the B-phase input is ON_.OFF, the count increases by 1.
When the A-phase input is OFF and the B-phase input is OFF->ON, the count decreases by 1.
When the input of phase B is ON and phase A is OFF->ON, the count decreases by 1.
When the A-phase input is ON and the B-phase input is ON->OFF, the count decreases by 1.
When the input of phase B is OFF and the input of phase A is ON->OFF, the count decreases by 1.

38.4 Register Description

38.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
PWM0	0x20E00000
PWM1	0x20700000
PWM2	0x20F00000
PWM3	0x21000000

Slave address can be divided into different length for different channels in one controller, which is shown as follows.

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Table 38-1 PWM Channel Address Map

Channel	Offset Address
Channel 0	0x00000
Channel 1	0x10000
Channel 2	0x20000
Channel 3	0x30000
Channel 4	0x40000
Channel 5	0x50000
Channel 6	0x60000
Channel 7	0x70000

38.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
PWM_VERSION_ID	0x0000	W	0x0401398F	Version ID Register
PWM_ENABLE	0x0004	W	0x00000000	Enable Register
PWM_CLK_CTRL	0x0008	W	0x00000000	Clock Control Register
PWM_CTRL	0x000C	W	0x00000000	Control Register
PWM_PERIOD	0x0010	W	0x00000000	Period Register
PWM_DUTY	0x0014	W	0x00000000	Duty Register
PWM_OFFSET	0x0018	W	0x00000000	Output Offset Register
PWM_RPT	0x001C	W	0x00000000	Repeat Register
PWM_FILTER_CTRL	0x0020	W	0x00000000	Filter Control Register
PWM_CNT	0x0024	W	0x00000000	Counter Register
PWM_ENABLE_DELAY	0x0028	W	0x00000000	Enable Delay Register
PWM_HPC	0x002C	W	0x00000000	High Polarity Capture Register

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Name	Offset	Size	Reset Value	Description
PWM_LPC	0x0030	W	0x00000000	Low Polarity Capture Register
PWM_BIPHASIC_COUNTER_CTRL0	0x0040	W	0x00000000	Biphasic counter control 0 register
PWM_BIPHASIC_COUNTER_CTRL1	0x0044	W	0x00000000	Biphasic counter control 1 register
PWM_BIPHASIC_COUNTER_TIMER_VALUE	0x0048	W	0x00000000	Biphasic counter timer value register
PWM_BIPHASIC_COUNTER_RESULT_VALUE	0x004C	W	0x00000000	Biphasic counter result value register
PWM_BIPHASIC_COUNTER_RESULT_VALUE_SYNC	0x0050	W	0x00000000	Biphasic counter result value register
PWM_INTSTS	0x0070	W	0x00000000	Interrupt Status Register
PWM_INT_EN	0x0074	W	0x00000000	Interrupt Enable Register
PWM_INT_MASK	0x0078	W	0x00000000	Interrupt Mask Register
PWM_FEATURE	0x007C	W	0x00000044	Feature Register
PWM_WAVE_MEM_ARBITER	0x0080	W	0x00000000	Waveform Generator Memory Arbiter Register
PWM_WAVE_MEM_STATUS	0x0084	W	0x00000000	Waveform Generator Memory Status Register

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Name	Offset	Size	Reset Value	Description
PWM_WAVE_CTRL	0x0088	W	0x00000010	Waveform Generator control register
PWM_WAVE_MAX	0x008C	W	0x00000000	Waveform Generator maximum register
PWM_WAVE_MIN	0x0090	W	0x00000000	Waveform Generator minimum register
PWM_WAVE_OFFSET	0x0094	W	0x00000000	Waveform Generator offset register
PWM_WAVE_MIDDLE	0x0098	W	0x00000000	Waveform Generator middle register
PWM_WAVE_HOLD	0x009C	W	0x00000000	Waveform Generator hold register
PWM_GLOBAL_ARBITER	0x00C0	W	0x00000000	Global Arbiter Register
PWM_GLOBAL_CTRL	0x00C4	W	0x00000000	Global Control Register
PWM_PWRMATCH_ARBITER	0x0100	W	0x00000000	Power Key Match Arbiter Register
PWM_PWRMATCH_CTRL	0x0104	W	0x00000000	Power Key Match Control Register
PWM_PWRMATCH_LPRE	0x0108	W	0x238C22C4	Power Key Match of Low Preload Register

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Name	Offset	Size	Reset Value	Description
PWM_PWRMATCH_HPRE	0x010C	W	0x11F81130	Power Key Match of High Preload Register
PWM_PWRMATCH_LD	0x0110	W	0x029401CC	Power Key Match of Low Data Register
PWM_PWRMATCH_HD_ZERO	0x0114	W	0x029401CC	Power Key Match of High Data for Zero Register
PWM_PWRMATCH_HD_ONE	0x0118	W	0x06FE0636	Power Key Match of High Data for One Register
PWM_PWRMATCH_VALUE0	0x011C	W	0x00000000	Power Key Match Value 0 Register
PWM_PWRMATCH_VALUE1	0x0120	W	0x00000000	Power Key Match Value 1 Register
PWM_PWRMATCH_VALUE2	0x0124	W	0x00000000	Power Key Match Value 2 Register
PWM_PWRMATCH_VALUE3	0x0128	W	0x00000000	Power Key Match Value 3 Register
PWM_PWRMATCH_VALUE4	0x012C	W	0x00000000	Power Key Match Value 4 Register
PWM_PWRMATCH_VALUE5	0x0130	W	0x00000000	Power Key Match Value 5 Register
PWM_PWRMATCH_VALUE6	0x0134	W	0x00000000	Power Key Match Value 6 Register
PWM_PWRMATCH_VALUE7	0x0138	W	0x00000000	Power Key Match Value 7 Register

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Name	Offset	Size	Reset Value	Description
PWM_PWRMATCH_VALUE8	0x013C	W	0x00000000	Power Key Match Value 8 Register
PWM_PWRMATCH_VALUE9	0x0140	W	0x00000000	Power Key Match Value 9 Register
PWM_PWRMATCH_VALUE10	0x0144	W	0x00000000	Power Key Match Value 10 Register
PWM_PWRMATCH_VALUE11	0x0148	W	0x00000000	Power Key Match Value 11 Register
PWM_PWRMATCH_VALUE12	0x014C	W	0x00000000	Power Key Match Value 12 Register
PWM_PWRMATCH_VALUE13	0x0150	W	0x00000000	Power Key Match Value 13 Register
PWM_PWRMATCH_VALUE14	0x0154	W	0x00000000	Power Key Match Value 14 Register
PWM_PWRMATCH_VALUE15	0x0158	W	0x00000000	Power Key Match Value 15 Register
PWM_PWRCAPTURE_VALUE	0x015C	W	0x00000000	Power Key Capture Value Register
PWM_IR_TRANS_ARBITER	0x0180	W	0x00000000	Power Key Match Control Register
PWM_IR_TRANS_CTRL0	0x0184	W	0x00001F00	IR Transmission control 0 register
PWM_IR_TRANS_CTRL1	0x0188	W	0x00000000	IR Transmission control 1 register
PWM_IR_TRANS_PRE	0x018C	W	0x11942328	IR transmission preload period

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Name	Offset	Size	Reset Value	Description
PWM_IR_TRANS_SPRE	0x0190	W	0x000008CA	IR transmission simple preload low period
PWM_IR_TRANS_LD	0x0194	W	0x00000230	IR Trans Out Data Low Period
PWM_IR_TRANS_HD	0x0198	W	0x069A0230	IR Trans Out High Period
PWM_IR_TRANS_BURST_FRAME	0x019C	W	0x2261A5E0	IR transmission frame and burst period
PWM_IR_TRANS_DATA_VALUE	0x01A0	W	0x00000000	IR Trans Output Data Value
PWM_IR_TRANS_STATUS	0x01A4	W	0x00000001	IR Trans Status
PWM_FREQ_ARBITER	0x01C0	W	0x00000000	Frequency Meter Arbiter Control Register
PWM_FREQ_CTRL	0x01C4	W	0x00000000	Frequency Meter control register
PWM_FREQ_TIMER_VALUE	0x01C8	W	0x00000000	Frequency Meter timer value register
PWM_FREQ_RESULT_VALUE	0x01CC	W	0x00000000	Frequency Meter result value register
PWM_FREQ_RESULT_VALUE_RAW	0x01D0	W	0x00000000	Frequency Meter result raw value register

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Name	Offset	Size	Reset Value	Description
PWM_COUNTER_ARBITER	0x0200	W	0x00000000	Counter Arbiter Control Register
PWM_COUNTER_CTRL	0x0204	W	0x00000000	Counter control register
PWM_COUNTER_LOW	0x0208	W	0x00000000	Counter Low register
PWM_COUNTER_HIGH	0x020C	W	0x00000000	Counter High register
PWM_WAVE_MEM	0x0400	W	0x00000000	Waveform Generator Memory Address Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

38.4.3 Detail Registers Description

PWM_VERSION_ID

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:24	RO	0x04	main_version Main version
23:16	RO	0x01	minor_version Minor version
15:0	RO	0x398f	svn_version SVN version

PWM_ENABLE

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:6	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
5	RW	0x0	pwm_cnt_rd_en PWM channel CNT read enable. The CNT can be read for debug. 1'b0: Disabled 1'b1: Enabled
4	W1T	0x0	pwm_global_join_en PWM join global control enable. When this bit is set to 1, the PWM channel is enabled by pwm_global_en instead of pwm_en, and the following register can be updated at the posedge of pwm_global_ctrl_update_en: PWM_CTRL, PWM_PERIOD, PWM_DUTY, PWM_OFFSET
3	RW	0x0	force_clk_en 1'b0: Disabled, when PWM channel is inactive state, the clk_pwm to PWM Clock pre-scale module is blocked to reduce power consumption. 1'b1: Enabled, the clk_pwm to PWM Clock pre-scale module is always enabled.
2	W1T	0x0	pwm_ctrl_update_en PWM control update enable. The bit will be auto cleaned. The following register can be updated at the posedge of pwm_ctrl_update_en: PWM_CTRL, PWM_PERIOD, PWM_DUTY, PWM_OFFSET
1	RW	0x0	pwm_en PWM enable 1'b0: Disabled 1'b1: Enabled If the PWM is worked in the one-shot mode, this bit will be cleared at the end of operation.
0	RW	0x0	pwm_clk_en PWM clock enable 1'b0: Disabled 1'b1: Enabled If the PWM is worked in the one-shot mode, this bit will be cleared at the end of operation.

PWM_CLK_CTRL

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15	RW	0x0	clk_global_sel Clock global selection 1'b0: Select current channel scale clock 1'b1: Select global channel scale clock
14:13	RW	0x0	clk_src_sel Clock source selection 2'b00: Select clk_pwm as root clock source, Clock is from PLL and the frequency can be configured. 2'b01: Select clk_pwm_osc as root clock source, Clock is from crystal oscillator and the frequency is fixed. 2'b10: Select clk_pwm_rc as root clock source, Clock is from RC oscillator and the frequency is fixed.
12:4	RW	0x000	scale This field defines the scale factor applied to pre-scaled clock. The value N means the clock is divided by 2*N. it is valid from 1~256.
3	RO	0x0	reserved
2:0	RW	0x0	prescale This field defines the pre-scale factor applied to input clock. The value N means that the input clock is divided by 2^N.

PWM_CTRL

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8:6	RW	0x0	pwm_in_sel PWM in channel selection, the default value is corresponding channel, User can configure to another channel. 3'b000: PWM channel 0 3'b001: PWM channel 1 3'b010: PWM channel 2 3'b011: PWM channel 3 3'b100: PWM channel 4 3'b101: PWM channel 5 3'b110: PWM channel 6 3'b111: PWM channel 7
5	RW	0x0	aligned_vld_n 0: Aligned Mode Valid 1: Aligned Mode Invalid

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Bit	Attr	Reset Value	Description
4	RW	0x0	output_mode 1'b0: Left aligned mode 1'b1: Center aligned mode
3	RW	0x0	inactive_pol This defines the output waveform polarity when PWM channel is in inactive state. The inactive state means that PWM finishes the complete waveform in one-shot mode or PWM channel is disabled. 1'b0: Negative 1'b1: Positive
2	RW	0x0	duty_pol This defines the polarity for duty cycle. PWM starts the output waveform with duty cycle. 1'b0: Negative 1'b1: Positive
1:0	RW	0x0	pwm_mode 2'b00: One shot mode, PWM produces the waveform within the repeated times defined by PWMx_CTRL_rpt. 2'b01: Continuous mode, PWM produces the waveform continuously. 2'b10: Capture mode, PWM measures the cycles of high/low polarity of input waveform. 2'b11: Reserved

PWM_PERIOD

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PERIOD This value defines the period of the output waveform for continuous mode or one-shot mode. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the bit [31:1] is considered and bit [0] always considered as 0.

PWM_DUTY

Address: **Operational Base** + offset (0x0014)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DUTY This value defines the duty cycle of the output waveform for continuous mode or one-shot mode. The PWM starts the output waveform with duty cycle. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the [31:1] is considered.

PWM_OFFSET

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	channel_output_offset If PWM is operated at the continuous mode or one-shot mode, this value defines the offset of the output waveform. This value is based on the PWM clock. The value ranges from 0 to (period-duty). This register takes effective when output aligned mode is invalid.

PWM_RPT

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	rpt_second_dimensional This field defines the second dimensional repeated effective periods of output waveform. It can be used only in one-shot mode. The second dimensional waveform counter will increase 1 when first dimensional waveform counter reach rpt_first_dimensional. When reach rpt_second_dimensional, the PWM channel will be disabled and the one-shot interrupt will be asserted. The value N means N+1 repeated effective periods. The total waveform number will be (rpt_first_dimensional+1) multiply by (rpt_second_dimensional+1).
15:0	RW	0x0000	rpt_first_dimensional This field defines the first dimensional repeated effective periods of output waveform. When reach rpt_first_dimensional, the waveform counter will wrap back to 0 and restart counting and the reload interrupt will be asserted. User can update the configuration in the interrupt. It can be used in one-shot mode and Continuous mode. The value N means N+1 repeated effective periods.

PWM_FILTER_CTRL

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Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9:4	RW	0x00	filter_number Filter window number
3:1	RO	0x0	reserved
0	RW	0x0	filter_enable 1'b0: Disabled 1'b1: Enabled

PWM_CNT

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CNT The 32-bit indicates current value of PWM Channel 0 counter. The counter runs at the rate of PWM clock. The value ranges from 0 to (2^32-1).

PWM_ENABLE_DELAY

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	pwm_enable_delay PWM enable delay

PWM_HPC

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HPC This value indicates the effective high polarity cycles of input waveform for capture mode. This value is based on the PWM clock. The value ranges from 0 to (2^32-1).

PWM_LPC

Address: **Operational Base** + offset (0x0030)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	LPC This value indicates the effective low polarity cycles of input waveform for capture mode. This value is based on the PWM clock. The value ranges from 0 to (2^32-1).

PWM_BIPHASIC_COUNTER_CTRL0

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	biphasic_counter_mode0_edge_sel biphasic counter phase edge selection for mode 0 1'b0: Posedge 1'b1: Negedge
8	RW	0x0	biphasic_counter_clk_force_en Biphasic counter clock force enable
7	W1T	0x0	biphasic_counter_sync_en Biphasic counter synchronous enable
6	W1T	0x0	timer_clk_switch_mode Timer clock switch mode, it can set to 1'b1 only when biphasic_counter_mode is mode0. 1'b0: Normal mode 1'b1: Switch timer clock and measured clock. It can be used to provide testing accuracy or reduce testing time when the frequency of measured clock is low. It can also be used in scenarios where the start time of the measured clock is uncertain
5:3	RW	0x0	biphasic_counter_mode Biphasic counter mode 3'h0: Mode0 3'h1: Mode1 3'h2: Mode2 3'h3: Mode3 3'h4: Mode4 Other: Reserved

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Bit	Attr	Reset Value	Description
2	RW	0x0	biphasic_counter_clk_sel Biphasic counter clock selection 1'b0: Select clk_pwm, clock is from PLL and the frequency can be configured. 1'b1: Select clk_pwm_osc, clock is from crystal oscillator and the frequency is fixed.
1	RW	0x0	biphasic_counter_continuous_mode Biphasic counter continuous mode
0	W1T	0x0	biphasic_counter_en Biphasic counter enable.

PWM_BIPHASIC_COUNTER_CTRL1

Address: **Operational Base** + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RO	0x00	reserved
10:4	RW	0x00	biphasic_counter_filter_number Filter window number
3:1	RO	0x0	reserved
0	RW	0x0	biphasic_counter_filter_enable 1'b0: Disabled 1'b1: Enabled

PWM_BIPHASIC_COUNTER_TIMER_VALUE

Address: **Operational Base** + offset (0x0048)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	biphasic_counter_timer_value Biphasic counter timer value, the unit is one cycle of biphasic counter timer clock.

PWM_BIPHASIC_COUNTER_RESULT_VALUE

Address: **Operational Base** + offset (0x004C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	biphasic_counte_result_value Biphasic counter result value, it can read only after interrupt biphasic_counter_IntSts is asserted.

PWM_BIPHASIC_COUNTER_RESULT_VALUE_SYNC

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Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	biphasic_counte_result_value_sync Biphasic counter result value with synchronized processing, it can read in real time when biphasic_counter_sync_en is set to 1.

PWM_INTSTS

Address: **Operational Base** + offset (0x0070)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	W1C	0x0	wave_middle_intsts Waveform address access middle address value interrupt status 1'b0: Interrupt not generated 1'b1: Interrupt generated
7	W1C	0x0	wave_max_intsts Waveform address access maximum address interrupt status 1'b0: Interrupt not generated 1'b1: Interrupt generated
6	W1C	0x0	it_trans_end_intsts IR Transmission end interrupt status 1'b0: Interrupt not generated 1'b1: Interrupt generated
5	W1C	0x0	pwr_intsts Power key match interrupt status 1'b0: Interrupt not generated 1'b1: Interrupt generated
4	W1C	0x0	freq_intsts Frequency meter interrupt status 1'b0: Interrupt not generated 1'b1: Interrupt generated
3	W1C	0x0	reload_intsts Reload interrupt status 1'b0: Interrupt not generated 1'b1: Interrupt generated
2	W1C	0x0	oneshot_end_intsts Waveform end interrupt status for one-shot mode. 1'b0: Interrupt not generated 1'b1: Interrupt generated
1	W1C	0x0	cap_hpc_intsts HPC interrupt status for capture mode. 1'b0: Interrupt not generated 1'b1: Interrupt generated

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Bit	Attr	Reset Value	Description
0	W1C	0x0	cap_lpc_intsts LPC interrupt status for capture mode. 1'b0: Interrupt not generated 1'b1: Interrupt generated

PWM_INT_EN

Address: **Operational Base** + offset (0x0074)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	wave_middle_int_en Waveform address access middle address enable 1'b0: Interrupt disabled 1'b1: Interrupt enabled
7	RW	0x0	wave_max_int_en Waveform address access maximum address interrupt enable 1'b0: Interrupt disabled 1'b1: Interrupt enabled
6	RW	0x0	it_trans_end_int_en IR Transmission end interrupt enable 1'b0: Interrupt disabled 1'b1: Interrupt enabled
5	RW	0x0	pwr_int_en Power key match interrupt enable 1'b0: Interrupt disabled 1'b1: Interrupt enabled
4	RW	0x0	freq_int_en Frequency meter interrupt enable 1'b0: Interrupt disabled 1'b1: Interrupt enabled
3	RW	0x0	reload_int_en Reload interrupt enable 1'b0: Interrupt disabled 1'b1: Interrupt enabled
2	RW	0x0	oneshot_end_int_en Waveform end interrupt enable for one-shot mode. 1'b0: Interrupt disabled 1'b1: Interrupt enabled

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Bit	Attr	Reset Value	Description
1	RW	0x0	cap_hpc_int_en HPC interrupt enable for capture mode 1'b0: Interrupt disabled 1'b1: Interrupt enabled
0	RW	0x0	cap_lpc_int_en LPC interrupt enable for capture mode 1'b0: Interrupt disabled 1'b1: Interrupt enabled

PWM_INT_MASK

Address: **Operational Base** + offset (0x0078)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	wave_middle_int_mask Waveform address access middle address mask 1'b0: Interrupt not mask 1'b1: Interrupt mask
7	RW	0x0	wave_max_int_mask Waveform address access maximum address interrupt mask 1'b0: Interrupt not mask 1'b1: Interrupt mask
6	RW	0x0	it_trans_end_int_mask IR Transmission end interrupt mask 1'b0: Interrupt not mask 1'b1: Interrupt mask
5	RW	0x0	pwr_int_mask Power key match interrupt mask 1'b0: Interrupt not mask 1'b1: Interrupt mask
4	RW	0x0	freq_int_mask Frequency meter interrupt mask 1'b0: Interrupt not mask 1'b1: Interrupt mask
3	RW	0x0	reload_Int_mask Reload interrupt mask 1'b0: Interrupt not mask 1'b1: Interrupt mask

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Bit	Attr	Reset Value	Description
2	RW	0x0	oneshot_end_mask Waveform end interrupt mask for one-shot mode. 1'b0: Interrupt not mask 1'b1: Interrupt mask
1	RW	0x0	cap_hpc_int_mask HPC interrupt mask for capture mode 1'b0: Interrupt not mask 1'b1: Interrupt mask
0	RW	0x0	cap_lpc_int_mask LPC interrupt mask for capture mode 1'b0: Interrupt not mask 1'b1: Interrupt mask

PWM_FEATURE

Address: **Operational Base** + offset (0x007C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	ledc_support LEDC support
14	RO	0x0	biphasic_counter_support Biphasic counter support
13	RO	0x0	filter_support Filter support
12	RO	0x0	wave_support Waveform generator support
11	RO	0x0	counter_support Counter support
10	RO	0x0	freq_meter_support Frequency meter support
9	RO	0x0	power_key_support Power key support
8	RO	0x0	ir_trans_support IR transmission support
7:4	RO	0x4	channel_index Channel index
3:0	RO	0x4	channel_num_support Channel number support

PWM_WAVE_MEM_ARBITER

Address: **Operational Base** + offset (0x0080)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
23:16	RW	0x00	wave_mem_read_lock Each bit controls the read lock of waveform generator memory. Once one channel obtains arbitration, other channels cannot read waveform generator memory. 1'b0: Don't lock 1'b1: Lock
15:8	RO	0x00	reserved
7:0	RW	0x00	wave_mem_grant Each bit controls the grant of waveform generator memory for one channel. Once one channel obtains arbitration, other channels cannot write waveform generator memory. 1'b0: Don't Grant 1'b1: Grant

PWM_WAVE_MEM_STATUS

Address: **Operational Base** + offset (0x0084)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	access_done Indicate the access to waveform generator memory is done.

PWM_WAVE_CTRL

Address: **Operational Base** + offset (0x0088)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:11	RW	0x00	wave_period_amplify Waveform generator table period value amplify, the value N means amplify by 2^N.
10:6	RW	0x00	wave_duty_amplify Waveform generator table duty value amplify, the value N means amplify by 2^N.
5:4	RW	0x1	wave_mem_clk_sel Waveform generator memory clock selection 2'b00: Select clk_pwm 2'b01: Select clk_pwm_osc 2'b10: Select clk_pwm_rc

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Bit	Attr	Reset Value	Description
3	RW	0x0	wave_update_mode Waveform generator update mode 1'b0: The address will wrap back to minimum address when increase to maximum address, and then increase again. 1'b1: The address will change to decreasing when increasing to the maximum address. it will return to increasing when decrease to the minimum value.
2	RW	0x0	wave_width_mode Waveform generator width mode 1'b0: 8bits 1'b1: 16bits Note: The table is 8bit, User can compose 16 bits with two adjacent addresses
1	RW	0x0	wave_period_en Waveform generator period enable. The period cycle of the output waveform is controlled by waveform generator table instead of register PWM_PERIOD when this bit is set to 1. The period will be updated every waveform number of rpt_first_dimensional.
0	RW	0x0	wave_duty_en Waveform generator duty enable. The duty cycle of the output waveform is controlled by waveform generator table instead of register PWM_DUTY when this bit is set to 1. The duty will be updated every waveform number of rpt_first_dimensional.

PWM_WAVE_MAX

Address: **Operational Base** + offset (0x008C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	wave_period_max The maximum index of period.
15:10	RO	0x00	reserved
9:0	RW	0x000	wave_duty_max The maximum index of duty.

PWM_WAVE_MIN

Address: **Operational Base** + offset (0x0090)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	wave_period_min The minimum index of period.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	wave_duty_min The minimum index of duty.

PWM_WAVE_OFFSET

Address: **Operational Base** + offset (0x0094)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	wave_offset The initial offset index of duty and period

PWM_WAVE_MIDDLE

Address: **Operational Base** + offset (0x0098)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	wave_middle The middle index of duty and period.

PWM_WAVE_HOLD

Address: **Operational Base** + offset (0x009C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	middle_hold The time to hold at middle index. the unit is waveform number of rpt_first_dimensional
15:8	RW	0x00	min_hold The time to hold at minimum index. the unit is waveform number of rpt_first_dimensional
7:0	RW	0x00	max_hold The time to hold at maximum index. the unit is waveform number of rpt_first_dimensional

PWM_GLOBAL_ARBITER

Address: **Operational Base** + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
23:16	RW	0x00	global_read_lock Each bit controls the read lock of global control registers. Once one channel obtains arbitration, other channels cannot read global registers. 1'b0: Don't lock 1'b1: Lock
15:8	RO	0x00	reserved
7:0	RW	0x00	global_grant Each bit controls the grant of global control for one channel. Once one channel obtains arbitration, other channels cannot write global registers. 1'b0: Don't Grant 1'b1: Grant

PWM_GLOBAL_CTRL

Address: **Operational Base** + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:2	RO	0x0000	reserved
1	W1T	0x0	global_pwm_ctrl_update_en PWM global control update enable. The bit will be auto cleaned. The following register can be updated at the posedge of pwm_ctrl_update_en: PWM_CTRL, PWM_PERIOD, PWM_DUTY, PWM_OFFSET
0	RW	0x0	global_pwm_en Global PWM enable 1'b0: Disabled 1'b1: Enabled If the PWM is worked in the one-shot mode, this bit will be cleared at the end of operation.

PWM_PWRMATCH_ARBITER

Address: **Operational Base** + offset (0x0100)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
23:16	RW	0x00	pwrkey_read_lock Each bit controls the read lock of power key function. Once one channel obtains arbitration, other channels cannot read power key registers. 1'b0: Don't lock 1'b1: Lock
15:8	RO	0x00	reserved
7:0	RW	0x00	pwrkey_grant Each bit controls the grant of power key function for one channel. Once one channel obtains arbitration, other channels cannot write power key registers. 1'b0: Don't Grant 1'b1: Grant

PWM_PWRMATCH_CTRL

Address: **Operational Base** + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:4	RO	0x000	reserved
3	RW	0x0	pwrkey_int_ctrl 1'b0: Assert interrupt after key capture with power key match 1'b1: Assert interrupt after key capture without power key match
2	RW	0x0	pwrkey_capture_ctrl 1'b0: Capture the value after interrupt 1'b1: Capture the value directly
1	RW	0x0	pwrkey_polarity 1'b0: PWM in polarity is positive 1'b1: PWM in polarity is negative
0	RW	0x0	pwrkey_enable 1'b0: Disabled 1'b1: Enabled

PWM_PWRMATCH_LPRE

Address: **Operational Base** + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	RW	0x238c	cnt_max The maximum counter value

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Bit	Attr	Reset Value	Description
15:0	RW	0x22c4	cnt_min The minimum counter value

PWM_PWRMATCH_HPRE

Address: **Operational Base** + offset (0x010C)

Bit	Attr	Reset Value	Description
31:16	RW	0x11f8	cnt_max The maximum counter value
15:0	RW	0x1130	cnt_min The minimum counter value

PWM_PWRMATCH_LD

Address: **Operational Base** + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	RW	0x0294	cnt_max The maximum counter value
15:0	RW	0x01cc	cnt_min The minimum counter value

PWM_PWRMATCH_HD_ZERO

Address: **Operational Base** + offset (0x0114)

Bit	Attr	Reset Value	Description
31:16	RW	0x0294	cnt_max The maximum counter value
15:0	RW	0x01cc	cnt_min The minimum counter value

PWM_PWRMATCH_HD_ONE

Address: **Operational Base** + offset (0x0118)

Bit	Attr	Reset Value	Description
31:16	RW	0x06fe	cnt_max The maximum counter value
15:0	RW	0x0636	cnt_min The minimum counter value

PWM_PWRMATCH_VALUE0

Address: **Operational Base** + offset (0x011C)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value0 Power key match value 0

PWM_PWRMATCH_VALUE1

Address: **Operational Base** + offset (0x0120)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value1 Power key match value 1

PWM_PWRMATCH_VALUE2

Address: **Operational Base** + offset (0x0124)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value2 Power key match value 2

PWM_PWRMATCH_VALUE3

Address: **Operational Base** + offset (0x0128)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value3 Power key match value 3

PWM_PWRMATCH_VALUE4

Address: **Operational Base** + offset (0x012C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value4 Power key match value 4

PWM_PWRMATCH_VALUE5

Address: **Operational Base** + offset (0x0130)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value5 Power key match value 5

PWM_PWRMATCH_VALUE6

Address: **Operational Base** + offset (0x0134)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value6 Power key match value 6

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PWM_PWRMATCH_VALUE7

Address: **Operational Base** + offset (0x0138)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value7 Power key match value 7

PWM_PWRMATCH_VALUE8

Address: **Operational Base** + offset (0x013C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value8 Power key match value 8

PWM_PWRMATCH_VALUE9

Address: **Operational Base** + offset (0x0140)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value9 Power key match value 9

PWM_PWRMATCH_VALUE10

Address: **Operational Base** + offset (0x0144)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value10 Power key match value 10

PWM_PWRMATCH_VALUE11

Address: **Operational Base** + offset (0x0148)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value11 Power key match value 11

PWM_PWRMATCH_VALUE12

Address: **Operational Base** + offset (0x014C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value12 Power key match value 12

PWM_PWRMATCH_VALUE13

Address: **Operational Base** + offset (0x0150)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value13 Power key match value 13

PWM_PWRMATCH_VALUE14

Address: **Operational Base** + offset (0x0154)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value14 Power key match value 14

PWM_PWRMATCH_VALUE15

Address: **Operational Base** + offset (0x0158)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwrkey_match_value15 Power key match value 15

PWM_PWRCAPTURE_VALUE

Address: **Operational Base** + offset (0x015C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pwrkey_capture_value Power key capture value

PWM_IR_TRANS_ARBITER

Address: **Operational Base** + offset (0x0180)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	ir_trans_read_lock Each bit controls the read lock of IR transmission function. Once one channel obtains arbitration, other channels cannot read power key registers. 1'b0: Don't lock 1'b1: Lock
15:8	RO	0x00	reserved
7:0	RW	0x00	ir_trans_grant Each bit controls the grant of IR transmission function for one channel. Once one channel obtains arbitration, other channels cannot write power key registers. 1'b0: Don't Grant 1'b1: Grant

PWM_IR_TRANS_CTRL0

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Address: **Operational Base** + offset (0x0184)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:14	RO	0x0	reserved
13	RW	0x0	ir_trans_clk_en_force PWM IR Trans Out Function clock enable force.
12:8	RW	0x1f	ir_trans_length_within_one_frame 0x00~0x1F is corresponding to data length 1~32
7:4	RW	0x0	ir_trans_format PWM IR Trans format 4'h0: NEC with simple repeat code 4'h1: NEC with full repeat code 4'h2: TC9012 4'h3: SONY Others: reserved
3	RW	0x0	ir_trans_mode 1'b0: One shot mode, PWM produces the waveform within the repeated times defined by ir_trans_rtp_cnt. 1'b1: Continuous mode, PWM produces the waveform continuously.
2	RW	0x0	ir_trans_inactive_pol This defines the output waveform polarity when PWM channel is in inactive state. The inactive state means that PWM finishes the complete waveform in one-shot mode or PWM channel is disabled. 1'b0: Negative 1'b1: Positive
1	RW	0x0	ir_trans_duty_pol This defines the polarity for duty cycle. PWM starts the output waveform with duty cycle. 1'b0: Negative 1'b1: Positive
0	RW	0x0	ir_trans_out_enable 1'b0: disable PWM IR Trans Out Function 1'b1: enable PWM IR Trans Out Function

PWM_IR_TRANS_CTRL1

Address: **Operational Base** + offset (0x0188)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:0	RW	0x0000	ir_trans_rpt This field defines the repeated number for IR transmission. The value N means N+1 repeated effective periods.

PWM_IR_TRANS_PRE

Address: **Operational Base** + offset (0x018C)

Bit	Attr	Reset Value	Description
31:16	RW	0x1194	ir_trans_out_high_preload IR Trans Out High Preload Register
15:0	RW	0x2328	ir_trans_out_low_preload IR Trans Out Low Preload Register

PWM_IR_TRANS_SPRE

Address: **Operational Base** + offset (0x0190)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x08ca	ir_trans_out_high_simple_preload PWM IR Trans Out High Simple Preload Register

PWM_IR_TRANS_LD

Address: **Operational Base** + offset (0x0194)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0230	ir_trans_out_data_low_period IR Trans Out Data Low Period Register

PWM_IR_TRANS_HD

Address: **Operational Base** + offset (0x0198)

Bit	Attr	Reset Value	Description
31:16	RW	0x069a	ir_trans_out_high_period_for_one IR Trans Out High Period for One Register
15:0	RW	0x0230	ir_trans_out_high_period_for_zero IR Trans Out High Period for Zero Register

PWM_IR_TRANS_BURST_FRAME

Address: **Operational Base** + offset (0x019C)

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Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x226	ir_trans_out_burst_period PWM IR Trans Out Burst Period Register
19:18	RO	0x0	reserved
17:0	RW	0x1a5e0	ir_trans_out_frame_period PWM IR Trans Out Frame Period

PWM_IR_TRANS_DATA_VALUE

Address: **Operational Base** + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ir_trans_out_value PWM IR Trans Out Value Register

PWM_IR_TRANS_STATUS

Address: **Operational Base** + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x1	ir_state_idle 1'b0: PWM IR Trans Busy 1'b1: PWM IR Trans Idle

PWM_FREQ_ARBITER

Address: **Operational Base** + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	freq_read_lock Each bit controls the read lock of frequency meter function. Once one channel obtains arbitration, other channels cannot read frequency meter registers. 1'b0: Don't lock 1'b1: Lock
15:8	RO	0x00	reserved
7:0	RW	0x00	freq_grant Each bit controls the grant of frequency meter function for one channel. Once one channel obtains arbitration, other channels cannot write frequency meter registers. 1'b0: Don't Grant 1'b1: Grant

PWM_FREQ_CTRL

Address: **Operational Base** + offset (0x01C4)

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:9	RO	0x00	reserved
8	RW	0x0	freq_continuous_start_mode Frequency Meter continuous start mode
7	RW	0x0	freq_timer_clk_sel Frequency meter timer clock selection 1'b0: Select clk_pwm, clock is from PLL and the frequency can be configured. 1'b1: Select clk_pwm_osc, clock is from crystal oscillator and the frequency is fixed.
6	W1T	0x0	freq_timer_clk_switch_mode Timer clock switch mode 1'b0: Normal mode 1'b1: Switch timer clock and measured clock. It Can be used to provide testing accuracy or reduce testing time when the frequency of measured clock is low. It can also be used in scenarios where the start time of the measured clock is uncertain
5:3	RW	0x0	freq_channel_sel Frequency Meter channel selection. It's valid only when freq_clk_sel set to 1'b0. 3'b000: PWM channel 0 3'b001: PWM channel 1 3'b010: PWM channel 2 3'b011: PWM channel 3 3'b100: PWM channel 4 3'b101: PWM channel 5 3'b110: PWM channel 6 3'b111: PWM channel 7
2	RO	0x0	reserved
1	RW	0x0	freq_clk_sel Frequency Meter clock selection 1'b0: Input from PWM IO 1'b1: Frequency clock from CRU
0	W1T	0x0	freq_en Frequency Meter enable.

PWM_FREQ_TIMER_VALUE

Address: **Operational Base** + offset (0x01C8)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	freq_timer_value Frequency Meter timer value, the unit is one cycle frequency meter timer clock.

PWM_FREQ_RESULT_VALUE

Address: **Operational Base** + offset (0x01CC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	freq_result_value The frequency result value, the unit is one cycle of tested clock. Once the freq_intsts interrupt is asserted, User can get the frequency by this value. When timer_clk_switch_mode set to 1'b0, the frequency result is (freq_timer*freq_result_value)/freq_timer_value. When timer_clk_switch_mode set to 1'b1, the frequency result is (freq_timer*freq_timer_value)/freq_result_value. Notes: freq_osc is the frequency of SOC crystal oscillator.

PWM_FREQ_RESULT_VALUE_RAW

Address: **Operational Base** + offset (0x01D0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	freq_result_value_raw The frequency result raw value.

PWM_COUNTER_ARBITER

Address: **Operational Base** + offset (0x0200)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	counter_read_lock Each bit controls the read lock of counter function. Once one channel obtains arbitration, other channels cannot read counter registers. 1'b0: Don't lock 1'b1: Lock
15:8	RO	0x00	reserved
7:0	RW	0x00	counter_grant Each bit controls the grant of counter for one channel. Once one channel obtains arbitration, other channels cannot write counter registers. 1'b0: Don't Grant 1'b1: Grant

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PWM_COUNTER_CTRL

Address: **Operational Base** + offset (0x0204)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16 bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:7	RO	0x000	reserved
6	W1T	0x0	counter_clr Counter value clear.
5:3	RW	0x0	counter_channel_sel Counter channel selection. It's valid only when counter_clk_sel set to 1'b0. 3'b000: PWM channel 0 3'b001: PWM channel 1 3'b010: PWM channel 2 3'b011: PWM channel 3 3'b100: PWM channel 4 3'b101: PWM channel 5 3'b110: PWM channel 6 3'b111: PWM channel 7
2:1	RW	0x0	counter_clk_sel Counter clock selection 1'b0: Input from PWM IO 1'b1: Counter clock from CRU
0	RW	0x0	counter_en Counter enable.

PWM_COUNTER_LOW

Address: **Operational Base** + offset (0x0208)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	counter_low_bits Indicates low 32 bits of counter value. The value of counter ranges from 0 to 2^64-1, The unit is one cycle of tested clock

PWM_COUNTER_HIGH

Address: **Operational Base** + offset (0x020C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	counter_high_bits Indicates high 32 bits of the counter value. The value of counter ranges from 0 to 2^64-1, The unit is one cycle of tested clock

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PWM_WAVE_MEM

Address: **Operational Base** + offset (0x0400)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	wave_mem_base_address Waveform Generator memory base address

38.5 Interface Description

Table 38-2 PWM_M0 Interface Description

Module Pin	Direction	Pin Name	IOMUX Setting
PWM0_CH0_M0	I/O	GPIO0_C4	GPIO0C_IOMUX_SEL_1[3:0] = 0x2
PWM0_CH1_M0	I/O	GPIO0_C5	GPIO0C_IOMUX_SEL_1[7:4] = 0x2
PWM0_CH2_M0	I/O	GPIO0_C6	GPIO0C_IOMUX_SEL_1[11:8] = 0x2
PWM0_CH3_M0	I/O	GPIO0_C7	GPIO0C_IOMUX_SEL_1[15:12] = 0x2
PWM0_CH4_M0	I/O	GPIO0_D0	GPIO0D_IOMUX_SEL_0[3:0] = 0x2
PWM0_CH5_M0	I/O	GPIO0_D1	GPIO0D_IOMUX_SEL_0[7:4] = 0x2
PWM0_CH6_M0	I/O	GPIO0_C1	GPIO0C_IOMUX_SEL_0[7:4] = 0x2
PWM0_CH7_M0	I/O	GPIO0_C0	GPIO0C_IOMUX_SEL_0[3:0] = 0x2
PWM1_CH0_M0	I/O	GPIO0_A5	GPIO0A_IOMUX_SEL_1[7:4] = 0x2
PWM1_CH1_M0	I/O	GPIO0_A1	GPIO0B_IOMUX_SEL_0[7:4] = 0x2
PWM1_CH2_M0	I/O	GPIO0_B3	GPIO0B_IOMUX_SEL_0[15:12] = 0x2
PWM1_CH3_M0	I/O	GPIO0_B4	GPIO0B_IOMUX_SEL_1[3:0] = 0x2
PWM2_CH0_M0	I/O	GPIO3_B2	GPIO3B_IOMUX_SEL_0[11:8] = 0x3
PWM2_CH1_M0	I/O	GPIO3_B3	GPIO3B_IOMUX_SEL_0[15:12] = 0x3
PWM2_CH2_M0	I/O	GPIO3_B4	GPIO3B_IOMUX_SEL_1[3:0] = 0x3
PWM2_CH3_M0	I/O	GPIO3_B5	GPIO3B_IOMUX_SEL_1[7:4] = 0x3
PWM2_CH4_M0	I/O	GPIO5_A0	GPIO5A_IOMUX_SEL_0[3:0] = 0x7
PWM2_CH5_M0	I/O	GPIO5_A1	GPIO5A_IOMUX_SEL_0[7:4] = 0x7
PWM2_CH6_M0	I/O	GPIO5_D6	GPIO5D_IOMUX_SEL_1[11:8] = 0x7
PWM2_CH7_M0	I/O	GPIO5_D7	GPIO5D_IOMUX_SEL_1[15:12] = 0x7
PWM3_CH0_M0	I/O	GPIO1_A0	GPIO1A_IOMUX_SEL_0[3:0] = 0x3
PWM3_CH1_M0	I/O	GPIO1_A1	GPIO1A_IOMUX_SEL_0[7:4] = 0x3
PWM3_CH2_M0	I/O	GPIO1_A2	GPIO1A_IOMUX_SEL_0[11:8] = 0x3
PWM3_CH3_M0	I/O	GPIO1_A3	GPIO1A_IOMUX_SEL_0[15:12] = 0x3
PWM3_CH4_M0	I/O	GPIO1_A4	GPIO1A_IOMUX_SEL_1[3:0] = 0x3
PWM3_CH5_M0	I/O	GPIO1_A5	GPIO1A_IOMUX_SEL_1[7:4] = 0x3
PWM3_CH6_M0	I/O	GPIO1_A6	GPIO1A_IOMUX_SEL_1[11:8] = 0x3
PWM3_CH7_M0	I/O	GPIO1_A7	GPIO1A_IOMUX_SEL_1[15:12] = 0x3

Table 38-3 PWM_M1 Interface Description

Module Pin	Direction	Pin Name	IOMUX Setting
PWM0_CH0_M1	I/O	GPIO5_A7	GPIO5A_IOMUX_SEL_1[15:12] = 0x7

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Module Pin	Direction	Pin Name	IOMUX Setting
PWM0_CH1_M1	I/O	GPIO5_A6	GPIO5A_IOMUX_SEL_1[11:8] = 0x7
PWM0_CH2_M1	I/O	GPIO5_A5	GPIO5A_IOMUX_SEL_1[7:4] = 0x7
PWM0_CH3_M1	I/O	GPIO5_A4	GPIO5A_IOMUX_SEL_1[3:0] = 0x7
PWM0_CH4_M1	I/O	GPIO4_A2	GPIO4A_IOMUX_SEL_0[11:8] = 0x4
PWM0_CH5_M1	I/O	GPIO4_A3	GPIO4A_IOMUX_SEL_0[15:12] = 0x4
PWM0_CH6_M1	I/O	GPIO4_A6	GPIO4A_IOMUX_SEL_1[11:8] = 0x4
PWM0_CH7_M1	I/O	GPIO4_A7	GPIO4A_IOMUX_SEL_1[15:12] = 0x4
PWM1_CH0_M1	I/O	GPIO5_D3	GPIO5D_IOMUX_SEL_0[15:12]= 0x7
PWM1_CH1_M1	I/O	GPIO5_D2	GPIO5D_IOMUX_SEL_0[11:8]= 0x7
PWM1_CH2_M1	I/O	GPIO5_D1	GPIO5D_IOMUX_SEL_0[7:4] = 0x7
PWM1_CH3_M1	I/O	GPIO5_D5	GPIO5D_IOMUX_SEL_1[7:4] = 0x7
PWM2_CH0_M1	I/O	GPIO5_B2	GPIO5B_IOMUX_SEL_0[11:8] = 0x7
PWM2_CH1_M1	I/O	GPIO5_B3	GPIO5B_IOMUX_SEL_0[15:12] = 0x7
PWM2_CH2_M1	I/O	GPIO5_B6	GPIO5B_IOMUX_SEL_1[11:8] = 0x7
PWM2_CH3_M1	I/O	GPIO5_B7	GPIO5B_IOMUX_SEL_1[15:12] = 0x7
PWM2_CH4_M1	I/O	GPIO7_A0	GPIO7A_IOMUX_SEL_0[3:0] = 0x5
PWM2_CH5_M1	I/O	GPIO7_A1	GPIO7A_IOMUX_SEL_0[7:4] = 0x5
PWM2_CH6_M1	I/O	GPIO7_A2	GPIO7A_IOMUX_SEL_0[11:8] = 0x5
PWM2_CH7_M1	I/O	GPIO7_A3	GPIO7A_IOMUX_SEL_0[15:12] = 0x5
PWM3_CH0_M1	I/O	GPIO5_C0	GPIO5C_IOMUX_SEL_0[3:0] = 0x7
PWM3_CH1_M1	I/O	GPIO5_C1	GPIO5C_IOMUX_SEL_0[7:4] = 0x7
PWM3_CH2_M1	I/O	GPIO5_C2	GPIO5C_IOMUX_SEL_0[11:8] = 0x7
PWM3_CH3_M1	I/O	GPIO5_C3	GPIO5C_IOMUX_SEL_0[15:12] = 0x7
PWM3_CH4_M1	I/O	GPIO5_C4	GPIO5C_IOMUX_SEL_1[3:0] = 0x7
PWM3_CH5_M1	I/O	GPIO5_C5	GPIO5C_IOMUX_SEL_1[7:4] = 0x7
PWM3_CH6_M1	I/O	GPIO5_C6	GPIO5C_IOMUX_SEL_1[11:8] = 0x7

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Module Pin	Direction	Pin Name	IOMUX Setting
PWM3_CH7_M1	I/O	GPIO5_C7	GPIO5C_IOMUX_SEL_1[15:12] = 0x7

Table 38-4 PWM_M2 Interface Description

Module Pin	Direction	Pin Name	IOMUX Setting
PWM0_CH0_M2	I/O	GPIO6_C0	GPIO6C_IOMUX_SEL_0[3:0] = 0x5
PWM0_CH1_M2	I/O	GPIO6_C1	GPIO6C_IOMUX_SEL_0[7:4] = 0x5
PWM0_CH2_M2	I/O	GPIO6_C2	GPIO6C_IOMUX_SEL_0[11:8] = 0x5
PWM0_CH3_M2	I/O	GPIO6_C3	GPIO6C_IOMUX_SEL_0[15:12] = 0x5
PWM0_CH4_M2	I/O	GPIO5_A3	GPIO5A_IOMUX_SEL_0[15:12] = 0x7
PWM0_CH5_M2	I/O	GPIO5_A2	GPIO5A_IOMUX_SEL_0[11:8] = 0x7
PWM0_CH6_M2	I/O	GPIO5_D0	GPIO5D_IOMUX_SEL_0[3:0] = 0x7
PWM0_CH7_M2	I/O	GPIO5_D4	GPIO5D_IOMUX_SEL_1[3:0] = 0x7
PWM1_CH0_M2	I/O	GPIO6_A0	GPIO6A_IOMUX_SEL_0[3:0] = 0x5
PWM1_CH1_M2	I/O	GPIO6_A1	GPIO6A_IOMUX_SEL_0[7:4] = 0x5
PWM1_CH2_M2	I/O	GPIO6_A2	GPIO6A_IOMUX_SEL_0[11:8] = 0x5
PWM1_CH3_M2	I/O	GPIO6_A3	GPIO6A_IOMUX_SEL_0[15:12] = 0x5
PWM2_CH0_M2	I/O	GPIO6_A4	GPIO6A_IOMUX_SEL_1[3:0] = 0x5
PWM2_CH1_M2	I/O	GPIO6_A5	GPIO6A_IOMUX_SEL_1[7:4] = 0x5
PWM2_CH2_M2	I/O	GPIO6_A6	GPIO6A_IOMUX_SEL_1[11:8] = 0x5
PWM2_CH3_M2	I/O	GPIO6_A7	GPIO6A_IOMUX_SEL_1[15:12] = 0x3

Notes: I=input, O=output, I/O=input/output.

38.6 Application Notes

38.6.1 PWM Capture Mode Standard Usage Flow

1. Set PWM_ENABLE.pwm_en to 1'b0 to disable the PWM channel.
2. Set PWM_CLK_CTRL.prescale/scale/clk_src_sel to configure the clock selection and division.
3. Set PWM_CTRL.pwm_mode to 2'b10 to select capture mode.
4. Set PWM_INT_EN.cap_lpc_int_en/cap_hpc_int_en to 1'b1 to enable the interrupt.
5. Set PWM_ENABLE.pwm_en/pwm_clk_en to 1'b1 to enable the channel.
6. When an interrupt is asserted, refer to PWM_INTSTS register to know the raw interrupt status. User should read the PWM_HPC register to know the effective high cycles of input waveforms when cap_hpc_intsts is asserted and read the PWM_LPC register to know the effective low cycles when cap_lpc_intsts is asserted. User should set 1'b1 to correspond bit of PWM_INTSTS to clear the interrupt.
7. If user want to disable PWM channel, set PWM_ENABLE.pwm_en/pwm_clk_en to 1'b0.

38.6.2 PWM Power key Capture Mode Standard Usage Flow

1. Set PWM_ENABLE.pwm_en to 1'b0 to disable the PWM channel.

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2. Set PWM_CLK_CTRL.prescale/scale/clk_src_sel to configure the clock selection and division. The clock frequency should be 1 MHz after division.
3. Set PWM_CTRL.pwm_mode to 2'b10 to select capture mode.
4. Set PWM_PWRMATCH_ARBITER.pwrkey_grant to 8'b01 to set channel 0 for capture.
5. Set PWM_INT_EN.pwr_int_en to 1'b1 to enable the interrupt.
6. Set PWM_PWRMATCH_VALUE0~15 registers for the 16 power key match value.
7.Set max_cnt and min_cnt of follow register: PWM_PWRMATCH_LPRE, PWM_PWRMATCH_HPRE, PWM_PWRMATCH_LD, PWM_PWRMATCH_HD_ZERO, PWM_PWRMATCH_HD_ONE. It doesn't need to set these registers if the default value can meet the requirement.
8. Set PWM_PWRMATCH_CTRL.pwrkey_polarity for the polarity of power key signal.
9. SetPWM_PWRMATCH_CTRL.pwrkey_enable to 1'b1 to enable power key mode.
10. Set PWM_FILTER_CTRL.filter_number/filter_enable to enable filter(Optional).
11. Set PWM_ENABLE.pwm_en/pwm_clk_en to 1'b1 to enable the channel.
12. When an interrupt is asserted, refer to PWM_INTSTS register to know the raw interrupt status, and refer to PWM_PWRCAPTURE_VALUE to know the power key capture value.User should set 1'b1 to correspond bit of PWM_INTSTS to clear the interrupt.
13. If user want to disable PWM channel, set PWM_ENABLE.pwm_en/pwm_clk_en to 1'b0.

38.6.3 PWM ContinuousStandard Usage Flow

1. Set PWM_ENABLE.pwm_en to 1'b0 to disable the PWM channel.
2. Set PWM_CLK_CTRL.prescale/scale/clk_src_sel to configure the clock selection and division.
3. Set PWM_CTRL.output_mode/duty_pol/inactive_pol to select output mode, duty polarity and inactive polarity.
4. Set PWM_PERIOD and PWM_DUTY register.
5. Set PWM_RPT.rpt_first_dimensional for reload operation (Optional).
6. Set PWM_CTRL.pwm_mode to 2'b01 to select continuous mode.
7. Set PWM_ENABLE.pwm_en/pwm_clk_en to 1'b1 to enable the channel.
8. Set PWM_PERIOD and DUTY, then set PWM_ENABLE.pwm_ctrl_update_en to 1'b1 to update configuration (Optional).
9. If user want to disable PWM channel, set PWM_ENABLE.pwm_en/pwm_clk_en to 1'b0.

38.6.4 PWM One-shot ModeStandard Usage Flow

1. Set PWM_ENABLE.pwm_en to 1'b0 to disable the PWM channel.
2. Set PWM_CLK_CTRL.prescale/scale/clk_src_sel to configure the clock selection and division.
3. Set PWM_CTRL.output_mode/duty_pol/inactive_pol to select output mode, duty polarity and inactive polarity.
4. Set PWM_PERIOD and PWM_DUTY register.
5. Set PWM_RPT.rpt_first_dimensional for reload operation (Option).
6. Set PWM_RPT.rpt_second_dimensional.
7. Set PWM_CTRL.pwm_mode to 2'b00 to select one shot mode.
8. Set INT_EN.oneshot_end_int_en to 1'b1 to enable interrupt.
9. Set PWM_ENABLE.pwm_en/pwm_clk_en to 1'b1 to enable the channel.
10. When an interrupt is asserted, refer to PWM_INTSTS register to know the raw interrupt. User should set 1'b1 to correspond bit of PWM_INTSTS to clear the interrupt. PWM_CTRL.pwm_en/pwm_clk_en is automatically cleared.

38.6.5 Multi-channel synchronous start UsageFlow

1. Set PWM_ENABLE.pwm_en of all synchronous channels to 1'b0 to disable the PWM channel.
2. Set PWM_CTRL.pwm_mode/output_mode/duty_pol/inactive_pol, PWM_PERIOD and PWM_DUTY register of all synchronous channels.
3. Set PWM_CLK_CTRL.prescale/scale/clk_src_sel of channel 0 to configure the clock selection and division.
4. Set PWM_Enable.pwm_global_join_en of all synchronous channels to 1'b1.
5. Enable the INT_EN.oneshot_end_int_en of channel 0 to enable interrupt generation if the channel is desired to work in the one-shot mode.
6. Set PWM_ENABLE.pwm_clk_en of channel 0 to 1'b1 to enable clock.

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7. Set PWM_GLOBAL_ARBITER.global_grant to 8'h01 to set channel 0 as main channel.
8. Set PWM_GLOBAL_CTRL.global_pwm_en to enable all synchronous channels.
9. Set PWM_PERIOD and DUTY to all synchronous channel, then set PWM_GLOBAL_CTRL.global_pwm_ctrl_update_en to 1'b1 to update configuration of all synchronous channels (Optional).
10.If user want to disable PWM channel,set PWM_GLOBAL_CTRL.global_pwm_en to 1'b0, then set PWM_CTRL.pwm_clk_en of channel 0 to 1'b0 to disable clock.

38.6.6 Clock counter UsageFlow

1. Set PWM_COUNTER_ARBITER.counter_grant to 8'h01 to use channel 0.
2. Set PWM_COUNTER_CTRL.counter_clk_sel/counter_channel_sel to select clock.
3. Set PWM_COUNTER_CTRL.counter_en to 1'b1 to enable clock counter.
4. Refer to PWM_COUNTER_LOW/ PWM_COUNTER_HIGH to gets the counter value.
5. If user want to disable clock counter, set PWM_COUNTER_CTRL.counter_en to 1'b0, then set PWM_COUNTER_ARBITER.counter_grant to 8'h0.

38.6.7 Clock Frequency meter UsageFlow

1. Set PWM_FREQ_ARBITER.freq_grant to 8'h01 to use channel 0.
2. Set PWM_FREQ_CTRL.freq_clk_sel/freq_channel_sel to select clock.
3. Set PWM_FREQ_CTRL.freq_timer_clk_sel to select timer clock.
4. Set PWM_FREQ_TIMER_VALUE.freq_timer_value to set timer.
5. Set PWM_INT_EN.freq_int_en to enable interrupt.
6. Set PWM_FREQ_CTRL.freq_en to 1'b1 to enable clock frequency meter.
7. When an interrupt is asserted, refer to PWM_INTSTS register to know the raw interrupt. Then refer PWM_FREQ_RESULT_VALUE.freq_result_value to get result. The frequency can be calculated as formula: frequency_timer* freq_result_value/ freq_timer_value. User should set 1'b1 to correspond bit of PWM_INTSTS to clear the interrupt.
8. If user want to disable clock frequency meter, set PWM_FREQ_ARBITER.freq_grant to 8'h0.

38.6.8 Biphasic Counter UsageFlow

1. Set PWM_BIPHASIC_COUNTER_CTRL0.biphasic_counter_clk_sel to select clock.
2. Set PWM_BIPHASIC_COUNTER_CTRL0.biphasic_counter_mode to select mode.
3. Set PWM_BIPHASIC_COUNTER_CTRL1.biphasic_counter_filter_number/ biphasic_counter_filter_enable to set the filter.
4. Set PWM_BIPHASIC_COUNTER_TIMER_VALUE. biphasic_counter_timer_value to set timer.
5. Set PWM_INT_EN.biphasic_couner_int_en to enable interrupt.
6. Set PWM_BIPHASIC_COUNTER_CTRL0.biphasic_counter_en to 1'b1 to enable biphasic counter.
7. When an interrupt is asserted, refer to PWM_INTSTS register to know the raw interrupt. Then refer PWM_BIPHASIC_COUNTER_RESULT_VALUE to get the result. User should set 1'b1 to correspond bit of PWM_INTSTS to clear the interrupt.

38.6.9 Generates Waveform Through Lookup Table UsageFlow

1. Set PWM_ENABLE.pwm_en to 1'b0 to disable the PWM channel.
2. Set PWM_CLK_CTRL.prescale/scale/clk_src_sel to configure the clock selection and division.
3. Set PWM_CTRL.output_mode/duty_pol/inactive_pol to select output mode, duty polarity and inactive polarity.
4. Set PWM_PERIOD register, the value should be 1~256.
5. Set PWM_WAVE_CTRL.wave_duty_en to 1'b1 to enable duty to reload through lookup table.
6. Set PWM_WAVE_CTRL.wave_update_mode to 1'b1.
7. Set PWM_WAVE_MAX.wave_duty_max.
8. Set PWM_WAVE_MIN.wave_duty_min.
9. Set the duty value in lookup table from offset address wave_duty_min to wave_duty_max. The base address of lookup table is PWM_WAVE_MEM.
10. Set PWM_RPT.rpt_first_dimensional for reloading interval.
11. Set PWM_CTRL.pwm_mode to 2'b01 to select continuous mode.
12. Set PWM_ENABLE.pwm_en/pwm_clk_en to 1'b1 to enable the channel.

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Chapter 39 RKCAN

39.1 Overview

CAN bus is a robust vehicle bus standard designed to allow microcontrollers and devices to communicate with each other in applications without a host computer. It is a message-based protocol, designed originally for multiplex electrical wiring within automobiles to save on copper, but is also used in many other contexts.
RKCAN controller supports the following features:

- Compatible with ISO 11898-1-2003 specification
- Support AHB slave interface
- Support AHB master interface
- Support classical transmit or receive standard frame
- Support classical transmit or receive extended frame
- Support transmit or receive data frame, remote frame, overload frame, error frame and frame interval
- Support transmit or receive error count
- Support acceptance filter
- Support bit error, bit stuffing error, form error, ack error and crc error
- Support interrupt and all interrupt can be masked
- Support controller status query
- Support error code check
- Support self test mode
- Support single sample and three sample configurable
- Support SJW(reSynchronization Jump Width) configurable
- Support BRP(system prescaler coefficient) configurable
- Support bit timing configurable
- Support loop-back mode for self-test operation
- Support silent mode for debug
- Support auto retransmission mode
- Support auto bus on after bus-off state
- Support 2 transmit buffers
- Support Internal Storage Mode
- Support protocol exception event
- Support DMA

39.2 Function Description

The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

39.2.1 Block Diagram

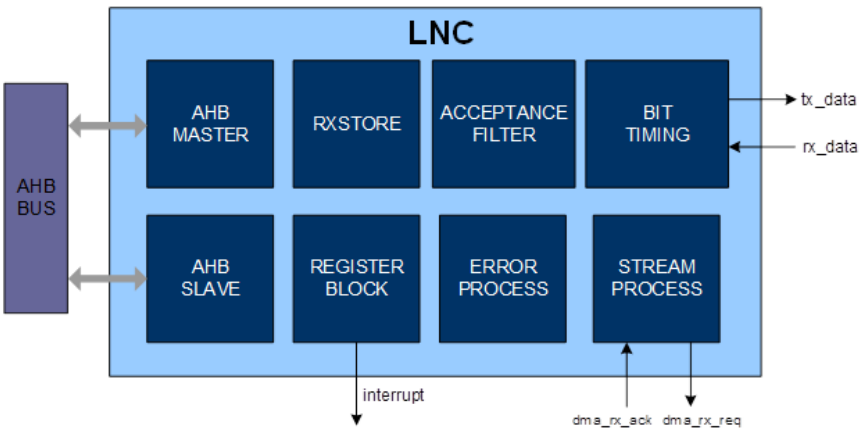

Fig. 39-1 RKCAN Block Diagram

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39.2.2 ACCEPTANCE FILTER

The Acceptance Filter (ATF) is a receive filter module. RKCAN can filter the received frames based on four identifiers: ID, RTR, and DLC. There are five sets of ID_RTR registers and one set of DLC registers for configuring the filter mode of RKCAN.The filtering mode based on ID and RTR has two types: List Mode and Mask Mode. The current ATF Mask register can be configured as either a mask mode or a list mode through the ATFMn.mask bit.

(1) Mask Mode: ATFM is used as the mask register of ATF, and RKCAN provides five sets of configurable 'filter-mask' registers.

(2) List Mode: ATFM is used as the filter register, and RKCAN provides ten configurable 'filter' registers."

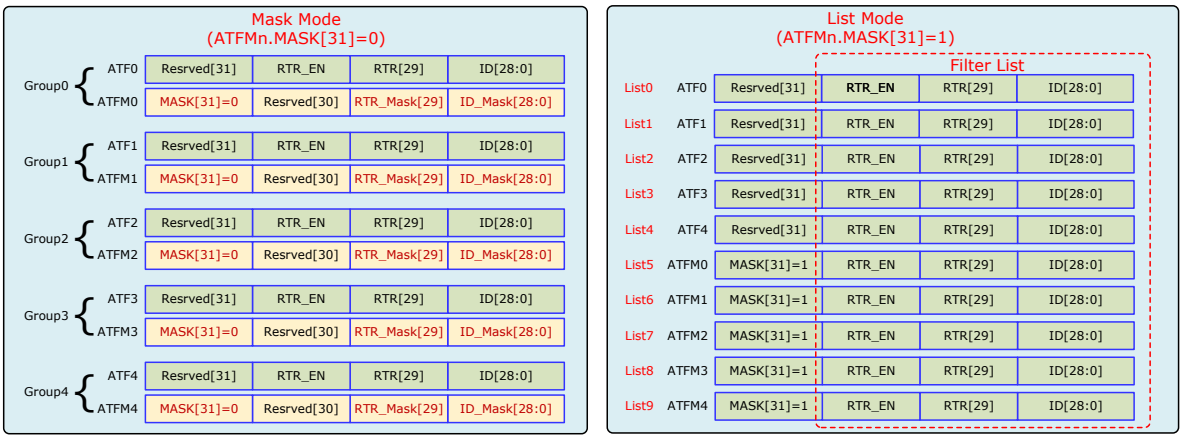

Fig. 39-2 ATF Mode

When filtering based on DLC, there are also two modes: Over Mode and Less Mode. The ATF_DLC.en bit is used to enable the DLC filter, the ARF_DLC.mode bit is used to select between the two modes, and the ATF_DLC.dlc[3:0] is used to configure the filter threshold.

(1) Over Mode: When ARF_DLC.mode is 0, if the dlc value of the received frame is greater than or equal to ATF_DLC.dlc[3:0], the frame can be received by RKCAN and stored in memory.

(2) Less Mode: When ARF_DLC.mode is 1, if the dlc value of the received frame is less than or equal to ATF_DLC.dlc[3:0], the frame can be received by RKCAN and stored in memory.

ATF_CTL[9:0] is used to control the switch status of ATF0~4 and ATFM0~4.

39.2.3 BIT TIMING

39.2.3.1 Bit Timing Logic

The bit timing logic controls the sampling point position through the buffer bits in the timing register to ensure the accuracy of the data sampling. The bit timing logic receives the clock frequency division signal for identification, sets the bus timing parameters, establishes synchronization parameters, and adjusts the bus transmission rate. At the same time, the bus is monitored and the message to be sent is transmitted to the bus at the set timing.

According to the provisions of the protocol: the bus is always at a high level when no message is sent, and the continuous recessive bit is monitored on the bus. At this time, the bus is in an idle state, and the arbitration priority is low, ready to receive data at any time. When the bus detects a transition from a recessive bit to a dominant bit, it is proved that the frame start bit starts transmitting, and the bus performs a hard synchronization in the bit start sync segment. Then, in the process of receiving the message, once the edge of the transition close to the sampling point is detected and the edge of the edge and the synchronization segment have a phase error lower than the synchronization width (SJW is taken when the value exceeds SJW), the controller executes once resynchronization, resynchronization can be performed multiple times during one data transmission.

39.2.3.2 Bit Timing Definition

The transmission time of each bit is divided into 4 parts:

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$$t_{nbt} = t_{sync_seg} + t_{prop_seg} + t_{phase_seg1} + t_{phase_seg2}$$

t_{sync_seg}, t_{prop_seg}, t_{phase_seg1} and t_{phase_seg2} are integer multiples of the unit time(t_{sclk}), and this unit time is a specific multiple of the system clock, which is determined by the division factor BRP in the bus timing register: 1. The counter is obtained by the BRP operation; 2. The system clock clk is counted by the counter; 3. When the limit is reached, a clock with a period of t_{sclk} is generated.

In the system design, considering the cyclical occurrence of each time period, a state machine with three states is used in the bit timing design. The three states correspond to the sync segment(sync_seg) and the phase buffer segment 1 (phase_seg1=phase_seg1+prog_seg) and the phase buffer segment 2 (phase_seg2), respectively. Where PHASE_SEG1 range: 1~16; PHASE_SEG2 range: 1~8; BRP range: 1~64.

$$t_{sync_seg} = 1 \times t_{sclk}$$

$$t_{prop_seg} + t_{phase_seg1} = t_{sclk} \times (8 \times TSEG1.3 + 4 \times TSEG1.2 + 2 \times TSEG1.1 + TSEG1.0 + 1)$$

$$t_{phase_seg2} = t_{sclk} \times (4 \times TSEG2.2 + 2 \times TSEG2.1 + TSEG1.0 + 1)$$

Define a counter to count t_{sclk}. When the count reaches the TSEG1, TSEG2 defined in the bus timing register and the length of the synchronization segment defined in the design, the system will generate the corresponding transition conditions: go_seg1, go_seg2, go_sync.

By judging these transition conditions, the control state machine cycles through the above three states.

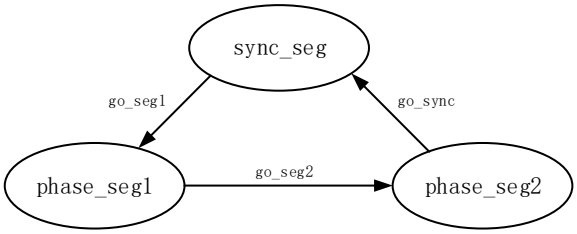

Fig. 39-3 Bit timing FSM

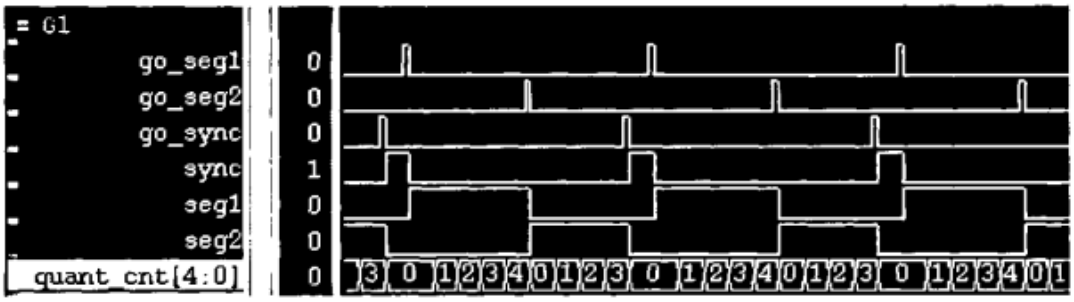

Fig. 39-4 Bit timing waveform diagram

39.2.3.3 Sampling Point and Sending Point

Sampling Point: According to the agreement, the sample point sample_point should be between phase_seg1 and phase_seg2. It is designed to be in the position of phase_seg2 synchronization. The sampling pulse width is defined as one system clock cycle.

Considering the accuracy of sampling, you can use the method of taking three samples to take the mean. The interval between each sample point is one t_{sclk}.

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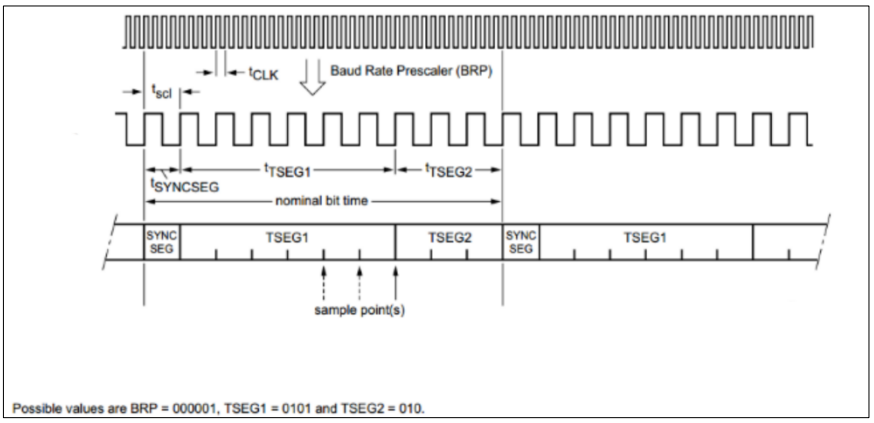

Fig. 39-5 Three sampling diagram

Sending Point: The location of the transmission point(tx_point) should be at the beginning of each bit time according to the protocol, and it is designed to synchronize it with the go_sync signal. In addition, if it is in sync or resynchronize, tx_point will be valid immediately.

39.2.3.4 Bit Synchronization

With the synchronization method, one or more nodes that satisfy the synchronization condition align their synchronization segments with the transmission data on the bus at a specific time. Synchronization occurs on the 1-to-0 transition edge in order to control the distance from the transition edge to the sample point. Two synchronization methods are defined in the bus communication protocol: hard synchronization and resynchronization.

Hard_sync: All nodes must be synchronized to the leading edge of the starting frame of the node that first started transmitting the message. At the beginning of each frame of data, a synchronization action is taken between the nodes.

Hard synchronization implementation method: determine whether the bus state meets the frame start condition specified in the protocol, and the node is not in the state of the data to be transmitted. At this time, a hard synchronization flag signal hard_sync is generated, and the pulse width is a system clock; The hard_sync entry is added to the control condition of the go_seg1 signal, and go_seg1 is valid immediately when the hard_sync signal is '1'. Therefore, once the hard synchronization condition is met, the system enters the phase_seg1 segment, thereby achieving synchronization.

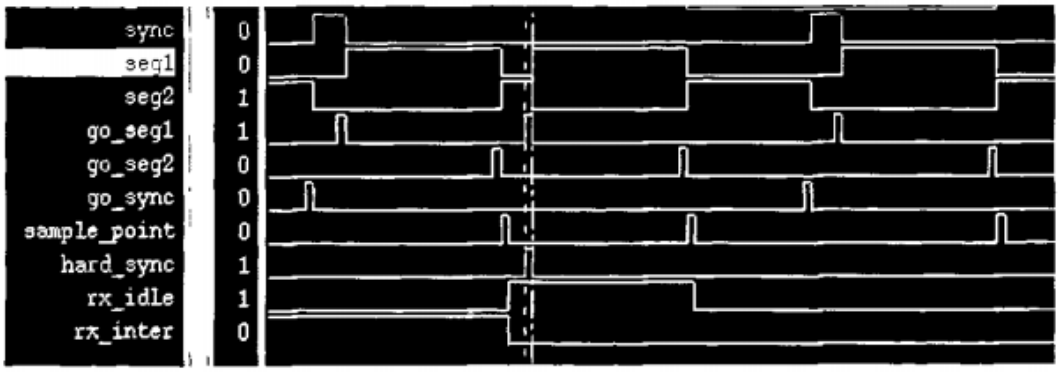

Fig. 39-6 Hard_sync waveform diagram

Resynchronization: In addition to generating hard synchronization at the beginning of each frame of data, the bus communication protocol also specifies the transmission of data for each frame. When the timing coordination between the nodes is not ideal, it will be resynchronized, so that the cooperation between the nodes is in a good state.

For the receiver, the bus changes it received should occur in the sync segment. Once the receiver's status violates this rule, the receiver will perform a resynchronization.

Two situations that require resynchronization:

1. The jump of the bus value '1' to '0' occurs between the sync segment and the sample point, which is a delay jump;
2. The jump of the bus value '1' to '0' occurs between the sample point and the sync segment, which is an early jump.

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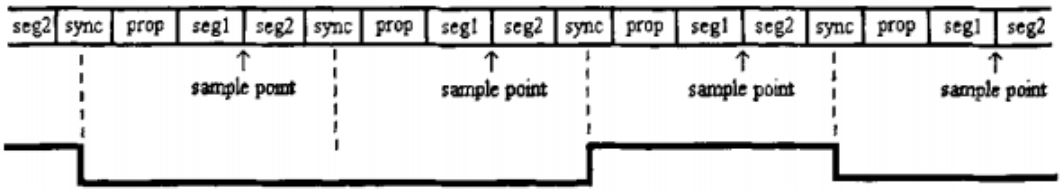

Fig. 39-7 Resynchronization

Resynchronization method:

1. Condition for resynchronization: the receiver is in a mode of receiving data (not inter-frame space or bus idle), and a resynchronization flag signal 'resync' is generated when a jump of the bus value '1' to '0' occurs;

2. According to the position of the resynchronization flag signal, it is determined that the abnormal jump is a delay jump or an early jump;

3. Counting the delay or the length of the advance by the counter;

4. In this bit, phase_seg1 is added with a delay time or phase_seg2 is subtracted from the advance time to obtain a new phase buffer time for the bit, thereby achieving synchronization.

39.2.4 RXSTORE

39.2.4.1 Internal Storage Mode

To store the frame data received by RKCAN only in the internal SRAM, the STR_CTL.stm needs to be configured as 0. The frame data received by RKCAN will only be stored in the internal SRAM. The size of the internal SRAM is 256x32bit. The CPU can query the remaining amount of data in the internal SRAM through the STR_STAT.intm_left_cnt register. After the CPU reads the data, the STR_STAT.intm_left_cnt will decrease accordingly. At the same time, the way the internal SRAM stores data can be divided into four data storage formats: Flexible, Short Fixed, Long Fixed, and Mixed. Use STR_CTL_ism_sel[1:0] to select among the four formats, the specific explanations are as follows:

(1) Flexible: The data of each frame is seamlessly stored in the SRAM according to its volume.

(2) Short Fixed: A fixed 4 words are used to store a frame of data.

(3) Long Fixed: A fixed 18 words are used to store a frame of data.

(4) Mixed: frames use 4 words to store a frame of data, and frames use 18 words to store a frame of data. It should be noted that when the external storage mode is turned on, the internal SRAM will still be used for data caching, and the STR_CTL_ism_sel[1:0] can still be used to select the format of the data cached in the internal SRAM, but the external memory uses a fixed 18 words to store a frame of data.

39.2.4.2 External Storage Mode

To store the frame data received by RKCAN in external memory (DDR or System Memory), the STORE_CTL.stm needs to be configured as 1, and registers such as TXTHR, START_ADDR, and EXTM_SIZE need to be configured. RKCAN will first store the received frame data in the internal SRAM. When the amount of data received by RKCAN exceeds the threshold set by TXTHR, it will automatically write the data stored in the internal SRAM to the external memory through AHB Master, and update the WADDR register to the tail address of the part of the external memory that has been written with data. At the same time, it updates the status of the two empty/full flags STR_STAT.extm_empty and STR_STAT.extm_full. RKCAN sends an interrupt to the CPU. The CPU can determine the amount of data that can be read by querying the value of the WADDR register. After the CPU completes the frame data reading, it needs to write the latest CPU_RD_ADDR value into the RADDR register of RKCAN. RKCAN will calculate the empty/full status of the memory based on the values of the RADDR and WADDR registers. The CPU can query the amount of data in the external memory through STR_STAT.extm_left_cnt, and query the remaining amount of data in the internal SRAM through STR_STAT.intm_left_cnt.
This feature is currently only used for debugging. For specific application details, please consult Rockchip.

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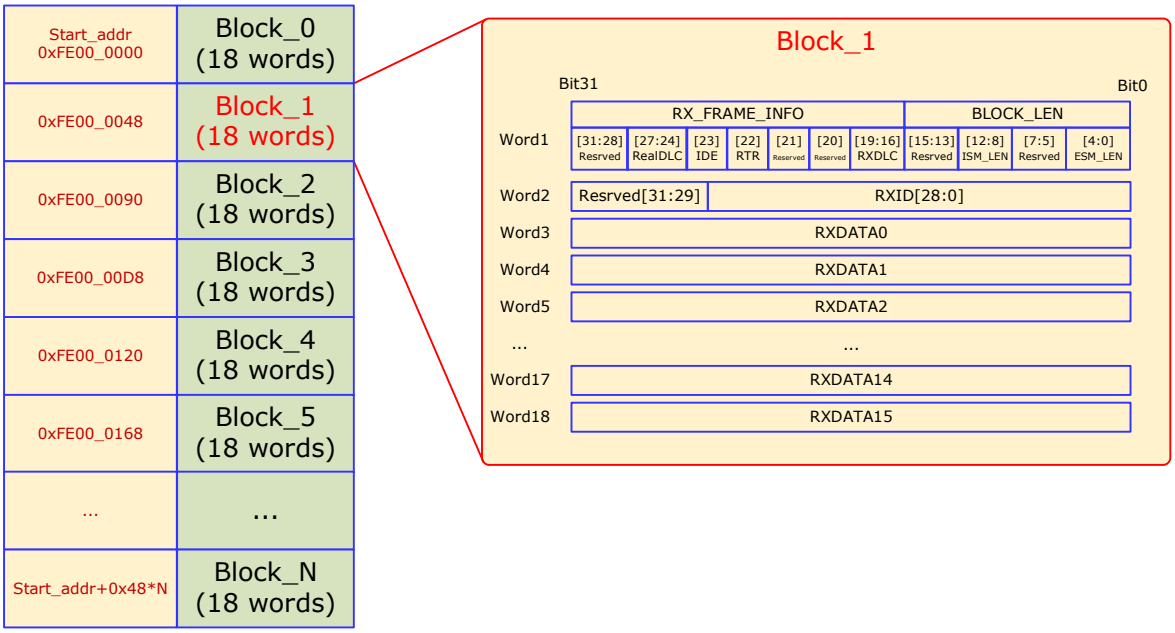

Fig. 39-8 Data storage format under external storage mode

39.2.4.3 ESM Timeout Mechanism

RKCAN also has a timeout mechanism to prevent the RKCAN receive buffer from overflowing when the CPU does not read data for a long time. The timeout threshold is configured through the BUF_TIMEOUT register. In internal storage mode, if the CPU does not read the data in the internal SRAM for a long time, a timeout interrupt will occur; in external storage mode, if the CPU does not update the value of the CPU_RD_ADDR register for a long time, a timeout interrupt will occur. The same interrupt flag is used in both modes.

39.2.5 ERROR PROCESS

There are five types of errors. Multiple errors can occur at the same time.

- **BIT ERROR**:
  A unit that is sending a bit on the bus also monitors the bus. A BIT ERROR has to be detected at that bit time, when the bit value that is monitored is different form the bit value that is sent. An exception is the sending of a 'recessive' bit during the stuffed bit stream of the ARBITRATION FIELD of during the ACK SLOT. Then no BIT ERROR occurs when a 'dominant' bit is monitored. A TRANSMITTER sending a PASSIVE ERROR FLAG and detecting a 'dominant' bit does not interpret this as a BIT ERROR.
- **BIT STUFF ERROR**:
  A STUFF ERROR has to be detected at the bit time of the 6th consecutive equal bit level in a message field that should be coded by the method of bit stuffing.
- **FORM ERROR**:
  A FORM ERROR has to be detected when a fixed-form bit field contains one or more illegal bits. (Exception is the detection of a dominant bit during the last bit of END OF FRAME by a RECEIVER, or the detection of a dominant bit during the last bit of ERROR DELIMITER or OVERLOAD DELIMITER by any node). When the value of a fixed STUFF-BIT in the RKCAN Long format CRC SEQUENCE is equal to its preceding bit, this shall also be detected as a FORM-ERROR.
- **ACK ERROR**:
  An ACK ERROR has to be detected by a transmitter whenever it does not monitor a 'dominant' bit during the ACK SLOT.
- **CRC ERROR**:
  The CRC sequence consists of the result of the CRC calculation by the transmitter. The receivers calculate the CRC in the same way as the transmitter. A CRC ERROR has to be detected, if the calculated result is not the same as that received in the

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CRC sequence.

39.3 Register Description

39.3.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

39.3.2 Registers Summary

Name	Offset	Size	Reset Value	Description
RKCAN_MODE	0x0000	W	0x00000000	Mode Configure Register
RKCAN_CMD	0x0004	W	0x00000000	Request Command Register
RKCAN_STATE	0x0008	W	0x00000000	Controller State Register
RKCAN_INT	0x000C	W	0x00000000	Interrupt State Register
RKCAN_INT_MASK	0x0010	W	0x00000000	Interrupt Mask Registers
RKCAN_NOMINAL_BITTIMING	0x0100	W	0x00000000	RKCAN Nominal Bit Timing Configure Register
RKCAN_LOOP_CNT	0x0110	W	0x00000000	Transmitter Delay Compensation Configure Register
RKCAN_DMA_CTRL	0x011C	W	0x00000000	DMA Mode Control Register
RKCAN_TIMESTAMP_CTRL	0x0130	W	0x00000007	Transmitter Delay Compensation Configure Register
RKCAN_TIMESTAMP	0x0134	W	0x00000001	Transmitter Delay Compensation Configure Register
RKCAN_TXFRAMEINFO	0x0200	W	0x00000000	RKCAN TX Frame Information Configuration Register
RKCAN_TXID	0x0204	W	0x00000000	RKCAN Transmit ID Register
RKCAN_TXDATA0	0x0208	W	0x00000000	RKCAN Transmit DATA0
RKCAN_TXDATA1	0x020C	W	0x00000000	RKCAN Transmit DATA1
RKCAN_TXDATA2	0x0210	W	0x00000000	RKCAN Transmit DATA2
RKCAN_TXDATA3	0x0214	W	0x00000000	RKCAN Transmit DATA3
RKCAN_TXDATA4	0x0218	W	0x00000000	RKCAN Transmit DATA4
RKCAN_TXDATA5	0x021C	W	0x00000000	RKCAN Transmit DATA5
RKCAN_TXDATA6	0x0220	W	0x00000000	RKCAN Transmit DATA6
RKCAN_TXDATA7	0x0224	W	0x00000000	RKCAN Transmit DATA7
RKCAN_TXDATA8	0x0228	W	0x00000000	RKCAN Transmit DATA8
RKCAN_TXDATA9	0x022C	W	0x00000000	RKCAN Transmit DATA9
RKCAN_TXDATA10	0x0230	W	0x00000000	RKCAN Transmit DATA10
RKCAN_TXDATA11	0x0234	W	0x00000000	RKCAN Transmit DATA11
RKCAN_TXDATA12	0x0238	W	0x00000000	RKCAN Transmit DATA12
RKCAN_TXDATA13	0x023C	W	0x00000000	RKCAN Transmit DATA13
RKCAN_TXDATA14	0x0240	W	0x00000000	RKCAN Transmit DATA14
RKCAN_TXDATA15	0x0244	W	0x00000000	RKCAN Transmit DATA15
RKCAN_BUF1_TXFRAMEINFO	0x0280	W	0x00000000	RKCAN TX Buffer1 Frame Information Configuration Register
RKCAN_BUF1_TXID	0x0284	W	0x00000000	RKCAN BUF1 Transmit ID Register
RKCAN_BUF1_TXDATA0	0x0288	W	0x00000000	RKCAN BUF1 Transmit DATA0
RKCAN_BUF1_TXDATA1	0x028C	W	0x00000000	RKCAN BUF1 Transmit DATA1
RKCAN_BUF1_TXDATA2	0x0290	W	0x00000000	RKCAN BUF1 Transmit DATA2
RKCAN_BUF1_TXDATA3	0x0294	W	0x00000000	RKCAN BUF1 Transmit DATA3
RKCAN_BUF1_TXDATA4	0x0298	W	0x00000000	RKCAN BUF1 Transmit DATA4
RKCAN_BUF1_TXDATA5	0x029C	W	0x00000000	RKCAN BUF1 Transmit DATA5
RKCAN_BUF1_TXDATA6	0x02A0	W	0x00000000	RKCAN BUF1 Transmit DATA6
RKCAN_BUF1_TXDATA7	0x02A4	W	0x00000000	RKCAN BUF1 Transmit DATA7

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Name	Offset	Size	Reset Value	Description
RKCAN_BUF1_TXDATA8	0x02A8	W	0x00000000	RKCAN BUF1 Transmit DATA8
RKCAN_BUF1_TXDATA9	0x02AC	W	0x00000000	RKCAN BUF1 Transmit DATA9
RKCAN_BUF1_TXDATA10	0x02B0	W	0x00000000	RKCAN BUF1 Transmit DATA10
RKCAN_BUF1_TXDATA11	0x02B4	W	0x00000000	RKCAN BUF1 Transmit DATA11
RKCAN_BUF1_TXDATA12	0x02B8	W	0x00000000	RKCAN BUF1 Transmit DATA12
RKCAN_BUF1_TXDATA13	0x02BC	W	0x00000000	RKCAN BUF1 Transmit DATA13
RKCAN_BUF1_TXDATA14	0x02C0	W	0x00000000	RKCAN BUF1 Transmit DATA14
RKCAN_BUF1_TXDATA15	0x02C4	W	0x00000000	RKCAN BUF1 Transmit DATA15
RKCAN_RXFRAMEINFO	0x0300	W	0x00000000	RKCAN RX Frame Information Configuration Register
RKCAN_RXID	0x0304	W	0x00000000	RKCAN Receive ID
RKCAN_RXTIMESTAMP	0x0308	W	0x00000000	RKCAN Receive Timestamp. Reserved
RKCAN_RXDATA0	0x030C	W	0x00000000	RKCAN Receive Data Reg0
RKCAN_RXDATA1	0x0310	W	0x00000000	RKCAN Receive Data Reg1
RKCAN_RXDATA2	0x0314	W	0x00000000	RKCAN Receive Data Reg2
RKCAN_RXDATA3	0x0318	W	0x00000000	RKCAN Receive Data Reg3
RKCAN_RXDATA4	0x031C	W	0x00000000	RKCAN Receive Data Reg4
RKCAN_RXDATA5	0x0320	W	0x00000000	RKCAN Receive Data Reg5
RKCAN_RXDATA6	0x0324	W	0x00000000	RKCAN Receive Data Reg6
RKCAN_RXDATA7	0x0328	W	0x00000000	RKCAN Receive Data Reg7
RKCAN_RXDATA8	0x032C	W	0x00000000	RKCAN Receive Data Reg8
RKCAN_RXDATA9	0x0330	W	0x00000000	RKCAN Receive Data Reg9
RKCAN_RXDATA10	0x0334	W	0x00000000	RKCAN Receive Data Reg10
RKCAN_RXDATA11	0x0338	W	0x00000000	RKCAN Receive Data Reg11
RKCAN_RXDATA12	0x033C	W	0x00000000	RKCAN Receive Data Reg12
RKCAN_RXDATA13	0x0340	W	0x00000000	RKCAN Receive Data Reg13
RKCAN_RXDATA14	0x0344	W	0x00000000	RKCAN Receive Data Reg14
RKCAN_RXDATA15	0x0348	W	0x00000000	RKCAN Receive Data Reg15
RKCAN_RX_STR_RDATA	0x0400	W	0x00000000	RX Storage Read Data
RKCAN_STR_CTL	0x0600	W	0x00000080	Storage Ctrl Register
RKCAN_STR_STATE	0x0604	W	0x00000000	Storage Ctrl Register
RKCAN_STR_TIMEOUT	0x0608	W	0x00002710	Storage Timeout Threshold Register
RKCAN_STR_WTM	0x060C	W	0x000168ED	Storage Water Mark Register
RKCAN_EXTM_START_ADDR	0x0610	W	0x00000000	External Memory Start Address
RKCAN_EXTM_SIZE	0x0614	W	0x000001F8	External Memory Size Register
RKCAN_EXTM_WADDR	0x0618	W	0x00000000	External Memory AHB Write Address
RKCAN_EXTM_RADDR	0x061C	W	0x00000000	External Memory Soft Read Address
RKCAN_EXTM_AHB_TXTHR	0x0620	W	0x00000000	AHB Master Transmit Threshold Level
RKCAN_EXTM_LEFT_CNT	0x0624	W	0x00000000	External Memory Left Counter
RKCAN_ATF0	0x0700	W	0x00000000	Acceptance Filter 0 Code Register
RKCAN_ATF1	0x0704	W	0x00000000	Acceptance Filter 1 Code Register
RKCAN_ATF2	0x0708	W	0x00000000	Acceptance Filter 2 Code Register
RKCAN_ATF3	0x070C	W	0x00000000	Acceptance Filter 3 Code Register
RKCAN_ATF4	0x0710	W	0x00000000	Acceptance Filter 4 Code Register
RKCAN_ATFM0	0x0714	W	0x1FFFFFFF	Acceptance Filter 0 Mask Register
RKCAN_ATFM1	0x0718	W	0x1FFFFFFF	Acceptance Filter 1 Mask Register
RKCAN_ATFM2	0x071C	W	0x1FFFFFFF	Acceptance Filter 2 Mask Register

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Name	Offset	Size	Reset Value	Description
RKCAN_ATFM3	0x0720	W	0x1FFFFFFF	Acceptance Filter 3 Mask Register
RKCAN_ATFM4	0x0724	W	0x1FFFFFFF	Acceptance Filter 4 Mask Register
RKCAN_ATF_DLC	0x0728	W	0x00000000	Acceptance DLC Filter Function
RKCAN_ATF_CTL	0x072C	W	0x00000000	Acceptance Filter Configure Register
RKCAN_SPACE_CTRL	0x0800	W	0x2A020100	Interframe Space Config Register
RKCAN_AUTO_RETX_CFG	0x0808	W	0x00000320	Configure Register for Auto Retransmission Function
RKCAN_AUTO_RETX_STATE0	0x080C	W	0x00000000	Auto Retransmission Status Register 0
RKCAN_AUTO_RETX_STATE1	0x0810	W	0x00000000	Auto Retransmission Status Register 0
RKCAN_OLF_CFG	0x0814	W	0x00000000	Overload Frame Configuration Register
RKCAN_RXINT_CTRL	0x0818	W	0x00000100	Multi Frame Interrupt(MFI) Configure Register
RKCAN_RXINT_TIMEOUT	0x081C	W	0x0000FFFF	MFI Timeout Threshold Register
RKCAN_WAVE_FILTER_CFG	0x0824	W	0x00000100	RKCAN Bus Wave Filter Configure
RKCAN_RBC_CFG	0x0828	W	0x000A120A	Recessive Bit Counter(RBC) Configure
RKCAN_TXCRC_CFG	0x082C	W	0x00000000	For Debug
RKCAN_BUSOFF_RCY_CFG	0x0830	W	0x00000000	Bus Off State Timer Recovery Mode Configuration Register
RKCAN_BUSOFF_RCY_THR	0x0834	W	0x00000000	
RKCAN_ACK_CFG	0x0840	W	0x00000000	
RKCAN_ERROR_CODE	0x0900	W	0x00000000	RX Error Code Register
RKCAN_ERROR_MASK	0x0904	W	0x00000000	Error Mask Register
RKCAN_RXCRC_VAL	0x0908	W	0x00000000	Recessive Bit Counter(RBC) Configure
RKCAN_CRC_CAL	0x090C	W	0x00000000	Recessive Bit Counter(RBC) Configure
RKCAN_RXERRORCNT	0x0910	W	0x00000000	Receive Error Counter Register
RKCAN_TXERRORCNT	0x0914	W	0x00000000	Transmit Error Counter Register
RKCAN_ARBIT_FAIL_STATE	0x0918	W	0x00000000	Arbiter Fail Code Register
RKCAN_RX_RXSRAM_RDATA	0x0C00	W	0x00000000	RX Storage Read Data
RKCAN_RTL_VERSION	0x0F0C	W	0xCFDBA0E3	RKCAN RTL version

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**- Double WORD (64 bits) access*

39.3.3 Detail Registers Description

RKCAN_MODE

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	RW	0x0	biterr_mode Error Frame Bit Error Handling Mode. 1'b0: When RKCAN is sending an error frame, if a bit_error is generated, the error frame is retransmitted. 1'b1: Don't resend.
17:16	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
15	RW	0x0	noack_mode When noack_mode is enabled, if the internal receive buffer of RKCAN is full and a new frame is received, RKCAN will no longer respond with an ACK. 1'b0: Disable; 1'b1: Enable.
14	RW	0x0	force_passive_err Force RKCAN into error passive station 1'b0: Disable; 1'b1: Enable.
13	RW	0x0	force_active_err Force RKCAN into error active station 1'b0: Disable; 1'b1: Enable.
12	RW	0x0	crcerr_pass_mode 1'b0: Send Passive Error when CRC Error detected; 1'b1: Not send Passive Error when CRC Error detected.
11	RW	0x0	crcerr_ack_mode 1'b0: Not send ACK when CRC Error detected; 1'b1: Send ACK when CRC Error detected.
10	RW	0x0	pass_err_mode 1'b0: PASSIVE Error Flag use recessive bits; 1'b1: PASSIVE Error Flag use dominant bits.
9:8	RO	0x0	reserved
7	RW	0x0	auto_bus_on Auto Bus On Enable. 1'b0: After the RKCAN has entered bus_off state, the software can start a bus_off_recovery sequence by resetting the work_mode to 0. 1'b1: Automatic reset TEC/REC to bus_on after 128 occurrence of 11 consecutive recessive bits have been monitored on the bus.
6	RO	0x0	reserved
5	RW	0x0	rxstx_mode Receive Self Transmit data mode. 1'b0: Disable; 1'b1: Enable. When the RKCAN sends data, it can also receive the data sent by itself.
4	RW	0x0	lback_mode Loopback Mode. 1'b0: Disable. 1'b1: Enable.
3	RW	0x0	silent_mode Silent Mode. 1'b0: Disable. 1'b1: Enable.
2	RW	0x0	self_test Reserved. Self check ACK slot when TX frame. Using ERROR_MASK[4]can achieve the same function When in self_test mode, the receiver does not need to return an ACK signal when receiving data. Therefore, no error ack will occur in self_test mode. When in 'lback_mode' or 'silent_mode', it needs to enable 'self_test' mode when sending frame.

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Bit	Attr	Reset Value	Description
1	RW	0x0	sleep_mode Sleep Mode This is the Sleep mode request bit. 1'b0: No such request. 1'b1: Request core to be in Sleep mode. This bit is cleared when the core wakes up from Sleep mode.
0	RW	0x0	work_mode Work Mode. 1'b0: Idle mode, RKCAN stop transmit and registers can be configured. 1'b1: Work mode, RKCAN enter the working mode, Receive/transmit data.

RKCAN_CMD

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	R/WSC	0x0	tx1_req Transmit request enable 1'b0: Disable 1'b1: Enable When 'tx1_req' is enable, the RKCAN buffer1 is in the transmit mode and cannot receive frames from other RKCANs. When the RKCAN buffer1 transmission frame complete, 'tx1_req' is automatically cleared to 0. Also, when RKCAN is set 'work_mode' to 'reset_mode', tx_req' is cleared to 0.
0	R/WSC	0x0	tx0_req Transmit request enable 1'b0: Disable 1'b1: Enable When 'tx0_req' is enable, the RKCAN buffer0 is in the transmit mode and cannot receive frames from other RKCANs. When the RKCAN buffer0 transmission frame complete, 'tx0_req' is automatically cleared to 0. Also, when RKCAN is set 'work_mode' to 'reset_mode', tx_req' is cleared to 0.

RKCAN_STATE

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RO	0x0	sleep_state Sleep state 1'b0: None 1'b1: RKCAN controller is in the sleep state
4	RO	0x0	bus_off_state Bus off state 1'b0: None 1'b1: Bus off state: When the error counter is incremented to 255, the RKCAN controller will enter the bus off state, generate an error warning interrupt and enter reset mode, waiting for the CPU to restart. (rx/tx_err_cnt >=32'd255)

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Bit	Attr	Reset Value	Description
3	RO	0x0	error_warning_state Error warning state 1'b0: None 1'b1: Error state: At least one error counter has reached the error warning threshold (rx/tx_err_cnt >=32'd96)
2	RO	0x0	tx_period Transmit state 1'b0: Not in transmit state 1'b1: RKCAN controller is in the transmit state
1	RO	0x0	rx_period Receive state 1'b0: Not in receive state 1'b1: RKCAN controller is in the receive state
0	RO	0x0	tx_buffer_full Transmit buffer full flag bit 1'b0: Not full 1'b1: TX buffer is full. There is data in buffer waiting to be sent or being sent.

RKCAN_INT

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	W1C	0x0	tbc_overflow_int Timestamp Base Counter Overflow Interrupt 1'b0: None 1'b1: Overflow Write 1 then clear.
19	W1C	0x0	busoff_rcy_int BusOff Timer Recovery Interrupt 1'b0: None 1'b1: BusOff timer recovery Write 1 then clear.
18	W1C	0x0	esm_wtm_int External Storage watermark Interrupt 1'b0: None 1'b1: The data in external storage reaches the watermark Write 1 then clear.
17	W1C	0x0	ism_wtm_int Internal Stotage watermark Interrupt 1'b0: None 1'b1: The data in internal storage reaches the watermark Write 1 then clear.
16	W1C	0x0	busint_int Enter Bus Integration Interrupt 1'b0: None 1'b1: Indicates RKCAN enter the bus integrationstate. Write 1 then clear.
15	W1C	0x0	rxstr_timeout_int RX Storage Timeout Interrupt 1'b0: None 1'b1: Indicates that data remain in rx stroage timeout. Write 1 then clear.
14	W1C	0x0	mfi_timeout_int Multi Frame Interrupt(MFI) Mode Timeout Interrupt

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Bit	Attr	Reset Value	Description
13	W1C	0x0	mfi_int Multi Frame Interrupt(MFI)
12	W1C	0x0	auto_retx_fail_int Automatic Transmit Failure Interrupt
11	W1C	0x0	wakeup_int Wakeup Interrupt 1'b0: None 1'b1: Indicates that the core entered Normal mode from Sleep mode. Write 1 then clear.
10	W1C	0x0	bus_off_recovery_int Bus off Recover Interrupt 1'b0: None 1'b1: Indicates that the core is recovered from Bus-off mode. Write 1 then clear.
9	W1C	0x0	bus_off_int Bus Off Interrupt 1'b0: None 1'b1: Indicates that the RKCAN core entered Bus-off mode. Write 1 then clear.
8	W1C	0x0	rxstr_overflow_int RX Storage Overflow Interrupt. 1'b0: None 1'b1: Indicates that a message has been lost. This condition occurs when a new message with ID matching to Receive Storage is received and the Receive Storage is full.
7	W1C	0x0	rxstr_full_int RX Storage full Interrupt. 1'b0: None 1'b1: Indicates that RX Storage is full based on watermark setting.
6	W1C	0x0	error_int Bus Error Interrupt 1'b0: None 1'b1: RKCAN bus error interrupt. This interrupt is generated when a bus error is detected. Error details can refer to the ERROR_CODE register. Write 1 then clear.
5	W1C	0x0	tx_arbit_fail_int Transmit Arbitration loss Interrupt 1'b0: None 1'b1: Arbitration loss interrupt. This interrupt is generated when the loss of arbitration is turned into a receiver. Write 1 then clear.
4	W1C	0x0	passive_error_int Passive Error Interrupt 1'b0: None 1'b1: Passive error interrupt. This interrupt is generated when the controller enters an error passive state (at least one error counter reaches 127) or returns from the error passive state to the error active state. Write 1 then clear.
3	W1C	0x0	overload_int Overload Frame Interrupt 1'b0: None 1'b1: RKCAN bus overload interrupt. This interrupt is generated when a overload frame is generated.

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Bit	Attr	Reset Value	Description
2	W1C	0x0	error_warning_int Error warning interrupt 1'b0: None 1'b1: Error_warning_int. This interrupt is generated when the error_warning_state bits change. Write 1 then clear.
1	W1C	0x0	tx_finish_int Transmit finish interrupt 1'b0: None 1'b1: Transmit finish interrupt. RKCAN controller sends the message. Write 1 then clear.
0	W1C	0x0	rx_finish_int Receive Finish Interrupt 1'b0: None 1'b1: Receive finish int. RKCAN controller has received the message and the rx_buffer is full. Write 1 then clear.

RKCAN_INT_MASK

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20	RW	0x0	tbc_overflow_int_mask 1'b0: Unmasked 1'b1: Masked
19	RW	0x0	busoff_rcy_int_mask 1'b0: Unmasked 1'b1: Masked
18	RW	0x0	esm_wtm_int_mask 1'b0: Unmasked 1'b1: Masked
17	RW	0x0	ism_wtm_int_mask 1'b0: Unmasked 1'b1: Masked
16	RW	0x0	busint_int_mask 1'b0: Unmasked 1'b1: Masked
15	RW	0x0	rxstr_timeout_int_mask 1'b0: Unmasked 1'b1: Masked
14	RW	0x0	mfi_timeout_int_mask 1'b0: Unmasked 1'b1: Masked
13	RW	0x0	mfi_int_mask 1'b0: Unmasked 1'b1: Masked
12	RW	0x0	auto_retx_fail_int_mask 1'b0: Unmasked 1'b1: Masked
11	RW	0x0	wakeup_int_mask 1'b0: Unmasked 1'b1: Masked
10	RW	0x0	bus_off_recovery_int_mask 1'b0: Unmasked 1'b1: Masked

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Bit	Attr	Reset Value	Description
9	RW	0x0	bus_off_int_mask 1'b0: Unmasked 1'b1: Masked
8	RW	0x0	rxstr_overflow_int_mask 1'b0: Unmasked 1'b1: Masked
7	RW	0x0	rxstr_full_int_mask 1'b0: Unmasked 1'b1: Masked
6	RW	0x0	error_int_mask 1'b0: Unmasked 1'b1: Masked
5	RW	0x0	tx_arbit_fail_int_mask 1'b0: Unmasked 1'b1: Masked
4	RW	0x0	passive_error_int_mask 1'b0: Unmasked 1'b1: Masked
3	RW	0x0	overload_int_mask 1'b0: Unmasked 1'b1: Masked
2	RW	0x0	error_warning_int_mask 1'b0: Unmasked 1'b1: Masked
1	RW	0x0	tx_finish_int_mask 1'b0: Unmasked 1'b1: Masked
0	RW	0x0	rx_finish_int_mask 1'b0: Unmasked 1'b1: Masked

RKCAN_NOMINAL_BITTIMING

Address: **Operational Base** + offset (0x0100)

Bit	Attr	Reset Value	Description
31	RW	0x0	sample_mode RKCAN controller sampling mode configuration register. When enabling triple sampling, it is necessary to configure the positions of two additional sampling points using the BRS_CFG[30:5] register. 1'b0: Single sample mode 1'b1: Three sample mode
30:24	RW	0x00	sjw SJW: Resynchronization Jump Width Each unit has a synchronization error due to a clock frequency deviation or a transmission delay. SJW is to compensate for the maximum value of this error.
23:16	RW	0x00	brq brp: system prescale coefficient Tsclk = 2 x Tclk x (brp + 1).
15	RO	0x0	reserved
14:8	RW	0x00	tseg2 Phase buffer segment 2 Tphase_seg2 = Tsclk x (tseg2 + 1)

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	tseg1 Phase buffer segment 1 Tphase_seg1 = Tsclk x (tseg1 + 1)

RKCAN_LOOP_CNT

Address: **Operational Base** + offset (0x0110)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	loop_delay_cnt Loop Delay Counter

RKCAN_DMA_CTRL

Address: **Operational Base** + offset (0x011C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	dma_rx_en DMA receive request enable 1'b0: Disable 1'b1: Enable When dma_rx_mode is enable, the RKCAN is in the DMA receive mode. Also, when RKCAN is set work_mode to reset_mode, rx_req is clear.
8:0	RW	0x000	dma_thr DMA transfer start threshold. Unit:word.

RKCAN_TIMESTAMP_CTRL

Address: **Operational Base** + offset (0x0130)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:4	RW	0x00	tbc_prescale Time Base Counter Prescaler bit 0 = TBC increments every 1 clock 1 = TBC increments every 2 clock ... 31 = TBC increments every 32 clock
3	RO	0x0	reserved
2	RW	0x1	tbc_clr Reset TBC.
1	RW	0x1	timestamp_mode Timestampe Mode Enable 1'b0: Disable. 1'b1: Enable.
0	RW	0x1	timestamp_cnt_en Time Base Counter (TBC) Enable 1'b0: Stop TBC. 1'b1: Enables TBC.

RKCAN_TIMESTAMP

Address: **Operational Base** + offset (0x0134)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000001	timestamp_cnt_val TBC Value.

RKCAN_TXFRAMEINFO

Address: **Operational Base** + offset (0x0200)

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Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	txframe_format 1'b0: Standard frame 1'b1: Extended frame
6	RW	0x0	tx_rtr 1'b0: Data frame 1'b1: Remote frame
5:4	RO	0x0	reserved
3:0	RW	0x0	txdata_length Transmit data length configure register. (unit:byte) 4'b0000: 0byte 4'b0001: 1byte 4'b0010: 2byte 4'b0011: 3byte 4'b0100: 4byte 4'b0101: 5byte 4'b0110: 6byte 4'b0111: 7byte 4'b1000: 8byte 4'b1001:12byte 4'b1010:16byte 4'b1011:20byte 4'b1100:24byte 4'b1101:32byte 4'b1110:48byte 4'b1111:64byte

RKCAN_TXID

Address: **Operational Base** + offset (0x0204)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	tx_id can_tx_id[28:0]

RKCAN_TXDATA0

Address: **Operational Base** + offset (0x0208)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data0 tx_data0[31:0]

RKCAN_TXDATA1

Address: **Operational Base** + offset (0x020C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data1 tx_data1[31:0]

RKCAN_TXDATA2

Address: **Operational Base** + offset (0x0210)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data2 tx_data2[31:0]

RKCAN_TXDATA3

Address: **Operational Base** + offset (0x0214)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data3 tx_data3[31:0]

RKCAN_TXDATA4

Address: **Operational Base** + offset (0x0218)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data4 tx_data4[31:0]

RKCAN_TXDATA5

Address: **Operational Base** + offset (0x021C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data5 tx_data5[31:0]

RKCAN_TXDATA6

Address: **Operational Base** + offset (0x0220)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data6 tx_data6[31:0]

RKCAN_TXDATA7

Address: **Operational Base** + offset (0x0224)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data7 tx_data7[31:0]

RKCAN_TXDATA8

Address: **Operational Base** + offset (0x0228)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data8 tx_data8[31:0]

RKCAN_TXDATA9

Address: **Operational Base** + offset (0x022C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data9 tx_data9[31:0]

RKCAN_TXDATA10

Address: **Operational Base** + offset (0x0230)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data10 tx_data10[31:0]

RKCAN_TXDATA11

Address: **Operational Base** + offset (0x0234)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data11 tx_data11[31:0]

RKCAN_TXDATA12

Address: **Operational Base** + offset (0x0238)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data12 tx_data12[31:0]

RKCAN_TXDATA13

Address: **Operational Base** + offset (0x023C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data13 tx_data13[31:0]

RKCAN_TXDATA14

Address: **Operational Base** + offset (0x0240)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data14 tx_data14[31:0]

RKCAN_TXDATA15

Address: **Operational Base** + offset (0x0244)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data15 tx_data15[31:0]

RKCAN_BUF1_TXFRAMEINFO

Address: **Operational Base** + offset (0x0280)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	txframe_format 1'b0: Standard frame 1'b1: Extended frame
6	RW	0x0	tx_rtr 1'b0: Data frame 1'b1: Remote frame
5:4	RO	0x0	reserved
3:0	RW	0x0	txdata_length Transmit data length configure register. (unit:byte) 4'b0000: 0byte 4'b0001: 1byte 4'b0010: 2byte 4'b0011: 3byte 4'b0100: 4byte 4'b0101: 5byte 4'b0110: 6byte 4'b0111: 7byte 4'b1000: 8byte 4'b1001:12byte 4'b1010:16byte 4'b1011:20byte 4'b1100:24byte 4'b1101:32byte 4'b1110:48byte 4'b1111:64byte

RKCAN_BUF1_TXID

Address: **Operational Base** + offset (0x0284)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28:0	RW	0x00000000	tx_id can_tx_id[28:0]

RKCAN_BUF1_TXDATA0
Address: **Operational Base** + offset (0x0288)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data0 tx_data0[31:0]

RKCAN_BUF1_TXDATA1
Address: **Operational Base** + offset (0x028C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data1 tx_data1[31:0]

RKCAN_BUF1_TXDATA2
Address: **Operational Base** + offset (0x0290)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data2 tx_data2[31:0]

RKCAN_BUF1_TXDATA3
Address: **Operational Base** + offset (0x0294)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data3 tx_data3[31:0]

RKCAN_BUF1_TXDATA4
Address: **Operational Base** + offset (0x0298)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data4 tx_data4[31:0]

RKCAN_BUF1_TXDATA5
Address: **Operational Base** + offset (0x029C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data5 tx_data5[31:0]

RKCAN_BUF1_TXDATA6
Address: **Operational Base** + offset (0x02A0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data6 tx_data6[31:0]

RKCAN_BUF1_TXDATA7
Address: **Operational Base** + offset (0x02A4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data7 tx_data7[31:0]

RKCAN_BUF1_TXDATA8
Address: **Operational Base** + offset (0x02A8)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data8 tx_data8[31:0]

RKCAN_BUF1_TXDATA9

Address: **Operational Base** + offset (0x02AC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data9 tx_data9[31:0]

RKCAN_BUF1_TXDATA10

Address: **Operational Base** + offset (0x02B0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data10 tx_data10[31:0]

RKCAN_BUF1_TXDATA11

Address: **Operational Base** + offset (0x02B4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data11 tx_data11[31:0]

RKCAN_BUF1_TXDATA12

Address: **Operational Base** + offset (0x02B8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data12 tx_data12[31:0]

RKCAN_BUF1_TXDATA13

Address: **Operational Base** + offset (0x02BC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data13 tx_data13[31:0]

RKCAN_BUF1_TXDATA14

Address: **Operational Base** + offset (0x02C0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data14 tx_data14[31:0]

RKCAN_BUF1_TXDATA15

Address: **Operational Base** + offset (0x02C4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	tx_data15 tx_data15[31:0]

RKCAN_RXFRAMEINFO

Address: **Operational Base** + offset (0x0300)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RO	0x0	rx_dlc Received DLC bit value.
7	RO	0x0	rxframe_format 1'b0: Standard frame 1'b1: Extended frame

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Bit	Attr	Reset Value	Description
6	RO	0x0	rx_rtr 1'b0: Data frame 1'b1: Remote frame
5:4	RO	0x0	reserved
3:0	RO	0x0	rxdata_length Transmit data length configure register. (unit:byte) 4'b0000: 0byte 4'b0001: 1byte 4'b0010: 2byte 4'b0011: 3byte 4'b0100: 4byte 4'b0101: 5byte 4'b0110: 6byte 4'b0111: 7byte 4'b1000: 8byte 4'b1001:12byte 4'b1010:16byte 4'b1011:20byte 4'b1100:24byte 4'b1101:32byte 4'b1110:48byte 4'b1111:64byte

RKCAN_RXID

Address: **Operational Base** + offset (0x0304)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RO	0x00000000	rx_id can_rx_id[28:0]

RKCAN_RXTIMESTAMP

Address: **Operational Base** + offset (0x0308)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	timestamp Reserved

RKCAN_RXDATA0

Address: **Operational Base** + offset (0x030C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data0 rx_data0[31:0] This register refresh after receiving the next frame.

RKCAN_RXDATA1

Address: **Operational Base** + offset (0x0310)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data1 rx_data1[31:0] This register refresh after receiving the next frame.

RKCAN_RXDATA2

Address: **Operational Base** + offset (0x0314)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data2 rx_data2[31:0] This register refresh after receiving the next frame.

RKCAN_RXDATA3

Address: **Operational Base** + offset (0x0318)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data3 rx_data3[31:0] This register refresh after receiving the next frame.

RKCAN_RXDATA4

Address: **Operational Base** + offset (0x031C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data4 rx_data4[31:0] This register refresh after receiving the next frame.

RKCAN_RXDATA5

Address: **Operational Base** + offset (0x0320)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data5 rx_data5[31:0] This register refresh after receiving the next frame.

RKCAN_RXDATA6

Address: **Operational Base** + offset (0x0324)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data6 rx_data6[31:0] This register refresh after receiving the next frame.

RKCAN_RXDATA7

Address: **Operational Base** + offset (0x0328)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data7 rx_data7[31:0] This register refresh after receiving the next frame.

RKCAN_RXDATA8

Address: **Operational Base** + offset (0x032C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data8 rx_data8[31:0] This register refresh after receiving the next frame.

RKCAN_RXDATA9

Address: **Operational Base** + offset (0x0330)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data9 rx_data9[31:0] This register refresh after receiving the next frame.

RKCAN_RXDATA10

Address: **Operational Base** + offset (0x0334)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data10 rx_data10[31:0] This register refresh after receiving the next frame.

RKCAN_RXDATA11

Address: **Operational Base** + offset (0x0338)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data11 rx_data11[31:0] This register refresh after receiving the next frame.

RKCAN_RXDATA12

Address: **Operational Base** + offset (0x033C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data12 rx_data12[31:0] This register refresh after receiving the next frame.

RKCAN_RXDATA13

Address: **Operational Base** + offset (0x0340)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data13 rx_data13[31:0] This register refresh after receiving the next frame.

RKCAN_RXDATA14

Address: **Operational Base** + offset (0x0344)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data14 rx_data14[31:0] This register refresh after receiving the next frame.

RKCAN_RXDATA15

Address: **Operational Base** + offset (0x0348)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_data15 rx_data15[31:0] This register refresh after receiving the next frame.

RKCAN_RX_STR_RDATA

Address: **Operational Base** + offset (0x0400)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_str_rdata RX strorage read data value

RKCAN_STR_CTL

Address: **Operational Base** + offset (0x0600)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	str_timeout_mode RX storage not read timeout threshold Mode. 1'b0: Disable; 1'b1: Enable.

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Bit	Attr	Reset Value	Description
7:6	RW	0x2	esm_sel External Storage Mode(ESM) Data Format Select 2'b00: Flexible; 2'b01: Short Fixed; 2'b10: Long Fixed; 2'b11: Mixed.
5	RO	0x0	reserved
4	RW	0x0	srst RX Storage Soft Reset Bit 1'b0: Disable 1'b1: Enable
3:2	RW	0x0	ism_sel Internal Storage Mode(ISM) Data Format Select 2'b00: Flexible; cover_mode must disable. 2'b01: Short Fixed; 2'b10: Long Fixed; 2'b11: Mixed. cover_mode must disable.
1	RW	0x0	stm Storage Mode 1'b0: Internal Storage Mode; 1'b1: External Storage Mode. RKCAN can use AHB Master interface to write the received frame data to External Memory(DDR or System Memory).
0	RW	0x0	buff_mode_en RX Buffer Mode Enable 1'b0: Disable. 1'b1: Enable, RKCAN only a set of RXDATA0~15 registers used as buffers to store received data, instead of internal SRAM or external memory.

RKCAN_STR_STATE

Address: **Operational Base** + offset (0x0604)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:17	RO	0x000	intm_frame_cnt Remaining frame count in RXFIFO. Unit: Frame. Only Support when cover_mode disable.
16:8	RO	0x000	intm_left_cnt The amount of data remaining in the Internal SRAM. Unit:Word.
7:4	RO	0x0	reserved
3	RO	0x0	extm_full External Memory Full Flag 1'b0: Not Full; 1'b1: Full;
2	RO	0x0	extm_empty External Memory Empty Flag 1'b0: Not Empty; 1'b1: Empty
1	RO	0x0	intm_full Internal Memory Full Flag 1'b0: Not Full; 1'b1: Full;

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Bit	Attr	Reset Value	Description
0	RO	0x0	intm_empty Internal Memory Empty Flag 1'b0: Not Empty; 1'b1: Empty

RKCAN_STR_TIMEOUT

Address: **Operational Base** + offset (0x0608)

Bit	Attr	Reset Value	Description
31:0	RW	0x00002710	str_timeout_thr RX storage not read timeout threshold value Internal Storage Mode: External Storage Mode:

RKCAN_STR_WTM

Address: **Operational Base** + offset (0x060C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:9	RW	0x0000b4	esm_watermark External Storage Watermark Register. Unit:Word.
8:0	RW	0x0ed	ism_watermark Internal Storage Watermark Register. The configurable range is from 0 to 256. Unit:Word. In ISM mode, when the amount of valid data in the RXFIFO is greater than the threshold set by ism_watermark, RKCAN will generate an ism_wtm_int interrupt.

RKCAN_EXTM_START_ADDR

Address: **Operational Base** + offset (0x0610)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	start_addr External Memory Start Address Used as the Start Address of AHB master output rxdata.

RKCAN_EXTM_SIZE

Address: **Operational Base** + offset (0x0614)

Bit	Attr	Reset Value	Description
31:0	RW	0x000001f8	ext_mem_size Configuration size of external storage space. Unit:Word. Must be power of 18.

RKCAN_EXTM_WADDR

Address: **Operational Base** + offset (0x0618)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	can_waddr RKCAN AHB Write Address

RKCAN_EXTM_RADDR

Address: **Operational Base** + offset (0x061C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cpu_raddr CPU Read Address

RKCAN_EXTM_AHB_TXTHR

Address: **Operational Base** + offset (0x0620)

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Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x000	ahb_txthr(V2) When the number of RXFIFO entries is greater than or equal to this value, the RKCAN will automatically transfer the data in the RXFIFO to the external via the AHB Master interface. The value ranges is 0~511.(Unit:byte)

RKCAN_EXTM_LEFT_CNT

Address: **Operational Base** + offset (0x0624)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:0	RO	0x000000	extm_left_cnt The amount of remaining data in external storage.(Unit:Word)

RKCAN_ATF0

Address: **Operational Base** + offset (0x0700)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	RTR_EN RTR Bit Filter Enable 1'b0: Disable. 1'b1: Enable.
29	RW	0x0	RTR RTR part of the Acceptance Filter 0. 1'b0: Data Frame; 1'b1: Remote Frame.
28:0	RW	0x00000000	ID ID part of the Acceptance Filter 0.

RKCAN_ATF1

Address: **Operational Base** + offset (0x0704)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	RTR_EN RTR Bit Filter Enable 1'b0: Disable. 1'b1: Enable.
29	RW	0x0	RTR RTR part of the Acceptance Filter 1. 1'b0: Data Frame; 1'b1: Remote Frame.
28:0	RW	0x00000000	ID ID part of the Acceptance Filter 0.

RKCAN_ATF2

Address: **Operational Base** + offset (0x0708)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	RTR_EN RTR Bit Filter Enable 1'b0: Disable. 1'b1: Enable.

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Bit	Attr	Reset Value	Description
29	RW	0x0	RTR RTR part of the Acceptance Filter 2. 1'b0: Data Frame; 1'b1: Remote Frame.
28:0	RW	0x00000000	ID ID part of the Acceptance Filter 0.

RKCAN_ATF3

Address: **Operational Base** + offset (0x070C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	RTR_EN RTR Bit Filter Enable 1'b0: Disable. 1'b1: Enable.
29	RW	0x0	RTR RTR part of the Acceptance Filter 3. 1'b0: Data Frame; 1'b1: Remote Frame.
28:0	RW	0x00000000	ID ID part of the Acceptance Filter 0.

RKCAN_ATF4

Address: **Operational Base** + offset (0x0710)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	RTR_EN RTR Bit Filter Enable 1'b0: Disable. 1'b1: Enable.
29	RW	0x0	RTR RTR part of the Acceptance Filter 4. 1'b0: Data Frame; 1'b1: Remote Frame.
28:0	RW	0x00000000	ID ID part of the Acceptance Filter 0.

RKCAN_ATFM0

Address: **Operational Base** + offset (0x0714)

Bit	Attr	Reset Value	Description
31	RW	0x0	MASK 1'b0: Mask Mode, Register ATF0M[30:0] is used to configure the mask filed of each rule for ATF0; 1'b1: List Mode, Register ATF0M[30:0] is used as acceptance filter ATF5;
30	RW	0x0	RTR_EN RTR Bit Filter Enable 1'b0: Disable. 1'b1: Enable.
29	RW	0x0	RTR RTR part of the Acceptance Filter M0. 1'b0: Data Frame; 1'b1: Remote Frame.

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Bit	Attr	Reset Value	Description
28:0	RW	0x1fffffff	ID when ATF0M.MASK is 1'b0, ATF0M.ID is ID part of the Acceptance Filter; when ATF0M.MASK is 1'b1, ATF0M.ID is ID Mask Field for ATF0.ID.

RKCAN_ATFM1

Address: **Operational Base** + offset (0x0718)

Bit	Attr	Reset Value	Description
31	RW	0x0	MASK 1'b0: Mask Mode, Register ATF1M[30:0] is used to configure the mask filed of each rule for ATF1; 1'b1: List Mode, Register ATF1M[30:0] is used as acceptance filter ATF6;
30	RW	0x0	RTR_EN RTR Bit Filter Enable 1'b0: Disable. 1'b1: Enable.
29	RW	0x0	RTR RTR part of the Acceptance Filter M1. 1'b0: Data Frame; 1'b1: Remote Frame.
28:0	RW	0x1fffffff	ID when ATF0M.MASK is 1'b0, ATF0M.ID is ID part of the Acceptance Filter; when ATF0M.MASK is 1'b1, ATF0M.ID is ID Mask Field for ATF0.ID.

RKCAN_ATFM2

Address: **Operational Base** + offset (0x071C)

Bit	Attr	Reset Value	Description
31	RW	0x0	MASK 1'b0: Mask Mode, Register ATF2M[30:0] is used to configure the mask filed of each rule for ATF2; 1'b1: List Mode, Register ATF2M[30:0] is used as acceptance filter ATF7;
30	RW	0x0	RTR_EN RTR Bit Filter Enable 1'b0: Disable. 1'b1: Enable.
29	RW	0x0	RTR RTR part of the Acceptance Filter M2. 1'b0: Data Frame; 1'b1: Remote Frame.
28:0	RW	0x1fffffff	ID when ATF0M.MASK is 1'b0, ATF0M.ID is ID part of the Acceptance Filter; when ATF0M.MASK is 1'b1, ATF0M.ID is ID Mask Field for ATF0.ID.

RKCAN_ATFM3

Address: **Operational Base** + offset (0x0720)

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Bit	Attr	Reset Value	Description
31	RW	0x0	MASK 1'b0: Mask Mode, Register ATF3M[30:0] is used to configure the mask filed of each rule for ATF3; 1'b1: List Mode, Register ATF3M[30:0] is used as acceptance filter ATF8;
30	RW	0x0	RTR_EN RTR Bit Filter Enable 1'b0: Disable. 1'b1: Enable.
29	RW	0x0	RTR RTR part of the Acceptance Filter M3. 1'b0: Data Frame; 1'b1: Remote Frame.
28:0	RW	0x1fffffff	ID when ATF0M.MASK is 1'b0, ATF0M.ID is ID part of the Acceptance Filter; when ATF0M.MASK is 1'b1, ATF0M.ID is ID Mask Field for ATF0.ID.

RKCAN_ATFM4

Address: **Operational Base** + offset (0x0724)

Bit	Attr	Reset Value	Description
31	RW	0x0	MASK 1'b0: Mask Mode, Register ATF4M[30:0] is used to configure the mask filed of each rule for ATF4; 1'b1: List Mode, Register ATF4M[30:0] is used as acceptance filter ATF9;
30	RW	0x0	RTR_EN RTR Bit Filter Enable 1'b0: Disable. 1'b1: Enable.
29	RW	0x0	RTR RTR part of the Acceptance Filter M4. 1'b0: Data Frame; 1'b1: Remote Frame.
28:0	RW	0x1fffffff	ID when ATF0M.MASK is 1'b0, ATF0M.ID is ID part of the Acceptance Filter; when ATF0M.MASK is 1'b1, ATF0M.ID is ID Mask Field for ATF0.ID.

RKCAN_ATF_DLC

Address: **Operational Base** + offset (0x0728)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	atf_dlc_mode 1'b0: Over Mode, DLC filter process is only passed if the DLC value of the message accepted is equal to or higher than the value of ATF_DLC.atf_dlc; 1'b1: Less Mode, DLC filter process is only passed if the DLC value of the message accepted is equal to or less than the value of ATF_DLC.atf_dlc.

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Bit	Attr	Reset Value	Description
4	RW	0x0	atf_dlc_en DLC Filter Enable 1'b0: Disable; 1'b1: Enable.
3:0	RW	0x0	atf_dlc Configure DLC value of received message.

RKCAN_ATF_CTL

Address: **Operational Base** + offset (0x072C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	atf9_en Acceptance Filter 9 Disable 1'b0: Disable; 1'b1: Enable.
8	RW	0x0	atf8_en Acceptance Filter 8 Disable 1'b0: Disable; 1'b1: Enable.
7	RW	0x0	atf7_en Acceptance Filter 7 Disable 1'b0: Disable; 1'b1: Enable.
6	RW	0x0	atf6_en Acceptance Filter 6 Disable 1'b0: Disable; 1'b1: Enable.
5	RW	0x0	atf5_en Acceptance Filter 5 Disable 1'b0: Disable; 1'b1: Enable.
4	RW	0x0	atf4_en Acceptance Filter 4 Disable 1'b0: Disable; 1'b1: Enable.
3	RW	0x0	atf3_en Acceptance Filter 3 Disable 1'b0: Disable; 1'b1: Enable.
2	RW	0x0	atf2_en Acceptance Filter 2 Disable 1'b0: Disable; 1'b1: Enable.
1	RW	0x0	atf1_en Acceptance Filter 1 Disable 1'b0: Disable; 1'b1: Enable.
0	RW	0x0	atf0_en Acceptance Filter 0 Enable 1'b0: Disable; 1'b1: Enable.

RKCAN_SPACE_CTRL

Address: **Operational Base** + offset (0x0800)

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Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x1	ack_to_acklim_set
28	RW	0x0	space_intermission_mode
27:24	RW	0xa	space_intermission_len
23:16	RW	0x02	space_to_sof
15:8	RW	0x01	space_to_overload_set1
7:0	RW	0x00	space_to_overload_set0

RKCAN_AUTO_RETX_CFG

Address: **Operational Base** + offset (0x0808)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19	RW	0x0	retx_cnt_self_clr retx_cnt clear bit.
18:3	RO	0x0064	retx_time_limit Auto Retx Time Threshold.
2	RW	0x0	auto_retx_cnt_clr Set to 1 to clear the Auto Retransmission Conter(auto_retx_cnt)
1	RW	0x0	retx_limit_en 1'b0: Diable retx_time_limit; Keep resending until the transmission is successful; 1'b1: Enable retx_time_limit; Stop retransmission when the number of retransmissions reaches the threshold;
0	RW	0x0	auto_retx_mode Auto Retransmission Mode 1'b0: Disable; 1'b1: Enable.

RKCAN_AUTO_RETX_STATE0

Address: **Operational Base** + offset (0x080C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	noack_cnt No ACK Counter
15:0	RO	0x0000	auto_retx_cnt Automatic Retransmission Counter

RKCAN_AUTO_RETX_STATE1

Address: **Operational Base** + offset (0x0810)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	txerr_cnt TX Error Counter
15:0	RO	0x0000	arbit_fail_cnt Arbit Fail Counter

RKCAN_OLF_CFG

Address: **Operational Base** + offset (0x0814)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	tx_wait_thr Used to configure the number of bits for transmission wait.
15:13	RO	0x0	reserved
12	RO	0x0	tx_wait_clr tx_wait_cnt Clear.

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Bit	Attr	Reset Value	Description
11	RO	0x0	tx_wait_mode Transmit wait mode. 1'b0: Immediate transmission; 1'b1: Wait for "tx_wait_thr" bits before transmitting.
10	RW	0x0	ovd_time 1'b0: Transmit one overload frame at a time; 1'b1: Continuously transmit two overload frame at a time.
9	RW	0x0	auto_ovd_mode Auto transmit Overload frame mode 1'b0: Disable; 1'b1: Enable;
8:0	RW	0x000	ovd_tx_thr Overload Frame Transmit Threshold Level. The configurable range is from 0 to 256. Unit:Word. When the remaining space of the RXFIFO is less than the threshold set by ovd_tx_thr, RKCAN will automatically send an overload frame.

RKCAN_RXINT_CTRL

Address: **Operational Base** + offset (0x0818)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	mfi_timeout_mode Multi Frame Interrupt(MFI) Timeout Mode 1'b0: Disable; 1'b1: Enable.
16	RW	0x0	mfi_mode Multi Frame Interrupt(MFI) Mode 1'b0: Generate an interrupt when a frame is received; 1'b1: Generate an interrupt when N frames are received, N is configured by RXINT.rxint_num.
15:0	RW	0x0100	rxint_num Used to configure mulit frame interrupt mode

RKCAN_RXINT_TIMEOUT

Address: **Operational Base** + offset (0x081C)

Bit	Attr	Reset Value	Description
31:0	RW	0x0000ffff	threshold Timeout Threshold for MFI Mode

RKCAN_WAVE_FILTER_CFG

Address: **Operational Base** + offset (0x0824)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:11	RW	0x0	filter_in_sel Filter input selection signal. 2'b00: rx_data; 2'b01: rx_data_ff1; 2'b10: rx_data_ff2; 2'b11: rx_data_ff3.
10	RW	0x0	filter_bypass Filter Bypass. 1'b0: Disable; 1'b1: Enable. The input RX signal bypasses the filter.

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Bit	Attr	Reset Value	Description
9	RW	0x0	filter_en Filter Enable 1'b0: Disable Filter; 1'b1: Enable Filter.
8	RW	0x1	filter_mode Filter Mode. 1'b0: RST Filter Mode; 1'b1: IDC Filter Mode. After encountering glitches, increment or decrement filter_cnt.
7:0	RW	0x00	filter_width Configure the filter bandwidth of the filter. Unit is can_clk cycle.

RKCAN_RBC_CFG

Address: **Operational Base** + offset (0x0828)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:16	RW	0x0a	integration_to_idle
15:13	RO	0x0	reserved
12:8	RW	0x12	passive_err_rbc
7:5	RO	0x0	reserved
4:0	RW	0x0a	active_err_rbc

RKCAN_TXCRC_CFG

Address: **Operational Base** + offset (0x082C)

Bit	Attr	Reset Value	Description
31	RW	0x0	force_txcrc_en
30	RW	0x0	force_rxcrc_en
29:22	RO	0x00	reserved
21:0	RW	0x000000	force_crc_val

RKCAN_BUSOFF_RCY_CFG

Address: **Operational Base** + offset (0x0830)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	rcy_sclr rcy_cnt & rcy_times Counter Clear.
8	RW	0x0	rcy_en Timer Recovery Mode Enable 1'b0: Disable; 1'b1: Enable.
7:0	RW	0x00	rcy_times_thr Recovery attempt threshold. 0~255.

RKCAN_BUSOFF_RCY_THR

Address: **Operational Base** + offset (0x0834)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rcy_cnt_thr Recovery timer threshold. (0~0xffffffff) rcy_cnt using can_clk as the counting clock.

RKCAN_ACK_CFG

Address: **Operational Base** + offset (0x0840)

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Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:1	RW	0x000	ack_delay_tseg When ack_delay_en is 1, the sampling point of the ACK_SLOT bit is counted using (tseg1+ack_delay_tseg).
0	RW	0x0	ack_delay_en ACK SLOT Delay Sample Enable 1'b0: Disable. 1'b1: Enable.

RKCAN_ERROR_CODE

Address: **Operational Base** + offset (0x0900)

Bit	Attr	Reset Value	Description
31	RW	0x0	tx_crc_error_flag When RKCAN is the transmitter, CRC error is detected. 1'b0: No CRC Error; 1'b1: An CRC Error has occurred.
30	RW	0x0	rx_crc_error_flag When RKCAN is the receiver, CRC error is detected. 1'b0: No CRC Error; 1'b1: An CRC Error has occurred.
29	RO	0x0	error_phase 1'b0: Arbitration Phase 1'b1: Data Phase
28:26	RO	0x0	error_type Error type: 3'b000: BIT ERROR 3'b001: BIT STUFF ERROR 3'b010: FORM ERROR 3'b011: ACK ERROR 3'b100: CRC ERROR
25	RW	0x0	error_direction error_direction' is used to indicate whether RKCAN was in a sending or receiving state when an error occurred. 1'b0: TX Node; 1'b1: RX Node.
24:19	RO	0x00	tx_state Indicate the status of TX FSM when an error occurs 6'b000001: TRANSMIT_IDLE 6'b000010: TRANSMIT_SOF_DLC 6'b000100: TRANSMIT_DATA 6'b001000: TRANSMIT_STUFF_COUNT 6'b010000: TRANSMIT_CRC 6'b100000: TRANSMIT_ACK_EOF

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Bit	Attr	Reset Value	Description
18:0	RO	0x00000	rx_state Indicate the status of RX FSM when an error occurs 19'b0000000000000000001: RECEIVE_STOP 19'b0000000000000000010: RECEIVE_BUS_INT 19'b0000000000000000100: RECEIVE_BUS_IDLE 19'b0000000000000001000: RECEIVE_SOF_IDE 19'b0000000000000010000: RECEIVE_ID2_RTR 19'b0000000000000100000: RECEIVE_LONGF 19'b0000000000001000000: RECEIVE_RES 19'b0000000000010000000: RECEIVE_BRS_ESI 19'b0000000000100000000: RECEIVE_DLC 19'b0000000001000000000: RECEIVE_DATA 19'b0000000010000000000: RECEIVE_STUFF_COUNT 19'b0000000100000000000: RECEIVE_CRC 19'b0000001000000000000: RECEIVE_CRC_LIM 19'b0000010000000000000: RECEIVE_ACK_SLOT 19'b0000100000000000000: RECEIVE_ACK_LIM 19'b0001000000000000000: RECEIVE_EOF 19'b0010000000000000000: RECEIVE_SPACE 19'b0100000000000000000: RECEIVE_OVERLOAD 19'b1000000000000000000: RECEIVE_ERROR

RKCAN_ERROR_MASK

Address: **Operational Base** + offset (0x0904)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	ack_error Error mask for ack error 1'b0: Unmasked 1'b1: Masked
3	RW	0x0	form_error Error mask for form error 1'b0: Unmasked 1'b1: Masked
2	RW	0x0	crc_error Error mask for crc error 1'b0: Unmasked 1'b1: Masked
1	RW	0x0	stuff_error Error mask for stuff error 1'b0: Unmasked 1'b1: Masked
0	RW	0x0	bit_error Error mask for bit error 1'b0: Unmasked 1'b1: Masked

RKCAN_RXCRC_VAL

Address: **Operational Base** + offset (0x0908)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RO	0x00	rxcrc_val For Debug.

RKCAN_CRC_CAL

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Address: **Operational Base** + offset (0x090C)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RO	0x00	crc_cal For Debug.

RKCAN_RXERRORCNT

Address: **Operational Base** + offset (0x0910)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	rx_err_cnt Receive Error Counter (REC). Actual state of the Receive Error Counter. Value between 0 and 127.

RKCAN_TXERRORCNT

Address: **Operational Base** + offset (0x0914)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RO	0x000	tx_err_cnt Transmit Error Counter (TEC). Actual state of the Transmit Error Counter. Value between 0 and 255.

RKCAN_ARBIT_FAIL_STATE

Address: **Operational Base** + offset (0x0918)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RO	0x000	arbit_fail_code This register indicates the bit position of arbitration section where the arbitration was lost.

RKCAN_RX_RXSRAM_RDATA

Address: **Operational Base** + offset (0x0C00)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rx_sram_rdata rx SRAM read data value Used for debug

RKCAN_RTL_VERSION

Address: **Operational Base** + offset (0x0F0C)

Bit	Attr	Reset Value	Description
31:0	RO	0xcfdba0e3	version RKCAN Version = 32'hCFD_B_A0_E3; CFD_B/F_Ax_Ex: CFD B: Beta Version; F: Formal Version; Ax: Major Version Number; Ex: Minor Version Number.

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39.4 Interface Description

39.5 Application Notes

39.5.1 Controller initialization flow

The controller must configure the registers after power-up or hardware reset. During the operation of the controller, a software reset request may be sent and reconfigured (re-initialized) as shown below.

After the initialization is completed, the controller enters the working mode, sends the frame to be sent to the buffer, and then sets the "send request" flag of the command register to start transmitting.

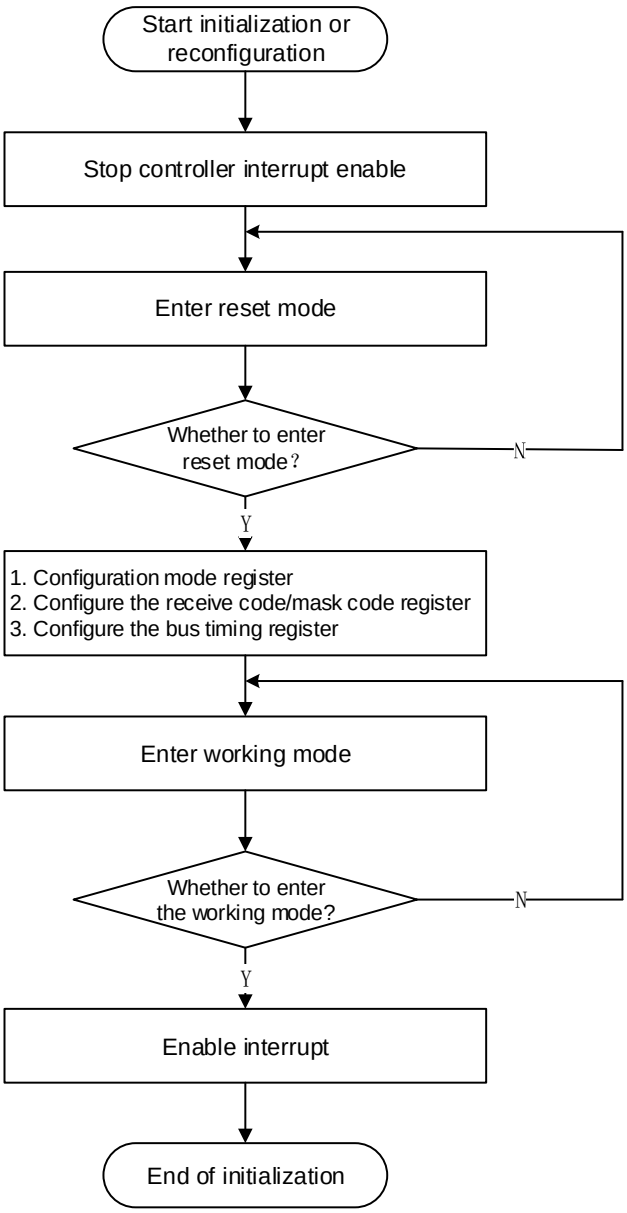

Fig. 39-9 Initialization Flow

39.5.2 Loop-back Mode

The controller must configure the registers after power-up or hardware reset. During the operation of the controller, a software reset request may be sent and reconfigured (re-initialized) as shown below.

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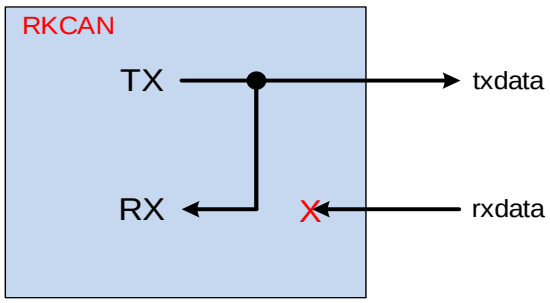

Fig. 39-10 Loop-back Mode

39.5.3 Silent Mode

The controller must configure the registers after power-up or hardware reset. During the operation of the controller, a software reset request may be sent and reconfigured (re-initialized) as shown below.

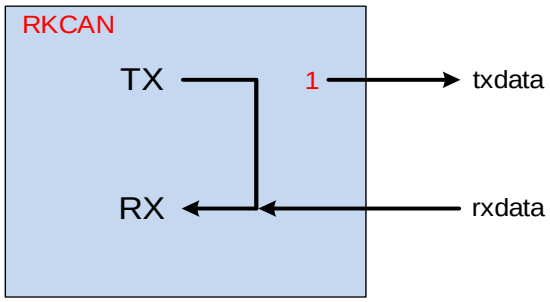

Fig. 39-11 Silent Mode

39.5.4 RXSTX Mode

(1)rxstx_mode=0, RKCAN cannot receive the data sent by itself;
(2)rxstx_mode=1, RKCAN can receive the data sent by itself, and when the ID of the frame is the same as the ID_CODE of RKCAN itself, RKCAN will store the frame information into RX storage.

39.5.5 Auto Retx Mode

RKCAN supports two automatic retransmission modes:

(1) Unlimited Retransmission Mode: There is no limit to the number of retransmissions until the retransmission is successful.

(2) Limited Retransmissions Mode: The threshold for the number of automatic retransmissions can be configured. If the limit threshold is reached and the retransmission is still not successful, the retransmission will stop, and a retransmission failure interrupt will be issued. RKCAN will also count the reasons and corresponding times that cause the transmission failure during the retransmission process, such as arbitration failure, NoACK, or bus error, etc.

39.5.6 Bus Off Recovery Mechanism

RKCAN supports three configurable Bus_off recovery mechanisms, which are:

(1) Automatic Recovery: When the RKCAN node detects 11 recessive bits (no active messages on the bus) appearing consecutively 128 times, it can automatically exit the Bus_off state.

(2) Timed Recovery: The timing length can be set by configuring the register. After the timer expires, RKCAN exits the Bus_off state. The software can implement fast recovery and slow recovery functions using the timed recovery mode.

(3) Manual Recovery: In manual recovery mode, RKCAN will not automatically exit the Bus-off state. It can only exit the Bus-off state by configuring the manual recovery register.

39.5.7 Sleep Mode

After enabling Sleep Mode, RKCAN will automatically enter a low-power mode when the bus is idle, turning off the internal clock. The internal clock will automatically turn on when

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there is a data frame on the bus or when a data frame needs to be sent.

39.5.8 Multi-frame Mode

RKCAN supports an interrupt being issued upon receiving each frame, and it can also be configured to issue an interrupt only after receiving N frames in multi-frame mode. This can reduce the number of interrupts and reduce software intervention. The related configuration can be found in the register RXINT_CTRL register and RXINT_TIMEOUT.

39.5.9 DMA Support

The RKCAN supports DMA signaling with the use of one output signals (dma_rx_req) to indicate when the receive data is ready to be read. When RKCAN_DMA_CTRL.dma_rx_en is set to 1, the DMA function is enabled. The dma_rx_req signal is asserted when the amount of remaining data in the RXFIFO exceeds the value set by RKCAN_DMA_CTRL.dma_thr.

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Chapter 40 Master Double Data Rate Serial Memory Controller (MASTER DSMC)

40.1 Overview

The DSMC module provides function and operation for interfacing to the DSMC memory devices, and the Rockchip LocalBus devices. The DSMC achieves high speed read/write throughput by double data rate interface.

The main feature is shown below.

- Support the double data rate interface
- Support up to select 4 chips
- Support 8-wire and 16-wire Swact
- erial transfer mode
- Support configurable write/read contiguous address merging transaction
- Support configurable write/read boundary address splitting transaction
- Support to transform WRAP transfer to INCR transfer
- Support byte access
- Support configurable DQS input clock delay line
- For LocalBus devices, support to assert the selecting signals CS simultaneously in the write transaction
- For LocalBus devices, support 3 clock mode: normal mode, always-on mode, no-edge-clk mode
- For LocalBus devices, support to request DMAC to transfer data when receiving interrupt 0/1
- For LocalBus devices, support configurable serial address width: 16 bits or 32 bits in different region

40.2 Block Diagram

DSMC is comprised of:

- APB Interface

The APB Interface implements the APB slave operation. Its data bus width is 32 bits.

- AXI Interface

The AXI Interface is a XIP interface to access internal device. Its data bus width is 64 bits.

- I/O Port Interface

External data interface to or from I/O pads.

- Core

The core module is used to control the data stream of TX/RX datapath.

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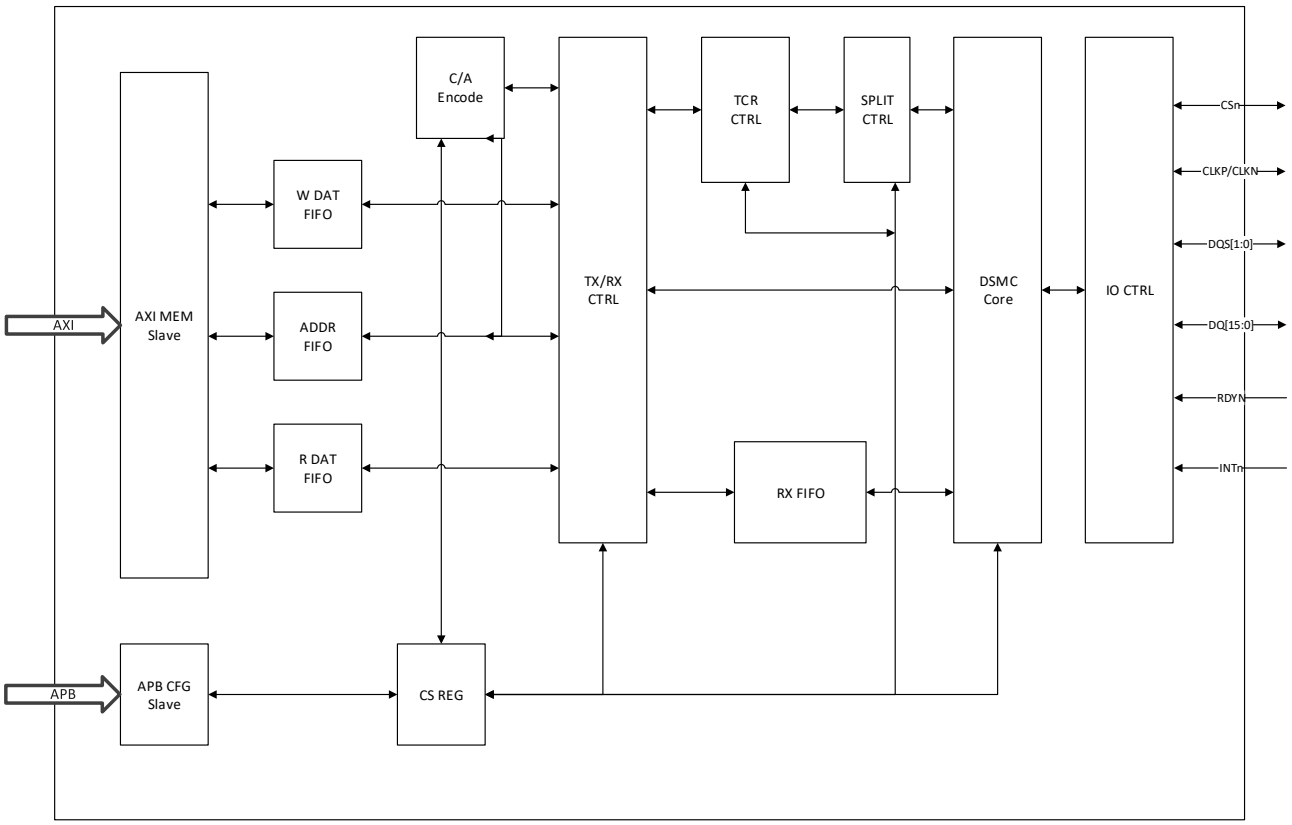

Fig. 40-1 DSMC Block Diagram

40.3 Function Description

The DSMC module is high throughput memory interface. It provides execute in place (XIP) and block copy access to DSMC memory devices (HyperRAM and HyperFlash). The DSMC module is compliant to the Cypress DSMC™ Specification. Meanwhile, it could access Rockchip LocalBus devices, and transfer instructions or bulk data with high speed.

40.3.1 DSMC Core

This section describes physical interface of DSMC module. The DSMC core generates DSMC timing from control signals.

40.3.1.1 Read

DSMC Core module asserts CSn, CLKP/CLKN, and DQ. Then, it outputs 3 words command/address, and reads 1 or more data by the timing of DQS. The DSMC Core puts the transaction request from AXI bus, such as the burst type and the burst length, to the C/A cycle on DSMC as is shown below.

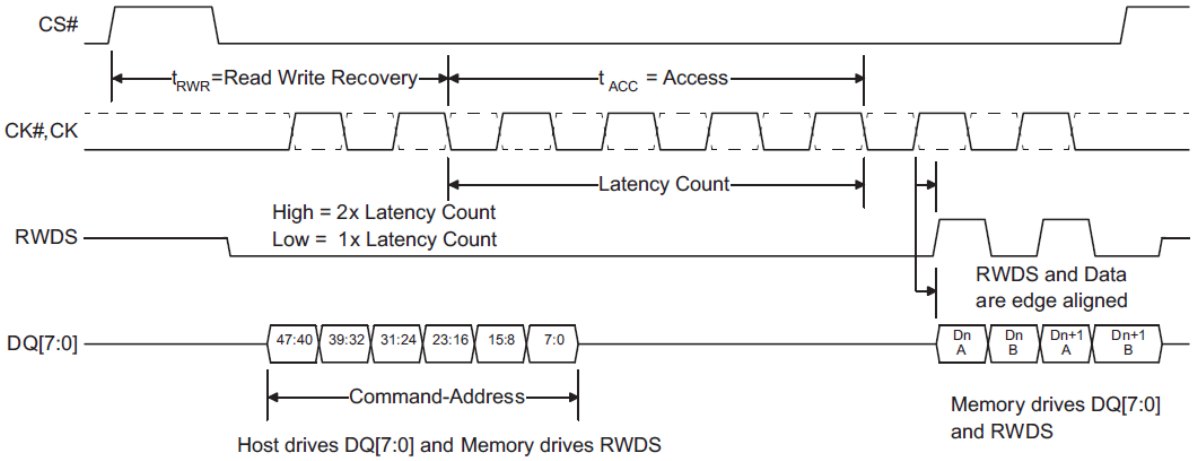

Fig. 40-2 HyperRAM Read Waveform

40.3.1.2 Write

This section describes the write operation of DSMC Core. The DSMC Core asserts CSn,

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CLKP/CLKN, and DQ. Then, it outputs 3 words command/address, and writes 1 or more data. For HyperRAM write operation, there is initial clock latency before writing data.

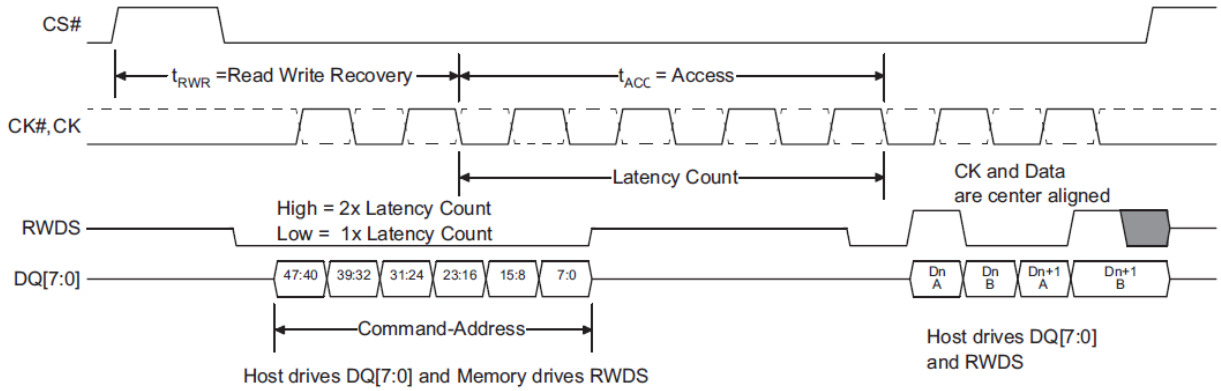

Fig. 40-3 HyperRAM Write Waveform

40.3.1.3 Byte Mask

This DSMC Memory Interface Controller outputs DQS signal as a byte mask during write operation. When byte access is requested from Main Controller, not write data is masked by DQS=HIGH. When target device is HyperFlash, byte masked data is written to device because of only supporting 16-bit access (byte masked data is fill in all 1 bit). In the HyperRAM Write Waveform, the D_n A and D_{n+1} B is invalid data which is masked.

40.3.2 TX/RX Controller

The TX/RX Controller performs operation control by state machine, and flow control of data between AXI bus and DSMC. In addition, when next access address is accepted by multiple outstanding address on AXI bus, it could be merged to the present transaction to improve the bandwidth if the address of subsequent access is continuous address to the present access.

40.3.3 C/A Encoder

DSMC memory device uses 6 bytes of command/address information to define the transactions characteristics. Table below shows the assignments of CA bit in DSMC Memory Interface Controller.

Table 40-1 C/A Format of DSMC for Hyper Device

C/A Bit	Name	Assignment
47	R/W#	0: Write, 1: Read
46	Target	CRT in DSMC_MCRn
45	Burst Type	0: WRAP, 1: INCR
44	RFU	0
43-16	Page Address	Address [31:4]
15	RFU	0
14-13	RFU	3
12-3	RFU	0
2-0	Column Address	Address [3:1]

note: The CA bit function of different devices slightly differs, and the exact meaning nead to be referred to the datasheet of the device.

40.3.4 FIFO

This section describes the FIFO for processing transaction request.

40.3.4.1 ADDR FIFO

ADR FIFO is a synchronizer module from AXI clock domain to DSMC clock domain. This FIFO has 46-bit width. This FIFO stores the control data which includes address, length, burst type and r/w flag. From these data, the control signals are generated for Main Controller.

40.3.4.2 W DAT FIFO

This FIFO is used to store the write data, valid information and strobe information written from the master in order to receive the command sequence of write buffer programming without a wait on AXI interface. The valid information indicates the 8-bit data is valid or not. The strobe information is used for strobe data from AXI interface to DSMC Core.

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When valid and strobe is 1, the 8-bit data is written data.

40.3.4.3 R DAT FIFO

This FIFO is used to store the data read from RX FIFO and the error detection information, and data stored is outputted according to timing of ACLK on AXI interface. This error information is transferred to HOST by RRESP signals.

40.3.5 LocalBus

40.3.5.1 Region division

The internal space of LocalBus device could be divided into different region, and they could be applied in suitable case. The size of regions is configured by DSMC_DEV_SIZE and DSMC_SLV_RGN_DIVn. The attribution of different region could be set to DPRA, REG or FIFO.

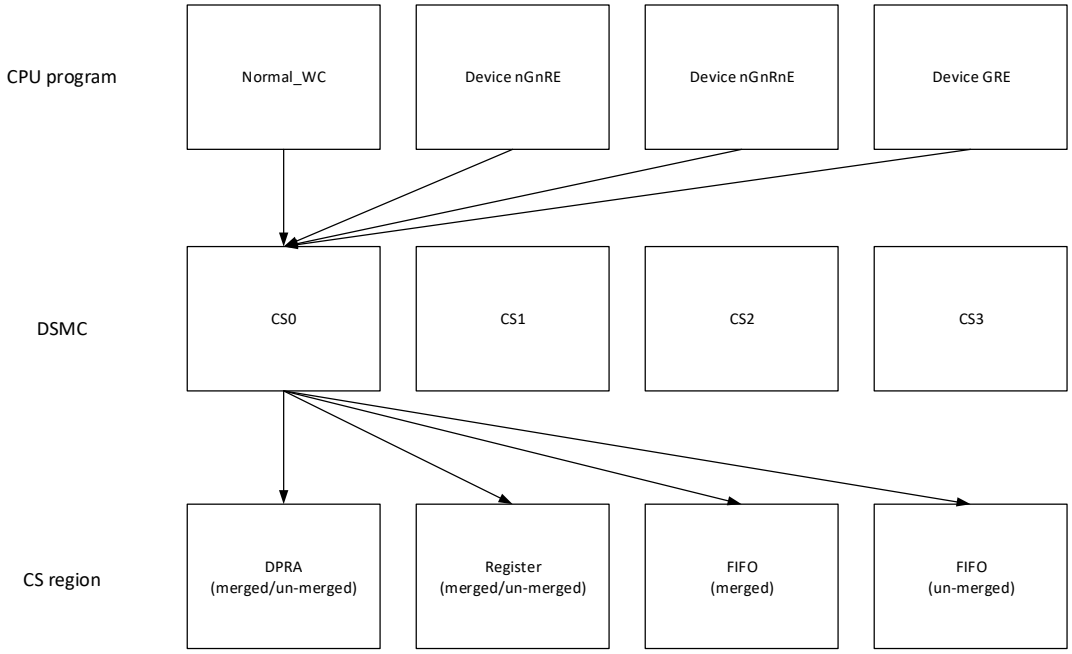

Fig. 40-4 Region Division of LocalBus Device

40.3.5.2 CA Encoder

Table 40-2 C/A Format of DSMC for LocalBus Device

C/A Bit	Name	Assignment
47	R/W#	0: Read, 1: Write
46	Target	CRT in DSMC_MCRn
45	Burst Type	0: WRAP, 1: INCR
44	Space Type	0: FIFO, 1: DPRA
43	FIFO Merge	0: No Merge, 1: Merge
42	RFU	0
41-40	Region	Region 0/1/2/3
39-32	Length	Burst length
31-0	Address	Address [31:0]

40.3.5.3 Back pressure

The back pressure mechanism is used to make full use of FIFO region space.

In the read transaction, when the FIFO is empty and could not provide data to the DSMC interface, the slave could enter the wait state, in which slave stop to send DQS clock, and latch the output DQ data. When the FIFO is recovered, the slave could continue sending the DQS and DQ, which could save bandwidth comparing to restart another burst.

In the write transaction, when the FIFO is full and could not receive data from the DSMC interface, the asynchronous signal DSMC_RDYN would be asserted. When the DSMC received, it would not send DQ and DSMC_CLK until the DSMC_RDYN is not asserted, which means there are enough space in the slave FIFO to accept data.

40.4 Register Description

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40.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

40.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
DSMC_VER	0x0000	W	0x03023FC7	IP Version Register
DSMC_CSR	0x0008	W	0x00000000	Controller Status Register
DSMC_TAR	0x0010	W	0x00000000	Transaction Allocation Register
DSMC_AXICTL	0x0014	W	0x00000020	AXI Transaction Control Register
DSMC_CLK_MD	0x0020	W	0x00000000	Clock Mode Register
DSMC_DQ_SMP_MD	0x0024	W	0x00000000	Clock Mode Register
DSMC_DEV_SIZE	0x0030	W	0x00000017	Device Region Size Register
DSMC_INT_EN	0x0040	W	0x00000000	Interrupt Enable Register
DSMC_INT_STATUS	0x0044	W	0x00000000	Interrupt Status Register
DSMC_INT_MASK	0x0048	W	0x00000000	Interrupt Mask Register
DSMC_DMA_EN	0x0050	W	0x00000000	DMA Request Enable Register
DSMC_DMA_REQ_NUM0	0x0054	W	0x00000000	DMA Request Number Register 0
DSMC_DMA_REQ_NUM1	0x0058	W	0x00000000	DMA Request Number Register 1
DSMC_DMA_MUX	0x005C	W	0x00000010	Interrupt to DMA Request Mux Register
DSMC_VDMC0	0x1000	W	0x00000226	Vendor Device Mode Control Register, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000
DSMC_MCR0	0x1010	W	0x00000003	CS0# Memory Configuration Register, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000
DSMC_MTR0	0x1014	W	0x00000022	CS0# Memory Base Address, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000
DSMC_WAIT_TIME0	0x1018	W	0x0003FFFF	CS0# Memory Base Address, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000
DSMC_BDRTCR0	0x1020	W	0x00000002	Boundary Transfer Control Register 0, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000
DSMC_MRGTCR0	0x1024	W	0x00000000	Merge Transfer Control Register 0, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000
DSMC_WRAP2INCR0	0x1028	W	0x00000000	The function register of changing WRAP to INCR, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000

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Name	Offset	Size	Reset Value	Description
DSMC_RDS_DLL0_CTL0	0x1030	W	0x80000010	RDS Clock DLL Control Register 0, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000
DSMC_RDS_DLL1_CTL0	0x1034	W	0x80000010	RDS Clock DLL Control Register 1, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000
DSMC_SLV_RGN_DIV0	0x1040	W	0x00000002	The division of slave region , and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000
DSMC_RGN0_ATTR0	0x1050	W	0x00000000	The attribution of region 0, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000
DSMC_RGN1_ATTR0	0x1054	W	0x00000000	The attribution of region 0, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000
DSMC_RGN2_ATTR0	0x1058	W	0x00000000	The attribution of region 2, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000
DSMC_RGN3_ATTR0	0x105C	W	0x00000000	The attribution of region 3, and it could be expanded to CS1/2/3# for sub base address 0x2000/0x3000/0x4000

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

40.4.3 Detail Registers Description

DSMC_VER

Address: Operational Base(0x21CA0000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RO	0x03023FC7	version IP Version

DSMC_CSR

Address: Operational Base(0x21CA0000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RO	0x0	wrstoerr Write RSTO error. This bit indicates whether HyperBus memory is under reset state in the latest write operation. 1'b0: Normal operation 1'b1: HyperBus memory is under reset When this bit is set, HyperBus Memory Controller IP responds by AXI SLVERR.

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Bit	Attr	Reset Value	Description
25	RO	0x0	wtrserr Write Transaction Error. This bit indicates whether AXI protocol is acceptable by HyperBus Memory Controller IP in the latest write transaction. 1'b0: Normal operation 1'b1: This protocol is not supported When this bit is set, HyperBus Memory Controller IP responds by AXI SLVERR.
24	RO	0x0	wdecerr Write Decode Error. This bit indicates whether access address is acceptable in the latest write transaction. 1'b0: Normal operation 1'b1: Access address is not reachable When this bit is set, HyperBus Memory Controller IP responds by AXI DECERR.
23:17	RO	0x00	reserved
16	RO	0x0	wact Write is Active. This bit indicates whether write transaction is in progress or not. 1'b0: Write is idle 1'b1: Write is active
15:12	RO	0x0	reserved
11	RO	0x0	rdsstall RDS Stall. This bit indicates whether read data transfer from HyperBus memory is stalled (RDS remains LOW) in the latest read transaction. 1'b0: Normal operation 1'b1: RDS is stalled When this bit is set, HyperBus Memory Controller IP responds by AXI SLVERR.
10	RO	0x0	rrstoerr Read RSTO error. This bit indicates whether HyperBus memory is under reset state in the latest read operation. 1'b0: Normal operation 1'b1: HyperBus memory is under reset When this bit is set, HyperBus Memory Controller IP responds by AXI SLVERR.
9	RO	0x0	rtrserr Read Transaction Error. This bit indicates whether AXI protocol is acceptable by HyperBus Memory Controller IP in the latest read transaction. 1'b0: Normal operation 1'b1: This protocol is not supported When this bit is set, HyperBus Memory Controller IP responds by AXI SLVERR.
8	RO	0x0	rdecerr Read Decode Error. This bit indicates whether access address is acceptable in the latest read transaction. 1'b0: Normal operation 1'b1: Access address is not reachable When this bit is set, HyperBus Memory Controller IP responds by AXI DECERR.
7:1	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
0	RO	0x0	ract Read is Active. This bit indicates whether read transaction is in progress or not. 1'b0: Read is idle 1'b1: Read is active

DSMC_TAR

Address: Operational Base(0x21CA0000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:4	RW	0x0	rta Read Transaction Allocation. 2'b00: 1 read transaction 2'b01: 2 read transactions 2'b10: 3 read transactions 2'b11: 4 read transactions
3:2	RO	0x0	reserved
1:0	RW	0x0	wta Write Transaction Allocation. 2'b00: 1 write transaction 2'b01: 2 write transactions 2'b10: 3 write transactions 2'b11: 4 write transactions

DSMC_AXICTL

Address: Operational Base(0x21CA0000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	rd_no_err The axi read response will be tied 0 if this bit is enabled. 1'b0: Disable 1'b1: Enable
7:6	RO	0x0	reserved
5:4	RW	0x2	write_bvalid_ctl 2'b00: Generate the bvalid after the burst data TX end in IO 2'b01: Generate the bvalid after the TX state machine accept the request FIFO 2'b10: Generate the bvalid after burst write granted by arbiter 2'b11: Reserved
3:1	RO	0x0	reserved
0	RW	0x0	nowait_write_data_done_en 1'b0: Disable 1'b1: Enable Only support "0" in current project

DSMC_CLK_MD

Address: Operational Base(0x21CA0000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	clk_mode This register is only configured in local bus application. 2'b00: Normal-toggle Mode, the ck only toggles when cs is asserted 2'b01: Always-on Mode, the ck is always on 2'b10: No-edge-clk Mode, the ck is always on except for the cs changing edge 2'b11: Reserved

DSMC_DQ_SMP_MD

Address: Operational Base(0x21CA0000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	additional_cycle_num 1'b0: the additional dsmc clock is not transmited until master receive the expected data from dqinfifo. 1'b1: the additional transmitted dsmc clock cycle equals 1.
1	RW	0x0	ck_cycle_mode 1'b0: the additional dsmc clock cycle is transmitted. 1'b1: the transmitted dsmc clock cycles equal the expected data number.
0	RO	0x0	reserved

DSMC_DEV_SIZE

Address: Operational Base(0x21CA0000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4:0	RW	0x17	dev_size Device Size 5'd0: 1 byte 5'd1: 2 bytes 5'd2: 4 bytes ..... 5'd10: 1K bytes ..... 5'd20: 1M bytes ..... 5'd31: 2G bytes In Memory-Mapped mode, the CS is controlled by AXI address bus, region size is used to generate CS.

DSMC_INT_EN

Address: Operational Base(0x21CA0000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	rdstall_int_en This bit is used to control the read stall time out interrupt enable. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3	RW	0x0	int_en3 This bit is used to control the interrupt3. This register is only valid in local bus application. 1'b0: Disable 1'b1: Enable
2	RW	0x0	int_en2 This bit is used to control the interrupt2. This register is only valid in local bus application. 1'b0: Disable 1'b1: Enable
1	RW	0x0	int_en1 This bit is used to control the interrupt1. This register is only valid in local bus application. 1'b0: Disable 1'b1: Enable
0	RW	0x0	int_en0 This bit is used to control the interrupt0. This register is only valid in local bus application. 1'b0: Disable 1'b1: Enable

DSMC_INT_STATUS

Address: Operational Base(0x21CA0000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	W1C	0x0	rdstall_int_status Read stall time out interrupt status of DSMC. High level means occurring interrupt. When a 1 is written into a corresponding bit of this register, the interrupt is cleared, and the bit is self-cleared at once. This register is only valid in local bus application.
3	W1C	0x0	int_status3 Interrupt 3 status of DSMC. High level means occurring interrupt. When a 1 is written into a corresponding bit of this register, the interrupt is cleared, and the bit is self-cleared at once. This register is only valid in local bus application.
2	W1C	0x0	int_status2 Interrupt 2 status of DSMC. High level means occurring interrupt. When a 1 is written into a corresponding bit of this register, the interrupt is cleared, and the bit is self-cleared at once. This register is only valid in local bus application.
1	W1C	0x0	int_status1 Interrupt 1 status of DSMC. High level means occurring interrupt. When a 1 is written into a corresponding bit of this register, the interrupt is cleared, and the bit is self-cleared at once. This register is only valid in local bus application.

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Bit	Attr	Reset Value	Description
0	W1C	0x0	int_status0 Interrupt 0 status of DSMC. High level means occurring interrupt. When a 1 is written into a corresponding bit of this register, the interrupt is cleared, and the bit is self-cleared at once. This register is only valid in local bus application.

DSMC_INT_MASK

Address: Operational Base(0x21CA0000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	rdstall_int_mask This register is used to mask the read stall interrupt. 1'b0: Interrupt is unmasked 1'b1: Interrupt is masked
3	RW	0x0	int_mask3 This register is only valid in local bus application. 1'b0: Interrupt is unmasked 1'b1: Interrupt is masked
2	RW	0x0	int_mask2 This register is only valid in local bus application. 1'b0: Interrupt is unmasked 1'b1: Interrupt is masked
1	RW	0x0	int_mask1 This register is only valid in local bus application. 1'b0: Interrupt is unmasked 1'b1: Interrupt is masked
0	RW	0x0	int_mask0 This register is only valid in local bus application. 1'b0: Interrupt is unmasked 1'b1: Interrupt is masked

DSMC_DMA_EN

Address: Operational Base(0x21CA0000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	dma_req_en1 This bit is used to control the DMA request from interrrupt1. This register is only valid in local bus application. 1'b0: Disable 1'b1: Enable
0	RW	0x0	dma_req_en0 This bit is used to control the DMA request from interrrupt0. This register is only valid in local bus application. 1'b0: Disable 1'b1: Enable

DSMC_DMA_REQ_NUM0

Address: Operational Base(0x21CA0000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	dma_req_num0 This register is used to indicate the DMA request number when DSMC accepts the interrupt0 from local bus slave. This register is only valid in local bus application.

DSMC_DMA_REQ_NUM1

Address: Operational Base(0x21CA0000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	dma_req_num1 This register is used to indicate the DMA request number when DSMC accepts the interrupt1 from local bus slave. This register is only valid in local bus application.

DSMC_DMA_MUX

Address: Operational Base(0x21CA0000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:4	RW	0x1	dma_req1_mux This bit field is used to select the interrupt to DMA request1. 2'b00: int0 2'b01: int1 2'h10: int2 2'b11: int3
3:2	RO	0x0	reserved
1:0	RW	0x0	dma_req0_mux This bit fiele is used to select the interrupt to DMA request0. 2'b00: int0 2'b01: int1 2'h10: int2 2'b11: int3

DSMC_VDMC0

Address: Operational Base(0x21CA0000) + offset (0x1000)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x1	latency_fixed Only valid to APM pSRAM Read Memory. 1'b0: Variable 1'b1: Fixed
8	RW	0x0	reset_cmd_mode Generate reset Command to Device. Only valid in APM mid when CR register mode is set. If this bit is set, any write access in CR mode will initiate the FF command sequence.
7:4	RW	0x2	protocol Device Type 4'h0: Reserved 4'h1: OPI_Xccela (reserved) 4'h2: HyperBus (reserved) 4'h3: Local Bus Others: Reserved

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Bit	Attr	Reset Value	Description
3:0	RW	0x6	mid MID 4'h1: Infineon/Cypress 4'h3: ISSI 4'h6: Winbond 4'hd: APM Others: Reserved

DSMC_MCR0

Address: Operational Base(0x21CA0000) + offset (0x1010)

Bit	Attr	Reset Value	Description
31	RW	0x0	maxen Maximum length Enable 1'b0: No configurable CS# low time 1'b1: Configurable CS# low time When this bit 1, CS# low time can be configurable by MAXLEN bit.
30:27	RO	0x0	reserved
26:18	RW	0x000	maxlen Maximum Length This bit indicates maximum read/write transaction length to memory. This bit is ignored when MAXEN bit is 0. 9'h000: 2 Byte (1 HyperBus CK) 9'h001: 4 Byte (2 HyperBus CK) 9'h002: 6 Byte (3 HyperBus CK) ..... 9'h1ff: 1024 Byte (512 HyperBus CK)
17	RW	0x0	tcmo True Continuous Merge Option. 1'b0: No merging WRAP and INCR 1'b1: Merging WRAP and INCR Note that this function can be used with the HyperBus memory with specific function. Please confirm whether it is corresponding HyperBus memory before enabling this function. If set to 1, it means the controller can merge the Wrap and INCR operation.
16	RW	0x0	acs Asymmetry Cache Support. 1'b0: No asymmetry cache system support. 1'b1: Asymmetry cache system support. This function should be disabled if the HyperBus memory itself supports the asymmetry cache system. If this bit set to 1, then the HyperBus memory interface controller accepts the wrap read transaction and compares the required wrap size with the wrap size of HyperBus memory in register; When the wrap size is the same, HyperBus memory interface controller requires the wrap burst read to HyperBus memory; When the wrap size differs, HyperBus memory interface controller emulates wrap burst read by requesting two continuous burst read to HyperBus memory.
15:6	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
5	RW	0x0	crt Configuration Register Target. 1'b0: Memory space 1'b1: CR space This bit indicates whether the read or write operation accesses the memory or CR space. This bit is mapped to CA[46] bit in HyperRAM. When using HyperFlash, this bit should be set to 0.
4	RW	0x0	devtype Device Type. 1'b0: HyperFlash 1'b1: HyperRAM Device type for control target. Only support "1'b1" in current project
3	RW	0x0	iowidth IO Width. 1'b0: x8 interface 1'b1: x16 interface Note that "1'b1: x16 interface" can be set when DEVTYPE is set to "1'b1: HyperRAM"
2	RW	0x0	exclusive_dqs This bit field indicates the number of valid dqs bit when io width is 16 bits, and it is only valid in local bus application. 1'b0: 2 bits 1'b1: 1 bit
1:0	RW	0x3	wrapsize Wrap Size. 2'b00: Reserved 2'b01: 32(Clocks), 64 bytes for x8 and 128 bytes for x16 2'b10: 8(Clocks), 16 bytes for x8 and 32 bytes for x16 2'b11: 16(Clocks), 32 bytes for x8 and 64 bytes for x16 The wrap burst length of HyperBus memory. This bit is ignored when the asymmetry cache support bit is 0. When the asymmetry cache support is 1, this bit should be set the same as wrap size of configuration register in HyperBus memory.

DSMC_MTR0

Address: Operational Base(0x21CA0000) + offset (0x1014)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	rcshi Read Chip Select High Between Operations. This bit indicates CS# high time for read between operations. 0x0 corresponds to 1.5 clock cycle, 0xF corresponds to 16.5 clock cycle.
27:24	RW	0x0	wcshi Write Chip Select High Between Operations. This bit indicates CS# high time for write between operations. 0x0 corresponds to 1.5 clock cycle, 0xF corresponds to 16.5 clock cycle.
23:20	RW	0x0	rcss Read Chip Select Setup to next CK rising edge. This bit indicates CS# setup time for read from CS# assertion. 0x0 corresponds to 1 clock cycle, 0xF corresponds to 16 clock cycles.

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Bit	Attr	Reset Value	Description
19:16	RW	0x0	wcss Write Chip Select Setup to next CK rising edge. This bit indicates CS# setup time for write from CS# assertion. 0x0 corresponds to 1 clock cycle, 0xF corresponds to 16 clock cycles.
15:12	RW	0x0	rcsh Read Chip Select Hold after CK falling edge. This bit indicates CS# hold time for read to CS# de-assertion. 0x0 corresponds to 1 clock cycle, 0xF corresponds to 16 clock cycles.
11:8	RW	0x0	wcsh Write Chip Select Hold after CK falling edge. This bit indicates CS# hold time for write to CS# de-assertion. 0x0 corresponds to 1 clock cycle, 0xF corresponds to 16 clock cycles.
7:4	RW	0x2	rltcy Read Latency Cycle. Only uses in HyperRAM. This bit indicates initial latency code for write access. This bit is ignored when MCRX.DEVTYPE is 0 (HyperFlash). 4'h0: 5 clock latency 4'h1: 6 clock latency 4'h2: 7 clock latency 4'h3: 8 clock latency 4'h4: 9 clock latency 4'h5: 10 clock latency 4'hb: 0 clock latency 4'hc: 1 clock latency 4'hd: 2 clock latency 4'he: 3 clock latency 4'hf: 4 clock latency Others: Reserved
3:0	RW	0x2	wltcy Write Latency Cycle. Only uses in HyperRAM. This bit indicates initial latency code for write access. This bit is ignored when MCRX.DEVTYPE is 0 (HyperFlash). 4'h0: 5 clock latency 4'h1: 6 clock latency 4'h2: 7 clock latency 4'h3: 8 clock latency 4'h4: 9 clock latency 4'h5: 10 clock latency 4'hb: 0 clock latency 4'hc: 1 clock latency 4'hd: 2 clock latency 4'he: 3 clock latency 4'hf: 4 clock latency Others: Reserved

DSMC_WAIT_TIME0

Address: Operational Base(0x21CA0000) + offset (0x1018)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
17:0	RW	0x3ffff	rdstall_wait_time This bit filed is used to configure the max wait time of the read stall status.

DSMC_BDRTCR0

Address: Operational Base(0x21CA0000) + offset (0x1020)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	rd_bdr_xfer_en Enable Cross Row Address Data Read Transfer. 1'b0: Disable 1'b1: Enable
4	RW	0x0	wr_bdr_xfer_en Enable Cross Row Address Data Write Transfer. 1'b0: Disable 1'b1: Enable
3	RO	0x0	reserved
2:0	RW	0x2	col_bit_num The valid column address bit, also the cycle numbers in the port. 3'h0: 6 bits 3'h1: 7 bits 3'h2: 8 bits 3'h3: 9 bits 3'h4: 10 bits 3'h5: 11 bits Others: Reserved

DSMC_MRGTCR0

Address: Operational Base(0x21CA0000) + offset (0x1024)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_merge_en 1'b0: Disable 1'b1: Enable
0	RW	0x0	write_merge_en 1'b0: Disable 1'b1: Enable

DSMC_WRAP2INCR0

Address: Operational Base(0x21CA0000) + offset (0x1028)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	wrap2incr_en This bit is used to enable the function of changing WRAP transfer to INCR transfer. This register is only configured in local bus application. 1'b0: Disable 1'b1: Enable

DSMC_RDS_DLL0_CTL0

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Address: Operational Base(0x21CA0000) + offset (0x1030)

Bit	Attr	Reset Value	Description
31	RW	0x1	rds_0_clk_smp_sel DQ[7:0] Sampling Clock Selection 1'b0: Without DLL 1'b1: With DLL
30:8	RO	0x000000	reserved
7:0	RW	0x10	rds_0_clk_delay_num RDS Clock 0 Delay Line Cell Number

DSMC_RDS_DLL1_CTL0

Address: Operational Base(0x21CA0000) + offset (0x1034)

Bit	Attr	Reset Value	Description
31	RW	0x1	rds_1_clk_smp_sel DQ[7:0] Sampling Clock Selection 1'b0: Without DLL 1'b1: With DLL
30:8	RO	0x000000	reserved
7:0	RW	0x10	rds_1_clk_delay_num RDS Clock 0 Delay Line Cell Number

DSMC_SLV_RGN_DIV0

Address: Operational Base(0x21CA0000) + offset (0x1040)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x2	slv_rgn_div This register is only valid in local bus application. This bit filed indicate the region division of the slave memory. 2'b00: 1 2'b01: 2 2'b10: 4 Others: Reserved

DSMC_RGN0_ATTR0

Address: Operational Base(0x21CA0000) + offset (0x1050)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	rgn0_addr_width This bit is used to indicate the address width of the CA phase when access region 0. 1'b0: 32 bits 1'b1: 16 bits
7	RW	0x0	rgn0_dum_clk_num Write transfer dummy clock cycle number. This bit field is valid only the write dummy clock is enabled. 1'b0: 1 cycle 1'b1: 2 cycles
6	RW	0x0	rgn0_dum_clk_en DSMC will output additional dummy clock cycle in write transaction when access region0. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
5	RW	0x0	rgn0_be_ctrled The cs0 accessing region0 will be controlled by other cs1/cs2/cs3 when this bit is enabled. 1'b0: Disabled 1'b1: Enable
4	RW	0x0	rgn0_ctrl The cs0 accessing region0 will control other cs1/cs2/cs3 when this bit is enabled. 1'b0: Disabled 1'b1: Enable
3:2	RO	0x0	reserved
1:0	RW	0x0	rgn0_attr This register is only valid in local bus application. The attribution of the region0 could be configured in this bit filed. 2'b00: Register 2'b01: DPRA 2'b10: No-Merge FIFO 2'b11: Merged FIFO

DSMC_RGN1_ATTR0

Address: Operational Base(0x21CA0000) + offset (0x1054)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	rgn1_addr_width This bit is used to indicate the address width of the CA phase when access region 1. 1'b0: 32 bits 1'b1: 16 bits
7	RW	0x0	rgn1_dum_clk_num Write transfer dummy clock cycle number. This bit field is valid only the write dummy clock is enabled. 1'b0: 1 cycle 1'b1: 2 cycles
6	RW	0x0	rgn1_dum_clk_en DSMC will output additional dummy clock cycle in write transaction when access region1. 1'b0: Disable 1'b1: Enable
5	RW	0x0	rgn1_be_ctrled The cs0 accessing region1 will be controlled by other cs1/cs2/cs3 when this bit is enabled. 1'b0: Disabled 1'b1: Enable
4	RW	0x0	rgn1_ctrl The cs0 accessing region1 will control other cs1/cs2/cs3 when this bit is enabled. 1'b0: Disabled 1'b1: Enable
3:2	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	rgn1_attr This register is only valid in local bus application. The attribution of the region1 could be configured in this bit filed. 2'b00: Register 2'b01: DPRA 2'b10: No-Merge FIFO 2'b11: Merged FIFO

DSMC_RGN2_ATTR0

Address: Operational Base(0x21CA0000) + offset (0x1058)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	rgn2_addr_width This bit is used to indicate the address width of the CA phase when access region 2. 1'b0: 32 bits 1'b1: 16 bits
7	RW	0x0	rgn2_dum_clk_num Write transfer dummy clock cycle number. This bit field is valid only when the write dummy clock is enabled. 1'b0: 1 cycle 1'b1: 2 cycles
6	RW	0x0	rgn2_wr_dum_clk_en DSMC will output additional dummy clock cycle in write transaction when access region2. 1'b0: Disable 1'b1: Enable
5	RW	0x0	rgn2_be_ctrled The cs0 accessing region2 will be controlled by other cs1/cs2/cs3 when this bit is enabled. 1'b0: Disabled 1'b1: Enable
4	RW	0x0	rgn2_ctrl The cs0 accessing region2 will control other cs1/cs2/cs3 when this bit is enabled. 1'b0: Disabled 1'b1: Enable
3:2	RO	0x0	reserved
1:0	RW	0x0	rgn2_attr This register is only valid in local bus application. The attribution of the region1 could be configured in this bit filed. 2'b00: Register 2'b01: DPRA 2'b10: No-Merge FIFO 2'b11: Merged FIFO

DSMC_RGN3_ATTR0

Address: Operational Base(0x21CA0000) + offset (0x105C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
8	RW	0x0	rgn3_addr_width This bit is used to indicate the address width of the CA phase when access region 3. 1'b0: 32 bits 1'b1: 16 bits
7	RW	0x0	rgn3_dum_clk_num Write transfer dummy clock cycle number. This bit field is valid only when the write dummy clock is enabled. 1'b0: 1 cycle 1'b1: 2 cycles
6	RW	0x0	rng3_dum_clk_en DSMC will output additional dummy clock cycle in write transaction when access region3. 1'b0: Disable 1'b1: Enable
5	RW	0x0	rgn3_be_ctrled The cs0 accessing region3 will be controlled by other cs1/cs2/cs3 when this bit is enabled. 1'b0: Disabled 1'b1: Enable
4	RW	0x0	rgn3_ctrl The cs0 accessing region3 will control other cs1/cs2/cs3 when this bit is enabled. 1'b0: Disabled 1'b1: Enable
3:2	RO	0x0	reserved
1:0	RW	0x0	rgn3_attr This register is only valid in local bus application. The attribution of the region3 could be configured in this bit filed. 2'b00: Register 2'b01: DPRA 2'b10: No-Merge FIFO 2'b11: Merged FIFO

Interface Description

Table 40-3 DSMC interface description

Module Pin	Direction	Pin Name	IOMUX Setting
CLKP	O	GPIO5_B7	GPIO5B_IOMUX_SEL_1[15:12]=4'h4
CLKN	O	GPIO5_B6	GPIO5B_IOMUX_SEL_1[11:8]=4'h4
CS0	O	GPIO5_B4	GPIO5B_IOMUX_SEL_1[3:0]=4'h4
CS1	O	GPIO5_A0	GPIO5A_IOMUX_SEL_0[3:0]=4'h4
CS2	O	GPIO5_D1	GPIO5D_IOMUX_SEL_0[7:4]=4'h4
CS3	O	GPIO5_D0	GPIO5D_IOMUX_SEL_0[3:0]=4'h4
RESETN	O	GPIO5_B2	GPIO5B_IOMUX_SEL_0[11:8]=4'h4
DQS0	I/O	GPIO5_B5	GPIO5B_IOMUX_SEL_1[7:4]=4'h4
DQS1	I/O	GPIO5_A1	GPIO5A_IOMUX_SEL_0[7:4]=4'h4
DQ0	I/O	GPIO5_C7	GPIO5C_IOMUX_SEL_1[15:12]=4'h4
DQ1	I/O	GPIO5_C6	GPIO5C_IOMUX_SEL_1[11:8]=4'h4
DQ2	I/O	GPIO5_C5	GPIO5C_IOMUX_SEL_1[7:4]=4'h4
DQ3	I/O	GPIO5_C4	GPIO5C_IOMUX_SEL_1[3:0]=4'h4
DQ4	I/O	GPIO5_C3	GPIO5C_IOMUX_SEL_0[15:12]=4'h4
DQ5	I/O	GPIO5_C2	GPIO5C_IOMUX_SEL_0[11:8]=4'h4

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Module Pin	Direction	Pin Name	IOMUX Setting
DQ6	I/O	GPIO5_C1	GPIO5C_IOMUX_SEL_0[7:4]=4'h4
DQ7	I/O	GPIO5_C0	GPIO5C_IOMUX_SEL_0[3:0]=4'h4
DQ8	I/O	GPIO5_B1	GPIO5B_IOMUX_SEL_0[7:4]=4'h4
DQ9	I/O	GPIO5_B0	GPIO5B_IOMUX_SEL_0[3:0]=4'h4
DQ10	I/O	GPIO5_A7	GPIO5A_IOMUX_SEL_1[15:12]=4'h4
DQ11	I/O	GPIO5_A6	GPIO5A_IOMUX_SEL_1[11:8]=4'h4
DQ12	I/O	GPIO5_A5	GPIO5A_IOMUX_SEL_1[7:4]=4'h4
DQ13	I/O	GPIO5_A4	GPIO5A_IOMUX_SEL_1[3:0]=4'h4
DQ14	I/O	GPIO5_A3	GPIO5A_IOMUX_SEL_0[15:12]=4'h4
DQ15	I/O	GPIO5_A2	GPIO5A_IOMUX_SEL_0[11:8]=4'h4
INT0	I	GPIO5_B6	GPIO5B_IOMUX_SEL_1[11:8]=4'h5
INT1	I	GPIO5_B2	GPIO5B_IOMUX_SEL_0[11:8]=4'h5
INT2	I	GPIO5_D3	GPIO5D_IOMUX_SEL_0[15:12]=4'h4
INT3	I	GPIO5_D2	GPIO5D_IOMUX_SEL_0[11:8]=4'h4
RDYN	I	GPIO5_B3	GPIO5B_IOMUX_SEL_0[15:12]=4'h4

Notes: I=input, O=output, I/O=input/output, bidirectional.

40.5 Application Notes

40.5.1 Typical Program Flow for Hyper Device

1. Configure the DSMC_DEV_SIZE according to the size of device applied.
2. Configure the DSMC_MRGTCRx to support merge operation, and the DSMC_BDRTCRx to support crossing the boundary.
3. Configure the DSMC_MTRx to adjust the transfer timing.
4. Configure DSMC_MCRx to access the slave configure register.
5. Set the slave configuration to be consistent with the host, such as write and read latency.
6. Configure DSMC_MCRx to access the slave memory space.

40.5.2 Typical Program Flow for LocalBus Device

1. Configure the DSMC_DEV_SIZE according to the size of device applied.
2. Configure the DSMC_MRGTCRx to support merge operation, and the DSMC_BDRTCRx to support crossing the boundary.
3. Configure the DSMC_MTRx to adjust the transfer timing.
4. Configure the DSMC_VDMCx to LocalBus.
5. Enable the DSMC_WRAP2INCRx function if the slave required.
6. Configure DSMC_MCRx to access the slave configure register.
7. Keep the configuration parameter of the slave is the same as the master.
8. Configure DSMC_MCRx to access the slave memory space.

40.5.3 Chip Select selection

This section describes how to select Chip Select. This controller can't assert two Chip Select at the same time except for the LocalBus write.

When the device size is configured, the 2 address bits higher than device size are used as chip select signals.

40.5.4 Configurable CS# Low Time

This section describes configurable CS# low time. HyperRAM has a regulation for CS# low time (t_{CSM}). To meet CS# low time, a read/write transaction can be regulated by setting MCRx.MAXLEN bit. By MCRx.MAXLEN bit, one transaction is split multi transactions.

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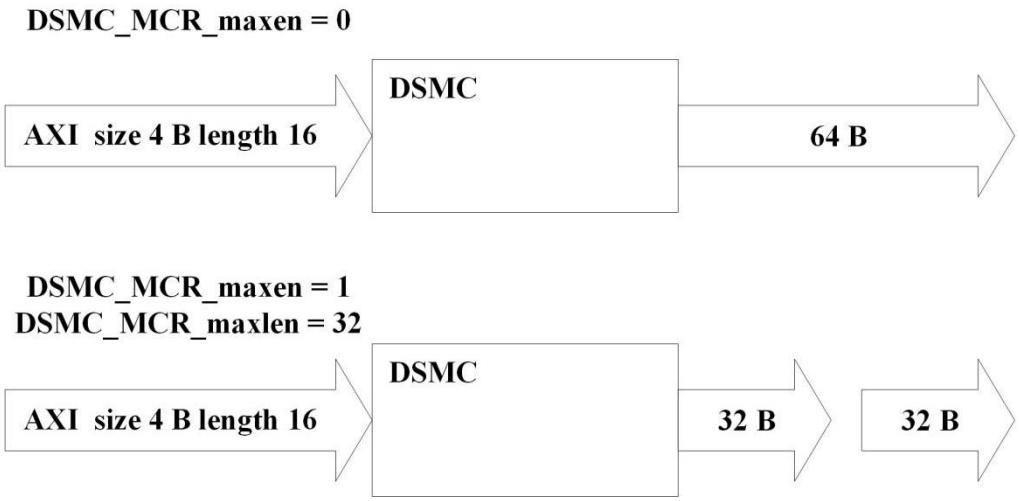

Fig. 40-5 Separated Transaction

40.5.5 Data Map

The data mapping relationship between memory and DSMC interface is shown as below.

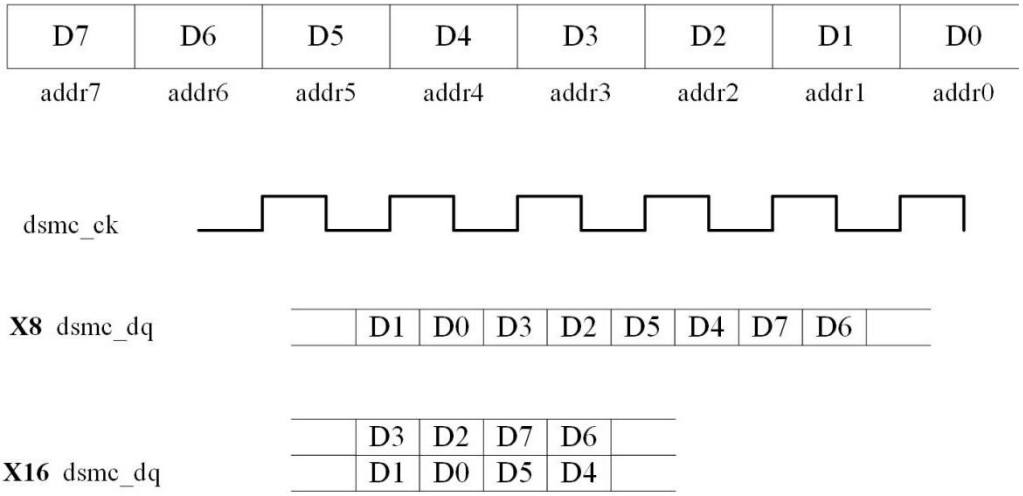

Fig. 40-6 Data Mapping Relationship Between Memory and DSMC Interface

40.5.6 Merge Operation

The merge operation function supports Hyper device and LocalBus device, and it is configured by the DSMC_MRGTCRx register.

- Merge operation removes address output period and latency cycles for subsequent transaction.
- When DSMC Memory Controller IP accepts subsequent read transaction with continuous address, it is merged to one CS# period on DSMC memory interface.

40.5.7 Timing Adjustment

This section describes the DSMC timing adjustment. DSMC core has timing adjustment circuit and timing adjustment is controlled by DSMC_MTRn. RCSHI, RCSS, and RCSH in DSMC_MTRn are used for the read timing adjustment, and WCSHI, WCSS, and WCSH in DSMC_MTRn are used for the write timing adjustment.

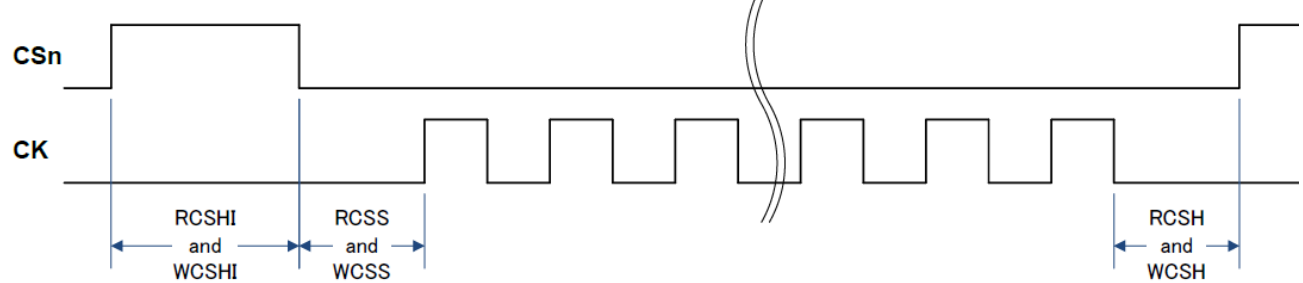

Fig. 40-7 Timing Adjustment

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Chapter 41 Mobile Storage Host Controller (SDMMC,EMMC)

41.1 Overview

The Mobile Storage Host Controller is designed to support Secure Digital memory (SD-max version 3.01) with 1-bit or 4-bit data width, Multimedia Card (MMC-max version 4.51) with 1-bit or 4-bit or 8-bit data width.
The Host Controller is instantiated for SDCARD, SDIO, EMMC. The interface difference between these instances is shown in "Interface Description".
The Host Controller supports following features:

- Bus Interface Features:
- Support AMBA AHB interface for master and slave
- Supports internal DMA interface (IDMAC)
- Supports 16/32-bit data transfers
- Single engine used for Transmit and Receive, which are mutually exclusive
- Dual-buffer and chained descriptor linked list
- Each descriptor can transfer up to 4KB of data in chained mode and 8KB of data in dual-buffer mode
- Programmable burst size for optimal host bus utilization
- Support combined single FIFO for both transmit and receive operations
- Support FIFO size of 256x32
- Support FIFO over-run and under-run prevention by stopping card clock
- Card Interface Features:
- Support Secure Digital memory protocol commands
- Support Secure Digital I/O protocol commands
- Support Multimedia Card protocol commands
- Support Command Completion Signal and interrupts to host
- Support CRC generation and error detection
- Support programmable baud rate
- Support power management and power switch
- Support card detection
- Support write protection
- Support hardware reset
- Support SDIO interrupts in 1-bit and 4-bit modes
- Support 4-bit mode in SDIO3.0
- Support SDIO suspend and resume operation
- Support SDIO read wait
- Support block size of 1 to 65,535 bytes
- Support 1-bit, 4-bit and 8-bit SDR modes
- Supports 4-bit and 8-bit DDR
- Support boot in 1-bit, 4-bit and 8-bit SDR modes
- Clock Interface Features:
- Support 0/90/180/270-degree phase shift operation for sample clock (cclk_in_sample) and drive clock (cclk_in_drv) relative to function clock (cclk_in) respectively
- Support phase tuning using delay line for sample clock (cclk_in_sample) and drive clock (cclk_in_drv) relative to function clock (cclk_in) respectively.
- The max number of delay element is 128. The average delay for every delay element is 39ps~75ps, the total delay is 5ns~9ns, varies with VT.

41.2 Block Diagram

The Host Controller consists of the following main functional blocks.

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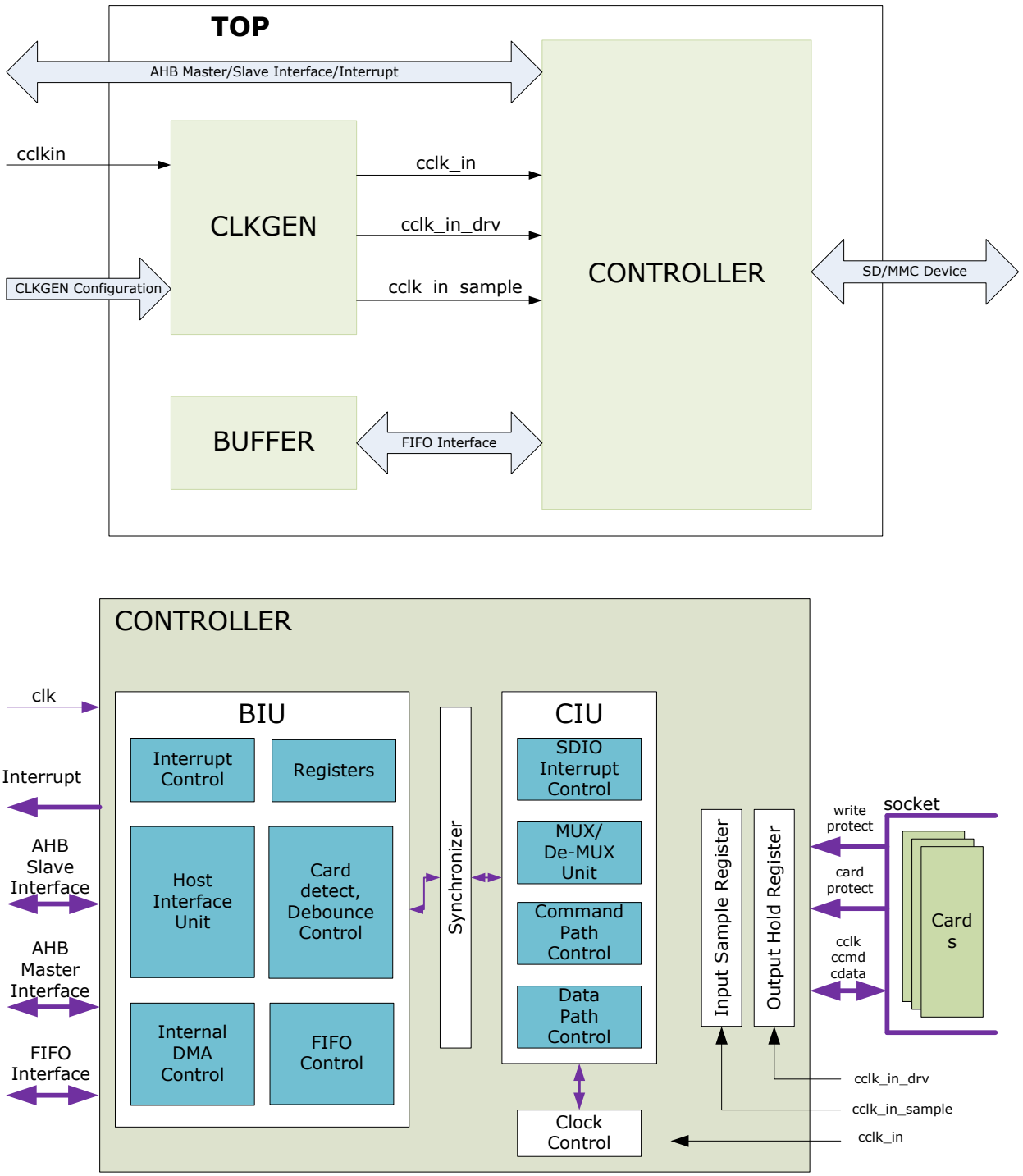

Fig.41-1 Mobile Storage Host Control Block Diagram

- Clock Generate Unit (CLKGEN): Generates card interface clock cclk_in/ cclk_sample/cclk_drv based on cclkin and configuration information.
  - cclkin: original clock
  - cclk_in: functional clock
  - cclk_sample: sample clock
  - cclk_drv: driver clock
- Asynchronous dual-port memory (BUFFER): Use a two-clock synchronous read and synchronous write dual-port RAM. One of the ports is connected to the host clock, and the other port is connected to the card clock.
- Bus Interface Unit (BIU): Provides AMBA AHB interfaces for register and data read/write.
- Card Interface Unit (CIU): Takes care of the SD/MMC protocols and provides clock management.

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41.3 Function Description

41.3.1 Bus Interface Unit

The Bus Interface Unit provides the following functions:

- Host interface
- Interrupt control
- Register access
- External FIFO access
- Card detection

41.3.1.1 Host Interface Unit

The Host Interface Unit is an AHB slave interface, which provides the interface between the SD/MMC card and the host bus.

41.3.1.2 Register Unit

The register unit is part of the bus interface unit; it provides read and write access to the registers.

All registers reside in the Bus Interface Unit clock domain. When a command is sent to a card by setting the start_bit, which is bit[31] of the SDMMC_CMD register, all relevant registers needed for the CIU operation are transferred to the CIU block. During this time, the registers that are transferred from the BIU to the CIU should not be written. The software should wait for the hardware to clear the start bit before writing to these registers again. The register unit has a hardware locking feature to prevent illegal writes to registers. The lock is necessary in order to avoid metastability violations, both because the host and card clock domains are different and to prevent illegal software operations.

Once a command start is issued by setting the start_bit of the SDMMC_CMD register, the following registers cannot be reprogrammed until the command is accepted by the card interface unit:

- SDMMC_CMD
- SDMMC_CMDARG
- SDMMC_BYTCNT
- SDMMC_BLKSIZ
- SDMMC_CLKDIV
- SDMMC_CLKENA
- SDMMC_CLKSRC
- SDMMC_TMOUT
- SDMMC_CTYPE

The hardware resets the start_bit once the CIU accepts the command. If a host write to any of these registers is attempted during this locked time, then the write is ignored and the hardware lock error bit is set in the raw interrupt status register. Additionally, if the interrupt is enabled and not masked for a hardware lock error, then an interrupt is sent to the host.

When the Card Interface Unit is in an idle state, it typically takes the following number of clocks for the command handshake, where clk is the BIU clock and cclk_in is the CIU clock:

3 (clk) + 3 (cclk_in)

Once a command is accepted, you can send another command to the CIU-which has a one-deep command queue-under the following conditions:

- If the previous command was not a data transfer command, the new command is sent to the SD/MMC card once the previous command completes.
- If the previous command is a data transfer command and if wait_prvdata_complete (bit[13]) of the SDMMC_CMD register is set for the new command, the new command is sent to the SD/MMC card only when the data transfer completes.

If the wait_prvdata_complete is 0, then the new command is sent to the SD/MMC card as soon as the previous command is sent. Typically, you should use this only to stop or abort a previous data transfer or query the card status in the middle of a data transfer.

41.3.1.3 Interrupt Controller Unit

The interrupt controller unit generates an interrupt that depends on the controller raw

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interrupt status, the interrupt-mask register, and the global interrupt-enable register bit. Once an interrupt condition is detected, it sets the corresponding interrupt bit in the raw interrupt status register SDMMC_RINTSTS. The raw interrupt status bit stays on until the software clears the bit by writing a 1 to the interrupt bit; a 0 leaves the bit untouched.
The interrupt port is an active-high, level-sensitive interrupt. The interrupt port is active only when any bit in the raw interrupt status register is active, the corresponding interrupt mask bit is 1, and the global interrupt enable bit is 1. The interrupt port is registered in order to avoid any combinational glitches.
The int_enable is reset to 0 on power-on, and the interrupt mask bits are set to 32'h0, which masks all the interrupts.
Notes:
Before enabling the interrupt, it is always recommended that you write 32'hffff_ffff to the raw interrupt status register in order to clear any pending unserviced interrupts. When clearing interrupts during normal operation, ensure that you clear only the interrupt bits that you serviced.
The SDIO Interrupts, Receive FIFO Data Request (RXDR), and Transmit FIFO Data Request (TXDR) are set by level-sensitive interrupt sources. Therefore, the interrupt source should be first cleared before you can clear the interrupt bit of the Raw Interrupt register. For example, on seeing the Receive FIFO Data Request (RXDR) interrupt, the FIFO should be emptied so that the "FIFO count greater than the RX-Watermark" condition, which triggers the interrupt, becomes inactive. The rest of the interrupts are triggered by a single clock-pulse-width source.

Table 41-1 Bits in Interrupt Status Register

Bits	Interrupt	Description
24	sdio_interrupt	Interrupt from SDIO card. In MMC-Ver3.3-only mode, these bits are always 0.
16	Card no-busy	If card exit busy status, the interrupt happened.
15	End Bit Error (read) / Write no CRC (EBE)	Error in end-bit during read operation, or no data CRC received during write operation. For MMC CMD19, there may be no CRC status returned by the card. Hence, EBE is set for CMD19. The application should not treat this as an error.
14	Auto Command Done (ACD)	Stop/abort commands automatically sent by card unit and not initiated by host; similar to Command Done (CD) interrupt. Recommendation: Software typically need not enable this for non CE-ATA accesses; Data Transfer Over (DTO) interrupt that comes after this interrupt determines whether data transfer has correctly competed.
13	Start Bit Error (SBE)	Error in data start bit when data is read from a card. In 4-bit mode, if DAT[0] line indicates start bit-that is, 0-and any of the other data bits do not have start bit, then this error is set. Busy Complete Interrupt when data is written to the card. This interrupt is generated after completion of busy driven by the card after the last data block is written into the card.
12	Hardware Locked write Error (HLE)	During hardware-lock period, write attempted to one of locked registers. When software sets the start_cmd bit in the SDMMC_CMD register, the Host Controller tries to load the command. If the command buffer is already filled with a command, this error is raised. The software then has to reload the command.
11	FIFO Underrun/ Overrun Error (FRUN)	Host tried to push data when FIFO was full, or host tried to read data when FIFO was empty. Typically

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Bits	Interrupt	Description
		this should not happen, except due to error in software. Card unit never pushes data into FIFO when FIFO is full, and pop data when FIFO is empty. If IDMAC is enabled, FIFO under-run/over-run can occur due to a programming error on MSIZE and watermark values in SDMMC_FIFOTH register.
10	Data Starvation by Host Timeout (HTO)	To avoid data loss, card clock out is stopped if FIFO is empty when writing to card, or FIFO is full when reading from card. Whenever card clock is stopped to avoid data loss, data-starvation timeout counter is started with data-timeout value. This interrupt is set if host does not fill data into FIFO during write to card, or does not read from FIFO during read from card before timeout period. Even after timeout, card clock stays in stopped state, with CIU state machines waiting. It is responsibility of host to push or pop data into FIFO upon interrupt, which automatically restarts cclk_out and card state machines. Even if host wants to send stop/abort command, it still needs to ensure it has to push or pop FIFO so that clock starts in order for stop/abort command to send on command signal along with data that is sent or received on data line.
9	Data Read Timeout (DRTO)	In Normal functioning mode: Data read timeout (DRTO) Data timeout occurred. Data Transfer Over (DTO) also set if data timeout occurs. In Boot Mode: Boot Data Start (BDS) When set, indicates that Host Controller has started to receive boot data from the card. A write to this register with a value of 1 clears this interrupt.
8	Response Timeout (RTO)	In normal functioning mode: Response timeout (RTO) Response timeout occurred. Command Done (CD) also set if response timeout occurs. If command involves data transfer and when response times out, no data transfer is attempted by Host Controller. In Boot Mode: Boot Ack Received (BAR) When expect_boot_ack is set, on reception of a boot acknowledge pattern—0-1-0—this interrupt is asserted. A write to this register with a value of 1 clears this interrupt.
7	Data CRC Error (DCRC)	Received Data CRC does not match with locally-generated CRC in CIU. Can also occur if the Write CRC status is incorrectly sampled by the Host.
6	Response CRC Error (RCRC)	Response CRC does not match with locally-generated CRC in CIU.
5	Receive FIFO Data Request (RXDR)	Interrupt set during read operation from card when FIFO level is greater than Receive-Threshold level. Recommendation: In DMA modes, this interrupt should not be enabled. In non-DMA mode: pop RX_WMark + 1 data from FIFO.

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Bits	Interrupt	Description

4	Transmit FIFO Data Request (TXDR)	Interrupt set during write operation to card when FIFO level reaches less than or equal to Transmit-Threshold level.
		Recommendation:
		In DMA modes, this interrupt should not be enabled.
		In non-DMA mode:
		if (pending_bytes > (FIFO_DEPTH - TX_WMark))
		push (FIFO_DEPTH - TX_WMark) data into FIFO
		else
		push pending_bytes data into FIFO

3	Data Transfer Over (DTO)	Indicates Data transfer completed. Though on detection of errors-Start Bit Error, Data CRC error, and so on, DTO may or may not be set; the application must issue CMD12, which ensures that DTO is set. Recommendation: In non-DMA mode, when data is read from card, on seeing interrupt, host should read any pending data from FIFO. In DMA mode, DMA controllers guarantee FIFO is flushed before interrupt. DTO bit is set at the end of the last data block, even if the device asserts MMC busy after the last data block.
2	Command Done (CD)	Command sent to card and got response from card, even if Response Error or CRC error occurs.
1	Response Error (RE)	Error in received response set if one of following occurs: • Transmission bit != 0 • Command index mismatch • End-bit != 1
0	Card-Detect (CDT)	When one or more cards inserted or removed, this interrupt occurs. Software should read card-detect register to determine current card status. Recommendation: After power-on and before enabling interrupts, software should read card detect register and store it in memory. When interrupt occurs, it should read card detect register and compare it with value stored in memory to determine which card(s) were removed/inserted. Before exiting ISR, software should update memory with new card-detect value.

41.3.1.4 FIFO Controller Unit

The FIFO controller interfaces the external FIFO to the host interface and the card controller unit. When FIFO overrun and under-run conditions occur, the card clock stops in order to avoid data loss.

The FIFO uses a two-clock synchronous read and synchronous write dual-port RAM. One of the ports is connected to the host clock (clk), and the second port is connected to the card clock (cclk_in).

41.3.1.5 Card Detection Unit

The register unit has registers that control the power. Power to each card can be selectively turned on or off.

The card detection unit looks for any changes in the card-detect signals for card insertion

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or card removal. It filters out the debounce associated with mechanical insertion or removal, and generates one interrupt to the host. You can program the debounce filter value.

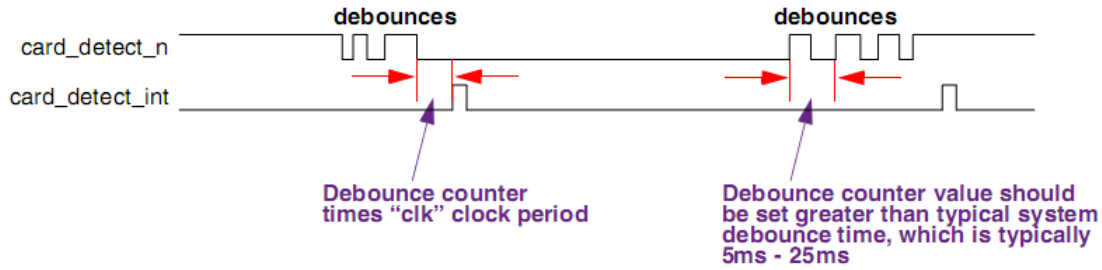

Fig. 41-2 SD/MMC Card-Detect Signal

41.3.2 Card Interface Unit

The Card Interface Unit (CIU) interfaces with the Bus Interface Unit (BIU) and the external devices. The host writes command parameters to the BIU control registers, and these parameters are then passed to the CIU. Depending on control register values, the CIU generates SD/MMC command and data traffic on a selected card bus according to SD/MMC protocol. The Host Controller accordingly controls the command and data path.

The following software restrictions should be met for proper CIU operation:

- Only one data transfer command can be issued at a time.
- During an open-ended card write operation, if the card clock is stopped because the FIFO is empty, the software must first fill the data into the FIFO and start the card clock. It can then issue only a stop/abort command to the card.
- When issuing card reset commands (CMD0, CMD15 or CMD52_reset) while a card data transfer is in progress, the software must set the stop_abort_cmd bit in the SDMMC_CMD register so that the Host Controller can stop the data transfer after issuing the card reset command.
- When the data end bit error is set in the SDMMC_RINTSTS register, the Host Controller does not guarantee SDIO interrupts. The software should ignore the SDIO interrupts and issue the stop/abort command to the card, so that the card stops sending the read data.
- If the card clock is stopped because the FIFO is full during a card read, the software should read at least two FIFO locations to start the card clock.

The CIU block consists of the following primary functional blocks:

- Command path
- Data path
- SDIO interrupt control
- Clock control
- Error detection

41.3.2.1 Command Path

The command path performs the following functions:

- Loads clock parameters
- Loads card command parameters
- Sends commands to card bus (ccmd_out line)
- Receives responses from card bus (ccmd_in line)
- Sends responses to BIU
- Drives the P-bit on command line

A new command is issued to the Host Controller by programming the BIU registers and setting the start_cmd bit in the SDMMC_CMD register. The BIU asserts start_cmd, which indicates that a new command is issued to the SD/MMC device. The command path loads this new command (command, command argument, timeout) and sends acknowledge to the BIU by asserting cmd_taken.

Once the new command is loaded, the command path state machine sends a command to the device bus-including the internally generated CRC7-and receives a response, if any. The state machine then sends the received response and signals to the BIU that the command is done, and then waits for eight clocks before loading a new command.

Load Command Parameters

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One of the following commands or responses is loaded in the command path:

- New command from BIU – When start_cmd is asserted, then the start_cmd bit is set in the SDMMC_CMD register.
- Internally generated auto-stop command – When the data path ends, the stop command request is loaded.
- IRQ response with RCA 0x000 – When the command path is waiting for an IRQ response from the MMC card and a "send irq response" request is signaled by the BIU, then the send_irq_response bit is set in the SDMMC_CTRL register.

Loading a new command from the BIU in the command path depends on the following SDMMC_CMD register bit settings:

- update_clock_registers_only – If this bit is set in the SDMMC_CMD register, the command path updates only the clock enable, clock divider, and clock source registers. If this bit is not set, the command path loads the command, command argument, and timeout registers; it then starts processing the new command.
- wait_prvdata_complete – If this bit is set, the command path loads the new command under one of the following conditions:
- Immediately, if the data path is free (that is, there is no data transfer in progress), or if an open-ended data transfer is in progress (byte_count = 0).
- After completion of the current data transfer, if a predefined data transfer is in progress.

Send Command and Receive Response

Once a new command is loaded in the command path, update_clock_registers_only bit is unset – the command path state machine sends out a command on the device bus; the command path state machine is illustrated in following figure.

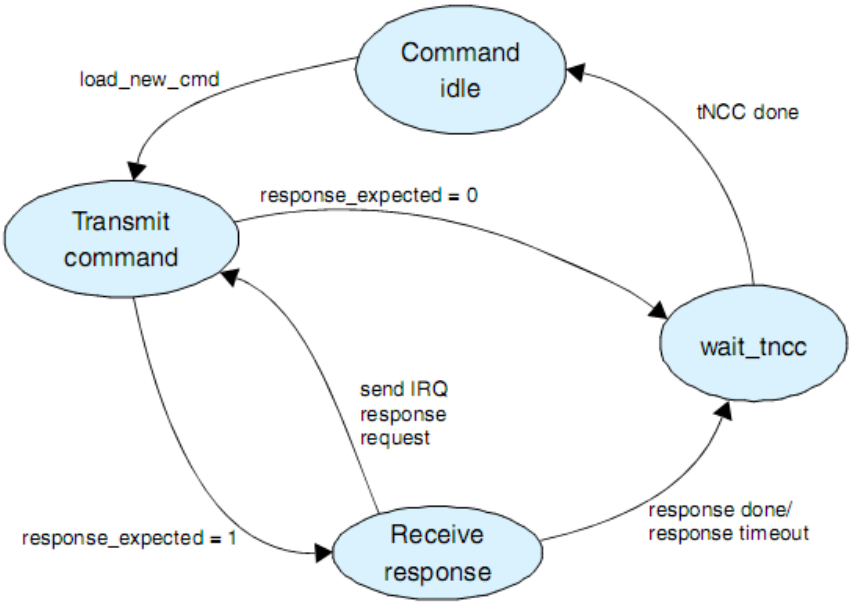

Fig. 41-3 Host Controller Command Path State Machine

The command path state machine performs the following functions, according to SDMMC_CMD register bit values:

- send_initialization – Initialization sequence of 80 clocks is sent before sending the command.
- response_expected – Response is expected for the command. After the command is sent out, the command path state machine receives a 48-bit or 136-bit response and sends it to the BIU. If the start bit of the card response is not received within the number of clocks programmed in the timeout register, then the response timeout and command done bit is set in the Raw Interrupt Status register as a signal to the BIU. If the response-expected bit is not set, the command path sends out a command and signals a response done to the BIU; that is, the command done bit is set in the Raw Interrupt Status register.
- response_length – If this bit is set, a 136-bit response is received; if it is not set, a 48-bit response is received.

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- check_response_crc – If this bit is set, the command path compares CRC7 received in the response with the internally-generated CRC7. If the two do not match, the response CRC error is signaled to the BIU; that is, the response CRC error bit is set in the Raw Interrupt Status register SDMMC_RINTSTS.

Send Response to BIU

If the response_expected bit is set in the SDMMC_CMD register, the received response is sent to the BIU. The Response0 register is updated for a short response, and the Response3, Response2, Response1, and Response0 registers are updated on a long response, after which the Command Done bit is set. If the response is for an auto_stop command sent by the CIU, the response is saved in the Response1 register, after which the Auto Command Done bit is set.

Additionally, the command path checks for the following:

- Transmission bit = 0
- Command index matches command index of the sent command
- End bit = 1 in received card response

The command index is not checked for a 136-bit response or if the check_response_crc bit is unset. For a 136-bit response and reserved CRC 48-bit responses, the command index is reserved-that is, 111111.

Polling Command Completion Signal

The device generates the Command Completion Signal in order to notify the host controller of the normal command completion or command termination.

Command Completion Signal Detection and Interrupt to Host Processor

If the ccs_expected bit is set in the SDMMC_CMD register, the Command Completion Signal (CCS) from the device is indicated by setting the Data Transfer Over (DTO) bit in the SDMMC_RINTSTS register. The Host Controller generates a Data Transfer Over (DTO) interrupt if this interrupt is not masked.

Command Completion Signal Timeout

If the command expects a CCS from the device—if the ccs_expected bit is set in the SDMMC_CMD register—the command state machine waits for the CCS and remains in a wait_CCSS state. If the device fails to send out the CCS, the host software should implement a timeout mechanism to free the command and data path. The host controller does not implement a hardware timer; it is the responsibility of the host software to maintain a software timer.

In the event of a CCS timeout, the host should issue a CCSD by setting the send_ccsd bit in the CTRL register. The host controller command state machine sends the CCSD to the device and exits to an idle state. After sending the CCSD, the host should also send a CMD12 to the device in order to abort the outstanding command.

Send Command Completion Signal Disable

If the send_ccsd bit is set in the SDMMC_CTRL register, the host sends a Command Completion Signal Disable (CCSD) pattern on the CMD line. The host can send the CCSD while waiting for the CCS or after a CCS timeout happens.

After sending the CCSD pattern, the host sets the Command Done (CD) bit in SDMMC_RINTSTS and also generates an interrupt to the host if the Command Done interrupt is not masked.

41.3.2.2 Data Path

The data path block pops the data FIFO and transmits data on cdata_out during a write data transfer, or it receives data on cdata_in and pushes it into the FIFO during a read data transfer. The data path loads new data parameters—that is, data expected, read/write data transfer, stream/block transfer, block size, byte count, card type, timeout registers—whenever a data transfer command is not in progress.

If the data_expected bit is set in the SDMMC_CMD register, the new command is a data transfer command and the data path starts one of the following:

- Transmit data if the read/write bit = 1
- Data receive if read/write bit = 0

Data Transmit

The data transmit state machine, illustrated in following figure, starts data transmission two clocks after a response for the data write command is received; this occurs even if the

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command path detects a response error or response CRC error. If a response is not received from the card because of a response timeout, data is not transmitted. Depending upon the value of the transfer_mode bit in the SDMMC_CMD register, the data transmit state machine puts data on the card data bus in a stream or in block(s).

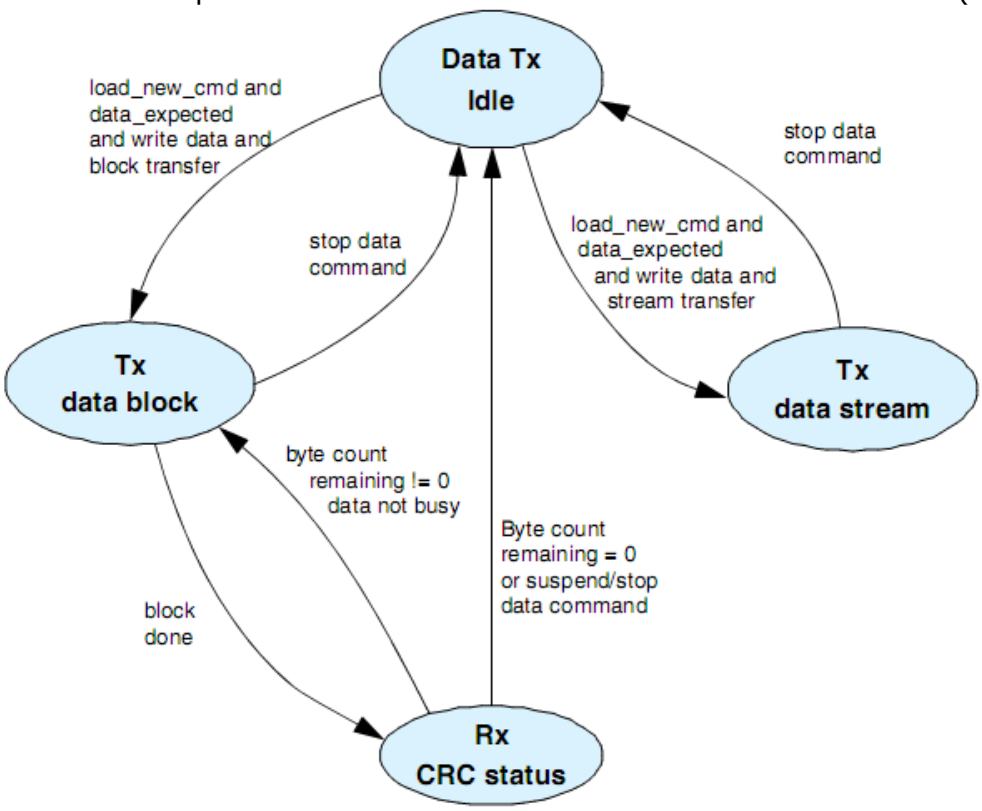

Fig. 41-4 Host Controller Data Transmit State Machine

Stream Data Transmit

If the transfer_mode bit in the SDMMC_CMD register is set to 1, it is a stream-write data transfer. The data path pops the FIFO from the BIU and transmits in a stream to the card data bus. If the FIFO becomes empty, the card clock is stopped and restarted once data is available in the FIFO.

If the byte_count register is programmed to 0, it is an open-ended stream-write data transfer. During this data transfer, the data path continuously transmits data in a stream until the host software issues a stop command. A stream data transfer is terminated when the end bit of the stop command and end bit of the data match over two clocks.

If the byte_count register is programmed with a non-zero value and the send_auto_stop bit is set in the SDMMC_CMD register, the stop command is internally generated and loaded in the command path when the end bit of the stop command occurs after the last byte of the stream write transfer matches.

This data transfer can also terminate if the host issues a stop command before all the data bytes are transferred to the card bus.

Single Block Data

If the transfer_mode bit in the SDMMC_CMD register is set to 0 and the byte_count register value is equal to the value of the block_size register, a single-block write-data transfer occurs. The data transmit state machine sends data in a single block, where the number of bytes equals the block size, including the internally-generated CRC16.

If the SDMMC_CTYPE register bit for the selected card – indicated by the card_num value in the SDMMC_CMD register – is set for a 1-bit, 4-bit, or 8-bit data transfer, the data is transmitted on 1, 4, or 8 data lines, respectively, and CRC16 is separately generated and transmitted for 1, 4, or 8 data lines, respectively.

After a single data block is transmitted, the data transmit state machine receives the CRC status from the card and signals a data transfer to the BIU; this happens when the data-transfer-over bit is set in the SDMMC_RINTSTS register.

If a negative CRC status is received from the card, the data path signals a data CRC error

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to the BIU by setting the data CRC error bit in the SDMMC_RINTSTS register.
Additionally, if the start bit of the CRC status is not received by two clocks after the end of the data block, a CRC status start bit error is signaled to the BIU by setting the write-no-CRC bit in the SDMMC_RINTSTS register.
Multiple Block Data
A multiple-block write-data transfer occurs if the transfer_mode bit in the SDMMC_CMD register is set to 0 and the value in the byte_count register is not equal to the value of the block_size register. The data transmit state machine sends data in blocks, where the number of bytes in a block equals the block size, including the internally-generated CRC16.
If the SDMMC_CTYPE register bit for the selected card – indicated by the card_num value in the SDMMC_CMD register – is set to 1-bit, 4-bit, or 8-bit data transfer, the data is transmitted on 1, 4, or 8 data lines, respectively, and CRC16 is separately generated and transmitted on 1, 4, or 8 data lines, respectively.
After one data block is transmitted, the data transmit state machine receives the CRC status from the card. If the remaining byte_count becomes 0, the data path signals to the BIU that the data transfer is done; this happens when the data-transfer-over bit is set in the SDMMC_RINTSTS register.
If the remaining data bytes are greater than 0, the data path state machine starts to transmit another data block.
If a negative CRC status is received from the card, the data path signals a data CRC error to the BIU by setting the data CRC error bit in the SDMMC_RINTSTS register, and continues further data transmission until all the bytes are transmitted.
Additionally, if the CRC status start bit is not received by two clocks after the end of a data block, a CRC status start bit error is signaled to the BIU by setting the write-no-CRC bit in the SDMMC_RINTSTS register; further data transfer is terminated.
If the send_auto_stop bit is set in the SDMMC_CMD register, the stop command is internally generated during the transfer of the last data block, where no extra bytes are transferred to the card. The end bit of the stop command may not exactly match the end bit of the CRC status in the last data block.
If the block size is less than 4, 16, or 32 for card data widths of 1 bit, 4 bits, or 8 bits, respectively, the data transmit state machine terminates the data transfer when all the data is transferred, at which time the internally generated stop command is loaded in the command path.
If the byte_count is 0 – the block size must be greater than 0 – it is an open-ended block transfer. The data transmit state machine for this type of data transfer continues the block-write data transfer until the host software issues a stop or abort command.
Data Receive
The data-receive state machine, illustrated in following figure, receives data two clock cycles after the end bit of a data read command, even if the command path detects a response error or response CRC error. If a response is not received from the card because a response timeout occurs, the BIU does not receive a signal that the data transfer is complete; this happens if the command sent by the Host Controller is an illegal operation for the card, which keeps the card from starting a read data transfer.
If data is not received before the data timeout, the data path signals a data timeout to the BIU and an end to the data transfer done. Based on the value of the transfer_mode bit in the SDMMC_CMD register, the data-receive state machine gets data from the card data bus in a stream or block(s).

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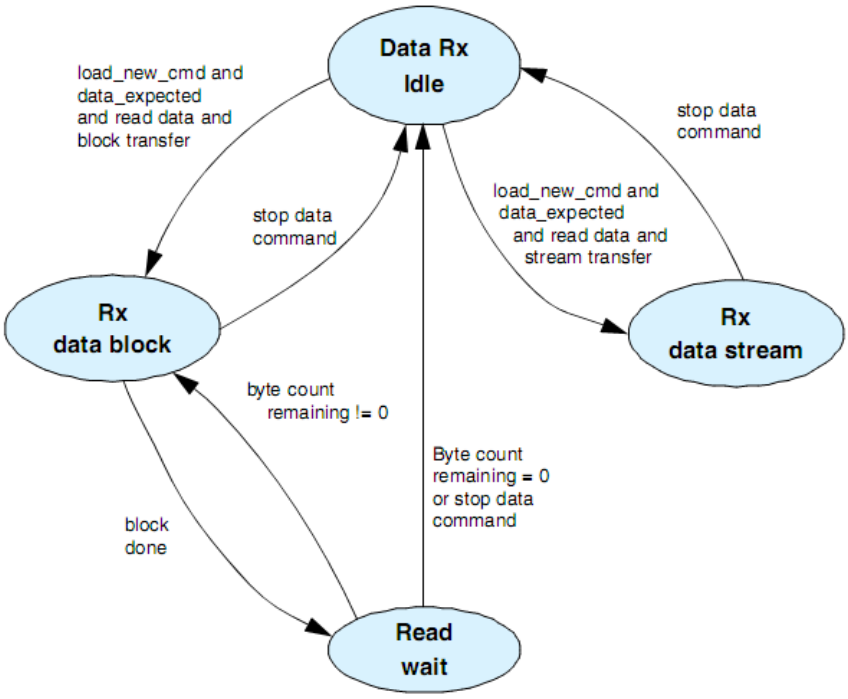

Fig. 41-5 Host Controller Data Receive State Machine

Stream Data Read

A stream-read data transfer occurs if the transfer_mode bit in the SDMMC_CMD register equals 1, at which time the data path receives data from the card and pushes it to the FIFO. If the FIFO becomes full, the card clock stops and restarts once the FIFO is no longer full.

An open-ended stream-read data transfer occurs if the byte_count register equals 0. During this type of data transfer, the data path continuously receives data in a stream until the host software issues a stop command. A stream data transfer terminates two clock cycles after the end bit of the stop command.

If the byte_count register contains a non-zero value and the send_auto_stop bit is set in the SDMMC_CMD register, a stop command is internally generated and loaded into the command path, where the end bit of the stop command occurs after the last byte of the stream data transfer is received. This data transfer can terminate if the host issues a stop or abort command before all the data bytes are received from the card.

Single-Block Data Read

A single-block read-data transfer occurs if the transfer_mode bit in the SDMMC_CMD register is set to 0 and the value of the byte_count register is equal to the value of the block_size register. When a start bit is received before the data times out, data bytes equal to the block size and CRC16 are received and checked with the internally-generated CRC16.

If the SDMMC_CTYPE register bit for the selected card – indicated by the card_num value in the SDMMC_CMD register – is set to a 1-bit, 4-bit, or 8-bit data transfer, data is received from 1, 4, or 8 data lines, respectively, and CRC16 is separately generated and checked for 1, 4, or 8 data lines, respectively. If there is a CRC16 mismatch, the data path signals a data CRC error to the BIU. If the received end bit is not 1, the BIU receives an end-bit error.

Multiple-Block Data Read

If the transfer_mode bit in the SDMMC_CMD register is set to 0 and the value of the byte_count register is not equal to the value of the block_size register, it is a multiple-block read-data transfer. The data-receive state machine receives data in blocks, where the number of bytes in a block is equal to the block size, including the internally-generated CRC16.

If the SDMMC_CTYPE register bit for the selected card – indicated by the card_num value in the SDMMC_CMD register – is set to a 1-bit, 4-bit, or 8-bit data transfer, data is received from 1, 4, or 8 data lines, respectively, and CRC16 is separately generated and checked for 1, 4, or 8 data lines, respectively.

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After a data block is received, if the remaining byte_count becomes 0, the data path signals a data transfer to the BIU.
If the remaining data bytes are greater than 0, the data path state machine causes another data block to be received. If CRC16 of a received data block does not match the internally-generated CRC16, a data CRC error to the BIU and data reception continue further data transmission until all bytes are transmitted.
Additionally, if the end of a received data block is not 1, data on the data path signals terminate the bit error to the CIU and the data-receive state machine terminates data reception, waits for data timeout, and signals to the BIU that the data transfer is complete.
If the send_auto_stop bit is set in the SDMMC_CMD register, the stop command is internally generated when the last data block is transferred, where no extra bytes are transferred from the card; the end bit of the stop command may not exactly match the end bit of the last data block.
If the requested block size for data transfers to cards is less than 4, 16, or 32 bytes for 1-bit, 4-bit, or 8-bit data transfer modes, respectively, the data-transmit state machine terminates the data transfer when all data is transferred, at which point the internally-generated stop command is loaded in the command path. Data received from the card after that are then ignored by the data path.
If the byte_count is 0—the block size must be greater than 0—it is an open-ended block transfer. For this type of data transfer, the data-receive state machine continues the block-read data transfer until the host software issues a stop or abort command.
Auto-Stop
The Host Controller internally generates a stop command and is loaded in the command path when the send_auto_stop bit is set in the SDMMC_CMD register.
The software should set the send_auto_stop bit according to details listed in following table.

Table 41-2 Auto-Stop Generation

Card type	Transfer type	Byte Count	send_auto_stop bit set	Comments
MMC	Stream read	0	No	Open-ended stream
MMC	Stream read	>0	Yes	Auto-stop after all bytes transfer
MMC	Stream write	0	No	Open-ended stream
MMC	Stream write	>0	Yes	Auto-stop after all bytes transfer
MMC	Single-block read	>0	No	Byte count =0 is illegal
MMC	Single-block write	>0	No	Byte count =0 is illegal
MMC	Multiple-block read	0	No	Open-ended multiple block
MMC	Multiple-block read	>0	Yes[1]	Pre-defined multiple block
MMC	Multiple-block write	0	No	Open-ended multiple block
MMC	Multiple-block write	>0	Yes[1]	Pre-defined multiple block
SDMEM	Single-block read	>0	No	Byte count =0 is illegal
SDMEM	Single-block write	>0	No	Byte count =0 illegal
SDMEM	Multiple-block read	0	No	Open-ended multiple block
SDMEM	Multiple-block read	>0	Yes	Auto-stop after all bytes transfer
SDMEM	Multiple-block write	0	No	Open-ended multiple block
SDMEM	Multiple-block	>0	Yes	Auto-stop after all bytes

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Card type	Transfer type	Byte Count	send_auto_stop bit set	Comments
	write			transfer
SDIO	Single-block read	>0	No	Byte count =0 is illegal
SDIO	Single-block write	>0	No	Byte count =0 illegal
SDIO	Multiple-block read	0	No	Open-ended multiple block
SDIO	Multiple-block read	>0	No	Pre-defined multiple block
SDIO	Multiple-block write	0	No	Open-ended multiple block
SDIO	Multiple-block write	>0	No	Pre-defined multiple block

①:The condition under which the transfer mode is set to block transfer and byte_count is equal to block size is treated as a single-block data transfer command for both MMC and SD cards. If byte_count = n*block_size (n = 2, 3, …), the condition is treated as a predefined multiple-block data transfer command. In the case of an MMC card, the host software can perform a predefined data transfer in two ways: 1) Issue the CMD23 command before issuing CMD18/CMD25 commands to the card – in this case, issue MD18/CMD25 commands without setting the send_auto_stop bit. 2) Issue CMD18/CMD25 commands without issuing CMD23 command to the card, with the send_auto_stop bit set. In this case, the multiple-block data transfer is terminated by an internally-generated auto-stop command after the programmed byte count.

The following list conditions for the auto-stop command.

- Stream read for MMC card with byte count greater than 0 – The Host Controller generates an internal stop command and loads it into the command path so that the end bit of the stop command is sent out when the last byte of data is read from the card and no extra data byte is received. If the byte count is less than 6 (48 bits), a few extra data bytes are received from the card before the end bit of the stop command is sent.
- Stream write for MMC card with byte count greater than 0 - The Host Controller generates an internal stop command and loads it into the command path so that the end bit of the stop command is sent when the last byte of data is transmitted on the card bus and no extra data byte is transmitted. If the byte count is less than 6 (48 bits), the data path transmits the data last in order to meet the above condition.
- Multiple-block read memory for SD card with byte count greater than 0 – If the block size is less than 4 (single-bit data bus), 16 (4-bit data bus), or 32 (8-bit data bus), the auto-stop command is loaded in the command path after all the bytes are read. Otherwise, the top command is loaded in the command path so that the end bit of the stop command is sent after the last data block is received.
- Multiple-block write memory for SD card with byte count greater than 0 – If the block size is less than 3 (single-bit data bus), 12 (4-bit data bus), or 24 (8-bit data bus), the auto-stop command is loaded in the command path after all data blocks are transmitted. Otherwise, the stop command is loaded in the command path so that the end bit of the stop command is sent after the end bit of the CRC status is received.

Precaution for host software during auto-stop – Whenever an auto-stop command is issued, the host software should not issue a new command to the SD/MMC device until the auto-stop is sent by the Host Controller and the data transfer is complete. If the host issues a new command during a data transfer with the auto-stop in progress, an auto-stop command may be sent after the new command is sent and its response is received; this can delay sending the stop command, which transfers extra data bytes. For a stream write, extra data bytes are erroneous data that can corrupt the card data. If the host wants to terminate the data transfer before the data transfer is complete, it can issue a stop or abort command, in which case the Host Controller does not generate an auto-stop command.

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41.3.2.3 Non-Data Transfer Commands that Use Data Path

Some non-data transfer commands (non-read/write commands) also use the data path. Following table lists the commands and register programming requirements for them.

Table 41-3 Non-data Transfer Commands and Requirements

Base Address [12:8]	CMD 27	CMD 30	CMD 42	ACMD 13	ACMD 22	ACMD 51
SDMMC_CMD register programming						
cmd_index	6'h1B	6'h1E	6'h2A	6'h0D	6'h16	6'h33
response_expect	1	1	1	1	1	1
rResponse_length	0	0	0	0	0	0
check_response_crc	1	1	1	1	1	1
data_expected	1	1	1	1	1	1
read/write	1	0	1	0	0	0
transfer_mode	0	0	0	0	0	0
send_auto_stop	0	0	0	0	0	0
wait_prevdata_complete	0	0	0	0	0	0
stop_abort_cmd	0	0	0	0	0	0
Command Argument register programming						
	stuff bits	32-bit write protect data address	stuff bits	stuff bits	stuff bits	stuff bits
Block Size register programming						
	16	4	Num_bytes①	64	4	8
Byte Count register programming						
	16	4	Num_bytes①	64	4	8

①: Num_bytes = No. of bytes specified as per the lock card data structure (Refer to the SD specification and the MMC specification)

41.3.2.4 SDIO Interrupt Control

Interrupts for SD cards are reported to the BIU by asserting an interrupt signal for two clock cycles. SDIO cards signal an interrupt by asserting cdata_in low during the interrupt period; an interrupt period for the selected card is determined by the interrupt control state machine. An interrupt period is always valid for non-active or non-selected cards, and 1-bit data mode for the selected card. An interrupt period for a wide-bus active or selected card is valid for the following conditions:

- Card is idle
- Non-data transfer command in progress
- Third clock after end bit of data block between two data blocks
- From two clocks after end bit of last data until end bit of next data transfer command

Bear in mind that, in the following situations, the controller does not sample the SDIO interrupt of the selected card when the card data width is 4 bits. Since the SDIO interrupt is level-triggered, it is sampled in a further interrupt period and the host does not lose any SDIO interrupt from the card.

- Read/Write Resume – The CIU treats the resume command as a normal data transfer command. SDIO interrupts during the resume command are handled similarly to other data commands. According to the SDIO specification, for the normal data command the interrupt period ends after the command end bit of the data command; for the resume command, it ends after the response end bit. In the case of the resume command, the Controller stops the interrupt sampling period after the resume command end bit, instead of stopping after the response end bit of the resume command.

Suspend during read transfer – If the read data transfer is suspended by the host, the host sets the abort_read_data bit in the controller to reset the data state machine. In the CIU, the SDIO interrupts are handled such that the interrupt sampling starts after the abort_read_data bit is set by the host. In this case the controller does not sample SDIO

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interrupts between the period from response of the suspend command to setting the abort_read_data bit, and starts sampling after setting the abort_read_data bit.

41.3.2.5 Clock Control

The clock control block provides different clock frequencies required for SD/MMC cards. The cclk_in signal is the source clock (cclk_in >= card max operating frequency) for clock divider of the clock control block. This source clock (cclk_in) is used to generate different card clock frequencies (cclk_out). The card clock can have different clock frequencies, since the card can be a low-speed card or a full-speed card. The Host Controller provides one clock signal (cclk_out).

The clock frequency of a card depends on the following clock control registers:

- Clock Divider register – Internal clock dividers are used to generate different clock frequencies required for card. The division factor for each clock divider can be programmed by writing to the Clock Divider register. A value of 0 represents a clock-divider bypass, a value of 1 represents a divide by 2.
- Clock Control register – cclk_out can be enabled or disabled for each card under the following conditions:
  - clk_enable – cclk_out for a card is enabled if the clk_enable bit for a card in the Clock Control register is programmed (set to 1) or disabled (set to 0).
  - Low-power mode – Low-power mode of a card can be enabled by setting the low-power mode bit of the Clock Control register to 1. If low-power mode is enabled to save card power, the cclk_out is disabled when the card is idle for at least 8 card clock cycles. It is enabled when a new command is loaded and the command path goes to a non-idle state.

Additionally, cclk_out is disabled when an internal FIFO is full – card read (no more data can be received from card) – or when the FIFO is empty – card write (no data is available for transmission). This helps to avoid FIFO overrun and underrun conditions. It is used by the command and data path to qualify cclk_in for driving outputs and sampling inputs at the programmed clock frequency for the selected card, according to the Clock Divider and Clock Source register values.

Under the following conditions, the card clock is stopped or disabled, along with the active clk_en, for the selected card:

- Clock can be disabled by writing to Clock Enable register (clk_en bit = 1).
- If low-power mode is selected and card is idle, or not selected for 8 clocks.
- FIFO is full and data path cannot accept more data from the card and data transfer is incomplete –to avoid FIFO overrun.

FIFO is empty and data path cannot transmit more data to the card and data transfer is incomplete – to avoid FIFO underrun.

41.3.2.6 Error Detection

- Response
  - Response timeout – Response expected with response start bit is not received within programmed number of clocks in timeout register.
  - Response CRC error – Response is expected and check response CRC requested; response CRC7 does not match with the internally-generated CRC7.
  - Response error – Response transmission bit is not 0, command index does not match with the command index of the send command, or response end bit is not 1.
- Data transmit
  - No CRC status – During a write data transfer, if the CRC status start bit is not received two clocks after the end bit of the data block is sent out, the data path does the following:
    - Signals no CRC status error to the BIU
    - Terminates further data transfer
    - Signals data transfer done to the BIU
  - Negative CRC – If the CRC status received after the write data block is negative (that is, not 010), a data CRC error is signaled to the BIU and further data transfer is continued.
  - Data starvation due to empty FIFO – If the FIFO becomes empty during a write data transmission, or if the card clock is stopped and the FIFO remains empty for data

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timeout clocks, then a data-starvation error is signaled to the BIU and the data path continues to wait for data in the FIFO.

- Data receive
  - Data timeout – During a read-data transfer, if the data start bit is not received before the number of clocks that were programmed in the timeout register, the data path does the following:
    - Signals data-timeout error to the BIU
    - Terminates further data transfer
    - Signals data transfer done to BIU
  - Data start bit error – During a 4-bit or 8-bit read-data transfer, if the all-bit data line does not have a start bit, the data path signals a data start bit error to the BIU and waits for a data timeout, after which it signals that the data transfer is done.
  - Data CRC error – During a read-data-block transfer, if the CRC16 received does not match with the internally generated CRC16, the data path signals a data CRC error to the BIU and continues further data transfer.
  - Data end-bit error – During a read-data transfer, if the end bit of the received data is not 1, the data path signals an end-bit error to the BIU, terminates further data transfer, and signals to the BIU that the data transfer is done.

Data starvation due to FIFO full – During a read data transmission and when the FIFO becomes full, the card clock is stopped. If the FIFO remains full for data timeout clocks, a data starvation error is signaled to the BIU (Data Starvation by Host Timeout bit is set in SDMMC_RINTSTS register) and the data path continues to wait for the FIFO to start to empty.

41.3.3 Internal Direct Memory Access Controller (IDMAC)

The Internal Direct Memory Access Controller (IDMAC) has a Control and Status Register (CSR) and a single Transmit/Receive engine, which transfers data from host memory to the device port and vice versa. The controller utilizes a descriptor to efficiently move data from source to destination with minimal Host CPU intervention. You can program the controller to interrupt the Host CPU in situations such as data Transmit and Receive transfer completion from the card, as well as other normal or error conditions.

The IDMAC and the Host driver communicate through a single data structure. CSR addresses 0x80 to 0x98 are reserved for host programming.

The IDMAC transfers the data received from the card to the Data Buffer in the Host memory, and it transfers Transmit data from the Data Buffer in the Host memory to the FIFO. Descriptors that reside in the Host memory act as pointers to these buffers.

A data buffer resides in physical memory space of the Host and consists of complete data or partial data. Buffers contain only data, while buffer status is maintained in the descriptor. Data chaining refers to data that spans multiple data buffers. However, a single descriptor cannot span multiple data.

A single descriptor is used for both reception and transmission. The base address of the list is written into Descriptor List Base Address Register (SDMMC_DBADDR @0x88). A descriptor list is forward linked. The Last Descriptor can point back to the first entry in order to create a ring structure. The descriptor list resides in the physical memory address space of the Host. Each descriptor can point to a maximum of two data buffers.

41.3.3.1 IDMAC CSR Access

When an IDMAC is introduced, an additional CSR space resides in the IDMAC that controls the IDMAC functionality. The host accesses the new CSR space in addition to the existing control register set in the BIU. The IDMAC CSR primarily contains descriptor information. For a write operation to the CSR, the respective CSR logic of the IDMAC and BIU decodes the address before accepting. For a read operation from the CSR, the appropriate CSR read path is enabled.

You can enable or disable the IDMAC operation by programming bit[25] in the SDMMC_CTRL register of the BIU. This allows the data transfer by accessing the slave interface on the AMBA bus if the IDMAC is present but disabled. When IDMAC is enabled, the FIFO cannot be accessed through the slave interface.

41.3.3.2 Descriptors

- Descriptor structures

The IDMAC uses these types of descriptor structures:

- Dual-Buffer Structure – The distance between two descriptors is determined by the Skip Length value programmed in the Descriptor Skip Length (DSL) field of the Bus Mode Register (SDMMC_BMOD @0x80).

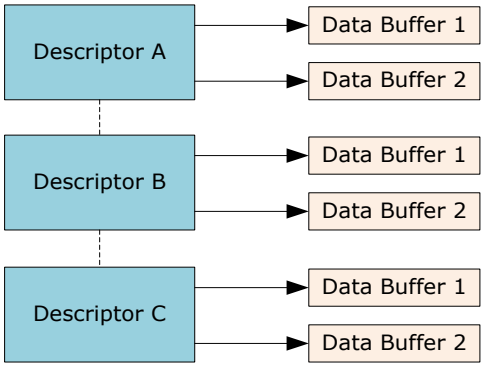

Fig. 41-6 Dual-Buffer Descriptor Structure

- Chain Structure – Each descriptor points to a unique buffer and the next descriptor.

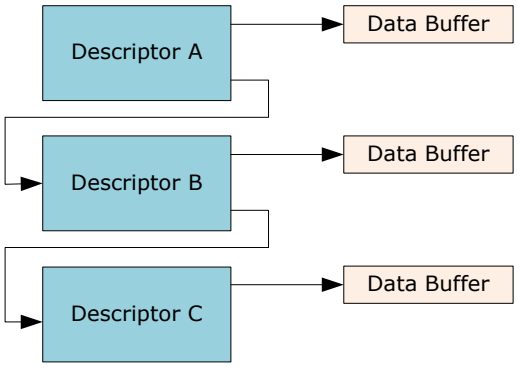

Fig. 41-7 Chain Descriptor Structure

- Descriptor formats

Following figure illustrates the internal formats of a descriptor. The descriptor addresses must be aligned to the bus width used for 32-bit AHB data buses. Each descriptor contains 16 bytes of control and status information. DES0 is a notation used to denote the [31:0] bits, DES1 to denote [63:32] bits, DES2 to denote [95:64] bits, DES3 to denote [127:96] bits.

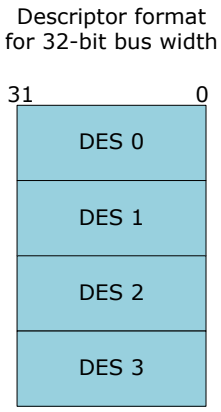

Fig. 41-8 Descriptor Formats for 32-bit AHB Address Bus Width

- The DES0 element in the IDMAC contains control and status information.

Table 41-4 Bits in IDMAC DES0 Element

Bit	Name	Description
31	OWN	When set, this bit indicates that the descriptor is owned by the IDMAC. When this bit is reset, it indicates that the descriptor is owned by the Host. The IDMAC clears this bit when it completes the data

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Bit	Name	Description
		transfer.
30	Card Error Summary (CES)	These error bits indicate the status of the transaction to or from the card. These bits are also present in SDMMC_RINTSTS Indicates the logical OR of the following bits: ● EBE: End Bit Error ● RTO: Response Time out ● RCRC: Response CRC ● SBE: Start Bit Error ● DRTO: Data Read Timeout ● DCRC: Data CRC for Receive ● RE: Response Error
29:6	Reserved	-
5	End of Ring (ER)	When set, this bit indicates that the descriptor list reached its final descriptor. The IDMAC returns to the base address of the list, creating a Descriptor Ring. This is meaningful for only a dual-buffer descriptor structure.
4	Second Address Chained (CH)	When set, this bit indicates that the second address in the descriptor is the Next Descriptor address rather than the second buffer address. When this bit is set, BS2 (DES1[25:13]) should be all zeros.
3	First Descriptor (FS)	When set, this bit indicates that this descriptor contains the first buffer of the data. If the size of the first buffer is 0, next Descriptor contains the beginning of the data.
2	Last Descriptor (LD)	This bit is associated with the last block of a DMA transfer. When set, the bit indicates that the buffers pointed to by this descriptor are the last buffers of the data. After this descriptor is completed, the remaining byte count is 0. In other words, after the descriptor with the LD bit set is completed, the remaining byte count should be 0.
1	Disable Interrupt on Completion (DIC)	When set, this bit will prevent the setting of the TI/RI bit of the IDMAC Status Register (IDSTS) for the data that ends in the buffer pointed to by this descriptor.
0	Reserved	-

■ The DES1 element contains the buffer size.

Table 41-5 Bits in IDMAC DES1 Element

Bit	Name	Description
31:26	Reserved	-
25:13	Buffer 2 Size (BS2)	These bits indicate the second data buffer byte size. The buffer size must be a multiple of 2, 4, or 8, depending upon the bus widths—16, 32, and 64 respectively. In the case where the buffer size is not a multiple of 2, 4, or 8, the resulting behavior is undefined. If this field is 0, the DMA ignores this buffer and proceeds to the next buffer in case of a dual-buffer structure. This field is not valid for chain structure; that is, if DES0[4] is set.
12:0	Buffer 1 Size (BS1)	Indicates the data buffer byte size, which must be a multiple of 2, 4, or 8 bytes, depending upon the bus widths—16, 32, and 64, respectively. In the case where the buffer size is not a multiple of 2, 4, or 8, the resulting behavior is undefined. This field should not be zero. Note: If there is only one buffer to be programmed, you need to use only the Buffer 1, and not Buffer 2.

■ The DES2 element contains the address pointer to the data buffer.

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Table 41-6 Bits in IDMAC DES2 Element

Bit	Name	Description
31:26	Reserved	
25:13	Buffer 2 Size (BS2)	These bits indicate the second data buffer byte size. The buffer size must be a multiple of 2, 4, or 8, depending upon the bus widths—16, 32, and 64 respectively. In the case where the buffer size is not a multiple of 2, 4, or 8, the resulting behavior is undefined. If this field is 0, the DMA ignores this buffer and proceeds to the next buffer in case of a dual-buffer structure. This field is not valid for chain structure; that is, if DES0[4] is set.
12:0	Buffer 1 Size (BS1)	Indicates the data buffer byte size, which must be a multiple of 2, 4, or 8 bytes, depending upon the bus widths—16, 32, and 64, respectively. In the case where the buffer size is not a multiple of 2, 4, or 8, the resulting behavior is undefined. This field should not be zero. Note: If there is only one buffer to be programmed, you need to use only the Buffer 1, and not Buffer 2.

- The DES3 element contains the address pointer to the next descriptor if the present descriptor is not the last descriptor in a chained descriptor structure or the second buffer address for a dual-buffer structure.

Table 41-7 Bits in IDMAC DES3 Element

Bit	Name	Description
31:0	Buffer Address Pointer 2/ Next Descriptor Address (BAP2)	These bits indicate the physical address of the second buffer when the dual-buffer structure is used. If the Second Address Chained (DES0[4]) bit is set, then this address contains the pointer to the physical memory where the Next Descriptor is present. If this is not the last descriptor, then the Next Descriptor address pointer must be bus-width aligned.

41.3.3.3 Initialization

IDMAC initialization occurs as follows:

1) Write to IDMAC Bus Mode Register—SDMMC_BMOD to set Host bus access parameters.
2) Write to IDMAC Interrupt Enable Register—SDMMC_IDINTEN to mask unnecessary interrupt causes.
3) The software driver creates either the Transmit or the Receive descriptor list. Then it writes to IDMAC Descriptor List Base Address Register (SDMMC_DBADDR), providing the IDMAC with the starting address of the list.
4) The IDMAC engine attempts to acquire descriptors from the descriptor lists.

- Host Bus Burst Access

The IDMAC attempts to execute fixed-length burst transfers on the AHB Master interface if configured using the FB bit of the IDMAC Bus Mode register. The maximum burst length is indicated and limited by the PBL field. The descriptors are always accessed in the maximum possible burst-size for the 16-bytes to be read— 16*8/bus-width.
The IDMAC initiates a data transfer only when sufficient space to accommodate the configured burst is available in the FIFO or the number of bytes to the end of data, when less than the configured burst-length.
The IDMAC indicates the start address and the number of transfers required to the AHB Master Interface. When the AHB Interface is configured for fixed-length bursts, then it transfers data using the best combination of INCR4/8/16 and SINGLE transactions. Otherwise, in no fixed-length bursts, it transfers data using INCR (undefined length) and SINGLE transactions.

- Host Data Buffer Alignment

The Transmit and Receive data buffers in host memory must be aligned, depending on the data width.

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- Buffer Size Calculations

The driver knows the amount of data to transmit or receive. For transmitting to the card, the IDMAC transfers the exact number of bytes to the FIFO, indicated by the buffer size field of DES1.

If a descriptor is not marked as last-LS bit of DES0-then the corresponding buffer(s) of the descriptor are full, and the amount of valid data in a buffer is accurately indicated by its buffer size field. If a descriptor is marked as last, then the buffer cannot be full, as indicated by the buffer size in DES1. The driver is aware of the number of locations that are valid in this case.

- Transmission

IDMAC transmission occurs as follows:

1) The Host sets up the elements (DES0-DES3) for transmission and sets the OWN bit (DES0[31]). The Host also prepares the data buffer.
2) The Host programs the write data command in the SDMMC_CMD register in BIU.
3) The Host will also program the required transmit threshold level (TX_WMark field in SDMMC_FIFOTH register).
4) The IDMAC determines that a write data transfer needs to be done as a consequence of step 2.
5) The IDMAC engine fetches the descriptor and checks the OWN bit. If the OWN bit is not set, it means that the host owns the descriptor. In this case the IDMAC enters suspend state and asserts the Descriptor Unable interrupt in the SDMMC_IDSTS register. In such a case, the host needs to release the IDMAC by writing any value to the poll demand register.
6) It will then wait for Command Done (CD) bit and no errors from BIU which indicates that a transfer can be done.
7) The IDMAC engine will now wait for a DMA interface request from BIU. This request will be generated based on the programmed transmit threshold value. For the last bytes of data which can’t be accessed using a burst, SINGLE transfers are performed on AHB Master Interface.
8) The IDMAC fetches the Transmit data from the data buffer in the Host memory and transfers to the FIFO for transmission to card.
9) When data spans across multiple descriptors, the IDMAC will fetch the next descriptor and continue with its operation with the next descriptor. The Last Descriptor bit in the descriptor indicates whether the data spans multiple descriptors or not.
10) When data transmission is complete, status information is updated in SDMMC_IDSTS register by setting Transmit Interrupt, if enabled. Also, the OWN bit is cleared by the IDMAC by performing a write transaction to DES0.

- Reception

IDMAC reception occurs as follows:

1) The Host sets up the element (DES0-DES3) for reception, sets the OWN (DES0[31]).
2) The Host programs the read data command in the SDMMC_CMD register in BIU.
3) The Host will program the required receive threshold level (RX_WMark field in FIFOTH register).
4) The IDMAC determines that a read data transfer needs to be done as a consequence of step 2.
5) The IDMAC engine fetches the descriptor and checks the OWN bit. If the OWN bit is not set, it means that the host owns the descriptor. In this case the DMA enters suspend state and asserts the Descriptor Unable interrupt in the SDMMC_IDSTS register. In such a case, the host needs to release the IDMAC by writing any value to the poll demand register.
6) It will then wait for Command Done (CD) bit and no errors from BIU which indicates that a transfer can be done.
7) The IDMAC engine will now wait for a DMA interface request from BIU. This request will be generated based on the programmed receive threshold value. For the last bytes of data which can’t be accessed using a burst, SINGLE transfers are performed on AHB.
8) The IDMAC fetches the data from the FIFO and transfer to Host memory.

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9) When data spans across multiple descriptors, the IDMAC will fetch the next descriptor and continue with its operation with the next descriptor. The Last Descriptor bit in the descriptor indicates whether the data spans multiple descriptors or not.
10) When data reception is complete, status information is updated in SDMMC_IDSTS register by setting Receive Interrupt, if enabled. Also, the OWN bit is cleared by the IDMAC by performing a write transaction to DES0.

- Interrupts

Interrupts can be generated as a result of various events. SDMMC_IDSTS register contains all the bits that might cause an interrupt. SDMMC_IDINTEN register contains an Enable bit for each of the events that can cause an interrupt.
There are two groups of summary interrupts-Normal and Abnormal-as outlined in SDMMC_IDSTS register. Interrupts are cleared by writing a 1 to the corresponding bit position. When all the enabled interrupts within a group are cleared, the corresponding summary bit is cleared. When both the summary bits are cleared, the interrupt signal dmac_intr_o is de-asserted.
Interrupts are not queued and if the interrupt event occurs before the driver has responded to it, no additional interrupts are generated. For example, Receive Interrupt—SDMMC_IDSTS[1] indicates that one or more data was transferred to the Host buffer. An interrupt is generated only once for simultaneous, multiple events. The driver must scan SDMMC_IDSTS register for the interrupt cause.

41.3.3.4 Variable Delay/Clock Generation Unit

Variable delay mechanism for the cclk_in_drv is useful in order to meet a range of hold-time requirements across modes. Variable delay mechanism for the cclk_in_sample is mandatory and is required to achieve the correct sampling point for data.
The Clock Generation Unit (CLKGEN) includes Phase Shift Unit and Delay Line Unit.
The Phase Shift Unit can shift cclk_in_sample/cclk_in_drv by 0/90/180/270-degree relative to cclk_in. The Delay Line Unit can shift cclk_in_sample/cclk_in_drv step by step in the unit of delay element. The delay value range is 21ps~48ps for every delay element; the max delay element number is 128.
The architecture is as follows.

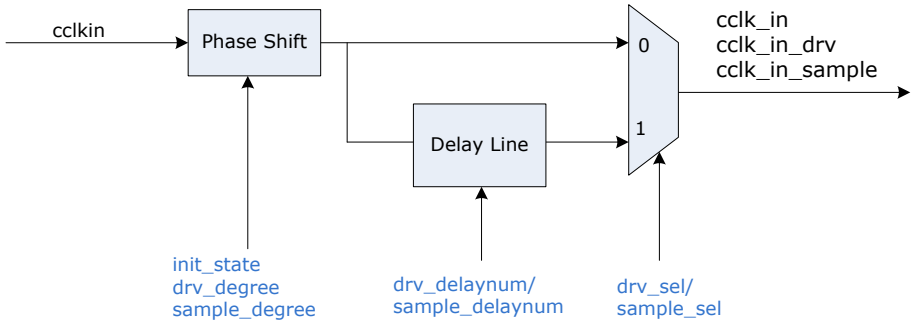

Fig. 41-9 Clock Generation Unit

41.4 Register Description

41.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Operational Base

Name	Base Address
SDCARD_BASE	0x21D60000
SDIO_BASE	0x21F60000
EMMC_BASE	0x21470000

41.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
SDMMC_CTRL	0x0000	W	0x00000000	Control register
SDMMC_PWREN	0x0004	W	0x00000000	Power enable register
SDMMC_CLKDIV	0x0008	W	0x00000000	Clock divider register
SDMMC_CLKSRC	0x000C	W	0x00000000	SD clock source register
SDMMC_CLKENA	0x0010	W	0x00000000	Clock enable register

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Name	Offset	Size	Reset Value	Description
SDMMC_TMOUT	0x0014	W	0xFFFFFF40	Timeout register
SDMMC_CTYPE	0x0018	W	0x00000000	Card type register
SDMMC_BLKSIZ	0x001C	W	0x00000200	Block size register
SDMMC_BYTCNT	0x0020	W	0x00000200	Byte count register
SDMMC_INTMASK	0x0024	W	0x00000000	Interrupt mask register
SDMMC_CMDARG	0x0028	W	0x00000000	Command argument register
SDMMC_CMD	0x002C	W	0x20000000	Command register
SDMMC_RESP0	0x0030	W	0x00000000	Response register 0
SDMMC_RESP1	0x0034	W	0x00000000	Response register 1
SDMMC_RESP2	0x0038	W	0x00000000	Response register 2
SDMMC_RESP3	0x003C	W	0x00000000	Response register 3
SDMMC_MINTSTS	0x0040	W	0x00000000	Masked interrupt status register
SDMMC_RINTSTS	0x0044	W	0x00000000	Raw interrupt status register
SDMMC_STATUS	0x0048	W	0x00000106	Status register
SDMMC_FIFOTH	0x004C	W	0x00FF0000	FIFO threshold register
SDMMC_CDETECT	0x0050	W	0x00000001	Card detect register
SDMMC_WRTPRT	0x0054	W	0x00000000	Write protect register
SDMMC_TCBCNT	0x005C	W	0x00000000	Transferred card byte count register
SDMMC_TBBCNT	0x0060	W	0x00000000	Transferred host to FIFO byte count register
SDMMC_DEBNCE	0x0064	W	0x00FFFFFF	Debounce count register
SDMMC_USRID	0x0068	W	0x20230001	User ID register
SDMMC_VERID	0x006C	W	0x5342270A	Version ID register
SDMMC_HCON	0x0070	W	0x04C434C1	Hardware configuration register
SDMMC_UHSREG	0x0074	W	0x00000000	UHS-1 control register
SDMMC_RSTN	0x0078	W	0x00000001	Hardware reset register
SDMMC_BMOD	0x0080	W	0x00000000	Bus mode register
SDMMC_PLDMND	0x0084	W	0x00000000	Poll demand register
SDMMC_DBADDR	0x0088	W	0x00000000	Descriptor list base address register
SDMMC_IDSTS	0x008C	W	0x00000000	Internal DMAC status register
SDMMC_IDINTEN	0x0090	W	0x00000000	Internal DMAC interrupt enable register
SDMMC_DSCADDR	0x0094	W	0x00000000	Current host descriptor address register
SDMMC_BUFADDR	0x0098	W	0x00000000	Current buffer descriptor address register
SDMMC_CARDTHRCTL	0x0100	W	0x00000000	Card threshold control register
SDMMC_BACKEND_POWER	0x0104	W	0x00000000	Back-end power register
SDMMC_EMMCDDR_REG	0x010C	W	0x00000000	eMMC4.5 DDR start bit detection control register
SDMMC_RDYINT_GEN	0x0120	W	0x00FF0000	Card ready interrupt generation control register
SDMMC_CLKGEN_CON0	0x0130	W	0x00000004	Clock generation control register 0
SDMMC_CLKGEN_CON1	0x0134	W	0x00000004	Clock generation control register 1
SDMMC_MISC_CON	0x0138	W	0x00000000	Miscellaneous control register
SDMMC_FIFO_BASE	0x0200	W	0x00000000	FIFO base address register

Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access

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41.4.3 Detail Registers Description

SDMMC_CTRL

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RW	0x0	use_internal_dmac Present only for the Internal DMAC configuration; else, it is reserved. 1'b0: The host performs data transfers through the slave interface 1'b1: Internal DMAC used for data transfer
24:12	RO	0x0000	reserved
11	RW	0x0	ceata_device_interrupt_status 1'b0: Interrupts not enabled in CE-ATA device 1'b1: Interrupts are enabled in CE-ATA device Software should appropriately write to this bit after power-on reset or any other reset to CE-ATA device. After reset, usually CE-ATA device interrupt is disabled. If the host enables CE-ATA device interrupt, then software should set this bit.
10	RW	0x0	send_auto_stop_ccsd 1'b0: Clear bit if Host Controller does not reset the bit 1'b1: Send internally generated STOP after sending CCSD to CE-ATA device NOTE: Always set send_auto_stop_ccsd and send_ccsd bits together send_auto_stop_ccsd should not be set independent of send_ccsd. When set, the Host Controller automatically sends internally-generated STOP command (CMD12) to CE-ATA device. After sending internally-generated STOP command, Auto Command Done (ACD) bit in SDMMC_RINTSTS is set and generates interrupt to host if Auto Command Done interrupt is not masked. After sending the CCSD, the Host Controller automatically clears send_auto_stop_ccsd bit.
9	RW	0x0	send_ccsd 1'b0: Clear bit if Host Controller does not reset the bit 1'b1: Send Command Completion Signal Disable (CCSD) to CE-ATA device When set, the Host Controller sends CCSD to CE-ATA device. Software sets this bit only if current command is expecting CCS (that is, RW_BLK) and interrupts are enabled in CE-ATA device. Once the CCSD pattern is sent to device, the Host Controller automatically clears send_ccsd bit. It also sets Command Done (CD) bit in SDMMC_RINTSTS register and generates interrupt to host if Command Done interrupt is not masked. NOTE: Once send_ccsd bit is set, it takes two card clock cycles to drive the CCSD on the CMD line. Due to this, during the boundary conditions it may happen that CCSD is sent to the CE-ATA device, even if the device signalled CCS.

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Bit	Attr	Reset Value	Description
8	RW	0x0	abort_read_data 1'b0: No change 1'b1: After suspend command is issued during read-transfer, software polls card to find when suspend happened. Once suspend occurs, software sets bit to reset data state-machine, which is waiting for next block of data. Bit automatically clears once data state machine resets to idle. Used in SDIO card suspend sequence.
7	RW	0x0	send_irq_response 1'b0: No change 1'b1: Send auto IRQ response Bit automatically clears once response is sent. To wait for MMC card interrupts, software issues CMD40, and the Host Controller waits for interrupt response from MMC card. In meantime, if software wants the Controller to exit waiting for interrupt state, it can set this bit, at which time the Host Controller command state-machine sends CMD40 response on bus and returns to idle state.
6	RW	0x0	read_wait 1'b0: Clear read wait 1'b1: Assert read wait For sending read-wait to SDIO cards.
5	RW	0x0	dma_enable 1'b0: Disable DMA transfer mode 1'b1: Enable DMA transfer mode Even when DMA mode is enabled, host can still push/pop data into or from FIFO; this should not happen during the normal operation. If there is simultaneous FIFO access from host/DMA, the data coherency is lost. Also, there is no arbitration inside the controller to prioritize simultaneous host/DMA access.
4	RW	0x0	int_enable Global interrupt enable/disable bit 1'b0: Disable interrupts 1'b1: Enable interrupts The int port is 1 only when this bit is 1 and one or more unmasked interrupts are set.
3	RO	0x0	reserved
2	W1C	0x0	dma_reset 1'b0: No change 1'b1: Reset internal DMA interface control logic To reset DMA interface, firmware should set bit to 1. This bit is auto-cleared after two AHB clocks.
1	W1C	0x0	fifo_reset 1'b0: No change 1'b1: Reset to data FIFO to reset FIFO pointers To reset FIFO, firmware should set bit to 1. This bit is auto-cleared after completion of reset operation.

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Bit	Attr	Reset Value	Description
0	W1C	0x0	controller_reset 1'b0: No change 1'b1: Reset Host Controller To reset Host Controller, firmware should set bit to 1. This bit is auto-cleared after two AHB and two cclk_in clock cycles. This resets: a. BIU/CIU interface b. CIU and state machines c. abort_read_data, send_irq_response, and read_wait bits of SDMMC_CTRL register d. start_cmd bit of SDMMC_CMD register Does not affect any registers or DMA interface, or FIFO or controller interrupts.

SDMMC_PWREN

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	power_enable Power on/off switch for the card. Once power is turned on, firmware should wait for regulator/switch ramp-up time before trying to initialize card. 1'b0: Power off 1'b1: Power on Bit values output to card_power_en port.

SDMMC_CLKDIV

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	clk_divider0 Clock divider-0 value. Clock division is 2*n. For example, value of 0 means divide by 2*0 = 0 (no division, bypass), value of 1 means divide by 2*1 = 2, and so on. The recommended value is 0 or 1.

SDMMC_CLKSRC

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1:0	RW	0x0	clk_source Clock divider source. 2'b00: Clock divider 0 The cclk_out is always from clock divider 0, and this register is not implemented.

SDMMC_CLKENA

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
16	RW	0x0	cclk_low_power Low-power control for SD card clock and MMC card clock supported. 1'b0: Non-low-power mode 1'b1: Low-power mode. Stop clock when card in IDLE (should be normally set to only MMC and SD memory cards; for SDIO cards, if interrupts must be detected, clock should not be stopped).
15:1	RO	0x0000	reserved
0	RW	0x0	cclk_enable Clock-enable control for SD card clock and MMC card clock supported. 1'b0: Clock disabled 1'b1: Clock enabled

SDMMC_TMOUT
Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:8	RW	0xffffff	data_timeout Value for card data read timeout; same value also used for data starvation by host timeout. Value is in number of card output clock. Note: The software timer should be used if the timeout value is in the order of 100 ms. In this case, read data timeout interrupt needs to be disabled.
7:0	RW	0x40	response_timeout Response timeout value. Value is in number of card output clock cclk_out.

SDMMC_CTYPE
Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	card_width_8 Indicates if card is 8-bit. 1'b0: Non 8-bit mode 1'b1: 8-bit mode
15:1	RO	0x0000	reserved
0	RW	0x0	card_width Indicates if card is 1-bit or 4-bit. 1'b0: 1-bit mode 1'b1: 4-bit mode

SDMMC_BLKSIZ
Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0200	block_size Block size

SDMMC_BYTCNT
Address: **Operational Base** + offset (0x0020)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000200	byte_count Number of bytes to be transferred; should be integer multiple of block size for block transfers. For undefined number of byte transfers, byte count should be set to 0. When byte count is set to 0, it is responsibility of host to explicitly send stop/abort command to terminate data transfer.

SDMMC_INTMASK

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	sdio_int_mask 1'b0: SDIO interrupt not masked 1'b1: SDIO interrupt masked
23:17	RO	0x00	reserved
16	RW	0x0	data_nobusy_int_mask 1'b0: Data no busy interrupt not masked 1'b1: Data no busy interrupt masked
15:0	RW	0x0000	int_mask Bits used to mask unwanted interrupts. Value of 0 masks interrupt; value of 1 enables interrupt. bit 15: End-bit error (read)/Write no CRC (EBE) bit 14: Auto command done (ACD) bit 13: Start-bit error (SBE) bit 12: Hardware locked write error (HLE) bit 11: FIFO underrun/overrun error (FRUN) bit 10: Data starvation-by-host timeout (HTO) /Volt_switch_int bit 9: Data read timeout (DRTO) bit 8: Response timeout (RTO) bit 7: Data CRC error (DCRC) bit 6: Response CRC error (RCRC) bit 5: Receive FIFO data request (RXDR) bit 4: Transmit FIFO data request (TXDR) bit 3: Data transfer over (DTO) bit 2: Command done (CD) bit 1: Response error (RE) bit 0: Card detect (CD)

SDMMC_CMDARG

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cmd_arg Value indicates command argument to be passed to card

SDMMC_CMD

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31	RW	0x0	start_cmd Start command. Once command is taken by CIU, bit is cleared. When bit is set, host should not attempt to write to any command registers. If write is attempted, hardware lock error is set in raw interrupt register. Once command is sent and response is received from SD/MMC cards, Command Done bit is set in raw interrupt register.

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Bit	Attr	Reset Value	Description
30	RO	0x0	reserved
29	RW	0x1	use_hold_reg Use hold register. 1'b0: CMD and DATA sent to card bypassing hold register 1'b1: CMD and DATA sent to card through the hold register
28	RW	0x0	volt_switch Voltage switch bit. 1'b0: No voltage switching 1'b1: Voltage switching enabled; must be set for CMD11 only.
27	RW	0x0	boot_mode Boot mode selection. 1'b0: Mandatory boot operation 1'b1: Alternate boot operation
26	RW	0x0	disable_boot Disable boot. When software sets this bit along with start_cmd, CIU terminates the boot operation. Do not set disable_boot and enable_boot together.
25	RW	0x0	expect_boot_ack Expect boot acknowledge. When software sets this bit along with enable_boot, CIU expects a boot acknowledge start pattern of 0-1-0 from the selected card.
24	RW	0x0	enable_boot Enable boot. This bit should be set only for mandatory boot mode. When Software sets this bit along with start_cmd, CIU starts the boot sequence for the corresponding card by asserting the CMD line low. Do not set disable_boot and enable_boot together.
23	RW	0x0	ccs_expected 1'b0: Interrupts are not enabled in CE-ATA device or command does not expect CCS from device 1'b1: Interrupts are enabled in CE-ATA device and RW_BLK command expects command completion signal from CE-ATA device If the command expects command completion signal (CCS) from the CE-ATA device, the software should set this control bit. The Host Controller sets data transfer over (DTO) bit in SDMMC_RINTSTS register and generates interrupt to host if data transfer over interrupt is not masked.
22	RW	0x0	read_ceata_device 1'b0: Host is not performing read access towards CE-ATA device 1'b1: Host is performing read access towards CE-ATA device Software should set this bit to indicate that CE-ATA device is being accessed for read transfer. This bit is used to disable read data timeout indication while performing CE-ATA read transfers. Maximum value of I/O transmission delay can be no less than 10 seconds. The Host Controller should not indicate read data timeout while waiting for data from CE-ATA device.

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Bit	Attr	Reset Value	Description
21	RW	0x0	update_clock_regs_only 1'b0: Normal command sequence 1'b1: Do not send commands, just update clock register value into card clock domain. Following register values transferred into card clock domain: SDMMC_CLKDIV, SDMMC_CLRSRC, SDMMC_CLKENA. Changes card clocks (change frequency, truncate off or on, and set low-frequency mode); provided in order to change clock frequency or stop clock without having to send command to cards. During normal command sequence, when update_clock_regs_only = 0, following control registers are transferred from BIU to CIU: SDMMC_CMD, SDMMC_CMDARG, SDMMC_TMOUT, SDMMC_CTYPE, SDMMC_BLKSIZ, SDMMC_BYTCNT. CIU uses new register values for new command sequence to card. When bit is set, there are no Command Done interrupts because no command is sent to SD_MMC_CEATA cards.
20:16	RO	0x00	reserved
15	RW	0x0	send_initialization 1'b0: Do not send initialization sequence (80 clocks of 1) before sending this command 1'b1: Send initialization sequence before sending this command After power on, 80 clocks must be sent to card for initialization before sending any commands to card. Bit should be set while sending first command to card so that controller will initialize clocks before sending command to card. This bit should not be set for either of the boot modes (alternate or mandatory).
14	RW	0x0	stop_abort_cmd 1'b0: Neither stop nor abort command to stop current data transfer in progress. If abort is sent to function-number currently selected or not in data-transfer mode, then bit should be set to 0. 1'b1: Stop or abort command intended to stop current data transfer in progress. When open-ended or predefined data transfer is in progress, and host issues stop or abort command to stop data transfer, bit should be set so that command/data state-machines of CIU can return correctly to idle state. This is also applicable for Boot mode transfers. To Abort boot mode, this bit should be set along with SDMMC_CMD[26]=disable_boot.
13	RW	0x0	wait_prvdata_complete 1'b0: Send command at once, even if previous data transfer has not completed 1'b1: Wait for previous data transfer completion before sending command The wait_prvdata_complete=0 option typically used to query status of card during data transfer or to stop current data transfer; card_number should be same as in previous command.

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Bit	Attr	Reset Value	Description
12	RW	0x0	send_auto_stop 1'b0: No stop command sent at end of data transfer 1'b1: Send stop command at end of data transfer When set, the Host Controller sends stop command to card at end of data transfer. a. When send_auto_stop bit should be set, since some data transfers do not need explicit stop commands b. Open-ended transfers that software should explicitly send to stop command Additionally, when "resume" is sent to resume-suspended memory access of SD-Combo card, bit should be set correctly if suspended data transfer needs send_auto_stop. Don't care if no data expected from card.
11	RW	0x0	transfer_mode 1'b0: Block data transfer command 1'b1: Stream data transfer command Don't care if no data expected.
10	RW	0x0	wr 1'b0: Read from card 1'b1: Write to card Don't care if no data expected from card.
9	RW	0x0	data_expected 1'b0: No data transfer expected (read/write) 1'b1: Data transfer expected (read/write)
8	RW	0x0	check_response_crc 1'b0: Do not check response CRC 1'b1: Check response CRC Some of command responses do not return valid CRC bits. Software should disable CRC checks for those commands in order to disable CRC checking by controller.
7	RW	0x0	response_length 1'b0: Short response expected from card 1'b1: Long response expected from card
6	RW	0x0	response_expect 1'b0: No response expected from card 1'b1: Response expected from card
5:0	RW	0x00	cmd_index Command index

SDMMC_RESP0

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	response0 Bit[31:0] of response

SDMMC_RESP1

Address: **Operational Base** + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	response1 Register represents bit[63:32] of long response. When CIU sends auto-stop command, then response is saved in register. Response for previous command sent by host is still preserved in response 0 register. Additional auto-stop issued only for data transfer commands, and response type is always "short" for them.

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SDMMC_RESP2
Address: **Operational Base** + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	response2 Bit[95:64] of long response

SDMMC_RESP3
Address: **Operational Base** + offset (0x003C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	response3 Bit[127:96] of long response

SDMMC_MINTSTS
Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RO	0x0	sdio_interrupt SDIO interrupt status when sdio_int_mask is set
23:17	RO	0x00	reserved
16	RW	0x0	data_nobusy_int_status Data no busy interrupt status when data_nobusy_int_mask is set
15:0	RO	0x0000	int_status Interrupt enabled only if corresponding bit in interrupt mask register is set. bit 15: End-bit error (read)/Write no CRC (EBE) bit 14: Auto command done (ACD) bit 13: Start-bit error (SBE) bit 12: Hardware locked write error (HLE) bit 11: FIFO underrun/overrun error (FRUN) bit 10: Data starvation-by-host timeout (HTO) /Volt_switch_int bit 9: Data read timeout (DRTO) bit 8: Response timeout (RTO) bit 7: Data CRC error (DCRC) bit 6: Response CRC error (RCRC) bit 5: Receive FIFO data request (RXDR) bit 4: Transmit FIFO data request (TXDR) bit 3: Data transfer over (DTO) bit 2: Command done (CD) bit 1: Response error (RE) bit 0: Card detect (CD)

SDMMC_RINTSTS
Address: **Operational Base** + offset (0x0044)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	R/WSC	0x0	sdio_interrupt Raw SDIO interrupt status. Write value of 1 clears this bit, and value of 0 leaves bit intact.
23:17	RO	0x00	reserved
16	R/WSC	0x0	data_nobusy_int_status Raw data no busy interrupt status. Write value of 1 clears this bit, and value of 0 leaves bit intact.

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Bit	Attr	Reset Value	Description
15:0	R/WSC	0x0000	int_status Raw interrupt status. Writes to bits clear status bit. Write value of 1 clears status bit, and value of 0 leaves bit intact. bit 15: End-bit error (read)/Write no CRC (EBE) bit 14: Auto command done (ACD) bit 13: Start-bit error (SBE) bit 12: Hardware locked write error (HLE) bit 11: FIFO underrun/overrun error (FRUN) bit 10: Data starvation-by-host timeout (HTO) /Volt_switch_int bit 9: Data read timeout (DRTO) bit 8: Response timeout (RTO) bit 7: Data CRC error (DCRC) bit 6: Response CRC error (RCRC) bit 5: Receive FIFO data request (RXDR) bit 4: Transmit FIFO data request (TXDR) bit 3: Data transfer over (DTO) bit 2: Command done (CD) bit 1: Response error (RE) bit 0: Card detect (CD)

SDMMC_STATUS

Address: **Operational Base** + offset (0x0048)

Bit	Attr	Reset Value	Description
31	RO	0x0	dma_req DMA request signal state
30	RO	0x0	dma_ack DMA acknowledge signal state
29:17	RO	0x0000	fifo_count Number of filled locations in FIFO
16:11	RO	0x00	response_index Index of previous response, including any auto-stop sent by core.
10	RO	0x0	data_state_mc_busy Data transmit or receive state-machine is busy
9	RO	0x0	data_busy Inverted version of raw selected card_data[0]. 1'b0: Card data not busy 1'b1: Card data busy
8	RO	0x1	data_3_status Raw selected card_data[3]; checks whether card is present. 1'b0: Card not present 1'b1: Card present

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Bit	Attr	Reset Value	Description
7:4	RO	0x0	command_fsm_states Command FSM states: 4'h0: Idle 4'h1: Send init sequence 4'h2: Tx cmd start bit 4'h3: Tx cmd tx bit 4'h4: Tx cmd index + arg 4'h5: Tx cmd crc7 4'h6: Tx cmd end bit 4'h7: Tx resp start bit 4'h8: Rx resp IRQ response 4'h9: Rx resp tx bit 4'ha: Rx resp cmd idx 4'hb: Rx resp data 4'hc: Rx resp crc7 4'hd: Rx resp end bit 4'he: Cmd path wait NCC 4'hf: Wait; CMD-to-response turnaround The command FSM state is represented using 19 bits. The SDMMC_STATUS register[7:4] has 4 bits to represent the command FSM states. Using these 4 bits, only 16 states can be represented. Thus three states cannot be represented in the SDMMC_STATUS[7:4] register. The three states that are not represented in the SDMMC_STATUS register[7:4] are: Bit 16: Wait for CCS Bit 17: Send CCSD Bit 18: Boot Mode Due to this, while command FSM is in "Wait for CCS state" or "Send CCSD" or "Boot Mode", the SDMMC_STATUS register indicates status as 0 for the bit field [7:4].
3	RO	0x0	fifo_full FIFO is full status
2	RO	0x1	fifo_empty FIFO is empty status
1	RO	0x1	fifo_tx_watermark FIFO reached Transmit watermark level; not qualified with data transfer.
0	RO	0x0	fifo_rx_watermark FIFO reached Receive watermark level; not qualified with data transfer.

SDMMC_FIFOTH

Address: **Operational Base** + offset (0x004C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
30:28	RW	0x0	dma_mutiple_transaction_size Burst size of multiple transaction; should be programmed same as DMA controller multiple-transaction-size SRC/DEST_MSIZE. 3'b000: 1 transfers 3'b001: 4 transfers 3'b010: 8 transfers 3'b011: 16 transfers 3'b100: 32 transfers 3'b101: 64 transfers 3'b110: 128 transfers 3'b111: 256 transfers The unit for transfer is 32bits.
27:16	RW	0x0ff	rx_wmark FIFO threshold watermark level when receiving data to card. When FIFO data count reaches greater than this number, DMA/FIFO request is raised. During end of packet, request is generated regardless of threshold programming in order to complete any remaining data. In non-DMA mode, when receiver FIFO threshold (RXDR) interrupt is enabled, then interrupt is generated instead of DMA request. During end of packet, interrupt is not generated if threshold programming is larger than any remaining data. It is responsibility of host to read remaining bytes on seeing Data Transfer Done interrupt. In DMA mode, at end of packet, even if remaining bytes are less than threshold, DMA request does single transfers to flush out any remaining bytes before Data Transfer Done interrupt is set. 12 bits-1 bit less than FIFO-count of status register, which is 13 bits. Limitation: rx_wmark <= FIFO_DEPTH-2 Recommended: (FIFO_DEPTH/2) - 1; (means greater than (FIFO_DEPTH/2) - 1) NOTE: In DMA mode during CCS time-out, the DMA does not generate the request at the end of packet, even if remaining bytes are less than threshold. In this case, there will be some data left in the FIFO. It is the responsibility of the application to reset the FIFO after the CCS timeout.
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x000	tx_wmark FIFO threshold watermark level when transmitting data to card. When FIFO data count is less than or equal to this number, DMA/FIFO request is raised. If Interrupt is enabled, then interrupt occurs. During end of packet, request or interrupt is generated, regardless of threshold programming. In non-DMA mode, when transmit FIFO threshold (TXDR) interrupt is enabled, then interrupt is generated instead of DMA request. During end of packet, on last interrupt, host is responsible for filling FIFO with only required remaining bytes (not before FIFO is full or after CIU completes data transfers, because FIFO may not be empty). In DMA mode, at end of packet, if last transfer is less than burst size, DMA controller does single cycles until required bytes are transferred. 12 bits -1 bit less than FIFO-count of status register, which is 13 bits. Limitation: tx_wmark >= 1; Recommended: FIFO_DEPTH/2; (means less than or equal to FIFO_DEPTH/2)

SDMMC_CDETECT
Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x1	card_detect_n Value on card_detect_n input port. 1'b0: Represents presence of card 1'b1: Represents absence of card

SDMMC_WRTPRT
Address: **Operational Base** + offset (0x0054)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	write_protect Value on card_write_prt input port. 1 represents write protection.

SDMMC_TCBCNT
Address: **Operational Base** + offset (0x005C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	trans_card_byte_count Number of bytes transferred by CIU unit to card

SDMMC_TBBCNT
Address: **Operational Base** + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	trans_fifo_byte_count Number of bytes transferred between host/DMA memory and BIU FIFO

SDMMC_DEBNCE
Address: **Operational Base** + offset (0x0064)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0xffffff	debounce_count Number of host clock used by debounce filter logic; typical debounce time is 5-25 ms.

SDMMC_USRID

Address: **Operational Base** + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RW	0x20230001	usrid User identification register

SDMMC_VERID

Address: **Operational Base** + offset (0x006C)

Bit	Attr	Reset Value	Description
31:0	RO	0x5342270a	verid Version identification register

SDMMC_HCON

Address: **Operational Base** + offset (0x0070)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RO	0x1	area_optimized 1'b0: No area optimization 1'b1: Area optimization
25:24	RO	0x0	num_clk_div divider number-1.
23	RO	0x1	set_clk_false_path 1'b0: No false path 1'b1: False path set
22	RO	0x1	impl_hold_reg 1'b0: No hold register 1'b1: Hold register
21	RO	0x0	fifo_ram_inside 1'b0: Outside 1'b1: Inside
20:18	RO	0x1	ge_dma_data_width 3'b000: 16 bits 3'b001: 32 bits 3'b010: 64 bits Others: Reserved
17:16	RO	0x0	dma_interface 2'b00: None 2'b01: INT_DMA 2'b10: GENERIC_DMA 2'b11: NON_INT_DMA
15:10	RO	0x0d	h_addr_width 6'h8: 9 bits 6'h9: 10 bits ..... 6'h1f: 32 bits Others: Reserved

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Bit	Attr	Reset Value	Description
9:7	RO	0x1	h_data_width 3'b000: 16 bits 3'b001: 32 bits 3'b010: 64 bits Others: Reserved
6	RO	0x1	h_bus_type 1'b0: APB 1'b1: AHB
5:1	RO	0x00	card_num Card number -1.
0	RO	0x1	card_type Card type. 1'b0: MMC_ONLY 1'b1: SD_MMC

SDMMC_UHSREG

Address: **Operational Base** + offset (0x0074)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	ddr_reg DDR mode. These bits indicate DDR mode of operation to the core for the data transfer. 1'b0: Non-DDR mode 1'b1: DDR mode
15:0	RO	0x0000	reserved

SDMMC_RSTN

Address: **Operational Base** + offset (0x0078)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x1	card_reset Hardware reset. 1'b0: Active mode 1'b1: Reset These bits cause the cards to enter pre-idle state, which requires them to be re-initialized.

SDMMC_BMOD

Address: **Operational Base** + offset (0x0080)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
10:8	RO	0x0	pbl Programmable burst length. These bits indicate the maximum number of beats to be performed in one IDMAC transaction. The IDMAC will always attempt to burst as specified in PBL each time it starts a Burst transfer on the host bus. The permissible values are 1, 4, 8, 16, 32, 64, 128 and 256. This value is the mirror of MSIZE of SDMMC_FIFOTH register. In order to change this value, write the required value to SDMMC_FIFOTH register. This is an encode value as follows. 3'b000: 1 transfers 3'b001: 4 transfers 3'b010: 8 transfers 3'b011: 16 transfers 3'b100: 32 transfers 3'b101: 64 transfers 3'b110: 128 transfers 3'b111: 256 transfers Transfer unit is 32 bits. PBL is a read-only value and is applicable only for data access; it does not apply to descriptor accesses.
7	RW	0x0	de IDMAC enable. When set, the IDMAC is enabled.
6:2	RW	0x00	dsl Descriptor skip length. Specifies the number of word to skip between two unchained descriptors. This is applicable only for dual buffer structure.
1	RW	0x0	fb Fixed burst. Controls whether the AHB Master interface performs fixed burst transfers or not. When set, the AHB will use only SINGLE, INCR4, INCR8 or INCR16 during start of normal burst transfers. When reset, the AHB will use SINGLE and INCR burst transfer operations.
0	RW	0x0	swr Software reset. When set, the DMA Controller resets all its internal registers. It is automatically cleared after 1 clock cycle.

SDMMC_PLDMND

Address: **Operational Base** + offset (0x0084)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	pd Poll demand. If the OWN bit of a descriptor is not set, the FSM goes to the suspend state. The host needs to write any value into this register for the IDMAC FSM to resume normal descriptor fetch operation.

SDMMC_DBADDR

Address: **Operational Base** + offset (0x0088)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sbl Start of descriptor list. Contains the base address of the first descriptor. The LSB bits[1:0] are ignored and taken as all-zero by the IDMAC internally. Hence these LSB bits are read-only.

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SDMMC_IDSTS
Address: **Operational Base** + offset (0x008C)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:13	RO	0x0	fsm DMAC FSM present state. 4'h0: DMA_IDLE 4'h1: DMA_SUSPEND 4'h2: DESC_RD 4'h3: DESC_CHK 4'h4: DMA_RD_REQ_WAI 4'h5: DMA_WR_REQ_WAI 4'h6: DMA_RD 4'h7: DMA_WR 4'h8: DESC_CLOSE Others: Reserved
12:10	RO	0x0	eb Error bits. Indicates the type of error that caused a bus error. Valid only with fatal bus. 3'h1: Host abort received during transmission 3'h2: Host abort received during reception Others: Reserved
9	RW	0x0	ais Abnormal interrupt summary. Logical OR of the following: SDMMC_IDSTS[2] fatal bus interrupt SDMMC_IDSTS[4] du bit interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes ais to be set is cleared. Writing a 1 clears this bit.
8	RW	0x0	nis Normal interrupt summary. Logical OR of the following: SDMMC_IDSTS[0] transmit interrupt SDMMC_IDSTS[1] receive interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes nis to be set is cleared. Writing a 1 clears this bit.
7:6	RO	0x0	reserved
5	RW	0x0	ces Card error summary. Indicates the status of the transaction to/from the card; also present in SDMMC_RINTSTS. Indicates the logical OR of the following bits: EBE: End Bit Error RTO: Response Timeout/Boot Ack Timeout RCRC: Response CRC SBE: Start Bit Error DRTO: Data Read Timeout/BDS timeout DCRC: Data CRC for Receive RE: Response Error Writing a 1 clears this bit. The abort condition of the IDMAC depends on the setting of this CES bit. If the CES bit is enabled, then the IDMAC aborts on a "response error"; however, it will not abort if the CES bit is cleared.

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Bit	Attr	Reset Value	Description
4	RW	0x0	dui Descriptor unavailable interrupt. This bit is set when the descriptor is unavailable due to OWN bit = 0 (DES0[31] =0). Writing a 1 clears this bit.
3	RO	0x0	reserved
2	RW	0x0	fbe Fatal bus error interrupt. Indicates that a bus error occurred (SDMMC_IDSTS[12:10]). When this bit is set, the DMA disables all its bus accesses. Writing a 1 clears this bit.
1	RW	0x0	ri Receive interrupt. Indicates the completion of data reception for a descriptor. Writing a 1 clears this bit.
0	RW	0x0	ti Transmit interrupt. Indicates that data transmission is finished for a descriptor. Writing 1 clears this bit.

SDMMC_IDINTEN

Address: **Operational Base** + offset (0x0090)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	ai Abnormal interrupt summary enable. When set, an abnormal interrupt is enabled. This bit enables the following bits: SDMMC_IDINTEN[2] fatal bus error interrupt SDMMC_IDINTEN[4] du interrupt
8	RW	0x0	ni Normal interrupt summary enable. When set, a normal interrupt is enabled. When reset, a normal interrupt is disabled. This bit enables the following bits: SDMMC_IDINTEN[0] transmit interrupt SDMMC_IDINTEN[1] receive interrupt
7:6	RO	0x0	reserved
5	RW	0x0	ces Card error summary interrupt enable. When set, it enables the card interrupt summary.
4	RW	0x0	du Descriptor unavailable interrupt. When set along with abnormal interrupt summary enable, the du interrupt is enabled.
3	RO	0x0	reserved
2	RW	0x0	fbe Fatal bus error enable. When set with abnormal interrupt summary enable, the fatal bus error interrupt is enabled. When reset, fatal bus error enable interrupt is disabled.
1	RW	0x0	ri Receive interrupt enable. When set with normal interrupt summary enable, receive interrupt is enabled. When reset, receive interrupt is disabled.

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Bit	Attr	Reset Value	Description
0	RW	0x0	ti Transmit interrupt enable. When set with normal interrupt summary enable, transmit interrupt is enabled. When reset, transmit interrupt is disabled.

SDMMC_DSCADDR

Address: **Operational Base** + offset (0x0094)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hda Host descriptor address pointer. This register points to the start address of the current descriptor read by the IDMAC. Cleared on reset. Pointer updated by IDMAC during operation.

SDMMC_BUFADDR

Address: **Operational Base** + offset (0x0098)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hba Host buffer address pointer. This register points to the current data buffer address being accessed by the IDMAC. Cleared on Reset. Pointer updated by IDMAC during operation.

SDMMC_CARDTHRCTL

Address: **Operational Base** + offset (0x0100)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	card_rd_thres Card read threshold size
15:2	RO	0x0000	reserved
1	RW	0x0	busy_clr_int_en Busy clear interrupt. 1'b0: Busy clear interrupt disabled 1'b1: Busy clear interrupt enabled Note: The application can disable this feature if it does not want to wait for a busy clear interrupt. For example, in a multi-card scenario, the application can switch to the other card without waiting for a busy to be completed. In such cases, the application can use the polling method to determine the status of busy. By default this feature is disabled and backward-compatible to the legacy drivers where polling is used.
0	RW	0x0	card_rd_thres_en Card read threshold enable. 1'b0: Card read threshold disabled 1'b1: Card read threshold enabled. The host initiates read transfer only if card_rd_thres amount of space is available in receive FIFO.

SDMMC_BACKEND_POWER

Address: **Operational Base** + offset (0x0104)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	back_end_power Back end power. 1'b0: Off; Reset 1'b1: Back-end power supplied to card application

SDMMC_EMMCDDR_REG

Address: **Operational Base** + offset (0x010C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	half_start_bit Control for start bit detection mechanism inside Host Controller based on duration of start bit. For eMMC 4.5, start bit can be: 1'b0: Full cycle (half_start_bit=0) 1'b1: Less than one full cycle (half_start_bit=1) Set half_start_bit=1 for eMMC 4.5 and above; set to 0 for SD applications.

SDMMC_RDYINT_GEN

Address: **Operational Base** + offset (0x0120)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RO	0x0	rdyint_cnt_finish Counter finish indication. When high, it indicates that the rdyint counter is finished.
23:16	RO	0xff	rdyint_cnt_status Couner status, reflect internal counter value.
15:9	RO	0x00	reserved
8	RW	0x0	rdyint_gen_working Working indication for rdyint generator. When high, Host Controller start to count and generate one rdyint trigger. After the rdyint trigger is generated, this bit will be set to 0 by Host Controller. So software should set it to 1 before detecting next interrupt.
7:0	RW	0x00	rdyint_gen_maxval Max counter value to detect cdata_in0 high value for generating rdyint, based on internal clock frequency.

SDMMC_CLKGEN_CON0

Address: **Operational Base** + offset (0x0130)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	drv_sel Selection for drive clock. 1'b0: Select clock delayed by phase shift 1'b1: Select clock delayed by phase shift and delay line It can be modified when init_state=1 and should be stable when init_state=0.
10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9:3	RW	0x00	drv_delaynum Delay element number configuration for drive clock. It can be modified when init_state=1 and should be stable when init_state=0.
2:1	RW	0x2	drv_degree Phase selection for drive clock. 2'h0: 0-degree 2'h1: 90-degree 2'h2: 180-degree 2'h3: 270-degree It can be modified when init_state=1 and should be stable when init_state=0.
0	RW	0x0	init_state Enable initialization for clock source. 1'b0: Disable 1'b1: Enable When init_state=1, the host clocks including drive clock and sample clock are inactive.

SDMMC_CLKGEN_CON1

Address: **Operational Base** + offset (0x0134)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:12	RO	0x0	reserved
11	RW	0x0	sample_sel Selection for sample clock. 1'b0: Select clock delayed by phase shift 1'b1: Select clock delayed by phase shift and delay line It can be modified when init_state=1 and should be stable when init_state=0.
10	RO	0x0	reserved
9:3	RW	0x00	sample_delaynum Delay element number configuration for sample clock. It can be modified when init_state=1 and should be stable when init_state=0.
2:1	RW	0x2	sample_degree Phase selection for sample clock. 2'h0: 0-degree 2'h1: 90-degree 2'h2: 180-degree 2'h3: 270-degree It can be modified when init_state=1 and should be stable when init_state=0.
0	RO	0x0	reserved

SDMMC_MISC_CON

Address: **Operational Base** + offset (0x0138)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable

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Bit	Attr	Reset Value	Description
15:6	RO	0x000	reserved
5	RW	0x0	mem_clkgat_enable Memory clock gate enable. 1b0: Disable 1'b1: Enable. Memory clock is gated automatically when memory is idle.
4:0	RO	0x00	reserved

SDMMC_FIFO_BASE
Address: **Operational Base** + offset (0x0200)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	fifo_base_addr FIFO base address

41.5 Interface Description

41.5.1 SDCARD Interface Description

Table 41-8 SDCARD Interface Description

Module Pin	Dir.	PAD Name	IOMUX Setting
sdcard_cclk	O	GPIO2_A4	GPIO2A_IOMUX_SEL_1=4'h1
sdcard_ccmd	I/O	GPIO2_A5	GPIO2A_IOMUX_SEL_1=4'h1
sdcard_cdata0	I/O	GPIO2_A0	GPIO2A_IOMUX_SEL_0=4'h1
sdcard_cdata1	I/O	GPIO2_A1	GPIO2A_IOMUX_SEL_0=4'h1
sdcard_cdata2	I/O	GPIO2_A2	GPIO2A_IOMUX_SEL_0=4'h1
sdcard_cdata3	I/O	GPIO2_A3	GPIO2A_IOMUX_SEL_0=4'h1
sdcard_cdetn	I	GPIO0_A5	GPIO0A_IOMUX_SEL_1=4'h1

Notes: I=input, O=output, I/O=input/output, bidirectional

41.5.2 SDIO Interface Description

Table 41-9 SDIO Interface Description

Module Pin	Dir.	PAD Name	IOMUX Setting
sdio_cclk	O	GPIO3_A0	GPIO3A_IOMUX_SEL_0=4'h1
sdio_ccmd	I/O	GPIO3_A1	GPIO3A_IOMUX_SEL_0=4'h1
sdio_cdata0	I/O	GPIO3_A2	GPIO3A_IOMUX_SEL_0=4'h1
sdio_cdata1	I/O	GPIO3_A3	GPIO3A_IOMUX_SEL_0=4'h1
sdio_cdata2	I/O	GPIO3_A4	GPIO3A_IOMUX_SEL_1=4'h1
sdio_cdata3	I/O	GPIO3_A5	GPIO3A_IOMUX_SEL_1=4'h1
sdio_cdetn	I	GPIO3_B6	GPIO3B_IOMUX_SEL_1=4'h3

Notes: I=input, O=output, I/O=input/output, bidirectional

41.5.3 EMMC Interface Description

Table 41-10 EMMC Interface Description

Module Pin	Dir.	PAD Name	IOMUX Setting
emmc_cclk	O	GPIO1_B3	GPIO1B_IOMUX_SEL_0=4'h1
emmc_ccmd	I/O	GPIO1_B1	GPIO1B_IOMUX_SEL_0=4'h1
emmc_cdata0	I/O	GPIO1_A0	GPIO1A_IOMUX_SEL_0=4'h1
emmc_cdata1	I/O	GPIO1_A1	GPIO1A_IOMUX_SEL_0=4'h1
emmc_cdata2	I/O	GPIO1_A2	GPIO1A_IOMUX_SEL_0=4'h1
emmc_cdata3	I/O	GPIO1_A3	GPIO1A_IOMUX_SEL_0=4'h1
emmc_cdata4	I/O	GPIO1_A4	GPIO1A_IOMUX_SEL_1=4'h1
emmc_cdata5	I/O	GPIO1_A5	GPIO1A_IOMUX_SEL_1=4'h1
emmc_cdata6	I/O	GPIO1_A6	GPIO1A_IOMUX_SEL_1=4'h1
emmc_cdata7	I/O	GPIO1_A7	GPIO1A_IOMUX_SEL_1=4'h1

Notes: I=input, O=output, I/O=input/output, bidirectional

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41.6 Application Notes

41.6.1 Software/Hardware Restriction

Before issuing a new data transfer command, the software should ensure that the card is not busy due to any previous data transfer command. Before changing the card clock frequency, the software must ensure that there are no data or command transfers in progress.

To avoid glitches in the card clock outputs, the software should use the following steps when changing the card clock frequency:

1) Before disable the clocks, ensure that the card is not busy due to any previous data command. To determine this, check for 0 in bit9 of SDMMC_STATUS register.
2) Update the Clock Enable register to disable clock. To ensure completion of any previous command before this update, send a command to the CIU to update the clock registers by setting:

- start_cmd bit
- "update clock registers only" bits
- "wait_previous data complete" bit

Wait for the CIU to take the command by polling for 0 on the start_cmd bit.

3) Set the start_cmd bit to update the Clock Divider and/or Clock Source register, and send a command to the CIU in order to update the clock registers; wait for the CIU to take the command.
4) Set start_cmd to update the Clock Enable register in order to enable the required clocks and send a command to the CIU to update the clock registers; wait for the CIU to take the command.

In non-DMA mode, while reading from a card, the Data Transfer Over (SDMMC_RINTSTS[3]) interrupt occurs as soon as the data transfer from the card is over. There still could be some data left in the FIFO, and the RX_WMark interrupt may or may not occur, depending on the remaining bytes in the FIFO. Software should read any remaining bytes upon seeing the Data Transfer Over (DTO) interrupt. While using the external DMA interface for reading from a card, the DTO interrupt occurs only after all the data is flushed to memory by the DMA interface unit.

While writing to a card in external DMA mode, if an undefined-length transfer is selected by setting the Byte Count Register to 0, the DMA logic will likely request more data than it will send to the card, since it has no way of knowing at which point the software will stop the transfer. The DMA request stops as soon as the DTO is set by the CIU.

If the software issues a controller_reset command by setting control register bit[0] to 1, all the CIU state machines are reset; the FIFO is not cleared. The DMA sends all remaining bytes to the host. In addition to a card-reset, if a FIFO reset is also issued, then:

- Any pending DMA transfer on the bus completes correctly
- DMA data read is ignored
- Write data is unknown(x)

Additionally, if dma_reset is also issued, any pending DMA transfer is abruptly terminated. When the DMA is used, the DMA controller channel should also be reset and reprogrammed.

If any of the previous data commands do not properly terminate, then the software should issue the FIFO reset in order to remove any residual data, if any, in the FIFO. After asserting the FIFO reset, you should wait until this bit is cleared.

One data-transfer requirement between the FIFO and host is that the number of transfers should be a multiple of the FIFO data width (32bits). For example, you want to write only 15 bytes to an SD/MMC card (SDMMC_BYTCNT), the host should write 16 bytes to the FIFO or program the DMA to do 16-byte transfers. The software can still program the Byte Count register to only 15, at which point only 15 bytes will be transferred to the card. Similarly, when 15 bytes are read from a card, the host should still read all 16 bytes from the FIFO.

It is recommended that you not change the FIFO threshold register in the middle of data transfers.

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41.6.2 Programming Sequence

41.6.2.1 Initialization

Following figure illustrates the initialization flow.

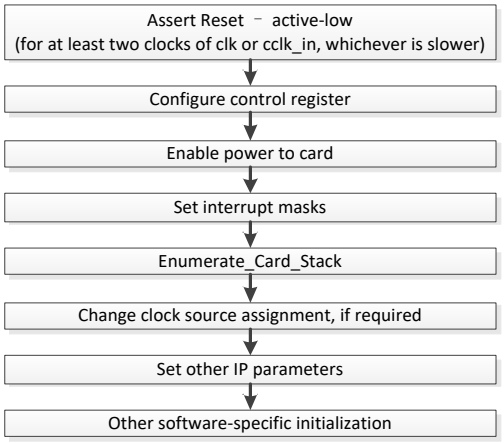

Fig. 41-10 Host Controller Initialization Sequence

Once the power and clocks are stable, reset_n should be asserted (active-low) for at least two cycles of clk or cclk_in, whichever is slower. The reset initializes the registers, ports, FIFO-pointers, DMA interface controls, and state-machines in the design. After power-on reset, the software should do the following:

1) Configure control register – For MMC mode, enable the open-drain pullup by setting enable_OD_pullup (bit24) in the SDMMC_CTRL register.
2) Enable power to cards – Before enabling the power, confirm that the voltage setting to the voltage regulators is correct. Enable power to the connected cards by setting the corresponding bit to 1 in the Power Enable register. Wait for the power ramp-up time.
3) Set masks for interrupts by clearing appropriate bits in the Interrupt Mask register. Set the global int_enable bit of the SDMMC_CTRL register. It is recommended that you write 0xffff_ffff to the Raw Interrupt register in order to clear any pending interrupts before setting the int_enable bit.
4) Enumerate card stack – Each card is enumerated according to card type; for details, refer to "Enumerated Card Stack". For enumeration, you should restrict the clock frequency to 400KHz.
5) Changing clock source assignment – set the card frequency using the clock-divider and clock-source registers; for details, refer to "Clock Programming". MMC cards operate at a maximum of 20MHz (at maximum of 52MHz in high-speed mode). SD mode operates at a maximum of 25MHz (at maximum of 50MHz in high-speed mode).
6) Set other parameters, which normally do not need to be changed with every command, with a typical value such as timeout values in cclk_out according to SD/MMC specifications.

- ResponseTimeOut = 0x64
- DataTimeOut = highest of one of the following:
  - (10*((TAAC*Fop)+(100*NSAC))
  - Host FIFO read/write latency from FIFO empty/full
- Set the debounce value to 25ms (default:0x0fffff) in host clock cycle units in the SDMMC_DEBNCE register.
- FIFO threshold value in bytes in the SDMMC_FIFOTH register. Typically, the threshold value can be set to half the FIFO depth; that is:
  - RX_WMark = (FIFO_DEPTH/2) - 1
  - TX_WMark = FIFO_DEPTH/2

41.6.2.2 Enumerated Card Stack

The card stack does the following:

- Enumerates all connected cards
- Sets the RCA for the connected cards
- Reads card-specific information

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- Stores card-specific information locally

Enumeration depends on the operating mode of the SD/MMC card; the card type is first identified and the appropriate card enumeration routine is called.

1) Check if the card is connected.
2) Clear the card type register to set the card width as a single bit. For the given card number, clear the corresponding bits in the card_type register. Clear the register bit for a 1-bit, 4-bit bus width. For example, for card number=1, clear bit 0 and bit 16 of the card_type register.
3) Set clock frequency to FOD=400KHz, maximum – Program clock divider0 (bits 0-7 in the SDMMC_CLKDIV register) value to one-half of the cclk_in frequency divided by 400KHz. For example, if cclk_in is 20MHz, then the value is 20, 000/(2*400)=25.
4) Identify the card type; that is, SD, MMC, or SDIO.

a. Send CMD5 first. If a response is received, then the card is SDIO
b. If not, send CMD8 with the following Argument

Bit[31:12] = 20'h0 //reserved bits
Bit[11:8] = 4'b0001 //VHS value
Bit[7:0] = 8'b10101010 //Preferred Check Pattern by SD2.0

c. If Response is received the card supports High Capacity SD2.0 then send ACMD41 with the following Argument

Bit[31] = 1'b0; //Reserved bits
Bit[30] = 1'b1; //High Capacity Status
Bit[29:24] = 6'h0; //Reserved bits
Bit[23:0] = Supported Voltage Range

d. If Response is received for ACMD41 then the card is SD. Otherwise the card is MMC.
e. If response is not received for initial CMD8 then card does not support High Capacity SD2.0, then issue CMD0 followed by ACMD41 with the following Argument

Bit[31] = 1'b0; //Reserved bits
Bit[30] = 1'b0; //High Capacity Status
Bit[29:24] = 6'h0; //Reserved bits
Bit[23:0] = Supported Voltage Range

5) Enumerate the card according to the card type.
6) Use a clock source with a frequency = Fod (that is, 400KHz) and use the following enumeration command sequence:

- SD card – Send CMD0, CMD8, ACMD41, CMD2, CMD3.
- MMC – Send CMD0, CMD1, CMD2, CMD3.

41.6.2.3 Clock Programming

The Host Controller supports one clock source. The clock to an individual card can be enabled or disabled. Registers that support this are:

- SDMMC_CLKDIV – Programs individual clock source frequency. SDMMC_CLKDIV limited to 0 or 1 is recommended.
- SDMMC_CLKSRC – Assign clock source for each card.
- SDMMC_CLKENA – Enables or disables clock for individual card and enables low-power mode, which automatically stops the clock to a card when the card is idle for more than 8 clocks.

The Host Controller loads each of these registers only when the start_cmd bit and the update_clk_regs_only bit in the SDMMC_CMD register are set. When a command is successfully loaded, the Host Controller clears this bit, unless the Host Controller already has another command in the queue, at which point it gives an HLE (Hardware Locked Error).

Software should look for the start_cmd and the update_clk_regs_only bits, and should also set the wait_prvdata_complete bit to ensure that clock parameters do not change during data transfer. Note that even though start_cmd is set for updating clock registers, the Host Controller does not raise a command_done signal upon command completion.

The following shows how to program these registers:

1) Confirm that no card is engaged in any transaction; if there is a transaction, wait until it finishes.

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2) Stop all clocks by writing 0 to the SDMMC_CLKENA register. Set the start_cmd, Update_clk_regs_only, and wait_prvdata_complete bits in the SDMMC_CMD register. Wait until start_cmd is cleared or an HLE is set; in case of an HLE, repeat the command.
3) Program the SDMMC_CLKDIV and SDMMC_CLKSRC registers, as required. Set the start_cmd, Update_clk_regs_only, and wait_prvdata_complete bits in the SDMMC_CMD register. Wait until start_cmd is cleared or an HLE is set; in case of an HLE, repeat the command.

Re-enable all clocks by programming the SDMMC_CLKENA register. Set the start_cmd, update_clk_regs_only, and wait_prvdata_complete bits in the SDMMC_CMD register. Wait until start_cmd is cleared or an HLE is set; in case of an HLE, repeat the command.

41.6.2.4 No-Data Command With or Without Response Sequence

To send any non-data command, the software needs to program the SDMMC_CMD register @0x2C and the SDMMC_CMDARG register @0x28 with appropriate parameters. Using these two registers, the Host Controller forms the command and sends it to the command bus. The Host Controller reflects the errors in the command response through the error bits of the SDMMC_RINTSTS register.

When a response is received – either erroneous or valid – the Host Controller sets the command_done bit in the SDMMC_RINTSTS register. A short response is copied in Response Register0, while along response is copied to all four response registers @0x30, 0x34, 0x38, and 0x3C. The Response3 register bit 31 represents the MSB, and the Response0 register bit 0 represents the LSB of a long response.

For basic commands or non-data commands, follow these steps:

1) Program the Command register @0x28 with the appropriate command argument parameter.
2) Program the Command register @0x2C with the settings in following table.

Table 41-11 Command Settings for No-Data Command

Parameter	Value	Description
Default		
start_cmd	1	-
use_hold_reg	1	Choose value based on speed mode being used;ref to “use_hold_reg” on SDMMC_CMD register
update_clk_regs_only	0	No clock parameters update command
data_expected	0	No data command
card number	0	Actual card number (one controller only connect one card, the num is No. 0)
cmd_index	command-index	-
send_initialization	0	Can be 1, but only for card reset commands, such as CMD0
stop_abort_cmd	0	Can be 1 for commands to stop data transfer, such as CMD12
response_length	0	Can be 1 for R2(long) response
response_expect	1	Can be 0 for commands with no response; for example, CMD0, CMD4, CMD15, and so on
User-selectable		
wait_prvdata_complete	1	Before sending command on

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Parameter	Value	Description
		command line, host should wait for completion of any data command in process, if any (recommended to always set this bit, unless the current command is to query status or stop data transfer when transfer is in progress)
check_response_crc	1	If host should crosscheck CRC of response received

3) Wait for command acceptance by host. The following happens when the command is loaded into the Host Controller:

- Host Controller accepts the command for execution and clears the start_cmd bit in the SDMMC_CMD register, unless one command is in process, at which point the Host Controller can load and keep the second command in the buffer.
- If the Host Controller is unable to load the command – that is, a command is already in progress, a second command is in the buffer, and a third command is attempted – then it generates an HLE (hardware-locked error).

4) Check if there is an HLE.
5) Wait for command execution to complete. After receiving either a response from a card or response timeout, the Host Controller sets the command_done bit in the SDMMC_RINTSTS register. Software can either poll for this bit or respond to a generated interrupt.
6) Check if response_timeout error, response_CRC error, or response error is set. This can be done either by responding to an interrupt raised by these errors or by polling bits 1, 6, and 8 from the SDMMC_RINTSTS register @0x44. If no response error is received, then the response is valid. If required, the software can copy the response from the response registers @0x30-0x3C.

Software should not modify clock parameters while a command is being executed.

41.6.2.5 Data Transfer Commands

Data transfer commands transfer data between the memory card and the Host Controller. To send a data command, the Host Controller needs a command argument, total data size, and block size. Software can receive or send data through the FIFO.

Before a data transfer command, software should confirm that the card is not busy and is in a transfer state, which can be done using the CMD13 and CMD7 commands, respectively.

For the data transfer commands, it is important that the same bus width that is programmed in the card should be set in the card type register @0x18.

The Host Controller generates an interrupt for different conditions during data transfer, which are reflected in the SDMMC_RINTSTS register @0x44 as:

1) Data_Transfer_Over (bit 3) – When data transfer is over or terminated. If there is a response timeout error, then the Host Controller does not attempt any data transfer and the "Data Transfer Over" bit is never set.
2) Transmit_FIFO_Data_request (bit 4) – FIFO threshold for transmitting data was reached; software is expected to write data, if available, in FIFO.
3) Receive_FIFO_Data_request (bit 5) – FIFO threshold for receiving data was reached; software is expected to read data from FIFO.
4) Data starvation by Host timeout (bit 10) – FIFO is empty during transmission or is full during reception. Unless software writes data for empty condition or reads data for full condition, the Host Controller cannot continue with data transfer. The clock to the card has been stopped.
5) Data read timeout error (bit 9) – Card has not sent data within the timeout period.
6) Data CRC error (bit 7) – CRC error occurred during data reception.
7) Start bit error (bit 13) – Start bit was not received during data reception.

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8) End bit error (bit 15) – End bit was not received during data reception or for a write operation; a CRC error is indicated by the card.

Conditions 6), 7), and 8) indicate that the received data may have errors. If there was a response timeout, then no data transfer occurred.

41.6.2.6 Single-Block or Multiple-Block Read

Steps involved in a single-block or multiple-block read are:

1) Write the data size in bytes in the SDMMC_BYTCNT register @0x20.
2) Write the block size in bytes in the SDMMC_BLKSIZ register @0x1C. The Host Controller expects data from the card in blocks of size SDMMC_BLKSIZ each.
3) Program the SDMMC_CMDARG register @0x28 with the data address of the beginning of a data read.
4) Program the Command register with the parameters listed in following table. For SD and MMC cards, use CMD17 for a single-block read and CMD18 for a multiple-block read. For SDIO cards, use CMD53 for both single-block and multiple-block transfers.

Table 41-12 Command Setting for Single or Multiple-Block Read

Parameter	Value	Description
Default		
start_cmd	1	-
use_hold_reg	1	Choose value based on speed mode being used;ref to "use_hold_reg" on SDMMC_CMD register
update_clk_regs_only	0	No clock parameters update command
card number	0	Actual card number (one controller only connect one card, the num is No.0)
send_initialization	0	Can be 1, but only for card reset commands, such as CMD0
stop_abort_cmd	0	Can be 1 for commands to stop data transfer, such as CMD12
send_auto_stop	0/1	-
transfer_mode	0	Block transfer
read_write	0	Read from card
data_expected	1	Data command
response_length	0	Can be 1 for R2(long) response
response_expect	1	Can be 0 for commands with no response; for example, CMD0, CMD4, CMD15, and so on
User-selectable		
cmd_index	command-index	-
wait_prvdata_complete	1	0: Sends command immediately 1: Sends command after previous data transfer ends
check_response_crc	1	0: Host Controller should not check response CRC 1: Host Controller should check response CRC

After writing to the SDMMC_CMD register, the Host Controller starts executing the command; when the command is sent to the bus, the command_done interrupt is generated.

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- Software should look for data error interrupts; that is, bits 7, 9, 13, and 15 of the SDMMC_RINTSTS register. If required, software can terminate the data transfer by sending a STOP command.
- Software should look for Receive_FIFO_Data_request and/or data starvation by host timeout conditions. In both cases, the software should read data from the FIFO and make space in the FIFO for receiving more data.

When a Data_Transfer_Over interrupt is received, the software should read the remaining data from the FIFO.

41.6.2.7 Single-Block or Multiple-Block Write

Steps involved in a single-block or multiple-block write are:

1) Write the data size in bytes in the SDMMC_BYTCNT register @0x20.
2) Write the block size in bytes in the SDMMC_BLKSIZ register @0x1C; the Host Controller sends data in blocks of size SDMMC_BLKSIZ each.
3) Program SDMMC_CMDARG register @0x28 with the data address to which data should be written.
4) Write data in the FIFO; it is usually best to start filling data the full depth of the FIFO.
5) Program the Command register with the parameters listed in following table.

Table 41-13 Command Settings for Single or Multiple-Block Write

Parameter	Value	Description
Default		
start_cmd	1	-
use_hold_reg	1	Choose value based on speed mode being used;ref to "use_hold_reg" on SDMMC_CMD register
update_clk_regs_only	0	No clock parameters update command
card number	0	Actual card number (one controller only connect one card, the num is No. 0)
send_initialization	0	Can be 1, but only for card reset commands, such as CMD0
stop_abort_cmd	0	Can be 1 for commands to stop data transfer, such as CMD12
send_auto_stop	0/1	-
transfer_mode	0	Block transfer
read_write	1	Write to card
data_expected	1	Data command
response_length	0	Can be 1 for R2(long) response
response_expect	1	Can be 0 for commands with no response; for example, CMD0, CMD4, CMD15, and so on
User-selectable		
cmd_index	command-index	-
wait_prvdata_complete	1	0: Sends command immediately 1: Sends command after previous data transfer ends
check_response_crc	1	0: Host Controller should not check response CRC 1: Host Controller should check response CRC

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After writing to the SDMMC_CMD register, Host Controller starts executing a command; when the command is sent to the bus, a command_done interrupt is generated.

- Software should look for data error interrupts; that is, for bits 7, 9, and 15 of the SDMMC_RINTSTS register. If required, software can terminate the data transfer by sending the STOP command.
- Software should look for Transmit_FIFO_Data_Request and/or timeout conditions from data starvation by the host. In both cases, the software should write data into the FIFO.

When a Data_Transfer_Over interrupt is received, the data command is over. For an open-ended block transfer, if the byte count is 0, the software must send the STOP command. If the byte count is not 0, then upon completion of a transfer of a given number of bytes, the Host Controller should send the STOP command, if necessary. Completion of the AUTO-STOP command is reflected by the Auto_command_done interrupt – bit 14 of the SDMMC_RINTSTS register. A response to AUTO_STOP is stored in SDMMC_RESP1 @0x34.

41.6.2.8 Sending Stop or Abort in Middle of Transfer

The STOP command can terminate a data transfer between a memory card and the Controller, while the ABORT command can terminate an I/O data transfer for only the SDIO_IOONLY and SDIO_COMBO cards.

- Send STOP command – Can be sent on the command line while a data transfer is in progress; this command can be sent at any time during a data transfer.

You can also use an additional setting for this command in order to set the Command register bits (5-0) to CMD12 and set bit 14 (stop_abort_cmd) to 1. If stop_abort_cmd is not set to 1, the Controller does not know that the user stopped a data transfer. Reset bit 13 of the Command register (wait_prvdata_complete) to 0 in order to make the Controller send the command at once, even though there is a data transfer in progress.
Send ABORT command – Can be used with only an SDIO_IOONLY or SDIO_COMBO card. To abort the function that is transferring data, program the function number in ASx bits (CCCR register of card, address 0x06, bits (0-2) using CMD52.

41.6.2.9 Read_Wait Sequence

Read_wait is used with only the SDIO card and can temporarily stall the data transfer—either from function or memory—and allow the host to send commands to any function within the SDIO device. The host can stall this transfer for as long as required. The Host Controller provides the facility to signal this stall transfer to the card. The steps for doing this are:

1) Check if the card supports the read_wait facility; read SRW (bit 2) of the CCCR register @0x08. If this bit is 1, then all functions in the card support the read_wait facility. Use CMD52 to read this bit.
2) If the card supports the read_wait signal, then assert it by setting the read_wait (bit 6) in the SDMMC_CTRL register @0x00.

Clear the read_wait bit in the SDMMC_CTRL register.

41.6.2.10 Controller/DMA/FIFO Reset Usage

- Controller reset – Resets the controller by setting the controller_reset bit (bit 0) in the SDMMC_CTRL register; this resets the CIU and state machines, and also resets the BIU-to-CIU interface. Since this reset bit is self-clearing, after issuing the reset, wait until this bit is cleared.
- FIFO reset - Resets the FIFO by setting the fifo_reset bit (bit 1) in the SDMMC_CTRL register; this resets the FIFO pointers and counters of the FIFO. Since this reset bit is self-clearing, after issuing the reset, wait until this bit is cleared.

In external DMA transfer mode, even when the FIFO pointers are reset, if there is a DMA transfer in progress, it could push or pop data to or from the FIFO; the DMA itself completes correctly. In order to clear the FIFO, the software should issue an additional FIFO reset and clear any FIFO under-run or overrun errors in the SDMMC_RAWINTS register caused by the DMA transfers after the FIFO was reset.

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41.6.2.11 Card Read Threshold

When an application needs to perform a Single or Multiple Block Read command, the application must program the SDMMC_CARDTHRCTL register with the appropriate Card Read Threshold size (CardRdThreshold) and set the Card Read Threshold Enable (CardRdThrEnable) bit to 1'b1. This additional programming ensures that the Host controller sends a Read Command only if there is space equal to the Card Read Threshold available in the Rx FIFO. This in turn ensures that the card clock is not stopped in the middle a block of data being transmitted from the card. The Card Read Threshold can be set to the block size of the transfer, which guarantees that there is a minimum of one block size of space in the RxFIFO before the controller enables the card clock. The Card Read Threshold is required when the Round Trip Delay is greater than 0.5cclk_in period.

41.6.2.12 Error Handling

The Host Controller implements error checking; errors are reflected in the SDMMC_RAWINTS register@0x44 and can be communicated to the software through an interrupt, or the software can poll for these bits. Upon power-on, interrupts are disabled (int_enable in the SDMMC_CTRL register is 0), and all the interrupts are masked (bits 0-31 of the SDMMC_INTMASK register; default is 0).

Error handling:

- Response and data timeout errors – For response timeout, software can retry the command. For data timeout, the Host Controller has not received the data start bit – either for the first block or the intermediate block – within the timeout period, so software can either retry the whole data transfer again or retry from a specified block onwards. By reading the contents of the SDMMC_TCBCNT later, the software can decide how many bytes remain to be copied.
- Response errors – Set when an error is received during response reception. In this case, the response that copied in the response registers is invalid. Software can retry the command.
- Data errors – Set when error in data reception are observed; for example, data CRC, start bit not found, end bit not found, and so on. These errors could be set for any block-first block, intermediate block, or last block. On receipt of an error, the software can issue a STOP or ABORT command and retry the command for either whole data or partial data.
- Hardware locked error – Set when the Host Controller cannot load a command issued by software. When software sets the start_cmd bit in the SDMMC_CMD register, the Host Controller tries to load the command. If the command buffer is already filled with a command, this error is raised. The software then has to reload the command.
- FIFO under-run/overrun error – If the FIFO is full and software tries to write data in the FIFO, then an overrun error is set. Conversely, if the FIFO is empty and the software tries to read data from the FIFO, an under-run error is set. Before reading or writing data in the FIFO, the software should read the fifo_empty or fifo_full bits in the Status register.
- Data starvation by host timeout – Raised when the Host Controller is waiting for software intervention to transfer the data to or from the FIFO, but the software does not transfer within the stipulated timeout period. Under this condition and when a read transfer is in process, the software should read data from the FIFO and create space for further data reception. When a transmit operation is in process, the software should fill data in the FIFO in order to start transferring data to the card.
- CRC Error on Command – If a CRC error is detected for a command, the CE-ATA device does not send a response, and a response timeout is expected from the Host Controller. The ATA layer is notified that an MMC transport layer error occurred.

Notes: During a multiple-block data transfer, if a negative CRC status is received from the device, the data path signals a data CRC error to the BIU by setting the data CRC error bit in the SDMMC_RINTSTS register. It then continues further data transmission until all the bytes are transmitted.

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41.6.2.13 Voltage Switching

The Host Controller supports SD 3.0 Ultra High Speed (UHS-1) and is capable of voltage switching in SD-mode, which can be applied to SD High-Capacity (SDHC) and SD Extended Capacity (SDXC) cards. UHS-1 supports only 4-bit mode.
However, whether the IO voltage of 1.8v supported or not is depended on the SoC design.
SD 3.0 UHS-1 supports the following transfer speed modes for UHS-50 and/or UHS-104 cards:

- DS – default-speed up to 25MHz, 3.3V signaling
- HS – high-speed up to 50MHz, 3.3V signaling
- SDR12 – SDR up to SDR 25MHz, 1.8V signaling
- SDR25 – SDR up to 50MHz, 1.8V signaling
- SDR50 – SDR up to 100MHz, 1.8V signaling
- DDR50 – DDR up to 50MHz, 1.8V signaling

Voltage selection can be done in only SD mode. The first CMD0 selects the bus mode-either SD mode or SPI mode. The card must be in SD mode in order for 1.8V signaling mode to apply, during which time the card cannot be switched to SPI mode or 3.3V signaling without a power cycle.
If the System BIOS in an embedded system already knows that it is connected to an SD 3.0 card, then the driver programs the Controller to initiate ACMD41. The software knows from the response of ACMD41 whether or not the card supports voltage switching to 1.8V.

- If bit 32 of ACMD41 response is 1'b1: card supports voltage switching and next command-CMD11-invokes voltage switching sequence. After CMD11 is started, the software must program the IO voltage selection register based on the soc architecture.
- If bit 32 of ACMD41 response is 1'b0: card does not support voltage switching and CMD11 should not be started.

If the card and host controller accept voltage switching, then they support UHS-1 modes of data transfer. After the voltage switch to 1.8V, SDR12 is the default speed.
Since the UHS-1 can be used in only 4-bit mode, the software must start ACMD6 and change the card data width to 4-bit mode; ACMD6 is driven in any of the UHS-1 speeds. If the host wants to select the DDR mode of data transfer, then the software must program the SDMMC_DDR_REG register in the CSR space with the appropriate card number.
To choose from any of the SDR or DDR modes, appropriate values should be programmed in the SDMMC_CLKDIV register.

41.6.2.14 Voltage Switch Operation

The Voltage Switch operation must be performed in SD mode only.

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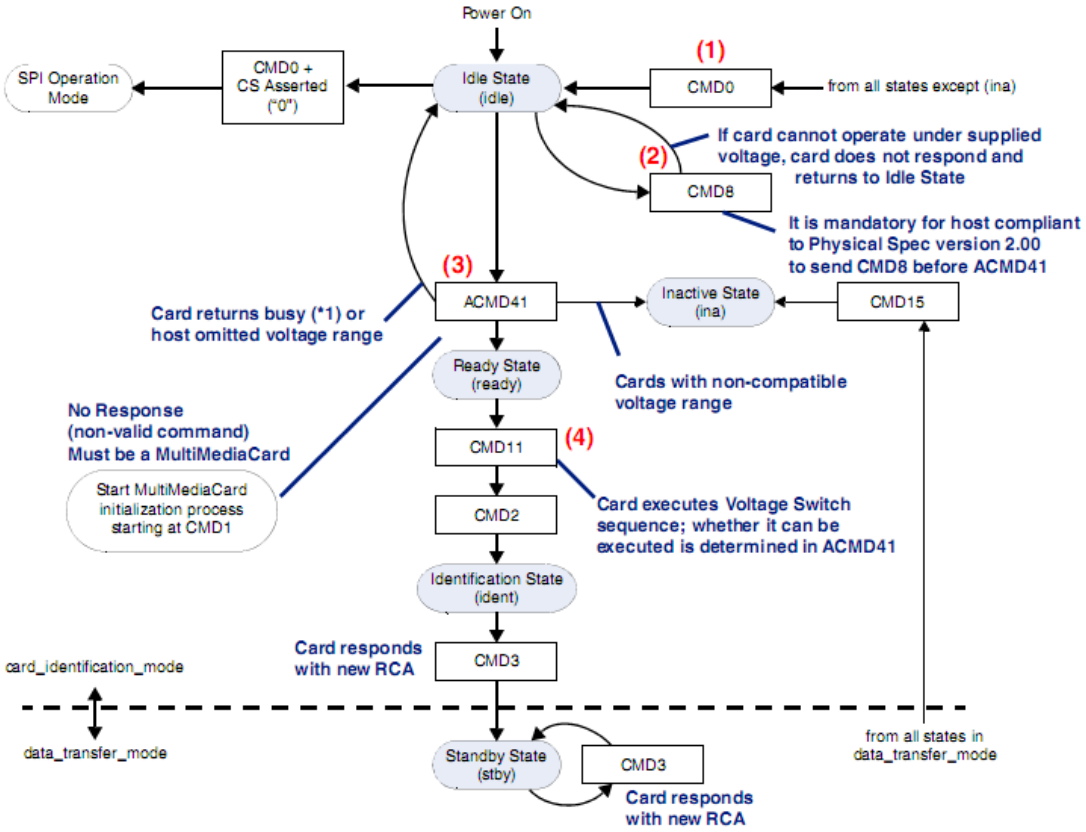

Fig. 41-11 Voltage Switching Command Flow Diagram

The following outlines the steps for the voltage switch programming sequence

1) Software Driver starts CMD0, which selects the bus mode as SD.
2) After the bus is in SD card mode, CMD8 is started in order to verify if the card is compatible with the SD Memory Card Specification, Version 2. 00. CMD8 determines if the card is capable of working within the host supply voltage specified in the VHS (19:16) field of the CMD; the card supports the current host voltage if a response to CMD8 is received.
3) ACMD 41 is started. The response to this command informs the software if the card supports voltage switching; bits 38, 36, and 32 are checked by the card argument of ACMD41; refer to following figure.

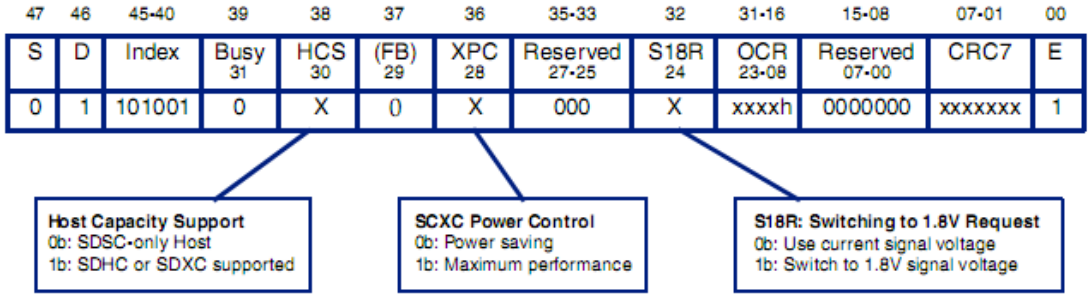

Fig. 41-12 ACMD41 Argument

- Bit 30 informs the card if host supports SDHC/SDXC or not; this bit should be set to 1'b1.
- Bit 28 can be either 1 or 0.
- Bit 24 should be set to 1'b1, indicating that the host is capable of voltage switching; refer to following figure.

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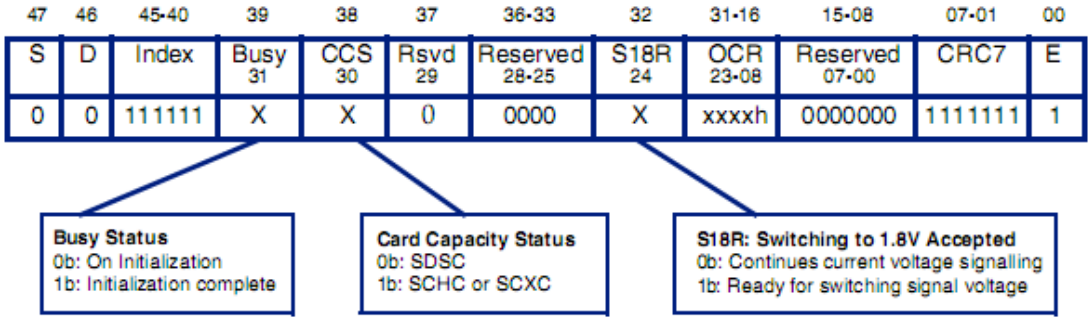

Fig. 41-13 ACMD41 Response (R3)

- Bit 30 – If set to 1'b1, card supports SDHC/SDXC; if set to 1'b0, card supports only SDSC
- Bit 24 – If set to 1'b1, card supports voltage switching and is ready for the switch
- Bit 31 – If set to 1'b1, initialization is over; if set to 1'b0, means initialization in process

If the card supports voltage switching, then the software must perform the steps discussed for either the "Voltage Switch Normal Scenario" or the "Voltage Switch Error Scenario".

41.6.2.15 Voltage Switch Normal Scenario

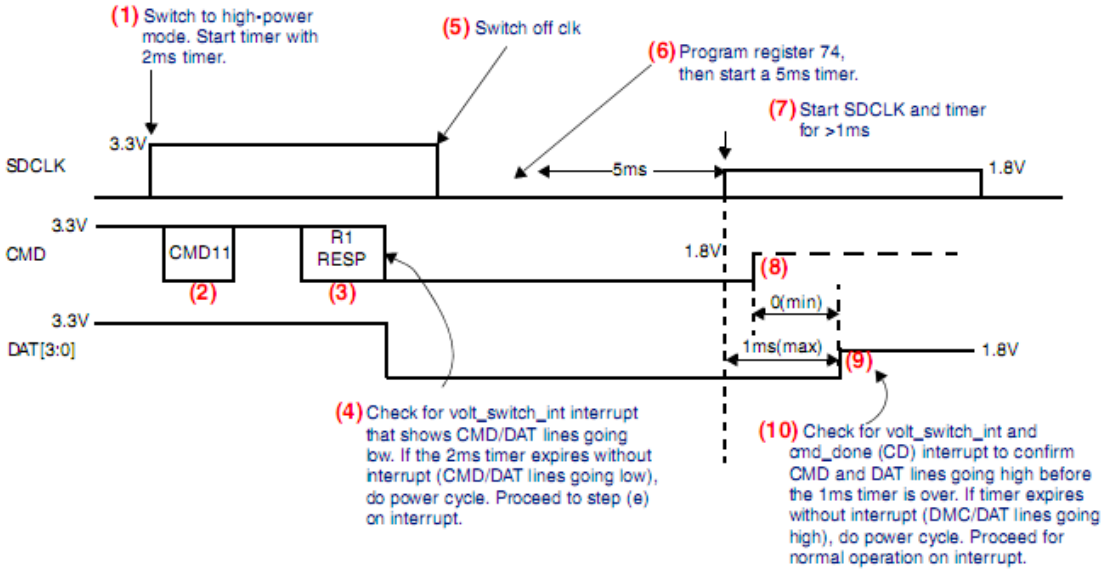

Fig. 41-14 Voltage Switch Normal Scenario

1) The host programs SDMMC_CLKENA—cclk_low_power register—with zero (0) for the corresponding card, which makes the host controller move to high-power mode. The application should start a timer with a recommended value of 2ms; this value of 2 ms is determined as below: Total cycles required for CMD11 = 48 cycles

Total cycles required for RESP R1 = 48 cycles
Maximum clock delay between MCD11 end to start of RESP1 = 60 cycles
Total = 48+48 + 60 = 160
Minimum frequency during enumeration is 100 KHz; that is, 10us
Total time = 160 * 10us = 1600us = 1. 6ms ~ 2ms

2) The host issues CMD11 to start the voltage switch sequence. Set bit 28 to 1'b1 in CMD when setting CMD11; for more information on setting bits, refer to "Boot Operation".
3) The card returns R1 response; the host controller does not generate cmd_done interrupt on receiving R1 response.
4) The card drives CMD and DAT [3:0] to low immediately after the response. The host controller generates interrupt (VOLT_SWITCH_INT) once the CMD or DAT [3:0] line goes low. The application should wait for this interrupt. If the 2ms timer expires without an interrupt (CMD/DAT lines going low), do a power cycle.

Note: Before doing a power cycle, switch off the card clock by programming

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SDMMC_CLKENA register
Proceed to step (5) on getting an interrupt (VOLT_SWITCH_INT).
Note: This interrupt must be cleared once this interrupt is received. Additionally, this interrupt should not be masked during the voltage switch sequence.
If the timer expires without interrupt (CMD/DAT lines going low), perform a power cycle.
Proceed to step (5) on interrupt.

1) Program the SDMMC_CLKENA register, with 0 for the corresponding card; the host stops supplying SDCLK.
2) Program Voltage register to the required values for the corresponding card. The application should start a timer > 5ms.
3) After the 5ms timer expires, the host voltage regulator is stable. Program SDMMC_CLKENA register, with 1 for the corresponding card; the host starts providing SDCLK at 1. 8V; this can be at zero time after Voltage register has been programmed. When the SDMMC_CLKENA register is programmed, the application should start another timer > 1ms.
4) By detecting SDCLK, the card drives CMD to high at 1. 8V for at least one clock and then stops driving (tri-state); CMD is triggered by the rising edge of SDCLK (SDR timing).
5) If switching to 1. 8V signaling is completed successfully, the card drives DAT [3:0] to high at 1. 8V for at least one clock and then stops driving (tri-state); DAT [3:0] is triggered by the rising edge of SDCLK (SDR timing). DAT[3:0] must be high within 1ms from the start of SDCLK.
6) The host controller generates a voltage switch interrupt (VOLT_SWITCH_INT) and a command done (CD) interrupt once the CMD and DAT[3:0] lines go high. The application should wait for this interrupt to confirm CMD and DAT lines going high before the 1ms timer is done.

If the timer expires without the voltage switch interrupt (VOLT_SWITCH_INT), a power cycle should be performed. Program the SDMMC_CLKENA register to stop the clock for the corresponding card number. Wait for the cmd_done (CD) interrupt. Proceed for normal operation on interrupt. After the sequence is completed, the host and the card start communication in SDR12 timing.

41.6.2.16 Voltage Switch Error Scenario

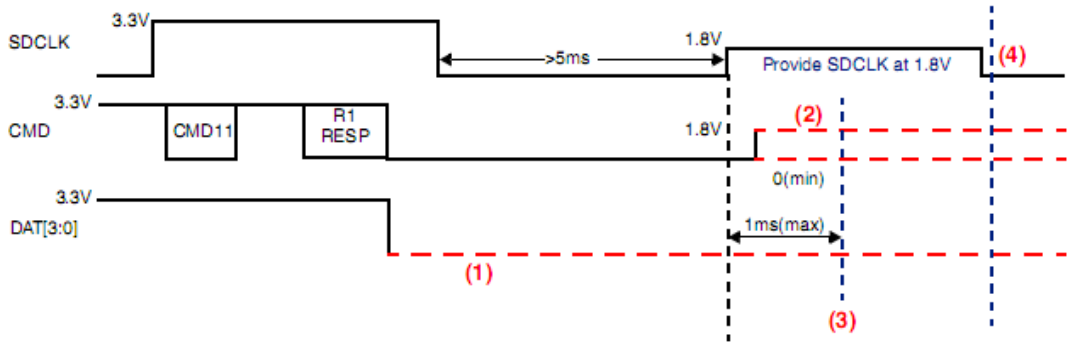

Fig. 41-15 Voltage Switch Error Scenario

1) If the interrupt (VOLT_SWITCH_INT) does not come, then the 2 ms timer should time out and a power cycle should be initiated.

Note: Before performing a power cycle, switch off the card clock by programming SDMMC_CLKENA register; no cmd_done (CD) interrupt is generated.
Additionally, if the card detects a voltage error at any point in between steps (5) and (7) in the card keeps driving DAT[3:0] to low until card power off.

2) CMD can be low or tri-state.
3) The host controller generates a voltage switch interrupt once the CMD and DAT[3:0] lines go high. The application should check for an interrupt to confirm CMD and DAT lines going high before the 1 ms timer is done.

If the 1 ms timer expires without interrupt (VOLT_SWITCH_INT) and cmd_done (CD), a power cycle should be performed. Program the SDMMC_CLKENA register to stop SDCLK of the corresponding card. Wait for the cmd_done interrupt. Proceed for normal operation on

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interrupt.

4) If DAT[3:0] is low, the host drives SDCLK to low and then stops supplying the card power.

Note: The card checks voltages of its own regulator output and host signals to ensure they are less than 2. 5V. Errors are indicated by (1) and (2).

- If voltage switching is accepted by the card, the default speed is SDR12.
- Command Done is given:
- If voltage switching is properly done, CMD and DAT line goes high.
- If switching is not complete, the 1ms timer expires, and the card clock is switched off.

Note: No other CMD should be driven before the voltage switching operation is completed and Command Done is received.

- The application should use CMD6 to check and select the particular function; the function appropriate-speed should be selected.

After the function switches, the application should program the correct value in the CLKDIV register, depending on the function chosen. Additionally, if Function 0x4 of the Access mode is chosen—that is, DDR50, then the application should also program 1'b1 in DDR_REG for the card number that has been selected for DDR50 mode.

41.6.3 DDR Operation

41.6.3.1 4-bit DDR Programming Sequence

DDR programming should be done only after the voltage switch operation has completed. The following outlines the steps for the DDR programming sequence:

1) Once the voltage switch operation is complete, the user must program voltage selection register to the required values for the corresponding card.

- To start a card to work in DDR mode, the application must program a bit of the newly defined SDMMC_UHSREG[16] register with a value of 1'b1.
- The bit that the user programs depends on which card is to be accessed in DDR mode.

To move back to SDR mode, a power cycle should be run on the card—putting the card in SDR12 mode—and only then should SDMMC_UHSREG[16]be set back to 1'b0 for the appropriate card.

41.6.3.2 8-bit DDR Programming Sequence

The following outlines the steps for the 8-bit DDR programming sequence:

1) The cclk_in signal should be twice the speed of the required cclk_out. Thus, if the cclk_out signal is required to be 50 MHz, the cclk_in signal should be 100 MHz.
2) The SDMMC_CLKDIV register should always be programmed with a value higher than zero (0); that is, a clock divider should always be used for 8-bit DDR mode.
3) The application must program the SDMMC_UHSREG[16] register (ddr_reg bits) by assigning it with a value of 1 for the bit corresponding to the card number; this causes the selected card to start working in DDR mode.

Depending on the card number, the SDMMC_CTYPE [16] bits should be set in order to make the host work in the 8-bit mode.

41.6.3.3 eMMC4.5 DDR START Bit

The eMMC4.5 changes the START bit definition in the following manner:

1) Receiver samples the START bit on the rising edge.
2) On the next rising edge after sampling the START bit, the receiver must sample the data.
3) Removes requirement of the START bit and END bit to be high for one full cycle.

Notes: The Host Controller does not support a START bit duration higher than one clock cycle. START bit durations of one or less than one clock cycle are supported and can be defined at the time of startup by programming the EMMC_DDR_REG register.

41.6.3.4 Reset Command/Moving From DDR50 to SDR12

To reset the mode of operation from DDR50 to SDR12, the following sequence of operations has to be done by the application:

1) Issue CMD0.
2) When CMD0 is received, the card changes from DDR50 to SDR12.

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3) Program the SDMMC_CLKDIV register with an appropriate value.
4) Set ddr_reg to 0.

Note: The Voltage register should not be programmed to 0 while switching from DDR50 to SDR12, since the card is still operating in 1.8V mode after receiving CMD0.

41.6.4 H/W Reset Operation

When the RST_n signal goes low, the card enters a pre-idle state from any state other than the inactive state.

The following outlines the steps for the H/W reset programming sequence:

1) Program CMD12 to end any transfer in process.
2) Wait for DTO, even if no response is sent back by the card.
3) Set the following resets:

- DMA reset–SDMMC_CTRL [2] bit
- FIFO reset–SDMMC_CTRL [1] bit

Note: The above steps are required only if a transfer is in process.

4) Program the SDMMC_RSTN register with a value of 0; this can be done at any time when the card is connected to the controller. This programming asserts the RST_n signal and resets the card.
5) Wait for minimum of 1 µs or cclk_in period, whichever is greater
6) After a minimum of 1 µs, the application should program a value of 0 into the SDMMC_RSTN register. This de-asserts the RST_n signal and takes the card out of reset.
7) The application can program a new CMD only after a minimum of 200 µs after the de-assertion of the RST_n signal, as per the MMC 4.41 standard.

Note: For backward compatibility, the RST_n signal is temporarily disabled in the card by default. The host may need to set the signal as either permanently enabled or permanently disabled before it uses the card.

41.6.5 FBE Scenarios

An FBE occurs due to an AHB error response on the AHB bus. This is a system error, so the software driver should not perform any further programming to the Host. The only recovery mechanism from such scenarios is to do one of the following:

- Issue a hard reset by asserting the reset_n signal
- Do a program controller reset by writing to the SDMMC_CTRL[0] bit

41.6.5.1 FIFO Overflow and Underflow

During normal data transfer conditions, FIFO overflow and underflow will not occur. However if there is a programming error, then FIFO overflow/underflow can result. For example, consider the following scenarios.

- For transmit: PBL=4, Tx watermark = 1. For the above programming values, if the FIFO has only one location empty, it issues a dma_req to IDMAC FSM. Due to PBL value=4, the IDMAC FSM performs 4 pushes into the FIFO. This will result in a FIFO overflow interrupt.
- For receive: PBL=4, Rx watermark = 1. For the above programming values, if the FIFO has only one location filled, it issues a dma_req to IDMAC FSM. Due to PBL value=4, the IDMAC FSM performs 4 pops to the FIFO. This will result in a FIFO underflow interrupt.

The driver should ensure that the number of bytes to be transferred as indicated in the descriptor should be a multiple of 4bytes with respect to H_DATA_WIDTH=32. For example, if the SDMMC_BYTCNT=13, the number of bytes indicated in the descriptor should be 16 for H_DATA_WIDTH=32.

41.6.5.2 Programming of PBL and Watermark Levels

The DMAC performs data transfers depending on the programmed PBL and threshold values.

Table 41-14 PBL and Watermark Levels

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PBL (Number of transfers)	Tx/Rx Watermark Value
1	Greater than or equal to 1
4	Greater than or equal to 4
8	Greater than or equal to 8
16	Greater than or equal to 16
32	Greater than or equal to 32
64	Greater than or equal to 64
128	Greater than or equal to 128
256	Greater than or equal to 256

41.6.6 Variable Delay Usage

The control signals for variable delay element usage are described in SDMMC_CLKGEN_CON0 and SDMMC_CLKGEN_CON1.

The following outlines the steps for clock generation sequence:

1) Assert init_state to soft reset the CLKGEN.
2) Configure drv_degree/sample_degree.
3) If fine adjustment required, delay line can be used by configuring drv_delaynum/sample_delaynum and drv_sel/sample_sel.
4) Dis-assert init_state to start CLKGEN.

41.6.7 Variable Delay Tuning

Tuning is defined by SD and MMC cards to determine the correct sampling point required for the host, especially for the speed modes SDR104 and HS200 where the output delays from the cards can be up to 2 UI. Tuning is required for other speed modes-such as DDR50-even though the output delay from the card is less than one cycle.

Command for tuning is different for different cards.

- SD Memory Card:
  - CMD19 – SD card for SDR50 and SDR104 speed modes. Tuning data is defined by card specifications.
  - CMD6 – SD card for speed modes not supporting CMD19. Tuning data is the 64byte SD status.
- Multimedia Card:
  - CMD21 – MMC card for HS200 speed mode. Tuning data is defined by card specifications.
  - CMD8 – MMC card for speed modes not supporting CMD21. Tuning data is 512 byte ExtCSD data.

The following is the procedure for variable delay tuning:

1) Set a phase shift of 0-degree on cclk_in_sample.
2) Send the Tuning command to the card; the card in turn sends an R1 response on the CMD line and tuning data on the DAT line.
3) If the host sees any of the errors—start bit error, data crc error, end bit error, data read time-out, response CRC error, response error—then the sampling point is incorrect.
4) Send CMD12 to bring the host controller state machines to idle.
   - The card may treat CMD12 as an invalid command because the card has successfully sent the tuning data, and it cannot send a response.
   - The host controller may generate a response time-out interrupt that must be cleared by software.
5) Repeat steps 2) to 4) by increasing the phase shift value or delay element number on cclk_in_sample until the correct sampling point is received such that the host does not see any of the errors.
6) Mark this phase shift value as the starting point of the sampling window.
7) Repeat steps 2 to 4 by increasing the phase shift value or delay element number on cclk_in_sample until the host sees the errors starting to come again or the phase shift value reaches 360-degree.
8) Mark the last successful phase shift value as the ending point of the sampling window.

A window is established where the tuning block is matched. For example, for a scenario

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where the tuning block is received correctly for a phase shift window of 90-degree and 180-degree, then an appropriate sampling point is established as 135-degree. Once a sampling point is established, no errors should be visible in the tuning block.

41.6.8 Card Detection Method

There are many methods for SDMMC/SDIO device detection.

- Method1: Using SDMMC_CDETECT register, which is value on card_detect_n input port. 0 represents presence of card. This method is available only for SDMMC/SDIO.
- Method2: Using card detection unit in Host Controller, outputting host interrupt. The card detection unit looks for any changes in the card-detect signals for card insertion or card removal. It filters out the debounce associated with mechanical insertion or removal, and generates one interrupt to the host. You can program the debounce filter value in SDMMC_DEBNCE [23:0]. Following figure illustrates the timing for card-detect signals. This method is available only for SDMMC/SDIO.

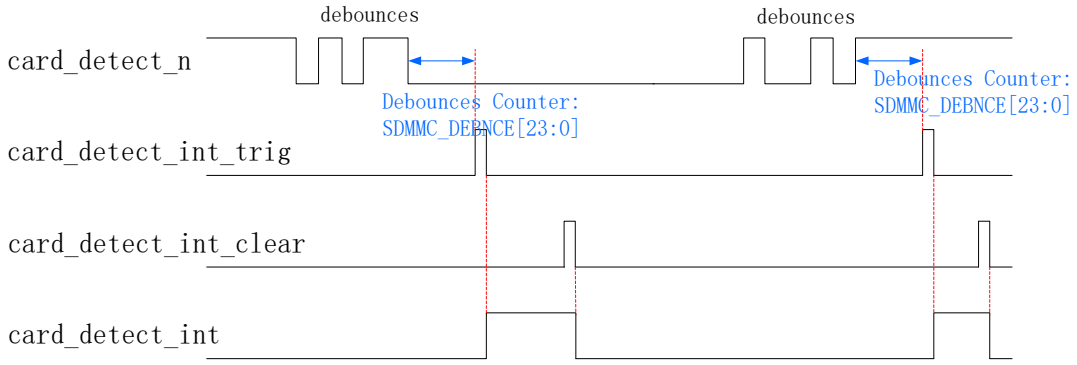

Fig. 41-16 Card Detection Method 2

- Method3: Using general card detection unit, outputting detect_dual_edge_int connecting to IRQ lines. Similar to Method2, except that the debounce time is configurable by grf; and the insertion/removal detection interrupt can be enabled or cleared respectively.

For SDMMC, the detect_dual_edge_int is IRQ line[185]. The detailed register information is:

Table 41-15 Register for SDMMC Card Detection Method 3

Signal Name	Source	Default	Description
sd_detectn_time	PMU_GRF_SDMMC_DET	0x3e8	SDMMC detect pin debounce time
sd_detectn_rising_edge_irq_en	PMU_GRF_SIG_DETECT_CON[0]	0	Enable SDMMC detect pin rising edge interrupt. 1'b0: Disable 1'b1: Enable
sd_detect_falling_edge_irq_en	PMU_GRF_SIG_DETECT_CON[1]	0	Enable SDMMC detect pin falling edge

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Signal Name	Source	Default	Description
			interrupt. 1'b0: Disable 1'b1: Enable
sd_detect_rising_edge_dectect_status	PMU_GRF_SIG_DETECT_STATUS[0]	0	SDMMC detect pin rising edge status. 1'b0: Inactive 1'b1: Active
sd_detect_falling_edge_detect_status	PMU_GRF_SIG_DETECT_STATUS[1]	0	SDMMC detect pin falling edge status. 1'b0: Inactive 1'b1: Active
sd_detect_rising_edge_dectect_clr	PMU_GRF_SIG_DETECT_CLR[0]	0	Enable clear for SDMMC detect pin rising edge interrupt. 1'b0: Disable 1'b1: Enable
sd_detect_falling_edge_detect_clr	PMU_GRF_SIG_DETECT_CLR[1]	0	Enable clear for SDMMC detect pin falling edge interrupt. 1'b0: Disable 1'b1: Enable

For SDIO, the detect_dual_edge_int is IRQ line[186]. The detailed register information is:

Table 41-16 Register for SDIO Card Detection Method 3

Signal Name	Source	Default	Description
sd_detectn_time	VEPU_GRF_SDMMC_DET	0x3e8	SDMMC detect pin

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Signal Name	Source	Default	Description
			debounce time
sd_detectn_rising_edge_irq_en	VEPU_GRF_SIG_DETECT_CON[0]	0	Enable SDMMC detect pin rising edge interrupt. 1'b0: Disable 1'b1: Enable
sd_detect_falling_edge_irq_en	VEPU_GRF_SIG_DETECT_CON[1]	0	Enable SDMMC detect pin falling edge interrupt. 1'b0: Disable 1'b1: Enable
sd_detect_rising_edge_dectect_status	VEPU_GRF_SIG_DETECT_STATUS[0]	0	SDMMC detect pin rising edge status. 1'b0: Inactive 1'b1: Active
sd_detect_falling_edge_detect_status	VEPU_GRF_SIG_DETECT_STATUS[1]	0	SDMMC detect pin falling edge status. 1'b0: Inactive 1'b1: Active
sd_detect_rising_edge_dectect_clr	VEPU_GRF_SIG_DETECT_CLR[0]	0	Enable clear for SDMMC detect pin rising edge interrupt. 1'b0: Disable 1'b1: Enable
sd_detect_falling_edge_detect_clr	VEPU_GRF_SIG_DETECT_CLR[1]	0	Enable clear for

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Signal Name	Source	Default	Description
			SDMMC detect pin falling edge interrupt. 1'b0: Disable 1'b1: Enable

41.6.9 SDMMC IOMUX With JTAG

The GPIO2_A2/GPIO2_A3 for sdcard_cdata2/sdcard_cdata3 is shared with jtag_tck/jtag_tms. The condition of usage for SDMMC or JTAG usage is as follows.

- If IOC2_GRF_JTAG_CON0[0] is equal to 1 and SD/MMC card is not detected within detection time (defined in IOC2_GRF_SDDET_DLY_CON, in the unit of XIN24M clock), the GPIOs are used for JTAG.
- Otherwise, the GPIOs' usage is defined by IOMUX configuration.

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Chapter 42 Gigabit Media Access Controller (GMAC)

42.1 Overview

GMAC Controller provides a complete Ethernet interface from processor to a Reduced Media Independent Interface (RMII) and Reduced Gigabit Media Independent Interface (RGMII) compliant Ethernet PHY.
The GMAC includes a DMA controller, which efficiently moves packet data from microprocessor's RAM, formats the data for an IEEE 802.3-2002 compliant packet and transmits the data to an Ethernet Physical Interface (PHY). It also efficiently moves packet data from RXFIFO to microprocessor's RAM.
The following features may or may not be present in the actual product. Please contact Rockchip for the actual feature configurations and the third-party licensing requirements.

42.1.1 GMAC Features

42.1.1.1 GMAC Tx and Rx Common Features

- (GMAC) Supports 10/100/1000-Mbps data transfer rates with the RGMII interfaces
- (GMAC) Supports 10/100-Mbps data transfer rates with the RMII interfaces
- (GMAC) Half-duplex operation:
  - CSMA/CD Protocol support
  - Flow control using back-pressure support (based on implementation-specific whitepapers and UNH Ethernet Clause 4 MAC Test Suite - Annex D)
  - (GMAC)Packet bursting and packet extension in 1000 Mbps half-duplex operation
- (GMAC) Standard IEEE 802.3az-2010 for Energy Efficient Ethernet in Reduced Gigabit Media Independent Interface (RGMII) PHYs
- (GMAC) 64-bit data transfer interface on the application side
- (GMAC) Full-duplex flow control operations (IEEE 802.3x Pause packets and Priority flow control)
- Support Ethernet packet timestamping as described in IEEE 1588-2002 and IEEE 1588-2008 (64-bit timestamps given in the Tx or Rx status of PTP packet). Both one-step and two-step timestamping is supported in TX direction
- Flexibility to control the Pulse-Per-Second (PPS) output signal (ptp_pps_o)
- (GMAC) Media clock generation and recovery
- (GMAC) MDIO (Clause 22 and Clause 45) master interface for PHY device configuration and management

42.1.1.2 GMAC Tx Features

- (GMAC)Preamble and start of packet data (SFD) insertion
- (GMAC)Separate 32-bit status for each packet transmitted from the application
- (GMAC)Automatic CRC and pad generation controllable on a per-packet basis
- (GMAC)Programmable packet length to support Standard or Jumbo Ethernet packets with up to16 KB of size
- (GMAC)Programmable Inter Packet Gap (40–96 bit times in steps of 8)
- (GMAC)IEEE 802.3x Flow Control automatic transmission of zero-quanta Pause packet when flowcontrol input transitions from assertion to de-assertion (in full-duplex mode)
- (GMAC)Frame Preemption for MAC Tx

42.1.1.3 GMAC Rx Features

- (GMAC)Automatic Pad and CRC Stripping options
- (GMAC)Option to disable Automatic CRC checking
- (GMAC)Preamble and SFD deletion
- (GMAC)Separate 112-bit or 128-bit status
- (GMAC)Programmable watchdog timeout limit
- (GMAC)IEEE 802.1Q VLAN tag detection and option to delete the VLAN tags in received packets
- (GMAC)Frame Preemption for MAC Rx

42.1.2 MTL Features

42.1.2.1 MTL Tx and Rx Common Features

- (GMAC) 32-bit, 64-bit, or 128-bit Transaction Layer block (bridges the application and

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the MAC)
- (GMAC) Data transfers executed using simple FIFO protocol
- (GMAC) Synchronization for all clocks in the design (Transmit, Receive, and Application clocks)
- (GMAC) Programmable burst length, up to half the size of the MTL Rx queue or Tx queue size, to support burst data transfer in the GMAC-MTL configuration
- (GMAC) Programmable threshold capability for each queue (default of 64 bytes)

42.1.2.2 MTL Tx Features
- (GMAC) Store-and-Forward mechanism or threshold mode (cut-through) for transmission to the MAC
- (GMAC) Programmable queue size in configurations with multiple queues. Each queue size can be programmed in terms of 256 bytes
- (GMAC) Automatic retransmission of collision packets in half-duplex mode
- (GMAC) Discard packets on late collision, excessive collisions, excessive deferral, and under-run conditions with appropriate status
- (GMAC) Disabling of Data Memory RAM chip-select when inactive to reduce power consumption

42.1.2.3 MTL Rx Features
- (GMAC) Rx queue sizes in the Receive path is 32 KB
- (GMAC) Insertion of Rx Status vectors into the Rx queue after the EOP transfer (in Threshold mode) and before SOP (in Store-and-Forward mode) in GMAC-MTL configuration
- P(GMAC) rogrammable Rx queue threshold (default fixed at 64 bytes) in Threshold (or cut-through) mode
- (GMAC) Statistics by generating pulses for packets dropped (because of overflow) in the Rx FIFO
- (GMAC) Automatic generation of Pause packet control or backpressure signal to the MAC based on the Rx Queue fill level

42.1.3 DMA Block Features
- (GMAC)64-bit data transfers
- (GMAC)Separate DMA channel in the Transmit path for each queue in MTL
- (GMAC)Single or multiple DMA channels for any number of queues in MTL Receive path
- (GMAC)Fully synchronous design operating on a single application clock (except for CSR module, when a separate CSR clock is configured)
- (GMAC)Byte-aligned addressing for data buffer support
- (GMAC)Dual-buffer (ring) descriptor support
- (GMAC)Descriptor architecture to allow large blocks of data transfer with minimum CPU intervention (each descriptor can transfer up to 32 KB of data)
- (GMAC)Comprehensive status reporting for normal operation and transfers with errors
- (GMAC)Individual programmable burst length for Tx DMA and Rx DMA engines for optimal host bus utilization
- (GMAC)Programmable interrupt options for different operational conditions
- (GMAC)Per-packet Transmit or Receive Complete Interrupt control
- (GMAC)Round-robin or fixed-priority arbitration between the Receive and Transmit engines
- (GMAC)Start and Stop modes
- (GMAC)Separate ports for host CSR access and host data interface
- (GMAC)support for TCP Segmentation Offload (TSO) and UDP Segmentation Offload (USO)
- (GMAC)Selectable number of Tx DMA channels with TSO/USO feature enabled
- Time-sensitive conditional packet fetching from system memory by comparing the Slot Time or IEEE 1588 time information provided in the descriptor (useful for AV applications)
- (GMAC)Programmable control for Transmit Descriptor posted writes to improve the throughput
- (GMAC)Sideband signals to control starting and stopping of DMA channels

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42.2 Block Diagram

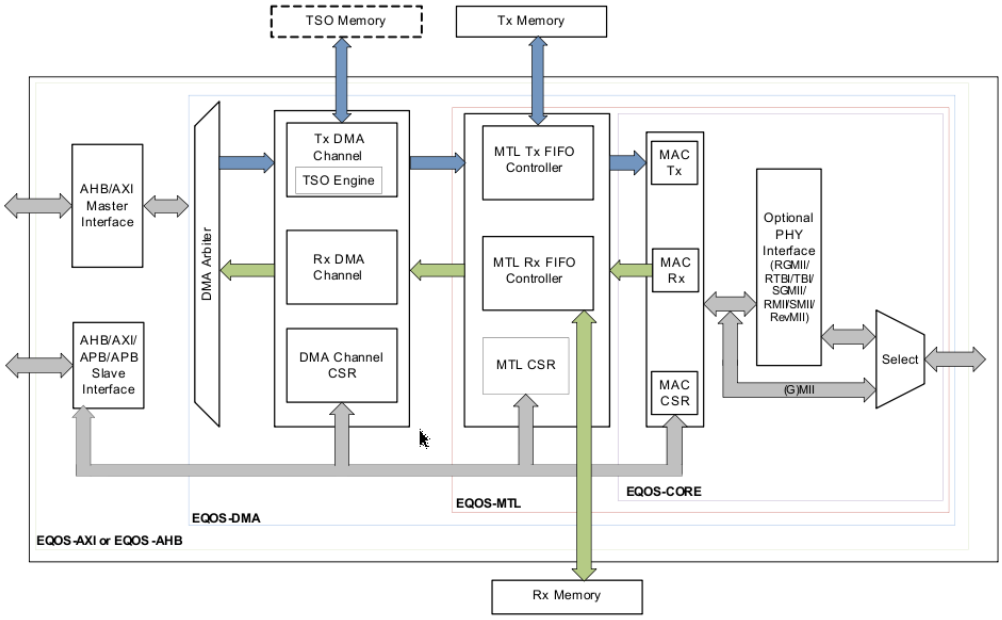

Fig. 42-1 GMAC Block Diagram

The GMAC is broken up into multiple separate functional units. These blocks are interconnected in the MAC module. The block diagram shows the general flow of data and control signals between these blocks.

The GMAC transfers data to system memory through the AXI master interface. The host CPU uses the APB Slave interface to access the GMAC subsystem's control and status registers (CSRs).

The GMAC supports the PHY interfaces of reduced GMII (RGMII) and reduced MII (RMII).

The Transmit FIFO (Tx FIFO) buffers data read from system memory by the DMA before transmission by the GMAC Core. Similarly, the Receive FIFO (Rx FIFO) stores the Ethernet frames received from the line until they are transferred to system memory by the DMA. These are asynchronous FIFOs, as they also transfer the data between the application clock and the GMAC line clocks.

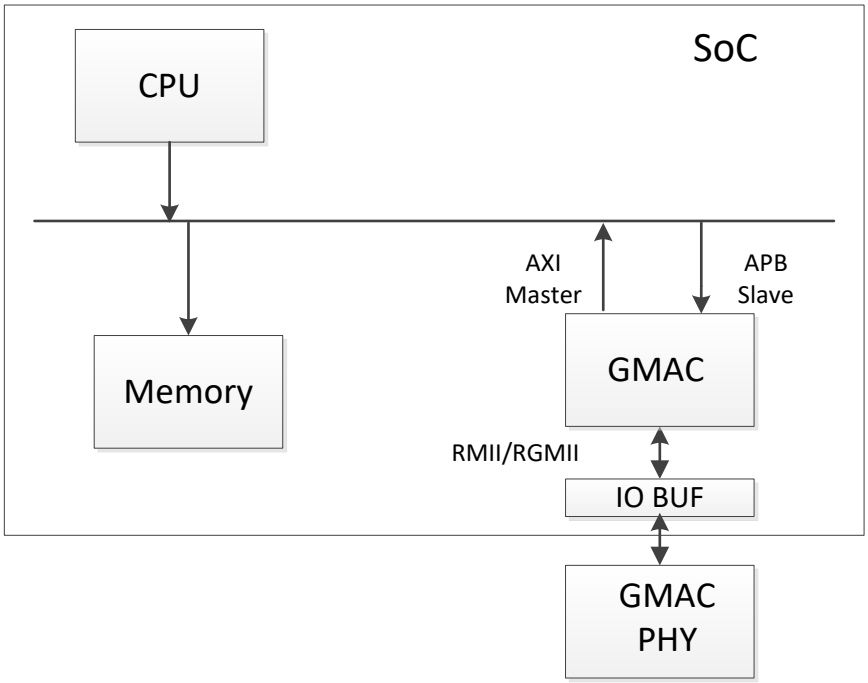

Fig. 42-2 GMAC in So C

GMAC Supports 10/100/1000-Mbps data transfer rates with the RGMII interfaces and

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Supports 10/100-Mbps data transfer rates with the RMII interfaces.

42.3 Function Description

42.3.1 Frame Structure

Data frames transmitted shall have the frame format shown in Fig.1-3.

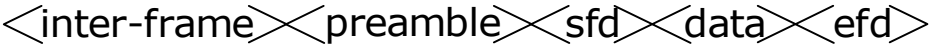

Fig. 42-3 Frame Format

The preamble <preamble> begins a frame transmission. The bit value of the preamble field consists of 7 octets with the following bit values:
10101010 10101010 10101010 10101010 10101010 10101010 10101010
The SFD (start frame delimiter) <sfd> indicates the start of a frame and follows the preamble.The bit value is 10101011.The data in a well formed frame shall consist of N octet's data.

42.3.1.1 RMII Interface timing diagram

The Reduced Media Independent Interface (RMII) specification reduces the pin count between Ethernet PHYs and Switch ASICs (only in 10/100 mode). According to the IEEE 802.3u standard, an MII contains 16 pins for data and control. In devices incorporating multiple MAC or PHY interfaces (such as switches), the number of pins adds significant cost with increase in port count. The RMII specification addresses this problem by reducing the pin count to 7 for each port - a 62.5% decrease in pin count.
The RMII module is instantiated between the GMAC and the PHY. This helps translation of the MAC's MII into the RMII. The RMII block has the following characteristics:
Supports 10-Mbps and 100-Mbps operating rates. It does not support 1000-Mbps operation.Two clock references are sourced externally or CRU, providing independent, 2-bit wide transmit and receive paths.

42.3.1.2 Transmit Bit Ordering

Each nibble from the MII must be transmitted on the RMII a di-bit at a time with the order of di-bit transmission shown in Fig. 42-4. The lower order bits (D1 and D0) are transmitted first followed by higher order bits (D2 and D3).

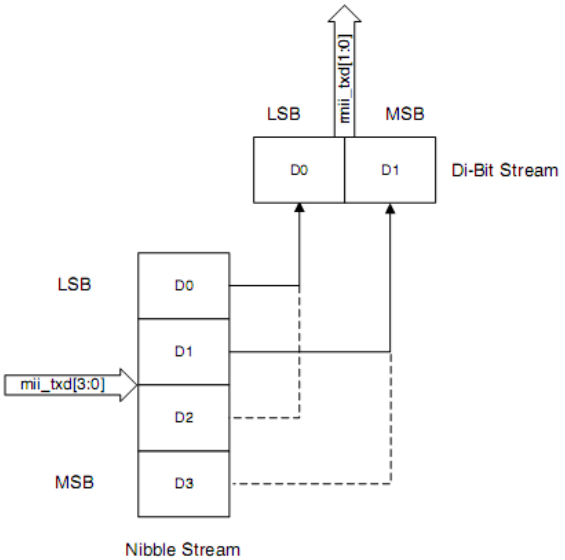

Fig. 42-4 RMII Transmission Bit Ordering

42.3.1.3 RMII Transmit Timing Diagrams

The follow figures show MII-to-RMII transaction timing.The clk_rmii_i (REF_CLK) frequency is 50MHz in RMII interface.In 10Mb/s mode, as the REF_CLK frequency is 10 times as the data rate, the value on rmii_txd_o[1:0] (TXD[1:0]) shall be valid such that TXD[1:0] may be sampled every 10th cycle,regard-less of the starting cycle within the group and yield the correct frame data.

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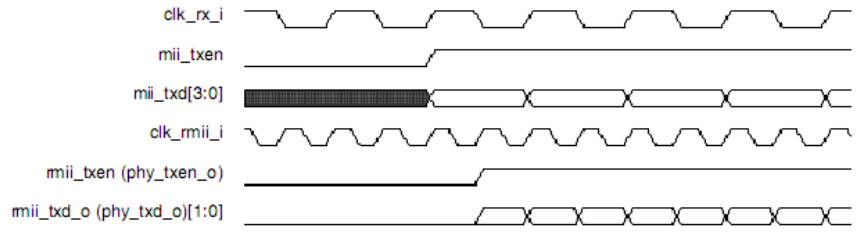

Fig. 42-5 Start of MII and RMII Transmission in 100-Mbps Mode

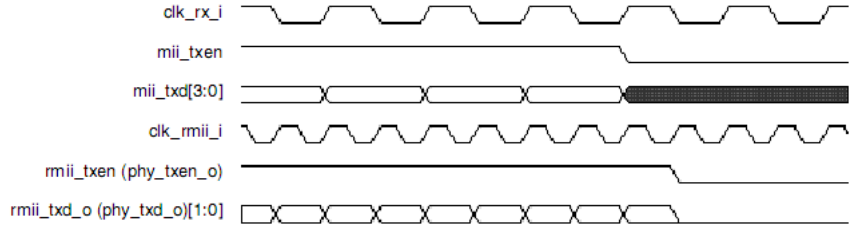

Fig. 42-6 End of MII and RMII Transmission in 100-Mbps Mode

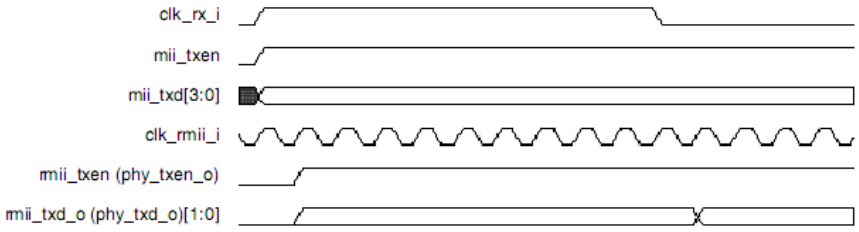

Fig. 42-7 Start of MII and RMII Transmission in 10-Mbps Mode

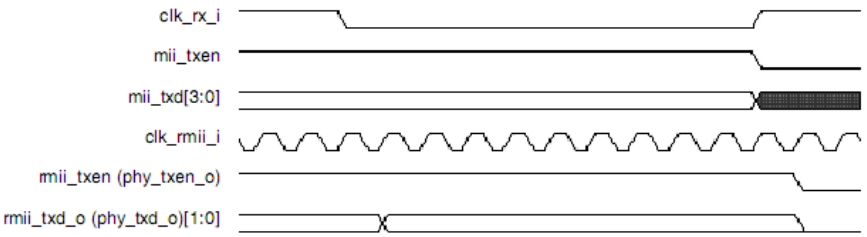

Fig. 42-8 End of MII and RMII Transmission in 10-Mbps Mode

42.3.1.4 Receive Bit Ordering

Each nibble is transmitted to the MII from the di-bit received from the RMII in the nibble transmission order shown in figure below. The lower order bits (D0 and D1) are received first, followed by the higher order bits (D2 and D3).

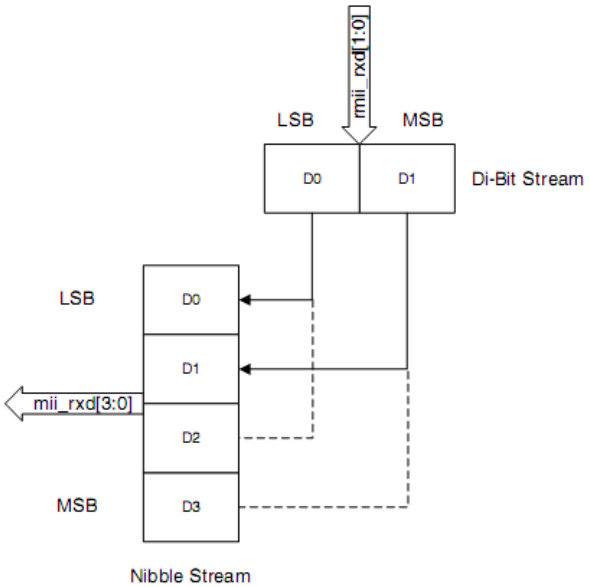

Fig. 42-9 RMII Receive Bit Ordering

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42.3.1.5 RGMII Interface

The Reduced Gigabit Media Independent Interface (RGMII) specification reduces the pin count of the interconnection between the GMAC 10/100/1000 controller and the PHY for GMII and MII interfaces. To achieve this, the data path and control signals are reduced and multiplexed together with both the edges of the transmission and receive clocks. For gigabit operation the clocks operate at 125 MHz; for 10/100 operation, the clock rates are 2.5 MHz/25 MHz.

In the GMAC 10/100/1000 controller, the RGMII module is instantiated between the GMAC core's GMII and the PHY to translate the control and data signals between the GMII and RGMII protocols.

The RGMII block has the following characteristics:

- Supports 10-Mbps, 100-Mbps, and 1000-Mbps operation rates
- For the RGMII block, no extra clock is required because both the edges of the incoming clocks are used
- The RGMII block extracts the in-band (link speed, duplex mode and link status) status signals from the PHY and provides them to the GMAC core logic for link detection

42.3.2 Station Management Agent

The application can access the PHY registers through the Station Management Agent (SMA) module. SMA is a two-wire Station Management interface (MIM).

For MIM accesses, the maximum operating frequency of the MDC (gmii_mdc_o) is 2.5 MHz, as specified in the IEEE 802.3. In the GMAC core, the gmii_mdc_o clock is derived from the application clock or clk_csr_i, using a divider-counter. The divide factor depends on the clock range setting (CR field) in the MAC_MDIO_Address register Select the clock divide factor as mentioned in the description of CR field of MAC_MDIO_Address register, to meet IEEE specifications. However, if your system supports higher clock frequencies on the MIM interface, there is a provision to select a different divider.

The MDIO frame structure is as follows:

Table 42-1 MDIO Clause 45 Frame Structure

Field	Description
IDLE	The mdio line is in tri-state; there is no clock on gmii_mdc_o signal.
PREAMBLE	32 continuous bits of value 1
START	Start of packet is 2'b00
OPCODE	■ 2'b00 ■ 2'b01 ■ 2'b10 ■ 2'b11
PHY ADDR	5-bit address select for one of 32 PHYs
DEV ADDR	5-bit address select for one of 32 devices
TA	Turnaround ■ 2'bZ0: Read and post-read increment address ■ 2'b10: Write and address MDIO accesses Where Z is the tri-state level
DATA/ADDRESS	16-bit value: For an address cycle (OPCODE = 2'b00), this frame contains the address of the register to be accessed on the next cycle. For the data cycle of a write frame, this field contains the data to be written to the register. For read or post-read increment address frames, this field contains the contents of the register read from the PHY. ■ In address and data write cycles, the GMAC drives the MDIO line during the transfer of these 16 bits. ■ In read and post-read increment address cycles, the PHY drives the MDIO line during the transfer of these 16 bits.

The frame structure for Clause 22 frames is also supported. The C45E bit in the MAC_MDIO_Address register can be programmed to enable Clause 22 or Clause 45 mode of operation. Table.1-2 shows the Clause 22 frame format.

Table 42-2 MDIO Clause 22 Frame Structure

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Field	Description
IDLE	The mdio line is in tri-state; there is no clock on gmii_mdc_o signal.
PREAMBLE	32 continuous bits of value 1
START	Start of packet is 2'b01
OPCODE	■ 2'b01 :Write ■ 2'b10 :Read
PHY ADDR	5-bit address select for one of 32 PHYs
DEV ADDR	5-bit address to select the register within each MMD
TA	Turnaround ■ 2'bZ0: Read and post-read increment address ■ 2'b10: Write and address MDIO accesses Where Z is the tri-state level
DATA/ADDRESS	Any 16-bit value: ■ In a write operation, the GMAC drives MDIO ■ In read operation, the PHY drives MDIO

In addition to normal read and write operations, the SMA also supports post-read increment address while operating in Clause 45 mode.

42.3.3 Power Management and Energy Efficient Ethernet

The GMAC supports the following techniques to save power.

- Magic Packet
- Remote Wakeup
- Energy Efficient Ethernet

The Magic Packet and Remove Wakeup techniques are used to save power in the host system when it is idle (Sleep mode) and has to be woken up only at the reception of specific packets from the Ethernet network. In the Sleep mode, the power to the host logic along with majority of the GMAC (except the MAC receiver logic), can be shut down. On receiving the specific packets from the network, the MAC provides the trigger to restore the power to the host system and come back to normal state.

The Energy Efficient Ethernet (EEE) mode is compliant with the IEEE 802.3az-2010 standard. It is primarily targeted to save power in the Ethernet port when there is no traffic on the line. In this mode, the host indicates to the far-end that it does not have any packets to transmit for near future and puts the transmitter port (MAC Controller, PCS and PHY layers) into low-power mode. Similarly, the Receiver port can also be put into low-power mode when the far-end host indicates that it does not have any traffic to transfer. This allows significant saving of power in the Ethernet port (mainly in the PHY) with intermittent and bursty traffic profile. The triggering of entry and exit out of the EEE mode is controlled by the MAC and is supported within the GMAC.

Simultaneous operation of the EEE mode along with any or both the other power saving modes is also supported in GMAC.

42.3.4 IEEE 1588 Timestamp Support

The IEEE 1588 defines a Precision Time Protocol (PTP) which enables precise synchronization of time in measurement and control systems. This protocol enables heterogeneous systems that include clocks of varying inherent precision, resolution, and stability to synchronize. The protocol supports system-wide synchronization accuracy in the sub-microsecond range with minimal network and local clock computing resources.

The GMAC supports the IEEE 1588-2002 (version 1) and IEEE 1588-2008 (version 2). The IEEE 1588-2002 supports PTP transported over UDP/IP and IEEE 1588-2008 supports PTP transported over Ethernet. The GMAC provides programmable support for both standards.

The controller supports the following features:

- Provides an option to take snapshot of all packets or only PTP type packets
- Provides an option to take snapshot of only event messages
- Provides an option to take the snapshot based on the clock type: ordinary, boundary, end-to-end transparent, and peer-to-peer transparent
- Provides an option to select the node to be a master or slave for ordinary and boundary clock
- Identifies the PTP message type, version, and PTP payload in packets sent directly

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over Ethernet and sends the status

- Provides an option to measure sub-second time in digital or binary format

42.3.5 TCP/IP Segmentation Offload (TSO) Engine

The TCP Segmentation Offload (TSO) engine is useful in offloading the TCP segmentation functions to the hardware.

It also supports UDP Segmentation Offload (USO) in which the UDP payload is segmented in the hardware. There are no sequencing/ordering controls available or updated in the segments, so it can be used in point to point applications in which out of order packets are not expected by the receiver. The description and flow of TSO mentioned in this section is same as USO, any deviation is provided as notes.

In the TCP segmentation offload (TSO) feature, the DMA splits a large TCP packet into multiple small packets and passes these packets to the MTL Tx Queue.

42.3.6 MAC Management Counters

The GMAC supports storing the statistics about the received and transmitted packets in registers that are accessible through the application.

The counters in the MAC Management Counters (MMC) module can be viewed as an extension of the register address space of the CSR module. The MMC module maintains a set of registers for gathering statistics on the received and transmitted packets. The register set includes a control register for controlling the behavior of the registers, two status registers containing interrupts generated (receive and transmit), and Interrupt Enable registers (receive and transmit). These registers are accessible from the Application through the MAC Control Interface (MCI). Each register is 32-bits wide. The write data is qualified with the corresponding mci_be_i signals. Therefore, non-32-bit accesses are allowed as long as the address is word-aligned. The MMCs are accessed using transactions, in the same way the CSR address space is accessed.

The MMC counters are free running. There is no separate enable for the counters to start. If a particular MMC counter is present in the RTL, it starts counting when corresponding packet is received or transmitted. The Receive MMC counters are updated for packets that are passed by the Address Filter (AFM) block. The statistics of packets, dropped by the AFM module, are not updated unless they are runt packets of less than 6 bytes (DA bytes are not received fully). To get statistics of all packets, set Bit 0 in the "MAC_Packet_Filter" register.

The MMC module gathers statistics on encapsulated IPv4, IPv6, TCP, UDP, or ICMP payloads in received Ethernet packets.

42.4 Register Description

42.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
GMAC_MAC_CONFIGURATION	0x0000	W	0x00008000	The MAC Configuration Register establishes the operating mode of the MAC
GMAC_MAC_EXT_CONFIGURATION	0x0004	W	0x00000000	The MAC Extended Configuration Register establishes the operating mode of the MAC
GMAC_MAC_PACKET_FILTER	0x0008	W	0x00000000	The MAC Packet Filter register contains the filter controls for receiving packets
GMAC_MAC_WATCHDOG_TIMEOUT	0x000C	W	0x00000000	The Watchdog Timeout register controls the watchdog timeout for received packets

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Name	Offset	Size	Reset Value	Description
GMAC_MAC_HASH_TABLE_REG0	0x0010	W	0x00000000	The Hash Table Register 0 contains the first 32 bits of the hash table
GMAC_MAC_HASH_TABLE_REG1	0x0014	W	0x00000000	The Hash Table Register 1 contains the second 32 bits of the hash table
GMAC_MAC_VLAN_TAG	0x0050	W	0x00000000	The VLAN Tag register identifies the IEEE 802.1Q VLAN type packets
GMAC_MAC_VLAN_HASH_TABLE	0x0058	W	0x00000000	When VTHM bit of the MAC_VLAN_Tag register is set, the 16-bit VLAN Hash Table register is used for group address filtering based on the VLAN tag
GMAC_MAC_Q0_TX_FLOW_CTRL	0x0070	W	0x00000000	The Flow Control register controls the generation and reception of the Control (Pause Command) packets by the Flow control module of the MAC
GMAC_MAC_RX_FLOW_CTRL	0x0090	W	0x00000000	The Receive Flow Control register controls the pausing of MAC Transmit based on the received Pause packet
GMAC_MAC_INTERRUPT_STATUS	0x00B0	W	0x00000000	The Interrupt Status register contains the status of interrupts
GMAC_MAC_INTERRUPT_ENABLE	0x00B4	W	0x00000000	The Interrupt Enable register contains the masks for generating the interrupts
GMAC_MAC_RX_TX_STATUS	0x00B8	W	0x00000000	The Receive Transmit Status register contains the Receive and Transmit Error status
GMAC_MAC_PMT_CONTROL_STATUS	0x00C0	W	0x00000000	The PMT Control and Status Register
GMAC_MAC_RWK_PACKET_FILTER	0x00C4	W	0x00000000	The Remote Wakeup Filter registers are implemented as 8, 16, or 32 indirect access registers (wkuppktfilter_reg#i) based on whether 4, 8, or 16 Remote Wakeup Filters are selected in the configuration and accessed by application through MAC_RWK_Packet_Filter register

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Name	Offset	Size	Reset Value	Description
GMAC_MAC_LPI_CONTROL_STATUS	0x00D0	W	0x00000000	The LPI Control and Status Register controls the LPI functions and provides the LPI interrupt status. The status bits are cleared when this register is read
GMAC_MAC_LPI_TIMERS_CONTROL	0x00D4	W	0x03E80000	The LPI Timers Control register controls the timeout values in the LPI states. It specifies the time for which the MAC transmits the LPI pattern and also the time for which the MAC waits before resuming the normal transmission
GMAC_MAC_LPI_ENTRY_TIMER	0x00D8	W	0x00000000	This register controls the Tx LPI entry timer. This counter is enabled only when bit[20](LPITE) bit of MAC_LPI_Control_Status is set to 1
GMAC_MAC_1US_TIC_COUNTER	0x00DC	W	0x00000063	This register controls the generation of the Reference time (1 microsecond tic) for all the LPI timers. This timer has to be programmed by the software initially
GMAC_MAC_PHYIF_CONTROL_STATUS	0x00F8	W	0x00000000	The PHY Interface Control and Status register indicates the status signals received by the SGMII, RGMII, or SMII interface (selected at reset) from the PHY. This register is optional
GMAC_MAC_VERSION	0x0110	W	0x00004051	The version register identifies the version of the DWC_ether_qos
GMAC_MAC_DEBUG	0x0114	W	0x00000000	The Debug register provides the debug status of various MAC blocks
GMAC_MAC_HW_FEATURE0	0x011C	W	0x400133E3	This register indicates the presence of first set of the optional features or functions
GMAC_MAC_HW_FEATURE1	0x0120	W	0x010E41A7	This register indicates the presence of second set of the optional features or functions

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Name	Offset	Size	Reset Value	Description
GMAC_MAC_HW_FEATURE2	0x0124	W	0x10000000	This register indicates the presence of third set of the optional features or functions
GMAC_MAC_HW_FEATURE3	0x0128	W	0x00000000	This register indicates the presence of fourth set the optional features or functions
GMAC_MAC_MDIO_ADDRESS	0x0200	W	0x00000000	The MDIO Address register controls the management cycles to external PHY through a management interface
GMAC_MAC_MDIO_DATA	0x0204	W	0x00000000	The MDIO Data register stores the Write data to be written to the PHY register located at the address specified in MAC_MDIO_Address
GMAC_MAC_ARP_ADDRESS	0x0210	W	0x00000000	The ARP Address register contains the IPv4 Destination Address of the MAC
GMAC_MAC_CSR_SW_CTRL	0x0230	W	0x00000000	This register contains SW programmable controls for changing the CSR access response and status bits clearing
GMAC_MAC_EXT_CFG1	0x0238	W	0x00000002	This register contains Split mode control field and offset field for Split Header feature
GMAC_MAC_PRESN_TIME_NS	0x0240	W	0x00000000	This register contains the 32-bit binary rollover equivalent time of the PTP System Time in ns
GMAC_MAC_PRESN_TIME_UPDT	0x0244	W	0x00000000	This field holds the 32-bit value of MAC 1722 Presentation Time in ns, that should be added to the Current Presentation Time Counter value. Init happens when TSINIT is set, and update happens when the TSUPDT bit is set (TSINIT and TSINIT defined in MAC_Timestamp_ Control register
GMAC_MAC_ADDRESS0_HIGH	0x0300	W	0x0000FFFF	The MAC Address0 High register holds the upper 16 bits of the first 6-byte MAC address of the station

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Name	Offset	Size	Reset Value	Description
GMAC_MAC_ADDRESS0_LOW	0x0304	W	0xFFFFFFFF	The MAC Address0 Low register holds the lower 32 bits of the 6-byte first MAC address of the station
GMAC_MMC_CONTROL	0x0700	W	0x00000000	This register establishes the operating mode of MMC
GMAC_MMC_RX_INTERRUPT	0x0704	W	0x00000000	Maintains the interrupts generated from all Receive statistics counters
GMAC_MMC_TX_INTERRUPT	0x0708	W	0x00000000	Maintains the interrupts generated from all Transmit statistics counters
GMAC_MMC_RX_INTERRUPT_MASK	0x070C	W	0x00000000	This register maintains the masks for interrupts generated from all Receive statistics counters
GMAC_MMC_TX_INTERRUPT_MASK	0x0710	W	0x00000000	This register maintains the masks for interrupts generated from all Transmit statistics counters
GMAC_TX_OCTET_COUNT_GOOD_BAD	0x0714	W	0x00000000	This register provides the number of bytes transmitted by the DWC_ether_qos, exclusive of preamble and retried bytes, in good and bad packets
GMAC_TX_PACKET_COUNT_GOOD_BAD	0x0718	W	0x00000000	This register provides the number of good and bad packets, exclusive of retried packets
GMAC_TX_UNDERFLOW_ERROR_PACKETS	0x0748	W	0x00000000	This register provides the number of packets aborted because of packets underflow error
GMAC_TX_CARRIER_ERROR_PACKETS	0x0760	W	0x00000000	This register provides the number of packets aborted because of carrier sense error (no carrier or loss of carrier)
GMAC_TX_OCTET_COUNT_GOOD	0x0764	W	0x00000000	This register provides the number of bytes exclusive of preamble, only in good packets
GMAC_TX_PACKET_COUNT_GOOD	0x0768	W	0x00000000	This register provides the number of good packets transmitted by DWC_ether_qos

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Name	Offset	Size	Reset Value	Description
GMAC_TX_PAUSE_PACKETS	0x0770	W	0x00000000	This register provides the number of good Pause packets by DWC_ether_qos
GMAC_RX_PACKETS_COUNT_GOOD_BAD	0x0780	W	0x00000000	This register provides the number of good and bad packets received by DWC_ether_qos
GMAC_RX_OCTET_COUNT_GOOD_BAD	0x0784	W	0x00000000	This register provides the number of bytes received by DWC_ether_qos, exclusive of preamble, in good and bad packets
GMAC_RX_OCTET_COUNT_GOOD	0x0788	W	0x00000000	This register provides the number of bytes received by DWC_ether_qos, exclusive of preamble, only in good packets
GMAC_RX_MULTICAST_PACKETS_GOOD	0x0790	W	0x00000000	This register provides the number of good multicast packets received by DWC_ether_qos
GMAC_RX_CRC_ERROR_PACKETS	0x0794	W	0x00000000	This register provides the number of packets received by DWC_ether_qos with CRC error
GMAC_RX_LENGTH_ERROR_PACKETS	0x07C8	W	0x00000000	This register provides the number of packets received by DWC_ether_qos with length error (Length Type field not equal to packet size), for all packets with valid length field
GMAC_RX_PAUSE_PACKETS	0x07D0	W	0x00000000	This register provides the number of good and valid Pause packets received by DWC_ether_qos
GMAC_RX_FIFO_OVERFLOW_PACKETS	0x07D4	W	0x00000000	This register provides the number of missed received packets because of FIFO overflow
GMAC_MMC_IPC_RX_INTERRUPT_MASK	0x0800	W	0x00000000	This register maintains the mask for the interrupt generated from the receive IPC statistic counters
GMAC_MMC_IPC_RX_INTERRUPT	0x0808	W	0x00000000	This register maintains the interrupt that the receive IPC statistic counters generate

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Name	Offset	Size	Reset Value	Description
GMAC_RXIPV4_GOOD_PACKETS	0x0810	W	0x00000000	This register provides the number of good IPv4 datagrams received by DWC_ether_qos with the TCP, UDP, or ICMP payload
GMAC_RXIPV4_HEADER_ERROR_PACKETS	0x0814	W	0x00000000	This register provides the number of IPv4 datagrams received by DWC_ether_qos with header (checksum, length, or version mismatch) errors
GMAC_RXIPV6_GOOD_PACKETS	0x0824	W	0x00000000	This register provides the number of good IPv6 datagrams received by DWC_ether_qos
GMAC_RXIPV6_HEADER_ERROR_PACKETS	0x0828	W	0x00000000	This register provides the number of IPv6 datagrams received by DWC_ether_qos with header (length or version mismatch) errors
GMAC_RXUDP_ERROR_PACKETS	0x0834	W	0x00000000	This register provides the number of good IP datagrams received by DWC_ether_qos whose UDP payload has a checksum error
GMAC_RXTCP_ERROR_PACKETS	0x083C	W	0x00000000	This register provides the number of good IP datagrams received by DWC_ether_qos whose TCP payload has a checksum error
GMAC_RXICMP_ERROR_PACKETS	0x0844	W	0x00000000	This register provides the number of good IP datagrams received by DWC_ether_qos whose ICMP payload has a checksum error
GMAC_RXIPV4_HEADER_ERROR_OCTETS	0x0854	W	0x00000000	This register provides the number of bytes received by DWC_ether_qos in IPv4 datagrams with header errors (checksum, length, version mismatch)
GMAC_RXIPV6_HEADER_ERROR_OCTETS	0x0868	W	0x00000000	This register provides the number of bytes received by DWC_ether_qos in IPv6 datagrams with header errors (length, version mismatch)

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Name	Offset	Size	Reset Value	Description
GMAC_RXUDP_ERROR_OCTETS	0x0874	W	0x00000000	This register provides the number of bytes received by DWC_ether_qos in a UDP segment that had checksum errors
GMAC_RXTCP_ERROR_OCTETS	0x087C	W	0x00000000	This register provides the number of bytes received by DWC_ether_qos in a TCP segment that had checksum errors
GMAC_RXICMP_ERROR_OCTETS	0x0884	W	0x00000000	This register provides the number of bytes received by DWC_ether_qos in a good ICMP segment
GMAC_MAC_TIMESTAMP_CONTROL	0x0B00	W	0x00000000	This register controls the operation of the System Time generator and processing of PTP packets for timestamping in the Receiver
GMAC_MAC_SUB_SECOND_INCREMENT	0x0B04	W	0x00000000	Specifies the value to be added to the internal system time register every cycle of clk_ptp_ref_i clock
GMAC_MAC_SYSTEM_TIME_SECS	0x0B08	W	0x00000000	The System Time Nanoseconds register, along with System Time Seconds register, indicates the current value of the system time maintained by the MAC
GMAC_MAC_SYSTEM_TIME_NS	0x0B0C	W	0x00000000	The System Time Nanoseconds register, along with System Time Seconds register, indicates the current value of the system time maintained by the MAC
GMAC_MAC_SYS_TIME_SECS_UPDATE	0x0B10	W	0x00000000	The System Time Seconds Update register, along with the System Time Nanoseconds Update register, initializes or updates the system time maintained by the MAC
GMAC_MAC_SYS_TIME_NS_UPDATE	0x0B14	W	0x00000000	MAC System Time Nanoseconds Update register

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Name	Offset	Size	Reset Value	Description
GMAC_MAC_TIMESTAMP_ADDEND	0x0B18	W	0x00000000	Timestamp Addend register. This register value is used only when the system time is configured for Fine Update mode (TSCFUPDT bit in the MAC_Timestamp_Control register)
GMAC_MAC_TIMESTAMP_STATUS	0x0B20	W	0x00000000	Timestamp Status register. All bits except Bits[27:25] gets cleared when the application reads this register
GMAC_MAC_TX_TS_STATUS_NS	0x0B30	W	0x00000000	This register contains the nanosecond part of timestamp captured for Transmit packets when Tx status is disabled
GMAC_MAC_TX_TS_STATUS_SECS	0x0B34	W	0x00000000	The register contains the higher 32 bits of the timestamp (in seconds) captured when a PTP packet is transmitted
GMAC_MAC_AUXILIARY_CONTROL	0x0B40	W	0x00000000	The Auxiliary Timestamp Control register controls the Auxiliary Timestamp snapshot
GMAC_MAC_AUXILIARY_TS_NS	0x0B48	W	0x00000000	The Auxiliary Timestamp Nanoseconds register, along with MAC_Auxiliary_Timestamp_Seconds, gives the 64-bit timestamp stored as auxiliary snapshot
GMAC_MAC_AUXILIARY_TS_SECS	0x0B4C	W	0x00000000	The Auxiliary Timestamp - Seconds register contains the lower 32 bits of the Seconds field of the auxiliary timestamp register
GMAC_MAC_TS_INGRESS_CORR_NS	0x0B58	W	0x00000000	This register contains the correction value in nanoseconds to be used with the captured timestamp value in the ingress path
GMAC_MAC_TS_EGRESS_CORR_NS	0x0B5C	W	0x00000000	This register contains the correction value in nanoseconds to be used with the captured timestamp value in the egress path
GMAC_MAC_TS_INGRESS_LATENCY	0x0B68	W	0x00000000	This register holds the Ingress MAC latency

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Name	Offset	Size	Reset Value	Description
GMAC_MAC_TS_EGRESS_LATENCY	0x0B6C	W	0x00000000	This register holds the Egress MAC latency
GMAC_MAC_PPS_CONTROL	0x0B70	W	0x00000000	PPS Control register
GMAC_MAC_PPS0_TARGET_TIME_SECONDS	0x0B80	W	0x00000000	The PPS Target Time Seconds register, along with PPS Target Time Nanoseconds register, is used to schedule an interrupt event [Bit 1 of MAC_Timestamp_Status] when the system time exceeds the value programmed in these registers
GMAC_MAC_PPS0_TARGET_TIME_NS	0x0B84	W	0x00000000	PPS0 Target Time Nanoseconds register
GMAC_MTL_OPERATION_MODE	0x0C00	W	0x00000000	The Operation Mode register establishes the Transmit and Receive operating modes and commands
GMAC_MTL_DBG_CTL	0x0C08	W	0x00000000	The FIFO Debug Access Control and Status register controls the operation mode of FIFO debug access
GMAC_MTL_DBG_STS	0x0C0C	W	0x02000000	The FIFO Debug Status register contains the status of FIFO debug access
GMAC_MTL_FIFO_DEBUG_DATA	0x0C10	W	0x00000000	The FIFO Debug Data register contains the data to be written to or read from the FIFOs
GMAC_MTL_INTERRUPT_STATUS	0x0C20	W	0x00000000	The software driver (application) reads this register during interrupt service routine or polling to determine the interrupt status of MTL queues and the MAC
GMAC_MTL_TXQ0_OPERATION_MODE	0x0D00	W	0x00000000	The Queue 0 Transmit Operation Mode register establishes the Transmit queue operating modes and commands
GMAC_MTL_TXQ0_UNDERFLOW	0x0D04	W	0x00000000	The Queue 0 Underflow Counter register contains the counter for packets aborted because of Transmit queue underflow and packets missed because of Receive queue packet flush

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Name	Offset	Size	Reset Value	Description
GMAC_MTL_TXQ0_DEBUG	0x0D08	W	0x00000000	The Queue 0 Transmit Debug register gives the debug status of various blocks related to the Transmit queue
GMAC_MTL_Q0_INTERRUPT_CTRL_STATUS	0x0D2C	W	0x00000000	This register contains the interrupt enable and status bits for the queue 0 interrupts
GMAC_MTL_RXQ0_OPERATION_MODE	0x0D30	W	0x00000000	The Queue 0 Receive Operation Mode register establishes the Receive queue operating modes and command
GMAC_MTL_RXQ0_MISS_PKT_OVF_CNT	0x0D34	W	0x00000000	The Queue 0 Missed Packet and Overflow Counter register contains the counter for packets missed because of Receive queue packet flush and packets discarded because of Receive queue overflow
GMAC_MTL_RXQ0_DEBUG	0x0D38	W	0x00000000	The Queue 0 Receive Debug register gives the debug status of various blocks related to the Receive queue
GMAC_DMA_MODE	0x1000	W	0x00000000	The Bus Mode register establishes the bus operating modes for the DMA
GMAC_DMA_SYSBUS_MODE	0x1004	W	0x00010000	The System Bus mode register controls the behavior of the AHB or AXI master
GMAC_DMA_INTERRUPT_STATUS	0x1008	W	0x00000000	The application reads this Interrupt Status register during interrupt service routine or polling to determine the interrupt status of DMA channels, MTL queues, and the MAC
GMAC_DMA_DEBUG_STATUS0	0x100C	W	0x00000000	The Debug Status 0 register gives the Receive and Transmit process status for DMA Channel 0-Channel 2 for debugging purpose
GMAC_AXI_LPI_ENTRY_INTERVAL	0x1040	W	0x00000000	This register is used to control the AXI LPI entry interval

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Name	Offset	Size	Reset Value	Description
GMAC_DMA_CH0_CONTROL	0x1100	W	0x00000000	The register specifies the MSS value for segmentation, length to skip between two descriptors, and 8xPBL mode
GMAC_DMA_CH0_TX_CONTROL	0x1104	W	0x00000000	The register controls the Tx features such as PBL, TCP segmentation, and Tx Channel weights
GMAC_DMA_CH0_RX_CONTROL	0x1108	W	0x00000000	The DMA Channel0 Receive Control register controls the Rx features such as PBL, buffer size, and extended status
GMAC_DMA_CH0_TXDESC_LIST_HADDRESS	0x1110	W	0x00000000	The Channel0 Tx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Transmit descriptor list
GMAC_DMA_CH0_TXDESC_LIST_ADDRESS	0x1114	W	0x00000000	The Channel0 Tx Descriptor List Address register points the DMA to the start of Transmit descriptor list
GMAC_DMA_CH0_RXDESC_LIST_HADDRESS	0x1118	W	0x00000000	The Channel0 Rx Descriptor List HAddress register has the higher 8 or 16 bits of the start address of the Receive descriptor list
GMAC_DMA_CH0_RXDESC_LIST_ADDRESS	0x111C	W	0x00000000	The Channel0 Rx Descriptor List Address register points the DMA to the start of Receive descriptor list
GMAC_DMA_CH0_TXDESC_TAIL_POINTER	0x1120	W	0x00000000	The Channel0 Tx Descriptor Tail Pointer register points to an offset from the base and indicates the location of the last valid descriptor
GMAC_DMA_CH0_RXDESC_TAIL_POINTER	0x1128	W	0x00000000	The Channel0 Rx Descriptor Tail Pointer Points to an offset from the base and indicates the location of the last valid descriptor
GMAC_DMA_CH0_TXDESC_RING_LENGTH	0x112C	W	0x00000000	The Tx Descriptor Ring Length register contains the length of the Transmit descriptor ring

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Name	Offset	Size	Reset Value	Description
GMAC_DMA_CH0_RXDESC_RING_LENGTH	0x1130	W	0x00000000	The Channel0 Rx Descriptor Ring Length register contains the length of the Receive descriptor circular ring
GMAC_DMA_CH0_INTERRUPT_ENABLE	0x1134	W	0x00000000	The Channel0 Interrupt Enable register enables the interrupts reported by the Status register
GMAC_DMA_CH0_RX_INTERRUPT_WATCHDOG_TIMER	0x1138	W	0x00000000	The Receive Interrupt Watchdog Timer register indicates the watchdog timeout for Receive Interrupt (RI) from the DMA
GMAC_DMA_CH0_CURRENT_APP_TXDESC	0x1144	W	0x00000000	The Channel0 Current Application Transmit Descriptor register points to the current Transmit descriptor read by the DMA
GMAC_DMA_CH0_CURRENT_APP_RXDESC	0x114C	W	0x00000000	The Channel0 Current Application Receive Descriptor register points to the current Receive descriptor read by the DMA
GMAC_DMA_CH0_CURREN_APP_TXBUFFER_H	0x1150	W	0x00000000	The Channeli Current Application Transmit Buffer Address High register has the higher 8 or 16 bits of the current address of the Transmit buffer address read by the DMA
GMAC_DMA_CH0_CURRENT_APP_TXBUFFER	0x1154	W	0x00000000	The Channel0 Current Application Transmit Buffer Address register points to the current Tx buffer address read by the DMA
GMAC_DMA_CH0_CURRENT_APP_RXBUFFER_H	0x1158	W	0x00000000	The Channeli Current Application Receive Buffer Address High register has the higher 8 or 16 bits of the current address of the Receive buffer address read by the DMA
GMAC_DMA_CH0_CURRENT_APP_RXBUFFER	0x115C	W	0x00000000	The Channel0 Current Application Receive Buffer Address register points to the current Rx buffer address read by the DMA

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Name	Offset	Size	Reset Value	Description
GMAC_DMA_CH0_STATUS	0x1160	W	0x00000000	The software driver (application) reads the Status register during interrupt service routine or polling to determine the status of the DMA
GMAC_DMA_CH0_MISS_FRAME_CNT	0x1164	W	0x00000000	This register has the number of packet counter that got dropped by the DMA either due to Bus Error or due to programming RPF field in DMA_CH$i_Rx_Control register
GMAC_DMA_CH0_RX_ERI_CNT	0x1168	W	0x00000000	The DMA_CH0_RX_ERI_Cnt registers provides the count of the number of times ERI was asserted

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

42.4.2 Detail Registers Description

GMAC_MAC_CONFIGURATION

Address: Operational Base(0x21C70000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	ARPEN ARP Offload Enable When this bit is set, the MAC can recognize an incoming ARP request packet and schedules the ARP packet for transmission. It forwards the ARP packet to the application and also indicate the events in the RxStatus. When this bit is reset, the MAC receiver does not recognize any ARP packet and indicates them as Type frame in the RxStatus. This bit is available only when the Enable IPv4 ARP Offload is selected. Values: 1'b0: ARP Offload is disabled 1'b1: ARP Offload is enabled
30:28	RO	0x0	reserved
27	RW	0x0	IPC Checksum Offload When set, this bit enables the IPv4 header checksum checking and IPv4 or IPv6 TCP, UDP, or ICMP payload checksum checking. When this bit is reset, the COE function in the receiver is disabled.The Layer 3 and Layer 4 Packet Filter and Enable Split Header features automatically selects the IPC Full Checksum Offload Engine on the Receive side. When any of these features are enabled, you must set the IPC bit. Values: 1'b0: IP header/payload checksum checking is disabled 1'b1: IP header/payload checksum checking is enabled

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Bit	Attr	Reset Value	Description
26:24	RW	0x0	IPG Inter-Packet Gap These bits control the minimum IPG between packets during transmission. This range of minimum IPG is valid in full-duplex mode.In the half-duplex mode, the minimum IPG can be configured only for 64-bit times (IPG = 100). Lower values are not considered. When a JAM pattern is being transmitted because of backpressure activation, the MAC does not consider the minimum IPG.The above function (IPG less than 96 bit times) is valid only when EIPGEN bit in MAC_Ext_Configuration register is reset. When EIPGEN is set, then the minimum IPG (greater than 96 bit times) is controlled as per the description given in EIPG field in MAC_Ext_Configuration register. Values: 3'b000: 96 bit times IPG 3'b001: 88 bit times IPG 3'b010: 80 bit times IPG 3'b011: 72 bit times IPG 3'b100: 64 bit times IPG 3'b101: 56 bit times IPG 3'b110: 48 bit times IPG 3'b111: 40 bit times IPG
23	RW	0x0	GPSLCE Giant Packet Size Limit Control Enable When this bit is set, the MAC considers the value in GPSL field in MAC_Ext_Configuration register to declare a received packet as Giant packet. This field must be programmed to more than 1,518 bytes. Otherwise, the MAC considers 1,518 bytes as giant packet limit. When this bit is reset, the MAC considers a received packet as Giant packet when its size is greater than 1,518 bytes (1522 bytes for tagged packet).The watchdog timeout limit, Jumbo Packet Enable and 2K Packet Enable have higher precedence over this bit, that is the MAC considers a received packet as Giant packet when its size is greater than 9,018 bytes (9,022 bytes for tagged packet) with Jumbo Packet Enabled and greater than 2,000 bytes with 2K Packet Enabled. The watchdog timeout, if enabled, terminates the received packet when watchdog limit is reached. Therefore, the programmed giant packet limit should be less than the watchdog limit to get the giant packet status. Values: 1'b0: Giant Packet Size Limit Control is disabled 1'b1: Giant Packet Size Limit Control is enabled

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Bit	Attr	Reset Value	Description
22	RW	0x0	S2KP IEEE 802.3as Support for 2K Packets When this bit is set, the MAC considers all packets with up to 2,000 bytes length as normal packets. When the JE bit is not set, the MAC considers all received packets of size more than 2K bytes as Giant packets.When this bit is reset and the JE bit is not set, the MAC considers all received packets of size more than 1,518 bytes (1,522 bytes for tagged) as giant packets. Note: When the JE bit is set, setting this bit has no effect on the giant packet status. Values: 1'b0: Support upto 2K packet is disabled 1'b1: Support upto 2K packet is Enabled
21	RW	0x0	CST CRC stripping for Type packets When this bit is set, the last four bytes (FCS) of all packets of Ether type (type field greater than 1,536) are stripped and dropped before forwarding the packet to the application. Note: For information about how the settings of the ACS bit and this bit impact the packet length, see the Table, Packet Length based on the CST and ACS Bits. Values: 1'b0: CRC stripping for Type packets is disabled 1'b1: CRC stripping for Type packets is enabled
20	RW	0x0	ACS Automatic Pad or CRC Stripping When this bit is set, the MAC strips the Pad or FCS field on the incoming packets only if the value of the length field is less than 1,536 bytes. All received packets with length field greater than or equal to 1,536 bytes are passed to the application without stripping the Pad or FCS field.When this bit is reset, the MAC passes all incoming packets to the application, without any modification. Note: For information about how the settings of CST bit and this bit impact the packet length, see the Table, Packet Length based on the CST and ACS Bit . Values: 1'b0: Automatic Pad or CRC Stripping is disabled 1'b1: Automatic Pad or CRC Stripping is enabled
19	RW	0x0	WD Watchdog Disable When this bit is set, the MAC disables the watchdog timer on the receiver. The MAC can receive packets of up to 16,383 bytes.When this bit is reset, the MAC does not allow more than 2,048 bytes (10,240 if JE is set high) of the packet being received. The MAC cuts off any bytes received after 2,048 bytes. Values: 1'b0: Watchdog is enabled 1'b1: Watchdog is disabled
18:17	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
16	RW	0x0	JE Jumbo Packet Enable When this bit is set, the MAC allows jumbo packets of 9,018 bytes (9,022 bytes for VLAN tagged packets) without reporting a giant packet error in the Rx packet status. Values: 1'b0: Jumbo packet is disabled 1'b1: Jumbo packet is enabled
15	RW	0x1	PS Port Select This bit selects the Ethernet line speed. This bit, along with Bit 14, selects the exact line speed. In the 10/100 Mbps-only (always 1) or 1000 Mbps-only (always 0) configurations, this bit is read-only (RO) with appropriate value. In default 10/100/1000 Mbps configurations, this bit is read-write (R/W). The mac_speed_o[1] signal reflects the value of this bit. Values: 1'b0: For 1000 or 2500 Mbps operations 1'b1: For 10 or 100 Mbps operations
14	RO	0x0	reserved
13	RW	0x0	DM Duplex Mode When this bit is set, the MAC operates in the full-duplex mode in which it can transmit and receive simultaneously. This bit is RO with default value of 1'b1 in the full-duplex-only configurations. Values: 1'b0: Half-duplex mode 1'b1: Full-duplex mode
12	RW	0x0	LM Loopback Mode When this bit is set, the MAC operates in the loopback mode at GMII or MII. The (G)MII Rx clock input (clk_rx_i) is required for the loopback to work properly. This is because the Tx clock is not internally looped back. Values: 1'b0: Loopback is disabled 1'b1: Loopback is enabled
11:10	RO	0x0	reserved
9	RW	0x0	DCRS Disable Carrier Sense During Transmission When this bit is set, the MAC transmitter ignores the (G)MII CRS signal during packet transmission in the half-duplex mode. As a result, no errors are generated because of Loss of Carrier or No Carrier during transmission. When this bit is reset, the MAC transmitter generates errors because of Carrier Sense. The MAC can even abort the transmission. Values: 1'b0: Enable Carrier Sense During Transmission 1'b1: Disable Carrier Sense During Transmission

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Bit	Attr	Reset Value	Description
8	RW	0x0	DR Disable Retry When this bit is set, the MAC attempts only one transmission. When a collision occurs on the GMII or MII interface, the MAC ignores the current packet transmission and reports a Packet Abort with excessive collision error in the Tx packet status.When this bit is reset, the MAC retries based on the settings of the BL field. This bit is applicable only in the half-duplex mode. Values: 1'b0: Enable Retry 1'b1: Disable Retry
7	RO	0x0	reserved
6:5	RW	0x0	BL Back-Off Limit The back-off limit determines the random integer number (r) of slot time delays (4,096 bit times for 1000/2500 Mbps; 512 bit times for 10/100 Mbps) for which the MAC waits before rescheduling a transmission attempt during retries after a collision. n = retransmission attempt. The random integer r takes the value in the range 0 <= r < 2^k This bit is applicable only in the half-duplex mode. Values: 2'b00: k = min(n,10) 2'b01: k = min(n,8) 2'b10: k = min(n,4) 2'b11: k = min(n,1)
4	RW	0x0	DC Deferral Check When this bit is set, the deferral check function is enabled in the MAC. The MAC issues a Packet Abort status, along with the excessive deferral error bit set in the Tx packet status, when the Tx state machine is deferred for more than 24,288 bit times in 10 or 100 Mbps mode. If the MAC is configured for 1000/2500 Mbps operation, the threshold for deferral is 155,680 bits times. Deferral begins when the transmitter is ready to transmit, but it is prevented because of an active carrier sense signal (CRS) on GMII or MII. The defer time is not cumulative. For example, if the transmitter defers for 10,000 bit times because the CRS signal is active and the CRS signal becomes inactive, the transmitter transmits and collision happens. Because of collision, the transmitter needs to back off and then defer again after back off completion. In such a scenario, the deferral timer is reset to 0, and it is restarted. When this bit is reset, the deferral check function is disabled and the MAC defers until the CRS signal goes inactive. This bit is applicable only in the half-duplex mode. Values: 1'b0: Deferral check function is disabled 1'b1: Deferral check function is enabled

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	PRELEN Preamble Length for Transmit packets These bits control the number of preamble bytes that are added to the beginning of every Tx packet. The preamble reduction occurs only when the MAC is operating in the full-duplex mode. Values: 2'b00: 7 bytes of preamble 2'b01: 5 bytes of preamble 2'b10: 3 bytes of preamble 2'b11: Reserved
1	RO	0x0	reserved
0	RW	0x0	RE Receiver Enable When this bit is set, the Rx state machine of the MAC is enabled for receiving packets from the GMII or MII interface. When this bit is reset, the MAC Rx state machine is disabled after it completes the reception of the current packet. The Rx state machine does not receive any more packets from the GMII or MII interface. Values: 1'b0: Receiver is disabled 1'b1: Receiver is enabled

GMAC_MAC_EXT_CONFIGURATION

Address: Operational Base(0x21C70000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	EIPG Extended Inter-Packet Gap The value in this field is applicable when the EIPGEN bit is set. This field (as Most Significant bits), along with IPG field in MAC_Configuration register, gives the minimum IPG greater than 96 bit times in steps of 8 bit times: {EIPG, IPG} 8'h00 - 104 bit times 8'h01 - 112 bit times 8'h02 - 120 bit times ---------- 8'hFF - 2144 bit times
24	RW	0x0	EIPGEN Extended Inter-Packet Gap Enable When this bit is set, the MAC interprets EIPG field and IPG field in MAC_Configuration register together as minimum IPG greater than 96 bit times in steps of 8 bit times. When this bit is reset, the MAC ignores EIPG field and interprets IPG field in MAC_Configuration register as minimum IPG less than or equal to 96 bit times in steps of 8 bit times. Note: The extended Inter-Packet Gap feature must be enabled when operating in Full-Duplex mode only. There may be undesirable effects on back-pressure function and frame transmission if it is enabled in Half-Duplex mode. Values: 1'b0: Extended Inter-Packet Gap is disabled 1'b1: Extended Inter-Packet Gap is enabled

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Bit	Attr	Reset Value	Description
23	RO	0x0	reserved
22:20	RW	0x0	HDSMS Maximum Size for Splitting the Header Data These bits indicate the maximum header size allowed for splitting the header data in the received packet. Values: 0x0 (64BYTES): Maximum Size for Splitting the Header Data is 64 bytes 0x1 (128BYTES): Maximum Size for Splitting the Header Data is 128 bytes 0x2 (256BYTES): Maximum Size for Splitting the Header Data is 256 bytes 0x3 (512BYTES): Maximum Size for Splitting the Header Data is 512 bytes 0x4 (1024BYTES): Maximum Size for Splitting the Header Data is 1024 bytes 0x5 (RSVD): Reserved
19	RO	0x0	reserved
18	RW	0x0	USP Unicast Slow Protocol Packet Detect When this bit is set, the MAC detects the Slow Protocol packets with unicast address of the station specified in the MAC_Address0_High and MAC_Address0_Low registers. The MAC also detects the Slow Protocol packets with the Slow Protocols multicast address (01-80-C2-00-00-02). When this bit is reset, the MAC detects only Slow Protocol packets with the Slow Protocol multicast address specified in the IEEE 802.3-2015, Section 5. Values: 1'b0: Unicast Slow Protocol Packet Detection is disabled 1'b1: Unicast Slow Protocol Packet Detection is enabled
17	RW	0x0	SPEN Slow Protocol Detection Enable When this bit is set, MAC processes the Slow Protocol packets (Ether Type 0x8809) and provides the Rx status. The MAC discards the Slow Protocol packets with invalid sub-types. When this bit is reset, the MAC forwards all error-free Slow Protocol packets to the application. The MAC considers such packets as normal Type packets. Values: 1'b0: Slow Protocol Detection is disabled 1'b1: Slow Protocol Detection is enabled
16	RW	0x0	DCRCC Disable CRC Checking for Received Packets When this bit is set, the MAC receiver does not check the CRC field in the received packets. When this bit is reset, the MAC receiver always checks the CRC field in the received packets. Values: 1'b0: CRC Checking is enabled 1'b1: CRC Checking is disabled
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:0	RW	0x0000	GPSL Giant Packet Size Limit If the received packet size is greater than the value programmed in this field in units of bytes, the MAC declares the received packet as Giant packet. The value programmed in this field must be greater than or equal to 1,518 bytes. Any other programmed value is considered as 1,518 bytes. For VLAN tagged packets, the MAC adds 4 bytes to the programmed value. When the Enable Double VLAN Processing option is selected, the MAC adds 8 bytes to the programmed value for double VLAN tagged packets. The value in this field is applicable when the GPSLCE bit is set in MAC_Configuration register.

GMAC_MAC_PACKET_FILTER

Address: Operational Base(0x21C70000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31	RW	0x0	RA Receive All When this bit is set, the MAC Receiver module passes all received packets to the application, irrespective of whether they pass the address filter or not. The result of the SA or DA filtering is updated (pass or fail) in the corresponding bit in the Rx Status Word. When this bit is reset, the Receiver module passes only those packets to the application that pass the SA or DA address filter. 0x0 (DISABLE): Receive All is disabled 0x1 (ENABLE): Receive All is enabled
30:17	RO	0x0000	reserved
16	RW	0x0	VTFE VLAN Tag Filter Enable When this bit is set, the MAC drops the VLAN tagged packets that do not match the VLAN Tag. When this bit is reset, the MAC forwards all packets irrespective of the match status of the VLAN Tag. Values: 1'b0: VLAN Tag Filter is disabled 1'b1: VLAN Tag Filter is enabled
15:11	RO	0x00	reserved
10	RW	0x0	HPF Hash or Perfect Filter When this bit is set, the address filter passes a packet if it matches either the perfect filtering or hash filtering as set by the HMC or HUC bit. When this bit is reset and the HUC or HMC bit is set, the packet is passed only if it matches the Hash filter. Values: 1'b0: Hash or Perfect Filter is disabled 2'b1: Hash or Perfect Filter is enabled
9:8	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
7:6	RW	0x0	PCF Pass Control Packets These bits control the forwarding of all control packets (including unicast and multicast Pause packets). Values: 2'b00: MAC filters all control packets from reaching the application 2'b01: MAC forwards all control packets except Pause packets to the application even if they fail the Address filter 2'b10: MAC forwards all control packets to the application even if they fail the Address filter 2'b11: MAC forwards the control packets that pass the Address filter
5	RW	0x0	DBF Disable Broadcast Packets When this bit is set, the AFM module blocks all incoming broadcast packets. In addition, it overrides all other filter settings. When this bit is reset, the AFM module passes all received broadcast packets. Values: 1'b0: Enable Broadcast Packets 1'b1: Disable Broadcast Packets
4	RW	0x0	PM Pass All Multicast When this bit is set, it indicates that all received packets with a multicast destination address (first bit in the destination address field is '1') are passed. When this bit is reset, filtering of multicast packet depends on HMC bit. Values: 1'b0: Pass All Multicast is disabled 1'b1: Pass All Multicast is enabled
3	RW	0x0	DAIF DA Inverse Filtering When this bit is set, the Address Check block operates in inverse filtering mode for the DA address comparison for both unicast and multicast packets. When this bit is reset, normal filtering of packets is performed. Values: 1'b0: DA Inverse Filtering is disabled 1'b1: DA Inverse Filtering is enabled
2	RW	0x0	HMC Hash Multicast When this bit is set, the MAC performs the destination address filtering of received multicast packets according to the hash table. When this bit is reset, the MAC performs the perfect destination address filtering for multicast packets, that is, it compares the DA field with the values programmed in DA registers. Values: 1'b0: Hash Multicast is disabled 1'b1: Hash Multicast is enabled
1:0	RO	0x0	reserved

GMAC_MAC_WATCHDOG_TIMEOUT

Address: Operational Base(0x21C70000) + offset (0x000C)

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Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	PWE Programmable Watchdog Enable When this bit is set and the WD bit of the MAC_Configuration register is reset, the WTO field is used as watchdog timeout for a received packet. When this bit is cleared, the watchdog timeout for a received packet is controlled by setting of WD and JE bits in MAC_Configuration register. Values: 1'b0: Programmable Watchdog is disabled 1'b1: Programmable Watchdog is enabled
7:4	RO	0x0	reserved
3:0	RW	0x0	WTO Watchdog Timeout When the PWE bit is set and the WD bit of the MAC_Configuration register is reset, this field is used as watchdog timeout for a received packet. If the length of a received packet exceeds the value of this field, such packet is terminated and declared as an error packet. Note: When the PWE bit is set, the value in this field should be more than 1,522 (0x05F2). Otherwise, the IEEE 802.3-specified valid tagged packets are declared as error packets and then dropped. Values: 4'b0000: 2 KB 4'b0001: 3 KB 4'b0010: 4 KB 4'b0011: 5 KB 4'b0100: 6 KB 4'b0101: 7 KB 4'b0110: 8 KB 4'b0111: 9 KB 4'b1000: 10 KB 4'b1001: 11 KB 4'b1010: 12 KB 4'b1011: 13 KB 4'b1100: 14 KB 4'b1101: 15 KB 4'b1110: 16383 Bytes 4'b1111: Reserved

GMAC_MAC_HASH_TABLE_REG0

Address: Operational Base(0x21C70000) + offset (0x0010)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HT31T0 MAC Hash Table First 32 Bits This field contains the first 32 Bits [31:0] of the Hash table. The Hash table is used for group address filtering. For hash filtering, the content of the destination address in the incoming packet is passed through the CRC logic and the upper six (seven in 128-bit Hash or eight in 256-bit Hash) bits of the CRC register are used to index the content of the Hash table. The most significant bits determines the register to be used (Hash Table Register X), and the least significant five bits determine the bit within the register. For example, a hash value of 6'b100000 (in 64-bit Hash) selects Bit 0 of the Hash Table Register 1, a value of 7b'1110000 (in 128-bit Hash) selects Bit 16 of the Hash Table Register 3 and a value of 8b'10111111 (in 256-bit Hash) selects Bit 31 of the Hash Table Register 5. The hash value of the destination address is calculated in the following way: 1. Calculate the 32-bit CRC for the DA (See IEEE 802.3, Section 3.2.8 for the steps to calculate CRC32). 2. Perform bitwise reversal for the value obtained in Step 1. 3. Take the upper 6 (or 7 or 8) bits from the value obtained in Step 2. If the corresponding bit value of the register is 1'b1, the packet is accepted. Otherwise, it is rejected. If the PM bit is set in MAC_Packet_Filter, all multicast packets are accepted regardless of the multicast hash values. If the Hash Table register is configured to be double-synchronized to the (G)MII clock domain, the synchronization is triggered only when Bits[31:24] (in little-endian mode) or Bits[7:0] (in big-endian mode) of the Hash Table Register X registers are written.If double-synchronization is enabled, consecutive writes to this register should be performed after at least four clock cycles in the destination clock domain.

GMAC_MAC_HASH_TABLE_REG1

Address: Operational Base(0x21C70000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HT63T32 MAC Hash Table Second 32 Bits This field contains the second 32 Bits [63:32] of the Hash table.

GMAC_MAC_VLAN_TAG

Address: Operational Base(0x21C70000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
24	RW	0x0	EVLRXS Enable VLAN Tag in Rx status When this bit is set, MAC provides the outer VLAN Tag in the Rx status. When this bit is reset, the MAC does not provide the outer VLAN Tag in Rx status. Values: 1'b0: VLAN Tag in Rx status is disabled 1'b1: VLAN Tag in Rx status is enabled
23	RO	0x0	reserved
22:21	RW	0x0	EVLS Enable VLAN Tag Stripping on Receive This field indicates the stripping operation on the outer VLAN Tag in received packet. Values: 2'b00: Do not strip 2'b01: Strip if VLAN filter passes 2'b10: Strip if VLAN filter fails 2'b11: Always strip
20	RW	0x0	DOVLTC Disable VLAN Type Check When this bit is set, the MAC does not check whether the VLAN Tag specified by the ERIVLT bit is of type S-VLAN or C-VLAN. When this bit is reset, the MAC filters or matches the VLAN Tag specified by the ERIVLT bit only when VLAN Tag type is similar to the one specified by the ERSVLM bit. Values: 1'b0: VLAN Type Check is enabled 1'b1: VLAN Type Check is disabled
19	RW	0x0	ERSVLM Enable Receive S-VLAN Match When this bit is set, the MAC receiver enables filtering or matching for S-VLAN (Type = 0x88A8) packets. When this bit is reset, the MAC receiver enables filtering or matching for C-VLAN (Type = 0x8100) packets. The ERIVLT bit determines the VLAN tag position considered for filtering or matching. Values: 1'b0: Receive S-VLAN Match is disabled 1'b1: Receive S-VLAN Match is enabled
18	RW	0x0	ESVL Enable S-VLAN When this bit is set, the MAC transmitter and receiver consider the S-VLAN packets (Type = 0x88A8) as valid VLAN tagged packets. Values: 1'b0: S-VLAN is disabled 1'b1: S-VLAN is enabled

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Bit	Attr	Reset Value	Description
17	RW	0x0	VTIM VLAN Tag Inverse Match Enable When this bit is set, this bit enables the VLAN Tag inverse matching. The packets without matching VLAN Tag are marked as matched. When reset, this bit enables the VLAN Tag perfect matching. The packets with matched VLAN Tag are marked as matched. Values: 1'b0: VLAN Tag Inverse Match is disabled 1'b1: VLAN Tag Inverse Match is enabled
16	RW	0x0	ETV Enable 12-Bit VLAN Tag Comparison When this bit is set, a 12-bit VLAN identifier is used for comparing and filtering instead of the complete 16-bit VLAN tag. Bits[11:0] of VLAN tag are compared with the corresponding field in the received VLAN-tagged packet. Similarly, when enabled, only 12 bits of the VLAN tag in the received packet are used for hash-based VLAN filtering. When this bit is reset, all 16 bits of the 15th and 16th bytes of the received VLAN packet are used for comparison and VLAN hash filtering. Values: 1'b0: 12-Bit VLAN Tag Comparison is disabled 1'b1: 12-Bit VLAN Tag Comparison is enabled
15:0	RW	0x0000	VL VLAN Tag Identifier for Receive Packets This field contains the 802.1Q VLAN tag to identify the VLAN packets. This VLAN tag identifier is compared to the 15th and 16th bytes of the packets being received for VLAN packets. The following list describes the bits of this field: 1. Bits[15:13]: User Priority 2. Bit 12: Canonical Format Indicator (CFI) or Drop Eligible Indicator (DEI) 3. Bits[11:0]: VLAN Identifier (VID) field of VLAN tag When the ETV bit is set, only the VID is used for comparison. If this field ([11:0] if ETV is set) is all zeros, the MAC does not check the 15th and 16th bytes for VLAN tag comparison and declares all packets with Type field value of 0x8100 or 0x88a8 as VLAN packets.

GMAC_MAC_VLAN_HASH_TABLE

Address: Operational Base(0x21C70000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	VLHT VLAN Hash Table This field contains the 16-bit VLAN Hash Table. For hash filtering, the content of the 16-bit VLAN tag or 12-bit VLAN ID (based on the ETV bit of MAC_VLAN_Tag Register) in the incoming packet is passed through the CRC logic. When ETV bit of MAC_VLAN_Tag register is set, the upper four bits of the calculated CRC are used to index the contents of the VLAN Hash table. When ETV bit of MAC_VLAN_Tag register is reset, the ones-complement of upper four bits of the calculated CRC are used to index the contents of the VLAN Hash table. For example, when ETV bit is set a hash value of 4b'1000 selects Bit 8 of the VLAN Hash table, whereas when ETV bit is reset a hash value of 4b'1000 selects Bit 7 of the VLAN Hash table. The hash value of the destination address is calculated in the following way: 1.Calculate the 32-bit CRC for the VLAN tag or ID (For steps to calculate CRC32, see Section 3.2.8 of IEEE 802.3). 2.Perform bitwise reversal for the value obtained in step 1. 3.Take the upper four bits from the value obtained in step 2. If the VLAN hash Table register is configured to be double-synchronized to the (G)MII clock domain, the synchronization is triggered only when Bits[15:8] (in little-endian mode) or Bits[7:0] (in big-endian mode) of this register are written. 1.If double-synchronization is enabled, consecutive writes to this register should be performed after at least four clock cycles in the destination clock domain.

GMAC_MAC_Q0_TX_FLOW_CTRL

Address: Operational Base(0x21C70000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	PT Pause Time This field holds the value to be used in the Pause Time field in the Tx control packet. If the Pause Time bits are configured to be double-synchronized to the (G)MII clock domain, consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.
15:8	RO	0x00	reserved
7	RW	0x0	DZPQ Disable Zero-Quanta Pause When this bit is set, it disables the automatic generation of the zero-quanta Pause packets on de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i or mti_flowctrl_i). When this bit is reset, normal operation with automatic zero-quanta Pause packet generation is enabled. Values: 1'b0: Zero-Quanta Pause packet generation is enabled 1'b1: Zero-Quanta Pause packet generation is disabled
6:2	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x0	TFE Transmit Flow Control Enable Full-Duplex Mode: In the full-duplex mode, when this bit is set, the MAC enables the flow control operation to Tx Pause packets. When this bit is reset, the flow control operation in the MAC is disabled, and the MAC does not transmit any Pause packets. Half-Duplex Mode: In the half-duplex mode, when this bit is set, the MAC enables the backpressure operation. When this bit is reset, the backpressure feature is disabled. Values: 1'b0: Transmit Flow Control is disabled 1'b1: Transmit Flow Control is enabled
0	RW	0x0	FCB_BPA Flow Control Busy or Backpressure Activate This bit initiates a Pause packet in the full-duplex mode and activates the backpressure function in the half-duplex mode if the TFE bit is set. Full-Duplex Mode: In the full-duplex mode, this bit should be read as 1'b0 before writing to this register. To initiate a Pause packet, the application must set this bit to 1'b1. During Control packet transfer, this bit continues to be set to indicate that a packet transmission is in progress. When Pause packet transmission is complete, the MAC resets this bit to 1'b0. You should not write to this register until this bit is cleared. Half-Duplex Mode: When this bit is set (and TFE bit is set) in the half-duplex mode, the MAC asserts the backpressure. During backpressure, when the MAC receives a new packet, the transmitter starts sending a JAM pattern resulting in a collision. This control register bit is logically ORed with the mti_flowctrl_i input signal for the backpressure function. When the MAC is configured for the full-duplex mode, the BPA is automatically disabled. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Flow Control Busy or Backpressure Activate is disabled 1'b1: Flow Control Busy or Backpressure Activate is enabled

GMAC_MAC_RX_FLOW_CTRL

Address: Operational Base(0x21C70000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x0	UP Unicast Pause Packet Detect A pause packet is processed when it has the unique multicast address specified in the IEEE 802.3. When this bit is set, the MAC can also detect Pause packets with unicast address of the station. This unicast address should be as specified in MAC_Address0_High and MAC_Address0_Low. When this bit is reset, the MAC only detects Pause packets with unique multicast address. Note: The MAC does not process a Pause packet if the multicast address is different from the unique multicast address. This is also applicable to the received PFC packet when the Priority Flow Control (PFC) is enabled. The unique multicast address (0x01_80_C2_00_00_01) is as specified in IEEE 802.1 Qbb-2011. Values: 1'b0: Unicast Pause Packet Detect disabled 1'b1: Unicast Pause Packet Detect enabled
0	RW	0x0	RFE Receive Flow Control Enable When this bit is set and the MAC is operating in full-duplex mode, the MAC decodes the received Pause packet and disables its transmitter for a specified (Pause) time. When this bit is reset or the MAC is operating in half-duplex mode, the decode function of the Pause packet is disabled. When PFC is enabled, flow control is enabled for PFC packets. The MAC decodes the received PFC packet and disables the Transmit queue, with matching priorities, for a duration of received Pause time. Values: 1'b0: Receive Flow Control is disabled 1'b1: Receive Flow Control is enabled

GMAC_MAC_INTERRUPT_STATUS

Address: Operational Base(0x21C70000) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	RO	0x0	MDIOIS MDIO Interrupt Status This bit indicates an interrupt event after the completion of MDIO operation. To reset this bit, the application has to read this bit/Write 1 to this bit when RCWE bit of MAC_CSR_SW_Ctrl register is set. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: MDIO Interrupt status not active 1'b1: MDIO Interrupt status active
17:15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14	RO	0x0	RXSTSIS Receive Status Interrupt This bit indicates the status of received packets. This bit is set when the RWT bit is set in the MAC_Rx_Tx_Status register. This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set) in the MAC_Rx_Tx_Status register. Values: 1'b0: Receive Interrupt status not active 1'b1: Receive Interrupt status active
13	RO	0x0	TXSTSIS Transmit Status Interrupt This bit indicates the status of transmitted packets. This bit is set when any of the following bits is set in the MAC_Rx_Tx_Status register: 1. Excessive Collision (EXCOL) 2. Late Collision (LCOL) 3. Excessive Deferral (EXDEF) 4. Loss of Carrier (LCARR) 5. No Carrier (NCARR) 6. Jabber Timeout (TJT) This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set) in the MAC_Rx_Tx_Status register. Values: 1'b0: Transmit Interrupt status not active 1'b1: Transmit Interrupt status active

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Bit	Attr	Reset Value	Description
12	RW	0x0	TSIS Timestamp Interrupt Status If the Timestamp feature is enabled, this bit is set when any of the following conditions is true: 1. The system time value is equal to or exceeds the value specified in the Target Time High and Low registers. 2. There is an overflow in the Seconds register. 3. The Target Time Error occurred, that is, programmed target time already elapsed. If the Auxiliary Snapshot feature is enabled, this bit is set when the auxiliary snapshot trigger is asserted. In configurations other than EQOS_CORE, when drop transmit status is enabled in MTL, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and MAC_Tx_Timestamp_Status_Seconds registers. When PTP offload feature is enabled, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and MAC_Tx_Timestamp_Status_Seconds registers, for PTO generated Delay Request and Pdelay request packets. This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set) in the MAC_Timestamp_Status register. Values: 1'b0: Timestamp Interrupt status not active 1'b1: Timestamp Interrupt status active
11	RO	0x0	MMCRXIPIS MMC Receive Checksum Offload Interrupt Status This bit is set high when an interrupt is generated in the MMC Receive Checksum Offload Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) and Enable Receive TCP/IP Checksum Check options. Values: 1'b0: MMC Receive Checksum Offload Interrupt status not active 1'b1: MMC Receive Checksum Offload Interrupt status active
10	RO	0x0	MMCTXIS MMC Transmit Interrupt Status This bit is set high when an interrupt is generated in the MMC Transmit Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option. Values: 1'b0: MMC Transmit Interrupt status not active 1'b1: MMC Transmit Interrupt status active

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Bit	Attr	Reset Value	Description
9	RO	0x0	MMCRXIS MMC Receive Interrupt Status This bit is set high when an interrupt is generated in the MMC Receive Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. This bit is valid only when you select the Enable MAC Management Counters (MMC) option. Values: 1'b0: MMC Receive Interrupt status not active 1'b1: MMC Receive Interrupt status active
8	RO	0x0	MMCIS MMC Interrupt Status This bit is set high when Bit 11, Bit 10, or Bit 9 is set high. This bit is cleared only when all these bits are low. This bit is valid only when you select the Enable MAC Management Counters (MMC) option. Values: 1'b0: MMC Interrupt status not active 1'b1: MMC Interrupt status active
7:6	RO	0x0	reserved
5	RO	0x0	LPIIS LPI Interrupt Status When the Energy Efficient Ethernet feature is enabled, this bit is set for any LPI state entry or exit in the MAC Transmitter or Receiver. This bit is cleared when the corresponding interrupt source bit of MAC_LPI_Control_Status register is read (or corresponding interrupt source bit of MAC_LPI_Control_Status register is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). Values: 0x0 (INACTIVE): LPI Interrupt status not active 0x1 (ACTIVE): LPI Interrupt status active
4	RO	0x0	PMTIS PMT Interrupt Status This bit is set when a Magic packet or Wake-on-LAN packet is received in the power-down mode (RWKPRCVD and MGKPRCVD bits in MAC_PMT_Control_Status register). This bit is cleared when corresponding interrupt source bit are cleared because of a Read operation to the MAC_PMT_Control_Status register (or corresponding interrupt source bit of MAC_PMT_Control_Status register is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). This bit is valid only when you select the Enable Power Management option. Values: 1'b0: PMT Interrupt status not active 1'b1: PMT Interrupt status active

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Bit	Attr	Reset Value	Description
3	RO	0x0	PHYIS PHY Interrupt This bit is set when rising edge is detected on the phy_intr_i input. This bit is cleared when this register is read (or this bit is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). Values: 1'b0: PHY Interrupt not detected 1'b1: PHY Interrupt detected
2:1	RO	0x0	reserved
0	RO	0x0	RGSMIIIS RGMII or SMII Interrupt Status This bit is set because of any change in value of the Link Status of RGMII or SMII interface (LNKSTS bit in MAC_PHYIF_Control_Status register). This bit is cleared when the MAC_PHYIF_Control_Status register is read (or LNKSTS bit of MAC_PHYIF_Control_Status register is written to 1 when RCWE bit of MAC_CSR_SW_Ctrl register is set). This bit is valid only when you select the optional RGMII or SMII PHY interface. Values: 0x0 (INACTIVE): RGMII or SMII Interrupt Status is not active 0x1 (ACTIVE): RGMII or SMII Interrupt Status is active

GMAC_MAC_INTERRUPT_ENABLE

Address: Operational Base(0x21C70000) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	RW	0x0	MDIOIE MDIO Interrupt Enable When this bit is set, it enables the assertion of the interrupt when MDIOIS field is set in the MAC_Interrupt_Status register. Values: 1'b0: MDIO Interrupt is disabled 1'b1: MDIO Interrupt is enabled
17:15	RO	0x0	reserved
14	RW	0x0	RXSTSIE Receive Status Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of RXSTSIS bit in the MAC_Interrupt_Status register. Values: 1'b0: Receive Status Interrupt is disabled 1'b1: Receive Status Interrupt is enabled
13	RW	0x0	TXSTSIE Transmit Status Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of TXSTSIS bit in the MAC_Interrupt_Status register. Values: 1'b0: Timestamp Status Interrupt is disabled 1'b1: Timestamp Status Interrupt is enabled

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Bit	Attr	Reset Value	Description
12	RW	0x0	TSIE Timestamp Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of TSIS bit in MAC_Interrupt_Status register. Values: 1'b0: Timestamp Interrupt is disabled 1'b1: Timestamp Interrupt is enabled
11:6	RO	0x00	reserved
5	RW	0x0	LPIIE LPI Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of LPIIS bit in MAC_Interrupt_Status register. Values: 0x0 (DISABLE): LPI Interrupt is disabled 0x1 (ENABLE): LPI Interrupt is enabled
4	RW	0x0	PMTIE PMT Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of PMTIS bit in MAC_Interrupt_Status register. Values: 1'b0: PMT Interrupt is disabled 1'b1: PMT Interrupt is enabled
3	RW	0x0	PHYIE PHY Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of PHYIS bit in MAC_Interrupt_Status register. Values: 1'b0: PHY Interrupt is disabled 1'b1: PHY Interrupt is enabled
2:1	RO	0x0	reserved
0	RW	0x0	RGSMIIIE RGMII or SMII Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of RGSMIIIS bit in MAC_Interrupt_Status register. Values: 0x0 (DISABLE): RGMII or SMII Interrupt is disabled 0x1 (ENABLE): RGMII or SMII Interrupt is enabled

GMAC_MAC_RX_TX_STATUS

Address: Operational Base(0x21C70000) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
8	RO	0x0	RWT Receive Watchdog Timeout This bit is set when a packet with length greater than 2,048 bytes is received (10, 240 bytes when Jumbo Packet mode is enabled) and the WD bit is reset in the MAC_Configuration register. This bit is set when a packet with length greater than 16,383 bytes is received and the WD bit is set in the MAC_Configuration register. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: No receive watchdog timeout 1'b1: Receive watchdog timed out
7:5	RO	0x0	reserved
4	RO	0x0	LCOL Late Collision When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the packet transmission aborted because a collision occurred after the collision window (64 bytes including Preamble in MII mode; 512 bytes including Preamble and Carrier Extension in GMII mode). This bit is not valid if the Underflow error occurs. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: No collision 1'b1: Late collision is sensed
3	RO	0x0	EXDEF Excessive Deferral When the DTXSTS bit is set in the MTL_Operation_Mode register and the DC bit is set in the MAC_Configuration register, this bit indicates that the transmission ended because of excessive deferral of over 24,288 bit times (155,680 in 1000/2500 Mbps mode or when Jumbo packet is enabled). Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: No Excessive deferral 1'b1: Excessive deferral

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Bit	Attr	Reset Value	Description
2	RO	0x0	LCARR Loss of Carrier When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the loss of carrier occurred during packet transmission, that is, the phy_crs_i signal was inactive for one or more transmission clock periods during packet transmission. This bit is valid only for packets transmitted without collision. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: Carrier is present 1'b1: Loss of carrier
1	RO	0x0	NCARR No Carrier When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the carrier signal from the PHY is not present at the end of preamble transmission. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: Carrier is present 1'b1: No carrier
0	RO	0x0	TJT Transmit Jabber Timeout This bit indicates that the Transmit Jabber Timer expired which happens when the packet size exceeds 2,048 bytes (10,240 bytes when the Jumbo packet is enabled) and JD bit is reset in the MAC_Configuration register. This bit is set when the packet size exceeds 16,383 bytes and the JD bit is set in the MAC_Configuration register. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: No Transmit Jabber Timeout 1'b1: Transmit Jabber Timeout occurr

GMAC_MAC_PMT_CONTROL_STATUS

Address: Operational Base(0x21C70000) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31	RW	0x0	RWKFILTRST Remote Wake-Up Packet Filter Register Pointer Reset When this bit is set, the remote wake-up packet filter register pointer is reset to 3'b000. It is automatically cleared after 1 clock cycle. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Remote Wake-Up Packet Filter Register Pointer is not Reset 1'b1: Remote Wake-Up Packet Filter Register Pointer is Reset

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Bit	Attr	Reset Value	Description
30:29	RO	0x0	reserved
28:24	RO	0x00	RWKPTR Remote Wake-up FIFO Pointer This field gives the current value (0 to 7, 15, or 31 when 4, 8, or 16 Remote Wake-up Packet Filters are selected) of the Remote Wake-up Packet Filter register pointer. When the value of this pointer is equal to maximum for the selected number of Remote Wake-up Packet Filters, the contents of the Remote Wake-up Packet Filter Register are transferred to the clk_rx_i domain when a Write occurs to that register.
23:11	RO	0x0000	reserved
10	RW	0x0	RWKPFE Remote Wake-up Packet Forwarding Enable When this bit is set along with RWKPKTEN, the MAC receiver drops all received frames until it receives the expected Wake-up frame. All frames after that event including the received wake-up frame are forwarded to application. This bit is then self-cleared on receiving the wake-up packet. The application can also clear this bit before the expected wake-up frame is received. In such cases, the MAC reverts to the default behavior where packets received are forwarded to the application. This bit must only be set when RWKPKTEN is set high and PWRDWN is set low. The setting of this bit has no effect when PWRDWN is set high. Note: If Magic Packet Enable and Wake-Up Frame Enable are both set along with setting of this bit and Magic Packet is received prior to wake-up frame, this bit is self-cleared on receiving Magic Packet, the received Magic packet is dropped, and all frames after received Magic Packet are forwarded to application. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Remote Wake-up Packet Forwarding is disabled 1'b1: Remote Wake-up Packet Forwarding is enabled
9	RW	0x0	GLBLUCAST Global Unicast When this bit set, any unicast packet filtered by the MAC (DAF) address recognition is detected as a remote wake-up packet. Values: 1'b0: Global unicast is disabled 1'b1: Global unicast is enabled
8:7	RO	0x0	reserved
6	RO	0x0	RWKPRCVD Remote Wake-Up Packet Received When this bit is set, it indicates that the power management event is generated because of the reception of a remote wake-up packet. This bit is cleared when this register is read. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: Remote wake-up packet is received 1'b1: Remote wake-up packet is received

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Bit	Attr	Reset Value	Description
5	RO	0x0	MGKPRCVD Magic Packet Received When this bit is set, it indicates that the power management event is generated because of the reception of a magic packet. This bit is cleared when this register is read. Access restriction applies. Clears on read (or write of 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: No Magic packet is received 1'b1: Magic packet is received
4:3	RO	0x0	reserved
2	RW	0x0	RWKPKTEN Remote Wake-Up Packet Enable When this bit is set, a power management event is generated when the MAC receives a remote wake-up packet. Values: 1'b0: Remote wake-up packet is disabled 1'b1: Remote wake-up packet is enabled
1	RW	0x0	MGKPKTEN Magic Packet Enable When this bit is set, a power management event is generated when the MAC receives a magic packet. Values: 1'b0: Magic Packet is disabled 1'b1: Magic Packet is enabled
0	RW	0x0	PWRDWN Power Down When this bit is set, the MAC receiver drops all received packets until it receives the expected magic packet or remote wake-up packet. This bit is then self-cleared and the power-down mode is disabled. The software can clear this bit before the expected magic packet or remote wake-up packet is received. The packets received by the MAC after this bit is cleared are forwarded to the application. This bit must only be set when the Magic Packet Enable, Global Unicast, or Remote Wake-Up Packet Enable bit is set high. Note: You can gate-off the CSR clock during the power-down mode. However, when the CSR clock is gated-off, you cannot perform any read or write operations on this register. Therefore, the Software cannot clear this bit. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Power down is disabled 1'b1: Power down is enabled

GMAC_MAC_RWK_PACKET_FILTER

Address: Operational Base(0x21C70000) + offset (0x00C4)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	WKUPFRMFTR(cont.) (4) If filters chained by And_Previous bit setting have complementary programming, then a frame may never pass the AND chained filter. For example, if Filter 2 And_Previous bit is set (bit 1 in Filter 2 command is set), Filter 1 Address_Type bit is set (bit 3 in Filter 1 command is set) indicating multicast detection and Filter 2 Address_Type bit is reset (bit 3 in Filter 2 command is reset) indicating unicast detection or vice versa, a remote wakeup frame does not pass the AND chained filter as a remote wakeup frame cannot be of both unicast and multicast address type. 4. Bit 0 is the enable for filter i. If Bit 0 is not set, filter i is disabled. Filter i Byte Mask: The filter i byte mask register defines the bytes of the packet that are examined by filter i (0, 1, 2, 3, .., 15) to determine whether or not a packet is a wake-up packet. 1. The MSB (31st bit) must be zero. 2. Bit j[30:0] is the byte mask. 3. If Bit j (byte number) of the byte mask is set, the CRC block processes the Filter i Offset + j of the incoming packet; otherwise Filter i Offset + j is ignored. Filter i Offset: The filter i offset register defines the offset (within the packet) from which the filter i examines the packets. 1. This 8-bit pattern-offset is the offset for the filter i first byte to be examined. 2. The minimum allowed offset is 12, which refers to the 13th byte of the packet. 3. The offset value 0 refers to the first byte of the packet. Filter i CRC-16: The filter i CRC-16 register contains the CRC-16 value calculated from the pattern and the byte mask programmed in the Remote Wakeup filter register. 1. The 16-bit CRC calculation uses the following polynomial: G(x) = x^16 + x^15 + x^2 + 1 2. Each mask, used in the hash function calculation, is compared with a 16-bit value associated with that mask. Each filter has the following: (1)32-bit Mask: Each bit in this mask corresponds to one byte in the detected packet. If the bit is 1, the corresponding byte is taken into the CRC16 calculation. (2) 8-bit Offset Pointer: Specifies the byte to start the CRC-16 computation. The pointer and the mask are used together to locate the bytes to be used in the CRC-16 calculations.

GMAC_MAC_LPI_CONTROL_STATUS

Address: Operational Base(0x21C70000) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
21	RW	0x0	LPITCSE LPI Tx Clock Stop Enable When this bit is set, the MAC asserts sbd_tx_clk_gating_ctrl_o signal high after it enters Tx LPI mode to indicate that the Tx clock to MAC can be stopped. When this bit is reset, the MAC does not assert sbd_tx_clk_gating_ctrl_o signal high after it enters Tx LPI mode. If RGMII Interface is selected, the Tx clock is required for transmitting the LPI pattern. The Tx Clock cannot be gated and so the LPITCSE bit cannot be programmed. Values: 0x0 (DISABLE): LPI Tx Clock Stop is disabled 0x1 (ENABLE): LPI Tx Clock Stop is enabled
20	RW	0x0	LPIATE LPI Timer Enable This bit controls the automatic entry of the MAC Transmitter into and exit out of the LPI state. When LPIATE, LPITXA and LPIEN bits are set, the MAC Transmitter enters LPI state only when the complete MAC TX data path is IDLE for a period indicated by the MAC_LPI_Entry_Timer register. After entering LPI state, if the data path becomes non-IDLE (due to a new packet being accepted for transmission), the Transmitter exits LPI state but does not clear LPIEN bit. This enables the re-entry into LPI state when it is IDLE again. When LPIATE is 0, the LPI Auto timer is disabled and MAC Transmitter enters LPI state based on the settings of LPITXA and LPIEN bit descriptions. Values: 0x0 (DISABLE): LPI Timer is disabled 0x1 (ENABLE): LPI Timer is enabled
19	RW	0x0	LPITXA LPI Tx Automate This bit controls the behavior of the MAC when it is entering or coming out of the LPI mode on the Transmit side. This bit is not functional in the EQOS-CORE configurations in which the Tx clock gating is done during the LPI mode. If the LPITXA and LPIEN bits are set to 1, the MAC enters the LPI mode only after all outstanding packets (in the core) and pending packets (in the application interface) have been transmitted. The MAC comes out of the LPI mode when the application sends any packet for transmission or the application issues a Tx FIFO Flush command. In addition, the MAC automatically clears the LPIEN bit when it exits the LPI state. If Tx FIFO Flush is set in the FTQ bit of MTL_TxQ0_Operation_Mode register, when the MAC is in the LPI mode, it exits the LPI mode.When this bit is 0, the LPIEN bit directly controls behavior of the MAC when it is entering or coming out of the LPI mode. Values: 0x0 (DISABLE): LPI Tx Automate is disabled 0x1 (ENABLE): LPI Tx Automate is enabled

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Bit	Attr	Reset Value	Description
18	RW	0x0	PLSEN PHY Link Status Enable This bit enables the link status received on the RGMII, SGMII, or SMII Receive paths to be used for activating the LPI LS TIMER. When this bit is set, the MAC uses the link-status bits of the MAC_PHYIF_Control_Status register and the PLS bit for the LPI LS Timer trigger. When this bit is reset, the MAC ignores the link-status bits of the MAC_PHYIF_Control_Status register and takes only the PLS bit. Values: 0x0 (DISABLE): PHY Link Status is disabled 0x1 (ENABLE): PHY Link Status is enabled
17	RW	0x0	PLS PHY Link Status This bit indicates the link status of the PHY. The MAC Transmitter asserts the LPI pattern only when the link status is up (OKAY) at least for the time indicated by the LPI LS TIMER. When this bit is set, the link is considered to be okay (UP) and when this bit is reset, the link is considered to be down. Values: 0x0 (DISABLE): link is down 0x1 (ENABLE): link is okay (UP)
16	RW	0x0	LPIEN LPI Enable When this bit is set, it instructs the MAC Transmitter to enter the LPI state. When this bit is reset, it instructs the MAC to exit the LPI state and resume normal transmission. This bit is cleared when the LPITXA bit is set and the MAC exits the LPI state because of the arrival of a new packet for transmission. Values: 0x0 (DISABLE): LPI state is disabled 0x1 (ENABLE): LPI state is enabled
15:10	RO	0x00	reserved
9	RO	0x0	RLPIST Receive LPI State When this bit is set, it indicates that the MAC is receiving the LPI pattern on the GMII or MII interface. Values: 0x0 (INACTIVE): Receive LPI state not detected 0x1 (ACTIVE): Receive LPI state detected
8	RO	0x0	TLPIST Transmit LPI State When this bit is set, it indicates that the MAC is transmitting the LPI pattern on the GMII or MII interface. Values: 0x0 (INACTIVE): Transmit LPI state not detected 0x1 (ACTIVE): Transmit LPI state detected
7:4	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
3	RO	0x0	RLPIEX Receive LPI Exit When this bit is set, it indicates that the MAC Receiver has stopped receiving the LPI pattern on the GMII or MII interface, exited the LPI state, and resumed the normal reception. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Note: This bit may not be set if the MAC stops receiving the LPI pattern for a very short duration, such as, less than three clock cycles of CSR clock. Values: 0x0 (INACTIVE): Receive LPI exit not detected 0x1 (ACTIVE): Receive LPI exit detected
2	RO	0x0	RLPIEN Receive LPI Entry When this bit is set, it indicates that the MAC Receiver has received an LPI pattern and entered the LPI state. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Note: This bit may not be set if the MAC stops receiving the LPI pattern for a very short duration, such as, less than three clock cycles of CSR clock. Values: 0x0 (INACTIVE): Receive LPI entry not detected 0x1 (ACTIVE): Receive LPI entry detected
1	RO	0x0	TLPIEX Transmit LPI Exit When this bit is set, it indicates that the MAC transmitter exited the LPI state after the application cleared the LPIEN bit and the LPI TW Timer has expired. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Values: 0x0 (INACTIVE): Transmit LPI exit not detected 0x1 (ACTIVE): Transmit LPI exit detected
0	RO	0x0	TLPIEN Transmit LPI Entry When this bit is set, it indicates that the MAC Transmitter has entered the LPI state because of the setting of the LPIEN bit. This bit is cleared by a read into this register (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Values: 0x0 (INACTIVE): Transmit LPI entry not detected 0x1 (ACTIVE): Transmit LPI entry detected

GMAC_MAC_LPI_TIMERS_CONTROL

Address: Operational Base(0x21C70000) + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RW	0x3e8	LST LPI LS Timer This field specifies the minimum time (in milliseconds) for which the link status from the PHY should be up (OKAY) before the LPI pattern can be transmitted to the PHY. The MAC does not transmit the LPI pattern even when the LPIEN bit is set unless the LPI LS Timer reaches the programmed terminal count. The default value of the LPI LS Timer is 1000 (1 sec) as defined in the IEEE standard.
15:0	RW	0x0000	TWT LPI TW Timer This field specifies the minimum time (in microseconds) for which the MAC waits after it stops transmitting the LPI pattern to the PHY and before it resumes the normal transmission. The TLPIEX status bit is set after the expiry of this timer.

GMAC_MAC_LPI_ENTRY_TIMER

Address: Operational Base(0x21C70000) + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:3	RW	0x00000	LPIET LPI Entry Timer This field specifies the time in microseconds the MAC waits to enter LPI mode, after it has transmitted all the frames. This field is valid and used only when LPITE and LPITXA are set to 1. Bits [2:0] are read-only so that the granularity of this timer is in steps of 8 micro-seconds.
2:0	RO	0x0	reserved

GMAC_MAC_1US_TIC_COUNTER

Address: Operational Base(0x21C70000) + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x063	TIC_1US_CNTR 1US TIC Counter The application must program this counter so that the number of clock cycles of CSR clock is 1us. (Subtract 1 from the value before programming). For example if the CSR clock is 100MHz then this field needs to be programmed to value 100 - 1 = 99 (which is 0x63). This is required to generate the 1US events that are used to update some of the EEE related counters.

GMAC_MAC_PHYIF_CONTROL_STATUS

Address: Operational Base(0x21C70000) + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
19	RO	0x0	LNKSTS Link Status This bit indicates whether the link is up (1'b1) or down (1'b0). Values: 0x0 (INACTIVE): Link down 0x1 (ACTIVE): Link up
18:17	RO	0x0	LNKSPEED Link Speed This bit indicates the current speed of the link. Bit 2 is reserved when the MAC is configured for the SMII PHY interface. Values: 0x0 (2500K): 2.5 MHz 0x1 (25M): 25 MHz 0x2 (125M): 125 MHz 0x3 (RSVD): Reserved
16	RO	0x0	LNKMOD Link Mode This bit indicates the current mode of operation of the link. Values: 0x0 (HDUPLX): Half-duplex mode 0x1 (FDUPLX): Full-duplex mode
15:2	RO	0x0000	reserved
1	RW	0x0	LUD Link Up or Down This bit indicates whether the link is up or down during transmission of configuration in the RGMII, SGMII, or SMII interface. Values: 0x0 (LINKDOWN): Link down 0x1 (LINKUP): Link up
0	RW	0x0	TC Transmit Configuration in RGMII, SGMII, or SMII When set, this bit enables the transmission of duplex mode, link speed, and link up or down information to the PHY in the RGMII, SMII, or SGMII port. When this bit is reset, no such information is driven to the PHY. The details of this feature are provided in the following sections: "Reduced Gigabit Media Independent Interface" "Serial Media Independent Interface" "Serial Gigabit Media Independent Interface" Values: 0x0 (DISABLE): Disable Transmit Configuration in RGMII, SGMII, or SMII 0x1 (ENABLE): Enable Transmit Configuration in RGMII, SGMII, or SMII

GMAC_MAC_VERSION

Address: Operational Base(0x21C70000) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x40	USERVER User-defined Version

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Bit	Attr	Reset Value	Description
7:0	RW	0x51	RKVER Rockchip-defined Version

GMAC_MAC_DEBUG

Address: Operational Base(0x21C70000) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18:17	RO	0x0	TFCSTS MAC Transmit Packet Controller Status This field indicates the state of the MAC Transmit Packet Controller module. Values: 2'b00: Idle state 2'b01: Waiting for one of the following: Status of the previous packet OR IPG or back off period to be over 2'b10: Generating and transmitting a Pause control packet (in full-duplex mode) 2'b11: Transferring input packet for transmission
16	RO	0x0	TPESTS MAC GMII or MII Transmit Protocol Engine Status When this bit is set, it indicates that the MAC GMII or MII transmit protocol engine is actively transmitting data, and it is not in the Idle state. Values: 1'b0: MAC GMII or MII Transmit Protocol Engine Status not detected 1'b1: MAC GMII or MII Transmit Protocol Engine Status detected
15:3	RO	0x0000	reserved
2:1	RO	0x0	RFCFCSTS MAC Receive Packet Controller FIFO Status When this bit is set, this field indicates the active state of the small FIFO Read and Write controllers of the MAC Receive Packet Controller module.
0	RO	0x0	RPESTS MAC GMII or MII Receive Protocol Engine Status When this bit is set, it indicates that the MAC GMII or MII receive protocol engine is actively receiving data, and it is not in the Idle state. Values: 0x0 (INACTIVE): MAC GMII or MII Receive Protocol Engine Status not detected 0x1 (ACTIVE): MAC GMII or MII Receive Protocol Engine Status detected

GMAC_MAC_HW_FEATURE0

Address: Operational Base(0x21C70000) + offset (0x011C)

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Bit	Attr	Reset Value	Description
31:28	RO	0x4	ACTPHYSEL Active PHY Selected When you have multiple PHY interfaces in your configuration, this field indicates the sampled value of phy_intf_sel_i during reset de-assertion. Values: 4'b0000: GMII or MII 4'b0001: RGMII 4'b0010: SGMII 4'b0011: TBI 4'b0100: RMII 4'b0101: RTBI 4'b0110: SMII 4'b0111: RevMII
27	RO	0x0	SAVLANINS Source Address or VLAN Insertion Enable This bit is set to 1 when the Enable SA and VLAN Insertion on Tx option is selected. Values: 1'b0: Source Address or VLAN Insertion Enable option is not selected 1'b1: Source Address or VLAN Insertion Enable option is selected
26:25	RO	0x0	TSSTSSEL Timestamp System Time Source This bit indicates the source of the Timestamp system time: This bit is set to 1 when the Enable IEEE 1588 Timestamp Support option is selected. Values: 2'b00: Internal 2'b01: External 2'b10: Both 2'b11: Reserved
24	RO	0x0	reserved
23	RO	0x0	MACADR32SEL MAC Addresses 32-63 Selected This bit is set to 1 when the Enable Additional 32 MAC Address Registers (32-63) option is selected. Values: 1'b0: MAC Addresses 32-63 Select option is not selected 1'b1: MAC Addresses 32-63 Select option is selected
22:18	RO	0x00	ADDMACADRSEL MAC Addresses 1-31 Selected This bit is set to 1 when the non-zero value is selected for Enable Additional 1-31 MAC Address Registers option.
17	RO	0x0	reserved
16	RO	0x1	RXCOESEL Receive Checksum Offload Enabled This bit is set to 1 when the Enable Receive TCP/IP Checksum Check option is selected. Values: 1'b0: Receive Checksum Offload Enable option is not selected 1'b1: Receive Checksum Offload Enable option is selected
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13	RO	0x1	EEESEL Energy Efficient Ethernet Enabled This bit is set to 1 when the Enable Energy Efficient Ethernet (EEE) option is selected. Values: 1'b0: Energy Efficient Ethernet Enable option is not selected 1'b1: Energy Efficient Ethernet Enable option is selected
12	RO	0x1	TSSEL IEEE 1588-2008 Timestamp Enabled This bit is set to 1 when the Enable IEEE 1588 Timestamp Support option is selected. Values: 1'b0: IEEE 1588-2008 Timestamp Enable option is not selected. 1'b1: IEEE 1588-2008 Timestamp Enable option is selected.
11:10	RO	0x0	reserved
9	RO	0x1	ARPOFFSEL ARP Offload Enabled This bit is set to 1 when the Enable IPv4 ARP Offload option is selected. Values: 1'b0: ARP Offload Enable option is not selected 1'b1: ARP Offload Enable option is selected
8	RO	0x1	MMCSEL RMON Module Enable This bit is set to 1 when the Enable MAC Management Counters (MMC) option is selected. Values: 1'b0: RMON Module Enable option is not selected 1'b1: RMON Module Enable option is selected
7	RO	0x1	MGKSEL PMT Magic Packet Enable This bit is set to 1 when the Enable Magic Packet Detection option is selected. Values: 1'b0: PMT Magic Packet Enable option is not selected 1'b1: PMT Magic Packet Enable option is selected
6	RO	0x1	RWKSEL PMT Remote Wake-up Packet Enable This bit is set to 1 when the Enable Remote Wake-Up Packet Detection option is selected. Values: 1'b0: PMT Remote Wake-up Packet Enable option is not selected 1'b1: PMT Remote Wake-up Packet Enable option is selected
5	RO	0x1	SMASEL SMA (MDIO) Interface This bit is set to 1 when the Enable Station Management (MDIO Interface) option is selected. Values: 1'b0: SMA (MDIO) Interface not selected 1'b1: SMA (MDIO) Interface selected

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Bit	Attr	Reset Value	Description
4	RO	0x0	VLHASH VLAN Hash Filter Selected This bit is set to 1 when the Enable VLAN Hash Table Based Filtering option is selected. Values: 1'b0: VLAN Hash Filter not selected 1'b1: VLAN Hash Filter selected
3	RO	0x0	PCSSEL PCS Registers (TBI, SGMII, or RTBI PHY interface) This bit is set to 1 when the TBI, SGMII, or RTBI PHY interface option is selected. Values: 1'b0: No PCS Registers (TBI, SGMII, or RTBI PHY interface) 1'b1: PCS Registers (TBI, SGMII, or RTBI PHY interface)
2	RO	0x0	HDSEL Half-duplex Support This bit is set to 1 when the half-duplex mode is selected. Values: 1'b0: No Half-duplex support 1'b1: Half-duplex support
1	RO	0x1	GMIISEL 1000 Mbps Support This bit is set to 1 when 1000 Mbps is selected as the Mode of Operation. Values: 1'b0: No 1000 Mbps support 1'b1: 1000 Mbps support
0	RO	0x1	MIISEL 10 or 100 Mbps Support This bit is set to 1 when 10/100 Mbps is selected as the Mode of Operation. Values: 1'b0: No 10 or 100 Mbps support 1'b1: 10 or 100 Mbps support

GMAC_MAC_HW_FEATURE1

Address: Operational Base(0x21C70000) + offset (0x0120)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:27	RO	0x0	L3L4FNUM Total number of L3 or L4 Filters This field indicates the total number of L3 or L4 filters: Values: 4'b0000: No L3 or L4 Filter 4'b0001: 1 L3 or L4 Filter 4'b0010: 2 L3 or L4 Filters 4'b0011: 3 L3 or L4 Filters 4'b0100: 4 L3 or L4 Filters 4'b0101: 5 L3 or L4 Filters 4'b0110: 6 L3 or L4 Filters 4'b0111: 7 L3 or L4 Filters 4'b1000: 8 L3 or L4 Filters
26	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
25:24	RO	0x1	HASHTBLSZ Hash Table Size This field indicates the size of the hash table: Values: 2'b00: No hash table 2'b01: 64 2'b10: 128 2'b11: 256
23	RO	0x0	POUOST One Step for PTP over UDP/IP Feature Enable This bit is set to 1 when the Enable One step timestamp for PTP over UDP/IP feature is selected. Values: 1'b0: One Step for PTP over UDP/IP Feature is not selected 1'b1: One Step for PTP over UDP/IP Feature is selected
22	RO	0x0	reserved
21	RO	0x0	RAVSEL Rx Side Only AV Feature Enable This bit is set to 1 when the Enable Audio Video Bridging option on Rx Side Only is selected. Values: 1'b0: Rx Side Only AV Feature is not selected 1'b1: Rx Side Only AV Feature is selected
20	RO	0x0	AVSEL AV Feature Enable This bit is set to 1 when the Enable Audio Video Bridging option is selected. Values: 1'b0: AV Feature is not selected 1'b1: AV Feature is selected
19	RO	0x1	DBGMEMA DMA Debug Registers Enable This bit is set to 1 when the Debug Mode Enable option is selected. Values: 1'b0: DMA Debug Registers option is not selected 1'b1: DMA Debug Registers option is selected
18	RO	0x1	TSOEN TCP Segmentation Offload Enable This bit is set to 1 when the Enable TCP Segmentation Offloading for TCP/IP Packets option is selected. Values: 1'b0: TCP Segmentation Offload Feature is not selected 1'b1: TCP Segmentation Offload Feature is selected
17	RO	0x1	SPHEN Split Header Feature Enable This bit is set to 1 when the Enable Split Header Structure option is selected. Values: 1'b0: Split Header Feature is not selected 1'b1: Split Header Feature is selected

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Bit	Attr	Reset Value	Description
16	RO	0x0	DCBEN DCB Feature Enable This bit is set to 1 when the Enable Data Center Bridging option is selected. Values: 1'b0: DCB Feature is not selected 1'b1: DCB Feature is selected
15:14	RO	0x1	ADDR64 Address Width This field indicates the configured address width: Values: 2'b00: 32 2'b01: 40 2'b10: 48 2'b11: Reserved
13	RO	0x0	reserved
12	RO	0x0	PTOEN PTP Offload Enable This bit is set to 1 when the Enable PTP Timestamp Offload Feature is selected. Values: 1'b0: PTP Offload feature is not selected 1'b1: PTP Offload feature is selected
11	RO	0x0	OSTEN One-Step Timestamping Enable This bit is set to 1 when the Enable One-Step Timestamp Feature is selected. Values: 1'b0: One-Step Timestamping feature is not selected 1'b1: One-Step Timestamping feature is selected
10:6	RO	0x06	TXFIFOSIZE MTL Transmit FIFO Size This field contains the configured value of MTL Tx FIFO in bytes expressed as Log to base 2 minus 7, that is, Log2(TXFIFO_SIZE) -7: Values: 0x0 (128B): 128 bytes 0x1 (256B): 256 bytes 0x2 (512B): 512 bytes 0x3 (1024B): 1024 bytes 0x4 (2048B): 2048 bytes 0x5 (4096B): 4096 bytes 0x6 (8192B): 8192 bytes 0x7 (16384B): 16384 bytes 0x8 (32KB): 32 KB 0x9 (64KB): 64 KB 0xa (128KB): 128 KB 0xb (RSVD): Reserved
5	RO	0x1	SPRAM Single Port RAM Enable This bit is set to 1 when the Use single port RAM Feature is selected. Values: 1'b0: Single Port RAM feature is not selected 1'b1: Single Port RAM feature is selected

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Bit	Attr	Reset Value	Description
4:0	RO	0x07	RXFIFOSIZE MTL Receive FIFO Size This field contains the configured value of MTL Rx FIFO in bytes expressed as Log to base 2 minus 7, that is, Log2(RXFIFO_SIZE) -7: Values: 5'b00000: 128 bytes 5'b00001: 256 bytes 5'b00010: 512 bytes 5'b00011: 1024 bytes 5'b00100: 2048 bytes 5'b00101: 4096 bytes 5'b00110: 8192 bytes 5'b00111: 16384 bytes 5'b01000: 32 KB 5'b01001: 64 KB 5'b01010: 128 KB 5'b01011: 256 KB 5'b01100: Reserved

GMAC_MAC_HW_FEATURE2

Address: Operational Base(0x21C70000) + offset (0x0124)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RO	0x1	AUXSNAPNUM Number of Auxiliary Snapshot Inputs This field indicates the number of auxiliary snapshot inputs: Values: 3'b000: No auxiliary input 3'b001: 1 auxiliary input 3'b010: 2 auxiliary input 3'b011: 3 auxiliary input 3'b100: 4 auxiliary input 3'b101: Reserved
27	RO	0x0	reserved
26:24	RO	0x0	PPSOUTNUM Number of PPS Outputs This field indicates the number of PPS outputs: Values: 3'b000: No PPS output 3'b001: 1 PPS output 3'b010: 2 PPS output 3'b011: 3 PPS output 3'b100: 4 PPS output 3'b101: Reserved
23:22	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
21:18	RO	0x0	TXCHCNT Number of DMA Transmit Channels This field indicates the number of DMA Transmit channels: Values: 4'b0000: 1 MTL Tx Channel 4'b0001: 2 MTL Tx Channels 4'b0010: 3 MTL Tx Channels 4'b0011: 4 MTL Tx Channels 4'b0100: 5 MTL Tx Channels 4'b0101: 6 MTL Tx Channels 4'b0110: 7 MTL Tx Channels 4'b0111: 8 MTL Tx Channels
17:16	RO	0x0	reserved
15:12	RO	0x0	RXCHCNT Number of DMA Receive Channels This field indicates the number of DMA Receive channels: Values: 4'b0000: 1 MTL Rx Channel 4'b0001: 2 MTL Rx Channels 4'b0010: 3 MTL Rx Channels 4'b0011: 4 MTL Rx Channels 4'b0100: 5 MTL Rx Channels 4'b0101: 6 MTL Rx Channels 4'b0110: 7 MTL Rx Channels 4'b0111: 8 MTL Rx Channels
11:10	RO	0x0	reserved
9:6	RO	0x0	TXQCNT Number of MTL Transmit Queues This field indicates the number of MTL Transmit queues: Values: 4'b0000: 1 MTL Tx Queue 4'b0001: 2 MTL Tx Queues 4'b0010: 3 MTL Tx Queues 4'b0011: 4 MTL Tx Queues 4'b0100: 5 MTL Tx Queues 4'b0101: 6 MTL Tx Queues 4'b0110: 7 MTL Tx Queues 4'b0111: 8 MTL Tx Queues
5:4	RO	0x0	reserved
3:0	RO	0x0	RXQCNT Number of MTL Receive Queues This field indicates the number of MTL Receive queues: Values: 4'b0000: 1 MTL Rx Queue 4'b0001: 2 MTL Rx Queues 4'b0010: 3 MTL Rx Queues 4'b0011: 4 MTL Rx Queues 4'b0100: 5 MTL Rx Queues 4'b0101: 6 MTL Rx Queues 4'b0110: 7 MTL Rx Queues 4'b0111: 8 MTL Rx Queues

GMAC_MAC_HW_FEATURE3

Address: Operational Base(0x21C70000) + offset (0x0128)

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Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:28	RO	0x0	ASP Automotive Safety Package Following are the encoding for the different Safety features. Values: 2'b00: No Safety features selected 2'b01: Only "ECC protection for external memory" feature is selected 2'b10: All the Automotive Safety features are selected without the "Parity Port Enable for external interface" feature 2'b11: All the Automotive Safety features are selected with the "Parity Port Enable for external interface" feature
27	RO	0x0	TBSSEL Time Based Scheduling Enable This bit is set to 1 when the Time Based Scheduling feature is selected. Values: 1'b0: Time Based Scheduling Enable feature is not selected 1'b1: Time Based Scheduling Enable feature is selected
26	RO	0x0	FPESEL Frame Preemption Enable This bit is set to 1 when the Enable Frame preemption feature is selected. Values: 1'b0: Frame Preemption Enable feature is not selected 1'b1: Frame Preemption Enable feature is selected
25:22	RO	0x0	reserved
21:20	RO	0x0	ESTWID Width of the Time Interval field in the Gate Control List This field indicates the width of the Configured Time Interval Field. Values: 2'b00: Width not configured 2'b01: 16 2'b10: 20 2'b11: 24
19:17	RW	0x0	ESTDEP Depth of the Gate Control List This field indicates the depth of Gate Control list expressed as Log2(DWC_EQOS_EST_DEP)-5. Values: 3'b000: No Depth configured 3'b001: 64 3'b010: 128 3'b011: 256 3'b100: 512 3'b101: 1024 3'b110: Reserved

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Bit	Attr	Reset Value	Description
16	RO	0x0	ESTSEL Enhancements to Scheduling Traffic Enable This bit is set to 1 when the Enable Enhancements to Scheduling Traffic feature is selected. Values: 1'b0: Enable Enhancements to Scheduling Traffic feature is not selected 1'b1: Enable Enhancements to Scheduling Traffic feature is selected
15	RO	0x0	reserved
14:13	RO	0x0	FRPES Flexible Receive Parser Table Entries size This field indicates the Max Number of Parser Entries supported by Flexible Receive Parser. Values: 2'b00: 64 Entries 2'b01: 128 Entries 2'b10: 256 Entries 2'b11: Reserved
12:11	RO	0x0	FRPBS Flexible Receive Parser Buffer size This field indicates the supported Max Number of bytes of the packet data to be Parsed by Flexible Receive Parser. Values: 2'b00: 64 Bytes 2'b01: 128 Bytes 2'b10: 256 Bytes 2'b11: Reserved
10:6	RO	0x00	reserved
5	RO	0x0	DVLAN Double VLAN Tag Processing Selected This bit is set to 1 when the Enable Double VLAN Processing Feature is selected. Values: 1'b0: Double VLAN option is not selected 1'b1: Double VLAN option is selected
4	RO	0x0	CBTISEL Queue/Channel based VLAN tag insertion on Tx Enable This bit is set to 1 when the Enable Queue/Channel based VLAN tag insertion on Tx Feature is selected. Values: 1'b0: Enable Queue/Channel based VLAN tag insertion on Tx feature is not selected 1'b1: Enable Queue/Channel based VLAN tag insertion on Tx feature is selected
3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2:0	RO	0x0	NRVF Number of Extended VLAN Tag Filters Enabled This field indicates the Number of Extended VLAN Tag Filters selected: Values: 3'b000: No Extended Rx VLAN Filters 3'b001: 4 Extended Rx VLAN Filters 3'b010: 8 Extended Rx VLAN Filters 3'b011: 16 Extended Rx VLAN Filters 3'b100: 24 Extended Rx VLAN Filters 3'b101: 32 Extended Rx VLAN Filters 3'b110: Reserved

GMAC_MAC_MDIO_ADDRESS

Address: Operational Base(0x21C70000) + offset (0x0200)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	PSE Preamble Suppression Enable When this bit is set, the SMA suppresses the 32-bit preamble and transmits MDIO frames with only 1 preamble bit. When this bit is 0, the MDIO frame always has 32 bits of preamble as defined in the IEEE specifications. Values: 1'b0: Preamble Suppression disabled 1'b1: Preamble Suppression enabled
26	RW	0x0	BTB Back to Back transactions When this bit is set and the NTC has value greater than 0, then the MAC informs the completion of a read or write command at the end of frame transfer (before the trailing clocks are transmitted). The software can thus initiate the next command which is executed immediately irrespective of the number trailing clocks generated for the previous frame. When this bit is reset, then the read/write command completion (GB is cleared) only after the trailing clocks are generated. In this mode, it is ensured that the NTC is always generated after each frame. This bit must not be set when NTC=0. Values: 1'b0: Back to Back transactions disabled 1'b1: Back to Back transactions enabled
25:21	RW	0x00	PA Physical Layer Address This field indicates which Clause 22 PHY devices (out of 32 devices) the MAC is accessing. For RevMII, this field gives the PHY Address of the RevMII module. This field indicates which Clause 45 capable PHYs (out of 32 PHYs) the MAC is accessing.

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Bit	Attr	Reset Value	Description
20:16	RW	0x00	RDA Register/Device Address These bits select the PHY register in selected Clause 22 PHY device. For RevMII, these bits select the CSR register in the RevMII Registers set. These bits select the Device (MMD) in selected Clause 45 capable PHY.
15	RO	0x0	reserved
14:12	RW	0x0	NTC Number of Trailing Clocks This field controls the number of trailing clock cycles generated on gmii_mdc_o (MDC) after the end of transmission of MDIO frame. The valid values can be from 0 to 7. Programming the value to 3'h3 indicates that there are additional three clock cycles on the MDC line after the end of MDIO frame transfer.
11:8	RW	0x0	CR CSR Clock Range The CSR Clock Range selection determines the frequency of the MDC clock according to the CSR clock frequency used in your design: 4'b0000: CSR clock = 60-100 MHz; MDC clock = CSR clock/42 4'b0001: CSR clock = 100-150 MHz; MDC clock = CSR clock/62 4'b0010: CSR clock = 20-35 MHz; MDC clock = CSR clock/16 4'b0011: CSR clock = 35-60 MHz; MDC clock = CSR clock/26 4'b0100: CSR clock = 150-250 MHz; MDC clock = CSR clock/102 4'b0101: CSR clock = 250-300 MHz; MDC clock = CSR clock/124 4'b0110: CSR clock = 300-500 MHz; MDC clock = CSR clock/204 4'b0111: CSR clock = 500-800 MHz; MDC clock = CSR clock/324 The suggested range of CSR clock frequency applicable for each value (when Bit 11 = 0) ensures that the MDC clock is approximately between 1.0 MHz to 2.5 MHz frequency range. When Bit 11 is set, you can achieve a higher frequency of the MDC clock than the frequency limit of 2.5 MHz (specified in the IEEE 802.3) and program a clock divider of lower value. For example, when CSR clock is of 100 MHz frequency and you program these bits as 1010, the resultant MDC clock is of 12.5 MHz which is above the range specified in IEEE 802.3. Program the following values only if the interfacing chips support faster MDC clocks: 4'b1000: CSR clock/4 4'b1001: CSR clock/6 4'b1010: CSR clock/8 4'b1011: CSR clock/10 4'b1100: CSR clock/12 4'b1101: CSR clock/14 4'b1110: CSR clock/16 4'b1111: CSR clock/18 These bits are not used for accessing RevMII. These bits are read-only if the RevMII interface is selected as single PHY interface.

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Bit	Attr	Reset Value	Description
7:5	RO	0x0	reserved
4	RW	0x0	SKAP Skip Address Packet When this bit is set, the SMA does not send the address packets before read, write, or post-read increment address packets. This bit is valid only when C45E is set. Values: 1'b0: Skip Address Packet is disabled 1'b1: Skip Address Packet is enabled
3	RW	0x0	GOC_1 GMII Operation Command 1 This bit is higher bit of the operation command to the PHY or RevMII, GOC_1 and GOC_O is encoded as follows: 2'b00: Reserved 2'b01: Write 2'b10: Post Read Increment Address for Clause 45 PHY 2'b11: Read When Clause 22 PHY or RevMII is enabled, only Write and Read commands are valid. Values: 1'b0: GMII Operation Command 1 is disabled 1'b1: GMII Operation Command 1 is enabled
2	RW	0x0	GOC_0 GMII Operation Command 0 This is the lower bit of the operation command to the PHY or RevMII. When in SMA mode (MDIO master) this bit along with GOC_1 determines the operation to be performed to the PHY. When only RevMII is selected in configuration this bit is read-only and tied to 1. Values: 1'b0: GMII Operation Command 0 is disabled 1'b1: GMII Operation Command 0 is enabled
1	RW	0x0	C45E Clause 45 PHY Enable When this bit is set, Clause 45 capable PHY is connected to MDIO. When this bit is reset, Clause 22 capable PHY is connected to MDIO. Values: 1'b0: Clause 45 PHY is disabled 1'b1: Clause 45 PHY is enabled

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Bit	Attr	Reset Value	Description
0	RW	0x0	GB GMII Busy The application sets this bit to instruct the SMA to initiate a Read or Write access to the MDIO slave. The MAC clears this bit after the MDIO frame transfer is completed. Hence the software must not write or change any of the fields in MAC_MDIO_Address and MAC_MDIO_Data registers as long as this bit is set. For write transfers, the application must first write 16-bit data in the GDl field (and also RA field when C45E is set) in MAC_MDIO_Data register before setting this bit. When C45E is set, it should also write into the RA field of MAC_MDIO_Data register before initiating a read transfer. When a read transfer is completed (GB=0), the data read from the PHY register is valid in the GD field of the MAC_MDIO_Data register. Note: Even if the addressed PHY is not present, there is no change in the functionality of this bit. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: GMII Busy is disabled 1'b1: GMII Busy is enabled

GMAC_MAC_MDIO_DATA

Address: Operational Base(0x21C70000) + offset (0x0204)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	RA Register Address This field is valid only when C45E is set. It contains the Register Address in the PHY to which the MDIO frame is intended for.
15:0	RW	0x0000	GD GMII Data This field contains the 16-bit data value read from the PHY or RevMII after a Management Read operation or the 16-bit data value to be written to the PHY or RevMII before a Management Write operation.

GMAC_MAC_ARP_ADDRESS

Address: Operational Base(0x21C70000) + offset (0x0210)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ARPPA ARP Protocol Address This field contains the IPv4 Destination Address of the MAC. This address is used for perfect match with the Protocol Address of Target field in the received ARP packet. This field is available only when the Enable IPv4 ARP Offload option is selected.

GMAC_MAC_CSR_SW_CTRL

Address: Operational Base(0x21C70000) + offset (0x0230)

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Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	RCWE Register Clear on Write 1 Enable When this bit is set, the access mode of some register fields changes to Clear on Write 1, the application needs to set that respective bit to 1 to clear it. When this bit is reset, the access mode of these register fields remain as Clear on Read. Values: 1'b0: Register Clear on Write 1 is disabled 1'b1: Register Clear on Write 1 is enabled

GMAC_MAC_EXT_CFG1

Address: Operational Base(0x21C70000) + offset (0x0238)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:8	RW	0x0	SPLM Split Mode These bits indicate the mode of splitting the incoming Rx packets. They are Values: 0x0 (L3L4): Split at L3/L4 header 0x1 (L2OFST): Split at L2 header with an offset. Always Split at SPLOFST bytes from the beginning of Length/Type field of the Frame 0x2 (COMBN): Combination mode: Split similar to SPLM=00 for IP packets that are untagged or tagged and VLAN stripped 0x3 (RSVD): Reserved
7	RO	0x0	reserved
6:0	RW	0x02	SPLOFST Split Offset These bits indicate the value of offset from the beginning of Length/Type field at which header split should take place when the appropriate SPLM is selected. The reset value of this field is 2 bytes indicating a split at L2 header. Value is in terms of bytes.

GMAC_MAC_PRESN_TIME_NS

Address: Operational Base(0x21C70000) + offset (0x0240)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:0	RO	0x000000	MPTN MAC 1722 Presentation Time in ns These bits indicate the value of the 32-bit binary rollover equivalent time of the PTP System Time in ns.

GMAC_MAC_PRESN_TIME_UPDT

Address: Operational Base(0x21C70000) + offset (0x0244)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MPTU MAC 1722 Presentation Time Update This field holds the init value or the update value for the presentation time. When used for update, this field holds the 32-bit value in ns, that should be added to the Current Presentation Time Counter value. Init happens when TSINIT is set, and update happens when the TSUPDT bit is set (TSINIT and TSINIT defined in MAC_Timestamp_ Control register). When ADDSUB field of MAC_System_Time_Nanoseconds_Update is set, this value is directly used for subtraction.

GMAC_MAC_ADDRESS0_HIGH

Address: Operational Base(0x21C70000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31	RO	0x0	AE Address Enable This bit is always set to 1. Values: 1'b0: This bit must be always set to 1 1'b1: This bit is always set to 1
30:16	RO	0x0000	reserved
15:0	RW	0xffff	ADDRHI MAC Address0[47:32] This field contains the upper 16 bits [47:32] of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets.

GMAC_MAC_ADDRESS0_LOW

Address: Operational Base(0x21C70000) + offset (0x0304)

Bit	Attr	Reset Value	Description
31:0	RW	0xffffffff	ADDRLO MAC Address0[31:0] This field contains the lower 32 bits of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets.

GMAC_MMC_CONTROL

Address: Operational Base(0x21C70000) + offset (0x0700)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
8	RW	0x0	UCDBC Update MMC Counters for Dropped Broadcast Packets Note: The CNTRST bit has a higher priority than the CNTPRST bit. Therefore, when the software tries to set both bits in the same write cycle, all counters are cleared and the CNTPRST bit is not set. When set, the MAC updates all related MMC Counters for Broadcast packets that are dropped because of the setting of the DBF bit of MAC_Packet_Filter register. When reset, the MMC Counters are not updated for dropped Broadcast packets. Values: 1'b0: Update MMC Counters for Dropped Broadcast Packets is disabled 1'b1: Update MMC Counters for Dropped Broadcast Packets is enabled
7:6	RO	0x0	reserved
5	RW	0x0	CNTPRSTLVL Full-Half Preset When this bit is low and the CNTPRST bit is set, all MMC counters get preset to almost-half value. All octet counters get preset to 0x7FFF_F800 (Half 2KBytes) and all packet-counters gets preset to 0x7FFF_FFF0 (Half 16). When this bit is high and the CNTPRST bit is set, all MMC counters get preset to almost-full value. All octet counters get preset to 0xFFFF_F800 (Full 2KBytes) and all packet-counters gets preset to 0xFFFF_FFF0 (Full 16). For 16-bit counters, the almost-half preset values are 0x7800 and 0x7FF0 for the respective octet and packet counters. Similarly, the almost-full preset values for the 16-bit counters are 0xF800 and 0xFFF0. Values: 1'b0: Full-Half Preset is disabled 1'b1: Full-Half Preset is enabled
4	RW	0x0	CNTPRST Counters Preset When this bit is set, all counters are initialized or preset to almost full or almost half according to the CNTPRSTLVL bit. This bit is cleared automatically after 1 clock cycle. This bit, along with the CNTPRSTLVL bit, is useful for debugging and testing the assertion of interrupts because of MMC counter becoming half-full or full. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. Values: 1'b0: Counters Preset is disabled 1'b1: Counters Preset is enabled

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Bit	Attr	Reset Value	Description
3	RW	0x0	CNTFREEZ MMC Counter Freeze When this bit is set, it freezes all MMC counters to their current value. Until this bit is reset to 0, no MMC counter is updated because of any transmitted or received packet. If any MMC counter is read with the Reset on Read bit set, then that counter is also cleared in this mode. Values: 1'b0: MMC Counter Freeze is disabled 1'b1: MMC Counter Freeze is enabled
2	RW	0x0	RSTONRD Reset on Read When this bit is set, the MMC counters are reset to zero after Read (self-clearing after reset). The counters are cleared when the least significant byte lane (Bits[7:0]) is read. Values: 1'b0: Reset on Read is disabled 1'b1: Reset on Read is enabled
1	RW	0x0	CNTSTOPRO Counter Stop Rollover When this bit is set, the counter does not roll over to zero after reaching the maximum value. Values: 1'b0: Counter Stop Rollover is disabled 1'b1: Counter Stop Rollover is enabled
0	RW	0x0	CNTRST Counters Reset When this bit is set, all counters are reset. This bit is cleared automatically after 1 clock cycle. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. Values: 1'b0: Counters are not reset 1'b1: All counters are reset

GMAC_MMC_RX_INTERRUPT

Address: Operational Base(0x21C70000) + offset (0x0704)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RO	0x0	RXFOVPIS MMC Receive FIFO Overflow Packet Counter Interrupt Status This bit is set when the rxfifooverflow counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive FIFO Overflow Packet Counter Interrupt Status not detected 1'b1: MMC Receive FIFO Overflow Packet Counter Interrupt Status detected

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Bit	Attr	Reset Value	Description
20	RO	0x0	RXPAUSPIS MMC Receive Pause Packet Counter Interrupt Status This bit is set when the rxpausepackets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 0x0 (INACTIVE): MMC Receive Pause Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Receive Pause Packet Counter Interrupt Status detected
19	RO	0x0	reserved
18	RO	0x0	RXLENERPIS MMC Receive Length Error Packet Counter Interrupt Status This bit is set when the rxlengtherror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive Length Error Packet Counter Interrupt Status not detected 1'b1: MMC Receive Length Error Packet Counter Interrupt Status detected
17:6	RO	0x000	reserved
5	RO	0x0	RXCRCERPIS MMC Receive CRC Error Packet Counter Interrupt Status This bit is set when the rxcrcerror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive CRC Error Packet Counter Interrupt Status not detecte 1'b1: MMC Receive CRC Error Packet Counter Interrupt Status detected
4	RO	0x0	RXMCGPIS MMC Receive Multicast Good Packet Counter Interrupt Status This bit is set when the rxmulticastpackets_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive Multicast Good Packet Counter Interrupt Status not detected 1'b1: MMC Receive Multicast Good Packet Counter Interrupt Status detected
3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2	RO	0x0	RXGOCTIS MMC Receive Good Octet Counter Interrupt Status This bit is set when the rxoctetcount_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive Good Octet Counter Interrupt Status not detected 1'b1: MMC Receive Good Octet Counter Interrupt Status detected
1	RO	0x0	RXGBOCTIS MMC Receive Good Bad Octet Counter Interrupt Status This bit is set when the rxoctetcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive Good Bad Octet Counter Interrupt Status not detected 1'b1: MMC Receive Good Bad Octet Counter Interrupt Status detected
0	RO	0x0	RXGBPKTIS MMC Receive Good Bad Packet Counter Interrupt Status This bit is set when the rxpacketcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive Good Bad Packet Counter Interrupt Status not detected 1'b1: MMC Receive Good Bad Packet Counter Interrupt Status detected

GMAC_MMC_TX_INTERRUPT

Address: Operational Base(0x21C70000) + offset (0x0708)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23	RO	0x0	TXPAUSPIS MMC Transmit Pause Packet Counter Interrupt Status This bit is set when the txpausepacketserror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 0x0 (INACTIVE): MMC Transmit Pause Packet Counter Interrupt Status not detected 0x1 (ACTIVE): MMC Transmit Pause Packet Counter Interrupt Status detected
22	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
21	RO	0x0	TXGPKTIS MMC Transmit Good Packet Counter Interrupt Status This bit is set when the txpacketcount_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Transmit Good Packet Counter Interrupt Status not detected 1'b1: MMC Transmit Good Packet Counter Interrupt Status detected
20	RO	0x0	TXGOCTIS MMC Transmit Good Octet Counter Interrupt Status This bit is set when the txoctetcount_g counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Transmit Good Octet Counter Interrupt Status not detected 1'b1: MMC Transmit Good Octet Counter Interrupt Status detected
19	RO	0x0	TXCARERPIS MMC Transmit Carrier Error Packet Counter Interrupt Status This bit is set when the txcarriererror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Transmit Carrier Error Packet Counter Interrupt Status not detected 1'b1: MMC Transmit Carrier Error Packet Counter Interrupt Status detected
18:14	RO	0x00	reserved
13	RO	0x0	TXUFLOWERPIS MMC Transmit Underflow Error Packet Counter Interrupt Status This bit is set when the txunderflowerror counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Transmit Underflow Error Packet Counter Interrupt Status not detected 1'b1: MMC Transmit Underflow Error Packet Counter Interrupt Status detected
12:2	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
1	RO	0x0	TXGBPKTIS MMC Transmit Good Bad Packet Counter Interrupt Status This bit is set when the txpacketcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Transmit Good Bad Packet Counter Interrupt Status not detected 1'b1: MMC Transmit Good Bad Packet Counter Interrupt Status detected
0	RO	0x0	TXGBOCTIS MMC Transmit Good Bad Octet Counter Interrupt Status This bit is set when the txoctetcount_gb counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Transmit Good Bad Octet Counter Interrupt Status not detected 1'b1: MMC Transmit Good Bad Octet Counter Interrupt Status detected

GMAC_MMC_RX_INTERRUPT_MASK

Address: Operational Base(0x21C70000) + offset (0x070C)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RW	0x0	RXFOVPIM MMC Receive FIFO Overflow Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxfifooverflow counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive FIFO Overflow Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive FIFO Overflow Packet Counter Interrupt Mask is enabled
20:19	RO	0x0	reserved
18	RW	0x0	RXLENERPIM MMC Receive Length Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxlengtherror counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive Length Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive Length Error Packet Counter Interrupt Mask is enabled
17:11	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
10	RW	0x0	RXPAUSPIM MMC Receive Pause Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxpausepackets counter reaches half of the maximum value or the maximum value. Values: 0x0 (DISABLE): MMC Receive Pause Packet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Receive Pause Packet Counter Interrupt Mask is enabled
9:6	RO	0x0	reserved
5	RW	0x0	RXCRCERPIM MMC Receive CRC Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxcrcerror counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive CRC Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive CRC Error Packet Counter Interrupt Mask is enabled
4	RW	0x0	RXMCGPIM MMC Receive Multicast Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxmulticastpackets_g counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive Multicast Good Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive Multicast Good Packet Counter Interrupt Mask is enabled
3	RO	0x0	reserved
2	RW	0x0	RXGOCTIM MMC Receive Good Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxoctetcount_g counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive Good Octet Counter Interrupt Mask is disabled 1'b1: MMC Receive Good Octet Counter Interrupt Mask is enabled
1	RW	0x0	RXGBOCTIM MMC Receive Good Bad Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxoctetcount_gb counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive Good Bad Octet Counter Interrupt Mask is disabled 1'b1: MMC Receive Good Bad Octet Counter Interrupt Mask is enabled

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Bit	Attr	Reset Value	Description
0	RW	0x0	RXGBPKTIM MMC Receive Good Bad Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxpacketcount_gb counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive Good Bad Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive Good Bad Packet Counter Interrupt Mask is enabled

GMAC_MMC_TX_INTERRUPT_MASK

Address: Operational Base(0x21C70000) + offset (0x0710)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23	RW	0x0	TXPAUSPIM MMC Transmit Pause Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txpausepackets counter reaches half of the maximum value or the maximum value. Values: 0x0 (DISABLE): MMC Transmit Pause Packet Counter Interrupt Mask is disabled 0x1 (ENABLE): MMC Transmit Pause Packet Counter Interrupt Mask is enabled
22	RO	0x0	reserved
21	RW	0x0	TXGPKTIM MMC Transmit Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txpacketcount_g counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Transmit Good Packet Counter Interrupt Mask is disabled 1'b1: MMC Transmit Good Packet Counter Interrupt Mask is enabled
20	RW	0x0	TXGOCTIM MMC Transmit Good Octet Counter Interrupt Mask Setting this bit masks the interrupt when the txoctetcount_g counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Transmit Good Octet Counter Interrupt Mask is disabled 1'b1: MMC Transmit Good Octet Counter Interrupt Mask is enabled

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Bit	Attr	Reset Value	Description
19	RW	0x0	TXCARERPIM MMC Transmit Carrier Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txcarriererror counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Transmit Carrier Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Transmit Carrier Error Packet Counter Interrupt Mask is enabled
18:14	RO	0x00	reserved
13	RW	0x0	TXUFLOWERPIM MMC Transmit Underflow Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txunderflowerror counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Transmit Underflow Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Transmit Underflow Error Packet Counter Interrupt Mask is enabled
12:2	RO	0x000	reserved
1	RW	0x0	TXGBPKTIM MMC Transmit Good Bad Packet Counter Interrupt Mask Setting this bit masks the interrupt when the txpacketcount_gb counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Transmit Good Bad Packet Counter Interrupt Mask is disabled 1'b1: MMC Transmit Good Bad Packet Counter Interrupt Mask is enabled
0	RW	0x0	TXGBOCTIM MMC Transmit Good Bad Octet Counter Interrupt Mask Setting this bit masks the interrupt when the txoctetcount_gb counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Transmit Good Bad Octet Counter Interrupt Mask is disabled 1'b1: MMC Transmit Good Bad Octet Counter Interrupt Mask is enabled

GMAC_TX_OCTET_COUNT_GOOD_BAD

Address: Operational Base(0x21C70000) + offset (0x0714)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXOCTGB Tx Octet Count Good Bad This field indicates the number of bytes transmitted, exclusive of preamble and retried bytes, in good and bad packets.

GMAC_TX_PACKET_COUNT_GOOD_BAD

Address: Operational Base(0x21C70000) + offset (0x0718)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXPKTGB Tx Packet Count Good Bad This field indicates the number of good and bad packets transmitted, exclusive of retried packets.

GMAC_TX_UNDERFLOW_ERROR_PACKETS

Address: Operational Base(0x21C70000) + offset (0x0748)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXUNDRFLW Tx Underflow Error Packets This field indicates the number of packets aborted because of packets underflow error.

GMAC_TX_CARRIER_ERROR_PACKETS

Address: Operational Base(0x21C70000) + offset (0x0760)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXCARR Tx Carrier Error Packets This field indicates the number of packets aborted because of carrier sense error (no carrier or loss of carrier).

GMAC_TX_OCTET_COUNT_GOOD

Address: Operational Base(0x21C70000) + offset (0x0764)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXOCTG Tx Octet Count Good This field indicates the number of bytes transmitted, exclusive of preamble, only in good packets.

GMAC_TX_PACKET_COUNT_GOOD

Address: Operational Base(0x21C70000) + offset (0x0768)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXPKTG Tx Packet Count Good This field indicates the number of good packets transmitted.

GMAC_TX_PAUSE_PACKETS

Address: Operational Base(0x21C70000) + offset (0x0770)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXPAUSE Tx Pause Packets This field indicates the number of good Pause packets transmitted.

GMAC_RX_PACKETS_COUNT_GOOD_BAD

Address: Operational Base(0x21C70000) + offset (0x0780)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXPKTGB Rx Packets Count Good Bad This field indicates the number of good and bad packets received.

GMAC_RX_OCTET_COUNT_GOOD_BAD

Address: Operational Base(0x21C70000) + offset (0x0784)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXOCTGB Rx Octet Count Good Bad This field indicates the number of bytes received, exclusive of preamble, in good and bad packets.

GMAC_RX_OCTET_COUNT_GOOD

Address: Operational Base(0x21C70000) + offset (0x0788)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXOCTG Rx Octet Count Good This field indicates the number of bytes received, exclusive of preamble, only in good packets.

GMAC_RX_MULTICAST_PACKETS_GOOD

Address: Operational Base(0x21C70000) + offset (0x0790)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXMCASTG Rx Multicast Packets Good This field indicates the number of good multicast packets received.

GMAC_RX_CRC_ERROR_PACKETS

Address: Operational Base(0x21C70000) + offset (0x0794)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXCRCERR Rx CRC Error Packets This field indicates the number of packets received with CRC error.

GMAC_RX_LENGTH_ERROR_PACKETS

Address: Operational Base(0x21C70000) + offset (0x07C8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXLENERR Rx Length Error Packets This field indicates the number of packets received with length error (Length Type field not equal to packet size), for all packets with valid length field.

GMAC_RX_PAUSE_PACKETS

Address: Operational Base(0x21C70000) + offset (0x07D0)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXPAUSEPKT Rx Pause Packets This field indicates the number of good and valid Pause packets received.

GMAC_RX_FIFO_OVERFLOW_PACKETS

Address: Operational Base(0x21C70000) + offset (0x07D4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXFIFOOVFL Rx FIFO Overflow Packets This field indicates the number of missed received packets because of FIFO overflow.

GMAC_MMC_IPC_RX_INTERRUPT_MASK

Address: Operational Base(0x21C70000) + offset (0x0800)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	RXICMPEROIM MMC Receive ICMP Error Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxicmp_err_octets counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive ICMP Error Octet Counter Interrupt Mask is disabled 1'b1: MMC Receive ICMP Error Octet Counter Interrupt Mask is enabled
28	RO	0x0	reserved
27	RW	0x0	RXTCPEROIM MMC Receive TCP Error Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxtcp_err_octets counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive TCP Error Octet Counter Interrupt Mask is disabled 1'b1: MMC Receive TCP Error Octet Counter Interrupt Mask is enabled
26	RO	0x0	reserved
25	RW	0x0	RXUDPEROIM MMC Receive UDP Error Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxudp_err_octets counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive UDP Error Octet Counter Interrupt Mask is disabled 1'b1: MMC Receive UDP Error Octet Counter Interrupt Mask is enabled
24:23	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
22	RW	0x0	RXIPV6HEROIM MMC Receive IPV6 Header Error Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv6_nopay_octets counter reaches half of the maximum value or the maximum value. Value: 1'b0: MMC Receive IPV6 Header Error Octet Counter Interrupt Mask is disabled 1'b1: MMC Receive IPV6 Header Error Octet Counter Interrupt Mask is enabled
21:18	RO	0x0	reserved
17	RW	0x0	RXIPV4HEROIM MMC Receive IPV4 Header Error Octet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv4_hdrerr_octets counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive IPV4 Header Error Octet Counter Interrupt Mask is disabled 1'b1: MMC Receive IPV4 Header Error Octet Counter Interrupt Mask is enabled
16:14	RO	0x0	reserved
13	RW	0x0	RXICMPERPIM MMC Receive ICMP Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxicmp_err_pkts counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive ICMP Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive ICMP Error Packet Counter Interrupt Mask is enabled
12	RO	0x0	reserved
11	RW	0x0	RXTCPERPIM MMC Receive TCP Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxtcp_err_pkts counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive TCP Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive TCP Error Packet Counter Interrupt Mask is enabled
10	RO	0x0	reserved
9	RW	0x0	RXUDPERPIM MMC Receive UDP Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxudp_err_pkts counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive UDP Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive UDP Error Packet Counter Interrupt Mask is enabled
8:7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6	RW	0x0	RXIPV6HERPIM MMC Receive IPV6 Header Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv6_hdrerr_pkts counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive IPV6 Header Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive IPV6 Header Error Packet Counter Interrupt Mask is enabled
5	RW	0x0	RXIPV6GPIM MMC Receive IPV6 Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv6_gd_pkts counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive IPV6 Good Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive IPV6 Good Packet Counter Interrupt Mask is enabled
4:2	RO	0x0	reserved
1	RW	0x0	RXIPV4HERPIM MMC Receive IPV4 Header Error Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv4_hdrerr_pkts counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive IPV4 Header Error Packet Counter Interrupt Mask is disabled 1'b1: MMC Receive IPV4 Header Error Packet Counter Interrupt Mask is enabled
0	RW	0x0	RXIPV4GPIM MMC Receive IPV4 Good Packet Counter Interrupt Mask Setting this bit masks the interrupt when the rxipv4_gd_pkts counter reaches half of the maximum value or the maximum value. Values: 1'b0: MMC Receive IPV4 Good Packet Counter Interrupt Mask is disable 1'b1: MMC Receive IPV4 Good Packet Counter Interrupt Mask is enabled

GMAC_MMC_IPC_RX_INTERRUPT

Address: Operational Base(0x21C70000) + offset (0x0808)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29	RO	0x0	RXICMPEROIS MMC Receive ICMP Error Octet Counter Interrupt Status This bit is set when the rxicmp_err_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive ICMP Error Octet Counter Interrupt Status not detected 1'b1: MMC Receive ICMP Error Octet Counter Interrupt Status detected
28	RO	0x0	reserved
27	RO	0x0	RXTCPEROIS MMC Receive TCP Error Octet Counter Interrupt Status This bit is set when the rxtcp_err_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive TCP Error Octet Counter Interrupt Status not detected 1'b1: MMC Receive TCP Error Octet Counter Interrupt Status detected
26	RO	0x0	reserved
25	RO	0x0	RXUDPEROIS MMC Receive UDP Error Octet Counter Interrupt Status This bit is set when the rxudp_err_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive UDP Error Octet Counter Interrupt Status not detected 1'b1: MMC Receive UDP Error Octet Counter Interrupt Status detected
24:23	RO	0x0	reserved
22	RO	0x0	RXIPV6HEROIS MMC Receive IPV6 Header Error Octet Counter Interrupt Status This bit is set when the rxipv6_hdrerr_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive IPV6 Header Error Octet Counter Interrupt Status not detected 1'b1: MMC Receive IPV6 Header Error Octet Counter Interrupt Status detected
21:18	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
17	RO	0x0	RXIPV4HEROIS MMC Receive IPV4 Header Error Octet Counter Interrupt Status This bit is set when the rxipv4_hdrerr_octets counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive IPV4 Header Error Octet Counter Interrupt Status not detected 1'b1: MMC Receive IPV4 Header Error Octet Counter Interrupt Status detected
16:14	RO	0x0	reserved
13	RO	0x0	RXICMPERPIS MMC Receive ICMP Error Packet Counter Interrupt Status This bit is set when the rxicmp_err_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive ICMP Error Packet Counter Interrupt Status not detected 1'b1: MMC Receive ICMP Error Packet Counter Interrupt Status detected
12	RO	0x0	reserved
11	RO	0x0	RXTCPERPIS MMC Receive TCP Error Packet Counter Interrupt Status This bit is set when the rxtcp_err_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive TCP Error Packet Counter Interrupt Status not detected 1'b1: MMC Receive TCP Error Packet Counter Interrupt Status detected
10	RO	0x0	reserved
9	RO	0x0	RXUDPERPIS MMC Receive UDP Error Packet Counter Interrupt Status This bit is set when the rxudp_err_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive UDP Error Packet Counter Interrupt Status not detected 1'b1: MMC Receive UDP Error Packet Counter Interrupt Status detected
8:7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6	RO	0x0	RXIPV6HERPIS MMC Receive IPV6 Header Error Packet Counter Interrupt Status This bit is set when the rxipv6_hdrerr_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive IPV6 Header Error Packet Counter Interrupt Status not detected 1'b1: MMC Receive IPV6 Header Error Packet Counter Interrupt Status detected
5	RO	0x0	RXIPV6GPIS MMC Receive IPV6 Good Packet Counter Interrupt Status This bit is set when the rxipv6_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive IPV6 Good Packet Counter Interrupt Status not detected 1'b1: MMC Receive IPV6 Good Packet Counter Interrupt Status detected
4:2	RO	0x0	reserved
1	RO	0x0	RXIPV4HERPIS MMC Receive IPV4 Header Error Packet Counter Interrupt Status This bit is set when the rxipv4_hdrerr_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive IPV4 Header Error Packet Counter Interrupt Status not detected 1'b1: MMC Receive IPV4 Header Error Packet Counter Interrupt Status detected
0	RO	0x0	RXIPV4GPIS MMC Receive IPV4 Good Packet Counter Interrupt Status This bit is set when the rxipv4_gd_pkts counter reaches half of the maximum value or the maximum value. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: MMC Receive IPV4 Good Packet Counter Interrupt Status not detected 1'b1: MMC Receive IPV4 Good Packet Counter Interrupt Status detected

GMAC_RXIPV4_GOOD_PACKETS

Address: Operational Base(0x21C70000) + offset (0x0810)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXIPV4GDPKT RxIPv4 Good Packets This field indicates the number of good IPv4 datagrams received with the TCP, UDP, or ICMP payload.

GMAC_RXIPV4_HEADER_ERROR_PACKETS

Address: Operational Base(0x21C70000) + offset (0x0814)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXIPV4HDRERRPKT RxIPv4 Header Error Packets This field indicates the number of IPv4 datagrams received with header (checksum, length, or version mismatch) errors.

GMAC_RXIPV6_GOOD_PACKETS

Address: Operational Base(0x21C70000) + offset (0x0824)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXIPV6GDPKT RxIPv6 Good Packets This field indicates the number of good IPv6 datagrams received with the TCP, UDP, or ICMP payload.

GMAC_RXIPV6_HEADER_ERROR_PACKETS

Address: Operational Base(0x21C70000) + offset (0x0828)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXIPV6HDRERRPKT RxIPv6 Header Error Packets This field indicates the number of IPv6 datagrams received with header (length or version mismatch) errors.

GMAC_RXUDP_ERROR_PACKETS

Address: Operational Base(0x21C70000) + offset (0x0834)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXUDPERRPKT RxUDP Error Packets This field indicates the number of good IP datagrams received whose UDP payload has a checksum error.

GMAC_RXTCP_ERROR_PACKETS

Address: Operational Base(0x21C70000) + offset (0x083C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXTCPERRPKT RxTCP Error Packets This field indicates the number of good IP datagrams received whose TCP payload has a checksum error.

GMAC_RXICMP_ERROR_PACKETS

Address: Operational Base(0x21C70000) + offset (0x0844)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXICMPERRPKT RxICMP Error Packets This field indicates the number of good IP datagrams received whose ICMP payload has a checksum error.

GMAC_RXIPV4_HEADER_ERROR_OCTETS

Address: Operational Base(0x21C70000) + offset (0x0854)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXIPV4HDRERROCT RxIPv4 Header Error Octets This field indicates the number of bytes received in IPv4 datagrams with header errors (checksum, length, version mismatch). The value in the Length field of IPv4 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

GMAC_RXIPV6_HEADER_ERROR_OCTETS

Address: Operational Base(0x21C70000) + offset (0x0868)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXIPV6HDRERROCT RxIPv6 Header Error Octets This field indicates the number of bytes received in IPv6 datagrams with header errors (length, version mismatch). The value in the Length field of IPv6 header is used to update this counter. (Ethernet header, FCS, pad, or IP pad bytes are not included in this counter.

GMAC_RXUDP_ERROR_OCTETS

Address: Operational Base(0x21C70000) + offset (0x0874)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXUDPERROCT RxUDP Error Octets This field indicates the number of bytes received in a UDP segment that had checksum errors. This counter does not count IP header bytes.

GMAC_RXTCP_ERROR_OCTETS

Address: Operational Base(0x21C70000) + offset (0x087C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXTCPERROCT RxTCP Error Octets This field indicates the number of bytes received in a TCP segment that had checksum errors. This counter does not count IP header bytes.

GMAC_RXICMP_ERROR_OCTETS

Address: Operational Base(0x21C70000) + offset (0x0884)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXICMPERROCT RxICMP Error Octets This field indicates the number of bytes received in a ICMP segment that had checksum errors. This counter does not count IP header bytes.

GMAC_MAC_TIMESTAMP_CONTROL

Address: Operational Base(0x21C70000) + offset (0x0B00)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	AV8021ASMEN AV 802.1AS Mode Enable When this bit is set, the MAC processes only untagged PTP over Ethernet packets for providing PTP status and capturing timestamp snapshots, that is, IEEE 802.1AS mode of operation. When PTP offload feature is enabled, for the purpose of PTP offload, the transport specific field in the PTP header is generated and checked based on the value of this bit. Values: 1'b0: AV 802.1AS Mode is disabled 1'b1: AV 802.1AS Mode is enabled
27:25	RO	0x0	reserved
24	RW	0x0	TXTSSTSM Transmit Timestamp Status Mode When this bit is set, the MAC overwrites the earlier transmit timestamp status even if it is not read by the software. The MAC indicates this by setting the TXTSSMIS bit of the MAC_Tx_Timestamp_Status_Nanoseconds register. When this bit is reset, the MAC ignores the timestamp status of current packet if the timestamp status of previous packet is not read by the software. The MAC indicates this by setting the TXTSSMIS bit of the MAC_Tx_Timestamp_Status_Nanoseconds register. Values: 1'b0: Transmit Timestamp Status Mode is disabled 1'b1: Transmit Timestamp Status Mode is enabled
23:19	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
18	RW	0x0	TSENMACADDR Enable MAC Address for PTP Packet Filtering When this bit is set, the DA MAC address (that matches any MAC Address register) is used to filter the PTP packets when PTP is directly sent over Ethernet. When this bit is set, received PTP packets with DA containing a special multicast or unicast address that matches the one programmed in MAC address registers are considered for processing as indicated below, when PTP is directly sent over Ethernet. For normal time stamping operation, MAC address registers 0 to 31 is considered for unicast destination address matching. For PTP offload, only MAC address register 0 is considered for unicast destination address matching. Values: 1'b0: MAC Address for PTP Packet Filtering is disabled 1'b1: MAC Address for PTP Packet Filtering is enabled
17:16	RW	0x0	SNAPTYPSEL Select PTP packets for Taking Snapshots These bits, along with Bits 15 and 14, decide the set of PTP packet types for which snapshot needs to be taken. The encoding is given in Timestamp Snapshot Dependency on Register Bits Table.
15	RW	0x0	TSMSTRENA Enable Snapshot for Messages Relevant to Master When this bit is set, the snapshot is taken only for the messages that are relevant to the master node. Otherwise, the snapshot is taken for the messages relevant to the slave node. Values: 1'b0: Snapshot for Messages Relevant to Master is disabled 1'b1: Snapshot for Messages Relevant to Master is enabled
14	RW	0x0	TSEVNTENA Enable Timestamp Snapshot for Event Messages When this bit is set, the timestamp snapshot is taken only for event messages (SYNC, Delay_Req, Pdelay_Req, or Pdelay_Resp). When this bit is reset, the snapshot is taken for all messages except Announce, Management, and Signaling. For more information about the timestamp snapshots, see Timestamp Snapshot Dependency on Register Bits Table. Values: 1'b0: Timestamp Snapshot for Event Messages is disabled 1'b1: Timestamp Snapshot for Event Messages is enabled
13	RW	0x0	TSIPV4ENA Enable Processing of PTP Packets Sent over IPv4-UDP When this bit is set, the MAC receiver processes the PTP packets encapsulated in IPv4-UDP packets. When this bit is reset, the MAC ignores the PTP transported over IPv4-UDP packets. This bit is set by default. Values: 1'b0: Processing of PTP Packets Sent over IPv4-UDP is disabled 1'b1: Processing of PTP Packets Sent over IPv4-UDP is enabled

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Bit	Attr	Reset Value	Description
12	RW	0x0	TSIPV6ENA Enable Processing of PTP Packets Sent over IPv6-UDP When this bit is set, the MAC receiver processes the PTP packets encapsulated in IPv6-UDP packets. When this bit is clear, the MAC ignores the PTP transported over IPv6-UDP packets. Values: 1'b0: Processing of PTP Packets Sent over IPv6-UDP is disabled 1'b1: Processing of PTP Packets Sent over IPv6-UDP is enabled
11	RW	0x0	TSIPENA Enable Processing of PTP over Ethernet Packets When this bit is set, the MAC receiver processes the PTP packets encapsulated directly in the Ethernet packets. When this bit is reset, the MAC ignores the PTP over Ethernet packets. Values: 1'b0: Processing of PTP over Ethernet Packets is disabled 1'b1: Processing of PTP over Ethernet Packets is enabled
10	RW	0x0	TSVER2ENA Enable PTP Packet Processing for Version 2 Format When this bit is set, the IEEE 1588 version 2 format is used to process the PTP packets. When this bit is reset, the IEEE 1588 version 1 format is used to process the PTP packets. The IEEE 1588 formats are described in 'PTP Processing and Control'. Values: 1'b0: PTP Packet Processing for Version 2 Format is disabled 1'b1: PTP Packet Processing for Version 2 Format is enabled
9	RW	0x0	TSCTRLSSR Timestamp Digital or Binary Rollover Control When this bit is set, the Timestamp Low register rolls over after 0x3B9A_C9FF value (that is, 1 nanosecond accuracy) and increments the timestamp (High) seconds. When this bit is reset, the rollover value of sub-second register is 0x7FFF_FFFF. The sub-second increment must be programmed correctly depending on the PTP reference clock frequency and the value of this bit. Values: 1'b0: Timestamp Digital or Binary Rollover Control is disabled 1'b1: Timestamp Digital or Binary Rollover Control is enabled
8	RW	0x0	TSENALL Enable Timestamp for All Packets When this bit is set, the timestamp snapshot is enabled for all packets received by the MAC. Values: 1'b0: Timestamp for All Packets disabled 1'b1: Timestamp for All Packets enabled
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6	RW	0x0	PTGE Presentation Time Generation Enable When this bit is set the Presentation Time generation will be enabled. Values: 0x0 (DISABLE): Presentation Time Generation is disabled 0x1 (ENABLE): Presentation Time Generation is enabled
5	RW	0x0	TSADDREG Update Addend Register When this bit is set, the content of the Timestamp Addend register is updated in the PTP block for fine correction. This bit is cleared when the update is complete. This bit should be zero before it is set. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Addend Register is not updated 1'b1: Addend Register is updated
4	RO	0x0	reserved
3	RW	0x0	TSUPDT Update Timestamp When this bit is set, the system time is updated (added or subtracted) with the value specified in MAC_System_Time_Seconds_Update and MAC_System_Time_Nanoseconds_Update registers. This bit should be zero before updating it. This bit is reset when the update is complete in hardware. The Timestamp Higher Word register (if enabled during core configuration) is not updated.When Media Clock Generation and Recovery is configured (DWC_EQOS_FLEXI_PPS_OUT_EN) and enabled MAC_Presn_Time_Updt should also be updated before setting this field. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Timestamp is not updated 1'b1: Timestamp is updated
2	RW	0x0	TSINIT Initalize Timestamp When this bit is set, the system time is initialized (overwritten) with the value specified in the MAC_System_Time_Seconds_Update and MAC_System_Time_Nanoseconds_Update registers. This bit should be zero before it is updated. This bit is reset when the initialization is complete. The Timestamp Higher Word register (if enabled during core configuration) can only be initialized.When Media Clock Generation and Recovery is configured (DWC_EQOS_FLEXI_PPS_OUT_EN) and enabled MAC_Presn_Time_Updt should also be updated before setting this field. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Timestamp is not initialized 1'b1: Timestamp is initialized

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Bit	Attr	Reset Value	Description
1	RW	0x0	TSCFUPDT Fine or Coarse Timestamp Update When this bit is set, the Fine method is used to update system timestamp. When this bit is reset, Coarse method is used to update the system timestamp. Values: 1'b0: Coarse method is used to update system timestamp 1'b1: Fine method is used to update system timestamp
0	RW	0x0	TSENA Enable Timestamp When this bit is set, the timestamp is added for Transmit and Receive packets. When disabled, timestamp is not added for transmit and receive packets and the Timestamp Generator is also suspended. You need to initialize the Timestamp (system time) after enabling this mode.On the Receive side, the MAC processes the 1588 packets only if this bit is set. Values: 1'b0: Timestamp is disabled 1'b1: Timestamp is enabled

GMAC_MAC_SUB_SECOND_INCREMENT

Address: Operational Base(0x21C70000) + offset (0x0B04)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	SSINC Sub-second Increment Value The value programmed in this field is accumulated every clock cycle (of clk_ptp_i) with the contents of the sub-second register. For example, when the PTP clock is 50 MHz (period is 20 ns), you should program 20 (0x14) when the System Time Nanoseconds register has an accuracy of 1 ns [Bit 9 (TSCTRLSSR) is set in MAC_Timestamp_Control]. When TSCTRLSSR is clear, the Nanoseconds register has a resolution of ~0.465 ns. In this case, you should program a value of 43 (0x2B) which is derived by 20 ns/0.465.
15:0	RO	0x0000	reserved

GMAC_MAC_SYSTEM_TIME_SECS

Address: Operational Base(0x21C70000) + offset (0x0B08)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TSS Timestamp Second The value in this field indicates the current value in seconds of the System Time maintained by the MAC.

GMAC_MAC_SYSTEM_TIME_NS

Address: Operational Base(0x21C70000) + offset (0x0B0C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
30:0	RW	0x00000000	TSSS Timestamp Sub Seconds The value in this field has the sub-second representation of time, with an accuracy of 0.46 ns. When Bit 9 is set in MAC_Timestamp_Control, each bit represents 1 ns. The maximum value is 0x3B9A_C9FF after which it rolls-over to zero.

GMAC_MAC_SYS_TIME_SECS_UPDATE

Address: Operational Base(0x21C70000) + offset (0x0B10)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TSS Timestamp Seconds The value in this field is the seconds part of the update. When ADDSUB is reset, this field must be programmed with the seconds part of the update value. When ADDSUB is set, this field must be programmed with the complement of the seconds part of the update value. For example, if 2.000000001 seconds need to be subtracted from the system time, the TSS field in the MAC_Timestamp_Seconds_Update register must be 0xFFFF_FFFE (that is, 2^32 - 2).

GMAC_MAC_SYS_TIME_NS_UPDATE

Address: Operational Base(0x21C70000) + offset (0x0B14)

Bit	Attr	Reset Value	Description
31	RW	0x0	ADDSUB Add or Subtract Time When this bit is set, the time value is subtracted with the contents of the update register. When this bit is reset, the time value is added with the contents of the update register. Values: 1'b0: Add time 1'b1: Subtract time

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Bit	Attr	Reset Value	Description
30:0	RW	0x00000000	TSSS Timestamp Sub Seconds The value in this field is the sub-seconds part of the update. When ADDSUB is reset, this field must be programmed with the sub-seconds part of the update value, with an accuracy based on the TSCTRLSSR bit of the MAC_Timestamp_Control register.When ADDSUB is set, this field must be programmed with the complement of the sub-seconds part of the update value as described below. When TSCTRLSSR bit in MAC_Timestamp_Control is set, the programmed value must be 10^9 - <sub-second value>. When TSCTRLSSR bit in MAC_Timestamp_Control is reset, the programmed value must be 2^31 - <sub-second_value>. When the TSCTRLSSR bit is reset in the MAC_Timestamp_Control register, each bit represents an accuracy of 0.46 ns. When the TSCTRLSSR bit is set in the MAC_Timestamp_Control register, each bit represents 1 ns and the programmed value should not exceed 0x3B9A_C9FF. For example, if 2.000000001 seconds need to be subtracted from the system time, then the TSSS field in the MAC_Timestamp_Nanoseconds_Update register must be 0x7FFF_FFFF (that is, 2^31 - 1), when TSCTRLSSR bit in MAC_Timestamp_Control is reset and 0x3B9A_C9FF (that is, 10^9 - 1), when TSCTRLSSR bit in MAC_Timestamp_Control is set.

GMAC_MAC_TIMESTAMP_ADDEND

Address: Operational Base(0x21C70000) + offset (0x0B18)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TSAR Timestamp Addend Register This field indicates the 32-bit time value to be added to the Accumulator register to achieve time synchronization.

GMAC_MAC_TIMESTAMP_STATUS

Address: Operational Base(0x21C70000) + offset (0x0B20)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RO	0x00	ATSNS Number of Auxiliary Timestamp Snapshots This field indicates the number of Snapshots available in the FIFO. A value equal to the selected depth of FIFO (4, 8, or 16) indicates that the Auxiliary Snapshot FIFO is full. These bits are cleared (to 00000) when the Auxiliary snapshot FIFO clear bit is set. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected.

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Bit	Attr	Reset Value	Description
24	RO	0x0	ATSSTM Auxiliary Timestamp Snapshot Trigger Missed This bit is set when the Auxiliary timestamp snapshot FIFO is full and external trigger was set. This indicates that the latest snapshot is not stored in the FIFO. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected. Values: 1'b0: Auxiliary Timestamp Snapshot Trigger Missed status not detected 1'b1: Auxiliary Timestamp Snapshot Trigger Missed status detected
23:16	RO	0x00	reserved
15	RO	0x0	TXTSSIS Tx Timestamp Status Interrupt Status In non-EQOS_CORE configurations when drop transmit status is enabled in MTL, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and MAC_Tx_Timestamp_Status_Seconds registers. When PTP offload feature is enabled, this bit is set when the captured transmit timestamp is updated in the MAC_Tx_Timestamp_Status_Nanoseconds and MAC_Tx_Timestamp_Status_Seconds registers, for PTO generated Delay Request and Pdelay request packets. This bit is cleared when the MAC_Tx_Timestamp_Status_Seconds register is read (or write to MAC_Tx_Timestamp_Status_Seconds register when RCWE bit of MAC_CSR_SW_Ctrl register is set). Values: 1'b0: Tx Timestamp Status Interrupt status not detected 1'b1: Tx Timestamp Status Interrupt status detected
14:4	RO	0x000	reserved
3	RO	0x0	TSTRGTERR0 Timestamp Target Time Error This bit is set when the latest target time programmed in the MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds registers elapses. This bit is cleared when the application reads this bit. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: Timestamp Target Time Error status not detected 1'b1: Timestamp Target Time Error status detected

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Bit	Attr	Reset Value	Description
2	RO	0x0	AUXTSTRIG Auxiliary Timestamp Trigger Snapshot This bit is set high when the auxiliary snapshot is written to the FIFO. This bit is valid only if the Add IEEE 1588 Auxiliary Snapshot option is selected. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: Auxiliary Timestamp Trigger Snapshot status not detected 1'b1: Auxiliary Timestamp Trigger Snapshot status detected
1	RO	0x0	TSTARGT0 Timestamp Target Time Reached When set, this bit indicates that the value of system time is greater than or equal to the value specified in the MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds registers. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: Timestamp Target Time Reached status not detected 1'b1: Timestamp Target Time Reached status detected
0	RO	0x0	TSSOVF Timestamp Seconds Overflow When this bit is set, it indicates that the seconds value of the timestamp (when supporting version 2 format) has overflowed beyond 32'hFFFF_FFFF. Access restriction applies. Clears on read (or this bit is written to 1 when RCWE bit in MAC_CSR_SW_Ctrl register is set). Self-set to 1 on internal event. Values: 1'b0: Timestamp Seconds Overflow status not detected 1'b1: Timestamp Seconds Overflow status detected

GMAC_MAC_TX_TS_STATUS_NS

Address: Operational Base(0x21C70000) + offset (0x0B30)

Bit	Attr	Reset Value	Description
31	RO	0x0	TXTSSMIS Transmit Timestamp Status Missed When this bit is set, it indicates one of the following: 1. The timestamp of the current packet is ignored if TXTSSTSM bit of the MAC_Timestamp_Control register is reset. 2. The timestamp of the previous packet is overwritten with timestamp of the current packet if TXTSSTSM bit of the MAC_Timestamp_Control register is set. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: Transmit Timestamp Status Missed status not detected 1'b1: Transmit Timestamp Status Missed status detected

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Bit	Attr	Reset Value	Description
30:0	RO	0x00000000	TXTSSLO Transmit Timestamp Status Low This field contains the 31 bits of the Nanoseconds field of the Transmit packet's captured timestamp.

GMAC_MAC_TX_TS_STATUS_SECS

Address: Operational Base(0x21C70000) + offset (0x0B34)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TXTSSHI Transmit Timestamp Status High This field contains the lower 32 bits of the Seconds field of Transmit packet's captured timestamp.

GMAC_MAC_AUXILIARY_CONTROL

Address: Operational Base(0x21C70000) + offset (0x0B40)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	ATSEN0 Auxiliary Snapshot 0 Enable This bit controls the capturing of Auxiliary Snapshot Trigger 0. When this bit is set, the auxiliary snapshot of the event on ptp_aux_trig_i[0] input is enabled. When this bit is reset, the events on this input are ignored. Values: 0x0 (DISABLE): Auxiliary Snapshot 0 is disabled 0x1 (ENABLE): Auxiliary Snapshot 0 is enabled
3:1	RO	0x0	reserved
0	RW	0x0	ATSFC Auxiliary Snapshot FIFO Clear When set, this bit resets the pointers of the Auxiliary Snapshot FIFO. This bit is cleared when the pointers are reset and the FIFO is empty. When this bit is high, the auxiliary snapshots are stored in the FIFO. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Auxiliary Snapshot FIFO Clear is disabled 1'b1: Auxiliary Snapshot FIFO Clear is enabled

GMAC_MAC_AUXILIARY_TS_NS

Address: Operational Base(0x21C70000) + offset (0x0B48)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:0	RO	0x00000000	AUXTSLO Auxiliary Timestamp Contains the lower 31 bits (nanoseconds field) of the auxiliary timestamp.

GMAC_MAC_AUXILIARY_TS_SECS

Address: Operational Base(0x21C70000) + offset (0x0B4C)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	AUXTSHI Auxiliary Timestamp Contains the lower 32 bits of the Seconds field of the auxiliary timestamp.

GMAC_MAC_TS_INGRESS_CORR_NS

Address: Operational Base(0x21C70000) + offset (0x0B58)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TSIC Timestamp Ingress Correction This field contains the ingress path correction value as defined by the Ingress Correction expression.

GMAC_MAC_TS_EGRESS_CORR_NS

Address: Operational Base(0x21C70000) + offset (0x0B5C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TSEC Timestamp Egress Correction This field contains the nanoseconds part of the egress path correction value as defined by the Egress Correction expression.

GMAC_MAC_TS_INGRESS_LATENCY

Address: Operational Base(0x21C70000) + offset (0x0B68)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	ITLNS Ingress Timestamp Latency, in sub-nanoseconds This register holds the average latency in sub-nanoseconds between the input ports (phy_rxd_i) of MAC and the actual point (GMII/MII) where the ingress timestamp is taken.
15:8	RO	0x00	ITLSNS Ingress Timestamp Latency, in nanoseconds This register holds the average latency in nanoseconds between the input ports (phy_rxd_i) of MAC and the actual point (GMII/MII) where the ingress timestamp is taken.
7:0	RO	0x00	reserved

GMAC_MAC_TS_EGRESS_LATENCY

Address: Operational Base(0x21C70000) + offset (0x0B6C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RO	0x00	ETLNS Egress Timestamp Latency, in nanoseconds This register holds the average latency in nanoseconds between the actual point (GMII/MII) where the egress timestamp is taken and the output ports (phy_txd_o) of the MAC.

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Bit	Attr	Reset Value	Description
15:8	RO	0x00	ETLSNS Egress Timestamp Latency, in sub-nanoseconds This register holds the average latency in sub-nanoseconds between the actual point (GMII/MII) where the egress timestamp is taken and the output ports (phy_txd_o) of the MAC.
7:0	RO	0x00	reserved

GMAC_MAC_PPS_CONTROL

Address: Operational Base(0x21C70000) + offset (0x0B70)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RW	0x0	MCGREN0 MCGR Mode Enable for PPS0 Output This field enables the 0th PPS instance to operate in PPS or MCGR mode. When set it operates in MCGR mode and on reset it operates in PPS mode. Values: 0x0 (PPS): 0th PPS instance is enabled to operate in PPS mode 0x1 (MCGR): 0th PPS instance is enabled to operate in MCGR mode
6:5	RW	0x0	TRGTMODSEL0 Target Time Register Mode for PPS0 Output This field indicates the Target Time registers (MAC_PPS0_Target_Time_Seconds and MAC_PPS0_Target_Time_Nanoseconds) mode for PPS0 output signal: Values: 0x0 (ONLY_INT): Target Time registers are programmed only for generating the interrupt event. The Flexible PPS function must not be enabled in this mode, otherwise spurious transitions may be observed on the corresponding ptp_pps_o output port 0x1 (RSVD): Reserved 0x2 (INT_ST): Target Time registers are programmed for generating the interrupt event and starting or stopping the PPS0 output signal generation 0x3 (ONLY_ST): Target Time registers are programmed only for starting or stopping the PPS0 output signal generation. No interrupt is asserted
4	RW	0x0	PPSEN0 Flexible PPS Output Mode Enable When this bit is set, Bits[3:0] function as PPSCMD. When this bit is reset, Bits[3:0] function as PPSCTRL (Fixed PPS mode). Values: 0x0 (DISABLE): Flexible PPS Output Mode is disabled 0x1 (ENABLE): Flexible PPS Output Mode is enabled

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	PPSCTRL_PPSCMD PPS Output Frequency Control This field controls the frequency of the PPS0 output (ptp_pps_o[0]) signal. The default value of PPSCTRL is 0000, and the PPS output is 1 pulse (of width clk_ptp_i) every second. For other values of PPSCTRL, the PPS output becomes a generated clock of following frequencies: 4'b0001: The binary rollover is 2 Hz, and the digital rollover is 1 Hz. 4'b0010: The binary rollover is 4 Hz, and the digital rollover is 2 Hz. 4'b0011: The binary rollover is 8 Hz, and the digital rollover is 4 Hz. 4'b0100: The binary rollover is 16 Hz, and the digital rollover is 8 Hz. ... 4'b1111: The binary rollover is 32.768 KHz and the digital rollover is 16.384 KHz. Note: In the binary rollover mode, the PPS output (ptp_pps_o) has a duty cycle of 50 percent with these frequencies. In the digital rollover mode, the PPS output frequency is an average number. The actual clock is of different frequency that gets synchronized every second. For example: 1. When PPSCTRL = 0001, the PPS (1 Hz) has a low period of 537 ms and a high period of 463 ms. 2. When PPSCTRL = 0010, the PPS (2 Hz) is a sequence of One clock of 50 percent duty cycle and 537 ms period Second clock of 463 ms period (268 ms low and 195 ms high). 3. When PPSCTRL = 0011, the PPS (4 Hz) is a sequence of Three clocks of 50 percent duty cycle and 268 ms period Fourth clock of 195 ms period (134 ms low and 61 ms high). This behavior is because of the non-linear toggling of bits in the digital rollover mode in the MAC_System_Time_Nanoseconds register.

GMAC_MAC_PPS0_TARGET_TIME_SECONDS

Address: Operational Base(0x21C70000) + offset (0x0B80)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	TSTRH0 PPS Target Time Seconds Register This field stores the time in seconds. When the timestamp value matches or exceeds both Target Timestamp registers, the MAC starts or stops the PPS signal output and generates an interrupt (if enabled) based on Target Time mode selected for the corresponding PPS output in the MAC_PPS_Control register. If DWC_EQOS_FLEXI_PPS_OUT_EN is enabled in the configuration and PTGE field of MAC_Timestamp_Control Register is set with Presentation time control set in recovery mode, then these bits indicate the TPT being programmed by the application and in generation mode it indicates the CPT generated at the sampled trigger.

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GMAC_MAC_PPS0_TARGET_TIME_NS

Address: Operational Base(0x21C70000) + offset (0x0B84)

Bit	Attr	Reset Value	Description
31	RW	0x0	TRGTBUSY0 PPS Target Time Register Busy The MAC sets this bit when the PPSCMD0 field in the MAC_PPS_Control register is programmed to 010 or 011. Programming the PPSCMD0 field to 010 or 011 instructs the MAC to synchronize the Target Time Registers to the PTP clock domain.The MAC clears this bit after synchronizing the Target Time Registers to the PTP clock domain The application must not update the Target Time Registers when this bit is read as 1. Otherwise, the synchronization of the previous programmed timegets corrupted. Values: 0x0 (INACTIVE): PPS Target Time Register Busy status is not detected 0x1 (ACTIVE): PPS Target Time Register Busy is detected
30:0	RW	0x00000000	TTSL0 Target Time Low for PPS Register This register stores the time in (signed) nanoseconds. When the value of the timestamp matches the value in both Target Timestamp registers, the MAC starts or stops the PPS signal output and generates an interrupt (if enabled) based on the TRGTMODSEL0 field (Bits [6:5]) in MAC_PPS_Control. When the TSCTRLSSR bit is reset in the MAC_Timestamp_Control register, this value should be (time in ns / 0.465). The actual start or stop time of the PPS signal output may have an error margin up to one unit of sub-second increment value. When the TSCTRLSSR bit is set in the MAC_Timestamp_Control register, this value should not exceed 0x3B9A_C9FF. The actual start or stop time of the PPS signal output may have an error margin up to one unit of sub-second increment value. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect.

GMAC_MTL_OPERATION_MODE

Address: Operational Base(0x21C70000) + offset (0x0C00)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9	RW	0x0	CNTCLR Counters Reset When this bit is set, all counters are reset. This bit is cleared automatically after 1 clock cycle. If this bit is set along with CNT_PRESET bit, CNT_PRESET has precedence. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 0x0 (DISABLE): Counters are not reset 0x1 (ENABLE): All counters are reset

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Bit	Attr	Reset Value	Description
8	RW	0x0	CNTPRST Counters Reset When this bit is set, all counters are reset. This bit is cleared automatically after 1 clock cycle. If this bit is set along with CNT_PRESET bit, CNT_PRESET has precedence. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 0x0 (DISABLE): Counters are not reset 0x1 (ENABLE): All counters are reset
7:2	RO	0x00	reserved
1	RW	0x0	DTXSTS Drop Transmit Status When this bit is set, the Tx packet status received from the MAC is dropped in the MTL. When this bit is reset, the Tx packet status received from the MAC is forwarded to the application. Values: 0x0 (DISABLE): Drop Transmit Status is disabled 0x1 (ENABLE): Drop Transmit Status is enabled
0	RO	0x0	reserved

GMAC_MTL_DBG_CTL

Address: Operational Base(0x21C70000) + offset (0x0C08)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	STSIE Transmit Status Available Interrupt Status Enable When this bit is set, an interrupt is generated when Transmit status is available in slave mode. Values: 1'b0: Transmit Packet Available Interrupt Status is disabled 1'b1: Transmit Packet Available Interrupt Status is enabled
14	RW	0x0	PKTIE Receive Packet Available Interrupt Status Enable When this bit is set, an interrupt is generated when EOP of received packet is written to the Rx FIFO. Values: 1'b0: Receive Packet Available Interrupt Status is disabled 1'b1: Receive Packet Available Interrupt Status is enabled
13:12	RW	0x0	FIFOSEL FIFO Selected for Access This field indicates the FIFO selected for debug access: Values: 2'b00: Tx FIFO 2'b01: Tx Status FIFO (only read access when SLVMOD is set) 2'b10: TSO FIFO (cannot be accessed when SLVMOD is set) 2'b11: Rx FIFO

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Bit	Attr	Reset Value	Description
11	RW	0x0	FIFOWREN FIFO Write Enable When this bit is set, it enables the Write operation on selected FIFO when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. Values: 1'b0: FIFO Write is disabled 1'b1: FIFO Write is enabled
10	RW	0x0	FIFORDEN FIFO Read Enable When this bit is set, it enables the Read operation on selected FIFO when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. Values: 1'b0: FIFO Read is disabled 1'b1: FIFO Read is enabled
9	RW	0x0	RSTSEL Reset Pointers of Selected FIFO When this bit is set, the pointers of the currently-selected FIFO are reset when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. Values: 1'b0: Reset Pointers of Selected FIFO is disabled 1'b1: Reset Pointers of Selected FIFO is enabled
8	RW	0x0	RSTALL Reset All Pointers When this bit is set, the pointers of all FIFOs are reset when FIFO Debug Access is enabled. This bit must not be written to 1 when FIFO Debug Access is not enabled, that is FDBGEN bit is 0. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. Values: 1'b0: Reset All Pointers is disabled 1'b1: Reset All Pointers is enabled
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:5	RW	0x0	PKTSTATE Encoded Packet State This field is used to write the control information to the Tx FIFO or Rx FIFO. Tx FIFO: 2'b00: Packet Data 2'b01: Control Word 2'b10: SOP Data 2'b11: EOP Data Rx FIFO: 2'b00: Packet Data 2'b01: Normal Status 2'b10: Last Status 2'b11: EOP Values: 2'b00: Packet Data 2'b01: Control Word/Normal Status 2'b10: SOP Data/Last Status 2'b11: EOP Data/EOP
4	RO	0x0	reserved
3:2	RW	0x0	BYTEEN Byte Enables This field indicates the number of data bytes valid in the data register during Write operation. This is valid only when PKTSTATE is 2'b10 (EOP) and Tx FIFO or Rx FIFO is selected. Values: 2'b00: Byte 0 valid 2'b01: Byte 0 and Byte 1 are valid 2'b10: Byte 0, Byte 1, and Byte 2 are valid 2'b11: All four bytes are valid
1	RW	0x0	DBGMOD Debug Mode Access to FIFO When this bit is set, it indicates that the current access to the FIFO is read, write, and debug access. In this mode, the following access types are allowed: 1. Read and Write access to Tx FIFO, TSO FIFO, and Rx FIFO 2. Read access is allowed to Tx Status FIFO. When this bit is reset, it indicates that the current access to the FIFO is slave access bypassing the DMA. In this mode, the following access are allowed: 1. Write access to the Tx FIFO 2. Read access to the Rx FIFO and Tx Status FIFO Values: 1'b0: Debug Mode Access to FIFO is disabled 1'b1: Debug Mode Access to FIFO is enabled
0	RW	0x0	FDBGEN FIFO Debug Access Enable When this bit is set, it indicates that the debug mode access to the FIFO is enabled. When this bit is reset, it indicates that the FIFO can be accessed only through a master interface. Values: 1'b0: FIFO Debug Access is disabled 1'b1: FIFO Debug Access is enabled

GMAC_MTL_DBG_STS

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Address: Operational Base(0x21C70000) + offset (0x0C0C)

Bit	Attr	Reset Value	Description
31:15	RO	0x00400	LOCR Remaining Locations in the FIFO Slave Access Mode: This field indicates the space available in selected FIFO. Debug Access Mode: This field contains the Write or Read pointer value of the selected FIFO during Write or Read operation, respectively. Reset: In single Tx Queue configurations, (DWC_EQOS_TXFIFO_SIZE/(DWC_EQOS_DATAWIDTH/8)), Otherwise 0000H.
14:10	RO	0x00	reserved
9	RW	0x0	STSI Transmit Status Available Interrupt Status When set, this bit indicates that the Slave mode Tx packet is transmitted, and the status is available in Tx Status FIFO. This bit is reset when 1 is written to this bit. Values: 1'b0: Transmit Status Available Interrupt Status not detected 1'b1: Transmit Status Available Interrupt Status detected
8	RW	0x0	PKTI Receive Packet Available Interrupt Status When set, this bit indicates that MAC layer has written the EOP of received packet to the Rx FIFO. This bit is reset when 1 is written to this bit. Values: 1'b0: Receive Packet Available Interrupt Status not detected 1'b1: Receive Packet Available Interrupt Status detected
7:5	RO	0x0	reserved
4:3	RO	0x0	BYTEEN Byte Enables This field indicates the number of data bytes valid in the data register during Read operation. This is valid only when PKTSTATE is 2'b10 (EOP) and Tx FIFO or Rx FIFO is selected. Values: 2'b00: Byte 0 valid 2'b01: Byte 0 and Byte 1 are valid 2'b10: Byte 0, Byte 1, and Byte 2 are valid 2'b11: All four bytes are valid

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Bit	Attr	Reset Value	Description
2:1	RO	0x0	PKTSTATE Encoded Packet State This field is used to get the control or status information of the selected FIFO. Tx FIFO: 2'b00: Packet Data 2'b01: Control Word 2'b10: SOP Data 2'b11: EOP Data Rx FIFO: 2'b00: Packet Data 2'b01: Normal Status 2'b10: Last Status 2'b11: EOP This field is applicable only for Tx FIFO and Rx FIFO during Read operation. Values: 2'b00: Packet Data 2'b01: Control Word/Normal Status 2'b10: SOP Data/Last Status 2'b11: EOP Data/EOP
0	RO	0x0	FIFOBUSY FIFO Busy When set, this bit indicates that a FIFO operation is in progress in the MAC and content of the following fields is not valid: 1. All other fields of this register 2. All fields of the MTL_FIFO_Debug_Data register Values: 1'b0: FIFO Busy not detected 1'b1: FIFO Busy detected

GMAC_MTL_FIFO_DEBUG_DATA

Address: Operational Base(0x21C70000) + offset (0x0C10)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	FDBGDATA FIFO Debug Data During debug or slave access write operation, this field contains the data to be written to the Tx FIFO, Rx FIFO, or TSO FIFO. During debug or slave access read operation, this field contains the data read from the Tx FIFO, Rx FIFO, TSO FIFO, or Tx Status FIFO.

GMAC_MTL_INTERRUPT_STATUS

Address: Operational Base(0x21C70000) + offset (0x0C20)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
17	RO	0x0	DBGIS Debug Interrupt status This bit indicates an interrupt event during the slave access. To reset this bit, the application must read the FIFO Debug Access Status register to get the exact cause of the interrupt and clear its source. Values: 1'b0: Debug Interrupt status not detected 1'b1: Debug Interrupt status detected
16:1	RO	0x0000	reserved
0	RO	0x0	Q0IS Queue 0 Interrupt status This bit indicates that there is an interrupt from Queue 0. To reset this bit, the application must read Queue 0 Interrupt Control and Status register to get the exact cause of the interrupt and clear its source. Values: 1'b0: Queue 0 Interrupt status not detected 1'b1: Queue 0 Interrupt status detected

GMAC_MTL_TXQ0_OPERATION_MODE

Address: Operational Base(0x21C70000) + offset (0x0D00)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:4	RW	0x0	TTC Transmit Threshold Control These bits control the threshold level of the MTL Tx Queue. The transmission starts when the packet size within the MTL Tx Queue is larger than the threshold. In addition, full packets with length less than the threshold are also transmitted. These bits are used only when the TSF bit is reset. Values: 3'b000: 32 bytes 3'b001: 64 bytes 3'b010: 96 bytes 3'b011: 128 bytes 3'b100: 192 bytes 3'b101: 256 bytes 3'b110: 384 bytes 3'b111: 512 bytes
3:2	RO	0x0	reserved
1	RW	0x0	TSF Transmit Store and Forward When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped. Values: 1'b0: Transmit Store and Forward is disabled 1'b1: Transmit Store and Forward is enabled

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Bit	Attr	Reset Value	Description
0	RW	0x0	FTQ Flush Transmit Queue When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. This bit is internally reset when the flushing operation is complete. Until this bit is reset, you should not write to the MTL_TxQ1_Operation_Mode register. The data which is already accepted by the MAC transmitter is not flushed. It is scheduled for transmission and results in underflow and runt packet transmission. Note: The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (clk_tx_i) should be active. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Flush Transmit Queue is disabled 1'b1: Flush Transmit Queue is enabled

GMAC_MTL_TXQ0_UNDERFLOW

Address: Operational Base(0x21C70000) + offset (0x0D04)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RO	0x0	UFCNTOVF Overflow Bit for Underflow Packet Counter This bit is set every time the Tx queue Underflow Packet Counter field overflows, that is, it has crossed the maximum count. In such a scenario, the overflow packet counter is reset to all-zeros and this bit indicates that the rollover happened. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: Overflow not detected for Underflow Packet Counter 1'b1: Overflow detected for Underflow Packet Counter
10:0	RO	0x000	UFFRMCNT Underflow Packet Counter This field indicates the number of packets aborted by the controller because of Tx Queue Underflow. This counter is incremented each time the MAC aborts outgoing packet because of underflow. The counter is cleared when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

GMAC_MTL_TXQ0_DEBUG

Address: Operational Base(0x21C70000) + offset (0x0D08)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
22:20	RO	0x0	STXSTSF Number of Status Words in Tx Status FIFO of Queue This field indicates the current number of status in the Tx Status FIFO of this queue.When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of status words in Tx Status FIFO.
19	RO	0x0	reserved
18:16	RO	0x0	PTXQ Number of Packets in the Transmit Queue This field indicates the current number of packets in the Tx Queue. When the DTXSTS bit of MTL_Operation_Mode register is set to 1, this field does not reflect the number of packets in the Transmit queue.
15:6	RO	0x000	reserved
5	RO	0x0	TXSTSFSTS MTL Tx Status FIFO Full Status When high, this bit indicates that the MTL Tx Status FIFO is full. Therefore, the MTL cannot accept any more packets for transmission. Values: 1'b0: MTL Tx Status FIFO Full status is not detected 1'b1: MTL Tx Status FIFO Full status is detected
4	RO	0x0	TXQSTS MTL Tx Queue Not Empty Status When this bit is high, it indicates that the MTL Tx Queue is not empty and some data is left for transmission. Values: 1'b0: MTL Tx Queue Not Empty status is not detected 1'b1: MTL Tx Queue Not Empty status is detected
3	RO	0x0	TWCSTS MTL Tx Queue Write Controller Status When high, this bit indicates that the MTL Tx Queue Write Controller is active, and it is transferring the data to the Tx Queue. Values: 1'b0: MTL Tx Queue Write Controller status is not detected 1'b1: MTL Tx Queue Write Controller status is detected
2:1	RO	0x0	TRCSTS MTL Tx Queue Read Controller Status This field indicates the state of the Tx Queue Read Controller: Values: 2'b00: Idle state 2'b01: Read state (transferring data to the MAC transmitter) 2'b10: Waiting for pending Tx Status from the MAC transmitter 2'b11: Flushing the Tx queue because of the Packet Abort request from the MAC

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Bit	Attr	Reset Value	Description
0	RO	0x0	TXQPAUSED Transmit Queue in Pause When this bit is high and the Rx flow control is enabled, it indicates that the Tx Queue is in the Pause condition (in the full-duplex only mode) because of the following: 1. Reception of the PFC packet for the priorities assigned to the Tx Queue when PFC is enabled 2. Reception of 802.3x Pause packet when PFC is disabled Values: 1'b0: Transmit Queue in Pause status is not detected 1'b1: Transmit Queue in Pause status is detected

GMAC_MTL_Q0_INTERRUPT_CTRL_STATUS

Address: Operational Base(0x21C70000) + offset (0x0D2C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	RXOIE Receive Queue Overflow Interrupt Enable When this bit is set, the Receive Queue Overflow interrupt is enabled. When this bit is reset, the Receive Queue Overflow interrupt is disabled. Values: 1'b0: Receive Queue Overflow Interrupt is disabled 1'b1: Receive Queue Overflow Interrupt is enabled
23:17	RO	0x00	reserved
16	RW	0x0	RXOVFIS Receive Queue Overflow Interrupt Status This bit indicates that the Receive Queue had an overflow while receiving the packet. If a partial packet is transferred to the application, the overflow status is set in RDES3[21]. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. Values: 1'b0: Receive Queue Overflow Interrupt Status not detected 1'b1: Receive Queue Overflow Interrupt Status detected
15:9	RO	0x00	reserved
8	RW	0x0	TXUIE Transmit Queue Underflow Interrupt Enable When this bit is set, the Transmit Queue Underflow interrupt is enabled. When this bit is reset, the Transmit Queue Underflow interrupt is disabled. Values: 1'b0: Transmit Queue Underflow Interrupt Status is disabled 1'b1: Transmit Queue Underflow Interrupt Status is enabled
7:1	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	TXUNFIS Transmit Queue Underflow Interrupt Status This bit indicates that the Transmit Queue had an underflow while transmitting the packet. Transmission is suspended and an Underflow Error TDES3[2] is set. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. Values: 1'b0: Transmit Queue Underflow Interrupt Status not detected 1'b1: Transmit Queue Underflow Interrupt Status detected

GMAC_MTL_RXQ0_OPERATION_MODE

Address: Operational Base(0x21C70000) + offset (0x0D30)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:14	RW	0x0	RFD Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) These bits control the threshold (fill-level of Rx queue) at which the flow control is de-asserted after activation: 0: Full minus 1 KB, that is, FULL 1 KB 1: Full minus 1.5 KB, that is, FULL 1.5 KB 2: Full minus 2 KB, that is, FULL 2 KB 3: Full minus 2.5 KB, that is, FULL 2.5 KB ... 62: Full minus 32 KB, that is, FULL 32 KB 63: Full minus 32.5 KB, that is, FULL 32.5 KB The de-assertion is effective only after flow control is asserted. Note: The value must be programmed in such a way to make sure that the threshold is a positive number. When the EHFC is set high, these values are applicable only when the Rx queue size determined by the RQS field of this register, is equal to or greater than 4 KB. For a given queue size, the values ranges between 0 and the encoding for FULL minus (QSIZE - 0.5 KB) and all other values are illegal. Here the term FULL and QSIZE refers to the queue size determined by the RQS field of this register. The width of this field depends on RX FIFO size selected during the configuration. Remaining bits are reserved and read only.
13:12	RO	0x0	reserved
11:8	RW	0x0	RFA Threshold for Activating Flow Control (in half-duplex and full-duplex) These bits control the threshold (fill-level of Rx queue) at which the flow control is activated:For more information on encoding for this field, see RFD.

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Bit	Attr	Reset Value	Description
7	RW	0x0	EHFC Enable Hardware Flow Control When this bit is set, the flow control signal operation, based on the fill-level of Rx queue, is enabled. When reset, the flow control operation is disabled. Values: 1'b0: Hardware Flow Control is disabled 1'b1: Hardware Flow Control is enabled
6	RW	0x0	DIS_TCP_EF Disable Dropping of TCP/IP Checksum Error Packets When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC. When this bit is reset, all error packets are dropped if the FEP bit is reset. Values: 1'b0: Dropping of TCP/IP Checksum Error Packets is enabled 1'b1: Dropping of TCP/IP Checksum Error Packets is disabled
5	RW	0x0	RSF Receive Queue Store and Forward When this bit is set, the DWC_ether_qos reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. When this bit is reset, the Rx queue operates in the Threshold (cut-through) mode, subject to the threshold specified by the RTC field of this register. Values: 1'b0: Receive Queue Store and Forward is disabled 1'b1: Receive Queue Store and Forward is enabled
4	RW	0x0	FEP Forward Error Packets When this bit is reset, the Rx queue drops packets with error status (CRC error, GMII_ER, watchdog timeout, or overflow). However, if the start byte (write) pointer of a packet is already transferred to the read controller side (in Threshold mode), the packet is not dropped. When this bit is set, all packets except the runt error packets are forwarded to the application or DMA. If the RSF bit is set and the Rx queue overflows when a partial packet is written, the packet is dropped irrespective of the setting of this bit. However, if the RSF bit is reset and the Rx queue overflows when a partial packet is written, a partial packet may be forwarded to the application or DMA. Values: 1'b0: Forward Error Packets is disabled 1'b1: Forward Error Packets is enabled

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Bit	Attr	Reset Value	Description
3	RW	0x0	FUP Forward Undersized Good Packets When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. When this bit is reset, the Rx queue drops all packets of less than 64 bytes, unless a packet is already transferred because of the lower value of Rx Threshold, for example, RTC = 01. Values: 1'b0: Forward Undersized Good Packets is disabled 1'b1: Forward Undersized Good Packets is enabled
2	RO	0x0	reserved
1:0	RW	0x0	RTC Receive Queue Threshold Control These bits control the threshold level of the MTL Rx queue (in bytes): The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred. This field is valid only when the RSF bit is zero. This field is ignored when the RSF bit is set to 1.

GMAC_MTL_RXQ0_MISS_PKT_OVF_CNT

Address: Operational Base(0x21C70000) + offset (0x0D34)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RO	0x0	MISCNTOVF Missed Packet Counter Overflow Bit When set, this bit indicates that the Rx Queue Missed Packet Counter crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: Missed Packet Counter overflow not detected 1'b1: Missed Packet Counter overflow detected
26:16	RO	0x000	MISPKTCNT Missed Packet Counter This field indicates the number of packets missed by the DWC_ether_qos because the application asserted ari_pkt_flush_i[] for this queue. This counter is incremented each time the application issues ari_pkt_flush_i[] for this queue. This counter is reset when this register is read with mci_be_i[0] at 1b1. In EQOS-DMA, EQOS-AXI, and EQOS-AHB configurations, This counter is incremented by 1 when the DMA discards the packet because of buffer unavailability. Access restriction applies. Clears on read. Self-set to 1 on internal event.
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11	RO	0x0	OVFCNTOVF Overflow Counter Overflow Bit When set, this bit indicates that the Rx Queue Overflow Packet Counter field crossed the maximum limit. Access restriction applies. Clears on read. Self-set to 1 on internal event. Values: 1'b0: Overflow Counter overflow not detected 1'b1: Overflow Counter overflow detected
10:0	RO	0x000	OVFPKTCNT Overflow Packet Counter This field indicates the number of packets discarded by the DWC_ether_qos because of Receive queue overflow. This counter is incremented each time the DWC_ether_qos discards an incoming packet because of overflow. This counter is reset when this register is read with mci_be_i[0] at 1'b1. Access restriction applies. Clears on read. Self-set to 1 on internal event.

GMAC_MTL_RXQ0_DEBUG

Address: Operational Base(0x21C70000) + offset (0x0D38)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RO	0x0	PRXQ Number of Packets in Receive Queue This field indicates the current number of packets in the Rx Queue. The theoretical maximum value for this field is 256KB/16B = 16K Packets, that is, Max_Queue_Size/Min_Packet_Size.
15:6	RO	0x000	reserved
5:4	RO	0x0	RXQSTS MTL Rx Queue Fill-Level Status This field gives the status of the fill-level of the Rx Queue: Values: 2'b00: Rx Queue empty 2'b01: Rx Queue fill-level below flow-control deactivate threshold 2'b10: Rx Queue fill-level above flow-control activate threshold 2'b11: Rx Queue full
3	RO	0x0	reserved
2:1	RO	0x0	RRCSTS MTL Rx Queue Read Controller State This field gives the state of the Rx queue Read controller: Values: 2'b00: Idle state 2'b01: Reading packet data 2'b10: Reading packet status (or timestamp) 2'b11: Flushing the packet data and status

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Bit	Attr	Reset Value	Description
0	RO	0x0	RWCSTS MTL Rx Queue Write Controller Active Status When high, this bit indicates that the MTL Rx queue Write controller is active, and it is transferring a received packet to the Rx Queue. Values: 1'b0: MTL Rx Queue Write Controller Active Status not detected 1'b1: MTL Rx Queue Write Controller Active Status detected

GMAC_DMA_MODE

Address: Operational Base(0x21C70000) + offset (0x1000)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	INTM Interrupt Mode This field defines the interrupt mode of DWC_ether_qos. The behavior of the following outputs changes depending on the following settings: 1. sbd_perch_tx_intr_o[] (Transmit Per Channel Interrupt) 2. sbd_perch_rx_intr_o[] (Receive Per Channel Interrupt) 3. sbd_intr_o (Common Interrupt) It also changes the behavior of the RI/TI bits in the DMA_CH0_Status. 2'b00: sbd_perch_* are pulse signals for each TX/RX packet transfer completion events (irrespective of whether corresponding interrupts are enabled) for which IOC bits are enabled in descriptor. sbd_intr_o is also asserted when corresponding interrupts are enabled and cleared only when software clears the corresponding RI/TI status bits. 2'b01: sbd_perch_* are level signals asserted on TX/RX packet transfer completion event when corresponding interrupts are enabled and de-asserted when the software clears the corresponding RI/TI status bits. The sbd_intr_o is not asserted for these TX/RX packet transfer completion events. 2'b10: sbd_perch_* are level signals asserted on TX/RX packet transfer completion event when corresponding interrupts are enabled and de-asserted when the software clears the corresponding RI/TI status bits. However, the signal is asserted again if the same event occurred again before it was cleared. The sbd_intr_o is not asserted for these TX/RX packet transfer completion events. 2'b11: Reserved Values: 2'b00: See above description 2'b01: See above description 2'b10: See above description 2'b11: Reserved
15:9	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
8	RW	0x0	DSPW Descriptor Posted Write When this bit is set to 0, the descriptor writes are always non-posted. When this bit is set to 1, the descriptor writes are non-posted only when IOC (Interrupt on completion) is set in last descriptor, otherwise the descriptor writes are always posted. Values: 1'b0: Descriptor Posted Write is disabled 1'b1: Descriptor Posted Write is enabled
7:1	RO	0x00	reserved
0	RW	0x0	SWR Software Reset When this bit is set, the MAC and the DMA controller reset the logic and all internal registers of the DMA, MTL, and MAC. This bit is automatically cleared after the reset operation is complete in all DWC_ether_qos clock domains. Before reprogramming any DWC_ether_qos register, a value of zero should be read in this bit. This bit must be read at least 4 CSR clock cycles after it is written to 1. Note: The reset operation is complete only when all resets in all active clock domains are de-asserted. Therefore, it is essential that all PHY inputs clocks (applicable for the selected PHY interface) are present for software reset completion. The time to complete the software reset operation depends on the frequency of the slowest active clock. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. Values: 1'b0: Software Reset is disabled 1'b1: Software Reset is enabled

GMAC_DMA_SYSBUS_MODE

Address: Operational Base(0x21C70000) + offset (0x1004)

Bit	Attr	Reset Value	Description
31	RW	0x0	EN_LPI Enable Low Power Interface (LPI) When set to 1, this bit enables the LPI mode supported by the EQOS-AXI configuration and accepts the LPI request from the AXI System Clock controller. When set to 0, this bit disables the LPI mode and always denies the LPI request from the AXI System Clock controller. Values: 1'b0: Low Power Interface (LPI) is disabled 1'b1: Low Power Interface (LPI) is enabled

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Bit	Attr	Reset Value	Description
30	RW	0x0	LPI_XIT_PKT Unlock on Magic Packet or Remote Wake-Up Packet When set to 1, this bit enables the AXI master to come out of the LPI mode only when the magic packet or remote wake-up packet is received. When set to 0, this bit enables the AXI master to come out of the LPI mode when any packet is received. Values: 1'b0: Unlock on Magic Packet or Remote Wake-Up Packet is disabled 1'b1: Unlock on Magic Packet or Remote Wake-Up Packet is enabled
29:26	RO	0x0	reserved
25:24	RW	0x0	WR_OSR_LMT AXI Maximum Write Outstanding Request Limit This value limits the maximum outstanding request on the AXI write interface. Maximum outstanding requests = WR_OSR_LMT + 1 Note: 1. Bit 26 is reserved if DWC_ETHER_QOS_AXI_MAX-_WR_REQ = 4 2. Bit 27 is reserved if DWC_ETHER_QOS_AXI_MAX-_WR_REQ!= 16
23:19	RO	0x00	reserved
18:16	RW	0x1	RD_OSR_LMT AXI Maximum Read Outstanding Request Limit This value limits the maximum outstanding request on the AXI read interface. Maximum outstanding requests = RD_OSR_LMT + 1 Note: 1. Bit 18 is reserved if parameter DWC_ETHER_QOS_AXI_-MAX_RD_REQ = 4 2. Bit 19 is reserved if parameter DWC_ETHER_QOS_AXI_-MAX_RD_REQ!= 16
15:13	RO	0x0	reserved
12	RW	0x0	AAL Address-Aligned Beats When this bit is set to 1, the EQOS-AXI or EQOS-AHB master performs address-aligned burst transfers on Read and Write channels. Values: 1'b0: Address-Aligned Beats is disabled 1'b1: Address-Aligned Beats is enabled
11	RW	0x0	EAME Enhanced Address Mode Enable. When this bit is set to 1, the DMA master enables the enhanced address mode (40-bit or 48-bit addressing mode). In this mode, the DMA engine uses either the 40- or 48-bit address, depending on the configuration. Values: 0x0 (DISABLE): Enhanced Address Mode is disabled 0x1 (ENABLE): Enhanced Address Mode is enabled

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Bit	Attr	Reset Value	Description
10	RW	0x0	AALE Automatic AXI LPI enable When set to 1, enables the AXI master to enter into LPI state when there is no activity in the DWC_ether_qos for number of system clock cycles programmed in the LPIEI field of AXI_LPI_Entry_Interval register. Values: 1'b0: Automatic AXI LPI is disabled 1'b1: Automatic AXI LPI is enabled
9:4	RO	0x00	reserved
3	RW	0x0	BLEN16 AXI Burst Length 16 When this bit is set to 1 or the FB bit is set to 0, the EQOS-AXI master can select a burst length of 16 on the AXI interface. When the FB bit is set to 0, setting this bit has no effect. Values: 1'b0: No effect 1'b1: AXI Burst Length 16
2	RW	0x0	BLEN8 AXI Burst Length 8 When this bit is set to 1 or the FB bit is set to 0, the EQOS-AXI master can select a burst length of 8 on the AXI interface. When the FB bit is set to 0, setting this bit has no effect. Values: 1'b0: No effect 1'b1: AXI Burst Length 8
1	RW	0x0	BLEN4 AXI Burst Length 4 When this bit is set to 1 or the FB bit is set to 0, the EQOS-AXI master can select a burst length of 4 on the AXI interface. When the FB bit is set to 0, setting this bit has no effect. Values: 1'b0: No effect 1'b1: AXI Burst Length 4
0	RW	0x0	FB Fixed Burst Length When this bit is set to 1, the EQOS-AXI master initiates burst transfers of specified lengths as given below. 1. Burst transfers of fixed burst lengths as indicated by the BLEN256, BLEN128, BLEN64, BLEN32, BLEN16, BLEN8, or BLEN4 field 2. Burst transfers of length 1 When this bit is set to 0, the EQOS-AXI master initiates burst transfers that are equal to or less than the maximum allowed burst length programmed in Bits[7:1]. Values: 1'b0: Fixed Burst Length is disabled 1'b1: Fixed Burst Length is enabled

GMAC_DMA_INTERRUPT_STATUS

Address: Operational Base(0x21C70000) + offset (0x1008)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
17	RO	0x0	MACIS MAC Interrupt Status This bit indicates an interrupt event in the MAC. To reset this bit to 1'b0, the software must read the corresponding register in the MAC to get the exact cause of the interrupt and clear its source. Values: 1'b0: MAC Interrupt Status not detected 1'b1: MAC Interrupt Status detected
16	RO	0x0	MTLIS MTL Interrupt Status This bit indicates an interrupt event in the MTL. To reset this bit to 1'b0, the software must read the corresponding register in the MTL to get the exact cause of the interrupt and clear its source. Values: 1'b0: MTL Interrupt Status not detected 1'b1: MTL Interrupt Status detected
15:1	RO	0x0000	reserved
0	RO	0x0	DC0IS DMA Channel 0 Interrupt Status This bit indicates an interrupt event in DMA Channel 0. To reset this bit to 1'b0, the software must read the corresponding register in DMA Channel 0 to get the exact cause of the interrupt and clear its source. Values: 1'b0: DMA Channel 0 Interrupt Status not detected 1'b1: DMA Channel 0 Interrupt Status detected

GMAC_DMA_DEBUG_STATUS0

Address: Operational Base(0x21C70000) + offset (0x100C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RO	0x0	TPS0 DMA Channel 0 Transmit Process State This field indicates the Tx DMA FSM state for Channel 0. The MSB of this field always returns 0. This field does not generate an interrupt. Values: 4'b0000: Stopped (Reset or Stop Transmit Command issued) 4'b0001: Running (Fetching Tx Transfer Descriptor) 4'b0010: Running (Waiting for status) 4'b0011: Running (Reading Data from system memory buffer and queuing it to the Tx buffer (Tx FIFO)) 4'b0100: Timestamp write state 4'b0101: Reserved for future use 4'b0110: Suspended (Tx Descriptor Unavailable or Tx Buffer Underflow) 4'b0111: Running (Closing Tx Descriptor)

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Bit	Attr	Reset Value	Description
11:8	RO	0x0	RPS0 DMA Channel 0 Receive Process State This field indicates the Rx DMA FSM state for Channel 0. The MSB of this field always returns 0. This field does not generate an interrupt. Values: 4'b0000: Stopped (Reset or Stop Receive Command issued) 4'b0001: Running (Fetching Rx Transfer Descriptor) 4'b0010: Reserved for future use 4'b0011: Running (Waiting for Rx packet) 4'b0100: Suspended (Rx Descriptor Unavailable) 4'b0101: Running (Closing the Rx Descriptor) 4'b0110: Timestamp write state 4'b0111: Running (Transferring the received packet data from the Rx buffer to the system memory)
7:2	RO	0x00	reserved
1	RO	0x0	AXRHSTS AXI Master Read Channel Status When high, this bit indicates that the read channel of the AXI master is active, and it is transferring the data. Values: 1'b0: AXI Master Read Channel Status not detected 1'b1: AXI Master Read Channel Status detected
0	RO	0x0	AXWHSTS AXI Master Write Channel or AHB Master Status EQOS-AXI Configuration: When high, this bit indicates that the write channel of the AXI master is active, and it is transferring data. EQOS-AHB Configuration: When high, this bit indicates that the AHB master FSMs are in the non-idle state. Values: 1'b0: AXI Master Write Channel or AHB Master Status not detected 1'b1: AXI Master Write Channel or AHB Master Status detected

GMAC_AXI_LPI_ENTRY_INTERVAL

Address: Operational Base(0x21C70000) + offset (0x1040)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	LPIEI LPI Entry Interval Contains the number of system clock cycles, multiplied by 64, to wait for an activity in the DWC_ether_qos to enter into the AXI low power state. 0 indicates 64 clock cycles.

GMAC_DMA_CH0_CONTROL

Address: Operational Base(0x21C70000) + offset (0x1100)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
24	RW	0x0	SPH Split Headers When this bit is set, the DMA splits the header and payload in the Receive path. The DMA writes the header to the Buffer Address1 of RDES0. The DMA writes the payload to the buffer to which the Buffer Address2 is pointing. The software must ensure that the header fits into the Receive buffers. If the header length exceeds the receive buffer size, the DMA does not split the header and payload. This bit is available only if Enable Split Header Structure option is selected. Values: 0x0 (DISABLE): Split Headers feature is disabled 0x1 (ENABLE): Split Headers feature is enabled
23:21	RO	0x0	reserved
20:18	RW	0x0	DSL Descriptor Skip Length This bit specifies the Word, Dword, or Lword number (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor. When the DSL value is equal to zero, the DMA takes the descriptor table as contiguous.
17	RO	0x0	reserved
16	RW	0x0	PBLx8 8xPBL mode When this bit is set, the PBL value programmed in Bits[21:16] in DMA_CH0_Tx_Control and Bits[21:16] in DMA_CH0_Rx_Control is multiplied by eight times. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value. 0x0 (DISABLE): 8xPBL mode is disabled 0x1 (ENABLE): 8xPBL mode is enabled
15:14	RO	0x0	reserved
13:0	RW	0x0000	MSS Maximum Segment Size This field specifies the maximum segment size that should be used while segmenting the packet. This field is valid only if the TSE bit of DMA_CH0_Tx_Control register is set. The value programmed in this field must be more than the configured Datawidth in bytes. It is recommended to use a MSS value of 64 bytes or more.

GMAC_DMA_CH0_TX_CONTROL

Address: Operational Base(0x21C70000) + offset (0x1104)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
21:16	RW	0x00	TxPBL Transmit Programmable Burst Length These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in DMA_CH0_Control register. 2. Set the TxPBL. Note: The maximum value of TxPBL must be less than or equal to half the Tx Queue size (TQS field of MTL_TxQ[n]_Operation_Mode register) in terms of beats. This is required so that the Tx Queue has space to store at least another Tx PBL worth of data while the MTL Tx Queue Controller is transferring data to MAC. For example, in 64-bit data width configurations the total locations in Tx Queue of size 512 bytes is 64, TxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	RW	0x0	IPBL Ignore PBL Requirement When this bit is set, the DMA does not check for PBL number of locations in the MTL before initiating a transfer. If space is not available, the MTL may use handshaking to slow the DMA. Note: This bit/mode must not be used when multiple Transmit DMA Channels are enabled as it may block other Transmit and Receive DMA Channels from accessing the Read Data Channel of AXI bus until space is available in Transmit Queue for current transfer. 0x0 (DISABLE): Ignore PBL Requirement is disabled 0x1 (ENABLE): Ignore PBL Requirement is enabled
14:13	RW	0x0	TSE_MODE TSE Mode 00: TSO/USO (segmentation functionality is enabled). In this mode, the setting of TSE bit enables the TSO/USO segmentation. 01: UFO with Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality with Checksum for all the UDP packets. 10: UFO without Checksum (UDP Fragmentation over IPv4 with Checksum). In this mode, the setting of TSE bit enables the UDP fragmentation functionality without Checksum for all the UDP packets. 11: Reserved 0x0 (TSO_USO): TSO/USO 0x1 (UFOWC): UFO with Checksum 0x2 (UFOWOC): UFO without Checksum 0x3 (RSVD): Reserved

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Bit	Attr	Reset Value	Description
12	RW	0x0	TSE TCP Segmentation Enabled When this bit is set, the DMA performs the TCP segmentation or UDP Segmentation/Fragmentation for packets in this channel. The TCP segmentation or UDP packet's segmentation/Fragmentation is done only for those packets for which the TSE bit (TDES0[19]) is set in the Tx Normal descriptor.When this bit is set, the TxPBL value must be greater than 4. 0x0 (DISABLE): TCP Segmentation is disabled 0x1 (ENABLE): TCP Segmentation is enabled
11:5	RO	0x00	reserved
4	RW	0x0	OSF Operate on Second Packet When this bit is set, it instructs the DMA to process the second packet of the Transmit data even before the status for the first packet is obtained. 0x0 (DISABLE): Operate on Second Packet disabled 0x1 (ENABLE): Operate on Second Packet enabled
3:1	RO	0x0	reserved
0	RW	0x0	ST Start or Stop Transmission Command When this bit is set, transmission is placed in the Running state. The DMA checks the Transmit list at the current position for a packet to be transmitted. The DMA tries to acquire descriptor from either of the following positions: 1.The current position in the list This is the base address of the Transmit list set by the DMA_CH0_TxDesc_List_Address register. 2.The position at which the transmission was previously stopped If the DMA does not own the current descriptor, the transmission enters the Suspended state and the TBU bit of the DMA_CH0_Status register is set. The Start Transmission command is effective only when the transmission is stopped. If the command is issued before setting the DMA_CH0_TxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current packet. The Next Descriptor position in the Transmit list is saved, and it becomes the current position when the transmission is restarted. To change the list address, you need to program DMA_CH0_TxDesc_List_Address register with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current packet is complete or the transmission is in the Suspended state. 0x0 (STOP): Stop Transmission Command 0x1 (START): Start Transmission Command

GMAC_DMA_CH0_RX_CONTROL

Address: Operational Base(0x21C70000) + offset (0x1108)

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Bit	Attr	Reset Value	Description
31	RW	0x0	RPF Rx Packet Flush When this bit is set to 1, then DWC_ether_qos automatically flushes the packet from the Rx Queues destined to this DMA Rx Channel, when it is stopped. When this bit remains set and the DMA is re-started by the software driver, the packets residing in the Rx Queues that were received when this RxDMA was stopped, get flushed out. The packets that are received by the MAC after the RxDMA is re-started are routed to the RxDMA. The flushing happens on the Read side of the Rx Queue. When this bit is set to 0, the DWC_ether_qos not flush the packet in the Rx Queue destined to this RxDMA Channel when it is STOP state. This may in turn cause head-of-line blocking in the corresponding RxQueue. 0x0 (DISABLE): Rx Packet Flush is disabled 0x1 (ENABLE): Rx Packet Flush is enabled
30:22	RO	0x000	reserved
21:16	RW	0x00	RxPBL Receive Programmable Burst Length These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following values: 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. To transfer more than 32 beats, perform the following steps: 1. Set the 8xPBL mode in the DMA_CH0_Control register. 2. Set the RxPBL. Note: The maximum value of RxPBL must be less than or equal to half the Rx Queue size (RQS field of MTL_RxQ[n]_Operation_Mode register) in terms of beats. This is required so that the Rx Queue has space to store at least another Rx PBL worth of data while the Rx DMA is transferring a block of data. For example, in 64-bit data width configurations the total locations in Rx Queue of size 512 bytes is 64, so RxPBL and 8xPBL needs to be programmed to less than or equal to 32.
15	RO	0x0	reserved
14:4	RW	0x000	RBSZ_13_y Receive Buffer size High RBSZ[13:0] is split into two fields higher RBSZ_13_y and lower RBSZ_3_0. The RBSZ[13:0] field indicates the size of the Rx buffers specified in bytes. The maximum buffer size is limited to 16K bytes. The buffer size is applicable to payload buffers when split headers are enabled. Note: The buffer size must be a multiple of 4, 8, or 16 depending on the data bus widths (32-bit, 64-bit, or 128-bit respectively). This is required even if the value of buffer address pointer is not aligned to data bus width. Hence the lower RBSZ_3_0 bits are read-only and the value is considered as all-zero. Thus the RBSZ_13_y indicates the buffer size in terms of locations (with the width same as bus-width).

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Bit	Attr	Reset Value	Description
3:1	RO	0x0	RBSZ_3_0 Receive Buffer size Low RBSZ[13:0] is split into two fields RBSZ_13_y and RBSZ_3_0. The RBSZ_3_0 is the lower field whose width is based on data bus width of the configuration. This field is of width 2, 3, or 4 bits for 32-bit, 64-bit, or 128-bit data bus width respectively. This field is read-only (RO)
0	RW	0x0	SR Start or Stop Receive When this bit is set, the DMA tries to acquire the descriptor from the Receive list and processes the incoming packets.The DMA tries to acquire descriptor from either of the following positions: 1.The current position in the list This is the address set by the DMA_CH0_RxDesc_List_Address register. 2.The position at which the Rx process was previously stopped If the DMA does not own the current descriptor, the reception is suspended and the RBU bit of the DMA_CH0_Status register is set. The Start Receive command is effective only when the reception is stopped. If the command is issued before setting the DMA_CH0_RxDesc_List_Address register, the DMA behavior is unpredictable. When this bit is reset, the Rx DMA operation is stopped after the transfer of the current packet. The next descriptor position in the Receive list is saved, and it becomes the current position after the Rx process is restarted. The Stop Receive command is effective only when the Rx process is in the Running (waiting for Rx packet) or Suspended state. 0x0 (STOP): Stop Receive 0x1 (START): Start Receive

GMAC_DMA_CH0_TXDESC_LIST_HADDRESS

Address: Operational Base(0x21C70000) + offset (0x1110)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	TDESHA Start of Transmit List This field contains the most-significant 8 or 16 bits of the 40- or 48-bit base address of the first descriptor in the Transmit descriptor list.

GMAC_DMA_CH0_TXDESC_LIST_ADDRESS

Address: Operational Base(0x21C70000) + offset (0x1114)

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Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	TDESLA Start of Transmit List This field contains the base address of the first descriptor in the Transmit descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: 31:2 for 32-bit configuration 31:3 for 64-bit configuration 31:4 for 128-bit configuration
2:0	RO	0x0	reserved

GMAC_DMA_CH0_RXDESC_LIST_HAADDRESS

Address: Operational Base(0x21C70000) + offset (0x1118)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	RDESHA Start of Receive List This field contains the most-significant 8 or 16 bits of the 40-bit or 48-bit base address of the first descriptor in the Rx Descriptor list.

GMAC_DMA_CH0_RXDESC_LIST_ADDRESS

Address: Operational Base(0x21C70000) + offset (0x111C)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	RDESLA Start of Receive List This field contains the base address of the first descriptor in the Rx Descriptor list. The DMA ignores the LSB bits (1:0, 2:0, or 3:0) for 32-bit, 64-bit, or 128-bit bus width and internally takes these bits as all-zero. Therefore, these LSB bits are read-only (RO). The width of this field depends on the configuration: 31:2 for 32-bit configuration 31:3 for 64-bit configuration 31:4 for 128-bit configuration
2:0	RO	0x0	reserved

GMAC_DMA_CH0_TXDESC_TAIL_POINTER

Address: Operational Base(0x21C70000) + offset (0x1120)

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Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	TDTP Transmit Descriptor Tail Pointer This field contains the tail pointer for the Tx descriptor ring. The software writes the tail pointer to add more descriptors to the Tx channel. The hardware tries to transmit all packets referenced by the descriptors between the head and the tail pointer registers. The width of this field depends on the configuration: 31:2 for 32-bit configuration 31:3 for 64-bit configuration 31:4 for 128-bit configuration
2:0	RO	0x0	reserved

GMAC_DMA_CH0_RXDESC_TAIL_POINTER

Address: Operational Base(0x21C70000) + offset (0x1128)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	RDRT Receive Descriptor Tail Pointer This field contains the tail pointer for the Rx descriptor ring. The software writes the tail pointer to add more descriptors to the Rx channel. The hardware tries to write all received packets to the descriptors referenced between the head and the tail pointer registers. The width of this field depends on the configuration: 31:2 for 32-bit configuration 31:3 for 64-bit configuration 31:4 for 128-bit configuration
2:0	RO	0x0	reserved

GMAC_DMA_CH0_TXDESC_RING_LENGTH

Address: Operational Base(0x21C70000) + offset (0x112C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	TDRL Transmit Descriptor Ring Length This field sets the maximum number of Tx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. we recommends a minimum ring descriptor length of 4. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

GMAC_DMA_CH0_RXDESC_RING_LENGTH

Address: Operational Base(0x21C70000) + offset (0x1130)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	RDRL Receive Descriptor Ring Length This register sets the maximum number of Rx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. For example, You can program any value up to 0x3FF in this field. This field is 10 bits wide, if you program 0x3FF, you can have 1024 descriptors. If you want to have 10 descriptors, program it to a value of 0x9.

GMAC_DMA_CH0_INTERRUPT_ENABLE

Address: Operational Base(0x21C70000) + offset (0x1134)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	NIE Normal Interrupt Summary Enable When this bit is set, the normal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: Bit 0: Transmit Interrupt Bit 2: Transmit Buffer Unavailable Bit 6: Receive Interrupt Bit 11: Early Receive Interrupt When this bit is reset, the normal interrupt summary is disabled. 0x0 (DISABLE): Normal Interrupt Summary is disabled 0x1 (ENABLE): Normal Interrupt Summary is enabled
14	RW	0x0	AIE Abnormal Interrupt Summary Enable When this bit is set, the abnormal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: Bit 1: Transmit Process Stopped Bit 7: Rx Buffer Unavailable Bit 8: Receive Process Stopped Bit 9: Receive Watchdog Timeout Bit 10: Early Transmit Interrupt Bit 12: Fatal Bus Error Bit 13: Context Descriptor Error When this bit is reset, the abnormal interrupt summary is disabled. 0x0 (DISABLE): Abnormal Interrupt Summary is disabled 0x1 (ENABLE): Abnormal Interrupt Summary is enabled
13	RW	0x0	CDEE Context Descriptor Error Enable When this bit is set along with the AIE bit, the Descriptor error interrupt is enabled. When this bit is reset, the Descriptor error interrupt is disabled. 0x0 (DISABLE): Context Descriptor Error is disabled 0x1 (ENABLE): Context Descriptor Error is enabled

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Bit	Attr	Reset Value	Description
12	RW	0x0	FBEE Fatal Bus Error Enable When this bit is set along with the AIE bit, the Fatal Bus error interrupt is enabled. When this bit is reset, the Fatal Bus Error error interrupt is disabled. 0x0 (DISABLE): Fatal Bus Error is disabled 0x1 (ENABLE): Fatal Bus Error is enabled
11	RW	0x0	ERIE Early Receive Interrupt Enable When this bit is set along with the NIE bit, the Early Receive interrupt is enabled. When this bit is reset, the Early Receive interrupt is disabled. 0x0 (DISABLE): Early Receive Interrupt is disabled 0x1 (ENABLE): Early Receive Interrupt is enabled
10	RW	0x0	ETIE Early Transmit Interrupt Enable When this bit is set along with the AIE bit, the Early Transmit interrupt is enabled. When this bit is reset, the Early Transmit interrupt is disabled. 0x0 (DISABLE): Early Transmit Interrupt is disabled 0x1 (ENABLE): Early Transmit Interrupt is enabled
9	RW	0x0	RWTE Receive Watchdog Timeout Enable When this bit is set along with the AIE bit, the Receive Watchdog Timeout interrupt is enabled. When this bit is reset, the Receive Watchdog Timeout interrupt is disabled. 0x0 (DISABLE): Receive Watchdog Timeout is disabled 0x1 (ENABLE): Receive Watchdog Timeout is enabled
8	RW	0x0	RSE Receive Stopped Enable When this bit is set along with the AIE bit, the Receive Stopped Interrupt is enabled. When this bit is reset, the Receive Stopped interrupt is disabled.
7	RW	0x0	RBUE Receive Buffer Unavailable Enable When this bit is set along with the AIE bit, the Receive Buffer Unavailable interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Receive Buffer Unavailable is disabled 0x1 (ENABLE): Receive Buffer Unavailable is enabled
6	RW	0x0	RIE Receive Interrupt Enable When this bit is set along with the NIE bit, the Receive Interrupt is enabled. When this bit is reset, the Receive Interrupt is disabled. 0x0 (DISABLE): Receive Interrupt is disabled 0x1 (ENABLE): Receive Interrupt is enabled
5:3	RO	0x0	reserved
2	RW	0x0	TBUE Transmit Buffer Unavailable Enable When this bit is set along with the NIE bit, the Transmit Buffer Unavailable interrupt is enabled. When this bit is reset, the Transmit Buffer Unavailable interrupt is disabled. 0x0 (DISABLE): Transmit Buffer Unavailable is disabled 0x1 (ENABLE): Transmit Buffer Unavailable is enabled

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Bit	Attr	Reset Value	Description
1	RW	0x0	TXSE Transmit Stopped Enable When this bit is set along with the AIE bit, the Transmission Stopped interrupt is enabled. When this bit is reset, the Transmission Stopped interrupt is disabled. 0x0 (DISABLE): Transmit Stopped is disabled 0x1 (ENABLE): Transmit Stopped is enabled
0	RW	0x0	TIE Transmit Interrupt Enable When this bit is set along with the NIE bit, the Transmit Interrupt is enabled. When this bit is reset, the Transmit Interrupt is disabled. 0x0 (DISABLE): Transmit Interrupt is disabled 0x1 (ENABLE): Transmit Interrupt is enabled

GMAC_DMA_CH0_RX_INTERRUPT_WATCHDOG_TIMER

Address: Operational Base(0x21C70000) + offset (0x1138)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:16	RW	0x0	RWTU Receive Interrupt Watchdog Timer Count Units This fields indicates the number of system clock cycles corresponding to one unit in RWT field. 2'b00: 256 2'b01: 512 2'b10: 1024 2'b11: 2048 For example, when RWT=2 and RWTU=1, the watchdog timer is set for 2*512=1024 system clock cycles.
15:8	RO	0x00	reserved
7:0	RW	0x00	RWT Receive Interrupt Watchdog Timer Count This field indicates the number of system clock cycles, multiplied by factor indicated in RWTU field, for which the watchdog timer is set. The watchdog timer is triggered with the programmed value after the Rx DMA completes the transfer of a packet for which the RI bit is not set in the DMA_CH0_Status register, because of the setting of Interrupt Enable bit in the corresponding descriptor RDES3[30]. When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of automatic setting of RI as per the Interrupt Enable bit RDES3[30] of any received packet.

GMAC_DMA_CH0_CURRENT_APP_TXDESC

Address: Operational Base(0x21C70000) + offset (0x1144)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CURTDESAPTR Application Transmit Descriptor Address Pointer The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

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GMAC_DMA_CH0_CURRENT_APP_RXDESC

Address: Operational Base(0x21C70000) + offset (0x114C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CURRDESAPTR Application Receive Descriptor Address Pointer The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

GMAC_DMA_CH0_CURREN_APP_TXBUFFER_H

Address: Operational Base(0x21C70000) + offset (0x1150)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	CURTBUFAPTRH Application Transmit Buffer Address Pointer The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

GMAC_DMA_CH0_CURRENT_APP_TXBUFFER

Address: Operational Base(0x21C70000) + offset (0x1154)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CURTBUFAPTR Application Transmit Buffer Address Pointer The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

GMAC_DMA_CH0_CURRENT_APP_RXBUFFER_H

Address: Operational Base(0x21C70000) + offset (0x1158)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RO	0x00	CURRBUFAPTRH Application Receive Buffer Address Pointer The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

GMAC_DMA_CH0_CURRENT_APP_RXBUFFER

Address: Operational Base(0x21C70000) + offset (0x115C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CURRBUFAPTR Application Receive Buffer Address Pointer The DMA updates this pointer during Rx operation. This pointer is cleared on reset.

GMAC_DMA_CH0_STATUS

Address: Operational Base(0x21C70000) + offset (0x1160)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
21:19	RO	0x0	REB Rx DMA Error Bits This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. 1.Bit 21 1'b1: Error during data transfer by Rx DMA 1'b0: No Error during data transfer by Rx DMA 2.Bit 20 1'b1: Error during descriptor access 1'b0: Error during data buffer access 3.Bit 19 1'b1: Error during read transfer 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
18:16	RO	0x0	TEB Tx DMA Error Bits This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. 1.Bit 18 1'b1: Error during data transfer by Tx DMA 1'b0: No Error during data transfer by Tx DMA 2.Bit 17 1'b1: Error during descriptor access 1'b0: Error during data buffer access 3.Bit 16 1'b1: Error during read transfer 1'b0: Error during write transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.
15	RW	0x0	NIS Normal Interrupt Summary Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: Bit 0: Transmit Interrupt Bit 2: Transmit Buffer Unavailable Bit 6: Receive Interrupt Bit 11: Early Receive Interrupt Only unmasked bits (interrupts for which interrupt enable is set in DMA_CH0_Interrupt_Enable register) affect the Normal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit which causes NIS to be set is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Normal Interrupt Summary status not detected 0x1 (ACTIVE): Normal Interrupt Summary status detected

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Bit	Attr	Reset Value	Description
14	RW	0x0	AIS Abnormal Interrupt Summary Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: Bit 1: Transmit Process Stopped Bit 7: Receive Buffer Unavailable Bit 8: Receive Process Stopped Bit 10: Early Transmit Interrupt Bit 12: Fatal Bus Error Bit 13: Context Descriptor Error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Abnormal Interrupt Summary status not detected 0x1 (ACTIVE): Abnormal Interrupt Summary status
13	RW	0x0	CDE Context Descriptor Error This bit indicates that the DMA Tx/Rx engine received a descriptor error, which indicates invalid context in the middle of packet flow (intermediate descriptor) or all one's descriptor in Tx case and on Rx side it indicates DMA has read a descriptor with either of the buffer address as ones which is considered to be invalid. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Context Descriptor Error status not detected 0x1 (ACTIVE): Context Descriptor Error status detected
12	RW	0x0	FBE Fatal Bus Error This bit indicates that a bus error occurred (as described in the EB field). When this bit is set, the corresponding DMA channel engine disables all bus accesses. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Fatal Bus Error status not detected 0x1 (ACTIVE): Fatal Bus Error status detected
11	RW	0x0	ERI Early Receive Interrupt This bit when set indicates that the RxDMA has completed the transfer of packet data to the memory. In configs supporting ERIC, When ERIC=0, this bit is set only after the Rx DMA has filled up a complete receive buffer with packet data. When ERIC=1, this bit is set after every burst transfer of data from the Rx DMA to the buffer.The setting of RI bit automatically clears this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Receive Interrupt status not detected 0x1 (ACTIVE): Early Receive Interrupt status detected

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Bit	Attr	Reset Value	Description
10	RW	0x0	ETI Early Transmit Interrupt This bit when set indicates that the TxDMA has completed the transfer of packet data to the MTL TXFIFO memory. In configs supporting ERIC: When ETIC=0, this bit is set only after the Tx DMA has transferred a complete packet to MTL. When ETIC=1, this bit is set after completion of (partial) packet data transfer from buffers in the Transmit descriptor in which IOC=1. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Early Transmit Interrupt status not detected 0x1 (ACTIVE): Early Transmit Interrupt status detected
9	RO	0x0	reserved
8	RW	0x0	RPS Receive Process Stopped This bit is asserted when the Rx process enters the Stopped state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Process Stopped status not detected 0x1 (ACTIVE): Receive Process Stopped status detected
7	RW	0x0	RBU Receive Buffer Unavailable This bit indicates that the application owns the next descriptor in the Receive list, and the DMA cannot acquire it. The Rx process is suspended. To resume processing Rx descriptors, the application should change the ownership of the descriptor and issue a Receive Poll Demand command. If this command is not issued, the Rx process resumes when the next recognized incoming packet is received. In ring mode, the application should advance the Receive Descriptor Tail Pointer register of a channel. This bit is set only when the DMA owns the previous Rx descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Buffer Unavailable status not detected 0x1 (ACTIVE): Receive Buffer Unavailable status detected
6	RW	0x0	RI Receive Interrupt This bit indicates that the packet reception is complete. When packet reception is complete, Bit 31 of RDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. The reception remains in the Running state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Receive Interrupt status not detected 0x1 (ACTIVE): Receive Interrupt status detected
5:3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2	RW	0x0	TBU Transmit Buffer Unavailable This bit indicates that the application owns the next descriptor in the Transmit list, and the DMA cannot acquire it. Transmission is suspended. The TPS0 field of the DMA_Debug_Status0 register explains the Transmit Process state transitions. To resume processing the Transmit descriptors, the application should do the following: 1. Change the ownership of the descriptor by setting Bit 31 of TDES3. 2. Issue a Transmit Poll Demand command. For ring mode, the application should advance the Transmit Descriptor Tail Pointer register of a channel. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Buffer Unavailable status not detected 0x1 (ACTIVE): Transmit Buffer Unavailable status
1	RW	0x0	TPS Transmit Process Stopped This bit is set when the transmission is stopped. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Process Stopped status not detected 0x1 (ACTIVE): Transmit Process Stopped status detected
0	RW	0x0	TI Transmit Interrupt This bit indicates that the packet transmission is complete. When transmission is complete, Bit 31 of TDES3 is reset in the last descriptor, and the specific packet status information is updated in the descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0x0 (INACTIVE): Transmit Interrupt status not detected 0x1 (ACTIVE): Transmit Interrupt status detected

GMAC_DMA_CH0_MISS_FRAME_CNT

Address: Operational Base(0x21C70000) + offset (0x1164)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RO	0x0	MFC0 Overflow status of the MFC Counter When this bit is set then the MFC counter does not get incremented further. The bit gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event. 0x0 (INACTIVE): Miss Frame Counter overflow not occurred 0x1 (ACTIVE): Miss Frame Counter overflow occurred
14:11	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
10:0	RO	0x000	MFC Dropped Packet Counters This counter indicates the number of packet counters that are dropped by the DMA either because of bus error or because of programming RPF field in DMA_CH0_Rx_Control register. The counter gets cleared when this register is read. Access restriction applies. Clears on read. Self-set to 1 on internal event.

GMAC_DMA_CH0_RX_ERI_CNT

Address: Operational Base(0x21C70000) + offset (0x1168)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	ECNT ERI Counter When ERIC bit of DMA_CH0_RX_Control register is set, this counter increments for burst transfer completed by the Rx DMA from the start of packet transfer. This counter will get reset at the start of new packet.

42.5 Interface Description

Table 42-3 GMAC mux0 Interface

Module Pin	Dir	Pad Name	IOMUX Setting
RMII/RGMII interface			
gmac_mclkinoutm0	I/O	VI_CIF_D12_M0/ETH_MCLK_M0/SPI1_CLK_M0/PDM_CLK0_M1/UART7_TX_M1/GPIO6_B4	GPIO6B_IOMUX_SEL_1[3:0]=3'h2
gmac_rxclkm0	I	VI_CIF_HSYNC_M0/ETH_RXCLK_M0/FEPHY_LEDSPD_M2/PWM0_CH3_M2/UART3_RX_M2/I2C2_SDA_M2/GPIO6_C3	GPIO6C_IOMUX_SEL_0[15:12]=3'h2
gmac_rxdvcrsm0	I	VI_CIF_D13_M0/ETH_RXCTL_M0/PDM_SDI0_M1/UART7_RX_M1/GPIO6_B5	GPIO6B_IOMUX_SEL_1[7:4]=3'h2
gmac_rxd0m0	I	VI_CIF_D10_M0/ETH_RXD0_M0/SPI1_MOSI_M0/PDM_SDI2_M1/UART6_RTSN_M1/GPIO6_B2	GPIO6B_IOMUX_SEL_0[11:8]=3'h2
gmac_rxd1m0	I	VI_CIF_D11_M0/ETH_RXD1_M0/SPI1_MISO_M0/PDM_SDI3_M1/UART6_CTSN_M1/GPIO6_B3	GPIO6B_IOMUX_SEL_0[15:12]=3'h2
gmac_rxd2m0	I	VI_CIF_D3_M0/ETH_RXD2_M0/CAN1_TXD_M1/SAI0_SDI0_M1/PWM1_CH3_M2/UART5_RX_M2/I2C4_SDA_M1/GPIO6_A3	GPIO6A_IOMUX_SEL_0[15:12]=3'h2
gmac_rxd3m0	I	VI_CIF_D4_M0/ETH_RXD3_M0/SAI0_MCLK_M1/PWM2_CH0_M2/UART5_RTSN_M2/I2C5_SCL_M3/GPIO6_A4	GPIO6A_IOMUX_SEL_1[3:0]=3'h2
gmac_txclkm0	O	VI_CIF_CLKOUT_M0/ETH_TXCLK_M0/FEPHY_LEDLINK_M2/PWM0_CH2_M2/UART3_TX_M2/GPIO6_C2	GPIO6C_IOMUX_SEL_0[11:8]=3'h2
gmac_txenm0	O	VI_CIF_D9_M0/ETH_TXCTL_M0/SPI1_CSN0_M0/SAI0_SDI1_M1/SAI0_SDO3_M1/UART6_RX_M1/GPIO6_B1	GPIO6B_IOMUX_SEL_0[7:4]

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			=3'h2
gmac_txd0m0	O	VI_CIF_D7_M0/ETH_TXD0_M0/PWM2_CH3_M2/SAI0_SDI3_M1/SAI0_SDO1_M1/UART4_CTSN_M2/GPIO6_A7	GPIO6A_IOMUX_SEL_1[15:12]=3'h2
gmac_txd1m0	O	VI_CIF_D8_M0/ETH_TXD1_M0/SPI1_CSN1_M0/SAI0_SDI2_M1/SAI0_SDO2_M1/UART6_TX_M1/GPIO6_B0	GPIO6B_IOMUX_SEL_0[3:0]=3'h2
gmac_txd2m0	O	VI_CIF_D5_M0/ETH_TXD2_M0/PWM2_CH1_M2/UART5_CTSN_M2/I2C5_SDA_M3/GPIO6_A5	GPIO6A_IOMUX_SEL_1[7:4]=3'h2
gmac_txd3m0	O	VI_CIF_D6_M0/ETH_TXD3_M0/PWM2_CH2_M2/UART4_RTSN_M2/GPIO6_A6	GPIO6A_IOMUX_SEL_1[11:8]=3'h2
gmac_refclkm0	O	VI_CIF_CLKIN_M0/ETH_CLK_25M_OUT_M0/PWM0_CH1_M2/UART3_CTSN_M2/GPIO6_C1	GPIO6C_IOMUX_SEL_0[7:4]=3'h2
ppstrigm0	I	VI_CIF_D0_M0/ETH_PPSTRIG_M0/CAN0_RXD_M1/SAI0_SCLK_M1/PWM1_CH0_M2/UART4_TX_M2/I2C3_SCL_M3/GPIO6_A0	GPIO6A_IOMUX_SEL_0[3:0]=3'h2
ptp_refclkm0	I	VI_CIF_D1_M0/ETH_PTP_REFCLK_M0/CAN0_TXD_M1/SAI0_LRCK_M1/PWM1_CH1_M2/UART4_RX_M2/I2C3_SDA_M3/GPIO6_A1	GPIO6A_IOMUX_SEL_0[7:4]=3'h2
ppsclkm0	O	VI_CIF_D2_M0/ETH_PPSCLK_M0/CAN1_RXD_M1/SAI0_SDO0_M1/PWM1_CH2_M2/UART5_TX_M2/I2C4_SCL_M1/GPIO6_A2	GPIO6A_IOMUX_SEL_0[11:8]=3'h2
Management interface			
gmac_mdcm0	O	VI_CIF_VSYNC_M0/ETH_MDC_M0/ETH_TESTRXCLK_OUT_M1/PWM0_CH0_M2/UART3_RTSN_M2/I2C2_SCL_M2/GPIO6_C0	GPIO6C_IOMUX_SEL_0[3:0]=3'h2
gmac_mdiom0	I/O	VI_CIF_D15_M0/ETH_MDIO_M0/ETH_TESTRXD_OUT_M1/PDM_CLK1_M1/UART7_CTSN_M1/GPIO6_B7	GPIO6B_IOMUX_SEL_1[15:12]=3'h2

Table 42-4 GMAC mux1 Interface

Module Pin	**Dir.**	**Pad Name**	**IOMUX Setting**
RMII/RGMII interface			
gmac_mclkinoutm1	I/O	VO_LCDC_D11/ETH_MCLK_M1/VI_CIF_D7_M1/DSMC_RDYN/PWM2_CH1_M1/UART6_CTSN_M0/GPIO5_B3	GPIO5B_IOMUX_SEL_0[15:12]=3'h2
gmac_rxclkm1	I	VO_LCDC_D23/ETH_RXCLK_M1/VI_CIF_HSYNC_M1/DSMC_D0/SAI1_SDI_M2/PWM3_CH7_M1/GPIO5_C7	GPIO5C_IOMUX_SEL_1[15:12]=3'h2
gmac_rxdvcrsm1	I	VO_LCDC_D8/ETH_RXCTL_M1/VI_CIF_D4_M1/DSMC_D9/IR_FPA_SDA2/UART6_TX_M0/GPIO5_B0	GPIO5B_IOMUX_SEL_0[3:0]=3'h2
gmac_rxd0m1	I	VO_LCDC_D9/ETH_RXD0_M1/VI_CIF_D5_M1/DSMC_D8/IR_FPA_SDA3/UART6_RX_M0/GPIO5_B1	GPIO5B_IOMUX_SEL_0[7:4]=3'h2
gmac_rxd1m1	I	VO_LCDC_D10/ETH_RXD1_M1/VI_CIF_D6_M1/DSMC_RESETN/DSMC_INT1/PWM2_CH0_M1/UART6_RTSN_M0/GPIO5_B2	GPIO5B_IOMUX_SEL_0[11:8]=3'h2
gmac_rxd2m	I	VO_LCDC_D19/ETH_RXD2_M1/VI_CIF_D15_M1/DSMC_D4/SAI1_MCLK_M2/PWM3_CH3_M1/GPIO5_C3	GPIO5C_IOMUX_SEL_0[15

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1			:12]=3'h2
gmac_rxd3m1	I	VO_LCDC_D20/ETH_RXD3_M1/VI_CIF_VSYNC_M1/DSMC_D3/SAI1_SDO_M2/PWM3_CH4_M1/GPIO5_C4	GPIO5C_IOMUX_SEL_1[3:0]=3'h2
gmac_txclkm1	O	VO_LCDC_D22/ETH_TXCLK_M1/VI_CIF_CLKIN_M1/DSMC_D1/SAI1_LRCK_M2/PWM3_CH6_M1/GPIO5_C6	GPIO5C_IOMUX_SEL_1[11:8]=3'h2
gmac_txenm1	O	VO_LCDC_D18/ETH_TXCTL_M1/VI_CIF_D14_M1/DSMC_D5/IR_FPA_SDA6/PWM3_CH2_M1/GPIO5_C2	GPIO5C_IOMUX_SEL_0[11:8]=3'h2
gmac_txd0m1	O	VO_LCDC_D15/ETH_TXD0_M1/VI_CIF_D11_M1/DSMC_CLKP/PWM2_CH3_M1/UART7_CTSN_M0/GPIO5_B7	GPIO5B_IOMUX_SEL_1[15:12]=3'h2
gmac_txd1m0	O	VO_LCDC_D16/ETH_TXD1_M1/VI_CIF_D12_M1/DSMC_D7/IR_FPA_SDA4/PWM3_CH0_M1/GPIO5_C0	GPIO5C_IOMUX_SEL_0[3:0]=3'h2
gmac_txd2m1	O	VO_LCDC_D21/ETH_TXD2_M1/VI_CIF_CLKOUT_M1/DSMC_D2/SAI1_SCLK_M2/PWM3_CH5_M1/GPIO5_C5	GPIO5C_IOMUX_SEL_1[7:4]=3'h2
gmac_txd3m1	O	VO_LCDC_D0/ETH_TXD3_M1/VI_CIF_D0_M1/DSMC_CSN1/IR_FPA_SDA0/PWM2_CH4_M0/UART4_RTSN_M1/GPIO5_A0	GPIO5A_IOMUX_SEL_0[3:0]=3'h2
gmac_refclkm1	O	VO_LCDC_D17/ETH_CLK_25M_OUT_M1/VI_CIF_D13_M1/DSMC_D6/IR_FPA_SDA5/PWM3_CH1_M1/GPIO5_C1	GPIO5C_IOMUX_SEL_0[7:4]=3'h2
ppstrigm1	I	VO_LCDC_HSYNC/SPI1_CLK_M2/ETH_PPSTRIG_M1/DSMC_CSN2/I2C3_SDA_M2/PWM1_CH2_M1/GPIO5_D1	GPIO5D_IOMUX_SEL_0[7:4]=3'h2
ptp_refclkm1	I	VO_LCDC_DEN/SPI1_CSN0_M2/ETH_PTP_REFCLK_M1/DSMC_CSN3/I2C3_SCL_M2/PWM0_CH6_M2/GPIO5_D0	GPIO5D_IOMUX_SEL_0[3:0]=3'h2
Ppsclkm1	O	VO_LCDC_D2/ETH_PPSCLK_M1/VI_CIF_D2_M1/DSMC_D15/SAI2_SDI1_M1/PWM0_CH5_M2/UART4_TX_M1/GPIO5_A2	GPIO5A_IOMUX_SEL_0[11:8]=3'h2
Management interface			
gmac_mdcm1	O	VO_LCDC_D14/ETH_MDC_M1/VI_CIF_D10_M1/DSMC_CLKN/DSMC_INT0/ETH_TESTRXCLK_OUT_M0/PWM2_CH2_M1/UART7_RTSN_M0/GPIO5_B6	GPIO5B_IOMUX_SEL_1[11:8]=3'h2
gmac_mdiom1	I/O	VO_LCDC_D13/ETH_MDIO_M1/VI_CIF_D9_M1/DSMC_DQS0/ETH_TESTRXD_OUT_M0/UART7_RX_M0/GPIO5_B5	GPIO5B_IOMUX_SEL_1[7:4]=3'h2

42.6 Application Note

42.6.1 GMAC Descriptors

The DMA engine uses descriptors to efficiently move data from source to destination with minimal application CPU intervention. The DMA is designed for packet-oriented data transfers such as packets in Ethernet. The DMA controller can be programmed to interrupt the application CPU for situations such as Packet Transmit and Receive Transfer completion, and other normal or error conditions.

The DMA and the application communicate through the following two data structures:

- Control and Status registers (CSR)
- Descriptor lists and data buffers

The base address of each list is written to the respective Tx Descriptor List Address register and Rx Descriptor List Address register. The descriptor list is forward linked and the next descriptor is always considered at a fixed offset to the current one. The offset is controlled by the DSL field of DMA_Ch[n]_Control register. The number of descriptors in

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the list is programmed in the respective Tx (or Rx) Descriptor Ring Length register. Once the DMA processes the last descriptor in the list, it automatically jumps back to the descriptor in the List Address register to create a descriptor ring.
The descriptor lists reside in the physical memory address space of the application. Each descriptor can point to a maximum of two buffers in the system memory. This enables two buffers to be used, physically addressed, rather than contiguous buffers in memory.
A data buffer resides in the application physical memory space and consists of an entire packet or part of a packet but cannot exceed a single packet. Buffers contain only data. Buffer status is maintained in the descriptor. Data chaining refers to packets that span multiple data buffers. However, a single descriptor cannot span multiple packets. The DMA skips to the data buffer of next packet when EOP is detected.
The GMAC supports the following two types of descriptors:

- Normal Descriptor: Normal descriptors are used for packet data and to provide control information applicable to the packets to be transmitted
- Context Descriptor: Context descriptors are used to provide control information applicable to the packet to be transmitted

The GMAC supports the ring structure for the DMA descriptor.

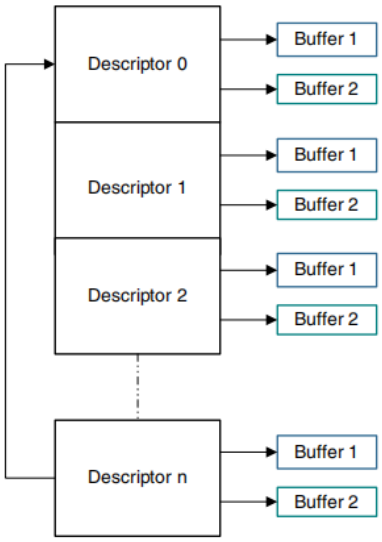

Fig. 42-10 Descriptor Ring Structure

In Ring structure, descriptors are separated by the Word, DWord, or LWord number programmed in the DSL field of the DMA_CH#_Control register. The application needs to program the total ring length, that is, the total number of descriptors in ring span in the following registers of a DMA channel:

- Transmit Descriptor Ring Length Register (DMA_CH#_TxDesc_Ring_Length)
- Receive Descriptor Ring Length Register (DMA_CH#_RxDesc_Ring_Length)

The Descriptor Tail Pointer Register contains the pointer to the descriptor address (N). The base address and the current descriptor pointer decide the address of the current descriptor that the DMA can process.
The descriptors up to one location less than the one indicated by the descriptor tail pointer (N – 1) are owned by the DMA. The DMA continues to process the descriptors until the following condition occurs:

Current Descriptor Pointer == Descriptor Tail Pointer

The DMA goes into the Suspend mode when this condition occurs. The application must perform a write to the Descriptor Tail pointer register and update the tail pointer so that the following condition is true:

Current Descriptor Pointer < Descriptor Tail Pointer

The DMA automatically wraps around the base address when the end of ring is reached. For descriptors owned by the application, the OWN bit of DES3 is reset to 0. For descriptors owned by the DMA, the OWN bit is set to 1. If the application has only one descriptor in the beginning, the application sets the last descriptor address (tail pointer) to

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Descriptor Base Address + 1. The DMA processes the first descriptor and then waits for the application to advance the tail pointer.

42.6.2 GMAC Transmit Descriptors

The DMA in GMAC requires at least one descriptor for a transmit packet. In addition to two buffers, two byte-count buffers, and two address pointers, the transmit descriptor has control fields which can be used to control the MAC operation on per-transmit packet basis. The Transmit Normal descriptor has two formats: Read format and Write-Back format.

42.6.3 GMAC Transmit Normal Descriptor (Read Format)

Table 42-4 TDES0 Normal Descriptor (Read Format)

Bit	Name	Description
31:0	BUF1AP	Buffer 1 Address Pointer or TSO Header Address Pointer These bits indicate the physical address of Buffer 1. These bits indicate the TSO Header Address pointer when the following bits are set: ■ TSE bit of TDES3 ■ FD bit of TDES3

Table 42-5 TDES1 Normal Descriptor (Read Format)

Bit	Name	Description
31:0	BUF2AP	Buffer 2 or Buffer 1 Address Pointer This bit indicates the physical address of Buffer 2 when a descriptor ring structure is used. There is no limitation for the buffer address alignment. In 40- or 48-bit addressing mode, these bits indicate the most-significant 8- or 16- bits of the Buffer 1 Address Pointer.

Table 42-6 TDES2 Normal Descriptor (Read Format)

Bit	Name	Description
31	IOC	Interrupt on Completion This bit controls the setting of TI and ETI status bits in the DMA_CH#_Status register. When ETIC = 1 and TDES2[LD] = 0, this bit sets the ETI bit. When TDES3[LD] = 1, this bit sets the TI status bit.
30	TTSE/TMWD	Transmit Timestamp Enable or External TSO Memory Write Enable This bit enables the IEEE1588 time stamping for Transmit packet referenced by the descriptor, if TSE bit is not set. If TSE bit is set and external TSO memory is enabled, setting this bit disables external TSO memory writing for this packet.
29:16	B2L	Buffer 2 Length The driver sets this field. When set, this field indicates Buffer 2 length
15:14	VTIR	VLAN Tag Insertion or Replacement These bits request the MAC to perform VLAN tagging or untagging before transmitting the packets. The application must set the CRC Pad Control bits appropriately when VLAN Tag Insertion, Replacement, or Deletion is enabled for the packet. The following list describes the values of these bits: ■ 2'b00: Do not add a VLAN tag. ■ 2'b01: Remove the VLAN tag from the packets before transmission. This option should be used only with the

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Bit	Name	Description
		VLAN packets. ■ 2'b10: Insert a VLAN tag with the tag value programmed in the MAC_VLAN_Incl register or context descriptor. ■ 2'b11: Replace the VLAN tag in packets with the tag value programmed in the MAC_VLAN_Incl register or context descriptor. This option should be used only with the VLAN packets. These bits are valid when the Enable SA and VLAN Insertion on Tx option is selected while configuring the core
13:0	HL or B1L	Header Length or Buffer 1 Length For Header length only bits [9:0] are taken. The size 13:0 is applicable only when interpreting buffer 1 length. If the TCP Segmentation Offload feature is enabled through the TSE bit of TDES3, this field is equal to the header length. When the TSE bit is set in TDES3, the header length includes the length in bytes from Ethernet Source address till the end of the TCP header. Themaximum header length supported for TSO feature is 1023 bytes. The maximum header length supported for TSO feature is 1023 bytes. If the TCP Segmentation Offload feature is not enabled, this field is equal to Buffer 1 length.

Table 42-7 TDES3 Normal Descriptor (Read Format)

Bit	Name	Description
31	OWN	Own Bit When this bit is set, it indicates that the DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit after it completes the transfer of data given in the associated buffer(s).
30	CTXT	Context Type This bit should be set to 1'b0 for normal descriptor.
29	FD	First Descriptor When this bit is set, it indicates that the buffer contains the first segment of a packet.
28	LD	Last Descriptor When this bit is set, it indicates that the buffer contains the last segment of the packet. When this bit is set, the B1L or B2L field should have a non-zero value.
27:26	CPC	CRC Pad Control This field controls the CRC and Pad Insertion for Tx packet. This field is valid only when the first descriptor bit (TDES3[29]) is set. The following list describes the values of Bits[27:26]: ■ 2'b00: CRC and Pad Insertion. The MAC appends the cyclic redundancy check (CRC) at the end of the transmitted packet of length greater than or equal to 60 bytes. The MAC automatically appends padding and CRC to a packet with length less than 60 bytes. ■ 2'b01: CRC Insertion (Disable Pad Insertion). The MAC appends the CRC at the end of the transmitted packet but it does not append padding. The application should ensure that the padding bytes are present in the packet being transferred from the Transmit Buffer, that

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Bit	Name	Description
		is, the packet being transferred from the Transmit Buffer is of length greater than or equal to 60 bytes. ■ 2'b10: Disable CRC Insertion. The MAC does not append the CRC at the end of the transmitted packet. The application should ensure that the padding and CRC bytes are present in the packet being transferred from the Transmit Buffer. ■ 2'b11: CRC Replacement. The MAC replaces the last four bytes of the transmitted packet with recalculated CRC bytes. The application should ensure that the padding and CRC bytes are present in the packet being transferred from the Transmit Buffer. This field is valid only for the first descriptor. Note: When the TSE bit is set, the MAC ignores this field because the CRC and pad insertion is always done for segmentation.
25:23	SAIC	SA Insertion Control These bits request the MAC to add or replace the Source Address field in the Ethernet packet with the value given in the MAC Address 0 register. The application must set the CRC Pad Control bits appropriately when SA Insertion Control is enabled for the packet. Bit 25 specifies the MAC Address Register (1 or 0) value that is used for Source Address insertion or replacement. The following list describes the values of Bits[24:23]: ■ 2'b00: Do not include the source address ■ 2'b01: Include or insert the source address. For reliable transmission, the application must provide frames without source addresses. ■ 2'b10: Replace the source address. For reliabletransmission, the application must provide frames with source addresses. ■ 2'b11: Reserved These bits are valid in the GMAC-DMA, GMAC-AXI, and GMAC-AHB configurations when the Enable SA and VLAN Insertion on Tx option is selected while configuring the core and when the First Segment control bit (TDES3 [29]) is set. This field is valid only for the first descriptor.
22:19	SLOTNUM or THL	SLOTNUM: Slot Number Control Bits in AV Mode These bits indicate the slot interval in which the data should be fetched from the corresponding buffers addressed by TDES0 or TDES1. When the Transmit descriptor is fetched, the DMA compares the slot number value in this field with the slot interval maintained in the RSN field DMA_CH#_Slot_Function_Control_Status. It fetches the data from the buffers only if a value matches. These bits are valid only for the AV channels. THL: TCP/UDP Header Length If the TSE bit is set, this field contains the length of the TCP/UDP header. The minimum value of this field must be 5 for TCP header. The value must be equal to 2 for UDP header. This field is valid only for the first descriptor.
18	TSE	TCP Segmentation Enable

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Bit	Name	Description
		When this bit is set, the DMA performs the TCP/UDP segmentation or UDP fragmentation for a packet depending on the TSE_MODE[1:0] bit of the DMA_CH(#i)_Tx_Control Register. This bit is valid only if the FD bit is set.
17:16	CIC/TPL	Checksum Insertion Control or TCP Payload Length These bits control the checksum calculation and insertion. The following list describes the bit encoding: ■ 2'b00: Checksum Insertion Disabled. ■ 2'b01: Only IP header checksum calculation and insertion are enabled. ■ 2'b10: IP header checksum and payload checksum calculation and insertion are enabled, but pseudo-header checksum is not calculated in hardware. ■ 2'b11: IP Header checksum and payload checksum calculation and insertion are enabled, andpseudo-header checksum is calculated in hardware. This field is valid when the Enable Transmit TCP/IP Checksum Offload option is selected and the TSE bit is reset. When the TSE bit is set, this field contains the upper bits [17:16] of the TCP Payload (or IP Payload for UDP fragmentation). This allows the TCP/UDP packet length field to be spanned across TDES3[17:0] to provide 256 KB packet length support. This field is valid only for the first descriptor.
15	TPL	Reserved or TCP Payload Length When the TSE bit is reset, this bit is reserved. When the TSE bit is set, this is Bit 15 of the TCP payload length [17:0]. This field is valid only when the Enable TCP Segmentation Offloading for TCP/IP Packets option is selected while configuring the core.
14:0	FL/TPL	Frame Length or TCP Payload Length This field is equal to the length of the packet to be transmitted in bytes. When the TSE bit is not set, this field is equal to the total length of the packet to be transmitted: Ethernet Header Length + TCP /IP Header Length – Preamble Length – SFD Length + Ethernet Payload Length When the TSE bit is set, this field is equal to the lower 15 bits of the TCP payload length in case of segmentation and IP payload in case of UDP fragmentation. In case of segmentation, this length does not includeEthernet header or TCP/UDP/IP header length. In case of fragmentation, this length does not include Ethernet header and IP header. When DWRR/WFQ algorithm is NOTenabled, value written into this field is not used when TSE = 0.

42.6.4 GMAC Transmit Normal Descriptor (Write-back Format)

The write-back format of the Transmit Descriptor includes timestamp low, timestamp high, OWN, and Status bits. The write-back format is applicable only for the last descriptor of the corresponding packet. The LD bit (TDES3[28]) is set in the descriptor where the DMA writes back the status and timestamp information for the corresponding Transmit packet. this format is only applicable to the last descriptor of a packet.

Table 42-8 TDES0 Normal Descriptor (Write-Back Format)

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Bit	Name	Description
31:0	TTSL	Transmit Packet Timestamp Low The DMA updates this field with least significant 32 bits of the timestamp captured for the corresponding Transmit packet. The DMA writes the timestamp only if TTSE bit of TDES2 is set in the first descriptor of the packet. This field has the timestamp only if the Last Segment bit (LS) in the descriptor is set and the Timestamp status (TTSS) bit is set

Table 42-9 TDES1 Normal Descriptor (Write-Back Format)

Bit	Name	Description
31:0	TTSH	Transmit Packet Timestamp High The DMA updates this field with the most significant 32 bits of the timestamp captured for corresponding transmit packet. The DMA writes the timestamp only if the TTSE bit of TDES2 is set in the first descriptor of the packet. This field has the timestamp only if the Last Segment bit (LS) in the descriptor is set and Timestamp status (TTSS) bit is set.

Table 42-10 TDES2 Normal Descriptor (Write-Back Format)

Bit	Name	Description
31:0	Rsvd	Reserved

Table 42-11 TDES2 Normal Descriptor (Write-Back Format)

Bit	Name	Description
31	OWN	Own Bit When this bit is set, it indicates that the DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit after it completes the transfer of data given in the associated buffer(s).
30	CTXT	Context Type This bit should be set to 1'b0 for normal descriptor.
29	FD	First Descriptor When this bit is set, it indicates that the buffer contains the first segment of a packet.
28	LD	Last Descriptor When this bit is set, it indicates that the buffer contains the last segment of the packet. When this bit is set, the B1L or B2L field should have a non-zero value.
27:24	Rsvd	Reserved
23	DE	Descriptor Error When this bit is set, it indicates that the descriptor content is incorrect. The DMA sets this bit during write-back while closing the descriptor. Descriptor Errors can be: ■ Incorrect sequence from the context descriptor. For example, a location after the first descriptor for a packet ■ All 1s ■ CTXT, LD, and FD bits set to 1 Note 1: When Descriptor Error occurs due to All 1s or CTXT, LD, and FD bits set to 1, the Transmit DMA closes the transmit descriptor with DE and LD bits set to 1. When IOC bit in TDES2 of corresponding first descriptor is set to 1, Transmit DMA will set the TI bit in the DMA_CH#_Status register.

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Bit	Name	Description
		Note 2: Based on CTXT, LD, and FD bits of the transmit descriptor, the subsequent descriptor might be considered as the First Descriptor (even if FD bit is not set) and partial packet is sent.
22:18	Rsvd	Reserved
17	TTSS	Tx Timestamp Status This status bit indicates that a timestamp has been captured for the corresponding transmit packet. When this bit is set, TDES0 and TDES1 have timestamp values that were captured for the Transmit packet. This field is valid only when the Last Segment control bit (TDES3 [28]) in a descriptor is set. This bit is valid only when IEEE1588 timestamping feature is enabled; otherwise, it is reserved.
16	EUE	ECC Uncorrectable Error Status Indicates the ECC uncorrectable error in the TSO memory. Note: Uncorrectable error in Transmit FIFO memory is reported with (Bit 13) FF = 1. This is because, all such packets are flushed by GMAC.
15	ES	Error Summary This bit indicates the logical OR of the following bits: ■ TDES3[0]: IP Header Error ■ TDES3[14]: Jabber Timeout ■ TDES3[13]: Packet Flush ■ TDES3[12]: Payload Checksum Error ■ TDES3[11]: Loss of Carrier ■ TDES3[10]: No Carrier ■ TDES3[9]: Late Collision ■ TDES3[8]: Excessive Collision ■ TDES3[3]: Excessive Deferral ■ TDES3[2]: Underflow Error This bit is also set when EUE (bit 16) is set
14	JT	Jabber Timeout This bit indicates that the MAC transmitter has experienced a jabber time-out. This bit is set only when the JD bit of the MAC_Configuration register is not set.
13	PF	Packet Flushed This bit indicates that the DMA or MTL flushed the packet because of a software flush command given by the CPU.
12	PCE	Payload Checksum Error This bit indicates that the Checksum Offload engine had a failure and did not insert any checksum into theencapsulated TCP, UDP, or ICMP payload. This failure can be either because of insufficient bytes, as indicated by the Payload Length field of the IP Header or the MTL starting to forward the packet to the MAC transmitter in Store-and-Forward mode without the checksum having been calculated yet. This second error condition only occurs when the Transmit FIFO depth is less than the length of the Ethernet packet being transmitted to avoid deadlock, the MTL starts forwarding the packet when the FIFO is full, even in the store-and-forward mode. This error can also occur when Bus Error is detected during

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Bit	Name	Description
		packet transfer. When the Full Checksum Offload engine is not enabled, this bit is reserved.
11	LoC	Loss of Carrier This bit indicates that Loss of Carrier occurred during packet transmission (that is, the gmii_crs_i signal was inactive for one or more transmit clock periods during packet transmission). This is valid only for the packets transmitted without collision and when the MAC operates in thehalf-duplex mode.
10	NC	No Carrier This bit indicates that the carrier sense signal form the PHY was not asserted during transmission.
9	LC	Late Collision This bit indicates that packet transmission was aborted because a collision occurred after the collision window (64 byte times including Preamble in MII mode and 512 byte times including Preamble and Carrier Extension in GMII mode). This bit is not valid if Underflow Error is set.
8	EC	Excessive Collision This bit indicates that the transmission was aborted after 16 successive collisions while attempting to transmit the current packet. If the DR bit is set in the MAC_Configuration register, this bit is set after first collision and the transmission of the packet is aborted.
7:4	CC	Collision Count This 4-bit counter value indicates the number of collisions occurred before the packet was transmitted. The count is not valid when the EC bit is set.
3	ED	Excessive Deferral This bit indicates that the transmission ended because of excessive deferral of over 24,288 bit times (155,680 bits times in 1000 Mbps mode or Jumbo Packet enabled mode) if DC bit is set in the MAC_Configuration register. When TBS is enabled in full duplex mode and this bit is set, it indicates that the frame has been dropped after the expiry time has reached.
2	UF	Underflow Error This bit indicates that the MAC aborted the packet because the data arrived late from the system memory. The underflow error can occur because of either of the following conditions: ■ The DMA encountered an empty Transmit Buffer while transmitting the packet ■ The application filled the MTL Tx FIFO slower than the MAC transmit rate The transmission process enter the suspended state and sets the underflow bit corresponding to a queue in the MTL_Interrupt_Status register.
1	DB	Deferred Bit This bit indicates that the MAC deferred before transmitting because of presence of carrier. This bit is valid only in the half-duplex mode.
0	IHE	IP Header Error When IP Header Error is set, this bit indicates that the Checksum Offload engine detected an IP header error. This bit is valid only when Tx Checksum Offload is

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Bit	Name	Description
		enabled. Otherwise, it is reserved. If COE detects an IP header error, it still inserts an IPv4 header checksum if the Ethernet Type field indicates an IPv4 payload. In full duplex mode, when EST/Qbv is enabled and this bit is set, it indicates the frame drop status due to Frame Size error or Schedule Error.

42.6.5 GMAC Transmit Context Descriptor

The context descriptor is used to provide the timestamps for one-step timestamp correction, VLAN Tag ID for VLAN insertion feature. The Transmit Context descriptor can be provided any time before a packet descriptor. The context is valid for the current packet and subsequent packets. The context descriptor is used to provide the timestamps for one-step timestamp correction and VLAN Tag ID for VLAN insertion feature. Write back is done on a context descriptor only to reset the OWN bit.

Bit	Name	Description
31:0	TTSL	Transmit Packet Timestamp Low For one-step correction, the driver can provide the lower 32 bits of timestamp in this descriptor word. The DMA uses this value as the low word for doing one-step timestamp correction. This field is valid only if the OSTC and TCMSSV bits of TDES3 context descriptor are set.

Table 42-12 TDES0 Context Descriptor

Table 42-13 TDES1 Context Descriptor

Bit	Name	Description
31:0	TTSH	Transmit Packet Timestamp High For one-step correction, the driver can provide the upper 32 bits of timestamp in this descriptor. The DMA uses this value as the high word for doing one-step timestamp correction. This field is valid only if the OSTC and TCMSSV bits of TDES3 context descriptor are set.

Table 42-14 TDES2 Context Descriptor

Bit	Name	Description
31:16	IVT	Inner VLAN Tag When the IVLTV bit of TDES3 context descriptor is set and the TCMSSV and OSTC bits of TDES3 context descriptor are reset, TDES2[31:16] contains the inner VLAN Tag to be inserted in the subsequent Transmit packets.
15:14	Reserved	Reserved
13:0	MSS	Maximum Segment Size When the Enable TCP Segmentation Offloading for TCP/IP Packets option is selected, the driver can provide maximum segment size in this field. This segment size is used while segmenting the TCP/IP payload. This field is valid only if the TCMSSV bit of TDES3 context descriptor is set and the OSTC bit of the TDES3 context descriptor is reset.

Table 42-15 TDES3 Context Descriptor

Bit	Name	Description
31	OWN	Own Bit When this bit is set, it indicates that the GMAC DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit immediately after the read.
30	CTXT	Context Type

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Bit	Name	Description
		This bit should be set to 1'b1 for Context descriptor.
29:28	Reserved	Reserved
27	OSTC	One-Step Timestamp Correction Enable When this bit is set, the DMA performs a one-step timestamp correction with reference to the timestamp values provided in TDES0 and TDES1.
26	TCMSSV	One-Step Timestamp Correction Input or MSS Valid When this bit and the OSTC bit are set, it indicates that the Timestamp Correction input provided in TDES0 and TDES1 is valid. When the OSTC bit is reset and this bit and the TSE bit of TDES3 are set in subsequent normal descriptor, it indicates that the MSS input in TDES2 is valid.
25:24	Reserved	Reserved
23	DE	Descriptor Error When this bit is set, it indicates that the descriptor content is incorrect.The DMA sets this bit during write-back while closing the context descriptor. Descriptor Errors can be: ■ Incorrect sequence from the context descriptor. For example, a location before the first descriptor for a packet ■ All 1s ■ CD, LD, and FD bits set to 1 Note 1: When Descriptor Error occurs due to All 1s or CTXT, LD, and FD bits set to 1, the Transmit DMA closes the transmit descriptor with DE and LD bits set to 1. When IOC bit in TDES2 of corresponding first descriptor is set to 1, Transmit DMA will set the TI bit in the DMA_CH#_Status Register. Note 2: Based on CTXT, LD, and FD bits of the transmit descriptor, the subsequent descriptor might be considered as the First Descriptor (even if FD bit is not set) and partial packet is sent.
22:20	Reserved	Reserved
19:18	IVTIR	Inner VLAN Tag Insert or Replace When this bit is set, these bits request the MAC to perform Inner VLAN tagging or un-tagging before transmitting the packets. If the packet is modified for VLAN tags, the MAC automatically recalculates and replaces the CRC bytes. The following list describes the values of these bits: ■ 2'b00: Do not add the inner VLAN tag. ■ 2'b01: Remove the inner VLAN tag from the packets before transmission. This option should be used only with the VLAN frames. ■ 2'b10: Insert an inner VLAN tag with the tag value programmed in the MAC_Inner_VLAN_Incl register or context descriptor. ■ 2'b11: Replace the inner VLAN tag in packets with the tag value programmed in the MAC_Inner_VLAN_Incl register or context descriptor. This option should be used only with the VLAN frames.

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Bit	Name	Description
		These bits are valid when the Enable SA and VLAN Insertion on Tx and Enable Double VLAN Processing options are selected.
17	IVLTV	Inner VLAN Tag Valid When this bit is set, it indicates that the IVT field of TDES2 is valid.
16	VLTV	VLAN Tag Valid When this bit is set, it indicates that the VT field of TDES3 is valid.
15:0	VT	VLAN Tag This field contains the VLAN Tag to be inserted or replaced in the packet. This field is used as VLAN Tag only when the VLTI bit of the MAC_VLAN_Incl register is reset.

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42.6.6 GMAC Receive Descriptors

The DMA in GMAC attempts to read a descriptor only if the Tail Pointer is different from the Base Pointer or current pointer. It is recommended to have a descriptor ring with a length that can accommodate at least two complete packets received by the MAC. Otherwise, the performance of the DMA is impacted greatly because of the unavailability of the descriptors. In such situations, the RxFIFO in MTL becomes full and starts dropping packets.

The following Receive Descriptors are present:

- Normal descriptors
- Context descriptors

All RX descriptors are prepared by the software and given to the DMA as "Normal" Descriptors with the content as shown in Receive Normal Descriptor (Read Format). The DMA reads this descriptor and after transferring a received packet (or part of) to the buffers indicated by the descriptor, the Rx DMA will close the descriptor with the corresponding packet status. The format of this status is given in the "Receive Normal Descriptor (Write-Back Format)". For some packets, the normal descriptor bits are not enough to write the complete status. For such packets, the RX DMA writes the extended status to the next descriptor (without processing or using the Buffers/ Pointers embedded in that descriptor). The format and content of the descriptor write back is described in "Receive Context Descriptor".

42.6.7 GMAC Receive Normal Descriptors(Read Format)

Table 42-16 TDES0 Normal Descriptor(Read Format)

Bit	Name	Description
31:0	BUF1AP	Header or Buffer 1 Address Pointer When the SPH bit of Control register of a channel is reset, these bits indicate the physical address of Buffer 1. When the SPH bit is set, these bits indicate the physical address of Header Buffer where the Rx DMA writes the L2/L3/L4 header bytes of the received packet. The application can program a byte-aligned address for this buffer which means that the LS bits of this field can be non-zero. However, while transferring the start of packet, the DMA performs a Write operation with RDES0[1:0] (or RDES0[2:0]/[3:0] in case of 64-/128-bit configuration) as zero. However, the packet data is shifted as per actual offset as given by buffer address pointer. If the address pointer points to a buffer where the middle or last part of the packet is stored, the DMA ignores the offset address and writes to the full location as indicated by the data-width.

Table 42-17 TDES1 Normal Descriptor(Read Format)

Bit	Name	Description
31:0	Reserved or BUF1AP	In 64-bit addressing mode, this field contains the most-significant 32 bits of the Buffer 1 Address Pointer. Otherwise, this field is reserved.

Table 42-18 TDES2 Normal Descriptor(Read Format)

Bit	Name	Description
31:0	Reserved or BUF1AP	In 64-bit addressing mode, this field contains the most-significant 32 bits of the Buffer 1 Address Pointer. Otherwise, this field is reserved.

Table 42-19 TDES3 Normal Descriptor(Read Format)

Bit	Name	Description
31	OWN	Own Bit When this bit is set, it indicates that the GMAC DMA owns the descriptor. When this bit is reset, it indicates

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Bit	Name	Description
		that the application owns the descriptor. The DMA clears this bit when either of the following conditions is true: ■ The DMA completes the packet reception ■ The buffers associated with the descriptor are full
30	IOC	Interrupt Enabled on Completion When this bit is set, an interrupt is issued to the application when the DMA closes this descriptor.
29:26	Rsvd	Reserved
25	BUF2V	Buffer 2 Address Valid When this bit is set, it indicates to the DMA that the buffer 2 address specified in RDES2 is valid. The application must set this bit so that the DMA can use the address, to which the Buffer 2 address in RDES2 is pointing, to write received packet data.
24	BUF1V	Buffer 1 Address Valid When set, this indicates to the DMA that the buffer 1 address specified in RDES1 is valid. The application must set this value if the address pointed to by Buffer 1 address in RDES1 can be used by the DMA to write received packet data.
23:0	Rsvd	Reserved

42.6.8 GMAC Receive Normal Descriptors(Write-Back Format)

Table 42-20 TDES0 Normal Descriptor(Write-Back Format)

Bit	Name	Description
31:16	IVT	Inner VLAN Tag This field contains the Inner VLAN tag of the received packet if the RS0V bit of RDES3 is set. This is valid only when Double VLAN tag processing and VLAN tag stripping are enabled.
15:0	OVT	Outer VLAN Tag This field contains the Outer VLAN tag of the received packet if the RS0V bit of RDES3 is set.

Table 42-21 TDES1 Normal Descriptor(Write-Back Format)

Bit	Name	Description
31:16	OPC	OAM Sub-Type Code, or MAC Control Packet opcode OAM Sub-Type Code If Bits[18:16] of RDES3 are set to 3'b111, this field contains the OAM sub-type and code fields. MAC Control Packet opcode If Bits[18:16] of RDES3 are set to 3'b110, this field contains the MAC Control packet opcode field.
15	TD	Timestamp Dropped This bit indicates that the timestamp was captured for this packet but it got dropped in the MTL Rx FIFO because of overflow. This bit is available only when you select the Timestamp feature. Otherwise, this bit is reserved.
14	TSA	Timestamp Available When Timestamp is present, this bit indicates that the timestamp value is available in a context descriptor word 2 (RDES2) and word 1(RDES1). This is valid only when the Last Descriptor bit (RDES3 [28]) is set. The context descriptor is written in the next descriptor just after the last normal descriptor for a packet.
13	PV	PTP Version

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Bit	Name	Description
		This bit indicates that the received PTP message has the IEEE 1588 version 2 format. When this bit is reset, it indicates the IEEE 1588 version 1 format. This bit is available only when you select the Timestamp feature. Otherwise, this bit is reserved.
12	PFT	PTP Packet Type This bit indicates that the PTP message is sent directly over Ethernet. This bit is available only when you select the Timestamp feature. Otherwise, this bit is reserved.
11:8	PMT	PTP Message Type These bits are encoded to give the type of the message received: ■ 0000: No PTP message received ■ 0001: SYNC (all clock types) ■ 0010: Follow_Up (all clock types) ■ 0011: Delay_Req (all clock types) ■ 0100: Delay_Resp (all clock types) ■ 0101: Pdelay_Req (in peer-to-peer transparent clock) ■ 0110: Pdelay_Resp (in peer-to-peer transparent clock) ■ 0111: Pdelay_Resp_Follow_Up (in peer-to-peer transparent clock) ■ 1000: Announce ■ 1001: Management ■ 1010: Signaling ■ 1011–1110: Reserved ■ 1111: PTP packet with Reserved message type These bits are available only when you select the Timestamp feature.
7	IPCE	IP Payload Error When this bit is set, it indicates either of the following: ■ The 16-bit IP payload checksum (that is, the TCP, UDP, or ICMP checksum) calculated by the MAC does not match the corresponding checksum field in the received segment. ■ The TCP, UDP, or ICMP segment length does not match the payload length value in the IP Header field. ■ The TCP, UDP, or ICMP segment length is less than minimum allowed segment length for TCP, UDP, or ICMP. Bit 15 (ES) of RDES3 is not set when this bit is set.
6	IPCB	IP Checksum Bypassed This bit indicates that the checksum offload engine is bypassed. This bit is available when you select the Enable Receive TCP/IP Checksum Check feature.
5	IPV6	IPv6 header Present This bit indicates that an IPV6 header is detected. When the Enable Split Header Feature option is selected and the SPH bit of Control Register of a channel is set, the IPV6 header is available in the header buffer area to which RDES0 is pointing.
4	IPV4	IPV4 Header Present This bit indicates that an IPV4 header is detected. When the SPH bit of RDES3 is set, the IPV4 header is available in the header buffer area to which RDES0 is pointing.
3	IPHE	IP Header Error When this bit is set, it indicates either of the following:

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Bit	Name	Description
		■ The 16-bit IPv4 header checksum calculated by the MAC does not match the received checksum bytes. ■ The IP datagram version is not consistent with the Ethernet Type value. ■ Ethernet packet does not have the expected number of IP header bytes. This bit is valid when either Bit 5 or Bit 4 is set. This bit is available when you select the Enable Receive TCP/IP Checksum Check feature.
2:0	PT	Payload Type These bits indicate the type of payload encapsulated in the IP datagram processed by the Receive Checksum Offload Engine (COE): ■ 3'b000: Unknown type or IP/AV payload not processed ■ 3'b001: UDP ■ 3'b010: TCP ■ 3'b011: ICMP ■ 3'b110: AV Tagged Data Packet ■ 3'b111: AV Tagged Control Packet ■ 3'b101: AV Untagged Control Packet ■ 3'b100: IGMP if IPV4 Header Present bit is set else DCB (LLDP) Control Packet If the COE does not process the payload of an IP datagram because there is an IP header error or fragmented IP, it sets these bits to 3'b000.

Table 42-22 TDES2 Normal Descriptor(Write-Back Format)

Bit	Name	Description
31:29	L3L4FM	Layer 3 and Layer 4 Filter Number Matched These bits indicate the number of the Layer 3 and Layer 4 Filter that matched the received packet: ■ 000: Filter 0 ■ 001: Filter 1 ■ 010: Filter 2 ■ 011: Filter 3 ■ 100: Filter 4 ■ 101: Filter 5 ■ 110: Filter 6 ■ 111: Filter 7 This field is valid only when Bit 28 or Bit 27 is set high. When more than one filter matches, these bits give the number of lowest filter. Note: This status is not available when Flexible RX Parser is enabled.
28	L4FM	Layer 4 Filter Match When this bit is set, it indicates that the received packet matches one of the enabled Layer 4 Port Number fields. This status is given only when one of the following conditions is true: ■ Layer 3 fields are not enabled and all enabled Layer 4 fields match ■ All enabled Layer 3 and Layer 4 filter fields match When more than one filter matches, this bit gives the layer 4 filter status of filter indicated by Bits[31:29]. Note: This status is not available when Flexible RX Parser is enabled.

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Bit	Name	Description
27	L3FM	Layer 3 Filter Match When this bit is set, it indicates that the received packet matches one of the enabled Layer 3 IP Address fields. This status is given only when one of the following conditions is true: ■ All enabled Layer 3 fields match and all enabled Layer 4 fields are bypassed ■ All enabled filter fields match When more than one filter matches, this bit gives the layer 3 filter status of filter indicated by Bits[31:29]. Note: This status is not available when Flexible RX Parser is enabled.
26:19	MADRM	MAC Address Match or Hash Value When the HF bit is reset, this field contains the MAC address register number that matched the Destination address of the received packet. This field is valid only if the DAF bit is reset. When the HF bit is set, this field contains the hash value computed by the MAC. A packet passes the hash filter when the bit corresponding to the hash value is set in the hash filter register. Note: This status is not available when Flexible RX Parser is enabled.
18	HF	Hash Filter Status When this bit is set, it indicates that the packet passed the MAC address hash filter. Bits[26:19] indicate the hashvalue. Note: This status is not available when Flexible RX Parser is enabled.
17	DAF/RXPI	Destination Address Filter Fail When Flexible RX Parser is disabled, and this bit is set, it indicates that the packet failed the DA Filter in the MAC. When Flexible RX Parser is enabled, this bit is set to indicate that the packet parsing is incomplete (RXPI) due to ECC error. Note: When this bit is set, ES bit of RDES3 is also set.
16	SAF/RXPD	SA Address Filter Fail When Flexible RX Parser is disabled, and this bit is set, it indicates that the packet failed the SA Filter in the MAC. When Flexible RX Parser is enabled, this bit is set to indicate that the packet is dropped (RXPD) by the parser. Note: When this bit is set, ES bit of RDES3 is also set.
15	OTS	VLAN Filter Status When set, this bit indicates that the VLAN Tag of the received packed passed the VLAN filter. This bit is valid only when DWC_GMAC_ERVFE is not enabled. If DWC_GMAC_ERVFE is enabled, the bit is redefined as Outer VLAN Tag Filter Status (OTS). This bit is valid for both Single and Double VLAN Tagged frames.
14	ITS	Inner VLAN Tag Filter Status (ITS) This bit is valid only when DWC_GMAC_ERVFE is enabled. This bit is valid only for Double VLAN Tagged frames, when Double VLAN Processing is enabled.

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Bit	Name	Description
		For more information, see the Filter Status topic.
13:11	Rsvd	Reserved
10	ARPNR	ARP Reply Not Generated When this bit is set, it indicates that the MAC did not generate the ARP Reply for received ARP Request packet. This bit is set when the MAC is busy transmitting ARP reply to earlier ARP request (only one ARP request is processed at a time). This bit is reserved when the Enable IPv4 ARP Offload option is not selected.
9:0	HL	L3/L4 Header Length This field contains the length of the header of the packet split by the MAC at L3 or L4 header. boundary as identified by the MAC receiver. This field is valid only when the first descriptor bit is set (FD = 1). The header data is written to the Buffer 1 address of corresponding descriptor. If header length is zero, this field is not valid. It implies that the MAC did not identify and split the header. This field is valid when the Enable Split Header Feature option is selected.

Table 42-23 TDES3 Normal Descriptor(Write-Back Format)

Bit	Name	Description
31	OWN	Own Bit When this bit is set, it indicates that the GMAC DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit when either of the following conditions is true: ■ The DMA completes the packet reception ■ The buffers associated with the descriptor are full
30	CTXT	Receive Context Descriptor When this bit is set, it indicates that the current descriptor is a context type descriptor. The DMA writes 1'b0 to this bit for normal receive descriptor. When CTXT and FD bits are used together, {CTXT, FD} ■ 2’b00: Intermediate Descriptor ■ 2’b01: First Descriptor ■ 2’b10: Reserved ■ 2’b11: Descriptor Error (due to all 1s) Note: When Descriptor Error occurs, the Receive DMA closes the receive descriptor indicating Descriptor Error. This receive descriptor is skipped and the buffer addresses are not used to write the packet data Receive DMA will set the CDE bit in DMA_CH#_Status register but not the RI bit even when IOC is set, as this is not marked as last receive descriptor for the packet. The subsequent valid receive descriptor is used to write the packet data.
29	FD	First Descriptor When this bit is set, it indicates that this descriptor contains the first buffer of the packet. If the size of the first buffer is 0, the second buffer contains the beginning of the packet. If the size of the second buffer is also 0, the next descriptor contains the beginning of the packet. See the CTXT bit description for details of using the CTXT bit and FD bit together.
28	LD	Last Descriptor

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Bit	Name	Description
		When this bit is set, it indicates that the buffers to which this descriptor is pointing are the last buffers of the packet.
27	RS2V	Receive Status RDES2 Valid When this bit is set, it indicates that the status in RDES2 is valid and it is written by the DMA. This bit is valid only when the LD bit of RDES3 is set.
26	RS1V	Receive Status RDES1 Valid When this bit is set, it indicates that the status in RDES1 is valid and it is written by the DMA. This bit is valid only when the LD bit of RDES3 is set.
25	RS0V	Receive Status RDES0 Valid When this bit is set, it indicates that the status in RDES0 is valid and it is written by the DMA. This bit is valid only when the LD bit of RDES3 is set.
24	CE	CRC Error When this bit is set, it indicates that a Cyclic Redundancy Check (CRC) Error occurred on the received packet. This field is valid only when the LD bit of RDES3 is set.
23	GP	Giant Packet When this bit is set, it indicates that the packet length exceeds the specified maximum Ethernet size of 1518, 1522, or 2000 bytes (9018 or 9022 bytes if jumbo packet enable is set). Note: Giant packet indicates only the packet length. It does not cause any packet truncation.
22	RWT	Receive Watchdog Timeout When this bit is set, it indicates that the Receive Watchdog Timer has expired while receiving the current packet. The current packet is truncated after watchdog timeout.
21	OE	Overflow Error When this bit is set, it indicates that the received packet is damaged because of buffer overflow in Rx FIFO. Note: This bit is set only when the DMA transfers a partial packet to the application. This happens only when the Rx FIFO is operating in the threshold mode. In thestore-and-forward mode, all partial packets are dropped completely in Rx FIFO.
20	RE	Receive Error When this bit is set, it indicates that the gmii_rxer_i signal is asserted while the gmii_rxdv_i signal is asserted during packet reception. This error also includes carrier extension error in the GMII and half-duplex mode. Error can be of less or no extension, or error (rxd!= 0f) during extension.
19	DE	Dribble Bit Error When this bit is set, it indicates that the received packet has a non-integer multiple of bytes (odd nibbles). This bit is valid only in the MII Mode.
18:16	LT	Length/Type Field This field indicates if the packet received is a length packet or a type packet. The encoding of the 3 bits is as follows: ■ 3'b000: The packet is a length packet ■ 3'b001: The packet is a type packet.

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Bit	Name	Description
		■ 3'b011: The packet is a ARP Request packet type ■ 3'b100: The packet is a type packet with VLAN Tag ■ 3'b101: The packet is a type packet with Double VLAN Tag ■ 3'b110: The packet is a MAC Control packet type ■ 3'b111: The packet is a OAM packet type ■ 3'b010: Reserved
15	ES	Error Summary When this bit is set, it indicates the logical OR of the following bits: ■ RDES3[24]: CRC Error ■ RDES3[19]: Dribble Error ■ RDES3[20]: Receive Error ■ RDES3[22]: Watchdog Timeout ■ RDES3[21]: Overflow Error ■ RDES3[23]: Giant Packet ■ RDES2[17]: Destination Address Filter Fail, when Flexible RX Parser is enabled ■ RDES2[16]: SA Address Filter Fail, when Flexible RX Parser is enabled This field is valid only when the LD bit of RDES3 is set.
14	PL	Packet Length These bits indicate the byte length of the received packet that was transferred to system memory (including CRC). This field is valid when the LD bit of RDES3 is set and Overflow Error bits are reset. The packet length also includes the two bytes appended to the Ethernet packet when IP checksum calculation is enabled and the received packet is not a MAC control packet. This field is valid when the LD bit of RDES3 is set. When the Last Descriptor and Error Summary bits are not set, this field indicates the accumulated number of bytes that have been transferred for the current packet.

42.6.9 GMAC Receive Context Descriptor

This descriptor is read-only for the application. Only the DMA can write to this descriptor. The context descriptor provides information about the extended status related to the last received packet. The Bit 30 of RDES3 indicates the context type descriptor.

Table 42-24 TDES0 Context Descriptor

Bit	Name	Description
31:0	RSTL	Receive Packet Timestamp Low The DMA updates this field with least significant 32 bits of the timestamp captured for corresponding Receive packet. When this field and the RTSH field of RDES1 show all-ones value, the timestamp must be considered as corrupt.

Table 42-25 TDES1 Context Descriptor

Bit	Name	Description
31:0	RSTH	Receive Packet Timestamp High The DMA updates this field with most significant 32 bits of the timestamp captured for correspondingreceive packet. When this field and the RTSL field of RDES0 show all-ones value, the timestamp must be considered as corrupt.

Table 42-26 TDES2 Context Descriptor

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Bit	Name	Description
31:0	Rsvd	Reserved

Table 42-27 TDES3 Context Descriptor

Bit	Name	Description
31	OWN	Own Bit When this bit is set, it indicates that the DMA owns the descriptor. When this bit is reset, it indicates that the application owns the descriptor. The DMA clears this bit when either of the following conditions is true: ■ The DMA completes the packet reception ■ The buffers associated with the descriptor are full
30	CTXT	Receive Context Descriptor When this bit is set, it indicates that the current descriptor is a context descriptor. The DMA writes 1'b1 to this bit for context descriptor. DMA writes 2'b11 to indicate adescriptor error due to all 1s. When CTXT and DE bits are used together, {CTXT, DE} ■ 2'b00: Reserved ■ 2'b01: Reserved ■ 2'b10: Context Descriptor ■ 2'b11: Descriptor Error Note: When Descriptor Error occurs, the Receive DMA closes the receive descriptor indicating Descriptor Error. This receive descriptor is skipped and the buffer addresses are not used to write the packet data Receive DMA will set the CDE bit in DMA_CH#_Status register but not the RI bit even when IOC is set, as this is not marked as last receive descriptor for the packet. The subsequent valid receive descriptor is used to write the packet data.
29	DE	Descriptor Error See the CTXT bit description for details of using theDE bit along with CTXT bit.
28:0	Rsvd	Reserved

42.6.10 GMAC Programming Guide

42.6.10.1 Initializing DMA

Complete the following steps to initialize the DMA:

1. Provide a software reset. This resets all of the MAC internal registers and logic (bit-0 of DMA_Mode).
2. Wait for the completion of the reset process (poll bit 0 of the DMA_Mode, which is only cleared after the reset operation is completed).
3. Program the following fields to initialize the DMA_SysBus_Mode register:

a. AAL

b. Fixed burst or undefined burst

c. Burst mode values in case of AHB bus interface, OSR_LMT in case of AXI bus interface.

d. If fixed length value is enabled, select the maximum burst length possible on the AXI Bus (bits [7:1])

4. Create a descriptor list for transmit and receive. In addition, ensure that the descriptors are owned by DMA (set bit 31 of descriptor TDES3/RDES3). For more information about descriptors, see section "Descriptors".
5. Program the Transmit and Receive Ring length registers (DMA_CH(#i)_TxDesc_Ring_Length (for i = 0; i <= DWC_GMAC_NUM_DMA_TX_CH-1) and DMA_CH(#i)_RxDesc_Ring_Length (for i = 0; i <= DWC_GMAC_NUM_DMA_RX_CH-1)). The ring length programmed must be at least 4.
6. Initialize receive and transmit descriptor list address with the base address of the transmit and receive descriptor (DMA_CH(#i)_TxDesc_List_Address (for i = 0; i <= DWC_GMAC_NUM_DMA_TX_CH-1), DMA_CH(#i)_RxDesc_List_Address (for i = 0; i <=

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DWC_GMAC_NUM_DMA_RX_CH-1)). Also, program transmit and receive tail pointer registers indicating to the DMA about the available descriptors (DMA_CH(#i)_TxDesc_Tail_Pointer (for i = 0; i <= DWC_GMAC_NUM_DMA_TX_CH-1) and DMA_CH(#i)_RxDesc_Tail_Pointer (for i = 0; i <= DWC_GMAC_NUM_DMA_RX_CH-1)).
7. Program the settings of the following registers for the parameters like maximum burst-length (PBL) initiated by DMA, descriptor skip lengths, OSP in case of TxDMA, RBSZ in case of RxDMA, and so on:

- DMA_CH(#i)_Control (for i = 0; i <= DWC_GMAC_NUM_DMA_TX_CH-1)
- DMA_CH(#i)_TX_Control (for i = 0; i <= DWC_GMAC_NUM_DMA_TX_CH-1)
- DMA_CH(#i)_RX_Control (for i = 0; i <= DWC_GMAC_NUM_DMA_RX_CH-1)

8. Enable the interrupts by programming the DMA_CH(#i)_Interrupt_Enable (for i = 0; i <=
DWC_GMAC_NUM_DMA_TX_CH-1) register.
9. Start the Receive and Transmit DMAs by setting SR (bit 0) of theDMA_CH(#i)_RX_Control (for i = 0; i <= DWC_GMAC_NUM_DMA_RX_CH-1) and ST (bit 0) of the DMA_CH(#i)_TX_Control (for i = 0; i <= DWC_GMAC_NUM_DMA_TX_CH-1)register.
10. Repeat steps 4 to 9 for all the Tx DMA and Rx DMA channels selected in the hardware.

42.6.10.2 Initializing MTL Registers

The Transaction Layer (MTL) registers must be initialized to establish the transmit and receive operating modes and commands.
Complete the following steps to initialize the MTL registers:
1. Program the Tx Scheduling (SCHALG) and Receive Arbitration Algorithm (RAA) fields in MTL_Operation_Mode to initialize the MTL operation in case of multiple Tx and Rx queues.
2. Program the Receive Queue to DMA mapping in MTL_RxQ_DMA_Map0 andMTL_RxQ_DMA_Map1 registers.
3. Program the following fields to initialize the mode of operation in the MTL_TxQ0_Operation_Mode register.
a. Transmit Store And Forward (TSF) or Transmit Threshold Control (TTC) in case of threshold mode
b. Transmit Queue Enable (TXQEN) to value 2'b10 to enable Transmit Queue0
c. Transmit Queue Size (TQS)
4. Program the following fields to initialize the mode of operation in the MTL_RxQ0_Operation_Mode register:
a. Receive Store and Forward (RSF) or RTC in case of Threshold mode
b. Flow Control Activation and De-activation thresholds for MTL Receive FIFO (RFA and RFD)
c. Error Packet and undersized good Packet forwarding enable (FEP and FUP)
d. Receive Queue Size (RQS)
5. Repeat previous two steps for all MTL Tx and Rx queues selected in the configuration.

42.6.10.3 Initializing MAC

The MAC configuration registers establish the operating mode of the MAC. These registers must be initialized before initializing the DMA.
The following MAC Initialization operations can be performed after DMA initialization. If the MAC initialization is completed before the DMA is configured, enable the MAC receiver (last step in the following sequence) only after the DMA is active. Otherwise, received frames fill the Rx FIFO and overflow.
1. Provide the MAC address registers: MAC_Address0_High and MAC_Address0_Low. If more than one MAC address is enabled in your configuration, program the MAC addresses appropriately.
2. Program the following fields to set the appropriate filters for the incoming frames in the MAC_Packet_Filter register:
a. Receive All
b. Promiscuous mode
c. Hash or Perfect Filter
d. Unicast, multicast, broadcast, and control frames filter settings

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3. Program the following fields for proper flow control in the MAC_Q0_Tx_Flow_Ctrlregister:
a. Pause time and other Pause frame control bits
b. Transmit Flow control bits
c. Flow Control Busy
4. Program the MAC_Interrupt_Enable register, as required, and if applicable, for your configuration.
5. Program the appropriate fields in the MAC_Configuration register. For ex: Inter-packet gap while transmission and jabber disable.
6. Set bit 0 and 1 in MAC_Configuration registers to start the MAC transmitter and receiver.

42.6.10.4 Performing Normal Receive and Transmit Operation

During normal operation of the GMAC, normal and transmit interrupts are read, descriptors polled, the DMA is suspended (if it does not own descriptors), and values of current host transmitter or receiver descriptor pointers are read for debugging.
For normal operation, complete the following steps:
1. For normal transmit and receive interrupts, read the interrupt status. Then, poll the descriptors, reading the status of the descriptor owned by the Host (either transmit or receive).
2. Set appropriate values for the descriptors, ensuring that transmit and receive descriptors are owned by the DMA to resume the transmission and reception of data.
3. If the descriptors are not owned by the DMA (or no descriptor is available), the DMA goes into SUSPEND state. The transmission or reception can be resumed by freeing the descriptors and writing the descriptor tail pointer to Tx/Rx tail pointer register (DMA_CH[n]_TxDesc_Tail_Pointer and DMA_CH[n]_RxDesc_Tail_Pointer).
4. The values of the current host transmitter or receiver descriptor address pointer can be read for the debug process (DMA_CH[n]_Current_App_TxDesc andDMA_CH[n]_Current_App_RxDesc).
5. The values of the current host transmit buffer address pointer and receive buffer address pointer can be read for the debug process (Register DMA_CH[n]_Current_App_TxBuffer and DMA_CH[n]_Current_App_RxBuffer)

42.6.10.5 Stopping and Starting Transmission

Complete the following steps to pause the transmission for some time.
1. Disable the Transmit DMA (if applicable) by clearing Bit 0 (ST) of DMA_CH(#i)_TX_Control (for i = 0; i <= DWC_GMAC_NUM_DMA_TX_CH-1) Register.
2. Wait for any previous frame transmissions to complete. You can check this by reading the appropriate bits of MTL_TxQ0_Debug Register (TRCSTS is not 01 and TXQSTS=0).
3. Disable the MAC transmitter and MAC receiver by clearing Bit (RE) and Bit 1(TE) of the MAC_Configuration Register.
4. Disable the Receive DMA (if applicable), after making sure that the data in the Rx FIFO is transferred to the system memory (by reading the appropriate bits of MTL_TxQ0_Debug Register, PRXQ=0 and RXQSTS=00).
5. Make sure that both Tx Queue and Rx Queue are empty (TXQSTS is 0 inMTL_TxQ0_Debug Register and RXQSTS is 0 in MTL_RxQ0_Debug Register).
6. To restart the operation, first start the DMAs, and then enable the MAC Transmitter and Receiver.

42.6.10.6 Initialization Guidelines for System Time Generation

You can enable the timestamp feature by setting Bit 0 of the MAC_Timestamp_Control Register. However, it is essential that the timestamp counter be initialized after this bit is set. Complete the following steps during GMAC initialization:
1. Mask the Timestamp Trigger interrupt by clearing the bit 16 of MAC_Interrupt_Enable Register.
2. Set Bit 0 of MAC_Timestamp_Control Register to enable timestamping.
3. Program MAC_Sub_Second_Increment Register based on the PTP clock frequency.
4. If you are using the Fine Correction approach, program MAC_Timestamp_Addend and set Bit 5 of MAC_Timestamp_Control Register.
5. Poll the MAC_Timestamp_Control Register until Bit 5 is cleared.

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6. Program Bit 1 of MAC_Timestamp_Control Register to select the Fine Update method (if required).
7. Program MAC_System_Time_Seconds_Update Register andMAC_System_Time_Nanoseconds_Update Register with the appropriate time value.
8. Set Bit 2 in MAC_Timestamp_Control Register.
The timestamp counter starts operation as soon as it is initialized with the value written in the Timestamp Update registers. If one-step timestamping is enabled
a. To enable one-step timestamping, program Bit 27 of the TDES3 Context Descriptor.
b. Program registers MAC_Timestamp_Ingress_Asym_Corr andMAC_Timestamp_Egress_Asym_Corr to update the correction field in PDelay_Req PTP messages.
9. Enable the MAC receiver and transmitter for proper timestamping.

42.6.10.7 Coarse Correction Method

To synchronize or update the system time in one process (coarse correction method), complete the following steps:
1. Set the offset (positive or negative) in the Timestamp Updateregisters(MAC_System_Time_Seconds_Update andMAC_System_Time_Nanoseconds_Update).
2. Set Bit 3 (TSUPDT) of MAC_Timestamp_Control Register. The value in the Timestamp Update registers is added to or subtracted from the system time when the TSUPDT bit is cleared.

42.6.10.8 Programming Guidelines for TSO

The TCP Segmentation Offload (TSO) engine is used to offload the TCP segmentation functions to the hardware. To program the TSO, set the TSE bit to enable TCP packet segmentation, and program descriptor fields to enable TSO for the current packet.
Complete the following steps to program TSO:
1. Program the TSE bit of corresponding DMA_CH[n]_Tx_Control register to enable TCP packet segmentation in that DMA.
2. In addition to the normal transfer descriptor setting, the following descriptor fields must be programmed to enable TSO for the current packet:
a. Enable TSE in Bit 18 of TDES3
b. Program the length of the un-segmented TCP/IP packet payload in bits [17:0] of TDES3 and the TCP header in bits [22:19] of TDES3.
c. Program the maximum size of the segment in MSS of DMA_CH[n]_Control register or MSS in the context descriptor. If MSS field is programmed in both DMA_CH[n]_Control register and in the context descriptor, the latest software programmed sequence is considered.
3. The header of the unsegmented TCP/IP packet should be in Buffer 1 of the first descriptor and this buffer must not hold any payload bytes. The payload is allocated to Buffer 2 and the buffers of the subsequent descriptors.

42.6.11 GMAC Clock Architecture

In RMII mode, reference clock and TX/RX clock can be from CRU or external OSC as following figure.

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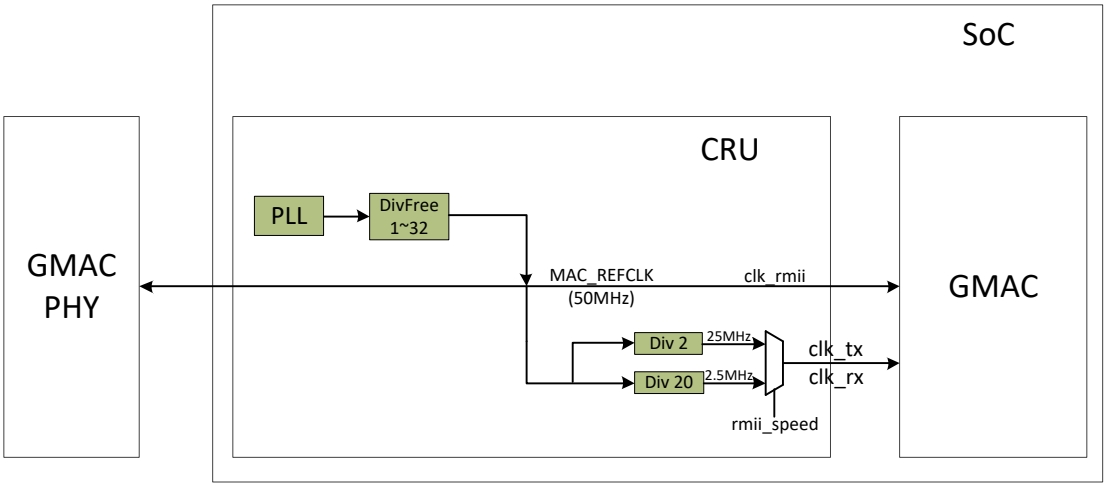

Fig. 42-11 RMII Clock Architecture When Clock Source From CRU

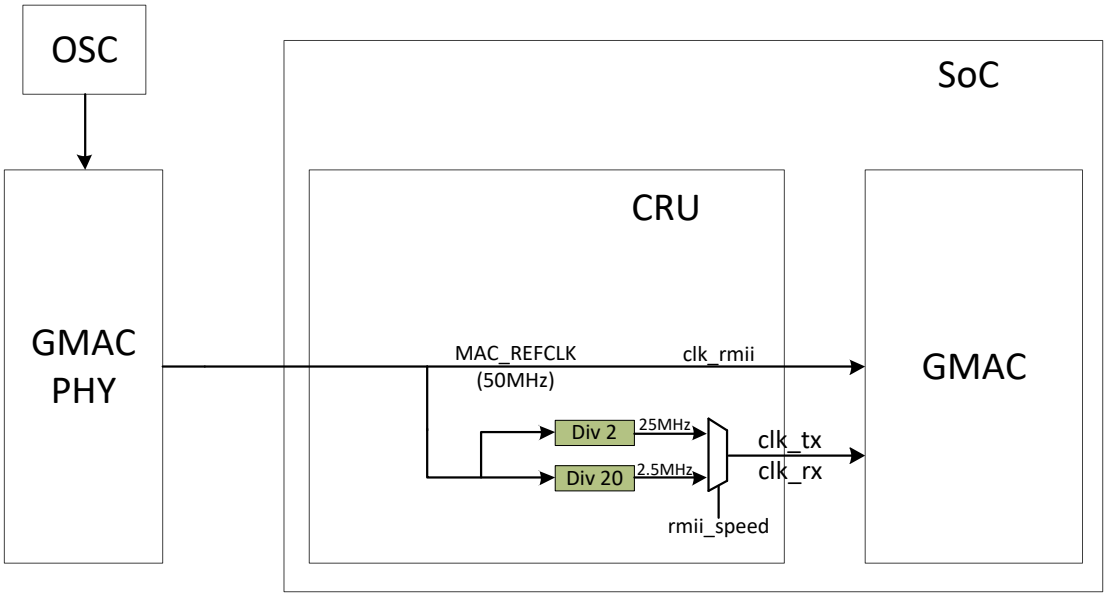

Fig. 42-12 RMII Clock Architecture When Clock Source From External OSC

In RGMII mode, clock architecture only supports that TX clock source is from CRU as following figure. In order to dynamically adjust the timing between TX/RX clocks with data, delayline is integrated in TX and RX clock path.

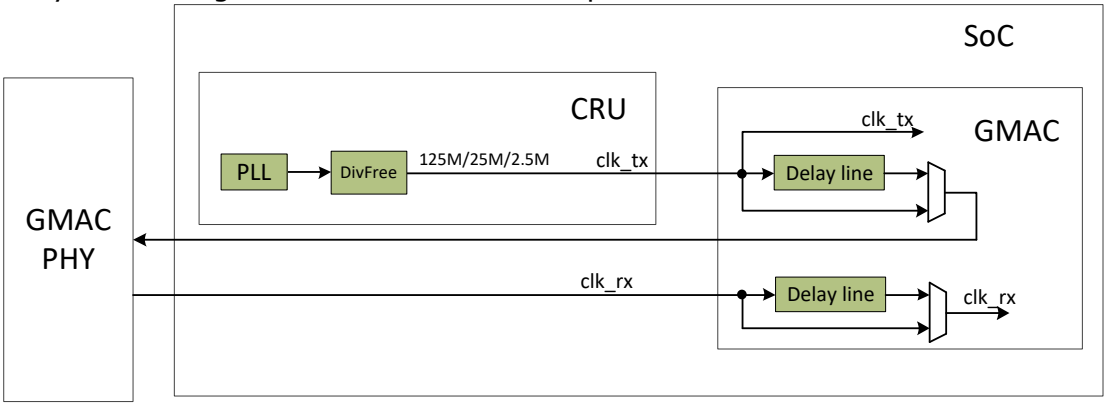

Fig. 42-13 RGMII Clock Architecture When Clock Source From CRU

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Chapter 43 FEPHY

43.1 Overview

The FEPHY is a low-power Ethernet Physical Layer transceiver with variable I/O voltage. The FEPHY works in both 10Base-T and 100Base-TX Fast Ethernet modes, and is fully compliant with the IEEE 802.3/802.3u standards.

FEPHY supports the following features:

- Integrated IEEE 802.3/802.3u compliant 10/100Mbps Ethernet PHY
- Support 10BASE-T/100BASE-TX
- Support both full and half-duplex for either 10 or 100 Mbps data rate
- Support Auto-Negotiation
- Support Auto-MDIX
- Support Wake on LAN (WoL)
- Support Energy Efficient Ethernet, Low Power Idle (EEE, LPI)
- Support Reduced Media Independent Interface (RMII)
- Support Serial Management Interface (SMI)
- Support 32 bits APB interface to access register bank
- Support LED status indicators
- Support that the four transmission pads to be used as GPIO
- Support 24/50 MHz input reference clock, and 50 MHz output clock
- Support P/N switching within differential signal groups

43.2 Block Diagram

FEPHY is functionally achieved by two parts of circuit, analog and digital.

Digital part is comprised of:

- clk_gen

The clk_gen module generate clocks of different phase and frequency to functional module of digital circuit, and its source clock from reference clock or AFE PLL (Analog Front End Phase Locked Loop).

- apb_slave

The APB interface could be configured to access internal register bank, and its data bus width is 32 bits.

- ten100_m

This module achieves function of SMI interface and physical coding layer of 10BASE-T and 100BASE-TX.

- dsp_m

The channel equalization and signal recovery of 100Mbps RX path are achieved.

- xtxd2xmt

This module serializes the parallel TX data, and encodes in Multi-Level Transmit 3 (MLT-3) format.

- analog_if

The analog interface drives the AFE according to the TX data.

- io_buffer

The io_buffer is added for RMII sampling sequence.

- i_ephy_sigdet_hysteresis

The energy detect hysteresis module in LPI mode.

- i_ephy_wol

Wake on LAN is achieved in this module.

Analog part includes GPIO and FEPHY_AFE, and the PAD could be used ad GPIO when FEPHY_AFE is idle. The FEPHY_AFE is comprised of:

- CB

The common block modules receive the control signal from digital circuit, and controls the working of other sub-modules.

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- TX calibration

The voltage of TX PAD is calibrated to 2.0 V in 10 Mbps mode and 1.0 V in 100 Mbps mode.

- TX

TX PAD driver.

- PLL

The phase lock loop is used to generate the clocks to other AFE sub-modules and digital circuits, and its source clock is reference clock.

- CMFB

The common mode feedback is to maintain the stability and accuracy of RX signals.

- CMFB_X

The common mode feedback module in MDIX mode.

- DAC

The DAC output could compensate the baseline wander.

- CTLE

The continuous time linear equalizer in RX path for data transmission over long distance or through channel with significant signal degradation.

- LPF

The low pass filter for anti-aliasing is to achieve better signal integrity.

- PGA

The programmable gain amplifier could be configured to adjust the RX signal to the best work range of the ADC.

- ADC

The analog to digital converter is allocated in RX path to sample data in 100 Mbps.

- Squelch

The squelch module is used to sample signal in 10 Mbps.

- Squelch_X

The squelch module in MDIX mode.

- Signal detect

The signal detect is used to receive data in LPI mode.

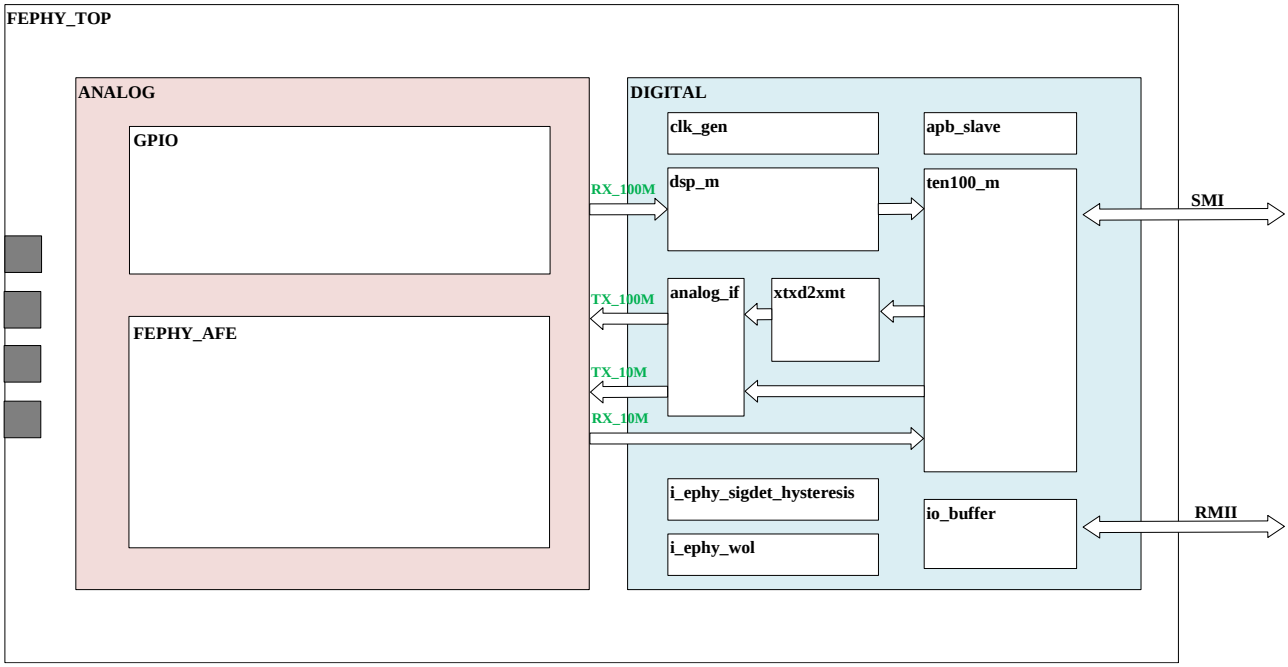

Fig. 43-1 FEPHY Block Diagram

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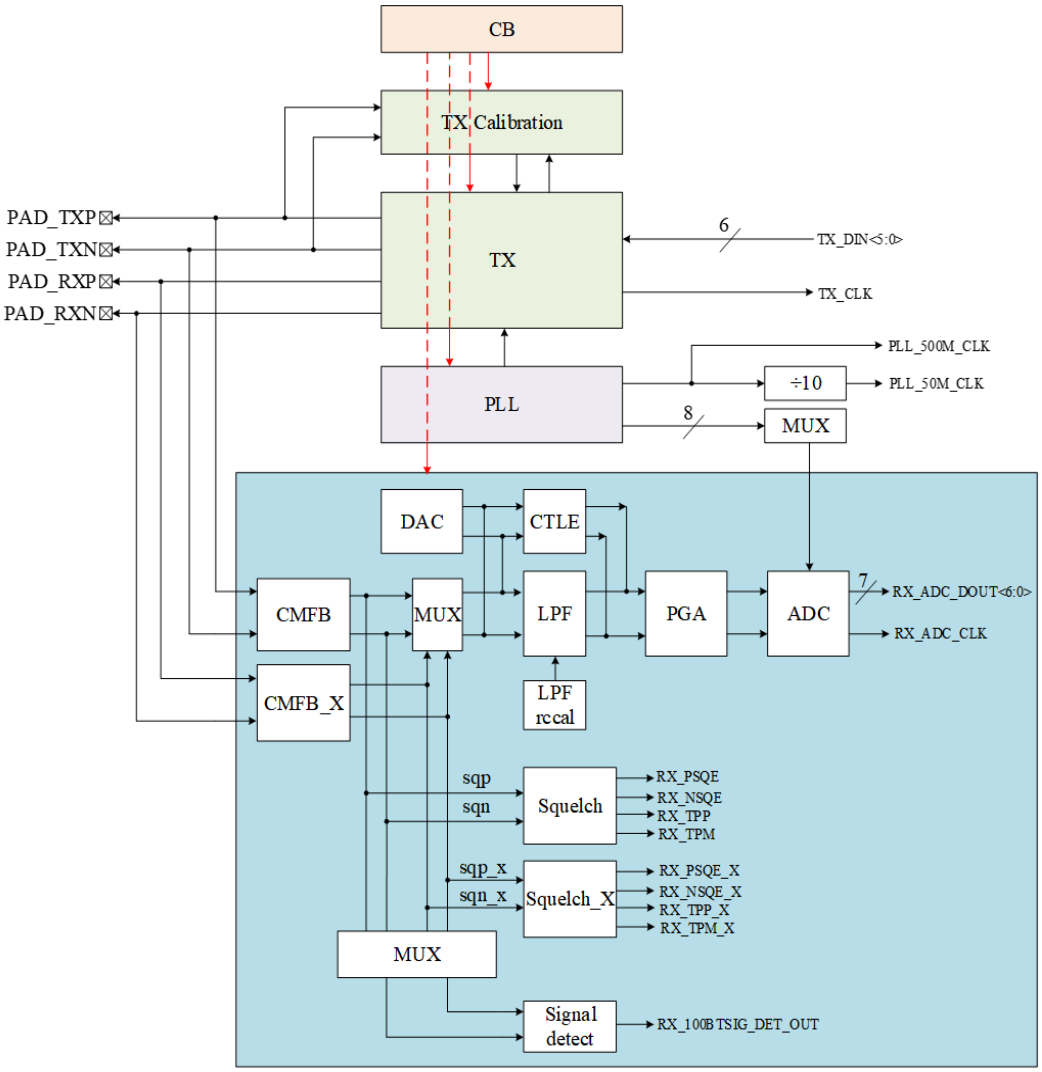

Fig. 43-2 FEPHY_AFE Block Diagram

43.3 Function Description

43.3.1 Clock

In RMII mode, reference clock "clk_in" can be from CRU (Clock Reset Unit, 50MHz) or external OSC (Oscillator, 24MHz), by configuring VICRU_VI_CLKSEL_CON01[1], and the corresponding GRF (GRF_VI_MACPHY_CON2[11:9]) need to be configured for the PLL inside the AFE, which could generate the clocks to other modules based on the input reference clock.

The frequency of SMI clock "MDC" should be less than 2.5 MHz.

43.3.2 Reset

Power down reset is automatically activated when the PHY comes out of power down mode. The internal power down reset is extended by 256us after exiting the power down mode to allow the PLL to stabilize before the logic is released from reset.

Hardware reset is controlled by CRU. If the hardware reset is driven by an external source, it should be held low for at least 100us to ensure that the core is properly reset.

Software reset is activated by writing a register. This signal is self-clearing. After the register writing, internal logic extends the reset by 256 us to allow PLL stabilization before releasing the logic from reset.

43.3.3 Serial Management Interface

The SMI is a simple, two-wire interface to connect a management entity and a managed PHY for the purposes of controlling the PHY and gathering status from the PHY. The SMI

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includes two signals, MDC (management data clock) and MDIO (management data input/output).

MDC is sourced by the MAC to the FEPHY as the timing reference for transfer of information on the MDIO signal. The minimum period for MDC shall be 400 ns.

MDIO is a bidirectional signal between the FEPHY and the MAC. It is used to transfer control information and status. Control information is driven by the MAC synchronously with respect to MDC and is sampled synchronously by the PHY. Status information is driven by the PHY synchronously with respect to MDC and is sampled synchronously by the MAC. MDIO shall be driven through three-state circuits that enable either the MAC or the PHY to drive the signal.

43.3.3.1 Signal timing characteristics

MDIO is a bidirectional signal that can be sourced by the MAC or the FEPHY. When the MAC sources the MDIO signal, the MAC shall provide a minimum of 10 ns of setup time and a minimum of 10 ns of hold time referenced to the rising edge of MDC, as shown in figure below.

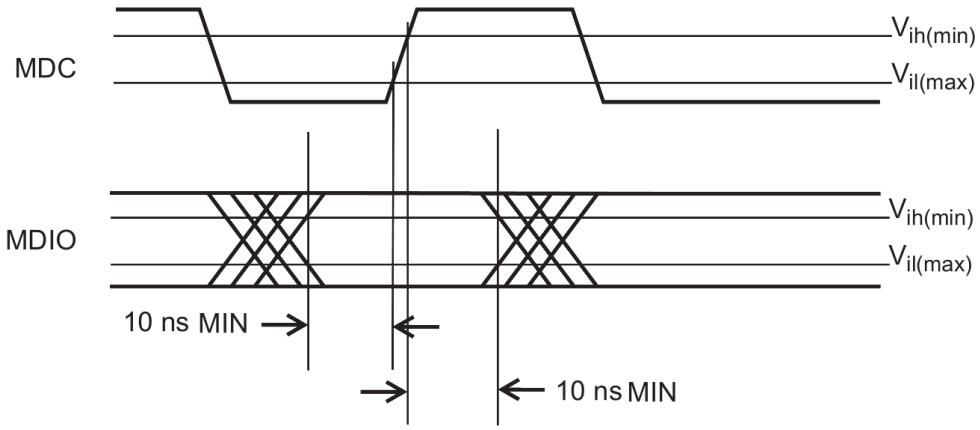

Fig. 43-3 MDIO sourced by the MAC

When the MDIO signal is sourced by the PHY, it is sampled by the MAC synchronously with respect to the rising edge of MDC. The clock to output delay from the FEPHY, shall be a minimum of 0 ns, and a maximum of 300 ns, as shown in figure below.

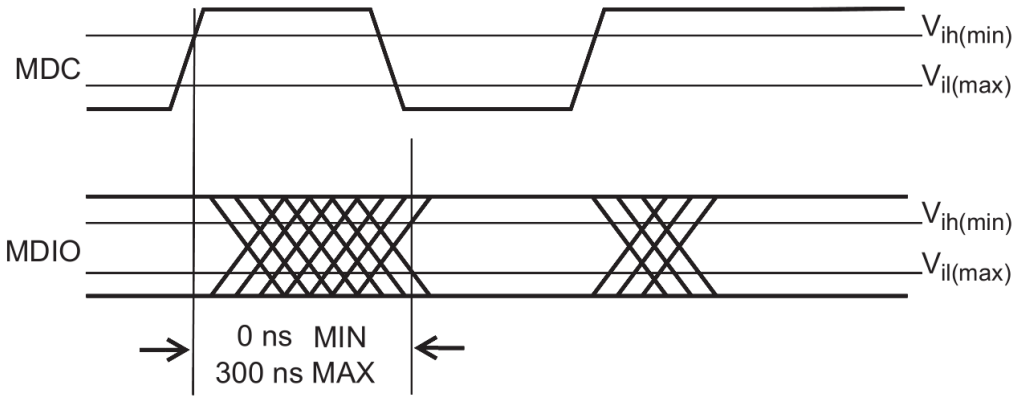

Fig. 43-4 MDIO sourced by the FEPHY

43.3.3.2 SMI Package Format

The management frame structure is shown in the table below, and the order of bit transmission shall be from left to right.

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Table 43-1 SMI Management Package Format

	Management frame fields							
	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
READ	1...1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
WRITE	1...1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

The IDLE condition on MDIO is a high-impedance state. All three state drivers shall be disabled and the FEPHY's pull-up resistor will pull the MDIO line to a logic one.

The PRE (preamble) of a sequence of 32 contiguous logic one bits on MDIO is sent by the MAC at the beginning of each transaction, with 32 corresponding cycles on MDC to provide the FEPHY with a pattern that it can use to establish synchronization.

The ST (start of frame) is indicated by a <01> pattern. This pattern assures transitions from the default logic one line state to zero and back to one.

The OP (operation code) for a read transaction is <10>, while the operation code for a write transaction is <01>.

The PHYAD (PHY Address) is five bits, allowing 32 unique PHY addresses.

The ST (start of frame) is five bits, allowing 32 individual registers to be addressed within each PHY. The first Register Address bit transmitted and received is the MSB of the address.

The TA (turnaround) time is a 2 bit time spacing between the Register Address field and the Data field of a management frame to avoid contention during a read transaction. For a read transaction, both the MAC and the FEPHY shall remain in a high-impedance state for the first bit time of the turnaround. The FEPHY shall drive a zero bit during the second bit time of the turnaround of a read transaction. During a write transaction, the MAC shall drive a one bit for the first bit time of the turnaround and a zero bit for the second bit time of the turnaround.

The DATA (data) field is 16 bits. The first data bit transmitted and received shall be bit 15 of the register being addressed.

43.3.3.3 Indirect register bank

To address more than 32 address space, indirect addressing scheme is used. In addition to SMI direct register bank, there are six other indirect register bank, and they shall be accessed via TST_CNTL, TST_READ1, TST_READ2, TST_WRITE. The access procedure of the indirect register banks could be referred in the Application Notes.

43.3.3.4 APB Interface

To conveniently control the FEPHY register bank, an APB slave logic is added. And the system could access the registers through APB when the APB select signal (VI_GRF_RKMACPHY_CON1[22]) is enabled. When APB select signal is asserted, MDIO access is invalid.Meanwhile, the APB interface also provides configurations for internal GRF.

43.3.4 Reduced Media Independent Interface

RMII (Reduced Media Independent Interface) is a low pin count specification between the MAC and the FEPHY.

43.3.4.1 RMII Signals Definition

The RMII signals is shown as below table.

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Table 43-2 SMI Management Package Format

Signal Name	Direction (with respect to the PHY)	Direction (with respect to the MAC)	Use
REF_CLK	Input	Input or Output	Synchronous clock reference for receive, transmit and control interface
CRS_DV	Output	Input	Carrier Sense/Receive Data Valid
RXD[1:0]	Output	Input	Receive Data
TX_EN	Input	Output	Transmit Enable
TXD[1:0]	Input	Output	Transmit Data
RX_ER	Output	Input (Not required)	Receive Error

REF_CLK is a continuous clock that provides the timing reference for CRS_DV, RXD[1:0], TX_EN, TXD[1:0], and RX_ER. REF_CLK is sourced by the MAC or an external source. The REF_CLK frequency shall be 50 MHz +/- 50 ppm with a duty cycle between 35% and 65% inclusive.

CRS_DV (Carrier Sense/Receive Data Valid) shall be asserted by the PHY when the receive medium is not idle. CRS_DV may toggle at 25MHz starting on a nibble boundary if bits accumulate due to the difference between local and recovered clock.

RXD[1:0] (Receive Data) RXD[1:0] shall transition synchronously to REF_CLK. For each clock period in which CRS_DV is asserted, RXD[1:0] transfers two bits of recovered data from the PHY. If False Carrier is detected , then RXD[1:0] shall be "10" until the end of the receive event. As the REF_CLK frequency is 10 times the data rate in 10Mbps mode the value on RXD[1:0] shall be valid such that RXD[1:0] may be sampled every 10th cycle.

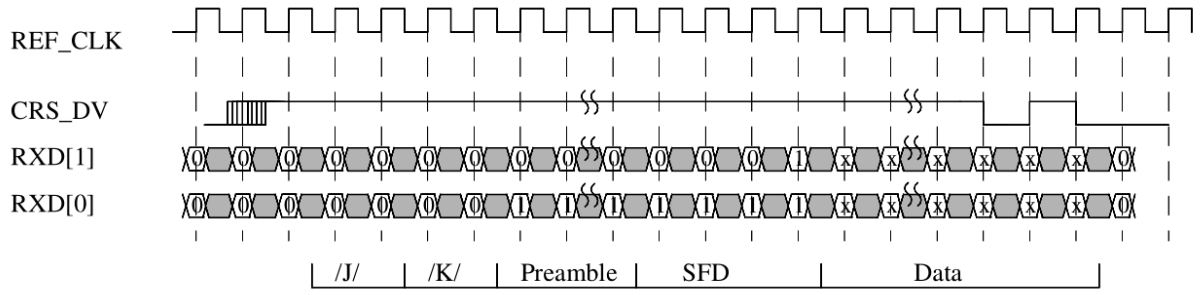

Fig. 43-5 RMII 100 Mbps Reception

TX_EN (Transmit Enable) indicates that the MAC is presenting di-bits on TXD[1:0] for transmission. TX_EN shall be asserted synchronously with the first nibble of the preamble and shall remain asserted while all di-bits to be transmitted are presented. TX_EN shall be negated prior to the first REF_CLK rising edge following the final di-bit of a frame. TX_EN shall transition synchronously with respect to REF_CLK.

TXD[1:0] (Transmit Data) shall transition synchronously with respect to REF_CLK. When TX_EN is asserted, TXD[1:0] are accepted for transmission by the FEPHY. As the REF_CLK frequency is 10 times the data rate in 10Mbps mode the value on TXD[1:0] shall be valid such that TXD[1:0] may be sampled every 10th cycle.

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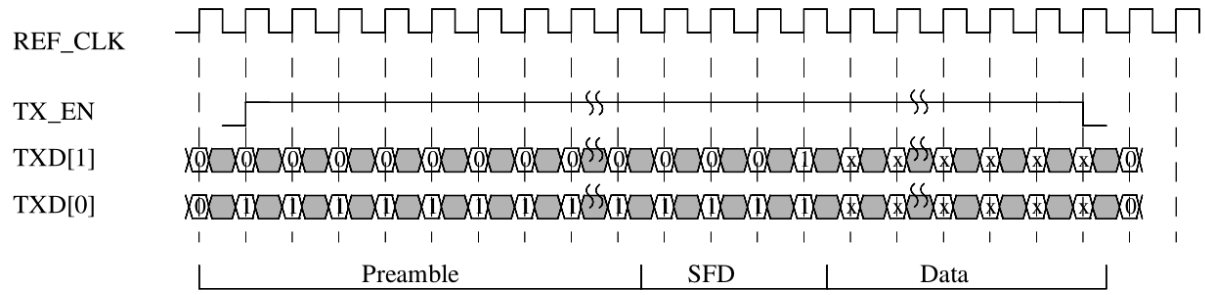

Fig. 43-6 RMII 100 Mbps Transmission

43.3.4.2 RMII Bit Order

Transmission and reception of each octet shall be done a di-bit at a time with the order of di-bit transmission and reception as shown below.

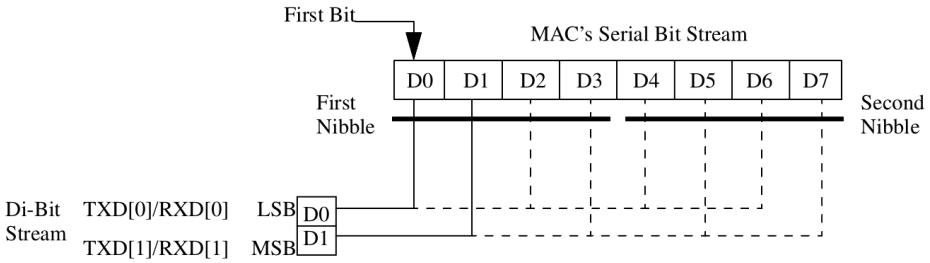

Fig. 43-7 RMII Bit Ordering

43.3.5 Package Format

Figure below shows the fields of an Ethernet packet: the Preamble, Start Frame Delimiter (SFD), the addresses of the MAC frame's destination and source, a length or type field to indicate the length or protocol type of the following field that contains the MAC client data, a field that contains padding if required, and the Frame Check Sequence (FCS) field containing a cyclic redundancy check value to detect errors in a received MAC frame. Of these fields, all are of fixed size except for the MAC Client Data, Pad and Extension fields, which may contain an integer number of octets between the minimum and maximum values that are determined by the specific implementation of the MAC.

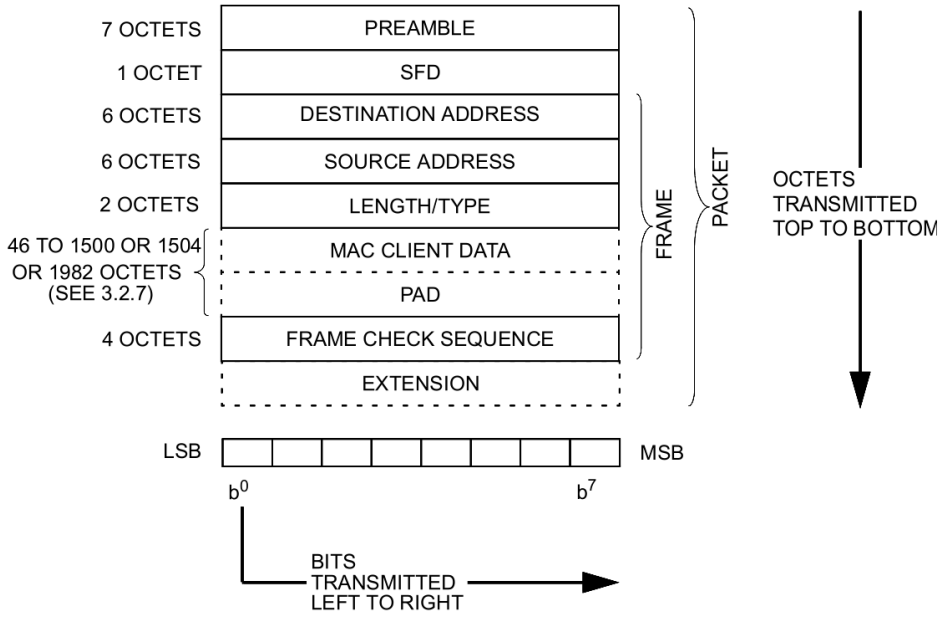

Fig. 43-8 Package Format

43.3.6 Auto-MDIX

Normally, Twisted Pair ports must be connected so that the Transmit pair on one end is connected to the Receive pair on the other end, and vice versa. If the cabling is done so

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that Transmit on one end is wired to Transmit on the other, and Receive is wired to Receive, the link will not come up.

The pads are wired oppositely in various Ethernet application, and some application need to be connect with "straight through" cable, while others need to be connected with a "crossover" cable to match up properly. The "straight through" wiring is known as "MDI" (Media Dependent Interface), and the "crossover" cable is known as "MDIX" (Media Dependent Interface with Crossover).

The Auto-MDIX capability for hardware to automatically correct errors in cable selection, making the distinction between MDI and MDIX.

43.3.7 Auto-Negotiation

The objective of the Auto-Negotiation function is to provide the means to exchange information between two devices that share a link segment and to automatically configure both devices to take maximum advantage of their abilities.

The basic mechanism to achieve Auto-Negotiation is to pass information encapsulated within a burst of closely spaced link integrity test pulses that individually meet the 10BASE-T Transmitter Waveform for Link Test Pulse. This burst of pulses is referred to as a Fast Link Pulse (FLP) Burst. The FLP Burst consists of a series of link integrity test pulses that form an alternating clock/data sequence. Extraction of the data bits from the FLP Burst yields a link codeword that identifies the operational modes supported by the remote device, as well as some information used for the Auto-Negotiation function's handshake mechanism.

A Fast Link Pulse Burst consists of 33 pulse positions. The 17 odd-numbered pulse positions shall contain a link pulse and represent clock information. The 16 even-numbered pulse positions shall represent data information as follows: a link pulse present in an even-numbered pulse position represents a logic one, and a link pulse absent from an even-numbered pulse position represents a logic zero. The encoding of data using pulses in an FLP Burst is illustrated in figure below.

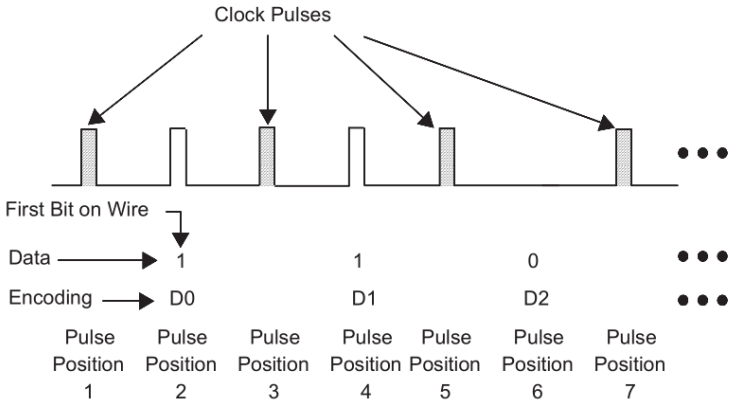

Fig. 43-9 RMII 100 Mbps Transmission

43.3.7.1 FLP Burst Timing

Clock pulses are differentiated from data pulses by the spacing between pulses as shown in figure below and enumerated in table below.

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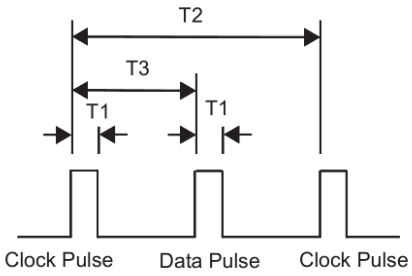

Fig. 43-10 FLP pulse-to-pulse timing

Fig. 43-11 FLP Burst to FLP Burst timing

Table 43-3 FLP Burst timing summary

	Parameter	Min.	Typ.	Max.	Units
T1	Clock/Data Pulse Width (Figure 14–13)		100		ns
T2	Clock Pulse to Clock Pulse	111	125	139	µs
T3	Clock Pulse to Data Pulse (Data = 1)	55.5	62.5	69.5	µs
T4	Pulses in a Burst	17 for 16-bit 49 for 48-bit		33 for 16-bit 97 for 48-bit	–
T5	Burst Width		2 for 16-bit 6 for 48-bit		ms
T6	FLP Burst to FLP Burst	8	16	24	ms
T7	Optimized FLP Burst to FLP Burst	8		8.5	ms

The first pulse in an FLP Burst shall be defined as a clock pulse. Clock pulses within an FLP Burst shall be spaced at 125 µs ± 14 µs. If the data bit representation of logic one is to be transmitted, a pulse shall occur 62.5 µs ± 7 µs after the preceding clock pulse. If a data bit representing logic zero is to be transmitted, there shall be no link integrity test pulses within 111 µs of the preceding clock pulse.The first link pulse in consecutive FLP Bursts shall occur at a 16 ms ± 8 ms interval when using non-optimized FLP Burst to FLP Burst timing, see parameter T6.

43.3.7.2 Link Codeword Encoding

The base link codeword transmitted within an FLP Burst shall convey the encoding shown in figure below. In an FLP Burst, D0 shall be the first bit transmitted.

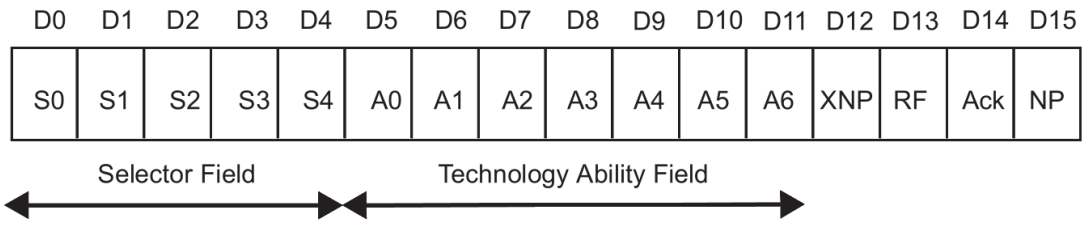

Fig. 43-12 Base Page Encoding

Selector Field (S[4:0]) is a five bit wide field, encoding 32 possible messages.

Technology Ability Field (A[6:0]) is a seven-bit wide field containing information indicating supported technologies specific to the selector field value. Table below summarizes the bit assignments. It is the responsibility of the Arbitration function to determine the common

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mode of operation shared by a Link Partner and to resolve multiple common modes.

Table 43-4 FLP Burst timing summary

Bit	Technology	Minimum cabling requirement
A0	10BASE-T	Two-pair Category 3
A1	10BASE-T full duplex	Two-pair Category 3
A2	100BASE-TX	Two-pair Category 5
A3	100BASE-TX full duplex	Two-pair Category 5
A4	100BASE-T4	Four-pair Category 3
A5	PAUSE operation for full duplex links	Not applicable
A6	Asymmetric PAUSE operation for full duplex Links	Not applicable

Extended Next Page (XNP) is encoded in bit D12 of the base link codeword.

Remote Fault (RF) is encoded in bit D13 of the base link codeword.

Acknowledge (Ack) is used by the Auto-Negotiation function to indicate that a device has successfully received its Link Partner's link codeword. The Acknowledge Bit is encoded in bit D14 regardless of the value of the Selector Field or link codeword encoding.

Next Page (NP) is encoded in bit D15 regardless of the Selector Field value or link codeword encoding.

43.3.7.3 Priority Resolution

Since a Local Device and a Link Partner may have multiple common abilities, a mechanism to resolve which mode to configure is required. The mechanism used by Auto-Negotiation is a Priority Resolution function that predefines the hierarchy of supported technologies. This technology is referred to as the Highest Common Denominator (HCD).

The following list shall represent the relative priorities of the technologies supported by the IEEE 802.3 Selector Field value, where priorities are listed from highest to lowest.

1) 100BASE-T2 full duplex
2) 100BASE-TX full duplex
3) 100BASE-T2
4) 100BASE-T4
5) 100BASE-TX
6) 10BASE-T full duplex
7) 10BASE-T

43.3.8 Energy Efficient Ethernet

The optional EEE capability combines the IEEE 802.3 Media Access Control (MAC) sublayer with a family of Physical Layers defined to support operation in the Low Power Idle (LPI) mode. When the LPI mode is enabled, systems on both sides of the link can save power during periods of low link utilization.

EEE also provides a protocol to coordinate transitions to or from a lower level of power consumption and does this without changing the link status and without dropping or corrupting frames.

43.3.8.1 PHY LPI transmit operation

When the start of "Assert LPI" encoding on the RMII is detected, the PHY signals sleep to its link partner to indicate that the local transmitter is entering LPI mode. The EEE requires the local PHY transmitter to go quiet after sleep is signalled.

The transmit function of the local PHY is enabled periodically to transmit refresh signals that are used by the link partner to update adaptive filters and timing circuits in order to maintain link integrity.

This quiet-refresh cycle continues until the reception of the normal interframe encoding on the RMII. The transmit function in the PHY communicates this to the link partner by

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sending a wake signal for a predefined period of time. The PHY then enters the normal operating state.

Figure below illustrates general principles of the EEE-capable transmitter operation. No data frames are lost or corrupted during the transition to or from the LPI mode.

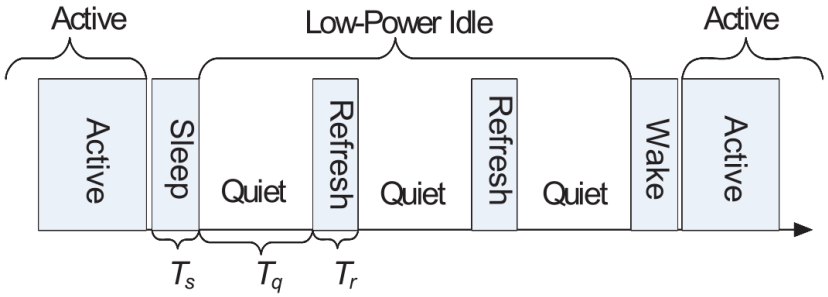

Fig. 43-13 Base Page Encoding

Ts is the period of time that the PHY transmits the sleep signal before turning all transmitters off. *Tq* is the period of time that the PHY remains quiet before sending the refresh signal. *Tr* is the duration of the refresh signal.

43.3.8.2 PHY LPI receive operation

In the receive direction, entering the LPI mode is triggered by the reception of a sleep signal from the link partner, which indicates that the link partner is about to enter the LPI mode. After sending the sleep signal, the link partner ceases transmission. When the receiver detects the sleep signal, the local PHY indicates "Assert LPI" on the RMII and the local receiver can disable some functionality to reduce power consumption.

The link partner periodically transmits refresh signals that are used by the local PHY to update adaptive coefficients and timing circuits. This quiet-refresh cycle continues until the link partner initiates transition back to normal mode by transmitting the wake signal for a predetermined period of time. This allows the local receiver to prepare for normal operation and transition from the "Assert LPI" encoding to the normal interframe encoding on the RMII. After a system specified recovery time, the link supports the nominal operational data rate.

43.3.8.3 RMII LPI Pattern

Special attention should be given to the fact that the RMII protocol does not specify the LPI pattern. Therefore, the EEE feature may be not supported for some MACs with RMII interface.

However, this FEPHY support EEE to save power with simple RMII pattern. RMII TX LPI pattern is that "TX_EN" to "1'b0" and "TXD" to "2'b01". Meanwhile, RMII RX LPI pattern with "CRS_DV" to "1'b0" and "RXD" to "2'b01" is asserted when the FEPHY enters RX LPI mode. To leverage the EEE capability of this FEPHY, an appropriately RMII-LPI-pattern-supporting MAC is required.

43.3.9 Wake on LAN

The PHY should be operating in normal mode for WoL detection. The circuit monitors the network traffic for the special packets called the "Magic Packet". If the magic packet is received, it must further check to see if the magic packet's content has the correct information (CRC check on the received magic packet). If the magic packet contents are correct then the circuit issue an interrupt to the system host controller to wake up the reset
of the circuitry and get the client out of the sleep mode.

A Magic packet is a frame addressed to the device, either a unicast to the programmed address or a broadcast with anywhere in a payload containing 48 '1's followed by 16 repetitions of the client's 48-bit MAC address, possibly followed by four or six byte password. If the MAC address of a node is 48'h00_11_22_33_44_55, then the GMAC scans for the data sequence:

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Destination Address Source Address ……. FF FF FF FF FF FF
00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55
00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55
00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55
00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55
…CRC

The WoL design monitors all the packets transmitted from the Ethernet PHY and generates the WoL interrupt and the status for the following packet conditions.
☐ Detection of Magic Packet with Perfect DA
☐ Detection of Magic Packet with Broadcast DA
☐ Detection of only Magic Packet (Debug)
Refer to register specification for details on control.

The interrupt can be masked through the Interrupt mask register and interrupt status is available on interrupt status register. MAC/Host controller should program the 48 bit MAC Address (Destination address) to the MAC address register.

43.3.10 Physical Coding

Manchester encoding is used for the transmission of packets in 10BASE-T mode. In 100BASE-TX mode, the receiving end needs to recover the clock information from the received data to ensure synchronization, which requires the transmission of the line in the binary stream has enough to jump , that is, there can not be too many consecutive high or low level, otherwise unable to extract clock information. Therefore, the combination of 4B/5B encoding and MLT-3 encoding are employed for 100BASE-TX.

43.3.10.1 Manchester Encoding

Manchester encoding is a binary signaling mechanism that combines data and clock into bit cells. Each bit cell is split into two halves with the second half containing the binary inverse of the first half; a transition always occurs in the middle of each bit cell. During the first half of the bit cell, the encoded signal is the logical complement of the bit value being encoded. During the second half of the bit cell, the encoded signal is the uncomplemented value of the bit being encoded. Examples of Manchester waveform are shown in figure below.

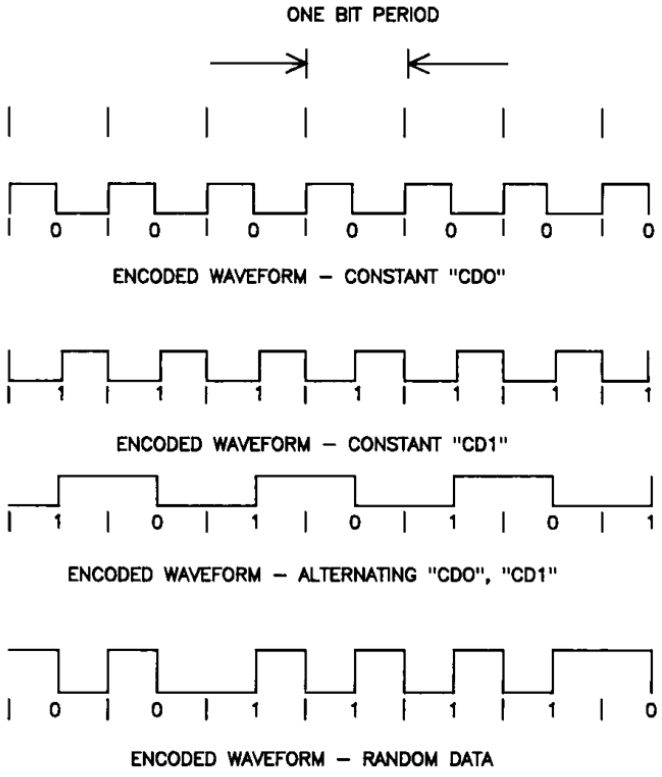

Fig. 43-14 Base Page Encoding

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43.3.10.2 4B/5B Encoding

The Physical Coding Sublayer maps four-bit nibbles from the MII into five-bit code-groups, and vice versa, using a 4B/5B block coding scheme.

The coding method used, derived from ISO/IEC 9314-1, provides

a. Adequate codes (32) to provide for all Data code-groups (16) plus necessary control code-groups.
b. Appropriate coding efficiency (4 data bits per 5 code-bits; 80%) to effect a 100 Mb/s Physical Layer interface on a 125 Mb/s physical channel.
c. Sufficient transition density to facilitate clock recovery (when not scrambled).

Table below specifies the interpretation assigned to each five bit code-group, including the mapping to the nibble-wide (TXD or RXD) Data signals on the MII. The 32 code-groups are divided into four categories as shown.

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Table 43-5 4B/5B code-groups

	PCS code-group [4:0] 4 3 2 1 0	Name	MII (TXD/RXD) <3:0> 3 2 1 0	Interpretation
DATA	1 1 1 1 0	0	0 0 0 0	Data 0
	0 1 0 0 1	1	0 0 0 1	Data 1
	1 0 1 0 0	2	0 0 1 0	Data 2
	1 0 1 0 1	3	0 0 1 1	Data 3
	0 1 0 1 0	4	0 1 0 0	Data 4
	0 1 0 1 1	5	0 1 0 1	Data 5
	0 1 1 1 0	6	0 1 1 0	Data 6
	0 1 1 1 1	7	0 1 1 1	Data 7
	1 0 0 1 0	8	1 0 0 0	Data 8
	1 0 0 1 1	9	1 0 0 1	Data 9
	1 0 1 1 0	A	1 0 1 0	Data A
	1 0 1 1 1	B	1 0 1 1	Data B
	1 1 0 1 0	C	1 1 0 0	Data C
	1 1 0 1 1	D	1 1 0 1	Data D
	1 1 1 0 0	E	1 1 1 0	Data E
	1 1 1 0 1	F	1 1 1 1	Data F
	1 1 1 1 1	I	undefined	IDLE; used as inter-stream fill code
	0 0 0 0 0	P	0 0 0 1	SLEEP; LPI code only for the EEE capability. Otherwise, Invalid code; refer to Table 22–1 and Table 22–2
CONTROL	1 1 0 0 0	J	0 1 0 1	Start-of-Stream Delimiter, Part 1 of 2; always used in pairs with K
	1 0 0 0 1	K	0 1 0 1	Start-of-Stream Delimiter, Part 2 of 2; always used in pairs with J
	0 1 1 0 1	T	undefined	End-of-Stream Delimiter, Part 1 of 2; always used in pairs with R
	0 0 1 1 1	R	undefined	End-of-Stream Delimiter, Part 2 of 2; always used in pairs with T
INVALID	0 0 1 0 0	H	Undefined	Transmit Error; used to force signaling errors
	0 0 0 0 0	V	Undefined	Invalid code
	0 0 0 0 1	V	Undefined	Invalid code
	0 0 0 1 0	V	Undefined	Invalid code
	0 0 0 1 1	V	Undefined	Invalid code
	0 0 1 0 1	V	Undefined	Invalid code
	0 0 1 1 0	V	Undefined	Invalid code
	0 1 0 0 0	V	Undefined	Invalid code
	0 1 1 0 0	V	Undefined	Invalid code
	1 0 0 0 0	V	Undefined	Invalid code
	1 1 0 0 1	V	Undefined	Invalid code

43.3.10.3 MLT-3 Encoding

The Encoder receives the scrambled NRZ data stream and encodes the stream into MLT-3 code for presentation to the driver, and vice versa. MLT-3 coding is similar to NRZI coding, but three instead of two levels are transmitted. MLT-3 cycles sequentially through the voltage levels −1, 0, +1, 0. It moves to the next state to transmit a 1 bit, and stays in the same state to transmit a 0 bit.

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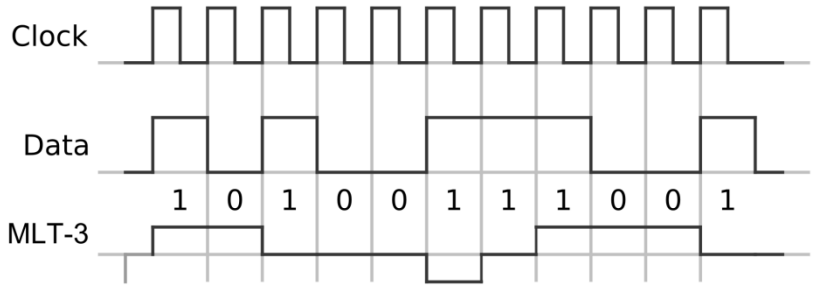

Fig. 43-15 MLT-3 Encoding

43.3.11 Digital Signal Process

The receiver includes a digital integrated Decision Feedback Equalizer (DFE) and Forward Equalizer (FEQ) for MLT-3 encoded signals. It receives samples from an A/D converter that operates at the baud rate. Subtracting each sample from the previous sample eliminates the Base Line Wander (BLW). It also decodes the MLT-3 signal prior to equalization and behaves as a whitening filter to improve adaptation.

The Equalizer is using a unique pipelined architecture, which can be used in a very fast clock rate implementation and combines the FEQ registers with the DFE registers. The exact sampling point is controlled by a second order loop which estimates the frequency offset and phase, using a phase error signal comprised of the difference between the largest coefficient of the DFE and the precursor coefficient of the FEQ.

In addition, the CTLE (Continuous Time Linear Equalizer) is also employed in AFE RX path for data transmission over long distance or through channel with significant signal degradation.

43.3.12 Interrupts

All of the following conditions can be configured to generate interrupt, and the interrupt status bits gets cleared once is is read. Refer to register specification for details on interrupts control.

- Detection of RX LPI Pattern.
- WoL on correct magic packet only (Debug purpose only)
- WoL on correct magic packet and DA for broadcast address
- WoL on magic packet receive and correct DA
- ENERGYON generated
- Auto-Negotiation complete
- Remote Fault Detected
- Link Down (link status negated)
- Auto-Negotiation Link Partner Acknowledge
- Parallel Detection Fault
- Auto-Negotiation Page Received

43.3.13 Loopback

The 10BAST-T/100BASE-TX FEPHY has three independent loop-back modes: Internal loopback, External loopback and Far-End loopback. To maintain the desired operating mode, Auto-Negotiation should be disabled before selecting Loopback mode.

43.3.13.1 Internal loopback

The internal loopback mode is enabled by setting a register bit. In this mode, the scrambled transmit data (output of the scrambler) is looped into the receive logic (input of the descrambler). The COL signal will be inactive in this mode, unless collision test is active. Nothing is transmitted to the line and the transmitters are powered down.

43.3.13.2 Far-End Loopback

The far-end Loopback mode is enabled by setting a register bit. This mode can be used only when the PHY is in 100Base-TX mode. In this mode, packets that arrive at the receiver are looped back out to the transmitter in 100Base-TX mode, the data path includes the analog and digital circuits.

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43.3.13.3 External Loopback

The external loopback can be performed while working in normal mode.

43.3.14 Power Down

43.3.14.1 True Power Down

In True Power Down mode the entire PHY is powered down except the SMI register interface. Access to the SMI registers is still possible, provided the external input clock is active. This is required in order to power up the PHY again via a register access.

The True Power Down mode is different from the General Power Down mode that is mentioned in the standard. This General Power Down mode corresponds to the PLL-Only mode, described in the table item above (please note that the standard does not say that the PLL is on in the so-called General Power Down mode).

43.3.14.2 General Power-Down

This power-down is controlled by register. In this mode the entire PHY, except the management interface, is powered-down and stays in that condition as long as the relevant bit is held high. When it is cleared, the PHY powers up and is automatically reset. General power down mode requires external clock to be always present. In this case PLL can be shut off.

43.3.15 LED

The FEPHY provides two LED signals (default high active). The Link LED output would be driven high whenever the PHY detects a valid link. The Speed LED output would be driven high when the operating speed is 100Mb/s or during Auto-Negotiation. This LED will go inactive when the operating speed is 10Mb/s or power down mode.

43.3.16 GPIO

The analog pad of FEPHY is Standard I/O multiplexed for pin saving. When working in FEPHY mode, the GPIO should be configured in high impedance state. And the configuration of GPIO could be referred in the standard I/O document (DTI GPIO 22ulp 18v33vcfs).

43.4 Register Description

43.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

If the GRF of APB selection is configured, the system could access the direct register bank through APB interface, instead of SMI. And when APB interface is enabled, all offset values of these registers must be shifted left by two bits, to align with Word type.

Meanwhile, the APB interface also provides configurations for internal GRF, whose offset addresses are already Word aligned.

When the APB interface is used, the operational base address is 0x21C90000.

43.4.2 Registers Summary for SMI

Name	Offset	Size	Reset Value	Description
SMI_CONTROL	0x0000	HW	0x00001000	Control Register
SMI_STATUS	0x0001	HW	0x00007809	Status Register
SMI_PHY_IDENTIFIER0	0x0002	HW	0x00000000	PHY Identifier Register 0
SMI_PHY_IDENTIFIER1	0x0003	HW	0x00004401	PHY Identifier Register 1

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Name	Offset	Size	Reset Value	Description
SMI_AUTO_NEGOTIATION_ADVERTISEMENT	0x0004	HW	0x000001E1	Auto-Negotiation Advertisement Register
SMI_AUTO_NEGOTIATION_LINK_PARTNER_ABILITY	0x0005	HW	0x00000001	Auto-Negotiation Link Partner Base Page Ability Register
SMI_AUTO_NEGOTIATION_EXPANSION	0x0006	HW	0x00000004	Auto-Negotiation Expansion Register
SMI_NEXT_PAGE_TRANSMIT_REGISTER	0x0007	HW	0x00002001	Auto-Negotiation Next Page Transmit Register
SMI_SILICON_REVISION	0x0010	HW	0x00000040	Silicon Revision Register
SMI_MODE_CONTROL_STATUS	0x0011	HW	0x00000080	Mode Control and Status Register
SMI_SPECIAL_MODES	0x0012	HW	0x000040E0	Special Register
SMI_SMII_CON_STATUS	0x0013	HW	0x00005400	SMII Control Status Register
SMI_TST_CNTL	0x0014	HW	0x00000000	TST_CNTL Register
SMI_TST_READ1	0x0015	HW	0x00000000	TST_READ1 Register
SMI_TST_READ2	0x0016	HW	0x00000000	TST_READ2 Register
SMI_TST_WRITE	0x0017	HW	0x00000000	TST_WRITE Register
SMI_POWER_DOWN_CONTRL	0x0018	HW	0x00000000	Power Down Control Register
SMI_LED_CTRL	0x0019	HW	0x0000007F	LED Control Register
SMI_RX_ERROR_CNT	0x001A	HW	0x00000000	RX Error Counter Register
SMI_SPECIAL_CONTROL_STATUS	0x001B	HW	0x0000000B	Special Control Status Register

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Name	Offset	Size	Reset Value	Description
SMI_SPECIAL_INTERNAL_TESTABILITY_CONTROL	0x001C	HW	0x00001400	Special Internal Testability Control Register
SMI_INT_STATUS	0x001D	HW	0x00000000	Interrupt Status Register
SMI_INT_MASK	0x001E	HW	0x00000000	Interrupt Mask Register
SMI_PHY_SPECIAL_CONTROL_STATUS	0x001F	HW	0x00000040	PHY Special Control Status Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

43.4.3 Detail Registers Description for SMI

SMI_CONTROL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
15	R/WSC	0x0	reset 1'b0: Normal operation 1'b1: PHY reset
14	RW	0x0	loopback 1'b0: Disable loopback mode 1'b1: Enable loopback mode
13	RW	0x0	speed_selection 1'b0: 10Mbps 1'b1: 100Mbps Ignored if Auto Negotiation is enabled (CONTROL[12]=1). Default FEPHY_iGRF_CON2[6:4], when FEPHY_iGRF_CON2[7]=1.
12	RW	0x1	auto_negotiation_enable 1'b0: Disable Auto-Negotiation process 1'b1: Enable Auto-Negotiation process Default FEPHY_iGRF_CON2[6:4], when FEPHY_iGRF_CON2[7]=1.
11	RW	0x0	power_down 1'b0: Normal operation 1'b1: Power down
10	RW	0x0	isolate 1'b0: Normal operation 1'b1: Electrically Isolate PHY from MII or GMII Default FEPHY_iGRF_CON2[6:4], when FEPHY_iGRF_CON2[7]=1.
9	R/WSC	0x0	restart_auto_negotiation 1'b0: Normal operation 1'b1: Restart Auto-Negotiation process

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Bit	Attr	Reset Value	Description
8	RW	0x0	duplex_mode 1'b0: Half duplex 1'b1: Full duplex Ignored if Auto Negotiation is enabled (CONTROL[12]=1). Default FEPHY_iGRF_CON2[6:4], when FEPHY_iGRF_CON2[7]=1.
7	RW	0x0	collision_test 1'b0: Disable COL signal test 1'b1: Enable COL signal test
6:0	RO	0x00	reserved

SMI_STATUS

Address: Operational Base + offset (0x0001)

Bit	Attr	Reset Value	Description
15	RO	0x0	phy_100base_t4 1'b0: PHY not able to perform 100BASE-T4 1'b1: PHY able to perform 100BASE-T4
14	RO	0x1	phy_100base_x_full_duplex 1'b0: PHY not able to perform full duplex 100BASE-X 1'b1: PHY able to perform full duplex 100BASE-X
13	RO	0x1	phy_100base_x_half_duplex 1'b0: PHY not able to perform half duplex 100BASE-X 1'b1: PHY able to perform half duplex 100BASE-X
12	RO	0x1	phy_10Mbs_full_duplex 1'b0: PHY not able to operate at 10Mbps in full duplex mode 1'b1: PHY able to operate at 10Mbps in full duplex mode
11	RO	0x1	phy_10Mbs_half_duplex 1'b0: PHY not able to operate at 10Mbps in half duplex mode 1'b1: PHY able to operate at 10Mbps in half duplex mode
10:6	RO	0x00	reserved
5	RO	0x0	auto_negotiation_complete 1'b0: Auto-Negotiation process not completed 1'b1: Auto-Negotiation process completed
4	RC	0x0	remote_fault 1'b0: No remote fault condition detected 1'b1: Remote fault condition detected
3	RO	0x1	auto_negotiation_ability 1'b0: PHY is not able to perform Auto-Negotiation 1'b1: PHY is able to perform Auto-Negotiation
2	RC	0x0	link_status 1'b0: Link is down 1'b1: Link is up
1	RC	0x0	jabber_detect 1'b0: No jabber condition detected 1'b1: Jabber condition detected
0	RO	0x1	extended_capability 1'b0: Basic register set capabilities only 1'b1: Extended register capabilities

SMI_PHY_IDENTIFIER0

Address: Operational Base + offset (0x0002)

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	organizationally_unique_identifier Default GRF cfg_phy_id[15:0] Assigned to the 3rd through 18th bits of the Organizationally Unique Identifier (OUI), respectively.

SMI_PHY_IDENTIFIER1

Address: Operational Base + offset (0x0003)

Bit	Attr	Reset Value	Description
15:10	RW	0x11	organizationally_unique_identifier Default GRF cfg_phy_id[21:16] Assigned to the 19th through 24th bits of the OUI.
9:4	RW	0x00	manufacturer_model_number Manufacturer Model Number Default GRF cfg_model_nr[5:0]
3:0	RW	0x1	revision_number Manufacturer Revision Number Default GRF cfg_rev_nr[3:0]

SMI_AUTO_NEGOTIATION_ADVERTISEMENT

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
15	RW	0x0	next_page 1'b0: Next page incapable 1'b1: Next page capable
14	RO	0x0	reserved
13	RW	0x0	remote_fault 1'b0: No remote fault 1'b1: Remote fault detected
12	RO	0x0	reserved
11:10	RW	0x0	pause_operation 2'b00: No PAUSE 2'b01: Asymmetric PAUSE toward link partner 2'b10: Symmetric PAUSE 2'b11: Both Symmetric PAUSE and Asymmetric PAUSE toward local device
9	RO	0x0	phy_100base_t4 1'b0: No T4 ability 1'b1: T4 ability
8	RW	0x1	phy_100base_tx_full_duplex 1'b0: No TX full duplex ability 1'b1: TX with full duplex ability Default FEPHY_iGRF_CON2[6:4], when FEPHY_iGRF_CON2[7]=1.
7	RW	0x1	phy_100base_tx 1'b0: No TX ability 1'b1: TX ability Default FEPHY_iGRF_CON2[6:4], when FEPHY_iGRF_CON2[7]=1.

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Bit	Attr	Reset Value	Description
6	RW	0x1	phy_10base_t_full_duplex 1'b0: No 10Mbps with full duplex ability 1'b1: 10Mbps with full duplex ability Default FEPHY_iGRF_CON2[6:4], when FEPHY_iGRF_CON2[7]=1.
5	RW	0x1	phy_10base_t 1'b0: No 10Mbps ability 1'b1: 10Mbps ability Default FEPHY_iGRF_CON2[6:4], when FEPHY_iGRF_CON2[7]=1.
4:0	RW	0x01	selector_field 5'h1: IEEE 802.3

SMI_AUTO_NEGOTIATION_LINK_PARTNER_ABILITY

Address: Operational Base + offset (0x0005)

Bit	Attr	Reset Value	Description
15	RO	0x0	next_page 1'b0: Next page incapable 1'b1: Next page capable
14	RO	0x0	acknowledge 1'b0: Link code word not yet received 1'b1: Link code word received from partner
13	RO	0x0	remote_fault 1'b0: No remote fault 1'b1: Remote fault detected
12:11	RO	0x0	reserved
10	RO	0x0	pause_operation 1'b0: Pause Operation is not supported by remote MAC 1'b1: Pause Operation is supported by remote MAC
9	RO	0x0	phy_100base_t4 1'b0: No T4 ability 1'b1: T4 ability
8	RO	0x0	phy_100base_tx_full_duplex 1'b0: No TX full duplex ability 1'b1: TX with full duplex ability Default FEPHY_iGRF_CON2[6:4], when FEPHY_iGRF_CON2[7]=1.
7	RO	0x0	phy_100base_tx 1'b0: No TX ability 1'b1: TX ability Default FEPHY_iGRF_CON2[6:4], when FEPHY_iGRF_CON2[7]=1.
6	RO	0x0	phy_10base_t_full_duplex 1'b0: No 10Mbps with full duplex ability 1'b1: 10Mbps with full duplex Default FEPHY_iGRF_CON2[6:4], when FEPHY_iGRF_CON2[7]=1.
5	RO	0x0	phy_10base_t 1'b0: No 10Mbps ability 1'b1: 10Mbps ability Default FEPHY_iGRF_CON2[6:4], when FEPHY_iGRF_CON2[7]=1.

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Bit	Attr	Reset Value	Description
4:0	WO	0x01	selector_field 5'h1: IEEE 802.3

SMI_AUTO_NEGOTIATION_EXPANSION

Address: Operational Base + offset (0x0006)

Bit	Attr	Reset Value	Description
15:5	RO	0x000	reserved
4	RC	0x0	parallel_detection_fault 1'b0: No fault detected by parallel detection logic 1'b1: Fault detected by parallel detection logic
3	RO	0x0	link_partner_next_page_able 1'b0: Link partner does not have next page ability 1'b1: Link partner has next page ability
2	RC	0x1	next_page_able 1'b0: Local device does not have next page ability 1'b1: Local device has next page ability
1	RO	0x0	page_received 1'b0: New page not yet received 1'b1: New page received
0	RO	0x0	link_partner_auto_negotiation_able 1'b0: Link partner does not have auto-negotiation ability 1'b1: Link partner has auto-negotiation ability

SMI_NEXT_PAGE_TRANSMIT_REGISTER

Address: Operational Base + offset (0x0007)

Bit	Attr	Reset Value	Description
15	RW	0x0	next_page 1'b0: Last page 1'b1: Additional next page(s) will follow
14	RO	0x0	reserved
13	RW	0x1	message_page 1'b0: Unformatted Page 1'b1: Message Page
12	RW	0x0	acknowledge_2 1'b0: Cannot comply with message 1'b1: Will comply with message
11	RO	0x0	toggle 1'b0: Previous value of the transmitted Link Code Word equaled logic one. 1'b1: Previous value of the transmitted Link Code Word equaled logic zero.
10:0	RW	0x001	message_unformatted_code_field 11 bit code word to be transmitted as next page received from Link Partner.

SMI_SILICON_REVISION

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
15:10	RO	0x00	reserved
9:6	RO	0x1	silicon_rev Four bit silicon revision identifier

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Bit	Attr	Reset Value	Description
5:0	RO	0x00	reserved

SMI_MODE_CONTROL_STATUS

Address: Operational Base + offset (0x0011)

Bit	Attr	Reset Value	Description
15	RW	0x0	edshort Sigon generation 1'b0: Sigon is asserted on input pulse that is longer then 20ns and guarantee to catch any pulse that is longer then 40ns (in practice, since we use asynchronous set, it is 40ns + minimum time needed for the assertion of the async set input to the ff). 1'b1: Sigon is asserted asynchronically on any input pulse, and stay high for at least one clock cycle.
14	RW	0x0	fastrip Fastrip enable 1'b0: Disable 1'b1: Enable
13	RW	0x0	edpwrdown Enable the Energy Detect Power-Down mode. 1'b0: Energy Detect Power-Down is disabled. 1'b1: Energy Detect Power-Down is enabled.
12	RO	0x0	reserved
11	RW	0x0	lowsqen The Low_Squelch signal is equal to LOWSQEN AND EDPWRDOWN. 1'b0: Implies a higher threshold (less sensitive). 1'b1: Implies a lower threshold (more sensitive).
10	RW	0x0	mdprebp Management Data Preamble Bypass 1'b0: Detect SMI packets with Preamble 1'b1: Detect SMI packets without preamble
9	RW	0x0	farloopback Force the module to the FAR Loop Back mode, i.e. all the received packets are sent back simultaneously (in 100Base-TX or in 100Base FX modes). This bit is only active in RMII/MII mode. This mode works even if MII Isolate (Reg0[10]) is set in RMII mode. In MII mode Reg0[10] bit needs to be cleared.
8	RW	0x0	fasttest Auto-Negotiation Test Mode 1'b0: Normal operation 1'b1: Activates test mode
7	RW	0x1	automdix_en Auto-MDIX enable bit 1'b0: Manual set of MDI/MDIX mode according to bit MDI mode 1'b1: Auto detect MDI/MDIX mode Default FEPHY_iGRF_CON3[0], when FEPHY_iGRF_CON3[1]=1. Not Affected by Software Reset.
6	RW	0x0	mdi_mode Manual set of MDI/MDIX mode. When Auto-MDIX enable bit is not set, this bit sets the MDI/MDIX mode. 1'b0: MDI mode 1'b1: MDIX mode

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Bit	Attr	Reset Value	Description
5	RO	0x0	reserved
4	RW	0x0	dcd_pat_gen When in test mode 1'b0: Disables DCD measuring pattern generation 1'b1: Enables DCD measuring pattern generation
3	RW	0x0	phyadbp 1'b0: Normal mode 1'b1: PHY disregards PHY address in SMI access write.
2	RW	0x0	force_good_link_status 1'b0: Normal operation 1'b1: Force 100TX- link active Note: this bit should be set only during lab testing
1	RO	0x0	energyon ENERGYON indicates whether energy is detected on the line. After the initial link up, If the Reg17[3] is set to 1, then it qualifies the energy loss with 256ms timer window to goes to 0 and to enter in to power down mode. Reset to 0 by hardware reset, unaffected by SW reset. Works when AN is disabled.
0	RO	0x0	reserved

SMI_SPECIAL_MODES

Address: Operational Base + offset (0x0012)

Bit	Attr	Reset Value	Description
15:14	RW	0x1	miimode MII Mode: set the mode of the MII 2'b00: MII interface. 2'b01: RMII interface 2'b10: SMII interface 2'b11: Reserved Default FEPHY_iGRF_CON2[9:8], when FEPHY_iGRF_CON2[11]=1. Not Affected by Software Reset.
13	RO	0x0	reserved
12	RW	0x0	dspbp DSP Bypass mode. Used only in special lab tests. Not Affected by Software Reset.
11	RW	0x0	sqbp SQUELCH Bypass mode Not Affected by Software Reset.
10	RW	0x0	fixmode Enables 100Base-FX mode. 1'b0: Disable 1'b1: Enable, and MODE should be set to 3'b011 (100M full duplex) or 3'b010 (100M half duplex) only. Not Affected by Software Reset.
9	RW	0x0	pllbp PLL Bypass mode 1'b0: PLL normal mode 1'b1: PLL Bypass mode Default FEPHY_iGRF_CON2[12], when FEPHY_iGRF_CON2[13]=1. Not Affected by Software Reset.

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Bit	Attr	Reset Value	Description
8	RW	0x0	adcbp ADC Bypass mode (debug mode) Default FEPHY_iGRF_CON2[14], when FEPHY_iGRF_CON2[15]=1. Not Affected by Software Reset.
7:5	RW	0x7	mode PHY Mode of operation Default FEPHY_iGRF_CON2[6:4], when FEPHY_iGRF_CON2[7]=1. Not Affected by Software Reset. 3'b000: 10BaseT, Half duplex, Auto negotiation disabled 3'b001: 10Base-T, Full duplex, Auto negotiation disabled 3'b010: 100Base-TX, Half duplex, Auto-negotiation disabled 3'b011: 100Base-TX, Full duplex, Auto-negotiation disabled 3'b100: 100Base-Tx, Half duplex, Auto-negotiation enabled 3'b101: Repeater mode, 100Base-Tx, Half duplex, Auto-negotiation enabled 3'b110: Power down mode, In this mode phy wake up in power down mode 3'b111: All capable, Full duplex, 10 & 100 BT, Auto negotiation enabled, Auto-MDIX enabled
4:0	RW	0x00	phyadd PHY Address. The PHY Address is used for the SMI address and for the initialization of the Cipher (Scrambler) key. Default set by the GRF cfg_phy_add signals, or FEPHY_iGRF_CON3[12:8], when FEPHY_iGRF_CON3[15]=1. Not Affected by Software Reset.

SMI_SMII_CON_STATUS

Address: Operational Base + offset (0x0013)

Bit	Attr	Reset Value	Description
15:14	RW	0x1	tx fifo depth Transmitter FIFO depth 2'b00: Initial filling 2 bytes 2'b01: Initial filling 5 bytes Others: Initial filling 23 bytes
13:12	RW	0x1	rx_fifo_depth Receiver FIFO depth 2'b00: Initial filling 2 bytes 2'b01: Initial filling 5 bytes Others: Initial filling 23 bytes
11	RW	0x0	smii_source_sync 1'b0: SMII normal mode 1'b1: SMII source Synchronous mode Not Affected by Software Reset
10	RW	0x1	lpbk_10hd_smii_dis In SMII mode, 10 BT half duplex 1'b0: Enables loopback 1'b1: Disables loopback
9:8	RO	0x0	reserved
7	RC	0x0	tx_eb_ovf Transmitter Elastic overflow
6	RC	0x0	tx_eb_udf Transmitter Elastic underflow

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Bit	Attr	Reset Value	Description
5	RC	0x0	rx_eb_ovf Receiver Elastic overflow
4	RC	0x0	rx_eb_udf Receiver Elastic underflow
3:2	RO	0x0	reserved
1	RO	0x0	rxadcuflw Receiver ADC underflow
0	RO	0x0	rxadcoflw Receiver ADC overflow

SMI_TST_CNTL

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
15	RW	0x0	read When setting this bit to 1, the content of the register that is selected by the READ ADDRESS will be latched to the TSTREAD1/2 registers. This bit is self-cleared.
14	RW	0x0	write When setting this bit to 1, the register that is selected by the WRITE ADDRESS is going to be written with the data from the TSTWRITE register. This bit is self-cleared.
13:11	RW	0x0	reg_bank_sel Selects register bank 3'b000: Selects DSP_0 register bank 3'b001: Selects WOL register bank 3'b010: Selects DSP_0 register bank, only for reading 3'b011: Selects BIST register bank 3'b100: Selects AFE register bank 3'b101: Selects DSP_1 register bank Others: Reserved
10	RW	0x0	test_mode Enable the Testability/Configuration mode 1'b0: Testability/Configuration mode disabled 1'b1: Testability/Configuration mode enabled
9:5	RW	0x00	read_address The address of the Testability/Configuration register that will be latched into the TSTREAD1 and TSTREAD2 registers.
4:0	RW	0x00	write_address The address of the Testability/Configuration register that will be written.

SMI_TST_READ1

Address: Operational Base + offset (0x0015)

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	read_data When reading registers with a size of less than 16 bits, this register contains the register data, starting from bit 0. When reading registers with a size of more than 16 bits, this register contains the less significant 16 bits of the register data.

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SMI_TST_READ2

Address: Operational Base + offset (0x0016)

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	read_data When reading registers with a size of less than 16 bits, this register contains zero. When reading registers with a size of more than 16 bits, this register contains the most significant 16 bits of the register data.

SMI_TST_WRITE

Address: Operational Base + offset (0x0017)

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	write_data This field contains the data that will be written to a specific register on the Programming transaction.

SMI_POWER_DOWN_CONTRL

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
15:4	RO	0x000	reserved
3	RW	0x0	hyst_on_x_amdix 1'b0: Normal mode 1'b1: Every 16 pulses is considered as 1 pulse at TX PAD
2	RW	0x0	hyst_on_amdix 1'b0: Normal mode 1'b1: Every 16 pulses is considered as 1 pulse at RX PAD
1	RW	0x0	power_up_reset Controls pulse generation on output pin powerup_reset 1'b0: Power up reset disable 1'b1: Power up reset enable Default FEPHY_iGRF_CON2[2], when FEPHY_iGRF_CON2[3]=1.
0	RW	0x0	true_power_down 1'b0: Normal operation 1'b1: PHY is put in True power down mode Default FEPHY_iGRF_CON2[0], when FEPHY_iGRF_CON2[1]=1.

SMI_LED_CTRL

Address: Operational Base + offset (0x0019)

Bit	Attr	Reset Value	Description
15:8	RW	0x00	led_ctrl LED control register, led_ctrl[0] control the transmit LED counter active, and led_ctrl[1] control the receive LED counter active, and led_ctrl[2] select link active signal after counting or link immediately to output.
7:0	RW	0x7f	led_blink_cnt Link active signal count value, determining the LEDs flash speed. The larger the value, the slower the LEDs flash.

SMI_RX_ERROR_CNT

Address: Operational Base + offset (0x001A)

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Bit	Attr	Reset Value	Description
15:0	RO	0x0000	rx_error_cnt RX error count. RX error (rx_er) cycles detect.

SMI_SPECIAL_CONTROL_STATUS

Address: Operational Base + offset (0x001B)

Bit	Attr	Reset Value	Description
15:13	RW	0x0	gpo_bits General purpose output for DFT Test.
12	RW	0x0	swrst_fast 1'b0: Normal mode 1'b1: Accelerates SW reset counter from 256 us to 10 us for production testing. Not Affected by Software Reset
11	RW	0x0	sqeoff Disable the SQE test (Heartbeat) 1'b0: SQE test is enabled. 1'b1: SQE test is disabled. Not Affected by Software Reset
10:8	RO	0x0	offset Parameters used when recovering data from scrambles.
7	RW	0x0	loop_qway 1'b0: Disable loopback mode 1'b1: Enable loopback mode When Reg0[14] is high, loop_qway is also high.
6	RW	0x0	tenlbt 1'b0: Normal mode 1'b1: Force 10BT CRS to high
5	RW	0x0	fefien Far End Fault Indication (FEFI) Enable 1'b0: FEFI generation and detection are disabled 1'b1: FEFI generation and detection are enabled Default when FXMODE configuration input is HIGH during reset.
4	RO	0x0	xpol Polarity state of the 10Base-T 1'b0: Normal polarity 1'b1: Reversed polarity

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Bit	Attr	Reset Value	Description
3:0	RO	0xb	arb_state Auto-negotiation State-machine state, 4'h0: X_DIS 4'h1: AD_DET 4'h2: SAVE_CODE 4'h3: COMP_CODE 4'h4: DEC_MATCH 4'h5: ACK_DET 4'h6: ACK_CHECK 4'h7: DEC_ACK 4'h8: COMPL_ACK 4'h9: LINK_GOOD_CHECK 4'ha: LINK_GOOD 4'hb: AUTO_EN 4'hc: LSTATUS_CHECK 4'hd: PDET_FAULT 4'he: NEXT_PAGE_WAIT Others: Reserved

SMI_SPECIAL_INTERNAL_TESTABILITY_CONTROL

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
15:10	RW	0x05	dpll_setup The filter threshold of CDR DPLL in 10Mbps mode.
9	RW	0x0	dis_dsp_rst Disable DSP reset when PLL100 is off. 1'b0: Normal mode 1'b1: The DSP reset mechanism is turned off
8	RW	0x0	xpol_fix_dis Disable Ethernet differential line polarity auto-adaptation judgement. 1'b0: Enable 1'b1: Disable
7:6	RW	0x0	tstbussamp Support for testbus(Debug IO) down-sampling 2'b00: 125 MHz, full rate 2'b01: 50 MHz, 2/5 rate 2'b10: 20 MHz, 1/5 rate Others: Reserved
5:4	RW	0x0	pattern_code Codes the pattern to be transmitted when bit 3 is set. Used in production testing. 2'b00: MII mode 2'b01: Zero pattern 2'b10: One zero pattern 2'b11: Two Zeros Two Ones pattern
3	RW	0x0	pattern_gen_en Enables pattern generation for 10MbpsTransmitter testing 1'b0: Disable 1'b1: Enable
2:0	RO	0x0	reserved

SMI_INT_STATUS

Address: Operational Base + offset (0x001D)

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Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12	RC	0x0	int12 1'b0: Not source of interrupt 1'b1: Detect RX LPI
11	RC	0x0	int11 1'b0: Not source of interrupt 1'b1: WOL on correct magic packet only (Debug purpose only)
10	RC	0x0	int10 1'b0: Not source of interrupt 1'b1: WOL on correct magic packet and DA for broadcast address
9	RC	0x0	int9 1'b0: Not source of interrupt 1'b1: WOL on magic packet receive and correct DA
8	RC	0x0	int8 1'b0: Not source of interrupt 1'b1: SMII elastic buffer overflow/underflow
7	RC	0x0	int7 1'b0: Not source of interrupt 1'b1: ENERGYON generated
6	RC	0x0	int6 1'b0: Not source of interrupt 1'b1: Auto-Negotiation complete
5	RC	0x0	int5 1'b0: Not source of interrupt 1'b1: Remote Fault Detected
4	RC	0x0	int4 1'b0: Not source of interrupt 1'b1: Link Down (link status negated)
3	RC	0x0	int3 1'b0: Not source of interrupt 1'b1: Auto-Negotiation LP Acknowledge
2	RC	0x0	int2 1'b0: Not source of interrupt 1'b1: Parallel Detection Fault
1	RC	0x0	int1 1'b0: Not source of interrupt 1'b1: Auto-Negotiation Page Received
0	RC	0x0	int0 1'b0: Not source of interrupt 1'b1: Detect error counter full

SMI_INT_MASK

Address: Operational Base + offset (0x001E)

Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12	RW	0x0	lpi_int_mask 1'b0: Interrupt source of detecting RX LPI is masked 1'b1: Interrupt source of detecting is enabled

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Bit	Attr	Reset Value	Description
11:9	RW	0x0	wol_int_mask This bit corresponds to the interrupt type in INT_STATUS[11:9] 1'b0: Interrupt source is masked 1'b1: Interrupt source is enabled
8:0	RW	0x000	int_mask Each bit corresponds to the interrupt type in INT_STATUS[8:0] 1'b0: Interrupt source is masked 1'b1: Interrupt source is enabled

SMI_PHY_SPECIAL_CONTROL_STATUS

Address: Operational Base + offset (0x001F)

Bit	Attr	Reset Value	Description
15	RW	0x0	bprmg Bypass Remove Glitch - for Production Testing.
14	RC	0x0	errcnt_full 1'b0: Error count not full 1'b1: Error count full
13	RW	0x0	err_cnt_dis Disable rx_er count, must be set to 0. 1'b0: Enable 1'b1: Disable
12	RO	0x0	autodone Auto-negotiation done indication 1'b0: Auto-negotiation is not done or disabled (or not active). 1'b1: Auto-negotiation is done.
11:7	RW	0x00	speconf Used for production testing.
6	RW	0x1	enable_4b5b 1'b0: Bypass encoder/decoder 1'b1: Enable 4B5B encoding/decoding. MAC Interface must be configured in MII mode.
5	RW	0x0	link_cutoff Cutoff link status 1'b0: Normal 1'b1: Cutoff
4:2	RO	0x0	speed_indication HCDSPEED value: 3'b001: 10MBase half-duplex 3'b101: 10MBase full-duplex 3'b010: 100MBase-TX half-duplex 3'b110: 100MBase-TX full-duplex Others: Reserved
1	RO	0x0	reserved
0	RW	0x0	scramble_disable 1'b0: Enable data scrambling 1'b1: Disable data scrambling

43.4.4 Registers Summary for DSP_0

Name	Offset	Size	Reset Value	Description
DSP_0_DCBL	0x0000	HW	0x00001354	DC and BLW Canceller Configuration Register

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Name	Offset	Size	Reset Value	Description
DSP_0_DBGCNTL	0x0001	HW	0x00000000	Debug Control Register
DSP_0_AMP_THR_1	0x0002	HW	0x00003BDF	Amplitude Threshold Register 1
DSP_0_AMP_THR_2	0x0003	HW	0x00000351	Amplitude Threshold Register 2
DSP_0_AMP_THR_3	0x0004	HW	0x000002DA	Amplitude Threshold Register 3
DSP_0_AMP_THR_4	0x0005	HW	0x00000268	Amplitude Threshold Register 4
DSP_0_AMP_THR_5	0x0006	HW	0x00000212	Amplitude Threshold Register 5
DSP_0_AMP_THR_6	0x0007	HW	0x000001EE	Amplitude Threshold Register 6
DSP_0_AMP_THR_7	0x0008	HW	0x000001C7	Amplitude Threshold Register 7
DSP_0_ENERGY_ON_LEVEL	0x0009	HW	0x00001CE7	Energy on Level Register
DSP_0_ENERGY_OFF_LEVEL_L	0x000A	HW	0x00006666	Energy off Level Low Register 0
DSP_0_ENERGY_OFF_LEVEL_H	0x000B	HW	0x00008776	Energy off Level High Register 0
DSP_0_ENERGY_THR_CNT	0x000C	HW	0x0000E244	Energy Threshold Counter Register
DSP_0_BINIT_L	0x000D	HW	0x00003333	BINIT Low Register 0
DSP_0_BINIT_H	0x000E	HW	0x00003333	BINIT High Register 0
DSP_0_DP_BASE_QTH	0x000F	HW	0x00000018	DP_BASE_QTH Register
DSP_0_DIFFZ_NDIR	0x0010	HW	0x00000115	DIFFZ_NDIR Register
DSP_0_CONFIG	0x0011	HW	0x000011B8	DSP Configuration Option Register 1
DSP_0_A1_CONFIG	0x0012	HW	0x00000000	Analog Test Point Configuration Register 1
DSP_0_A2_CONFIG	0x0013	HW	0x00001000	Analog Test Point Configuration Register 2
DSP_0_A3_CONFIG	0x0014	HW	0x00007180	Analog Test Point Configuration Register 3
DSP_0_A4_CONFIG	0x0015	HW	0x00000010	Analog Test Point Configuration Register 4
DSP_0_A5_CONFIG	0x0016	HW	0x00008406	Analog Test Point Configuration Register 5
DSP_0_A6_CONFIG	0x0017	HW	0x00000080	Analog Test Point Configuration Register 6
DSP_0_A7_CONFIG	0x0018	HW	0x0000000F	Analog Test Point Configuration Register 7
DSP_0_DSP_CONFIG2	0x0019	HW	0x000000D0	DSP Configuration Option Register 2
DSP_0_A8_CONFIG	0x001A	HW	0x0000000D	Analog Test Point Configuration Register 8
DSP_0_A9_CONFIG	0x001B	HW	0x00000040	Analog Test Point Configuration Register 9
DSP_0_A10_CONFIG	0x001C	HW	0x00000010	Analog Test Point Configuration Register 10
DSP_0_DSP_CONFIG3	0x001E	HW	0x00000000	DSP Configuration Option Register 3
DSP_0_A12_CONFIG	0x001F	HW	0x00000009	Analog Test Point Configuration Register 12

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*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

43.4.5 Detail Registers Description for DSP_0

DSP_0_DCBL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
15	RW	0x0	dac_pd BLW DAC power down: If (DACPD_SRC) == 1 then from Reg 1'b0: BLW DAC is enabled. 1'b1: BLW DAC is powered down.
14:12	RW	0x1	blw_avg_mu The weight of current BLW compensation 3'b000: Shift left 3bit 3'b001: Shift left 4bit 3'b010: Shift left 5bit 3'b011: Shift left 6bit 3'b101: Shift left 0bit 3'b110: Shift left 1bit 3'b111: Shift left 2bit Others: Reserved
11	RW	0x0	dac_pd_src PD control for BLW DAC 1'b0: Hardware controlled 1'b1: Software controlled, by DCBL[15]
10:8	RW	0x3	blw_filt_mu The weight of BLW change predictor 3'b000: Shift left 7bit 3'b001: Shift left 6bit 3'b010: Shift left 5bit 3'b011: Shift left 4bit 3'b100: Shift left 3bit 3'b101: Shift left 2bit 3'b110: Shift left 1bit 3'b111: Shift left 0bit
7	RW	0x0	blw_polarity_100 Direction of BLW correction 1'b0: Drift in the opposite direction from the baseline wander. 1'b1: Drift in the positive direction from the baseline wander.
6:4	RW	0x5	blw_mu_100 Correction coefficient 3'b000: Shift left 7bit 3'b001: Shift left 6bit 3'b010: Shift left 5bit 3'b011: Shift left 4bit 3'b100: Shift left 3bit 3'b101: Shift left 2bit 3'b110: Shift left 1bit 3'b111: Shift left 0bit
3	RW	0x0	dac_test_en Enable bypass the BLW outputs from dbg_bp_in pins (dac_bypass_en=1) or from pattern generation. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
2	RW	0x1	blw_en_100 BLW canceling enable 1'b0: Disable 1'b1: Enable
1:0	RW	0x0	blw_window_100 A parameter for calculating the DC level of the receive signal. The DC level is used as guard level that smoothes the current BLW compensation, to avoid future peaks due to abrupt peak levels. 2'b00: Corrected every 8 cycles 2'b01: Corrected every 128 cycles 2'b10: Corrected every 256 cycles 2'b11: Corrected every 512 cycles

DSP_0_DBGCNTL

Address: Operational Base + offset (0x0001)

Bit	Attr	Reset Value	Description
15:12	RW	0x0	monitor Define which set of signals is connected to the external pins. 4'b0000: Default mode, 8'h0. 4'b0001: About NRZ data, FX data, clock phase change, decider data and so on. 4'b0010: About decider data, ADC in. 4'b0011: About decider data, error data. 4'b0100: About DSP state, ADC in. 4'b0101: About ADC under flow, ADC over flow, ADC in. 4'b0110: About ADC in, auto gain. 4'b0111: About clock phase change, error data. 4'b1000: About DSP violation state, state, BLW correct. 4'b1001: About DSP read[7:0]. 4'b1010: About DSP read[15:8]. 4'b1011: About DSP read[23:16]. 4'b1100: About DSP read[7:0], or[15:8], or[23:16]. 4'b1101: About parallel data, NRZI data, BIST done, BIST fail. 4'b1110: About energy on, TX MDIX en, auto-MDIX state. 4'b1111: About squelch relevant parameter.
11:9	RW	0x0	clk_outm Set the state of the CLK_OUT pin. 3'b000: High-impedance. 3'b001: The internal 125MHz receive clock (RX_125) is connected to this pin. 3'b010: The internal 20MHz receive clock (CLK20) is connected to this pin. 3'b011: The internal 20MHz transmit clock (TX20) is connected to this pin. 3'b100: The MII 25MHz transmit clock (TX_CLK) is connected to this pin. 3'b101: The internal 100MHz receive clock (RXCLK100) is connected to this pin. 3'b110: The internal 25MHz receive clock (RX_25) is connected to this pin. 3'b111: The internal ref_clk is connected to this pin. Others: Reserved

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Bit	Attr	Reset Value	Description
8:7	RW	0x0	freezem Set the Freeze mode of the DSP: 2'b00: No freeze, this is the Continuous mode of the chip. 2'b01: Freeze Immediately. At this mode the DSP clock is stopped. All other clocks in the chip are remained toggling. Others: Reserved
6	RO	0x0	reserved
5:3	RW	0x0	trigmode DSP module trigger mode, all mode determine whether the DSP module is valid. 3'b000: Normal mode, trigger is according to interrupt 3'b001: Input pin, float the trigger 3'b010: Freeze imn, trigger is according to the freeze bit 3'b011: Energy drop, trigger is according to the off_energy_set bit 3'b100: Energy detect, trigger is according to the on_energy_set bit Others: Trigger is according to interrupt
2	RW	0x0	tstpts Enable to tri-state (high impedance) the TSTPx pins 1'b0: Normal mode 1'b1: The pins are forced into tri-state
1	RW	0x0	nrziout Enable to output the NRZI stream, during 100Base TX mode, on the DPECL driver (during 100Base-FX mode, this bit is disregarded). 1'b0: No signal is generated on the DEPCL output. 1'b1: NRZI signal is generated on the DEPCL output.
0	RW	0x0	monitor_sel Debug IO group selection. 1'b0: Default IO output 1'b1: Mainly provides higher ADC accuracy related

DSP_0_AMP_THR_1

Address: Operational Base + offset (0x0002)

Bit	Attr	Reset Value	Description
15:14	RO	0x0	reserved
13:11	RW	0x7	stable_count_threshold Stable count threshold value of energy detect.
10:0	RW	0x3df	amp_thresh_1 1st amplitude threshold, providing appropriate adaptive parameters according to the threshold.

DSP_0_AMP_THR_2

Address: Operational Base + offset (0x0003)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10:0	RW	0x351	amp_thresh_2 2nd amplitude threshold, providing appropriate adaptive parameters according to the threshold.

DSP_0_AMP_THR_3

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Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10:0	RW	0x2da	amp_thresh_3 3rd amplitude threshold, providing appropriate adaptive parameters according to the threshold.

DSP_0_AMP_THR_4

Address: Operational Base + offset (0x0005)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10:0	RW	0x268	amp_thresh_4 4th amplitude threshold, providing appropriate adaptive parameters according to the threshold.

DSP_0_AMP_THR_5

Address: Operational Base + offset (0x0006)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10:0	RW	0x212	amp_thresh_5 5th amplitude threshold, providing appropriate adaptive parameters according to the threshold.

DSP_0_AMP_THR_6

Address: Operational Base + offset (0x0007)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10:0	RW	0x1ee	amp_thresh_6 6th amplitude threshold, providing appropriate adaptive parameters according to the threshold.

DSP_0_AMP_THR_7

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10:0	RW	0x1c7	amp_thresh_7 7th amplitude threshold, providing appropriate adaptive parameters according to the threshold.

DSP_0_ENERGY_ON_LEVEL

Address: Operational Base + offset (0x0009)

Bit	Attr	Reset Value	Description
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:11	RW	0x3	feq_coeff_low_thresh Detect weather FEQ coefficient is small or not, set the threshold value. 3'b000: Threshold value is 0 3'b001: Threshold value is 0.0625 3'b010: Threshold value is 0.125 3'b011: Threshold value is 0.25 3'b100: Threshold value is 0.5 3'b101: Threshold value is 0.75 3'b110: Threshold value is 1.0 3'b111: Threshold value is 1.5
10:5	RW	0x27	health_thresh Health threshold value of health monitor.
4:0	RW	0x07	on_energy_level Over energy detection threshold value, compared with input sample data. Data format: 5 bit decimal.

DSP_0_ENERGY_OFF_LEVEL_L

Address: Operational Base + offset (0x000A)

Bit	Attr	Reset Value	Description
15:12	RW	0x6	off_energy_level_3 Set the off energy threshold value according to the self-adapting gain value. Select this value when the 3rd gain is selected. Data format: 4 bit decimal, and starting with percentiles.
11:8	RW	0x6	off_energy_level_2 Set the off energy threshold value according to the self-adapting gain value. Select this value when the 2nd gain is selected. Data format: 4 bit decimal, and starting with percentiles.
7:4	RW	0x6	off_energy_level_1 Set the off energy threshold value according to the self-adapting gain value. Select this value when the 1st gain is selected. Data format: 4 bit decimal, and starting with percentiles.
3:0	RW	0x6	off_energy_level_0 Set the off energy threshold value according to the self-adapting gain value. Select this value when the 0th gain is selected. Data format: 4 bit decimal, and starting with percentiles.

DSP_0_ENERGY_OFF_LEVEL_H

Address: Operational Base + offset (0x000B)

Bit	Attr	Reset Value	Description
15:12	RW	0x8	off_energy_level_7 Set the off energy threshold value according to the self-adapting gain value. Select this value when the 7th gain is selected. Data format: 4 bit decimal, and starting with percentiles.

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Bit	Attr	Reset Value	Description
11:8	RW	0x7	off_energy_level_6 Set the off energy threshold value according to the self-adapting gain value. Select this value when the 6th gain is selected. Data format: 4 bit decimal, and starting with percentiles.
7:4	RW	0x7	off_energy_level_5 Set the off energy threshold value according to the self-adapting gain value. Select this value when the 5th gain is selected. Data format: 4 bit decimal, and starting with percentiles.
3:0	RW	0x6	off_energy_level_4 Set the off energy threshold value according to the self-adapting gain value. Select this value when the 4th gain is selected. Data format: 4 bit decimal, and starting with percentiles.

DSP_0_ENERGY_THR_CNT

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
15:14	RW	0x3	off_energy_cnt_thresh_st1 Off energy count threshold value selection when reset set at high. 2'b00: 32 cycles 2'b01: 64 cycles 2'b10: 128 cycles 2'b11: 256 cycles
13:6	RW	0x89	off_energy_cnt_thresh Off energy count threshold value when reset set at low. When the off energy count is greater than this value, the DSP state machine will return to idle state.
5:0	RW	0x04	on_energy_cnt_thresh On energy count threshold value. Only when on energy count is greater than this value, the DSP state machine can work normally.

DSP_0_BINIT_L

Address: Operational Base + offset (0x000D)

Bit	Attr	Reset Value	Description
15:12	RW	0x3	binit3 Set reset coefficient value of Feed Forward Equalizer, according to the self-adapting gain value. Select this value when the 3rd gain is selected. Data format: 4 bit integer.
11:8	RW	0x3	binit2 Set reset coefficient value of Feed Forward Equalizer, according to the self-adapting gain value. Select this value when the 2nd gain is selected. Data format: 4 bit integer.
7:4	RW	0x3	binit1 Set reset coefficient value of Feed Forward Equalizer, according to the self-adapting gain value. Select this value when the 1st gain is selected. Data format: 4 bit integer.

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Bit	Attr	Reset Value	Description
3:0	RW	0x3	binit0 Set reset coefficient value of Feed Forward Equalizer, according to the self-adapting gain value. Select this value when the 0th gain is selected. Data format: 4 bit integer.

DSP_0_BINIT_H

Address: Operational Base + offset (0x000E)

Bit	Attr	Reset Value	Description
15:12	RW	0x3	binit7 Set reset coefficient value of Feed Forward Equalizer, according to the self-adapting gain value. Select this value when the 7th gain is selected. Data format: 4 bit integer.
11:8	RW	0x3	binit6 Set reset coefficient value of Feed Forward Equalizer, according to the self-adapting gain value. Select this value when the 6th gain is selected. Data format: 4 bit integer.
7:4	RW	0x3	binit5 Set reset coefficient value of Feed Forward Equalizer, according to the self-adapting gain value. Select this value when the 5th gain is selected. Data format: 4 bit integer.
3:0	RW	0x3	binit4 Set reset coefficient value of Feed Forward Equalizer, according to the self-adapting gain value. Select this value when the 4th gain is selected. Data format: 4 bit integer.

DSP_0_DP_BASE_QTH

Address: Operational Base + offset (0x000F)

Bit	Attr	Reset Value	Description
15:14	RO	0x0	reserved
13:8	RW	0x00	dp_base Compensation for the difference between FEQ and DFE coefficients. Data format: 1 bit integer, 5 bit decimal.
7:0	RW	0x18	v_conut_thsh Violation count threshold for decision module. When timeout, if the number of violations is greater than this value, the DSP state machine will return to idle.

DSP_0_DIFFZ_NDIR

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
15:10	RO	0x00	reserved
9:8	RW	0x1	ndir_sel_dir When a violation is judged, the clock phase will move in one direction several times in succession, and then continuously in the other direction, with the single-direction movement period as follows: 2'b00: 4 times 2'b01: 8 times 2'b10: 16 times 2'b11: 32 times

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Bit	Attr	Reset Value	Description
7:0	RW	0x15	low_dz_thrsh_pos Low delta-Z threshold for CDR module. When the absolute value of the clock phase difference is smaller than this value, it will be treated as a violation and no phase adjustment will be performed.

DSP_0_CONFIG

Address: Operational Base + offset (0x0011)

Bit	Attr	Reset Value	Description
15	RW	0x0	err_predictor_disable Whether to disable the error prediction of the ERR module. 1'b0: Enable 1'b1: Disable
14	RO	0x0	reserved
13	RW	0x0	feq_mode FEQ Mode, valid only when adc_mode is set at 6bit mode. 1'b0: FEQ coeff is up to 8 1'b1: FEQ coeff is up to 16
12	RW	0x1	adc_mode ADC Mode 1'b0: 6bit ADC mode 1'b1: 7bit ADC mode
11	RW	0x0	force_init_state Force DSP to initial state. 1'b0: Release 1'b1: Force
10	RW	0x0	phase_src Whether phase correction is controlled by software or hardware. 1'b0: Hardware controlled, from CDR module. 1'b1: Software controlled, from DSP_CONFIG2[10:9].
9:6	RW	0x6	dsp_off_bits Disable the DFE taps. 4'b0000: disable the taps, from 13th to 22th taps 4'b0001: enable all of the taps 4'b0010: disable the 22th tap 4'b0011: disable the 21th and 22th taps 4'b0100: disable the taps, from 20th to 22th taps 4'b0101: disable the taps, from 19th to 22th taps 4'b0110: disable the taps, from 18th to 22th taps 4'b0111: disable the taps, from 17th to 22th taps 4'b1000: disable the taps, from 16th to 22th taps 4'b1001: disable the taps, from 15th to 22th taps 4'b1010: disable the taps, from 14th to 22th taps 4'b1011: disable the taps, from 13th to 22th taps 4'b1100: disable the taps, from 11th to 22th taps 4'b1101: disable the taps, from 9th to 22th taps 4'b1110: disable the taps, from 7th to 22th taps 4'b1111: disable the taps, from 5th to 22th taps
5	RW	0x1	df_shift_lvl Drift frequency level for CDR module. 1.b0: shift right by 7 1.b1: shift right by 8

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Bit	Attr	Reset Value	Description
4:3	RW	0x3	dp_shift_lvl Drift phase level for CDR module. 2'b00: shift right by 11 2'b01: shift right by 12 2'b10: shift right by 13 2'b11: shift right by 14
2	RW	0x0	dfe_pos_sat_en Whether the coefficient adaptation result is allowed to be positive. 1'b0: Disable 1'b1: Enable
1	RW	0x0	mlt3_en Whether the two data before and after the DSP output are processed differentially. 1'b0: Enable Differential MLT3 to NRZI conversion. 1'b1: Enable normal MLT3 to NRZI conversion
0	RW	0x0	diff_off Whether the two data before and after the ADC input are processed differentially. 1'b0: Enable the input differentiation mode 1'b1: Disable the input differentiation mode

DSP_0_A1_CONFIG

Address: Operational Base + offset (0x0012)

Bit	Attr	Reset Value	Description
15:14	RO	0x0	analog_id Analog version
13	RW	0x0	dac_bypass_en Option to bypass the BLW outputs from CO_BPIN 1'b0: Disable 1'b0: Enable
12:11	RO	0x0	reserved
10	RW	0x0	rx_sq_tst_sqvrp_en RX Squelch Test mode, Enable Squelch SQ Vrefp on ATP 1'b0: Disable 1'b1: Enable
9	RW	0x0	rx_sq_tst_davrp_en RX Squelch Test mode, Enable Squelch DATA Vrefp ATP 1'b0: Disable 1'b1: Enable
8	RW	0x0	rx_sq_tst_vcom_en RX Squelch Test mode, Enable VCOM on ATP 1'b0: Disable 1'b1: Enable
7:6	RW	0x0	rx_dac_tst_sel RX BLW DAC Analog Test Point Control 2'b00: No output 2'b01: Test output current of RXP 2'b10: Test output current of RXP 2'b11: Test output current of RXP and RXN
5:0	RO	0x00	reserved

DSP_0_A2_CONFIG

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Address: Operational Base + offset (0x0013)

Bit	Attr	Reset Value	Description
15	RO	0x0	reserved
14:12	RW	0x1	rx_adcvref_isel ADC Vref bias current selection 2'b00: 7.5uA 2'b01: 10uA 2'b10: 12.5uA 2'b11: 15uA
11:10	RO	0x0	reserved
9	RW	0x0	rx_adc_cksel RX ADC clk selection 1'b0: 125MHz 1'b1: 62.5MHz
8	RW	0x0	rx_clk_inv Invert Receiver clock control bit 1'b0: RX Clock not inverted 1'b1: RX Clock inverted
7	RW	0x0	rx_pga_byps Receiver LPF/PGA bypass 1'b0: LPF/PGA is enabled 1'b1: LPF/PGA is bypassed
6	RO	0x0	reserved
5	RW	0x0	rx_mdix_en Recevier MDIX mode enable. Valid only when RX_SRC=1. 1'b0: MDI - Receiver connected to RXP/N. 1'b1: MDIX - Receiver connected to TXP/N.
4	RW	0x0	rx_adc_pd RX ADC power down signal. Valid only when RX_SRC=1. 1'b0: Power up 1'b1: Power down (LPF/PGA/CTLE also be disabled)
3:1	RO	0x0	reserved
0	RW	0x0	rx_src Receiver source 1'b0: Receiver block inputs are controlled by the digital state machines (normal mode). 1'b1: Receiver block inputs are controlled by register A2_CONFIG bits.

DSP_0_A3_CONFIG

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
15:12	RW	0x7	rx_ftune_manual RX LPF POLE tuning manual setting
11	RW	0x0	rx_ftune_src RX LPF pole tuning code selection 1'b0: from internal rcosc calibration results 1'b1: from manual setting
10	RW	0x0	rx_dac_strb_inv Invert RX BLW DACDA strobe signal

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Bit	Attr	Reset Value	Description
9:8	RW	0x1	rx_dac_pole_sel RX BLW DAC Pole trimming 2'b00: 608kHz 2'b01: 922kHz 2'b10: 1.23MHz 2'b11: 1.23MHz
7:5	RW	0x4	rx_100btsig_vref_sel RX 100BT signal detect reference voltage selection 3'b000: 20mV 3'b001: 40mV 3'b010: 60mV 3'b011: 80mV 3'b100: 100mV 3'b101: 120mV 3'b110: 140mV 3'b111: 160mV
4:3	RO	0x0	reserved
2	RW	0x0	rx_100btsig_en RX 100BT signal detect enable
1	RW	0x0	rx_cmfb_exp_sink RX CMFB sink current enhanced
0	RW	0x0	rx_cmfb_pd RX Common-mode feedback power down signal. Valid only when RX_SRC=1. 1'b0: Power up 1'b1: Power down

DSP_0_A4_CONFIG

Address: Operational Base + offset (0x0015)

Bit	Attr	Reset Value	Description
15	RW	0x0	rcosc_clk_test RCOSC_CLK test enable 1'b0: Disable 1'b1: Enable
14:8	RO	0x00	reserved
7	RW	0x0	cb_pd Central bias power down. Valid only if CB_SRC=1. 1'b0: Power up 1'b1: Power down
6	RO	0x0	reserved
5:4	RW	0x1	cb_rxcm_ctrl Adjust receiver common-mode reference voltage 2'b00: 0.45V 2'b01: 0.475V 2'b10: 0.5V 2'b11: 0.525V
3:1	RO	0x0	reserved
0	RW	0x0	cb_src CB Source 1'b0: CB block inputs are controlled by the digital state machines (normal mode). 1'b1: CB block inputs are controlled by register A4_CONFIG bits.

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DSP_0_A5_CONFIG

Address: Operational Base + offset (0x0016)

Bit	Attr	Reset Value	Description
15	RW	0x1	tx_classa 1'b0: Class B (Code 00 is used to drive zero) 1'b1: Class A (Code 11 is used to drive zero)
14:12	RW	0x0	tx_clkph_sel PLL TXCLK Phase Selector (For Multi Port Application)
11	RW	0x0	tx_clk_inv Invert Transmitter Clock control bit 1'b0: TX Clock not inverted 1'b1: TX Clock inverted
10	RW	0x1	tx_clk100_en Transmitter Clock 100/125Mhz control bit. Valid only when TX_SRC=1 (smooth mux) 1'b0: TX Clock is 125Mhz (100BT mode). 1'b1: TX Clock is 100Mhz (10BT mode).
9	RW	0x0	cb_tx_sel10 Transmitter mode select (Amplitude control). Valid only when TX_SRC=1. 1'b0: 100BT mode 1'b1: 10BT mode
8	RW	0x0	tx_mdix_en Transmitter MDIX mode enable. Valid only when TX_SRC=1. 1'b0: TX output from TX PAD 1'b1: TX output from RX PAD
7	RW	0x0	tx_pd Transmitter channel power down. Valid only when TX_SRC=1. 1'b0: Power up 1'b1: Power down
6:4	RW	0x0	tx_slope_10 Transmitter slope control 3'b000: Transmit 10BaseT (2/2/2/2)
3:1	RW	0x3	tx_slope_100 Transmitter slope control 3'b011: Transmit 100BaseT (1/1/1/1)
0	RW	0x0	tx_src TX Source 1'b0: TX block inputs are controlled by the digital state machines (normal mode). 1'b1: TX block inputs are controlled by register A5_CONFIG bits.

DSP_0_A6_CONFIG

Address: Operational Base + offset (0x0017)

Bit	Attr	Reset Value	Description
15:9	RO	0x00	reserved
8:5	RW	0x4	pll_cp_cur_ctrl PLL CP current fine tune
4:3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2	RW	0x0	pll_vco_force_en Force PLL Vctrl in open loop mode 1'b0: No force 1'b1: Force
1	RW	0x0	pll_pd PLL power down control. Valid only when PLL_SRC=1. 1'b0: Power up 1'b1: Power down
0	RW	0x0	pll_src PLL Source 1'b0: PLL block inputs are controlled by the digital state machines (normal mode). 1'b1: PLL block inputs are controlled by register A6_CONFIG bits.

DSP_0_A7_CONFIG

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
15:6	RO	0x000	reserved
5	RW	0x0	atpselp AMP100 pattern generate enable 1'b0: From TXDA 1'b1: From AMP PATTERN

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Bit	Attr	Reset Value	Description
4:0	RW	0x0f	cb_tx_amp Transmitter amplitude control for 100M mode. (10M mode, see A12_CONFIG) 5'h0: 826mV 5'h1: 840mV 5'h2: 854mV 5'h3: 868mV 5'h4: 882mV 5'h5: 896mV 5'h6: 910mV 5'h7: 924mV 5'h8: 938mV 5'h9: 952mV 5'ha: 966mV 5'hb: 980mV 5'hc: 994mV 5'hd: 1.08V 5'he: 1.022V 5'hf: 1.036V 5'h10: 1.050V 5'h11: 1.064V 5'h12: 1.078V 5'h13: 1.092V 5'h14: 1.106V 5'h15: 1.12V 5'h16: 1.134V 5'h17: 1.148V 5'h18: 1.162V 5'h19: 1.176V 5'h1a: 1.19V 5'h1b: 1.204V 5'h1c: 1.218V 5'h1d: 1.232V 5'h1e: 1.246V 5'h1f: 1.26V

DSP_0_DSP_CONFIG2

Address: Operational Base + offset (0x0019)

Bit	Attr	Reset Value	Description
15:12	RO	0x0	reserved
11	RW	0x0	blw_state2_dis 1'b0: Enable BLW module reset operation when condition meets. 1'b1: Disable BLW module reset operation.
10:9	RW	0x0	ext_phase_en_val_wr External control 2'b00: external strobe phase=0, external increment phase=0 2'b01: external strobe phase=0, external increment phase=1 2'b10: external strobe phase=1, external increment phase=0 2'b11: external strobe phase=1, external increment phase=1

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Bit	Attr	Reset Value	Description
8	RW	0x0	ext_phase_en_wr Whether phase correction is controlled by software or hardware. 1'b0: Hardware controlled, from CDR module, function is similar to CONFIG[10]. 1'b1: Software controlled, from DSP_CONFIG[10:9].
7:4	RW	0xd	zero_violations_count_thresh Zero violation count threshold value
3	RW	0x0	mlt3_blw_rst_dis 1'b0: Enable the count of MLT3 zero times. 1'b1: Disabel the count of MLT3 zero times.
2	RW	0x0	xrxd_blw_rst_dis 1'b0: Enable BLW module reset operation when condition meets. 1'b1: Disable BLW module reset operation.
1	RW	0x0	force_fx_clk 1'b0: Normal mode 1'b1: Force FX module clock to keep working
0	RW	0x0	force_dsp_nrm_clk 1'b0: Normal mode 1'b1: Force DSP module clock to keep working

DSP_0_A8_CONFIG

Address: Operational Base + offset (0x001A)

Bit	Attr	Reset Value	Description
15:14	RO	0x0	reserved
13:6	RW	0x00	pll_tst_sel PLL test select
5:4	RO	0x0	reserved
3:0	RW	0xd	pll_lpf_res_sel PLL LPF R value (ohm) control 4'b0000: 48k 4'b0001: 44k 4'b0010: 40k 4'b0011: 36k 4'b0100: 40k 4'b0101: 36k 4'b0110: 32k 4'b0111: 28k 4'b1000: 32k 4'b1001: 28k 4'b1010: 24k 4'b1011: 20k 4'b1100: 24k 4'b1101: 20k 4'b1110: 16k 4'b1111: 12k

DSP_0_A9_CONFIG

Address: Operational Base + offset (0x001B)

Bit	Attr	Reset Value	Description
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14	RW	0x0	rcosc_pd RX RCOSC Calibration power down 1'b0: Power up 1'b1: Power down
13:9	RO	0x00	reserved
8	RW	0x0	rx_sq_lpf_bpys RX Squelch Low-Pass-Filter bypass enable 1'b0: Normal mode 1'b1: Bypass mode
7:6	RW	0x1	rx_sq_lpf_sel Adjust RX Squelch LPF poles 2'b00: 28MHz 2'b01: 26MHz 2'b10: 24MHz 2'b11: 22MHz
5:4	RO	0x0	reserved
3	RW	0x0	rx_sq_lvth RX Squelch extended length mode (lower comparator threshold) 1'b0: Value decided by RX_SQ_REF_SEL[2:0] 1'b1: 20mV
2	RW	0x0	rx_sq_x_en TXP/N Squelch power down signal. Valid only when SQ_SRC=1. 1'b0: Power up 1'b1: Power down
1	RW	0x0	rx_sq_en RXP/N Squelch power down signal. Valid only when SQ_SRC=1. 1'b0: Power up 1'b1: Power down
0	RW	0x0	sq_src Squelch Source 1'b0: Squelch blocks inputs are controlled by the digital state machines (normal mode). 1'b1: Squelch blocks inputs are controlled by register A9_CONFIG bits.

DSP_0_A10_CONFIG

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
15:10	RO	0x00	reserved
9	RW	0x0	txda_bypass_en Option to Bypass the TXDA to analog from CO_BPIN 1'b0: TXDA 1'b1: CO_BPIN
8:7	RO	0x0	reserved
6	RW	0x0	cb_tstvbg_en Test internal Band gap on ATP

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Bit	Attr	Reset Value	Description
5:4	RW	0x1	cb_extc_sel Enable external bias current 2'b00: External 100uA bias current enable 2'b01: External 100uA bias current disable 2'b10: External 100uA bias current enable 2'b11: External 100uA bias current enable
3	RW	0x0	cb_extvbg_en Enables external Band gap reference 1'b0: Voltage reference is generated internally 1'b1: Drive external band-gap reference thru ATP
2:0	RO	0x0	reserved

DSP_0_DSP_CONFIG3

Address: Operational Base + offset (0x001E)

Bit	Attr	Reset Value	Description
15:10	RO	0x00	reserved
9	RW	0x0	fx_dsp_out_sel A back door may modify previous bug. 1'b0: FX MDIO read 1'b1: DSP MDIO read
8	RW	0x0	dfe_13to22_dis 1'b0: The work taps of DFE depends on CONFIG[9:6]. 1'b1: Mandatory shutdown the 13th to 22th taps.
7:5	RO	0x0	reserved
4	RW	0x0	ext_gain_en External gain value enable 1'b0: Disable 1'b1: Enable
3:0	RW	0x0	ext_gain External gain value. Valid only when EXT_GAIN_EN=1.

DSP_0_A12_CONFIG

Address: Operational Base + offset (0x001F)

Bit	Attr	Reset Value	Description
15:5	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
4:0	RW	0x09	cb_10m_tx_amp Transmitter amplitude Control for 10M mode 5'h0: 1.54V 5'h1: 1.596V 5'h2: 1.652V 5'h3: 1.708V 5'h4: 1.764V 5'h5: 1.820V 5'h6: 1.876V 5'h7: 1.932V 5'h8: 1.988V 5'h9: 2.044V 5'ha: 2.100V 5'hb: 2.156V 5'hc: 2.212V 5'hd: 2.268V 5'he: 2.324V 5'hf: 2.380V

43.4.6 Registers Summary for WOL

Name	Offset	Size	Reset Value	Description
WOL_MAC_DA_ADDRS_0	0x0000	HW	0x00000000	6-Bytes MAC Address Register 0
WOL_MAC_DA_ADDRS_1	0x0001	HW	0x00000000	6-Bytes MAC Address Register 1
WOL_MAC_DA_ADDRS_2	0x0002	HW	0x00000000	6-Bytes MAC Address Register 2
WOL_WOL_CONTROL	0x0003	HW	0x00000000	WOL Common Control Register
WOL_EPHY_LPI_CNTRL	0x0004	HW	0x00000250	EPHY LPI Common Control Register
WOL_EPHY_LPI_RX_TW_TS_TIMER	0x0005	HW	0x000014FA	EEE LPI Receiver Wait & Sleep Timer Count Register
WOL_EPHY_LPI_RX_TI_TQ_TIMER	0x0006	HW	0x000015FA	EEE LPI Receiver Quiet & Idle Timer Count Register

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Name	Offset	Size	Reset Value	Description
WOL_EPHY_LPI_RX_LINK_FAIL_TIMER	0x0007	HW	0x0000005B	EEE LPI Receiver Link Fail Timer Count Register
WOL_EPHY_LPI_TX_TIMER	0x0008	HW	0x0000C9C9	EEE LPI Transmitter Sleep & Quiet Timer Count Register
WOL_EPHY_BIST_CONTROL	0x0009	HW	0x00000400	BIST Control Register
WOL_WOL_STATUS	0x000A	HW	0x00000000	WOL Status Bits Register
WOL_EPHY_LPI_RX_WAKE_ERR_CNTR	0x000B	HW	0x00000000	EEE LPI Receiver Wake Error Count Register
WOL_EPHY_LPI_STATUS	0x000C	HW	0x00000000	EEE LPI Transmit and Receiver Status Register
WOL_EPHY_BIST_STATUS	0x000D	HW	0x00000000	EPHY BIST Status Register
WOL_EHPY_LPI_SIGDET_HYSTER_CNTRL	0x000E	HW	0x0000FFFF	LPI Signal Detect of Hysteresis Register
WOL_EPHY_LPI_SIGDET_CNTRL	0x000F	HW	0x00000008	EPHY LPI Signal Detect Control Register
WOL_EPHY_SIGDET_HIGH_HYSTERESIS_WIN_CNT	0x0010	HW	0x000003FF	EPHY Signal High Hysteresis Window Count Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

43.4.7 Detail Registers Description for WOL

WOL_MAC_DA_ADDRS_0

Address: Operational Base + offset (0x0000)

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	mac_da_addrs_0 Two bytes of MAC address, from bit15 to bit0.

WOL_MAC_DA_ADDRS_1

Address: Operational Base + offset (0x0001)

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	mac_da_addrs_1 Two bytes of MAC address, from bit31 to bit16.

WOL_MAC_DA_ADDRS_2

Address: Operational Base + offset (0x0002)

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	mac_da_addrs_2 Two bytes of MAC address, from bit47 to bit32.

WOL_WOL_CONTROL

Address: Operational Base + offset (0x0003)

Bit	Attr	Reset Value	Description
15:5	RO	0x000	reserved
4	RW	0x0	wol_check_sa_unicast_en Enable the unicast check on the SA address. This configuration is used along with the i_wol_mag_pkt_da_en and the i_wol_mag_pkt_broadcast_en configuration register bits. 1'b0: Disable 1'b1: Enable
3	RW	0x0	wol_mag_pkt_en Enable Wake of LAN for only Magic packet detection. 1'b0: Disable 1'b1: Enable
2	RW	0x0	wol_mag_pkt_broadcast_en Enable Wake of LAN for Magic packet detection with broadcast DA. 1'b0: Disable 1'b1: Enable
1	RW	0x0	wol_mag_pkt_da_en Enable Wake of LAN for Magic packet detection with perfect DA. 1'b0: Disable 1'b1: Enable
0	RW	0x0	wol_en Enable the Wake of LAN detection logic 1'b0: Disable 1'b1: Enable

WOL_EPHY_LPI_CNTRL

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14	RW	0x0	ephy_lpi_bypass_afe_rx_pd 1'b0: AFE-PD TX signals gated during LPI-RX quiet. 1'b1: AFE-PD TX signals gateless during LPI-RX quiet.
13	RW	0x0	ephy_lpi_bypass_afe_tx_pd 1'b0: AFE-PD TX signals gated during LPI-TX quiet. 1'b1: AFE-PD TX signals gateless during LPI-TX quiet.
12	RW	0x0	ephy_lpi_bypass_dsp_freeze 1'b0: Gate the DSP module clock during EEE-RX-LPI quiet state. 1'b1: Pass the DSP module clock during EEE-RX-LPI quiet state.
11	RW	0x0	ephy_10bte_mode_enable 1'b0: Disable EEE 10BTe mode in AFE. 1'b1: Enable EEE 10BTe mode in AFE.
10	RW	0x0	ephy_lpi_rx_mode_sel Mode selection to AFE 100BT signal detect circuit. 1'b0: LPI mode If input is <200mV peak to peak the detector output is LOW. If input is >400mV peak to peak the detector output is HIGH. 1'b1: Normal mode If input is <200mV peak to peak the detector output is LOW. If input is >100mV peak to peak the detector output is HIGH.
9	RW	0x1	ephy_lpi_rx_100bt_sig_det_enable 1'b0: Disable 100BT signal detect circuit in AFE. 1'b1: Enable 100BT signal detect circuit in AFE for LPI mode operation in RX side.
8	RW	0x0	ephy_lpi_rx_wake_err_cntr_clr Clears the wake error counter status register. It is self-clearing bit.
7:3	RW	0x0a	ephy_lpi_rx_clk_stop_en_range This register range should be programmed between d'10 to d'31 indicating that that the Rx clock to MII interface should be killed on detection of LPI mode after this programmable count. This register is valid only when the ephy_lpi_rx_clk_stop register bit is enabled. (Default value = hA).
2	RW	0x0	ephy_lpi_rx_clk_stop 1'b0: Do no gate the Rx-clock during LPI mode. 1'b1: Gate the Rx-clock to MII once the LPI is detected from the Rx-PHY.
1	RW	0x0	ephy_lpi_rx_enable 1'b0: LPI mode is disabled in RX-side. 1'b1: LPI mode is enabled in RX-side.
0	RW	0x0	ephy_lpi_tx_enable 1'b0: LPI mode is disabled in TX-side. 1'b1: LPI mode is enabled in TX-side.

WOL_EPHY_LPI_RX_TW_TS_TIMER

Address: Operational Base + offset (0x0005)

Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:8	RW	0x14	ephy_lpi_rx_tw_timer The LPI-RX wait counter which is decremented internally with 1 us event to generate the timer done status. The clock frequency which is used to generate the 1 us event is 25 MHz (40 ns period).
7:0	RW	0xfa	ephy_lpi_rx_ts_timer The LPI Sleep or Refresh counter which is decremented internally with 1 us event to generate the timer done status. The clock frequency which is used to generate the 1 us event is 25 MHz (40 ns period).

WOL_EPHY_LPI_RX_TI_TQ_TIMER

Address: Operational Base + offset (0x0006)

Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12:8	RW	0x15	ephy_lpi_rx_ti_timer The LPI-RX idle counter which is decremented internally with Rx clock event of 25 MHz clock frequency (40 ns period).
7:0	RW	0xfa	ephy_lpi_rx_tq_timer The LPI-RX quiet counter which is decremented internally with 100 us event to generate the timer done status. The clock frequency which is used to generate the 1 us event is 25 MHz (40 ns period).

WOL_EPHY_LPI_RX_LINK_FAIL_TIMER

Address: Operational Base + offset (0x0007)

Bit	Attr	Reset Value	Description
15:7	RO	0x000	reserved
6:0	RW	0x5b	ephy_lpi_rx_link_fail_timer The LPI-RX link fail timer counter which is decremented internally with 1 us event to generate the timer done status. The clock frequency which is used to generate the 1 us event is 25 MHz (40 ns period).

WOL_EPHY_LPI_TX_TIMER

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
15:8	RW	0xc9	ephy_lpi_tx_tq_timer Quiet timer value
7:0	RW	0xc9	ephy_lpi_tx_ts_tr_timer Sleep/refresh timer value

WOL_EPHY_BIST_CONTROL

Address: Operational Base + offset (0x0009)

Bit	Attr	Reset Value	Description
15:10	RW	0x01	bist_tx_en_cnt Write tx_en count, actual value = {bist_tx_en_cnt, 2'b0}.
9:2	RW	0x00	bist_dv_cnt BIST data valid count

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Bit	Attr	Reset Value	Description
1	RW	0x0	bist_valid 1'b0: Bist data invalid 1'b1: Bist data valid, count completion of DV can plus one
0	RW	0x0	bist_enable 1'b0: Disable old BIST test 1'b1: Enable old BIST test

WOL_WOL_STATUS

Address: Operational Base + offset (0x000A)

Bit	Attr	Reset Value	Description
15:3	RO	0x0000	reserved
2	RO	0x0	wol_mag_pkt_sts Set to 1 on reception of only Magic packet (debug).
1	RO	0x0	wol_mag_pkt_broadcast_sts Set to 1 on reception of Magic packet with broadcast DA match.
0	RO	0x0	wol_mag_pkt_da_sts Set to 1 on reception of Magic packet with perfect programmed DA match.

WOL_EPHY_LPI_RX_WAKE_ERR_CNTR

Address: Operational Base + offset (0x000B)

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	ephy_lpi_rx_wake_err_cntr The LPI_RX wake error counter status. This counter clears on setting the register bit ephy_lpi_rx_wake_err_cntr_clr. The counter held all ones in case of overflow.

WOL_EPHY_LPI_STATUS

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12	RO	0x0	ephy_lpi_descrambler_lock 1'b0: Enable scramble function 1'b1: Disable scramble function
11	RO	0x0	ephy_lpi_100bt_signal_det_sts Output signal detect/energy detect indication
10:8	RO	0x0	ephy_lpi_tx_state PCS-TX FSM state
7	RO	0x0	ephy_lpi_tx_detected 1'b0: EPHY-TX not detected the LPI mode. 1'b1: EPHY-TX detected the LPI mode and entering the LPI state.
6	RO	0x0	ephy_lpi_tx_quiet_state 1'b1: EPHY-TX LPI state machine is in quiet state in which power down action has been taken. 1'b0: LPI-FSM is not in quiet state.
5	RO	0x0	ephy_lpi_rx_quiet_state 1'b0: LPI-FSM is not in quiet state. 1'b1: EPHY-RX LPI state machine is in quiet state in which power down action has been taken.

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Bit	Attr	Reset Value	Description
4	RO	0x0	ephy_lpi_rx_detected 1'b0: EPHY-RX not detected the LPI mode. 1'b1: EPHY-RX detected the LPI mode and entering the LPI state.
3:0	RO	0x0	ephy_pcs_rx_fsm_state PCS-RX FSM state

WOL_EPHY_BIST_STATUS

Address: Operational Base + offset (0x000D)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10	RO	0x0	rxdv_detect_error RXDV detect error
9:2	RO	0x00	bist_err_count Count BIST failure time
1	RO	0x0	bist_fail Failure of BIST test
0	RO	0x0	bist_done Completion of BIST test

WOL_EHPY_LPI_SIGDET_HYSTER_CNTRL

Address: Operational Base + offset (0x000E)

Bit	Attr	Reset Value	Description
15:8	RW	0xff	ephy_lpi_sigdet_low_hyster_cntrl Low hysteresis count to detect the consecutive low pulses.
7:0	RW	0xff	ephy_lpi_sigdet_high_hyster_cntrl High hysteresis count to detect the consecutive high pulses.

WOL_EPHY_LPI_SIGDET_CNTRL

Address: Operational Base + offset (0x000F)

Bit	Attr	Reset Value	Description
15:4	RO	0x000	reserved
3	RW	0x1	ephy_ed_enable Energy detect enable from local register configuration.
2	RW	0x0	ephy_force_lpi_tx Force LPI TX
1	RO	0x0	reserved
0	RW	0x0	ephy_lpi_rx_sigdet Force mode enable for the signal detect from TOP level input pin controlled from SOC register.

WOL_EPHY_SIGDET_HIGH_HYSTERESIS_WIN_CNT

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
15:0	RW	0x03ff	ephy_sigdet_high_hysterises_win_cnt Window to be programmed to detect the number consecutive high or low pulses.

43.4.8 Registers Summary for BIST

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Name	Offset	Size	Reset Value	Description
BIST_BIST_CTRL	0x0000	HW	0x00000000	BIST Control Register
BIST_BIST_STATUS	0x0001	HW	0x00000000	BIST Status Register
BIST_BIST_PREAMBLE_SFD_IPG_LENGTH	0x0002	HW	0x00000000	Preamble, SFD & IPG Length Register
BIST_BIST_PACKET_DATA_LENGTH	0x0003	HW	0x00000000	Packet Data Length Register
BIST_BIST_DA_0	0x0004	HW	0x00000000	Lower 16 Bits of Destination Address
BIST_BIST_DA_1	0x0005	HW	0x00000000	Middle 16 Bits of Destination Address
BIST_BIST_DA_2	0x0006	HW	0x00000000	Higher 16 Bits of Destination Address
BIST_BIST_SA_0	0x0007	HW	0x00000000	Lower 16 Bits of Source Address
BIST_BIST_SA_1	0x0008	HW	0x00000000	Middle 16 bits of Source Address
BIST_BIST_SA_2	0x0009	HW	0x00000000	Higher 16 bits of Source Address
BIST_BIST_NIBBLE_CNT	0x000A	HW	0x00000000	Programmable Total Count of Nibble Register
BIST_BIST_ERROR_COUNT	0x000B	HW	0x00000000	Bit Error Count Register
BIST_BIST_RECEIVED_NIBBLE_CNT	0x000C	HW	0x00000000	Total Received Nibble Count Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

43.4.9 Detail Registers Description for BIST

BIST_BIST_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
15	RW	0x0	bist_measure_freeze Freezes the BIST measure & is applicable only when bist_tx_en_sequence_en is set to high.
14	RW	0x0	bist_da_sa_fcs_en 1'b0: Disable sending FCS & DA SA 1'b1: Enable sending FCS & DA SA
13:8	RW	0x00	bist_tx_en_cnt Counts the number of tx_en before asserting rxdv_detect_error when rxdv is not detected in bist_checker (see bit rxdv_detect_error). This register is internally multiplied by 4.

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Bit	Attr	Reset Value	Description
7	RW	0x0	bist_tx_en_sequence_en 1'b0: Generation of BIST signals is governed by register bit bist_tx_en_cnt 1'b1: Generation of BIST signals is continuous
6:4	RW	0x0	bist_prbs_select Different type of PRBS is selected 3'b000: PRBS4 3'b001: PRBS5 3'b010: PRBS6 3'b011: PRBS7 3'b100: PRBS8 3'b101: PRBS9 3'b110: PRBS12 3'b111: PRBS13
3:2	RW	0x0	bist_prbs_constant_data_sel 2'b00: Constant data is sent (4'h6) 2'b01: Divide by4 clock pattern is sent 2'b10: Ramp data is sent 2'b11: PRBS output is sent (see bist_prbs_select)
1	RW	0x0	bist_valid This is valid only when bist_enable is set high. 1'b0: Send zeros on txd, tx_er & tx_en 1'b1: Send internal generator output
0	RW	0x0	bist_enable Selects between BIST generator output or from MAC for PCS interface. 1'b0: From Mac (txd, tx_er & tx_en) 1'b1: From internal BIST generator

BIST_BIST_STATUS

Address: Operational Base + offset (0x0001)

Bit	Attr	Reset Value	Description
15:4	RO	0x000	reserved
3	RO	0x0	rx_er_detect_error Indicates rx_er is detected when rxdv is high.
2	RO	0x0	rxdv_detect_error Indicates the rxdv is not detected even after programmable tx_en is sent (see bits bist_tx_en_cnt).
1	RO	0x0	bist_fail Indicates the BIST failure. It is asserted either check on 1. Bit error is found 2. RXDV is not detected 3. Error injection is failed (not received expected errors) 4. RX_ER detected when RXDV is high 5. Mismatch between number of transmitted & received nibbles
0	RO	0x0	bist_done Indicates the completion of bist check. It is asserted either check on 1. Bit error count is saturated to 0xFFFF 2. Programmable wait time is over after the completion of all packets are sent by the BIST generator 3. Forced by programming bist_measure_freeze

BIST_BIST_PREAMBLE_SFD_IPG_LENGTH

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Address: Operational Base + offset (0x0002)

Bit	Attr	Reset Value	Description
15:8	RW	0x00	bist_ipg_length Length of IPG in bytes (96 bits as per IEEE standard)
7:4	RW	0x0	bist_sfd_length Length of SFD in bytes
3:0	RW	0x0	bist_preamble_length Length of preamble in bytes

BIST_BIST_PACKET_DATA_LENGTH

Address: Operational Base + offset (0x0003)

Bit	Attr	Reset Value	Description
15:13	RW	0x0	wait_after_tx_en_cnt Number of 1us wait after the completion of all packets & assert bist_done to the checker. It is effective when bist_tx_en_sequence_en is set to zero. It is internally multiply by 2.
12:0	RW	0x0000	bist_data_length Length of Packet data in bytes

BIST_BIST_DA_0

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	bist_da_0 [15:0] of Destination Address

BIST_BIST_DA_1

Address: Operational Base + offset (0x0005)

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	bist_da_1 [31:16] of Destination Address

BIST_BIST_DA_2

Address: Operational Base + offset (0x0006)

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	bist_da_2 [47:32] of Destination Address

BIST_BIST_SA_0

Address: Operational Base + offset (0x0007)

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	bist_sa_0 [15:0] of Source Address

BIST_BIST_SA_1

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	bist_sa_1 [31:16] of Source Address

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BIST_BIST_SA_2

Address: Operational Base + offset (0x0009)

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	bist_sa_2 [47:32] of Source Address

BIST_BIST_NIBBLE_CNT

Address: Operational Base + offset (0x000A)

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	bist_nibble_cnt Number of nibbles is transmitted by the BIST generator. Formula for the calculation of this register: (bist_data_length*2) *(tx_en_cnt * 4). This is compared against received nibble count at the BIST checker & asserts bist_fail if there is mismatch.

BIST_BIST_ERROR_COUNT

Address: Operational Base + offset (0x000B)

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	bist_err_count Indicates the bit error count when the word counter reached bist_word_cnt (Word counter reaches first).

BIST_BIST_RECEIVED_NIBBLE_CNT

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	bist_received_nibble_cnt Indicates the total count of nibble received.

43.4.10 Registers Summary for AFE

Name	Offset	Size	Reset Value	Description
AFE_CB_CTRL0	0x0000	HW	0x00000149	Common Block Control Register 0
AFE_CB_CTRL1	0x0001	HW	0x00000000	Common Block Control Register 1
AFE_PLL_CTRL0	0x0002	HW	0x00001000	PLL Control Register 0
AFE_PLL_CTRL1	0x0003	HW	0x00000100	PLL Control Register 1
AFE_PLL_CTRL2	0x0004	HW	0x00000009	PLL Control Register 2
AFE_TX_CTRL0	0x0005	HW	0x00000046	TX Calibration Control Register 0
AFE_TX_CTRL1	0x0006	HW	0x00000200	TX TEST and SPARE Control Register 1
AFE_TX_STATUS	0x0007	HW	0x00000000	TX Calibration Status Register
AFE_RX_GAIN0	0x0008	HW	0x00004321	RX PGA GAIN Register 0
AFE_RX_GAIN1	0x0009	HW	0x00007655	RX PGA GAIN Register 1
AFE_RX_GAIN2	0x000A	HW	0x00009887	RX PGA GAIN Register 2
AFE_RX_GAIN3	0x000B	HW	0x0000CCB9	RX PGA GAIN Register 3
AFE_RX_CMFB_GAIN0	0x000C	HW	0x00005555	RX CMFB GAIN Register 0
AFE_RX_CMFB_GAIN1	0x000D	HW	0x00005555	RX CMFB GAIN Register 0

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Name	Offset	Size	Reset Value	Description
AFE_RX_GAIN	0x000E	HW	0x00000000	RX PGA and CMFB Gain Register
AFE_RX_CTRL0	0x0010	HW	0x00000022	RX LDO Control Register 0
AFE_RX_CTRL1	0x0011	HW	0x00000000	RX CDR Control Register 1
AFE_RX_CTRL2	0x0012	HW	0x00000010	RX LPF and RCOSC Control Register 2
AFE_RX_CTRL3	0x0013	HW	0x00004101	RX CTLE Control Register 3
AFE_RX_CTRL4	0x0014	HW	0x00000030	RX ADC Control Register 4
AFE_RX_CTRL5	0x0015	HW	0x00000023	RX ADC and DAC Control Register 5
AFE_RX_CTRL6	0x0016	HW	0x00000104	RX SQ Control Register 6
AFE_RX_CTRL7	0x0017	HW	0x00000000	RX SQ Control Register 7
AFE_RX_CTRL8	0x0018	HW	0x00000000	RX SQ Control Register 8
AFE_RX_CTRL9	0x0019	HW	0x00000020	RX 100BTSIG Control Register 9
AFE_RX_CTRL10	0x001A	HW	0x00000000	RX Test Control Register 10
AFE_RX_CTRL11	0x001B	HW	0x0000A815	RX Spare Control Register 11
AFE_RX_CTRL12	0x001C	HW	0x00000000	RX Test Control Register 12
AFE_RX_CTRL13	0x001D	HW	0x00000000	RX Test Control Register 13
AFE_RX_STATUS0	0x001E	HW	0x00000000	RX CDR Status Register 0
AFE_RX_STATUS1	0x001F	HW	0x00000000	RX SQ and 100BTSIG Status Register 1

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

43.4.11 Detail Registers Description for AFE

AFE_CB_CTRL0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
15:12	RO	0x0	reserved
11:10	RW	0x0	cb_iptrn_sel IB_20u_PLL_BIAS[1:0] control
9:8	RW	0x1	cb_rxldovref_sel RX LDO Vref voltage selection 2'b00: 575mV 2'b01: 600mV 2'b10: 625mV 2'b11: 650mV
7	RW	0x0	cb_intres_en Current gen inner resistor enable 1'b0: External resistor enable mode 1'b1: Internal resistor enable mode
6:4	RW	0x4	cb_intres_sel Current gen inner res adjust
3:2	RW	0x2	cb_sqvref_sel SQ reference voltage adjust 2'b00: 0.75V 2'b01: 0.775V 2'b10: 0.80V 2'b11: 0.825V
1:0	RW	0x1	cb_rxadc_vref_sel Adjust receiver ADC common-mode reference voltage. 2'b00: 0.45V 2'b01: 0.50V 2'b10: 0.55V 2'b11: 0.60V

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AFE_CB_CTRL1

Address: Operational Base + offset (0x0001)

Bit	Attr	Reset Value	Description
15:4	RO	0x000	reserved
3:0	RW	0x0	cb_tst_sel CB test mode control

AFE_PLL_CTRL0

Address: Operational Base + offset (0x0002)

Bit	Attr	Reset Value	Description
15:10	RW	0x04	pll_loop_div_sel PLL post-divider N control. Valid only when PLL_DIV_OVWR_EN=1. 6'h0: /5 6'h1: /5 6'h2: /10 6'h3: /10 ... 6'h3f: /315
9	RW	0x0	pll_div_ovwr_en PLL div enable 1'b0: Disable 1'b1: Enable
8:4	RW	0x00	pll_pre_div_sel PLL pre-divider N control. Valid only when PLL_DIV_OVWR_EN=1. 5'h0: Bypass 5'h1: Bypass 5'h2: /2 5'h3: /3 ... 5'h1f: /31
3:0	RW	0x0	pll_vco_force_crtl PLL Vctrl force voltage set

AFE_PLL_CTRL1

Address: Operational Base + offset (0x0003)

Bit	Attr	Reset Value	Description
15:10	RO	0x00	reserved
9:8	RW	0x1	pll_kvco_ctrl PLL KVCO control
7	RO	0x0	reserved
6	RW	0x0	pll_fl_en PLL fast lock enable 1'b0: Disable 1'b1: Enable
5:4	RW	0x0	pll_fl_sel PLL fast lock time control 2'b00: ~20 us 2'b01: ~40 us 2'b10: ~80 us 2'b11: ~160 us

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Bit	Attr	Reset Value	Description
3	RW	0x0	pll_flck_sel PLL fast lock clk select 1'b0: REF clk 1'b1: FB clk
2:0	RW	0x0	pll_cp_cur_sel PLL CP current unit number select: 20uA * ([2]*4+[1]*2+[0]*1+1)

AFE_PLL_CTRL2

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
15:12	RW	0x0	pll_spare PLL reserved
11:9	RO	0x0	reserved
8	RW	0x0	pll_tst_en PLL test mode enable 1'b0: Disable 1'b1: Enable
7	RW	0x0	pll_ldt_force PLL lock detect force 1'b0: Np force 1'b1: Force
6:4	RW	0x0	pll_ldt_ch_ctrl PLL analog mode lock detect threshold select
3:2	RW	0x2	pll_ldt_cn_sel PLL counter mode lock detect set 2'b00: ~20 us 2'b01: ~40 us 2'b10: ~80 us 2'b11: ~160 us
1	RW	0x0	pll_ldt_sel PLL lock detect mode select 1'b0: Analog mode 1'b1: Counter mode
0	RW	0x1	pll_ldt_en PLL lock detect enable 1'b0: Disable 1'b1: Enable

AFE_TX_CTRL0

Address: Operational Base + offset (0x0005)

Bit	Attr	Reset Value	Description
15:12	RO	0x0	reserved
11	RW	0x0	tx_halfi_en TX driver bias current decrease half enable 1'b0: Normal current 1'b1: Normal current x0.5
10	RW	0x0	tx_pulse_en TX DAC short pulse gen enable, used for better p/n bias setting up if needed. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
9	RW	0x0	tx_decp_en TX DAC decouple function enable; used for decrease bias ripple if needed. 1'b0: Disable 1'b1: Enable
8	RW	0x0	txrx_rterm_en Enable TX internal term resistor
7	RO	0x0	reserved
6:4	RW	0x4	tx_calib_vref_ctrl TX calibration Vref selection
3	RO	0x0	reserved
2	RW	0x1	tx_calib_sel TX calibration mode selection 1'b0: Manual setting 1'b1: Auto calibration
1	RW	0x1	tx_calib_clk_fsel TX calibration clk frequency selection 1'b0: Ref clk 1'b1: Ref clk div 4
0	RW	0x0	tx_calib_en TX calibration enable 1'b0: Disable 1'b1: Enable

AFE_TX_CTRL1

Address: Operational Base + offset (0x0006)

Bit	Attr	Reset Value	Description
15	RW	0x0	tx_spare_7 Used as initial rest signal for calibration 1'b0: Calibration is reset 1'b1: Calibration normal mode
14	RW	0x0	tx_spare_6 No used
13	RW	0x0	tx_spare_5 1'b0: TX calib clk is ref_clk div4 1'b1: TX calib clk is ref_clk
12	RW	0x0	tx_spare_4 1'b0: In TX calib mode, tx input clk source is ref_clk or ref_clk div4 1'b1: In TX calib mode, tx input clk source is 500MHz from PLL
11	RW	0x0	tx_spare_3 TX half i enable, valid only when TX_SPARE_2to1=2'b00. 1'b0: Disable 1'b1: Enable
10:9	RW	0x1	tx_spare_2to1 2'b00: TX_halfi_en is controlled by TX_SPARE[3] 2'b10: TX_halfi_en is the same as TX calib enable signal Others: tx_halfi_en is from digital
8	RW	0x0	tx_spare_0 1'b0: TX calib enable signal from digital 1'b1: TX calib enable signal from analog
7	RW	0x0	tx_tst_vssh_en TX VSSH test enable

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Bit	Attr	Reset Value	Description
6	RO	0x0	reserved
5:0	RW	0x00	tx_tst_sel TX TEST mode control

AFE_TX_STATUS

Address: Operational Base + offset (0x0007)

Bit	Attr	Reset Value	Description
15:9	RO	0x00	reserved
8:4	RO	0x00	tx_calib_mon TX calibration results monitor
3	RO	0x0	reserved
2	RO	0x0	tx_calib_amp_all0 TX calibration results all 0
1	RO	0x0	tx_calib_amp_all1 TX calibration results all 1
0	RO	0x0	tx_calib_pass TX calibration pass

AFE_RX_GAIN0

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
15:12	RW	0x4	rx_pga_gain_3 Set the 3rd RX PGA gain value 4'h0: 1.000 (0.00 dB) 4'h1: 1.083 (0.70 dB) 4'h2: 1.174 (1.39 dB) 4'h3: 1.273 (2.09 dB) 4'h4: 1.381 (2.80 dB) 4'h5: 1.500 (3.52 dB) 4'h6: 1.632 (4.25 dB) 4'h7: 1.778 (5.00 dB) 4'h8: 1.941 (5.76 dB) 4'h9: 2.123 (6.55 dB) 4'ha: 2.333 (7.36 dB) 4'hb: 2.571 (8.20 dB) 4'hc: 2.846 (9.09 dB) 4'hd: 3.167 (10.01 dB) 4'he: 3.546 (10.99 dB) 4'hf: 4.000 (12.04 dB)

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Bit	Attr	Reset Value	Description
11:8	RW	0x3	rx_pga_gain_2 Set the 2nd RX PGA gain value 4'h0: 1.000 (0.00 dB) 4'h1: 1.083 (0.70 dB) 4'h2: 1.174 (1.39 dB) 4'h3: 1.273 (2.09 dB) 4'h4: 1.381 (2.80 dB) 4'h5: 1.500 (3.52 dB) 4'h6: 1.632 (4.25 dB) 4'h7: 1.778 (5.00 dB) 4'h8: 1.941 (5.76 dB) 4'h9: 2.123 (6.55 dB) 4'ha: 2.333 (7.36 dB) 4'hb: 2.571 (8.20 dB) 4'hc: 2.846 (9.09 dB) 4'hd: 3.167 (10.01 dB) 4'he: 3.546 (10.99 dB) 4'hf: 4.000 (12.04 dB)
7:4	RW	0x2	rx_pga_gain_1 Set the 1st RX PGA gain value 4'h0: 1.000 (0.00 dB) 4'h1: 1.083 (0.70 dB) 4'h2: 1.174 (1.39 dB) 4'h3: 1.273 (2.09 dB) 4'h4: 1.381 (2.80 dB) 4'h5: 1.500 (3.52 dB) 4'h6: 1.632 (4.25 dB) 4'h7: 1.778 (5.00 dB) 4'h8: 1.941 (5.76 dB) 4'h9: 2.123 (6.55 dB) 4'ha: 2.333 (7.36 dB) 4'hb: 2.571 (8.20 dB) 4'hc: 2.846 (9.09 dB) 4'hd: 3.167 (10.01 dB) 4'he: 3.546 (10.99 dB) 4'hf: 4.000 (12.04 dB)
3:0	RW	0x1	rx_pga_gain_0 Set the 0th RX PGA gain value 4'h0: 1.000 (0.00 dB) 4'h1: 1.083 (0.70 dB) 4'h2: 1.174 (1.39 dB) 4'h3: 1.273 (2.09 dB) 4'h4: 1.381 (2.80 dB) 4'h5: 1.500 (3.52 dB) 4'h6: 1.632 (4.25 dB) 4'h7: 1.778 (5.00 dB) 4'h8: 1.941 (5.76 dB) 4'h9: 2.123 (6.55 dB) 4'ha: 2.333 (7.36 dB) 4'hb: 2.571 (8.20 dB) 4'hc: 2.846 (9.09 dB) 4'hd: 3.167 (10.01 dB) 4'he: 3.546 (10.99 dB) 4'hf: 4.000 (12.04 dB)

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AFE_RX_GAIN1

Address: Operational Base + offset (0x0009)

Bit	Attr	Reset Value	Description
15:12	RW	0x7	rx_pga_gain_7 Set the 7th RX PGA gain value 4'h0: 1.000 (0.00 dB) 4'h1: 1.083 (0.70 dB) 4'h2: 1.174 (1.39 dB) 4'h3: 1.273 (2.09 dB) 4'h4: 1.381 (2.80 dB) 4'h5: 1.500 (3.52 dB) 4'h6: 1.632 (4.25 dB) 4'h7: 1.778 (5.00 dB) 4'h8: 1.941 (5.76 dB) 4'h9: 2.123 (6.55 dB) 4'ha: 2.333 (7.36 dB) 4'hb: 2.571 (8.20 dB) 4'hc: 2.846 (9.09 dB) 4'hd: 3.167 (10.01 dB) 4'he: 3.546 (10.99 dB) 4'hf: 4.000 (12.04 dB)
11:8	RW	0x6	rx_pga_gain_6 Set the 6th RX PGA gain value 4'h0: 1.000 (0.00 dB) 4'h1: 1.083 (0.70 dB) 4'h2: 1.174 (1.39 dB) 4'h3: 1.273 (2.09 dB) 4'h4: 1.381 (2.80 dB) 4'h5: 1.500 (3.52 dB) 4'h6: 1.632 (4.25 dB) 4'h7: 1.778 (5.00 dB) 4'h8: 1.941 (5.76 dB) 4'h9: 2.123 (6.55 dB) 4'ha: 2.333 (7.36 dB) 4'hb: 2.571 (8.20 dB) 4'hc: 2.846 (9.09 dB) 4'hd: 3.167 (10.01 dB) 4'he: 3.546 (10.99 dB) 4'hf: 4.000 (12.04 dB)

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Bit	Attr	Reset Value	Description
7:4	RW	0x5	rx_pga_gain_5 Set the 5th RX PGA gain value 4'h0: 1.000 (0.00 dB) 4'h1: 1.083 (0.70 dB) 4'h2: 1.174 (1.39 dB) 4'h3: 1.273 (2.09 dB) 4'h4: 1.381 (2.80 dB) 4'h5: 1.500 (3.52 dB) 4'h6: 1.632 (4.25 dB) 4'h7: 1.778 (5.00 dB) 4'h8: 1.941 (5.76 dB) 4'h9: 2.123 (6.55 dB) 4'ha: 2.333 (7.36 dB) 4'hb: 2.571 (8.20 dB) 4'hc: 2.846 (9.09 dB) 4'hd: 3.167 (10.01 dB) 4'he: 3.546 (10.99 dB) 4'hf: 4.000 (12.04 dB)
3:0	RW	0x5	rx_pga_gain_4 Set the 4th RX PGA gain value 4'h0: 1.000 (0.00 dB) 4'h1: 1.083 (0.70 dB) 4'h2: 1.174 (1.39 dB) 4'h3: 1.273 (2.09 dB) 4'h4: 1.381 (2.80 dB) 4'h5: 1.500 (3.52 dB) 4'h6: 1.632 (4.25 dB) 4'h7: 1.778 (5.00 dB) 4'h8: 1.941 (5.76 dB) 4'h9: 2.123 (6.55 dB) 4'ha: 2.333 (7.36 dB) 4'hb: 2.571 (8.20 dB) 4'hc: 2.846 (9.09 dB) 4'hd: 3.167 (10.01 dB) 4'he: 3.546 (10.99 dB) 4'hf: 4.000 (12.04 dB)

AFE_RX_GAIN2

Address: Operational Base + offset (0x000A)

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Bit	Attr	Reset Value	Description
15:12	RW	0x9	rx_pga_gain_11 Set the 11th RX PGA gain value 4'h0: 1.000 (0.00 dB) 4'h1: 1.083 (0.70 dB) 4'h2: 1.174 (1.39 dB) 4'h3: 1.273 (2.09 dB) 4'h4: 1.381 (2.80 dB) 4'h5: 1.500 (3.52 dB) 4'h6: 1.632 (4.25 dB) 4'h7: 1.778 (5.00 dB) 4'h8: 1.941 (5.76 dB) 4'h9: 2.123 (6.55 dB) 4'ha: 2.333 (7.36 dB) 4'hb: 2.571 (8.20 dB) 4'hc: 2.846 (9.09 dB) 4'hd: 3.167 (10.01 dB) 4'he: 3.546 (10.99 dB) 4'hf: 4.000 (12.04 dB)
11:8	RW	0x8	rx_pga_gain_10 Set the 10th RX PGA gain value 4'h0: 1.000 (0.00 dB) 4'h1: 1.083 (0.70 dB) 4'h2: 1.174 (1.39 dB) 4'h3: 1.273 (2.09 dB) 4'h4: 1.381 (2.80 dB) 4'h5: 1.500 (3.52 dB) 4'h6: 1.632 (4.25 dB) 4'h7: 1.778 (5.00 dB) 4'h8: 1.941 (5.76 dB) 4'h9: 2.123 (6.55 dB) 4'ha: 2.333 (7.36 dB) 4'hb: 2.571 (8.20 dB) 4'hc: 2.846 (9.09 dB) 4'hd: 3.167 (10.01 dB) 4'he: 3.546 (10.99 dB) 4'hf: 4.000 (12.04 dB)
7:4	RW	0x8	rx_pga_gain_9 Set the 9th RX PGA gain value 4'h0: 1.000 (0.00 dB) 4'h1: 1.083 (0.70 dB) 4'h2: 1.174 (1.39 dB) 4'h3: 1.273 (2.09 dB) 4'h4: 1.381 (2.80 dB) 4'h5: 1.500 (3.52 dB) 4'h6: 1.632 (4.25 dB) 4'h7: 1.778 (5.00 dB) 4'h8: 1.941 (5.76 dB) 4'h9: 2.123 (6.55 dB) 4'ha: 2.333 (7.36 dB) 4'hb: 2.571 (8.20 dB) 4'hc: 2.846 (9.09 dB) 4'hd: 3.167 (10.01 dB) 4'he: 3.546 (10.99 dB) 4'hf: 4.000 (12.04 dB)

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Bit	Attr	Reset Value	Description
3:0	RW	0x7	rx_pga_gain_8 Set the 8th RX PGA gain value 4'h0: 1.000 (0.00 dB) 4'h1: 1.083 (0.70 dB) 4'h2: 1.174 (1.39 dB) 4'h3: 1.273 (2.09 dB) 4'h4: 1.381 (2.80 dB) 4'h5: 1.500 (3.52 dB) 4'h6: 1.632 (4.25 dB) 4'h7: 1.778 (5.00 dB) 4'h8: 1.941 (5.76 dB) 4'h9: 2.123 (6.55 dB) 4'ha: 2.333 (7.36 dB) 4'hb: 2.571 (8.20 dB) 4'hc: 2.846 (9.09 dB) 4'hd: 3.167 (10.01 dB) 4'he: 3.546 (10.99 dB) 4'hf: 4.000 (12.04 dB)

AFE_RX_GAIN3

Address: Operational Base + offset (0x000B)

Bit	Attr	Reset Value	Description
15:12	RW	0xc	rx_pga_gain_15 Set the 15th RX PGA gain value 4'h0: 1.000 (0.00 dB) 4'h1: 1.083 (0.70 dB) 4'h2: 1.174 (1.39 dB) 4'h3: 1.273 (2.09 dB) 4'h4: 1.381 (2.80 dB) 4'h5: 1.500 (3.52 dB) 4'h6: 1.632 (4.25 dB) 4'h7: 1.778 (5.00 dB) 4'h8: 1.941 (5.76 dB) 4'h9: 2.123 (6.55 dB) 4'ha: 2.333 (7.36 dB) 4'hb: 2.571 (8.20 dB) 4'hc: 2.846 (9.09 dB) 4'hd: 3.167 (10.01 dB) 4'he: 3.546 (10.99 dB) 4'hf: 4.000 (12.04 dB)

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Bit	Attr	Reset Value	Description
11:8	RW	0xc	rx_pga_gain_14 Set the 14th RX PGA gain value 4'h0: 1.000 (0.00 dB) 4'h1: 1.083 (0.70 dB) 4'h2: 1.174 (1.39 dB) 4'h3: 1.273 (2.09 dB) 4'h4: 1.381 (2.80 dB) 4'h5: 1.500 (3.52 dB) 4'h6: 1.632 (4.25 dB) 4'h7: 1.778 (5.00 dB) 4'h8: 1.941 (5.76 dB) 4'h9: 2.123 (6.55 dB) 4'ha: 2.333 (7.36 dB) 4'hb: 2.571 (8.20 dB) 4'hc: 2.846 (9.09 dB) 4'hd: 3.167 (10.01 dB) 4'he: 3.546 (10.99 dB) 4'hf: 4.000 (12.04 dB)
7:4	RW	0xb	rx_pga_gain_13 Set the 13th RX PGA gain value 4'h0: 1.000 (0.00 dB) 4'h1: 1.083 (0.70 dB) 4'h2: 1.174 (1.39 dB) 4'h3: 1.273 (2.09 dB) 4'h4: 1.381 (2.80 dB) 4'h5: 1.500 (3.52 dB) 4'h6: 1.632 (4.25 dB) 4'h7: 1.778 (5.00 dB) 4'h8: 1.941 (5.76 dB) 4'h9: 2.123 (6.55 dB) 4'ha: 2.333 (7.36 dB) 4'hb: 2.571 (8.20 dB) 4'hc: 2.846 (9.09 dB) 4'hd: 3.167 (10.01 dB) 4'he: 3.546 (10.99 dB) 4'hf: 4.000 (12.04 dB)
3:0	RW	0x9	rx_pga_gain_12 Set the 12th RX PGA gain value 4'h0: 1.000 (0.00 dB) 4'h1: 1.083 (0.70 dB) 4'h2: 1.174 (1.39 dB) 4'h3: 1.273 (2.09 dB) 4'h4: 1.381 (2.80 dB) 4'h5: 1.500 (3.52 dB) 4'h6: 1.632 (4.25 dB) 4'h7: 1.778 (5.00 dB) 4'h8: 1.941 (5.76 dB) 4'h9: 2.123 (6.55 dB) 4'ha: 2.333 (7.36 dB) 4'hb: 2.571 (8.20 dB) 4'hc: 2.846 (9.09 dB) 4'hd: 3.167 (10.01 dB) 4'he: 3.546 (10.99 dB) 4'hf: 4.000 (12.04 dB)

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AFE_RX_CMFB_GAIN0

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
15:14	RW	0x1	rx_cmfb_gain_7 Set the 7th RX CMFB gain value 2'b00: 0.24 2'b01: 0.31 2'b10: 0.34 2'b11: 0.38
13:12	RW	0x1	rx_cmfb_gain_6 Set the 6th RX CMFB gain value 2'b00: 0.24 2'b01: 0.31 2'b10: 0.34 2'b11: 0.38
11:10	RW	0x1	rx_cmfb_gain_5 Set the 5th RX CMFB gain value 2'b00: 0.24 2'b01: 0.31 2'b10: 0.34 2'b11: 0.38
9:8	RW	0x1	rx_cmfb_gain_4 Set the 4th RX CMFB gain value 2'b00: 0.24 2'b01: 0.31 2'b10: 0.34 2'b11: 0.38
7:6	RW	0x1	rx_cmfb_gain_3 Set the 3rd RX CMFB gain value 2'b00: 0.24 2'b01: 0.31 2'b10: 0.34 2'b11: 0.38
5:4	RW	0x1	rx_cmfb_gain_2 Set the 2nd RX CMFB gain value 2'b00: 0.24 2'b01: 0.31 2'b10: 0.34 2'b11: 0.38
3:2	RW	0x1	rx_cmfb_gain_1 Set the 1st RX CMFB gain value 2'b00: 0.24 2'b01: 0.31 2'b10: 0.34 2'b11: 0.38
1:0	RW	0x1	rx_cmfb_gain_0 Set the 0th RX CMFB gain value 2'b00: 0.24 2'b01: 0.31 2'b10: 0.34 2'b11: 0.38

AFE_RX_CMFB_GAIN1

Address: Operational Base + offset (0x000D)

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Bit	Attr	Reset Value	Description
15:14	RW	0x1	rx_cmfb_gain_15 Set the 15th RX CMFB gain value 2'b00: 0.24 2'b01: 0.31 2'b10: 0.34 2'b11: 0.38
13:12	RW	0x1	rx_cmfb_gain_14 Set the 14th RX CMFB gain value 2'b00: 0.24 2'b01: 0.31 2'b10: 0.34 2'b11: 0.38
11:10	RW	0x1	rx_cmfb_gain_13 Set the 13th RX CMFB gain value 2'b00: 0.24 2'b01: 0.31 2'b10: 0.34 2'b11: 0.38
9:8	RW	0x1	rx_cmfb_gain_12 Set the 12th RX CMFB gain value 2'b00: 0.24 2'b01: 0.31 2'b10: 0.34 2'b11: 0.38
7:6	RW	0x1	rx_cmfb_gain_11 Set the 11th RX CMFB gain value 2'b00: 0.24 2'b01: 0.31 2'b10: 0.34 2'b11: 0.38
5:4	RW	0x1	rx_cmfb_gain_10 Set the 10th RX CMFB gain value 2'b00: 0.24 2'b01: 0.31 2'b10: 0.34 2'b11: 0.38
3:2	RW	0x1	rx_cmfb_gain_9 Set the 9th RX CMFB gain value 2'b00: 0.24 2'b01: 0.31 2'b10: 0.34 2'b11: 0.38
1:0	RW	0x1	rx_cmfb_gain_8 Set the 8th RX CMFB gain value 2'b00: 0.24 2'b01: 0.31 2'b10: 0.34 2'b11: 0.38

AFE_RX_GAIN

Address: Operational Base + offset (0x000E)

Bit	Attr	Reset Value	Description
15:6	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
5:4	RW	0x0	rx_cmfb_gain Set RX CMFB gain value. Valid only when RX_SRC=1. 2'b00: 0.28 2'b01: 0.33 2'b10: 0.38 2'b11: 0.42
3:0	RW	0x0	rx_pga_gain Set RX PGA gain value. Valid only when RX_SRC=1. 4'b0000: 1.000 (0.00 dB) 4'b0001: 1.083 (0.70 dB) 4'b0010: 1.174 (1.39 dB) 4'b0011: 1.273 (2.09 dB) 4'b0100: 1.381 (2.80 dB) 4'b0101: 1.500 (3.52 dB) 4'b0110: 1.632 (4.25 dB) 4'b0111: 1.778 (5.00 dB) 4'b1000: 1.941 (5.76 dB) 4'b1001: 2.123 (6.55 dB) 4'b1010: 2.333 (7.36 dB) 4'b1011: 2.571 (8.20 dB) 4'b1100: 2.846 (9.09 dB) 4'b1101: 3.167 (10.01 dB) 4'b1110: 3.546 (10.99 dB) 4'b1111: 4.000 (12.04 dB)

AFE_RX_CTRL0

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
15:6	RO	0x000	reserved
5:4	RW	0x2	rx_ldo_voutsel RX LDO output voltage selection 2'b00: 0.875 2'b01: 0.90 2'b10: 0.95 2'b11: 1.05
3	RO	0x0	reserved
2	RW	0x0	rx_ldo_tst_en RX LDO output voltage test enable signal, high active 1'b0: Disable 1'b1: Enable
1	RW	0x1	rx_ldo_en RX LDO enable signal, high active 1'b0: Disable 1'b1: Enable
0	RW	0x0	rx_ldo_byps RX LDO bypass signal, high active 1'b0: No bypass 1'b1: Bypass

AFE_RX_CTRL1

Address: Operational Base + offset (0x0011)

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Bit	Attr	Reset Value	Description
15:9	RO	0x00	reserved
8	RW	0x0	rx_cdr_phctrl_sel RX CDR phase control selection 1'b0: CDR loop output 1'b1: Manual setting
7:0	RW	0x00	rx_cdr_phctrl_manual RX CDR phase control manual setting, one-hot coding configuration.

AFE_RX_CTRL2

Address: Operational Base + offset (0x0012)

Bit	Attr	Reset Value	Description
15	RO	0x0	reserved
14	RW	0x0	rx_rcosc_ufclamp_en RX RCOSC underflow clamp enable 1'b0: Disable 1'b1: Enable
13	RW	0x0	rx_rcosc_tst_en RX RCOSC output clk test enable 1'b0: Disable 1'b1: Enable
12	RW	0x0	rx_rcosc_offset_subtract RX RCOSC offset value subtract enable 1'b0: Add offset value 1'b1: Subtract offset value
11:8	RW	0x0	rx_rcosc_offsetin RX RCOSC offset value setting
7	RO	0x0	reserved
6	RW	0x0	rx_lpf_lowzeta RX LPF low zeta enable 1'b0: zeta = 0.66 1'b1: zeta = 0.33
5:4	RW	0x1	rx_lpfpga_isel LPF/PGA OP bias current selection 2'b00: 7.5uA 2'b01: 10uA 2'b10: 12.5uA 2'b11: 15uA
3	RW	0x0	rx_lpfgain_sel RX LPF gain selection 1'b0: low gain 1'b1: high gain
2	RW	0x0	rx_itst_en RX current test enable 1'b0: disable ibias test 1'b1: enable ibias test
1	RW	0x0	rx_tst_en RX inside signal test enable, MUX signal to pad PAD_TST_INOUT 1'b0: Disable, digital path gate to 0, analog path High-Z 1'b1: Enable

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Bit	Attr	Reset Value	Description
0	RW	0x0	rx_vcm_src_sel RX vcm voltage source selection 1'b0: Internal voltage 1'b1: External voltage

AFE_RX_CTRL3

Address: Operational Base + offset (0x0013)

Bit	Attr	Reset Value	Description
15	RO	0x0	reserved
14:12	RW	0x4	rx_ctle_isel RX CTLE current bias value selection 3'b000: 10uA 3'b001: 20uA 3'b010: 30uA 3'b011: 40uA 3'b100: 50uA 3'b101: 60uA 3'b110: 70uA 3'b111: 80uA
11:10	RO	0x0	reserved
9:8	RW	0x1	rx_ctle_dc_gain RX CTLE DC gain setting 2'b00: -3dB 2'b01: -0.9dB 2'b10: 1.5dB 2'b11: 4.2dB
7:4	RW	0x0	rx_ctle_ac_gain RX CTLE AC gain setting 4'h0: -1.8dB 4'h1: 1.3dB 4'h2: 4.2dB 4'h3: 6.4dB 4'h4: 8.2dB 4'h5: 9.7dB 4'h6: 11dB 4'h7: 12dB 4'h8: 13dB 4'h9: 14.5dB 4'ha: 15.7dB 4'hb: 16.7dB 4'hc: 17.5dB 4'hd: 18.5dB 4'he: 19.2dB 4'hf: 20dB
3:2	RO	0x0	reserved
1	RW	0x0	rx_ctle_isrc_sel RX CTLE current source generation selection 1'b0: From constant-gm bias current 1'b1: From vbg/r bias current
0	RW	0x1	rx_ctle_en RX CTLE enable signal 1'b0: CTLE disable, LPF enable 1'b1: CTLE enable, LPF disable

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AFE_RX_CTRL4

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
15:8	RW	0x00	rx_adc_tst_sel RX ADC test selection RX_ADC_TST_SEL[7]: connect to GPIO input TST_OE EPHY digital signal test path Output Tri-state control: 1'b0: Output hiz, PAD_TST_INOUT used as analog signal test pad 1'b1: Normal mode, PAD_TST_INPUT used as digital signal test pad RX_ADC_TST_SEL[6]: connect to GPIO input TST_OD EPHY digital signal test path open drain function: 1'b0: Digital signal test normal mode 1'b1: Digital signal test Open drain mode
7:6	RO	0x0	reserved
5:4	RW	0x3	rx_adcop_isel ADC OP bias current selection 2'b00: 10uA 2'b01: 15uA 2'b10: 20uA 2'b11: 25uA
3:1	RO	0x0	reserved
0	RW	0x0	rx_adc_tst_en ADC test enable control 1'b0: Disable 1'b1: Enable

AFE_RX_CTRL5

Address: Operational Base + offset (0x0015)

Bit	Attr	Reset Value	Description
15:12	RO	0x0	reserved
11:10	RW	0x0	rx_dac_cur_sel RX BLW DAC output current ratio selector 2'b00: 1:1.5 2'b01: 1:2.0 2'b10: 1:2.5 2'b11: 1:3.0
9:8	RW	0x0	rx_dac_bias_sel RX BLW DAC input current bias selection 2'b00: 10uA 2'b01: 12.5uA 2'b10: 15uA 2'b11: 17.5uA
7	RO	0x0	reserved
6:4	RW	0x2	rx_adc_vrefsel [1:0] RX ADC Vref selection 2'b00: 450mV 2'b10: 500mV 2'b01: 550mV 2'b11: 600mV [2] reuse as RX ADC OP 1st stage output VCM selection
3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2:0	RW	0x3	rx_adc_vcmsel RX ADC OP 1st stage output VCM selection.

AFE_RX_CTRL6

Address: Operational Base + offset (0x0016)

Bit	Attr	Reset Value	Description
15:12	RO	0x0	reserved
11	RW	0x0	rx_sqtrim_vcm_sel RX Squelch comp offset trimming vcm selection 1'b0: input signal vcm 1'b1: internal generated vcm
10	RW	0x0	rx_sqtrim_ck_sel RX Squelch comp offset trimming clk selection 1'b0: ref clk 1'b1: ref clk div4
9:8	RW	0x1	rx_sqcmp_data_isel RX Squelch comp current bias selection 2'b00: 5uA 2'b01: 10uA 2'b10: 15uA 2'b11: 20uA
7:6	RW	0x0	rx_sqtrim_mon_sel Select trim code on digital test point 2'b00: TX cmp2 2'b01: TX cmp1 2'b10: RX cmp2 2'b11: RX cmp1
5	RW	0x0	rx_sq_trim_en RX SQ comp offset trim enable 1'b0: Disable 1'b1: Enable
4	RW	0x0	rx_sq_cmptrim_byps RX SQ comp offset trim bypass 1'b0: No bypass 1'b1: Bypass
3	RO	0x0	reserved
2:0	RW	0x4	rx_sq_ref_sel Adjust RX Squelch reference voltage Vref Vref_data 3'b000: 0.15 0.034 3'b001: 0.17 0.038 3'b010: 0.194 0.044 3'b011: 0.229 0.052 3'b100: 0.279 0.063 3'b101: 0.313 0.071 3'b110: 0.356 0.080 3'b111: 0.461 0.093 Vref used for nqse/nqse_x and pqse/pqse_x. Vref_data used for tpp/tpp_x and tpm/tpm_x.

AFE_RX_CTRL7

Address: Operational Base + offset (0x0017)

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Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12:8	RW	0x00	rx_sqtrim_ext_n RX Squelch trimming code manual setting
7:5	RO	0x0	reserved
4:0	RW	0x00	rx_sqtrim_ext_p RX Squelch trimming code manual setting

AFE_RX_CTRL8

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12:8	RW	0x00	rx_sqtrim_ext_n_x RX Squelch trimming code manual setting
7:5	RO	0x0	reserved
4:0	RW	0x00	rx_sqtrim_ext_p_x RX Squelch trimming code manual setting

AFE_RX_CTRL9

Address: Operational Base + offset (0x0019)

Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12:8	RW	0x00	rx_100btsig_trim_ext RX 100BT signal detect comparator offset trimming code manual setting
7:6	RO	0x0	reserved
5:4	RW	0x2	rx_100btsig_cmp_isel RX 100BT signal detect comp current selection 2'b00: 150uA 2'b01: 195uA 2'b10: 255uA 2'b11: 300uA
3	RW	0x0	rx_100btsig_trim_vcm_sel RX 100BT signal detect comp offset trimming vcm selection 1'b0: input signal vcm 1'b1: internal generated vcm
2	RW	0x0	rx_100btsig_trim_ck_sel RX 100BT signal detect comp offset trimming clock selection 1'b0: ref clock 1'b1: ref clock div4
1	RW	0x0	rx_100btsig_trim_byps RX 100BT signal detect comparator offset trimming bypass 1'b0: No bypass 1'b1: Bypass
0	RW	0x0	rx_100btsig_trim_en RX 100BT signal detect comparator offset trimming enable 1'b0: Disable 1'b1: Enable

AFE_RX_CTRL10

Address: Operational Base + offset (0x001A)

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	rx_tst_digsel RX digital signal test selection
7:0	RW	0x00	rx_tst_anasel RX analog signal test selection

AFE_RX_CTRL11

Address: Operational Base + offset (0x001B)

Bit	Attr	Reset Value	Description
15:0	RW	0xa815	rx_spare [1:0]: RX ADC stage5/6 op current control 2'b00: 10uA 2'b01: 15uA 2'b10: 20uA 2'b11: 25uA [3:2]: RX ADC stage3/4 op current control 2'b00: 10uA 2'b01: 15uA 2'b10: 20uA 2'b11: 25uA [5:4]: RX ADC stage1/2 op current control 2'b00: 10uA 2'b01: 15uA 2'b10: 20uA 2'b11: 25uA [6]: RX ADC stage5/6 op current double enable [7]: RX ADC stage3/4 op current double enable [8]: RX ADC stage1/2 op current double enable [9]: RX ADC sh op current double enable [10]: RX ADC vref gen op current double enable [11]: TX current boost enable [13:12]: RX ADC stage3/4 op 1st stage common mode current control [15:14]: RX ADC stage5/6 op 1st stage common mode current control

AFE_RX_CTRL12

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
15:8	RW	0x00	tst_dig_sel Digital signal test selection
7:0	RW	0x00	tst_ana_sel Analog signal test selection

AFE_RX_CTRL13

Address: Operational Base + offset (0x001D)

Bit	Attr	Reset Value	Description
15:1	RO	0x0000	reserved
0	RW	0x0	tst_mode Analog test Mode enable 1'b0: Disable 1'b1: Enable

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AFE_RX_STATUS0

Address: Operational Base + offset (0x001E)

Bit	Attr	Reset Value	Description
15:8	RO	0x00	reserved
7:0	RO	0x00	rx_cdr_phctrl_mon RX CDR phase status monitor

AFE_RX_STATUS1

Address: Operational Base + offset (0x001F)

Bit	Attr	Reset Value	Description
15	RO	0x0	rx_100btsig_trim_dpass RX 100BT signal detect comparator offset trimming pass monitor
14:13	RO	0x0	reserved
12:8	RO	0x00	rx_100btsig_trim_mon RX 100BT signal detect comparator offset trimming results monitor
7:5	RO	0x0	reserved
4:0	RO	0x00	rx_sqtrim_mon RX SQ comp offset trimming results monitor

43.4.12 Registers Summary for DSP_1

Name	Offset	Size	Reset Value	Description
DSP_1_AMP_THR_8	0x0000	HW	0x000001A2	Amplitude Threshold Register 8
DSP_1_AMP_THR_9	0x0001	HW	0x00000187	Amplitude Threshold Register 9
DSP_1_AMP_THR_10	0x0002	HW	0x00000167	Amplitude Threshold Register 10
DSP_1_AMP_THR_11	0x0003	HW	0x0000014C	Amplitude Threshold Register 11
DSP_1_AMP_THR_12	0x0004	HW	0x00000137	Amplitude Threshold Register 12
DSP_1_AMP_THR_13	0x0005	HW	0x0000011C	Amplitude Threshold Register 13
DSP_1_AMP_THR_14	0x0006	HW	0x0000010B	Amplitude Threshold Register 14
DSP_1_AMP_THR_15	0x0007	HW	0x000000FA	Amplitude Threshold Register 15
DSP_1_ENERGY_OFF_LEVEL_1_L	0x0008	HW	0x00008888	Energy on Level Low Register 1
DSP_1_ENERGY_OFF_LEVEL_1_H	0x0009	HW	0x00008888	Energy on Level High Register 1
DSP_1_BINIT_1_L	0x000A	HW	0x00003333	BINIT Low Register 1
DSP_1_BINIT_1_H	0x000B	HW	0x00003333	BINIT High Register 1
DSP_1_FEQ2_RSTVAL_1STFRAC	0x000C	HW	0x00000000	FEQ2 Initial Value - 1st Fractional Part Register
DSP_1_CTLE_LPF_THR_SEL	0x000D	HW	0x000011F4	CTLE and LPF Threshold and Enable Register
DSP_1_CTLE_GIAN_0123	0x000E	HW	0x00004321	CTLE Gain Register 0
DSP_1_CTLE_GIAN_4567	0x000F	HW	0x00007765	CTLE Gain Register 1

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Name	Offset	Size	Reset Value	Description
DSP_1_CTLE_GIAN_8to11	0x0010	HW	0x0000A988	CTLE Gain Register 2
DSP_1_CTLE_GIAN_12to15	0x0011	HW	0x0000EDCB	CTLE Gain Register 3
DSP_1_CTLE_GAIN_DFT	0x0015	HW	0x00000001	Default CTLE Gain Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

43.4.13 Detail Registers Description for DSP_1

DSP_1_AMP_THR_8

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10:0	RW	0x1a2	amp_thresh_8 8th amplitude threshold, providing appropriate adaptive parameters according to the threshold.

DSP_1_AMP_THR_9

Address: Operational Base + offset (0x0001)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10:0	RW	0x187	amp_thresh_9 9th amplitude threshold, providing appropriate adaptive parameters according to the threshold.

DSP_1_AMP_THR_10

Address: Operational Base + offset (0x0002)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10:0	RW	0x167	amp_thresh_10 10th amplitude threshold, providing appropriate adaptive parameters according to the threshold.

DSP_1_AMP_THR_11

Address: Operational Base + offset (0x0003)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10:0	RW	0x14c	amp_thresh_11 11th amplifier threshold, determines the reset coefficient value of Feed Forward Equalizer.

DSP_1_AMP_THR_12

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10:0	RW	0x137	amp_thresh_12 12th amplitude threshold, providing appropriate adaptive parameters according to the threshold.

DSP_1_AMP_THR_13

Address: Operational Base + offset (0x0005)

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Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10:0	RW	0x11c	amp_thresh_13 13th amplitude threshold, providing appropriate adaptive parameters according to the threshold.

DSP_1_AMP_THR_14

Address: Operational Base + offset (0x0006)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10:0	RW	0x10b	amp_thresh_14 14th amplitude threshold, providing appropriate adaptive parameters according to the threshold.

DSP_1_AMP_THR_15

Address: Operational Base + offset (0x0007)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10:0	RW	0x0fa	amp_thresh_15 15th amplitude threshold, providing appropriate adaptive parameters according to the threshold.

DSP_1_ENERGY_OFF_LEVEL_1_L

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
15:12	RW	0x8	off_energy_level_11 Set the off energy threshold value according to the self-adapting gain value. Select this value when the 11th gain is selected. Data format: 4 bit decimal, and starting with percentiles.
11:8	RW	0x8	off_energy_level_10 Set the off energy threshold value according to the self-adapting gain value. Select this value when the 10th gain is selected. Data format: 4 bit decimal, and starting with percentiles.
7:4	RW	0x8	off_energy_level_9 Set the off energy threshold value according to the self-adapting gain value. Select this value when the 9th gain is selected. Data format: 4 bit decimal, and starting with percentiles.
3:0	RW	0x8	off_energy_level_8 Set the off energy threshold value according to the self-adapting gain value. Select this value when the 8th gain is selected. Data format: 4 bit decimal, and starting with percentiles.

DSP_1_ENERGY_OFF_LEVEL_1_H

Address: Operational Base + offset (0x0009)

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Bit	Attr	Reset Value	Description
15:12	RW	0x8	off_energy_level_15 Set the off energy threshold value according to the self-adapting gain value. Select this value when the 12th gain is selected. Data format: 4 bit decimal, and starting with percentiles.
11:8	RW	0x8	off_energy_level_14 Set the off energy threshold value according to the self-adapting gain value. Select this value when the 12th gain is selected. Data format: 4 bit decimal, and starting with percentiles.
7:4	RW	0x8	off_energy_level_13 Set the off energy threshold value according to the self-adapting gain value. Select this value when the 12th gain is selected. Data format: 4 bit decimal, and starting with percentiles.
3:0	RW	0x8	off_energy_level_12 Set the off energy threshold value according to the self-adapting gain value. Select this value when the 12th gain is selected. Data format: 4 bit decimal, and starting with percentiles.

DSP_1_BINIT_1_L

Address: Operational Base + offset (0x000A)

Bit	Attr	Reset Value	Description
15:12	RW	0x3	binit11 Set reset coefficient value of Feed Forward Equalizer, according to the self-adapting gain value. Select this value when the 11th gain is selected. Data format: 4 bit integer.
11:8	RW	0x3	binit10 Set reset coefficient value of Feed Forward Equalizer, according to the self-adapting gain value. Select this value when the 10th gain is selected. Data format: 4 bit integer.
7:4	RW	0x3	binit9 Set reset coefficient value of Feed Forward Equalizer, according to the self-adapting gain value. Select this value when the 9th gain is selected. Data format: 4 bit integer.
3:0	RW	0x3	binit8 Set reset coefficient value of Feed Forward Equalizer, according to the self-adapting gain value. Select this value when the 8th gain is selected. Data format: 4 bit integer.

DSP_1_BINIT_1_H

Address: Operational Base + offset (0x000B)

Bit	Attr	Reset Value	Description
15:12	RW	0x3	binit15 Set reset coefficient value of Feed Forward Equalizer, according to the self-adapting gain value. Select this value when the 15th gain is selected. Data format: 4 bit integer.
11:8	RW	0x3	binit14 Set reset coefficient value of Feed Forward Equalizer, according to the self-adapting gain value. Select this value when the 14th gain is selected. Data format: 4 bit integer.

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Bit	Attr	Reset Value	Description
7:4	RW	0x3	binit13 Set reset coefficient value of Feed Forward Equalizer, according to the self-adapting gain value. Select this value when the 13th gain is selected. Data format: 4 bit integer.
3:0	RW	0x3	binit12 Set reset coefficient value of Feed Forward Equalizer, according to the self-adapting gain value. Select this value when the 12th gain is selected. Data format: 4 bit integer.

DSP_1_FEQ2_RSTVAL_1STFRAC

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	feq2_rstval_1stfrac The first fractional part of the FEQ2 initial value of each auto-gain gear. For example, 16'h1 means that the initial fraction of the FEQ2 coefficient corresponding to the first gain value is 0.5. 16'h3 means that the initial fraction of the FEQ2 coefficient corresponding to the first gain value and the second gain value is 0.5.

DSP_1_CTLE_LPF_THR_SEL

Address: Operational Base + offset (0x000D)

Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12	RW	0x1	ctle_auto_gain_en The CTLE gain gear is automatically selected based on the cable length. 1'b0: Disable 1'b1: Enable
11	RW	0x0	ctle_auto_use_en Automatically switch between CTLE and LPF modes based on cable length. 1'b0: Disable 1'b1: Enable
10:0	RW	0x1f4	ctle_lpf_thr Automatic switching threshold for CTLE and LPF modes.

DSP_1_CTLE_GIAN_0123

Address: Operational Base + offset (0x000E)

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Bit	Attr	Reset Value	Description
15:12	RW	0x4	ctle_gain3 Set 3rd RX CTLE AC gain value 4'h0: -1.8dB 4'h1: 1.3dB 4'h2: 4.2dB 4'h3: 6.4dB 4'h4: 8.2dB 4'h5: 9.7dB 4'h6: 11dB 4'h7: 12dB 4'h8: 13dB 4'h9: 14.5dB 4'ha: 15.7dB 4'hb: 16.7dB 4'hc: 17.5dB 4'hd: 18.5dB 4'he: 19.2dB 4'hf: 20dB
11:8	RW	0x3	ctle_gain2 Set 2nd RX CTLE AC gain value 4'h0: -1.8dB 4'h1: 1.3dB 4'h2: 4.2dB 4'h3: 6.4dB 4'h4: 8.2dB 4'h5: 9.7dB 4'h6: 11dB 4'h7: 12dB 4'h8: 13dB 4'h9: 14.5dB 4'ha: 15.7dB 4'hb: 16.7dB 4'hc: 17.5dB 4'hd: 18.5dB 4'he: 19.2dB 4'hf: 20dB
7:4	RW	0x2	ctle_gain1 Set 1st RX CTLE AC gain value 4'h0: -1.8dB 4'h1: 1.3dB 4'h2: 4.2dB 4'h3: 6.4dB 4'h4: 8.2dB 4'h5: 9.7dB 4'h6: 11dB 4'h7: 12dB 4'h8: 13dB 4'h9: 14.5dB 4'ha: 15.7dB 4'hb: 16.7dB 4'hc: 17.5dB 4'hd: 18.5dB 4'he: 19.2dB 4'hf: 20dB

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Bit	Attr	Reset Value	Description
3:0	RW	0x1	ctle_gain0 Set 0th RX CTLE AC gain value 4'h0: -1.8dB 4'h1: 1.3dB 4'h2: 4.2dB 4'h3: 6.4dB 4'h4: 8.2dB 4'h5: 9.7dB 4'h6: 11dB 4'h7: 12dB 4'h8: 13dB 4'h9: 14.5dB 4'ha: 15.7dB 4'hb: 16.7dB 4'hc: 17.5dB 4'hd: 18.5dB 4'he: 19.2dB 4'hf: 20dB

DSP_1_CTLE_GIAN_4567

Address: Operational Base + offset (0x000F)

Bit	Attr	Reset Value	Description
15:12	RW	0x7	ctle_gain7 Set 7th RX CTLE AC gain value 4'h0: -1.8dB 4'h1: 1.3dB 4'h2: 4.2dB 4'h3: 6.4dB 4'h4: 8.2dB 4'h5: 9.7dB 4'h6: 11dB 4'h7: 12dB 4'h8: 13dB 4'h9: 14.5dB 4'ha: 15.7dB 4'hb: 16.7dB 4'hc: 17.5dB 4'hd: 18.5dB 4'he: 19.2dB 4'hf: 20dB

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Bit	Attr	Reset Value	Description
11:8	RW	0x7	ctle_gain6 Set 6th RX CTLE AC gain value 4'h0: -1.8dB 4'h1: 1.3dB 4'h2: 4.2dB 4'h3: 6.4dB 4'h4: 8.2dB 4'h5: 9.7dB 4'h6: 11dB 4'h7: 12dB 4'h8: 13dB 4'h9: 14.5dB 4'ha: 15.7dB 4'hb: 16.7dB 4'hc: 17.5dB 4'hd: 18.5dB 4'he: 19.2dB 4'hf: 20dB
7:4	RW	0x6	ctle_gain5 Set 5th RX CTLE AC gain value 4'h0: -1.8dB 4'h1: 1.3dB 4'h2: 4.2dB 4'h3: 6.4dB 4'h4: 8.2dB 4'h5: 9.7dB 4'h6: 11dB 4'h7: 12dB 4'h8: 13dB 4'h9: 14.5dB 4'ha: 15.7dB 4'hb: 16.7dB 4'hc: 17.5dB 4'hd: 18.5dB 4'he: 19.2dB 4'hf: 20dB
3:0	RW	0x5	ctle_gain4 Set 4th RX CTLE AC gain value 4'h0: -1.8dB 4'h1: 1.3dB 4'h2: 4.2dB 4'h3: 6.4dB 4'h4: 8.2dB 4'h5: 9.7dB 4'h6: 11dB 4'h7: 12dB 4'h8: 13dB 4'h9: 14.5dB 4'ha: 15.7dB 4'hb: 16.7dB 4'hc: 17.5dB 4'hd: 18.5dB 4'he: 19.2dB 4'hf: 20dB

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DSP_1_CTLE_GIAN_8to11

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
15:12	RW	0xa	ctle_gain11 Set 11th RX CTLE AC gain value 4'h0: -1.8dB 4'h1: 1.3dB 4'h2: 4.2dB 4'h3: 6.4dB 4'h4: 8.2dB 4'h5: 9.7dB 4'h6: 11dB 4'h7: 12dB 4'h8: 13dB 4'h9: 14.5dB 4'ha: 15.7dB 4'hb: 16.7dB 4'hc: 17.5dB 4'hd: 18.5dB 4'he: 19.2dB 4'hf: 20dB
11:8	RW	0x9	ctle_gain10 Set 10th RX CTLE AC gain value 4'h0: -1.8dB 4'h1: 1.3dB 4'h2: 4.2dB 4'h3: 6.4dB 4'h4: 8.2dB 4'h5: 9.7dB 4'h6: 11dB 4'h7: 12dB 4'h8: 13dB 4'h9: 14.5dB 4'ha: 15.7dB 4'hb: 16.7dB 4'hc: 17.5dB 4'hd: 18.5dB 4'he: 19.2dB 4'hf: 20dB

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Bit	Attr	Reset Value	Description
7:4	RW	0x8	ctle_gain9 Set 9th RX CTLE AC gain value 4'h0: -1.8dB 4'h1: 1.3dB 4'h2: 4.2dB 4'h3: 6.4dB 4'h4: 8.2dB 4'h5: 9.7dB 4'h6: 11dB 4'h7: 12dB 4'h8: 13dB 4'h9: 14.5dB 4'ha: 15.7dB 4'hb: 16.7dB 4'hc: 17.5dB 4'hd: 18.5dB 4'he: 19.2dB 4'hf: 20dB
3:0	RW	0x8	ctle_gain8 Set 8th RX CTLE AC gain value 4'h0: -1.8dB 4'h1: 1.3dB 4'h2: 4.2dB 4'h3: 6.4dB 4'h4: 8.2dB 4'h5: 9.7dB 4'h6: 11dB 4'h7: 12dB 4'h8: 13dB 4'h9: 14.5dB 4'ha: 15.7dB 4'hb: 16.7dB 4'hc: 17.5dB 4'hd: 18.5dB 4'he: 19.2dB 4'hf: 20dB

DSP_1_CTLE_GIAN_12to15

Address: Operational Base + offset (0x0011)

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Bit	Attr	Reset Value	Description
15:12	RW	0xe	ctle_gain15 Set 15th RX CTLE AC gain value 4'h0: -1.8dB 4'h1: 1.3dB 4'h2: 4.2dB 4'h3: 6.4dB 4'h4: 8.2dB 4'h5: 9.7dB 4'h6: 11dB 4'h7: 12dB 4'h8: 13dB 4'h9: 14.5dB 4'ha: 15.7dB 4'hb: 16.7dB 4'hc: 17.5dB 4'hd: 18.5dB 4'he: 19.2dB 4'hf: 20dB
11:8	RW	0xd	ctle_gain14 Set 14th RX CTLE AC gain value 4'h0: -1.8dB 4'h1: 1.3dB 4'h2: 4.2dB 4'h3: 6.4dB 4'h4: 8.2dB 4'h5: 9.7dB 4'h6: 11dB 4'h7: 12dB 4'h8: 13dB 4'h9: 14.5dB 4'ha: 15.7dB 4'hb: 16.7dB 4'hc: 17.5dB 4'hd: 18.5dB 4'he: 19.2dB 4'hf: 20dB
7:4	RW	0xc	ctle_gain13 Set 13th RX CTLE AC gain value 4'h0: -1.8dB 4'h1: 1.3dB 4'h2: 4.2dB 4'h3: 6.4dB 4'h4: 8.2dB 4'h5: 9.7dB 4'h6: 11dB 4'h7: 12dB 4'h8: 13dB 4'h9: 14.5dB 4'ha: 15.7dB 4'hb: 16.7dB 4'hc: 17.5dB 4'hd: 18.5dB 4'he: 19.2dB 4'hf: 20dB

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Bit	Attr	Reset Value	Description
3:0	RW	0xb	ctle_gain12 Set 12th RX CTLE AC gain value 4'h0: -1.8dB 4'h1: 1.3dB 4'h2: 4.2dB 4'h3: 6.4dB 4'h4: 8.2dB 4'h5: 9.7dB 4'h6: 11dB 4'h7: 12dB 4'h8: 13dB 4'h9: 14.5dB 4'ha: 15.7dB 4'hb: 16.7dB 4'hc: 17.5dB 4'hd: 18.5dB 4'he: 19.2dB 4'hf: 20dB

DSP_1_CTLE_GAIN_DFT

Address: Operational Base + offset (0x0015)

Bit	Attr	Reset Value	Description
15:4	RO	0x000	reserved
3:0	RW	0x1	default_gain Set default RX CTLE AC gain value, for energy detection status. 4'h0: -1.8dB 4'h1: 1.3dB 4'h2: 4.2dB 4'h3: 6.4dB 4'h4: 8.2dB 4'h5: 9.7dB 4'h6: 11dB 4'h7: 12dB 4'h8: 13dB 4'h9: 14.5dB 4'ha: 15.7dB 4'hb: 16.7dB 4'hc: 17.5dB 4'hd: 18.5dB 4'he: 19.2dB 4'hf: 20dB

43.4.14 Registers Summary for DSP_ST

Name	Offset	Size	Reset Value	Description
DSP_ST_TST_MODE_OUT	0x0000	W	0x00000000	Test Mode Output Register
DSP_ST_FEQ1_COEFF	0x0001	W	0x00000000	FEQ1 Coefficient Register
DSP_ST_FEQ2_COEFF	0x0002	W	0x00000000	FEQ2 Coefficient Register
DSP_ST_DFE1_COEFF	0x0003	W	0x00000000	DFE1 Coefficient Register
DSP_ST_DFE2_COEFF	0x0004	W	0x00000000	DFE2 Coefficient Register
DSP_ST_DFE3_COEFF	0x0005	W	0x00000000	DFE3 Coefficient Register
DSP_ST_DFE4_COEFF	0x0006	W	0x00000000	DFE4 Coefficient Register
DSP_ST_DFE5_COEFF	0x0007	W	0x00000000	DFE5 Coefficient Register

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Name	Offset	Size	Reset Value	Description
DSP_ST_DFE6_COEFF	0x0008	W	0x00000000	DFE6 Coefficient Register
DSP_ST_DFE7_COEFF	0x0009	W	0x00000000	DFE7 Coefficient Register
DSP_ST_DFE8_COEFF	0x000A	W	0x00000000	DFE8 Coefficient Register
DSP_ST_DFE9_COEFF	0x000B	W	0x00000000	DFE9 Coefficient Register
DSP_ST_DFE10_COEFF	0x000C	W	0x00000000	DFE10 Coefficient Register
DSP_ST_DFE11_COEFF	0x000D	W	0x00000000	DFE11 Coefficient Register
DSP_ST_DFE12_COEFF	0x000E	W	0x00000000	DFE12 Coefficient Register
DSP_ST_EQ_OUT_P2	0x000F	W	0x00000000	Output Sum of the Penultimate Equalizers Register
DSP_ST_DSP_PARM_QUERY1	0x0010	W	0x00000000	Parameter Query Register 1
DSP_ST_DSP_PARM_QUERY2	0x0011	W	0x00000000	Parameter Query Register 2
DSP_ST_DSP_PARM_QUERY3	0x0012	W	0x00000000	Parameter Query Register 3
DSP_ST_DSP_PARM_QUERY4	0x0013	W	0x00000000	Parameter Query Register 4
DSP_ST_A3_CONFIG	0x0014	W	0x00000000	Analog Receiver Common Mode and DAC Configuration Register
DSP_ST_A4_CONFIG	0x0015	W	0x00000000	Central Bias Configuration Register 1
DSP_ST_A5_CONFIG	0x0016	W	0x00000000	Transmitter Configuration Register
DSP_ST_A6_CONFIG	0x0017	W	0x00000000	PLL Configuration Register 1
DSP_ST_TM_PARM_QUERY1	0x0018	W	0x00000000	Parameter from Timing Module Register 1
DSP_ST_TM_PARM_QUERY2	0x0019	W	0x00000000	Parameter from Timing Module Register 2
DSP_ST_TM_PARM_QUERY3	0x001A	W	0x00000000	Parameter from Timing Module Register 3
DSP_ST_TM_PARM_QUERY4	0x001B	W	0x00000000	Parameter from Timing Module Register 4
DSP_ST_ABS_X_ACC_INT	0x001C	W	0x00000000	ADC Sampling Absolute Sum Register
DSP_ST_DFE13_COEFF	0x001D	W	0x00000000	DFE13 Coefficient Register
DSP_ST_DFE14_15_COEFF	0x001E	W	0x00000000	DFE14 and DFE15 Coefficient Register
DSP_ST_DFE16_17_COEFF	0x001F	W	0x00000000	DFE16 and DFE17 Coefficient Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

43.4.15 Detail Registers Description for DSP_ST

DSP_ST_TST_MODE_OUT

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
20:17	RW	0x0	ctle_gain Adaptive CTLE gain value 4'h0: -1.8dB 4'h1: 1.3dB 4'h2: 4.2dB 4'h3: 6.4dB 4'h4: 8.2dB 4'h5: 9.7dB 4'h6: 11dB 4'h7: 12dB 4'h8: 13dB 4'h9: 14.5dB 4'ha: 15.7dB 4'hb: 16.7dB 4'hc: 17.5dB 4'hd: 18.5dB 4'he: 19.2dB 4'hf: 20dB
16	RO	0x0	energy_detect 1'b0: The detected ADC amplitude does not meet the requirements. 1'b1: The detected ADC amplitude meets the requirements.
15	RO	0x0	mlt3_zero_violation 1'b0: Normal 1'b1: The DSP decision value equals 0 for 64 consecutive periods.
14	RO	0x0	off_energy_detect 1'b0: Normal 1'b1: The ADC amplitude is detected to be less than the threshold.
13	RO	0x0	blw_valid 1'b0: The BLW module is not working 1'b1: Baseline wander valid
12	RO	0x0	time_out_violation 1'b0: Normal 1'b1: DSP adaptation time is greater than 0.917ms.
11	RO	0x0	feq_coeff_is_small 1'b0: Normal 1'b1: The adaptive result of FEQ2 coefficient is less than the threshold value.
10:9	RO	0x0	state DSP working state 2'b00: Searching for energy 2'b01: Searching for optimal gain 2'b10: Allowing for adaptation Others: Reserved
8	RO	0x0	blw_valid 1'b0: The BLW module is not working 1'b1: Baseline wander valid
7	RO	0x0	off_energy_detect 1'b0: Normal 1'b1: The ADC amplitude is detected to be less than the threshold.

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Bit	Attr	Reset Value	Description
6	RO	0x0	allow_transition_2st1 Energy detecting meets needs, and the state machine changes from state 0 to state 1.
5:2	RO	0x0	gain_pre The pre-gain value adapts to the network cable length.
1:0	RO	0x0	state DSP working state 2'b00: Searching for energy 2'b01: Searching for optimal gain 2'b10: Allowing for adaptation Others: Reserved

DSP_ST_FEQ1_COEFF

Address: Operational Base + offset (0x0001)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:0	RO	0x000000	feq1_coeff The adaptive coefficient value of the 1st FEQ

DSP_ST_FEQ2_COEFF

Address: Operational Base + offset (0x0002)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:0	RO	0x000000	feq2_coeff The adaptive coefficient value of the 2nd FEQ

DSP_ST_DFE1_COEFF

Address: Operational Base + offset (0x0003)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	dfe1_coeff The adaptive coefficient value of the DFE1

DSP_ST_DFE2_COEFF

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	dfe2_coeff The adaptive coefficient value of the DFE2

DSP_ST_DFE3_COEFF

Address: Operational Base + offset (0x0005)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	dfe3_coeff The adaptive coefficient value of the DFE3

DSP_ST_DFE4_COEFF

Address: Operational Base + offset (0x0006)

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Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	dfe4_coeff The adaptive coefficient value of the DFE4

DSP_ST_DFE5_COEFF

Address: Operational Base + offset (0x0007)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	dfe5_coeff The adaptive coefficient value of the DFE5

DSP_ST_DFE6_COEFF

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	dfe6_coeff The adaptive coefficient value of the DFE6

DSP_ST_DFE7_COEFF

Address: Operational Base + offset (0x0009)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	dfe7_coeff The adaptive coefficient value of the DFE7

DSP_ST_DFE8_COEFF

Address: Operational Base + offset (0x000A)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	dfe8_coeff The adaptive coefficient value of the DFE8

DSP_ST_DFE9_COEFF

Address: Operational Base + offset (0x000B)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	dfe9_coeff The adaptive coefficient value of the DFE9

DSP_ST_DFE10_COEFF

Address: Operational Base + offset (0x000C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	dfe10_coeff The adaptive coefficient value of the DFE10

DSP_ST_DFE11_COEFF

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Address: Operational Base + offset (0x000D)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	dfe11_coeff The adaptive coefficient value of the DFE11

DSP_ST_DFE12_COEFF

Address: Operational Base + offset (0x000E)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	dfe12_coeff The adaptive coefficient value of the DFE12

DSP_ST_EQ_OUT_P2

Address: Operational Base + offset (0x000F)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	eq_out_p2 Output result of the penultimate equalizer

DSP_ST_DSP_PARM_QUERY1

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:14	RO	0x0	dec_nm1_real Decision result
13:7	RO	0x00	err_nm1_real_6Q5 The error between the decision and the actual value
6:0	RO	0x00	x_diff Differential ADC input

DSP_ST_DSP_PARM_QUERY2

Address: Operational Base + offset (0x0011)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:15	RO	0x000	violation_count Violation count
14:8	RO	0x00	abs_err_nm1 The absolute error between the decision and the actual value
7	RO	0x0	violation_state 1'b0: The decision result does not accord with mlt3 difference law 1'b1: The decision result accords with mlt3 difference law
6:0	RO	0x00	abs_max_err Absolute value of the maximum error

DSP_ST_DSP_PARM_QUERY3

Address: Operational Base + offset (0x0012)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
21:20	RO	0x0	a1_config[15:14] Analog version
19:16	RO	0x0	reserved
15:0	RO	0x0000	fx_or_norm Optical fiber or normal mode output It is intended to use address[1] to control whether the output result is the fiber result or the normal mode result, but the actual value cannot be set to normal mode.

DSP_ST_DSP_PARM_QUERY4

Address: Operational Base + offset (0x0013)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:15	RO	0x00	a2_config[15:8] See A2_CONFIG[15:8]
14	RO	0x0	a2_config[0] Receiver Source 1'b0: Receiver block inputs are controlled by the digital state machines (normal mode). 1'b1: Receiver block inputs are controlled by register A2_CONFIG bits
13:0	RO	0x0000	feq_out2 FEQ2 output

DSP_ST_A3_CONFIG

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	a3_config See A3_CONFIG

DSP_ST_A4_CONFIG

Address: Operational Base + offset (0x0015)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	a4_config See A4_CONFIG

DSP_ST_A5_CONFIG

Address: Operational Base + offset (0x0016)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RO	0x0000	a5_config See A5_CONFIG

DSP_ST_A6_CONFIG

Address: Operational Base + offset (0x0017)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15:0	RO	0x0000	a6_config See A6_CONFIG

DSP_ST_TM_PARM_QUERY1

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RO	0x0	many_violation The violation of the DSP result exceeded the threshold. Real-time update.
20	RO	0x0	zero_violation There is no violation of the DSP decision. Real-time update.
19:0	RO	0x00000	df_reg Frequency drift, real-time update

DSP_ST_TM_PARM_QUERY2

Address: Operational Base + offset (0x0019)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RO	0x0	data_valid The DSP adaptive process is complete
20	RO	0x0	sign_bit When a violation is judged, the clock phase will move in one direction several times in succession, and then continuously in the other direction, with the single-direction movement period as follows: 2'b00: 4 times 2'b01: 8 times 2'b10: 16 times 2'b11: 32 times
19	RO	0x0	abs_small_dz Delta Z is less than the threshold and is determined as violation, real-time update
18	RO	0x0	delta_dz_b21 Delta Z symbol bit, real-time update
17	RO	0x0	delta_dz_is_small Delta Z is less than the threshold and is determined as violation, real-time update
16:14	RO	0x0	z_rnd_add The result of rounding the cumulative value of clock phase change, real-time update
13:8	RO	0x00	dp_reg Phase drift, real-time update
7:0	RO	0x00	vber_lock Lock violation count, no real-time update

DSP_ST_TM_PARM_QUERY3

Address: Operational Base + offset (0x001A)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
21	RO	0x0	health_thresh_reached The DSP adaptive process does not have many violations when the health threshold time is reached
20:0	RO	0x000000	z_reg The result of the cumulative value of clock phase change, real-time update

DSP_ST_TM_PARM_QUERY4

Address: Operational Base + offset (0x001B)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RO	0x0	c_count_ovf Counter for modulo 256, real-time update
20:0	RO	0x000000	dz_reg_old_z The result of the last cumulative value of clock phase change, real-time update, real-time update

DSP_ST_ABS_X_ACC_INT

Address: Operational Base + offset (0x001C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:12	RO	0x0	state DSP working state 2'b00: Searching for energy 2'b01: Searching for optimal gain 2'b10: Allowing for adaptation Others: Reserved
11:0	RO	0x000	abs_x_acc_int ADC sampling absolute sum result

DSP_ST_DFE13_COEFF

Address: Operational Base + offset (0x001D)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:14	RO	0x0000	dfe13_coeff The adaptive coefficient value of the DFE13
13:0	RO	0x0000	reserved

DSP_ST_DFE14_15_COEFF

Address: Operational Base + offset (0x001E)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:12	RO	0x000	dfe15_coeff The adaptive coefficient value of the DFE15 dfe15_coeff[13:2]
11:0	RO	0x000	dfe14_coeff The adaptive coefficient value of the DFE14 dfe14_coeff[13:2]

DSP_ST_DFE16_17_COEFF

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Address: Operational Base + offset (0x001F)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:12	RO	0x000	dfe17_coeff The adaptive coefficient value of the DFE17 dfe17_coeff[13:2
11:0	RO	0x000	dfe16_coeff The adaptive coefficient value of the DFE16 dfe16_coeff[13:2]

43.4.16 Registers Summary for iGRF

Name	Offset	Size	Reset Value	Description
iGRF_FEPHY_iGRF_CON0	0x0080	HW	0x00000000	FEPHY Internal GRF Control Register 0
iGRF_FEPHY_iGRF_CON1	0x0084	HW	0x00000000	FEPHY Internal GRF Control Register 1
iGRF_FEPHY_iGRF_CON2	0x0088	HW	0x00000170	FEPHY Internal GRF Control Register 2
iGRF_FEPHY_iGRF_CON3	0x008C	HW	0x00000101	FEPHY Internal GRF Control Register 3
iGRF_FEPHY_iGRF_CON8	0x00A0	HW	0x00000072	FEPHY Internal GRF Control Register 8
iGRF_FEPHY_iGRF_CON9	0x00A4	HW	0x00000000	FEPHY Internal GRF Control Register 9
iGRF_RX_OFFSET_STATUS0	0x00C0	HW	0x00000000	RX Offset Status Register 0
iGRF_RX_OFFSET_STATUS1	0x00C4	HW	0x00000000	RX Offset Status Register 1

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

43.4.17 Detail Registers Description for iGRF

iGRF_FEPHY_iGRF_CON0

Address: Operational Base(0x21C90000) + offset (0x0080)

Bit	Attr	Reset Value	Description
15:12	RO	0x0	reserved
11	RW	0x0	dsp_rd_bank_sel Read DSP_0 register bank mode 1'b0: Different from the input field 1'b1: Same as the input field
10	RW	0x0	tx_rx_block_en Enable TX and RX isolation. 1'b0: Disable 1'b1: Enable
9	RW	0x0	force_init_state Force DSP state at IDLE state 1'b0: No force 1'b1: Force
8	RW	0x0	force_ctle Force enable CTLE, when ctle_auto_usr_en=1. 1'b0: No force 1'b1: Force
7:2	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x0	tx10_lutvec_start_frame_enhance_dis Disable frame start enhancement process in 10BT mode. 1'b0: Enable 1'b1: Disable
0	RW	0x0	autoxover_block_sq_extend_dis Extend the end of block sq while PAD used at TX function. 1'b0: Enable 1'b1: Disable

iGRF_FEPHY_iGRF_CON1

Address: Operational Base(0x21C90000) + offset (0x0084)

Bit	Attr	Reset Value	Description
15:8	RO	0x00	reserved
7:0	RW	0x00	port_dbg_ctrl_sel Testout pin new group selection (port_dbg_ctrl_sel[6:0]).Valid only when port_dbg_ctrl_sel[7]=1.

iGRF_FEPHY_iGRF_CON2

Address: Operational Base(0x21C90000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	adcbp_src Signal adcbp source 1'b0: Signal input is controlled by SMI register. 1'b1: Signal input is controlled by iGRF register.
14	RW	0x0	adcbp ADC Bypass mode (debug mode). Valid only when adcbp_src=1. Not Affected by Software Reset.
13	RW	0x0	pllbp_src Signal pllbp source 1'b0: Signal input is controlled by SMI register. 1'b1: Signal input is controlled by iGRF register.
12	RW	0x0	pllbp PLL Bypass mode. Valid only when pllbp_src=1. 1'b0: PLL normal mode 1'b1: PLL Bypass mode Not Affected by Software Reset.
11	RW	0x0	miimode_src Signal miimode source 1'b0: Signal input is controlled by SMI register. 1'b1: Signal input is controlled by iGRF register.
10	RO	0x0	reserved
9:8	RW	0x1	miimode MII Mode: set the mode of the MII. Valid only when miimode_src=1. 2'b00: MII interface. 2'b01: RMII interface 2'b10: SMII interface 2'b11: Reserved Not Affected by Software Reset.

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Bit	Attr	Reset Value	Description
7	RW	0x0	mode_src Signal mode source 1'b0: Signal input is controlled by SMI register. 1'b1: Signal input is controlled by iGRF register.
6:4	RW	0x7	mode PHY Mode of operation. Valid only when power_up_reset_src=1. 3'b000: 10BaseT, Half duplex, Auto negotiation disabled 3'b001: 10Base-T, Full duplex, Auto negotiation disabled 3'b010: 100Base-TX, Half duplex, Auto-negotiation disabled 3'b011: 100Base-TX, Full duplex, Auto-negotiation disabled 3'b100: 100Base-Tx, Half duplex, Auto-negotiation enabled 3'b101: Repeater mode, 100Base-Tx, Half duplex, Auto-negotiation enabled 3'b110: Power down mode, in this mode phy wake up in power down mode 3'b111: All capable, Full duplex, 10 & 100 BT, Auto negotiation enabled, Auto-MDIX enabled Not Affected by Software Reset.
3	RW	0x0	power_up_reset_src Signal power_up_reset source 1'b0: Signal input is controlled by SMI register. 1'b1: Signal input is controlled by iGRF register.
2	RW	0x0	power_up_reset Controls pulse generation on output pin powerup_reset. Valid only when power_up_reset_src=1. 1'b0: Power up reset disable 1'b1: Power up reset enable
1	RW	0x0	true_power_down_src Signal true_power_down source 1'b0: Signal input is controlled by SMI register. 1'b1: Signal input is controlled by iGRF register.
0	RW	0x0	true_power_down Valid only when true_power_down_src=1. 1'b0: Normal operation 1'b1: PHY is put in True power down mode

iGRF_FEPHY_iGRF_CON3

Address: Operational Base(0x21C90000) + offset (0x008C)

Bit	Attr	Reset Value	Description
15	RW	0x0	phyadd_src Signal phyadd source 1'b0: Signal input is controlled by SMI register. 1'b1: Signal input is controlled by iGRF register.
14:13	RO	0x0	reserved
12:8	RW	0x01	phyadd PHY Address. The PHY Address is used for the SMI address and for the initialization of the Cipher (Scrambler) key. Valid only when phyadd_src=1. Not Affected by Software Reset.
7:2	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x0	automdix_en_src Signal automdix_en source 1'b0: Signal input is controlled by SMI register. 1'b1: Signal input is controlled by iGRF register.
0	RW	0x1	automdix_en Auto-MDIX enable bit. Valid only when automdix_en_src=1. 1'b0: Manual set of MDI/MDIX mode according to bit MDI mode 1'b1: Auto detect MDI/MDIX mode Not Affected by Software Reset.

iGRF_FEPHY_iGRF_CON8

Address: Operational Base(0x21C90000) + offset (0x00A0)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10	RW	0x0	mlt3_zero_violation_st2_direct_to_st0_en When the decided result is 64 consecutive zeros at DSP state2 (i.e. mlt3_zero_violation=1), the DSP state machine directly jumps to state0. 1'b0: Disable 1'b1: Enable
9	RW	0x0	mlt3_zero_violation_st2_blw_re_act When the decided result is 64 consecutive zeros at DSP state2 (i.e. mlt3_zero_violation=1), BLW is turned off and can be turned on again. 1'b0: Disable 1'b1: Enable
8	RW	0x0	mlt3_zero_violation_st2_gain_re_init_en When the decided result is 64 consecutive zeros at DSP state2 (i.e. mlt3_zero_violation=1), initialize PGA gain value. 1'b0: Disable 1'b1: Enable
7	RW	0x0	mlt3_zero_violation_st2_blw_dis_en When the decided result is 64 consecutive zeros at DSP state2 (i.e. mlt3_zero_violation=1), disable baseline wander (BLW) module. 1'b0: BLW always on 1'b1: Enable above feature
6	RW	0x1	rx_ctle_offset_energy_off_st2_cmpst_en Enable energy-off compensation at DSP state2 for RX CTLE offset. 1'b0: Disable 1'b1: Enable
5	RW	0x1	rx_ctle_offset_energy_off_st1_cmpst_en Enable energy-off compensation at DSP state1 for RX CTLE offset. 1'b0: Disable 1'b1: Enable
4	RW	0x1	rx_ctle_offset_energy_off_st0_cmpst_en Enable energy-off compensation at DSP state0 for RX CTLE offset. 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
3	RW	0x0	rx_ctle_offset_xin_cmpst_en Enable Xin compensation for RX CTLE offset. 1'b0: Disable 1'b1: Enable
2	RW	0x0	rx_ctle_offset_dsp_cmpst_en Offset compensation calculation method. 1'b0: Manual calculation 1'b1: Using $signed calculation
1	RW	0x1	rx_ctle_offset_energy_on_cmpst_en Enable energy-on compensation for RX CTLE offset. 1'b0: Disable 1'b1: Enable
0	RW	0x0	rx_offset_calib_en RX offset calibration enable. 1'b0: Enable 1'b1: Disable

iGRF_FEPHY_iGRF_CON9

Address: Operational Base(0x21C90000) + offset (0x00A4)

Bit	Attr	Reset Value	Description
15	RW	0x0	sel_rx_dac_bias_level Set the DAC compensation level to rx_dac_bias_level. 1'b0: Auto DAC compensation gain 1'b1: Manual Seting
14:12	RW	0x0	rx_dac_bias_level The ADC code is expected to compensate the DAC code directly, but the values are not directly equivalent. The greater the offset captured by the ADC, the greater the compensation required, so the greater taht 3bit value, the greater the compensation provided.
11	RW	0x0	sel_dig_rx_dac_step_sel DAC amplitude and precision selection. 1'b0: Come from the software configuration. 1'b1: Depend on the offset captured by the ADC.
10	RW	0x0	sel_rx_adc_ctle_offset_latched_to_dac 1'b0: Auto DAC compensation gain 1'b1: No auto DAC compensation gain
9:8	RW	0x0	sel_dac_corr_pre_with_dc_compset_5bit_muxed Select DAC compensation source. 2'b00: BLW DAC correction code 2'b01: BLW DAC correction code - ADC offset code 2'b10: - ADC offset code 2'b11: Software configuration
7:5	RO	0x0	reserved
4:0	RW	0x00	sw_dac_corr_pre_with_dc_compset_5bit_muxed The DAC's compensation comes from the software configuration.

iGRF_RX_OFFSET_STATUS0

Address: Operational Base(0x21C90000) + offset (0x00C0)

Bit	Attr	Reset Value	Description
15:9	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
8:7	RO	0x0	rx_adc_ctle_offset_error Reflect the error of ADC and DAC code. The amplitude ranges from -1 to +1. 2'b00: abs_rx_adc_ctle_offset_latched <= 0.3125V 2'b01: abs_rx_adc_ctle_offset_latched <= 0.4375V 2'b11: abs_rx_adc_ctle_offset_latched > 0.4375V Others: Reserved
6:0	RW	0x00	rx_adc_ctle_offset_latched The offset sampled by the RX ADC, which is generated by the CTLE.

iGRF_RX_OFFSET_STATUS1

Address: Operational Base(0x21C90000) + offset (0x00C4)

Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10:8	RO	0x0	rx_dac_bias_level The ADC code is expected to compensate the DAC code directly, but the values are not directly equivalent. The greater the offset captured by the ADC, the greater the compensation required, so the greater taht 3bit value, the greater the compensation provided. This value may come from the software configuration (FEPHY_iGRF_CON9[14:12]) or from auto-adaptation, depending on FEPHY_iGRF_CON9[15].
7:0	RO	0x00	rx_adc_ctle_offset_latched_to_dac The offset value after compensating for ADC and DAC code errors.

43.5 Interface Description

Table 43-6 FEPHY Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
IOMUX0			
LED_LINK	O	GPIO3_B4	GPIO3B_IOMUX_SEL_1[3:0]=4'h6
LED_SPEED	O	GPIO3_B5	GPIO3B_IOMUX_SEL_1[7:4]=4'h6
IOMUX1			
LED_LINK	O	GPIO5_D4	GPIO5D_IOMUX_SEL_1[3:0]=4'h1
LED_SPEED	O	GPIO5_D5	GPIO5D_IOMUX_SEL_1[7:4]=4'h1
IOMUX2			
LED_LINK	O	GPIO6_C2	GPIO6C_IOMUX_SEL_0[11:8]=4'h3
LED_SPEED	O	GPIO6_C3	GPIO6C_IOMUX_SEL_0[15:12]=4'h3
TEST OUT INTERFACE			
TESTDATA0	O	GPIO6_A4	GPIO6A_IOMUX_SEL_1[3:0]=4'h8
TESTDATA1	O	GPIO6_A5	GPIO6A_IOMUX_SEL_1[7:4]=4'h8
TESTDATA2	O	GPIO6_A6	GPIO6A_IOMUX_SEL_1[11:8]=4'h8
TESTDATA3	O	GPIO6_A7	GPIO6A_IOMUX_SEL_1[15:12]=4'h8
TESTDATA4	O	GPIO6_B0	GPIO6B_IOMUX_SEL_0[3:0]=4'h8
TESTDATA5	O	GPIO6_B1	GPIO6B_IOMUX_SEL_0[7:4]=4'h8
TESTDATA6	O	GPIO6_B2	GPIO6B_IOMUX_SEL_0[11:8]=4'h8
TESTDATA7	O	GPIO6_B3	GPIO6B_IOMUX_SEL_0[15:12]=4'h8
TESTCLK	O	GPIO6_B7	GPIO6B_IOMUX_SEL_1[15:12]=4'h8
RMII_RXD0	O	GPIO6_A0	GPIO6A_IOMUX_SEL_0[3:0]=4'h8

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Module Pin	Direction	Pad Name	IOMUX Setting
RMII_RXD1	O	GPIO6_A1	GPIO6A_IOMUX_SEL_0[7:4]=4'h8
RMII_CLK	O	GPIO6_B4	GPIO6B_IOMUX_SEL_1[3:0]=4'h8
RMII_RXER	O	GPIO6_B5	GPIO6B_IOMUX_SEL_1[7:4]=4'h8
RMII_DVCRS	O	GPIO6_B6	GPIO6B_IOMUX_SEL_1[11:8]=4'h8

Notes: I=input, O=output, I/O=input/output, bidirectional

43.6 Application Notes

43.6.1 Direct Register Bank Access

Normally, the MAC access direct register bank through SMI. And the timing sequence is introduced in the Function Description part.

If the GRF (VI_GRF_RKMACPHY_CON1[22]) of APB select is configured, the system could access the direct register bank through APB interface, instead of SMI. And when APB interface is enabled, all offset values of these registers must be shifted left by two bits, to align with Word type. And the operational base address is 0x21C90000.

43.6.2 Indirect Register Bank Access

In addition to SMI direct register bank, there are six other indirect register bank, and they shall be accessed via TST_CNTL, TST_READ1, TST_READ2, TST_WRITE.

- 0x0: DSP_0 register bank. When FEPHY_iGRF_CON0[11]=1, system reads DSP_0; otherwise, it reads DSP_ST.
- 0x1: WoL register bank
- 0x2: DSP_0 register bank, only for reading. Valid when FEPHY_iGRF_CON0[11]=0.
- 0x3: BIST register bank
- 0x4: AFE register bank
- 0x5: DSP_1 register bank

43.6.2.1 WoL/BIST Register Bank Access

Procedure to write into WoL/BIST register bank.

1. Write the data to TST_WRITE register.
2. Write to the TST_CNTL with the WRITE ADDRESS set to the register address and the WRITE bit set to "1". REG_BANK_SEL should be set to WoL or BIST.

Procedure to Read into WoL/BIST register bank.

1. Write to the TST_CNTL with the READ ADDRESS set to the register address and the READ bit set to "1". REG_BANK_SEL should be set to WoL or BIST.
2. Read the data from the TST_READ1.

43.6.2.2 DSP/AFE Register Bank Access

The procedure to enable access to DSP (DSP_0 and DSP_1) and AFE register banks is that the TSTMODE bit in TST_CNTL should be toggled from 0->1->0->1.

Steps:

1. TSTCNTL = 0x0400
2. TSTCNTL = 0x0000
3. TSTCNTL = 0x0400

If system reset or soft reset is applied same steps should be followed to enable register access. At any point of time if write to TST_CNTL with TSTMODE =0, access to DSP and AFE registers are disabled.

Procedure to write into DSP and AFE register bank

1. Write the data to TST_WRITE register.
2. Write to the TST_CNTL with the WRITE ADDRESS set to the register address and the WRITE
3. bit set to "1" (and TSTMODE bit is "1"). REG_BANK_SEL should be set to DSP_0 or DSP_1 or AFE.

Procedure to Read into DSP and AFE register bank

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1. Write to the TST_CNTL with the READ ADDRESS set to the register address and the READ bit set to “1” (and TSTMODE bit is "1"). REG_BANK_SEL should be set to DSP_0 or DSP_1 or AFE.
2. Read the data from the TST_READ1 register and if needed (if the register that has been read is larger then 16 bits) read also the data from TST_READ2 register.

Note: If FEPHY_iGRF_CON0[11]=1, the DSP_0 read registers are the same as DSP_0 write registers. If FEPHY_iGRF_CON0[11]=0, the DSP_0 read registers are actually DSP_ST read registers, and the REG_BANK_SEL of real DSP_0 read registers is 0x2.

43.6.3 Programming Guide

The programming procedure needs to comply with the practical application scenario, such as configuration of clock frequency and duplex mode. A normal programming guide is listed below.

1. Configure the GRF to initialize. Clock mode register of clk_freq_sel should be set according to application. The GRF of configuration mode is important to select speed mode, duplex mode, and Auto-Negotiation mode. Configuration mode default settings are All capable, Full Duplex, 10 & 100 BT, Auto negotiation enabled, Auto-MDIX enabled. Default setting can be changed by configuring internal GRF FEPHY_iGRF_CON2[6:4], when FEPHY_iGRF_CON2[7]=1. Lastly, phy_enable is set to 1 to enable the FEPHY.
2. Wait the PLL to be locked, and wait the calibration is completed if enabled, then deassert the reset to the FEPHY.
3. Wait the FEPHY to link up and complete Auto-Negotiation if enabled, by polling the STATUS register. And if Auto-Negotiation is enable, the MAC working mode of speed and duplex should be configured according to the result of Auto-Negotiation in the speed_indication of PHY_SPECIAL_CONTROL_STATUS.
4. The packet could be transferred through the RMII. If necessary, the interrupt could be enabled to reflect the transmission progress.

43.6.4 LPI mode

Special attention should be given to the fact that the RMII protocol does not specify the LPI pattern. Therefore, the EEE feature may be not supported for some MACs with RMII interface.

However, this FEPHY support EEE to save power with simple RMII pattern. RMII TX LPI pattern is that "TX_EN" to "1'b0" and "TXD" to "2'b01". Meanwhile, RMII RX LPI pattern with "CRS_DV" to "1'b0" and "RXD" to "2'b01" is asserted when the FEPHY enters RX LPI mode. To leverage the EEE capability of this FEPHY, an appropriately RMII-LPI-pattern-supporting MAC is required.

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CHAPTER 44 IMAGE SIGNAL PROCESSING (ISP)

44.1 Introduction

44.1.1 Overview

The Image Signal Processing (ISP) is a complete video and still picture input unit which contains standard sensor picture data processing functions, such as image processing, scaling. This unit supports image sensors with integrated YCbCr processing and also simple CMOS sensors delivering RGB Bayer pattern without any integrated image processing.

Image processing contains many functions, such as HDR_MGE, HDR_DRC, BAY3DNR, DEBAYER and so on. Scaling is used for downsizing the sensor data for displaying them on the screen, and also can be used for digital zoom effects, because scaling is capable of up-scaling as well. The camera interface provides parallel data and MIPI support, so that ISP can be connected to PHY devices or IP blocks directly. All data is transmitted via the memory interface (MI) to a AXI bus system using a bus master interface. Programming is done by register read/write transactions using an AHB slave interface.

ISP supports the following features:

- VICAP input: RX raw8/raw10/raw12/raw14/raw16
- Maximum input: 3840x2160@30fps (resolution no more than 4096x3072), compatible with 7680x4320, throughput 32M@8fps
- Minimum input: 264x264
- RGBIR: Remosaic RGB-IR pattern to RGB pattern
- Auto Enhance (AE)/Histogram, Auto Focus (AF) and Auto White Balance (AWB) statistics output
- BLC: Black Level Correction
- DPCC: Static/Dynamic Defect Pixel Cluster Correction
- PDAF: Phase Detection Auto Focus
- LSC: Lens Shading Correction
- Bayer-3DNR: Temporal Bayer-raw Noise Reduction
- CAC: Chromatic Aberration Correction
- HDR-Merge: 2-Frame Merge into High-Dynamic Range
- Expander: Sensor expander
- GIC: Green Imbalance Correction
- HDR-DRC: HDR Dynamic Range Compression, tone mapping in RGB filed
- DeBayer: Advanced Adaptive Demosaic
- CCM/CSM: Color Correction Matrix, RGB2YUV
- Gamma: Gamma out correction
- Dehaze/Enhance: Automatic dehaze and effect enhancement
- LocalHist: local histogram to enhance local contrast
- HSV: Hue, Saturation, Value color palette for customer
- LDCH: Lens Distortion Correction in the Horizontal direction
- YNR: Spatial luma (Y) Noise Reduction in YUV domain
- CNR: Spatial chroma (C) Noise Reduction in YUV domain
- Sharp: Image sharpening and boundary filtering
- Gain: Image local gain
- Multi-sensor reuse ISP, 2 sensors for maximum
- Bus interface: 32bit AHB configuration, 128bit AXI R/W
- Low power, auto-gating for each block
- MI R/W burst group to improve memory utilization
- MI 2 paths output, MP stepless scaling, SP 1080p (width no more than 1920) scaling
- tile4x4 output
- Online mode: support data from VICAP and data to Encoder, data from ISP to VPSS, ISP to VPSL
- Support ISP2NPU with AI-ISP path, BAY3D output IIR data and gain data to DDR which used by NPU

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44.1.2 Using constrains

1) Sensor's hblank time is not less than 1% of each row time, or not less than 4 cycles (working clock). The vblank time does not exceed 40 rows.
2) The YNR, CNR, SHARP and ENHANCE should be on or off at the same time. YNR, SHARP and ENHANCE has its own bypass control. If you want to bypass a module, you can turn on its bypass of the module. The bypass signal of YNR includes sw_ynr_hi_pass, sw_ynr_mi_bypass and sw_ynr_lo_bypass. The bypass control of SHARP includes sw_sharp_bypass. The bypass control of ENHANCE includes sw_enh_bypass. CNR does NOT support bypass, which is the critical path in ISP.
3) The enable of gain of source module follows the enable of source module automatically, which can also bypass separately with sw_xxx_gain_bypass_en in 0x3f00, which is not recommend.
4) MI burst group supports 1~2 burst available which is more friendly to DDR.
5) For HDR on-the-fly mode, sw_ibuf_hold_watermark (address offset 0x1c0c[15:0]) is used to hold DDR read to control read rate.
6) LDCH module will adaptively consider that the table consists of an integer of 13 bits and a decimal of 3 bits when the width of table is bigger than 4080. If developers still want to use the table composed of integer of 12 bits and decimal of 4 bits, sw_ldch_force_map_en (address offset 0x3b00[6]) must be configured to 1 and sw_ldch_map13p3_en (address offset 0x3b00[7]) must be configured to 0, and ensure that the right boundary of table cannot exceed an integer of 12 bits (i.e., 4095).
7) Support the image resolution with width 4pixel alignment and height 4pixel alignment. when AIPRE function is enabled, height should be 8pixel aligned.
8) After all configurations of ISP are completed, configure MI force update, and finally start MI readback.
9) It is recommended that GAIN module is always on to improve the image effect. It is not recommended to switch GAIN dynamically, unless the ISP data stream is transmitted completely.
10) When ADRC is enabled, CAC or DEBAYER is disabled, hardware will automatically enable and bypass these two modules for data delayline requirement. This self-adaption configuration can be disabled, which is not recommend.
11) ISP MI write supports output image vertical flip. Vertical flip operation is configured to each path independently. When vertical flip is enabled, the corresponding write virtual width register and write size register should NOT be configured to 0.
12) ISP self path (SP) supports ARGB8888/RGB888/RGB565 output format. When SP vertical flip is enabled with RGB output format, the output image width must be 4pixel aligned for ARGB8888 and 8pixel aligned for RGB565.
13) Constraints on full resolution online scale-up：
    (1) Formula: Core_freq/scale_times/fps/(1+hblank)/(1+vblank)
    (2) Example: Core clk 630MHz, 4x scale-up, 30fps, h/v blank 10%
    630 / 4 / 30 / (1+0.1) / (1+0.1) = 4.34M
    (3) Summary: At Core clk 630MHz, ISP can only handle online scale-up at 4.34M@30fps, and the resolution is related to the four coefficients above.
14) pre-BLC use sw_isp_ob_offset as before, while post-BLC after BAY3D use sw_isp_ob_offset1 (address offset 0x3068[16:24]) for new.

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44.2 Block Diagram

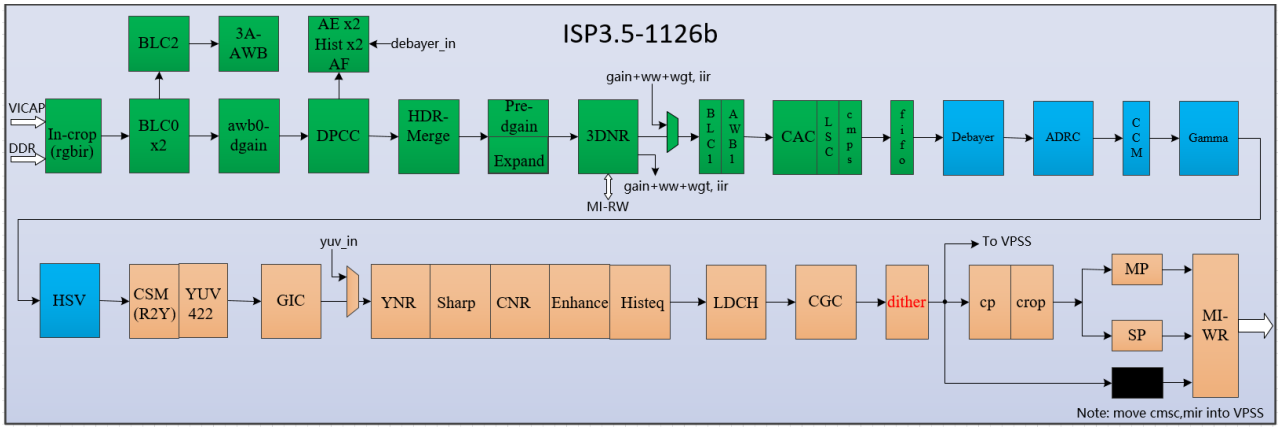

Fig. 44-1 ISP Block Diagram

The number of delay line from ISP output to input is about 30~40 lines.

ISP comprises with:

- VICAP Direct Interface
- RAW Processing
- RGB Processing
- YUV Processing
- Memory Interface (MI)

4 channels of data of RXPHY input to VICAP and one channel can directly input to ISP to make a direct connection between HDR on the fly and no-HDR. When VICAP on the fly to ISP, the vblank between frames should be at least 34 lines.

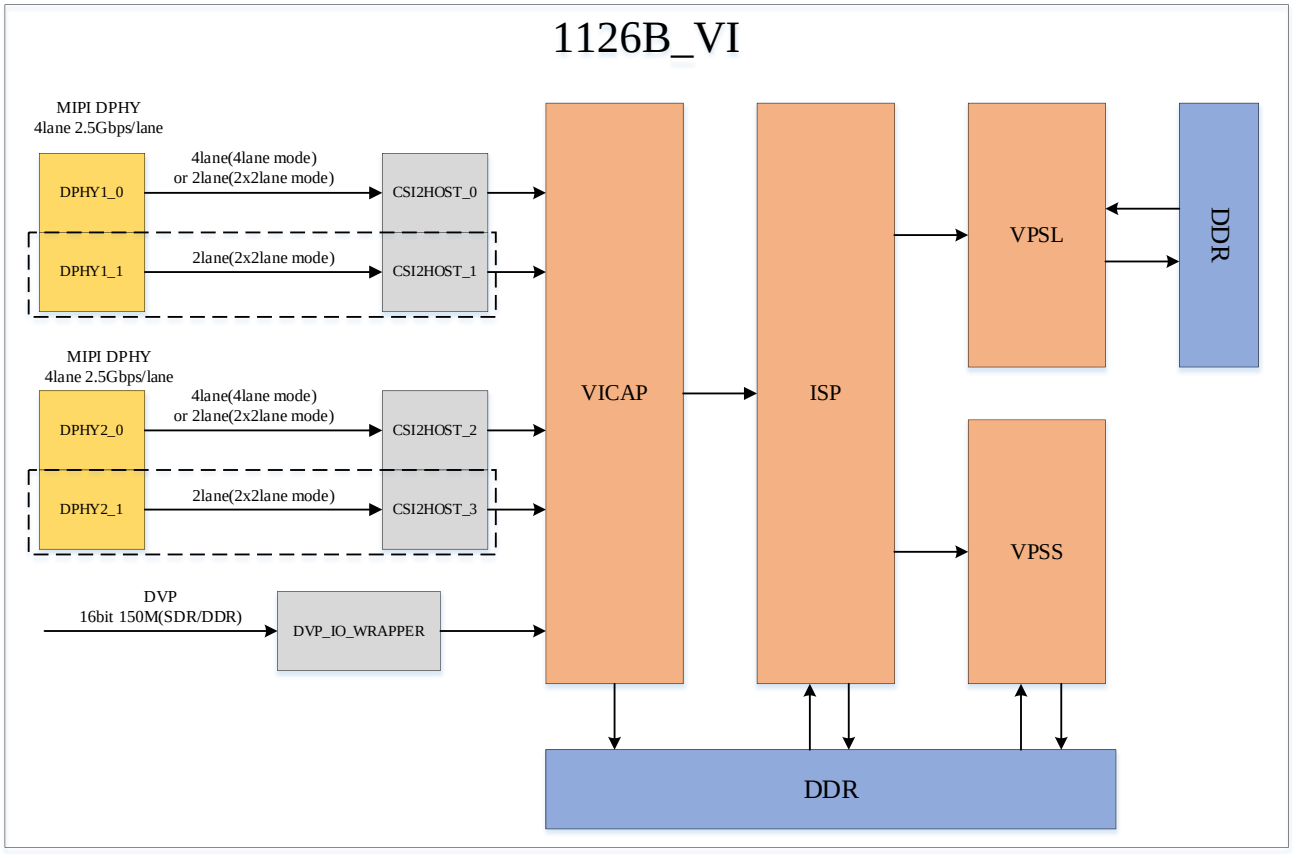

Fig. 44-2 ISP Data Flow

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44.3 Function Description

44.3.1 CSI2RX (MIPI)

1. Overview

The raw data come from VICAP or MI.

2. Features

- Support HDR stream: frame mode, line mode
- Support MIPI raw read back framex1, framex2

44.3.1.1 Block Descriptions

Raw-picture into DDR support un-compact and compact (including swap) mode:

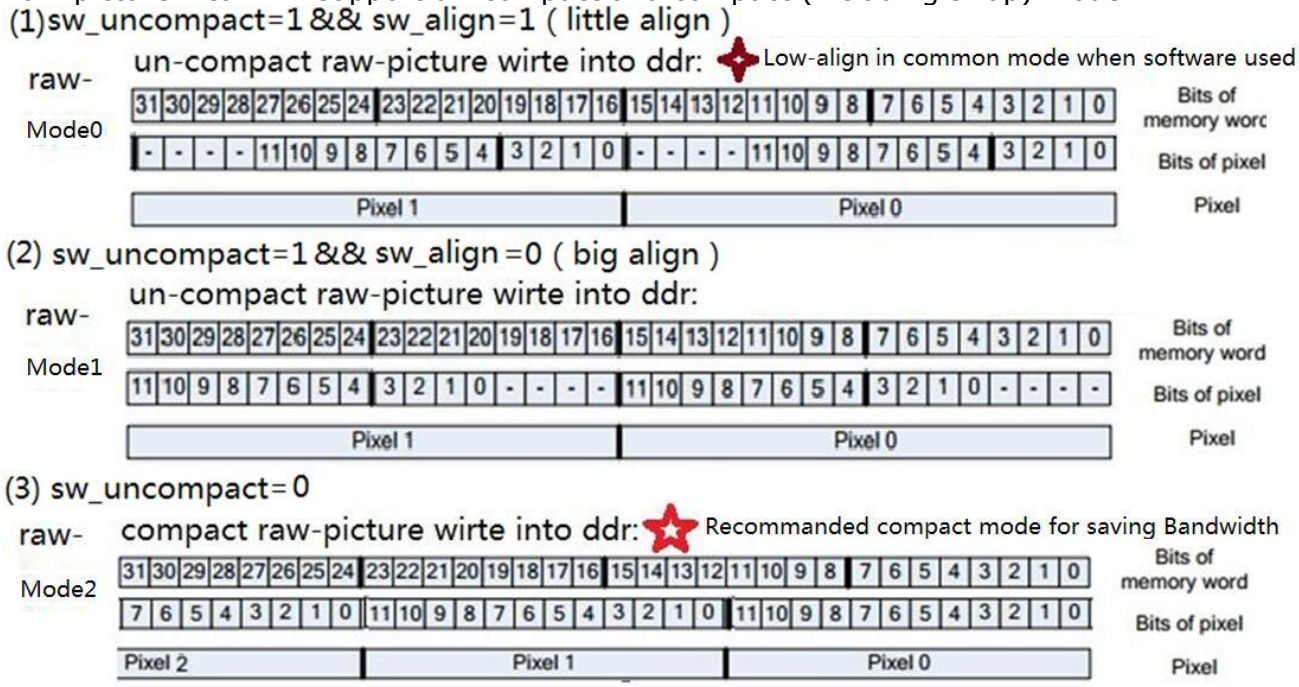

Figure 44-1 Un-compact and Compact (including swap) Mode

The function mode of CSI2RX depend on the configuration of sw_ibuf_op_mode, which are shown in the following table.

Table 44-1 CSI2RX Function Mode

Sw_ibuf_op_mode	Function	Interval mode	HDR mode	Need DDR
0	normal	NA	N	N
4	raw_rdback_framex1	NA	N	Y
5	raw_rdback_framex2	frame/line	Y	Y
8	frame_line_x2_ddr	frame/line	Y	Y

(1) frame_line_x2_ddr mode (2IDs--HDR mode)

The 2IDs inter frame mode or inter line mode has L-data and S-data. VICAP will transfer L-data to DDR and output S-data to ISP. Then ISP will read back L-data when S-data arrives ISP.

(2) raw_rdback_framex2 mode (2IDs--HDR mode)

The difference between frame_line_x2_ddr mode and raw_rdback_framex2 mode is that S-data also needs to go in and out of DDR. S-data is output from VICAP to DDR. Then S-data is read back through channel DMARX2 (DMARXS). The time to start read back is up to the user. Start once, read back one frame of L-data, M-data.

(3) raw_rdback_framex1 mode

Under raw_rdback_framex1 mode, S-data is processed by VICAP and output from VICAP to DDR. Then S-data is read back through channel DMARX2 (DMARXS). The time to start DMARXS is up to the user. Start once, read back one frame of S-data.

(4) normal mode (Single ID--linear mode)

The single ID mode is the normal sensor mode. The single ID data is input to CSI2HOST through D-PHY interface. CSI2HOST decodes the PPI stream data of D-PHY, then output to

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VICAP. VICAP parse the CSI2HOST output data to pixel and output to ISP.

44.3.2 Memory Interface (MI)

The memory interface unit (MI) is responsible for reading/writing image data from/to the system memory (DDR). The MI has six main tasks, which can operate independently:

- Take image data from the main path, either in YCbCr or RAW format, and write it into DDR.
- Take image data from BAY3D module, and take it back from the DDR to BAY3D module.
- Take image data from DBR module, and take it back from the DDR to DBR module.
- Take image data of LUT data from the DDR to HSV/LDCH/LSC module.

Memory Interface is as following:

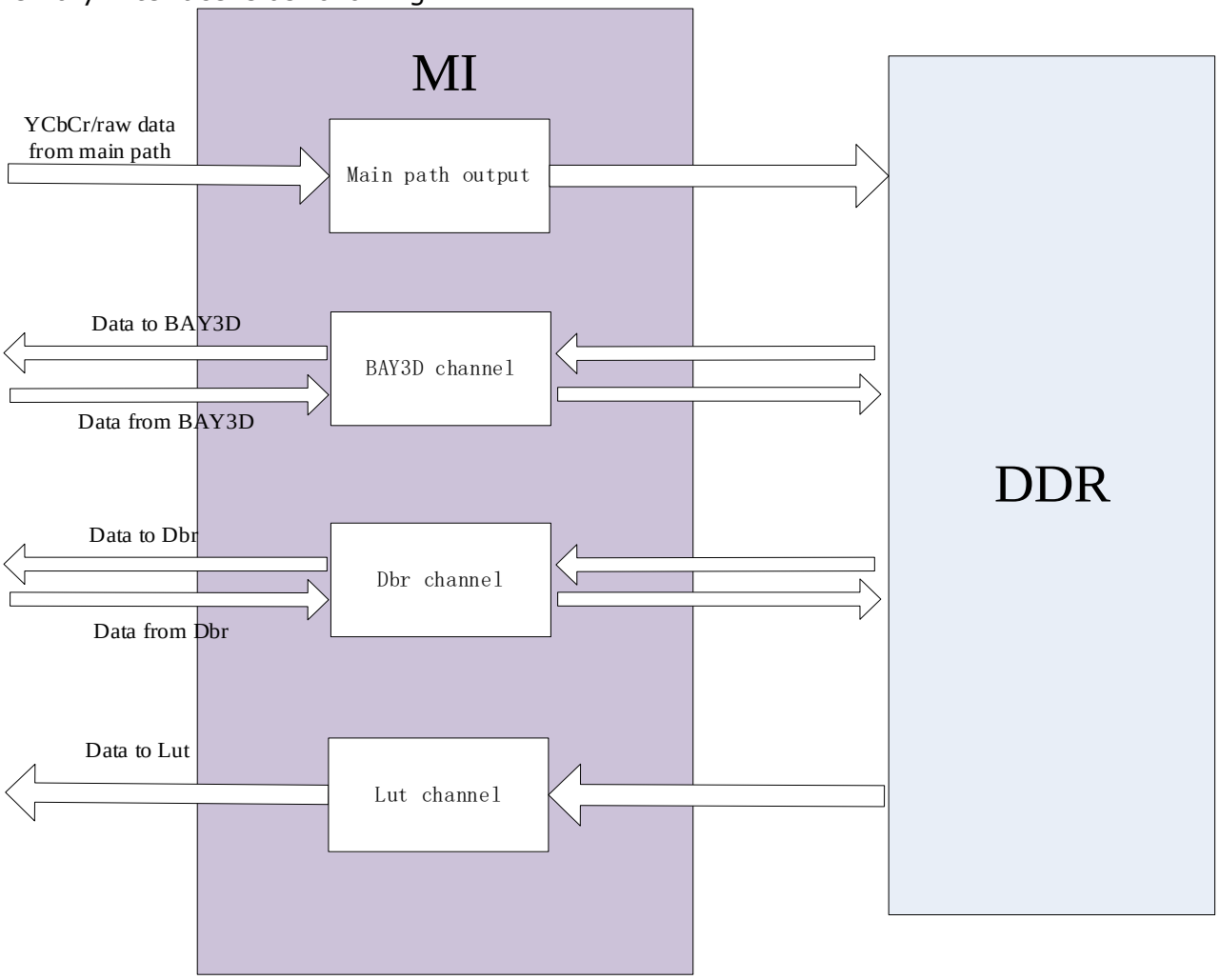

Fig. 44-3 Memory Interface

The following registers need to be configured to use different channels:

(1) Main path

The registers need to be configured are as follows (xx means Y, CB and CR):

- MI_MP_WR_xx_BASE

This is the base address of the memory area to use for that buffer.

This register protects from non-aligned access. The bits 0 to 2 are hard wired to 3'b000. As a consequence any byte address that is written to the register will automatically be re-mapped to the next lower 64bit aligned address: *write(MI_MP_WR_xx_BASE, address_value)* is equivalent to *write(MI_MP_WR_xx_BASE, address_value & 0xFFFFFFF8)*. Anyhow, in order to avoid confusion, it is not recommended to use non-aligned address values for access. It is also not recommended to actively consider the register slice for register access in order to avoid unnecessary mask and shift operations.

In addition, the programmed base address shall be burst aligned with respect to the burst length configured in MI_WR_CTRL.

Set control bit init_base_en before updating so that a forced or automatic update can take

effect.

- MI_MP_WR_xx_SIZE

Size of main picture ring buffer or raw data ring buffer.
Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configure update.
Set control bit init_base_en before updating so that a forced or automatic update can take effect.
Note: This register protects from non-aligned access.

- MI_MP_xx_OFFS_CNT_INIT

This is the initial offset (in bytes) for writing to the buffer after e.g., a soft reset. Usually, to write to the buffer from the very beginning, an offset of zero is to be programmed into this register.

- MI_MP_xx_OFFS_CNT_START

This is a read-only register, which holds the offset at which the MI had written the last processed frame. This register is updated at frame end, so at any given time, it contains always the starting offset of the last completely processed frame.

- MI_WR_CTRL

This register is a global write control register of main path, include path_enable, wr_format and so on. Refer to MI_WR_CTRL register description for details.

(2) BAY3D/DBR/LUT channel

The registers need to be configured are as follows (xx include RAW0~RAW1, LUT and DBR):

- xx_WR_BASE

DDR write base address, similar to MI_SP_WR_xx_BASE. Refer to register description for details.

- xx_WR_SIZE

DDR write size, similar to MI_SP_WR_xx_SIZE. Refer to register description for details.

- xx_WR_LENGHT

Line length of DDR write in pixel, also known as line stride. If no line stride is used, line length must match image width. For example, raw8 mode must be a multiple of 8.

- xx_RD_BASE

Image read start address.

- xx_RD_LENGTH

Line length of DDR read in pixel, also known as line stride.

- MI_WR_CTRL2

This register is a global write control register of BAY3D/DBR/LUT channel. Refer to register description for details.

- MI_RD_CTRL2

This register is a control register of BAY3D/DBR/LUT channel, refer to MI_WR_CTRL register description for details.

44.3.3 ISP_CORE

44.3.3.1 INFORM

The input formatter module is responsible for sampling data from the sensor device and providing it to the other blocks in the processing pipelines.

44.3.3.2 OUTFORM

At the output of the ISP sub-module the image data may be cropped a third time.

The following figure illustrates the different possible regions which can be defined by register settings. Some of these regions may have the same size and offset (settings), if a differentiation is not needed.

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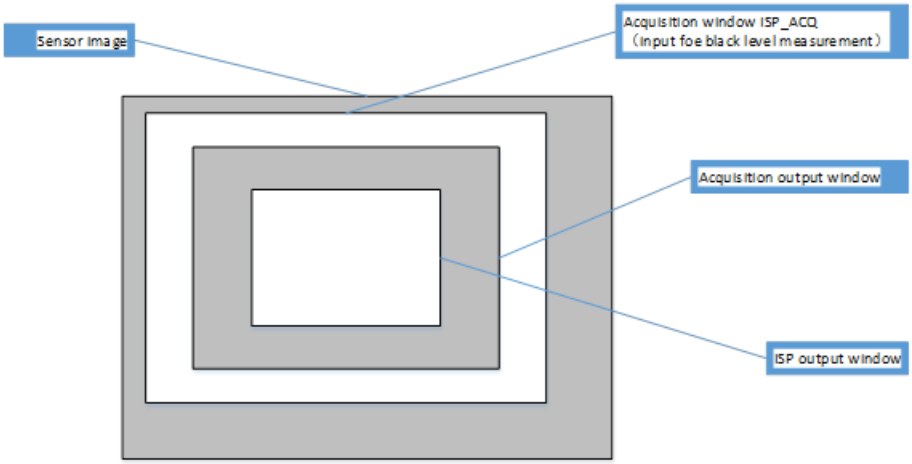

Fig. 44-4 Possible Cropping Regions of ISP

44.3.3.3 BLC

Black Level Correction (BLC) module is a function to subtract a DC offset from picture data.

A CMOS sensor always has a so-called black level shift. So that pixels with no light on them will not read out the value zero. This value varies with different setting for the exposure. This black level can easily be detected by special pixels on the sensor that are permanently covered, i.e., they are always black.

BLC module reads out the values of these pixels, calculates their mean value and then subtracts these values from all pixels that represent the picture frame (in automatic mode).

44.3.3.4 DPCC

Dynamic Defect Pixel Cluster Correction (DPCC) module is used to correct the defect pixels of the sensor in the beginning of the ISP pipeline. DPCC module supports detection and cor rection of single pixels and small cluster defects. It detects and corrects defects pixels on ra w Bayer image data at each RAW frame.

44.3.3.5 HDR

High Dynamic Range (HDR) refers to the high ratio of brightest value and darkest value contained in an image, that is, the number of levels of gray scale division between brightest and darkest is big. The larger the dynamic range, the richer the level of representation and the wider the color space.

Dynamic range calculation formula: dynamic_range = 20log(MaxIntensity / MinIntensity), where MaxIntensity means maximum brightness value, MinIntensity means minimum brightness value.

HDR unit is composed of both HDR-MGE module and HDR-DRC. HDR-MGE realizes the function of two frames synthesizing one frame. HDR-DRC realizes wide dynamic compression in RGB filed

44.3.3.6 BAY3D

Bayer-3DNR (BAY3D for short) module mainly realizes advanced temporal noise reduction of image in raw format. Motion detection in high and low frequency domain, Kalman filter is applied to reduce high frequency and low frequency noise, image edges and details are preserved at the same time.

44.3.3.7 LSC

Lens Shade Correction (LSC) is designed to deal the problems of lens shading and vignette. It is done during input data processing: If the lens shading correction is enabled, each pixel is processed and corrected according to the stored settings. LSC is done by multiplying

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each input pixel with its respective correction value. Only the correction factors at predefined sector corners as well as the sector positions are stored. The captured frames are evaluated by software and the calculated parameters for LSC are stored in multiple illumination specific tables e.g., in external memory or on a flash device. The software controls LSC process by loading or updating the correct tables into the hardware module.

It is also possible to use different LSC parameters for different environment conditions, e.g., lightness, light direction or sensor position.

44.3.3.8 DEBAYER

The DEBAYER module outputs RGB data after interpolation and filtering operation of the input Bayer data. The filtering operation can be bypassed by software configuration, and DEBAYER module can also output three RGB components of the same value in black-and-white mode.

44.3.3.9 CCM

Color Correct Matrix (CCM) is used to correct the color crosstalk because of three channels response of sensor when only one channel color input. For example, when the sensor input is red, the other two channels GB not only R is also response too. CCM is working to reduce this crosstalk to make color brighter in color. The adjustment factor is added to adjust CCM working strength. The factor is works at dark range and bright range, which are symmetry.

44.3.3.10 GAMMA_OUT

Because the human eye's perception of natural brightness is non-linear, the dynamic range and gray-scale budget of the medium we use to record and display the picture are limited. In this premise, gamma is produced which is the mapping relationship between the natural brightness and the subjective gray-scale experience.

44.3.3.11 ENHANCE

ENHANCE extracts the middle and high frequency information of the image through spatial filtering, and adaptively scales them to enhance the contrast and details of the output image.

44.3.3.12 YUV-HIST

HIST in YUV domain adjusts the contrast of the input image through histogram equalization, enhancing local contrast without affecting the overall contrast.

44.3.3.13 HSV

HSV color domain shows the hue (H), saturation (S), value (V) of colors intuitively, which provides more precise color perception than RGB color domain does.

44.3.3.14 LDCH

LDCH module achieves distortion correction in horizontal direction under fisheye lens.

LDCH module needs to take table from DDR through MI unit. When the resolution is small, it is recommended that the MI burst length configuration of images should be greater than the width of table, otherwise, the fetching will hang.

44.3.3.15 YUV-2DNR

YUV-2DNR consists of two modules, YNR and CNR. YNR is used to reduce the noise of Y component, and CNR is used to reduce the color noise.

YUV-2DNR supports the following features:
Support the independent configuration of Y component and UV component denoising intensity.
Support the independent configuration of high-frequency and low-frequency noise

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suppression.

44.3.3.16 SHARP

SHARP includes two functions: image sharpening and boundary filtering. sharpening can sharpen the intermediate frequency and high frequency respectively. Boundary filtering is to do another level of filtering on the sharpening results, remove the boundary burrs, and finally add a level of general sharpening to supplement the image details.

SHARP supports the following features:
Support image sharpening and boundary filtering
Support sharpening of medium-low frequency and high frequency respectively
Support adaptive filtering and specified coefficient filtering
Support detail enhancement

44.3.3.17 GAIN

GAIN is used to adjust the local gain of image, and guide the noise reduction of GIC, YNR, CNR, and SHARP.

44.3.3.18 CSM

CSM module realizes data conversion from RGB to YUV format.

44.3.3.19 CONV422

CONV422 module change YUV444 format data to YUV422 format.

44.3.3.20 SCL-RESIZE

The resize modules get pictures in YCbCr 4:2:2 format, and scale them by an arbitrary factor up or down to a new format. See following figure for a module overview:

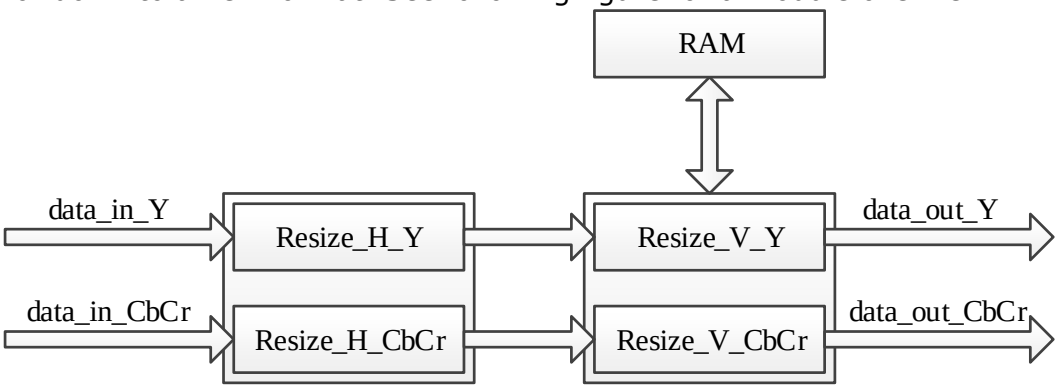

Fig. 44-5 Block Diagram of the Resize Module

The resize module is configurable for horizontal and vertical up- or down-scaling. Discrete values for the scaling factors of the luminance and the two chrominance components allow conversion between YUV4:2:2 and YUV4:2:0 color format and support of uneven line width.

Phase shift registers are provided to shift the output pixel positions with respect to the input pixel positions. For example, this allows format conversion between cosited and non-cosited color schemes.

In sensor mode this module supports only down-scaling because of the sensor cannot be stopped from delivering data during one frame.

The resize module is able to process luminance and chrominance data independently, i.e., there are separate pipelines for luminance and chrominance processing using dedicated scale factors and phase offsets. This allows format conversion to be done (YCbCr 4:2:2 to 4:2:0).

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44.3.3.21 FLASH_LIGHT

The sensor interface supports triggering of a LED or tube flash light. To control a flash light device, the flash light output and the prelight output can be used. A trigger event could active both the flash light and the prelight. This event may either be a positive or negative edge from the camera or a positive edge from any other trigger source at the input port 'vds_vsync'.

Programming respective configuration register can determine the signal polarity, flash delay time and flash light time.

44.3.3.22 EXPANDER

ISP expander decompresses the compressed data from HDR sensor to get the uncompressed data for subsequent processing, max 20bit.

44.3.3.23 RGBIR

RGB-IR camera has no IR filter when acquire image, ISP support RGB-IR camera by using RGBIR module to remove the IR pattern to get the bayer pattern.

44.3.3.24 GIC

Green Imbalance Correction (GIC) is a method to correct the color imbalance in captured images. The principle is that each pixel in the captured image is used to represent a set of colors, and there is a selected specific color pixel in the set of colors. The horizontal and vertical gradient data are derived from a set of pixel blocks surrounding the single pixel, and the pixel blocks are classified according to the visual characteristics of the part of the image. A compensation value based on gradient data and visual characteristics is determined, and the compensation value is applied to the pixel block.

44.3.3.25 CAC

Due to the difference wavelengths of light, the index of refraction is various. As a result, a purple band appears along the boundary between the light and dark parts of the object when the photograph is taken. Chromatic Aberration Correction (CAC) is used to correct the problem.

44.3.4 3A

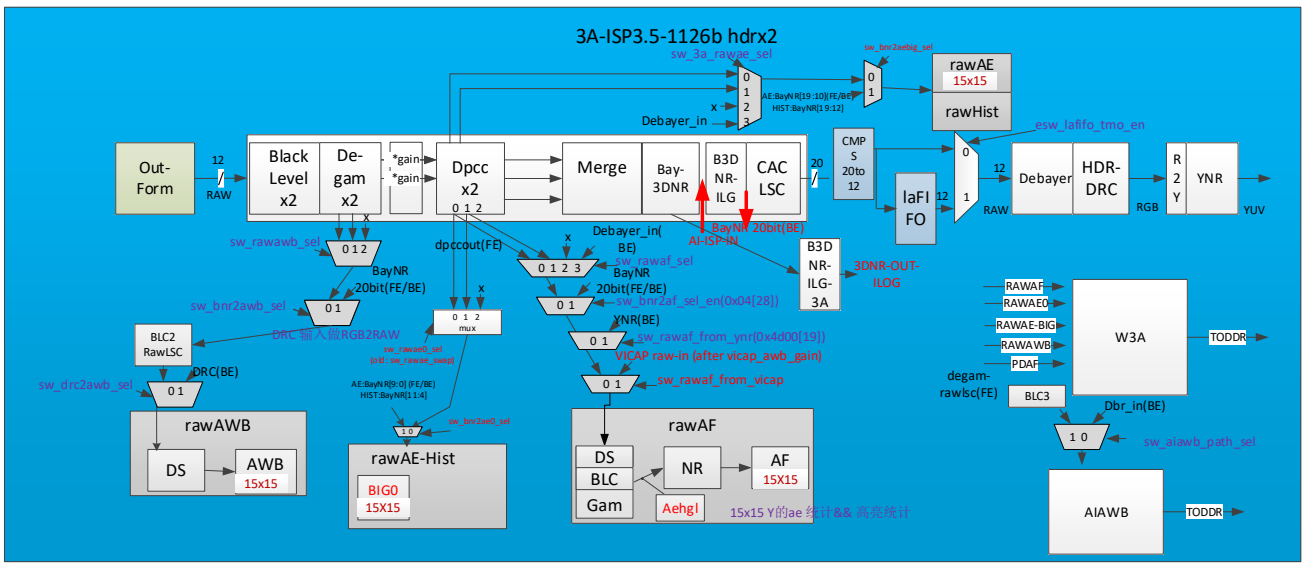

Fig. 44-6 3A-ISP3.3

44.3.4.1 AF

AF realizes the function of Auto Focus. The main part of AF control will be completed in the software: the search algorithm for the maximum definition in the image will be realized in the software, and the motion of the lens will be controlled by the software. The hardware AF module mainly realizes the measurement of image definition by configuring the configuration register. Filtering and gamma are added to facilitate the dark field processing.

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It supports a 5x5 size window and a separate window. Because its input data format is raw, AF here is named RAWAF.

44.3.4.2 AE

AE realizes the function of Auto Exposure. The input source is raw format. There are two AE modules here, both are RAWAE_BIG. RAWAE_BIG supports 15x15 statistics window.

44.3.4.3 AWB

AWB module provides Auto White Balance function, and configures the gains of the R, Gr, Gb and B components. Because its input data format is raw, AWB here is named RAWAWB. RAWAWB has 3 engines for finding valid white points (XY UV and 3DYUV domain).

It supports a 5x5 size window for white points or all points. It accumulates R, G, B channel data of all white points in XY domain for small normal and big window and for 7 source lights.

44.3.4.4 HIST

Histogram (HIST) counts the number of pixels with the same or similar values. In general, a histogram is a graphical representation of the pattern of change that exists in the intensity value of a color or luminance plane. It is often shown as a vertical bar chart to indicate the frequency level of data collected over a specific range. The measurement can be used in different applications. The common application is to display the information of the end user, or to improve the exposure control and so on.

There are two HIST modules here, both are RAW HIST_BIG. RAW HIST_BIG supports 15x15 statistics window.

44.3.4.5 PDAF

Phase Detection Auto Focus (PDAF) module here replaces the PDAF points inside the raw input data with corresponding 3x3 median data.

44.4 Register Description

The ISP uses a distributed configuration register scheme, so there is no central unit containing all programming registers, but all sub-modules contain their own programming registers. An address space is reserved for each sub-module inside the total ISP controller.

Table 44-2 ISP module base address

Module	Description	Offset Address
RGBIR	Remosaic RGB-IR pattern to RGB pattern	0X2E00
BLS	Black level subtraction	0X3000
EXPAND	sensor expander	0x3200
DPCC	Defect pixel cluster correction	0X3400
HDRMGE	High dynamic range merge	0X3800
BAY3D	Temporal noise reduction in raw space	0X2B00
CAC	Chromatic Aberration Correction	0X2600
LSC	Lens shade correction	0X2200
HDRTMO	High dynamic range tone mapping	0X3900
GIC	Green Imbalance Correction	0X2F00
DEBAYER	DeBayer	0X2500
CCM	Color correct matrix	0X0700
GAMMA_OUT	Gamma out	0X0900
2DNR-YNR	Filter the noise of Y component	0X2700

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Module	Description	Offset Address
2DNR-CNR	Filter the noise of C component	0X2800
SHARP	Image sharpening and boundary filtering	0X2900
LDCH	Lens distortion correction in horizontal	0X3B00
ENHANCE	Effect enhancement	0X3A00
HIST	local histogram to enhance local contrast	0X3C00
HSV	Hue, Saturation, Value color palette for customer	0X3E00
GAIN	Image local gain	0X3F00
BILINEAR_SCALE	MP/SP/BP bilinear scale	0X0C00,0X1000
ISP_CORE	ISP top module	0X0400
FLASH	ISP flash light	0X0660
CTRL	Marvin top control	0X0000
RAWAE_BIG	Auto exposure big version	0X4400,0X4500
RAWAF	Auto focus	0x4D00
RAWAWB	Auto white balancing	0X5000
RAWHIST_BIG	Histogram calculation big	0X4800,0X4900
IE_CMSK	Image Effect and privacy cover/mosaic	0x0200
CPROC	Color Processing	0x0800
DUAL_CROP	Dual Crop	0x0880
W3A	3A data to DDR	0x4000
AI	AI-ISP to NPU	0x1200

44.4.1 Registers Summary

44.4.1.1 MIPI

Name	Offset	Size	Reset Value	Description
CSI2RX_1C00_CTRL0	0x0000	W	0x20820000	Version of the CSI-2 host controller 0
CSI2RX_1C00_CTRL1	0x0004	W	0x00032103	Version of the CSI-2 host controller 1
CSI2RX_1C00_CTRL2	0x0008	W	0x00000000	Version of the CSI-2 host controller 2
CSI2RX_1C00_CTRL3	0x000C	W	0x00000000	Version of the CSI-2 host controller 3
CSI2RX_1C00_CSI2_RESETN	0x0010	W	0x00000003	CSI-2 controller reset
CSI2RX_1C00_DATA_IDS_1	0x0018	W	0x0000002B	List of Data Ids for which IDI reports line boundary matching errors (CSI2_HOST_N_DATA_IDS > 0). Data IDs for which IDI reports line boundary matching errors
CSI2RX_1C00_ERR_OVERFLOW	0x0028	W	0x00000000	Error state overflow register
CSI2RX_1C00_ERR_STAT	0x002C	W	0x00000000	Error state
CSI2RX_1C00_MASK_OVERFLOW	0x0038	W	0x00000000	Error state overflow register

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Name	Offset	Size	Reset Value	Description
CSI2RX_1C00_MASK_STAT	0x003C	W	0x00000000	Error state register 3
CSI2RX_1C00_RAW_RD_CTRL	0x0080	W	0x00000000	RAW_RD control register, the channel that read picture data from DDR
CSI2RX_1C00_RAW_RD_LINECNT_RO	0x0084	W	0x00000000	RAW_RD line counter
CSI2RX_1C00_RAW_RD_PIC_SIZE	0x0088	W	0x00000000	RAW_RD picture size
CSI2RX_1C00_RAW2_RD_LINECNT_RO	0x008C	W	0x00000000	RAW2_RD line counter
CSI2RX_1C00_ISP_LINECNT_RO	0x00B4	W	0x00000000	Current line counter
CSI2RX_1C00_RAW_WR_IBUF_STATUS_RO	0x00B8	W	0x00000000	HDR ibuf status
CSI2RX_1C00_FPN_CTRL	0x00D0	W	0x00000000	FPN control register
CSI2RX_1C00_FPN_TABLE_CTRL	0x00D4	W	0x00000001	FPN data write control register. The memory write address clear when finish
CSI2RX_1C00_FPN_TABLE_DATA0	0x00D8	W	0x00000000	FPN data register to memory. FPN data to memory, the memory write address add 1 after write
CSI2RX_1C00_FPN_TABLE_DATA1	0x00DC	W	0x00000000	FPN data register to memory. FPN data to memory, the memory write address add 1 after write
CSI2RX_1C00_VERSION	0x00FC	W	0x02013323	Version of the CSI-2 host controller

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

44.4.1.2 MMU

Name	Offset	Size	Reset Value	Description
MMU_DTE_ADDR	0x0000	W	0x00000000	MMU current page Table address
MMU_STATUS	0x0004	W	0x00000000	MMU status register
MMU_COMMAND	0x0008	W	0x00000000	MMU command register
MMU_PAGE_FAULT_ADDR	0x000C	W	0x00000000	MMU logical address of last page fault
MMU_ZAP_ONE_LINE	0x0010	W	0x00000000	MMU Zap cache line register
MMU_INT_RAWSTAT	0x0014	W	0x00000000	MMU raw interrupt status register
MMU_INT_CLEAR	0x0018	W	0x00000000	MMU raw interrupt status register
MMU_INT_MASK	0x001C	W	0x00000000	MMU raw interrupt status register
MMU_INT_STATUS	0x0020	W	0x00000000	MMU raw interrupt status register
MMU_AUTO_GATING	0x0024	W	0x80000000	MMU auto gating

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

44.4.1.3 MI

Name	Offset	Size	Reset Value	Description
MI_1400_MI_WR_CTRL	0x0000	W	0x200A0000	Global write control register
MI_1400_MI_WR_INIT	0x0004	W	0x00000020	Control register for address initialization and skip function

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Name	Offset	Size	Reset Value	Description
MI_1400_MI_MP_WR_Y_BASE	0x0008	W	0x00000000	Base address for main picture Y component, JPEG or raw data
MI_1400_MI_MP_WR_Y_SIZE	0x000C	W	0x00000000	Size of main picture Y component, JPEG or raw data
MI_1400_MI_MP_WR_Y_OFFS_CNT	0x0010	W	0x00000000	Offset counter initial value for main picture Y, JPEG or raw data
MI_1400_MI_MP_WR_Y_OFFS_CNT_START	0x0014	W	0x00000000	Offset counter start value for main picture Y, JPEG or raw data
MI_1400_MI_MP_WR_Y_IRQ_OFFS	0x0018	W	0x00000000	Fill level interrupt offset value for main picture Y, JPEG or raw data
MI_1400_MI_MP_WR_CB_BASE	0x001C	W	0x00000000	Base address for main picture Cb component ring buffer
MI_1400_MI_MP_WR_CB_SIZE	0x0020	W	0x00000000	Size of main picture Cb component ring buffer
MI_1400_MI_MP_WR_CB_OFFS_CNT	0x0024	W	0x00000000	Offset counter initial value for main picture Cb component ring buffer
MI_1400_MI_MP_WR_CB_OFFS_CNT_START	0x0028	W	0x00000000	Offset counter start value for main picture Cb component ring buffer
MI_1400_MI_MP_WR_CR_BASE	0x002C	W	0x00000000	Base address for main picture Cr component ring buffer
MI_1400_MI_MP_WR_CR_SIZE	0x0030	W	0x00000000	Size of main picture Cr component ring buffer
MI_1400_MI_MP_WR_CR_OFFS_CNT	0x0034	W	0x00000000	Offset counter initial value for main picture Cr component ring buffer
MI_1400_MI_MP_WR_CR_OFFS_CNT_START	0x0038	W	0x00000000	Offset counter start value for main picture Cr component ring buffer
MI_1400_MI_SP_WR_Y_BASE	0x003C	W	0x00000000	Base address for self picture Y component ring buffer
MI_1400_MI_SP_WR_Y_SIZE	0x0040	W	0x00000000	Size of self picture Y component ring buffer
MI_1400_MI_SP_WR_Y_OFFS_CNT	0x0044	W	0x00000000	Offset counter initial value for self picture Y component ring buffer
MI_1400_MI_SP_WR_Y_OFFS_CNT_START	0x0048	W	0x00000000	Offset counter start value for self picture Y component ring buffer
MI_1400_MI_SP_WR_Y_LLENGTH	0x004C	W	0x00000000	Line length of self picture Y component
MI_1400_MI_SP_WR_CB_BASE	0x0050	W	0x00000000	Base address for self picture Cb component ring buffer
MI_1400_MI_SP_WR_CB_SIZE	0x0054	W	0x00000000	Size of self picture Cb component ring buffer
MI_1400_MI_SP_WR_CB_OFFS_CNT	0x0058	W	0x00000000	Offset counter initial value for self picture Cb component ring buffer
MI_1400_MI_SP_WR_CB_OFFS_CNT_START	0x005C	W	0x00000000	Offset counter start value for self picture Cb component ring buffer
MI_1400_MI_SP_WR_CR_BASE	0x0060	W	0x00000000	Base address for self picture Cr component ring buffer
MI_1400_MI_SP_WR_CR_SIZE	0x0064	W	0x00000000	Size of self picture Cr component ring buffer
MI_1400_MI_SP_WR_CR_OFFS_CNT	0x0068	W	0x00000000	Offset counter initial value for self picture Cr component ring buffer

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Name	Offset	Size	Reset Value	Description
MI_1400_MI_SP_WR_CR_OFFS_CNT_START	0x006C	W	0x00000000	Offset counter start value for self picture Cr component ring buffer
MI_1400_MI_WR_BYTE_CNT	0x0070	W	0x00000000	Counter value of JPEG or RAW data bytes
MI_1400_MI_WR_CTRL_SHD	0x0074	W	0x00000000	Global control internal shadow register
MI_1400_MI_MP_WR_Y_BASE_SHD	0x0078	W	0x00000000	Base address shadow register for main picture Y component, JPEG or raw data ring buffer
MI_1400_MI_MP_WR_Y_SIZE_SHD	0x007C	W	0x00000000	Size shadow register of main picture Y component, JPEG or raw data
MI_1400_MI_MP_WR_Y_OFFS_CNT_SHD	0x0080	W	0x00000000	Current offset counter of main picture Y component, JPEG or raw data ring buffer
MI_1400_MI_MP_WR_Y_IRQ_OFFS_SHD	0x0084	W	0x00000000	Shadow register of fill level interrupt offset value for main picture Y component, JPEG or raw data
MI_1400_MI_MP_WR_CB_BASE_SHD	0x0088	W	0x00000000	Base address shadow register for main picture Cb component ring buffer
MI_1400_MI_MP_WR_CB_SIZE_SHD	0x008C	W	0x00000000	Size shadow register of main picture Cb component ring buffer
MI_1400_MI_MP_WR_CB_OFFS_CNT_SHD	0x0090	W	0x00000000	Current offset counter of main picture Cb component ring buffer
MI_1400_MI_MP_WR_CR_BASE_SHD	0x0094	W	0x00000000	Base address shadow register for main picture Cr component ring buffer
MI_1400_MI_MP_WR_CR_SIZE_SHD	0x0098	W	0x00000000	Size shadow register of main picture Cr component ring buffer
MI_1400_MI_MP_WR_CR_OFFS_CNT_SHD	0x009C	W	0x00000000	Current offset counter of main picture Cr component ring buffer
MI_1400_MI_SP_WR_Y_BASE_SHD	0x00A0	W	0x00000000	Base address shadow register for self picture Y component ring buffer
MI_1400_MI_SP_WR_Y_SIZE_SHD	0x00A4	W	0x00000000	Size shadow register of self picture Y component ring buffer
MI_1400_MI_SP_WR_Y_OFFS_CNT_SHD	0x00A8	W	0x00000000	Current offset counter of self picture Y component ring buffer
MI_1400_MI_SP_WR_CB_BASE_AD_SHD	0x00B0	W	0x00000000	Base address shadow register for self picture Cb component ring buffer
MI_1400_MI_SP_WR_CB_SIZE_SHD	0x00B4	W	0x00000000	Size shadow register of self picture Cb component ring buffer
MI_1400_MI_SP_WR_CB_OFFS_CNT_SHD	0x00B8	W	0x00000000	Current offset counter of self picture Cb component ring buffer
MI_1400_MI_SP_WR_CR_BASE_AD_SHD	0x00BC	W	0x00000000	Base address shadow register for self picture Cr component ring buffer
MI_1400_MI_SP_WR_CR_SIZE_SHD	0x00C0	W	0x00000000	Size shadow register of self picture Cr component ring buffer
MI_1400_MI_SP_WR_CR_OFFS_CNT_SHD	0x00C4	W	0x00000000	Current offset counter of self picture Cr component ring buffer

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Name	Offset	Size	Reset Value	Description
MI_1400_MI_RD_Y_PIC_START_AD	0x00C8	W	0x00000000	Y component image start address
MI_1400_MI_RD_Y_PIC_WIDTH	0x00CC	W	0x00000000	Y component image width
MI_1400_MI_RD_Y_LLENGTH	0x00D0	W	0x00000000	Y component original line length
MI_1400_MI_RD_Y_PIC_SIZE	0x00D4	W	0x00000000	Y component image size
MI_1400_MI_RD_CB_PIC_START_AD	0x00D8	W	0x00000000	Cb component image start address
MI_1400_MI_RD_CR_PIC_START_AD	0x00E8	W	0x00000000	Cr component image start address
MI_1400_MI_IMSC	0x00F8	W	0x00000000	Interrupt Mask1'b1: Interrupt active1'b0: Interrupt masked
MI_1400_MI_RIS	0x00FC	W	0x00000000	Raw Interrupt Status
MI_1400_MI_MIS	0x0100	W	0x00000000	Masked Interrupt Status
MI_1400_MI_ICR	0x0104	W	0x00000000	Interrupt Clear Register
MI_1400_MI_ISR	0x0108	W	0x00000000	Interrupt Set Register
MI_1400_MI_STATUS	0x010C	W	0x00000000	MI Status Register
MI_1400_MI_STATUS_CLR	0x0110	W	0x00000000	MI Status Clear Register
MI_1400_MI_SP_WR_Y_PIC_WIDTH	0x0114	W	0x00000000	Y component image width for self picture
MI_1400_MI_SP_WR_Y_PIC_HEIGHT	0x0118	W	0x00000000	Y component image height for self picture
MI_1400_MI_SP_WR_Y_PIC_SIZE	0x011C	W	0x00000000	Y component image size for self picture
MI_1400_MI_RD_CTRL	0x0120	W	0x00000000	DMA read control register
MI_1400_MI_RD_START	0x0124	W	0x00000000	DMA start register
MI_1400_MI_RD_STATUS	0x0128	W	0x00000000	DMA status register
MI_1400_MI_WR_PIXEL_CNT	0x012C	W	0x00000000	Counter value for defect pixel list
MI_1400_MI_MP_WR_Y_BASE2	0x0130	W	0x00000000	Base address 2 (ping pong) for main picture Y component
MI_1400_MI_MP_WR_CB_BASE2	0x0134	W	0x00000000	Base address 2 (ping pong) for main picture CB component
MI_1400_MI_MP_WR_CR_BASE2	0x0138	W	0x00000000	Base address 2 (ping pong) for main picture CR component
MI_1400_MI_SP_WR_Y_BASE2	0x013C	W	0x00000000	Base address 2 (ping pong) for self picture Y component
MI_1400_MI_SP_WR_CB_BASE2	0x0140	W	0x00000000	Base address 2 (ping pong) for self picture CB component
MI_1400_MI_SP_WR_CR_BASE2	0x0144	W	0x00000000	Base address 2 (ping pong) for self picture CR component
MI_1400_MI_WR_XTD_FORMAT_CTRL	0x0148	W	0x00000000	Extended Storage Format Control for main, self and dma read path
MI_1400_MI_WR_ID	0x0154	W	0x65432100	AXI write id group1
MI_1400_MI_MP_WR_Y_IRQ_OFFS2	0x01E0	W	0x00000000	Fill level interrupt2 offset value for main picture Y, JPEG or raw data
MI_1400_MI_MP_WR_Y_IRQ_OFFS2_SHD	0x01E4	W	0x00000000	Shadow register of fill level interrupt2 offset value for main picture Y component, JPEG or raw data

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Name	Offset	Size	Reset Value	Description
MI_1400_MI_MP_WR_Y_LLENGTH	0x01E8	W	0x00000000	Line length of main picture Y component
MI_1400_MI_MP_WR_Y_PIC_WIDTH	0x01EC	W	0x00000000	Y component image width for main picture
MI_1400_MI_MP_WR_Y_PIC_HEIGHT	0x01F0	W	0x00000000	Y component image height for main picture
MI_1400_MI_MP_WR_Y_PIC_SIZE	0x01F4	W	0x00000000	Y component image size
MI_1400_MI_MP_WR_CTRL	0x01F8	W	0x00000200	Main path write control register
MI_1400_MI_BP_WR_CTRL	0x0200	W	0x00000200	Bypass path write control register
MI_1400_MI_BP_WR_Y_BASE	0x0204	W	0x00000000	Base address for bypass picture Y component ring buffer
MI_1400_MI_BP_WR_Y_SIZE	0x0208	W	0x00000000	Size of bypass picture Y component ring buffer
MI_1400_MI_BP_WR_Y_OFFS_CNT	0x020C	W	0x00000000	Offset counter initial value for bypass picture Y component ring buffer
MI_1400_MI_BP_WR_Y_OFFS_CNT_START	0x0210	W	0x00000000	Offset counter start value for bypass picture Y component ring buffer
MI_1400_MI_BP_WR_Y_LLENGTH	0x0214	W	0x00000000	Line length of bypass picture Y component
MI_1400_MI_BP_WR_Y_PIC_WIDTH	0x0218	W	0x00000000	Y component image width for bypass picture
MI_1400_MI_BP_WR_Y_PIC_HEIGHT	0x021C	W	0x00000000	Y component image height for bypass picture
MI_1400_MI_BP_WR_Y_PIC_SIZE	0x0220	W	0x00000000	Y component image size for bypass picture
MI_1400_MI_BP_WR_CB_BASE	0x0224	W	0x00000000	Base address for bypass picture Cb component ring buffer
MI_1400_MI_BP_WR_CB_SIZE	0x0228	W	0x00000000	Size of bypass picture Cb component ring buffer
MI_1400_MI_BP_WR_CB_OFFS_CNT	0x022C	W	0x00000000	Offset counter initial value for bypass picture Cb component ring buffer
MI_1400_MI_BP_WR_CB_OFFS_CNT_START	0x0230	W	0x00000000	Offset counter start value for bypass picture Cb component ring buffer
MI_1400_MI_BP_WR_Y_BASE_SHD	0x0234	W	0x00000000	Base address shadow register for bypass picture Y component ring buffer
MI_1400_MI_BP_WR_Y_SIZE_SHD	0x0238	W	0x00000000	Size shadow register of bypass picture Y component ring buffer
MI_1400_MI_BP_WR_Y_OFFS_CNT_SHD	0x023C	W	0x00000000	Current offset counter of bypass picture Y component ring buffer
MI_1400_MI_BP_WR_CB_BASE_SHD	0x0240	W	0x00000000	Base address shadow register for bypass picture Cb component ring buffer
MI_1400_MI_BP_WR_CB_SIZE_SHD	0x0244	W	0x00000000	Size shadow register of bypass picture Cb component ring buffer
MI_1400_MI_BP_WR_CB_OFFS_CNT_SHD	0x0248	W	0x00000000	Current offset counter of bypass picture Cb component ring buffer

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Name	Offset	Size	Reset Value	Description
MI_1400_MI_BP_WR_Y_BASE2	0x024C	W	0x00000000	Base address 2 (ping pong) for bypass picture Y component
MI_1400_MI_BP_WR_CB_BASE2	0x0250	W	0x00000000	Base address 2 (ping pong) for bypass picture Cb component
MI_1400_MI_MP_WR_Y_END_ADDR	0x0260	W	0x00000000	MP y frame end address
MI_1400_MI_MP_WR_CB_END_ADDR	0x0264	W	0x00000000	MP uv frame end address
MI_1400_MI_SP_WR_Y_END_ADDR	0x0268	W	0x00000000	SP y frame end address
MI_1400_MI_SP_WR_CB_END_ADDR	0x026C	W	0x00000000	SP uv frame end address
MI_1400_MI_BP_WR_Y_END_ADDR	0x0270	W	0x00000000	BP y frame end address
MI_1400_MI_BP_WR_CB_END_ADDR	0x0274	W	0x00000000	BP uv frame end address
MI_1400_MI_MPDS_WR_Y_END_ADDR	0x0278	W	0x00000000	MPDS y frame end address
MI_1400_MI_MPDS_WR_CB_END_ADDR	0x027C	W	0x00000000	MPDS uv frame end address
MI_1400_MI_BPDS_WR_Y_END_ADDR	0x0280	W	0x00000000	BPDS y frame end address
MI_1400_MI_BPDS_WR_CB_END_ADDR	0x0284	W	0x00000000	BPDS uv frame end address
MI_1400_MI_MPDS_WR_CTRL	0x02A0	W	0x00000200	Main path down sampling write control register
MI_1400_MI_MPDS_WR_Y_BASE	0x02A4	W	0x00000000	Base address for main path down sampling Y component
MI_1400_MI_MPDS_WR_Y_SIZE	0x02A8	W	0x00000000	Size of main path down sampling Y component
MI_1400_MI_MPDS_WR_Y_OFFS_CNT	0x02AC	W	0x00000000	Offset counter initial value for main path down sampling Y
MI_1400_MI_MPDS_WR_Y_OFFS_CNT_START	0x02B0	W	0x00000000	Offset counter start value for main path down sampling Y
MI_1400_MI_MPDS_WR_Y_LLENGTH	0x02B4	W	0x00000000	Line length of main path down sampling Y component
MI_1400_MI_MPDS_WR_Y_PIC_WIDTH	0x02B8	W	0x00000000	Y component image width for main path down sampling
MI_1400_MI_MPDS_WR_Y_PIC_HEIGHT	0x02BC	W	0x00000000	Y component image height for main path down sampling
MI_1400_MI_MPDS_WR_Y_PIC_SIZE	0x02C0	W	0x00000000	Y component image size
MI_1400_MI_MPDS_WR_CB_BASE	0x02C4	W	0x00000000	Base address for main path down sampling UV component
MI_1400_MI_MPDS_WR_CB_SIZE	0x02C8	W	0x00000000	Size of main path down sampling UV component
MI_1400_MI_MPDS_WR_CB_OFFS_CNT	0x02CC	W	0x00000000	Offset counter initial value for main path down sampling UV
MI_1400_MI_MPDS_WR_CB_OFFS_CNT_START	0x02D0	W	0x00000000	Offset counter start value for main path down sampling CB
MI_1400_MI_MPDS_WR_Y_BASE_SHD	0x02D4	W	0x00000000	Base address shadow register for main path down sampling Y component ring buffer

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Name	Offset	Size	Reset Value	Description
MI_1400_MI_MPDS_WR_Y_SIZE_SHD	0x02D8	W	0x00000000	Size shadow register of main path down sampling Y component
MI_1400_MI_MPDS_WR_Y_OFFS_CNT_SHD	0x02DC	W	0x00000000	Current offset counter of main path down samplinge Y component ring buffer
MI_1400_MI_MPDS_WR_CB_BASE_SHD	0x02E0	W	0x00000000	Base address shadow register for main path down sampling UV component ring buffer
MI_1400_MI_MPDS_WR_CB_SIZE_SHD	0x02E4	W	0x00000000	Size shadow register of main path down sampling UV component ring buffer
MI_1400_MI_MPDS_WR_CB_OFFS_CNT_SHD	0x02E8	W	0x00000000	Current offset counter of main path down sampling UV component ring buffer
MI_1400_MI_BPDS_WR_CTRL	0x02F0	W	0x00000200	Bypass path down sampling write control register
MI_1400_MI_BPDS_WR_Y_BASE	0x02F4	W	0x00000000	Base address for bypass path down sampling Y component
MI_1400_MI_BPDS_WR_Y_SIZE	0x02F8	W	0x00000000	Size of bypass path down sampling Y component
MI_1400_MI_BPDS_WR_Y_OFFS_CNT	0x02FC	W	0x00000000	Offset counter initial value for bypass path down sampling Y
MI_1400_MI_BPDS_WR_Y_OFFS_CNT_START	0x0300	W	0x00000000	Offset counter start value for bypass path down sampling Y
MI_1400_MI_BPDS_WR_Y_LLENGTH	0x0304	W	0x00000000	Line length of bypass path down sampling Y component
MI_1400_MI_BPDS_WR_Y_PIC_WIDTH	0x0308	W	0x00000000	Y component image width for bypass path down sampling
MI_1400_MI_BPDS_WR_Y_PIC_HEIGHT	0x030C	W	0x00000000	Y component image height for bypass path down sampling
MI_1400_MI_BPDS_WR_Y_PIC_SIZE	0x0310	W	0x00000000	Y component image size
MI_1400_MI_BPDS_WR_CB_BASE	0x0314	W	0x00000000	Base address for bypass path down sampling UV component
MI_1400_MI_BPDS_WR_CB_SIZE	0x0318	W	0x00000000	Size of bypass path down sampling UV component
MI_1400_MI_BPDS_WR_CB_OFFS_CNT	0x031C	W	0x00000000	Offset counter initial value for bypass path down sampling UV
MI_1400_MI_BPDS_WR_CB_OFFS_CNT_START	0x0320	W	0x00000000	Offset counter start value for bypass path down sampling CB
MI_1400_MI_BPDS_WR_Y_BASE_SHD	0x0324	W	0x00000000	Base address shadow register for bypass path down sampling Y component ring buffer
MI_1400_MI_BPDS_WR_Y_SIZE_SHD	0x0328	W	0x00000000	Size shadow register of bypass path down sampling Y component
MI_1400_MI_BPDS_WR_Y_OFFS_CNT_SHD	0x032C	W	0x00000000	Current offset counter of bypass path down sampling Y component ring buffer
MI_1400_MI_BPDS_WR_CB_BASE_SHD	0x0330	W	0x00000000	Base address shadow register for bypass path down sampling UV component ring buffer
MI_1400_MI_BPDS_WR_CB_SIZE_SHD	0x0334	W	0x00000000	Size shadow register of bypass path down sampling UV component ring buffer

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Name	Offset	Size	Reset Value	Description
MI_1400_MI_BPDS_WR_CB_OFFS_CNT_SHD	0x0338	W	0x00000000	Current offset counter of bypass path down sampling UV component ring buffer
MI_1400_MI_WR_CTRL2	0x0400	W	0x00000400	New path control register
MI_1400_MI_WR_ID2	0x0404	W	0x00000000	AXI write id group2
MI_1400_MI_RD_CTRL2	0x0408	W	0x00A50800	DMA path control register
MI_1400_MI_RD_ID	0x040C	W	0x00000000	AXI read id group
MI_1400_MI_WR_CTRL2_SHD	0x0410	W	0x00000000	New path control register
MI_1400_MI_WR_WRAP_CTRL	0x0414	W	0x00000037	MI write wrap control
MI_1400_MI_WR_VFLIP_CTRL	0x0418	W	0x00000000	MI write wrap control
MI_1400_RAW0_RD_BASE	0x0470	W	0x00000000	Base address for mipi raw0 rx. Raw write function move to VICAP, not support in ISP3.X....
MI_1400_RAW0_RD_LENGTH	0x0474	W	0x00000000	Line length of raw0 rx (virtual width). Raw write function move to VICAP, not support in ISP3.X....
MI_1400_RAW0_RD_BASE_SHD	0x0478	W	0x00000000	Base shadow address for mipi raw0 rx. Update mode include hdr_dbg read pulse.Raw write function move to VICAP, not support in ISP3.X....
MI_1400_RAW0_RD_SIZE	0x047C	W	0x00000000	Frame size of raw0 read
MI_1400_RAW1_RD_BASE	0x0480	W	0x00000000	Base address for mipi raw1 rx. Raw write function move to VICAP, not support in ISP3.X....
MI_1400_RAW1_RD_LENGTH	0x0484	W	0x00000000	Line length of raw1 rx (virtual width). Raw write function move to VICAP, not support in ISP3.X....
MI_1400_RAW1_RD_BASE_SHD	0x0488	W	0x00000000	Base shadow address for mipi raw1 rx. Update mode include hdr_dbg read pulse.Raw write function move to VICAP, not support in ISP3.X....
MI_1400_RAW1_RD_SIZE	0x048C	W	0x00000000	Frame size of raw1 read
MI_1400_RAWS_RD_BASE	0x0490	W	0x00000000	Base address for mipi raws rx. Raw write function move to VICAP, not support in ISP3.X....
MI_1400_RAWS_RD_LENGTH	0x0494	W	0x00000000	Line length of raws rx (virtual width). Raw write function move to VICAP, not support in ISP3.X....
MI_1400_RAWS_RD_BASE_SHD	0x0498	W	0x00000000	Base shadow address for mipi rawsrx. Update mode include hdr_dbg read pulse.Raw write function move to VICAP, not support in ISP3.X....
MI_1400_RAWS_RD_SIZE	0x049C	W	0x00000000	Frame size of raws read
MI_1400_RAW_RD_WRAP_CTRL	0x04A0	W	0x00000000	AXI configure read control for module registers, except MMU.
MI_1400_RAWS_RD_OFFS_BASE	0x04A4	W	0x00000000	Raws offset address for two sensors slice boundary expand

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Name	Offset	Size	Reset Value	Description
MI_1400_RAW0_RD_WRAP_DEBUG0	0x04B0	W	0x00000000	Raw0 dma read wrap debug0
MI_1400_RAW0_RD_WRAP_DEBUG1	0x04B4	W	0x00000000	Raw0 dma read wrap debug1
MI_1400_RAWS_RD_WRAP_DEBUG0	0x04B8	W	0x00000000	Raws dma read wrap debug0
MI_1400_RAWS_RD_WRAP_DEBUG1	0x04BC	W	0x00000000	Raws dma read wrap debug1
MI_1400_LUT_CAC_RD_BASE	0x0530	W	0x00000000	Base address for cac read
MI_1400_LUT_CAC_RD_H_WSIZE	0x0534	W	0x00000000	Cac word size
MI_1400_LUT_CAC_RD_V_SIZE	0x0538	W	0x00000000	Cac lut v_size
MI_1400_LUT_3D_RD_BASE	0x0540	W	0x00000000	Base address for 3d lut read
MI_1400_LUT_LSC_RD_BASE	0x0544	W	0x00000000	Base address for lsc lut read
MI_1400_LUT_LDCH_RD_BASE	0x0548	W	0x00000000	Base address for ldch lut read
MI_1400_LUT_3D_RD_WSIZE	0x0550	W	0x000002D9	3d lut word size
MI_1400_LUT_LSC_RD_WSIZE	0x0554	W	0x00000000	3d lut word size
MI_1400_LUT_LDCH_RD_H_WSIZE	0x0558	W	0x00000000	Ldch lut word size
MI_1400_LUT_LDCH_RD_V_SIZE	0x055C	W	0x00000000	Ldch lut vertical size
MI_1400_AIISP_GAIN_RD_HV_SIZE	0x0560	W	0x00000000	AI-ISP gain read horizontal and vertical size
MI_1400_W3A_WR_SIZE	0x0564	W	0x00000000	Size of 3a write data
MI_1400_W3A_WR_LENGTH	0x0568	W	0x00000000	Line length of 3a write (virtual width)
MI_1400_W3A_WR_BASE_SHD	0x056C	W	0x00000000	Base address shadow register for 3a write data ring buffer
MI_1400_AIISP_RD_BASE	0x0570	W	0x00000000	Base address for ai-isp data read
MI_1400_AIISP_RD_LENGTH	0x0574	W	0x00000000	Line length of ai-isp data read (virtual width)
MI_1400_AIISP_RD_BASE_SHD	0x0578	W	0x00000000	Base shadow address for ai-isp data read
MI_1400_W3A_WR_BASE	0x057C	W	0x00000000	AXI write 3A data to DDR address
MI_1400_GAIN_WR_BASE	0x0580	W	0x00000000	Base address for gain data write
MI_1400_GAIN_WR_SIZE	0x0584	W	0x00000000	Size of gain write data
MI_1400_GAIN_WR_LENGTH	0x0588	W	0x00000000	Line length of gain data write (virtual width)
MI_1400_GAIN_WR_BASE2	0x058C	W	0x00000000	Base address 2 for gain data write
MI_1400_GAIN_WR_BASE_SHD	0x0590	W	0x00000000	Base address shadow register for gain write data ring buffer
MI_1400_BAY3D_IIR_WR_BASE	0x05A0	W	0x00000000	Base address for bayer 3dnr iir write
MI_1400_BAY3D_IIR_WR_SIZE	0x05A4	W	0x00000000	Size of bayer 3dnr iir write data

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Name	Offset	Size	Reset Value	Description
MI_1400_BAY3D_IIR_WR_LENGTH	0x05A8	W	0x00000000	Line length of bayer 3dnr iir write (virtual width)
MI_1400_BAY3D_IIR_WR_BASE_SHD	0x05AC	W	0x00000000	Base address shadow register for bayer 3dnr iir write data ring buffer
MI_1400_BAY3D_IIR_RD_BASE	0x05B0	W	0x00000000	Base address for bayer 3dnr read
MI_1400_BAY3D_IIR_RD_LENGTH	0x05B4	W	0x00000000	Line length of bayer 3dnr read (virtual width)
MI_1400_BAY3D_IIR_RD_BASE_SHD	0x05B8	W	0x00000000	Base shadow address for bayer 3dnr read
MI_1400_BAY3D_CUR_WR_BASE	0x05C0	W	0x00000000	Base address for bayer 3dnr current write
MI_1400_BAY3D_CUR_WR_SIZE	0x05C4	W	0x00000000	Size of bayer 3dnr current write data
MI_1400_BAY3D_CUR_WR_LENGTH	0x05C8	W	0x00000000	Line length of bayer 3dnr current write (virtual width)
MI_1400_BAY3D_CUR_WR_BASE_SHD	0x05CC	W	0x00000000	Base address shadow register for bayer 3dnr current write data ring buffer
MI_1400_BAY3D_CUR_RD_BASE	0x05D0	W	0x00000000	Base address for bayer 3dnr read
MI_1400_BAY3D_CUR_RD_LENGTH	0x05D4	W	0x00000000	Line length of bayer 3dnr read (virtual width)
MI_1400_BAY3D_CUR_RD_BASE_SHD	0x05D8	W	0x00000000	Base shadow address for bayer 3dnr read
MI_1400_BAY3D_CUR_RD_SIZE	0x05DC	W	0x00000000	Frame size of bayer 3dnr read
MI_1400_BAY3D_DS_WR_BASE	0x05E0	W	0x00000000	Base address for bayer 3dnr down scale write
MI_1400_BAY3D_DS_WR_SIZE	0x05E4	W	0x00000000	Size of bayer 3dnr down scale write data
MI_1400_BAY3D_DS_WR_LENGTH	0x05E8	W	0x00000000	Line length of bayer 3dnr down scale write (virtual width)
MI_1400_BAY3D_DS_WR_BASE_SHD	0x05EC	W	0x00000000	Base address shadow register for bayer 3dnr down scale write data ring buffer
MI_1400_BAY3D_DS_RD_BASE	0x05F0	W	0x00000000	Base address for bayer 3dnr read
MI_1400_BAY3D_DS_RD_LENGTH	0x05F4	W	0x00000000	Line length of bayer 3dnr read (virtual width)
MI_1400_BAY3D_DS_RD_BASE_SHD	0x05F8	W	0x00000000	Base shadow address for bayer 3dnr read
MI_1400_B3DMCH_RD_BASE	0x0600	W	0x00000000	Base address for b3dmch read
MI_1400_B3DMCH_RD_LENGTH	0x0604	W	0x00000000	Line length of b3dmch read (virtual width)
MI_1400_B3DMCH_RD_HWSIZE	0x0608	W	0x00000000	B3dmch read word size of horizontal direction
MI_1400_B3DMCH_RD_VSIZE	0x060C	W	0x00000000	B3dmch size of vertical direction
MI_1400_IRLDCV_RD_BASE	0x0610	W	0x00000000	Base address for irldc vertical read

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Name	Offset	Size	Reset Value	Description
MI_1400_IRLDCV_RD_LENGTH	0x0614	W	0x00000000	Line length of irldc vertical read (virtual width)
MI_1400_IRLDCV_RD_HWSIZE	0x0618	W	0x00000000	Irldc vertical read word size of horizontal direction
MI_1400_IRLDCV_RD_VSIZE	0x061C	W	0x00000000	Irldc vertical size of vertical direction
MI_1400_IRLDCV_RD_BASE_SHD	0x0624	W	0x00000000	Base shadow address for irldc vertical read
MI_1400_B3DMCV_RD_BASE	0x0630	W	0x00000000	Base address for b3dmcv read
MI_1400_B3DMCV_RD_LENGTH	0x0634	W	0x00000000	Line length of b3dmcv read (virtual width)
MI_1400_B3DMCV_RD_HWSIZE	0x0638	W	0x00000000	B3dmcv read word size of horizontal direction
MI_1400_B3DMCV_RD_VSIZE	0x063C	W	0x00000000	B3dmcv size of vertical direction
MI_1400_AXI_CONF_RD_CTRL	0x0640	W	0x80000000	AXI configure read control for module registers, except MMU.
MI_1400_AXI_CONF_RD_BASE	0x0644	W	0x00000000	Base address for axi configure read
MI_1400_AXI_CONF_RD_H_WSIZE	0x0648	W	0x00000000	AXI configure read word size of horizontal direction
MI_1400_AXI_CONF_RD_V_SIZE	0x064C	W	0x00000000	AXI configure size of vertical direction
MI_1400_FRM_BUF_WR_BASE	0x0650	W	0x00000000	Base address for frame buffer write
MI_1400_FRM_BUF_WR_SIZE	0x0654	W	0x00000000	Size of frame buffer write data
MI_1400_FRM_BUF_RD_BASE	0x0658	W	0x00000000	Base address for frame buff read
MI_1400_AXI_RW_DBG	0x0660	W	0x00000000	AXI debug

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

44.4.1.4 ISP_TOP

Name	Offset	Size	Reset Value	Description
ISP_0400_CTRL0	0x0000	W	0x00006000	Global control register
ISP_0400_CTRL1	0x0004	W	0x0F800060	ISP acquisition properties
ISP_0400_ACQ_H_OFFS	0x0008	W	0x00000000	Horizontal input offset
ISP_0400_ACQ_V_OFFS	0x000C	W	0x00000000	Vertical input offset
ISP_0400_ACQ_H_SIZE	0x0010	W	0x10001000	Horizontal input size
ISP_0400_ACQ_V_SIZE	0x0014	W	0x00000C00	Vertical input size
ISP_0400_ACQ_NR_FRAMES	0x0018	W	0x00000000	Number of frames to be captured
ISP_0400_AWB1_GAIN_G	0x0130	W	0x01000100	Auto white balance gain green after bayer-3dnr
ISP_0400_AWB1_GAIN_RB	0x0134	W	0x01000100	Auto white balance gain red and blue after bayer-3dnr
ISP_0400_AWB0_GAIN0_G	0x0138	W	0x01000100	Auto white balance gain green for normal channel and short-expose frame

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Name	Offset	Size	Reset Value	Description
ISP_0400_AWB0_GAIN0_RB	0x013C	W	0x01000100	Auto white balance gain red and blue for normal channel and short-expose frame
ISP_0400_AWB0_GAIN1_G	0x0140	W	0x00000000	Auto white balance gain green for Long-Expose frame(HDRx2) or Middle-Expose frame(HDRx3)
ISP_0400_AWB0_GAIN1_RB	0x0144	W	0x00000000	Auto white balance gain red and blue for Long-Expose frame(HDRx2) or Middle-Expose frame(HDRx3)
ISP_0400_AWB0_GAIN2_G	0x0148	W	0x00000000	Auto white balance gain green for Long-Expose frame(HDRx3)
ISP_0400_AWB0_GAIN2_RB	0x014C	W	0x00000000	Auto white balance gain red and blue for Long-Expose frame(HDRx3)
ISP_0400_HURRY_CTRL	0x0158	W	0x00006583	Isp interconnect hurry control
ISP_0400_AWQOS_CTRL	0x015C	W	0x00123121	AXI write qos to interconnect control
ISP_0400_ARQOS_CTRL	0x0160	W	0x01212131	AXI read qos to interconnect control
ISP_0400_IRQ_CFG0	0x0164	W	0x00000000	ISP out irq configure register0
ISP_0400_IRQ_CFG1	0x0168	W	0x00000000	ISP out irq configure register1
ISP_0400_CC_COEFF_0	0x0170	W	0x00000021	Color conversion coefficient 0
ISP_0400_CC_COEFF_1	0x0174	W	0x00000040	Color conversion coefficient 1
ISP_0400_CC_COEFF_2	0x0178	W	0x0000000D	Color conversion coefficient 2
ISP_0400_CC_COEFF_3	0x017C	W	0x000001ED	Color conversion coefficient 3
ISP_0400_CC_COEFF_4	0x0180	W	0x000001DB	Color conversion coefficient 4
ISP_0400_CC_COEFF_5	0x0184	W	0x00000038	Color conversion coefficient 5
ISP_0400_CC_COEFF_6	0x0188	W	0x00000038	Color conversion coefficient 6
ISP_0400_CC_COEFF_7	0x018C	W	0x000001D1	Color conversion coefficient 7
ISP_0400_CC_COEFF_8	0x0190	W	0x000001F7	Color conversion coefficient 8
ISP_0400_OUT_H_OFFS	0x0194	W	0x00000000	Horizontal offset of output window
ISP_0400_OUT_V_OFFS	0x0198	W	0x00000000	Vertical offset of output window
ISP_0400_OUT_H_SIZE	0x019C	W	0x00001000	Output horizontal picture size
ISP_0400_OUT_V_SIZE	0x01A0	W	0x00000C00	Output vertical picture size
ISP_0400_FLAGS_SHD	0x01A8	W	0x00000000	Flags (current status) of certain signals and Shadow registers for enable signals
ISP_0400_OUT_H_OFFS_SHD	0x01AC	W	0x00000000	Current horizontal offset of output window (shadow register)
ISP_0400_OUT_V_OFFS_SHD	0x01B0	W	0x00000000	Current vertical offset of output window (shadow register)
ISP_0400_OUT_H_SIZE_SHD	0x01B4	W	0x00000000	Current output horizontal picture size (shadow register)
ISP_0400_OUT_V_SIZE_SHD	0x01B8	W	0x00000000	Current output vertical picture size (shadow register)
ISP_0400_ISP_IMSC	0x01BC	W	0x00000000	Interrupt mask
ISP_0400_ISP_RIS	0x01C0	W	0x00000000	Raw interrupt status
ISP_0400_ISP_MIS	0x01C4	W	0x00000000	Masked interrupt status
ISP_0400_ISP_ICR	0x01C8	W	0x00000000	Interrupt clear register, high clear
ISP_0400_ISP_ISR	0x01CC	W	0x00000000	Interrupt set register, high set
ISP_0400_ISP3A_IMSC	0x01D0	W	0x00000000	Interrupt mask
ISP_0400_ISP3A_RIS	0x01D4	W	0x00000000	Raw interrupt status

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Name	Offset	Size	Reset Value	Description
ISP_0400_ISP3A_MIS	0x01D8	W	0x00000000	Masked interrupt status
ISP_0400_ISP3A_ICR	0x01DC	W	0x00000000	Interrupt clear register
ISP_0400_ERR	0x023C	W	0x00000000	ISP error register
ISP_0400_ERR_CLR	0x0240	W	0x00000000	ISP error clear registerplease reference ERR
ISP_0400_FRAME_COUNT	0x0244	W	0x00000000	Frame counter
ISP_0400_DEBUG1	0x0248	W	0x00000000	RKISP_DEBUG1
ISP_0400_DEBUG2	0x024C	W	0x00000000	RKISP_DEBUG2
ISP_0400_DEBUG3	0x0250	W	0x00000000	RKISP_DEBUG3
ISP_0400_DEBUG4	0x0254	W	0x00000000	RKISP_DEBUG4
ISP_0400_YNR_LUMA_RCTRL	0x0290	W	0x00000000	YNR luma ahb readback control register
ISP_0400_YNR_LUMA_RDATA	0x0294	W	0x00000000	YNR luma ahb readback data.
ISP_0400_STITCH_CTRL0	0x0298	W	0x00000000	Multi-sensor stitch control0
ISP_0400_STITCH_CTRL1	0x029C	W	0x00000000	Multi-sensor stitch control1
ISP_0400_STITCH_CTRL2	0x02A0	W	0x00000000	Multi-sensor stitch control2
ISP_0400_SLICE_ST_CTRL	0x02A4	W	0x00000000	ISP slice start control
ISP_0400_AIISP_LINE_CNT	0x02A8	W	0x00000000	AI-ISP_DEBUG

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

44.4.1.5 CTRL

Name	Offset	Size	Reset Value	Description
CTRL_0000_VI_ISP_EN	0x0000	W	0x00000000	Isp_top_en control
CTRL_0000_VI_ISP_PATH	0x0004	W	0x00000000	3A path select
CTRL_0000_VI_ID	0x0008	W	0x03012106	Revision identification register
CTRL_0000_VI_ISP_CLK_CTRL	0x000C	W	0x00000000	Internal clock control register
CTRL_0000_VI_ICCL	0x0010	W	0x00006F5B	Internal clock control register
CTRL_0000_VI_IRCL	0x0014	W	0x00000000	Internal reset control register
CTRL_0000_VI_DPCL	0x0018	W	0x00000000	Data path control register
CTRL_0000_SWS_CFG	0x001C	W	0x00000000	Isp2enc handshake signals and 3A write

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

44.4.1.6 BLS

Name	Offset	Size	Reset Value	Description
ISP_BLS_3000_CTRL	0x0000	W	0x00000000	Global control register
ISP_BLS_3000_SAMPLES	0x0004	W	0x00000000	Samples register
ISP_BLS_3000_H1_START	0x0008	W	0x00000000	Window 1 horizontal start
ISP_BLS_3000_H1_STOP	0x000C	W	0x00000000	Window 1 horizontal stop
ISP_BLS_3000_V1_START	0x0010	W	0x00000000	Window 1 vertical start
ISP_BLS_3000_V1_STOP	0x0014	W	0x00000000	Window 1 vertical stop
ISP_BLS_3000_H2_START	0x0018	W	0x00000000	Window 2 horizontal start
ISP_BLS_3000_H2_STOP	0x001C	W	0x00000000	Window 2 horizontal stop
ISP_BLS_3000_V2_START	0x0020	W	0x00000000	Window 2 vertical start
ISP_BLS_3000_V2_STOP	0x0024	W	0x00000000	Window 2 vertical stop

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Name	Offset	Size	Reset Value	Description
ISP_BLS_3000_BLC0_A_FIXED	0x0028	W	0x00000000	Fixed black level A of main-path
ISP_BLS_3000_BLC0_B_FIXED	0x002C	W	0x00000000	Fixed black level B of main-path
ISP_BLS_3000_BLC0_C_FIXED	0x0030	W	0x00000000	Fixed black level C of main-path
ISP_BLS_3000_BLC0_D_FIXED	0x0034	W	0x00000000	Fixed black level D of main-path
ISP_BLS_3000_A_MEASURED	0x0038	W	0x00000000	Measured black level A
ISP_BLS_3000_B_MEASURED	0x003C	W	0x00000000	Measured black level B
ISP_BLS_3000_C_MEASURED	0x0040	W	0x00000000	Measured black level C
ISP_BLS_3000_D_MEASURED	0x0044	W	0x00000000	Measured black level D
ISP_BLS_3000_BLS1_A_FIXED	0x0048	W	0x00000000	Fixed black level A of bay3dnr-blc
ISP_BLS_3000_BLS1_B_FIXED	0x004C	W	0x00000000	Fixed black level B of bay3dnr-blc
ISP_BLS_3000_BLS1_C_FIXED	0x0050	W	0x00000000	Fixed black level C of bay3dnr-blc
ISP_BLS_3000_BLS1_D_FIXED	0x0054	W	0x00000000	Fixed black level D of bay3dnr-blc
ISP_BLS_3000_BLS2_A_FIXED	0x0058	W	0x00000000	Fixed black level A of 3a-awb
ISP_BLS_3000_BLS2_B_FIXED	0x005C	W	0x00000000	Fixed black level B of 3a-awb
ISP_BLS_3000_BLS2_C_FIXED	0x0060	W	0x00000000	Fixed black level C of 3a-awb
ISP_BLS_3000_BLS2_D_FIXED	0x0064	W	0x00000000	Fixed black level D of 3a-awb
ISP_BLS_3000_ISP_OB_OFFSET	0x0068	W	0x00000000	OB value for protecting dark texture, if not equal to zero then bls1 will auto-enable
ISP_BLS_3000_ISP_OB_PREDGAIN	0x006C	W	0x00000100	OB pre-dgain8,8 for replacing adrc-gain, in linear mode
ISP_BLS_3000_ISP_OB_MAX	0x0070	W	0x000FFFFF	AWB1 max value clip, value equal to predgain*0xfff.
ISP_BLS_3000_BLS3_AB_FIXED	0x0074	W	0x00000000	Signed two's complement, value range from -4096 to +4095, a positive value will be subtracted from the pixel values.
ISP_BLS_3000_BLS3_CD_FIXED	0x0078	W	0x00000000	Signed two's complement, value range from -4096 to +4095, a positive value will be subtracted from the pixel values.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

44.4.1.7 DPCC

Name	Offset	Size	Reset Value	Description
ISP_DPCC_3400_CTRL0	0x0000	W	0x00000004	DPCC global control 0

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Name	Offset	Size	Reset Value	Description
ISP_DPCC_3400_CTRL1	0x0004	W	0x00000003	DPCC global control 1
ISP_DPCC_3400_CTRL2	0x0008	W	0x00000001	DPCC global control 2
ISP_DPCC_3400_ENGINE0_CTRL	0x000C	W	0x00000101	All this methods enable bits for ENGINE0
ISP_DPCC_3400_ENGINE1_CTRL	0x0010	W	0x00000101	All this methods enable bits for ENGINE1
ISP_DPCC_3400_ENGINE2_CTRL	0x0014	W	0x00000101	All this methods enable bits for ENGINE2
ISP_DPCC_3400_ENGINE0_SET0	0x0018	W	0x00000000	EPD set0
ISP_DPCC_3400_ENGINE0_SET1	0x001C	W	0x00000404	EPD set1
ISP_DPCC_3400_ENGINE0_SET2	0x0020	W	0x00000400	PD factor
ISP_DPCC_3400_ENGINE0_SET3	0x0024	W	0x00000A0A	RDD factor
ISP_DPCC_3400_ENGINE0_SET4	0x0028	W	0x00002020	RD factor
ISP_DPCC_3400_ENGINE1_SET0	0x002C	W	0x00000000	EPD set0
ISP_DPCC_3400_ENGINE1_SET1	0x0030	W	0x00000404	EPD set1
ISP_DPCC_3400_ENGINE1_SET2	0x0034	W	0x00000400	PD factor
ISP_DPCC_3400_ENGINE1_SET3	0x0038	W	0x00000A0A	RDD factor
ISP_DPCC_3400_ENGINE1_SET4	0x003C	W	0x00002020	RD factor
ISP_DPCC_3400_ENGINE2_SET0	0x0040	W	0x00000000	EPD set0
ISP_DPCC_3400_ENGINE2_SET1	0x0044	W	0x00000404	EPD set1
ISP_DPCC_3400_ENGINE2_SET2	0x0048	W	0x00000400	PD factor
ISP_DPCC_3400_ENGINE2_SET3	0x004C	W	0x00000A0A	RDD factor
ISP_DPCC_3400_ENGINE2_SET4	0x0050	W	0x00002020	RD factor
ISP_DPCC_3400_ENGINE_OD_SET	0x0054	W	0x00000000	Order Detect Limits
ISP_DPCC_3400_ENGINE_RDD_SET	0x0058	W	0x0000073F	RDD range set
ISP_DPCC_3400_PDAF_EN	0x0070	W	0x00000000	Pdaf enable
ISP_DPCC_3400_PDAF_POINT_EN	0x0074	W	0x00000000	Enable for each pdaf point
ISP_DPCC_3400_PDAF_OFFSET	0x0078	W	0x00000000	Pdaf point offset position in wrapper
ISP_DPCC_3400_PDAF_WRAP	0x007C	W	0x00000000	Pdaf pattern size
ISP_DPCC_3400_PDAF_SCOPE	0x0080	W	0x00000000	The number of DPCC pattern
ISP_DPCC_3400_PDAF_POINT_0	0x0084	W	0x00000000	Point0 & point1 coordinate

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Name	Offset	Size	Reset Value	Description
ISP_DPCC_3400_PDAF_POINT_1	0x0088	W	0x00000000	Point2 & point3 coordinate
ISP_DPCC_3400_PDAF_POINT_2	0x008C	W	0x00000000	Point4 & point5 coordinate
ISP_DPCC_3400_PDAF_POINT_3	0x0090	W	0x00000000	Point6 & point7 coordinate
ISP_DPCC_3400_PDAF_POINT_4	0x0094	W	0x00000000	Point8 & point9 coordinate
ISP_DPCC_3400_PDAF_POINT_5	0x0098	W	0x00000000	Point10 & point11 coordinate
ISP_DPCC_3400_PDAF_POINT_6	0x009C	W	0x00000000	Point12 & point13 coordinate
ISP_DPCC_3400_PDAF_POINT_7	0x00A0	W	0x00000000	Point14 & point15 coordinate
ISP_DPCC_3400_PDAF_FORWARD_MED	0x00A4	W	0x00000000	Median value = center point = pdaf point , select forward median value or backwrad median value to replace pdaf point

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

44.4.1.8 HDRMGE

Name	Offset	Size	Reset Value	Description
ISP_HDRMGE_3800_CTRL	0x0000	W	0x00000000	Global control
ISP_HDRMGE_3800_GAIN0	0x0008	W	0x01000400	Gain0 configuration of S-frame
ISP_HDRMGE_3800_GAIN1	0x000C	W	0x04000100	Gain1 configuration of M-frame
ISP_HDRMGE_3800_GAIN2	0x0010	W	0x00000040	Gain2 configuration of L-frame (1106 no use)
ISP_HDRMGE_3800_LIGHTZ	0x0014	W	0x00FF00FF	Light zone configuration
ISP_HDRMGE_3800_MS_DIFF	0x0018	W	0x80000080	Ms_diff configuration
ISP_HDRMGE_3800_LM_DIFF	0x001C	W	0x80000080	Lm_diff configuration (1106 no use)
ISP_HDRMGE_3800_DIFF_Y0	0x0020	W	0x00000000	Y value of L-curve0,1 configuration
ISP_HDRMGE_3800_DIFF_Y1	0x0024	W	0x00C900C9	Y value of L-curve0,1 configuration
ISP_HDRMGE_3800_DIFF_Y2	0x0028	W	0x01FA01FA	Y value of L-curve0,1 configuration
ISP_HDRMGE_3800_DIFF_Y3	0x002C	W	0x02C002C0	Y value of L-curve0,1 configuration
ISP_HDRMGE_3800_DIFF_Y4	0x0030	W	0x032F032F	Y value of L-curve0,1 configuration
ISP_HDRMGE_3800_DIFF_Y5	0x0034	W	0x03700370	Y value of L-curve0,1 configuration
ISP_HDRMGE_3800_DIFF_Y6	0x0038	W	0x03970397	Y value of L-curve0,1 configuration
ISP_HDRMGE_3800_DIFF_Y7	0x003C	W	0x03B103B1	Y value of L-curve0,1 configuration

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Name	Offset	Size	Reset Value	Description
ISP_HDRMGE_3800_DIFF_Y8	0x0040	W	0x03C203C2	Y value of L-curve0,1 configuration
ISP_HDRMGE_3800_DIFF_Y9	0x0044	W	0x03CF03CF	Y value of L-curve0,1 configuration
ISP_HDRMGE_3800_DIFF_Y10	0x0048	W	0x03D803D8	Y value of L-curve0,1 configuration
ISP_HDRMGE_3800_DIFF_Y11	0x004C	W	0x03DE03DE	Y value of L-curve0,1 configuration
ISP_HDRMGE_3800_DIFF_Y12	0x0050	W	0x03E403E4	Y value of L-curve0,1 configuration
ISP_HDRMGE_3800_DIFF_Y13	0x0054	W	0x03E803E8	Y value of L-curve0,1 configuration
ISP_HDRMGE_3800_DIFF_Y14	0x0058	W	0x03EB03EB	Y value of L-curve0,1
ISP_HDRMGE_3800_DIFF_Y15	0x005C	W	0x03EE03EE	Y value of L-curve0,1
ISP_HDRMGE_3800_DIFF_Y16	0x0060	W	0x03F003F0	Y value of L-curve0,1
ISP_HDRMGE_3800_OVER_Y0	0x0070	W	0x0310C400	Y value of ES-curve
ISP_HDRMGE_3800_OVER_Y1	0x0074	W	0x05715C01	Y value of ES-curve configuration
ISP_HDRMGE_3800_OVER_Y2	0x0078	W	0x09826004	Y value of ES-curve configuration
ISP_HDRMGE_3800_OVER_Y3	0x007C	W	0x0FB3EC0E	Y value of ES-curve configuration
ISP_HDRMGE_3800_OVER_Y4	0x0080	W	0x18360C31	Y value of ES-curve configuration
ISP_HDRMGE_3800_OVER_Y5	0x0084	W	0x22088098	Y value of ES-curve configuration
ISP_HDRMGE_3800_OVER_Y6	0x0088	W	0x2B7ADD83	Y value of ES-curve configuration
ISP_HDRMGE_3800_OVER_Y7	0x008C	W	0x331CC6B7	Y value of ES-curve configuration
ISP_HDRMGE_3800_OVER_Y8	0x0090	W	0x386E1B86	Y value of ES-curve configuration
ISP_HDRMGE_3800_OVER_Y9	0x0094	W	0x3BBEEFDA	Y value of ES-curve configuration
ISP_HDRMGE_3800_OVER_Y10	0x0098	W	0x3DAF6BF5	Y value of ES-curve configuration
ISP_HDRMGE_3800_OVER_Y11	0x009C	W	0x3EBFAFFD	Y value of ES-curve configuration
ISP_HDRMGE_3800_OVER_Y12	0x00A0	W	0x3F5FD7FF	Y value of ES-curve configuration
ISP_HDRMGE_3800_OVER_Y13	0x00A4	W	0x3FAFEBFF	Y value of ES-curve configuration
ISP_HDRMGE_3800_OVER_Y14	0x00A8	W	0x3FDFF7FF	Y value of ES-curve configuration
ISP_HDRMGE_3800_OVER_Y15	0x00AC	W	0x3FEFFBFF	Y value of ES-curve configuration
ISP_HDRMGE_3800_OVER_Y16	0x00B0	W	0x3FFFFFFF	Y value of ES-curve configuration
ISP_HDRMGE_3800_EACH_GAIN	0x00B4	W	0x01000400	Gain configuration of each-raw

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*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

44.4.1.9 EXPANDER

Name	Offset	Size	Reset Value	Description
ISP_EXPANDER_3100_EXPD_K15	0x0000	W	0x00000000	EXPD_K15, k = slope*2^sw_expd_k_shift
ISP_EXPANDER_3100_EXPD_K16	0x0004	W	0x00000000	EXPD_K15, k = slope*2^sw_expd_k_shift
ISP_EXPANDER_3100_EXPD_K17	0x0008	W	0x00000000	EXPD_K17, k = slope*2^sw_expd_k_shift
ISP_EXPANDER_3100_EXPD_K18	0x000C	W	0x00000000	EXPD_K18, k = slope*2^sw_expd_k_shift
ISP_EXPANDER_3100_EXPD_K19	0x0010	W	0x00000000	EXPD_K19, k = slope*2^sw_expd_k_shift
ISP_EXPANDER_3100_EXPD_K20	0x0014	W	0x00000000	EXPD_K20, k = slope*2^sw_expd_k_shift
ISP_EXPANDER_3100_EXPD_K21	0x0018	W	0x00000000	EXPD_K21, k = slope*2^sw_expd_k_shift
ISP_EXPANDER_3100_EXPD_K22	0x001C	W	0x00000000	EXPD_K22, k = slope*2^sw_expd_k_shift
ISP_EXPANDER_3100_EXPD_K23	0x0020	W	0x00000000	EXPD_K23, k = slope*2^sw_expd_k_shift
ISP_EXPANDER_3100_EXPD_K24	0x0024	W	0x00000000	EXPD_K24, k = slope*2^sw_expd_k_shift
ISP_EXPANDER_3100_EXPD_K25	0x0028	W	0x00000000	EXPD_K25, k = slope*2^sw_expd_k_shift
ISP_EXPANDER_3100_EXPD_K26	0x002C	W	0x00000000	EXPD_K26, k = slope*2^sw_expd_k_shift
ISP_EXPANDER_3100_EXPD_K27	0x0030	W	0x00000000	EXPD_K27, k = slope*2^sw_expd_k_shift
ISP_EXPANDER_3100_EXPD_K28	0x0034	W	0x00000000	EXPD_K28, k = slope*2^sw_expd_k_shift
ISP_EXPANDER_3100_EXPD_K29	0x0038	W	0x00000000	EXPD_K29, k = slope*2^sw_expd_k_shift
ISP_EXPANDER_3100_EXPD_K30	0x003C	W	0x00000000	EXPD_K30, k = slope*2^sw_expd_k_shift
ISP_EXPANDER_3100_EXPD_K31	0x0040	W	0x00000000	EXPD_K31, k = slope*2^sw_expd_k_shift
ISP_EXPANDER_3100_EXPD_IMAX	0x0044	W	0x0000FFFF	Expd input maximum
ISP_EXPANDER_3100_EXPD_OMAX	0x0048	W	0x000FFFFF	Expd output maximum
ISP_EXPANDER_3100_EXPD_CTRL	0x0100	W	0x000000D0	Expd ctrl
ISP_EXPANDER_3100_EXPD_X00_01	0x0104	W	0x02000000	EXPD_X00_01,coordinate x
ISP_EXPANDER_3100_EXPD_X02_03	0x0108	W	0x048C0346	EXPD_X02_03,coordinate x
ISP_EXPANDER_3100_EXPD_X04_05	0x010C	W	0x071805D2	EXPD_X04_05,coordinate x
ISP_EXPANDER_3100_EXPD_X06_07	0x0110	W	0x09A4085E	EXPD_X06_07,coordinate x

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Name	Offset	Size	Reset Value	Description
ISP_EXPANDER_3100_EXPD_X08_09	0x0114	W	0x0C300AEA	EXPD_X08_09,coordinate x
ISP_EXPANDER_3100_EXPD_X10_11	0x0118	W	0x0EBC0D76	EXPD_X10_11,coordinate x
ISP_EXPANDER_3100_EXPD_X12_13	0x011C	W	0x0FFF0FFF	EXPD_X12_13,coordinate x
ISP_EXPANDER_3100_EXPD_X14_15	0x0120	W	0x0FFF0FFF	EXPD_X14_15,coordinate x
ISP_EXPANDER_3100_EXPD_X16_17	0x0124	W	0x0FFF0FFF	EXPD_X14_15,coordinate x
ISP_EXPANDER_3100_EXPD_X18_19	0x0128	W	0x0FFF0FFF	EXPD_X14_15,coordinate x
ISP_EXPANDER_3100_EXPD_X20_21	0x012C	W	0x0FFF0FFF	EXPD_X14_15,coordinate x
ISP_EXPANDER_3100_EXPD_X22_23	0x0130	W	0x0FFF0FFF	EXPD_X14_15,coordinate x
ISP_EXPANDER_3100_EXPD_X24_25	0x0134	W	0x0FFF0FFF	EXPD_X14_15,coordinate x
ISP_EXPANDER_3100_EXPD_X26_27	0x0138	W	0x0FFF0FFF	EXPD_X14_15,coordinate x
ISP_EXPANDER_3100_EXPD_X28_29	0x013C	W	0x0FFF0FFF	EXPD_X14_15,coordinate x
ISP_EXPANDER_3100_EXPD_X30_31	0x0140	W	0x0FFF0FFF	EXPD_X14_15,coordinate x
ISP_EXPANDER_3100_EXPD_Y0	0x0144	W	0x00000000	EXPD_Y0
ISP_EXPANDER_3100_EXPD_Y1	0x0148	W	0x00000200	EXPD_Y1
ISP_EXPANDER_3100_EXPD_Y2	0x014C	W	0x00000400	EXPD_Y2
ISP_EXPANDER_3100_EXPD_Y3	0x0150	W	0x00000800	EXPD_Y3
ISP_EXPANDER_3100_EXPD_Y4	0x0154	W	0x00001000	EXPD_Y4
ISP_EXPANDER_3100_EXPD_Y5	0x0158	W	0x00002000	EXPD_Y5
ISP_EXPANDER_3100_EXPD_Y6	0x015C	W	0x00004000	EXPD_Y6
ISP_EXPANDER_3100_EXPD_Y7	0x0160	W	0x00008000	EXPD_Y7
ISP_EXPANDER_3100_EXPD_Y8	0x0164	W	0x00010000	EXPD_Y8
ISP_EXPANDER_3100_EXPD_Y9	0x0168	W	0x00020000	EXPD_Y9
ISP_EXPANDER_3100_EXPD_Y10	0x016C	W	0x00040000	EXPD_Y10
ISP_EXPANDER_3100_EXPD_Y11	0x0170	W	0x00080000	EXPD_Y11
ISP_EXPANDER_3100_EXPD_Y12	0x0174	W	0x000FFFFF	EXPD_Y12
ISP_EXPANDER_3100_EXPD_Y13	0x0178	W	0x000FFFFF	EXPD_Y13
ISP_EXPANDER_3100_EXPD_Y14	0x017C	W	0x000FFFFF	EXPD_Y14

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Name	Offset	Size	Reset Value	Description
ISP_EXPANDER_3100_EXPD_Y15	0x0180	W	0x000FFFFF	EXPD_Y15
ISP_EXPANDER_3100_EXPD_Y16	0x0184	W	0x000FFFFF	EXPD_Y16
ISP_EXPANDER_3100_EXPD_Y17	0x0188	W	0x000FFFFF	EXPD_Y17
ISP_EXPANDER_3100_EXPD_Y18	0x018C	W	0x000FFFFF	EXPD_Y18
ISP_EXPANDER_3100_EXPD_Y19	0x0190	W	0x000FFFFF	EXPD_Y19
ISP_EXPANDER_3100_EXPD_Y20	0x0194	W	0x000FFFFF	EXPD_Y20
ISP_EXPANDER_3100_EXPD_Y21	0x0198	W	0x000FFFFF	EXPD_Y21
ISP_EXPANDER_3100_EXPD_Y22	0x019C	W	0x000FFFFF	EXPD_Y22
ISP_EXPANDER_3100_EXPD_Y23	0x01A0	W	0x000FFFFF	EXPD_Y23
ISP_EXPANDER_3100_EXPD_Y24	0x01A4	W	0x000FFFFF	EXPD_Y24
ISP_EXPANDER_3100_EXPD_Y25	0x01A8	W	0x000FFFFF	EXPD_Y25
ISP_EXPANDER_3100_EXPD_Y26	0x01AC	W	0x000FFFFF	EXPD_Y26
ISP_EXPANDER_3100_EXPD_Y27	0x01B0	W	0x000FFFFF	EXPD_Y27
ISP_EXPANDER_3100_EXPD_Y28	0x01B4	W	0x000FFFFF	EXPD_Y28
ISP_EXPANDER_3100_EXPD_Y29	0x01B8	W	0x000FFFFF	EXPD_Y29
ISP_EXPANDER_3100_EXPD_Y30	0x01BC	W	0x000FFFFF	EXPD_Y30
ISP_EXPANDER_3100_EXPD_Y31	0x01C0	W	0x000FFFFF	EXPD_Y31
ISP_EXPANDER_3100_EXPD_K0	0x01C4	W	0x00002000	EXPD_K0,slope k = slope*2^sw_expd_k_shift, slope = (yn-yn-1)/(xn-xn-1)
ISP_EXPANDER_3100_EXPD_K1	0x01C8	W	0x00003241	EXPD_K1, k = slope*2^sw_expd_k_shift
ISP_EXPANDER_3100_EXPD_K2	0x01CC	W	0x00006483	EXPD_K2, k = slope*2^sw_expd_k_shift
ISP_EXPANDER_3100_EXPD_K3	0x01D0	W	0x0000C907	EXPD_K3, k = slope*2^sw_expd_k_shift
ISP_EXPANDER_3100_EXPD_K4	0x01D4	W	0x0001920F	EXPD_K4, k = slope*2^sw_expd_k_shift
ISP_EXPANDER_3100_EXPD_K5	0x01D8	W	0x0003241F	EXPD_K5, k = slope*2^sw_expd_k_shift
ISP_EXPANDER_3100_EXPD_K6	0x01DC	W	0x0006483E	EXPD_K6, k = slope*2^sw_expd_k_shift
ISP_EXPANDER_3100_EXPD_K7	0x01E0	W	0x000C907D	EXPD_K7, k = slope*2^sw_expd_k_shift
ISP_EXPANDER_3100_EXPD_K8	0x01E4	W	0x001920FB	EXPD_K8, k = slope*2^sw_expd_k_shift

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Name	Offset	Size	Reset Value	Description
ISP_EXPANDER_3100_EXPD_K9	0x01E8	W	0x003241F6	EXPD_K9, k = slope*2^sw_expd_k_shift
ISP_EXPANDER_3100_EXPD_K10	0x01EC	W	0x006483ED	EXPD_K10, k = slope*2^sw_expd_k_shift
ISP_EXPANDER_3100_EXPD_K11	0x01F0	W	0x00CAE5BF	EXPD_K11, k = slope*2^sw_expd_k_shift
ISP_EXPANDER_3100_EXPD_K12	0x01F4	W	0x00000000	EXPD_K12, k = slope*2^sw_expd_k_shift
ISP_EXPANDER_3100_EXPD_K13	0x01F8	W	0x00000000	EXPD_K13, k = slope*2^sw_expd_k_shift
ISP_EXPANDER_3100_EXPD_K14	0x01FC	W	0x00000000	EXPD_K14, k = slope*2^sw_expd_k_shift

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

44.4.1.10 BAY3D

Name	Offset	Size	Reset Value	Description
BAY3D_2B00_BAY3D_CTRL0	0x0000	W	0x00000000	BAY3D control0
BAY3D_2B00_BAY3D_CTRL1	0x0004	W	0x00003800	BAY3D control1
BAY3D_2B00_BAY3D_CTRL2	0x0008	W	0x00000000	BAY3D control2
BAY3D_2B00_BAY3D_CTRL3	0x000C	W	0x3F3F0002	BAY3D control3
BAY3D_2B00_BAY3D_TRANS0	0x0010	W	0x08000100	BAY3D transform curve config
BAY3D_2B00_BAY3D_TRANS1	0x0014	W	0x000FFFFF	BAY3D transform curve config
BAY3D_2B00_BAY3D_PRE_SIGSCL	0x0058	W	0x00000000	BAY3D pre spnr sigma scale
BAY3D_2B00_BAY3D_PREHI_SIGOF	0x0068	W	0x00000000	BAY3D pre spnr guide wgt
BAY3D_2B00_BAY3D_CURHISPW0	0x0070	W	0x00000000	BAY3D cur spnr filter coef
BAY3D_2B00_BAY3D_CURHISPW1	0x0074	W	0x00000000	BAY3D cur spnr filter coef
BAY3D_2B00_BAY3D_IIRSX0	0x0084	W	0x00000000	BAY3D pre spnr sigma index 0 1
BAY3D_2B00_BAY3D_IIRSX2	0x0088	W	0x00000000	BAY3D pre spnr sigma index 2 3
BAY3D_2B00_BAY3D_IIRSX4	0x008C	W	0x00000000	BAY3D pre spnr sigma index 4 5
BAY3D_2B00_BAY3D_IIRSX6	0x0090	W	0x00000000	BAY3D pre spnr sigma index 6 7
BAY3D_2B00_BAY3D_IIRSX8	0x0094	W	0x00000000	BAY3D pre spnr sigma index 8 9
BAY3D_2B00_BAY3D_IIRSXA	0x0098	W	0x00000000	BAY3D pre spnr sigma index 10 11
BAY3D_2B00_BAY3D_IIRSXC	0x009C	W	0x00000000	BAY3D pre spnr sigma index 12 13

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Name	Offset	Size	Reset Value	Description
BAY3D_2B00_BAY3D_IIRSXE	0x00A0	W	0x00000000	BAY3D pre spnr sigma index 14 15
BAY3D_2B00_BAY3D_IIRSY0	0x00A4	W	0x00000000	BAY3D pre spnr sigma value 0 1
BAY3D_2B00_BAY3D_IIRSY2	0x00A8	W	0x00000000	BAY3D pre spnr sigma value 2 3
BAY3D_2B00_BAY3D_IIRSY4	0x00AC	W	0x00000000	BAY3D pre spnr sigma value 4 5
BAY3D_2B00_BAY3D_IIRSY6	0x00B0	W	0x00000000	BAY3D pre spnr sigma value 6 7
BAY3D_2B00_BAY3D_IIRSY8	0x00B4	W	0x00000000	BAY3D pre spnr sigma value 8 9
BAY3D_2B00_BAY3D_IIRSYA	0x00B8	W	0x00000000	BAY3D pre spnr sigma value 10 11
BAY3D_2B00_BAY3D_IIRSYC	0x00BC	W	0x00000000	BAY3D pre spnr sigma value 12 13
BAY3D_2B00_BAY3D_IIRSYE	0x00C0	W	0x00000000	BAY3D pre spnr sigma value 14 15
BAY3D_2B00_BAY3D_PREHI_SIGSCL	0x00C4	W	0x00000000	BAY3D prehi spnr sigma scale
BAY3D_2B00_BAY3D_PREHI_WSCL	0x00C8	W	0x00000000	BAY3D prehi spnr wgt scale
BAY3D_2B00_BAY3D_PREHIWMM	0x00CC	W	0x00000000	BAY3D prehi spnr wgt config
BAY3D_2B00_BAY3D_PREHISIGOF	0x00D4	W	0x00000000	BAY3D prehi spnr wgt config
BAY3D_2B00_BAY3D_PREHISIGSCL	0x00D8	W	0x00000000	BAY3D pre spnr sigma scale
BAY3D_2B00_BAY3D_PREHISPW0	0x00DC	W	0x00000000	BAY3D prehi spnr filter coef
BAY3D_2B00_BAY3D_PREHISPW1	0x00E0	W	0x00000000	BAY3D prehi spnr filter coef
BAY3D_2B00_BAY3D_PRELOSIGCSL	0x00E4	W	0x00000000	BAY3D prelo spnr sigma scale
BAY3D_2B00_BAY3D_PRELOSIGOF	0x00E8	W	0x00000000	BAY3D prelo spnr wgt scale
BAY3D_2B00_BAY3D_PREHI_NRCT	0x00F0	W	0x00000000	BAY3D prehi spnr noise ctrl
BAY3D_2B00_BAY3D_TNRSX0	0x0100	W	0x00000000	BAY3D sigma index 0 1
BAY3D_2B00_BAY3D_TNRSX2	0x0104	W	0x00000000	BAY3D sigma index 2 3
BAY3D_2B00_BAY3D_TNRSX4	0x0108	W	0x00000000	BAY3D sigma index 4 5
BAY3D_2B00_BAY3D_TNRSX6	0x010C	W	0x00000000	BAY3D sigma index 6 7
BAY3D_2B00_BAY3D_TNRSX8	0x0110	W	0x00000000	BAY3D sigma index 8 9
BAY3D_2B00_BAY3D_TNRSXA	0x0114	W	0x00000000	BAY3D sigma index 10 11
BAY3D_2B00_BAY3D_TNRSXC	0x0118	W	0x00000000	BAY3D sigma index 12 13
BAY3D_2B00_BAY3D_TNRSXE	0x011C	W	0x00000000	BAY3D sigma index 14 15

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Name	Offset	Size	Reset Value	Description
BAY3D_2B00_BAY3D_TNRSX10	0x0120	W	0x00000000	BAY3D sigma index 16 17
BAY3D_2B00_BAY3D_TNRSX12	0x0124	W	0x00000000	BAY3D sigma index 18 19
BAY3D_2B00_BAY3D_TNRSY0	0x0128	W	0x00000000	BAY3D sigma value 0 1
BAY3D_2B00_BAY3D_TNRSY2	0x012C	W	0x00000000	BAY3D sigma value 2 3
BAY3D_2B00_BAY3D_TNRSY4	0x0130	W	0x00000000	BAY3D sigma value 4 5
BAY3D_2B00_BAY3D_TNRSY6	0x0134	W	0x00000000	BAY3D sigma value 6 7
BAY3D_2B00_BAY3D_TNRSY8	0x0138	W	0x00000000	BAY3D sigma value 8 9
BAY3D_2B00_BAY3D_TNRSYA	0x013C	W	0x00000000	BAY3D sigma value 10 11
BAY3D_2B00_BAY3D_TNRSYC	0x0140	W	0x00000000	BAY3D sigma value 12 13
BAY3D_2B00_BAY3D_TNRSYE	0x0144	W	0x00000000	BAY3D sigma value 14 15
BAY3D_2B00_BAY3D_TNRSY10	0x0148	W	0x00000000	BAY3D sigma value 16 17
BAY3D_2B00_BAY3D_TNRSY12	0x014C	W	0x00000000	BAY3D sigma value 18 19
BAY3D_2B00_BAY3D_HIWD0	0x0150	W	0x00000000	BAY3D lpf hi coef
BAY3D_2B00_BAY3D_HIWD3	0x0154	W	0x00000000	BAY3D lpf hi coef
BAY3D_2B00_BAY3D_HIWD6	0x0158	W	0x00000000	BAY3D lpf hi coef
BAY3D_2B00_BAY3D_LOWD0	0x015C	W	0x00000000	BAY3D lpf lo coef
BAY3D_2B00_BAY3D_LOWD3	0x0160	W	0x00000000	BAY3D lpf lo coef
BAY3D_2B00_BAY3D_LOWD6	0x0164	W	0x00000000	BAY3D lpf lo coef
BAY3D_2B00_BAY3D_GF3	0x0168	W	0x00000000	BAY3D sigma index filter coef
BAY3D_2B00_BAY3D_GF4	0x016C	W	0x00000000	BAY3D sigma index filter coef
BAY3D_2B00_BAY3D_VIIR	0x0170	W	0x00000000	BAY3D vfilter config
BAY3D_2B00_BAY3D_LFSCL	0x0174	W	0x00000000	BAY3D lowgt calc
BAY3D_2B00_BAY3D_LFSCLTH	0x0178	W	0x00000000	BAY3D lowgt calc
BAY3D_2B00_BAY3D_DSWGTSCL	0x017C	W	0x00000000	BAY3D lodiff calc
BAY3D_2B00_BAY3D_WGTLASTSCL	0x0180	W	0x00000000	BAY3D prewgt calc
BAY3D_2B00_BAY3D_WGTSCL0	0x0184	W	0x00000000	BAY3D mode0 lowgt scale
BAY3D_2B00_BAY3D_WGTSCL1	0x0188	W	0x00000000	BAY3D mode1 lowgt scale
BAY3D_2B00_BAY3D_WGTSCL2	0x018C	W	0x00000000	BAY3D mode1 wgt scale

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Name	Offset	Size	Reset Value	Description
BAY3D_2B00_BAY3D_WGTOFF	0x0190	W	0x00000000	BAY3D mode0 lowgt offset
BAY3D_2B00_BAY3D_WGT1OFF	0x0194	W	0x00000000	BAY3D mode1 lowgt offset
BAY3D_2B00_BAY3D_SIGORG	0x0198	W	0x00000000	BAY3D sigma square
BAY3D_2B00_BAY3D_WGTLO_L	0x019C	W	0x00000000	BAY3D lowgt clip limit
BAY3D_2B00_BAY3D_WGTLO_H	0x01A0	W	0x00000000	BAY3D lowgt clip limit
BAY3D_2B00_BAY3D_STH_SCL	0x01A4	W	0x00000000	BAY3D softthresh scale
BAY3D_2B00_BAY3D_STH_LIMIT	0x01A8	W	0x00000000	BAY3D softthresh limit
BAY3D_2B00_BAY3D_HIKEEP	0x01AC	W	0x00000000	BAY3D hiwgt limit
BAY3D_2B00_BAY3D_PIXMAX	0x01B0	W	0x00000000	BAY3D pix max
BAY3D_2B00_BAY3D_SIGNUMTH	0x01B4	W	0x00000000	BAY3D sigma thresh
BAY3D_2B00_BAY3D_MONR	0x01B8	W	0x00000000	BAY3D noise balance
BAY3D_2B00_BAY3D_SIGSCL	0x01BC	W	0x00000000	BAY3D sigma scale
BAY3D_2B00_BAY3D_DSOFF	0x01D0	W	0x00000000	BAY3D lowgt offset
BAY3D_2B00_BAY3D_DSSCL	0x01D4	W	0x00000000	BAY3D lowgt scale
BAY3D_2B00_BAY3D_ME0	0x01D8	W	0x00000000	BAY3D me cost config
BAY3D_2B00_BAY3D_ME1	0x01DC	W	0x00000000	BAY3D me cost config
BAY3D_2B00_BAY3D_ME2	0x01E0	W	0x00000000	BAY3D me cost config
BAY3D_2B00_BAY3D_WGTMAX	0x01E4	W	0x00000000	BAY3D lowgt motion limit
BAY3D_2B00_BAY3D_WGT1MAX	0x01E8	W	0x00000000	BAY3D mode1 wgt limit
BAY3D_2B00_BAY3D_WGTM0	0x01EC	W	0x00000000	BAY3D mode0 wgt config
BAY3D_2B00_BAY3D_LOCOEF0	0x01F0	W	0x00000000	BAY3D lowgt config
BAY3D_2B00_BAY3D_LOCOEF1	0x01F4	W	0x00000000	BAY3D lowgt config
BAY3D_2B00_BAY3D_DPC0	0x01F8	W	0x00000000	BAY3D spnr dpcc
BAY3D_2B00_BAY3D_DPC1	0x01FC	W	0x00000000	BAY3D spnr dpcc
BAY3D_2B00_BAY3D_PRELOWGT	0x020C	W	0x00000000	BAY3D spnr dpcc
BAY3D_2B00_BAY3D_MIDBIG0	0x0280	W	0x00000000	BAY3D md large config
BAY3D_2B00_BAY3D_MIDBIG1	0x0284	W	0x00000000	BAY3D md large config
BAY3D_2B00_BAY3D_MIDBIG2	0x0288	W	0x00000000	BAY3D md large config

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Name	Offset	Size	Reset Value	Description
BAY3D_2B00_BAY3D_MONROFF	0x028C	W	0x00000000	BAY3D noise balance offset
BAY3D_2B00_BAY3D_TNRSUM	0x02D4	W	0x00000000	BAY3D sigma number
BAY3D_2B00_BAY3D_TNRYO0	0x02D8	W	0x00000000	BAY3D sigma statistics y out
BAY3D_2B00_BAY3D_TNRYO1	0x02DC	W	0x00000000	BAY3D sigma statistics y out
BAY3D_2B00_BAY3D_TNRYO2	0x02E0	W	0x00000000	BAY3D sigma statistics y out
BAY3D_2B00_BAY3D_TNRYO3	0x02E4	W	0x00000000	BAY3D sigma statistics y out
BAY3D_2B00_BAY3D_TNRYO4	0x02E8	W	0x00000000	BAY3D sigma statistics y out
BAY3D_2B00_BAY3D_TNRYO5	0x02EC	W	0x00000000	BAY3D sigma statistics y out
BAY3D_2B00_BAY3D_TNRYO6	0x02F0	W	0x00000000	BAY3D sigma statistics y out
BAY3D_2B00_BAY3D_TNRYO7	0x02F4	W	0x00000000	BAY3D sigma statistics y out
BAY3D_2B00_BAY3D_TNRYO8	0x02F8	W	0x00000000	BAY3D sigma statistics y out
BAY3D_2B00_BAY3D_TNRYO9	0x02FC	W	0x00000000	BAY3D sigma statistics y out

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

44.4.1.11 CAC

Name	Offset	Size	Reset Value	Description
ISP_CAC_2600_CTRL	0x0000	W	0x00000000	Cac Control
ISP_CAC_2600_PSF_PARA	0x0004	W	0x00000002	Point Spread Function(PSF) Parameter
ISP_CAC_2600_HIGH_DIRECT	0x0008	W	0x00000400	High Direct
ISP_CAC_2600_OVER_EXPO0	0x000C	W	0x00007D38	Overexposure Parameter0
ISP_CAC_2600_OVER_EXPO1	0x0010	W	0x0000FA70	Overexposure Parameter1
ISP_CAC_2600_FLAT	0x0014	W	0x00000010	Flat Parameter
ISP_CAC_2600_GAUSS_COEFF	0x0018	W	0x00000012	Chroma Low Filter and Weight Color Gauss Coefficient
ISP_CAC_2600_RATIO	0x001C	W	0x05000100	Search Range Ratio And Residual Chroma Ratio
ISP_CAC_2600_WGT_COLOR_B	0x0020	W	0x00066666	Weight Color of Blue
ISP_CAC_2600_WGT_COLOR_R	0x0024	W	0x00000000	Weight Color of Red
ISP_CAC_2600_WGT_COLOR_SLOPE_B	0x0028	W	0x00001400	Blue Weight Color Slope
ISP_CAC_2600_WGT_COLOR_SLOPE_R	0x002C	W	0x00002800	Red Weight Color Slope
ISP_CAC_2600_WGT_COLOR_LUMA0	0x0030	W	0x0000642D	Weight Color Luminance Parameter 0

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Name	Offset	Size	Reset Value	Description
ISP_CAC_2600_WGT_COLOR_LUMA1	0x0034	W	0x000000A4	Weight Color Luminance Parameter 1
ISP_CAC_2600_WGT_OVER_EXPO0	0x0038	W	0x0000C85A	Weight Overexposure Parameter 0
ISP_CAC_2600_WGT_OVER_EXPO1	0x003C	W	0x000000A4	Weight Overexposure Parameter 1
ISP_CAC_2600_WGT_CONTRAST0	0x0040	W	0x0009999A	Weight Contrast Parameter 0
ISP_CAC_2600_WGT_CONTRAST1	0x0044	W	0x00000D55	Weight Contrast Parameter 1
ISP_CAC_2600_WGT_CONTRAST2	0x0048	W	0x00000000	Weight Contrast Parameter 2
ISP_CAC_2600_WGT_DARK_AREA0	0x004C	W	0x0000C85A	Weight Dark Area Parameter0
ISP_CAC_2600_WGT_DARK_AREA1	0x0050	W	0x000000A4	Weight Dark Area Parameter1
ISP_CAC_2600_PSF_B0	0x0054	W	0x08080808	PSF Kernel 0 of Blue
ISP_CAC_2600_PSF_B1	0x0058	W	0x08080808	PSF Kernel 1 of Blue
ISP_CAC_2600_PSF_B2	0x005C	W	0x00080808	PSF Kernel 2 of Blue
ISP_CAC_2600_PSF_R0	0x0060	W	0x08080808	PSF Kernel 0 of Red
ISP_CAC_2600_PSF_R1	0x0064	W	0x08080808	PSF Kernel 1 of Red
ISP_CAC_2600_PSF_R2	0x0068	W	0x00080808	PSF Kernel 2 of Red
ISP_CAC_2600_RO_CNT	0x00F8	W	0x00000000	Cac Counter Read
ISP_CAC_2600_DEBUF	0x00FC	W	0x00000000	Cac Debug Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

44.4.1.12 LSC

Name	Offset	Size	Reset Value	Description
ISP_LSC_2200_CTRL	0x0000	W	0x00000000	Lens shade control
ISP_LSC_2200_TABLE_RAM_ADDR_R	0x0004	W	0x00000000	Table RAM Address for red component
ISP_LSC_2200_TABLE_RAM_ADDR_GR	0x0008	W	0x00000000	Table RAM Address for green (red) component
ISP_LSC_2200_TABLE_RAM_ADDR_B	0x000C	W	0x00000000	Table RAM Address for blue component
ISP_LSC_2200_TABLE_RAM_ADDR_GB	0x0010	W	0x00000000	Table RAM Address for green (blue) component
ISP_LSC_2200_TABLE_DATA_R	0x0014	W	0x00000000	Sample table red
ISP_LSC_2200_TABLE_DATA_GR	0x0018	W	0x00000000	Sample table green (red)
ISP_LSC_2200_TABLE_DATA_B	0x001C	W	0x00000000	Sample table blue
ISP_LSC_2200_TABLE_DATA_GB	0x0020	W	0x00000000	Sample table green (blue)
ISP_LSC_2200_FACTOR_X_01	0x0024	W	0x00000000	Gradient table x
ISP_LSC_2200_FACTOR_X_23	0x0028	W	0x00000000	Gradient table x
ISP_LSC_2200_FACTOR_X_45	0x002C	W	0x00000000	Gradient table x

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Name	Offset	Size	Reset Value	Description
ISP_LSC_2200_FACTOR_X_67	0x0030	W	0x00000000	Gradient table x
ISP_LSC_2200_FACTOR_Y_01	0x0034	W	0x00000000	Gradient table y
ISP_LSC_2200_FACTOR_Y_23	0x0038	W	0x00000000	Gradient table y
ISP_LSC_2200_FACTOR_Y_45	0x003C	W	0x00000000	Gradient table y
ISP_LSC_2200_FACTOR_Y_67	0x0040	W	0x00000000	Gradient table y
ISP_LSC_2200_SIZE_X_01	0x0044	W	0x00000000	Size table
ISP_LSC_2200_SIZE_X_23	0x0048	W	0x00000000	Size table
ISP_LSC_2200_SIZE_X_45	0x004C	W	0x00000000	Size table
ISP_LSC_2200_SIZE_X_67	0x0050	W	0x00000000	Size table
ISP_LSC_2200_SIZE_Y_01	0x0054	W	0x00000000	Size table
ISP_LSC_2200_SIZE_Y_23	0x0058	W	0x00000000	Size table
ISP_LSC_2200_SIZE_Y_45	0x005C	W	0x00000000	Size table
ISP_LSC_2200_SIZE_Y_67	0x0060	W	0x00000000	Size table
ISP_LSC_2200_TABLE_SEL	0x0064	W	0x00000000	Lens shade table set selection
ISP_LSC_2200_ISP_LSC_STATUS	0x0068	W	0x00000000	Status of lens shade
ISP_LSC_2200_FACTOR_X_89	0x0070	W	0x00000000	Gradient table x
ISP_LSC_2200_FACTOR_X_AB	0x0074	W	0x00000000	Gradient table x
ISP_LSC_2200_FACTOR_X_CD	0x0078	W	0x00000000	Gradient table x
ISP_LSC_2200_FACTOR_X_EF	0x007C	W	0x00000000	Gradient table x
ISP_LSC_2200_FACTOR_Y_89	0x0080	W	0x00000000	Gradient table y
ISP_LSC_2200_FACTOR_Y_AB	0x0084	W	0x00000000	Gradient table y
ISP_LSC_2200_FACTOR_Y_CD	0x0088	W	0x00000000	Gradient table y
ISP_LSC_2200_FACTOR_Y_EF	0x008C	W	0x00000000	Gradient table y
ISP_LSC_2200_SIZE_X_89	0x0090	W	0x00000000	Size table
ISP_LSC_2200_SIZE_X_AB	0x0094	W	0x00000000	Size table
ISP_LSC_2200_SIZE_X_CD	0x0098	W	0x00000000	Size table
ISP_LSC_2200_SIZE_X_EF	0x009C	W	0x00000000	Size table

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Name	Offset	Size	Reset Value	Description
ISP_LSC_2200_SIZE_Y_89	0x00A0	W	0x00000000	Size table
ISP_LSC_2200_SIZE_Y_AB	0x00A4	W	0x00000000	Size table
ISP_LSC_2200_SIZE_Y_CD	0x00A8	W	0x00000000	Size table
ISP_LSC_2200_SIZE_Y_EF	0x00AC	W	0x00000000	Size table

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

44.4.1.13 HDRDRC

Name	Offset	Size	Reset Value	Description
ISP_RGBxDRC_3900_CTRL0	0x0000	W	0x00000000	Global hdr-control-0
ISP_RGBxDRC_3900_CTRL1	0x0004	W	0x83904100	Drc control1
ISP_RGBxDRC_3900_LPRATIO	0x0008	W	0x40000000	lp-ratio
ISP_RGBxDRC_3900_BILAT0	0x000C	W	0x60807700	Bilateral configuration-0
ISP_RGBxDRC_3900_BILAT1	0x0010	W	0x00000008	Bilateral configuration-1
ISP_RGBxDRC_3900_BILAT2	0x0014	W	0x00100400	Bilateral configuration-2
ISP_RGBxDRC_3900_BILAT3	0x0018	W	0x01000100	Bilateral configuration-3
ISP_RGBxDRC_3900_BILAT4	0x001C	W	0x00770010	Bilateral configuration-4
ISP_RGBxDRC_3900_GAIN_Y0	0x0020	W	0x04000400	Curve gain Y0~Y16
ISP_RGBxDRC_3900_GAIN_Y1	0x0024	W	0x04000400	Curve gain Y0~Y16
ISP_RGBxDRC_3900_GAIN_Y2	0x0028	W	0x04000400	Curve gain Y0~Y16
ISP_RGBxDRC_3900_GAIN_Y3	0x002C	W	0x04000400	Curve gain Y0~Y16
ISP_RGBxDRC_3900_GAIN_Y4	0x0030	W	0x04000400	Curve gain Y0~Y16
ISP_RGBxDRC_3900_GAIN_Y5	0x0034	W	0x04000400	Curve gain Y0~Y16
ISP_RGBxDRC_3900_GAIN_Y6	0x0038	W	0x04000400	Curve gain Y0~Y16
ISP_RGBxDRC_3900_GAIN_Y7	0x003C	W	0x04000400	Curve gain Y0~Y16
ISP_RGBxDRC_3900_GAIN_Y8	0x0040	W	0x00000400	Curve gain Y0~Y16
ISP_RGBxDRC_3900_COMPRES_Y0	0x0044	W	0x00470000	Curve compress Y0~Y16
ISP_RGBxDRC_3900_COMPRES_Y1	0x0048	W	0x00CB008B	Curve compress Y0~Y16
ISP_RGBxDRC_3900_COMPRES_Y2	0x004C	W	0x01400107	Curve compress Y0~Y16

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Name	Offset	Size	Reset Value	Description
ISP_RGBxDRC_3900_COMPRES_Y3	0x0050	W	0x01AA0176	Curve compress Y0~Y16
ISP_RGBxDRC_3900_COMPRES_Y4	0x0054	W	0x023601DB	Curve compress Y0~Y16
ISP_RGBxDRC_3900_COMPRES_Y5	0x0058	W	0x02D40289	Curve compress Y0~Y16
ISP_RGBxDRC_3900_COMPRES_Y6	0x005C	W	0x035A031A	Curve compress Y0~Y16
ISP_RGBxDRC_3900_COMPRES_Y7	0x0060	W	0x03CC0396	Curve compress Y0~Y16
ISP_RGBxDRC_3900_COMPRES_Y8	0x0064	W	0x00000400	Curve compress Y0~Y16
ISP_RGBxDRC_3900_SCALE_Y0	0x0068	W	0x00020000	Curve scale Y0~Y16
ISP_RGBxDRC_3900_SCALE_Y1	0x006C	W	0x004C0014	Curve scale Y0~Y16
ISP_RGBxDRC_3900_SCALE_Y2	0x0070	W	0x017D00C1	Curve scale Y0~Y16
ISP_RGBxDRC_3900_SCALE_Y3	0x0074	W	0x03040277	Curve scale Y0~Y16
ISP_RGBxDRC_3900_SCALE_Y4	0x0078	W	0x042A0397	Curve scale Y0~Y16
ISP_RGBxDRC_3900_SCALE_Y5	0x007C	W	0x05C704BB	Curve scale Y0~Y16
ISP_RGBxDRC_3900_SCALE_Y6	0x0080	W	0x074706A4	Curve scale Y0~Y16
ISP_RGBxDRC_3900_SCALE_Y7	0x0084	W	0x07E807B0	Curve scale Y0~Y16
ISP_RGBxDRC_3900_SCALE_Y8	0x0088	W	0x00000800	Curve scale Y0~Y16
ISP_RGBxDRC_3900_IIRWG_GAIN	0x008C	W	0x00000000	Drc_min_ogain, drc_iir_weight
ISP_RGBxDRC_3900_SFTHD_Y0	0x0090	W	0x00F600FB	Curve_Luma soft threshold Y0~Y16
ISP_RGBxDRC_3900_SFTHD_Y1	0x0094	W	0x00E300EF	Curve_Luma soft threshold Y0~Y16
ISP_RGBxDRC_3900_SFTHD_Y2	0x0098	W	0x00B700D0	Curve_Luma soft threshold Y0~Y16
ISP_RGBxDRC_3900_SFTHD_Y3	0x009C	W	0x0082009B	Curve_Luma soft threshold Y0~Y16
ISP_RGBxDRC_3900_SFTHD_Y4	0x00A0	W	0x0060006D	Curve_Luma soft threshold Y0~Y16
ISP_RGBxDRC_3900_SFTHD_Y5	0x00A4	W	0x00530058	Curve_Luma soft threshold Y0~Y16
ISP_RGBxDRC_3900_SFTHD_Y6	0x00A8	W	0x004F0050	Curve_Luma soft threshold Y0~Y16
ISP_RGBxDRC_3900_SFTHD_Y7	0x00AC	W	0x004D004E	Curve_Luma soft threshold Y0~Y16
ISP_RGBxDRC_3900_SFTHD_Y8	0x00B0	W	0x0000004D	Curve_Luma soft threshold Y0~Y16
ISP_RGBxDRC_3900_LUMA_MIX	0x00B4	W	0x00000080	Luma mix weight config

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

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44.4.1.14 GIC

Name	Offset	Size	Reset Value	Description
ISP_GIC_2F00_CTRL	0x0000	W	0x02000018	Control register
ISP_GIC_2F00_MEDFLT_PARA	0x0004	W	0x00800062	Median filter para for Y component
ISP_GIC_2F00_MEDFLTUV_PARA	0x0008	W	0x00800062	Median filter parameter for UV component
ISP_GIC_2F00_NOISE_SCALE	0x000C	W	0x00000080	Noise curve scale
ISP_GIC_2F00_BILAT_PARA1	0x0010	W	0x006A00EC	Bilateral filter paramter1
ISP_GIC_2F00_BILAT_PARA2	0x0014	W	0x00000080	Bilateral filter paramter2
ISP_GIC_2F00_DISWGT_COEFF	0x0018	W	0x000A1018	Bilateral filter distance weight coefficient
ISP_GIC_2F00_SIGMA_Y0	0x0020	W	0x000D000B	Y0 group of sigma table
ISP_GIC_2F00_SIGMA_Y1	0x0024	W	0x0010000E	Y1 group of sigma table
ISP_GIC_2F00_SIGMA_Y2	0x0028	W	0x00120011	Y2 group of sigma table
ISP_GIC_2F00_SIGMA_Y3	0x002C	W	0x00140014	Y3 group of sigma table
ISP_GIC_2F00_SIGMA_Y4	0x0030	W	0x00160015	Y4 group of sigma table
ISP_GIC_2F00_SIGMA_Y5	0x0034	W	0x00180017	Y5 group of sigma table
ISP_GIC_2F00_SIGMA_Y6	0x0038	W	0x00180018	Y6 group of sigma table
ISP_GIC_2F00_SIGMA_Y7	0x003C	W	0x00190018	Y7 group of sigma table
ISP_GIC_2F00_SIGMA_Y8	0x0040	W	0x00000019	Y8 group of sigma table
ISP_GIC_2F00_LUMA_DX	0x0044	W	0x07887766	Bilateral filter threshold-curve luma delta-x (get log2) of axis-x.Curve start point: axis-x = 0, axis >= 0
ISP_GIC_2F00_THRED_Y0	0x0050	W	0x000D000B	Y0 group of maximum threshold table
ISP_GIC_2F00_THRED_Y1	0x0054	W	0x0011000E	Y1 group of maximum threshold table
ISP_GIC_2F00_THRED_Y2	0x0058	W	0x00170014	Y2 group of maximum threshold table
ISP_GIC_2F00_THRED_Y3	0x005C	W	0x00190018	Y3 group of maximum threshold table
ISP_GIC_2F00_MIN_THRED_Y0	0x0060	W	0x00000000	Y0 group of minimum threshold table
ISP_GIC_2F00_MIN_THRED_Y1	0x0064	W	0x00000000	Y1 group of maximum threshold table
ISP_GIC_2F00_MIN_THRED_Y2	0x0068	W	0x00000000	Y2 group of minimum threshold table
ISP_GIC_2F00_MIN_THRED_Y3	0x006C	W	0x00000000	Y3 group of minimum threshold table
ISP_GIC_2F00_THRED_SCALE	0x0070	W	0x00000080	Threshold scale
ISP_GIC_2F00_LOFLTGR_COEFF	0x0074	W	0x04040404	Low pass filtering coefficient of Gr channel.
ISP_GIC_2F00_LOFLTGB_COEFF	0x0078	W	0x00000606	Low pass filtering coefficient of Gb channel.
ISP_GIC_2F00_SUM_LOFLT_INV	0x007C	W	0x000000AB	The inverse of the threshold low-pass filter coefficient sum
ISP_GIC_2F00_LOFLTTHRED_COEFF	0x0080	W	0x00000804	Low pass filtering coefficient.

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Name	Offset	Size	Reset Value	Description
ISP_GIC_2F00_GAIN	0x0090	W	0x00800010	Low pass filtering coefficient of Gb channel.
ISP_GIC_2F00_GAIN_SLOPE	0x0094	W	0x00100000	Gain linearized slope
ISP_GIC_2F00_GAIN_THRED	0x0098	W	0x03F30000	Gain linearized threshold

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

44.4.1.15 DEBAYER

Name	Offset	Size	Reset Value	Description
ISP_DEBAYER_2500_CONTROL	0x0000	W	0x00000110	DEBAYER CONTROL
ISP_DEBAYER_2500_LUMA_DX	0x0004	W	0x09AA9988	LUMX DX REGISTER
ISP_DEBAYER_2500_G_INTERP	0x0010	W	0x040D6381	G INTERPOLATION REGISTER
ISP_DEBAYER_2500_G_INTERP_FILTER1	0x0014	W	0x041C021E	THIS FILTER IS FOR GETTING THE EDGE OF LOW FREQUENCY
ISP_DEBAYER_2500_G_INTERP_FILTER2	0x0018	W	0x041E021F	THIS FILTER IS FOR GETTING THE DETAIL OF HIGH FREQUENCY
ISP_DEBAYER_2500_G_INTERP_OFFSET_ALPHA	0x001C	W	0x00400004	G INTERPOLATION OFFSET REGISTER
ISP_DEBAYER_2500_G_INTERP_DRCT_OFFSET0	0x0020	W	0x00100010	G INTERPOLATION DRCT OFFSET REGISTER
ISP_DEBAYER_2500_G_INTERP_DRCT_OFFSET1	0x0024	W	0x00100010	G INTERPOLATION DRCT OFFSET REGISTER
ISP_DEBAYER_2500_G_INTERP_DRCT_OFFSET2	0x0028	W	0x00100010	G INTERPOLATION DRCT OFFSET REGISTER
ISP_DEBAYER_2500_G_INTERP_DRCT_OFFSET3	0x002C	W	0x00100010	G INTERPOLATION DRCT OFFSET REGISTER
ISP_DEBAYER_2500_G_FILTER_MODE_OFFSET	0x0050	W	0x00014000	G FILTER REGISTER
ISP_DEBAYER_2500_G_FILTER_FILTER	0x0054	W	0x00081020	G FILTER FILTER REGISTER
ISP_DEBAYER_2500_G_FILTER_VSIGMA0	0x0058	W	0x08000800	G FILTER VSIGMA REGISTER
ISP_DEBAYER_2500_G_FILTER_VSIGMA1	0x005C	W	0x02000400	G FILTER VSIGMA REGISTER
ISP_DEBAYER_2500_G_FILTER_VSIGMA2	0x0060	W	0x00CD0155	G FILTER VSIGMA REGISTER
ISP_DEBAYER_2500_G_FILTER_VSIGMA3	0x0064	W	0x00800092	G FILTER VSIGMA REGISTER
ISP_DEBAYER_2500_C_FILTER_GUIDE_GAUS	0x0070	W	0x00102040	C FILTER GUIDE GAUS REGISTER
ISP_DEBAYER_2500_C_FILTER_CE_GAUS	0x0074	W	0x00102040	C FILTER CE GAUS REGISTER
ISP_DEBAYER_2500_C_FILTER_ALPHA_GAUS	0x0078	W	0x00102040	C FILTER ALPHA GAUS REGISTER
ISP_DEBAYER_2500_C_FILTER_LOG_OFFSET	0x007C	W	0x80010080	C FILTER LOG OFFSET REGISTER
ISP_DEBAYER_2500_C_FILTER_ALPHA	0x0080	W	0x00400000	C FILTER ALPHA REGISTER

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Name	Offset	Size	Reset Value	Description
ISP_DEBAYER_2500_C_FILTER_EDGE	0x0084	W	0x00400000	C FILTER EDGE REGISTER
ISP_DEBAYER_2500_C_FILTER_IIR_0	0x0088	W	0x005A08D8	C FILTER IIR REGISTER 0
ISP_DEBAYER_2500_C_FILTER_IIR_1	0x008C	W	0x0000023A	C FILTER IIR REGISTER 1

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

44.4.1.16 CCM

Name	Offset	Size	Reset Value	Description
ISP_CCM_0700_CTRL	0x0000	W	0x00000000	ISP CCM Enable
ISP_CCM_0700_COEFF0_R	0x0004	W	0x07B70065	CCM matrix R coefficient 0 & 1
ISP_CCM_0700_COEFF1_R	0x0008	W	0x000007E4	CCM matrix R coefficient 2 & offset
ISP_CCM_0700_COEFF0_G	0x000C	W	0x005807D9	CCM matrix G coefficient 0 & 1
ISP_CCM_0700_COEFF1_G	0x0010	W	0x000007CF	CCM matrix G coefficient 2 & offset
ISP_CCM_0700_COEFF0_B	0x0014	W	0x07B70002	CCM matrix B coefficient 0&1
ISP_CCM_0700_COEFF1_B	0x0018	W	0x00000046	CCM matrix B coefficient 2 & offset
ISP_CCM_0700_COEFF0_Y	0x001C	W	0x004B0026	The R&G coefficient of RGB2Y calculation
ISP_CCM_0700_COEFF1_Y	0x0020	W	0x0000000F	The B coefficient of RGB2Y calculation
ISP_CCM_0700_ALP_Y0	0x0024	W	0x04000400	CCM curve definition y0 & y1
ISP_CCM_0700_ALP_Y1	0x0028	W	0x04000400	CCM curve definition y2 & y3
ISP_CCM_0700_ALP_Y2	0x002C	W	0x04000400	CCM curve definition y4 & y5
ISP_CCM_0700_ALP_Y3	0x0030	W	0x04000400	CCM curve definition y6 & y7
ISP_CCM_0700_ALP_Y4	0x0034	W	0x04000400	CCM curve definition y8 & y9
ISP_CCM_0700_ALP_Y5	0x0038	W	0x04000400	CCM curve definition y10 & y11
ISP_CCM_0700_ALP_Y6	0x003C	W	0x04000400	CCM curve definition y12 & y13
ISP_CCM_0700_ALP_Y7	0x0040	W	0x04000400	CCM curve definition y14 & y15
ISP_CCM_0700_ALP_Y8	0x0044	W	0x00000400	CCM curve definition y16
ISP_CCM_0700_BOUND_BIT	0x0048	W	0x0000000A	Curve inflection point, the value is 2^bound_bit.
ISP_CCM_0700_ENHANCE0	0x004C	W	0x00000000	CCM color enhance0
ISP_CCM_0700_ENHANCE1	0x0050	W	0x00000000	CCM color enhance1
ISP_CCM_0700_HF_THD	0x0054	W	0x0500F033	CCM High Frequency Threshold
ISP_CCM_0700_HF_FACTOR0	0x0058	W	0x03E00400	CCM High Frequency Factor Curve0
ISP_CCM_0700_HF_FACTOR1	0x005C	W	0x03A003C0	CCM High Frequency Factor Curve1
ISP_CCM_0700_HF_FACTOR2	0x0060	W	0x03600380	CCM High Frequency Factor Curve2
ISP_CCM_0700_HF_FACTOR3	0x0064	W	0x03200340	CCM High Frequency Factor Curve3

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Name	Offset	Size	Reset Value	Description
ISP_CCM_0700_HF_FACTOR4	0x0068	W	0x02E00300	CCM High Frequency Factor Curve4
ISP_CCM_0700_HF_FACTOR5	0x006C	W	0x02A002C0	CCM High Frequency Factor Curve5
ISP_CCM_0700_HF_FACTOR6	0x0070	W	0x02600280	CCM High Frequency Factor Curve6
ISP_CCM_0700_HF_FACTOR7	0x0074	W	0x02200240	CCM High Frequency Factor Curve7
ISP_CCM_0700_HF_FACTOR8	0x0078	W	0x00000200	CCM High Frequency Factor Curve8

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

44.4.1.17 GAMMA_OUT

Name	Offset	Size	Reset Value	Description
ISP_GAMMA_OUT_0900_CTRL	0x0000	W	0x00000000	Global control register
ISP_GAMMA_OUT_0900_OFFSET	0x0004	W	0x00000000	Offset configuration register
ISP_GAMMA_OUT_0900_Y0	0x0010	W	0x00010000	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y1	0x0014	W	0x00030002	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y2	0x0018	W	0x00050004	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y3	0x001C	W	0x00070006	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y4	0x0020	W	0x000A0008	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y5	0x0024	W	0x000E000C	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y6	0x0028	W	0x00140010	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y7	0x002C	W	0x001C0018	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y8	0x0030	W	0x00280020	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y9	0x0034	W	0x00380030	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y10	0x0038	W	0x00500040	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y11	0x003C	W	0x00700060	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y12	0x0040	W	0x00A00080	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y13	0x0044	W	0x00E000C0	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y14	0x0048	W	0x01400100	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y15	0x004C	W	0x01C00180	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y16	0x0050	W	0x02800200	Y value of gamma_out curve configuration register

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Name	Offset	Size	Reset Value	Description
ISP_GAMMA_OUT_0900_Y17	0x0054	W	0x03800300	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y18	0x0058	W	0x05000400	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y19	0x005C	W	0x07000600	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y20	0x0060	W	0x0A000800	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y21	0x0064	W	0x0E000C00	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y22	0x0068	W	0x0FFF0FFF	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y23	0x006C	W	0x0FFF0FFF	Y value of gamma_out curve configuration register
ISP_GAMMA_OUT_0900_Y24	0x0070	W	0x00000FFF	Y value of gamma_out curve configuration register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

44.4.1.18 HIST

Name	Offset	Size	Reset Value	Description
ISP_HIST_3C00_CTRL	0x0000	W	0x00000001	Hist Control
ISP_HIST_3C00_HF_STAT	0x0004	W	0x000A0908	Hist High Filter Statistics
ISP_HIST_3C00_BLOCK_SIZE	0x0008	W	0x00400040	Hist Block Size
ISP_HIST_3C00_THUMB_SIZE	0x000C	W	0x00000808	Hist Thumb Size
ISP_HIST_3C00_HIST_MAP0	0x0010	W	0x00330000	Hist Map 0
ISP_HIST_3C00_HIST_MAP1	0x0014	W	0x00000080	Hist Map 1
ISP_HIST_3C00_IIR	0x0018	W	0x00080001	IIR Filter
ISP_HIST_3C00_POS_ALPHA0	0x001C	W	0x20002020	Posedge Alpha 0
ISP_HIST_3C00_POS_ALPHA1	0x0020	W	0x20202020	Posedge Alpha 1
ISP_HIST_3C00_POS_ALPHA2	0x0024	W	0x20202020	Posedge Alpha 2
ISP_HIST_3C00_POS_ALPHA3	0x0028	W	0x20202020	Posedge Alpha 3
ISP_HIST_3C00_POS_ALPHA4	0x002C	W	0x00000020	Posedge Alpha 4
ISP_HIST_3C00_NEG_ALPHA0	0x0030	W	0x20202020	Negative Alpha 0
ISP_HIST_3C00_NEG_ALPHA1	0x0034	W	0x20202020	Negative Alpha 1
ISP_HIST_3C00_NEG_ALPHA2	0x0038	W	0x20202020	Negative Alpha 2
ISP_HIST_3C00_NEG_ALPHA3	0x003C	W	0x20202020	Negative Alpha 3
ISP_HIST_3C00_NEG_ALPHA4	0x0040	W	0x00000020	Negative Alpha 4

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Name	Offset	Size	Reset Value	Description
ISP_HIST_3C00_HIST_IIR0	0x0080	W	0x00000000	Hist IIR0
ISP_HIST_3C00_HIST_IIR1	0x0084	W	0x00000000	Hist IIR1
ISP_HIST_3C00_HIST_IIR2	0x0088	W	0x00000000	Hist IIR2
ISP_HIST_3C00_HIST_IIR3	0x008C	W	0x00000000	Hist IIR3
ISP_HIST_3C00_HIST_IIR4	0x0090	W	0x00000000	Hist IIR4
ISP_HIST_3C00_HIST_IIR5	0x0094	W	0x00000000	Hist IIR5
ISP_HIST_3C00_HIST_IIR6	0x0098	W	0x00000000	Hist IIR6
ISP_HIST_3C00_HIST_IIR7	0x009C	W	0x00000000	Hist IIR7
ISP_HIST_3C00_HIST_RW	0x00A0	W	0x00000000	Hist IIR Read or Write
ISP_HIST_3C00_HIST_STAB	0x00A4	W	0x00000011	Hist Stable Frame Number
ISP_HIST_3C00_HIST_UV_SCL	0x00A8	W	0x00000020	Hist UV Scale
ISP_HIST_3C00_ERR_FLAG	0x00FC	W	0x00000000	Hist Error Flag

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

44.4.1.19 ENHANCE

Name	Offset	Size	Reset Value	Description
ISP_ENH_3A00_CTRL	0x0000	W	0x00000200	Cac Control
ISP_ENH_3A00_IIR_FLT	0x0004	W	0x0D050040	Contrast Iir Filter
ISP_ENH_3A00_BILAT_FLT3X3	0x0008	W	0x4080000C	Bilateral Filter 3X3
ISP_ENH_3A00_BILAT_FLT5X5	0x000C	W	0x0005000A	Bilateral Filter 5X5
ISP_ENH_3A00_GLOBAL_STRG	0x0010	W	0x00000600	Global Strength
ISP_ENH_3A00_LUMA_LUT0	0x0014	W	0x04000400	Luma Look Up Table 0
ISP_ENH_3A00_LUMA_LUT1	0x0018	W	0x04000400	Luma Look Up Table 1
ISP_ENH_3A00_LUMA_LUT2	0x001C	W	0x04000400	Luma Look Up Table 2
ISP_ENH_3A00_LUMA_LUT3	0x0020	W	0x04000400	Luma Look Up Table 3
ISP_ENH_3A00_LUMA_LUT4	0x0024	W	0x04000400	Luma Look Up Table 4
ISP_ENH_3A00_LUMA_LUT5	0x0028	W	0x04000400	Luma Look Up Table 5
ISP_ENH_3A00_LUMA_LUT6	0x002C	W	0x04000400	Luma Look Up Table 6
ISP_ENH_3A00_LUMA_LUT7	0x0030	W	0x04000400	Luma Look Up Table 7

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Name	Offset	Size	Reset Value	Description
ISP_ENH_3A00_LUMA_LUT8	0x0034	W	0x00000400	Luma Look Up Table 8
ISP_ENH_3A00_DETAIL_IDX0	0x0038	W	0x02004008	Detail Strength Index 0
ISP_ENH_3A00_DETAIL_IDX1	0x003C	W	0x10020040	Detail Strength Index 1
ISP_ENH_3A00_DETAIL_IDX2	0x0040	W	0x00100200	Detail Strength Index 2
ISP_ENH_3A00_DETAIL_POWER	0x0044	W	0x00000000	Detail Strength Power
ISP_ENH_3A00_DETAIL_VALUE0	0x0048	W	0x04000400	Detail Strength Value 0
ISP_ENH_3A00_DETAIL_VALUE1	0x004C	W	0x04000400	Detail Strength Value 1
ISP_ENH_3A00_DETAIL_VALUE2	0x0050	W	0x04000400	Detail Strength Value 2
ISP_ENH_3A00_DETAIL_VALUE3	0x0054	W	0x04000400	Detail Strength Value 3
ISP_ENH_3A00_PRE_FRAME	0x007C	W	0x00000011	Enhance Previous Frame Counter
ISP_ENH_3A00_IIR0	0x0080	W	0x00000000	Enhance Down Scale IIR0
ISP_ENH_3A00_IIR1	0x0084	W	0x00000000	Enhance Down Scale IIR1
ISP_ENH_3A00_IIR2	0x0088	W	0x00000000	Enhance Down Scale IIR2
ISP_ENH_3A00_IIR3	0x008C	W	0x00000000	Enhance Down Scale IIR3
ISP_ENH_3A00_IIR4	0x0090	W	0x00000000	Enhance Down Scale IIR4
ISP_ENH_3A00_IIR5	0x0094	W	0x00000000	Enhance Down Scale IIR5
ISP_ENH_3A00_IIR6	0x0098	W	0x00000000	Enhance Down Scale IIR6
ISP_ENH_3A00_IIR7	0x009C	W	0x00000000	Enhance Down Scale IIR7
ISP_ENH_3A00_IIR8	0x00A0	W	0x00000000	Enhance Down Scale IIR8
ISP_ENH_3A00_IIR9	0x00A4	W	0x00000000	Enhance Down Scale IIR9
ISP_ENH_3A00_IIR_RW	0x00A8	W	0x00000000	Enhance IIR Read or Write
ISP_ENH_3A00_ERR_FLAG	0x00FC	W	0x00000000	Enhance Error Flag

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

44.4.1.20 HSV

Name	Offset	Size	Reset Value	Description
ISP_HSV_3E00_CTRL	0x0000	W	0x0000000E	HSV control register
ISP_HSV_3E00_MODE_CTRL	0x0004	W	0x00128D24	HSV LUT mode register
ISP_HSV_3E00_UPDATE	0x0008	W	0x00000000	HSV lut update register
ISP_HSV_3E00_HSV_1DLUT_CFG	0x000C	W	0x00000000	HSV 1DLUT CFG
ISP_HSV_3E00_HSV_2DLUT0_CFG	0x0010	W	0x00000000	HSV 2DLUT0 CFG
ISP_HSV_3E00_HSV_2DLUT1_CFG	0x0014	W	0x00000000	HSV 2DLUT1 CFG
ISP_HSV_3E00_HSV_2DLUT2_CFG	0x0018	W	0x00000000	HSV 2DLUT2 CFG

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

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44.4.1.21 YNR

Name	Offset	Size	Reset Value	Description
YNR_2700_GLOBAL_CTRL	0x0000	W	0x00000030	Control register
YNR_2700_GAIN_CTRL	0x0010	W	0x00808010	GAIN CONTROL
YNR_2700_GAIN_ADJ_0_2	0x0014	W	0x01004010	Gain adjust 0-2
YNR_2700_GAIN_ADJ_3_5	0x0018	W	0x01004010	Gain adjust 3-5
YNR_2700_GAIN_ADJ_6_8	0x001C	W	0x01004010	Gain adjust 6-8
YNR_2700_RNR_MAX_R	0x0020	W	0x00003754	Control register
YNR_2700_RNR_CENTER_COOR	0x0024	W	0x00000001	Control register
YNR_2700_RNR_STRENGTH03	0x0028	W	0x10101010	RNR strength adjust curve
YNR_2700_RNR_STRENGTH47	0x002C	W	0x10101010	RNR strength adjust curve
YNR_2700_RNR_STRENGTH8b	0x0030	W	0x10101010	RNR strength adjust curve
YNR_2700_RNR_STRENGTHcf	0x0034	W	0x10101010	RNR strength adjust curve
YNR_2700_RNR_STRENGTH16	0x0038	W	0x00000010	RNR strength adjust curve
YNR_2700_SGM_DX_0_1	0x0040	W	0x00400000	X increments of noise intensity curve
YNR_2700_SGM_DX_2_3	0x0044	W	0x00C00080	X increments of noise intensity curve
YNR_2700_SGM_DX_4_5	0x0048	W	0x01400100	X increments of noise intensity curve
YNR_2700_SGM_DX_6_7	0x004C	W	0x01C00180	X increments of noise intensity curve
YNR_2700_SGM_DX_8_9	0x0050	W	0x02400200	X increments of noise intensity curve
YNR_2700_SGM_DX_10_11	0x0054	W	0x02C00280	X increments of noise intensity curve
YNR_2700_SGM_DX_12_13	0x0058	W	0x03400300	X increments of noise intensity curve
YNR_2700_SGM_DX_14_15	0x005C	W	0x03C00380	X increments of noise intensity curve
YNR_2700_SGM_DX_16	0x0060	W	0x00000400	X increments of noise intensity curve
YNR_2700_SGM_Y_0_1	0x0064	W	0x00A0004C	Noise intensity of low frequency coefficient
YNR_2700_SGM_Y_2_3	0x0068	W	0x00E400D0	Noise intensity of low frequency coefficient
YNR_2700_SGM_Y_4_5	0x006C	W	0x00E400E8	Noise intensity of low frequency coefficient
YNR_2700_SGM_Y_6_7	0x0070	W	0x00CC00D8	Noise intensity of low frequency coefficient
YNR_2700_SGM_Y_8_9	0x0074	W	0x00C000C4	Noise intensity of low frequency coefficient
YNR_2700_SGM_Y_10_11	0x0078	W	0x00B800BC	Noise intensity of low frequency coefficient

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Name	Offset	Size	Reset Value	Description
YNR_2700_SGM_Y_12_13	0x007C	W	0x00A400B4	Noise intensity of low frequency coefficient
YNR_2700_SGM_Y_14_15	0x0080	W	0x00540088	Noise intensity of low frequency coefficient
YNR_2700_SGM_Y_16	0x0084	W	0x00000028	Noise intensity of low frequency coefficient
YNR_2700_MI_TEX2WGT_SCALE_0_1_2	0x0088	W	0x01004840	Scale of middle frequency text to weight
YNR_2700_MI_TEX2WGT_SCALE_3_4_5	0x008C	W	0x00201008	Scale of middle frequency text to weight
YNR_2700_MI_TEX2WGT_SCALE_6_7_8	0x0090	W	0x00100401	Scale of middle frequency text to weight
YNR_2700_LO_TEX2WGT_SCALE_0_1_2	0x0094	W	0x01004840	Scale of low frequency text to weight
YNR_2700_LO_TEX2WGT_SCALE_3_4_5	0x0098	W	0x00201008	Scale of low frequency text to weight
YNR_2700_LO_TEX2WGT_SCALE_6_7_8	0x009C	W	0x00100401	Scale of low frequency text to weight
YNR_2700_HI_SIGMA_GAIN	0x00A0	W	0x00408002	HI SIGMA GAIN
YNR_2700_HI_GAUS_COE	0x00A4	W	0x0028E2D0	NLM COEFFICIENT
YNR_2700_HI_WEIGHT	0x00A8	W	0x00040000	HI WEIGHT
YNR_2700_HI_GAUS1_COE_0_2	0x00AC	W	0x00804420	HI GAUS1 COE
YNR_2700_HI_GAUS1_COE_3_5	0x00B0	W	0x00301C0E	HI GAUS1 COE
YNR_2700_HI_TEXT	0x00B4	W	0x40040080	HI TEXT
YNR_2700_MI_GAUS_COE	0x00C0	W	0x0050200C	MI GAUS COE
YNR_2700_MI_STRG_DETAIL	0x00C4	W	0x00CC0040	MI STRG DETAIL
YNR_2700_MI_WEIGHT	0x00C8	W	0x08010080	MI WEIGHT
YNR_2700_MI_GAUS_COE1	0x00D0	W	0x00001006	MI GAUS COE1
YNR_2700_DSIIR_COE	0x00DC	W	0x08032000	Coe of ynr ds iir filter
YNR_2700_LO_STRG_DETAIL	0x00E0	W	0x00400040	LO STRG DETAIL
YNR_2700_LO_LIMIT_SCALE	0x00E4	W	0x09280040	LO LIMIT SCALE
YNR_2700_LO_WEIGHT	0x00E8	W	0x00024080	LO WEIGHT
YNR_2700_LO_TEXT_THRED	0x00EC	W	0x00199332	LO TEXT THRED
YNR_2700_FUSION_WEIT_ADJ_0_3	0x00F0	W	0x80808080	Fusion Weight adjust 0-3
YNR_2700_FUSION_WEIT_ADJ_4_7	0x00F4	W	0x80808080	Fusion Weight adjust 4-7
YNR_2700_FUSION_WEIT_ADJ_8	0x00F8	W	0x00000080	Fusion Weight adjust 8

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

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44.4.1.22 CNR

Name	Offset	Size	Reset Value	Description
ISP_CNR_2800_CTRL	0x0000	W	0x00000002	Global control
ISP_CNR_2800_EXGAIN	0x0004	W	0x00008080	External gain value
ISP_CNR_2800_THUMB1	0x0008	W	0x00C000A0	The parameter1 used in lbf1x7 module
ISP_CNR_2800_THUMB_BF_RATIO	0x000C	W	0x00000400	The parameter2 used in lbf1x7 module
ISP_CNR_2800_LBF_WEITD	0x0010	W	0x80808080	The distance weight in lbf1x7 module
ISP_CNR_2800_IIR_PARA1	0x0014	W	0x05A04D85	The parameter1 of IIR filter module
ISP_CNR_2800_IIR_PARA2	0x0018	W	0x00003A02	The parameter2 of IIR filter module
ISP_CNR_2800_GAUS_COE1	0x001C	W	0x061C1104	Gaussian filter coefficient parameter1
ISP_CNR_2800_GAUS_COE2	0x0020	W	0x0000301C	Gaussian filter coefficient parameter2
ISP_CNR_2800_GAUS_RATIO	0x0024	W	0x40000400	Gaussian and bf3x3 module parameter
ISP_CNR_2800_BF_PARA1	0x0028	W	0x0801B340	Bilateral filter 3x3 parameter1
ISP_CNR_2800_BF_PARA2	0x002C	W	0x00000014	Bilateral filter 3x3 parameter2
ISP_CNR_2800_SIGMA0	0x0030	W	0x405580FF	Sigma adj ratio curve y0~y3
ISP_CNR_2800_SIGMA1	0x0034	W	0x1015202B	Sigma adj ratio curve y4~y7
ISP_CNR_2800_SIGMA2	0x0038	W	0x01020408	Sigma adj ratio curve y8~y11
ISP_CNR_2800_SIGMA3	0x003C	W	0x00000001	Sigma adj ratio curve y12
ISP_CNR_2800_IIR_GLOBAL_GAIN	0x0040	W	0x00000040	The parameters for IIR gain control
ISP_CNR_2800_WGT_SIGMA0	0x0044	W	0x405580FF	The in data weight adj ratio curve y0~y3 in 3x3bf
ISP_CNR_2800_WGT_SIGMA1	0x0048	W	0x405580FF	The in data weight adj ratio curve y4~y7 in 3x3bf
ISP_CNR_2800_WGT_SIGMA2	0x004C	W	0x01020408	The in data weight adj ratio curve y8~y11 in 3x3bf
ISP_CNR_2800_WGT_SIGMA3	0x0050	W	0x00000001	Wgt sigma curve y12
ISP_CNR_2800_GAUS_X_SIGMAR0	0x0054	W	0x055200FF	Luma index0~index2 of hiFlt sigma curve.
ISP_CNR_2800_GAUS_X_SIGMAR1	0x0058	W	0x055200FF	Luma index3~index5 of hiFlt sigma curve.
ISP_CNR_2800_GAUS_X_SIGMAR2	0x005C	W	0x000200FF	Luma index6~index7 of hiFlt sigma curve.
ISP_CNR_2800_GAUS_Y_SIGMAR0	0x0060	W	0x008000FF	HiFlt sigma curve y0~y1
ISP_CNR_2800_GAUS_Y_SIGMAR1	0x0064	W	0x008000FF	HiFlt sigma curve y2~y3
ISP_CNR_2800_GAUS_Y_SIGMAR2	0x0068	W	0x008000FF	HiFlt sigma curve y4~y5
ISP_CNR_2800_GAUS_Y_SIGMAR3	0x006C	W	0x008000FF	HiFlt sigma curve y6~y7
ISP_CNR_2800_IIR_SIGMAR0	0x0070	W	0x00FFFFFF	LoFlt sigma curve y0~y3

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Name	Offset	Size	Reset Value	Description
ISP_CNR_2800_IIR_SIGMAR1	0x0074	W	0x00FFFFFF	LoFlt sigma curve y4~y7
ISP_CNR_2800_IIR_SIGMAR2	0x0078	W	0x00FFFFFF	LoFlt sigma curve y8~y11
ISP_CNR_2800_IIR_SIGMAR3	0x007C	W	0x000000FF	LoFlt sigma curve y12
ISP_CNR_2800_HSV_CURVE0	0x0080	W	0x00FFFFFF	Hsv adjust table0~3
ISP_CNR_2800_HSV_CURVE1	0x0084	W	0x00FFFFFF	Hsv adjust table4~7
ISP_CNR_2800_HSV_CURVE2	0x0088	W	0x0000FFFF	Hsv adjust table8~9
ISP_CNR_2800_SAT_CURVE0	0x008C	W	0x00FFFFFF	Sat adjust table0~3
ISP_CNR_2800_SAT_CURVE1	0x0090	W	0x00FFFFFF	Sat adjust table4~7
ISP_CNR_2800_SAT_CURVE2	0x0094	W	0x0000FFFF	Sat adjust table8~9
ISP_CNR_2800_GAIN_ADJ_CURVE0	0x0098	W	0x00FFFFFF	Gain adjust table0~3
ISP_CNR_2800_GAIN_ADJ_CURVE1	0x009C	W	0x00FFFFFF	Gain adjust table4~7
ISP_CNR_2800_GAIN_ADJ_CURVE2	0x00A0	W	0x0000FFFF	Gain adjust table8~9

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

44.4.1.23 SHARP

Name	Offset	Size	Reset Value	Description
ISP_SHARP_2900_CTRL	0x0000	W	0x00000000	Global control
ISP_SHARP_2900_TEXTURE0	0x0004	W	0x00000000	Texture parameter0
ISP_SHARP_2900_TEXTURE1	0x0008	W	0x00000000	Texture parameter1
ISP_SHARP_2900_TEXTURE2	0x000C	W	0x00000000	Texture parameter2
ISP_SHARP_2900_TEXTURE3	0x0010	W	0x00000000	Texture parameter3
ISP_SHARP_2900_TEXTURE4	0x0014	W	0x00000000	Texture parameter4
ISP_SHARP_2900_HPF_KERNEL0	0x0018	W	0x00000000	Kernel parameter0
ISP_SHARP_2900_HPF_KERNEL1	0x001C	W	0x00000000	Kernel parameter1
ISP_SHARP_2900_TEXFLT_KERNEL	0x0020	W	0x00000000	Texture kernel parameter
ISP_SHARP_2900_DETAIL0	0x0024	W	0x00000000	Detail parameter0
ISP_SHARP_2900_LUMA_DX	0x002C	W	0x00000000	Luma index parameter1
ISP_SHARP_2900_PBF_VSIGMA0	0x0030	W	0x00000000	Prebifilter vsigma0

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Name	Offset	Size	Reset Value	Description
ISP_SHARP_2900_PBF_VSIGMA1	0x0034	W	0x00000000	Prebifilter vsigma1
ISP_SHARP_2900_PBF_VSIGMA2	0x0038	W	0x00000000	Prebifilter vsigma2
ISP_SHARP_2900_PBF_VSIGMA3	0x003C	W	0x00000000	Prebifilter vsigma3
ISP_SHARP_2900_PBF_KERNEL	0x0040	W	0x00000000	Prebifilter kernel
ISP_SHARP_2900_DETAIL_KERNEL0	0x0044	W	0x00000000	Detail kernel0
ISP_SHARP_2900_DETAIL_KERNEL1	0x0048	W	0x00000000	Detail kernel1
ISP_SHARP_2900_DETAIL_KERNEL2	0x004C	W	0x00000000	Detail kernel2
ISP_SHARP_2900_GAIN	0x0050	W	0x00000000	Global gain
ISP_SHARP_2900_GAIN_ADJ0	0x0054	W	0x00000000	Gain adjust parameter0
ISP_SHARP_2900_GAIN_ADJ1	0x0058	W	0x00000000	Gain adjust parameter1
ISP_SHARP_2900_GAIN_ADJ2	0x005C	W	0x00000000	Gain adjust parameter2
ISP_SHARP_2900_GAIN_ADJ3	0x0060	W	0x00000000	Gain adjust parameter3
ISP_SHARP_2900_GAIN_ADJ4	0x0064	W	0x00000000	Gain adjust parameter4
ISP_SHARP_2900_EDGE0	0x0068	W	0x00000000	Edge parameter0
ISP_SHARP_2900_EDGE1	0x006C	W	0x00000000	Edge parameter1
ISP_SHARP_2900_EDGE_KERNEL0	0x0070	W	0x00000000	Edge kernel0
ISP_SHARP_2900_EDGE_KERNEL1	0x0074	W	0x00000000	Edge kernel1
ISP_SHARP_2900_EDGE_KERNEL2	0x0078	W	0x00000000	Edge kernel2
ISP_SHARP_2900_EDGE_WGT_VAL0	0x007C	W	0x00000000	Edge weight curve y0
ISP_SHARP_2900_EDGE_WGT_VAL1	0x0080	W	0x00000000	Edge weight curve y1
ISP_SHARP_2900_EDGE_WGT_VAL2	0x0084	W	0x00000000	Edge weight curve y2
ISP_SHARP_2900_EDGE_WGT_VAL3	0x0088	W	0x00000000	Edge weight curve y3
ISP_SHARP_2900_EDGE_WGT_VAL4	0x008C	W	0x00000000	Edge weight curve y2
ISP_SHARP_2900_EDGE_WGT_VAL5	0x0090	W	0x00000000	Edge weight curve y5
ISP_SHARP_2900_LUMA_ADJ_STRG0	0x0094	W	0x00000000	Luma adjust curve y0
ISP_SHARP_2900_LUMA_ADJ_STRG1	0x0098	W	0x00000000	Luma adjust curve y1
ISP_SHARP_2900_CENTER	0x009C	W	0x00000000	Center point position
ISP_SHARP_2900_OUT_LIMIT	0x00A0	W	0x00000000	Limit

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Name	Offset	Size	Reset Value	Description
ISP_SHARP_2900_TEX_X_INV_FIX0	0x00A4	W	0x00000000	Equal to (1<<22/hw_sharp_flat_maxLimit)
ISP_SHARP_2900_TEX_X_INV_FIX1	0x00A8	W	0x00000000	Equal to (1<<22/(hw_sharp_edge_minLimit - hw_sharp_flat_maxLimit))
ISP_SHARP_2900_TEX_X_INV_FIX2	0x00AC	W	0x00000000	Equal to (1<<22/(1024-hw_sharp_edge_minLimit))
ISP_SHARP_2900_LOCAL_STRG1	0x00B4	W	0x00000000	The local weight of the lossTexInHinr layer generated based on texture weight0~1
ISP_SHARP_2900_LOCAL_STRG2	0x00B8	W	0x00000000	The local weight of the lossTexInHinr layer generated based on texture weight0~2
ISP_SHARP_2900_DETAIL_SCALE_TAB0	0x00C0	W	0x00000000	Detail scale table0
ISP_SHARP_2900_DETAIL_SCALE_TAB1	0x00C4	W	0x00000000	Detail scale table1
ISP_SHARP_2900_DETAIL_SCALE_TAB2	0x00C8	W	0x00000000	Detail scale table2
ISP_SHARP_2900_DETAIL_SCALE_TAB3	0x00CC	W	0x00000000	Detail scale table3
ISP_SHARP_2900_DETAIL_SCALE_TAB4	0x00D0	W	0x00000000	Detail scale table4
ISP_SHARP_2900_DETAIL_SCALE_TAB5	0x00D4	W	0x00000000	Detail scale table5
ISP_SHARP_2900_DETAIL_TEX_CLIP0	0x00D8	W	0x00000000	Detail texture clip0
ISP_SHARP_2900_DETAIL_TEX_CLIP1	0x00DC	W	0x00000000	Detail texture clip1
ISP_SHARP_2900_DETAIL_TEX_CLIP2	0x00E0	W	0x00000000	Detail texture clip2
ISP_SHARP_2900_DETAIL_TEX_CLIP3	0x00E4	W	0x00000000	Detail texture clip3
ISP_SHARP_2900_DETAIL_TEX_CLIP4	0x00E8	W	0x00000000	Detail texture clip4
ISP_SHARP_2900_DETAIL_TEX_CLIP5	0x00EC	W	0x00000000	Detail texture clip5
ISP_SHARP_2900_GRAIN_TEX_CLIP0	0x00F0	W	0x00000000	Grain texture clip0
ISP_SHARP_2900_GRAIN_TEX_CLIP1	0x00F4	W	0x00000000	Grain texture clip1
ISP_SHARP_2900_GRAIN_TEX_CLIP2	0x00F8	W	0x00000000	Grain texture clip2
ISP_SHARP_2900_GRAIN_TEX_CLIP3	0x00FC	W	0x00000000	Grain texture clip3
ISP_SHARP_2900_GRAIN_TEX_CLIP4	0x0100	W	0x00000000	Grain texture clip4
ISP_SHARP_2900_GRAIN_TEX_CLIP5	0x0104	W	0x00000000	Grain texture clip5
ISP_SHARP_2900_DETAIL_LUMA_CLIP0	0x0108	W	0x00000000	Detail luma clip0
ISP_SHARP_2900_DETAIL_LUMA_CLIP1	0x010C	W	0x00000000	Detail luma clip1

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Name	Offset	Size	Reset Value	Description
ISP_SHARP_2900_DETAIL_LUMA_CLIP2	0x0110	W	0x00000000	Detail luma clip2
ISP_SHARP_2900_DETAIL_LUMA_CLIP3	0x0114	W	0x00000000	Detail luma clip3
ISP_SHARP_2900_DETAIL_LUMA_CLIP4	0x0118	W	0x00000000	Detail luma clip4
ISP_SHARP_2900_DETAIL_LUMA_CLIP5	0x011C	W	0x00000000	Detail luma clip5
ISP_SHARP_2900_GRAIN_STRG	0x0120	W	0x00000000	Hiest strength
ISP_SHARP_2900_HUE_ADJ_TAB0	0x0124	W	0x00000000	Hue adujst table0
ISP_SHARP_2900_HUE_ADJ_TAB1	0x0128	W	0x00000000	Hue adujst table1
ISP_SHARP_2900_HUE_ADJ_TAB2	0x012C	W	0x00000000	Hue adujst table2
ISP_SHARP_2900_DISATANCE_ADJ0	0x0130	W	0x00000000	Distance adjust parameter0
ISP_SHARP_2900_DISATANCE_ADJ1	0x0134	W	0x00000000	Distance adjust parameter1
ISP_SHARP_2900_DISATANCE_ADJ2	0x0138	W	0x00000000	Distance adjust parameter2
ISP_SHARP_2900_TEX2DETAIL_STRG0	0x013C	W	0x00000000	The local weight of the detail layer generated based on texture weight, with an x-axis of [0, 128, 256, 384, 512, 640, 768, 896, 1024]Fixed-point:[0, 1, 10]
ISP_SHARP_2900_TEX2DETAIL_STRG1	0x0140	W	0x00000000	The local weight of the detail layer generated based on texture weight, with an x-axis of [0, 128, 256, 384, 512, 640, 768, 896, 1024]Fixed-point:[0, 1, 10]
ISP_SHARP_2900_TEX2DETAIL_STRG2	0x0144	W	0x00000000	The local weight of the detail layer generated based on texture weight, with an x-axis of [0, 128, 256, 384, 512, 640, 768, 896, 1024]Fixed-point:[0, 1, 10]
ISP_SHARP_2900_NOISE_SIGMA0	0x0148	W	0x00000000	Noise sigma0
ISP_SHARP_2900_NOISE_SIGMA1	0x014C	W	0x00000000	Noise sigma1
ISP_SHARP_2900_NOISE_SIGMA2	0x0150	W	0x00000000	Noise sigma2
ISP_SHARP_2900_NOISE_SIGMA3	0x0154	W	0x00000000	Noise sigma3
ISP_SHARP_2900_NOISE_SIGMA4	0x0158	W	0x00000000	Noise sigma4
ISP_SHARP_2900_TEX2MFDETAIL_STRG0	0x015C	W	0x00000000	The local weight of the middle detail layer generated based on texture weight, with an x-axis of [0, 128, 256, 384, 512, 640, 768, 896, 1024]Fixed-point:[0, 1, 10]

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Name	Offset	Size	Reset Value	Description
ISP_SHARP_2900_TEX2MIDETAIL_STRG1	0x0160	W	0x00000000	The local weight of the middle detail layer generated based on texture weight, with an x-axis of [0, 128, 256, 384, 512, 640, 768, 896, 1024]Fixed-point:[0, 1, 10]
ISP_SHARP_2900_TEX2MIDETAIL_STRG2	0x0164	W	0x00000000	The local weight of the middle detail layer generated based on texture weight, with an x-axis of [0, 128, 256, 384, 512, 640, 768, 896, 1024]Fixed-point:[0, 1, 10]
ISP_SHARP_2900_LOSSTEXINHINR_STRG	0x016C	W	0x00000000	LossTexInHinr strength
ISP_SHARP_2900_NOISE_CURVE0	0x0170	W	0x00000000	Noise curve0
ISP_SHARP_2900_NOISE_CURVE1	0x0174	W	0x00000000	Noise curve0
ISP_SHARP_2900_NOISE_CURVE2	0x0178	W	0x00000000	Noise curve2
ISP_SHARP_2900_NOISE_CURVE3	0x017C	W	0x00000000	Noise curve3
ISP_SHARP_2900_NOISE_CURVE4	0x0180	W	0x00000000	Noise curve4
ISP_SHARP_2900_NOISE_CURVE5	0x0184	W	0x00000000	Noise curve5
ISP_SHARP_2900_NOISE_CURVE6	0x0188	W	0x00000000	Noise curve6
ISP_SHARP_2900_NOISE_CURVE7	0x018C	W	0x00000000	Noise curve7
ISP_SHARP_2900_NOISE_CURVE8	0x0190	W	0x00000000	Noise curve8
ISP_SHARP_2900_NOISE_CLIP	0x0194	W	0x00000000	Noise clip
ISP_SHARP_2900_EDGEWGTFLT_KERNEL	0x0198	W	0x00000000	Edge wgt flt kernel
ISP_SHARP_2900_EDGE_GLOBAL_CLIP	0x01A0	W	0x00000000	Edge global clip
ISP_SHARP_2900_MIDETAIL	0x01A4	W	0x00000000	Middle detail
ISP_SHARP_2900_MIDETAIL_CLIP	0x01A8	W	0x00000000	Global clip val of middle detail
ISP_SHARP_2900_SATURATION_STRG0	0x01AC	W	0x00000000	Saturation2strg 0
ISP_SHARP_2900_SATURATION_STRG1	0x01B0	W	0x00000000	Saturation2strg 1
ISP_SHARP_2900_SATURATION_STRG2	0x01B4	W	0x00000000	Saturation2strg2

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

44.4.1.24 LDCH_B3DMC

Name	Offset	Size	Reset Value	Description
ISP_LDCH_3B00_LDCH_ADR_STS	0x0000	W	0x00000001	LDCH control register

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Name	Offset	Size	Reset Value	Description
ISP_LDCH_3B00_LDCH_BIC_TABLE0	0x0004	W	0x00000000	LDCH bicubic mode table0
ISP_LDCH_3B00_LDCH_BIC_TABLE1	0x0008	W	0x00000000	LDCH bicubic mode table1
ISP_LDCH_3B00_LDCH_BIC_TABLE2	0x000C	W	0x00000000	LDCH bicubic mode table2
ISP_LDCH_3B00_LDCH_BIC_TABLE3	0x0010	W	0x00000000	LDCH bicubic mode table3
ISP_LDCH_3B00_LDCH_BIC_TABLE4	0x0014	W	0x00000000	LDCH bicubic mode table4
ISP_LDCH_3B00_LDCH_BIC_TABLE5	0x0018	W	0x00000000	LDCH bicubic mode table5
ISP_LDCH_3B00_LDCH_BIC_TABLE6	0x001C	W	0x00000000	LDCH bicubic mode table6
ISP_LDCH_3B00_LDCH_BIC_TABLE7	0x0020	W	0x00000000	LDCH bicubic mode table7
ISP_LDCH_3B00_LDCH_BIC_TABLE8	0x0024	W	0x00000000	LDCH bicubic mode table8
ISP_LDCH_3B00_LDCH_OUT_HSIZE	0x0028	W	0x00000000	if ldch output hsize not equal input size, then use this reg
ISP_LDCH_3B00_B3DMCV_CTRL	0x0080	W	0x00000000	B3DMCV controller
ISP_LDCH_3B00_B3DMCV_WR_ADDR	0x00A8	W	0x00000000	B3DMCV DDR write address base
ISP_LDCH_3B00_B3DMCV_WR_STRIDE	0x00AC	W	0x00000000	B3DMCV DDR write stride
ISP_LDCH_3B00_B3DMCV_FFFF_OFF	0x00B0	W	0x00000000	B3DMCV map last 0xffff position
ISP_LDCH_3B00_B3DMCH_ADR_STS	0x00E0	W	0x00000000	B3DMCH controller
ISP_LDCH_3B00_B3DMC_EXTBOUND1	0x00E8	W	0x00000000	B3DMC other configuration

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

44.4.1.25 GAIN

Name	Offset	Size	Reset Value	Description
ISP_GAIN_3F00_CTRL	0x0000	W	0x00000000	Gain control
ISP_GAIN_3F00_GAIN_G0	0x0004	W	0x00000040	HDR merge gain0 or initial gain when HDR disable
ISP_GAIN_3F00_GAIN_G1_G2	0x0008	W	0x00400040	Gain1 & gain2 for HDR_MERGE
ISP_GAIN_3F00_FIFO_STATUS	0x000C	W	0x00000000	All FIFO status

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

44.4.1.26 BILINEAR_SCALE

Operational Base

Name	Base Address
MP_SCALE	0x21D00C00
SP_SCALE	0x21D01000

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Name	Offset	Size	Reset Value	Description
BILINEAR_SCALE_1000_SCALE_CTRL	0x0000	W	0x00000000	Global control register
BILINEAR_SCALE_1000_SCALE_UPDATE	0x0004	W	0x00000020	Shadow update register
BILINEAR_SCALE_1000_SCALE_SRC_SIZE	0x0008	W	0x00000000	Scale size of source (input)
BILINEAR_SCALE_1000_SCALE_DST_SIZE	0x000C	W	0x00000000	Scale size of destination (output)
BILINEAR_SCALE_1000_SCALE_HY_FAC	0x0010	W	0x00000000	Horizontal luminance scale factor register
BILINEAR_SCALE_1000_SCALE_HC_FAC	0x0014	W	0x00000000	Horizontal chrominance scale factor register
BILINEAR_SCALE_1000_SCALE_VY_FAC	0x0018	W	0x00000000	Vertical luminance scale factor register
BILINEAR_SCALE_1000_SCALE_VC_FAC	0x001C	W	0x00000000	Vertical chrominance scale factor register
BILINEAR_SCALE_1000_SCALE_HY_OFFS	0x0020	W	0x00000000	Horizontal luminance scale coordinate offset register for bilinear
BILINEAR_SCALE_1000_SCALE_HC_OFFS	0x0024	W	0x00000000	Horizontal chrominance scale coordinate offset register for bilinear
BILINEAR_SCALE_1000_SCALE_VY_OFFS	0x0028	W	0x00000000	Vertical luminance scale coordinate offset register for bilinear
BILINEAR_SCALE_1000_SCALE_VC_OFFS	0x002C	W	0x00000000	Vertical chrominance scale coordinate offset register for bilinear
BILINEAR_SCALE_1000_SCALE_HY_SIZE	0x0040	W	0x00000000	Scale out Y size
BILINEAR_SCALE_1000_SCALE_HC_SIZE	0x0044	W	0x00000000	Scale out UV size for average
BILINEAR_SCALE_1000_SCALE_HY_OFFS_MI	0x0048	W	0x00000000	DDR data width is 128bit but Y data width is 8bit. This register configure the offset of first Y pixel in 128bit, which range from 0~15.
BILINEAR_SCALE_1000_SCALE_HC_OFFS_MI	0x004C	W	0x00000000	DDR data width is 128bit but UV data width is 8bit. This register configure the offset of first UV pixel in 128bit, which range from 0~15.
BILINEAR_SCALE_1000_SCALE_IN_CROP_OFFSET	0x0050	W	0x00000000	Scale in data cut first some pixels if needed.
BILINEAR_SCALE_1000_SCALE_CTRL_SHD	0x0080	W	0x00000000	Global control shadow register
BILINEAR_SCALE_1000_SCALE_SRC_SIZE_SHD	0x0088	W	0x00000000	Scale size of source (input), shadow register
BILINEAR_SCALE_1000_SCALE_DST_SIZE_SHD	0x008C	W	0x00000000	Scale size of destination (output), shadow register
BILINEAR_SCALE_1000_SCALE_HY_FAC_SHD	0x0090	W	0x00000000	Horizontal luminance scale factor shadow register
BILINEAR_SCALE_1000_SCALE_HC_FAC_SHD	0x0094	W	0x00000000	Horizontal chrominance scale factor shadow register

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Name	Offset	Size	Reset Value	Description
BILINEAR_SCALE_1000_SCALE_VY_FAC_SHD	0x0098	W	0x00000000	Vertical luminance scale factor shadow register
BILINEAR_SCALE_1000_SCALE_VC_FAC_SHD	0x009C	W	0x00000000	Vertical chrominance scale factor shadow register
BILINEAR_SCALE_1000_SCALE_HY_OFFS_SHD	0x00A0	W	0x00000000	Horizontal luminance scale coordinate offset shadow register for bilinear
BILINEAR_SCALE_1000_SCALE_HC_OFFS_SHD	0x00A4	W	0x00000000	Horizontal chrominance scale coordinate offset shadow register for bilinear
BILINEAR_SCALE_1000_SCALE_VY_OFFS_SHD	0x00A8	W	0x00000000	Vertical luminance scale coordinate offset shadow register for bilinear
BILINEAR_SCALE_1000_SCALE_VC_OFFS_SHD	0x00AC	W	0x00000000	Vertical chrominance scale coordinate offset shadow register for bilinear
BILINEAR_SCALE_1000_SCALE_HY_SIZE_SHD	0x00C0	W	0x00000000	Scale out Y size shadow signal
BILINEAR_SCALE_1000_SCALE_HC_SIZE_SHD	0x00C4	W	0x00000000	Scale out UV size shadow signal
BILINEAR_SCALE_1000_SCALE_HY_OFFS_MI_SHD	0x00C8	W	0x00000000	Shadow signal of sw_scl_hy_offs_mi
BILINEAR_SCALE_1000_SCALE_HC_OFFS_MI_SHD	0x00CC	W	0x00000000	Shadow signal of sw_scl_hc_offs_mi
BILINEAR_SCALE_1000_SCALE_IN_CROP_OFFSET_SHD	0x00D0	W	0x00000000	Scale in data cut first some pixels if needed, shadow register.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**- Double WORD (64 bits) access*

44.4.1.27 DUAL_CROP

Name	Offset	Size	Reset Value	Description
DUAL_CROP_0880_CTRL	0x0000	W	0x00000000	Global control register
DUAL_CROP_0880_M_H_OFFS	0x0004	W	0x00000080	MP path h offset
DUAL_CROP_0880_M_V_OFFS	0x0008	W	0x00000080	MP path v offset
DUAL_CROP_0880_M_H_SIZE	0x000C	W	0x00000080	MP path h size
DUAL_CROP_0880_M_V_SIZE	0x0010	W	0x00000C00	MP path v size
DUAL_CROP_0880_S_H_OFFS	0x0014	W	0x00000080	SP path h offset
DUAL_CROP_0880_S_V_OFFS	0x0018	W	0x00000080	SP path v offset
DUAL_CROP_0880_S_H_SIZE	0x001C	W	0x00000080	SP path h size
DUAL_CROP_0880_S_V_SIZE	0x0020	W	0x00000C00	SP path v size
DUAL_CROP_0880_M_H_OFFS_SHD	0x0024	W	0x00000080	MP path h offset shadow signal
DUAL_CROP_0880_M_V_OFFS_SHD	0x0028	W	0x00000080	MP path v offset shadow signal

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Name	Offset	Size	Reset Value	Description
DUAL_CROP_0880_M_H_SIZE_SHD	0x002C	W	0x00000080	MP path h size shadow signal
DUAL_CROP_0880_M_V_SIZE_SHD	0x0030	W	0x00000000	MP path v size shadow signal
DUAL_CROP_0880_S_H_OFFS_SHD	0x0034	W	0x00000080	SP path h offset
DUAL_CROP_0880_S_V_OFFS_SHD	0x0038	W	0x00000080	SP path v offset shadow signal
DUAL_CROP_0880_S_H_SIZE_SHD	0x003C	W	0x00000080	SP path h size shadow signal
DUAL_CROP_0880_S_V_SIZE_SHD	0x0040	W	0x00000080	SP path v size shadow signal
DUAL_CROP_0880_FBC_H_OFFS	0x0044	W	0x00000080	FBC path h offset
DUAL_CROP_0880_FBC_V_OFFS	0x0048	W	0x00000080	FBC path v offset
DUAL_CROP_0880_FBC_H_SIZE	0x004C	W	0x00000080	FBC path h size
DUAL_CROP_0880_FBC_V_SIZE	0x0050	W	0x00000080	FBC path v size
DUAL_CROP_0880_FBC_H_OFFS_SHD	0x0054	W	0x00000080	FBC path h offset
DUAL_CROP_0880_FBC_V_OFF_SHD	0x0058	W	0x00000080	FBC path v offset
DUAL_CROP_0880_FBC_H_SIZE_SHD	0x005C	W	0x00000080	FBC path h size
DUAL_CROP_0880_FBC_V_SIZE_SHD	0x0060	W	0x00000080	FBC path v size

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

44.4.1.28 FLASH

Name	Offset	Size	Reset Value	Description
ISP_FLASH_0660_CMD	0x0000	W	0x00000000	Flash command
ISP_FLASH_0660_CONFIG	0x0004	W	0x00000000	Flash configure
ISP_FLASH_0660_PREDIV	0x0008	W	0x00000000	Flash Counter Pre-Divider
ISP_FLASH_0660_DELAY	0x000C	W	0x00000000	Flash Delay
ISP_FLASH_0660_TIME	0x0010	W	0x00000000	Flash time
ISP_FLASH_0660_MAXP	0x0014	W	0x00000000	Maximum value for flash or preflash

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

44.4.1.29 RAWAF

Name	Offset	Size	Reset Value	Description
ISP_RAWAF_4D00_CTRL	0x0000	W	0x00C100B6	This is the control register for RAWAF measurement unit
ISP_RAWAF_4D00_OFFSET_WINA	0x0004	W	0x00030003	Top Left corner of measure window A

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Name	Offset	Size	Reset Value	Description
ISP_RAWAF_4D00_SIZE_WINA	0x0008	W	0x00000000	Size of measure window A
ISP_RAWAF_4D00_OFFSET_WINB	0x000C	W	0x00000000	Top Left corner of measure window B
ISP_RAWAF_4D00_SIZE_WINB	0x0010	W	0x00000000	Size of measure window B
ISP_RAWAF_4D00_INT_LINE	0x0014	W	0x000FC963	Line of window 15x15 that need to produce int signal
ISP_RAWAF_4D00_CTRL1	0x0018	W	0x00000000	Size of measure window A
ISP_RAWAF_4D00_HIGHLIT_CNT_WINB	0x001C	W	0x00000000	Sharpness Value Status Register of Window B
ISP_RAWAF_4D00_H1IIR_SUMB	0x0020	W	0x00000000	Sharpness Value Status Register of Window B
ISP_RAWAF_4D00_H2IIR_SUMB	0x0024	W	0x00000000	Sharpness Value Status Register of Window B
ISP_RAWAF_4D00_V1IIR_SUMB	0x0028	W	0x00000000	Sharpness Value Status Register of Window B
ISP_RAWAF_4D00_V2IIR_SUMB	0x002C	W	0x00000000	Sharpness Value Status Register of Window B
ISP_RAWAF_4D00_LUM_B	0x0030	W	0x00000000	Luminance Value Status Register of Window B
ISP_RAWAF_4D00_GAMMA_Y0	0x0034	W	0x002D0000	Include y0 and y1 value of gamma table
ISP_RAWAF_4D00_GAMMA_Y1	0x0038	W	0x00B3006C	Include y2 and y3 value of gamma table
ISP_RAWAF_4D00_GAMMA_Y2	0x003C	W	0x015800F5	Include y4 and y5 value of gamma table
ISP_RAWAF_4D00_GAMMA_Y3	0x0040	W	0x01CB0199	Include y6 and y7 value of gamma table
ISP_RAWAF_4D00_GAMMA_Y4	0x0044	W	0x023701F4	Include y8 and y9 value of gamma table
ISP_RAWAF_4D00_GAMMA_Y5	0x0048	W	0x02A4026E	Include y10 and y11 value of gamma table
ISP_RAWAF_4D00_GAMMA_Y6	0x004C	W	0x034102F7	Include y12 and y13 value of gamma table
ISP_RAWAF_4D00_GAMMA_Y7	0x0050	W	0x03C20380	Include y14 and y15 value of gamma table
ISP_RAWAF_4D00_GAMMA_Y8	0x0054	W	0x000003FF	Include y16 value of gamma table
ISP_RAWAF_4D00_INT_STATE	0x0058	W	0x00000000	Int state of five line interrupt
ISP_RAWAF_4D00_HIIR_THRESH	0x005C	W	0x00200020	AF measurement threshold
ISP_RAWAF_4D00_H1_IIR1_COE01	0x0060	W	0x02BB0200	H1IIR1 filter coefficient
ISP_RAWAF_4D00_H1_IIR1_COE23	0x0064	W	0x003F0F19	H1IIR1 filter coefficient
ISP_RAWAF_4D00_H1_IIR1_COE45	0x0068	W	0x0EB10000	H1IIR1 filter coefficient
ISP_RAWAF_4D00_H_CURVEL	0x006C	W	0x05061C40	LDG curve for H1 H2
ISP_RAWAF_4D00_H1_IIR2_COE01	0x0070	W	0x01BF0200	H1IIR2 filter coefficient

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Name	Offset	Size	Reset Value	Description
ISP_RAWAF_4D00_H1_IIR2_COE23	0x0074	W	0x00AC0E7E	H1IIR2 filter coefficient
ISP_RAWAF_4D00_H1_IIR2_COE45	0x0078	W	0x0FC10000	H1IIR2 filter coefficient
ISP_RAWAF_4D00_H_CURVEH	0x007C	W	0x057808B9	LDG curve for H1 H2
ISP_RAWAF_4D00_H2_IIR1_COE01	0x0080	W	0x02720200	H2IIR1 filter coefficient
ISP_RAWAF_4D00_H2_IIR1_COE23	0x0084	W	0x00670ECB	H2IIR1 filter coefficient
ISP_RAWAF_4D00_H2_IIR1_COE45	0x0088	W	0x0F990000	H2IIR1 filter coefficient
ISP_RAWAF_4D00_V_CURVEL	0x008C	W	0x05061C40	LDG curve for V1 V2
ISP_RAWAF_4D00_H2_IIR2_COE01	0x0090	W	0x01BF0200	H2IIR2 filter coefficient
ISP_RAWAF_4D00_H2_IIR2_COE23	0x0094	W	0x00AC0E9F	H2IIR2 filter coefficient
ISP_RAWAF_4D00_H2_IIR2_COE45	0x0098	W	0x0F540000	H2IIR2 filter coefficient
ISP_RAWAF_4D00_V_CURVEH	0x009C	W	0x057808B9	LDG curve for V1 V2
ISP_RAWAF_4D00_V_IIR_COE0	0x00A0	W	0x00AB00AB	VIIR filter coefficient
ISP_RAWAF_4D00_V_IIR_COE1	0x00A4	W	0x00330033	VIIR filter coefficient
ISP_RAWAF_4D00_V_IIR_COE2	0x00A8	W	0x00E700E7	VIIR filter coefficient
ISP_RAWAF_4D00_CORING_H	0x00AC	W	0x00E700E7	CORING for H direction input = (max(input - fv_thresh, 0) * fv_slope) >> AF_CORE_SLOP_FIX_BITS; ret = min(input, fv_limit);
ISP_RAWAF_4D00_V_FIR_COE0	0x00B0	W	0x02000200	1x3 VFIR filter coefficient
ISP_RAWAF_4D00_V_FIR_COE1	0x00B4	W	0x00000000	1x3 VFIR filter coefficient
ISP_RAWAF_4D00_V_FIR_COE2	0x00B8	W	0x0E000E00	1x3 VFIR filter coefficient
ISP_RAWAF_4D00_CORING_V	0x00BC	W	0x00E700E7	CORING for V direction
ISP_RAWAF_4D00_GAUS_COE_03	0x00C0	W	0x10081008	GAUS filter coefficient
ISP_RAWAF_4D00_GAUS_COE_47	0x00C4	W	0x10081020	GAUS filter coefficient
ISP_RAWAF_4D00_GAUS_COE_8	0x00C8	W	0x00000008	GAUS filter coefficient
ISP_RAWAF_4D00_HVIIR_VAR_SHIFT	0x00CC	W	0x00000000	Variable shift register
ISP_RAWAF_4D00_HIGHLIT_THRESH	0x00D0	W	0x000003CC	Threshold and ram_star_addr register
ISP_RAWAF_4D00_THRES	0x00D8	W	0x00000000	Threshold and ram_star_addr register

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Name	Offset	Size	Reset Value	Description
ISP_RAWAF_4D00_RAM_DATA	0x00E0	W	0x00000000	Read 15x15 sum data in ram should choose this address, then data will be read out by AHB bus, or write to DDR. Total data is 225*5 wordsIf (rd_cnt < 225*4) read hviir data(word0:v1iir;word1:v2iir;word2:h1iir;word3:h2iir etc.) else read aehgl data(each word: low12bit is average_aeN, high 20bit is highlight_numN)

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

44.4.1.30 RAWAE

Operational Base

Name	Base Address
RAWAE_BIG	0x21D04400
RAWAE0_BIG	0x21D04500

Name	Offset	Size	Reset Value	Description
RAWAE_BIG_4400_4500_CTRL	0x0000	W	0x00000000	Exposure control
RAWAE_BIG_4400_4500_WND0_BLK_SIZE	0x0004	W	0x00000000	Size of one block for window0
RAWAE_BIG_4400_4500_WND0_OFFSET	0x0008	W	0x00000000	Offset of one block for window0
RAWAE_BIG_4400_4500_RAM_CTRL	0x000C	W	0x00000000	RAM address offset
RAWAE_BIG_4400_4500_WND1_SIZE	0x0010	W	0x00000000	Size of single separated window
RAWAE_BIG_4400_4500_WND1_OFFSET	0x0014	W	0x00000000	Offset of single separated window
RAWAE_BIG_4400_4500_WND1_SUMR	0x0030	W	0x00000000	Sum R channel data for this single separated window
RAWAE_BIG_4400_4500_WND1_SUMG	0x0040	W	0x00000000	Sum G channel data for this single separated window
RAWAE_BIG_4400_4500_WND1_SUMB	0x0050	W	0x00000000	Sum B channel data for this single separated window
RAWAE_BIG_4400_4500_RO_MEAN_BASE_ADDR	0x0080	W	0x00000000	Mean luminance value of block 00 ~ee(total 225) Read data from RAM, support burst16

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

44.4.1.31 RAWAWB

Name	Offset	Size	Reset Value	Description
ISP_RAWAWB_5000_CTRL	0x0000	W	0x00000000	Global control register
ISP_RAWAWB_5000_BLK_CTRL	0x0004	W	0xFFFF0000	Block control register
ISP_RAWAWB_5000_WIN_OFFS	0x0008	W	0x00000000	Awb vertical and horizontal offset of measure window

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Name	Offset	Size	Reset Value	Description
ISP_RAWAWB_5000_WIN_SIZE	0x000C	W	0x00000000	Awb vertical and horizontal window size
ISP_RAWAWB_5000_LIMIT_RG_MAX	0x0010	W	0x00000000	Max red and green value in white point detection
ISP_RAWAWB_5000_LIMIT_BY_MAX	0x0014	W	0x00000000	Max blue and luminance value in white point detection
ISP_RAWAWB_5000_LIMIT_RG_MIN	0x0018	W	0x00000000	Min red and green value in white point detection
ISP_RAWAWB_5000_LIMIT_BY_MIN	0x001C	W	0x00000000	Min blue and luminance value in white point detection
ISP_RAWAWB_5000_WEIGHT_CURVE_CTRL	0x0020	W	0x00000000	Weight curve control
ISP_RAWAWB_5000_YWEIGHT_CURVE_XCOOR03	0x0024	W	0x60402000	The X coordinate of Y weight curve
ISP_RAWAWB_5000_YWEIGHT_CURVE_XCOOR47	0x0028	W	0xE0C0A080	The X coordinate of Y weight curve
ISP_RAWAWB_5000_YWEIGHT_CURVE_XCOOR8	0x002C	W	0x000000FF	The X coordinate of Y weight curve
ISP_RAWAWB_5000_YWEIGHT_CURVE_YCOOR03	0x0030	W	0x20202020	The Y coordinate of Y weight curve
ISP_RAWAWB_5000_YWEIGHT_CURVE_YCOOR47	0x0034	W	0x20202020	The Y coordinate of Y weight curve
ISP_RAWAWB_5000_YWEIGHT_CURVE_YCOOR8	0x0038	W	0x01000020	The Y coordinate of Y weight curve
ISP_RAWAWB_5000_PRE_WBGAIN_INV	0x003C	W	0x01000100	This is a white balance gain invert operation
ISP_RAWAWB_5000_UV_DETC_VERTEX0_0	0x0040	W	0x00000000	UV detect, vertex
ISP_RAWAWB_5000_UV_DETC_VERTEX1_0	0x0044	W	0x00000000	UV detect, vertex
ISP_RAWAWB_5000_UV_DETC_VERTEX2_0	0x0048	W	0x00000000	UV detect, vertex
ISP_RAWAWB_5000_UV_DETC_VERTEX3_0	0x004C	W	0x00000000	UV detect, vertex
ISP_RAWAWB_5000_UV_DETC_ISLOPE01_0	0x0050	W	0x00000000	UV detect, slope inversion
ISP_RAWAWB_5000_UV_DETC_ISLOPE12_0	0x0054	W	0x00000000	UV detect, slope inversion
ISP_RAWAWB_5000_UV_DETC_ISLOPE23_0	0x0058	W	0x00000000	UV detect, slope inversion
ISP_RAWAWB_5000_UV_DETC_ISLOPE30_0	0x005C	W	0x00000000	UV detect, slope inversion
ISP_RAWAWB_5000_UV_DETC_VERTEX0_1	0x0060	W	0x00000000	UV detect, vertex
ISP_RAWAWB_5000_UV_DETC_VERTEX1_1	0x0064	W	0x00000000	UV detect, vertex
ISP_RAWAWB_5000_UV_DETC_VERTEX2_1	0x0068	W	0x00000000	UV detect, vertex
ISP_RAWAWB_5000_UV_DETC_VERTEX3_1	0x006C	W	0x00000000	UV detect, vertex
ISP_RAWAWB_5000_UV_DETC_ISLOPE01_1	0x0070	W	0x00000000	UV detect, slope inversion
ISP_RAWAWB_5000_UV_DETC_ISLOPE12_1	0x0074	W	0x00000000	UV detect, slope inversion

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Name	Offset	Size	Reset Value	Description
ISP_RAWAWB_5000_UV_DETC_ISLOPE23_1	0x0078	W	0x00000000	UV detect, slope inversion
ISP_RAWAWB_5000_UV_DETC_ISLOPE30_1	0x007C	W	0x00000000	UV detect, slope inversion
ISP_RAWAWB_5000_UV_DETC_VERTEX0_2	0x0080	W	0x00000000	UV detect, vertex
ISP_RAWAWB_5000_UV_DETC_VERTEX1_2	0x0084	W	0x00000000	UV detect, vertex
ISP_RAWAWB_5000_UV_DETC_VERTEX2_2	0x0088	W	0x00000000	UV detect, vertex
ISP_RAWAWB_5000_UV_DETC_VERTEX3_2	0x008C	W	0x00000000	UV detect, vertex
ISP_RAWAWB_5000_UV_DETC_ISLOPE01_2	0x0090	W	0x00000000	UV detect, slope inversion
ISP_RAWAWB_5000_UV_DETC_ISLOPE12_2	0x0094	W	0x00000000	UV detect, slope inversion
ISP_RAWAWB_5000_UV_DETC_ISLOPE23_2	0x0098	W	0x00000000	UV detect, slope inversion
ISP_RAWAWB_5000_UV_DETC_ISLOPE30_2	0x009C	W	0x00000000	UV detect, slope inversion
ISP_RAWAWB_5000_UV_DETC_VERTEX0_3	0x00A0	W	0x00000000	UV detect, vertex
ISP_RAWAWB_5000_UV_DETC_VERTEX1_3	0x00A4	W	0x00000000	UV detect, vertex
ISP_RAWAWB_5000_UV_DETC_VERTEX2_3	0x00A8	W	0x00000000	UV detect, vertex
ISP_RAWAWB_5000_UV_DETC_VERTEX3_3	0x00AC	W	0x00000000	UV detect, vertex
ISP_RAWAWB_5000_UV_DETC_ISLOPE01_3	0x00B0	W	0x00000000	UV detect, slope inversion
ISP_RAWAWB_5000_UV_DETC_ISLOPE12_3	0x00B4	W	0x00000000	UV detect, slope inversion
ISP_RAWAWB_5000_UV_DETC_ISLOPE23_3	0x00B8	W	0x00000000	UV detect, slope inversion
ISP_RAWAWB_5000_UV_DETC_ISLOPE30_3	0x00BC	W	0x00000000	UV detect, slope inversion
ISP_RAWAWB_5000_CCM_COEFF0_R	0x01C0	W	0x07B70065	CCM matrix R coefficient 0 & 1
ISP_RAWAWB_5000_CCM_COEFF1_R	0x01C4	W	0x000007E4	CCM matrix R coefficient 2 & offset
ISP_RAWAWB_5000_CCM_COEFF0_G	0x01C8	W	0x005807D9	CCM matrix G coefficient 0 & 1
ISP_RAWAWB_5000_CCM_COEFF1_G	0x01CC	W	0x000007CF	CCM matrix G coefficient 2 & offset
ISP_RAWAWB_5000_CCM_COEFF0_B	0x01D0	W	0x07B70002	CCM matrix B coefficient 0&1
ISP_RAWAWB_5000_CCM_COEFF1_B	0x01D4	W	0x00000046	CCM matrix B coefficient 2 & offset
ISP_RAWAWB_5000_RGB2XY_WT01	0x01FC	W	0x00000000	RGB2XY weight matrix, coefficient 01
ISP_RAWAWB_5000_RGB2XY_WT2	0x0200	W	0x00000000	RGB2XY weight matrix, coefficient 2
ISP_RAWAWB_5000_RGB2XY_MAT0_XY	0x0204	W	0x00000000	RGB2XY, rotation matrix, first column XY

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Name	Offset	Size	Reset Value	Description
ISP_RAWAWB_5000_RGB2XY_MAT1_XY	0x0208	W	0x00000000	RGB2XY, rotation matrix, second column XY
ISP_RAWAWB_5000_RGB2XY_MAT2_XY	0x020C	W	0x00000000	RGB2XY, rotation matrix, third column XY
ISP_RAWAWB_5000_XY_DETC_NOR_X_0	0x0210	W	0x00000000	XY detect, x boundary of normal range
ISP_RAWAWB_5000_XY_DETC_NOR_Y_0	0x0214	W	0x00000000	XY detect, y boundary of normal range
ISP_RAWAWB_5000_XY_DETC_BIG_X_0	0x0218	W	0x00000000	XY detect, x boundary of big range
ISP_RAWAWB_5000_XY_DETC_BIG_Y_0	0x021C	W	0x00000000	XY detect, y boundary of big range
ISP_RAWAWB_5000_XY_DETC_NOR_X_1	0x0228	W	0x00000000	XY detect, x boundary of normal range
ISP_RAWAWB_5000_XY_DETC_NOR_Y_1	0x022C	W	0x00000000	XY detect, y boundary of normal range
ISP_RAWAWB_5000_XY_DETC_BIG_X_1	0x0230	W	0x00000000	XY detect, x boundary of big range
ISP_RAWAWB_5000_XY_DETC_BIG_Y_1	0x0234	W	0x00000000	XY detect, y boundary of big range
ISP_RAWAWB_5000_XY_DETC_NOR_X_2	0x0240	W	0x00000000	XY detect, x boundary of normal range
ISP_RAWAWB_5000_XY_DETC_NOR_Y_2	0x0244	W	0x00000000	XY detect, y boundary of normal range
ISP_RAWAWB_5000_XY_DETC_BIG_X_2	0x0248	W	0x00000000	XY detect, x boundary of big range
ISP_RAWAWB_5000_XY_DETC_BIG_Y_2	0x024C	W	0x00000000	XY detect, y boundary of big range
ISP_RAWAWB_5000_XY_DETC_NOR_X_3	0x0258	W	0x00000000	XY detect, x boundary of normal range
ISP_RAWAWB_5000_XY_DETC_NOR_Y_3	0x025C	W	0x00000000	XY detect, y boundary of normal range
ISP_RAWAWB_5000_XY_DETC_BIG_X_3	0x0260	W	0x00000000	XY detect, x boundary of big range
ISP_RAWAWB_5000_XY_DETC_BIG_Y_3	0x0264	W	0x00000000	XY detect, y boundary of big range
ISP_RAWAWB_5000_MULTIWINDOW_EXC_CTRL	0x02B8	W	0x00000000	The horizontal and vertical offset of multi-window
ISP_RAWAWB_5000_MULTIWINDOW0_OFFS	0x02BC	W	0x00000000	The horizontal and vertical offset of multi-window
ISP_RAWAWB_5000_MULTIWINDOW0_SIZE	0x02C0	W	0x00000000	The horizontal and vertical size of multi-window
ISP_RAWAWB_5000_MULTIWINDOW1_OFFS	0x02C4	W	0x00000000	The horizontal and vertical offset of multi-window
ISP_RAWAWB_5000_MULTIWINDOW1_SIZE	0x02C8	W	0x00000000	The horizontal and vertical size of multi-window
ISP_RAWAWB_5000_MULTIWINDOW2_OFFS	0x02CC	W	0x00000000	The horizontal and vertical offset of multi-window
ISP_RAWAWB_5000_MULTIWINDOW2_SIZE	0x02D0	W	0x00000000	The horizontal and vertical size of multi-window
ISP_RAWAWB_5000_MULTIWINDOW3_OFFS	0x02D4	W	0x00000000	The horizontal and vertical offset of multi-window
ISP_RAWAWB_5000_MULTIWINDOW3_SIZE	0x02D8	W	0x00000000	The horizontal and vertical size of multi-window

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Name	Offset	Size	Reset Value	Description
ISP_RAWAWB_5000_EXC_WP_REGION0_XU	0x02FC	W	0x00000000	The left and right boundary of exclude region in UV or XY range
ISP_RAWAWB_5000_EXC_WP_REGION0_YV	0x0300	W	0x00000000	The top and bottom boundary of exclude region in UV or XY range
ISP_RAWAWB_5000_EXC_WP_REGION1_XU	0x0304	W	0x00000000	The left and right boundary of exclude region in UV or XY range
ISP_RAWAWB_5000_EXC_WP_REGION1_YV	0x0308	W	0x00000000	The top and bottom boundary of exclude region in UV or XY range
ISP_RAWAWB_5000_EXC_WP_REGION2_XU	0x030C	W	0x00000000	The left and right boundary of exclude region in UV or XY range
ISP_RAWAWB_5000_EXC_WP_REGION2_YV	0x0310	W	0x00000000	The top and bottom boundary of exclude region in UV or XY range
ISP_RAWAWB_5000_EXC_WP_REGION3_XU	0x0314	W	0x00000000	The left and right boundary of exclude region in UV or XY range
ISP_RAWAWB_5000_EXC_WP_REGION3_YV	0x0318	W	0x00000000	The top and bottom boundary of exclude region in UV or XY range
ISP_RAWAWB_5000_EXC_WP_REGION4_XU	0x031C	W	0x00000000	The left and right boundary of exclude region in UV or XY range
ISP_RAWAWB_5000_EXC_WP_REGION4_YV	0x0320	W	0x00000000	The top and bottom boundary of exclude region in UV or XY range
ISP_RAWAWB_5000_EXC_WP_REGION5_XU	0x0324	W	0x00000000	The left and right boundary of exclude region in UV or XY range
ISP_RAWAWB_5000_EXC_WP_REGION5_YV	0x0328	W	0x00000000	The top and bottom boundary of exclude region in UV or XY range
ISP_RAWAWB_5000_EXC_WP_REGION6_XU	0x032C	W	0x00000000	The left and right boundary of exclude region in UV or XY range
ISP_RAWAWB_5000_EXC_WP_REGION6_YV	0x0330	W	0x00000000	The top and bottom boundary of exclude region in UV or XY range
ISP_RAWAWB_5000_EXC_WP_WEIGHT0_3	0x0334	W	0x3F3F3F3F	The top and bottom boundary of exclude region in UV or XY range
ISP_RAWAWB_5000_EXC_WP_WEIGHT4_6	0x0338	W	0x003F3F3F	The top and bottom boundary of exclude region in UV or XY range
ISP_RAWAWB_5000_SUM_RGAIN_NOR_0	0x0340	W	0x00000000	White point R-gain sum with Y-weight and block weight
ISP_RAWAWB_5000_SUM_BGAIN_NOR_0	0x0348	W	0x00000000	White point B-gain sum with Y-weight and block weight
ISP_RAWAWB_5000_WP_NUM_NOR_0	0x034C	W	0x00000000	White point sum number with Y-weight and block weight
ISP_RAWAWB_5000_SUM_RGAIN_BIG_0	0x0350	W	0x00000000	White point R-gain sum with Y-weight and block weight
ISP_RAWAWB_5000_SUM_BGAIN_BIG_0	0x0358	W	0x00000000	White point B-gain sum with Y-weight and block weight
ISP_RAWAWB_5000_WP_NUM_BIG_0	0x035C	W	0x00000000	White point sum number with Y-weight and block weight
ISP_RAWAWB_5000_SUM_RGAIN_NOR_1	0x0370	W	0x00000000	White point R-gain sum with Y-weight and block weight
ISP_RAWAWB_5000_SUM_BGAIN_NOR_1	0x0378	W	0x00000000	White point B-gain sum with Y-weight and block weight
ISP_RAWAWB_5000_WP_NUM_NOR_1	0x037C	W	0x00000000	White point sum number with Y-weight and block weight
ISP_RAWAWB_5000_SUM_RGAIN_BIG_1	0x0380	W	0x00000000	White point R-gain sum with Y-weight and block weight
ISP_RAWAWB_5000_SUM_BGAIN_BIG_1	0x0388	W	0x00000000	White point B-gain sum with Y-weight and block weight

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Name	Offset	Size	Reset Value	Description
ISP_RAWAWB_5000_WP_NUM_BIG_1	0x038C	W	0x00000000	White point sum number with Y-weight and block weight
ISP_RAWAWB_5000_SUM_RGAIN_NOR_2	0x03A0	W	0x00000000	White point R-gain sum with Y-weight and block weight
ISP_RAWAWB_5000_SUM_BGAIN_NOR_2	0x03A8	W	0x00000000	White point B-gain sum with Y-weight and block weight
ISP_RAWAWB_5000_WP_NUM_NOR_2	0x03AC	W	0x00000000	White point sum number with Y-weight and block weight
ISP_RAWAWB_5000_SUM_RGAIN_BIG_2	0x03B0	W	0x00000000	White point R-gain sum with Y-weight and block weight
ISP_RAWAWB_5000_SUM_BGAIN_BIG_2	0x03B8	W	0x00000000	White point B-gain sum with Y-weight and block weight
ISP_RAWAWB_5000_WP_NUM_BIG_2	0x03BC	W	0x00000000	White point sum number with Y-weight and block weight
ISP_RAWAWB_5000_SUM_RGAIN_NOR_3	0x03D0	W	0x00000000	White point R-gain sum with Y-weight and block weight
ISP_RAWAWB_5000_SUM_BGAIN_NOR_3	0x03D8	W	0x00000000	White point B-gain sum with Y-weight and block weight
ISP_RAWAWB_5000_WP_NUM_NOR_3	0x03DC	W	0x00000000	White point sum number with Y-weight and block weight
ISP_RAWAWB_5000_SUM_BGAIN_BIG_3	0x03E0	W	0x00000000	White point B-gain sum with Y-weight and block weight
ISP_RAWAWB_5000_SUM_RGAIN_BIG_3	0x03E8	W	0x00000000	White point R-gain sum with Y-weight and block weight
ISP_RAWAWB_5000_WP_NUM_BIG_3	0x03EC	W	0x00000000	White point sum number with Y-weight and block weight
ISP_RAWAWB_5000_SUM_R_EXC_0	0x05E0	W	0x00000000	R-gain sum in the exclude range
ISP_RAWAWB_5000_SUM_B_EXC_0	0x05E8	W	0x00000000	B-gain sum in the exclude range
ISP_RAWAWB_5000_WP_NM_EXC_0	0x05EC	W	0x00000000	White point in the exclude range
ISP_RAWAWB_5000_SUM_R_EXC_1	0x05F0	W	0x00000000	R-gain sum in the exclude range
ISP_RAWAWB_5000_SUM_B_EXC_1	0x05F8	W	0x00000000	B-gain sum in the exclude range
ISP_RAWAWB_5000_WP_NM_EXC_1	0x05FC	W	0x00000000	White point in the exclude range
ISP_RAWAWB_5000_SUM_R_EXC_2	0x0600	W	0x00000000	R-gain sum in the exclude range
ISP_RAWAWB_5000_SUM_B_EXC_2	0x0608	W	0x00000000	B-gain sum in the exclude range
ISP_RAWAWB_5000_WP_NM_EXC_2	0x060C	W	0x00000000	White point in the exclude range
ISP_RAWAWB_5000_SUM_R_EXC_3	0x0610	W	0x00000000	R-gain sum in the exclude range
ISP_RAWAWB_5000_SUM_B_EXC_3	0x0618	W	0x00000000	B-gain sum in the exclude range
ISP_RAWAWB_5000_WP_NM_EXC_3	0x061C	W	0x00000000	White point in the exclude range
ISP_RAWAWB_5000_Y_HIST01	0x0620	W	0x00000000	Y HIST bin
ISP_RAWAWB_5000_Y_HIST23	0x0624	W	0x00000000	Y HIST bin

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Name	Offset	Size	Reset Value	Description
ISP_RAWAWB_5000_Y_HIST45	0x0628	W	0x00000000	Y HIST bin
ISP_RAWAWB_5000_Y_HIST67	0x062C	W	0x00000000	Y HIST bin
ISP_RAWAWB_5000_WPNUM2_0	0x0630	W	0x00000000	White pixel num2
ISP_RAWAWB_5000_WPNUM2_1	0x0634	W	0x00000000	White pixel num2
ISP_RAWAWB_5000_WPNUM2_2	0x0638	W	0x00000000	White pixel num2
ISP_RAWAWB_5000_WPNUM2_3	0x063C	W	0x00000000	White pixel num2
ISP_RAWAWB_5000_WRAM_CTRL	0x0654	W	0x00000000	Control of BLK weight ram
ISP_RAWAWB_5000_WRAM_DATA_BASE	0x0660	W	0x00000000	The Weight of BLK system. The user will always configure this base address 45 times for 15x15 weights

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

44.4.1.32 RAWHIST

Operational Base

Name	Base Address
RAWHIST_BIG	0x21D04800
RAWHIST0_BIG	0x21D04900

Name	Offset	Size	Reset Value	Description
ISP_RAWHIST_BIG_4800_4900_CTRL	0x0000	W	0x20000000	Histogram properties
ISP_RAWHIST_BIG_4800_4900_SIZE	0x0004	W	0x00000000	Horizontal (sub-)window size
ISP_RAWHIST_BIG_4800_4900_OFFS	0x0008	W	0x00000000	Histogram window horizontal offset
ISP_RAWHIST_BIG_4800_4900_HRAM_CTRL	0x000C	W	0x00000000	HRAM address offset
ISP_RAWHIST_BIG_4800_4900_RAW2Y_CC	0x0010	W	0x000D2021	The offset of RAW2Y formula
ISP_RAWHIST_BIG_4800_4900_WRAM_CTRL	0x0014	W	0x00000000	RAM offset for write or read
ISP_RAWHIST_BIG_4800_4900_WEIGHT_BASE	0x0040	W	0x20820820	Weighting factor for sub-windows total 25 factor
ISP_RAWHIST_BIG_4800_4900_RO_BASE_BIN	0x0080	W	0x00000000	Histogram measurement result bin 0..255(total 256)

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

44.4.1.33 IE_CMSK

Name	Offset	Size	Reset Value	Description
IMG_EFF_0200_IMG_EFF_CTRL	0x0000	W	0x00000000	Img_eff_ctrl

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

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44.4.1.34 CPROC

Name	Offset	Size	Reset Value	Description
CPROC_0800_CTRL	0x0000	W	0x00000000	Global control register
CPROC_0800_CONTRAST	0x0004	W	0x00000080	Color Processing contrast register
CPROC_0800_BRIGHTNESS	0x0008	W	0x00000000	Color Processing brightness register
CPROC_0800_SATURATION	0x000C	W	0x00000080	Color Processing saturation register
CPROC_0800_HUE	0x0010	W	0x00000000	Color Processing hue register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

44.4.1.35 MPFBC

Name	Offset	Size	Reset Value	Description
ISP_MPFBC_18C0_CTRL	0x0000	W	0x00000E02	MPFBC control

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

44.4.1.36 3A_COMMON

Name	Offset	Size	Reset Value	Description
COMMON3A_W3A_CTRL0	0x0000	W	0x00000000	The main control register of W3A
COMMON3A_W3A_CTRL1	0x0004	W	0x00000F00	The control register of W3A
COMMON3A_W3A_INT_EN	0x0010	W	0x00000000	The interrupt enable register of W3A
COMMON3A_W3A_INT_STAT	0x0014	W	0x00000000	The interrupt raw status register of W3A
COMMON3A_W3A_MASK_INT_STAT	0x0018	W	0x00000000	The interrupt mask status register of W3A
COMMON3A_W3A_AEBIG_ADDR	0x0020	W	0x00000000	The AEBIG addr
COMMON3A_W3A_AECH0_ADDR	0x0024	W	0x00000000	The AECH0 addr
COMMON3A_W3A_AF_ADDR	0x0030	W	0x00000000	The AF addr
COMMON3A_W3A_AWB_ADDR	0x0034	W	0x00000000	The AWB addr
COMMON3A_W3A_PDAF_ADDR	0x0038	W	0x00000000	The PDAF addr
COMMON3A_W3A_AEBIG_ADDR_SHD	0x0040	W	0x00000000	The AEBIG shadow addr
COMMON3A_W3A_AE0_ADDR_SHD	0x0044	W	0x00000000	The AECH0 shadow addr
COMMON3A_W3A_AF_ADDR_SHD	0x0050	W	0x00000000	The AF shadow addr
COMMON3A_W3A_AWB_ADDR_SHD	0x0054	W	0x00000000	The AWB shadow addr
COMMON3A_W3A_PDAF_ADDR_SHD	0x0058	W	0x00000000	The PDAF shadow addr
COMMON3A_VI3A_CTRL0	0x0080	W	0x0000000C	The main control register of VI3A
COMMON3A_VI3A_CTRL1	0x0084	W	0x00000000	The control register of VI3A
COMMON3A_VI3A_INT_EN	0x0090	W	0x00000000	The interrupt enable register of VI3A

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Name	Offset	Size	Reset Value	Description
COMMON3A_VI3A_INT_STAT	0x0094	W	0x00000000	The interrupt raw status register of W3A
COMMON3A_VI3A_MASK_INT_STAT	0x0098	W	0x00000000	The interrupt mask status register of W3A
COMMON3A_VI3A_BLS_FIXED_0	0x00A0	W	0x00020001	The BLS parameter of VI3A
COMMON3A_VI3A_BLS_FIXED_1	0x00A4	W	0x00040003	The BLS parameter of VI3A
COMMON3A_VI3A_GAIN_0	0x00A8	W	0x01020101	The GAIN parameter of VI3A
COMMON3A_VI3A_GAIN_1	0x00AC	W	0x01040103	The GAIN parameter of VI3A
COMMON3A_W3A_FE_INT_EN	0x00C0	W	0x00000000	The interrupt enable register of W3A front end
COMMON3A_W3A_FE_INT_STAT	0x00C4	W	0x00000000	The interrupt raw status register of W3A front end
COMMON3A_W3A_FE_MASK_INT_STAT	0x00C8	W	0x00000000	The interrupt mask status register of W3A front end
COMMON3A_W3A_DBG0	0x00F0	W	0x00000000	The debug message of W3A

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

44.4.1.37 AI

Name	Offset	Size	Reset Value	Description
ISP_AI_1200_CTRL	0x0000	W	0x00000010	Control register
ISP_AI_1200_SIGMA_Y0	0x0010	W	0x000D000B	Y0 group of sigma-curve table
ISP_AI_1200_SIGMA_Y1	0x0014	W	0x000D000B	Y1 group of sigma-curve table
ISP_AI_1200_SIGMA_Y2	0x0018	W	0x000D000B	Y2 group of sigma-curve table
ISP_AI_1200_SIGMA_Y3	0x001C	W	0x000D000B	Y3 group of sigma-curve table
ISP_AI_1200_SIGMA_Y4	0x0020	W	0x000D000B	Y4 group of sigma-curve table
ISP_AI_1200_SIGMA_Y5	0x0024	W	0x000D000B	Y5 group of sigma-curve table
ISP_AI_1200_SIGMA_Y6	0x0028	W	0x000D000B	Y6 group of sigma-curve table
ISP_AI_1200_SIGMA_Y7	0x002C	W	0x000D000B	Y7 group of sigma-curve table
ISP_AI_1200_SIGMA_Y8	0x0030	W	0x000D000B	Y8 group of sigma-curve table
ISP_AI_1200_SIGMA_Y9	0x0034	W	0x000D000B	Y9 group of sigma-curve table
ISP_AI_1200_SIGMA_Y10	0x0038	W	0x000D000B	Y10 group of sigma-curve table
ISP_AI_1200_SIGMA_Y11	0x003C	W	0x000D000B	Y11 group of sigma-curve table
ISP_AI_1200_SIGMA_Y12	0x0040	W	0x000D000B	Y12 group of sigma-curve table
ISP_AI_1200_SIGMA_Y13	0x0044	W	0x000D000B	Y13 group of sigma-curve table
ISP_AI_1200_SIGMA_Y14	0x0048	W	0x000D000B	Y14 group of sigma-curve table
ISP_AI_1200_SIGMA_Y15	0x004C	W	0x000D000B	Y15 group of sigma-curve table
ISP_AI_1200_SIGMA_Y16	0x0050	W	0x0000000D	Y16 group of sigma-curve table
ISP_AI_1200_AIPRE_NL_WR_BASE	0x0054	W	0x00000000	Nlinear ddr wr base
ISP_AI_1200_AIPRE_NL_WR_STRIDE	0x0058	W	0x00000000	Nlinear ddr wr stride
ISP_AI_1200_AIPRE_GAIN_WR_BASE	0x005C	W	0x00000000	AIPRE gain ddr wr base
ISP_AI_1200_AIPRE_GAIN_WR_STRIDE	0x0060	W	0x00000000	AIPRE gain ddr wr stride
ISP_AI_1200_AIPRE_NL_PRE	0x0064	W	0x00000000	AIPRE nlinear parameter

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Name	Offset	Size	Reset Value	Description
ISP_AI_1200_AIPRE_GAIN_PARA	0x0068	W	0x00000000	AIPRE gain parameter
ISP_AI_1200_AIPRE_SIGMA_CURVE0	0x006C	W	0x00000000	Y0 group of nlinear sigma-curve table
ISP_AI_1200_AIPRE_SIGMA_CURVE1	0x0070	W	0x00000000	Y1 group of nlinear sigma-curve table
ISP_AI_1200_AIPRE_SIGMA_CURVE2	0x0074	W	0x00000000	Y2 group of nlinear sigma-curve table
ISP_AI_1200_AIPRE_SIGMA_CURVE3	0x0078	W	0x00000000	Y3 group of nlinear sigma-curve table
ISP_AI_1200_AIPRE_SIGMA_CURVE4	0x007C	W	0x00000000	Y4 group of nlinear sigma-curve table
ISP_AI_1200_AIPRE_SIGMA_CURVE5	0x0080	W	0x00000000	Y5 group of nlinear sigma-curve table
ISP_AI_1200_AIPRE_SIGMA_CURVE6	0x0084	W	0x00000000	Y6 group of nlinear sigma-curve table
ISP_AI_1200_AIPRE_SIGMA_CURVE7	0x0088	W	0x00000000	Y7 group of nlinear sigma-curve table
ISP_AI_1200_AIPRE_SIGMA_CURVE8	0x008C	W	0x00000000	Y8 group of nlinear sigma-curve table
ISP_AI_1200_AIPRE_SIGMA_CURVE9	0x0090	W	0x00000000	Y9 group of nlinear sigma-curve table
ISP_AI_1200_AIPRE_SIGMA_CURVE10	0x0094	W	0x00000000	Y10 group of nlinear sigma-curve table
ISP_AI_1200_AIPRE_NOISE0	0x0098	W	0x00000000	AIPRE noise parameter group0
ISP_AI_1200_AIPRE_NOISE1	0x009C	W	0x00000000	AIPRE noise parameter group1
ISP_AI_1200_AIPRE_NOISE2	0x00A0	W	0x00000000	AIPRE noise parameter group2

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

44.4.1.38 RGBIR

Name	Offset	Size	Reset Value	Description
RGBIR_EN	0x0000	W	0x00000000	The enable of RGBIR
RGBIR_THETA	0x0004	W	0x00000000	The coefficient of RGBIR -- theta
RGBIR_DELTA	0x0008	W	0x00000004	The coefficient of RGBIR -- delta
RGBIR_SCALE0	0x000C	W	0x0000007B	The scale weight of channel 0
RGBIR_SCALE1	0x0010	W	0x00000073	The scale weight of channel 1
RGBIR_SCALE2	0x0014	W	0x00000072	The scale weight of channel 2
RGBIR_SCALE3	0x0018	W	0x00000079	The scale weight of channel 3
RGBIR_LUMA_POINT0	0x001C	W	0x330CA320	The luma point 0 1 2 of the curve
RGBIR_LUMA_POINT1	0x0020	W	0x348D0338	The luma point 3 4 5 of the curve
RGBIR_LUMA_POINT2	0x0024	W	0x390DC350	The luma point 6 7 8 of the curve
RGBIR_LUMA_POINT3	0x0028	W	0x3D8F43B0	The luma point 9 10 11 of the curve
RGBIR_LUMA_POINT4	0x002C	W	0x3F0FA3E0	The luma point 12 13 14 of the curve
RGBIR_LUMA_POINT5	0x0030	W	0x001003F8	The luma point 15 16 of the curve
RGBIR_SCALE_MAP0	0x0034	W	0x03D5FB00	The scale map 0 1 2 of the curve
RGBIR_SCALE_MAP1	0x0038	W	0x030DAEE8	The scale map 3 4 5 of the curve
RGBIR_SCALE_MAP2	0x003C	W	0x007CAEAD	The scale map 6 7 8 of the curve

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Name	Offset	Size	Reset Value	Description
RGBIR_SCALE_MAP3	0x0040	W	0x00040208	The scale map 9 10 11 of the curve
RGBIR_SCALE_MAP4	0x0044	W	0x00000001	The scale map 12 13 14 of the curve
RGBIR_SCALE_MAP5	0x0048	W	0x00000000	The scale map 15 16 of the curve

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access, **DW**-Double WORD (64 bits) access*

44.4.2 Detail Registers Description

44.4.2.1 MIPI

CSI2RX_1C00_CTRL0

Address: Operational Base(0x21D01C00) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:12	RW	0x0	sw_dma_2frm_mode Raw read back two/three frames mode, only the last frame valid 2'b00: Normal one frame mode 2'b01: Two frame mode 2'b10: Three frame mode 2'b11: Reserved
11:8	RW	0x0	sw_ibuf_op_mode 4'h0: Normal_mode (no hdr). 4'h4: Raw_rdback_frame1(start use sw_dma_rdback_p) 4'h5: Hdr_rdback_frame2 (start use sw_dma_rdback_p) 4'h6: Hdr_rdback_frame3 (start use sw_dma_rdback_p) 4'h8: Hdr_frame_linex2_ddr_mode 4'h12: Hdr_frame_linex3_ddr_mode Others: Reserved
7	RW	0x0	sw_ibuf_op_frame_stmode Op_mode=8,12 framex2/x3 start mode 1'b0: RawS frame_st then start 1'b1: RawM/L frame_end then start
6:2	RO	0x00	reserved
1	RW	0x0	sw_csi_2pix_dis Ibuf in and out pixel mode 1'b1: One pixel mode 1'b0: Two pixel mode
0	RW	0x0	sw_csi2rx_en_p Csi rx read enable under hdr debug mode, auto-clear Note: CTRL0[0] read back is mipi readback working

CSI2RX_1C00_CTRL1

Address: Operational Base(0x21D01C00) + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	ro_csi2rx_enable Mipi mode enable (~sw_dvp_mode)
29:28	RW	0x0	sw_ibuf_lvl1_sel2 Ibuf2_m select 2'b00: Ibuf2_m_i 2'b01: Ibuf1_l_i 2'b10: Ibuf0_s_i

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Bit	Attr	Reset Value	Description
27:26	RW	0x0	sw_ibuf_lvl1_sel1 Ibuf1_l select 2'b00: Ibuf1_l_i 2'b01: Ibuf0_s_i 2'b10: Ibuf2_m_i
25:24	RW	0x0	sw_ibuf_lvl1_sel0 Ibuf0_s select 2'b00: Ibuf0_s_i 2'b01: Ibuf1_l_i 2'b10: Ibuf2_m_i
23	RW	0x0	sw_ibuf_lvl0_sel3 Ibuf3_r_i select 1'b0: Csi0_mipi[chan3_sel] 1'b1: Raw2_mipi(from DDR)
22	RW	0x0	sw_ibuf_lvl0_sel2 Ibuf2_l_i select 1'b0: Csi0_mipi[chan2_sel] 1'b1: Raw1_mipi(from DDR)
21	RW	0x0	sw_ibuf_lvl0_sel1 Ibuf1_l_i select 1'b0: Csi0_mipi[chan1_sel] 1'b1: Raw0_mipi(from DDR)
20	RW	0x0	sw_ibuf_lvl0_sel0 Ibuf0_s_i select 1'b0: Csi0_mipi[chan0_sel] 1'b1: Csi1_mipi[chan0_sel]
19	RO	0x0	reserved
18:16	RW	0x3	sw_csi_chan3_sel Csi0_mipi[7:0] chan3 select
15	RO	0x0	reserved
14:12	RW	0x2	sw_csi_chan2_sel Csi0_mipi[7:0] chan2 select
11	RO	0x0	reserved
10:8	RW	0x1	sw_csi_chan1_sel Csi0_mipi[7:0] chan1 select
7	RO	0x0	reserved
6:4	RW	0x0	sw_csi_chan0_sel Csi0_mipi[7:0] + csi1_mipi[7:0] chan0 select
3:2	RO	0x0	reserved
1:0	RW	0x3	sw_csi_lane Number of active data lanes 2'b00: 1 data lane (lane 0) 2'b01: 2 data lanes (lanes 0 and 1) 2'b10: 3 data lanes (lanes 0, 1, and 2) 2'b11: 4 data lanes (All) Can only be updated when the D-PHY lane is in Stop state. Value after Reset: CSI2_HOST_NUMBER_OF_LANES-1 = 0x3

CSI2RX_1C00_CTRL2

Address: Operational Base(0x21D01C00) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_ibuf_hblank_count Mipi in buffer horizontal blank counter
23:20	RW	0x0	sw_rdbak_hold_diff Raw readback hold diff value for pipeline full

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Bit	Attr	Reset Value	Description
19:14	RO	0x00	reserved
13:0	RW	0x0000	sw_csi_isp_linecnt Isp line counter reach interrupt for ro_err3[15]

CSI2RX_1C00_CTRL3

Address: Operational Base(0x21D01C00) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_ibuf_hold_watermark HDR input buffer hold watermark. For ddr read hold, to control read rate. For example, image resolution 1920x1080, configure sw_ibuf_hold_watermark = 1920 / 2 = 960. Note: sw_ibuf_hold_watermark Only used in hdr line mode, otherwise default sw_ibuf_hold_watermark = 0.

CSI2RX_1C00_CSI2_RESETN

Address: Operational Base(0x21D01C00) + offset (0x0010)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_csi_delete_2pix_dis Disable delete mipi_hsync for invalid 2pixel at line end
30:2	RO	0x00000000	reserved
1	R/WSC	0x1	sw_csi_fifo_clr_n Fifo clear. Active Low. Auto-clear Write then clear
0	R/WSC	0x1	sw_csi_rxbyte_rst_n Reset output. Active Low. Auto-clear Write then clear

CSI2RX_1C00_DATA_IDS_1

Address: Operational Base(0x21D01C00) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x2b	sw_csi_id0 Data ID 0 [dt0_vc[1:0], dt0_dt[5:0]] Channel 0

CSI2RX_1C00_ERR_OVERFLOW

Address: Operational Base(0x21D01C00) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19	RC	0x0	ibuf3r_overflow Ibuf_r_fifo overflow
18:16	RC	0x0	ibufx3_overflow Ibufx3 overflow [0]: ibuf_s_fifo overflow [1]: ibuf_l_fifo overflow [2]: ibuf_m_fifo overflow
15	RO	0x0	reserved
14	RC	0x0	afifo22_overflow Afifo22 overflow
13	RC	0x0	afifo21_overflow Afifo21 overflow

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Bit	Attr	Reset Value	Description
12	RC	0x0	afifo20_overflow Afifo20 overflow
11:0	RO	0x000	reserved

CSI2RX_1C00_ERR_STAT

Address: Operational Base(0x21D01C00) + offset (0x002C)

Bit	Attr	Reset Value	Description
31	RW	0x0	mipi_drop_frm Mipi drop frame state
30:17	RO	0x0000	reserved
16	RC	0x0	mipi_linecnt Line counter number reach the sw_csi_isp_linecnt
15:7	RO	0x000	reserved
6	RC	0x0	raw2_rd_frame_end Raw2 read data frame end
5	RC	0x0	raw1_rd_frame_end Raw1 read data frame end
4	RC	0x0	raw0_rd_frame_end Raw0 read data frame end
3:0	RO	0x0	reserved

CSI2RX_1C00_MASK_OVERFLOW

Address: Operational Base(0x21D01C00) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19	RW	0x0	sw_imsk_ibuf3r_overflow Mask for ibuf_r_fifo overflow
18:16	RW	0x0	sw_imsk_ibufx3_overflow Mask for ibufx3 overflow [0]: ibuf_s_fifo overflow [1]: ibuf_l_fifo overflow [2]: ibuf_m_fifo overflow
15	RO	0x0	reserved
14	RW	0x0	sw_imsk_afifo22_overflow Mask for afifo22 overflow
13	RW	0x0	sw_imsk_afifo21_overflow Mask for afifo21 overflow
12	RW	0x0	sw_imsk_afifo20_overflow Mask for afifo20 overflow
11:0	RO	0x000	reserved

CSI2RX_1C00_MASK_STAT

Address: Operational Base(0x21D01C00) + offset (0x003C)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_imsk_mipi_drop_frm Mask for mipi drop frame state
30:17	RO	0x0000	reserved
16	RW	0x0	sw_imsk_csi_isp_linecnt Mask for line counter number reach the sw_csi_isp_linecnt
15:7	RO	0x000	reserved
6	RW	0x0	sw_imsk_raw2_rd_frame_end Mask for raw2_rd data frame_end
5	RW	0x0	sw_imsk_raw1_rd_frame_end Mask for raw_rd1 data frame_end

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Bit	Attr	Reset Value	Description
4	RW	0x0	sw_imsk_raw0_rd_frame_end Mask for raw_rd0 data frame_end
3:0	RO	0x0	reserved

CSI2RX_1C00_RAW_RD_CTRL

Address: Operational Base(0x21D01C00) + offset (0x0080)

Bit	Attr	Reset Value	Description
31	W1C	0x0	sw_rxself_force_upd Raws mipi rx self force update Note: If readback this register, it's mipi working.
30	RW	0x0	sw_rx0self_force_upd Rx0 self force update Note: If readback this register, it's mipi working.
29:8	RO	0x000000	reserved
7:5	RW	0x0	sw_csi_raw_rd_chan_sel Raw_rd sw_csi_id_7to0 id input id select, default id0
4	RW	0x0	sw_csi_raw_rd_align Raw_rd pix-out align mode 1'b0: big-endian 1'b1: little-endian
3	RW	0x0	sw_csi_raw_rd_uncompact Raw_rd pix-out simg_mod enable
2	RW	0x0	sw_csi_raw2_rd_en_org Raw_rd1 enable Auto clear when finish
1	RW	0x0	sw_csi_raw1_rd_en_org Raw_rd1 enable Auto clear when finish
0	RW	0x0	sw_csi_raw0_rd_en_org Raw_rd0 enable Auto clear when finish

CSI2RX_1C00_RAW_RD_LINECNT_RO

Address: Operational Base(0x21D01C00) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_raw1_rd_isp_line_cnt Current raw_rd1 to isp line counter
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_raw0_rd_isp_line_cnt Current raw_rd0 to isp line counter

CSI2RX_1C00_RAW_RD_PIC_SIZE

Address: Operational Base(0x21D01C00) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_csi_raw_rd_v_size_org If (sw_csi_raw_rd_v_size_org equal 0), use regs_acq_v_size value.
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_csi_raw_rd_h_size_org If (sw_csi_raw_rd_h_size_org equal 0), use regs_acq_h_size value.

CSI2RX_1C00_RAW2_RD_LINECNT_RO

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Address: Operational Base(0x21D01C00) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	ro_raw2_rd_isp_line_cnt Current raw2_rd to isp line counter

CSI2RX_1C00_ISP_LINECNT_RO

Address: Operational Base(0x21D01C00) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	ro_csi_isp_line_cnt Current csi to isp line counter

CSI2RX_1C00_RAW_WR_IBUF_STATUS_RO

Address: Operational Base(0x21D01C00) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RO	0x000000	ro_ibuf3_debug_status ibuf working debug status, mipi_clk

CSI2RX_1C00_FPN_CTRL

Address: Operational Base(0x21D01C00) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:2	RW	0x0	sw_fpn_bits Calculate data bits selection 2'b00: [3'b000, x] 2'b01: [2'b00, x, 1'b0] 2'b10: [1'b0, x, 2'b00] 2'b11: [x, 3'b000] Note: "x" is 4 bits data, frame FPN_TABLE_DATA
1	RW	0x0	sw_cfpn_n Column fpn enable, active low 1'b0: Col fpn 1'b1: Row fpn
0	RW	0x0	sw_fpn_en FPN enable 1'b0: Disable 1'b1: Enable

CSI2RX_1C00_FPN_TABLE_CTRL

Address: Operational Base(0x21D01C00) + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x1	sw_fpn_cfg_ing Write fpn data to memory, active high 1'b0: Disable/finish configuration 1'b1: Write table data to memory enable

CSI2RX_1C00_FPN_TABLE_DATA0

Address: Operational Base(0x21D01C00) + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_fpn0_table_data FPN data register to memory

CSI2RX_1C00_FPN_TABLE_DATA1

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Address: Operational Base(0x21D01C00) + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_fpn1_table_data FPN data register to memory

CSI2RX_1C00_VERSION

Address: Operational Base(0x21D01C00) + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:0	RO	0x02013323	version_id Version of the DWC_mipi_csi2_host Value after Reset: 32'h02013323 Integrated in ISP (max: 02, min: 01, svn: 23323)

44.4.2.2 MMU

MMU_DTE_ADDR

Address: Operational Base(0x21D07F00) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_dte_addr MMU current page Table address

MMU_STATUS

Address: Operational Base(0x21D07F00) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:6	RO	0x00	page_fault_bus_id Index of master reponsible for last page fault.
5	RO	0x0	page_fault_is_write The direction of access for last page fault 1'b0: Read 1'b1: Write
4	RO	0x0	replay_buffer_empty The MMU replay buffer is empty
3	RO	0x0	mmu_idle The MMU is idle when accesses are being translated and there are no unfinished translated accesses
2	RO	0x0	stail_active MMU stall mode currently enabled. The mode is enabled by command
1	RO	0x0	page_fault_active MMU page fault mode currently enabled . The mode is enabled by command
0	RO	0x0	paging_enabled Paging is enabled

MMU_COMMAND

Address: Operational Base(0x21D07F00) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved

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Bit	Attr	Reset Value	Description
2:0	WO	0x0	mmu_cmd MMU_CMD. This can be 3'b000: MMU_ENABLE_PAGING 3'b001: MMU_DISABLE_PAGING 3'b010: MMU_ENABLE_STALL 3'b011: MMU_DISABLE_STALL 3'b100: MMU_ZAP_CACHE 3'b101: MMU_PAGE_FAULT_DONE 3'b110: MMU_FORCE_RESET

MMU_PAGE_FAULT_ADDR

Address: Operational Base(0x21D07F00) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	page_fault_addr Address of last page fault.

MMU_ZAP_ONE_LINE

Address: Operational Base(0x21D07F00) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	mmu_zap_one_line Address to be invalidated from the page table cache.

MMU_INT_RAWSTAT

Address: Operational Base(0x21D07F00) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error Read bus error
0	RW	0x0	page_fault Page fault

MMU_INT_CLEAR

Address: Operational Base(0x21D07F00) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	WO	0x0	read_bus_error Read bus error
0	WO	0x0	page_fault Page fault

MMU_INT_MASK

Address: Operational Base(0x21D07F00) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RW	0x0	read_bus_error Read bus error
0	RW	0x0	page_fault Page fault

MMU_INT_STATUS

Address: Operational Base(0x21D07F00) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	read_bus_error Read bus error

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Bit	Attr	Reset Value	Description
0	RO	0x0	page_fault Page fault

MMU_AUTO_GATING

Address: Operational Base(0x21D07F00) + offset (0x0024)

Bit	Attr	Reset Value	Description
31	RW	0x1	sw_mmu_old_en mmu old version enable, need set 1.
30:1	RO	0x00000000	reserved
0	RW	0x0	mmu_auto_gating When it is 1'b1, the mmu will auto gating it self.

44.4.2.3 MI

MI_1400_MI_WR_CTRL

Address: Operational Base(0x21D01400) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RW	0x2	sw_sp_wr_output_format Selects output format of self picture. For possible restrictions see sub-chapter "Picture Orientation" in chapter "Self Path Output Programming". 3'b111: RGB 888 3'b110: ARGB 888 3'b101: RGB 666 3'b100: RGB 565 3'b011: YCbCr 4:4:4 3'b010: YCbCr 4:2:2 3'b001: YCbCr 4:2:0 3'b000: YCbCr 4:0:0 Note: - Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path. - For RGB output format the SP input format must be YCbCr 4:2:2 -For ARGB888 format, Alpha is configurable (15f8[23:16]). - If sw_sp_wr_v_flip = 1 and yuv420 format, need to configure sw_sp_wr_output_format = 1.
27:26	RW	0x0	sw_sp_wr_input_format Selects input format of self picture. For possible restrictions see sub-chapter "Picture Orientation" in chapter "Self Path Output Programming". 2'b11: YCbCr 4:4:4 2'b10: YCbCr 4:2:2 2'b01: YCbCr 4:2:0 2'b00: YCbCr 4:0:0 Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path.

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Bit	Attr	Reset Value	Description
25:24	RW	0x0	sw_sp_wr_format Defines how YCbCr self picture data is written to memory. Must be set to 00 if RGB conversion is active. Note that with RGB conversion active the output format is always interleaved. 2'b00: Reserved 2'b01: Semi planar, for YCbCr 4:2:x 2'b10: Interleaved (combined), for YCbCr 4:2:2 only 2'b11: Reserved Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path.
23:22	RW	0x0	sw_mp_wr_format Defines how YCbCr main picture data is written to memory. 2'b00: Reserved 2'b01: Semi planar, for YCbCr 4:2:x 2'b10: Interleaved (combined), for YCbCr 4:2:2 only 2'b11: Reserved Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the main path.
21	RW	0x0	sw_mi_wr_init_offset_en Enables updating of the offset counters shadow registers for raw path to the programmed register initial values. The update will be executed either when a forced software update occurs (in register MI_INIT bit cfg_upd = 1) or when an automatic configuration update signal arrives at the MI input port. The latter is split into raw picture. So only the corresponding raw shadow registers are affected. After a picture skip has been performed init_offset_en selects between skip restart and skip initial mode (see bit skip in register MI_INIT).
20	RW	0x0	sw_mi_wr_init_base_en Enables updating of the base address and buffer size shadow registers for main and self picture to the programmed register initial values. MI_MP/SP_Y/CB/CR_BASE_AD_INIT -> MI_MP/SP_Y/CB/CR_BASE_AD_SHD MI_MP/SP_Y/CB/CR_SIZE_INIT -> MI_MP/SP_Y/CB/CR_SIZE_SHD The update will be executed either when a forced software update occurs (in register MI_INIT bit cfg_upd = 1) or when an automatic configuration update signal arrives at the MI input port. The latter is split into main and self picture. So only the corresponding main/self shadow registers are affected.
19:18	RW	0x2	sw_mi_wr_burst_len_chrom_org Burst length for Cb or Cr data affecting write port. 2'b00: 4-beat bursts 2'b01: 8-beat bursts 2'b10: 16-beat bursts 2'b11: Reserved Ignored if 8- or 16-beat bursts are not supported. If rotation is active, then only 4-beat bursts will be generated in self path, regardless of the setting here. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the main and self path.

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Bit	Attr	Reset Value	Description
17:16	RW	0x2	sw_mi_wr_burst_len_lum_org Burst length for Y data affecting write port. 2'b00: 4-beat bursts 2'b01: 8-beat bursts 2'b10: 16-beat bursts 2'b11: Reserved Ignored if 8- or 16-beat bursts are not supported. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the main and self path.
15	RW	0x0	sw_mi_wr_last_pixel_sig_en Enables the last pixel signalization 1'b1: Enabled 1'b0: Disabled
14	RW	0x0	sw_sp_wr_auto_upd Automatic update of configuration registers for self path at frame end. 1'b1: Enabled 1'b0: Disabled
13	RW	0x0	sw_mp_wr_auto_upd Automatic update of configuration registers for main path at frame end. 1'b1: Enabled 1'b0: Disabled Note: If mp pingpong enable, it needs to be set "1".
12	RW	0x0	sw_sp_wr_pingpong_en Pingpong mode of configuration registers for self path at frame end. 1'b1: Enabled 1'b0: Disabled
11	RW	0x0	sw_mp_wr_pingpong_en Pingpong mode of configuration registers for main path at frame end. 1'b1: Enabled 1'b0: Disabled
10	RW	0x0	sw_mi_wr_422noncosited Enables self path YCbCr422non-co-sited -> YCbCr444 interpolation (M5_v6, M5_v7 only) 1'b1: YCbCr422 data are non_co-sited (Cb and Cr samples are centered between Y samples) so modified interpolation is activated 1'b0: YCbCr422 data are co-sited (Y0 Cb0 and Cr0 are sampled at the same position) Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path.
9	RW	0x0	sw_mi_wr_cbcr_full_range Enables CbCr full range for self path YCbCr -> RGB conversion (M5_v6, M5_v7 only) 1'b1: CbCr have full range (0..255) 1'b0: CbCr have compressed range range (16..240) Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path.

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Bit	Attr	Reset Value	Description
8	RW	0x0	sw_mi_wr_y_full_range Enables Y full range for self path YCbCr -> RGB conversion (M5_v6, M5_v7 only) 1'b1: Y has full range (0..255) 1'b0: Y has compressed range (16..235) Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path.
7	RW	0x0	sw_mi_wr_byte_swap Enable uv swap function YVYU mode: 1'b0: YVYU (U,LSB) 1'b1: YUYV (V,LSB) YUV-SP mode: 1'b0: VU (U,LSB) 1'b1: UV (V,LSB)
6:4	RO	0x0	reserved
3:0	RW	0x0	sw_mi_wr_path_enable Enable data paths of MI according to the following table: 4'h0: Disabled, no data is transferred 4'h1: YUV data output, main-path only (mp_enable only) 4'h2: Self-path only, output data format depending on other settings (sp_enable only) 4'h3: YUV data output in main-path and self-path image data active 4'h4: JPEG data output, main-path only (jpeg_enable only) 4'h5: Not allowed 4'h6: JPEG data output in main-path and self-path image data active 4'h7: Not allowed 4'h8: RAW data output, main-path only (raw_enable only) 4'h9: Defect pixel data on self-path, image data on main-path 4'h10: Defect pixel data on main-path, image data on self-path 4'h11: Not allowed 4'h12: Defect pixel data on self-path, JPEG data on main-path 4'h13: Defect pixel data on main-path only 4'h14: Defect pixel data on self-path only 4'h15: Defect pixel data on self-path, RAW data on main-path Programmed value becomes effective (visible in shadow register) after a soft reset, a forced software update or an automatic configuration update. Affects MI_IN and MI_OUT module.

MI_1400_MI_WR_INIT

Address: Operational Base(0x21D01400) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6	RW	0x0	sw_mi_update_last_pixel_en If this bit set 1, MI IN and MI OUT module will update at the time of dual crop module sent out the last pixel
5	RW	0x1	sw_mi_update_mode 1'b0: Old mode 1'b1: New mode, all path will update when frame_end In new mode, all path registers of MI will be updated at right time; (Not support input RAW/JEPG mode)

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Bit	Attr	Reset Value	Description
4	W1C	0x0	sys_mi_cfg_upd Forced configuration update. Leads to an immediate update of the shadow registers. Depending on the two initial enable bits in the MI_CTRL register (init_offset_en and init_base_en) the offset counter, base address and buffer size shadow registers are also updated.
3	RO	0x0	reserved
2	W1C	0x0	sw_mi_skip Skip of current or next starting main picture: Aborts writing of main picture image data of the current frame to RAM (after the current burst transmission has been completed). Further main picture data up to the end of the current frame are discarded. No further macro block line interrupt (mblk_line), no wrap around interrupt for main picture (wrap_mp_y/cb/cr) and no fill level interrupt (fill_mp_y) are generated. Skip does not affect the generation of the main path frame end interrupt (mp_frame_end). Skip does not affect the processing of self picture and its corresponding interrupts namely the self path frame end interrupt (sp_frame_end). The byte counter (register MI_WR_BYTE_CNT) is not affected. It produces the correct number of JPEG or RAW data bytes at the end of the current (skipped) frame. After a skip has been performed the offset counter for the main picture at the start of the following frame are set depending on the bit init_offset_en in register MI_WR_CTRL: - Skip restart mode (init_offset_en = 0) The offset counters of the main picture are restarted at the old start values of the previous skipped frame. - Skip initial mode (init_offset_en = 1) The offset counters of the main picture are initialized with the register contents of the offset counter initial registers without any additional forced software update or automatic configuration update.
1:0	RO	0x0	reserved

MI_1400_MI_MP_WR_Y_BASE

Address: Operational Base(0x21D01400) + offset (0x0008)

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Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_mp_wr_y_base Base address of main picture Y component ring buffer, JPEG ring buffer or raw data ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. --- MI_MP_Y_BASE_AD_INIT --- Note: This register protects from non-aligned access. The bits 0 to 2 are hard wired to "000". As a consequence any byte address that is written to the register will automatically be re-mapped to the next lower 64 bit aligned address: write (MI_MP_Y_BASE_AD_INIT, address_value) is equivalent to write(MI_MP_Y_BASE_AD_INIT, address_value & 0xFFFFFFF8). Anyhow, in order to avoid confusion it is NOT recommended to use non-aligned address values for access. It is also NOT recommended to actively consider the register slice for register access in order to avoid unnecessary mask and shift operations. In addition, if camera IC provides AXI interfaces the programmed base address shall be burst aligned with respect to the burst length configured in MI_WR_CTRL. Set control bit init_base_en before updating so that a forced or automatic update can take effect.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_Y_SIZE

Address: Operational Base(0x21D01400) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_mp_wr_y_size Size of main picture Y component ring buffer, JPEG ring buffer or raw data ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. --- MI_MP_Y_SIZE_INIT --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details. Set control bit init_base_en before updating so that a forced or automatic update can take effect.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_Y_OFFS_CNT

Address: Operational Base(0x21D01400) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28:4	RW	0x0000000	sw_mp_wr_y_offs_cnt Offset counter initial value of main picture Y component ring buffer, JPEG ring buffer or raw data ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. --- MI_MP_WR_Y_OFFS_CNT --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details. Set control bit init_base_en before updating so that a forced or automatic update can take effect. Check exceptional handling in skip modes.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_Y_OFFS_CNT_START

Address: Operational Base(0x21D01400) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_mp_wr_y_offs_cnt_start Offset counter value which points to the start address of the previously processed picture (main picture Y component, JPEG or raw data). Updated at frame end. Note: A soft reset resets the contents to the reset value. --- MI_MP_WR_Y_OFFS_CNT_START --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_Y_IRQ_OFFS

Address: Operational Base(0x21D01400) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_mp_wr_y_irq_offs Reaching this programmed value by the current offset counter for addressing main picture Y component, JPEG or raw data leads to generation of fill level interrupt fill_mp_y. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. --- MI_MP_WR_Y_IRQ_OFFS --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CB_BASE

Address: Operational Base(0x21D01400) + offset (0x001C)

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Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_mp_wr_cb_base Base address of main picture Cb component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_MP_WR_CB_BASE --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details. Refer also to MI_MP_WR_Y_BASE with respect to the burst alignment restriction for AXI.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CB_SIZE

Address: Operational Base(0x21D01400) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RW	0x000000	sw_mp_wr_cb_size Size of main picture Cb component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_MP_WR_CB_SIZE --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_CB_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CB_OFFS_CNT

Address: Operational Base(0x21D01400) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RW	0x000000	sw_mp_wr_cb_offs_cnt Offset counter initial value of main picture Cb component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. Check exceptional handling in skip modes. --- MI_MP_WR_CB_OFFS_CNT --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CB_OFFS_CNT_START

Address: Operational Base(0x21D01400) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:4	RO	0x000000	sw_mp_wr_cb_offs_cnt_start Offset counter value which points to the start address of the previously processed picture (main picture Cb component). Updated at frame end. --- MI_MP_WR_CB_OFFS_CNT_START --- Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CR_BASE

Address: Operational Base(0x21D01400) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_mp_wr_cr_base Base address of main picture Cr component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_MP_WR_CR_BASE --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details. Refer also to MI_MP_WR_Y_BASE with respect to the burst alignment restriction for AXI.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CR_SIZE

Address: Operational Base(0x21D01400) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RW	0x000000	sw_mp_wr_cr_size Size of main picture Cr component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_MP_WR_CR_SIZE --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CR_OFFS_CNT

Address: Operational Base(0x21D01400) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:4	RW	0x000000	sw_mp_wr_cr_offs_cnt Offset counter initial value of main picture Cr component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. Check exceptional handling in skip modes. --- MI_MP_WR_CR_OFFS_CNT --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CR_OFFS_CNT_START

Address: Operational Base(0x21D01400) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_mp_wr_cr_offs_cnt_start Offset counter value which points to the start address of the previously processed picture (main picture Cr component). Updated at frame end. Note: Soft reset will reset the contents to reset value. --- MI_MP_WR_CR_OFFS_CNT_START --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_Y_BASE

Address: Operational Base(0x21D01400) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_sp_wr_y_base Base address of self picture Y component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_SP_WR_Y_BASE --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details. Refer also to MI_MP_WR_Y_BASE with respect to the burst alignment restriction for AXI.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_Y_SIZE

Address: Operational Base(0x21D01400) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28:4	RW	0x0000000	sw_sp_wr_y_size Size of self picture Y component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_SP_WR_Y_SIZE --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_Y_OFFS_CNT

Address: Operational Base(0x21D01400) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_sp_wr_y_offs_cnt Offset counter initial value of self picture Y component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_SP_WR_Y_OFFS_CNT --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_Y_OFFS_CNT_START

Address: Operational Base(0x21D01400) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_sp_y_offs_cnt_start Offset counter value which points to the start address of the previously processed picture (self picture Y component). Updated at frame end. Note: Soft reset will reset the contents to reset value. --- MI_SP_WR_Y_OFFS_CNT_START --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_Y_LLENGTH

Address: Operational Base(0x21D01400) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
14:0	RW	0x0000	sw_sp_wr_y_llength_tmp Line length of self picture Y component or RGB picture in pixel, also known as line stride. If no line stride is used, line length must match image width. For Y component the line length in 4:2:x planar mode must be a multiple of 16, for all other component modes a multiple of 4 and for RGB 565 a multiple of 2. There are no restrictions for RGB 888/666. In planar mode the line length of the Cb and Cr component is assumed according to the YCbCr format, i.e. half for 4:2:x and the same size for 4:4:4. In semi planar 4:2:x mode the line length of the Cb and Cr component is assumed the same size. Note: Line length always refers to the line length of the output image. This is particularly important when rotating. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path. If ARGB888 vflip, you need to configure sw_sp_wr_y_llength_tmp to be the self picture width, which will be multiplied by 4 inside the hardware (argb storage format).

MI_1400_MI_SP_WR_CB_BASE

Address: Operational Base(0x21D01400) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_sp_wr_cb_base Base address of self picture Cb component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_SP_WR_CB_BASE --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details. Refer also to MI_MP_WR_Y_BASE with respect to the burst alignment restriction for AXI.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CB_SIZE

Address: Operational Base(0x21D01400) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RW	0x000000	sw_sp_wr_cb_size Size of self picture Cb component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_SP_WR_CB_SIZE --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CB_OFFS_CNT

Address: Operational Base(0x21D01400) + offset (0x0058)

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Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RW	0x000000	sw_sp_cb_offs_cnt_init Offset counter initial value of self picture Cb component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_SP_WR_CB_OFFS_CNT --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CB_OFFS_CNT_START

Address: Operational Base(0x21D01400) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_sp_wr_cb_offs_cnt_start Offset counter value which points to the start address of the previously processed picture (self picture Cb component). Updated at frame end. Note: Soft reset will reset the contents to reset value. --- MI_SP_WR_CB_OFFS_CNT_START --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CR_BASE

Address: Operational Base(0x21D01400) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_sp_wr_cr_base Base address of self picture Cr component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_SP_WR_CR_BASE --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details. Refer also to MI_MP_WR_Y_BASE with respect to the burst alignment restriction for AXI.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CR_SIZE

Address: Operational Base(0x21D01400) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:4	RW	0x000000	sw_sp_wr_cr_size Size of self picture Cr component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_SP_WR_CR_SIZE --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CR_OFFS_CNT

Address: Operational Base(0x21D01400) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RW	0x000000	sw_sp_wr_cr_offs_cnt Offset counter initial value of self picture Cr component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_SP_WR_CR_OFFS_CNT --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CR_OFFS_CNT_START

Address: Operational Base(0x21D01400) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_sp_wr_cr_offs_cnt_start Offset counter value which points to the start address of the previously processed picture (self picture Cr component). Updated at frame end. --- MI_SP_WR_CR_OFFS_CNT_START --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_WR_BYTE_CNT

Address: Operational Base(0x21D01400) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	byte_cnt Counter value specifies the number of JPEG or RAW data bytes of the last transmitted frame. Updated at frame end. A soft reset will set the byte counter to zero.

MI_1400_MI_WR_CTRL_SHD

Address: Operational Base(0x21D01400) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
19:16	RO	0x0	path_enable_out Path_enable shadow register for module MI_OUT (former raw_enable_out, jpeg_enable_out, sp_enable_out, mp_enable_out)
15:4	RO	0x000	reserved
3:0	RO	0x0	path_enable_in Path_enable shadow register for module MI_IN (former raw_enable_in, jpeg_enable_in, sp_enable_in, mp_enable_in)

MI_1400_MI_MP_WR_Y_BASE_SHD

Address: Operational Base(0x21D01400) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_mp_wr_y_base_shd Base address of main picture Y component ring buffer, JPEG ring buffer or raw data ring buffer. --- MI_MP_WR_Y_BASE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_Y_SIZE_SHD

Address: Operational Base(0x21D01400) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_mp_wr_y_size_shd Size of main picture Y component ring buffer, JPEG ring buffer or raw data ring buffer. --- MI_MP_WR_Y_SIZE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_Y_OFFS_CNT_SHD

Address: Operational Base(0x21D01400) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_mp_wr_y_offs_cnt_shd Current offset counter of main picture Y component, JPEG or raw data ring buffer for address generation Note: Soft reset will reset the contents to reset value. --- MI_MP_WR_Y_OFFS_CNT_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_Y_IRQ_OFFS_SHD

Address: Operational Base(0x21D01400) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28:4	RO	0x0000000	sw_mp_wr_y_irq_offs_shd Reaching this offset value by the current offset counter for addressing main picture Y component, JPEG or raw data leads to generation of fill level interrupt fill_mp_y. --- MI_MP_WR_Y_IRQ_OFFS_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CB_BASE_SHD

Address: Operational Base(0x21D01400) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_mp_wr_cb_base_shd Base address of main picture Cb component ring buffer. --- MI_MP_WR_CB_BASE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CB_SIZE_SHD

Address: Operational Base(0x21D01400) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_mp_wr_cb_size_shd Size of main picture Cb component ring buffer. --- MI_MP_WR_CB_SIZE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CB_OFFS_CNT_SHD

Address: Operational Base(0x21D01400) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_mp_wr_cb_offs_cnt_shd Current offset counter of main picture Cb component ring buffer for address generation Note: Soft reset will reset the contents to reset value. --- MI_MP_WR_CB_OFFS_CNT_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CR_BASE_SHD

Address: Operational Base(0x21D01400) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_mp_wr_cr_base_shd Base address of main picture Cr component ring buffer. --- MI_MP_CR_BASE_AD_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CR_SIZE_SHD

Address: Operational Base(0x21D01400) + offset (0x0098)

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Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_mp_wr_cr_size_shd Size of main picture Cr component ring buffer. --- MI_MP_WR_CR_SIZE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CR_OFFS_CNT_SHD

Address: Operational Base(0x21D01400) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_mp_wr_cr_offs_cnt_shd Current offset counter of main picture Cr component ring buffer for address generation Note: Soft reset will reset the contents to reset value. --- MI_MP_WR_CR_OFFS_CNT_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_Y_BASE_SHD

Address: Operational Base(0x21D01400) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_sp_wr_y_base_shd Base address of self picture Y component ring buffer. --- MI_SP_WR_Y_BASE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_Y_SIZE_SHD

Address: Operational Base(0x21D01400) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_sp_wr_y_size_shd Size of self picture Y component ring buffer. --- MI_SP_WR_Y_SIZE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_Y_OFFS_CNT_SHD

Address: Operational Base(0x21D01400) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_sp_wr_y_offs_cnt_shd Current offset counter of self picture Y component ring buffer for address generation Note: Soft reset will reset the contents to reset value. --- MI_SP_WR_Y_OFFS_CNT_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

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MI_1400_MI_SP_WR_CB_BASE_AD_SHD

Address: Operational Base(0x21D01400) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_sp_wr_cb_base_shd Base address of self picture Cb component ring buffer. --- MI_SP_WR_CB_BASE_AD_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CB_SIZE_SHD

Address: Operational Base(0x21D01400) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_sp_wr_cb_size_shd Size of self picture Cb component ring buffer. --- MI_SP_WR_CB_SIZE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CB_OFFS_CNT_SHD

Address: Operational Base(0x21D01400) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_sp_wr_cb_offs_cnt_shd Current offset counter of self picture Cb component ring buffer for address generation Note: Soft reset will reset the contents to reset value. --- MI_SP_WR_CB_OFFS_CNT_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CR_BASE_AD_SHD

Address: Operational Base(0x21D01400) + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_sp_wr_cr_base_shd Base address of self picture Cr component ring buffer. --- MI_SP_WR_CR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CR_SIZE_SHD

Address: Operational Base(0x21D01400) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_sp_wr_cr_size_shd Size of self picture Cr component ring buffer. --- MI_SP_WR_CR_SIZE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CR_OFFS_CNT_SHD

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Address: Operational Base(0x21D01400) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_sp_wr_cr_offs_cnt_shd Current offset counter of self picture Cr component ring buffer for address generation Note: Soft reset will reset the contents to reset value. --- MI_SP_WR_CR_OFFS_CNT_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_RD_Y_PIC_START_AD

Address: Operational Base(0x21D01400) + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_mi_rd_y_pic_start_ad Image start address of the y component Note: Must be multiple of 4 in interleaved mode.

MI_1400_MI_RD_Y_PIC_WIDTH

Address: Operational Base(0x21D01400) + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	sw_mi_rd_y_pic_width Image width of the Y component in pixel. For YCbCr 4:2:x the image width must be a multiple of 2. In planar mode the image width of the Cb and Cr component is assumed according to the YCbCr format, i.e. half for 4:2:x and the same size for 4:4:4. In semi planar 4:2:x mode the image width of the Cb component (which includes Cr) is assumed the same size. In interleave mode no Cb/Cr image width is used.

MI_1400_MI_RD_Y_LLENGTH

Address: Operational Base(0x21D01400) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	sw_mi_rd_y_llength Line length of the Y component of the original image in memory For an uncropped image, where lines follow each other without offset (no line stride), line length must match image width. For Y component the line length in 4:2:x planar mode must be a multiple of 8, for all other component modes a multiple of 4. In planar mode the line length of the Cb and Cr component is assumed according to the YCbCr format, i.e. half for 4:2:x and the same size for 4:4:4. In semi planar 4:2:x mode the line length of the Cb component (which includes Cr) is assumed the same size. In interleave mode no Cb/Cr line length is used.

MI_1400_MI_RD_Y_PIC_SIZE

Address: Operational Base(0x21D01400) + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:0	RW	0x0000000	sw_mi_rd_y_pic_size Image size of the Y component in pixel which has to be the Y line length multiplied by the Y image height (dma_y_llength * dma_y_pic_height). In planar mode the image size of the Cb and Cr component is assumed according to the YCbCr format, i.e. a quarter for 4:2:0, half for 4:2:2 and the same for 4:4:4. In semi planar mode the image size of the Cb component (which includes Cr) is assumed half for 4:2:0 and the same size for 4:2:2. In interleave mode no Cb/Cr image size is used.

MI_1400_MI_RD_CB_PIC_START_AD

Address: Operational Base(0x21D01400) + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_mi_rd_cb_pic_start_ad Image start address of the Cb component Note: Must be multiple of 2 in semi-planar mode.

MI_1400_MI_RD_CR_PIC_START_AD

Address: Operational Base(0x21D01400) + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_mi_rd_cr_pic_start_ad Image start address of the Cr component

MI_1400_MI_IMSC

Address: Operational Base(0x21D01400) + offset (0x00F8)

Bit	Attr	Reset Value	Description
31	RW	0x0	mpfbc_wr_frame_end Mask mpfbc write end of frame interrupt
30	RW	0x0	isp_bus_err Mask bit for isp bus error interrupt
29	RW	0x0	bpds_frame_end Mask bypass down-sampling picture end of frame interrupt
28	RW	0x0	mpds_frame_end Mask main down-sampling picture end of frame interrupt
27	RW	0x0	wrap_bp_cb Mask bit for bypass picture Cb address wrap interrupt
26	RW	0x0	wrap_bp_y Mask bit for bypass picture Y address wrap interrupt
25	RW	0x0	bp_frame_end Mask bypass path write end of frame interrupt
24	RW	0x0	bay3d_ds_frame_end Mask bay3d down scale write end of frame interrupt
23	RW	0x0	bay3d_cur_frame_end Mask bay3d current write end of frame interrupt
22	RW	0x0	bay3d_iir_frame_end Mask bay3d iir write end of frame interrupt
21	RW	0x0	gain_wr_frame_end Mask gain write end of frame interrupt
20	RW	0x0	dbr_wr_frame_end Mask debayer-in write end of frame interrupt
19	RW	0x0	raw3_wr_frame_end Mask raw1 tx end of frame interrupt
18	RW	0x0	raw2_wr_frame_end Mask raw2 tx end of frame interrupt

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Bit	Attr	Reset Value	Description
17	RW	0x0	raw1_wr_frame_end Mask raw1 tx end of frame interrupt
16	RW	0x0	raw0_wr_frame_end Mask raw0 tx end of frame interrupt
15	RO	0x0	reserved
14	RW	0x0	sw_all_frame_end_en Mask all picture end of frame interrupt
13	RW	0x0	sw_y12c_frame_end_en Mask of Y12 C COMPENT picture end of frame interrupt
12	RW	0x0	sw_y12y_frame_end_en Mask of Y12 Y COMPENT picture end of frame interrupt
11	RW	0x0	dma_ready Mask bit for dma ready interrupt
10	RW	0x0	fill_mp_y2 Mask bit for fill level interrupt 2 of main picture Y, JPEG or raw data
9	RW	0x0	wrap_sp_cr Mask bit for self picture Cr address wrap interrupt
8	RW	0x0	wrap_sp_cb Mask bit for self picture Cb address wrap interrupt
7	RW	0x0	wrap_sp_y Mask bit for self picture Y address wrap interrupt
6	RW	0x0	wrap_mp_cr Mask bit for main picture Cr address wrap interrupt
5	RW	0x0	wrap_mp_cb Mask bit for main picture Cb address wrap interrupt
4	RW	0x0	wrap_mp_y Mask bit for main picture Y address wrap interrupt
3	RW	0x0	fill_mp_y Mask bit for fill level interrupt of main picture Y, JPEG or raw data
2	RW	0x0	mblk_line Mask bit for macro block line interrupt of main picture (16 lines of Y, 8 lines of Cb and 8 lines of Cr are written into RAM)
1	RW	0x0	sp_frame_end Mask self picture end of frame interrupt
0	RW	0x0	mp_frame_end Mask main picture end of frame interrupt

MI_1400_MI_RIS

Address: Operational Base(0x21D01400) + offset (0x00FC)

Bit	Attr	Reset Value	Description
31	RO	0x0	mpfbc_wr_frame_end Raw status of mpfbc write end of frame interrupt
30	RO	0x0	isp_bus_err Raw status of isp bus error interrupt
29	RO	0x0	bpds_frame_end Raw status of bypass down-sampling picture end of frame interrupt
28	RO	0x0	mpds_frame_end Raw status of main down-sampling picture end of frame interrupt
27	RO	0x0	wrap_bp_cb Raw status of bypass picture Cb address wrap interrupt
26	RO	0x0	wrap_bp_y Raw status of bypass picture Y address wrap interrupt

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Bit	Attr	Reset Value	Description
25	RO	0x0	bp_frame_end Raw status of bypass path write end of frame interrupt
24	RO	0x0	bay3d_ds_frame_end Raw status of bay3d down scale write end of frame interrupt
23	RO	0x0	bay3d_cur_frame_end Raw status of bay3d current write end of frame interrupt
22	RO	0x0	bay3d_iir_frame_end Raw status of bay3d iir write end of frame interrupt
21	RO	0x0	gain_wr_frame_end Raw status of gain write end of frame interrupt
20	RO	0x0	dbr_wr_frame_end Raw status of debayer-in write end of frame interrupt
19	RO	0x0	raw3_wr_frame_end Raw status of raw0 tx end of frame interrupt
18	RO	0x0	raw2_wr_frame_end Raw status of raw2 tx end of frame interrupt
17	RO	0x0	raw1_wr_frame_end Raw status of raw1 tx end of frame interrupt
16	RO	0x0	raw0_wr_frame_end Raw status of raw0 tx end of frame interrupt
15	RO	0x0	reserved
14	RO	0x0	ro_all_frame_end_rawsts Raw status of all picture end of frame interrupt
13	RO	0x0	ro_y12c_frame_end_rawsts Raw status of Y12 C picture end of frame interrupt
12	RO	0x0	ro_y12y_frame_end_rawsts Raw status of Y12 Y picture end of frame interrupt
11	RO	0x0	dma_ready Raw status of dma ready interrupt
10	RO	0x0	fill_mp_y2 Raw status of fill level interrupt 2 of main picture Y, JPEG or raw data
9	RO	0x0	wrap_sp_cr Raw status of self picture Cr address wrap interrupt
8	RO	0x0	wrap_sp_cb Raw status of self picture Cb address wrap interrupt
7	RO	0x0	wrap_sp_y Raw status of self picture Y address wrap interrupt
6	RO	0x0	wrap_mp_cr Raw status of main picture Cr address wrap interrupt
5	RO	0x0	wrap_mp_cb Raw status of main picture Cb address wrap interrupt
4	RO	0x0	wrap_mp_y Raw status of main picture Y address wrap interrupt
3	RO	0x0	fill_mp_y Raw status of fill level interrupt of main picture Y, JPEG or raw data
2	RO	0x0	mblk_line Raw status of macro block line interrupt of main picture (16 lines of Y, 8 lines of Cb and 8 lines of Cr are written into RAM, valid only for planar and semi-planar mode)
1	RO	0x0	sp_frame_end Raw status of self picture end of frame interrupt
0	RO	0x0	mp_frame_end Raw status of main picture end of frame interrupt

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MI_1400_MI_MIS

Address: Operational Base(0x21D01400) + offset (0x0100)

Bit	Attr	Reset Value	Description
31	RO	0x0	mpfbc_wr_frame_end Masked status of mpfbc write end of frame interrupt
30	RO	0x0	isp_bus_err Masked status of isp bus error interrupt
29	RO	0x0	bpds_frame_end Masked status of bypass down-sampling picture end of frame interrupt
28	RO	0x0	mpds_frame_end Masked status of main down-sampling picture end of frame interrupt
27	RO	0x0	wrap_bp_cb Masked status of bypass picture Cb address wrap interrupt
26	RO	0x0	wrap_bp_y Masked status of bypass picture Y address wrap interrupt
25	RO	0x0	bp_frame_end Masked status of bypass path write end of frame interrupt
24	RO	0x0	bay3d_ds_frame_end Masked status of bay3d down scale write end of frame interrupt
23	RO	0x0	bay3d_cur_frame_end Masked status of bay3d current write end of frame interrupt
22	RO	0x0	bay3d_iir_frame_end Masked status of bay3d iir write end of frame interrupt
21	RO	0x0	gain_wr_frame_end Masked status of gain write end of frame interrupt
20	RO	0x0	dbr_wr_frame_end Masked status of debayer-in write end of frame interrupt
19	RO	0x0	raw3_wr_frame_end Masked status of raw3 tx end of frame interrupt
18	RO	0x0	raw2_wr_frame_end Masked status of raw2 tx end of frame interrupt
17	RO	0x0	raw1_wr_frame_end Masked status of raw1 tx end of frame interrupt
16	RO	0x0	raw0_wr_frame_end Masked status of raw0 tx end of frame interrupt
15	RO	0x0	reserved
14	RO	0x0	ro_all_frame_end_sts Masked status of all picture end of frame interrupt
13	RO	0x0	ro_y12c_frame_end_sts Masked status of Y12 C picture end of frame interrupt
12	RO	0x0	ro_y12y_frame_end_sts Masked status of Y12 Y picture end of frame interrupt
11	RO	0x0	dma_ready Masked status of dma ready interrupt
10	RO	0x0	fill_mp_y2 Masked status of fill level interrupt 2 of main picture Y, JPEG or raw data
9	RO	0x0	wrap_sp_cr Masked status of self picture Cr address wrap interrupt
8	RO	0x0	wrap_sp_cb Masked status of self picture Cb address wrap interrupt
7	RO	0x0	wrap_sp_y Masked status of self picture Y address wrap interrupt

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Bit	Attr	Reset Value	Description
6	RO	0x0	wrap_mp_cr Masked status of main picture Cr address wrap interrupt
5	RO	0x0	wrap_mp_cb Masked status of main picture Cb address wrap interrupt
4	RO	0x0	wrap_mp_y Masked status of main picture Y address wrap interrupt
3	RO	0x0	fill_mp_y Masked status of fill level interrupt of main picture Y, JPEG or raw data
2	RO	0x0	mblk_line Masked status of macro block line interrupt of main picture (16 lines of Y, 8 lines of Cb and 8 lines of Cr are written into RAM, valid only for planar and semi-planar mode)
1	RO	0x0	sp_frame_end Masked status of self picture end of frame interrupt
0	RO	0x0	mp_frame_end Masked status of main picture end of frame interrupt

MI_1400_MI_ICR

Address: Operational Base(0x21D01400) + offset (0x0104)

Bit	Attr	Reset Value	Description
31	WO	0x0	mpfbc_wr_frame_end Clear mpfbc write end of frame interrupt
30	WO	0x0	isp_bus_err Clear isp bus error interrupt
29	WO	0x0	bpds_frame_end Clear bypass down-sampling picture end of frame interrupt
28	WO	0x0	mpds_frame_end Clear main down-sampling picture end of frame interrupt
27	WO	0x0	wrap_bp_cb Clear bypass picture Cb address wrap interrupt
26	WO	0x0	wrap_bp_y Clear bypass picture Y address wrap interrupt
25	WO	0x0	bp_frame_end Clear bypass path write end of frame interrupt
24	WO	0x0	bay3d_ds_frame_end Clear bay3d down scale write end of frame interrupt
23	WO	0x0	bay3d_cur_frame_end Clear bay3d current write end of frame interrupt
22	WO	0x0	bay3d_iir_frame_end Clear bay3d iir write end of frame interrupt
21	WO	0x0	gain_wr_frame_end Clear gain write end of frame interrupt
20	WO	0x0	dbr_wr_frame_end Clear debayer-in write end of frame interrupt
19	WO	0x0	raw3_wr_frame_end Clear raw3 tx end of frame interrupt
18	WO	0x0	raw2_wr_frame_end Clear raw2 tx end of frame interrupt
17	WO	0x0	raw1_wr_frame_end Clear raw1 tx end of frame interrupt
16	WO	0x0	raw0_wr_frame_end Clear raw0 tx end of frame interrupt
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14	WO	0x0	sw_all_frame_end_clr Clear all picture end of frame interrupt
13	WO	0x0	sw_y12c_frame_end_clr Clear Y12 C picture end of frame interrupt
12	WO	0x0	sw_y12y_frame_end_clr Clear Y12 Y picture end of frame interrupt
11	WO	0x0	dma_ready Clear dma ready interrupt
10	WO	0x0	fill_mp_y2 Clear fill level interrupt 2
9	WO	0x0	wrap_sp_cr Clear self picture Cr address wrap interrupt
8	WO	0x0	wrap_sp_cb Clear self picture Cb address wrap interrupt
7	WO	0x0	wrap_sp_y Clear self picture Y address wrap interrupt
6	WO	0x0	wrap_mp_cr Clear main picture Cr address wrap interrupt
5	WO	0x0	wrap_mp_cb Clear main picture Cb address wrap interrupt
4	WO	0x0	wrap_mp_y Clear main picture Y address wrap interrupt
3	WO	0x0	fill_mp_y Clear fill level interrupt
2	WO	0x0	mblk_line Clear macro block line interrupt
1	WO	0x0	sp_frame_end Clear self picture end of frame interrupt
0	WO	0x0	mp_frame_end Clear main picture end of frame interrupt

MI_1400_MI_ISR

Address: Operational Base(0x21D01400) + offset (0x0108)

Bit	Attr	Reset Value	Description
31	WO	0x0	mpfbc_wr_frame_end Set mpfbc write end of frame interrupt
30	WO	0x0	isp_bus_err Set isp bus error interrupt
29	WO	0x0	bpds_frame_end Set bypass down-sampling picture end of frame interrupt
28	WO	0x0	mpds_frame_end Set main down-sampling picture end of frame interrupt
27	WO	0x0	wrap_bp_cb Set bypass picture Cb address wrap interrupt
26	WO	0x0	wrap_bp_y Set bypass picture Y address wrap interrupt
25	WO	0x0	bp_frame_end Set bypass path write end of frame interrupt
24	WO	0x0	bay3d_ds_frame_end Set bay3d down scale write end of frame interrupt
23	WO	0x0	bay3d_cur_frame_end Set bay3d current write end of frame interrupt
22	WO	0x0	bay3d_iir_frame_end Set bay3d iir write end of frame interrupt

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Bit	Attr	Reset Value	Description
21	WO	0x0	gain_wr_frame_end Set gain write end of frame interrupt
20	WO	0x0	dbr_wr_frame_end Set debayer-in write end of frame interrupt
19	WO	0x0	raw3_wr_frame_end Set raw3 tx end of frame interrupt
18	WO	0x0	raw2_wr_frame_end Set raw2 tx end of frame interrupt
17	WO	0x0	raw1_wr_frame_end Set raw1 tx end of frame interrupt
16	WO	0x0	raw0_wr_frame_end Set raw0 tx end of frame interrupt
15	RO	0x0	reserved
14	RW	0x0	sw_all_frame_end_set Set all picture end of frame interrupt
13	RW	0x0	sw_y12c_frame_end_set Set Y12 C picture end of frame interrupt
12	RW	0x0	sw_y12y_frame_end_set Set Y12 Y picture end of frame interrupt
11	WO	0x0	dma_ready Set dma ready interrupt
10	WO	0x0	fill_mp_y2 Set fill level interrupt 2
9	WO	0x0	wrap_sp_cr Set self picture Cr address wrap interrupt
8	WO	0x0	wrap_sp_cb Set self picture Cb address wrap interrupt
7	WO	0x0	wrap_sp_y Set self picture Y address wrap interrupt
6	WO	0x0	wrap_mp_cr Set main picture Cr address wrap interrupt
5	WO	0x0	wrap_mp_cb Set main picture Cb address wrap interrupt
4	WO	0x0	wrap_mp_y Set main picture Y address wrap interrupt
3	WO	0x0	fill_mp_y Set fill level interrupt
2	WO	0x0	mblk_line Set macro block line interrupt
1	WO	0x0	sp_frame_end Set self picture end of frame interrupt
0	WO	0x0	mp_frame_end Set main picture end of frame interrupt

MI_1400_MI_STATUS

Address: Operational Base(0x21D01400) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22	RO	0x0	bpds_cb_full FIFO full flag of Cb FIFO in main path down sampling asserted since last clear
21	RO	0x0	bpds_y_full FIFO full flag of Y FIFO in bypass path down sampling asserted since last clear

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Bit	Attr	Reset Value	Description
20	RO	0x0	mpds_cb_full FIFO full flag of Cb FIFO in main path down sampling asserted since last clear
19	RO	0x0	mpds_y_full FIFO full flag of Y FIFO in main path down sampling asserted since last clear
18	RO	0x0	bp_cb_fifo_full FIFO full flag of Cb FIFO in bypass path asserted since last clear
17	RO	0x0	bp_y_fifo_full FIFO full flag of Y FIFO in bypass path asserted since last clear
16	RO	0x0	bay3d_ds_fifo_full FIFO full flag of bay3d down scale FIFO asserted since last clear
15	RO	0x0	bay3d_cur_fifo_full FIFO full flag of bay3d current FIFO asserted since last clear
14	RO	0x0	bay3d_iir_fifo_full FIFO full flag of bay3d iir FIFO asserted since last clear
13	RO	0x0	gain_fifo_full FIFO full flag of gain FIFO asserted since last clear
12	RO	0x0	dbr_wr_y_fifo_full FIFO full flag of Y FIFO in debayer-in write path asserted since last clear
11	RO	0x0	raw3_wr_y_fifo_full FIFO full flag of Y FIFO in raw3 tx path asserted since last clear
10	RO	0x0	raw2_wr_y_fifo_full FIFO full flag of Y FIFO in raw2 tx path asserted since last clear
9	RO	0x0	raw1_wr_y_fifo_full FIFO full flag of Y FIFO in raw1 tx path asserted since last clear
8	RO	0x0	raw0_wr_y_fifo_full FIFO full flag of Y FIFO in raw0 tx path asserted since last clear
7	RO	0x0	reserved
6	RO	0x0	sp_cr_fifo_full FIFO full flag of Cr FIFO in self path asserted since last clear
5	RO	0x0	sp_cb_fifo_full FIFO full flag of Cb FIFO in self path asserted since last clear
4	RO	0x0	sp_y_fifo_full FIFO full flag of Y FIFO in self path asserted since last clear
3	RO	0x0	reserved
2	RO	0x0	mp_cr_fifo_full FIFO full flag of Cr FIFO in main path asserted since last clear
1	RO	0x0	mp_cb_fifo_full FIFO full flag of Cb FIFO in main path asserted since last clear
0	RO	0x0	mp_y_fifo_full FIFO full flag of Y FIFO in main path asserted since last clear

MI_1400_MI_STATUS_CLR

Address: Operational Base(0x21D01400) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved
18	WO	0x0	bp_cb_fifo_full Clear status of Cb FIFO full flag in bypass path
17	WO	0x0	bp_y_fifo_full Clear status of Y FIFO full flag in bypass path
16	WO	0x0	bay3d_ds_fifo_full Clear status of bay3d down scale FIFO full flag

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Bit	Attr	Reset Value	Description
15	WO	0x0	bay3d_cur_fifo_full Clear status of bay3d current FIFO full flag
14	WO	0x0	bay3d_iir_fifo_full Clear status of bay3d iir FIFO full flag
13	WO	0x0	gain_fifo_full Clear status of gain FIFO full flag
12	WO	0x0	dbr_wr_y_fifo_full Clear status of Y FIFO full flag in debayer-in write path
11	WO	0x0	raw3_wr_y_fifo_full Clear status of Y FIFO full flag in raw3 tx path
10	WO	0x0	raw2_wr_y_fifo_full Clear status of Y FIFO full flag in raw2 tx path
9	WO	0x0	raw1_wr_y_fifo_full Clear status of Y FIFO full flag in raw1 tx path
8	WO	0x0	raw0_wr_y_fifo_full Clear status of Y FIFO full flag in raw0 tx path
7	RO	0x0	reserved
6	WO	0x0	sp_cr_fifo_full Clear status of Cr FIFO full flag in self path
5	WO	0x0	sp_cb_fifo_full Clear status of Cb FIFO full flag in self path
4	WO	0x0	sp_y_fifo_full Clear status of Y FIFO full flag in self path
3	RO	0x0	reserved
2	WO	0x0	mp_cr_fifo_full Clear status of Cr FIFO full flag in main path
1	WO	0x0	mp_cb_fifo_full Clear status of Cb FIFO full flag in main path
0	WO	0x0	mp_y_fifo_full Clear status of Y FIFO full flag in main path

MI_1400_MI_SP_WR_Y_PIC_WIDTH

Address: Operational Base(0x21D01400) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	sw_sp_wr_y_pic_width Image width of the self picture Y component or RGB picture in pixel. For YCbCr 4:2:x and RGB 565 the image width must be a multiple of 2. If no line stride is used but flipping required, the image width must be a multiple of 8 for 4:2:x planar or 4 for 4:4:4 planar/4:2:x semi planar. There are no restrictions for RGB 888/666. In planar mode the image width of the Cb and Cr component is assumed according to the YCbCr format, i.e. half for 4:2:x and the same size for 4:4:4. In semi planar 4:2:x mode the image width of the Cb component (which includes Cr) is assumed the same size. In interleave mode no Cb/Cr image width is used. Note: Image width always refers to the picture width of the output image. This is particularly important when rotating. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path.

MI_1400_MI_SP_WR_Y_PIC_HEIGHT

Address: Operational Base(0x21D01400) + offset (0x0118)

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Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	sw_sp_wr_y_pic_height Image height of the y component or RGB picture in pixel. In planar and semi planar mode the image width of the Cb and Cr component is assumed according to the YCbCr format, i.e. half for 4:2:0 and the same for 4:2:2 and 4:4:4. Note: Image height always refers to the picture height of the output image. This is particularly important when rotating. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path.

MI_1400_MI_SP_WR_Y_PIC_SIZE

Address: Operational Base(0x21D01400) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	sw_sp_wr_y_pic_size Image size of the Y component or RGB picture in pixel which has to be the Y line length multiplied by the Y image height (sp_y_llength * sp_y_pic_height). In planar mode the image size of the Cb and Cr component is assumed according to the YCbCr format, i.e. a quarter for 4:2:0, half for 4:2:2 and the same for 4:4:4. In semi planar mode the image size of the Cb and Cr component is assumed half for 4:2:0 and the same size for 4:2:2. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the self path.

MI_1400_MI_RD_CTRL

Address: Operational Base(0x21D01400) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	sw_mi_rd_start_sel DMA read start mode 1'b1: sw_mi_rd_start_pre 1'b0: sw_mi_rd_start_pre toggle
13:12	RW	0x0	sw_mi_rd_rgb_format Selects RGB Bayer data of read DMA picture 2'b00: No DMA RGB Bayer data 2'b01: 8 bit RGB Bayer data 2'b10: 16 bit RGB Bayer data (12 bit used) Bytes are organized MSB first and 4 lower bits of LSB remain unused: byte_even -> bayer[11:4], byte_odd[7:4] -> bayer[3:0] 2'b11: Reserved.
11	RO	0x0	reserved
10	RW	0x0	sw_mi_rd_frame_end_disable Suppresses v_end so that no frame end can be detected by following instances. Note: The dma_ready interrupt is raised as usual, but the dma_frame_end interrupt will not be generated until v_end has been enabled again.

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Bit	Attr	Reset Value	Description
9	RW	0x0	sw_mi_rd_continuous_en Enables continuous mode. If set the same frame is read back over and over. A start pulse on dma_start is needed only for the first time. To stop continuous mode reset this bit (takes effect after the next frame end) or execute a soft reset. This bit is intended to be used in conjunction with the Superimpose feature.
8	RW	0x0	sw_mi_rd_byte_swap Enables change of DMA byte order of the 32 bit input word at read port 1'b1: Byte order is mirrored but the bit order within one byte doesn't change 1'b0: No byte mirroring
7:6	RW	0x0	sw_mi_rd_inout_format Selects input/output format of DMA picture. 2'b11: YCbCr 4:4:4 2'b10: YCbCr 4:2:2 2'b01: YCbCr 4:2:0 2'b00: YCbCr 4:0:0
5:4	RW	0x0	sw_mi_rd_format Defines how YCbCr picture data is read from memory. 2'b00: Reserved, planar not support now 2'b01: Semi planar, for YCbCr 4:2:x 2'b10: Interleaved (combined), for YCbCr 4:2:2 and RGB only 2'b11: Reserved
3:2	RW	0x0	sw_mi_rd_burst_len_chrom Burst length for Cb or Cr data affecting DMA read port. 2'b00: 4-beat bursts 2'b01: 8-beat bursts 2'b10: 16-beat bursts 2'b11: Reserved Ignored if 8- or 16-beat bursts are not supported.
1:0	RW	0x0	sw_mi_rd_burst_len_lum Burst length for Y data affecting DMA read port. 2'b00: 4-beat bursts 2'b01: 8-beat bursts 2'b10: 16-beat bursts 2'b11: Reserved Ignored if 8- or 16-beat bursts are not supported.

MI_1400_MI_RD_START

Address: Operational Base(0x21D01400) + offset (0x0124)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	WO	0x0	sys_mi_rd_start_pre Enables DMA access. Additionally main or self path has to be enabled separately.

MI_1400_MI_RD_STATUS

Address: Operational Base(0x21D01400) + offset (0x0128)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	sw_mi_rd_active If set DMA access is active.

MI_1400_MI_WR_PIXEL_CNT

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Address: Operational Base(0x21D01400) + offset (0x012C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	pix_cnt Counter value specifies the number of pixels of the defect pixel list generated by DPCC of the last transmitted frame. Updated at frame end. A soft reset will set the counter to zero.

MI_1400_MI_MP_WR_Y_BASE2

Address: Operational Base(0x21D01400) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_mp_wr_y_base2 2nd ping pong base address of main picture Y component buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_MP_WR_Y_BASE2 --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details. Refer also to MI_MP_WR_Y_BASE with respect to the burst alignment restriction for AXI.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CB_BASE2

Address: Operational Base(0x21D01400) + offset (0x0134)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_mp_wr_cb_base2 2nd ping pong base address of main picture CB component buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_MP_WR_CB_BASE2 --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_CB_BASE register description for details. Refer also to MI_MP_WR_CB_BASE with respect to the burst alignment restriction for AXI.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_CR_BASE2

Address: Operational Base(0x21D01400) + offset (0x0138)

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Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_mp_wr_cr_base2 2nd ping pong base address of main picture CR component buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_MP_WR_CR_BASE2 --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_CR_BASE register description for details. Refer also to MI_MP_WR_CR_BASE with respect to the burst alignment restriction for AXI.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_Y_BASE2

Address: Operational Base(0x21D01400) + offset (0x013C)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_mp_wr_y_base2 2nd ping pong base address of main picture Y component buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_MP_WR_Y_BASE2 --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details. Refer also to MI_MP_WR_Y_BASE with respect to the burst alignment restriction for AXI.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CB_BASE2

Address: Operational Base(0x21D01400) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_mp_wr_cb_base2 2nd ping pong base address of main picture CB component buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_MP_WR_CB_BASE2 --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_CB_BASE register description for details. Refer also to MI_MP_WR_CB_BASE with respect to the burst alignment restriction for AXI.
3:0	RO	0x0	reserved

MI_1400_MI_SP_WR_CR_BASE2

Address: Operational Base(0x21D01400) + offset (0x0144)

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Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_mp_wr_cr_base2 2nd ping pong base address of main picture CR component buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_MP_WR_CR_BASE2 --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_CR_BASE register description for details. Refer also to MI_MP_WR_CR_BASE with respect to the burst alignment restriction for AXI.
3:0	RO	0x0	reserved

MI_1400_MI_WR_XTD_FORMAT_CTRL

Address: Operational Base(0x21D01400) + offset (0x0148)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	RW	0x0	sw_mi_wr_nv21_dma_read 1'b0: DMA read path: Use NV12 storage format for semi-planar YCbCr 4:2:x mode, Cb is located on even addresses. 1'b1: DMA read path: Use NV21 storage format for semi-planar YCbCr 4:2:x mode, Cr is located on even addresses.
1	RW	0x0	sw_mi_wr_nv21_self 1'b0: Self path: Use NV12 storage format for semi-planar YCbCr 4:2:x mode, Cb is located on even addresses. 1'b1: Self path: Use NV21 storage format for semi-planar YCbCr 4:2:x mode, Cr is located on even addresses. Note: If RGB888, do RB swap.
0	RW	0x0	sw_mi_wr_nv21_main 1'b0: Main path: Use NV12 storage format for semi-planar YCbCr 4:2:x mode, Cb is located on even addresses. 1'b1: Main path: Use NV21 storage format for semi-planar YCbCr 4:2:x mode, Cr is located on even addresses.

MI_1400_MI_WR_ID

Address: Operational Base(0x21D01400) + offset (0x0154)

Bit	Attr	Reset Value	Description
31:28	RO	0x6	sw_spcr_wr_axi_id Spcr write id
27:24	RO	0x5	sw_spcb_wr_axi_id Spcb write id
23:20	RO	0x4	sw_spy_wr_axi_id Spy write id
19:16	RO	0x3	sw_mpcr_wr_axi_id Mpcr write id
15:12	RO	0x2	sw_mpcb_wr_axi_id Mpcb write id
11:8	RO	0x1	sw_mpy_wr_axi_id Mpy write id
7:0	RO	0x00	reserved

MI_1400_MI_MP_WR_Y_IRQ_OFFS2

Address: Operational Base(0x21D01400) + offset (0x01E0)

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Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_mp_wr_y_irq_offs2 Reaching this programmed value by the current offset counter for addressing main picture Y component, JPEG or raw data leads to generation of fill level interrupt fill_mp_y. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. --- MI_MP_WR_Y_IRQ_OFFS --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_Y_IRQ_OFFS2_SHD

Address: Operational Base(0x21D01400) + offset (0x01E4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_mp_wr_y_irq_offs2_shd Reaching this offset value by the current offset counter for addressing main picture Y component, JPEG or raw data leads to generation of fill level interrupt fill_mp_y. --- MI_MP_WR_Y_IRQ_OFFS_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_Y_LLENGTH

Address: Operational Base(0x21D01400) + offset (0x01E8)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	sw_mp_wr_y_llegnth Line length of main picture Y component in pixel, also known as line stride. If no line stride is used, line length must match image width. For Y component the line length in 4:2:x planar mode must be a multiple of 16. In planar mode the line length of the Cb and Cr component is assumed according to the YCbCr. In semi planar 4:2:x mode the line length of the Cb and Cr component is assumed the same size. Note: Line length always refers to the line length of the output image. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the main path.

MI_1400_MI_MP_WR_Y_PIC_WIDTH

Address: Operational Base(0x21D01400) + offset (0x01EC)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
14:0	RW	0x0000	sw_mp_wr_y_pic_width Image width of the main picture Y component or RGB picture in pixel. For YCbCr 4:2:x and RGB 565 the image width must be a multiple of 2. If no line stride is used but flipping required, the image width must be a multiple of 8 for 4:2:x planar or 4 for 4:4:4 planar/4:2:x semi planar. There are no restrictions for RGB 888/666. In planar mode the image width of the Cb and Cr component is assumed according to the YCbCr format, i.e. half for 4:2:x and the same size for 4:4:4. In semi planar 4:2:x mode the image width of the Cb component (which includes Cr) is assumed the same size. In interleave mode no Cb/Cr image width is used. Note: Image width always refers to the picture width of the output image. This is particularly important when rotating. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the main path.

MI_1400_MI_MP_WR_Y_PIC_HEIGHT

Address: Operational Base(0x21D01400) + offset (0x01F0)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	sw_mp_wr_y_pic_height Image height of the y component or RGB picture in pixel. In planar and semi planar mode the image width of the Cb and Cr component is assumed according to the YCbCr format, i.e. half for 4:2:0 and the same for 4:2:2 and 4:4:4. Note: Image height always refers to the picture height of the output image. This is particularly important when rotating. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the main path.

MI_1400_MI_MP_WR_Y_PIC_SIZE

Address: Operational Base(0x21D01400) + offset (0x01F4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	sw_mp_wr_y_pic_size Image size of the Y component or RGB picture in pixel which has to be the Y line length multiplied by the Y image height (sp_y_llength * sp_y_pic_height). In planar mode the image size of the Cb and Cr component is assumed according to the YCbCr format, i.e. a quarter for 4:2:0, half for 4:2:2 and the same for 4:4:4. In semi planar mode the image size of the Cb and Cr component is assumed half for 4:2:0 and the same size for 4:2:2. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the main path.

MI_1400_MI_MP_WR_CTRL

Address: Operational Base(0x21D01400) + offset (0x01F8)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_mp_wr_align_dis 1'b0: Mp+sp burst align 1'b1: Disable mi_mp+mi_sp write burst align
30:24	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
23:16	RW	0x00	sw_sp_wr_rgb888_alpha The RGB888 format of the self path supports filling with configurable alpha bits.
15:14	RO	0x0	reserved
13:12	RW	0x0	sw_mi_wr_tile_sel 2'b0: Disable tile out 2'b1: MP tile out 2'b2: SP tile out 2'b3: Not allowed
11	RO	0x0	reserved
10:8	RW	0x2	sw_mp_wr_output_format Selects output format of main picture. 3'b000: YCbCr 4:0:0 3'b001: YCbCr 4:2:0 3'b010: YCbCr 4:2:2 Others: Reserved Note: - Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the main path. - If sw_mp_wr_v_flip = 1 and yuv420 format, need to configure sw_mp_wr_output_format = 1.
7:0	RO	0x00	reserved

MI_1400_MI_BP_WR_CTRL

Address: Operational Base(0x21D01400) + offset (0x0200)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:8	RW	0x2	sw_bp_wr_output_format Selects output format of bypass picture. 3'b000: YCbCr 4:0:0 3'b001: YCbCr 4:2:0 3'b010: YCbCr 4:2:2 Others: Reserved Note: - Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the bypass path. - If sw_bp_wr_v_flip = 1 and yuv420 format, need to configure sw_bp_wr_output_format = 1.
7:6	RO	0x0	reserved
5:4	RW	0x0	sw_bp_wr_format Defines how YCbCr bypass picture data is written to memory. 2'b00: Reserved 2'b01: Semi planar, for YCbCr 4:2:x 2'b10: Interleaved (combined), for YCbCr 4:2:2 only 2'b11: Reserved Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the bypass path.
3	RO	0x0	reserved
2	RW	0x0	sw_bp_wr_pingpong_en Pingpong mode of configuration registers for bypass path write at frame end. 1'b1: Enabled 1'b0: Disabled

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Bit	Attr	Reset Value	Description
1	RW	0x0	sw_bp_wr_auto_update Automatic update of configuration registers for bypass path at frame end. 1'b1: Enabled 1'b0: Disabled
0	RW	0x0	sw_bp_wr_enable Enables of bypass path

MI_1400_MI_BP_WR_Y_BASE

Address: Operational Base(0x21D01400) + offset (0x0204)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_bp_wr_y_base Base address of bypass picture Y component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_BP_WR_Y_BASE --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details. Refer also to MI_MP_WR_Y_BASE with respect to the burst alignment restriction for AXI.
3:0	RO	0x0	reserved

MI_1400_MI_BP_WR_Y_SIZE

Address: Operational Base(0x21D01400) + offset (0x0208)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_bp_wr_y_size Size of bypass picture Y component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_BP_WR_Y_SIZE --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_BP_WR_Y_OFFS_CNT

Address: Operational Base(0x21D01400) + offset (0x020C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_bp_wr_y_offs_cnt Offset counter initial value of bypass picture Y component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_BP_WR_Y_OFFS_CNT --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.

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Bit	Attr	Reset Value	Description
3:0	RO	0x0	reserved

MI_1400_MI_BP_WR_Y_OFFS_CNT_START

Address: Operational Base(0x21D01400) + offset (0x0210)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_bp_wr_y_offs_cnt_start Offset counter value which points to the start address of the previously processed picture (self picture Y component). Updated at frame end. Note: Soft reset will reset the contents to reset value. --- MI_BP_WR_Y_OFFS_CNT_START --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_BP_WR_Y_LLENGTH

Address: Operational Base(0x21D01400) + offset (0x0214)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	sw_bp_wr_y_llegnth Line length of main picture Y component in pixel, also known as line stride. If no line stride is used, line length must match image width. For Y component the line length in 4:2:x planar mode must be a multiple of 16. In planar mode the line length of the Cb and Cr component is assumed according to the YCbCr. In semi planar 4:2:x mode the line length of the Cb and Cr component is assumed the same size. Note: Line length always refers to the line length of the output image. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the bypass path.

MI_1400_MI_BP_WR_Y_PIC_WIDTH

Address: Operational Base(0x21D01400) + offset (0x0218)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	sw_bp_wr_y_pic_width Image width of the bypass picture Y component or RGB picture in pixel. For YCbCr 4:2:x and RGB 565 the image width must be a multiple of 2. If no line stride is used but flipping required, the image width must be a multiple of 8 for 4:2:x planar or 4 for 4:4:4 planar/4:2:x semi planar. There are no restrictions for RGB 888/666. In planar mode the image width of the Cb and Cr component is assumed according to the YCbCr format, i.e. half for 4:2:x and the same size for 4:4:4. In semi planar 4:2:x mode the image width of the Cb component (which includes Cr) is assumed the same size. In interleave mode no Cb/Cr image width is used. Note: Image width always refers to the picture width of the output image. This is particularly important when rotating. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the bypass path.

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MI_1400_MI_BP_WR_Y_PIC_HEIGHT

Address: Operational Base(0x21D01400) + offset (0x021C)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	sw_bp_wr_y_pic_height Image height of the y component or RGB picture in pixel. In planar and semi planar mode the image width of the Cb and Cr component is assumed according to the YCbCr format, i.e. half for 4:2:0 and the same for 4:2:2 and 4:4:4. Note: Image height always refers to the picture height of the output image. This is particularly important when rotating. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the bypass path.

MI_1400_MI_BP_WR_Y_PIC_SIZE

Address: Operational Base(0x21D01400) + offset (0x0220)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	sw_bp_wr_y_pic_size Image size of the Y component or RGB picture in pixel which has to be the Y line length multiplied by the Y image height (sp_y_llength * sp_y_pic_height). In planar mode the image size of the Cb and Cr component is assumed according to the YCbCr format, i.e. a quarter for 4:2:0, half for 4:2:2 and the same for 4:4:4. In semi planar mode the image size of the Cb and Cr component is assumed half for 4:2:0 and the same size for 4:2:2. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the bypass path.

MI_1400_MI_BP_WR_CB_BASE

Address: Operational Base(0x21D01400) + offset (0x0224)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_bp_wr_cb_base Base address of bypass picture Cb component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_BP_WR_CB_BASE --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details. Refer also to MI_MP_WR_Y_BASE with respect to the burst alignment restriction for AXI.
3:0	RO	0x0	reserved

MI_1400_MI_BP_WR_CB_SIZE

Address: Operational Base(0x21D01400) + offset (0x0228)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:4	RW	0x000000	sw_bp_wr_cb_size Size of bypass picture Cb component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_BP_WR_CB_SIZE --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_CB_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_BP_WR_CB_OFFS_CNT

Address: Operational Base(0x21D01400) + offset (0x022C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RW	0x000000	sw_bp_wr_cb_offs_cnt Offset counter initial value of bypass picture Cb component ring buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. Check exceptional handling in skip modes. --- MI_BP_WR_CB_OFFS_CNT --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_BP_WR_CB_OFFS_CNT_START

Address: Operational Base(0x21D01400) + offset (0x0230)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_bp_wr_cb_offs_cnt_start Offset counter value which points to the start address of the previously processed picture (bypass picture Cb component). Updated at frame end. --- MI_BP_WR_CB_OFFS_CNT_START --- Note: This register protects from non-aligned access. Refer to MI_MP_Y_BASE_AD_INIT register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_BP_WR_Y_BASE_SHD

Address: Operational Base(0x21D01400) + offset (0x0234)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_bp_wr_y_base_shd Base address of bypass picture Y component ring buffer. --- MI_BP_WR_Y_BASE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_BP_WR_Y_SIZE_SHD

Address: Operational Base(0x21D01400) + offset (0x0238)

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Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_bp_wr_y_size_shd Size of bypass picture Y component ring buffer. --- MI_BP_WR_Y_SIZE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_BP_WR_Y_OFFS_CNT_SHD

Address: Operational Base(0x21D01400) + offset (0x023C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_sp_wr_y_offs_cnt_shd Current offset counter of bypass picture Y component ring buffer for address generation Note: Soft reset will reset the contents to reset value. --- MI_BP_WR_Y_OFFS_CNT_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_BP_WR_CB_BASE_SHD

Address: Operational Base(0x21D01400) + offset (0x0240)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_bp_wr_cb_base_shd Base address of bypass picture Cb component ring buffer. --- MI_BP_WR_CB_BASE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_BP_WR_CB_SIZE_SHD

Address: Operational Base(0x21D01400) + offset (0x0244)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_bp_wr_cb_size_shd Size of bypass picture Cb component ring buffer. --- MI_BP_WR_CB_SIZE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_MI_BP_WR_CB_OFFS_CNT_SHD

Address: Operational Base(0x21D01400) + offset (0x0248)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_mp_wr_cb_offs_cnt_shd Current offset counter of bypass picture Cb component ring buffer for address generation Note: Soft reset will reset the contents to reset value. --- MI_BP_WR_CB_OFFS_CNT_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
3:0	RO	0x0	reserved

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MI_1400_MI_BP_WR_Y_BASE2

Address: Operational Base(0x21D01400) + offset (0x024C)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_bp_wr_y_base2 2nd ping pong base address of bypass picture Y component buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_BP_WR_Y_BASE2 --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details. Refer also to MI_MP_WR_Y_BASE with respect to the burst alignment restriction for AXI.
3:0	RO	0x0	reserved

MI_1400_MI_BP_WR_CB_BASE2

Address: Operational Base(0x21D01400) + offset (0x0250)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_bp_wr_cb_base2 2nd ping pong base address of bypass picture CB component buffer. Programmed value becomes effective (visible in corresponding shadow register) after a soft reset, a forced software update or an automatic configuration update. Note: Set control bit init_base_en before updating so that a forced or automatic update can take effect. --- MI_BP_WR_CB_BASE2 --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_CB_BASE register description for details. Refer also to MI_MP_WR_CB_BASE with respect to the burst alignment restriction for AXI.
3:0	RO	0x0	reserved

MI_1400_MI_MP_WR_Y_END_ADDR

Address: Operational Base(0x21D01400) + offset (0x0260)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_mp_wr_y_end_addr MP y frame end address readback, used for MP wrap debug.

MI_1400_MI_MP_WR_CB_END_ADDR

Address: Operational Base(0x21D01400) + offset (0x0264)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_mp_wr_cb_end_addr MP uv frame end address readback, used for MP wrap debug.

MI_1400_MI_SP_WR_Y_END_ADDR

Address: Operational Base(0x21D01400) + offset (0x0268)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_sp_wr_y_end_addr SP y frame end address readback, used for SP wrap debug.

MI_1400_MI_SP_WR_CB_END_ADDR

Address: Operational Base(0x21D01400) + offset (0x026C)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_sp_wr_cb_end_addr SP uv frame end address readback, used for SP wrap debug.

MI_1400_MI_BP_WR_Y_END_ADDR

Address: Operational Base(0x21D01400) + offset (0x0270)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_bp_wr_y_end_addr BP y frame end address readback, used for BP wrap debug.

MI_1400_MI_BP_WR_CB_END_ADDR

Address: Operational Base(0x21D01400) + offset (0x0274)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_bp_wr_cb_end_addr BP uv frame end address readback, used for BP wrap debug.

MI_1400_MI_MPDS_WR_Y_END_ADDR

Address: Operational Base(0x21D01400) + offset (0x0278)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_mpds_wr_y_end_addr MPDS y frame end address readback, used for MPDS wrap debug.

MI_1400_MI_MPDS_WR_CB_END_ADDR

Address: Operational Base(0x21D01400) + offset (0x027C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_mpds_wr_cb_end_addr MPDS uv frame end address readback, used for MPDS wrap debug.

MI_1400_MI_BPDS_WR_Y_END_ADDR

Address: Operational Base(0x21D01400) + offset (0x0280)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_bpds_wr_y_end_addr BPDS y frame end address readback, used for BPDS wrap debug.

MI_1400_MI_BPDS_WR_CB_END_ADDR

Address: Operational Base(0x21D01400) + offset (0x0284)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_bpds_wr_cb_end_addr BPDS uv frame end address readback, used for BPDS wrap debug.

MI_1400_MI_MPDS_WR_CTRL

Address: Operational Base(0x21D01400) + offset (0x02A0)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_mpds_wr_dis Disable of main path down sampling. 1'b1: Disable 1'b0: Enabled
30	RW	0x0	sw_mpds_ram_ckg_dis Disable of main path down sampling used memory clock gating.
29:11	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
10:8	RW	0x2	sw_mpds_wr_output_format Selects output format of main path down sampling. 3'b000: YCbCr 4:0:0 3'b001: YCbCr 4:2:0 3'b010: YCbCr 4:2:2 others: Reserved Note: - Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the main path down sampling. - If sw_mpds_wr_v_flip = 1 and yuv420 format, need to configure sw_mpds_wr_output_format = 1.
7:6	RO	0x0	reserved
5:4	RW	0x0	sw_mpds_wr_format Defines how YCbCr main down-sampling picture data is written to memory. 2'b00: Reserved 2'b01: Semi planar, for YCbCr 4:2:x 2'b10: Interleaved (combined), for YCbCr 4:2:2 only 2'b11: Reserved Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the main down-sampling path.
3:2	RO	0x0	reserved
1	RW	0x0	sw_mpds_wr_auto_update Automatic update of configuration registers for main path down sampling at frame end. 1'b1: Enabled 1'b0: Disabled
0	RW	0x0	sw_mpds_wr_enable Enables of main path down sampling for output shadow generation.

MI_1400_MI_MPDS_WR_Y_BASE

Address: Operational Base(0x21D01400) + offset (0x02A4)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_mpds_wr_y_base Base address of main path down sampling Y component ring buffer.
3:0	RO	0x0	reserved

MI_1400_MI_MPDS_WR_Y_SIZE

Address: Operational Base(0x21D01400) + offset (0x02A8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_mpds_wr_y_size Size of main path down sampling Y component ring buffer
3:0	RO	0x0	reserved

MI_1400_MI_MPDS_WR_Y_OFFS_CNT

Address: Operational Base(0x21D01400) + offset (0x02AC)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28:4	RW	0x0000000	sw_mpds_wr_y_offs_cnt Offset counter initial value of main path down sampling Y component ring buffer.
3:0	RO	0x0	reserved

MI_1400_MI_MPDS_WR_Y_OFFS_CNT_START

Address: Operational Base(0x21D01400) + offset (0x02B0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_mpds_wr_y_offs_cnt_start Offset counter value which points to the start address of the previously processed picture (main path down sampling Y component). Updated at frame end. Note: A soft reset resets the contents to the reset value.
3:0	RO	0x0	reserved

MI_1400_MI_MPDS_WR_Y_LLENGTH

Address: Operational Base(0x21D01400) + offset (0x02B4)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	sw_mpds_wr_y_llength_tmp Line length of main path down sampling Y component in pixel, also known as line stride. If no line stride is used, line length must match image width.

MI_1400_MI_MPDS_WR_Y_PIC_WIDTH

Address: Operational Base(0x21D01400) + offset (0x02B8)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	sw_mpds_wr_y_pic_width Image width of the main path down sampling Y component.

MI_1400_MI_MPDS_WR_Y_PIC_HEIGHT

Address: Operational Base(0x21D01400) + offset (0x02BC)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	sw_mpds_wr_y_pic_height Image height of the y component in pixel.

MI_1400_MI_MPDS_WR_Y_PIC_SIZE

Address: Operational Base(0x21D01400) + offset (0x02C0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	sw_mpds_wr_y_pic_size Image size of the Y component picture in pixel which has to be the Y line length multiplied by the Y image height (mpds_y_llength * mpds_y_pic_height).

MI_1400_MI_MPDS_WR_CB_BASE

Address: Operational Base(0x21D01400) + offset (0x02C4)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_mpds_wr_cb_base Base address of main path down sampling UV component ring buffer.

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Bit	Attr	Reset Value	Description
3:0	RO	0x0	reserved

MI_1400_MI_MPDS_WR_CB_SIZE

Address: Operational Base(0x21D01400) + offset (0x02C8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RW	0x000000	sw_mpds_wr_cb_size Size of main path down sampling UV component ring buffer
3:0	RO	0x0	reserved

MI_1400_MI_MPDS_WR_CB_OFFS_CNT

Address: Operational Base(0x21D01400) + offset (0x02CC)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RW	0x000000	sw_mpds_wr_cb_offs_cnt Offset counter initial value of main path down sampling UV component ring buffer.
3:0	RO	0x0	reserved

MI_1400_MI_MPDS_WR_CB_OFFS_CNT_START

Address: Operational Base(0x21D01400) + offset (0x02D0)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_mpds_wr_cb_offs_cnt_start Offset counter value which points to the start address of the previously processed picture (main path down sampling UV component). Updated at frame end. Note: A soft reset resets the contents to the reset value.
3:0	RO	0x0	reserved

MI_1400_MI_MPDS_WR_Y_BASE_SHD

Address: Operational Base(0x21D01400) + offset (0x02D4)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_mpds_wr_y_base_shd Base address shadow of main path down sampling Y component ring buffer.
3:0	RO	0x0	reserved

MI_1400_MI_MPDS_WR_Y_SIZE_SHD

Address: Operational Base(0x21D01400) + offset (0x02D8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_mpds_wr_y_size_shd Size of main path down sampling Y component ring buffer.
3:0	RO	0x0	reserved

MI_1400_MI_MPDS_WR_Y_OFFS_CNT_SHD

Address: Operational Base(0x21D01400) + offset (0x02DC)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_mpds_wr_y_offs_cnt_shd Current offset counter of main path down sampling Y component ring buffer for address generation.
3:0	RO	0x0	reserved

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MI_1400_MI_MPDS_WR_CB_BASE_SHD

Address: Operational Base(0x21D01400) + offset (0x02E0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_mps_wr_cb_base_shd Base address of main path down sampling UV component ring buffer.
3:0	RO	0x0	reserved

MI_1400_MI_MPDS_WR_CB_SIZE_SHD

Address: Operational Base(0x21D01400) + offset (0x02E4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_mpds_wr_cr_size_shd Size of main path down sampling UV component ring buffer.
3:0	RO	0x0	reserved

MI_1400_MI_MPDS_WR_CB_OFFS_CNT_SHD

Address: Operational Base(0x21D01400) + offset (0x02E8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_mpds_wr_cb_offs_cnt_shd Current offset counter of main path down sampling UV component ring buffer for address generation.
3:0	RO	0x0	reserved

MI_1400_MI_BPDS_WR_CTRL

Address: Operational Base(0x21D01400) + offset (0x02F0)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_bpds_wr_dis Disable of bypass path down sampling. 1'b1: Disable 1'b0: Enabled
30	RW	0x0	sw_bpds_ram_ckg_dis Disable of bypass path down sampling used memory clock gating.
29:11	RO	0x00000	reserved
10:8	RW	0x2	sw_bpds_wr_output_format Selects output format of bypass path down sampling. 3'b000: YCbCr 4:0:0 3'b001: YCbCr 4:2:0 3'b010: YCbCr 4:2:2 Others: Reserved Note: - Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the bypass path down sampling. - If sw_bpds_wr_v_flip = 1 and yuv420 format, need to configure sw_bpds_wr_output_format = 1.
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:4	RW	0x0	sw_bpds_wr_format Defines how YCbCr bypass down-sampling picture data is written to memory. 2'b00: Reserved 2'b01: Semi planar, for YCbCr 4:2:x 2'b10: Interleaved (combined), for YCbCr 4:2:2 only 2'b11: Reserved Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the bypass down-sampling path.
3	RW	0x0	sw_bpsp_ds_mux_en Down sampling input mux enable, from bypass path or self path. 1'b1: BPDS from self path 1'b0: BPDS from bypass path
2	RO	0x0	reserved
1	RW	0x0	sw_bpds_wr_auto_update Automatic update of configuration registers for bypass path down sampling at frame end. 1'b1: Enabled 1'b0: Disabled
0	RW	0x0	sw_bpds_wr_enable Enables of bypass path down sampling for output shadow generation.

MI_1400_MI_BPDS_WR_Y_BASE

Address: Operational Base(0x21D01400) + offset (0x02F4)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_bpds_wr_y_base Base address of bypass path down sampling Y component ring buffer.
3:0	RO	0x0	reserved

MI_1400_MI_BPDS_WR_Y_SIZE

Address: Operational Base(0x21D01400) + offset (0x02F8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_bpds_wr_y_size Size of bypass path down sampling Y component ring buffer
3:0	RO	0x0	reserved

MI_1400_MI_BPDS_WR_Y_OFFS_CNT

Address: Operational Base(0x21D01400) + offset (0x02FC)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_bpds_wr_y_offs_cnt Offset counter initial value of bypass path down sampling Y component ring buffer.
3:0	RO	0x0	reserved

MI_1400_MI_BPDS_WR_Y_OFFS_CNT_START

Address: Operational Base(0x21D01400) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28:4	RO	0x0000000	sw_bpds_wr_y_offs_cnt_start Offset counter value which points to the start address of the previously processed picture (bypass path down sampling Y component). Updated at frame end. Note: A soft reset resets the contents to the reset value.
3:0	RO	0x0	reserved

MI_1400_MI_BPDS_WR_Y_LLENGTH

Address: Operational Base(0x21D01400) + offset (0x0304)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	sw_bpds_wr_y_llength_tmp Line length of bypass path down sampling Y component in pixel, also known as line stride. If no line stride is used, line length must match image width.

MI_1400_MI_BPDS_WR_Y_PIC_WIDTH

Address: Operational Base(0x21D01400) + offset (0x0308)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	sw_bpds_wr_y_pic_width Image width of the bypass path down sampling Y component.

MI_1400_MI_BPDS_WR_Y_PIC_HEIGHT

Address: Operational Base(0x21D01400) + offset (0x030C)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	sw_bpds_wr_y_pic_height Image height of the y component in pixel.

MI_1400_MI_BPDS_WR_Y_PIC_SIZE

Address: Operational Base(0x21D01400) + offset (0x0310)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	sw_bpds_wr_y_pic_size Image size of the Y component picture in pixel which has to be the Y line length multiplied by the Y image height (bpds_y_llength * bpds_y_pic_height).

MI_1400_MI_BPDS_WR_CB_BASE

Address: Operational Base(0x21D01400) + offset (0x0314)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_bpds_wr_cb_base Base address of bypass path down sampling UV component ring buffer.
3:0	RO	0x0	reserved

MI_1400_MI_BPDS_WR_CB_SIZE

Address: Operational Base(0x21D01400) + offset (0x0318)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RW	0x000000	sw_bpds_wr_cb_size Size of bypass path down sampling UV component ring buffer
3:0	RO	0x0	reserved

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MI_1400_MI_BPDS_WR_CB_OFFS_CNT

Address: Operational Base(0x21D01400) + offset (0x031C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RW	0x000000	sw_bpds_wr_cb_offs_cnt Offset counter initial value of bypass path down sampling UV component ring buffer.
3:0	RO	0x0	reserved

MI_1400_MI_BPDS_WR_CB_OFFS_CNT_START

Address: Operational Base(0x21D01400) + offset (0x0320)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_bpds_wr_cb_offs_cnt_start Offset counter value which points to the start address of the previously processed picture (bypass path down sampling UV component). Updated at frame end. Note: A soft reset resets the contents to the reset value.
3:0	RO	0x0	reserved

MI_1400_MI_BPDS_WR_Y_BASE_SHD

Address: Operational Base(0x21D01400) + offset (0x0324)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_bpds_wr_y_base_shd Base address shadow of bypass path down sampling Y component ring buffer.
3:0	RO	0x0	reserved

MI_1400_MI_BPDS_WR_Y_SIZE_SHD

Address: Operational Base(0x21D01400) + offset (0x0328)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_bpds_wr_y_size_shd Size of bypass path down sampling Y component ring buffer.
3:0	RO	0x0	reserved

MI_1400_MI_BPDS_WR_Y_OFFS_CNT_SHD

Address: Operational Base(0x21D01400) + offset (0x032C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RO	0x0000000	sw_bpds_wr_y_offs_cnt_shd Current offset counter of bypass path down sampling Y component ring buffer for address generation.
3:0	RO	0x0	reserved

MI_1400_MI_BPDS_WR_CB_BASE_SHD

Address: Operational Base(0x21D01400) + offset (0x0330)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_bps_wr_cb_base_shd Base address of bypass path down sampling UV component ring buffer.
3:0	RO	0x0	reserved

MI_1400_MI_BPDS_WR_CB_SIZE_SHD

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Address: Operational Base(0x21D01400) + offset (0x0334)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_bpds_wr_cr_size_shd Size of bypass path down sampling UV component ring buffer.
3:0	RO	0x0	reserved

MI_1400_MI_BPDS_WR_CB_OFFS_CNT_SHD

Address: Operational Base(0x21D01400) + offset (0x0338)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:4	RO	0x000000	sw_bpds_wr_cb_offs_cnt_shd Current offset counter of bypass path down sampling UV component ring buffer for address generation.
3:0	RO	0x0	reserved

MI_1400_MI_WR_CTRL2

Address: Operational Base(0x21D01400) + offset (0x0400)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_itself_force_pro_dis Itself force update protection disable
30	RO	0x0	reserved
29	RW	0x0	sw_path_sel_fix_dis MI path select fix disable 1'b0: enable 1'b1: disable If sw_path_sel_fix_dis is 1, maybe MI path enable input shadow update fail when When auto-update and self-update are used together.
28	WO	0x0	sys_rxirldc_force_upd IR-LDCV read update
27	RO	0x0	reserved
26	WO	0x0	sys_bpdsself_force_upd Force update of configuration registers for bypass path down sampling DMA write.
25	WO	0x0	sys_mpdsself_force_upd Force update of configuration registers for main path down sampling DMA write.
24	W1C	0x0	sys_bay3d_dsself_force_upd Force update of configuration registers for bay3dnr down scale frame DMA write.
23	W1C	0x0	sys_bay3d_curself_force_upd Force update of configuration registers for bay3dnr current frame DMA write.
22	W1C	0x0	sys_bay3d_iirself_force_upd Force update of configuration registers for bay3dnr iir frame DMA write.
21	W1C	0x0	sys_gainself_force_upd Force update of configuration registers for gain DMA write.
20	W1C	0x0	sys_dbr_3a_self_force_upd Force update of configuration registers for debayer or 3a DMA write.
19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18	RW	0x0	sw_bay3d_ds_wr_auto_upd Automatic update of configuration registers for bay3d down scale write at frame end. 1'b1: Enabled 1'b0: Disabled
17	RW	0x0	sw_bay3d_cur_wr_auto_upd Automatic update of configuration registers for bay3d current write at frame end. 1'b1: Enabled 1'b0: Disabled
16	RW	0x0	sw_bay3d_iir_wr_auto_upd Automatic update of configuration registers for bay3d iir write at frame end. 1'b1: Enabled 1'b0: Disabled
15	RW	0x0	sw_mi_wr_id_poll_dis MI write axi-id polling disable, backdoor
14	WO	0x0	sys_mi_wr_id_poll_clr MI write axi-id polling clear counter
13	RW	0x0	sw_gain_wr_auto_upd Automatic update of configuration registers for gain write at frame end. 1'b1: Enabled 1'b0: Disabled
12	RW	0x0	sw_gain_wr_pingpong_en Pingpong mode of configuration registers for gain write at frame end. 1'b1: Enabled 1'b0: Disabled
11	WO	0x0	sys_rxaiisp_force_upd AI-ISP read update
10	RW	0x1	sw_w3a_wr_auto_upd Automatic update of configuration registers for 3a write at frame end. 1'b1: Enabled 1'b0: Disabled
9:8	RO	0x0	reserved
7	WO	0x0	sys_rxb3d_force_upd Force update of configuration registers for bay3d DMA read.
6	WO	0x0	sys_bpself_force_upd Force update of configuration registers for bypass path DMA write.
5	WO	0x0	sys_spself_force_upd Force update of configuration registers for self path DMA write.
4	WO	0x0	sys_mpself_force_upd Force update of configuration registers for main path DMA write.
3:0	RO	0x0	reserved

MI_1400_MI_WR_ID2

Address: Operational Base(0x21D01400) + offset (0x0404)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	sw_bay3d_iir_wr_axi_id Bay3d iir write id, read only
27:24	RO	0x0	sw_gain_wr_axi_id Gain write id, read only

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Bit	Attr	Reset Value	Description
23:20	RO	0x0	sw_dbr_wr_axi_id Debayer-in write id, read only
19:0	RO	0x00000	reserved

MI_1400_MI_RD_CTRL2

Address: Operational Base(0x21D01400) + offset (0x0408)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_mi_new_rw_burst_dis 1'b0: Self-adaption enable 1'b1: Self-adaption disable
30	RW	0x0	sw_raw_rd_old Old-mi read. 1'b0: Disable 1'b1: Enable
29	RO	0x0	reserved
28	RW	0x0	sw_rw_mi_group_fix Fix group mode, backdoor
27	RW	0x0	sw_lut_raddr_shd_dis lut read address shadow disable 1'b1: disable 1'b0: enable
26:24	RO	0x0	reserved
23:22	RW	0x2	sw_rawx_rd_burst_len Burst length for raw data affecting DMA read port. 2'b00: 4-beat bursts 2'b01: 8-beat bursts 2'b10: 16-beat bursts 2'b11: 2-beat bursts Ignored if 8- or 16-beat bursts are not supported. Note: Programmed value becomes effective immediately. So read to the register only if no picture data is sent to the main and self path.
21:20	RW	0x2	sw_rawx_wr_burst_len Burst length for raw data affecting DMA write port. 2'b00: 4-beat bursts 2'b01: 8-beat bursts 2'b10: 16-beat bursts 2'b11: 2-beat bursts Ignored if 8- or 16-beat bursts are not supported. Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the main and self path.
19:18	RW	0x1	sw_rd_rawx_group_mode Group mode for raw data affecting DMA read port. 2'b00: BurstN*4 2'b01: BurstN*3 2'b10: BurstN*2 2'b11: BurstN*1 Note: Programmed value becomes effective immediately. So read to the register only if no picture data is sent to the main and self path.

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Bit	Attr	Reset Value	Description
17:16	RW	0x1	sw_wr_rawx_group_mode Group mode for raw data affecting DMA write port. 2'b00: BurstN*4 2'b01: BurstN*3 2'b10: BurstN*2 2'b11: BurstN*1 Note: Programmed value becomes effective immediately. So write to the register only if no picture data is sent to the main and self path.
15:14	RO	0x0	reserved
13:10	RW	0x2	sw_mi_dgb_rw_id AXI debug read/write ID, for AXI command and data counter.
9:7	RO	0x0	reserved
6	RW	0x0	sw_bay3d_ds_rw_one_addr_en DDR address of debayer-in read is the same to bay3d down scale write
5	RW	0x0	sw_bay3d_cur_rw_one_addr_en DDR address of debayer-in read is the same to bay3d current write
4	RW	0x0	sw_bay3d_iir_rw_one_addr_en DDR address of debayer-in read is the same to bay3d iir write
3	RW	0x0	sw_dbr_rw_one_addr_en DDR address of debayer-in read is the same to debayer-in write
2	RW	0x0	sw_raws_rw_one_addr_en DDR address of raw2 rx is the same to raw2 tx
1	RW	0x0	sw_raw1_rw_one_addr_en DDR address of raw1 rx is the same to raw1 tx
0	RW	0x0	sw_raw0_rw_one_addr_en DDR address of raw0 rx is the same to raw0 tx

MI_1400_MI_RD_ID

Address: Operational Base(0x21D01400) + offset (0x040C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	sw_bay3d_ds_rd_axi_id Bay3d down scale read id, read only
27:24	RO	0x0	sw_bay3d_cur_rd_axi_id Bay3d current read id, read only
23:20	RO	0x0	sw_bay3d_iir_rd_axi_id Bay3d iir read id, read only
19:16	RO	0x0	sw_lut_rd_axi_id Mipi lut read id, read only
15:12	RO	0x0	sw_dbr_rd_axi_id Mipi debayer-in read id, read only
11:8	RO	0x0	sw_raws_rd_axi_id Mipi raw2 rx id, read only
7:4	RO	0x0	sw_raw1_rd_axi_id Mipi raw1 rx id, read only
3:0	RO	0x0	sw_raw0_rd_axi_id Mipi raw0 rx id, read only

MI_1400_MI_WR_CTRL2_SHD

Address: Operational Base(0x21D01400) + offset (0x0410)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29	RO	0x0	stat_bpds_en_out_shd Bypass path down sampling output enable shadow in isp_mi.
28	RO	0x0	stat_mpds_en_out_shd Main path down sampling output enable shadow in isp_mi.
27	RO	0x0	reserved
26	RO	0x0	stat_bay3d_ds_wr_en_out_shd Bay3dnr down-sampling path output enable shadow in isp_mi.
25	RO	0x0	stat_bay3d_iir_wr_en_out_shd Bay3dnr iir path output enable shadow in isp_mi.
24	RO	0x0	stat_bay3d_cur_wr_en_out_shd Bay3dnr current path output enable shadow in isp_mi.
23	RO	0x0	reserved
22	RO	0x0	stat_gain_wr_en_out_shd Gain path output enable shadow in isp_mi.
21	RO	0x0	stat_dbr_wr_en_out_shd Debayer mi-mux path output enable shadow in isp_mi.
20	RO	0x0	stat_bp_en_out_shd Bypass path output enable shadow in isp_mi.
19:14	RO	0x00	reserved
13	RO	0x0	stat_bpds_en_in_shd Bypass path down sampling input enable shadow in isp_mi.
12	RO	0x0	stat_mpds_en_in_shd Main path down sampling input enable shadow in isp_mi.
11	RO	0x0	reserved
10	RO	0x0	stat_bay3d_ds_wr_en_in_shd Bay3dnr down-sampling path input enable shadow in isp_mi.
9	RO	0x0	stat_bay3d_iir_wr_en_in_shd Bay3dnr iir path input enable shadow in isp_mi.
8	RO	0x0	stat_bay3d_cur_wr_en_in_shd Bay3dnr current path input enable shadow in isp_mi.
7	RO	0x0	reserved
6	RO	0x0	stat_gain_wr_en_in_shd Gain path input enable shadow in isp_mi.
5	RO	0x0	stat_dbr_wr_en_in_shd Debayer mi-mux path input enable shadow in isp_mi.
4	RO	0x0	stat_bp_en_in_shd Bypass path input enable shadow in isp_mi.
3:0	RO	0x0	reserved

MI_1400_MI_WR_WRAP_CTRL

Address: Operational Base(0x21D01400) + offset (0x0414)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	sw_bpds_wr_frmend_upd_dis Frame end address shadow update disable of bypass path down sampling.
27	RW	0x0	sw_mpds_wr_frmend_upd_dis Frame end address shadow update disable of main path down sampling.
26	RW	0x0	sw_bp_wr_frmend_upd_dis Frame end address shadow update disable of bypass path.
25	RW	0x0	sw_sp_wr_frmend_upd_dis Frame end address shadow update disable of self path.
24	RW	0x0	sw_mp_wr_frmend_upd_dis Frame end address shadow update disable of main path.

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Bit	Attr	Reset Value	Description
23:14	RO	0x000	reserved
13	RW	0x0	sw_bpds_dynamic_upd_addr Wrap dynamic address update enable of bypass path down sampling.
12	RW	0x0	sw_mpds_dynamic_upd_addr Wrap dynamic address update enable of main path down sampling.
11	RO	0x0	reserved
10	RW	0x0	sw_bp_dynamic_upd_addr Wrap dynamic address update enable of bypass path.
9	RW	0x0	sw_sp_dynamic_upd_addr Wrap dynamic address update enable of self path.
8	RW	0x0	sw_mp_dynamic_upd_addr Wrap dynamic address update enable of main path.
7:6	RO	0x0	reserved
5	RW	0x1	sw_bpds_wr_init_offset_en Enables updating of the offset counters shadow registers for bypass path down sampling to the programmed register initial values. MI_MPDS_Y/CB/CR_OFFS_CNT_INIT -> MI_MPDS_Y/CB/CR_OFFS_CNT_SHD The update will be executed either when a forced software update occurs (in register MI_INIT bit cfg_upd = 1) or when an automatic configuration update signal arrives at the MI input port. The latter is split into bypass path down sampling picture. So only the corresponding bypass path down sampling shadow registers are affected. After a picture skip has been performed init_offset_en selects between skip restart and skip initial mode (see bit skip in register MI_INIT).
4	RW	0x1	sw_mpds_wr_init_offset_en Enables updating of the offset counters shadow registers for main path down sampling to the programmed register initial values. MI_MPDS_Y/CB/CR_OFFS_CNT_INIT -> MI_MPDS_Y/CB/CR_OFFS_CNT_SHD The update will be executed either when a forced software update occurs (in register MI_INIT bit cfg_upd = 1) or when an automatic configuration update signal arrives at the MI input port. The latter is split into main path down sampling picture. So only the corresponding main path down sampling shadow registers are affected. After a picture skip has been performed init_offset_en selects between skip restart and skip initial mode (see bit skip in register MI_INIT).
3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2	RW	0x1	sw_bp_wr_init_offset_en Enables updating of the offset counters shadow registers for bypass path to the programmed register initial values. MI_BP_Y/CB/CR_OFFS_CNT_INIT ->MI_BP_Y/CB/CR_OFFS_CNT_SHD The update will be executed either when a forced software update occurs (in register MI_INIT bit cfg_upd = 1) or when an automatic configuration update signal arrives at the MI input port. The latter is split into bypass path picture. So only the corresponding bypass path shadow registers are affected. After a picture skip has been performed init_offset_en selects between skip restart and skip initial mode (see bit skip in register MI_INIT).
1	RW	0x1	sw_sp_wr_init_offset_en Enables updating of the offset counters shadow registers for self path to the programmed register initial values. MI_SP_Y/CB/CR_OFFS_CNT_INIT ->MI_SP_Y/CB/CR_OFFS_CNT_SHD The update will be executed either when a forced software update occurs (in register MI_INIT bit cfg_upd = 1) or when an automatic configuration update signal arrives at the MI input port. The latter is split into self path picture. So only the corresponding self path shadow registers are affected. After a picture skip has been performed init_offset_en selects between skip restart and skip initial mode (see bit skip in register MI_INIT).
0	RW	0x1	sw_mp_wr_init_offset_en Enables updating of the offset counters shadow registers for main path to the programmed register initial values. MI_MP_Y/CB/CR_OFFS_CNT_INIT ->MI_MP_Y/CB/CR_OFFS_CNT_SHD The update will be executed either when a forced software update occurs (in register MI_INIT bit cfg_upd = 1) or when an automatic configuration update signal arrives at the MI input port. The latter is split into main path picture. So only the corresponding main path shadow registers are affected. After a picture skip has been performed init_offset_en selects between skip restart and skip initial mode (see bit skip in register MI_INIT).

MI_1400_MI_WR_VFLIP_CTRL

Address: Operational Base(0x21D01400) + offset (0x0418)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x0	sw_bpds_wr_v_flip Vertical flipping of bypass down-sampling picture. For Y component the line length in 4:2:x planar mode must be a multiple of 16. 1'b1: Enabled 1'b0: Disabled Note: - Readback is shadow register. - If sw_bpds_wr_v_flip = 1, need to configure sw_bpds_wr_y_pic_size.

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Bit	Attr	Reset Value	Description
4	RW	0x0	sw_mpds_wr_v_flip Vertical flipping of main down-sampling picture. For Y component the line length in 4:2:x planar mode must be a multiple of 16. 1'b1: Enabled 1'b0: Disabled Note: - Readback is shadow register. - If sw_mpds_wr_v_flip = 1, need to configure sw_mpds_wr_y_pic_size.
3	RO	0x0	reserved
2	RW	0x0	sw_bp_wr_v_flip Vertical flipping of bypass picture. For Y component the line length in 4:2:x planar mode must be a multiple of 16. 1'b1: Enabled 1'b0: Disabled Note: - Readback is shadow register. - If sw_bp_wr_v_flip = 1, need to configure sw_bp_wr_y_pic_size.
1	RW	0x0	sw_sp_wr_v_flip Vertical flipping of mainself picture. For Y component the line length in 4:2:x planar mode must be a multiple of 16. 1'b1: Enabled 1'b0: Disabled Note: - Readback is shadow register. - If sw_sp_wr_v_flip = 1, need to configure sw_sp_wr_y_pic_size.
0	RW	0x0	sw_mp_wr_v_flip Vertical flipping of main picture. For Y component the line length in 4:2:x planar mode must be a multiple of 16. 1'b1: Enabled 1'b0: Disabled Note: - Readback is shadow register. - If sw_mp_wr_v_flip = 1, need to configure sw_mp_wr_y_pic_size.

MI_1400_RAW0_RD_BASE

Address: Operational Base(0x21D01400) + offset (0x0470)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_raw0_rd_base Base address of raw0 rx data ring buffer.
3:0	RO	0x0	reserved

MI_1400_RAW0_RD_LENGTH

Address: Operational Base(0x21D01400) + offset (0x0474)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_raw0_rd_length Line length of raw0 rx in pixel, also known as line stride.

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MI_1400_RAW0_RD_BASE_SHD

Address: Operational Base(0x21D01400) + offset (0x0478)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_raw0_rd_base_shd Base shadow address of raw0 rx data ring buffer.
3:0	RO	0x0	reserved

MI_1400_RAW0_RD_SIZE

Address: Operational Base(0x21D01400) + offset (0x047C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_raw0_rd_frmsize Frame size of raw0 read, only used in wrap mode.

MI_1400_RAW1_RD_BASE

Address: Operational Base(0x21D01400) + offset (0x0480)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_raw1_rd_base Base address of raw1 rx data ring buffer.
3:0	RO	0x0	reserved

MI_1400_RAW1_RD_LENGTH

Address: Operational Base(0x21D01400) + offset (0x0484)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_raw1_rd_length Line length of raw1 rx in pixel, also known as line stride.

MI_1400_RAW1_RD_BASE_SHD

Address: Operational Base(0x21D01400) + offset (0x0488)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	sw_raw1_rd_base_shd Base shadow address of raw1 rx data ring buffer.
3:0	RO	0x0	reserved

MI_1400_RAW1_RD_SIZE

Address: Operational Base(0x21D01400) + offset (0x048C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_raw1_rd_frmsize Frame size of raw1 read, only used in wrap mode.

MI_1400_RAWS_RD_BASE

Address: Operational Base(0x21D01400) + offset (0x0490)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_raws_rd_base Base address of raws rx data ring buffer.
3:0	RO	0x0	reserved

MI_1400_RAWS_RD_LENGTH

Address: Operational Base(0x21D01400) + offset (0x0494)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_raws_rd_length Line length of raws rx in pixel, also known as line stride.

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MI_1400_RAWS_RD_BASE_SHD

Address: Operational Base(0x21D01400) + offset (0x0498)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_raws_rd_base_shd Base shadow address of raws rx data ring buffer.
3:0	RO	0x0	reserved

MI_1400_RAWS_RD_SIZE

Address: Operational Base(0x21D01400) + offset (0x049C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_raws_rd_frmsize Frame size of raws read, only used in wrap mode.

MI_1400_RAW_RD_WRAP_CTRL

Address: Operational Base(0x21D01400) + offset (0x04A0)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:8	RW	0x0	sw_raw_rd_thred_lcnt Read threshold line counter, for wrap. (isp_read_lcnt + sw_raw_rd_thred_lcnt) < vicap_write_lcnt
7:6	RO	0x0	reserved
5	RW	0x0	sw_raws_rd_hold_dis Raws dma read hold disable, waiting vicap write for wrap
4	RW	0x0	sw_raw0_rd_hold_dis Raw0 dma read hold disable, waiting vicap write for wrap
3:2	RO	0x0	reserved
1	RW	0x0	sw_raws_rd_init_dis Raws dma read init disable, 1'b1 for wrap address continue. Note: Readback is shadow registger.
0	RW	0x0	sw_raw0_rd_init_dis Raw0 dma read init disable, 1'b1 for wrap address continue. Note: Readback is shadow registger.

MI_1400_RAWS_RD_OFFS_BASE

Address: Operational Base(0x21D01400) + offset (0x04A4)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_raws_rd_offs_base Raws offset address for two sensors slice boundary expand. Note: Readback is shadow register.
3:0	RO	0x0	reserved

MI_1400_RAW0_RD_WRAP_DEBUG0

Address: Operational Base(0x21D01400) + offset (0x04B0)

Bit	Attr	Reset Value	Description
31	RO	0x0	ro_raw0_vicap_overflow Vicap L-frame dma write overflow flag
30	RO	0x0	reserved
29:16	RO	0x0000	ro_raw0_rd_vcnt ISP L-frame(raw0) dma read line counter
15:13	RO	0x0	reserved
12:0	RO	0x0000	ro_raw0_vicap_vcnt Vicap L-frame dma write line counter

MI_1400_RAW0_RD_WRAP_DEBUG1

Address: Operational Base(0x21D01400) + offset (0x04B4)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_raw0_rd_cur_pos Raw0 dma read current position address

MI_1400_RAWS_RD_WRAP_DEBUG0

Address: Operational Base(0x21D01400) + offset (0x04B8)

Bit	Attr	Reset Value	Description
31	RO	0x0	ro_raws_vicap_overflow Vicap S-frame dma write overflow flag
30	RO	0x0	reserved
29:16	RO	0x0000	ro_raws_rd_vcnt ISP raws dma read line counter
15:13	RO	0x0	reserved
12:0	RO	0x0000	ro_raws_vicap_vcnt Vicap S-frame dma write line counter

MI_1400_RAWS_RD_WRAP_DEBUG1

Address: Operational Base(0x21D01400) + offset (0x04BC)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_raws_rd_cur_pos Raws dma read current position address

MI_1400_LUT_CAC_RD_BASE

Address: Operational Base(0x21D01400) + offset (0x0530)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_caclut_rd_base Base address of cac lut read data ring buffer.
3:0	RO	0x0	reserved

MI_1400_LUT_CAC_RD_H_WSIZE

Address: Operational Base(0x21D01400) + offset (0x0534)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	sw_cac_lut_h_wsize Cac lut horizontal size, word unit cac_wsize = bigmode_en ? (pic_width+126)>>7 : (pic_width+62)>>6, lut_h_wsize = cac_wsize*9

MI_1400_LUT_CAC_RD_V_SIZE

Address: Operational Base(0x21D01400) + offset (0x0538)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_cac_lut_v_size Cac lut vertical size cac_hsize = bigmode_en ? (pic_height+126)>>7 : (pic_height+62)>>6, lut_v_size = cac_hsize*2

MI_1400_LUT_3D_RD_BASE

Address: Operational Base(0x21D01400) + offset (0x0540)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_3dlut_rd_base Base address of 3d lut read data ring buffer.
3:0	RO	0x0	reserved

MI_1400_LUT_LSC_RD_BASE

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Address: Operational Base(0x21D01400) + offset (0x0544)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_lsclut_rd_base Base address of lsc lut read data ring buffer.
3:0	RO	0x0	reserved

MI_1400_LUT_LDCH_RD_BASE

Address: Operational Base(0x21D01400) + offset (0x0548)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_ldch_rd_base Base address of ldch lut read data ring buffer.
3:0	RO	0x0	reserved

MI_1400_LUT_3D_RD_WSIZE

Address: Operational Base(0x21D01400) + offset (0x0550)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x2d9	sw_3d_lut_wsize 3d lut actual size, word unit

MI_1400_LUT_LSC_RD_WSIZE

Address: Operational Base(0x21D01400) + offset (0x0554)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	sw_lsc_lut_wsize Lsc lut actual size, word unit

MI_1400_LUT_LDCH_RD_H_WSIZE

Address: Operational Base(0x21D01400) + offset (0x0558)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	sw_ldch_lut_h_wsize Ldch lut horizontal size, word unit (((pic_width+15)/16+1)+1)/2

MI_1400_LUT_LDCH_RD_V_SIZE

Address: Operational Base(0x21D01400) + offset (0x055C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_ldch_lut_v_size Ldch lut vertical size (pic_height+7)/8+1

MI_1400_AIISP_GAIN_RD_HV_SIZE

Address: Operational Base(0x21D01400) + offset (0x0560)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:13	RW	0x0000	sw_aiisp_gain_rd_vsize AI-ISP gain read vertical size, and 1/2 down-sampling
12:0	RW	0x0000	sw_aiisp_gain_rd_wsize AI-ISP gain read horizontal word size, and 1/8 down-sampling gain_data[31:0] = [6'b0, wgt[5:0], w1[5:0], w0[5:0], gain[7:0]]

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MI_1400_W3A_WR_SIZE

Address: Operational Base(0x21D01400) + offset (0x0564)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_dbr_wr_size Size of debayer-in write data ring buffer.
3:0	RO	0x0	reserved

MI_1400_W3A_WR_LENGTH

Address: Operational Base(0x21D01400) + offset (0x0568)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RW	0x000	sw_w3a_wr_length Line length of 3a write in pixel, also known as line stride. If no line stride is used, line length must match image width.
3:0	RO	0x0	reserved

MI_1400_W3A_WR_BASE_SHD

Address: Operational Base(0x21D01400) + offset (0x056C)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	w3a_wr_base_shd Base address of 3a write data ring buffer. --- W3A_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to W3A_WR_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_AIISP_RD_BASE

Address: Operational Base(0x21D01400) + offset (0x0570)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_aiisp_rd_base Base address of ai-isp data read data ring buffer.
3:0	RO	0x0	reserved

MI_1400_AIISP_RD_LENGTH

Address: Operational Base(0x21D01400) + offset (0x0574)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_aiisp_rd_length Line length of ai-isp read in pixel, also known as line stride.

MI_1400_AIISP_RD_BASE_SHD

Address: Operational Base(0x21D01400) + offset (0x0578)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	aiisp_rd_base_shd Base shadow address of ai-isp data read data ring buffer.
3:0	RO	0x0	reserved

MI_1400_W3A_WR_BASE

Address: Operational Base(0x21D01400) + offset (0x057C)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_w3a_wr_base Base shadow address of 3a write data ring buffer.
3:0	RO	0x0	reserved

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MI_1400_GAIN_WR_BASE

Address: Operational Base(0x21D01400) + offset (0x0580)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_gain_wr_base Base address of gain write data ring buffer.
3:0	RO	0x0	reserved

MI_1400_GAIN_WR_SIZE

Address: Operational Base(0x21D01400) + offset (0x0584)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_gain_wr_size Size of gain write data ring buffer.
3:0	RO	0x0	reserved

MI_1400_GAIN_WR_LENGTH

Address: Operational Base(0x21D01400) + offset (0x0588)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RW	0x000	sw_gain_wr_length Line length of gain write in pixel, also known as line stride. If no line stride is used, line length must match image width.
3:0	RO	0x0	reserved

MI_1400_GAIN_WR_BASE2

Address: Operational Base(0x21D01400) + offset (0x058C)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_gain_wr_base2 Base address of gain write data ring buffer.
3:0	RO	0x0	reserved

MI_1400_GAIN_WR_BASE_SHD

Address: Operational Base(0x21D01400) + offset (0x0590)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	gain_wr_base_shd Base address of gain write data ring buffer. --- GAIN_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to GAIN_WR_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_BAY3D_IIR_WR_BASE

Address: Operational Base(0x21D01400) + offset (0x05A0)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_bay3d_iir_wr_base Base address of bayer 3dnr iir write data ring buffer.
3:0	RO	0x0	reserved

MI_1400_BAY3D_IIR_WR_SIZE

Address: Operational Base(0x21D01400) + offset (0x05A4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_bay3d_iir_wr_size Size of bayer 3dnr iir write data ring buffer.
3:0	RO	0x0	reserved

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MI_1400_BAY3D_IIR_WR_LENGTH

Address: Operational Base(0x21D01400) + offset (0x05A8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RW	0x000	sw_bay3d_iir_wr_length Line length of bayer 3dnr iir write in pixel, also known as line stride. If no line stride is used, line length must match image width.
3:0	RO	0x0	reserved

MI_1400_BAY3D_IIR_WR_BASE_SHD

Address: Operational Base(0x21D01400) + offset (0x05AC)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	bay3d_wr_iir_base_shd Base address of bayer 3dnr iir write data ring buffer. --- BAY3D_IIR_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to BAY3D_IIR_WR_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_BAY3D_IIR_RD_BASE

Address: Operational Base(0x21D01400) + offset (0x05B0)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_bay3d_iir_rd_base Base address of bayer 3dnr iir read data ring buffer.
3:0	RO	0x0	reserved

MI_1400_BAY3D_IIR_RD_LENGTH

Address: Operational Base(0x21D01400) + offset (0x05B4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_bay3d_iir_rd_length Line length of bayer 3dnr iir read in pixel, also known as line stride.

MI_1400_BAY3D_IIR_RD_BASE_SHD

Address: Operational Base(0x21D01400) + offset (0x05B8)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	bay3d_iir_rd_base_shd Base shadow address of bayer 3dnr iir read data ring buffer.
3:0	RO	0x0	reserved

MI_1400_BAY3D_CUR_WR_BASE

Address: Operational Base(0x21D01400) + offset (0x05C0)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_bay3d_cur_wr_base Base address of bayer 3dnr current write data ring buffer.
3:0	RO	0x0	reserved

MI_1400_BAY3D_CUR_WR_SIZE

Address: Operational Base(0x21D01400) + offset (0x05C4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28:4	RW	0x0000000	sw_bay3d_cur_wr_size Size of bayer 3dnr current write data ring buffer.
3:0	RO	0x0	reserved

MI_1400_BAY3D_CUR_WR_LENGTH

Address: Operational Base(0x21D01400) + offset (0x05C8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RW	0x000	sw_bay3d_cur_wr_length Line length of bayer 3dnr current write in pixel, also known as line stride. If no line stride is used, line length must match image width.
3:0	RO	0x0	reserved

MI_1400_BAY3D_CUR_WR_BASE_SHD

Address: Operational Base(0x21D01400) + offset (0x05CC)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	bay3d_cur_wr_base_shd Base address of bayer 3dnr current write data ring buffer. --- BAY3D_CUR_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to BAY3D_CUR_WR_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_BAY3D_CUR_RD_BASE

Address: Operational Base(0x21D01400) + offset (0x05D0)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_bay3d_cur_rd_base Base address of bayer 3dnr current read data ring buffer.
3:0	RO	0x0	reserved

MI_1400_BAY3D_CUR_RD_LENGTH

Address: Operational Base(0x21D01400) + offset (0x05D4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_bay3d_cur_rd_length Line length of bayer 3dnr current read in pixel, also known as line stride.

MI_1400_BAY3D_CUR_RD_BASE_SHD

Address: Operational Base(0x21D01400) + offset (0x05D8)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	bay3d_cur_rd_base_shd Base shadow address of bayer 3dnr current read data ring buffer.
3:0	RO	0x0	reserved

MI_1400_BAY3D_CUR_RD_SIZE

Address: Operational Base(0x21D01400) + offset (0x05DC)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_bay3d_cur_rd_frmsize Frame size of bayer 3dnr read, only used in wrap mode.

MI_1400_BAY3D_DS_WR_BASE

Address: Operational Base(0x21D01400) + offset (0x05E0)

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Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_bay3d_ds_wr_base Base address of bayer 3dnr down scale write data ring buffer.
3:0	RO	0x0	reserved

MI_1400_BAY3D_DS_WR_SIZE

Address: Operational Base(0x21D01400) + offset (0x05E4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_bay3d_ds_wr_size Size of bayer 3dnr down scale write data ring buffer.
3:0	RO	0x0	reserved

MI_1400_BAY3D_DS_WR_LENGTH

Address: Operational Base(0x21D01400) + offset (0x05E8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:4	RW	0x000	sw_bay3d_ds_wr_length Line length of bayer 3dnr down scale write in pixel, also known as line stride. If no line stride is used, line length must match image width.
3:0	RO	0x0	reserved

MI_1400_BAY3D_DS_WR_BASE_SHD

Address: Operational Base(0x21D01400) + offset (0x05EC)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	bay3d_ds_wr_base_shd Base address of bayer 3dnr iir write data ring buffer. --- BAY3D_IIR_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to BAY3D_IIR_WR_BASE register description for details.
3:0	RO	0x0	reserved

MI_1400_BAY3D_DS_RD_BASE

Address: Operational Base(0x21D01400) + offset (0x05F0)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_bay3d_ds_rd_base Base address of bayer 3dnr down scale read data ring buffer.
3:0	RO	0x0	reserved

MI_1400_BAY3D_DS_RD_LENGTH

Address: Operational Base(0x21D01400) + offset (0x05F4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_bay3d_ds_rd_length Line length of bayer 3dnr down scale read in pixel, also known as line stride.

MI_1400_BAY3D_DS_RD_BASE_SHD

Address: Operational Base(0x21D01400) + offset (0x05F8)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	bay3d_ds_rd_base_shd Base shadow address of bayer 3dnr down scale read data ring buffer.
3:0	RO	0x0	reserved

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MI_1400_B3DMCH_RD_BASE

Address: Operational Base(0x21D01400) + offset (0x0600)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_b3dmch_rd_base Base address of b3dmch lut

MI_1400_B3DMCH_RD_LENGTH

Address: Operational Base(0x21D01400) + offset (0x0604)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_b3dmch_rd_length Line length of b3dmch lut

MI_1400_B3DMCH_RD_HWSIZE

Address: Operational Base(0x21D01400) + offset (0x0608)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	sw_b3dmch_wsize Horizontal size of b3dmch lut

MI_1400_B3DMCH_RD_VSIZE

Address: Operational Base(0x21D01400) + offset (0x060C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_b3dmch_vsize Vertical size of b3dmch lut

MI_1400_IRLDCV_RD_BASE

Address: Operational Base(0x21D01400) + offset (0x0610)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_irldcv_rd_base Base address of irldc vertical read data ring buffer.
3:0	RO	0x0	reserved

MI_1400_IRLDCV_RD_LENGTH

Address: Operational Base(0x21D01400) + offset (0x0614)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_irldcv_rd_length Line length of irldc vertical read in pixel, also known as line stride.

MI_1400_IRLDCV_RD_H_WSIZE

Address: Operational Base(0x21D01400) + offset (0x0618)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	sw_irldcv_rd_wsize Irldc vertical size of horizontal direction, word unit

MI_1400_IRLDCV_RD_V_SIZE

Address: Operational Base(0x21D01400) + offset (0x061C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
13:0	RW	0x0000	sw_irldcv_rd_vsize Irldc vertical size of vertical direction

MI_1400_IRLDCV_RD_BASE_SHD

Address: Operational Base(0x21D01400) + offset (0x0624)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	irldcv_rd_base_shd Base shadow address of irldc vertical read data ring buffer.
3:0	RO	0x0	reserved

MI_1400_B3DMCV_RD_BASE

Address: Operational Base(0x21D01400) + offset (0x0630)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_b3dmcv_rd_base Base address of b3dmcv lut

MI_1400_B3DMCV_RD_LENGTH

Address: Operational Base(0x21D01400) + offset (0x0634)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	sw_b3dmcv_rd_length Line length of b3dmcv lut

MI_1400_B3DMCV_RD_HWSIZE

Address: Operational Base(0x21D01400) + offset (0x0638)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	sw_b3dmcv_wsize Horizontal size of b3dmcv lut

MI_1400_B3DMCV_RD_VSIZE

Address: Operational Base(0x21D01400) + offset (0x063C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_b3dmcv_vsize Vertical size of b3dmcv lut

MI_1400_AXI_CONF_RD_CTRL

Address: Operational Base(0x21D01400) + offset (0x0640)

Bit	Attr	Reset Value	Description
31	RO	0x1	axi_conf_rd_status AXI configure read status. 1'b1: axi configure done. 1'b0: auto-start axi configure at mi all_frame_end
30	RO	0x0	ro_axi_conf_might_fail AXI configure might fail. 1'b1: isp_in_vsync is valid in the period of axi configure, maybe configure fail.
29	RO	0x0	ro_frm_buf_rw_conflict This status just detect whether write and read of frame buffer occur at the same time. It may not cause errors.
28	RO	0x0	ro_wr_frm_buf_error Error occurs when bay3d_ds and frame buffer write DDR at the same time.

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Bit	Attr	Reset Value	Description
27:17	RO	0x000	reserved
16	RW	0x0	sys_frm_buf_self_force_upd Write and read frame buffer data enable shadow force update. Note: - Readback is shadow register.
15:12	RO	0x0	reserved
11	RO	0x0	sw_rd_frm_buf_en_shd Read frame buffer data enable shadow. Shadow is updated by mi_all_frame_end.
10	RO	0x0	sw_wr_frm_buf_en_shd Write frame buffer data enable shadow. Shadow is updated by mi_all_frame_end.
9	RW	0x0	sw_rd_frm_buf_en Read frame buffer data enable.
8	RW	0x0	sw_wr_frm_buf_en Write frame buffer data enable. Bay3d_ds write path is reused by write frame buffer.
7:5	RO	0x0	reserved
4	W1C	0x0	sys_axi_conf_rd_clear AXI configure read clear to pull down axi_conf_rd_status for next frame auto axi configure.
3	RO	0x0	reserved
2	RW	0x0	sw_axi_conf_rd_end_sel Frame end selection for next axi configure read start. 1'b0: ISP core out frame end 1'b1: MI all frame end
1	RW	0x0	sw_axi_conf_rd_st_mode AXI configure read start mode. 1'b0: aoto-start axi configure at mi all_frame_end when axi_conf_rd_status is 0. 1'b1: start axi configure at sys_axi_conf_rd_st is 1.
0	W1C	0x0	sys_axi_conf_rd_st AXI configure read start.

MI_1400_AXI_CONF_RD_BASE

Address: Operational Base(0x21D01400) + offset (0x0644)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_axi_conf_rd_base Base address of axi configure read data ring buffer.
3:0	RO	0x0	reserved

MI_1400_AXI_CONF_RD_H_WSIZE

Address: Operational Base(0x21D01400) + offset (0x0648)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	sw_axi_conf_wsize AXI configure size of horizontal direction, word unit

MI_1400_AXI_CONF_RD_V_SIZE

Address: Operational Base(0x21D01400) + offset (0x064C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_axi_conf_vsize AXI configure size of vertical direction

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MI_1400_FRM_BUF_WR_BASE

Address: Operational Base(0x21D01400) + offset (0x0650)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_frm_buf_wr_base Base address of frame buffer write data ring buffer.
3:0	RO	0x0	reserved

MI_1400_FRM_BUF_WR_SIZE

Address: Operational Base(0x21D01400) + offset (0x0654)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:4	RW	0x0000000	sw_frm_buf_wr_size Size of frame buffer write data ring buffer.
3:0	RO	0x0	reserved

MI_1400_FRM_BUF_RD_BASE

Address: Operational Base(0x21D01400) + offset (0x0658)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_frm_buf_rd_base Base address of frame buffer read data ring buffer.
3:0	RO	0x0	reserved

MI_1400_AXI_RW_DBG

Address: Operational Base(0x21D01400) + offset (0x0660)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	ro_axi_rw_dbg Debug message of axi read and write.
3:0	RO	0x0	reserved

44.4.2.4 ISP_TOP

ISP_0400_CTRL0

Address: Operational Base(0x21D00400) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	sw_cgc_ratio_en Cgc ratio mode 1'b1: Ration use 219/224 1'b0: Ration use
28	RW	0x0	sw_cgc_yuv_limit Yuv cgc enable 1'b1: Limit range 1'b0: Full range(bypass)
27:17	RO	0x000	reserved
16	RW	0x0	sw_en_12bit_unpack Isp_dma: Raw16to12->isp(unpack csi-raw12, 8-8-4/4)
15	RW	0x0	sw_en_12bit_packed Isp_dma: Raw16to12->isp(pack csi-raw12, 8-8-4/4)

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Bit	Attr	Reset Value	Description
14	RW	0x1	sw_csm_c_range Color Space Matrix chrominance clipping range for ISP output 1'b0: CbCr range 64..960 (16..240) according to ITU-R BT.601 standard 1'b1: Full UV range 0..1023 (0..255) Numbers in brackets are for 8 bit resolution. This bit also configures the YCbCr sequence align block accordingly
13	RW	0x1	sw_csm_y_range Color Space Matrix luminance clipping range for ISP output 1'b0: Y range 64..940 (16..235) according to ITU-R BT.601 standard 1'b1: Full Y range 0..1023 (0..255) Numbers in brackets are for 8 bit resolution. This bit also configures the YCbCr sequence align block accordingly
12	RW	0x0	sw_flash_mode 1'b0: Sensor interface works independently from flash control unit 1'b1: One frame is captured when signaled by flash control unit
11	RO	0x0	reserved
10	WO	0x0	sys_cfg_gen_upd 1'b1: Generate frame synchronous configuration signal at the output of ISP for shadow registers of the following processing modules, write only
9	WO	0x0	sys_cfg_force_upd 1'b1: Immediately configure (update) shadow registers, write only
8	RW	0x0	sys_cfg_gen_upd_fix 1'b1: Permanent configure (update) shadow registers on frame end
7	RW	0x0	isp_awb_enable Auto white balance ON/OFF
6	RW	0x0	sw_gamma_in_enable Sensor De-gamma ON/OFF
5	RW	0x0	sw_mir_enable 1'b1: ISP out yuv mirror enabled 1'b0: ISP out yuv mirror disabled There is a line delay from input to output. Note: Readback is shadow register.
4	RW	0x0	sw_inform_enable 1'b1: Input formatter enabled 1'b0: Input formatter disabled The ISP input formatter is enabled or disabled by this bit immediately, but always starts or stops acquisition frame synchronously

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Bit	Attr	Reset Value	Description
3:1	RW	0x0	sw_isp_mode 3'b000: RAW picture with BT.601 sync (ISP bypass) 3'b001: ITU-R BT.656 (YUV with embedded sync) 3'b010: ITU-R BT.601 (YUV input with H and Vsync signals) 3'b011: Bayer RGB processing with H and Vsync signals 3'b100: Data mode (ISP bypass, sync signals interpreted as data enable) 3'b101: Bayer RGB processing with BT.656 synchronization 3'b110: RAW picture with ITU-R BT.656 synchronization (ISP bypass) 3'b111: Reserved Side effect: If RAW, BT.601, BT.656, or data mode is selected, the clock of the ISP SRAMs (ISP line buffer, Lens Shading, Bad Pixel) is switched off. Only in Bayer RGB mode the clock to the SRAMs is enabled. This further reduces power consumption
0	RW	0x0	sw_isp_enable 1'b1: ISP data output enabled 1'b0: ISP data output disabled Controls output formatter frame synchronously, if isp_gen_cfg_upd is used to activate this bit. For immediate update isp_cfg_upd must be used. --- ISP_CTRL --- Note: Partly write-only

ISP_0400_CTRL1

Address: Operational Base(0x21D00400) + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	sw_noc_idle_dis ISP to NOC idle disable
29:28	RO	0x0	reserved
27	W1C	0x1	sys_raw3d_fst_frame 3drawnr 1st_frame pulse signal
26	W1C	0x1	sys_cnr_fst_frame Cnr 1st_frame pulse signal
25	W1C	0x1	sys_yhist_fst_frame Yhist 1st_frame pulse signal
24	W1C	0x1	sys_enh_fst_frame Enhance 1st_frame pulse signal
23	W1C	0x1	sys_ynr_fst_frame Ynr 1st_frame pulse signal
22	RW	0x0	sys_gic_fst_frame Gic 1st_frame pulse signal
21	RW	0x0	sw_dualedge_en Old dvp for ccir656, not use now It has been deleted in isp-lite version.
20	RW	0x0	sw_bt1120_en 1'b0: Disable bt1120 mode 1'b1: Enable bt1120 mode Old dvp for ccir656, not use now It has been deleted in isp-lite version.
19	W1C	0x0	sys_shp_fst_frame Sharp 1st_frame pulse signal
18:17	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
16	RW	0x0	sw_yuv_dma_sel 1'b0: Use align or conversion data for isp_is input 1'b1: Use dma yuv read data for isp_is input
15	RW	0x0	sw_rgb_dma_sel 1'b0: Use input formatter data for latency fifo 1'b1: Use dma rgb read data for latency fifo
14:12	RW	0x0	sw_input_selection 3'b000: 12Bit external Interface 3'b001: 10Bit Interface, append 2 zeroes as LSBs 3'b010: 10Bit Interface, append 2 MSBs as LSBs 3'b011: 8Bit Interface, append 4 zeroes as LSBs 3'b100: 8Bit Interface, append 4 MSBs as LSBs Others: Reserved It has been deleted in isp-lite version.
11	RW	0x0	sw_field_inv 1'b1: Swap odd and even fields 1'b0: Do not swap fields Old dvp for ccir656, not use now It has been deleted in isp-lite version.
10:9	RW	0x0	sw_field_selection 2'b00: Sample all fields (do not care about fields) 2'b01: Sample only even fields 2'b10: Sample only odd fields 2'b11: Reserved Old dvp for ccir656, not use now It has been deleted in isp-lite version.
8:7	RW	0x0	sw_ccir_seq 2'b00: YCbYCr 2'b01: YCrYCb 2'b10: CbYCrY 2'b11: CrYCbY Old dvp for ccir656, not use now
6:5	RW	0x3	sw_conv_422 2'b00 - Co-sited color sub-sampling Y0Cb0Cr0 C Y1 2'b01 - Interleaved color sub-sampling Y0Cb0 C Y1Cr1 (not recommended) 2'b10 - Non-cosited color sub-sampling Y0Cb(0+1)/2 C Y1Cr(0+1)/2 2'b11 - UV 1/2 sample (drop mode)
4:3	RW	0x0	sw_bayer_pat Color components from sensor, starting with top left position in sampled frame (reprogram with ISP_ACQ_H_OFFS, ISP_ACQ_V_OFFS) 2'b00 - First line: RGRG..., second line: GBGB..., etc. 2'b01 - First line: GRGR..., second line: BGBG..., etc. 2'b10 - First line: GBGB..., second line: RGRG..., etc. 2'b11 - First line: BGBG..., second line: GRGR..., etc. This configuration applies for the black level area after cropping by the input formatter

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Bit	Attr	Reset Value	Description
2:1	RW	0x0	sw_bayer_pat_fe Color components from sensor, starting with top left position in sampled frame (reprogram with ISP_ACQ_H_OFFS, ISP_ACQ_V_OFFS) 2'b00 - First line: RGRG..., second line: GBGB..., etc. 2'b01 - First line: GRGR..., second line: BGBG..., etc. 2'b10 - First line: GBGB..., second line: RGRG..., etc. 2'b11 - First line: BGBG..., second line: GRGR..., etc. This configuration applies for the black level area after cropping by the input formatter Note: this configration is used for aiisp front end module(when aiisp is enable)
0	RW	0x0	sw_bayer_upd_fe_en 1'b1: AIISP front end module use bayer_pat_f and force_upd_f enabled 1'b0: AIISP front end module use bayer_pat_f and force_upd_f disabled

ISP_0400_ACQ_H_OFFS

Address: Operational Base(0x21D00400) + offset (0x0008)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RW	0x0	sw_sensor_index Multi-sensor index used 3'b000: Sensor0 index 3'b001: Sensor1 index 3'b010: Sensor2 index 3'b011: Sensor3 index 3'b100: Sensor4 index Then same as sensor_id in old version
27:24	RW	0x0	sw_sensor_force_index Frame buffer is divided to 16 equal parts. If sw_sensor_mode is not meeting demand, you can use this reg to generate the desire shape of frame buffer. For example, when sensor_id=0, configure the register value to 0; when sensor_id=1, configure the register value to 8. Then this configure is equal to configure sw_sensor_mode to 1(two sensor of same size).
23	RO	0x0	reserved
22:20	RW	0x0	sw_sensor_mode Multi-sensor mode (outside sensor numbers): 3'b00: One sensor 3'b01: Two sensor of same size 3'b10: Four sensor of same size 3'b100:Three sensor of one big and two small(8M+4M+4M) 3'b101:Two sensor of one big and one small(13M+2M) Others: Reserved eg:8M=3840x2160;4M=2688x1536;13M=4224x3136
19:15	RO	0x00	reserved
14:0	RW	0x0000	sw_acq_h_offs Horizontal sample offset in 8-bit samples (yuv: 4 samples=2pix)

ISP_0400_ACQ_V_OFFS

Address: Operational Base(0x21D00400) + offset (0x000C)

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Bit	Attr	Reset Value	Description
31:28	RW	0x0	sw_fifo2drc_size Fifo size for b3d2drcpath delayline
27:14	RO	0x0000	reserved
13:0	RW	0x0000	sw_acq_v_offs Vertical sample offset in lines

ISP_0400_ACQ_H_SIZE

Address: Operational Base(0x21D00400) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	sw_acq_h_size_bay3dmi sw_acq_h_size_bay3dmi for bay3d size configure, when not configure, hardware will auto-calculate
15	RO	0x0	reserved
14:0	RW	0x1000	sw_acq_h_size Horizontal sample size in 12-bit samples YUV input: 2 samples = 1 pixel, else 1 sample = 1 pixel. So in YUV mode ACQ_H_SIZE must be twice as large as horizontal image size Horizontal image size must always be even except in raw picture mode. If an odd size is programmed the value will be truncated to even size

ISP_0400_ACQ_V_SIZE

Address: Operational Base(0x21D00400) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0c00	sw_acq_v_size Vertical sample size in lines

ISP_0400_ACQ_NR_FRAMES

Address: Operational Base(0x21D00400) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	sw_acq_nr_frames Number of input frames to be sampled (0 = continuous)

ISP_0400_AWB1_GAIN_G

Address: Operational Base(0x21D00400) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x100	sw_awb1_gain_gr Gain value for green component in red line 100h = 1, unsigned integer value, range 0 to 15 with 8 bit fractional part.
15:12	RO	0x0	reserved
11:0	RW	0x100	sw_awb1_gain_gb Gain value for green component in blue line 100h = 1, unsigned integer value, range 0 to 15 with 8 bit fractional part.

ISP_0400_AWB1_GAIN_RB

Address: Operational Base(0x21D00400) + offset (0x0134)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x100	sw_awb1_gain_r Gain value for red component 100h = 1, unsigned integer value, range 0 to 15 with 8 bit fractional part.

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Bit	Attr	Reset Value	Description
15:12	RO	0x0	reserved
11:0	RW	0x100	sw_awb1_gain_b Gain value for blue component 100h = 1, unsigned integer value, range 0 to 15 with 8 bit fractional part.

ISP_0400_AWB0_GAIN0_G

Address: Operational Base(0x21D00400) + offset (0x0138)

Bit	Attr	Reset Value	Description
31:16	RW	0x0100	sw_awb_gain0_gr Gain value for green component in red line 100h = 1, unsigned integer value, range 0 to 255 with 8 bit fractional part.
15:0	RW	0x0100	sw_awb_gain0_gb Gain value for green component in blue line 100h = 1, unsigned integer value, range 0 to 255 with 8 bit fractional part.

ISP_0400_AWB0_GAIN0_RB

Address: Operational Base(0x21D00400) + offset (0x013C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0100	sw_awb_gain0_r Gain value for red component 100h = 1, unsigned integer value, range 0 to 255 with 8 bit fractional part.
15:0	RW	0x0100	sw_awb_gain0_b Gain value for blue component 100h = 1, unsigned integer value, range 0 to 255 with 8 bit fractional part.

ISP_0400_AWB0_GAIN1_G

Address: Operational Base(0x21D00400) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_awb_gain1_gr Gain value for green component in red line 100h = 1, unsigned integer value, range 0 to 255 with 8 bit fractional part.
15:0	RW	0x0000	sw_awb_gain1_gb Gain value for green component in blue line 100h = 1, unsigned integer value, range 0 to 255 with 8 bit fractional part.

ISP_0400_AWB0_GAIN1_RB

Address: Operational Base(0x21D00400) + offset (0x0144)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_awb_gain1_r Gain value for red component 100h = 1, unsigned integer value, range 0 to 255 with 8 bit fractional part.
15:0	RW	0x0000	sw_awb_gain1_b Gain value for blue component 100h = 1, unsigned integer value, range 0 to 255 with 8 bit fractional part.

ISP_0400_AWB0_GAIN2_G

Address: Operational Base(0x21D00400) + offset (0x0148)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_awb_gain2_gr Gain value for green component in red line 100h = 1, unsigned integer value, range 0 to 255 with 8 bit fractional part. (3562 no use)

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	sw_awb_gain2_gb Gain value for green component in blue line 100h = 1, unsigned integer value, range 0 to 255 with 8 bit fractional part. (3562 no use)

ISP_0400_AWB0_GAIN2_RB

Address: Operational Base(0x21D00400) + offset (0x014C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_awb_gain2_r Gain value for red component 100h = 1, unsigned integer value, range 0 to 255 with 8 bit fractional part. (3562 no use)
15:0	RW	0x0000	sw_awb_gain2_b Gain value for blue component 100h = 1, unsigned integer value, range 0 to 255 with 8 bit fractional part. (3562 no use)

ISP_0400_HURRY_CTRL

Address: Operational Base(0x21D00400) + offset (0x0158)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:12	RW	0x6	sw_noc_hurry_r_mode Lafifo wr-channel, 3bit: hurry_req assert high when left water level<(hurry_w1_mode/8) fifo empty, recommended value=0x6;
11:8	RW	0x5	sw_noc_hurry_w1_mode Ibuf0-S rw-channel, 3bit: hurry_req assert high when left water level<(hurry_w1_mode/16) fifo empty, recommended value=0x5;
7:4	RW	0x8	sw_noc_hurry_w0_mode Lafifo wr-channel, 3bit: hurry_req assert high when left water level<(hurry_w1_mode/8) fifo empty, recommended value=0x8
3	RO	0x0	reserved
2:0	RW	0x3	sw_noc_hurry_value 3'b000: The Low priority to interconnect ..... 3'b111: The first High priority to interconnect

ISP_0400_AWQOS_CTRL

Address: Operational Base(0x21D00400) + offset (0x015C)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:20	RW	0x1	sw_aw_allwr_qos1 Register1 of other channel (except bay3d) write qos to interconnect, configure 0 to 7, default 1
19	RO	0x0	reserved
18:16	RW	0x2	sw_aw_allwr_qos2 Register2 of other channel (except bay3d) write qos to interconnect, configure 0 to 7, default 2
15	RO	0x0	reserved
14:12	RW	0x3	sw_aw_allwr_qos3 Register3 of other channel (except bay3d) write qos to interconnect, configure 0 to 7, default 3
11	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
10:8	RW	0x1	sw_aw_bay3d_qos1 Register1 of bay3d write qos to interconnect, configure 0 to 7, default 1
7	RO	0x0	reserved
6:4	RW	0x2	sw_aw_bay3d_qos2 Register2 of bay3d write qos to interconnect, configure 0 to 7, default 2
3:1	RO	0x0	reserved
0	RW	0x1	sw_aw_qos_en All bus channel AXI write qos to interconnect, enable

ISP_0400_ARQOS_CTRL

Address: Operational Base(0x21D00400) + offset (0x0160)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:24	RW	0x1	sw_ar_rawx3_qos1 Register1 of rawx3 read qos to interconnect, configure 0 to 7, default 1
23	RO	0x0	reserved
22:20	RW	0x2	sw_ar_rawx3_qos2 Register2 of rawx3 read qos to interconnect, configure 0 to 7, default 2
19	RO	0x0	reserved
18:16	RW	0x1	sw_ar_bay3d_qos1 Register1 of bay3d read qos to interconnect, configure 0 to 7, default 1
15	RO	0x0	reserved
14:12	RW	0x2	sw_ar_bay3d_qos2 Register2 of bay3d read qos to interconnect, configure 0 to 7, default 2
11	RO	0x0	reserved
10:8	RW	0x1	sw_ar_others_qos1 Other channel (except bay3d and mmu) write qos to interconnect, configure 0 to 7, default 1
7	RO	0x0	reserved
6:4	RW	0x3	sw_ar_mmu_qos3 MMU write qos to interconnect, configure 0 to 7, default 3
3:1	RO	0x0	reserved
0	RW	0x1	sw_ar_qos_en All bus channel AXI read qos to interconnect, enable

ISP_0400_IRQ_CFG0

Address: Operational Base(0x21D00400) + offset (0x0164)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_isp_irq_line1 ISP out irq line1 configuration for half frame interrupt of image height. And ISP_IRQ is generated by interrupt bit[24].
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_isp_irq_line0 ISP out irq line0 configuration for quarter frame interrupt of image height. And ISP_IRQ is generated by interrupt bit[25]. Note: sw_isp_irq_line0 is reused by ISP slice done (isp out or ai-isp read).

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ISP_0400_IRQ_CFG1

Address: Operational Base(0x21D00400) + offset (0x0168)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_aiisp_wr_irq_line AI-ISP write irq line configuration for bay3d iir-wr interrupt of image height. And ISP_IRQ is generated by interrupt bit[18].
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_isp_irq_line2 ISP out irq line2 configuration for three quarters frame interrupt of image height. And ISP_IRQ is generated by interrupt bit[23].

ISP_0400_CC_COEFF_0

Address: Operational Base(0x21D00400) + offset (0x0170)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	sw_csm_y_offset If this signal is 0, will use old function(Y = f(coe_x) + 0 or 16). If this signal is not 0, Y = f(coe_x) + sw_csm_y_offset
23:16	RW	0x00	sw_csm_c_offset If this signal is 0, will use old function(Cb/r = f(coe_x) + 128). If this signal is not 0, Cb/r = f(coe_x) + sw_csm_c_offset
15:9	RO	0x00	reserved
8:0	RW	0x021	sw_csm_coeff0 Coefficient 0 for color space conversion --- ISP_CC_COEFF_0 --- Note: All color conversion coefficients are signed integer values with 7 bit fractional part, range -2 to 1.992

ISP_0400_CC_COEFF_1

Address: Operational Base(0x21D00400) + offset (0x0174)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x040	sw_csm_coeff1 Coefficient 1 for color space conversion

ISP_0400_CC_COEFF_2

Address: Operational Base(0x21D00400) + offset (0x0178)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x00d	sw_csm_coeff2 Coefficient 2 for color space conversion

ISP_0400_CC_COEFF_3

Address: Operational Base(0x21D00400) + offset (0x017C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x1ed	sw_csm_coeff3 Coefficient 3 for color space conversion

ISP_0400_CC_COEFF_4

Address: Operational Base(0x21D00400) + offset (0x0180)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x1db	sw_csm_coeff4 Coefficient 4 for color space conversion

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ISP_0400_CC_COEFF_5

Address: Operational Base(0x21D00400) + offset (0x0184)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x038	sw_csm_coeff5 Coefficient 5 for color space conversion

ISP_0400_CC_COEFF_6

Address: Operational Base(0x21D00400) + offset (0x0188)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x038	sw_csm_coeff6 Coefficient 6 for color space conversion

ISP_0400_CC_COEFF_7

Address: Operational Base(0x21D00400) + offset (0x018C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x1d1	sw_csm_coeff7 Coefficient 7 for color space conversion

ISP_0400_CC_COEFF_8

Address: Operational Base(0x21D00400) + offset (0x0190)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x1f7	sw_csm_coeff8 Coefficient 8 for color space conversion

ISP_0400_OUT_H_OFFS

Address: Operational Base(0x21D00400) + offset (0x0194)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_out_h_offs Vertical picture offset in lines

ISP_0400_OUT_V_OFFS

Address: Operational Base(0x21D00400) + offset (0x0198)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_out_v_offs Vertical picture offset in lines

ISP_0400_OUT_H_SIZE

Address: Operational Base(0x21D00400) + offset (0x019C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
30:16	RW	0x0000	sw_out1_h_size Horizontal picture size for front end module in pixel if ISP_MODE is set to 3'b001: ITU-R BT.656 YUV 3'b010: ITU-R BT.601 YUV 3'b011: ITU-R BT.601 Bayer RGB 3'b101: ITU-R BT.656 Bayer RGB Only even numbers are accepted, because complete quadruples of YUYV(YCbYCr) are needed for the 422 output. (If an odd size is programmed the value will be truncated to even size)
15	RO	0x0	reserved
14:0	RW	0x1000	sw_out_h_size Horizontal picture size in pixel if ISP_MODE is set to 3'b001: ITU-R BT.656 YUV 3'b010: ITU-R BT.601 YUV 3'b011: ITU-R BT.601 Bayer RGB 3'b101: ITU-R BT.656 Bayer RGB Only even numbers are accepted, because complete quadruples of YUYV(YCbYCr) are needed for the 422 output. (If an odd size is programmed the value will be truncated to even size)

ISP_0400_OUT_V_SIZE

Address: Operational Base(0x21D00400) + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	sw_out1_v_size Vertical picture size in lines for front end module
13:0	RW	0x0c00	sw_out_v_size Vertical picture size in lines

ISP_0400_FLAGS_SHD

Address: Operational Base(0x21D00400) + offset (0x01A8)

Bit	Attr	Reset Value	Description
31	RO	0x0	s_hsync State of ISP input port s_hsync, for test purposes
30	RO	0x0	s_vsync State of ISP input port s_vsync, for test purposes
29:28	RO	0x0	reserved
27:16	RO	0x000	s_data State of ISP input port s_data, for test purposes
15:3	RO	0x0000	reserved
2	RO	0x0	inform_field Current field information (0=odd, 1=even)
1	RO	0x0	isp_inform_enable_shd Input formatter enable shadow register
0	RO	0x0	isp_enable_shd ISP enable shadow register shows, if ISP currently outputs data (1) or not (0)

ISP_0400_OUT_H_OFFS_SHD

Address: Operational Base(0x21D00400) + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	isp_out_h_offs_shd Current vertical picture offset in lines

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ISP_0400_OUT_V_OFFS_SHD

Address: Operational Base(0x21D00400) + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	isp_out_v_offs_shd Current vertical picture offset in lines

ISP_0400_OUT_H_SIZE_SHD

Address: Operational Base(0x21D00400) + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RO	0x0000	isp_out_h_size_shd Current horizontal picture size in pixel

ISP_0400_OUT_V_SIZE_SHD

Address: Operational Base(0x21D00400) + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	isp_out_v_size_shd Vertical picture size in lines

ISP_0400_ISP_IMSC

Address: Operational Base(0x21D00400) + offset (0x01BC)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	sw_imsc_fetch_lut_end 1'b1: Enable interrupt 1'b0: Mask out
29	RW	0x0	sw_imsc_baynr_frame_end 1'b1: Enable interrupt 1'b0: Mask out
28	RW	0x0	sw_imsc_bay3d_post_st 1'b1: Enable interrupt 1'b0: Mask out
27	RW	0x0	sw_imsc_bay3d_in_linecnt_done 1'b1: Enable interrupt 1'b0: Mask out
26	RW	0x0	sw_imsc_bay3d_in_done 1'b1: Enable interrupt 1'b0: Mask out
25	RW	0x0	sw_imsc_out_quarter 1'b1: Enable interrupt 1'b0: Mask out
24	RW	0x0	sw_imsc_out_half 1'b1: Enable interrupt 1'b0: Mask out
23	RW	0x0	sw_imsc_out_frm_end 1'b1: Enable interrupt 1'b0: Mask out
22	RW	0x0	sw_imsc_gain_err 1'b1: Enable interrupt 1'b0: Mask out
21	RW	0x0	sw_imsc_dhaz_done 1'b1: Enable interrupt 1'b0: Mask out

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Bit	Attr	Reset Value	Description
20	RW	0x0	sw_imsc_hdr_done 1'b1: Enable interrupt 1'b0: Mask out
19	RO	0x0	reserved
18	RW	0x0	sw_imsc_exp_end 1'b1: Enable interrupt 1'b0: Mask out
17	RW	0x0	sw_imsc_flash_cap 1'b1: Enable interrupt 1'b0: Mask out
16	RW	0x0	sw_imsc_lsc_lut_err 1'b1: Enable interrupt 1'b0: Mask out
15	RW	0x0	sw_imsc_ldcv_irq 1'b1: Enable interrupt 1'b0: Mask out
14:12	RO	0x0	reserved
11	RW	0x0	sw_imsc_shutter_off 1'b1: Enable interrupt 1'b0: Mask out
10	RW	0x0	sw_imsc_shutter_on 1'b1: Enable interrupt 1'b0: Mask out
9	RW	0x0	sw_imsc_flash_off 1'b1: Enable interrupt 1'b0: Mask out
8	RW	0x0	sw_imsc_flash_on 1'b1: Enable interrupt 1'b0: Mask out
7	RW	0x0	sw_imsc_h_start 1'b1: Enable interrupt 1'b0: Mask out
6	RW	0x0	sw_imsc_v_start 1'b1: Enable interrupt 1'b0: Mask out
5	RW	0x0	sw_imsc_frame_in 1'b1: Enable interrupt 1'b0: Mask out
4	RW	0x0	sw_imsc_awb_done 1'b1: Enable interrupt 1'b0: Mask out
3	RW	0x0	sw_imsc_pic_size_err 1'b1: Enable interrupt 1'b0: Mask out
2	RW	0x0	sw_imsc_data_loss 1'b1: Enable interrupt 1'b0: Mask out
1	RW	0x0	sw_imsc_frame 1'b1: Enable interrupt 1'b0: Mask out
0	RW	0x0	sw_imsc_isp_off 1'b1: Enable interrupt 1'b0: Mask out

ISP_0400_ISP_RIS

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Address: Operational Base(0x21D00400) + offset (0x01C0)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	ris_fetch_lut_end LUT readback DDR complete, high valid
29	RO	0x0	ris_baynr_frame_end BAYBR module complete, high valid
28	RO	0x0	ris_bay3d_post_st BAY3D module next frame start signal generate before current frame_end, high valid
27	RO	0x0	ris_bay3d_in_linecnt_done BAY3D module current line counter done, high valid
26	RO	0x0	ris_bay3d_in_done BAY3D module current write buffer empty, high valid
25	RO	0x0	ris_out_quarter ISP output frame transmit quarter, high valid
24	RO	0x0	ris_out_half ISP output frame transmit half, high valid
23	RO	0x0	ris_out_frm_end ISP output frame complete, high valid
22	RO	0x0	ris_gain_err GAIN module error flag, high valid
21	RO	0x0	ris_dhaz_done DHAZ module complete, high valid
20	RO	0x0	ris_hdr_done HDR module complete, high valid
19	RO	0x0	reserved
18	RO	0x0	ris_exp_end Exposure measurement complete, high valid
17	RO	0x0	ris_flash_cap Signaling captured frame, high valid
16	RO	0x0	ris_lsc_lut_err LSC and RAWLSC LUT update error, high valid
15	RO	0x0	ris_ldcv_irq LDCV frame end or LDCV map error, high valid
14:12	RO	0x0	reserved
11	RO	0x0	ris_shutter_off Mechanical shutter is switched off, high valid
10	RO	0x0	ris_shutter_on Mechanical shutter is switched on, high valid
9	RO	0x0	ris_flash_off Flash light is switched off, high valid
8	RO	0x0	ris_flash_on Flash light is switched on, high valid
7	RO	0x0	ris_h_start Start edge of h_sync, high valid
6	RO	0x0	ris_v_start Start edge of v_sync, high valid
5	RO	0x0	ris_frame_in Sampled input frame is complete, high valid
4	RO	0x0	ris_awb_done White balancing measurement cycle is complete, results can be read out, high valid
3	RO	0x0	ris_pic_size_err Picture size violation occurred, programming seems wrong, high valid

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Bit	Attr	Reset Value	Description
2	RO	0x0	ris_data_loss Loss of data occurred within a line, processing failure, high valid
1	RO	0x0	ris_frame Frame was completely put out, high valid
0	RO	0x0	ris_isp_off Isp output was disabled (vsynced) due to f_cnt reached or manual, high valid

ISP_0400_ISP_MIS

Address: Operational Base(0x21D00400) + offset (0x01C4)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	mis_fetch_lut_end LUT readback DDR complete, high valid
29	RO	0x0	mis_baynr_frame_end BAYBR module complete, high valid
28	RO	0x0	mis_bay3d_post_st BAY3D module next frame start signal generate before current frame_end, high valid
27	RO	0x0	mis_bay3d_in_linecnt_done BAY3D module current line counter done, high valid
26	RO	0x0	mis_bay3d_in_done BAY3D module current write buffer empty, high valid
25	RO	0x0	mis_out_quarter ISP output frame transmit quarter, high valid
24	RO	0x0	mis_out_half ISP output frame transmit half, high valid
23	RO	0x0	mis_out_frm_end ISP output frame complete, high valid
22	RO	0x0	mis_gain_err GAIN module error flag, high valid
21	RO	0x0	mis_dhaz_done DHAZ module complete, high valid
20	RO	0x0	mis_hdr_done HDR module complete, high valid
19	RO	0x0	reserved
18	RO	0x0	mis_exp_end Exposure measurement complete, high valid
17	RO	0x0	mis_flash_cap Captured is frame is detected, high valid
16	RO	0x0	mis_lsc_lut_err LSC and RAWLSC LUT update error, high valid
15	RO	0x0	mis_ldcv_irq LDCV frame end or LDCV map error, high valid. When ldcv close, this signal is equal to LDCV in_frame_end.
14:12	RO	0x0	reserved
11	RO	0x0	mis_shutter_off Mechanical shutter is switched off, high valid
10	RO	0x0	mis_shutter_on Mechanical shutter is switched on, high valid
9	RO	0x0	mis_flash_off Flash light is switched off, high valid
8	RO	0x0	mis_flash_on Flash light is switched on, high valid

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Bit	Attr	Reset Value	Description
7	RO	0x0	mis_h_start Start edge of h_sync, high valid
6	RO	0x0	mis_v_start Start edge of v_sync, high valid
5	RO	0x0	mis_frame_in Sampled input frame is complete, high valid
4	RO	0x0	mis_awb_done White balancing measurement cycle is complete, results can be read out, high valid
3	RO	0x0	mis_pic_size_err Picture size violation occurred, programming seems wrong, high valid
2	RO	0x0	mis_data_loss Loss of data occurred within a line, processing failure, high valid
1	RO	0x0	mis_frame Frame was completely put out, high valid each MIS[31:0] signals high, set IRQ.
0	RO	0x0	mis_isp_off Isp was turned off (vsync) due to f_cnt reached or manual, high valid each MIS[31:0] signals high, set IRQ.

ISP_0400_ISP_ICR

Address: Operational Base(0x21D00400) + offset (0x01C8)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	WO	0x0	sys_icr_fetch_lut_end Clear interrupt
29	WO	0x0	sys_icr_baynr_frame_end Clear interrupt
28	WO	0x0	sys_icr_bay3d_post_st Clear interrupt
27	WO	0x0	sys_icr_bay3d_in_linecnt_done Clear interrupt
26	WO	0x0	sys_icr_bay3d_in_done Clear interrupt
25	WO	0x0	sys_icr_out_quarter Clear interrupt
24	WO	0x0	sys_icr_out_half Clear interrupt
23	WO	0x0	sys_icr_out_frm_end Clear interrupt
22	WO	0x0	sys_icr_gain_err Clear interrupt
21	WO	0x0	sys_icr_dhaz_done Clear interrupt
20	WO	0x0	sys_icr_hdr_done Clear interrupt
19	RO	0x0	reserved
18	WO	0x0	sys_icr_exp_end Clear interrupt
17	WO	0x0	sys_icr_flash_cap Clear interrupt
16	WO	0x0	sys_icr_lsc_lut_err Clear interrupt

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Bit	Attr	Reset Value	Description
15	WO	0x0	sys_icr_ldcv_irq Clear interrupt
14:12	RO	0x0	reserved
11	WO	0x0	sys_icr_shutter_off Clear interrupt
10	WO	0x0	sys_icr_shutter_on Clear interrupt
9	WO	0x0	sys_icr_flash_off Clear interrupt
8	WO	0x0	sys_icr_flash_on Clear interrupt
7	WO	0x0	sys_icr_h_start Clear interrupt
6	WO	0x0	sys_icr_v_start Clear interrupt
5	WO	0x0	sys_icr_frame_in Clear interrupt
4	WO	0x0	sys_icr_awb_done Clear interrupt
3	WO	0x0	sys_icr_pic_size_err Clear interrupt
2	WO	0x0	sys_icr_data_loss Clear interrupt
1	WO	0x0	sys_icr_frame Clear interrupt
0	WO	0x0	sys_icr_isp_off Clear interrupt

ISP_0400_ISP_ISR

Address: Operational Base(0x21D00400) + offset (0x01CC)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	WO	0x0	sys_isr_fetch_lut_end Set interrupt
29	WO	0x0	sys_isr_baynr_frame_end Set interrupt
28	WO	0x0	sys_isr_bay3d_post_st Set interrupt
27	WO	0x0	sys_isr_bay3d_in_linecnt_done Set interrupt
26	WO	0x0	sys_isr_bay3d_in_done Set interrupt
25	WO	0x0	sys_isr_out_quarter Set interrupt
24	WO	0x0	sys_isr_out_half Set interrupt
23	WO	0x0	sys_isr_out_frm_end Set interrupt
22	WO	0x0	sys_isr_gain_err Set interrupt
21	WO	0x0	sys_isr_dhaz_done Set interrupt
20	WO	0x0	sys_isr_hdr_done Set interrupt
19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18	WO	0x0	sys_isr_exp_end Set interrupt
17	WO	0x0	sys_isr_flash_cap Set interrupt
16	WO	0x0	sys_isr_lsc_lut_err Set interrupt
15	WO	0x0	sys_isr_ldcv_irq Set interrupt
14:12	RO	0x0	reserved
11	WO	0x0	sys_isr_shutter_off Set interrupt
10	WO	0x0	sys_isr_shutter_on Set interrupt
9	WO	0x0	sys_isr_flash_off Set interrupt
8	WO	0x0	sys_isr_flash_on Set interrupt
7	WO	0x0	sys_isr_h_start Set interrupt
6	WO	0x0	sys_isr_v_start Set interrupt
5	WO	0x0	sys_isr_frame_in Set interrupt
4	WO	0x0	sys_isr_awb_done Set interrupt
3	WO	0x0	sys_isr_pic_size_err Set interrupt
2	WO	0x0	sys_isr_data_loss Set interrupt
1	WO	0x0	sys_isr_frame Set interrupt
0	WO	0x0	sys_isr_isp_off Set interrupt

ISP_0400_ISP3A_IMSC

Address: Operational Base(0x21D00400) + offset (0x01D0)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	sw_imsc_aiawb_done 1'b1: Enable interrupt 1'b0: Mask out
13	RW	0x0	sw_imsc_w3a_err 1'b1: Enable interrupt 1'b0: Mask out
12	RW	0x0	sw_imsc_sws_3a_ddr_done 1'b1: Enable interrupt 1'b0: Mask out
11	RW	0x0	sw_imsc_rawawb_done 1'b1: Enable interrupt 1'b0: Mask out
10	RW	0x0	sw_imsc_rawaf_done 1'b1: Enable interrupt 1'b0: Mask out

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Bit	Attr	Reset Value	Description
9	RW	0x0	sw_imsc_awbsync_done 1'b1: Enable interrupt 1'b0: Mask out
8	RW	0x0	sw_imsc_rawaf_all_of 1'b1: Enable interrupt 1'b0: Mask out
7	RW	0x0	sw_imsc_rawhist_ch2_done 1'b1: Enable interrupt 1'b0: Mask out
6	RW	0x0	sw_imsc_rawhist_ch1_done 1'b1: Enable interrupt 1'b0: Mask out
5	RW	0x0	sw_imsc_rawhist_ch0_done 1'b1: Enable interrupt 1'b0: Mask out
4	RW	0x0	sw_imsc_rawhist_big_done 1'b1: Enable interrupt 1'b0: Mask out
3	RW	0x0	sw_imsc_rawae_ch2_done 1'b1: Enable interrupt 1'b0: Mask out
2	RW	0x0	sw_imsc_rawae_ch1_done 1'b1: Enable interrupt 1'b0: Mask out
1	RW	0x0	sw_imsc_rawae_ch0_done 1'b1: Enable interrupt 1'b0: Mask out
0	RW	0x0	sw_imsc_rawae_big_done 1'b1: Enable interrupt 1'b0: Mask out

ISP_0400_ISP3A_RIS

Address: Operational Base(0x21D00400) + offset (0x01D4)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RO	0x0	ris_aiawb_done AIAWB module complete
13	RO	0x0	ris_w3a_err W3A error
12	RO	0x0	ris_sws_3a_ddr_done 3a result write to DDR done flag
11	RO	0x0	ris_rawawb_done RAWAWB module complete
10	RO	0x0	ris_rawaf_done RAWAF module complete
9	RO	0x0	ris_awbsync_done AWBSYNC module complete
8	RO	0x0	ris_rawaf_all_of Auto focus all overflow
7	RO	0x0	ris_rawhist_ch2_done RAWHIST 2channel complete
6	RO	0x0	ris_rawhist_ch1_done RAWHIST 1channel complete
5	RO	0x0	ris_rawhist_ch0_done RAWHIST 0channel complete

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Bit	Attr	Reset Value	Description
4	RO	0x0	ris_rawhist_big_done RAWHIST BIG module complete
3	RO	0x0	ris_rawae_ch2_done RAWAE 2channel complete
2	RO	0x0	ris_rawae_ch1_done RAWAE 1channel complete
1	RO	0x0	ris_rawae_ch0_done RAWAE 0channel complete
0	RO	0x0	ris_rawae_big_done RAWAE BIG module complete

ISP_0400_ISP3A_MIS

Address: Operational Base(0x21D00400) + offset (0x01D8)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RO	0x0	mis_aiawb_done AIAWB module complete
13	RO	0x0	mis_w3a_err W3A error
12	RO	0x0	mis_sws_3a_ddr_done 3a result write to DDR done flag
11	RO	0x0	mis_rawawb_done RAWAWB module complete
10	RO	0x0	mis_rawaf_done RAWAF module complete
9	RO	0x0	mis_awbsync_done AWBSYNC module complete
8	RO	0x0	mis_rawaf_all_of Auto focus all overflow
7	RO	0x0	mis_rawhist_ch2_done RAWHIST 2channel complete
6	RO	0x0	mis_rawhist_ch1_done RAWHIST 1channel complete
5	RO	0x0	mis_rawhist_ch0_done RAWHIST 0channel complete
4	RO	0x0	mis_rawhist_big_done RAWHIST BIG module complete
3	RO	0x0	mis_rawae_ch2_done RAWAE 2channel complete
2	RO	0x0	mis_rawae_ch1_done RAWAE 1channel complete
1	RO	0x0	mis_rawae_ch0_done RAWAE 0channel complete
0	RO	0x0	mis_rawae_big_done RAWAE BIG module complete

ISP_0400_ISP3A_ICR

Address: Operational Base(0x21D00400) + offset (0x01DC)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	WO	0x0	sys_icr_aiawb_done Clear interrupt
13	WO	0x0	sys_w3a_err Clear interrupt

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Bit	Attr	Reset Value	Description
12	WO	0x0	sys_icr_sws_3a_ddr_done Clear interrupt
11	WO	0x0	sys_icr_rawawb_done Clear interrupt
10	WO	0x0	sys_icr_rawaf_done Clear interrupt
9	WO	0x0	sys_icr_awbsync_done Clear interrupt
8	WO	0x0	sys_icr_rawaf_all_of Clear interrupt
7	WO	0x0	sys_icr_rawhist_ch2_done Clear interrupt
6	WO	0x0	sys_icr_rawhist_ch1_done Clear interrupt
5	WO	0x0	sys_icr_rawhist_ch0_done Clear interrupt
4	WO	0x0	sys_icr_rawhist_big_done Clear interrupt
3	WO	0x0	sys_icr_rawae_ch2_done Clear interrupt
2	WO	0x0	sys_icr_rawae_ch1_done Clear interrupt
1	WO	0x0	sys_icr_rawae_ch0_done Clear interrupt
0	WO	0x0	sys_icr_rawae_big_done Clear interrupt

ISP_0400_ERR

Address: Operational Base(0x21D00400) + offset (0x023C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	RO	0x0	aiawb_datloss_err AIAWB may data loss when AIAWBIN.
6	RO	0x0	is_size_err Size error is generated in image stabilization sub-module
5	RO	0x0	drclsc_lut_err This error is generated by DRC LUT configure error
4	RO	0x0	rawlsc_lut_err This error is generated by RAWLSC LUT configure error
3	RO	0x0	lsc_lut_err This error is generated by LSC LUT configure error. (This bit will assert high when update this LUT select from DDR mode and can not finish update at vsync period)
2	RO	0x0	outform_size_err Size error is generated in out mux sub-module
1	RO	0x0	isp_out_size_err Size error for ispout
0	RO	0x0	inform_size_err size error is generated in inform sub-module --- ISP_ERR --- Note: For debug purposes the ISP_ERR and ISP_ERR_CLR are implemented. For the case when a PIC_SIZE_ERR interrupt is signaled the SW is able to see in which sub-module this error is generated. Writing to the ISP_ERR_CLR register clears this bit

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ISP_0400_ERR_CLR

Address: Operational Base(0x21D00400) + offset (0x0240)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7	WO	0x0	aiawb_datloss_err_clr This error is cleared
6	WO	0x0	is_size_err_clr Size error is cleared
5	WO	0x0	drclsc_lut_err_clr This error is cleared
4	WO	0x0	rawlsc_lut_err_clr This error is cleared
3	WO	0x0	lsc_lut_err_clr This error is cleared
2	WO	0x0	outform_size_err_clr Size error is cleared
1	WO	0x0	ispout_size_err_clr Size error is cleared
0	WO	0x0	inform_size_err_clr Size error is cleared

ISP_0400_FRAME_COUNT

Address: Operational Base(0x21D00400) + offset (0x0244)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:28	RO	0x0	ro_lut_state Fetch lut: 3'b000: Idle 3'b001: Lsc 3'b010: 3dlut 3'b011: Cac 3'b100: Ldch
27:10	RO	0x00000	reserved
9:0	RO	0x000	frame_counter Current frame count of processing --- ISP_FRAME_COUNT --- Note: In the ISP_FRAME_COUNT register the number of processed frames are displayed. For example: If a 8 is programmed into the ISP_ACQ_NR_FRAMES register, a read access to the ISP_FRAME_COUNT register during processing of the first picture shows a 7. After the entire frames are processed the ISP_OFF interrupt is generated and the ISP_FRAME_COUNT has the count zero. In case a "0" is programmed into the ISP_ACQ_NR_FRAMES register (continues mode) the ISP_FRAME_COUNT register keeps the value "0".

ISP_0400_DEBUG1

Address: Operational Base(0x21D00400) + offset (0x0248)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	ro_fifo_space2full Space2full status group: [ro_ibuf2_space2full, ro_ibuf1_space2full, ro_ibuf0_space2full, 4'b0, ro_outfifo_space2full, ro_lafifo_space2full]

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Bit	Attr	Reset Value	Description
7:0	RO	0x00	ro_isp2enc_frm_cnt ISP to encoder frame counter Frame counter from mp or isp out. MUX register 0x001c[0].

ISP_0400_DEBUG2

Address: Operational Base(0x21D00400) + offset (0x024C)

Bit	Attr	Reset Value	Description
31	RO	0x0	bay3d_fifo_iir_full Bay3d fifo iir full
30	RO	0x0	bay3d_fifo_cur_full Bay3d fifo current full
29:16	RO	0x0000	outform_vcnt Module outform vertical counter
15:13	RO	0x0	reserved
12:0	RO	0x0000	ro_isp2enc_line_cnt ISP to encoder line counter. Line counter from mp or isp out. MUX register 0x001c[0].

ISP_0400_DEBUG3

Address: Operational Base(0x21D00400) + offset (0x0250)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	isp_pipe_ack ISP pipeline group: [mge_val, mge_ack, rawnr_val, rawnr_ack, bay3d_val, bay3d_ack, tmo_val, tmo_ack, gic_val, gic_ack, dbr_val, dbr_ack, debayer_val, debayer_ack, ccm_val, ccm_ack, gamma_out_val, gamma_out_ack, dhaz_val, dhaz_ack, lut3d_val, lut3d_ack, ldch_val, ldch_ack, conv422_val, conv422_ack, ynr_val, ynr_ack, shp_val, shp_ack, cgc_val, cgc_ack, 2'b0, cac_val, cac_ack, isp_out_val, isp_out_ack, isp_in_val, isp_in_ack]

ISP_0400_DEBUG4

Address: Operational Base(0x21D00400) + offset (0x0254)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	isp_pipe_ack1 ISP pipeline group1: [24'b0, gic_in_val, gic_in_ack, dpcc_val, dpcc_ack, expd_val, expd_ack, ynr_in_val, ynr_in_ack]

ISP_0400_YNR_LUMA_RCTRL

Address: Operational Base(0x21D00400) + offset (0x0290)

Bit	Attr	Reset Value	Description
31	RO	0x0	ro_ynr_luma_rdback_rdy YNR luma ahb readback ready flag. Configure sys_ynr_luma_rdback_st, then wait ro_ynr_luma_rdback_rdy = 1.
30	RO	0x0	reserved
29:16	RW	0x0000	sys_ynr_luma_rdback_offs YNR luma ahb readback offset in ram.
15:1	RO	0x0000	reserved
0	W1C	0x0	sys_ynr_luma_rdback_st YNR luma ahb readback start. And sys_ynr_luma_rdback_st is used for internal counter and cross-asynchronous fifo clearing.

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ISP_0400_YNR_LUMA_RDATA

Address: Operational Base(0x21D00400) + offset (0x0294)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	cfg_ynr_luma_rdata YNR luma pixel value. Each pixel occupies 8 bits in cfg_ynr_luma_rdata.

ISP_0400_STITCH_CTRL0

Address: Operational Base(0x21D00400) + offset (0x0298)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_stitch_off0 Sensor1 strat offset It has been deleted in isp-lite version.
15:5	RO	0x000	reserved
4:3	RW	0x0	sw_stitch_sen_id Sensor index of current read register. 2'b00: Current read is sensor 0 2'b01: Current read is sensor 1 2'b10: Current read is sensor 2 2'b11: Current read is sensor 3 It has been deleted in isp-lite version.
2:1	RW	0x0	sw_stitch_mode Multi-sensor stitch mode. 2'b00: Two sensor 2'b01: Three sensor 2'b10: Four sensor 2'b11: Reserved It has been deleted in isp-lite version.
0	RW	0x0	sw_stitch_en Multi-sensor stitch enable. 1'b1: Enable 1'b0: Disable It has been deleted in isp-lite version.

ISP_0400_STITCH_CTRL1

Address: Operational Base(0x21D00400) + offset (0x029C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_stitch_off2 Sensor3 strat offset It has been deleted in isp-lite version.
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_stitch_off1 Sensor2 strat offset It has been deleted in isp-lite version.

ISP_0400_STITCH_CTRL2

Address: Operational Base(0x21D00400) + offset (0x02A0)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	sw_lsc_stitch_lut_off2 Lsc sensor3 start lut offset It has been deleted in isp-lite version.

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	sw_lsc_stitch_lut_off1 Lsc sensor2 start lut offset It has been deleted in isp-lite version.
3:0	RW	0x0	sw_lsc_stitch_lut_off0 Lsc sensor1 start lut offset It has been deleted in isp-lite version.

ISP_0400_SLICE_ST_CTRL

Address: Operational Base(0x21D00400) + offset (0x02A4)

Bit	Attr	Reset Value	Description
31	RO	0x0	isp_slice_done ISP slice done, stop working. It is pulled up when ro_isp_out_line_cnt is equal to sw_isp_irq_line0.
30	RO	0x0	reserved
29:16	RO	0x0000	ro_isp_out_line_cnt ISP out line counter, which will auto clear when frame end.
15:2	RO	0x0000	reserved
1	RW	0x0	sw_isp_slice_en ISP slice enable 1'b0: Disable 1'b1: Enable Note: AI-ISP must enable ISP slice function.
0	W1C	0x0	sys_isp_slice_st ISP slice start, which is used to continue ISP processing when isp_line_done is high.

ISP_0400_AIISP_LINE_CNT

Address: Operational Base(0x21D00400) + offset (0x02A8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	ro_aiisp_rd_line_cnt AI-ISP read line counter. Line counter from ai-isp data read.
15:14	RO	0x0	reserved
13:0	RO	0x0000	ro_aiisp_wr_line_cnt AI-ISP write line counter. Line counter from bay3d iir-wr.

44.4.2.5 CTRL

CTRL_0000_VI_ISP_EN

Address: Operational Base(0x21D00000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	vi_ccl_dis Isp_top enable for all marvin sub_module 1'b0: Isp is disable 1'b1: Isp is enable

CTRL_0000_VI_ISP_PATH

Address: Operational Base(0x21D00000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
30	RW	0x0	sw_bnr2ae0_sel_en RAWAE0 data from BAYNR(AE:BayNR[9:0]HIST:BayNR[11:4]) out select bit .
29	RW	0x0	sw_bnr2aebig_sel_en RAWAEBIG data from BAYNR(AE:BayNR[19:10] HIST:BayNR[19:12]) out select bit.
28	RW	0x0	sw_bnr2af_sel_en RAWAF data from BAYNR out select bit.
27	RW	0x0	sw_drc2awb_sel_en RAWAWB data from ADRC out select bit.
26	RW	0x0	sw_bnr2awb_sel_en RAWAWB data from BAYNR out select bit.
25:24	RW	0x0	sw_lsc_cfg_path_sel Here mainLSC, rawLSC, drcLSC share the same configuration address space. 2'b00: mainLSC, rawLSC, drcLSC will be all configured and selected mainLSC configuration readback data. 2'b01: Only mainLSC will be configured and selected mainLSC configuration readback data. 2'b10: Only rawLSC will be configured and selected rawLSC configuration readback data. 2'b11: Only drcLSC will be configured and selected drcLSC configuration readback data.
23:22	RW	0x0	sw_3a_rawae012_swap 3A-rawae(hist)0-1 swap: 2'b00: RAWAE0 for StrmCh0, RAWAE1 for StrmCh1, RAWAE2 for StrmCh2; 2'b01: RAWAE0 for StrmCh1, RAWAE1 for StrmCh0, RAWAE2 for StrmCh2; 2'b10: RAWAE0 for StrmCh2, RAWAE1 for StrmCh1, RAWAE2 for StrmCh0;
21:20	RW	0x0	sw_3a_rawawb_sel 2'b00: Gamma-in0 with awb 2'b01: Gamma-in1 with awb 2'b10: Gamma-in2 with awb
19:18	RW	0x0	sw_3a_rawaf_sel 2'b00: Awb0 out path 2'b01: Awb1 out path 2'b10: Awb2 out path 2'b11: Debayer in path
17:16	RW	0x0	sw_3a_rawae_sel 2'b00: Awb0 out path 2'b01: Awb1 out path 2'b10: Awb2 out path 2'b11: Debayer in path
15:0	RO	0x0000	reserved

CTRL_0000_VI_ID

Address: Operational Base(0x21D00000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:24	RO	0x03	ro_isp_version_major Major version
23:16	RO	0x01	ro_isp_version_minor Minor version

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Bit	Attr	Reset Value	Description
15:0	RO	0x2106	ro_isp_version_date Year, Month

CTRL_0000_VI_ISP_CLK_CTRL

Address: Operational Base(0x21D00000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31	RW	0x0	marvinmi_clk_alwayson Marvin_mi processing clock control 1'b1: Clock always on 1'b0: Clock auto-gate
30	RW	0x0	mipi_clk_alwayson Simipi & mipi0 & mipi1 processing clock control, not used now 1'b1: Clock always on 1'b0: Clock auto-gate
29	RW	0x0	rszs_clk_alwayson Rszs processing clock control 1'b1: Clock always on 1'b0: Clock auto-gate
28	RW	0x0	jpeg_clk_alwayson Jpeg processing clock control 1'b1: Clock always on 1'b0: Clock auto-gate
27	RW	0x0	dpmux_clk_alwayson Dpmux processing clock control 1'b1: Clock always on 1'b0: Clock auto-gate
26	RW	0x0	rszm_clk_alwayson Rszm processing clock control 1'b1: Clock always on 1'b0: Clock auto-gate
25	RW	0x0	si_clk_alwayson Si processing clock control 1'b1: Clock always on 1'b0: Clock auto-gate
24	RW	0x0	ie_clk_alwayson Iemux & ie processing clock control 1'b1: Clock always on 1'b0: Clock auto-gate
23	RW	0x0	cp_clk_alwayson Cp processing clock control 1'b1: Clock always on 1'b0: Clock auto-gate
22	RW	0x0	mi_raw_rd_clk_on Isp_mi raw read path clock always on 1'b1: Clock always on 1'b0: Clock auto-gate
21	RW	0x0	mi_read_clk_on Isp_mi dma read clock always on 1'b1: Clock always on 1'b0: Clock auto-gate
20	RW	0x0	mi_raw1_clk_on Isp_mi raw1 write path clock always on 1'b1: Clock always on 1'b0: Clock auto-gate

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Bit	Attr	Reset Value	Description
19	RW	0x0	mi_raw0_clk_on Isp_mi raw0 write path clock always on 1'b1: Clock always on 1'b0: Clock auto-gate
18	RW	0x0	mi_sp_clk_on Isp_mi self path clock always on 1'b1: Clock always on 1'b0: Clock auto-gate
17	RW	0x0	mi_y12_clk_on Isp_mi y12 path clock always on 1'b1: Clock always on 1'b0: Clock auto-gate
16	RW	0x0	mi_dp_clk_on Isp_mi dpcc path clock always on 1'b1: Clock always on 1'b0: Clock auto-gate
15	RW	0x0	mi_jpeg_clk_on Isp_mi jpeg path clock always on 1'b1: Clock always on 1'b0: Clock auto-gate
14	RW	0x0	mi_mp_clk_on Isp_mi main path clock always on 1'b1: Clock always on 1'b0: Clock auto-gate
13	RW	0x0	mi_ldc_clk_on Isp_mi ldc path clock always on 1'b1: Clock always on 1'b0: Clock auto-gate
12	RW	0x0	ldc_ram_clk_on Ldc_ram clock control, for ram 1'b1: Clock always on 1'b0: Clock auto-gate
11	RW	0x0	aclk_isp_clk_on Aclk_isp clock control, for ram 1'b1: Clock always on 1'b0: Clock auto-gate
10	RW	0x0	jpeg_ram_clk_on Jpeg ram clock control, not used now 1'b1: Clock always on 1'b0: Clock auto-gate
9	RW	0x0	rsz_ram_clk_on Rsz ram clock control 1'b1: Clock always on 1'b0: Clock auto-gate
8	RW	0x0	isp_ie_ram_clk_on Isp_ie_ram clock control 1'b1: Clock always on 1'b0: Clock auto-gate
7	RW	0x0	isp_dpcc_ram_clk_on Isp_dpcc_ram clock control 1'b1: Clock always on 1'b0: Clock auto-gate
6	RW	0x0	isp_dem_ram_clk_on Isp_dem_ram clock control 1'b1: Clock always on 1'b0: Clock auto-gate

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Bit	Attr	Reset Value	Description
5	RW	0x0	isp_fifo_ram_clk_on Isp_fifo_ram clock control 1'b1: Clock always on 1'b0: Clock auto-gate
4	RW	0x0	mipi_ram_clk_on Mipi_ram clock control 1'b1: Clock always on 1'b0: Clock auto-gate
3	RW	0x0	isp_3a_clk_on 3A processing clock control 1'b1: Clock always on 1'b0: Clock auto-gate
2	RW	0x0	isp_yuv_clk_on Yuv path clock control 1'b1: Clock always on 1'b0: Clock auto-gate
1	RW	0x0	isp_rgb_clk_on Rgb path clock control 1'b1: Clock always on 1'b0: Clock auto-gate
0	RW	0x0	isp_raw_clk_on Raw path clock control 1'b1: Clock always on 1'b0: Clock auto-gate

CTRL_0000_VI_ICCL

Address: Operational Base(0x21D00000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x1	vi_mpfbc_clk_enable Mpfbc clock enable 1'b1: Processing mode 1'b0: Power safe
13	RW	0x1	vi_brsz_clk_enable Bypass picture resize clock enable 1'b1: Processing mode 1'b0: Power safe
12	RO	0x0	reserved
11	RW	0x1	vi_mipi_clk_enable MIPI interface clock enable 1'b1: Processing mode 1'b0: Power safe
10	RW	0x1	vi_smia_clk_enable SMIA interface clock enable 1'b1: Processing mode 1'b0: Power safe
9	RW	0x1	vi_simp_clk_enable Superimpose clock enable 1'b1: Processing mode 1'b0: Power safe
8	RW	0x1	vi_ie_clk_enable Image effect clock enable 1'b1: Processing mode 1'b0: Power safe
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6	RW	0x1	vi_mi_clk_enable Memory interface clock enable 1'b1: Processing mode 1'b0: Power safe
5	RW	0x1	vi_jpeg_clk_enable JPEG encoder clock enable 1'b1: Processing mode 1'b0: Power safe
4	RW	0x1	vi_srsz_clk_enable Self picture resize clock enable 1'b1: Processing mode 1'b0: Power safe
3	RW	0x1	vi_mrsz_clk_enable Main picture resize clock enable 1'b1: Processing mode 1'b0: Power safe
2	RO	0x0	reserved
1	RW	0x1	vi_cp_clk_enable Color processing clock enable 1'b1: Processing mode 1'b0: Power safe
0	RW	0x1	vi_isp_clk_enable Isp processing clock enable 1'b1: Processing mode 1'b0: Power safe

CTRL_0000_VI_IRCL

Address: Operational Base(0x21D00000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31	W1C	0x0	arst_safety_isp_done Safety reset isp done.
30	RW	0x0	sw_rst_protect_dis Safety protect reset disable
29	RW	0x0	sw_wr_outstanding_dis AXI write not outstanding disable for clean-rst
28	RW	0x0	sw_resp_wait_dis AXI write response waiting disable for clean-rst
27:14	RO	0x0000	reserved
13	RW	0x0	vi_3a_soft_rst 3A software reset 1'b0: Processing mode 1'b1: Reset state 3a can be reset by vi_isp_soft_rst too.
12	RO	0x0	reserved
11	RW	0x0	vi_mipi_soft_rst MIPI Interface software reset 1'b0: Processing mode 1'b1: Reset state
10	RW	0x0	vi_smia_soft_rst SMIA Interface software reset, not used now
9	RW	0x0	vi_simp_soft_rst Superimpose software reset 1'b0: Processing mode 1'b1: Reset state

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Bit	Attr	Reset Value	Description
8	RW	0x0	vi_ie_soft_rst Image effect software reset 1'b0: Processing mode 1'b1: Reset state
7	W1C	0x0	vi_marvin_rst Hardware reset of entire marvin, global reset when high valid 1'b0: Processing mode 1'b1: Reset state
6	RW	0x0	vi_mi_soft_rst Memory interface software reset 1'b0: Processing mode 1'b1: Reset state
5	RW	0x0	vi_jpeg_soft_rst JPEG encoder software reset 1'b0: Processing mode 1'b1: Reset state
4	RW	0x0	vi_srsz_soft_rst Self-picture resize software reset 1'b0: Processing mode 1'b1: Reset state
3	RW	0x0	vi_mrsz_soft_rst Main-picture resize software reset 1'b0: Processing mode 1'b1: Reset state
2	RW	0x0	vi_ycs_soft_rst Y/C splitter software reset 1'b0: Processing mode 1'b1: Reset state
1	RW	0x0	vi_cp_soft_rst Color processing software reset 1'b0: Processing mode 1'b1: Reset state
0	RW	0x0	vi_isp_soft_rst Isp software reset 1'b0: Processing mode 1'b1: Reset state

CTRL_0000_VI_DPCL

Address: Operational Base(0x21D00000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RW	0x0	vi_mi_debug_mode Vi_mi_debug_mode, open clock-gating used
13	RW	0x0	vi_old_mi_sel_rd Vi_old_mi_sel_rd, open clock-gating used
12	RW	0x0	vi_old_mi_sel_wr Vi_old_mi_sel_wr, open clock-gating used
11	RW	0x0	vi_dma_spmux 1'b0: Data from camera interface to self resize 1'b1: Data from DMA read port to self resize
10	RW	0x0	vi_dma_iemux 1'b0: Data from camera interface to image effects 1'b1: Data from DMA read port to image effects

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Bit	Attr	Reset Value	Description
9:8	RW	0x0	if_select selects input interface 2'd0: Parallel interface 2'd1: LVDS interface 2'd2: MIPI interface 2'd3: Reserved
7	RO	0x0	reserved
6:4	RW	0x0	vi_dma_switch DMA read data path selector 0: Path to SPMUX 1: Path to Superimpose 2: Path to Image Effects 3: Reserved 4: Path to ISP Bayer RGB 5: Path to ISP YCNR 6~7: Reserved
3:2	RW	0x0	vi_chan_mode Y/C splitter channel mode 2'd0: Disabled 2'd1: Main path and raw data mode 2'd2: Self path mode 2'd3: Main and self path mode
1:0	RW	0x0	vi_mp_mux Data path selector for main path 2'b00: Data from DMA read port to JPEG encoder 2'b01: Data from main resize to MI, uncompressed 2'b10: Data from main resize to JPEG encoder 2'b11: Reserved

CTRL_0000_SWS_CFG

Address: Operational Base(0x21D00000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31	RO	0x0	isp2pp_hold Enc2isp pipeline hold, read only
30	RW	0x0	sw_isp2enc_path_en_shd ISP to Encoder path enable, shadow register.
29	RO	0x0	sws_working Sws_working for 3a writing status
28	RO	0x0	reserved
27	RW	0x0	sw_clk_dsu_gate_en 1'b0: Clock off during reset 1'b1: Clock on during reset Note: No cross asynchronization for different clock domain
26	RW	0x0	sw_3d_dbr_start_mode 3A begin to write DDR mode 1'b0: After debayer end and all module end 1'b1: Just after debayer end
25	RW	0x0	sw_mipi2isp_fifo_dis V_blank hold fifo disable, backdoor
24	RW	0x0	sw_3a_ddr_write_en 3A result load to DDR enable
23:6	RO	0x00000	reserved
5	RW	0x0	sw_isp2enc_path_en ISP to Encoder path enable

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Bit	Attr	Reset Value	Description
4	RW	0x0	sw_dither_en isp dither enable
3	RW	0x0	sw_ack_frm_pro_dis Vblank optimize disable
2	RW	0x0	sw_mipi_drop_frm_dis Mipi drop frame disable 1'b0: Enable, default 1'b1: Disable Note: only mipi on-the-fly mode needs to use drop frame
1	RW	0x0	sw_isp2pp_pipe_en Isp2pp or isp2enc pipeline handshake, would hold isp pipe when enable
0	RW	0x0	sw_isp2enc_cnt_sel Isp2enc line counter selection. 1'b0: line counter from mp out 1'b1: line counter from isp out

44.4.2.6 BLS

ISP_BLS_3000_CTRL

Address: Operational Base(0x21D03000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	bls_working BLS working signal
29:7	RO	0x000000	reserved
6	RW	0x0	sw_bls3_en BLS3 module before rawlsc only used for AIAWB. BLS3 will share config with BLS2.
5	RW	0x0	sw_bls2_en BLS2 module before rawlsc only used for RAWAWB.
4	RW	0x0	sw_bls1_en BLS1 module after baynr 1'b1: Black level subtraction is enabled 1'b0: Bypass the black level processing
3:2	RW	0x0	sw_bls_win_en 2'b00: No measuring is performed 2'b01: Only window 1 is measured 2'b10: Only window 2 is measured 2'b11: Both windows are measured
1	RW	0x0	sw_bls_mode 1'b1: Subtract measured values 1'b0: Subtract fixed values
0	RW	0x0	sw_bls_en 1'b1: Black level subtraction is enabled 1'b0: Bypass the black level processing

ISP_BLS_3000_SAMPLES

Address: Operational Base(0x21D03000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x00	sw_bls_samples This number to the power of two gives the number of measure samples for each Bayer position. Range 0x00: 2^0=1 to 0x12: 2^18=262144. This number is also the divider for the accumulator for each Bayer position. The accumulation will be stopped, if the number of measured pixels for the current Bayer position is equal to the number of samples. The measure windows must be positioned that way that the number of included pixels of each Bayer position included by both windows is equal or greater than the number of measure samples calculated by 2^BLS_SAMPLES. NOTE: The number of pixels of one Bayer position is 1/4 of the number of all Pixels included by the measure windows.

ISP_BLS_3000_H1_START

Address: Operational Base(0x21D03000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_bls_h1_start Black pixel window 1 horizontal start position

ISP_BLS_3000_H1_STOP

Address: Operational Base(0x21D03000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_bls_h1_stop Black pixel window 1 horizontal stop position

ISP_BLS_3000_V1_START

Address: Operational Base(0x21D03000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_bls_v1_start Black pixel window 1 vertical start position

ISP_BLS_3000_V1_STOP

Address: Operational Base(0x21D03000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_bls_v1_stop Black pixel window 1 vertical stop position

ISP_BLS_3000_H2_START

Address: Operational Base(0x21D03000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_bls_h2_start Black pixel window 2 horizontal start position

ISP_BLS_3000_H2_STOP

Address: Operational Base(0x21D03000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
13:0	RW	0x0000	sw_bls_h2_stop Black pixel window 2 horizontal stop position

ISP_BLS_3000_V2_START

Address: Operational Base(0x21D03000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_bls_v2_start Black pixel window 2 vertical start position

ISP_BLS_3000_V2_STOP

Address: Operational Base(0x21D03000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_bls_v2_stop Black pixel window 2 vertical stop position

ISP_BLS_3000_BLC0_A_FIXED

Address: Operational Base(0x21D03000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	sw_bls_a_fixed Fixed black level for A pixels. Signed two's complement, value range from -4096 to +4095, a positive value will be subtracted from the pixel values.

ISP_BLS_3000_BLC0_B_FIXED

Address: Operational Base(0x21D03000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	sw_bls_b_fixed Fixed black level for B pixels. Signed two's complement, value range from -4096 to +4095.

ISP_BLS_3000_BLC0_C_FIXED

Address: Operational Base(0x21D03000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	sw_bls_c_fixed Fixed black level for C pixels. Signed two's complement, value range from -4096 to +4095.

ISP_BLS_3000_BLC0_D_FIXED

Address: Operational Base(0x21D03000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	sw_bls_d_fixed Fixed black level for D pixels. Signed two's complement, value range from -4096 to +4095.

ISP_BLS_3000_A_MEASURED

Address: Operational Base(0x21D03000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
11:0	RO	0x000	sw_bls_a_measured Measured black level for A pixels

ISP_BLS_3000_B_MEASURED

Address: Operational Base(0x21D03000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	sw_bls_b_measured Measured black level for B pixels

ISP_BLS_3000_C_MEASURED

Address: Operational Base(0x21D03000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	sw_bls_c_measured Measured black level for C pixels

ISP_BLS_3000_D_MEASURED

Address: Operational Base(0x21D03000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	sw_bls_d_measured Measured black level for D pixels

ISP_BLS_3000_BLS1_A_FIXED

Address: Operational Base(0x21D03000) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	sw_bls1_a_fixed Fixed black level for A pixels of bay3dnr-blc ; Signed two's complement, value range from -4096 to +4095, a positive value will be subtracted from the pixel values.

ISP_BLS_3000_BLS1_B_FIXED

Address: Operational Base(0x21D03000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	sw_bls1_b_fixed Fixed black level for B pixels of bay3dnr-blc. Signed two's complement, value range from -4096 to +4095.

ISP_BLS_3000_BLS1_C_FIXED

Address: Operational Base(0x21D03000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	sw_bls1_c_fixed Fixed black level for C pixels of bay3dnr-blc. Signed two's complement, value range from -4096 to +4095.

ISP_BLS_3000_BLS1_D_FIXED

Address: Operational Base(0x21D03000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x0000	sw_bls1_d_fixed Fixed black level for D pixels of bay3dnr-blc. Signed two's complement, value range from -4096 to +4095.

ISP_BLS_3000_BLS2_A_FIXED

Address: Operational Base(0x21D03000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	sw_bls2_a_fixed Fixed black level for A pixels of 3a-awb. Signed two's complement, value range from -4096 to +4095, a positive value will be subtracted from the pixel values.

ISP_BLS_3000_BLS2_B_FIXED

Address: Operational Base(0x21D03000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	sw_bls2_b_fixed Fixed black level for B pixels of 3a-awb. Signed two's complement, value range from -4096 to +4095.

ISP_BLS_3000_BLS2_C_FIXED

Address: Operational Base(0x21D03000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	sw_bls2_c_fixed Fixed black level for C pixels of 3a-awb. Signed two's complement, value range from -4096 to +4095.

ISP_BLS_3000_BLS2_D_FIXED

Address: Operational Base(0x21D03000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	sw_bls2_d_fixed Fixed black level for D pixels of 3a-awb. Signed two's complement, value range from -4096 to +4095.

ISP_BLS_3000_ISP_OB_OFFSET

Address: Operational Base(0x21D03000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_isp_ob_offset1 Add OB_offset1 for protecting dark texture(low 9bit in 12bit).
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_isp_ob_offset Add OB_offset for protecting dark texture(low 9bit in 12bit), if not equal to zero then bls1 will auto-enable

ISP_BLS_3000_ISP_OB_PREDGAIN

Address: Operational Base(0x21D03000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0100	sw_isp_ob_predgain OB pre-dgain{8,8} for replacing adrc-gain, in linear mode. When this value is configured to 0, pre-dgain is disabled.

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ISP_BLS_3000_ISP_OB_MAX

Address: Operational Base(0x21D03000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	sw_isp_ob_max AWB1 max value clip, value equal to predgain*0xfff

ISP_BLS_3000_BLS3_AB_FIXED

Address: Operational Base(0x21D03000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_bls3_b_fixed Fixed black level for B pixels of aiawb.
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_bls3_a_fixed Fixed black level for A pixels of 3a-awb.

ISP_BLS_3000_BLS3_CD_FIXED

Address: Operational Base(0x21D03000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_bls3_d_fixed Fixed black level for D pixels of aiawb.
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_bls3_c_fixed Fixed black level for C pixels of 3a-awb.

44.4.2.7 DPCC

ISP_DPCC_3400_CTRL0

Address: Operational Base(0x21D03400) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	ro_dpcc_working DPCC working signal
29:3	RO	0x0000000	reserved
2	RW	0x1	sw_dpcc_step1_en DPCC step1 enable bit
1	RW	0x0	sw_dpcc_grayscale_mode 1'b0: RAW BAYER mode input 1'b1: Gray mode input
0	RW	0x0	sw_dpcc_enable DPCC module enable bit

ISP_DPCC_3400_CTRL1

Address: Operational Base(0x21D03400) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RW	0x0	sw_dpcc_border_bypss_mode 1'b0: Border do DPCC 1'b1: Border(left and right two colum) output bypass
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:5	RW	0x0	sw_dpcc_roc_out_sel 2'b00: ROC(Rank Order Check) method1 2'b01: ROC method2 2'b10: ROC method3 2'b11: Reserved
4	RW	0x0	sw_dpcc_output_sel 1'b0: Select median mode 1'b1: Select ROC output mode
3:2	RW	0x0	sw_dpcc_median_mode_sel Bit0 for Green channel, bit1 for rb channel. 1'b0: Select 4 or 5 pixel output median 1'b1: Select 9 pixel (3x3) output median
1:0	RW	0x3	sw_dpcc_incl_center_en Output median mode 2x2+1 enable bit. Bit0 for Green channel, bit1 for rb channel.

ISP_DPCC_3400_CTRL2

Address: Operational Base(0x21D03400) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x1	sw_dpcc_engine_en DPCC engine enable bit Bit0 for engine0, bit1 for engine1,bit2 for engine2, bit3 for engine3.

ISP_DPCC_3400_ENGINE0_CTRL

Address: Operational Base(0x21D03400) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RW	0x01	sw_dpcc_engine0_rb_set Bit0: Peak detect(PD) enable bit Bit1: Edge preservation detect(EPD) enable bit Bit2: Order detect(EPD) enable bit Bit3: Rank differernce detect(RDD) enable bit Bit4: Rank detect(RD) enable bit Bit5: Rank Order detect(ROD) enable bit
7:6	RO	0x0	reserved
5:0	RW	0x01	sw_dpcc_engine0_green_set Bit0: Peak detect(PD) enable bit Bit1: Edge preservation detect(EPD) enable bit Bit2: Order detect(EPD) enable bit Bit3: Rank differernce detect(RDD) enable bit Bit4: Rank detect(RD) enable bit Bit5: Rank Order detect(ROD) enable bit

ISP_DPCC_3400_ENGINE1_CTRL

Address: Operational Base(0x21D03400) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x01	sw_dpcc_engine1_rb_set Bit0: Peak detect(PD) enable bit Bit1: Edge preservation detect(EPD) enable bit Bit2: Order detect(EPD) enable bit Bit3: Rank differernce detect(RDD) enable bit Bit4: Rank detect(RD) enable bit Bit5: Rank Order detect(ROD) enable bit
7:6	RO	0x0	reserved
5:0	RW	0x01	sw_dpcc_engine1_green_set Bit0: Peak detect(PD) enable bit Bit1: Edge preservation detect(EPD) enable bit Bit2: Order detect(EPD) enable bit Bit3: Rank differernce detect(RDD) enable bit Bit4: Rank detect(RD) enable bit Bit5: Rank Order detect(ROD) enable bit

ISP_DPCC_3400_ENGINE2_CTRL

Address: Operational Base(0x21D03400) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RW	0x01	sw_dpcc_engine2_rb_set Bit0: Peak detect(PD) enable bit Bit1: Edge preservation detect(EPD) enable bit Bit2: Order detect(EPD) enable bit Bit3: Rank differernce detect(RDD) enable bit Bit4: Rank detect(RD) enable bit Bit5: Rank Order detect(ROD) enable bit
7:6	RO	0x0	reserved
5:0	RW	0x01	sw_dpcc_engine2_green_set Bit0: Peak detect(PD) enable bit Bit1: Edge preservation detect(EPD) enable bit Bit2: Order detect(EPD) enable bit Bit3: Rank differernce detect(RDD) enable bit Bit4: Rank detect(RD) enable bit Bit5: Rank Order detect(ROD) enable bit

ISP_DPCC_3400_ENGINE0_SET0

Address: Operational Base(0x21D03400) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_dpcc_rod_mindis1_rb Min distance for ROD0
23:16	RW	0x00	sw_dpcc_rod_mindis1_g Min distance for ROD0
15:8	RW	0x00	sw_dpcc_epd0_thr_rb EPD threshold config value(U8)
7:0	RW	0x00	sw_dpcc_epd0_thr_g EPD threshold config value(U8)

ISP_DPCC_3400_ENGINE0_SET1

Address: Operational Base(0x21D03400) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	sw_dpcc_rod0_dis_min Distance scale for min channel
23:22	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
21:16	RW	0x00	sw_dpcc_rod0_dis_max Distance scale for max channel
15:14	RO	0x0	reserved
13:8	RW	0x04	sw_dpcc_epd0_fac_rb EPD factor(U6)
7:6	RO	0x0	reserved
5:0	RW	0x04	sw_dpcc_epd0_fac_g EPD factor(U6)

ISP_DPCC_3400_ENGINE0_SET2

Address: Operational Base(0x21D03400) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RW	0x04	sw_dpcc_pd0_fac_rb PD factor U6
7:6	RO	0x0	reserved
5:0	RW	0x00	sw_dpcc_pd0_fac_g PD factorU6

ISP_DPCC_3400_ENGINE0_SET3

Address: Operational Base(0x21D03400) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x0a	sw_dpcc_rdd0_thr_rb RDD factorU8
7:0	RW	0x0a	sw_dpcc_rdd0_thr_g RDD factorU8

ISP_DPCC_3400_ENGINE0_SET4

Address: Operational Base(0x21D03400) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RW	0x20	sw_dpcc_rd0_fac_rb RD factor(U6)
7:6	RO	0x0	reserved
5:0	RW	0x20	sw_dpcc_rd0_fac_g RD factor(U6)

ISP_DPCC_3400_ENGINE1_SET0

Address: Operational Base(0x21D03400) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_dpcc_rod1_mindis_rb Min distance for ROD1
23:16	RW	0x00	sw_dpcc_rod1_mindis_g Min distance for ROD1
15:8	RW	0x00	sw_dpcc_epd1_thr_rb EPD threshold config value(U8)
7:0	RW	0x00	sw_dpcc_epd1_thr_g EPD threshold config value(U8)

ISP_DPCC_3400_ENGINE1_SET1

Address: Operational Base(0x21D03400) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:24	RW	0x00	sw_dpcc_rod1_dis_min Distance scale for min channel
23:22	RO	0x0	reserved
21:16	RW	0x00	sw_dpcc_rod1_dis_max Distance scale for max channel
15:14	RO	0x0	reserved
13:8	RW	0x04	sw_dpcc_epd1_fac_rb EPD factor(U6)
7:6	RO	0x0	reserved
5:0	RW	0x04	sw_dpcc_epd1_fac_g EPD factor(U6)

ISP_DPCC_3400_ENGINE1_SET2

Address: Operational Base(0x21D03400) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RW	0x04	sw_dpcc_pd1_fac_rb PD factor U6
7:6	RO	0x0	reserved
5:0	RW	0x00	sw_dpcc_pd1_fac_g PD factorU6

ISP_DPCC_3400_ENGINE1_SET3

Address: Operational Base(0x21D03400) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x0a	sw_dpcc_rdd1_thr_rb RDD factorU8
7:0	RW	0x0a	sw_dpcc_rdd1_thr_g RDD factorU8

ISP_DPCC_3400_ENGINE1_SET4

Address: Operational Base(0x21D03400) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RW	0x20	sw_dpcc_rd1_fac_rb RD factor(U6)
7:6	RO	0x0	reserved
5:0	RW	0x20	sw_dpcc_rd1_fac_g RD factor(U6)

ISP_DPCC_3400_ENGINE2_SET0

Address: Operational Base(0x21D03400) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_dpcc_rod2_mindis_rb Min distance for ROD0
23:16	RW	0x00	sw_dpcc_rod2_mindis_g Min distance for ROD0
15:8	RW	0x00	sw_dpcc_epd2_thr_rb EPD threshold config value(U8)
7:0	RW	0x00	sw_dpcc_epd2_thr_g EPD threshold config value(U8)

ISP_DPCC_3400_ENGINE2_SET1

Address: Operational Base(0x21D03400) + offset (0x0044)

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Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	sw_dpcc_rod2_dis_min Distance scale for min channel
23:22	RO	0x0	reserved
21:16	RW	0x00	sw_dpcc_rod2_dis_max Distance scale for max channel
15:14	RO	0x0	reserved
13:8	RW	0x04	sw_dpcc_epd2_fac_rb EPD factor(U6)
7:6	RO	0x0	reserved
5:0	RW	0x04	sw_dpcc_epd2_fac_g EPD factor(U6)

ISP_DPCC_3400_ENGINE2_SET2

Address: Operational Base(0x21D03400) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RW	0x04	sw_dpcc_pd2_fac_rb PD factor U6
7:6	RO	0x0	reserved
5:0	RW	0x00	sw_dpcc_pd2_fac_g PD factorU6

ISP_DPCC_3400_ENGINE2_SET3

Address: Operational Base(0x21D03400) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x0a	sw_dpcc_rdd2_thr_rb RDD factorU8
7:0	RW	0x0a	sw_dpcc_rdd2_thr_g RDD factorU8

ISP_DPCC_3400_ENGINE2_SET4

Address: Operational Base(0x21D03400) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RW	0x20	sw_dpcc_rd2_fac_rb RD factor(U6)
7:6	RO	0x0	reserved
5:0	RW	0x20	sw_dpcc_rd2_fac_g RD factor(U6)

ISP_DPCC_3400_ENGINE_OD_SET

Address: Operational Base(0x21D03400) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x0	sw_dpcc_od2_range OD range for engine2, bit[1:0] for green channel, bit[3:2] for rb channel.
7:4	RW	0x0	sw_dpcc_od1_range OD range for engine1, bit[1:0] for green channel, bit[3:2] for rb channel.
3:0	RW	0x0	sw_dpcc_od0_range OD range for engine0, bit[1:0] for green channel, bit[3:2] for rb channel.

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ISP_DPCC_3400_ENGINE_RDD_SET

Address: Operational Base(0x21D03400) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:8	RW	0x7	sw_dpcc_rdd2_range RDD range for engine2, bit[1:0] for green channel, bit[3:2] for rb channel.
7:4	RW	0x3	sw_dpcc_rdd1_range RDD range for engine1, bit[1:0] for green channel, bit[3:2] for rb channel.
3:0	RW	0xf	sw_dpcc_rdd0_range RDD range for engine0, bit[1:0] for green channel, bit[3:2] for rb channel.

ISP_DPCC_3400_PDAF_EN

Address: Operational Base(0x21D03400) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	sw_pdaf_en PDAF point replace enable bit

ISP_DPCC_3400_PDAF_POINT_EN

Address: Operational Base(0x21D03400) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15	RW	0x0	sw_pdaf_point15_en Point15 replace enable bit
14	RW	0x0	sw_pdaf_point14_en Point14 replace enable bit
13	RW	0x0	sw_pdaf_point13_en Point13 replace enable bit
12	RW	0x0	sw_pdaf_point12_en Point12 replace enable bit
11	RW	0x0	sw_pdaf_point11_en Point11 replace enable bit
10	RW	0x0	sw_pdaf_point10_en Point10 replace enable bit
9	RW	0x0	sw_pdaf_point9_en Point9 replace enable bit
8	RW	0x0	sw_pdaf_point8_en Point8 replace enable bit
7	RW	0x0	sw_pdaf_point7_en Point7 replace enable bit
6	RW	0x0	sw_pdaf_point6_en Point6 replace enable bit
5	RW	0x0	sw_pdaf_point5_en Point5 replace enable bit
4	RW	0x0	sw_pdaf_point4_en Point4 replace enable bit
3	RW	0x0	sw_pdaf_point3_en Point3 replace enable bit
2	RW	0x0	sw_pdaf_point2_en Point2 replace enable bit
1	RW	0x0	sw_pdaf_point1_en Point1 replace enable bit

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Bit	Attr	Reset Value	Description
0	RW	0x0	sw_pdaf_point0_en Point0 replace enable bit

ISP_DPCC_3400_PDAF_OFFSET

Address: Operational Base(0x21D03400) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_pdaf_offsety The beginning y coordinate of pdaf pattern
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_pdaf_offsetx The beginning x coordinate of pdaf pattern

ISP_DPCC_3400_PDAF_WRAP

Address: Operational Base(0x21D03400) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	sw_pdaf_wrapy The height of pattren , 0x00 is 1, 0x0f is 16
15:8	RO	0x00	reserved
7:0	RW	0x00	sw_pdaf_wrapx The width of pattren , 0x00 is 1, 0x0f is 16

ISP_DPCC_3400_PDAF_SCOPE

Address: Operational Base(0x21D03400) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_pdaf_wrapy_num The num of wrapy
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_pdaf_wrapx_num The num of wrapx

ISP_DPCC_3400_PDAF_POINT_0

Address: Operational Base(0x21D03400) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_pdaf_point1_y Point1 y coordinate
23:16	RW	0x00	sw_pdaf_point1_x Point1 x coordinate
15:8	RW	0x00	sw_pdaf_point0_y Point0 y coordinate
7:0	RW	0x00	sw_pdaf_point0_x Point0 x coordinate

ISP_DPCC_3400_PDAF_POINT_1

Address: Operational Base(0x21D03400) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_pdaf_point3_y Point3 y coordinate
23:16	RW	0x00	sw_pdaf_point3_x Point3 x coordinate
15:8	RW	0x00	sw_pdaf_point2_y Point2 y coordinate

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	sw_pdaf_point2_x Point2 x coordinate

ISP_DPCC_3400_PDAF_POINT_2

Address: Operational Base(0x21D03400) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_pdaf_point5_y Point5 y coordinate
23:16	RW	0x00	sw_pdaf_point5_x Point5 x coordinate
15:8	RW	0x00	sw_pdaf_point4_y Point4 y coordinate
7:0	RW	0x00	sw_pdaf_point4_x Point4 x coordinate

ISP_DPCC_3400_PDAF_POINT_3

Address: Operational Base(0x21D03400) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_pdaf_point7_y Point7 y coordinate
23:16	RW	0x00	sw_pdaf_point7_x Point7 x coordinate
15:8	RW	0x00	sw_pdaf_point6_y Point6 y coordinate
7:0	RW	0x00	sw_pdaf_point6_x Point6 x coordinate

ISP_DPCC_3400_PDAF_POINT_4

Address: Operational Base(0x21D03400) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_pdaf_point9_y Point9 y coordinate
23:16	RW	0x00	sw_pdaf_point9_x Point9 x coordinate
15:8	RW	0x00	sw_pdaf_point8_y Point8 y coordinate
7:0	RW	0x00	sw_pdaf_point8_x Point8 x coordinate

ISP_DPCC_3400_PDAF_POINT_5

Address: Operational Base(0x21D03400) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_pdaf_point11_y Point11 y coordinate
23:16	RW	0x00	sw_pdaf_point11_x Point11 x coordinate
15:8	RW	0x00	sw_pdaf_point10_y Point10 y coordinate
7:0	RW	0x00	sw_pdaf_point10_x Point10 x coordinate

ISP_DPCC_3400_PDAF_POINT_6

Address: Operational Base(0x21D03400) + offset (0x009C)

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_pdaf_point13_y Point13 y coordinate
23:16	RW	0x00	sw_pdaf_point13_x Point13 x coordinate
15:8	RW	0x00	sw_pdaf_point12_y Point12 y coordinate
7:0	RW	0x00	sw_pdaf_point12_x Point12 x coordinate

ISP_DPCC_3400_PDAF_POINT_7

Address: Operational Base(0x21D03400) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_pdaf_point15_y Point15 y coordinate
23:16	RW	0x00	sw_pdaf_point15_x Point15 x coordinate
15:8	RW	0x00	sw_pdaf_point14_y Point14 y coordinate
7:0	RW	0x00	sw_pdaf_point14_x Point14 x coordinate

ISP_DPCC_3400_PDAF_FORWARD_MED

Address: Operational Base(0x21D03400) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	sw_pdaf_forward_med 1'b0: Select backward median value to replace pdaf point 1'b1: Select forward median value to replace pdaf point

44.4.2.8 HDRMGE

ISP_HDRMGE_3800_CTRL

Address: Operational Base(0x21D03800) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	hw_hdrmge_en_shd HDR-Merge enable shadow
30	RO	0x0	ro_hdrmge_working Hdrmge working status
29:8	RO	0x000000	reserved
7	RW	0x0	hw_hdrmge_s_base_mode HDR-Merge hugemsk enable, shadow reg 1'b0: Normal mode in sw_hdrmge_s_base_en 1'b1: Force long frame mode
6	RW	0x0	hw_hdrmge_channelDetection_en Enable each_raw merge for noise reduce
5:4	RW	0x0	hw_hdrmge_dbg_mode Merge debug mode 2'b00: Debug mode off 2'b01: Channel0 of S 2'b10: Channel1 of M 2'b11: Channel2 of L In HDRX2 debug config: sw_hdrmge_en=0sw_hdrmge_mode=1hdrmge_dbg_mode=2, it would select Channel1 bypass output.

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	hw_hdrmge_frame_mode HDR-Merge mode 2'b00: Normal 2'b01: Framex2 2'b10: Framex3
1	RW	0x0	hw_hdrmge_shortBase_en HDR-Merge hugemsk enable, shadow reg 1'b0: Long base method 1'b1: Short base method
0	RW	0x0	hw_hdrmge_module_en HDR-Merge function enable, shadow reg

ISP_HDRMGE_3800_GAIN0

Address: Operational Base(0x21D03800) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x100	hw_hdrmge_short_invGain 1/Short -gain=[0,12}, shadow reg
15:14	RO	0x0	reserved
13:0	RW	0x0400	hw_hdrmge_short_gain Short -gain=[6,6], shadow reg

ISP_HDRMGE_3800_GAIN1

Address: Operational Base(0x21D03800) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x400	hw_hdrmge_medium_invGain 1/Middle-gain=[0,12], shadow reg (1106 no use)
15:11	RO	0x00	reserved
10:0	RW	0x100	hw_hdrmge_medium_gain Middle-gain=[5,6], shadow reg

ISP_HDRMGE_3800_GAIN2

Address: Operational Base(0x21D03800) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x40	hw_hdrmge_long_gain Long -gain=[1,6], shadow reg (1106 no use)

ISP_HDRMGE_3800_LIGHTZ

Address: Operational Base(0x21D03800) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	hw_hdrmge_lmDiff_offset Merge lm_dif_0p15 for diff-offset of (M_frame*gain1 - L_frame*gain2*0p9)/gain1 + 0p15.
23:16	RW	0xff	hw_hdrmge_lmDiff_scale Merge lm_dif_0p9 for diff-scale of (M_frame*gain1 - L_frame*gain2*0p9)/gain1 + 0p15.
15:8	RW	0x00	hw_hdrmge_msDiff_offset Merge ms_0p15 for diff-offset of (S_frame*gain0 - M_frame*gain1*0p8)/gain0 + 0p15.
7:0	RW	0xff	hw_hdrmge_msDiff_scale Merge ms_dif_0p8 for diff-scale of (S_frame*gain0 - M_frame*gain1*0p8)/gain0 + 0p15.

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ISP_HDRMGE_3800_MS_DIFF

Address: Operational Base(0x21D03800) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:22	RW	0x200	hw_hdrmge_msAbsDiffThred_maxLimit Threshold-high of ms for clipping diff, [0,10]
21:12	RW	0x000	hw_hdrmge_msAbsDiffThred_minLimit Threshold-low of ms for clipping diff, [0,10]
11	RO	0x0	reserved
10:0	RW	0x080	hw_hdrmge_msAbsDiff_scale Ms-diff*scale[3,8] into range 0-255, {3,8}

ISP_HDRMGE_3800_LM_DIFF

Address: Operational Base(0x21D03800) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:22	RW	0x200	hw_hdrmge_lmAbsDiffThred_maxLimit Merge threshold-high of lm for clipping diff, [0,10] (1106 no use)
21:12	RW	0x000	hw_hdrmge_lmAbsDiffThred_minLimit Merge threshold-low of lm for clipping diff, [0,10] (1106 no use)
11	RO	0x0	reserved
10:0	RW	0x080	hw_hdrmge_lmAbsDiff_scale Merge lm-diff*scale[3,8] into range 0-255, [3,8] (1106 no use)

ISP_HDRMGE_3800_DIFF_Y0

Address: Operational Base(0x21D03800) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	hw_hdrmge_lmLumaDiff2wgt_val0 L-curve1 maskUseCur=D of Y0
15:10	RO	0x00	reserved
9:0	RW	0x000	hw_hdrmge_msLumaDiff2wgt_val0 L-curve0 maskUseCur=D of Y0

ISP_HDRMGE_3800_DIFF_Y1

Address: Operational Base(0x21D03800) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x0c9	hw_hdrmge_lmLumaDiff2wgt_val1 L-curve1 maskUseCur=D of Y1
15:10	RO	0x00	reserved
9:0	RW	0x0c9	hw_hdrmge_msLumaDiff2wgt_val1 L-curve0 maskUseCur=D of Y1

ISP_HDRMGE_3800_DIFF_Y2

Address: Operational Base(0x21D03800) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x1fa	hw_hdrmge_lmLumaDiff2wgt_val2 L-curve1 maskUseCur=D of Y2
15:10	RO	0x00	reserved
9:0	RW	0x1fa	hw_hdrmge_msLumaDiff2wgt_val2 L-curve0 maskUseCur=D of Y2

ISP_HDRMGE_3800_DIFF_Y3

Address: Operational Base(0x21D03800) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RW	0x2c0	hw_hdrmge_lmLumaDiff2wgt_val3 L-curve1 maskUseCur=D of Y3
15:10	RO	0x00	reserved
9:0	RW	0x2c0	hw_hdrmge_msLumaDiff2wgt_val3 L-curve0 maskUseCur=D of Y3

ISP_HDRMGE_3800_DIFF_Y4

Address: Operational Base(0x21D03800) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x32f	hw_hdrmge_lmLumaDiff2wgt_val4 L-curve1 maskUseCur=D of Y4
15:10	RO	0x00	reserved
9:0	RW	0x32f	hw_hdrmge_msLumaDiff2wgt_val4 L-curve0 maskUseCur=D of Y4

ISP_HDRMGE_3800_DIFF_Y5

Address: Operational Base(0x21D03800) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x370	hw_hdrmge_lmLumaDiff2wgt_val5 L-curve1 maskUseCur=D
15:10	RO	0x00	reserved
9:0	RW	0x370	hw_hdrmge_msLumaDiff2wgt_val5 L-curve0 maskUseCur=D

ISP_HDRMGE_3800_DIFF_Y6

Address: Operational Base(0x21D03800) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x397	hw_hdrmge_lmLumaDiff2wgt_val6 L-curve1 maskUseCur=D
15:10	RO	0x00	reserved
9:0	RW	0x397	hw_hdrmge_msLumaDiff2wgt_val6 L-curve0 maskUseCur=D

ISP_HDRMGE_3800_DIFF_Y7

Address: Operational Base(0x21D03800) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x3b1	hw_hdrmge_lmLumaDiff2wgt_val7 L-curve1 maskUseCur=D
15:10	RO	0x00	reserved
9:0	RW	0x3b1	hw_hdrmge_msLumaDiff2wgt_val7 L-curve0 maskUseCur=D

ISP_HDRMGE_3800_DIFF_Y8

Address: Operational Base(0x21D03800) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x3c2	hw_hdrmge_lmLumaDiff2wgt_val8 L-curve1 maskUseCur=D
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x3c2	hw_hdrmge_msLumaDiff2wgt_val8 L-curve0 maskUseCur=D

ISP_HDRMGE_3800_DIFF_Y9

Address: Operational Base(0x21D03800) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x3cf	hw_hdrmge_lmLumaDiff2wgt_val9 L-curve1 maskUseCur=D
15:10	RO	0x00	reserved
9:0	RW	0x3cf	hw_hdrmge_msLumaDiff2wgt_val9 L-curve0 maskUseCur=D

ISP_HDRMGE_3800_DIFF_Y10

Address: Operational Base(0x21D03800) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x3d8	hw_hdrmge_lmLumaDiff2wgt_val10 L-curve1 maskUseCur=D
15:10	RO	0x00	reserved
9:0	RW	0x3d8	hw_hdrmge_msLumaDiff2wgt_val10 L-curve0 maskUseCur=D

ISP_HDRMGE_3800_DIFF_Y11

Address: Operational Base(0x21D03800) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x3de	hw_hdrmge_lmLumaDiff2wgt_val11 L-curve1 maskUseCur=D
15:10	RO	0x00	reserved
9:0	RW	0x3de	hw_hdrmge_msLumaDiff2wgt_val11 L-curve0 maskUseCur=D

ISP_HDRMGE_3800_DIFF_Y12

Address: Operational Base(0x21D03800) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x3e4	hw_hdrmge_lmLumaDiff2wgt_val12 L-curve1 maskUseCur=D
15:10	RO	0x00	reserved
9:0	RW	0x3e4	hw_hdrmge_msLumaDiff2wgt_val12 L-curve0 maskUseCur=D

ISP_HDRMGE_3800_DIFF_Y13

Address: Operational Base(0x21D03800) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x3e8	hw_hdrmge_lmLumaDiff2wgt_val13 L-curve1 maskUseCur=D
15:10	RO	0x00	reserved
9:0	RW	0x3e8	hw_hdrmge_msLumaDiff2wgt_val13 L-curve0 maskUseCur=D

ISP_HDRMGE_3800_DIFF_Y14

Address: Operational Base(0x21D03800) + offset (0x0058)

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Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x3eb	hw_hdrmge_lmLumaDiff2wgt_val14 L-curve1 maskUseCur=D
15:10	RO	0x00	reserved
9:0	RW	0x3eb	hw_hdrmge_msLumaDiff2wgt_val14 L-curve0 maskUseCur=D

ISP_HDRMGE_3800_DIFF_Y15

Address: Operational Base(0x21D03800) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x3ee	hw_hdrmge_lmLumaDiff2wgt_val15 L-curve1 maskUseCur=D
15:10	RO	0x00	reserved
9:0	RW	0x3ee	hw_hdrmge_msLumaDiff2wgt_val15 L-curve0 maskUseCur=D

ISP_HDRMGE_3800_DIFF_Y16

Address: Operational Base(0x21D03800) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x3f0	hw_hdrmge_lmLumaDiff2wgt_val16 L-curve1 maskUseCur=D of Y16
15:10	RO	0x00	reserved
9:0	RW	0x3f0	hw_hdrmge_msLumaDiff2wgt_val16 L-curve0 maskUseCur=D of Y16

ISP_HDRMGE_3800_OVER_Y0

Address: Operational Base(0x21D03800) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x031	hw_hdrmge_lmRawDiff2wgt_val0 Curve: sw_hdrmge_l_raw1_xx for each_raw MS diff of curve-L
19:10	RW	0x031	hw_hdrmge_msRawDiff2wgt_val0 Curve: sw_hdrmge_l_raw0_xx for each_raw MS diff of curve-L
9:0	RW	0x000	hw_hdrmge_luma2wgt_val0 E-curve over_exp_normal of Y-0

ISP_HDRMGE_3800_OVER_Y1

Address: Operational Base(0x21D03800) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x057	hw_hdrmge_lmRawDiff2wgt_val1 Curve: sw_hdrmge_l_raw1_xx for each_raw MS diff of curve-L
19:10	RW	0x057	hw_hdrmge_msRawDiff2wgt_val1 Curve: sw_hdrmge_l_raw0_xx for each_raw MS diff of curve-L
9:0	RW	0x001	hw_hdrmge_luma2wgt_val1 E-curve over_exp_normal of Y-1

ISP_HDRMGE_3800_OVER_Y2

Address: Operational Base(0x21D03800) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:20	RW	0x098	hw_hdrmge_lmRawDiff2wgt_val2 sw_hdrmge_l_raw1_xx for each_raw MS diff of curve-L
19:10	RW	0x098	hw_hdrmge_msRawDiff2wgt_val2 Curve: sw_hdrmge_l_raw0_xx for each_raw MS diff of curve-L
9:0	RW	0x004	hw_hdrmge_luma2wgt_val2 E-curve over_exp_normal of Y-2

ISP_HDRMGE_3800_OVER_Y3

Address: Operational Base(0x21D03800) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x0fb	hw_hdrmge_lmRawDiff2wgt_val3 Curve: sw_hdrmge_l_raw1_xx for each_raw MS diff of curve-L
19:10	RW	0x0fb	hw_hdrmge_msRawDiff2wgt_val3 Curve: sw_hdrmge_l_raw0_xx for each_raw MS diff of curve-L
9:0	RW	0x00e	hw_hdrmge_luma2wgt_val3 E-curve over_exp_normal of Y-3

ISP_HDRMGE_3800_OVER_Y4

Address: Operational Base(0x21D03800) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x183	hw_hdrmge_lmRawDiff2wgt_val4 Curve: sw_hdrmge_l_raw1_xx for each_raw MS diff of curve-L
19:10	RW	0x183	hw_hdrmge_msRawDiff2wgt_val4 Curve: sw_hdrmge_l_raw0_xx for each_raw MS diff of curve-L
9:0	RW	0x031	hw_hdrmge_luma2wgt_val4 E-curve over_exp_normal of Y-4

ISP_HDRMGE_3800_OVER_Y5

Address: Operational Base(0x21D03800) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x220	hw_hdrmge_lmRawDiff2wgt_val5 Curve: sw_hdrmge_l_raw1_xx for each_raw MS diff of curve-L
19:10	RW	0x220	hw_hdrmge_msRawDiff2wgt_val5 Curve: sw_hdrmge_l_raw0_xx for each_raw MS diff of curve-L
9:0	RW	0x098	hw_hdrmge_luma2wgt_val5 E-curve over_exp_normal of Y-5

ISP_HDRMGE_3800_OVER_Y6

Address: Operational Base(0x21D03800) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x2b7	hw_hdrmge_lmRawDiff2wgt_val6 Curve: sw_hdrmge_l_raw1_xx for each_raw MS diff of curve-L
19:10	RW	0x2b7	hw_hdrmge_msRawDiff2wgt_val6 Curve: sw_hdrmge_l_raw0_xx for each_raw MS diff of curve-L
9:0	RW	0x183	hw_hdrmge_luma2wgt_val6 E-curve over_exp_normal of Y-6

ISP_HDRMGE_3800_OVER_Y7

Address: Operational Base(0x21D03800) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:20	RW	0x331	hw_hdrmge_lmRawDiff2wgt_val7 Curve: sw_hdrmge_l_raw1_xx for each_raw MS diff of curve-L
19:10	RW	0x331	hw_hdrmge_msRawDiff2wgt_val7 Curve: sw_hdrmge_l_raw0_xx for each_raw MS diff of curve-L
9:0	RW	0x2b7	hw_hdrmge_luma2wgt_val7 E-curve over_exp_normal of Y-7

ISP_HDRMGE_3800_OVER_Y8

Address: Operational Base(0x21D03800) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x386	hw_hdrmge_lmRawDiff2wgt_val8 Curve: sw_hdrmge_l_raw1_xx for each_raw MS diff of curve-L
19:10	RW	0x386	hw_hdrmge_msRawDiff2wgt_val8 Curve: sw_hdrmge_l_raw0_xx for each_raw MS diff of curve-L
9:0	RW	0x386	hw_hdrmge_luma2wgt_val8 E-curve over_exp_normal of Y-8

ISP_HDRMGE_3800_OVER_Y9

Address: Operational Base(0x21D03800) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x3bb	hw_hdrmge_lmRawDiff2wgt_val9 Curve: sw_hdrmge_l_raw1_xx for each_raw MS diff of curve-L
19:10	RW	0x3bb	hw_hdrmge_msRawDiff2wgt_val9 Curve: sw_hdrmge_l_raw0_xx for each_raw MS diff of curve-L
9:0	RW	0x3da	hw_hdrmge_luma2wgt_val9 E-curve over_exp_normal of Y-9

ISP_HDRMGE_3800_OVER_Y10

Address: Operational Base(0x21D03800) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x3da	hw_hdrmge_lmRawDiff2wgt_val10 Curve: sw_hdrmge_l_raw1_xx for each_raw MS diff of curve-L
19:10	RW	0x3da	hw_hdrmge_msRawDiff2wgt_val10 Curve: sw_hdrmge_l_raw0_xx for each_raw MS diff of curve-L
9:0	RW	0x3f5	hw_hdrmge_luma2wgt_val10 E-curve over_exp_normal of Y-10

ISP_HDRMGE_3800_OVER_Y11

Address: Operational Base(0x21D03800) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x3eb	hw_hdrmge_lmRawDiff2wgt_val11 Curve: sw_hdrmge_l_raw1_xx for each_raw MS diff of curve-L
19:10	RW	0x3eb	hw_hdrmge_msRawDiff2wgt_val11 Curve: sw_hdrmge_l_raw0_xx for each_raw MS diff of curve-L
9:0	RW	0x3fd	hw_hdrmge_luma2wgt_val11 E-curve over_exp_normal of Y-11

ISP_HDRMGE_3800_OVER_Y12

Address: Operational Base(0x21D03800) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:20	RW	0x3f5	hw_hdrmge_lmRawDiff2wgt_val12 Curve: sw_hdrmge_l_raw1_xx for each_raw MS diff of curve-L
19:10	RW	0x3f5	hw_hdrmge_msRawDiff2wgt_val12 Curve: sw_hdrmge_l_raw0_xx for each_raw MS diff of curve-L
9:0	RW	0x3ff	hw_hdrmge_luma2wgt_val12 E-curve over_exp_normal of Y-12

ISP_HDRMGE_3800_OVER_Y13

Address: Operational Base(0x21D03800) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x3fa	hw_hdrmge_lmRawDiff2wgt_val13 Curve: sw_hdrmge_l_raw1_xx for each_raw MS diff of curve-L
19:10	RW	0x3fa	hw_hdrmge_msRawDiff2wgt_val13 Curve: sw_hdrmge_l_raw0_xx for each_raw MS diff of curve-L
9:0	RW	0x3ff	hw_hdrmge_luma2wgt_val13 E-curve over_exp_normal of Y-13

ISP_HDRMGE_3800_OVER_Y14

Address: Operational Base(0x21D03800) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x3fd	hw_hdrmge_lmRawDiff2wgt_val14 Curve: sw_hdrmge_l_raw1_xx for each_raw MS diff of curve-L
19:10	RW	0x3fd	hw_hdrmge_msRawDiff2wgt_val14 Curve: sw_hdrmge_l_raw0_xx for each_raw MS diff of curve-L
9:0	RW	0x3ff	hw_hdrmge_luma2wgt_val14 E-curve over_exp_normal of Y-14

ISP_HDRMGE_3800_OVER_Y15

Address: Operational Base(0x21D03800) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x3fe	hw_hdrmge_lmRawDiff2wgt_val15 Curve: sw_hdrmge_l_raw1_xx for each_raw MS diff of curve-L
19:10	RW	0x3fe	hw_hdrmge_msRawDiff2wgt_val15 Curve: sw_hdrmge_l_raw0_xx for each_raw MS diff of curve-L
9:0	RW	0x3ff	hw_hdrmge_luma2wgt_val15 E-curve over_exp_normal of Y-15

ISP_HDRMGE_3800_OVER_Y16

Address: Operational Base(0x21D03800) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x3ff	hw_hdrmge_lmRawDiff2wgt_val16 Curve: sw_hdrmge_l_raw1_xx for each_raw MS diff of curve-L
19:10	RW	0x3ff	hw_hdrmge_msRawDiff2wgt_val16 Curve: sw_hdrmge_l_raw0_xx for each_raw MS diff of curve-L
9:0	RW	0x3ff	hw_hdrmge_luma2wgt_val16 E-curve over_exp_normal of Y-16

ISP_HDRMGE_3800_EACH_GAIN

Address: Operational Base(0x21D03800) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
26:16	RW	0x100	hw_hdrmge_channelDetn_mediumGain Raw_gain1[5,6] for raw_each_diff1 = M*raw_gain1 - L, only for HDRx3
15:14	RO	0x0	reserved
13:0	RW	0x0400	hw_hdrmge_channelDetn_shortGain Raw_gain0[8,6] for raw_each_diff0 = S*raw_gain0 - M, for HDRx2 and HDRx3

ISP_HDRMGE_3800_FORCE_LONG0

Address: Operational Base(0x21D03800) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x040	sw_hdrmge_midluma_scale Middle-luma-scale=[6,6]

ISP_HDRMGE_3800_FORCE_LONG1

Address: Operational Base(0x21D03800) + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0xfff	sw_hdrmge_midlumathred_minlimit Middle-mid-luma-thred-minlimit=[0,12]
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_hdrmge_midlumathred_maxlimit Middle-mid-luma-thred-maxlimit=[0,12]

44.4.2.9 EXPANDER

ISP_EXPANDER_3100_EXPD_K15

Address: Operational Base(0x21D03100) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	sw_expd_k15 Slope config expd_k = k<<sw_expd_k_shift

ISP_EXPANDER_3100_EXPD_K16

Address: Operational Base(0x21D03100) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	sw_expd_k16 Slope config expd_k = k<<sw_expd_k_shift

ISP_EXPANDER_3100_EXPD_K17

Address: Operational Base(0x21D03100) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	sw_expd_k17 Slope config expd_k = k<<sw_expd_k_shift

ISP_EXPANDER_3100_EXPD_K18

Address: Operational Base(0x21D03100) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	sw_expd_k18 Slope config expd_k = k<<sw_expd_k_shift

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ISP_EXPANDER_3100_EXPD_K19

Address: Operational Base(0x21D03100) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	sw_expd_k19 Slope config expd_k = k<<sw_expd_k_shift

ISP_EXPANDER_3100_EXPD_K20

Address: Operational Base(0x21D03100) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	sw_expd_k20 Slope config expd_k = k<<sw_expd_k_shift

ISP_EXPANDER_3100_EXPD_K21

Address: Operational Base(0x21D03100) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	sw_expd_k21 Slope config expd_k = k<<sw_expd_k_shift

ISP_EXPANDER_3100_EXPD_K22

Address: Operational Base(0x21D03100) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	sw_expd_k22 Slope config expd_k = k<<sw_expd_k_shift

ISP_EXPANDER_3100_EXPD_K23

Address: Operational Base(0x21D03100) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	sw_expd_k23 Slope config expd_k = k<<sw_expd_k_shift

ISP_EXPANDER_3100_EXPD_K24

Address: Operational Base(0x21D03100) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	sw_expd_k24 Slope config expd_k = k<<sw_expd_k_shift

ISP_EXPANDER_3100_EXPD_K25

Address: Operational Base(0x21D03100) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	sw_expd_k25 Slope config expd_k = k<<sw_expd_k_shift

ISP_EXPANDER_3100_EXPD_K26

Address: Operational Base(0x21D03100) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	sw_expd_k26 Slope config expd_k = k<<sw_expd_k_shift

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ISP_EXPANDER_3100_EXPD_K27

Address: Operational Base(0x21D03100) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	sw_expd_k27 Slope config expd_k = k<<sw_expd_k_shift

ISP_EXPANDER_3100_EXPD_K28

Address: Operational Base(0x21D03100) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	sw_expd_k28 Slope config expd_k = k<<sw_expd_k_shift

ISP_EXPANDER_3100_EXPD_K29

Address: Operational Base(0x21D03100) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	sw_expd_k29 Slope config expd_k = k<<sw_expd_k_shift

ISP_EXPANDER_3100_EXPD_K30

Address: Operational Base(0x21D03100) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	sw_expd_k30 Slope config expd_k = k<<sw_expd_k_shift

ISP_EXPANDER_3100_EXPD_K31

Address: Operational Base(0x21D03100) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	sw_expd_k31 Slope config expd_k = k<<sw_expd_k_shift

ISP_EXPANDER_3100_EXPD_IMAX

Address: Operational Base(0x21D03100) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0xffff	sw_expd_imax Expd input maximum

ISP_EXPANDER_3100_EXPD_OMAX

Address: Operational Base(0x21D03100) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	sw_expd_omax Expd output maximum

ISP_EXPANDER_3100_EXPD_CTRL

Address: Operational Base(0x21D03100) + offset (0x0100)

Bit	Attr	Reset Value	Description
31	RO	0x0	isp_expd_working Working signal

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Bit	Attr	Reset Value	Description
30	RO	0x0	sw_expd_en_shd expd_en shd 1'b1: Enable 1'b0: Disable
29	RO	0x0	reserved
28	RW	0x0	sw_expd_mode_shd Expd input mode: 1'b0: 12bit input 1'b1: 16bit input
27:9	RO	0x00000	reserved
8	RW	0x0	sw_expd_mode Expd input mode: 1'b0: 12bit input 1'b1: 16bit input
7:4	RW	0xd	sw_expd_k_shift Slope amplification factor, k_cfg = slope*2^sw_expd_k_shift
3:1	RO	0x0	reserved
0	RW	0x0	sw_expd_en expd_en 1'b1: Enable 1'b0: Disable

ISP_EXPANDER_3100_EXPD_X00_01

Address: Operational Base(0x21D03100) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	RW	0x0200	sw_expd_x1 Coordinate x
15:0	RW	0x0000	sw_expd_x0 Coordinate x

ISP_EXPANDER_3100_EXPD_X02_03

Address: Operational Base(0x21D03100) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	RW	0x048c	sw_expd_x3 Coordinate x
15:0	RW	0x0346	sw_expd_x2 Coordinate x

ISP_EXPANDER_3100_EXPD_X04_05

Address: Operational Base(0x21D03100) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0718	sw_expd_x5 Coordinate x
15:0	RW	0x05d2	sw_expd_x4 Coordinate x

ISP_EXPANDER_3100_EXPD_X06_07

Address: Operational Base(0x21D03100) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	RW	0x09a4	sw_expd_x7 Coordinate x
15:0	RW	0x085e	sw_expd_x6 Coordinate x

ISP_EXPANDER_3100_EXPD_X08_09

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Address: Operational Base(0x21D03100) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:16	RW	0x0c30	sw_expd_x9 Coordinate x
15:0	RW	0x0aea	sw_expd_x8 Coordinate x

ISP_EXPANDER_3100_EXPD_X10_11

Address: Operational Base(0x21D03100) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:16	RW	0x0ebc	sw_expd_x11 Coordinate x
15:0	RW	0x0d76	sw_expd_x10 Coordinate x

ISP_EXPANDER_3100_EXPD_X12_13

Address: Operational Base(0x21D03100) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0fff	sw_expd_x13 Coordinate x
15:0	RW	0x0fff	sw_expd_x12 Coordinate x

ISP_EXPANDER_3100_EXPD_X14_15

Address: Operational Base(0x21D03100) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:16	RW	0x0fff	sw_expd_x15 Coordinate x
15:0	RW	0x0fff	sw_expd_x14 Coordinate x

ISP_EXPANDER_3100_EXPD_X16_17

Address: Operational Base(0x21D03100) + offset (0x0124)

Bit	Attr	Reset Value	Description
31:16	RW	0x0fff	sw_expd_x17 Coordinate x
15:0	RW	0x0fff	sw_expd_x16 Coordinate x

ISP_EXPANDER_3100_EXPD_X18_19

Address: Operational Base(0x21D03100) + offset (0x0128)

Bit	Attr	Reset Value	Description
31:16	RW	0x0fff	sw_expd_x19 Coordinate x
15:0	RW	0x0fff	sw_expd_x18 Coordinate x

ISP_EXPANDER_3100_EXPD_X20_21

Address: Operational Base(0x21D03100) + offset (0x012C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0fff	sw_expd_x21 Coordinate x
15:0	RW	0x0fff	sw_expd_x20 Coordinate x

ISP_EXPANDER_3100_EXPD_X22_23

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Address: Operational Base(0x21D03100) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:16	RW	0x0fff	sw_expd_x23 Coordinate x
15:0	RW	0x0fff	sw_expd_x22 Coordinate x

ISP_EXPANDER_3100_EXPD_X24_25

Address: Operational Base(0x21D03100) + offset (0x0134)

Bit	Attr	Reset Value	Description
31:16	RW	0x0fff	sw_expd_x25 Coordinate x
15:0	RW	0x0fff	sw_expd_x24 Coordinate x

ISP_EXPANDER_3100_EXPD_X26_27

Address: Operational Base(0x21D03100) + offset (0x0138)

Bit	Attr	Reset Value	Description
31:16	RW	0x0fff	sw_expd_x27 Coordinate x
15:0	RW	0x0fff	sw_expd_x26 Coordinate x

ISP_EXPANDER_3100_EXPD_X28_29

Address: Operational Base(0x21D03100) + offset (0x013C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0fff	sw_expd_x29 Coordinate x
15:0	RW	0x0fff	sw_expd_x28 Coordinate x

ISP_EXPANDER_3100_EXPD_X30_31

Address: Operational Base(0x21D03100) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:16	RW	0x0fff	sw_expd_x31 Coordinate x
15:0	RW	0x0fff	sw_expd_x30 Coordinate x

ISP_EXPANDER_3100_EXPD_Y0

Address: Operational Base(0x21D03100) + offset (0x0144)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_expd_y0 Coordinate y

ISP_EXPANDER_3100_EXPD_Y1

Address: Operational Base(0x21D03100) + offset (0x0148)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00200	sw_expd_y1 Coordinate y

ISP_EXPANDER_3100_EXPD_Y2

Address: Operational Base(0x21D03100) + offset (0x014C)

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Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00400	sw_expd_y2 Coordinate y

ISP_EXPANDER_3100_EXPD_Y3

Address: Operational Base(0x21D03100) + offset (0x0150)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00800	sw_expd_y3 Coordinate y

ISP_EXPANDER_3100_EXPD_Y4

Address: Operational Base(0x21D03100) + offset (0x0154)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x01000	sw_expd_y4 Coordinate y

ISP_EXPANDER_3100_EXPD_Y5

Address: Operational Base(0x21D03100) + offset (0x0158)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x02000	sw_expd_y5 Coordinate y

ISP_EXPANDER_3100_EXPD_Y6

Address: Operational Base(0x21D03100) + offset (0x015C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x04000	sw_expd_y6 Coordinate y

ISP_EXPANDER_3100_EXPD_Y7

Address: Operational Base(0x21D03100) + offset (0x0160)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x08000	sw_expd_y7 Coordinate y

ISP_EXPANDER_3100_EXPD_Y8

Address: Operational Base(0x21D03100) + offset (0x0164)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x10000	sw_expd_y8 Coordinate y

ISP_EXPANDER_3100_EXPD_Y9

Address: Operational Base(0x21D03100) + offset (0x0168)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x20000	sw_expd_y9 Coordinate y

ISP_EXPANDER_3100_EXPD_Y10

Address: Operational Base(0x21D03100) + offset (0x016C)

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Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x40000	sw_expd_y10 Coordinate y

ISP_EXPANDER_3100_EXPD_Y11

Address: Operational Base(0x21D03100) + offset (0x0170)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x80000	sw_expd_y11 Coordinate y

ISP_EXPANDER_3100_EXPD_Y12

Address: Operational Base(0x21D03100) + offset (0x0174)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	sw_expd_y12 Coordinate y

ISP_EXPANDER_3100_EXPD_Y13

Address: Operational Base(0x21D03100) + offset (0x0178)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	sw_expd_y13 Coordinate y

ISP_EXPANDER_3100_EXPD_Y14

Address: Operational Base(0x21D03100) + offset (0x017C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	sw_expd_y14 Coordinate y

ISP_EXPANDER_3100_EXPD_Y15

Address: Operational Base(0x21D03100) + offset (0x0180)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	sw_expd_y15 Coordinate y

ISP_EXPANDER_3100_EXPD_Y16

Address: Operational Base(0x21D03100) + offset (0x0184)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	sw_expd_y16 Coordinate y

ISP_EXPANDER_3100_EXPD_Y17

Address: Operational Base(0x21D03100) + offset (0x0188)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	sw_expd_y17 Coordinate y

ISP_EXPANDER_3100_EXPD_Y18

Address: Operational Base(0x21D03100) + offset (0x018C)

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Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	sw_expd_y18 Coordinate y

ISP_EXPANDER_3100_EXPD_Y19

Address: Operational Base(0x21D03100) + offset (0x0190)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	sw_expd_y19 Coordinate y

ISP_EXPANDER_3100_EXPD_Y20

Address: Operational Base(0x21D03100) + offset (0x0194)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	sw_expd_y20 Coordinate y

ISP_EXPANDER_3100_EXPD_Y21

Address: Operational Base(0x21D03100) + offset (0x0198)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	sw_expd_y21 Coordinate y

ISP_EXPANDER_3100_EXPD_Y22

Address: Operational Base(0x21D03100) + offset (0x019C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	sw_expd_y22 Coordinate y

ISP_EXPANDER_3100_EXPD_Y23

Address: Operational Base(0x21D03100) + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	sw_expd_y23 Coordinate y

ISP_EXPANDER_3100_EXPD_Y24

Address: Operational Base(0x21D03100) + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	sw_expd_y24 Coordinate y

ISP_EXPANDER_3100_EXPD_Y25

Address: Operational Base(0x21D03100) + offset (0x01A8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	sw_expd_y25 Coordinate y

ISP_EXPANDER_3100_EXPD_Y26

Address: Operational Base(0x21D03100) + offset (0x01AC)

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Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	sw_expd_y26 Coordinate y

ISP_EXPANDER_3100_EXPD_Y27

Address: Operational Base(0x21D03100) + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	sw_expd_y27 Coordinate y

ISP_EXPANDER_3100_EXPD_Y28

Address: Operational Base(0x21D03100) + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	sw_expd_y28 Coordinate y

ISP_EXPANDER_3100_EXPD_Y29

Address: Operational Base(0x21D03100) + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	sw_expd_y29 Coordinate y

ISP_EXPANDER_3100_EXPD_Y30

Address: Operational Base(0x21D03100) + offset (0x01BC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	sw_expd_y30 Coordinate y

ISP_EXPANDER_3100_EXPD_Y31

Address: Operational Base(0x21D03100) + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	sw_expd_y31 Coordinate y

ISP_EXPANDER_3100_EXPD_K0

Address: Operational Base(0x21D03100) + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x002000	sw_expd_k0 Slope config expd_k = k<<sw_expd_k_shift, k = (y1-y0)/(x1-x0)

ISP_EXPANDER_3100_EXPD_K1

Address: Operational Base(0x21D03100) + offset (0x01C8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x003241	sw_expd_k1 Slope config expd_k = k<<sw_expd_k_shift

ISP_EXPANDER_3100_EXPD_K2

Address: Operational Base(0x21D03100) + offset (0x01CC)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x006483	sw_expd_k2 Slope config expd_k = k<<sw_expd_k_shift

ISP_EXPANDER_3100_EXPD_K3

Address: Operational Base(0x21D03100) + offset (0x01D0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x00c907	sw_expd_k3 Slope config expd_k = k<<sw_expd_k_shift

ISP_EXPANDER_3100_EXPD_K4

Address: Operational Base(0x21D03100) + offset (0x01D4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x01920f	sw_expd_k4 Slope config expd_k = k<<sw_expd_k_shift

ISP_EXPANDER_3100_EXPD_K5

Address: Operational Base(0x21D03100) + offset (0x01D8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x03241f	sw_expd_k5 Slope config expd_k = k<<sw_expd_k_shift

ISP_EXPANDER_3100_EXPD_K6

Address: Operational Base(0x21D03100) + offset (0x01DC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x06483e	sw_expd_k6 Slope config expd_k = k<<sw_expd_k_shift

ISP_EXPANDER_3100_EXPD_K7

Address: Operational Base(0x21D03100) + offset (0x01E0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x0c907d	sw_expd_k7 Slope config expd_k = k<<sw_expd_k_shift

ISP_EXPANDER_3100_EXPD_K8

Address: Operational Base(0x21D03100) + offset (0x01E4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x1920fb	sw_expd_k8 Slope config expd_k = k<<sw_expd_k_shift

ISP_EXPANDER_3100_EXPD_K9

Address: Operational Base(0x21D03100) + offset (0x01E8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x3241f6	sw_expd_k9 Slope config expd_k = k<<sw_expd_k_shift

ISP_EXPANDER_3100_EXPD_K10

Address: Operational Base(0x21D03100) + offset (0x01EC)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x6483ed	sw_expd_k10 Slope config expd_k = k<<sw_expd_k_shift

ISP_EXPANDER_3100_EXPD_K11

Address: Operational Base(0x21D03100) + offset (0x01F0)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0xcae5bf	sw_expd_k11 Slope config expd_k = k<<sw_expd_k_shift

ISP_EXPANDER_3100_EXPD_K12

Address: Operational Base(0x21D03100) + offset (0x01F4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	sw_expd_k12 Slope config expd_k = k<<sw_expd_k_shift

ISP_EXPANDER_3100_EXPD_K13

Address: Operational Base(0x21D03100) + offset (0x01F8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	sw_expd_k13 Slope config expd_k = k<<sw_expd_k_shift

ISP_EXPANDER_3100_EXPD_K14

Address: Operational Base(0x21D03100) + offset (0x01FC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	sw_expd_k14 Slope config expd_k = k<<sw_expd_k_shift

44.4.2.10 BAY3D

BAY3D_2B00_BAY3D_CTRL0

Address: Operational Base(0x21D02B00) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	sys_itself_force_upd_bay3d_working Sys_itself_force_upd, write only BTNR working, read only
30	RO	0x0	reserved
29:28	RW	0x0	sw_bay3d_iir_rw_fmt_shd Pre frame data format read or write DDR (shadow)
27:25	RO	0x0	reserved
24	RO	0x0	hw_btnr_motionEst_en_shd BTNR motion estimate enable (shadow) 1'b1: Enable 1'b0: Disable
23:19	RO	0x00	reserved
18	RO	0x0	sw_bay3d_bypass_en_shd BTNR data path bypass enable (shadow) 1'b1: Enable 1'b0: Disable
17	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
16	RO	0x0	sw_bay3d_en_shd BTNR enable (shadow) 1'b1: Enable 1'b0: Disable
15	RO	0x0	reserved
14:13	RW	0x0	sw_bay3d_iir_rw_fmt Pre frame data format read or write DDR 2'd0: 12bit compact format 2'd1: 16bit sparse format 2'd2: 16bit high precesion format 2'd3: 16bit high precesion format, iir ldc Data format reference application notes
12	RW	0x0	sw_bay3d_clk_on Clock always on
11:9	RO	0x0	reserved
8	RW	0x0	hw_btnr_motionEst_en BTNR motion estimate enable 1'b1: Enable 1'b0: Disable
7:5	RW	0x0	hw_btnr_outUsePre_mode BTNR image details and noise balance mode. 3'b001: iir spnr based motion denoise mode, one frame delay,mid noise balance enable,cur iteration enable 3'b010: iir spnr based motion denoise mode, one frame delay,mid noise balance enable,cur iteration disable 3'b011: iir spnr based motion denoise mode, one frame delay,mid noise balance disable,cur iteration enable 3'b100: iir spnr based motion denoise mode, one frame delay,mid noise balance disable,cur iteration disable 3'b101: iir spnr based motion denoise mode, no frame delay,mid noise balance enable,cur iteration disable 3'b110: iir spnr based motion denoise mode, no frame delay,mid noise balance disable,cur iteration disable 3'b000: cur spnr based motion denoise mode, no frame delay,mid noise balance disable,cur iteration enable, not recommended 3'b111: reserved
4	RW	0x0	sw_bay3d_afifo_clr_en BTNR afifo clear when frame start enable 1'b1: Enable 1'b0: Disable
3	RW	0x0	bayertnr_soft_mode_mode IIR write ddr data mode 1'b1: Write iir_ddr_data to DDR, aiisp data path 1'b0: Write iir_out_data to DDR, normal data path Data path reference to application notes
2	RO	0x0	reserved
1	RW	0x0	hw_btnr_tnrModule_bypass_en BTNR data path bypass enable 1'b1: Enable 1'b0: Disable When this bit is enabled, the BTNR module is still working, and the output data is consistent with the input data
0	RW	0x0	hw_btnr_tnrModule_en BTNR module enable 1'b1: Enable 1'b0: Disable

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BAY3D_2B00_BAY3D_CTRL1

Address: Operational Base(0x21D02B00) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25	RW	0x0	hw_btnr_mdWgtOut_en Output mdWgt data for debug 1'b1: Enable 1'b0: Disable
24:23	RO	0x0	reserved
22	RW	0x0	hw_btnr_curSpnrOut_en Output cur spnr data for debug 1'b1: Enable 1'b0: Disable
21	RW	0x0	hw_btnr_mdOnlyLo_en Output loMgeWgt data for debug 1'b1: Enable 1'b0: Disable
20	RW	0x0	hw_btnr_preSpnrOut_en Output cur spnr data for debug 1'b1: Enable 1'b0: Disable
19:18	RO	0x0	reserved
17:16	RW	0x0	hw_btnr_LoMgeWgt_mode Low motion detect weight merge source select 2'b00: min of loDiff, loWgt and largeloWgt 2'b01: loDiff 2'b10: loWgt 2'b11: largeloWgt
15	RW	0x0	hw_btnr_LoDetection_bypass_en Lo motion detect bypass enable. 1'b1: Enable 1'b0: Disable
14	RO	0x0	reserved
13	RW	0x1	hw_btnr_SigHfilt_en loDiffMd sigma channel hfilt enable 1'b1: Enable 1'b0: Disable
12	RW	0x1	hw_btnr_LoDiffHfilt_en loDiffMd diff channel hfilt enable 1'b1: Enable 1'b0: Disable
11	RW	0x1	hw_btnr_LoWgtHfilt_en loWgtMd hfilt enable 1'b1: Enable 1'b0: Disable
10	RW	0x0	hw_btnr_LpfLo_bypass_en Motion detect lo freq Gauss filter bypass enable. 1'b1: Enable 1'b0: Disable
9	RW	0x0	hw_btnr_LoDiffVfilt_bypass_en Motion detect lo freq vert filter bypass enable. 1'b1: Enable 1'b0: Disable

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Bit	Attr	Reset Value	Description
8	RW	0x0	hw_btnr_LpfHi_bypass_en Motion detect hi freq Gauss filter bypass enable. 1'b1: Enable 1'b0: Disable
7	RW	0x0	hw_btnr_MotionDetect_bypass_en Motion Detect bypass enable 1'b1: Enable 1'b0: Disable
6	RW	0x0	hw_btnr_prePixOut_mode Data selected to be written to ddr. 1'b1: softthresh result 1'b0: no softthresh result
5	RW	0x0	hw_btnr_mdLargeLoMdWgt_bypass_en Large low motion detect use for next frame motion detect bypass enable. 1'b1: Enable 1'b0: Disable
4	RW	0x0	hw_btnr_mdLargeLoGaussFilter_bypass_en Large low motion detect weight gauss filter bypass enable. 1'b1: Enable 1'b0: Disable
3	RW	0x0	hw_btnr_mdLargeLoMinFilter_bypass_en Large low motion detect weight min filter bypass enable. 1'b1: Enable 1'b0: Disable
2	RW	0x0	hw_btnr_mdLargeLoUse_mode Large low motion detect source select 1'b0: loWgt 1'b1: loDiff
1	RW	0x0	hw_btnr_tnrsigmaCurveDouble_en TNR sigma curve split enable. 1'b1: Set tnrLuma2sigma_val0~9, tnrLuma2sigma_val10~19 as two curve, used in hdr mode 1'b0: Set tnrLuma2sigma_val0~19 as one curve, used in linear mode
0	RW	0x0	hw_btnr_transf_bypass_en BTNR data transform bypass enable 1'b1: Enable 1'b0: Disable

BAY3D_2B00_BAY3D_CTRL2

Address: Operational Base(0x21D02B00) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26	RW	0x0	hw_btnr_preSpnrDpcFlt_prewgt_en Pre spnr dpc filter use pre wgt enable 1'b0: disable 1'b1: enable
25	RW	0x0	hw_btnr_preSpnrDpcFlt_mode Pre spnr dpc filter mode
24	RW	0x0	hw_btnr_preSpnrDpcNrBal_mode Pre spnr dpc filter noise balance mode

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Bit	Attr	Reset Value	Description
23	RW	0x0	hw_btnr_preSpnrDpcFlt_en Pre spnr dpc filter enable 1'b0: disable 1'b1: enable
22	RW	0x0	sw_prelo_avg_lp_en Pre spnr low freq channel averge low power mode enable 1'b1: Enable 1'b0: Disable When this bit is enabled, the spnr module works in low power mode
21	RW	0x0	sw_prehi_bf_lp_en Pre spnr high freq bilafilter low power mode enable 1'b1: Enable 1'b0: Disable When this bit is enabled, the spnr module works in low power mode
20	RW	0x0	sw_prehi_gic_lp_en Pre spnr high freq green imblance correction low power mode enable 1'b1: Enable 1'b0: Disable When this bit is enabled, the spnr module works in low power mode
19:16	RO	0x0	reserved
15	RW	0x0	hw_btnr_preSpnrLoFilterRbWgt_mode Pre spnr lo freq filter RB weight calc mode. 1'b1: rb channel separate wgt 1'b0: rb channel share wgt
14	RW	0x0	hw_btnr_preSpnrHiFilterRbWgt_mode Pre spnr hi freq filter RB weight calc mode. 1'b1: rb channel separate wgt 1'b0: rb channel share wgt
13	RW	0x0	hw_btnr_preSpnrLoFilterWgt_mode Pre spnr lo freq filter weight calc mode. 1'b1: 4 channel separate wgt 1'b0: 4 channel share wgt
12	RW	0x0	hw_btnr_preSpnrHiFilterWgt_mode Pre spnr hi freq filter weight calc mode. 1'b1: 4 channel separate wgt 1'b0: 4 channel share wgt
11	RW	0x0	hw_btnr_preSpnrHiNoiseCtrl_en Pre spnr hi freq wgt calc merge guide pixel and original pixel by kalman data enable. 1'b1: Enable 1'b0: Disable
10	RW	0x0	hw_btnr_preSpnrSigmaIdxFilt_mode Pre spnr sigma curve index pixel lowpass filter coeff select. 1'b1: Less average coeff 1'b0: More average coeff
9	RW	0x0	hw_btnr_preSpnrSigmaIdxFilt_bypass_en Pre spnr sigma curve index pixel lowpass filter bypass enable. 1'b1: Enable 1'b0: Disable

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Bit	Attr	Reset Value	Description
8	RW	0x0	hw_btnr_preSpnrHiGuideFilter_bypass_en Pre spnr hi freq guide filter bypass enable. 1'b1: Enable 1'b0: Disable
7	RW	0x0	hw_btnr_preSpnrsigmaCurveDouble_en Pre SPNR sigma curve split enable. 1'b1: Set spnrLuma2sigma_val0~7, spnrLuma2sigma_val8~15 as two curve, used in hdr mode 1'b0: Set spnrLuma2sigma_val0~15 as one curve, used in linear mode
6	RW	0x0	hw_btnr_preSpnrHiFilter_bypass_en Pre spnr hi freq filter bypass enable. 1'b1: Enable 1'b0: Disable
5	RW	0x0	hw_btnr_preSpnrLoFilter_bypass_en Pre spnr lo freq filter bypass enable. 1'b1: Enable 1'b0: Disable
4	RW	0x0	hw_btnr_spnrPresigmaUse_en Pre spnr use pre sigma enable. 1'b1: Enable 1'b0: Disable
3	RW	0x0	hw_btnr_preSpnrHiFilterGicEnhance_en Pre spnr hi freq filter's grgb correct enhance enable. 1'b1: Enable 1'b0: Disable
2	RW	0x0	hw_btnr_preSpnrHiFilterGic_en Pre hi freq filter's grgb correct enable. 1'b1: Enable 1'b0: Disable
1	RO	0x0	reserved
0	RW	0x0	hw_btnr_curSpnrFilter_bypass_en Cur spnr bypass enable. 1'b1: Enable 1'b0: Disable

BAY3D_2B00_BAY3D_CTRL3

Address: Operational Base(0x21D02B00) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x3f	hw_btnr_sigmaCalcMgeWgtHdrSht_thred Short exposure hdr megre weight threshold for sigma calc, U0.6
23:22	RO	0x0	reserved
21:16	RW	0x3f	hw_btnr_mgeWgtHdrSht_thred Hdr megre weight threshold for short exposure, U0.6
15:5	RO	0x000	reserved
4:3	RW	0x0	hw_btnr_kalmanWgtDs_mode Kalman weight downsacle mode 2'b00: Avergae 2'b01: Max 2'b10: Min 2'b11: Reserved

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Bit	Attr	Reset Value	Description
2	RW	0x0	hw_btnr_mgeWgtDs_mode Hdr megre weight downscale mode 1'b0: Average 1'b1: Max
1	RW	0x1	hw_btnr_WgtCal_mode Weight calc mode 1'b1: Mode 1, wgt calc by sigma curve 1'b0: Mode 0, adaptive wgt calc
0	RW	0x0	hw_btnr_transf_mode BTNR data transform curve mode 1'b0: Log curve 1'b1: Sqrt curve

BAY3D_2B00_BAY3D_TRANS0

Address: Operational Base(0x21D02B00) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0800	hw_btnr_itransfMode_offset Offset used for Inverse transformation
15:14	RW	0x0	hw_btnr_transfMode_scale Scale used for transformation
13	RO	0x0	reserved
12:0	RW	0x0100	hw_btnr_transfMode_offset Offset used for transformation

BAY3D_2B00_BAY3D_TRANS1

Address: Operational Base(0x21D02B00) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0xfffff	hw_btnr_transfData_maxLimit The maximum value limit for the transformation

BAY3D_2B00_BAY3D_PRE_SIGSCL

Address: Operational Base(0x21D02B00) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	hw_btnr_preSpnrSigmaCtrl_scale Pre sigma scale

BAY3D_2B00_BAY3D_PREHI_SIGOF

Address: Operational Base(0x21D02B00) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:7	RO	0x0000000	reserved
6:0	RW	0x00	hw_btnr_preSpnrHiGuideOut_wgt Pre spnr 5x5 and 3x3 guide filter mix weight, U0.6

BAY3D_2B00_BAY3D_CURHISPW0

Address: Operational Base(0x21D02B00) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x00	hw_btnr_curSpnrFilter_coeff2 Cur spnr filter coeff 2, U0.8 , sum of all coeff must be 256
15:14	RO	0x0	reserved
13:8	RW	0x00	hw_btnr_curSpnrFilter_coeff1 Cur spnr filter coeff 1, U0.8 , sum of all coeff must be 256

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	hw_btnr_curSpnrFilter_coeff0 Cur spnr filter coeff 0, U0.8 , sum of all coeff must be 256

BAY3D_2B00_BAY3D_CURHISPW1

Address: Operational Base(0x21D02B00) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x00	hw_btnr_curSpnrFilter_coeff5 Cur spnr filter coeff 5, U0.8 , sum of all coeff must be 256
15:14	RO	0x0	reserved
13:8	RW	0x00	hw_btnr_curSpnrFilter_coeff4 Cur spnr filter coeff 4, U0.8 , sum of all coeff must be 256
7:6	RO	0x0	reserved
5:0	RW	0x00	hw_btnr_curSpnrFilter_coeff3 Cur spnr filter coeff 3, U0.8 , sum of all coeff must be 256

BAY3D_2B00_BAY3D_IIRSX0

Address: Operational Base(0x21D02B00) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_preSpnrLuma2sigma_idx1 Pre spnr sigma curve lut index 1, U0.12
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_btnr_preSpnrLuma2sigma_idx0 Pre spnr sigma curve lut index 0, U0.12

BAY3D_2B00_BAY3D_IIRSX2

Address: Operational Base(0x21D02B00) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_preSpnrLuma2sigma_idx3 Pre spnr sigma index 3
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_btnr_preSpnrLuma2sigma_idx2 Pre spnr sigma index 2

BAY3D_2B00_BAY3D_IIRSX4

Address: Operational Base(0x21D02B00) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_preSpnrLuma2sigma_idx5 Pre spnr sigma index 5
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_btnr_preSpnrLuma2sigma_idx4 Pre spnr sigma index 4

BAY3D_2B00_BAY3D_IIRSX6

Address: Operational Base(0x21D02B00) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_preSpnrLuma2sigma_idx7 Pre spnr sigma index 7
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x000	hw_btnr_preSpnrLuma2sigma_idx6 Pre spnr sigma index 6

BAY3D_2B00_BAY3D_IIRSX8

Address: Operational Base(0x21D02B00) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_preSpnrLuma2sigma_idx9 Pre spnr sigma index 9
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_btnr_preSpnrLuma2sigma_idx8 Pre spnr sigma index 8

BAY3D_2B00_BAY3D_IIRSXA

Address: Operational Base(0x21D02B00) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_preSpnrLuma2sigma_idx11 Pre spnr sigma index 11
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_btnr_preSpnrLuma2sigma_idx10 Pre spnr sigma index 10

BAY3D_2B00_BAY3D_IIRSXC

Address: Operational Base(0x21D02B00) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_preSpnrLuma2sigma_idx13 Pre spnr sigma index 13
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_btnr_preSpnrLuma2sigma_idx12 Pre spnr sigma index 12

BAY3D_2B00_BAY3D_IIRSXE

Address: Operational Base(0x21D02B00) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_preSpnrLuma2sigma_idx15 Pre spnr sigma index 15
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_btnr_preSpnrLuma2sigma_idx14 Pre spnr sigma index 14

BAY3D_2B00_BAY3D_IIRSY0

Address: Operational Base(0x21D02B00) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_preSpnrLuma2sigma_val1 Pre spnr sigma curve lut value 1, U0.12
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_btnr_preSpnrLuma2sigma_val0 Pre spnr sigma curve lut value 0, U0.12

BAY3D_2B00_BAY3D_IIRSY2

Address: Operational Base(0x21D02B00) + offset (0x00A8)

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Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_preSpnrLuma2sigma_val3 Pre spnr sigma value 3
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_btnr_preSpnrLuma2sigma_val2 Pre spnr sigma value 2

BAY3D_2B00_BAY3D_IIRSY4

Address: Operational Base(0x21D02B00) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_preSpnrLuma2sigma_val5 Pre spnr sigma value 5
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_btnr_preSpnrLuma2sigma_val4 Pre spnr sigma value 4

BAY3D_2B00_BAY3D_IIRSY6

Address: Operational Base(0x21D02B00) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_preSpnrLuma2sigma_val7 Pre spnr sigma value 7
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_btnr_preSpnrLuma2sigma_val6 Pre spnr sigma value 6

BAY3D_2B00_BAY3D_IIRSY8

Address: Operational Base(0x21D02B00) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_preSpnrLuma2sigma_val9 Pre spnr sigma value 9
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_btnr_preSpnrLuma2sigma_val8 Pre spnr sigma value 8

BAY3D_2B00_BAY3D_IIRSYA

Address: Operational Base(0x21D02B00) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_preSpnrLuma2sigma_val11 Pre spnr sigma value 11
15:0	RW	0x0000	hw_btnr_preSpnrLuma2sigma_val10 Pre spnr sigma value 10

BAY3D_2B00_BAY3D_IIRSYC

Address: Operational Base(0x21D02B00) + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_preSpnrLuma2sigma_val13 Pre spnr sigma value 13
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x000	hw_btnr_preSpnrLuma2sigma_val12 Pre spnr sigma value 12

BAY3D_2B00_BAY3D_IIRSYE

Address: Operational Base(0x21D02B00) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_preSpnrLuma2sigma_val15 Pre spnr sigma value 15
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_btnr_preSpnrLuma2sigma_val14 Pre spnr sigma value 14

BAY3D_2B00_BAY3D_PREHI_SIGSCL

Address: Operational Base(0x21D02B00) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	hw_btnr_preSpnrHiSigma_scale Pre spnr hi freq sigma scale, U4.8

BAY3D_2B00_BAY3D_PREHI_WSCL

Address: Operational Base(0x21D02B00) + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	hw_btnr_preSpnrHiWgtCalc_scale Pre spnr hi freq filter range weight scale, U2.6

BAY3D_2B00_BAY3D_PREHIWMM

Address: Operational Base(0x21D02B00) + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	hw_btnr_preSpnrHIWgtCalc_offset Pre spnr hi freq filter range weight offset.U8
15:8	RO	0x00	reserved
7:0	RW	0x00	hw_btnr_preSpnrHiFilterWgt_minLimit Pre spnr hi freq filter range weight calc minlimit.U0.8

BAY3D_2B00_BAY3D_PREHISIGOF

Address: Operational Base(0x21D02B00) + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	hw_btnr_preSpnrSigmaHdrSht_offset Pre spnr sigma offset for hdr short exposure frame, invalid in linear mode.U8.0
23:16	RW	0x00	hw_btnr_preSpnrSigma_offset Pre spnr sigma offset for hdr long exposure frame or linear mode. U8.0
15:8	RO	0x00	reserved
7:0	RW	0x00	hw_btnr_preSpnrHiFilterOut_wgt Pre spnr hi freq filter pixel and original pixel merge weight.U1.7

BAY3D_2B00_BAY3D_PREHISIGSCL

Address: Operational Base(0x21D02B00) + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:16	RW	0x0000	hw_btnr_preSpnrSigmaHdrSht_scale Pre spnr sigma scale for hdr short exposure frame, invalid in linear mode.U6.8
15:14	RO	0x0	reserved
13:0	RW	0x0000	hw_btnr_preSpnrSigma_scale Pre spnr sigma scale for hdr long exposure frame or linear mode. U6.8

BAY3D_2B00_BAY3D_PREHISPW0

Address: Operational Base(0x21D02B00) + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x00	hw_btnr_preSpnrHiFilter_coeff2 Pre spnr high filter coeff 2, U0.6
15:14	RO	0x0	reserved
13:8	RW	0x00	hw_btnr_preSpnrHiFilter_coeff1 Pre spnr high filter coeff 1, U0.6
7:6	RO	0x0	reserved
5:0	RW	0x00	hw_btnr_preSpnrHiFilter_coeff0 Pre spnr high filter coeff 0, U0.6

BAY3D_2B00_BAY3D_PREHISPW1

Address: Operational Base(0x21D02B00) + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x00	hw_btnr_preSpnrHiFilter_coeff5 Pre spnr high filter coeff 5, U0.6
15:14	RO	0x0	reserved
13:8	RW	0x00	hw_btnr_preSpnrHiFilter_coeff4 Pre spnr high filter coeff 4, U0.6
7:6	RO	0x0	reserved
5:0	RW	0x00	hw_btnr_preSpnrHiFilter_coeff3 Pre spnr high filter coeff 3, U0.6

BAY3D_2B00_BAY3D_PRELOSIGCSL

Address: Operational Base(0x21D02B00) + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	hw_btnr_preSpnrLoSigma_scale Pre spnr lo freq filter sigma scale. U4.8

BAY3D_2B00_BAY3D_PRELOSIGOF

Address: Operational Base(0x21D02B00) + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	hw_btnr_preSpnrLoWgtCalc_scale Pre spnr lo freq filter range weight scale.U2.6
15:8	RO	0x00	reserved
7:0	RW	0x00	hw_btnr_preSpnrLoWgtCalc_offset Pre spnr lo freq filter range weight offset.U8

BAY3D_2B00_BAY3D_PREHI_NRCT

Address: Operational Base(0x21D02B00) + offset (0x00F0)

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Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:16	RW	0x00	hw_btnr_preSpnrHiNoiseCtrl_offset Offset of pre spnr hi freq guide pixel and original pixel merge weight. U0.7
15:10	RO	0x00	reserved
9:0	RW	0x000	hw_btnr_preSpnrHiNoiseCtrl_scale Scale of pre spnr hi freq guide pixel and original pixel merge weight.U3.7

BAY3D_2B00_BAY3D_TNRSX0

Address: Operational Base(0x21D02B00) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_tnrLuma2sigma_idx1 Tnr sigma curve lut index 1, U0.12
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_btnr_tnrLuma2sigma_idx0 Tnr sigma curve lut index 0, U0.12

BAY3D_2B00_BAY3D_TNRSX2

Address: Operational Base(0x21D02B00) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_tnrLuma2sigma_idx3 Tnr sigma index 3
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_btnr_tnrLuma2sigma_idx2 Tnr sigma index 2

BAY3D_2B00_BAY3D_TNRSX4

Address: Operational Base(0x21D02B00) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_tnrLuma2sigma_idx5 Tnr sigma index 5
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_btnr_tnrLuma2sigma_idx4 Tnr sigma index 4

BAY3D_2B00_BAY3D_TNRSX6

Address: Operational Base(0x21D02B00) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_tnrLuma2sigma_idx7 Tnr sigma index 7
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_btnr_tnrLuma2sigma_idx6 Tnr sigma index 6

BAY3D_2B00_BAY3D_TNRSX8

Address: Operational Base(0x21D02B00) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:16	RW	0x000	hw_btnr_tnrLuma2sigma_idx9 Tnr sigma index 9
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_btnr_tnrLuma2sigma_idx8 Tnr sigma index 8

BAY3D_2B00_BAY3D_TNRSXA

Address: Operational Base(0x21D02B00) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_tnrLuma2sigma_idx11 Tnr sigma index 11
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_btnr_tnrLuma2sigma_idx10 Tnr sigma index 10

BAY3D_2B00_BAY3D_TNRSXC

Address: Operational Base(0x21D02B00) + offset (0x0118)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_tnrLuma2sigma_idx13 Tnr sigma index 13
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_btnr_tnrLuma2sigma_idx12 Tnr sigma index 12

BAY3D_2B00_BAY3D_TNRSXE

Address: Operational Base(0x21D02B00) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_tnrLuma2sigma_idx15 Tnr sigma index 15
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_btnr_tnrLuma2sigma_idx14 Tnr sigma index 14

BAY3D_2B00_BAY3D_TNRSX10

Address: Operational Base(0x21D02B00) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_tnrLuma2sigma_idx17 Tnr sigma index 17
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_btnr_tnrLuma2sigma_idx16 Tnr sigma index 16

BAY3D_2B00_BAY3D_TNRSX12

Address: Operational Base(0x21D02B00) + offset (0x0124)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_tnrLuma2sigma_idx19 Tnr sigma index 19
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x000	hw_btnr_tnrLuma2sigma_idx18 Tnr sigma index 18

BAY3D_2B00_BAY3D_TNRSY0

Address: Operational Base(0x21D02B00) + offset (0x0128)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_tnrLuma2sigma_val1 Tnr sigma curve lut value 1, U0.12
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_btnr_tnrLuma2sigma_val0 Tnr sigma curve lut value 0, U0.12

BAY3D_2B00_BAY3D_TNRSY2

Address: Operational Base(0x21D02B00) + offset (0x012C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_tnrLuma2sigma_val3 Tnr sigma value 3
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_btnr_tnrLuma2sigma_val2 Tnr sigma value 2

BAY3D_2B00_BAY3D_TNRSY4

Address: Operational Base(0x21D02B00) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_tnrLuma2sigma_val5 Tnr sigma value 5
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_btnr_tnrLuma2sigma_val4 Tnr sigma value 4

BAY3D_2B00_BAY3D_TNRSY6

Address: Operational Base(0x21D02B00) + offset (0x0134)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_tnrLuma2sigma_val7 Tnr sigma value 7
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_btnr_tnrLuma2sigma_val6 Tnr sigma value 6

BAY3D_2B00_BAY3D_TNRSY8

Address: Operational Base(0x21D02B00) + offset (0x0138)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_tnrLuma2sigma_val9 Tnr sigma value 9
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_btnr_tnrLuma2sigma_val8 Tnr sigma value 8

BAY3D_2B00_BAY3D_TNRSYA

Address: Operational Base(0x21D02B00) + offset (0x013C)

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Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_tnrLuma2sigma_val11 Tnr sigma value 11
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_btnr_tnrLuma2sigma_val10 Tnr sigma value 10

BAY3D_2B00_BAY3D_TNRSYC

Address: Operational Base(0x21D02B00) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_tnrLuma2sigma_val13 Tnr sigma value 13
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_btnr_tnrLuma2sigma_val12 Tnr sigma value 12

BAY3D_2B00_BAY3D_TNRSYE

Address: Operational Base(0x21D02B00) + offset (0x0144)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_tnrLuma2sigma_val15 Tnr sigma value 15
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_btnr_tnrLuma2sigma_val14 Tnr sigma value 14

BAY3D_2B00_BAY3D_TNRSY10

Address: Operational Base(0x21D02B00) + offset (0x0148)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_tnrLuma2sigma_val17 Tnr sigma value 17
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_btnr_tnrLuma2sigma_val16 Tnr sigma value 16

BAY3D_2B00_BAY3D_TNRSY12

Address: Operational Base(0x21D02B00) + offset (0x014C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_tnrLuma2sigma_val19 Tnr sigma value 19
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_btnr_tnrLuma2sigma_val18 Tnr sigma value 18

BAY3D_2B00_BAY3D_HIWD0

Address: Operational Base(0x21D02B00) + offset (0x0150)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	hw_btnr_LpfHi_coeff2 Hi freq diff gauss filter coeff2 of motion detect ,U0.10, sum of all coeff must be 1024

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Bit	Attr	Reset Value	Description
19:10	RW	0x000	hw_btnr_LpfHi_coeff1 Hi freq diff gauss filter coeff1 of motion detect ,U0.10, sum of all coeff must be 1024
9:0	RW	0x000	hw_btnr_LpfHi_coeff0 Hi freq diff gauss filter coeff0 of motion detect ,U0.10, sum of all coeff must be 1024

BAY3D_2B00_BAY3D_HIWD3

Address: Operational Base(0x21D02B00) + offset (0x0154)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	hw_btnr_LpfHi_coeff5 Hi freq diff gauss filter coeff5 of motion detect ,U0.10, sum of all coeff must be 1024
19:10	RW	0x000	hw_btnr_LpfHi_coeff4 Hi freq diff gauss filter coeff4 of motion detect ,U0.10, sum of all coeff must be 1024
9:0	RW	0x000	hw_btnr_LpfHi_coeff3 Hi freq diff gauss filter coeff3 of motion detect ,U0.10, sum of all coeff must be 1024

BAY3D_2B00_BAY3D_HIWD6

Address: Operational Base(0x21D02B00) + offset (0x0158)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	hw_btnr_LpfHi_coeff8 Hi freq diff gauss filter coeff8 of motion detect ,U0.10, sum of all coeff must be 1024
19:10	RW	0x000	hw_btnr_LpfHi_coeff7 Hi freq diff gauss filter coeff7 of motion detect ,U0.10, sum of all coeff must be 1024
9:0	RW	0x000	hw_btnr_LpfHi_coeff6 Hi freq diff gauss filter coeff6 of motion detect ,U0.10, sum of all coeff must be 1024

BAY3D_2B00_BAY3D_LOWD0

Address: Operational Base(0x21D02B00) + offset (0x015C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	hw_btnr_LpfLo_coeff2 Lo freq diff gauss filter coeff2 of motion detect ,U0.10, sum of all coeff must be 1024
19:10	RW	0x000	hw_btnr_LpfLo_coeff1 Lo freq diff gauss filter coeff1 of motion detect ,U0.10, sum of all coeff must be 1024
9:0	RW	0x000	hw_btnr_LpfLo_coeff0 Lo freq diff gauss filter coeff0 of motion detect ,U0.10, sum of all coeff must be 1024

BAY3D_2B00_BAY3D_LOWD3

Address: Operational Base(0x21D02B00) + offset (0x0160)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:20	RW	0x000	hw_btnr_LpfLo_coeff5 Lo freq diff gauss filter coeff5 of motion detect ,U0.10, sum of all coeff must be 1024
19:10	RW	0x000	hw_btnr_LpfLo_coeff4 Lo freq diff gauss filter coeff4 of motion detect ,U0.10, sum of all coeff must be 1024
9:0	RW	0x000	hw_btnr_LpfLo_coeff3 Lo freq diff gauss filter coeff3 of motion detect ,U0.10, sum of all coeff must be 1024

BAY3D_2B00_BAY3D_LOWD6

Address: Operational Base(0x21D02B00) + offset (0x0164)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	hw_btnr_LpfLo_coeff8 Lo freq diff gauss filter coeff8 of motion detect ,U0.10, sum of all coeff must be 1024
19:10	RW	0x000	hw_btnr_LpfLo_coeff7 Lo freq diff gauss filter coeff7 of motion detect ,U0.10, sum of all coeff must be 1024
9:0	RW	0x000	hw_btnr_LpfLo_coeff6 Lo freq diff gauss filter coeff6 of motion detect ,U0.10, sum of all coeff must be 1024

BAY3D_2B00_BAY3D_GF3

Address: Operational Base(0x21D02B00) + offset (0x0168)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	hw_btnr_SigmaIdxFilt_coeff3 TNR sigma curve index pixel lowpass filter coeff3,U0.8, sum of all coeff must be 256
23:16	RW	0x00	hw_btnr_SigmaIdxFilt_coeff2 TNR sigma curve index pixel lowpass filter coeff2,U0.8, sum of all coeff must be 256
15:8	RW	0x00	hw_btnr_SigmaIdxFilt_coeff1 TNR sigma curve index pixel lowpass filter coeff1,U0.8, sum of all coeff must be 256
7:0	RW	0x00	hw_btnr_SigmaIdxFilt_coeff0 TNR sigma curve index pixel lowpass filter coeff0,U0.8, sum of all coeff must be 256

BAY3D_2B00_BAY3D_GF4

Address: Operational Base(0x21D02B00) + offset (0x016C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_LoWgtCalFirstLineSigma_scale Scale of loWgtMD sigma vertical IIR filter's first line coeff.U6.8
15:8	RW	0x00	hw_btnr_SigmaIdxFilt_coeff5 TNR sigma curve index pixel lowpass filter coeff5,U0.8, sum of all coeff must be 256
7:0	RW	0x00	hw_btnr_SigmaIdxFilt_coeff4 TNR sigma curve index pixel lowpass filter coeff4,U0.8, sum of all coeff must be 256

BAY3D_2B00_BAY3D_VIIR

Address: Operational Base(0x21D02B00) + offset (0x0170)

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Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:22	RW	0x00	hw_btnr_LoDiffFirstLine_scale Scale of diff channel of loDiffMd vertical IIR filter's first line coeff.U2.4
21:16	RW	0x00	hw_btnr_SigFirstLine_scale Scale of sigma channel of loDiffMd vertical IIR filter's first line coeff.U2.4
15:10	RO	0x00	reserved
9:5	RW	0x00	hw_btnr_LoWgtVfilt_wgt loWgtMd channel max limit of vertical IIR filter coeff.U1.4,[0,16]
4:0	RW	0x00	hw_btnr_LoDiffVfilt_wgt loWgtMd channel max limit of vertical IIR filter coeff.U1.4,[0,16]

BAY3D_2B00_BAY3D_LFSCL

Address: Operational Base(0x21D02B00) + offset (0x0174)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	hw_btnr_LoWgtCal_scale Scale of lo freq motion weight calc for loWgtMd channel.U4.10
15:14	RO	0x0	reserved
13:0	RW	0x0000	hw_btnr_LoWgtCal_offset Offset of lo freq motion weight calc for loWgtMd channel.U4.10

BAY3D_2B00_BAY3D_LFSCLTH

Address: Operational Base(0x21D02B00) + offset (0x0178)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	hw_btnr_Mode0Base_ratio Base ratio of motion detect mode 0, the higher the value is, the more likely it is to be judged as motion.U4.10
15:14	RO	0x0	reserved
13:0	RW	0x0000	hw_btnr_LoWgtCal_maxLimit Max limit of lo freq motion weight calc for loWgtMd channel.U4.10

BAY3D_2B00_BAY3D_DSWGTSCL

Address: Operational Base(0x21D02B00) + offset (0x017C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	hw_btnr_LoDiffWgtCal_scale Scale of lo freq motion weight calc for loDiffMd channel.U4.10
15:14	RO	0x0	reserved
13:0	RW	0x0000	hw_btnr_LoDiffWgtCal_offset Offset of lo freq motion weight calc for loDiffMd channel.U4.10

BAY3D_2B00_BAY3D_WGTLASTSCL

Address: Operational Base(0x21D02B00) + offset (0x0180)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	hw_btnr_LoMgePreWgt_scale Previous frame motion weight scale for lo motion detect.U4.10
15:14	RO	0x0	reserved
13:0	RW	0x0000	hw_btnr_LoMgePreWgt_offset Previous frame motion weight offset for lo motion detect.U4.10

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BAY3D_2B00_BAY3D_WGTSCL0

Address: Operational Base(0x21D02B00) + offset (0x0184)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	hw_btnr_Mode0LoWgtHdrsht_scale Motion detect mode 0 lo weight calc offset for for hdr short exposure frame, invalid in linear mode.U4.10
15:14	RO	0x0	reserved
13:0	RW	0x0000	hw_btnr_Mode0LoWgt_scale Motion detect mode 0 lo weight calc offset for hdr long exposure frame or linear mode.U4.10

BAY3D_2B00_BAY3D_WGTSCL1

Address: Operational Base(0x21D02B00) + offset (0x0188)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	hw_btnr_Mode1LoWgtHdrSht_scale Motion detect mode 1 lo weight calc scale for for hdr short exposure frame, invalid in linear mode.U4.10
15:14	RO	0x0	reserved
13:0	RW	0x0000	hw_btnr_Mode1LoWgt_scale Motion detect mode 1 lo weight calc scale for hdr long exposure frame or linear mode.U4.10

BAY3D_2B00_BAY3D_WGTSCL2

Address: Operational Base(0x21D02B00) + offset (0x018C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	hw_btnr_Mode1WgtHdrSht_scale Motion detect mode 1 weight calc scalefor for hdr short exposure frame, invalid in linear mode.U4.10
15:14	RO	0x0	reserved
13:0	RW	0x0000	hw_btnr_Mode1Wgt_scale Motion detect mode 1 weight calc scale for hdr long exposure frame or linear mode.U4.10

BAY3D_2B00_BAY3D_WGTOFF

Address: Operational Base(0x21D02B00) + offset (0x0190)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	hw_btnr_Mode1LoWgtHdrSht_offset Motion detect mode 1 lo weight calc offset for for hdr short exposure frame, invalid in linear mode.U4.10
15:14	RO	0x0	reserved
13:0	RW	0x0000	hw_btnr_Mode1LoWgt_offset Motion detect mode 1 lo weight calc offset for hdr long exposure frame or linear mode.U4.10

BAY3D_2B00_BAY3D_WGT1OFF

Address: Operational Base(0x21D02B00) + offset (0x0194)

Bit	Attr	Reset Value	Description
31:20	RW	0x000	hw_btnr_Mode1Wgt_offset Motion detect mode 1 weight calc offset.U0.12
19:10	RW	0x000	hw_btnr_Mode1Wgt_minLimit Mode 1 weight min limit

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	hw_btnr_autoSigmaCountWgt_thred Threshold of motion weight for auto sigma curve statistics.U0.10

BAY3D_2B00_BAY3D_SIGORG

Address: Operational Base(0x21D02B00) + offset (0x0198)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:0	RW	0x0000000	hw_btnr_tnrOutSigmaSq The square of the noise sigma of the still region of the output image, this parameter is not commonly used at present.U10.16

BAY3D_2B00_BAY3D_WGTLO_L

Address: Operational Base(0x21D02B00) + offset (0x019C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	hw_btnr_loWgtClipHdrSht_minLimit Min limit for the filter weight in temporal domain for hdr short exposure frame, invalid in linear mode.U4.10
15:14	RO	0x0	reserved
13:0	RW	0x0000	hw_btnr_loWgtClip_minLimit Min limit for the filter weight in temporal domain for hdr long exposure frame or linear mode.U4.10

BAY3D_2B00_BAY3D_WGTLO_H

Address: Operational Base(0x21D02B00) + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	hw_btnr_loWgtClipHdrSht_maxLimit Max limit for the filter weight in temporal domain for hdr short exposure frame, invalid in linear mode.U4.10
15:14	RO	0x0	reserved
13:0	RW	0x0000	hw_btnr_loWgtClip_maxLimit Max limit for the filter weight in temporal domain for hdr long exposure frame or linear mode.U4.10

BAY3D_2B00_BAY3D_STH_SCL

Address: Operational Base(0x21D02B00) + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_loPreRbSoftThresh_scale Soft thresholding sigma scale for RB channel.U2.10
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_btnr_loPreGgSoftThresh_scale Soft thresholding sigma scale for G channel.U2.10

BAY3D_2B00_BAY3D_STH_LIMIT

Address: Operational Base(0x21D02B00) + offset (0x01A8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_loPreSoftThresh_minLimit Soft thresholding delta value min limit.U2.10
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_btnr_loPreSoftThresh_maxLimit Soft thresholding delta value max limit.U2.10

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BAY3D_2B00_BAY3D_HIKEEP

Address: Operational Base(0x21D02B00) + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	hw_btnr_motionEstLoWgt_thred Motion estimate low weight threshold, motion compensation will be done only in areas of the image greater than this threshold. U0.12
15:8	RW	0x00	hw_btnr_preSpnrHiWgt_minLimit Pre hi freq spnr output weight in temporal domain min limit.U0.8
7:0	RW	0x00	hw_btnr_curSpnrHiWgt_minLimit Pre hi freq spnr output weight in temporal domain min limit.U0.8

BAY3D_2B00_BAY3D_PIXMAX

Address: Operational Base(0x21D02B00) + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	hw_btnr_pix_maxLimit Pixel max limit after transform.U0.12

BAY3D_2B00_BAY3D_SIGNUMTH

Address: Operational Base(0x21D02B00) + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	hw_btnr_autoSigmaCountCnt_thred Sigma statistic num threshold

BAY3D_2B00_BAY3D_MONR

Address: Operational Base(0x21D02B00) + offset (0x01B8)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	hw_btnr_gainOut_maxLimit Local gain output max limit.U0.8
23:22	RO	0x0	reserved
21:11	RW	0x000	hw_btnr_outUseMdNoiseBalNr_strg Md freq filter out weight for noise balance.U1.10
10:0	RW	0x000	hw_btnr_outUseHiNoiseBalNr_strg Hi freq filter out weight for noise balance.U1.10

BAY3D_2B00_BAY3D_SIGSCL

Address: Operational Base(0x21D02B00) + offset (0x01BC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	hw_btnr_SigmaHdrSht_scale Tnr sigma scale for hdr short exposure frame, invalid in linear mode. U6.8
15:14	RO	0x0	reserved
13:0	RW	0x0000	hw_btnr_Sigma_scale Tnr sigma scale for hdr long exposure frame or linear mode. U6.8

BAY3D_2B00_BAY3D_DSOFF

Address: Operational Base(0x21D02B00) + offset (0x01D0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	hw_btnr_LoWgtCalFirstLineVfilt_wgt LoWgtMD vertical IIR filter first line coeff.U1.4,range[0,16]
23:22	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
21:10	RW	0x000	hw_btnr_LoDiffVfilt_offset LoDiffMD vertical IIR filter weight calc offset.U12
9:0	RW	0x000	hw_btnr_LoWgtVfilt_offset LoWgtMD vertical IIR filter weight calc offset.U10

BAY3D_2B00_BAY3D_DSSCL

Address: Operational Base(0x21D02B00) + offset (0x01D4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	hw_btnr_LoDiffFirstLineVfilt_wgt LoDiffMD vertical IIR filter first line coeff.U1.4,range[0,16]
23	RO	0x0	reserved
22:16	RW	0x00	hw_btnr_LoDiffVfilt_scale LoWgtMD vertical IIR filter weight calc scalet.U7
15:11	RO	0x00	reserved
10:8	RW	0x0	hw_btnr_LoDiffVfiltScale_bit LoDiffMD vertical IIR filter weight calc right shift bit,U3
7:6	RO	0x0	reserved
5:0	RW	0x00	hw_btnr_LoWgtVfilt_scale LoWgtMD vertical IIR filter weight calc scale.U2.4

BAY3D_2B00_BAY3D_ME0

Address: Operational Base(0x21D02B00) + offset (0x01D8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:28	RW	0x0	hw_btnr_motionEstSadVert_wgt0 Motion estimate sad vertical weight for up line, range[1,3]
27	RO	0x0	reserved
26:16	RW	0x000	hw_btnr_motionEstUpMvxCost_scale Motion estimate up motion vector x sad cost scale,U1.10
15:14	RO	0x0	reserved
13:0	RW	0x0000	hw_btnr_motionEstUpMvxCost_offset Motion estimate up motion vector x sad cost offset.U14

BAY3D_2B00_BAY3D_ME1

Address: Operational Base(0x21D02B00) + offset (0x01DC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:28	RW	0x0	hw_btnr_motionEstSadVert_wgt1 Motion estimate sad vertical weight for middle line, range[1,3]
27	RO	0x0	reserved
26:16	RW	0x000	hw_btnr_motionEstUpLeftMvxCost_scale Motion estimate up left motion vector x sad cost scale.U1.10
15:14	RO	0x0	reserved
13:0	RW	0x0000	hw_btnr_motionEstUpLeftMvxCost_offset Motion estimate up left motion vector x sad cost offset.U14

BAY3D_2B00_BAY3D_ME2

Address: Operational Base(0x21D02B00) + offset (0x01E0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:28	RW	0x0	hw_btnr_motionEstSadVert_wgt2 Motion estimate sad vertical weight for down line, range[1,3]
27	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
26:16	RW	0x000	hw_btnr_motionEstUpRightMvxCost_scale Motion estimate up right motion vector x sad cost scale.U1.10
15:14	RO	0x0	reserved
13:0	RW	0x0000	hw_btnr_motionEstUpRightMvxCost_offset Motion estimate up right motion vector x sad cost offset.U14

BAY3D_2B00_BAY3D_WGTMAX

Address: Operational Base(0x21D02B00) + offset (0x01E4)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	hw_btnr_lowgtClipMotion_maxLimit Tnr filter weight max limit,valid only when motion compensation enable.U14

BAY3D_2B00_BAY3D_WGT1MAX

Address: Operational Base(0x21D02B00) + offset (0x01E8)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	hw_btnr_Mode1Wgt_maxLimit Motion detect mode 1 weight calc max limit .U0.14

BAY3D_2B00_BAY3D_WGTM0

Address: Operational Base(0x21D02B00) + offset (0x01EC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	hw_btnr_Mode0WgtOut_offset Motion detect mode 0 weight offset
15:11	RO	0x00	reserved
10:0	RW	0x000	hw_btnr_Mode0WgtOut_maxLimit Motion detect mode 0 weight max limit

BAY3D_2B00_BAY3D_LOCOEF0

Address: Operational Base(0x21D02B00) + offset (0x01F0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	hw_btnr_SigHflt_coeff0 Sig hfilter coeff
23:20	RW	0x0	hw_btnr_SigHflt_coeff1 Sig hfilter coeff
19	RO	0x0	reserved
18:16	RW	0x0	hw_btnr_SigHflt_coeff2 Sig hfilter coeff
15:13	RO	0x0	reserved
12:8	RW	0x00	hw_btnr_LoWgtHflt_coeff0 LoDif hfilter coeff0
7:4	RW	0x0	hw_btnr_LoWgtHflt_coeff1 LoDif hfilter coeff1
3	RO	0x0	reserved
2:0	RW	0x0	hw_btnr_LoWgtHflt_coeff2 LoDif hfilter coeff2

BAY3D_2B00_BAY3D_LOCOEF1

Address: Operational Base(0x21D02B00) + offset (0x01F4)

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Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:8	RW	0x00	hw_btnr_LoDifHflt_coeff0 LoWgt hfilter coeff
7:4	RW	0x0	hw_btnr_LoDifHflt_coeff1 LoWgt hfilter coeff
3	RO	0x0	reserved
2:0	RW	0x0	hw_btnr_LoDifHflt_coeff2 LoWgt hfilter coeff

BAY3D_2B00_BAY3D_DPC0

Address: Operational Base(0x21D02B00) + offset (0x01F8)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	hw_btnr_PreSpnrDpcWk_offset Pre spnr dpc offset
15:8	RW	0x00	hw_btnr_PreSpnrDpcWk_scale Pre spnr dpc scale
7	RO	0x0	reserved
6:4	RW	0x0	hw_btnr_PreSpnrDpc_str Pre spnr dpc strength
3:2	RW	0x0	hw_btnr_PreSpnrDpcDark_str Pre spnr dpc dark strength
1:0	RW	0x0	hw_btnr_PreSpnrDpcBright_str Pre spnr dpc bright strength

BAY3D_2B00_BAY3D_DPC1

Address: Operational Base(0x21D02B00) + offset (0x01FC)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_PreSpnrDpcSoftThr_scale Pre spnr dpc soft threshold scale
15:11	RO	0x00	reserved
10:0	RW	0x000	hw_btnr_PreSpnrDpcNrBal_str Pre spnr dpc noise balance strength

BAY3D_2B00_BAY3D_PRELOWGT

Address: Operational Base(0x21D02B00) + offset (0x020C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	hw_btnr_preSpnrLoFilterWgt_min Pre spnr lo freq filter range weight calc minlimit.U0.8
15:8	RW	0x00	hw_btnr_preSpnrLoFilterOut_wgt Pre spnr lo freq filter pixel and original pixel merge weight.U1.7
7:0	RW	0x00	hw_btnr_preSpnrLoValWgtOut_wgt Pre spnr lo freq filter weight's averge and average weight merge weight.U1.7

BAY3D_2B00_BAY3D_MIDBIG0

Address: Operational Base(0x21D02B00) + offset (0x0280)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_mdLargeLoMdwgt_scale Extremely lo freq motion detect weight calc scale.U4.8
15:8	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	hw_btnr_mdLargeLoMdwgt_offset Extremely lo freq motion detect weight calc offset.U0.8

BAY3D_2B00_BAY3D_MIDBIG1

Address: Operational Base(0x21D02B00) + offset (0x0284)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_btnr_mdLargeLoWgtAdd_offset Extremely lo freq motion detect weight filter calc postive offset.U0.12
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_btnr_mdLargeLoWgtCut_offset Extremely lo freq motion detect weight filter calc negative offset.U0.12

BAY3D_2B00_BAY3D_MIDBIG2

Address: Operational Base(0x21D02B00) + offset (0x0288)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	hw_btnr_mdLargeLoWgt_scale Extremely lo freq weight detect weight filter calc scale.4.8

BAY3D_2B00_BAY3D_MONROFF

Address: Operational Base(0x21D02B00) + offset (0x028C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	WO	0x000	hw_btnr_outUseMdNoiseBalNr_off Md freq filter out weight offset for noise balance
15:11	RO	0x00	reserved
10:0	WO	0x000	hw_btnr_outUseHiNoiseBalNr_off Hi freq filter out weight offset for noise balance

BAY3D_2B00_BAY3D_TNRSUM

Address: Operational Base(0x21D02B00) + offset (0x02D4)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:0	RO	0x0000000	ro_bay3d_sigma_num The number of pixel satisfying the noise sigma statistic condition

BAY3D_2B00_BAY3D_TNRYO0

Address: Operational Base(0x21D02B00) + offset (0x02D8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RO	0x000	ro_bay3d_sigma_y1 Tnr sigma statistic value 1
15:12	RO	0x0	reserved
11:0	RO	0x000	ro_bay3d_sigma_y0 Tnr sigma statistic value 0

BAY3D_2B00_BAY3D_TNRYO1

Address: Operational Base(0x21D02B00) + offset (0x02DC)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RO	0x000	ro_bay3d_sigma_y3 Tnr sigma statistic value 3

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Bit	Attr	Reset Value	Description
15:12	RO	0x0	reserved
11:0	RO	0x000	ro_bay3d_sigma_y2 Tnr sigma statistic value 2

BAY3D_2B00_BAY3D_TNRYO2

Address: Operational Base(0x21D02B00) + offset (0x02E0)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RC	0x000	ro_bay3d_sigma_y5 Tnr sigma statistic value 5
15:12	RO	0x0	reserved
11:0	RO	0x000	ro_bay3d_sigma_y4 Tnr sigma statistic value 4

BAY3D_2B00_BAY3D_TNRYO3

Address: Operational Base(0x21D02B00) + offset (0x02E4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RO	0x000	ro_bay3d_sigma_y7 Tnr sigma statistic value 7
15:12	RO	0x0	reserved
11:0	RO	0x000	ro_bay3d_sigma_y6 Tnr sigma statistic value 6

BAY3D_2B00_BAY3D_TNRYO4

Address: Operational Base(0x21D02B00) + offset (0x02E8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RO	0x000	ro_bay3d_sigma_y9 Tnr sigma statistic value 9
15:12	RO	0x0	reserved
11:0	RO	0x000	ro_bay3d_sigma_y8 Tnr sigma statistic value 8

BAY3D_2B00_BAY3D_TNRYO5

Address: Operational Base(0x21D02B00) + offset (0x02EC)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RO	0x000	ro_bay3d_sigma_y11 Tnr sigma statistic value 11
15:12	RO	0x0	reserved
11:0	RO	0x000	ro_bay3d_sigma_y10 Tnr sigma statistic value 10

BAY3D_2B00_BAY3D_TNRYO6

Address: Operational Base(0x21D02B00) + offset (0x02F0)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RO	0x000	ro_bay3d_sigma_y13 Tnr sigma statistic value 13
15:12	RO	0x0	reserved
11:0	RO	0x000	ro_bay3d_sigma_y12 Tnr sigma statistic value 12

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BAY3D_2B00_BAY3D_TNRYO7

Address: Operational Base(0x21D02B00) + offset (0x02F4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RO	0x000	ro_bay3d_sigma_y15 Tnr sigma statistic value 15
15:12	RO	0x0	reserved
11:0	RO	0x000	ro_bay3d_sigma_y14 Tnr sigma statistic value 14

BAY3D_2B00_BAY3D_TNRYO8

Address: Operational Base(0x21D02B00) + offset (0x02F8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RO	0x000	ro_bay3d_sigma_y17 Tnr sigma statistic value 17
15:12	RO	0x0	reserved
11:0	RO	0x000	ro_bay3d_sigma_y16 Tnr sigma statistic value 16

BAY3D_2B00_BAY3D_TNRYO9

Address: Operational Base(0x21D02B00) + offset (0x02FC)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RO	0x000	ro_bay3d_sigma_y19 Tnr sigma statistic value 19
15:12	RO	0x0	reserved
11:0	RO	0x000	ro_bay3d_sigma_y18 Tnr sigma statistic value 18

44.4.2.11 CAC

ISP_CAC_2600_CTRL

Address: Operational Base(0x21D02600) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	W1C	0x0	sys_itself_force_upd Cac itself force update
30	RO	0x0	sw_cac_bypass_shd Cac bypass enable shadow.
29	RW	0x0	sw_cac_edgeDSetect_en_shd Cac edge detect enable shadow.
28	RW	0x0	sw_cac_negClip0_en_shd Cac negative clip enable shadow.
27	RW	0x0	cac_working Cac working flag 1'b0: Not working 1'b1: Working
26:22	RO	0x00	reserved
21	RW	0x0	sw_cacT_wgt_color_en_shd Cac weight color enable shadow.
20:6	RO	0x0000	reserved
5	RW	0x0	sw_cacT_wgt_color_en Cac weight color enable 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
4	RO	0x0	reserved
3	RW	0x0	hw_cacT_negClip0_en Cac negative clip enable 1'b0: No clip 1'b1: Negative data clip to 0
2	RW	0x0	hw_cacT_edgeDetect_en Cac edge detect enable 1'b0: Disable 1'b1: Enable
1	RW	0x0	hw_cacT_module_bypass Cac bypass enable 1'b0: Disable 1'b1: Enable
0	RW	0x0	hw_cacT_module_en 1'b0: Disable 1'b1: Enable

ISP_CAC_2600_PSF_PARA

Address: Operational Base(0x21D02600) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x2	hw_cacT_psfTableFix_bit Point spread function(PSF) shift bits. Range: [0, 10]

ISP_CAC_2600_HIGH_DIRECT

Address: Operational Base(0x21D02600) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0400	hw_cacT_hiDrct_ratio High frequency direct ratio Range: [0, 4] Fixed-point: [0, 3, 10]

ISP_CAC_2600_OVER_EXPO0

Address: Operational Base(0x21D02600) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x07d38	hw_cacT_overExpo_thred Overexposure threshold Range: [0, 2^20-1]

ISP_CAC_2600_OVER_EXPO1

Address: Operational Base(0x21D02600) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:0	RW	0x00fa70	hw_cacT_overExpo_adj Overexposure adjust Range: [0, 2^20]

ISP_CAC_2600_FLAT

Address: Operational Base(0x21D02600) + offset (0x0014)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	hw_cacT_flat_offset Flat offset Range: [0, 65535]
15:5	RO	0x000	reserved
4:0	RW	0x10	hw_cacT_flat_thred Flat threshold Range: [0, 1] Fixed-point: [0, 1, 4]

ISP_CAC_2600_GAUSS_COEFF

Address: Operational Base(0x21D02600) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:12	RW	0x0	hw_cacT_colorLoFlt_coeff1 Color Low Filter Coefficient 1. Range: [0, 4] Note: ((hw_cacT_colorLoFlt_coeff0+2*hw_cacT_colorLoFlt_coeff1)<=7) && ((hw_cacT_colorLoFlt_coeff0+2*hw_cacT_colorLoFlt_coeff1)>=1) .
11	RO	0x0	reserved
10:8	RW	0x0	hw_cacT_colorLoFlt_coeff0 Color Low Filter Coefficient 0. Range: [0, 4] Note: ((hw_cacT_colorLoFlt_coeff0+2*hw_cacT_colorLoFlt_coeff1)<=7) && ((hw_cacT_colorLoFlt_coeff0+2*hw_cacT_colorLoFlt_coeff1)>=1) .
7	RO	0x0	reserved
6:4	RW	0x1	hw_cacT_chromaLoFlt_coeff1 Chroma Low Filter Coefficient 1. Range: [0, 4] Note: ((hw_cacT_chromaLoFlt_coeff0 + 2*hw_cacT_chromaLoFlt_coeff1) <= 7) && ((hw_cacT_chromaLoFlt_coeff0 + 2*hw_cacT_chromaLoFlt_coeff1) >= 1).
3	RO	0x0	reserved
2:0	RW	0x2	hw_cacT_chromaLoFlt_coeff0 Chroma Low Filter Coefficient 0. Range: [0, 4] Note: ((hw_cacT_chromaLoFlt_coeff0+2*hw_cacT_chromaLoFlt_coeff1) <=7) && ((hw_cacT_chromaLoFlt_coeff0 + 2*hw_cacT_chromaLoFlt_coeff1)>=1).

ISP_CAC_2600_RATIO

Address: Operational Base(0x21D02600) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x500	hw_cacT_residualChroma_ratio Residual Chroma Ratio. Range: [0, 1] Fixed-point: [0, 1, 10]

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Bit	Attr	Reset Value	Description
15:11	RO	0x00	reserved
10:0	RW	0x100	hw_cacT_searchRange_ratio Search Range Ratio. Range: [0, 1] Fixed-point: [0, 1, 10]

ISP_CAC_2600_WGT_COLOR_B

Address: Operational Base(0x21D02600) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x066666	hw_cacT_wgtColorB_minThred Blue minimum threshold of color weight. Range: [0, 15.9] Fixed-point: [0, 4, 20]

ISP_CAC_2600_WGT_COLOR_R

Address: Operational Base(0x21D02600) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	hw_cacT_wgtColorR_minThred Red minimum threshold of color weight. Range: [0, 15.9] Fixed-point: [0, 4, 20]

ISP_CAC_2600_WGT_COLOR_SLOPE_B

Address: Operational Base(0x21D02600) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:0	RW	0x001400	hw_cacT_wgtColorB_slope Blue slope of color weight. Range: [0, 1024] Fixed-point: [0, 11, 10]

ISP_CAC_2600_WGT_COLOR_SLOPE_R

Address: Operational Base(0x21D02600) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:0	RW	0x002800	hw_cacT_wgtColorR_slope Red slope of color weight. Range: [0, 1024] Fixed-point: [0, 11, 10]

ISP_CAC_2600_WGT_COLOR_LUMA0

Address: Operational Base(0x21D02600) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x0642d	hw_cacT_wgtColor_minLuma Minimum luminance of color weight. Range: [0, 2^20-1]

ISP_CAC_2600_WGT_COLOR_LUMA1

Address: Operational Base(0x21D02600) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
24:0	RW	0x00000a4	hw_cacT_wgtColorLuma_slope Luminance slope of color weight. Range: [0, 16] Fixed-point: [0, 5, 20]

ISP_CAC_2600_WGT_OVER_EXPO0

Address: Operational Base(0x21D02600) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x0c85a	hw_cacT_wgtOverExpo_minThred Minimum threshold of overexposure weight. Range: [0, 2^20-1]

ISP_CAC_2600_WGT_OVER_EXPO1

Address: Operational Base(0x21D02600) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:0	RW	0x00000a4	hw_cacT_wgtOverExpo_slope Slope of overexposure weight. Range: [0, 16] Fixed-point: [0, 5, 20]

ISP_CAC_2600_WGT_CONTRAST0

Address: Operational Base(0x21D02600) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:0	RW	0x09999a	hw_cacT_wgtContrast_minThred Minimum threshold of contrast weight. Range: [0, 1] Fixed-point: [0, 1, 20]

ISP_CAC_2600_WGT_CONTRAST1

Address: Operational Base(0x21D02600) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0d55	hw_cacT_wgtContrast_slope Slope of contrast weight. Range: [0, 16] Fixed-point: [0, 5, 10]

ISP_CAC_2600_WGT_CONTRAST2

Address: Operational Base(0x21D02600) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	hw_cacT_wgtContrast_offset Offset of contrast weight. Range: [0, 2^20-1]

ISP_CAC_2600_WGT_DARK_AREA0

Address: Operational Base(0x21D02600) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x0c85a	hw_cacT_wgt_dark_thed Threshold of dark area weight. Range: [0, 2^20-1]

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ISP_CAC_2600_WGT_DARK_AREA1

Address: Operational Base(0x21D02600) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:0	RW	0x00000a4	hw_cacT_wgt_dark_slope Slope of dark area weight. Range: [0, 16] Fixed-point: [0, 5, 20]

ISP_CAC_2600_PSF_B0

Address: Operational Base(0x21D02600) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:24	RW	0x08	hw_cacT_psf_b_ker3 Cac psf kernerl 3 of blue. Range: [0, 0.99] Fixed-point: [0, 0, 8]
23:16	RW	0x08	hw_cacT_psf_b_ker2 Cac psf kernerl 2 of blue. Range: [0, 0.99] Fixed-point: [0, 0, 8]
15:8	RW	0x08	hw_cacT_psf_b_ker1 Cac psf kernerl 1 of blue. Range: [0, 0.99] Fixed-point: [0, 0, 8]
7:0	RW	0x08	hw_cacT_psf_b_ker0 Cac psf kernerl 0 of blue. Range: [0, 0.99] Fixed-point: [0, 0, 8]

ISP_CAC_2600_PSF_B1

Address: Operational Base(0x21D02600) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:24	RW	0x08	hw_cacT_psf_b_ker7 Cac psf kernerl 7 of blue. Range: [0, 0.99] Fixed-point: [0, 0, 8]
23:16	RW	0x08	hw_cacT_psf_b_ker6 Cac psf kernerl 6 of blue. Range: [0, 0.99] Fixed-point: [0, 0, 8]
15:8	RW	0x08	hw_cacT_psf_b_ker5 Cac psf kernerl 5 of blue. Range: [0, 0.99] Fixed-point: [0, 0, 8]
7:0	RW	0x08	hw_cacT_psf_b_ker4 Cac psf kernerl 4 of blue. Range: [0, 0.99] Fixed-point: [0, 0, 8]

ISP_CAC_2600_PSF_B2

Address: Operational Base(0x21D02600) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
23:16	RW	0x08	hw_cacT_psf_b_ker10 Cac psf kernerl 10 of blue. Range: [0, 0.99] Fixed-point: [0, 0, 8]
15:8	RW	0x08	hw_cacT_psf_b_ker9 Cac psf kernerl 9 of blue. Range: [0, 0.99] Fixed-point: [0, 0, 8]
7:0	RW	0x08	hw_cacT_psf_b_ker8 Cac psf kernerl 8 of blue. Range: [0, 0.99] Fixed-point: [0, 0, 8]

ISP_CAC_2600_PSF_R0

Address: Operational Base(0x21D02600) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:24	RW	0x08	hw_cacT_psf_r_ker3 Cac psf kernerl 3 of red. Range: [0, 0.99] Fixed-point: [0, 0, 8]
23:16	RW	0x08	hw_cacT_psf_r_ker2 Cac psf kernerl 2 of red. Range: [0, 0.99] Fixed-point: [0, 0, 8]
15:8	RW	0x08	hw_cacT_psf_r_ker1 Cac psf kernerl 1 of red. Range: [0, 0.99] Fixed-point: [0, 0, 8]
7:0	RW	0x08	hw_cacT_psf_r_ker0 Cac psf kernerl 0 of red. Range: [0, 0.99] Fixed-point: [0, 0, 8]

ISP_CAC_2600_PSF_R1

Address: Operational Base(0x21D02600) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:24	RW	0x08	hw_cacT_psf_r_ker7 Cac psf kernerl 7 of red. Range: [0, 0.99] Fixed-point: [0, 0, 8]
23:16	RW	0x08	hw_cacT_psf_r_ker6 Cac psf kernerl 6 of red. Range: [0, 0.99] Fixed-point: [0, 0, 8]
15:8	RW	0x08	hw_cacT_psf_r_ker5 Cac psf kernerl 5 of red. Range: [0, 0.99] Fixed-point: [0, 0, 8]
7:0	RW	0x08	hw_cacT_psf_r_ker4 Cac psf kernerl 4 of red. Range: [0, 0.99] Fixed-point: [0, 0, 8]

ISP_CAC_2600_PSF_R2

Address: Operational Base(0x21D02600) + offset (0x0068)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x08	hw_cacT_psf_r_ker10 Cac psf kernerl 10 of red. Range: [0, 0.99] Fixed-point: [0, 0, 8]
15:8	RW	0x08	hw_cacT_psf_r_ker9 Cac psf kernerl 9 of red. Range: [0, 0.99] Fixed-point: [0, 0, 8]
7:0	RW	0x08	hw_cacT_psf_r_ker8 Cac psf kernerl 8 of red. Range: [0, 0.99] Fixed-point: [0, 0, 8]

ISP_CAC_2600_RO_CNT

Address: Operational Base(0x21D02600) + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RO	0x0000	ro_row_cnt Cac picture row counter
15:13	RO	0x0	reserved
12:0	RO	0x0000	ro_col_cnt Cac picture column counter

ISP_CAC_2600_DEBUF

Address: Operational Base(0x21D02600) + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13	RO	0x0	ro_chroma_fifo_err_flag Chroma fifo full error flag.
12	RO	0x0	ro_conv_fifo_err_flag Convolution fifo full error flag.
11	RO	0x0	ro_g_fifo_err_flag Green fifo full error flag.
10	RO	0x0	ro_chroma_fifo_full_err Chroma fifo full error.
9	RO	0x0	ro_chroma_fifo_empty Chroma fifo empty.
8	RO	0x0	ro_chroma_fifo_full Chroma fifo full.
7	RO	0x0	reserved
6	RO	0x0	ro_conv_fifo_full_err Convolution fifo full error.
5	RO	0x0	ro_conv_fifo_empty Convolution fifo empty.
4	RO	0x0	ro_conv_fifo_full Convolution fifo full.
3	RO	0x0	ro_g_fifo_full_err Green fifo full error.
2	RO	0x0	ro_g_fifo_empty Green fifo empty.
1	RO	0x0	ro_g_fifo_full Green fifo full.
0	RO	0x0	reserved

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44.4.2.12 LSC

ISP_LSC_2200_CTRL

Address: Operational Base(0x21D02200) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	W1C	0x0	sys_itself_force_upd For force update this module configuration
30	RO	0x0	ro_lsc_lut_loading Lsc lut loading flag
29:26	RO	0x0	reserved
25:24	RW	0x0	sys_itself_lut_mode LSC update mode 2'b00: Open frame_end and force update load lut mode 2'b11: soft control force update load lut mode; Suggest use force-upd load lut mode
23:5	RO	0x00000	reserved
4	RW	0x0	sws_pre_rd_st_mode 1'b0: mainLSC will read the table at the time of BLS frame start, rawLSC and drcLSC will read the table at the time of itself frame end. 1'b1: mainLSC will read the table at the time of itself frame end, rawLSC and drcLSC will read the table at the time of BLS frame start. Note: Path select of LSC is configured in sw_lsc_cfg_path_sel (address offset 0x0004[25:24]).
3	RO	0x0	reserved
2	RW	0x0	sw_lsc_sector_config16x16_en 1'b0: The sector will configure 8x8 and map to right and down(Old mode) 1'b1: All the 16x16 sector will be configured(New mode)
1	WO	0x0	lsc_lut_en Load correction factor from DDR, and will be cleared when begin to load DDR
0	RW	0x0	lsc_en 1'b0: lsc disable 1'b1: lsc enable

ISP_LSC_2200_TABLE_RAM_ADDR_R

Address: Operational Base(0x21D02200) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x000	ram_addr_r Table address in internal RAM of the R color component. Range from 0 to 152.

ISP_LSC_2200_TABLE_RAM_ADDR_GR

Address: Operational Base(0x21D02200) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x000	ram_addr_gr Table address in internal RAM of the GR color component. Range from 0 to 152.

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ISP_LSC_2200_TABLE_RAM_ADDR_B

Address: Operational Base(0x21D02200) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x000	ram_addr_b Table address in internal RAM of the B color component. Range from 0 to 152.

ISP_LSC_2200_TABLE_RAM_ADDR_GB

Address: Operational Base(0x21D02200) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x000	ram_addr_gb Table address in internal RAM of the GB color component. Range from 0 to 152.

ISP_LSC_2200_TABLE_DATA_R

Address: Operational Base(0x21D02200) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:0	RW	0x0000000	ram_r_data R component ram rdata0 , which stored its tables. The address will automatically increments by 1 each time when it is read.

ISP_LSC_2200_TABLE_DATA_GR

Address: Operational Base(0x21D02200) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:0	RW	0x0000000	ram_gr_data GR component ram rdata0 , which stored its tables. The address will automatically increments by 1 each time when it is read.

ISP_LSC_2200_TABLE_DATA_B

Address: Operational Base(0x21D02200) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:0	RW	0x0000000	ram_b_data B component ram rdata0 , which stored its tables. The address will automatically increments by 1 each time when it is read.

ISP_LSC_2200_TABLE_DATA_GB

Address: Operational Base(0x21D02200) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:0	RW	0x0000000	ram_gr_data GB component ram rdata0 , which stored its tables. The address will automatically increments by 1 each time when it is read.

ISP_LSC_2200_FACTOR_X_01

Address: Operational Base(0x21D02200) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	factor_x_1 Factor calculation for x-gradient of sector 1
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x000	factor_x_0 Factor calculation for x-gradient of sector 0

ISP_LSC_2200_FACTOR_X_23

Address: Operational Base(0x21D02200) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	factor_x_3 Factor calculation for x-gradient of sector 3
15:12	RO	0x0	reserved
11:0	RW	0x000	factor_x_2 Factor calculation for x-gradient of sector 2

ISP_LSC_2200_FACTOR_X_45

Address: Operational Base(0x21D02200) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	factor_x_5 Factor calculation for x-gradient of sector 5
15:12	RO	0x0	reserved
11:0	RW	0x000	factor_x_4 Factor calculation for x-gradient of sector 4

ISP_LSC_2200_FACTOR_X_67

Address: Operational Base(0x21D02200) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	factor_x_7 Factor calculation for x-gradient of sector 7
15:12	RO	0x0	reserved
11:0	RW	0x000	factor_x_6 Factor calculation for x-gradient of sector 6

ISP_LSC_2200_FACTOR_Y_01

Address: Operational Base(0x21D02200) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	factor_y_1 Factor calculation for y-gradient of sector 1
15:12	RO	0x0	reserved
11:0	RW	0x000	factor_y_0 Factor calculation for y-gradient of sector 0

ISP_LSC_2200_FACTOR_Y_23

Address: Operational Base(0x21D02200) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	factor_y_3 Factor calculation for y-gradient of sector 3
15:12	RO	0x0	reserved
11:0	RW	0x000	factor_y_2 Factor calculation for y-gradient of sector 2

ISP_LSC_2200_FACTOR_Y_45

Address: Operational Base(0x21D02200) + offset (0x003C)

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Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	factor_y_5 Factor calculation for y-gradient of sector 5
15:12	RO	0x0	reserved
11:0	RW	0x000	factor_y_4 Factor calculation for y-gradient of sector 4

ISP_LSC_2200_FACTOR_Y_67

Address: Operational Base(0x21D02200) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	factor_y_7 Factor calculation for y-gradient of sector 7
15:12	RO	0x0	reserved
11:0	RW	0x000	factor_y_6 Factor calculation for y-gradient of sector 6

ISP_LSC_2200_SIZE_X_01

Address: Operational Base(0x21D02200) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	x_size_1 Sector size 1 in x-direction
15:10	RO	0x00	reserved
9:0	RW	0x000	x_size_0 Sector size 0 in x-direction Note:The sum of the sector sizes in x direction must equal to "picture width / 2". Each size sector x can not be smaller than 10.

ISP_LSC_2200_SIZE_X_23

Address: Operational Base(0x21D02200) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	x_size_3 Sector size 3 in x-direction
15:10	RO	0x00	reserved
9:0	RW	0x000	x_size_2 Sector size 2 in x-direction

ISP_LSC_2200_SIZE_X_45

Address: Operational Base(0x21D02200) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	x_size_5 Sector size 5 in x-direction
15:10	RO	0x00	reserved
9:0	RW	0x000	x_size_4 Sector size 4in x-direction

ISP_LSC_2200_SIZE_X_67

Address: Operational Base(0x21D02200) + offset (0x0050)

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Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	x_size_7 Sector size 7 in x-direction
15:10	RO	0x00	reserved
9:0	RW	0x000	x_size_6 Sector size 6 in x-direction

ISP_LSC_2200_SIZE_Y_01

Address: Operational Base(0x21D02200) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	y_size_1 Sector size 1 in y-direction
15:10	RO	0x00	reserved
9:0	RW	0x000	y_size_0 Sector size 0 in y-direction Note:The sum of the sector sizes in y direction must equal to "picture height / 2". Each size sector y can not be smaller than 8.

ISP_LSC_2200_SIZE_Y_23

Address: Operational Base(0x21D02200) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	y_size_3 Sector size 3 in y-direction
15:10	RO	0x00	reserved
9:0	RW	0x000	y_size_2 Sector size 2 in y-direction

ISP_LSC_2200_SIZE_Y_45

Address: Operational Base(0x21D02200) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	y_size_5 Sector size 5 in y-direction
15:10	RO	0x00	reserved
9:0	RW	0x000	y_size_4 Sector size 4 in y-direction

ISP_LSC_2200_SIZE_Y_67

Address: Operational Base(0x21D02200) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	y_size_7 Sector size 7 in y-direction
15:10	RO	0x00	reserved
9:0	RW	0x000	y_size_6 Sector size 6 in y-direction

ISP_LSC_2200_TABLE_SEL

Address: Operational Base(0x21D02200) + offset (0x0064)

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Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	table_sel 1'b0: Active tables set is table 0. 1'b1: Active tables set is table 1. Note: This is a shadow register. Table set 0 access by SW at table address 0...153. Table set 1 access at table address 154...307.

ISP_LSC_2200_ISP_LSC_STATUS

Address: Operational Base(0x21D02200) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:2	RO	0x00000000	reserved
1	RO	0x0	active_table 1'b0: Currently active tables set is table set 0 1'b1: Currently active tables set is table set 1
0	RO	0x0	lsc_en_status 1'b0: Lens shading correction is currently off 1'b1: Lens shading correction is currently on

ISP_LSC_2200_FACTOR_X_89

Address: Operational Base(0x21D02200) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	factor_x_9 Factor calculation for x-gradient of sector 9
15:12	RO	0x0	reserved
11:0	RW	0x000	factor_x_8 Factor calculation for x-gradient of sector 8

ISP_LSC_2200_FACTOR_X_AB

Address: Operational Base(0x21D02200) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	factor_x_b Factor calculation for x-gradient of sector b
15:12	RO	0x0	reserved
11:0	RW	0x000	factor_x_a Factor calculation for x-gradient of sector a

ISP_LSC_2200_FACTOR_X_CD

Address: Operational Base(0x21D02200) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	factor_x_d Factor calculation for x-gradient of sector d
15:12	RO	0x0	reserved
11:0	RW	0x000	factor_x_c Factor calculation for x-gradient of sector c

ISP_LSC_2200_FACTOR_X_EF

Address: Operational Base(0x21D02200) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	factor_x_f Factor calculation for x-gradient of sector f
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x000	factor_x_e Factor calculation for x-gradient of sector e

ISP_LSC_2200_FACTOR_Y_89

Address: Operational Base(0x21D02200) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	factor_y_9 Factor calculation for y-gradient of sector 9
15:12	RO	0x0	reserved
11:0	RW	0x000	factor_y_8 Factor calculation for y-gradient of sector 8

ISP_LSC_2200_FACTOR_Y_AB

Address: Operational Base(0x21D02200) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	factor_y_b Factor calculation for y-gradient of sector b
15:12	RO	0x0	reserved
11:0	RW	0x000	factor_y_a Factor calculation for y-gradient of sector a

ISP_LSC_2200_FACTOR_Y_CD

Address: Operational Base(0x21D02200) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	factor_y_d Factor calculation for y-gradient of sector d
15:12	RO	0x0	reserved
11:0	RW	0x000	factor_y_c Factor calculation for y-gradient of sector c

ISP_LSC_2200_FACTOR_Y_EF

Address: Operational Base(0x21D02200) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	factor_y_f Factor calculation for y-gradient of sector f
15:12	RO	0x0	reserved
11:0	RW	0x000	factor_y_e Factor calculation for y-gradient of sector e

ISP_LSC_2200_SIZE_X_89

Address: Operational Base(0x21D02200) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	x_size_9 Sector size 9 in x-direction
15:10	RO	0x00	reserved
9:0	RW	0x000	x_size_8 Sector size 8 in x-direction

ISP_LSC_2200_SIZE_X_AB

Address: Operational Base(0x21D02200) + offset (0x0094)

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Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	x_size_b Sector size b in x-direction
15:10	RO	0x00	reserved
9:0	RW	0x000	x_size_a Sector size a in x-direction

ISP_LSC_2200_SIZE_X_CD

Address: Operational Base(0x21D02200) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	x_size_d Sector size d in x-direction
15:10	RO	0x00	reserved
9:0	RW	0x000	x_size_c Sector size c in x-direction

ISP_LSC_2200_SIZE_X_EF

Address: Operational Base(0x21D02200) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	x_size_f Sector size f in x-direction
15:10	RO	0x00	reserved
9:0	RW	0x000	x_size_e Sector size e in x-direction

ISP_LSC_2200_SIZE_Y_89

Address: Operational Base(0x21D02200) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	y_size_9 Sector size 9 in y-direction
15:10	RO	0x00	reserved
9:0	RW	0x000	y_size_8 Sector size 8 in y-direction

ISP_LSC_2200_SIZE_Y_AB

Address: Operational Base(0x21D02200) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	y_size_b Sector size b in y-direction
15:10	RO	0x00	reserved
9:0	RW	0x000	y_size_a Sector size a in y-direction

ISP_LSC_2200_SIZE_Y_CD

Address: Operational Base(0x21D02200) + offset (0x00A8)

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Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	y_size_d Sector size d in y-direction
15:10	RO	0x00	reserved
9:0	RW	0x000	y_size_c Sector size c in y-direction

ISP_LSC_2200_SIZE_Y_EF

Address: Operational Base(0x21D02200) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	y_size_f Sector size f in y-direction
15:10	RO	0x00	reserved
9:0	RW	0x000	y_size_e Sector size e in y-direction

44.4.2.13 HDRDRC

ISP_RGBxDRC_3900_CTRL0

Address: Operational Base(0x21D03900) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	W1C	0x0	sys_itself_force_upd When write 1, it will force_upd drc module; auto-clear.
30	RO	0x0	ro_drc_working Drc working, high valid, read only.
29	RW	0x0	hw_adrc_raw_dly_dis Backdoor: disable lafifo2xdrc delay 2k/16 of raw_in bypass-path
28:4	RO	0x0000000	reserved
3	RW	0x0	hw_adrc_gainx32_en Input raw would leftshift 1bit, then max gain equal to x32 when it is enable in hdrx2 version.
2	RW	0x0	hw_adrc_compsBypass_en Backdoor: adrc input 20bit compression bypss, then max clip equal to 0xfff.
1	RW	0x0	hw_adrc_bypass_en Drc bypass enable.
0	RW	0x0	hw_adrc_module_en Drc function enable, shadow reg.

ISP_RGBxDRC_3900_CTRL1

Address: Operational Base(0x21D03900) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:28	RW	0x8	hw_adrc_logTransform_offsetbits Log offset: indata+(1<<offset_pow2), then log2data-offset_pow2.
27	RO	0x0	reserved
26:14	RW	0x0e41	hw_adrc_compsIdxLuma_scale Integer, fraction=[2,11], scale plgmax range(0~24576) for trans compress.

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Bit	Attr	Reset Value	Description
13:0	RW	0x0100	hw_adrc_drcGainIdxLuma_scale Integer, fraction=[6,8], pluma scale for table index of gain2raw.

ISP_RGBxDRC_3900_LPRATIO

Address: Operational Base(0x21D03900) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:24	RW	0x40	hw_adrc_adjGainIdxLuma_scale Integer, fraction=[0,8], for plgt*delta_scalein into scale table.
23:12	RW	0x000	hw_adrc_hiDetail_ratio Integer, fraction=[1,11], for delt=delt + gain_scl*hpdetail_ratio used.
11:0	RW	0x000	hw_adrc_loDetail_ratio Integer, fraction=[1,11], for delt=(lgt-nglt) + (lgt-maxl)*lpdetail_ratio used.

ISP_RGBxDRC_3900_BILAT0

Address: Operational Base(0x21D03900) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:24	RW	0x60	hw_adrc_bifilt_curPixelWgt Integer, fraction=[4,4]<<7, bilateral weight of current pix.
23	RW	0x1	hw_adrc_thumbThred_en Enable sw_drc_thumb_thd_neg.
22:17	RO	0x00	reserved
16:8	RW	0x077	hw_adrc_thumbThred_neg [1,8], bilat5x5 thumb negative clip value, unsigned value.
7:0	RW	0x00	hw_adrc_bifilt_wgtOffset The high 8bit of value={1,11}, bilateral weight offset for array_wt(bilateral weight){1,15}.

ISP_RGBxDRC_3900_BILAT1

Address: Operational Base(0x21D03900) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	hw_adrc_filtLuma_softThred [2,8], Luma_soft_thd: threshold constrain luma, clip(org_luma--soft_thd, org_luma+soft_thd).
15:5	RO	0x000	reserved
4	RW	0x0	hw_adrc_comps_mode Log mode: 1, lg[3,9]; 0,lg[4,8];
3:0	RW	0x8	hw_adrc_comps_offsetbits Compression offset for lg and dlg, default=8.

ISP_RGBxDRC_3900_BILAT2

Address: Operational Base(0x21D03900) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x10	hw_adrc_thumb_scale [4,4], Thumb scale, thumb*thumb_scale >>4.
15:12	RO	0x0	reserved
11:0	RW	0x400	hw_adrc_thumb_maxLimit [4,8], thumb clip value, min(thumb, thumb_clip).

ISP_RGBxDRC_3900_BILAT3

Address: Operational Base(0x21D03900) + offset (0x0018)

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Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x100	hw_adrc_loRange_invSigma Integer, fraction=[2,8], bil3x3 range sigma invert weight; (diff*range_sigma_inv)^2.
15:10	RO	0x00	reserved
9:0	RW	0x100	hw_adrc_hiRange_invSigma Integer, fraction=[2,8], bil5x5 range sigma invert weight; (diff*range_sigma_inv)^2.

ISP_RGBxDRC_3900_BILAT4

Address: Operational Base(0x21D03900) + offset (0x001C)

Bit	Attr	Reset Value	Description
31	RW	0x0	hw_adrc_bifiltSoftThred_en High valid, enable soft_thd constrain bilateral luminance for clip(org_luma-soft_thd,org_luma+soft_thd), shadow reg.
30:27	RO	0x0	reserved
26:16	RW	0x077	hw_adrc_bifilt_softThred {3,11}, Soft_thd constrain bilateral luminance for clip(org_luma-soft_thd,org_luma+soft_thd), shadow reg.
15:8	RW	0x00	hw_adrc_bifilt_hiWgt Integer, fraction=[0,8], range 0~255, Weight_bilat for plgt=(thd4x8*W + (16-W)*thd4x32) when bilateral X/W.
7:5	RO	0x0	reserved
4:0	RW	0x10	hw_adrc_bifilt_wgt Integer, fraction=[1,4], range 0~16, Weight_bilat for plgt=(plgt*W + (16-W)*plgmax) when bilateral filter out.

ISP_RGBxDRC_3900_GAIN_Y0

Address: Operational Base(0x21D03900) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0400	hw_adrc_luma2drcGain_val1 [3,10], Curve_gain2raw y1.
15:13	RO	0x0	reserved
12:0	RW	0x0400	hw_adrc_luma2drcGain_val0 [3,10], Curve_gain2raw y0.

ISP_RGBxDRC_3900_GAIN_Y1

Address: Operational Base(0x21D03900) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0400	hw_adrc_luma2drcGain_val3 [3,10], Curve_gain2raw y3.
15:13	RO	0x0	reserved
12:0	RW	0x0400	hw_adrc_luma2drcGain_val2 [3,10], Curve_gain2raw y2.

ISP_RGBxDRC_3900_GAIN_Y2

Address: Operational Base(0x21D03900) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0400	hw_adrc_luma2drcGain_val5 [3,10], Curve_gain2raw y5.
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x0400	hw_adrc_luma2drcGain_val4 [3,10], Curve_gain2raw y4.

ISP_RGBxDRC_3900_GAIN_Y3

Address: Operational Base(0x21D03900) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0400	hw_adrc_luma2drcGain_val7 [3,10], Curve_gain2raw y7.
15:13	RO	0x0	reserved
12:0	RW	0x0400	hw_adrc_luma2drcGain_val6 [3,10], Curve_gain2raw y6.

ISP_RGBxDRC_3900_GAIN_Y4

Address: Operational Base(0x21D03900) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0400	hw_adrc_luma2drcGain_val9 [3,10], Curve_gain2raw y9.
15:13	RO	0x0	reserved
12:0	RW	0x0400	hw_adrc_luma2drcGain_val8 [3,10], Curve_gain2raw y8.

ISP_RGBxDRC_3900_GAIN_Y5

Address: Operational Base(0x21D03900) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0400	hw_adrc_luma2drcGain_val11 [3,10], Curve_gain2raw y11.
15:13	RO	0x0	reserved
12:0	RW	0x0400	hw_adrc_luma2drcGain_val10 [3,10], Curve_gain2raw y10.

ISP_RGBxDRC_3900_GAIN_Y6

Address: Operational Base(0x21D03900) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0400	hw_adrc_luma2drcGain_val13 [3,10], Curve_gain2raw y13.
15:13	RO	0x0	reserved
12:0	RW	0x0400	hw_adrc_luma2drcGain_val12 [3,10], Curve_gain2raw y12.

ISP_RGBxDRC_3900_GAIN_Y7

Address: Operational Base(0x21D03900) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0400	hw_adrc_luma2drcGain_val15 [3,10], Curve_gain2raw y15.
15:13	RO	0x0	reserved
12:0	RW	0x0400	hw_adrc_luma2drcGain_val14 [3,10], Curve_gain2raw y14.

ISP_RGBxDRC_3900_GAIN_Y8

Address: Operational Base(0x21D03900) + offset (0x0040)

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Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0400	hw_adrc_luma2drcGain_val16 [3,10], Curve_gain2raw y16.

ISP_RGBxDRC_3900_COMPRES_Y0

Address: Operational Base(0x21D03900) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x047	hw_adrc_luma2luma_val1 [3,8], Curve_compress y1.
15:11	RO	0x00	reserved
10:0	RW	0x000	hw_adrc_luma2luma_val0 [3,8], Curve_compress y0.

ISP_RGBxDRC_3900_COMPRES_Y1

Address: Operational Base(0x21D03900) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x0cb	hw_adrc_luma2luma_val3 [3,8], Curve_compress y3.
15:11	RO	0x00	reserved
10:0	RW	0x08b	hw_adrc_luma2luma_val2 [3,8], Curve_compress y2.

ISP_RGBxDRC_3900_COMPRES_Y2

Address: Operational Base(0x21D03900) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x140	hw_adrc_luma2luma_val5 [3,8], Curve_compress y5.
15:11	RO	0x00	reserved
10:0	RW	0x107	hw_adrc_luma2luma_val4 [3,8], Curve_compress y4.

ISP_RGBxDRC_3900_COMPRES_Y3

Address: Operational Base(0x21D03900) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x1aa	hw_adrc_luma2luma_val7 [3,8], Curve_compress y7.
15:11	RO	0x00	reserved
10:0	RW	0x176	hw_adrc_luma2luma_val6 [3,8], Curve_compress y6.

ISP_RGBxDRC_3900_COMPRES_Y4

Address: Operational Base(0x21D03900) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x236	hw_adrc_luma2luma_val9 [3,8], Curve_compress y9.
15:11	RO	0x00	reserved
10:0	RW	0x1db	hw_adrc_luma2luma_val8 [3,8], Curve_compress y8.

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ISP_RGBxDRC_3900_COMPRES_Y5

Address: Operational Base(0x21D03900) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x2d4	hw_adrc_luma2luma_val11 [3,8], Curve_compress y11.
15:11	RO	0x00	reserved
10:0	RW	0x289	hw_adrc_luma2luma_val10 [3,8], Curve_compress y10

ISP_RGBxDRC_3900_COMPRES_Y6

Address: Operational Base(0x21D03900) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x35a	hw_adrc_luma2luma_val13 [3,8], Curve_compress y13.
15:11	RO	0x00	reserved
10:0	RW	0x31a	hw_adrc_luma2luma_val12 [3,8], Curve_compress y12.

ISP_RGBxDRC_3900_COMPRES_Y7

Address: Operational Base(0x21D03900) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x3cc	hw_adrc_luma2luma_val15 [3,8], Curve_compress y15.
15:11	RO	0x00	reserved
10:0	RW	0x396	hw_adrc_luma2luma_val14 [3,8], Curve_compress y14.

ISP_RGBxDRC_3900_COMPRES_Y8

Address: Operational Base(0x21D03900) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x400	hw_adrc_luma2luma_val16 [3,8], Curve_compress y16.

ISP_RGBxDRC_3900_SCALE_Y0

Address: Operational Base(0x21D03900) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x002	hw_adrc_luma2scale_val1 [1,11], Curve_scale y1.
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_adrc_luma2scale_val0 [1,11], Curve_scale y0.

ISP_RGBxDRC_3900_SCALE_Y1

Address: Operational Base(0x21D03900) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x04c	hw_adrc_luma2scale_val3 [1,11], Curve_scale y3.
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x014	hw_adrc_luma2scale_val2 [1,11], Curve_scale y2.

ISP_RGBxDRC_3900_SCALE_Y2

Address: Operational Base(0x21D03900) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x17d	hw_adrc_luma2scale_val5 [1,11], Curve_scale y5.
15:12	RO	0x0	reserved
11:0	RW	0x0c1	hw_adrc_luma2scale_val4 [1,11], Curve_scale y4.

ISP_RGBxDRC_3900_SCALE_Y3

Address: Operational Base(0x21D03900) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x304	hw_adrc_luma2scale_val7 [1,11], Curve_scale y7.
15:12	RO	0x0	reserved
11:0	RW	0x277	hw_adrc_luma2scale_val6 [1,11], Curve_scale y6.

ISP_RGBxDRC_3900_SCALE_Y4

Address: Operational Base(0x21D03900) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x42a	hw_adrc_luma2scale_val9 [1,11], Curve_scale y9.
15:12	RO	0x0	reserved
11:0	RW	0x397	hw_adrc_luma2scale_val8 [1,11], Curve_scale y8.

ISP_RGBxDRC_3900_SCALE_Y5

Address: Operational Base(0x21D03900) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x5c7	hw_adrc_luma2scale_val11 [1,11], Curve_scale y11.
15:12	RO	0x0	reserved
11:0	RW	0x4bb	hw_adrc_luma2scale_val10 [1,11], Curve_scale y10.

ISP_RGBxDRC_3900_SCALE_Y6

Address: Operational Base(0x21D03900) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x747	hw_adrc_luma2scale_val13 [1,11], Curve_scale y13.
15:12	RO	0x0	reserved
11:0	RW	0x6a4	hw_adrc_luma2scale_val12 [1,11], Curve_scale y12.

ISP_RGBxDRC_3900_SCALE_Y7

Address: Operational Base(0x21D03900) + offset (0x0084)

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Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x7e8	hw_adrc_luma2scale_val15 [1,11], Curve_scale y15.
15:12	RO	0x0	reserved
11:0	RW	0x7b0	hw_adrc_luma2scale_val14 [1,11], Curve_scale y14.

ISP_RGBxDRC_3900_SCALE_Y8

Address: Operational Base(0x21D03900) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x800	hw_adrc_luma2scale_val16 [1,11], Curve_scale y16.

ISP_RGBxDRC_3900_IIRWG_GAIN

Address: Operational Base(0x21D03900) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:0	RW	0x0000	hw_adrc_compsGain_minLimit [1,15], Drc out gain clip value, shadow reg.

ISP_RGBxDRC_3900_SFTHD_Y0

Address: Operational Base(0x21D03900) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x0f6	hw_adrc_thumbDiff2thred_val1 [1,8], Curve_Luma soft threshold value of curve-y1.
15:9	RO	0x00	reserved
8:0	RW	0x0fb	hw_adrc_thumbDiff2thred_val0 [1,8], Curve_Luma soft threshold value of curve-y0.

ISP_RGBxDRC_3900_SFTHD_Y1

Address: Operational Base(0x21D03900) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x0e3	hw_adrc_thumbDiff2thred_val3 [1,8], Curve_Luma soft threshold value of curve-y3.
15:9	RO	0x00	reserved
8:0	RW	0x0ef	hw_adrc_thumbDiff2thred_val2 [1,8], Curve_Luma soft threshold value of curve-y2.

ISP_RGBxDRC_3900_SFTHD_Y2

Address: Operational Base(0x21D03900) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x0b7	hw_adrc_thumbDiff2thred_val5 [1,8], Curve_Luma soft threshold value of curve-y5.
15:9	RO	0x00	reserved
8:0	RW	0x0d0	hw_adrc_thumbDiff2thred_val4 [1,8], Curve_Luma soft threshold value of curve-y4.

ISP_RGBxDRC_3900_SFTHD_Y3

Address: Operational Base(0x21D03900) + offset (0x009C)

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Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x082	hw_adrc_thumbDiff2thred_val7 [1,8], Curve_Luma soft threshold value of curve-y7.
15:9	RO	0x00	reserved
8:0	RW	0x09b	hw_adrc_thumbDiff2thred_val6 [1,8], Curve_Luma soft threshold value of curve-y6.

ISP_RGBxDRC_3900_SFTHD_Y4

Address: Operational Base(0x21D03900) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x060	hw_adrc_thumbDiff2thred_val9 [1,8], Curve_Luma soft threshold value of curve-y9.
15:9	RO	0x00	reserved
8:0	RW	0x06d	hw_adrc_thumbDiff2thred_val8 [1,8], Curve_Luma soft threshold value of curve-y8.

ISP_RGBxDRC_3900_SFTHD_Y5

Address: Operational Base(0x21D03900) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x053	hw_adrc_thumbDiff2thred_val11 [1,8], Curve_Luma soft threshold value of curve-y11.
15:9	RO	0x00	reserved
8:0	RW	0x058	hw_adrc_thumbDiff2thred_val10 [1,8], Curve_Luma soft threshold value of curve-y10.

ISP_RGBxDRC_3900_SFTHD_Y6

Address: Operational Base(0x21D03900) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x04f	hw_adrc_thumbDiff2thred_val13 [1,8], Curve_Luma soft threshold value of curve-y13.
15:9	RO	0x00	reserved
8:0	RW	0x050	hw_adrc_thumbDiff2thred_val12 [1,8], Curve_Luma soft threshold value of curve-y12.

ISP_RGBxDRC_3900_SFTHD_Y7

Address: Operational Base(0x21D03900) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x04d	hw_adrc_thumbDiff2thred_val15 [1,8], Curve_Luma soft threshold value of curve-y15.
15:9	RO	0x00	reserved
8:0	RW	0x04e	hw_adrc_thumbDiff2thred_val14 [1,8], Curve_Luma soft threshold value of curve-y14.

ISP_RGBxDRC_3900_SFTHD_Y8

Address: Operational Base(0x21D03900) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x04d	hw_adrc_thumbDiff2thred_val16 [1,8], Curve_Luma soft threshold value of curve-y16.

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ISP_RGBxDRC_3900_LUMA_MIX

Address: Operational Base(0x21D03900) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	hw_adrc_minLuma_wgt [1,7], Luma mix weight config3.
15:8	RW	0x00	hw_adrc_midLuma_wgt [1,7], Luma mix weight config2.
7:0	RW	0x80	hw_adrc_maxLuma_wgt [1,7], Luma mix weight config1.

44.4.2.14 GIC

ISP_GIC_2F00_CTRL

Address: Operational Base(0x21D02F00) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	W1C	0x0	sys_itself_force_upd When write 1, it will force_upd gic module; auto-clear. Note: Reaback is the shadow of sw_gic_en.
30	RO	0x0	ro_gic_woking 1'b1: GIC is working 1'b0: GIC is not working
29	RO	0x0	ro_gic_pipe_error GIC pipeline error state. Cleared by sys_itself_force_upd.
28	RO	0x0	sw_gic_bypass_en_shd GIC bypass enable, shadow register.
27	RO	0x0	sw_gic_pro_mode_shd GIC filter process mode, shadow register. 1'b0: Median filter 1'b1: Gaus filter
26	RO	0x0	sw_gic_manualnoisecurve_en_shd GIC manual noise curve enable, shadow register.
25	RO	0x1	sw_gic_manualnoisethred_en_shd GIC manual thredshold curve enable, shadow register.
24	RO	0x0	sw_gic_gain_bypass_en_shd GIC gain bypass enable, shadow register.
23:6	RO	0x00000	reserved
5	RW	0x0	sw_gic_gain_bypass_en GIC gain bypass enable.
4	RW	0x1	sw_gic_manualnoisethred_en GIC manual thredshold curve enable. 1.b0: Adaptive calculation 1'b1: Configure thredshold curve
3	RW	0x1	sw_gic_manualnoisecurve_en GIC manual noise curve enable. 1.b0: Noise curve from sharp 1'b1: Noise curve from configuration
2	RW	0x0	sw_gic_pro_mode GIC filter process mode. 1'b0: Median filter 1'b1: Gaus filter
1	RW	0x0	sw_gic_bypass_en GIC bypass enable. Keep pipeline, data bypass. Note: If sw_gic_bypass_en = 1, sw_gic_en must be set 1.

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Bit	Attr	Reset Value	Description
0	RW	0x0	sw_gic_en 1'b1: Enable gic module 1'b0: Close gic module Note: This shadow register is CTRL[31].

ISP_GIC_2F00_MEDFLT_PARA

Address: Operational Base(0x21D02F00) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x80	sw_gic_medflt_ratio Median filter in and out data fusion ratio. Integer, fraction=[1, 7]
15:8	RO	0x00	reserved
7:4	RW	0x6	sw_gic_medflt_maxthred Maxmum clipping index after 3x3 data sorting. Note: Range is 1~7
3:0	RW	0x2	sw_gic_medflt_minthred Minimum clipping index after 3x3 data sorting. Note: Range is 1~7

ISP_GIC_2F00_MEDFLTUV_PARA

Address: Operational Base(0x21D02F00) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x80	sw_gic_medfltuv_ratio Median filter in and out data fusion ratio. Integer, fraction=[1, 7]
15:8	RO	0x00	reserved
7:4	RW	0x6	sw_gic_medfltuv_maxthred Maxmum clipping index after 3x3 data sorting. Note: Range is 1~7
3:0	RW	0x2	sw_gic_medfltuv_minthred Minimum clipping index after 3x3 data sorting. Note: Range is 1~7

ISP_GIC_2F00_NOISE_SCALE

Address: Operational Base(0x21D02F00) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x080	sw_gic_noisecurve_scale Bilateral filter sigma curve scale factor. Integer, fraction=[3, 7]

ISP_GIC_2F00_BILAT_PARA1

Address: Operational Base(0x21D02F00) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x6a	sw_gic_bffltwgt_scale Bilateral filter weigt scale factor. Integer, fraction=[3, 5]
15:10	RO	0x00	reserved
9:0	RW	0x0ec	sw_gic_bffltwgt_offset Bilateral filter weigt offset

ISP_GIC_2F00_BILAT_PARA2

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Address: Operational Base(0x21D02F00) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x80	sw_gic_bfflt_ratio Bilateral filter in and out data fusion weight. Integer, fraction=[1, 7]

ISP_GIC_2F00_DISWGT_COEFF

Address: Operational Base(0x21D02F00) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x0a	sw_gic_bfflt_coeff_2 Bilateral filter distance weight, corner point of 3x3 window Integer, fraction=[1, 5]
15:14	RO	0x0	reserved
13:8	RW	0x10	sw_gic_bfflt_coeff_1 Bilateral filter distance weight, cross point of 3x3 window Integer, fraction=[1, 5]
7:6	RO	0x0	reserved
5:0	RW	0x18	sw_gic_bfflt_coeff_0 Bilateral filter distance weight, center point of 3x3 window Integer, fraction=[1, 5] |sw_gic_bfflt_coeff_2 sw_gic_bfflt_coeff_1 sw_gic_bfflt_coeff_2| |sw_gic_bfflt_coeff_1 sw_gic_bfflt_coeff_0 sw_gic_bfflt_coeff_1| |sw_gic_bfflt_coeff_2 sw_gic_bfflt_coeff_1 sw_gic_bfflt_coeff_2|

ISP_GIC_2F00_SIGMA_Y0

Address: Operational Base(0x21D02F00) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x00d	sw_gic_bfflt_vsigma_y1 Curve-y1 value of sigma table.
15:10	RO	0x00	reserved
9:0	RW	0x00b	sw_gic_bfflt_vsigma_y0 Curve-y0 value of sigma table.

ISP_GIC_2F00_SIGMA_Y1

Address: Operational Base(0x21D02F00) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x010	sw_gic_bfflt_vsigma_y3 Curve-y3 value of sigma table.
15:10	RO	0x00	reserved
9:0	RW	0x00e	sw_gic_bfflt_vsigma_y2 Curve-y2 value of sigma table.

ISP_GIC_2F00_SIGMA_Y2

Address: Operational Base(0x21D02F00) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RW	0x012	sw_gic_bfflt_vsigma_y5 Curve-y5 value of sigma table.
15:10	RO	0x00	reserved
9:0	RW	0x011	sw_gic_bfflt_vsigma_y4 Curve-y4 value of sigma table.

ISP_GIC_2F00_SIGMA_Y3

Address: Operational Base(0x21D02F00) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x014	sw_gic_bfflt_vsigma_y7 Curve-y7 value of sigma table.
15:10	RO	0x00	reserved
9:0	RW	0x014	sw_gic_bfflt_vsigma_y6 Curve-y6 value of sigma table.

ISP_GIC_2F00_SIGMA_Y4

Address: Operational Base(0x21D02F00) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x016	sw_gic_bfflt_vsigma_y9 Curve-y9 value of sigma table.
15:10	RO	0x00	reserved
9:0	RW	0x015	sw_gic_bfflt_vsigma_y8 Curve-y8 value of sigma table.

ISP_GIC_2F00_SIGMA_Y5

Address: Operational Base(0x21D02F00) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x018	sw_gic_bfflt_vsigma_y11 Curve-y11 value of sigma table.
15:10	RO	0x00	reserved
9:0	RW	0x017	sw_gic_bfflt_vsigma_y10 Curve-y10 value of sigma table.

ISP_GIC_2F00_SIGMA_Y6

Address: Operational Base(0x21D02F00) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x018	sw_gic_bfflt_vsigma_y13 Curve-y13 value of sigma table.
15:10	RO	0x00	reserved
9:0	RW	0x018	sw_gic_bfflt_vsigma_y12 Curve-y12 value of sigma table.

ISP_GIC_2F00_SIGMA_Y7

Address: Operational Base(0x21D02F00) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x019	sw_gic_bfflt_vsigma_y15 Curve-y15 value of sigma table.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x018	sw_gic_bfflt_vsigma_y14 Curve-y14 value of sigma table.

ISP_GIC_2F00_SIGMA_Y8

Address: Operational Base(0x21D02F00) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x019	sw_gic_bfflt_vsigma_y16 Curve-y16 value of sigma table.

ISP_GIC_2F00_LUMA_DX

Address: Operational Base(0x21D02F00) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x7	sw_gic_luma_dx6 Threshold-curve luma delta-x6, get log2(x7-x6).
23:20	RW	0x8	sw_gic_luma_dx5 Threshold-curve luma delta-x5, get log2(x6-x5).
19:16	RW	0x8	sw_gic_luma_dx4 Threshold-curve luma delta-x4, get log2(x5-x4).
15:12	RW	0x7	sw_gic_luma_dx3 Threshold-curve luma delta-x3, get log2(x4-x3).
11:8	RW	0x7	sw_gic_luma_dx2 Threshold-curve luma delta-x2, get log2(x3-x2).
7:4	RW	0x6	sw_gic_luma_dx1 Threshold-curve luma delta-x1, get log2(x2-x1).
3:0	RW	0x6	sw_gic_luma_dx0 Threshold-curve luma delta-x0, get log2(x1-x0). E.g. If delta-x0 = 128, sw_gic_luma_dx0 = 7 (2^7 = 128).

ISP_GIC_2F00_THRED_Y0

Address: Operational Base(0x21D02F00) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x00d	sw_gic_thred_y1 Curve-y1 value of maximum threshold table.
15:9	RO	0x00	reserved
8:0	RW	0x00b	sw_gic_thred_y0 Curve-y0 value of maximum threshold table.

ISP_GIC_2F00_THRED_Y1

Address: Operational Base(0x21D02F00) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x011	sw_gic_thred_y3 Curve-y3 value of maximum threshold table.
15:9	RO	0x00	reserved
8:0	RW	0x00e	sw_gic_thred_y2 Curve-y2 value of maximum threshold table.

ISP_GIC_2F00_THRED_Y2

Address: Operational Base(0x21D02F00) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
24:16	RW	0x017	sw_gic_thred_y5 Curve-y5 value of maximum threshold table.
15:9	RO	0x00	reserved
8:0	RW	0x014	sw_gic_thred_y4 Curve-y4 value of maximum threshold table.

ISP_GIC_2F00_THRED_Y3

Address: Operational Base(0x21D02F00) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x019	sw_gic_thred_y7 Curve-y7 value of maximum threshold table.
15:9	RO	0x00	reserved
8:0	RW	0x018	sw_gic_thred_y6 Curve-y6 value of maximum threshold table.

ISP_GIC_2F00_MIN_THRED_Y0

Address: Operational Base(0x21D02F00) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_gic_minthred_y1 Curve-y1 value of minimum threshold table.
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_gic_minthred_y0 Curve-y0 value of minimum threshold table.

ISP_GIC_2F00_MIN_THRED_Y1

Address: Operational Base(0x21D02F00) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_gic_minthred_y3 Curve-y3 value of minimum threshold table.
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_gic_minthred_y2 Curve-y2 value of minimum threshold table.

ISP_GIC_2F00_MIN_THRED_Y2

Address: Operational Base(0x21D02F00) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_gic_minthred_y5 Curve-y5 value of minimum threshold table.
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_gic_minthred_y4 Curve-y4 value of minimum threshold table.

ISP_GIC_2F00_MIN_THRED_Y3

Address: Operational Base(0x21D02F00) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_gic_minthred_y7 Curve-y7 value of minimum threshold table.
15:9	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
8:0	RW	0x000	sw_gic_minthred_y6 Curve-y6 value of minimum threshold table.

ISP_GIC_2F00_THRED_SCALE

Address: Operational Base(0x21D02F00) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x080	sw_gic_autonoisethred_scale Adaptive calculation of the scaling factor of the threshold. Integer, fraction=[3, 7]

ISP_GIC_2F00_LOFLTGR_COEFF

Address: Operational Base(0x21D02F00) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x04	sw_gic_lofltgr_coeff_3 Low pass filtering coefficient of Gr channel, for threshold calculation.
23:21	RO	0x0	reserved
20:16	RW	0x04	sw_gic_lofltgr_coeff_2 Low pass filtering coefficient of Gr channel, for threshold calculation.
15:13	RO	0x0	reserved
12:8	RW	0x04	sw_gic_lofltgr_coeff_1 Low pass filtering coefficient of Gr channel, for threshold calculation.
7:5	RO	0x0	reserved
4:0	RW	0x04	sw_gic_lofltgr_coeff_0 Low pass filtering coefficient of Gr channel, for threshold calculation.

ISP_GIC_2F00_LOFLTGB_COEFF

Address: Operational Base(0x21D02F00) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:8	RW	0x06	sw_gic_lofltgb_coeff_1 Low pass filtering coefficient of Gb channel, for threshold calculation.
7:5	RO	0x0	reserved
4:0	RW	0x06	sw_gic_lofltgb_coeff_0 Low pass filtering coefficient of Gb channel, for threshold calculation.

ISP_GIC_2F00_SUM_LOFLT_INV

Address: Operational Base(0x21D02F00) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x00ab	sw_gic_sumlofltcoeff_inv The inverse of the threshold low-pass filter coefficient sum. Integer, fraction=[1, 12] Note: 1) sw_gic_lofltgr_coeff_0*2 + sw_gic_lofltgr_coeff_2*2 + sw_gic_lofltgr_coeff_1 + sw_gic_lofltgr_coeff_3 = sw_gic_lofltgb_coeff_0*2 + sw_gic_lofltgb_coeff_1*2 2) sw_gic_sumlofltcoeff_inv == (4096 + (sw_gic_lofltgb_coeff_0 + sw_gic_lofltgb_coeff_1)) / (sw_gic_lofltgb_coeff_0*2 _ sw_gic_lofltgb_coeff_1*2)

ISP_GIC_2F00_LOFLTTHRED_COEFF

Address: Operational Base(0x21D02F00) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:8	RW	0x08	sw_gic_loflttthred_coeff_1 Low pass filtering coefficient, for threshold calculation. Note: sw_gic_loflttthred_coeff_0*2 + sw_gic_loflttthred_coeff_1 = 16
7:5	RO	0x0	reserved
4:0	RW	0x04	sw_gic_loflttthred_coeff_0 Low pass filtering coefficient, for threshold calculation.

ISP_GIC_2F00_GAIN

Address: Operational Base(0x21D02F00) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x80	sw_gic_localgain_scale Gic local gain scale. Range: [0, 1] Fixed-point: [0, 1, 7]
15:12	RW	0x0	sw_gic_globalgain_alpha Gic global gain alpha. Range: [0, 1] Fixed-point: [0, 1, 3]
11:10	RO	0x0	reserved
9:0	RW	0x010	sw_gic_global_gain Gic global gain Range: [0, 63] Fixed-point: [0, 6, 4]

ISP_GIC_2F00_GAIN_SLOPE

Address: Operational Base(0x21D02F00) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0010	sw_gic_gain_scale Gain linearized slope. Integer, fraction=[7, 7]
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_gic_gain_offset Gain linearized axis-x start offset. Integer, fraction=[6, 4]

ISP_GIC_2F00_GAIN_THRED

Address: Operational Base(0x21D02F00) + offset (0x0098)

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Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x3f3	sw_gic_gainadjflt_maxthred Gain linearized axis-y end. Integer, fraction=[3, 7]
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_gic_gainadjflt_minthred Gain linearized axis-y start. Integer, fraction=[3, 7]

44.4.2.15 DEBAYER

ISP_DEBAYER_2500_CONTROL

Address: Operational Base(0x21D02500) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	ro_debayer_filter_c_en_shd The shadow register of hw_dmT_cntFlt_en.
30	RO	0x0	ro_debayer_filter_g_en_shd The shadow register of hw_dmT_gOutlsFlt_en.
29	RO	0x0	ro_debayer_en_shd The shadow register of sw_debayer_en
28	RO	0x0	ro_debayer_working 1'b0: Debayer module is not working 1'b1: Debayer module is working
27	RO	0x0	ro_debayer_bypass_shd Debayer bypass shadow.
26:9	RO	0x00000	reserved
8	RW	0x1	hw_dmT_cntFlt_en 1'b0: C filter module will bypass 1'b1: Enable c filter module
7:5	RO	0x0	reserved
4	RW	0x1	hw_dmT_gOutlsFlt_en 1'b0: G filter module will bypass 1'b1: Enable g filter
3:2	RO	0x0	reserved
1	RW	0x0	hw_dmT_bypass Debayer bypass.
0	RW	0x0	hw_dmT_en 1'b0: Debayer module will bypass 1'b1: Enable debayer

ISP_DEBAYER_2500_LUMA_DX

Address: Operational Base(0x21D02500) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x9	hw_dmT_luma_val7 Distance between point 6 and point 7.The actual distance is equal to 2^sw_debayer_luma_dx7.
23:20	RW	0xa	hw_dmT_luma_val6 Distance between point 5 and point 6.The actual distance is equal to 2^sw_debayer_luma_dx6.
19:16	RW	0xa	hw_dmT_luma_val5 Distance between point 4 and point 5.The actual distance is equal to 2^sw_debayer_luma_dx5.

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Bit	Attr	Reset Value	Description
15:12	RW	0x9	hw_dmT_luma_val4 Distance between point 3 and point 4.The actual distance is equal to 2^sw_debayer_luma_dx4.
11:8	RW	0x9	hw_dmT_luma_val3 Distance between point 2 and point 3.The actual distance is equal to 2^sw_debayer_luma_dx3.
7:4	RW	0x8	hw_dmT_luma_val2 Distance between point 1 and point 2.The actual distance is equal to 2^sw_debayer_luma_dx2.
3:0	RW	0x8	hw_dmT_luma_val1 Distance between point 0 and point 1.The actual distance is equal to 2^sw_debayer_luma_dx1. Note :The total distacne must be equal to 4096.

ISP_DEBAYER_2500_G_INTERP

Address: Operational Base(0x21D02500) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x04	hw_dmT_gInterpSharpStrg_maxLimit The level of sharp in the g interpolation. Range: [0,15.75] Fixed-point: [0,4,2]
23:16	RW	0x0d	hw_dmT_drctMethod_thred Select thed
15:12	RW	0x6	hw_dmT_loDrct_thred Range: [0,0.5] Fixed-point: [0,0,4]
11:8	RW	0x3	hw_dmT_hiDrct_thred Range: [0,0.5] Fixed-point: [0,0,4]
7:4	RW	0x8	hw_dmT_hiTexture_thred Range: [0,1.875] Fixed-point: [0,1,3]
3:1	RO	0x0	reserved
0	RW	0x1	hw_dmT_gInterpClip_en Clip enable for g interpolation If enable this bit, the interpolated g will be cliped to [Gmin,Gmax].

ISP_DEBAYER_2500_G_INTERP_FILTER1

Address: Operational Base(0x21D02500) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x04	hw_dmT_loDrctFlt_coeff4 Range: [-16,15] Fixed-point: [1,4,0] Note: coe3+coe4=0
23:21	RO	0x0	reserved
20:16	RW	0x1c	hw_dmT_loDrctFlt_coeff3 Range: [-16,15] Fixed-point: [1,4,0] Note: coe3+coe4=0
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:8	RW	0x02	hw_dmT_loDrctFlt_coeff2 Range: [-16,15] Fixed-point: [1,4,0] Note: coe1+coe2=0
7:5	RO	0x0	reserved
4:0	RW	0x1e	hw_dmT_loDrctFlt_coeff1 Range: [-16,15] Fixed-point: [1,4,0] Note: coe1+coe2=0

ISP_DEBAYER_2500_G_INTERP_FILTER2

Address: Operational Base(0x21D02500) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x04	hw_dmT_hiDrctFlt_coeff4 Range: [-16,15] Fixed-point: [1,4,0] Note: 2*coe3+coe4=0
23:21	RO	0x0	reserved
20:16	RW	0x1e	hw_dmT_hiDrctFlt_coeff3 Range: [-16,15] Fixed-point: [1,4,0] Note: 2*coe3+coe4=0
15:13	RO	0x0	reserved
12:8	RW	0x02	hw_dmT_hiDrctFlt_coeff2 Range: [-16,15] Fixed-point: [1,4,0] Note: 2*coe1+coe2=0
7:5	RO	0x0	reserved
4:0	RW	0x1f	hw_dmT_hiDrctFlt_coeff1 Range: [-16,15] Fixed-point: [1,4,0] Note: 2*coe1+coe2=0

ISP_DEBAYER_2500_G_INTERP_OFFSET_ALPHA

Address: Operational Base(0x21D02500) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:16	RW	0x40	hw_dmT_gradLoFlt_alpha Alpha for grad filter. Range: [0,64]
15:12	RO	0x0	reserved
11:0	RW	0x004	hw_dmT_gInterpSharpStrg_offset Gain offset for G interpolation

ISP_DEBAYER_2500_G_INTERP_DRCT_OFFSET0

Address: Operational Base(0x21D02500) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x010	hw_dmT_drct_offset1 Drct offset 1.
15:12	RO	0x0	reserved
11:0	RW	0x010	hw_dmT_drct_offset0 Drct offset 0.

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ISP_DEBAYER_2500_G_INTERP_DRCT_OFFSET1

Address: Operational Base(0x21D02500) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x010	hw_dmT_drct_offset3 Drct offset 3.
15:12	RO	0x0	reserved
11:0	RW	0x010	hw_dmT_drct_offset2 Drct offset 2.

ISP_DEBAYER_2500_G_INTERP_DRCT_OFFSET2

Address: Operational Base(0x21D02500) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x010	hw_dmT_drct_offset5 Drct offset 1.
15:12	RO	0x0	reserved
11:0	RW	0x010	hw_dmT_drct_offset4 Drct offset 0.

ISP_DEBAYER_2500_G_INTERP_DRCT_OFFSET3

Address: Operational Base(0x21D02500) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x010	hw_dmT_drct_offset7 Drct offset 3.
15:12	RO	0x0	reserved
11:0	RW	0x010	hw_dmT_drct_offset6 Drct offset 2.

ISP_DEBAYER_2500_G_FILTER_MODE_OFFSET

Address: Operational Base(0x21D02500) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x001	hw_dmT_gOutlsFltRange_offset Offset for G filter
15	RO	0x0	reserved
14:4	RW	0x400	hw_dmT_gOutlsFlt_ratio Bilateral filter fusion ratio.
3:1	RO	0x0	reserved
0	RW	0x0	hw_dmT_gOutlsFlt_mode 1'b0: Maxmin filter 1'b1: Bilateral filter

ISP_DEBAYER_2500_G_FILTER_FILTER

Address: Operational Base(0x21D02500) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x08	hw_dmT_gOutlsFlt_coeff2 G bilateral filter spatial coeff2.
15:8	RW	0x10	hw_dmT_gOutlsFlt_coeff1 G bilateral filter spatial coeff1.
7:0	RW	0x20	hw_dmT_gOutlsFlt_coeff0 G bilateral filter spatial coeff0.

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ISP_DEBAYER_2500_G_FILTER_VSIGMA0

Address: Operational Base(0x21D02500) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:16	RW	0x0800	hw_dmT_gOutlsFlt_vsigma1 Vsigma 1.
15:0	RW	0x0800	hw_dmT_gOutlsFlt_vsigma0 Vsigma 0.

ISP_DEBAYER_2500_G_FILTER_VSIGMA1

Address: Operational Base(0x21D02500) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:16	RW	0x0200	hw_dmT_gOutlsFlt_vsigma3 Vsigma 3.
15:0	RW	0x0400	hw_dmT_gOutlsFlt_vsigma2 Vsigma 2.

ISP_DEBAYER_2500_G_FILTER_VSIGMA2

Address: Operational Base(0x21D02500) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	RW	0x00cd	hw_dmT_gOutlsFlt_vsigma5 Vsigma 5.
15:0	RW	0x0155	hw_dmT_gOutlsFlt_vsigma4 Vsigma 4.

ISP_DEBAYER_2500_G_FILTER_VSIGMA3

Address: Operational Base(0x21D02500) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RW	0x0080	hw_dmT_gOutlsFlt_vsigma7 Vsigma 7.
15:0	RW	0x0092	hw_dmT_gOutlsFlt_vsigma6 Vsigma 6.

ISP_DEBAYER_2500_C_FILTER_GUIDE_GAUS

Address: Operational Base(0x21D02500) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x10	hw_dmT_cnrLoGuideLpf_coeff2 Guide gaussian filter coefficient 2. Range: [0,1) Fixed-point: [0,0,8] Note: coe0+4*coe1+4*coe2=256
15:8	RW	0x20	hw_dmT_cnrLoGuideLpf_coeff1 Guide gaussian filter coefficient 1. Range: [0,1) Fixed-point: [0,0,8] Note: coe0+4*coe1+4*coe2=256
7:0	RW	0x40	hw_dmT_cnrLoGuideLpf_coeff0 Guide gaussian filter coefficient 0. Range: [0,1) Fixed-point: [0,0,8] Note: coe0+4*coe1+4*coe2=256

ISP_DEBAYER_2500_C_FILTER_CE_GAUS

Address: Operational Base(0x21D02500) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
23:16	RW	0x10	hw_dmT_cnrPreFlt_coeff2 CE gaussian filter coefficient 2. Range: [0,1) Fixed-point: [0,0,8] Note: coe0+4*coe1+4*coe2=256
15:8	RW	0x20	hw_dmT_cnrPreFlt_coeff1 CE gaussian filter coefficient 1. Range: [0,1) Fixed-point: [0,0,8] Note: coe0+4*coe1+4*coe2=256
7:0	RW	0x40	hw_dmT_cnrPreFlt_coeff0 CE gaussian filter coefficient 0. Range: [0,1) Fixed-point: [0,0,8] Note: coe0+4*coe1+4*coe2=256

ISP_DEBAYER_2500_C_FILTER_ALPHA_GAUS

Address: Operational Base(0x21D02500) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x10	hw_dmT_cnrAlphaLpf_coeff2 Alpha gaussian filter coefficient 2. Range: [0,1) Fixed-point: [0,0,8] Note: coe0+4*coe1+4*coe2=256
15:8	RW	0x20	hw_dmT_cnrAlphaLpf_coeff1 Alpha gaussian filter coefficient 1. Range: [0,1) Fixed-point: [0,0,8] Note: coe0+4*coe1+4*coe2=256
7:0	RW	0x40	hw_dmT_cnrAlphaLpf_coeff0 Alpha gaussian filter coefficient 0. Range: [0,1) Fixed-point: [0,0,8] Note: coe0+4*coe1+4*coe2=256

ISP_DEBAYER_2500_C_FILTER_LOG_OFFSET

Address: Operational Base(0x21D02500) + offset (0x007C)

Bit	Attr	Reset Value	Description
31	RW	0x1	hw_dmT_logTrans_en Log trans enable.
30:28	RO	0x0	reserved
27:16	RW	0x001	hw_dmT_cnrLogGuide_offset Guide log offset
15:13	RO	0x0	reserved
12:0	RW	0x0080	hw_dmT_cnrLogGrad_offset Hf log offset

ISP_DEBAYER_2500_C_FILTER_ALPHA

Address: Operational Base(0x21D02500) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:12	RW	0x00400	hw_dmT_cnrMoireAlpha_scale Alpha scale. Range: [0,1024) Fixed-point: [0,10,10]

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Bit	Attr	Reset Value	Description
11:0	RW	0x000	hw_dmT_cnrMoireAlpha_offset Alpha offset

ISP_DEBAYER_2500_C_FILTER_EDGE

Address: Operational Base(0x21D02500) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:12	RW	0x00400	hw_dmT_cnrEdgeAlpha_scale Edge scale. Range: [0,1024) Fixed-point: [0,10,10]
11:0	RW	0x000	hw_dmT_cnrEdgeAlpha_offset Edge offset

ISP_DEBAYER_2500_C_FILTER_IIR_0

Address: Operational Base(0x21D02500) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x05a	hw_dmT_cnrLoFltWgt_slope Weight slope
15:14	RO	0x0	reserved
13:8	RW	0x08	hw_dmT_cnrLoFltStrg_shift Exp shift bits The most significant bit = 0 denotes right shift, and the most significant bit = 1 denotes left shift.
7:0	RW	0xd8	hw_dmT_cnrLoFltStrg_inv CE sigma

ISP_DEBAYER_2500_C_FILTER_IIR_1

Address: Operational Base(0x21D02500) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RW	0x02	hw_dmT_cnrLoFltWgt_minThred Weight ghost
7	RO	0x0	reserved
6:0	RW	0x3a	hw_dmT_cnrLoFltWgt_maxLimit Weight clip

ISP_DEBAYER_2500_C_FILTER_BF

Address: Operational Base(0x21D02500) + offset (0x0090)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	hw_dmT_cnrHiFltCur_wgt BF current weight
23	RO	0x0	reserved
22:16	RW	0x01	hw_dmT_cnrHiFltWgt_minLimit BF clip
15:0	RW	0x0800	hw_dmT_cnrHiFlt_vsigma BF sigma. Range: [0,1) Fixed-point: [0,0,16]

44.4.2.16 CCM

ISP_CCM_0700_CTRL

Address: Operational Base(0x21D00700) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_ccm_en_shd Shadow of sw_ccm_en
30	RW	0x0	ccm_working CCM working flag, read only. 1'b0: Closed 1'b1: Working
29	RW	0x0	sw_ccm_enh_adj_en_shd Shadow of sw_ccm_enh_adj_en
28	RW	0x0	sw_ccm_asym_adj_en_shd Shadow of sw_ccm_asym_adj_en
27	RW	0x0	sw_ccm_sat_decay_en_shd Shadow of sw_ccm_sat_decay_en
26:9	RO	0x00000	reserved
8	RW	0x0	sw_ccm_ckg_dis CCM clock gating. 1'b0: Gating enable 1'b1: Gating disable
7:5	RO	0x0	reserved
4	RW	0x0	sw_ccm_sat_decay_en Enable CCM saturation decay. 1'b1: Enable 1'b0: Disable
3	RW	0x0	sw_ccm_asym_adj_en Enable asymmetrical curve for luminance adjust. 1'b1: Use asymmetrical curve 1'b0: Use symmetrical curve
2	RW	0x0	sw_ccm_enh_adj_en Enable CCM color enhance adjust 1'b1: Enable 1'b0: Disable
1	RW	0x0	sw_ccm_highy_adjust_dis Disable CCM high Y alpha adjustment bit 1'b1: High Y alpha adjustment disable 1'b0: High Y alpha adjustment
0	RW	0x0	sw_ccm_en_i Enable CCM module 1'b1: Enable 1'b0: Disable The reset value is 1'b0

ISP_CCM_0700_COEFF0_R

Address: Operational Base(0x21D00700) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x7b7	sw_ccm_coeff1_r The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit fractional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff], so the value is expanded 128 times.
15:11	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
10:0	RW	0x065	sw_ccm_coeff0_r The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit fractional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff], so the value is expanded 128 times.

ISP_CCM_0700_COEFF1_R

Address: Operational Base(0x21D00700) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_ccm_offset_r The R offset value for CCM calculation. The range of offset value is from 0 to 4095.
15:11	RO	0x00	reserved
10:0	RW	0x7e4	sw_ccm_coeff2_r The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit fractional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff], so the value is expanded 128 times.

ISP_CCM_0700_COEFF0_G

Address: Operational Base(0x21D00700) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x058	sw_ccm_coeff1_g The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit fractional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff], so the value is expanded 128 times.
15:11	RO	0x00	reserved
10:0	RW	0x7d9	sw_ccm_coeff0_g The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit fractional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff], so the value is expanded 128 times.

ISP_CCM_0700_COEFF1_G

Address: Operational Base(0x21D00700) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_ccm_offset_g The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit fractional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff], so the value is expanded 128 times.
15:11	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
10:0	RW	0x7cf	sw_ccm_coeff2_g The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit fractional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff], so the value is expanded 128 times.

ISP_CCM_0700_COEFF0_B

Address: Operational Base(0x21D00700) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x7b7	sw_ccm_coeff1_b The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit fractional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff], so the value is expanded 128 times.
15:11	RO	0x00	reserved
10:0	RW	0x002	sw_ccm_coeff0_b The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit fractional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff], so the value is expanded 128 times.

ISP_CCM_0700_COEFF1_B

Address: Operational Base(0x21D00700) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_ccm_offset_b The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit fractional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff], so the value is expanded 128 times.
15:11	RO	0x00	reserved
10:0	RW	0x046	sw_ccm_coeff2_b The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit fractional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff], so the value is expanded 128 times.

ISP_CCM_0700_COEFF0_Y

Address: Operational Base(0x21D00700) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x04b	sw_ccm_coeff1_y The G coefficient value of RGB2Y calculation. The value is expanded 128 times.
15:11	RO	0x00	reserved
10:0	RW	0x026	sw_ccm_coeff0_y The R coefficient value of RGB2Y calculation. The value is expanded 128 times.

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ISP_CCM_0700_COEFF1_Y

Address: Operational Base(0x21D00700) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x00f	sw_ccm_coeff2_y The B coefficient value of RGB2Y calculation. The value is expanded 128 times.

ISP_CCM_0700_ALP_Y0

Address: Operational Base(0x21D00700) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x400	sw_ccm_alp_y1 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. When sw_ccm_asym_adj_en = 0, use for symmetrical curve, the value of y-axis point is expanded 128 times. When sw_ccm_asym_adj_en = 1, use for asymmetrical left curve, the value of y-axis point is expanded 256 times.
15:11	RO	0x00	reserved
10:0	RW	0x400	sw_ccm_alp_y0 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. When sw_ccm_asym_adj_en = 0, use for symmetrical curve, the value of y-axis point is expanded 128 times. When sw_ccm_asym_adj_en = 1, use for asymmetrical left curve, the value of y-axis point is expanded 256 times.

ISP_CCM_0700_ALP_Y1

Address: Operational Base(0x21D00700) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x400	sw_ccm_alp_y3 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. When sw_ccm_asym_adj_en = 0, use for symmetrical curve, the value of y-axis point is expanded 128 times. When sw_ccm_asym_adj_en = 1, use for asymmetrical left curve, the value of y-axis point is expanded 256 times.
15:11	RO	0x00	reserved
10:0	RW	0x400	sw_ccm_alp_y2 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. When sw_ccm_asym_adj_en = 0, use for symmetrical curve, the value of y-axis point is expanded 128 times. When sw_ccm_asym_adj_en = 1, use for asymmetrical left curve, the value of y-axis point is expanded 256 times.

ISP_CCM_0700_ALP_Y2

Address: Operational Base(0x21D00700) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
26:16	RW	0x400	sw_ccm_alp_y5 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. When sw_ccm_asym_adj_en = 0, use for symmetrical curve, the value of y-axis point is expanded 128 times. When sw_ccm_asym_adj_en = 1, use for asymmetrical left curve, the value of y-axis point is expanded 256 times.
15:11	RO	0x00	reserved
10:0	RW	0x400	sw_ccm_alp_y4 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. When sw_ccm_asym_adj_en = 0, use for symmetrical curve, the value of y-axis point is expanded 128 times. When sw_ccm_asym_adj_en = 1, use for asymmetrical left curve, the value of y-axis point is expanded 256 times.

ISP_CCM_0700_ALP_Y3

Address: Operational Base(0x21D00700) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x400	sw_ccm_alp_y7 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. When sw_ccm_asym_adj_en = 0, use for symmetrical curve, the value of y-axis point is expanded 128 times. When sw_ccm_asym_adj_en = 1, use for asymmetrical left curve, the value of y-axis point is expanded 256 times.
15:11	RO	0x00	reserved
10:0	RW	0x400	sw_ccm_alp_y6 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. When sw_ccm_asym_adj_en = 0, use for symmetrical curve, the value of y-axis point is expanded 128 times. When sw_ccm_asym_adj_en = 1, use for asymmetrical left curve, the value of y-axis point is expanded 256 times.

ISP_CCM_0700_ALP_Y4

Address: Operational Base(0x21D00700) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x400	sw_ccm_alp_y9 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. When sw_ccm_asym_adj_en = 0, use for symmetrical curve, the value of y-axis point is expanded 128 times. When sw_ccm_asym_adj_en = 1, use for asymmetrical right curve, the value of y-axis point is expanded 256 times.
15:11	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
10:0	RW	0x400	sw_ccm_alp_y8 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. When sw_ccm_asym_adj_en = 0, use for symmetrical curve, the value of y-axis point is expanded 128 times. When sw_ccm_asym_adj_en = 1, use for asymmetrical left curve, the value of y-axis point is expanded 256 times.

ISP_CCM_0700_ALP_Y5

Address: Operational Base(0x21D00700) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x400	sw_ccm_alp_y11 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. When sw_ccm_asym_adj_en = 0, use for symmetrical curve, the value of y-axis point is expanded 128 times. When sw_ccm_asym_adj_en = 1, use for asymmetrical right curve, the value of y-axis point is expanded 256 times.
15:11	RO	0x00	reserved
10:0	RW	0x400	sw_ccm_alp_y10 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. When sw_ccm_asym_adj_en = 0, use for symmetrical curve, the value of y-axis point is expanded 128 times. When sw_ccm_asym_adj_en = 1, use for asymmetrical right curve, the value of y-axis point is expanded 256 times.

ISP_CCM_0700_ALP_Y6

Address: Operational Base(0x21D00700) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x400	sw_ccm_alp_y13 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. When sw_ccm_asym_adj_en = 0, use for symmetrical curve, the value of y-axis point is expanded 128 times. When sw_ccm_asym_adj_en = 1, use for asymmetrical right curve, the value of y-axis point is expanded 256 times.
15:11	RO	0x00	reserved
10:0	RW	0x400	sw_ccm_alp_y12 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. When sw_ccm_asym_adj_en = 0, use for symmetrical curve, the value of y-axis point is expanded 128 times. When sw_ccm_asym_adj_en = 1, use for asymmetrical right curve, the value of y-axis point is expanded 256 times.

ISP_CCM_0700_ALP_Y7

Address: Operational Base(0x21D00700) + offset (0x0040)

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Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x400	sw_ccm_alp_y15 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. When sw_ccm_asym_adj_en = 0, use for symmetrical curve, the value of y-axis point is expanded 128 times. When sw_ccm_asym_adj_en = 1, use for asymmetrical right curve, the value of y-axis point is expanded 256 times.
15:11	RO	0x00	reserved
10:0	RW	0x400	sw_ccm_alp_y14 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. When sw_ccm_asym_adj_en = 0, use for symmetrical curve, the value of y-axis point is expanded 128 times. When sw_ccm_asym_adj_en = 1, use for asymmetrical right curve, the value of y-axis point is expanded 256 times.

ISP_CCM_0700_ALP_Y8

Address: Operational Base(0x21D00700) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_ccm_alp_y17 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. When sw_ccm_asym_adj_en = 0, this register is useless. When sw_ccm_asym_adj_en = 1, use for asymmetrical right curve, the value of y-axis point is expanded 256 times.
15:11	RO	0x00	reserved
10:0	RW	0x400	sw_ccm_alp_y16 CCM curve y-axis point definition for ccm input pixel's luminance. The range of the coefficient is from 0 to 1024, so the value is 11-bit unsigned. When sw_ccm_asym_adj_en = 0, use for symmetrical curve, the value of y-axis point is expanded 128 times. When sw_ccm_asym_adj_en = 1, use for asymmetrical right curve, the value of y-axis point is expanded 256 times.

ISP_CCM_0700_BOUND_BIT

Address: Operational Base(0x21D00700) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	sw_ccm_right_bit CCM alpha interpolation curve's inflection right point. The inflection point is 2^sw_ccm_right_bit. When sw_ccm_asym_adj_en = 0, this register is useless. When sw_ccm_asym_adj_en = 1, the max value is 4'd11 because the inflection point's max value is 2048.

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Bit	Attr	Reset Value	Description
3:0	RW	0xa	sw_ccm_bound_bit CCM alpha interpolation curve's inflection point. The inflection point is 2^sw_ccm_bound_bit. When sw_ccm_asym_adj_en = 0, the max value is 4'd10 because the inflection point's max value is 1024. When sw_ccm_asym_adj_en = 1, the max value is 4'd11 because the inflection point's max value is 2048.

ISP_CCM_0700_ENHANCE0

Address: Operational Base(0x21D00700) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_ccm_color_coef1_g2y The R coefficient value of RGB2Y calculation, use in color enhance adjust enable. The value is expanded 128 times.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_ccm_color_coef0_r2y The R coefficient value of RGB2Y calculation, use in color enhance adjust enable. The value is expanded 128 times.

ISP_CCM_0700_ENHANCE1

Address: Operational Base(0x21D00700) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_ccm_color_enh_rat_max Maximum compression ratio limit for dynamic range in enhance mode.
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_ccm_color_coef2_b2y The R coefficient value of RGB2Y calculation, use in color enhance adjust enable. The value is expanded 128 times.

ISP_CCM_0700_HF_THD

Address: Operational Base(0x21D00700) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0500	sw_ccm_hf_scale CCM scale of high frequency. Range: [0, 63] Fixed-point: [0, 6, 8]
15:8	RW	0xf0	sw_ccm_hf_up CCM up threshold of high frequency. Range: [0, 1] Fixed-point: [0, 0, 8]
7:0	RW	0x33	sw_ccm_hf_low CCM low threshold of high frequency. Range: [0, 1] Fixed-point: [0, 0, 8]

ISP_CCM_0700_HF_FACTOR0

Address: Operational Base(0x21D00700) + offset (0x0058)

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Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x3e0	sw_ccm_hf_factor1 CCM factor curve1 of high frequency. Range: [0, 1] Fixed-point: [0, 1, 10]
15:11	RO	0x00	reserved
10:0	RW	0x400	sw_ccm_hf_factor0 CCM factor curve0 of high frequency. Range: [0, 1] Fixed-point: [0, 1, 10]

ISP_CCM_0700_HF_FACTOR1

Address: Operational Base(0x21D00700) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x3a0	sw_ccm_hf_factor3 CCM factor curve3 of high frequency. Range: [0, 1] Fixed-point: [0, 1, 10]
15:11	RO	0x00	reserved
10:0	RW	0x3c0	sw_ccm_hf_factor2 CCM factor curve2 of high frequency. Range: [0, 1] Fixed-point: [0, 1, 10]

ISP_CCM_0700_HF_FACTOR2

Address: Operational Base(0x21D00700) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x360	sw_ccm_hf_factor5 CCM factor curve5 of high frequency. Range: [0, 1] Fixed-point: [0, 1, 10]
15:11	RO	0x00	reserved
10:0	RW	0x380	sw_ccm_hf_factor4 CCM factor curve4 of high frequency. Range: [0, 1] Fixed-point: [0, 1, 10]

ISP_CCM_0700_HF_FACTOR3

Address: Operational Base(0x21D00700) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x320	sw_ccm_hf_factor7 CCM factor curve7 of high frequency. Range: [0, 1] Fixed-point: [0, 1, 10]
15:11	RO	0x00	reserved
10:0	RW	0x340	sw_ccm_hf_factor6 CCM factor curve6 of high frequency. Range: [0, 1] Fixed-point: [0, 1, 10]

ISP_CCM_0700_HF_FACTOR4

Address: Operational Base(0x21D00700) + offset (0x0068)

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Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x2e0	sw_ccm_hf_factor9 CCM factor curve9 of high frequency. Range: [0, 1] Fixed-point: [0, 1, 10]
15:11	RO	0x00	reserved
10:0	RW	0x300	sw_ccm_hf_factor8 CCM factor curve8 of high frequency. Range: [0, 1] Fixed-point: [0, 1, 10]

ISP_CCM_0700_HF_FACTOR5

Address: Operational Base(0x21D00700) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x2a0	sw_ccm_hf_factor11 CCM factor curve11 of high frequency. Range: [0, 1] Fixed-point: [0, 1, 10]
15:11	RO	0x00	reserved
10:0	RW	0x2c0	sw_ccm_hf_factor10 CCM factor curve10 of high frequency. Range: [0, 1] Fixed-point: [0, 1, 10]

ISP_CCM_0700_HF_FACTOR6

Address: Operational Base(0x21D00700) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x260	sw_ccm_hf_factor13 CCM factor curve13 of high frequency. Range: [0, 1] Fixed-point: [0, 1, 10]
15:11	RO	0x00	reserved
10:0	RW	0x280	sw_ccm_hf_factor12 CCM factor curve12 of high frequency. Range: [0, 1] Fixed-point: [0, 1, 10]

ISP_CCM_0700_HF_FACTOR7

Address: Operational Base(0x21D00700) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x220	sw_ccm_hf_factor15 CCM factor curve15 of high frequency. Range: [0, 1] Fixed-point: [0, 1, 10]
15:11	RO	0x00	reserved
10:0	RW	0x240	sw_ccm_hf_factor14 CCM factor curve14 of high frequency. Range: [0, 1] Fixed-point: [0, 1, 10]

ISP_CCM_0700_HF_FACTOR8

Address: Operational Base(0x21D00700) + offset (0x0078)

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Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x200	sw_ccm_hf_factor16 CCM factor curve16 of high frequency. Range: [0, 1] Fixed-point: [0, 1, 10]

44.4.2.17 GAMMA_OUT

ISP_GAMMA_OUT_0900_CTRL

Address: Operational Base(0x21D00900) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	sw_gamma_out_en_shd Gamma_out enable shadow
30	RO	0x0	gamma_out_working Gamma_out working status
29:3	RO	0x0000000	reserved
2	RW	0x0	sw_gamma_out_finalx4_dense_en If this bit set 1, the 44 segments gamma out curve will change to 48 segments. The adder 4 segments will add at the final. The detail as follows: the segmentation from 0 to 4095 (48 segments): 1111 1111 2222 4444 8888 16.16.16.16 32.32.32.32 64.64.64.64 128.128.128.128 256.256.256.256 256.256.256.256 256.256.256.256; (old 512.512.512.512 change to new 256.256.256.256 256.256.256.256) Note: If this bit is 0, only need configure sw_gamma_out_y0 to sw_gamma_out_y44. if this bit is 1, need configure sw_gamma_out_y0 to sw_gamma_out_y48.
1	RW	0x0	sw_gamma_out_equ_segm 1'b0: Division like segmentation of gamma curve (default after reset) the segmentation from 0 to 4095 (44 segments): 1111 1111 2222 4444 8888 16.16.16.16 32.32.32.32 64.64.64.64 128.128.128.128 256.256.256.256 512.512.512.512; 1'b1: Equidistant segmentation (all segments are equally)
0	RW	0x0	sw_gamma_out_en 1'b0: Gamma_out disable 1'b1: Gamma_out enable

ISP_GAMMA_OUT_0900_OFFSET

Address: Operational Base(0x21D00900) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:0	RW	0x0000	sw_gamma_out_offset Offset value of gamma_out curve

ISP_GAMMA_OUT_0900_Y0

Address: Operational Base(0x21D00900) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:16	RW	0x001	sw_gamma_out_y1 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_gamma_out_y0 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y1

Address: Operational Base(0x21D00900) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x003	sw_gamma_out_y3 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x002	sw_gamma_out_y2 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y2

Address: Operational Base(0x21D00900) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x005	sw_gamma_out_y5 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x004	sw_gamma_out_y4 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y3

Address: Operational Base(0x21D00900) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x007	sw_gamma_out_y7 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x006	sw_gamma_out_y6 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y4

Address: Operational Base(0x21D00900) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x00a	sw_gamma_out_y9 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x008	sw_gamma_out_y8 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y5

Address: Operational Base(0x21D00900) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x00e	sw_gamma_out_y11 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x00c	sw_gamma_out_y10 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y6

Address: Operational Base(0x21D00900) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x014	sw_gamma_out_y13 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x010	sw_gamma_out_y12 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y7

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Address: Operational Base(0x21D00900) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x01c	sw_gamma_out_y15 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x018	sw_gamma_out_y14 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y8

Address: Operational Base(0x21D00900) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x028	sw_gamma_out_y17 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x020	sw_gamma_out_y16 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y9

Address: Operational Base(0x21D00900) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x038	sw_gamma_out_y19 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x030	sw_gamma_out_y18 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y10

Address: Operational Base(0x21D00900) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x050	sw_gamma_out_y21 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

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Bit	Attr	Reset Value	Description
15:12	RO	0x0	reserved
11:0	RW	0x040	sw_gamma_out_y20 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y11

Address: Operational Base(0x21D00900) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x070	sw_gamma_out_y23 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x060	sw_gamma_out_y22 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y12

Address: Operational Base(0x21D00900) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0a0	sw_gamma_out_y25 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x080	sw_gamma_out_y24 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y13

Address: Operational Base(0x21D00900) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0e0	sw_gamma_out_y27 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x0c0	sw_gamma_out_y26 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

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ISP_GAMMA_OUT_0900_Y14

Address: Operational Base(0x21D00900) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x140	sw_gamma_out_y29 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x100	sw_gamma_out_y28 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y15

Address: Operational Base(0x21D00900) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x1c0	sw_gamma_out_y31 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x180	sw_gamma_out_y30 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y16

Address: Operational Base(0x21D00900) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x280	sw_gamma_out_y33 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x200	sw_gamma_out_y32 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y17

Address: Operational Base(0x21D00900) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:16	RW	0x380	sw_gamma_out_y35 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x300	sw_gamma_out_y34 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y18

Address: Operational Base(0x21D00900) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x500	sw_gamma_out_y37 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x400	sw_gamma_out_y36 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y19

Address: Operational Base(0x21D00900) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x700	sw_gamma_out_y39 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0x600	sw_gamma_out_y38 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y20

Address: Operational Base(0x21D00900) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0xa00	sw_gamma_out_y41 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x800	sw_gamma_out_y40 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y21

Address: Operational Base(0x21D00900) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0xe00	sw_gamma_out_y43 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0xc00	sw_gamma_out_y42 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y22

Address: Operational Base(0x21D00900) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0xfff	sw_gamma_out_y45 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0xfff	sw_gamma_out_y44 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y23

Address: Operational Base(0x21D00900) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0xfff	sw_gamma_out_y47 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.
15:12	RO	0x0	reserved
11:0	RW	0xfff	sw_gamma_out_y46 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

ISP_GAMMA_OUT_0900_Y24

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Address: Operational Base(0x21D00900) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0xfff	sw_gamma_out_y48 GAMMA curve y-axis point definition for gamma_out input pixels. The range of the y value is from 0 to 4095, so the value is 12-bit unsigned. The initial value correspond to the 44-segment version.

44.4.2.18 HIST

ISP_HIST_3C00_CTRL

Address: Operational Base(0x21D03C00) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	W1C	0x0	sys_itself_force_upd Hist self force update
30	RO	0x0	hist_working Hist working flag, read only. 1'b0: Closed 1'b1: Working
29:27	RO	0x0	reserved
26	RW	0x0	sw_hist_mem_froce_shd Shadow of sw_hist_mem_force.
25:6	RO	0x00000	reserved
5	RW	0x0	sw_hist_mem_force Contrast limited adaptive histogram equalization memory mode force. 1'b0: Use auto mode of hardware 1'b1: Use sw_hist_mem_mode
4	RW	0x0	sw_hist_mem_mode Contrast limited adaptive histogram equalization memory mode. 1'b0: Memory use 18 bit mode 1'b1: Memory use 36 bit mode
3:2	RO	0x0	reserved
1	RW	0x0	sw_hist_bypass 1'b0: Disable 1'b1: Enable
0	RW	0x1	sw_hist_en Hist equalization, must shadow. 1'b0: Disable 1'b1: Enable

ISP_HIST_3C00_HF_STAT

Address: Operational Base(0x21D03C00) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x00a	sw_hist_count_min_limit Hist count minimum limit of weight. Range: [0, 1] Fixed-point: [0, 1, 8]
15:8	RW	0x09	sw_hist_count_offset Hist noise count offset. Range: [0, 255] Fixed-point: [0, 8, 0]
7:5	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
4:0	RW	0x08	sw_hist_count_scale Hist noise count scale. Range: [0, 7] Fixed-point: [0, 3, 2]

ISP_HIST_3C00_BLOCK_SIZE

Address: Operational Base(0x21D03C00) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x040	sw_hist_blk_wid Hist block width, it has to be even, width=ceil(pic_width/sw_hist_thumb_col). Note: Maximum block width=4672/4=1168, so 66<=blk_wid<=1168. 4672 is maximum picture width for 4K, 4 is minimum sw_hist_thumb_col. The rightmost block must be less than or equal to sw_hist_blk_wid.
15:10	RO	0x00	reserved
9:0	RW	0x040	sw_hist_blk_het Hist block height, it has to be even, height=ceil(pic_height/sw_hist_thumb_row). Note: Maximum block height=3504/4=876, so 64<=blk_het<=876. The bottom block must be less than or equal to sw_hist_blk_het.

ISP_HIST_3C00_THUMB_SIZE

Address: Operational Base(0x21D03C00) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:8	RW	0x08	sw_hist_thumb_col Hist thumb col, it has to be even. Note: The configuration parameter is {4, 6, 8, 10}.
7:5	RO	0x0	reserved
4:0	RW	0x08	sw_hist_thumb_row Hist thumb row, it has to be even. Note: The configuration parameter is {4, 6, 8}.

ISP_HIST_3C00_HIST_MAP0

Address: Operational Base(0x21D03C00) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x033	sw_hist_user_set Hist map user set. Range: [0, 1] Fixed-point: [0, 1, 8]
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_hist_merge_alpha Hist map merge alpha. Range: [0, 1] Fixed-point: [0, 1, 8]

ISP_HIST_3C00_HIST_MAP1

Address: Operational Base(0x21D03C00) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
21:16	RW	0x00	sw_hist_gain_ref_wgt Hist map gain reference weight Range: [0, 0.99] Fixed-point: [0, 0, 6]
15:9	RO	0x00	reserved
8:0	RW	0x080	sw_hist_map_count_scale Hist map count scale Range: [0, 1] Fixed-point: [0, 1, 8]

ISP_HIST_3C00_IIR

Address: Operational Base(0x21D03C00) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:16	RW	0x8	sw_hist_flt_cur_wgt Hist iir filter cur weight. Range: [1, 15]
15:9	RO	0x00	reserved
8:0	RW	0x001	sw_hist_flt_inv_sigma Hist iir filter 1/sigma. Range: [0, 1] Fixed-point: [0, 1, 8]

ISP_HIST_3C00_POS_ALPHA0

Address: Operational Base(0x21D03C00) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:24	RW	0x20	sw_hist_pos_alpha3 Hist posedge alpha 3 of output merge. Range: [0, 3.99] Fixed-point: [0, 2, 6]
23:16	RW	0x00	sw_hist_pos_alpha2 Hist posedge alpha 2 of output merge. Range: [0, 3.99] Fixed-point: [0, 2, 6]
15:8	RW	0x20	sw_hist_pos_alpha1 Hist posedge alpha 1 of output merge. Range: [0, 3.99] Fixed-point: [0, 2, 6]
7:0	RW	0x20	sw_hist_pos_alpha0 Hist posedge alpha 0 of output merge. Range: [0, 3.99] Fixed-point: [0, 2, 6]

ISP_HIST_3C00_POS_ALPHA1

Address: Operational Base(0x21D03C00) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:24	RW	0x20	sw_hist_pos_alpha7 Hist posedge alpha 7 of output merge. Range: [0, 3.99] Fixed-point: [0, 2, 6]
23:16	RW	0x20	sw_hist_pos_alpha6 Hist posedge alpha 6 of output merge. Range: [0, 3.99] Fixed-point: [0, 2, 6]

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Bit	Attr	Reset Value	Description
15:8	RW	0x20	sw_hist_pos_alpha5 Hist posedge alpha 5 of output merge. Range: [0, 3.99] Fixed-point: [0, 2, 6]
7:0	RW	0x20	sw_hist_pos_alpha4 Hist posedge alpha 4 of output merge. Range: [0, 3.99] Fixed-point: [0, 2, 6]

ISP_HIST_3C00_POS_ALPHA2

Address: Operational Base(0x21D03C00) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:24	RW	0x20	sw_hist_pos_alpha11 Hist posedge alpha 11 of output merge. Range: [0, 3.99] Fixed-point: [0, 2, 6]
23:16	RW	0x20	sw_hist_pos_alpha10 Hist posedge alpha 10 of output merge. Range: [0, 3.99] Fixed-point: [0, 2, 6]
15:8	RW	0x20	sw_hist_pos_alpha9 Hist posedge alpha 8 of output merge. Range: [0, 3.99] Fixed-point: [0, 2, 6]
7:0	RW	0x20	sw_hist_pos_alpha8 Hist posedge alpha 8 of output merge. Range: [0, 3.99] Fixed-point: [0, 2, 6]

ISP_HIST_3C00_POS_ALPHA3

Address: Operational Base(0x21D03C00) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:24	RW	0x20	sw_hist_pos_alpha15 Hist posedge alpha 15 of output merge. Range: [0, 3.99] Fixed-point: [0, 2, 6]
23:16	RW	0x20	sw_hist_pos_alpha14 Hist posedge alpha 14 of output merge. Range: [0, 3.99] Fixed-point: [0, 2, 6]
15:8	RW	0x20	sw_hist_pos_alpha13 Hist posedge alpha 13 of output merge. Range: [0, 3.99] Fixed-point: [0, 2, 6]
7:0	RW	0x20	sw_hist_pos_alpha12 Hist posedge alpha 12 of output merge. Range: [0, 3.99] Fixed-point: [0, 2, 6]

ISP_HIST_3C00_POS_ALPHA4

Address: Operational Base(0x21D03C00) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x20	sw_hist_pos_alpha16 Hist posedge alpha 16 of output merge. Range: [0, 3.99] Fixed-point: [0, 2, 6]

ISP_HIST_3C00_NEG_ALPHA0

Address: Operational Base(0x21D03C00) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:24	RW	0x20	sw_hist_neg_alpha3 Hist negative alpha 3 of output merge. Range: [0, 3.99] Fixed-point: [0, 2, 6]
23:16	RW	0x20	sw_hist_neg_alpha2 Hist negative alpha 2 of output merge. Range: [0, 3.99] Fixed-point: [0, 2, 6]
15:8	RW	0x20	sw_hist_neg_alpha1 Hist negative alpha 1 of output merge. Range: [0, 3.99] Fixed-point: [0, 2, 6]
7:0	RW	0x20	sw_hist_neg_alpha0 Hist negative alpha 0 of output merge. Range: [0, 3.99] Fixed-point: [0, 2, 6]

ISP_HIST_3C00_NEG_ALPHA1

Address: Operational Base(0x21D03C00) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:24	RW	0x20	sw_hist_neg_alpha7 Hist negative alpha 7 of output merge. Range: [0, 3.99] Fixed-point: [0, 2, 6]
23:16	RW	0x20	sw_hist_neg_alpha6 Hist negative alpha 6 of output merge. Range: [0, 3.99] Fixed-point: [0, 2, 6]
15:8	RW	0x20	sw_hist_neg_alpha5 Hist negative alpha 5 of output merge. Range: [0, 3.99] Fixed-point: [0, 2, 6]
7:0	RW	0x20	sw_hist_neg_alpha4 Hist negative alpha 4 of output merge. Range: [0, 3.99] Fixed-point: [0, 2, 6]

ISP_HIST_3C00_NEG_ALPHA2

Address: Operational Base(0x21D03C00) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:24	RW	0x20	sw_hist_neg_alpha11 Hist negative alpha 11 of output merge. Range: [0, 3.99] Fixed-point: [0, 2, 6]

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Bit	Attr	Reset Value	Description
23:16	RW	0x20	sw_hist_neg_alpha10 Hist negative alpha 10 of output merge. Range: [0, 3.99] Fixed-point: [0, 2, 6]
15:8	RW	0x20	sw_hist_neg_alpha9 Hist negative alpha 9 of output merge. Range: [0, 3.99] Fixed-point: [0, 2, 6]
7:0	RW	0x20	sw_hist_neg_alpha8 Hist negative alpha 8 of output merge. Range: [0, 3.99] Fixed-point: [0, 2, 6]

ISP_HIST_3C00_NEG_ALPHA3

Address: Operational Base(0x21D03C00) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:24	RW	0x20	sw_hist_neg_alpha15 Hist negative alpha 15 of output merge. Range: [0, 3.99] Fixed-point: [0, 2, 6]
23:16	RW	0x20	sw_hist_neg_alpha14 Hist negative alpha 14 of output merge. Range: [0, 3.99] Fixed-point: [0, 2, 6]
15:8	RW	0x20	sw_hist_neg_alpha13 Hist negative alpha 13 of output merge. Range: [0, 3.99] Fixed-point: [0, 2, 6]
7:0	RW	0x20	sw_hist_neg_alpha12 Hist negative alpha 12 of output merge. Range: [0, 3.99] Fixed-point: [0, 2, 6]

ISP_HIST_3C00_NEG_ALPHA4

Address: Operational Base(0x21D03C00) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x20	sw_hist_neg_alpha16 Hist negative alpha 16 of output merge. Range: [0, 3.99] Fixed-point: [0, 2, 6]

ISP_HIST_3C00_HIST_IIR0

Address: Operational Base(0x21D03C00) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_hist_iir1 Block hist iir data1.
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_hist_iir0 Block hist iir data0.

ISP_HIST_3C00_HIST_IIR1

Address: Operational Base(0x21D03C00) + offset (0x0084)

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Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_hist_iir3 Block hist iir data3.
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_hist_iir2 Block hist iir data2.

ISP_HIST_3C00_HIST_IIR2

Address: Operational Base(0x21D03C00) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_hist_iir5 Block hist iir data5.
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_hist_iir4 Block hist iir data4.

ISP_HIST_3C00_HIST_IIR3

Address: Operational Base(0x21D03C00) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_hist_iir7 Block hist iir data7.
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_hist_iir6 Block hist iir data6.

ISP_HIST_3C00_HIST_IIR4

Address: Operational Base(0x21D03C00) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_hist_iir9 Block hist iir data9.
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_hist_iir8 Block hist iir data8.

ISP_HIST_3C00_HIST_IIR5

Address: Operational Base(0x21D03C00) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_hist_iir11 Block hist iir data11.
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_hist_iir10 Block hist iir data10.

ISP_HIST_3C00_HIST_IIR6

Address: Operational Base(0x21D03C00) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_hist_iir13 Block hist iir data13.
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	sw_hist_iir12 Block hist iir data12.

ISP_HIST_3C00_HIST_IIR7

Address: Operational Base(0x21D03C00) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_hist_iir15 Block hist iir data15.
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_hist_iir14 Block hist iir data14.

ISP_HIST_3C00_HIST_RW

Address: Operational Base(0x21D03C00) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	W1C	0x0	sys_hist_iir_wr_clear Hist iir memory write clear pluse.
23:16	RW	0x00	sw_hist_iir_wr_id Hist iir memory write index, index=blk_row_id*sw_dhaz_thumb_col+blk_col_id, use for 8K thumb boundary iir data. Range: [0, 255] Fixed-poiot: [0, 8, 0]
15:10	RO	0x00	reserved
9	RO	0x0	ro_iir_rdata_val Hist iir memory read data valid. 1'b0: sw_hist_iir0 ~ ro_iir_data15 invalid and sys_iir_rd_p can not be configured 1'b1: ro_iir_data0 ~ ro_iir_data15 valid
8	W1C	0x0	sys_hist_iir_rd_p Hist iir memory read pluse, if ro_iir_rdata_val is 0, the iir memory is busy, can not be configured sys_iir_rd_p, if ro_iir_rdata_val is 1, the iir memory is idle, sys_iir_rd_p can be configured.
7:0	RW	0x00	sw_hist_iir_rd_id Hist iir memory read index, index=blk_row_id*sw_dhaz_thumb_col+blk_col_id, use for 8K thumb boundary iir data. Range: [0, 255] Fixed-poiot: [0, 8, 0]

ISP_HIST_3C00_HIST_STAB

Address: Operational Base(0x21D03C00) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x1	stab_frame_cnt1 stab_frame_cnt of sensor 1
3:0	RW	0x1	stab_frame_cnt0 stab_frame_cnt of sensor 0

ISP_HIST_3C00_HIST_UV_SCL

Address: Operational Base(0x21D03C00) + offset (0x00A8)

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Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x20	sw_hist_saturate_scale Hist gain scale of saturate. Range: [0, 7.99] Fixed-point: [0, 3, 5]

ISP_HIST_3C00_ERR_FLAG

Address: Operational Base(0x21D03C00) + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RO	0x0	ro_lf_fifo_full_err ro_lf_fifo_full_err flag.

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ISP_ENH_3A00_CTRL

Address: Operational Base(0x21D03A00) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	W1C	0x0	sys_itself_force_upd Cac itself force update
30	RW	0x0	sw_enh_bypass_shd Shadow of sw_enh_bypass. 1'b0: Disable 1'b1: Enable
29	RW	0x0	sw_enh_blf3_bypass_shd Shadow of sw_enh_blf3_bypass. 1'b0: Disable 1'b1: Enable
28:17	RO	0x000	reserved
16	RW	0x0	enh_working Enhance working. 1'b0: Closed 1'b1: Working
15:13	RO	0x0	reserved
12:8	RW	0x02	sw_enh_scl_het Enhance scale_height=ceil(pic_height/129)
7:6	RO	0x0	reserved
5:4	RW	0x0	sw_enh_het_aliquant The remainder of the image height divided by 3. 2'b00: The remainder is 0 2'b01: The remainder is 1 2'b10: The remainder is 2 2'b11: Reserved
3	RW	0x0	sw_enh_ckg_dis Enhance clock gating. 1'b0: Gating enable 1'b1: Gating disable
2	RW	0x0	hw_enh_blf3_bypass Contrast bilateral filter 3x3 bypass. 1'b0: Disable 1'b1: Enable
1	RW	0x0	hw_enh_bypass 1'b0: Disable 1'b1: Enable

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Bit	Attr	Reset Value	Description
0	RW	0x0	hw_enh_en 1'b0: Disable 1'b1: Enable

ISP_ENH_3A00_IIR_FLT

Address: Operational Base(0x21D03A00) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x0d	hw_enh_iir_cur_wgt Contrast iir filter current weight. Range: [0, 1] Fixed-point: [0, 1, 5]
23:21	RO	0x0	reserved
20:16	RW	0x05	hw_enh_iir_soft_thed Contrast iir filter soft threshold. Range: [0, 31]
15:9	RO	0x00	reserved
8:0	RW	0x040	hw_enh_iir_inv_sigma Contrast iir filter 1/sigma. Range: [0, 1] Fixed-point: [0, 1, 8]

ISP_ENH_3A00_BILAT_FLT3X3

Address: Operational Base(0x21D03A00) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:28	RW	0x4	hw_enh_blf3_thumb_cur_wgt Contrast bilateral filter 3x3 thumb filter current weight. Range: [1, 15]
27:25	RO	0x0	reserved
24:16	RW	0x080	hw_enh_blf3_cur_wgt Contrast bilateral filter 3x3 current weight. Range: [0, 1] Fixed-point: [0, 1, 8]
15:9	RO	0x00	reserved
8:0	RW	0x00c	hw_enh_blf3_inv_sigma Contrast bilateral filter 3x3 1/sigma. Range: [0, 1] Fixed-point: [0, 1, 8]

ISP_ENH_3A00_BILAT_FLT5X5

Address: Operational Base(0x21D03A00) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x05	hw_enh_blf5_cur_wgt Contrast bilateral filter 5x5 current weight. Range: [0, 1] Fixed-point: [0, 1, 5]
15:9	RO	0x00	reserved
8:0	RW	0x00a	hw_enh_blf5_inv_sigma Contrast bilateral filter 5x5 1/sigma. Range: [0, 1] Fixed-point: [0, 1, 8]

ISP_ENH_3A00_GLOBAL_STRG

Address: Operational Base(0x21D03A00) + offset (0x0010)

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Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0600	hw_enh_global_strg Contrast global strength. Range: [0, 15.99] Fixed-point: [0, 4, 10]

ISP_ENH_3A00_LUMA_LUT0

Address: Operational Base(0x21D03A00) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x400	hw_enh_lum2strg1 Contrast luma to strength 1. Range: [0, 1] Fixed-point: [0, 1, 10]
15:11	RO	0x00	reserved
10:0	RW	0x400	hw_enh_lum2strg0 Contrast luma to strength 0. Range: [0, 1] Fixed-point: [0, 1, 10]

ISP_ENH_3A00_LUMA_LUT1

Address: Operational Base(0x21D03A00) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x400	hw_enh_lum2strg3 Contrast luma to strength 3. Range: [0, 1] Fixed-point: [0, 1, 10]
15:11	RO	0x00	reserved
10:0	RW	0x400	hw_enh_lum2strg2 Contrast luma to strength 2. Range: [0, 1] Fixed-point: [0, 1, 10]

ISP_ENH_3A00_LUMA_LUT2

Address: Operational Base(0x21D03A00) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x400	hw_enh_lum2strg5 Contrast luma to strength 5. Range: [0, 1] Fixed-point: [0, 1, 10]
15:11	RO	0x00	reserved
10:0	RW	0x400	hw_enh_lum2strg4 Contrast luma to strength 4. Range: [0, 1] Fixed-point: [0, 1, 10]

ISP_ENH_3A00_LUMA_LUT3

Address: Operational Base(0x21D03A00) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
26:16	RW	0x400	hw_enh_lum2strg7 Contrast luma to strength 7. Range: [0, 1] Fixed-point: [0, 1, 10]
15:11	RO	0x00	reserved
10:0	RW	0x400	hw_enh_lum2strg6 Contrast luma to strength 6. Range: [0, 1] Fixed-point: [0, 1, 10]

ISP_ENH_3A00_LUMA_LUT4

Address: Operational Base(0x21D03A00) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x400	hw_enh_lum2strg9 Contrast luma to strength 9. Range: [0, 1] Fixed-point: [0, 1, 10]
15:11	RO	0x00	reserved
10:0	RW	0x400	hw_enh_lum2strg8 Contrast luma to strength 8. Range: [0, 1] Fixed-point: [0, 1, 10]

ISP_ENH_3A00_LUMA_LUT5

Address: Operational Base(0x21D03A00) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x400	hw_enh_lum2strg11 Contrast luma to strength 11. Range: [0, 1] Fixed-point: [0, 1, 10]
15:11	RO	0x00	reserved
10:0	RW	0x400	hw_enh_lum2strg10 Contrast luma to strength 10. Range: [0, 1] Fixed-point: [0, 1, 10]

ISP_ENH_3A00_LUMA_LUT6

Address: Operational Base(0x21D03A00) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x400	hw_enh_lum2strg13 Contrast luma to strength 13. Range: [0, 1] Fixed-point: [0, 1, 10]
15:11	RO	0x00	reserved
10:0	RW	0x400	hw_enh_lum2strg12 Contrast luma to strength 12. Range: [0, 1] Fixed-point: [0, 1, 10]

ISP_ENH_3A00_LUMA_LUT7

Address: Operational Base(0x21D03A00) + offset (0x0030)

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Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x400	hw_enh_lum2strg15 Contrast luma to strength 15. Range: [0, 1] Fixed-point: [0, 1, 10]
15:11	RO	0x00	reserved
10:0	RW	0x400	hw_enh_lum2strg14 Contrast luma to strength 14. Range: [0, 1] Fixed-point: [0, 1, 10]

ISP_ENH_3A00_LUMA_LUT8

Address: Operational Base(0x21D03A00) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x400	hw_enh_lum2strg16 Contrast luma to strength 16. Range: [0, 1] Fixed-point: [0, 1, 10]

ISP_ENH_3A00_DETAIL_IDX0

Address: Operational Base(0x21D03A00) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x020	hw_enh_detail2strg_idx2 Contrast detail to strength index 2. Range: [0, 1023]
19:10	RW	0x010	hw_enh_detail2strg_idx1 Contrast detail to strength index 1. Range: [0, 1023]
9:0	RW	0x008	hw_enh_detail2strg_idx0 Contrast detail to strength index 0. Range: [0, 1023]

ISP_ENH_3A00_DETAIL_IDX1

Address: Operational Base(0x21D03A00) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x100	hw_enh_detail2strg_idx5 Contrast detail to strength index 5. Range: [0, 1023]
19:10	RW	0x080	hw_enh_detail2strg_idx4 Contrast detail to strength index 4. Range: [0, 1023]
9:0	RW	0x040	hw_enh_detail2strg_idx3 Contrast detail to strength index 3. Range: [0, 1023]

ISP_ENH_3A00_DETAIL_IDX2

Address: Operational Base(0x21D03A00) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:10	RW	0x400	hw_enh_detail2strg_idx7 Contrast detail to strength index 7. Range: [0, 1024]

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Bit	Attr	Reset Value	Description
9:0	RW	0x200	hw_enh_detail2strg_idx6 Contrast detail to strength index 6. Range: [0, 1023]

ISP_ENH_3A00_DETAIL_POWER

Address: Operational Base(0x21D03A00) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	hw_enh_detail2strg_power6 Contrast detail to strength power 6. Range: [0, 10]
23:20	RW	0x0	hw_enh_detail2strg_power5 Contrast detail to strength power 5. Range: [0, 10]
19:16	RW	0x0	hw_enh_detail2strg_power4 Contrast detail to strength power 4. Range: [0, 10]
15:12	RW	0x0	hw_enh_detail2strg_power3 Contrast detail to strength power 3. Range: [0, 10]
11:8	RW	0x0	hw_enh_detail2strg_power2 Contrast detail to strength power 2. Range: [0, 10]
7:4	RW	0x0	hw_enh_detail2strg_power1 Contrast detail to strength power 1. Range: [0, 10]
3:0	RW	0x0	hw_enh_detail2strg_power0 Contrast detail to strength power 0. Range: [0, 10]

ISP_ENH_3A00_DETAIL_VALUE0

Address: Operational Base(0x21D03A00) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x400	hw_enh_detail2strg_val1 Contrast detail to strength value 1. Range: [0, 1] Fixed-point: [0, 1, 10]
15:11	RO	0x00	reserved
10:0	RW	0x400	hw_enh_detail2strg_val0 Contrast detail to strength value 0. Range: [0, 1] Fixed-point: [0, 1, 10]

ISP_ENH_3A00_DETAIL_VALUE1

Address: Operational Base(0x21D03A00) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x400	hw_enh_detail2strg_val3 Contrast detail to strength value 3. Range: [0, 1] Fixed-point: [0, 1, 10]
15:11	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
10:0	RW	0x400	hw_enh_detail2strg_val2 Contrast detail to strength value 2. Range: [0, 1] Fixed-point: [0, 1, 10]

ISP_ENH_3A00_DETAIL_VALUE2

Address: Operational Base(0x21D03A00) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x400	hw_enh_detail2strg_val5 Contrast detail to strength value 5. Range: [0, 1] Fixed-point: [0, 1, 10]
15:11	RO	0x00	reserved
10:0	RW	0x400	hw_enh_detail2strg_val4 Contrast detail to strength value 4. Range: [0, 1] Fixed-point: [0, 1, 10]

ISP_ENH_3A00_DETAIL_VALUE3

Address: Operational Base(0x21D03A00) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x400	hw_enh_detail2strg_val7 Contrast detail to strength value 7. Range: [0, 1] Fixed-point: [0, 1, 10]
15:11	RO	0x00	reserved
10:0	RW	0x400	hw_enh_detail2strg_val6 Contrast detail to strength value 6. Range: [0, 1] Fixed-point: [0, 1, 10]

ISP_ENH_3A00_PRE_FRAME

Address: Operational Base(0x21D03A00) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x1	pre_wet_frame_cnt1 pre_wet_frame_cnt of sensor 1
3:0	RW	0x1	pre_wet_frame_cnt0 pre_wet_frame_cnt of sensor 0

ISP_ENH_3A00_IIR0

Address: Operational Base(0x21D03A00) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_enh_iir3 Enhance down scale iir data3.
23:16	RW	0x00	sw_enh_iir2 Enhance down scale iir data2.
15:8	RW	0x00	sw_enh_iir1 Enhance down scale iir data1.
7:0	RW	0x00	sw_enh_iir0 Enhance down scale iir data0.

ISP_ENH_3A00_IIR1

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Address: Operational Base(0x21D03A00) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_enh_iir7 Enhance down scale iir data7.
23:16	RW	0x00	sw_enh_iir6 Enhance down scale iir data6.
15:8	RW	0x00	sw_enh_iir5 Enhance down scale iir data5.
7:0	RW	0x00	sw_enh_iir4 Enhance down scale iir data4.

ISP_ENH_3A00_IIR2

Address: Operational Base(0x21D03A00) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_enh_iir11 Enhance down scale iir data11.
23:16	RW	0x00	sw_enh_iir10 Enhance down scale iir data10.
15:8	RW	0x00	sw_enh_iir9 Enhance down scale iir data9.
7:0	RW	0x00	sw_enh_iir8 Enhance down scale iir data8.

ISP_ENH_3A00_IIR3

Address: Operational Base(0x21D03A00) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_enh_iir15 Enhance down scale iir data15.
23:16	RW	0x00	sw_enh_iir14 Enhance down scale iir data14.
15:8	RW	0x00	sw_enh_iir13 Enhance down scale iir data13.
7:0	RW	0x00	sw_enh_iir12 Enhance down scale iir data12.

ISP_ENH_3A00_IIR4

Address: Operational Base(0x21D03A00) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_enh_iir19 Enhance down scale iir data19.
23:16	RW	0x00	sw_enh_iir18 Enhance down scale iir data18.
15:8	RW	0x00	sw_enh_iir17 Enhance down scale iir data17.
7:0	RW	0x00	sw_enh_iir16 Enhance down scale iir data16.

ISP_ENH_3A00_IIR5

Address: Operational Base(0x21D03A00) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_enh_iir23 Enhance down scale iir data23.
23:16	RW	0x00	sw_enh_iir22 Enhance down scale iir data22.
15:8	RW	0x00	sw_enh_iir21 Enhance down scale iir data21.

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	sw_enh_iir20 Enhance down scale iir data20.

ISP_ENH_3A00_IIR6

Address: Operational Base(0x21D03A00) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_enh_iir27 Enhance down scale iir data27.
23:16	RW	0x00	sw_enh_iir26 Enhance down scale iir data26.
15:8	RW	0x00	sw_enh_iir25 Enhance down scale iir data25.
7:0	RW	0x00	sw_enh_iir24 Enhance down scale iir data24.

ISP_ENH_3A00_IIR7

Address: Operational Base(0x21D03A00) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_enh_iir31 Enhance down scale iir data31.
23:16	RW	0x00	sw_enh_iir30 Enhance down scale iir data30.
15:8	RW	0x00	sw_enh_iir29 Enhance down scale iir data29.
7:0	RW	0x00	sw_enh_iir28 Enhance down scale iir data28.

ISP_ENH_3A00_IIR8

Address: Operational Base(0x21D03A00) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_enh_iir35 Enhance down scale iir data35.
23:16	RW	0x00	sw_enh_iir34 Enhance down scale iir data34.
15:8	RW	0x00	sw_enh_iir33 Enhance down scale iir data33.
7:0	RW	0x00	sw_enh_iir32 Enhance down scale iir data32.

ISP_ENH_3A00_IIR9

Address: Operational Base(0x21D03A00) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	sw_enh_iir36 Enhance down scale iir data36.

ISP_ENH_3A00_IIR_RW

Address: Operational Base(0x21D03A00) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	sys_enh_iir_wr_clear Enhance iir memory write clear pluse.
23:22	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
21:16	RW	0x00	sw_enh_iir_wr_row Hist iir memory write row. Range: [0, 12]
15:10	RO	0x00	reserved
9	RW	0x0	ro_iir_rdata_val Enhance iir memory read data valid. 1'b0: sw_enh_iir0 ~ sw_enh_iir36 invalid and sys_enh_iir_rd_p can not be configured 1'b1: sw_enh_iir0 ~ sw_enh_iir36 valid
8	W1C	0x0	sys_enh_iir_rd_p Enhance iir memory read pluse, if ro_iir_rdata_val is 0, the iir memory is busy, can not be configured sys_enh_iir_rd_p, if ro_iir_rdata_val is 1, the iir memory is idle, sys_enh_iir_rd_p can be configured.
7:6	RO	0x0	reserved
5:0	RW	0x00	sw_enh_iir_rd_row Enhance iir memory read row. Range: [0, 12]

ISP_ENH_3A00_ERR_FLAG

Address: Operational Base(0x21D03A00) + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8	RO	0x0	ro_hi_in_ack_err ro_hi_in_ack_err flag.
7	RO	0x0	ro_ynr_fifo_full_err ro_ynr_fifo_full_err flag.
6	RO	0x0	ro_blf5_fifo_full_err ro_blf5_fifo_full_err flag.
5	RO	0x0	ro_hi_fifo_full_err ro_hi_fifo_full_err flag.
4	RO	0x0	ro_blf3_fifo_full_err ro_blf3_fifo_full_err flag.
3	RO	0x0	ro_iir_fifo_full_err ro_iir_fifo_full_err flag.
2	RO	0x0	ro_ds4_fifo_full_err ro_ds4_fifo_full_err flag.
1	RO	0x0	ro_ds128_fifo_full_err ro_ds128_fifo_full_err flag.
0	RO	0x0	ro_hi_in_ack ro_hi_in_ack

44.4.2.20 HSV

ISP_HSV_3E00_CTRL

Address: Operational Base(0x21D03E00) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	sys_itself_force_upd 1'b1: itself update for hsv to update shadow register. The signal will be auto clear after cfg_wr for one cycle.
30	RW	0x0	sys_hsv_tbl_clr_p Auto clr, clr all lut cfg ctrl register.
29	RW	0x0	sys_hsv_soft_rst_p Auto clr, hsv itself soft rst.

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Bit	Attr	Reset Value	Description
28:26	RO	0x0	reserved
25:24	RW	0x0	sys_itself_lut_mode Lut update mode 2'b00: Open frame_end and force update load lut mode 2'b11: soft control force update load lut mode Suggest use force-upd load lut mode.
23:12	RO	0x000	reserved
11	RW	0x0	sw_hsv_gate_dis 1'b0: Hsv clk gate is enable 1'b1: Hsv clk gate is disable
10	RW	0x0	sys_hsv_lut_dbg_rd_p Auto clr, the pulse can readback LUT through ahb.
9	RW	0x0	sw_hsv_ahb_cfg_lut_en 1'b0: Hsv ahb addr mapping cfg lut is disable 1'b1: Hsv ahb addr mapping cfg lut is enable
8	RW	0x0	sw_hsv_fix_rw_conflict 1'b0: Hsv lut rd has higher priority than lut wr 1'b1: Hsv lut wr has higher priority than lut rd
7	RO	0x0	reserved
6	RW	0x0	sw_hsv_2dlut12_cfg_en 1'b0: 2dlut12 config is disable 1'b1: 2dlut12 config is enable
5	RW	0x0	sw_hsv_2dlut2_en 1'b0: 2dlut2 module is disable 1'b1: 2dlut2 module is enable
4	RW	0x0	sw_hsv_2dlut1_en 1'b0: 2dlut1 module is disable 1'b1: 2dlut1 module is enable
3	RW	0x1	sw_hsv_2dlut0_en 1'b0: 2dlut0 module is disable 1'b1: 2dlut0 module is enable
2	RW	0x1	sw_hsv_1dlut1_en 1'b0: 1dlut1 module is disable 1'b1: 1dlut1 module is enable
1	RW	0x1	sw_hsv_1dlut0_en 1'b0: 1dlut0 module is disable 1'b1: 1dlut0 module is enable
0	RW	0x0	sw_hsv_en 1'b0: Module is disable 1'b1: Module is enable

ISP_HSV_3E00_MODE_CTRL

Address: Operational Base(0x21D03E00) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:20	RW	0x1	sw_hsv_2dlut2_item_mode 2'b00: h_out = 2dlut2_out 2'b01: s_out = 2dlut2_out 2'b10: v_out = 2dlut2_out
19:18	RW	0x0	sw_hsv_2dlut1_item_mode 2'b00: h_out = 2dlut1_out 2'b01: s_out = 2dlut1_out 2'b10: v_out = 2dlut1_out

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Bit	Attr	Reset Value	Description
17:16	RW	0x2	sw_hsv_2dlut0_item_mode 2'b00: h_out = 2dlut0_out 2'b01: s_out = 2dlut0_out 2'b10: v_out = 2dlut0_out
15:13	RW	0x4	sw_hsv_1dlut1_item_mode 3'b000: h_out = (h_in + 1dlut1_out) 3'b001: s_out = (s_in + 1dlut1_out) 3'b010: v_out = (v_in + 1dlut1_out) 3'b011: h_out = 1dlut1_out 3'b100: s_out = 1dlut1_out 3'b101: v_out = 1dlut1_out
12:10	RW	0x3	sw_hsv_1dlut0_item_mode 3'b000: h_out = (h_in + 1dlut0_out) 3'b001: s_out = (s_in + 1dlut0_out) 3'b010: v_out = (v_in + 1dlut0_out) 3'b011: h_out = 1dlut0_out 3'b100: s_out = 1dlut0_out 3'b101: v_out = 1dlut0_out
9:8	RW	0x1	sw_hsv_2dlut2_idx_mode 2'b00: 2dlut2 module input is h and s 2'b01: 2dlut2 module input is h and v 2'b10: 2dlut2 module input is s and v
7:6	RW	0x0	sw_hsv_2dlut1_idx_mode 2'b00: 2dlut1 module input is h and s 2'b01: 2dlut1 module input is h and v 2'b10: 2dlut1 module input is s and v
5:4	RW	0x2	sw_hsv_2dlut0_idx_mode 2'b00: 2dlut0 module input is h and s 2'b01: 2dlut0 module input is h and v 2'b10: 2dlut0 module input is s and v
3:2	RW	0x1	sw_hsv_1dlut1_idx_mode 2'b00: 1dlut1 module input is h 2'b01: 1dlut1 module input is s 2'b10: 1dlut1 module input is v
1:0	RW	0x0	sw_hsv_1dlut0_idx_mode 2'b00: 1dlut0 module input is h 2'b01: 1dlut0 module input is s 2'b10: 1dlut0 module input is v

ISP_HSV_3E00_UPDATE

Address: Operational Base(0x21D03E00) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	sw_hsv_lut_update_en HSV lut update pulse signal: 1'b0: Disable 1'b1: Enable

ISP_HSV_3E00_HSV_1DLUT_CFG

Address: Operational Base(0x21D03E00) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	reserved

ISP_HSV_3E00_HSV_2DLUT0_CFG

Address: Operational Base(0x21D03E00) + offset (0x0010)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	reserved

ISP_HSV_3E00_HSV_2DLUT1_CFG

Address: Operational Base(0x21D03E00) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	reserved

ISP_HSV_3E00_HSV_2DLUT2_CFG

Address: Operational Base(0x21D03E00) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	reserved

ISP_HSV_3E00_HSV_DBG0

Address: Operational Base(0x21D03E00) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	ro_hsv_dbg0 HSV debug messge0.

ISP_HSV_3E00_HSV_DBG1

Address: Operational Base(0x21D03E00) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	ro_hsv_dbg1 HSV debug messge1.

ISP_HSV_3E00_HSV_DBG2

Address: Operational Base(0x21D03E00) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	ro_hsv_dbg2 HSV debug messge2.

ISP_HSV_3E00_HSV_DBG3

Address: Operational Base(0x21D03E00) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	ro_hsv_dbg3 HSV debug messge3.

ISP_HSV_3E00_HSV_DBG_LUT

Address: Operational Base(0x21D03E00) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	ro_hsv_dbg_lut HSV debug read back LUT value.

44.4.2.21 YNR

YNR_2700_GLOBAL_CTRL

Address: Operational Base(0x21D02700) + offset (0x0000)

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Bit	Attr	Reset Value	Description
31	RO	0x0	ro_ynr_en_shd YNR enable shadow bit.
30	RO	0x0	ro_gain_en_shd GAIN enable shadow bit.
29	RO	0x0	ro_ynr_hiSpnr_bypass_shd YNR high frequency filter bypass shadow bit.
28	RO	0x0	ro_ynr_miSpnr_bypass_shd YNR middle frequency filter bypass shadow bit.
27	RW	0x0	ro_ynr_loSpnr_bypass_shd YNR low frequency bypass enable shadow bit
26	RO	0x0	reserved
25	RW	0x0	ro_ynr_text2loStrg_shd Shp2ynr text enable shadow bit.
24:21	RO	0x0	reserved
20	RO	0x0	ro_fifo_overflow FIFO overflow debug signal.
19:16	RO	0x0	reserved
15	RW	0x0	hw_ynr_gate_dis A backdoor for YNR internal gating
14:9	RO	0x00	reserved
8	RW	0x0	hw_ynr_tex2wgt_en Text2weight text enable bit
7	RW	0x0	hw_ynr_dsfilt_bypass YNR downsample iir filter bypass bit
6	RW	0x0	hw_ynr_hi_lp_en Low power mode 1'b1: Disable part of non-local means. 1'b0: Enable all non-local means.
5	RW	0x1	hw_ynr_tex2loStrg_en Shp2ynr text enable bit
4	RW	0x1	hw_ynr_rnr_en RNR enable bit
3	RW	0x0	hw_ynr_loSpnr_bypass YNR low frequency filter bypass bit
2	RW	0x0	hw_ynr_miSpnr_bypass YNR middle frequency filter bypass bit
1	RW	0x0	hw_ynr_hiSpnr_bypass YNR high frequency filter bypass bit
0	RW	0x0	hw_ynr_en YNR enable bit

YNR_2700_GAIN_CTRL

Address: Operational Base(0x21D02700) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x80	hw_ynr_localGain_scale 1 bit integer and 7 bit fraction, for localgain/iso.
15:12	RW	0x8	hw_ynr_gainMerge_alpha Global gain alpha for YNR {1i,3f} data range:[0,8]. Gain = (sw_ynr_global_gain_alpha * sw_ynr_global_gain + (8-sw_ynr_global_gain_alpha)*local_gain)>>3
11:10	RO	0x0	reserved
9:0	RW	0x010	hw_ynr_globalSet_gain Global gain for YNR ({6i,4f})

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YNR_2700_GAIN_ADJ_0_2

Address: Operational Base(0x21D02700) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:20	RW	0x010	hw_ynr_loSpnrGain2Strg_val2 gain2strength for low-NR, 5 bit integer and 4 bit fraction
19	RO	0x0	reserved
18:10	RW	0x010	hw_ynr_loSpnrGain2Strg_val1 gain2strength for low-NR, 5 bit integer and 4 bit fraction
9	RO	0x0	reserved
8:0	RW	0x010	hw_ynr_loSpnrGain2Strg_val0 gain2strength for low-NR, 5 bit integer and 4 bit fraction

YNR_2700_GAIN_ADJ_3_5

Address: Operational Base(0x21D02700) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:20	RW	0x010	hw_ynr_loSpnrGain2Strg_val5 gain2strength for low-NR, 5 bit integer and 4 bit fraction
19	RO	0x0	reserved
18:10	RW	0x010	hw_ynr_loSpnrGain2Strg_val4 gain2strength for low-NR, 5 bit integer and 4 bit fraction
9	RO	0x0	reserved
8:0	RW	0x010	hw_ynr_loSpnrGain2Strg_val3 gain2strength for low-NR, 5 bit integer and 4 bit fraction

YNR_2700_GAIN_ADJ_6_8

Address: Operational Base(0x21D02700) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:20	RW	0x010	hw_ynr_loSpnrGain2Strg_val8 gain2strength for low-NR, 5 bit integer and 4 bit fraction
19	RO	0x0	reserved
18:10	RW	0x010	hw_ynr_loSpnrGain2Strg_val7 gain2strength for low-NR, 5 bit integer and 4 bit fraction
9	RO	0x0	reserved
8:0	RW	0x010	hw_ynr_loSpnrGain2Strg_val6 gain2strength for low-NR, 5 bit integer and 4 bit fraction

YNR_2700_RNR_MAX_R

Address: Operational Base(0x21D02700) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x3754	hw_ynr_rnr_maxRadius 9 bit integer and 5 bit fraction {M(9bit),E(5bit)}.1/R^2= M/(2^E), M and E will be calculated automatically by driver. Use RNR module when no exgain. RNR module will reduce the influence of LSC.

YNR_2700_RNR_CENTER_COOR

Address: Operational Base(0x21D02700) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	hw_ynr_rnr_Vcenter RNR center coordinate

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Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12:0	RW	0x0001	hw_ynr_rnr_Hcenter RNR center coordinate. Note: The bit0 =0 means RNR use configure mode, the default mode is not configure mode.

YNR_2700_RNR_STRENGTH03

Address: Operational Base(0x21D02700) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:24	RW	0x10	hw_ynr_radius2strg_val3 strength for radial-based noise reduction, 4 bit integer and 4 bit fraction
23:16	RW	0x10	hw_ynr_radius2strg_val2 strength for radial-based noise reduction, 4 bit integer and 4 bit fraction
15:8	RW	0x10	hw_ynr_radius2strg_val1 strength for radial-based noise reduction, 4 bit integer and 4 bit fraction
7:0	RW	0x10	hw_ynr_radius2strg_val0 strength for radial-based noise reduction, 4 bit integer and 4 bit fraction

YNR_2700_RNR_STRENGTH47

Address: Operational Base(0x21D02700) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:24	RW	0x10	hw_ynr_radius2strg_val7 strength for radial-based noise reduction, 4 bit integer and 4 bit fraction
23:16	RW	0x10	hw_ynr_radius2strg_val6 strength for radial-based noise reduction, 4 bit integer and 4 bit fraction
15:8	RW	0x10	hw_ynr_radius2strg_val5 strength for radial-based noise reduction, 4 bit integer and 4 bit fraction
7:0	RW	0x10	hw_ynr_radius2strg_val4 strength for radial-based noise reduction, 4 bit integer and 4 bit fraction

YNR_2700_RNR_STRENGTH8b

Address: Operational Base(0x21D02700) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:24	RW	0x10	hw_ynr_radius2strg_val11 strength for radial-based noise reduction, 4 bit integer and 4 bit fraction
23:16	RW	0x10	hw_ynr_radius2strg_val10 strength for radial-based noise reduction, 4 bit integer and 4 bit fraction
15:8	RW	0x10	hw_ynr_radius2strg_val9 strength for radial-based noise reduction, 4 bit integer and 4 bit fraction
7:0	RW	0x10	hw_ynr_radius2strg_val8 strength for radial-based noise reduction, 4 bit integer and 4 bit fraction

YNR_2700_RNR_STRENGTHcf

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Address: Operational Base(0x21D02700) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:24	RW	0x10	hw_ynr_radius2strg_val15 strength for radial-based noise reduction, 4 bit integer and 4 bit fraction
23:16	RW	0x10	hw_ynr_radius2strg_val14 strength for radial-based noise reduction, 4 bit integer and 4 bit fraction
15:8	RW	0x10	hw_ynr_radius2strg_val13 strength for radial-based noise reduction, 4 bit integer and 4 bit fraction
7:0	RW	0x10	hw_ynr_radius2strg_val12 strength for radial-based noise reduction, 4 bit integer and 4 bit fraction

YNR_2700_RNR_STRENGTH16

Address: Operational Base(0x21D02700) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x10	hw_ynr_radius2strg_val16 strength for radial-based noise reduction, 4 bit integer and 4 bit fraction

YNR_2700_SGM_DX_0_1

Address: Operational Base(0x21D02700) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x040	hw_ynr_luma2sima_idx1 Sigma point x coordinate [0-1024]
15:11	RO	0x00	reserved
10:0	RW	0x000	hw_ynr_luma2sima_idx0 Sigma point x coordinate [0-1024]

YNR_2700_SGM_DX_2_3

Address: Operational Base(0x21D02700) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x0c0	hw_ynr_luma2sima_idx3 Sigma point x coordinate [0-1024]
15:11	RO	0x00	reserved
10:0	RW	0x080	hw_ynr_luma2sima_idx2 Sigma point x coordinate [0-1024]

YNR_2700_SGM_DX_4_5

Address: Operational Base(0x21D02700) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x140	hw_ynr_luma2sima_idx5 Sigma point x coordinate [0-1024]
15:11	RO	0x00	reserved
10:0	RW	0x100	hw_ynr_luma2sima_idx4 Sigma point x coordinate [0-1024]

YNR_2700_SGM_DX_6_7

Address: Operational Base(0x21D02700) + offset (0x004C)

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Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x1c0	hw_ynr_luma2sima_idx7 Sigma point x coordinate [0-1024]
15:11	RO	0x00	reserved
10:0	RW	0x180	hw_ynr_luma2sima_idx6 Sigma point x coordinate [0-1024]

YNR_2700_SGM_DX_8_9

Address: Operational Base(0x21D02700) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x240	hw_ynr_luma2sima_idx9 Sigma point x coordinate [0-1024]
15:11	RO	0x00	reserved
10:0	RW	0x200	hw_ynr_luma2sima_idx8 Sigma point x coordinate [0-1024]

YNR_2700_SGM_DX_10_11

Address: Operational Base(0x21D02700) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x2c0	hw_ynr_luma2sima_idx11 Sigma point x coordinate [0-1024]
15:11	RO	0x00	reserved
10:0	RW	0x280	hw_ynr_luma2sima_idx10 Sigma point x coordinate [0-1024]

YNR_2700_SGM_DX_12_13

Address: Operational Base(0x21D02700) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x340	hw_ynr_luma2sima_idx13 Sigma point x coordinate [0-1024]
15:11	RO	0x00	reserved
10:0	RW	0x300	hw_ynr_luma2sima_idx12 Sigma point x coordinate [0-1024]

YNR_2700_SGM_DX_14_15

Address: Operational Base(0x21D02700) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x3c0	hw_ynr_luma2sima_idx15 Sigma point x coordinate [0-1024]
15:11	RO	0x00	reserved
10:0	RW	0x380	hw_ynr_luma2sima_idx14 Sigma point x coordinate [0-1024]

YNR_2700_SGM_DX_16

Address: Operational Base(0x21D02700) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x400	hw_ynr_luma2sima_idx16 Sigma point x coordinate [0-1024]

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YNR_2700_SGM_Y_0_1

Address: Operational Base(0x21D02700) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0a0	hw_ynr_luma2sima_val1 14bit unsigned, 9bit integer and 5bit fraction.
15:12	RO	0x0	reserved
11:0	RW	0x04c	hw_ynr_luma2sima_val0 14bit unsigned, 9bit integer and 5bit fraction. The interval widths in x direction are defined in SGM_DX_1_8 or SGM_DX_9_16.

YNR_2700_SGM_Y_2_3

Address: Operational Base(0x21D02700) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0e4	hw_ynr_luma2sima_val3 14bit unsigned, 9bit integer and 5bit fraction.
15:12	RO	0x0	reserved
11:0	RW	0x0d0	hw_ynr_luma2sima_val2 14bit unsigned, 9bit integer and 5bit fraction.

YNR_2700_SGM_Y_4_5

Address: Operational Base(0x21D02700) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0e4	hw_ynr_luma2sima_val5 14bit unsigned, 9bit integer and 5bit fraction.
15:12	RO	0x0	reserved
11:0	RW	0x0e8	hw_ynr_luma2sima_val4 14bit unsigned, 9bit integer and 5bit fraction.

YNR_2700_SGM_Y_6_7

Address: Operational Base(0x21D02700) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0cc	hw_ynr_luma2sima_val7 14bit unsigned, 9bit integer and 5bit fraction.
15:12	RO	0x0	reserved
11:0	RW	0x0d8	hw_ynr_luma2sima_val6 14bit unsigned, 9bit integer and 5bit fraction.

YNR_2700_SGM_Y_8_9

Address: Operational Base(0x21D02700) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0c0	hw_ynr_luma2sima_val9 14bit unsigned, 9bit integer and 5bit fraction.
15:12	RO	0x0	reserved
11:0	RW	0x0c4	hw_ynr_luma2sima_val8 14bit unsigned, 9bit integer and 5bit fraction.

YNR_2700_SGM_Y_10_11

Address: Operational Base(0x21D02700) + offset (0x0078)

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Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0b8	hw_ynr_luma2sima_val11 14bit unsigned, 9bit integer and 5bit fraction.
15:12	RO	0x0	reserved
11:0	RW	0x0bc	hw_ynr_luma2sima_val10 14bit unsigned, 9bit integer and 5bit fraction.

YNR_2700_SGM_Y_12_13

Address: Operational Base(0x21D02700) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0a4	hw_ynr_luma2sima_val13 14bit unsigned, 9bit integer and 5bit fraction.
15:12	RO	0x0	reserved
11:0	RW	0x0b4	hw_ynr_luma2sima_val12 14bit unsigned, 9bit integer and 5bit fraction.

YNR_2700_SGM_Y_14_15

Address: Operational Base(0x21D02700) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x054	hw_ynr_luma2sima_val15 14bit unsigned, 9bit integer and 5bit fraction.
15:12	RO	0x0	reserved
11:0	RW	0x088	hw_ynr_luma2sima_val14 14bit unsigned, 9bit integer and 5bit fraction.

YNR_2700_SGM_Y_16

Address: Operational Base(0x21D02700) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x028	hw_ynr_luma2sima_val16 14bit unsigned, 9bit integer and 5bit fraction.

YNR_2700_MI_TEX2WGT_SCALE_0_1_2

Address: Operational Base(0x21D02700) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:20	RW	0x10	hw_ynr_mispnr_tex2wgtscale2 7bit unsigned.
19:17	RO	0x0	reserved
16:10	RW	0x12	hw_ynr_mispnr_tex2wgtscale1 7bit unsigned.
9:7	RO	0x0	reserved
6:0	RW	0x40	hw_ynr_mispnr_tex2wgtscale0 7bit unsigned.

YNR_2700_MI_TEX2WGT_SCALE_3_4_5

Address: Operational Base(0x21D02700) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:20	RW	0x02	hw_ynr_mispnr_tex2wgtscale5 7bit unsigned.
19:17	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
16:10	RW	0x04	hw_ynr_mispnr_tex2wgtscale4 7bit unsigned.
9:7	RO	0x0	reserved
6:0	RW	0x08	hw_ynr_mispnr_tex2wgtscale3 7bit unsigned.

YNR_2700_MI_TEX2WGT_SCALE_6_7_8

Address: Operational Base(0x21D02700) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:20	RW	0x01	hw_ynr_mispnr_tex2wgtscale8 7bit unsigned.
19:17	RO	0x0	reserved
16:10	RW	0x01	hw_ynr_mispnr_tex2wgtscale7 7bit unsigned.
9:7	RO	0x0	reserved
6:0	RW	0x01	hw_ynr_mispnr_tex2wgtscale6 7bit unsigned.

YNR_2700_LO_TEX2WGT_SCALE_0_1_2

Address: Operational Base(0x21D02700) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:20	RW	0x10	hw_ynr_lospnr_tex2wgtscale2 7bit unsigned.
19:17	RO	0x0	reserved
16:10	RW	0x12	hw_ynr_lospnr_tex2wgtscale1 7bit unsigned.
9:7	RO	0x0	reserved
6:0	RW	0x40	hw_ynr_lospnr_tex2wgtscale0 7bit unsigned.

YNR_2700_LO_TEX2WGT_SCALE_3_4_5

Address: Operational Base(0x21D02700) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:20	RW	0x02	hw_ynr_lospnr_tex2wgtscale5 7bit unsigned.
19:17	RO	0x0	reserved
16:10	RW	0x04	hw_ynr_lospnr_tex2wgtscale4 7bit unsigned.
9:7	RO	0x0	reserved
6:0	RW	0x08	hw_ynr_lospnr_tex2wgtscale3 7bit unsigned.

YNR_2700_LO_TEX2WGT_SCALE_6_7_8

Address: Operational Base(0x21D02700) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:20	RW	0x01	hw_ynr_lospnr_tex2wgtscale8 7bit unsigned.
19:17	RO	0x0	reserved
16:10	RW	0x01	hw_ynr_lospnr_tex2wgtscale7 7bit unsigned.

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Bit	Attr	Reset Value	Description
9:7	RO	0x0	reserved
6:0	RW	0x01	hw_ynr_lospnr_tex2wgtscale6 7bit unsigned.

YNR_2700_HI_SIGMA_GAIN

Address: Operational Base(0x21D02700) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x040	hw_ynr_hiSpnr_strg Denoise scale of high frequency noise. Range: [0,16) Fixed-point: [0,4,6]
15:11	RW	0x10	hw_ynr_hiSpnrLocalGain_alpha Control the use ratio of local gain and global gain. Range: [0,1] Fixed-point: [0,1,4]
10:0	RW	0x002	hw_ynr_hiSpnrSigma_minLimit Minimum noise sigma for high frequency noise.

YNR_2700_HI_GAUS_COE

Address: Operational Base(0x21D02700) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:18	RW	0x0a	hw_ynr_hiSpnrFilt_coeff3 Coefficient 3 of gaussian filter which counts for distance factor. Range: [0,15] Fixed-point: [0,4,0]
17:12	RW	0x0e	hw_ynr_hiSpnrFilt_coeff2 Coefficient 2 of gaussian filter which counts for distance factor. Range: [0,15] Fixed-point: [0,4,0]
11:6	RW	0x0b	hw_ynr_hiSpnrFilt_coeff1 Coefficient 1 of gaussian filter which counts for distance factor. Range: [0,15] Fixed-point: [0,4,0]
5:0	RW	0x10	hw_ynr_hiSpnrFilt_coeff0 Coefficient 0 of gaussian filter which counts for distance factor. Range: [0,15] Fixed-point: [0,4,0]

YNR_2700_HI_WEIGHT

Address: Operational Base(0x21D02700) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:10	RW	0x0100	hw_ynr_hiSpnrFilt_centerWgt Extra weight for original central pixel.
9:0	RW	0x000	hw_ynr_hiSpnrFilt_wgt_Offset Offset that subtracted from calculated weight of each pixel.

YNR_2700_HI_GAUS1_COE_0_2

Address: Operational Base(0x21D02700) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:20	RW	0x008	hw_ynr_hiSpnrFilt1_coeff2 Gaus coefficient 2 of Gaussian filter in hi-NR.

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Bit	Attr	Reset Value	Description
19	RO	0x0	reserved
18:10	RW	0x011	hw_ynr_hiSpnrFilt1_coeff1 Gaus coefficient 1 of Gaussian filter in hi-NR.
9	RO	0x0	reserved
8:0	RW	0x020	hw_ynr_hiSpnrFilt1_coeff0 Gaus coefficient 0 of Gaussian filter in hi-NR.

YNR_2700_HI_GAUS1_COE_3_5

Address: Operational Base(0x21D02700) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:20	RW	0x003	hw_ynr_hiSpnrFilt1_coeff5 Gaus coefficient 5 of Gaussian filter in hi-NR.
19	RO	0x0	reserved
18:10	RW	0x007	hw_ynr_hiSpnrFilt1_coeff4 Gaus coefficient 4 of Gaussian filter in hi-NR.
9	RO	0x0	reserved
8:0	RW	0x00e	hw_ynr_hiSpnrFilt1_coeff3 Gaus coefficient 3 of Gaussian filter in hi-NR.

YNR_2700_HI_TEXT

Address: Operational Base(0x21D02700) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:22	RW	0x100	hw_ynr_hiSpnrFilt1_wgtAlpha global weighting factor for Gaussian filtered result. Range: [0,1] Fixed-point: [0,1,8]
21:12	RW	0x040	hw_ynr_hiSpnrFilt1_texScale scale factor of texture value for hi-NR
11	RO	0x0	reserved
10:0	RW	0x080	hw_ynr_hiSpnrFilt1_texThred texture threshold for texture detection to decide detail or flat regions Range: [0,8] Fixed-point: [0,3,8]

YNR_2700_MI_GAUS_COE

Address: Operational Base(0x21D02700) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:20	RW	0x05	hw_ynr_miSpnrFilt_coeff2 Gaus coefficient 2 for mi-NR.
19:15	RO	0x00	reserved
14:10	RW	0x08	hw_ynr_miSpnrFilt_coeff1 Gaus coefficient 1 for mi-NR.
9:8	RO	0x0	reserved
7:0	RW	0x0c	hw_ynr_miSpnrFilt_coeff0 Gaus coefficient 0 for mi-NR.

YNR_2700_MI_STRG_DETAIL

Address: Operational Base(0x21D02700) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:16	RW	0x0cc	hw_ynr_miSpnrSoftThred_scale scale factor of soft-threshold operation for mi-NR when blending input. Range: [0,4] Fixed-point: [0,2,10]
15:10	RO	0x00	reserved
9:0	RW	0x040	hw_ynr_miSpnr_strg global strength for mi-NR, which scale the noise sigma value

YNR_2700_MI_WEIGHT

Address: Operational Base(0x21D02700) + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:24	RW	0x08	hw_ynr_miEhance_scale Scale factor of blending mi-freqency detail to NR result.
23	RW	0x0	hw_ynr_miEhance_scale_en MIEhance scale enable bit.
22:21	RO	0x0	reserved
20:10	RW	0x040	hw_ynr_miSpnrFilt_centerWgt Extra weight for original central pixel for mi-NR. Range: [0,1] Fixed-point: [0,1,10]
9:8	RO	0x0	reserved
7:0	RW	0x80	hw_ynr_miSpnr_wgt blending weight of input for mi-NR Range: [0,1] Fixed-point: [0,1,7]

YNR_2700_MI_GAUS_COE1

Address: Operational Base(0x21D02700) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:10	RW	0x4	hw_ynr_miSpnrFilt_coeff4 Gaus coefficient 4 for mi-NR.
9:4	RO	0x00	reserved
3:0	RW	0x6	hw_ynr_miSpnrFilt_coeff3 Gaus coefficient 3 for mi-NR.

YNR_2700_DSIIR_COE

Address: Operational Base(0x21D02700) + offset (0x00DC)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:21	RW	0x040	hw_ynr_dsfilt_strg Strength of ds iir filter.
20:10	RW	0x0c8	hw_ynr_dsfilt_centerwgt Center weight of ds iir filter.
9:0	RW	0x000	hw_ynr_dsfilt_diffoffset Delta offset of ds iir filter.

YNR_2700_LO_STRG_DETAIL

Address: Operational Base(0x21D02700) + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:16	RW	0x040	hw_ynr_loSpnrSoftThred_scale scale factor of soft-threshold operation for mi-NR when blending input. Range: [0,4] Fixed-point: [0,2,10]
15:10	RO	0x00	reserved
9:0	RW	0x040	hw_ynr_loSpnr_strg global strength for low-NR, which scale the noise sigma value

YNR_2700_LO_LIMIT_SCALE

Address: Operational Base(0x21D02700) + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x9	hw_ynr_tex2loStrg_exponent exponent of sharpen2ynr texture based strength
23	RO	0x0	reserved
22:12	RW	0x280	hw_ynr_tex2loStrg_mantissa mantissa of sharpen2ynr texture based strength
11:10	RO	0x0	reserved
9:0	RW	0x040	hw_ynr_loSpnrThumbThred_scale scale factor of soft-threshold operation between reference pixel and down-scaled pixel

YNR_2700_LO_WEIGHT

Address: Operational Base(0x21D02700) + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	hw_ynr_loEnhance_scale Scale factor of blending lo-freqency detail to NR result.
23	RO	0x0	reserved
22:10	RW	0x0090	hw_ynr_loSpnrFilt_centerWgt Extra weight for original central pixel for low-NR
9:8	RO	0x0	reserved
7:0	RW	0x80	hw_ynr_loSpnr_wgt blending weight of input for low-NR Range: [0,1] Fixed-point: [0,1,7]

YNR_2700_LO_TEXT_THRED

Address: Operational Base(0x21D02700) + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:12	RW	0x199	hw_ynr_tex2loStrg_lowerThred lower threshold of sharpen2ynr texture value for texture-strength curve
11:10	RO	0x0	reserved
9:0	RW	0x332	hw_ynr_tex2loStrg_upperThred upper threshold of sharpen2ynr texture value for texture-strength curve

YNR_2700_FUSION_WEIT_ADJ_0_3

Address: Operational Base(0x21D02700) + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:24	RW	0x80	hw_ynr_loGain2wgt_val3 scale factor of blending weight for nr-result in low-NR, 1 bit integer and 7 bit fraction

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Bit	Attr	Reset Value	Description
23:16	RW	0x80	hw_ynr_loGain2wgt_val2 scale factor of blending weight for nr-result in low-NR, 1 bit integer and 7 bit fraction
15:8	RW	0x80	hw_ynr_loGain2wgt_val1 scale factor of blending weight for nr-result in low-NR, 1 bit integer and 7 bit fraction
7:0	RW	0x80	hw_ynr_loGain2wgt_val0 scale factor of blending weight for nr-result in low-NR, 1 bit integer and 7 bit fraction

YNR_2700_FUSION_WEIT_ADJ_4_7

Address: Operational Base(0x21D02700) + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:24	RW	0x80	hw_ynr_loGain2wgt_val7 scale factor of blending weight for nr-result in low-NR, 1 bit integer and 7 bit fraction
23:16	RW	0x80	hw_ynr_loGain2wgt_val6 scale factor of blending weight for nr-result in low-NR, 1 bit integer and 7 bit fraction
15:8	RW	0x80	hw_ynr_loGain2wgt_val5 scale factor of blending weight for nr-result in low-NR, 1 bit integer and 7 bit fraction
7:0	RW	0x80	hw_ynr_loGain2wgt_val4 scale factor of blending weight for nr-result in low-NR, 1 bit integer and 7 bit fraction

YNR_2700_FUSION_WEIT_ADJ_8

Address: Operational Base(0x21D02700) + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x80	hw_ynr_loGain2wgt_val8 scale factor of blending weight for nr-result in low-NR, 1 bit integer and 7 bit fraction

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ISP_CNR_2800_CTRL

Address: Operational Base(0x21D02800) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	hw_cnrT_en_shd CNR enable shadow register
30	RO	0x0	ro_cnr_working CNR working status
29	RO	0x0	hw_cnrT_exgain_bypass_shd CNR gain enable shadow signal 1'b0: Disable 1'b1: Enable
28:19	RO	0x000	reserved
18	RW	0x0	sw_cnr_hsv_alpha_en CNR hsv alhpa enable signal 1'b0: Use old alpha 1'b1: Use hsv alpha
17:12	RW	0x00	hw_cnrT_loFlt_coeff Weights of six points participating in iir calculation.

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Bit	Attr	Reset Value	Description
11	RW	0x0	sw_cnr_local_alpha_dis CNR bf3x3 out local alpha disable signal. 1'b0: Use local alpha 1'b1: Use global alpha
10:9	RO	0x0	reserved
8	RW	0x0	hw_cnrT_hiFltWgt0_mode CNR bf3x3 outdata select when bf3x3 weight is 0. 1'b0: Source data 1'b1: Gaussian data
7	RO	0x0	reserved
6	RW	0x0	sw_cnr_uv_dis Low power mode, force output value to 0x200
5:4	RW	0x0	hw_cnrT_thumb_mode CNR down sampling mode 2'b00: 2x2 mode 2'b01: 4x4 mode 2'b10: 8x6 mode 2'b11: 8x4 mode 3576 CNR can only support 4x4 and 8x4 mode.
3	RO	0x0	reserved
2	RO	0x0	hw_cnrT_yuv422mode_en Always be 0, reserved for later version. 3576 CNR can only support 420 mode.
1	RW	0x1	hw_cnrT_exgain_bypass External gain bypass enable signal, read back is shadow register. 1'b1: Bypass is enable, external gain value is fixed to sw_cnr_egain_mux. 1'b0: Bypass is disable, use external gain.
0	RW	0x0	hw_cnrT_en CNR enable signal 1'b1: CNR enable 1'b0: CNR disable

ISP_CNR_2800_EXGAIN

Address: Operational Base(0x21D02800) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	hw_cnrT_localGain_scale To enlarge external gain, range from 8 to 128.
15:12	RW	0x8	hw_cnr_global_gain_alpha Global gain alpha for CNR, data range [0,8]. Gain = (sw_cnr_global_gain_alpha * sw_cnr_global_gain + (8 - sw_cnr_global_gain_alpha) * local_gain) >> 3
11:10	RO	0x0	reserved
9:0	RW	0x080	hw_cnrT_global_gain Global gain for CNR

ISP_CNR_2800_THUMB1

Address: Operational Base(0x21D02800) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x00c0	hw_cnrT_loBfFlt_vsigmaY The sigma Y used in lbf1x7 module. Range: [1,16383] Fixed-point:[0,0,14]

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Bit	Attr	Reset Value	Description
15:14	RO	0x0	reserved
13:0	RW	0x00a0	hw_cnrT_loBfFlt_vsigmaUV The sigma UV used in lbf1x7 module. Range: [1,16383] Fixed-point:[0,0,14]

ISP_CNR_2800_THUMB_BF_RATIO

Address: Operational Base(0x21D02800) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:11	RO	0x000000	reserved
10:0	RW	0x400	hw_cnrT_loBfFlt_alpha Control the fusion weight of loBfFlt data and in_data in lbf1x7 module. range from 0 to 1024. Range: [0,1024] Fixed-point:[0,1,7]

ISP_CNR_2800_LBF_WEITD

Address: Operational Base(0x21D02800) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:24	RW	0x80	hw_cnrT_thumbBf_coeff3 The distance weight3 in lbf1x7 module. Range: [0,128] Fixed-point:[0,1,7]
23:16	RW	0x80	hw_cnrT_thumbBf_coeff2 The distance weight2 in lbf1x7 module. Range: [0,128] Fixed-point:[0,1,7]
15:8	RW	0x80	hw_cnrT_thumbBf_coeff1 The distance weight1 in lbf1x7 module. Range: [0,128] Fixed-point:[0,1,7]
7:0	RW	0x80	hw_cnrT_thumbBf_coeff0 The distance weight0 in lbf1x7 module. Range: [0,128] Fixed-point:[0,1,7]

ISP_CNR_2800_IIR_PARA1

Address: Operational Base(0x21D02800) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x05a	hw_cnrT_loFltWgt_slope The slope of bf weight curve in IIR filter Fixed-point:[0,3,7]
19:18	RO	0x0	reserved
17:12	RW	0x04	hw_cnrT_expX_shiftBit Control shift in IIR filter, bit 6 control the shift direction. 1'b1: Shift left 1'b0: Shift right Bit 0~5 control the shift number. When shift left, the max value of bit 0~5 is 4; When shift right, the max value of bit 0~5 is 16.
11:4	RW	0xd8	hw_cnrT_loFlt_vsigma The strength of IIR filter Fixed-point:[0,0,8]

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Bit	Attr	Reset Value	Description
3:0	RW	0x5	hw_cnrT_loFltUV_gain UV gain of IIR filter. Range: [0,8]

ISP_CNR_2800_IIR_PARA2

Address: Operational Base(0x21D02800) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:8	RW	0x3a	hw_cnrT_loFltWgt_maxLimit Clip weight in IIR filter, range from 1 to 63. Fixed-point:[0,4,3]
7:6	RO	0x0	reserved
5:0	RW	0x02	hw_cnrT_loFltWgt_minThred clip sum weight in IIR filter , control the max iir filter strength. Fixed-point:[0,0,6]

ISP_CNR_2800_GAUS_COE1

Address: Operational Base(0x21D02800) + offset (0x001C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x06	hw_cnrT_gausFlt_coeff3 Gaussian filter coefficient3 Fixed-point:[0,0,7]
23	RO	0x0	reserved
22:16	RW	0x1c	hw_cnrT_gausFlt_coeff2 Gaussian filter coefficient2 Fixed-point:[0,0,7]
15	RO	0x0	reserved
14:8	RW	0x11	hw_cnrT_gausFlt_coeff1 Gaussian filter coefficient1 Fixed-point:[0,0,7]
7	RO	0x0	reserved
6:0	RW	0x04	hw_cnrT_gausFlt_coeff0 Gaussian filter coefficient0 Fixed-point:[0,0,7]

ISP_CNR_2800_GAUS_COE2

Address: Operational Base(0x21D02800) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:8	RW	0x30	hw_cnrT_gausFlt_coeff5 Gaussian filter coefficient5 Fixed-point:[0,0,7]
7	RO	0x0	reserved
6:0	RW	0x1c	hw_cnrT_gausFlt_coeff4 Gaussian filter coefficient4 Fixed-point:[0,0,7]

ISP_CNR_2800_GAUS_RATIO

Address: Operational Base(0x21D02800) + offset (0x0024)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
30:20	RW	0x400	hw_cnrT_hiFlt_alpha The fusion weight of bf3x3 out_data and in_data, range from 0 to 1024. Fixed-point:[0,1,10]
19:12	RW	0x00	hw_cnrT_hiFltWgt_minLimit The min weight in bf3x3 module, range from 0 to 128. Fixed-point:[0,0,8]
11	RO	0x0	reserved
10:0	RW	0x400	hw_cnrT_gausFlt_alpha The fusion weight of gaus_out_data and gaus_in_data, range from 0 to 1024. Fixed-point:[0,1,10]

ISP_CNR_2800_BF_PARA1

Address: Operational Base(0x21D02800) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:24	RW	0x08	hw_cnrT_hiFltCur_wgt The in_data weight in bf3x3 bilateral filter Fixed-point:[0,1,7] 3576 do not use it.
23:22	RO	0x0	reserved
21:8	RW	0x01b3	hw_cnrT_hiFltGlobal_vsigma The sigma of bf3x3 module Fixed-point:[0,0,14] 3576 do not use it.
7	RO	0x0	reserved
6:0	RW	0x40	hw_cnrT_hiFltUV_gain UV gain of bf3x3 module Fixed-point:[0,3,4]

ISP_CNR_2800_BF_PARA2

Address: Operational Base(0x21D02800) + offset (0x002C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0000	hw_cnrT_satAdj_scale The saturation adjust scale in bf3x3 module, range from 0 to 16384. Fixed-point:[0,15,10]
15:9	RO	0x00	reserved
8:0	RW	0x014	hw_cnrT_satAdj_offset The saturation adjust offset in bf3x3 module

ISP_CNR_2800_SIGMA0

Address: Operational Base(0x21D02800) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:24	RW	0x40	hw_cnrT_gainAdjHiFltSgm_ratio3 Sigma adj ratio curve y3 Fixed-point:[0,2,6]
23:16	RW	0x55	hw_cnrT_gainAdjHiFltSgm_ratio2 Sigma adj ratio curve y2 Fixed-point:[0,2,6]
15:8	RW	0x80	hw_cnrT_gainAdjHiFltSgm_ratio1 Sigma adj ratio curve y1 Fixed-point:[0,2,6]

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Bit	Attr	Reset Value	Description
7:0	RW	0xff	hw_cnrT_gainAdjHiFltSgm_ratio0 Sigma adj ratio curve y0 Fixed-point:[0,2,6]

ISP_CNR_2800_SIGMA1

Address: Operational Base(0x21D02800) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:24	RW	0x10	hw_cnrT_gainAdjHiFltSgm_ratio7 Sigma adj ratio curve y7 Fixed-point:[0,2,6]
23:16	RW	0x15	hw_cnrT_gainAdjHiFltSgm_ratio6 Sigma adj ratio curve y6 Fixed-point:[0,2,6]
15:8	RW	0x20	hw_cnrT_gainAdjHiFltSgm_ratio5 Sigma adj ratio curve y5 Fixed-point:[0,2,6]
7:0	RW	0x2b	hw_cnrT_gainAdjHiFltSgm_ratio4 Sigma adj ratio curve y4 Fixed-point:[0,2,6]

ISP_CNR_2800_SIGMA2

Address: Operational Base(0x21D02800) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:24	RW	0x01	hw_cnrT_gainAdjHiFltSgm_ratio11 Sigma adj ratio curve y11 Fixed-point:[0,2,6]
23:16	RW	0x02	hw_cnrT_gainAdjHiFltSgm_ratio10 Sigma adj ratio curve y10 Fixed-point:[0,2,6]
15:8	RW	0x04	hw_cnrT_gainAdjHiFltSgm_ratio9 Sigma adj ratio curve y9 Fixed-point:[0,2,6]
7:0	RW	0x08	hw_cnrT_gainAdjHiFltSgm_ratio8 Sigma adj ratio curve y8 Fixed-point:[0,2,6]

ISP_CNR_2800_SIGMA3

Address: Operational Base(0x21D02800) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	hw_cnrT_bfMerge_maxLimit CNR bf3x3 merge maxlimit.
15:8	RO	0x00	reserved
7:0	RW	0x01	hw_cnrT_gainAdjHiFltSgm_ratio12 Sigma adj ratio curve y12 Fixed-point:[0,2,6]

ISP_CNR_2800_IIR_GLOBAL_GAIN

Address: Operational Base(0x21D02800) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	hw_cnrT_bfAlpha_maxLimit CNR bf3x3 alpha maxlimit.
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:8	RW	0x0	hw_cnrT_loFltGlobalSgmRatio_alpha The fusion weight of global sigma adj ratio and local adj ration in IIR filter.
7:0	RW	0x40	hw_cnrT_loFltGlobalSgm_ratio The global sigma adj ratio in IIR filter Fixed-point:[0,4,4]

ISP_CNR_2800_WGT_SIGMA0

Address: Operational Base(0x21D02800) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:24	RW	0x40	hw_cnrT_gainAdjHiFltCur_wgt3 The in data weight adj ratio curve y3 in 3x3bf Fixed-point:[0,2,6]
23:16	RW	0x55	hw_cnrT_gainAdjHiFltCur_wgt2 The in data weight adj ratio curve y2 in 3x3bf Fixed-point:[0,2,6]
15:8	RW	0x80	hw_cnrT_gainAdjHiFltCur_wgt1 The in data weight adj ratio curve y1 in 3x3bf Fixed-point:[0,2,6]
7:0	RW	0xff	hw_cnrT_gainAdjHiFltCur_wgt0 The in data weight adj ratio curve y0 in 3x3bf Fixed-point:[0,2,6]

ISP_CNR_2800_WGT_SIGMA1

Address: Operational Base(0x21D02800) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:24	RW	0x40	hw_cnrT_gainAdjHiFltCur_wgt7 The in data weight adj ratio curve y7 in 3x3bf Fixed-point:[0,2,6]
23:16	RW	0x55	hw_cnrT_gainAdjHiFltCur_wgt6 The in data weight adj ratio curve y6 in 3x3bf Fixed-point:[0,2,6]
15:8	RW	0x80	hw_cnrT_gainAdjHiFltCur_wgt5 The in data weight adj ratio curve y5 in 3x3bf Fixed-point:[0,2,6]
7:0	RW	0xff	hw_cnrT_gainAdjHiFltCur_wgt4 The in data weight adj ratio curve y4 in 3x3bf Fixed-point:[0,2,6]

ISP_CNR_2800_WGT_SIGMA2

Address: Operational Base(0x21D02800) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:24	RW	0x01	hw_cnrT_gainAdjHiFltCur_wgt11 The in data weight adj ratio curve y11 in 3x3bf Fixed-point:[0,2,6]
23:16	RW	0x02	hw_cnrT_gainAdjHiFltCur_wgt10 The in data weight adj ratio curve y10 in 3x3bf Fixed-point:[0,2,6]
15:8	RW	0x04	hw_cnrT_gainAdjHiFltCur_wgt9 The in data weight adj ratio curve y9 in 3x3bf Fixed-point:[0,2,6]
7:0	RW	0x08	hw_cnrT_gainAdjHiFltCur_wgt8 The in data weight adj ratio curve y8 in 3x3bf Fixed-point:[0,2,6]

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ISP_CNR_2800_WGT_SIGMA3

Address: Operational Base(0x21D02800) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x01	hw_cnrT_gainAdjHiFltCur_wgt12 The in data weight adj ratio curve y12 in 3x3bf Fixed-point:[0,2,6]

ISP_CNR_2800_GAUS_X_SIGMAR0

Address: Operational Base(0x21D02800) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x055	hw_cnrT_hiFltVsigma_idx2 Luma index2 of hiFlt sigma curve.
19:10	RW	0x080	hw_cnrT_hiFltVsigma_idx1 Luma index1 of hiFlt sigma curve.
9:0	RW	0x0ff	hw_cnrT_hiFltVsigma_idx0 Luma index0 of hiFlt sigma curve.

ISP_CNR_2800_GAUS_X_SIGMAR1

Address: Operational Base(0x21D02800) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x055	hw_cnrT_hiFltVsigma_idx5 Luma index5 of hiFlt sigma curve.
19:10	RW	0x080	hw_cnrT_hiFltVsigma_idx4 Luma index4 of hiFlt sigma curve.
9:0	RW	0x0ff	hw_cnrT_hiFltVsigma_idx3 Luma index3 of hiFlt sigma curve.

ISP_CNR_2800_GAUS_X_SIGMAR2

Address: Operational Base(0x21D02800) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:10	RW	0x080	hw_cnrT_hiFltVsigma_idx7 Luma index7 of hiFlt sigma curve.
9:0	RW	0x0ff	hw_cnrT_hiFltVsigma_idx6 Luma index6 of hiFlt sigma curve.

ISP_CNR_2800_GAUS_Y_SIGMAR0

Address: Operational Base(0x21D02800) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0080	hw_cnrT_hiFlt_vsigma1 HiFlt sigma curve y1 Fixed-point:[0,0,14]
15:14	RO	0x0	reserved
13:0	RW	0x00ff	hw_cnrT_hiFlt_vsigma0 HiFlt sigma curve y0 Fixed-point:[0,0,14]

ISP_CNR_2800_GAUS_Y_SIGMAR1

Address: Operational Base(0x21D02800) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:16	RW	0x0080	hw_cnrT_hiFlt_vsigma3 HiFlt sigma curve y3 Fixed-point:[0,0,14]
15:14	RO	0x0	reserved
13:0	RW	0x00ff	hw_cnrT_hiFlt_vsigma2 HiFlt sigma curve y2 Fixed-point:[0,0,14]

ISP_CNR_2800_GAUS_Y_SIGMAR2

Address: Operational Base(0x21D02800) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0080	hw_cnrT_hiFlt_vsigma5 HiFlt sigma curve y5 Fixed-point:[0,0,14]
15:14	RO	0x0	reserved
13:0	RW	0x00ff	hw_cnrT_hiFlt_vsigma4 HiFlt sigma curve y4 Fixed-point:[0,0,14]

ISP_CNR_2800_GAUS_Y_SIGMAR3

Address: Operational Base(0x21D02800) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0080	hw_cnrT_hiFlt_vsigma7 HiFlt sigma curve y7 Fixed-point:[0,0,14]
15:14	RO	0x0	reserved
13:0	RW	0x00ff	hw_cnrT_hiFlt_vsigma6 HiFlt sigma curve y6 Fixed-point:[0,0,14]

ISP_CNR_2800_IIR_SIGMAR0

Address: Operational Base(0x21D02800) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	hw_cnrT_loFlt_vsigma3 LoFlt sigma curve y3 Fixed-point:[0,2,6]
23:16	RW	0xff	hw_cnrT_loFlt_vsigma2 LoFlt sigma curve y2 Fixed-point:[0,2,6]
15:8	RW	0xff	hw_cnrT_loFlt_vsigma1 LoFlt sigma curve y1 Fixed-point:[0,2,6]
7:0	RW	0xff	hw_cnrT_loFlt_vsigma0 LoFlt sigma curve y0 Fixed-point:[0,2,6]

ISP_CNR_2800_IIR_SIGMAR1

Address: Operational Base(0x21D02800) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	hw_cnrT_loFlt_vsigma7 LoFlt sigma curve y7 Fixed-point:[0,2,6]

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Bit	Attr	Reset Value	Description
23:16	RW	0xff	hw_cnrT_loFlt_vsigma6 LoFlt sigma curve y6 Fixed-point:[0,2,6]
15:8	RW	0xff	hw_cnrT_loFlt_vsigma5 LoFlt sigma curve y5 Fixed-point:[0,2,6]
7:0	RW	0xff	hw_cnrT_loFlt_vsigma4 LoFlt sigma curve y4 Fixed-point:[0,2,6]

ISP_CNR_2800_IIR_SIGMAR2

Address: Operational Base(0x21D02800) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	hw_cnrT_loFlt_vsigma11 LoFlt sigma curve y11 Fixed-point:[0,2,6]
23:16	RW	0xff	hw_cnrT_loFlt_vsigma10 LoFlt sigma curve y10 Fixed-point:[0,2,6]
15:8	RW	0xff	hw_cnrT_loFlt_vsigma9 LoFlt sigma curve y9 Fixed-point:[0,2,6]
7:0	RW	0xff	hw_cnrT_loFlt_vsigma8 LoFlt sigma curve y8 Fixed-point:[0,2,6]

ISP_CNR_2800_IIR_SIGMAR3

Address: Operational Base(0x21D02800) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xff	hw_cnrT_loFlt_vsigma12 LoFlt sigma curve y12 Fixed-point:[0,2,6]

ISP_CNR_2800_HSV_CURVE0

Address: Operational Base(0x21D02800) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	hw_cnrT_hsvAdjAlpha_table3 Hsv adjust table y3 Range: [0,128] Fixed-point:[0,7,1]
23:16	RW	0xff	hw_cnrT_hsvAdjAlpha_table2 Hsv adjust table y2 Range: [0,128] Fixed-point:[0,7,1]
15:8	RW	0xff	hw_cnrT_hsvAdjAlpha_table1 Hsv adjust table y1 Range: [0,128] Fixed-point:[0,7,1]
7:0	RW	0xff	hw_cnrT_hsvAdjAlpha_table0 Hsv adjust table y0 Range: [0,128] Fixed-point:[0,7,1]

ISP_CNR_2800_HSV_CURVE1

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Address: Operational Base(0x21D02800) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	hw_cnrT_hsvAdjAlpha_table7 Hsv adjust table y7 Range: [0,128] Fixed-point:[0,7,1]
23:16	RW	0xff	hw_cnrT_hsvAdjAlpha_table6 Hsv adjust table y6 Range: [0,128] Fixed-point:[0,7,1]
15:8	RW	0xff	hw_cnrT_hsvAdjAlpha_table5 Hsv adjust table y5 Range: [0,128] Fixed-point:[0,7,1]
7:0	RW	0xff	hw_cnrT_hsvAdjAlpha_table4 Hsv adjust table y4 Range: [0,128] Fixed-point:[0,7,1]

ISP_CNR_2800_HSV_CURVE2

Address: Operational Base(0x21D02800) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0xff	hw_cnrT_hsvAdjAlpha_table9 Hsv adjust table y9 Range: [0,128] Fixed-point:[0,7,1]
7:0	RW	0xff	hw_cnrT_hsvAdjAlpha_table8 Hsv adjust table y8 Range: [0,128] Fixed-point:[0,7,1]

ISP_CNR_2800_SAT_CURVE0

Address: Operational Base(0x21D02800) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	hw_cnrT_satAdjAlpha_table3 Sat adjust table y3 Range: [0,128] Fixed-point:[0,7,1]
23:16	RW	0xff	hw_cnrT_satAdjAlpha_table2 Sat adjust table y2 Range: [0,128] Fixed-point:[0,7,1]
15:8	RW	0xff	hw_cnrT_satAdjAlpha_table1 Sat adjust table y1 Range: [0,128] Fixed-point:[0,7,1]
7:0	RW	0xff	hw_cnrT_satAdjAlpha_table0 Sat adjust table y0 Range: [0,128] Fixed-point:[0,7,1]

ISP_CNR_2800_SAT_CURVE1

Address: Operational Base(0x21D02800) + offset (0x0090)

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	hw_cnrT_satAdjAlpha_table7 Sat adjust table y7 Range: [0,128] Fixed-point:[0,7,1]
23:16	RW	0xff	hw_cnrT_satAdjAlpha_table6 Sat adjust table y6 Range: [0,128] Fixed-point:[0,7,1]
15:8	RW	0xff	hw_cnrT_satAdjAlpha_table5 Sat adjust table y5 Range: [0,128] Fixed-point:[0,7,1]
7:0	RW	0xff	hw_cnrT_satAdjAlpha_table4 Sat adjust table y4 Range: [0,128] Fixed-point:[0,7,1]

ISP_CNR_2800_SAT_CURVE2

Address: Operational Base(0x21D02800) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0xff	hw_cnrT_satAdjAlpha_table5 Sat adjust table y5 Range: [0,128] Fixed-point:[0,7,1]
7:0	RW	0xff	hw_cnrT_satAdjAlpha_table8 Sat adjust table y8 Range: [0,128] Fixed-point:[0,7,1]

ISP_CNR_2800_GAIN_ADJ_CURVE0

Address: Operational Base(0x21D02800) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	hw_cnrT_gainAdjAlpha_table3 Gain adjust table y3 Range: [0,255] Fixed-point:[0,4,4]
23:16	RW	0xff	hw_cnrT_gainAdjAlpha_table2 Gain adjust table y2 Range: [0,255] Fixed-point:[0,4,4]
15:8	RW	0xff	hw_cnrT_gainAdjAlpha_table1 Gain adjust table y1 Range: [0,255] Fixed-point:[0,4,4]
7:0	RW	0xff	hw_cnrT_gainAdjAlpha_table0 Gain adjust table y0 Range: [0,255] Fixed-point:[0,4,4]

ISP_CNR_2800_GAIN_ADJ_CURVE1

Address: Operational Base(0x21D02800) + offset (0x009C)

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	hw_cnrT_gainAdjAlpha_table7 Gain adjust table y7 Range: [0,255] Fixed-point:[0,4,4]
23:16	RW	0xff	hw_cnrT_gainAdjAlpha_table6 Gain adjust table y6 Range: [0,255] Fixed-point:[0,4,4]
15:8	RW	0xff	hw_cnrT_gainAdjAlpha_table5 Gain adjust table y5 Range: [0,255] Fixed-point:[0,4,4]
7:0	RW	0xff	hw_cnrT_gainAdjAlpha_table4 Gain adjust table y4 Range: [0,255] Fixed-point:[0,4,4]

ISP_CNR_2800_GAIN_ADJ_CURVE2

Address: Operational Base(0x21D02800) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0xff	hw_cnrT_gainAdjAlpha_table9 Gain adjust table y9 Range: [0,255] Fixed-point:[0,4,4]
7:0	RW	0xff	hw_cnrT_gainAdjAlpha_table8 Gain adjust table y8 Range: [0,255] Fixed-point:[0,4,4]

44.4.2.23 SHARP

ISP_SHARP_2900_CTRL

Address: Operational Base(0x21D02900) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	hw_sharp_en_shd Sharp enable shadow signal.
30	RO	0x0	sharp_working SHARP working signal.
29	RO	0x0	hw_sharp_bypass_en_shd The shadow register of sw_sharp_bypass_en_i.
28	RO	0x0	hw_sharp_noiseEst_mode_shd The shadow register of hw_sharp_noiseEst_mode_i.
27	RO	0x0	hw_sharp_localGain_bypass_shd The shadow register of hw_sharp_localGain_bypass_i.
26	RO	0x0	hw_sharp_noiseCurve_mode_shd The shadow register of hw_sharp_noiseCurve_mode_i.
25:15	RO	0x000	reserved

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Bit	Attr	Reset Value	Description
14:12	RW	0x0	hw_sharp_debug_mode SHARP debug mode 3'b000: sharp out data 3'b001: texture weight 3'b010: detail local weight 3'b011: edge pos weight 3'b100: detail pos scale 3'b101: detail pos thred
11	RO	0x0	reserved
10	RW	0x0	sw_detail_lp_en Close detail layer operation for low power mode.
9	RW	0x0	hw_sharp_gainWgt_mode the mode of gain weight generation method 1'b1: use noise balance curve 1'b0: use manually configured curve
8	RW	0x0	hw_sharp_noiseCurve_mode_i the mode of noise curve configuration 1'b1: use outside config curve 1'b0: use hardware statistics curve
7	RW	0x0	hw_sharp_radiusStep_mode The step of distance curve. 1'b1: 256 1'b0: 128
6	RW	0x0	hw_sharp_noiseCalc_mode SHARP noise calculate mode 1'b1: 5x5 mode 1'b0: 3x3 mode
5	RW	0x0	hw_sharp_detailFusionWgt_mode the output mode of detail fusion weight. 1'b1: The larger the texture weight, the smaller the weight of using hi_hf 1'b0: The larger the texture weight, the greater the weight of using hi_hf
4	RW	0x0	hw_sharp_maxminFlt_mode SHARP maxmin filter mode 1'b1: 7x7 mode 1'b0: 5x5 mode
3	RW	0x0	hw_sharp_texEst_mode_i SHARP derivative estiamtion mode 1'b1: 7x7 mode 1'b0: 5x5 mode
2	RW	0x0	hw_sharp_localGain_bypass_i SHARP gain bypass enable signal 1'b1: enable 1'b0: disable
1	RW	0x0	hw_sharp_bypass_en_i SHARP bypass enable signal 1'b1: enable 1'b0: disable
0	RW	0x0	hw_sharp_en_i SHARP enable signal 1'b1: enable 1'b0: disable

ISP_SHARP_2900_TEXTURE0

Address: Operational Base(0x21D02900) + offset (0x0004)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	hw_sharp_fstSigma_scale The noise scale of denominator when calculating first-order derivative weight Fixed-point:[0,10,6]
15:0	RW	0x0000	hw_sharp_fstNoise_scale The noise scale value when calculating the first-order derivative weight Fixed-point:[0,10,6]

ISP_SHARP_2900_TEXTURE1

Address: Operational Base(0x21D02900) + offset (0x0008)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0000	hw_sharp_fstWgt_scale the scaling coefficient of first-order derivative weight Fixed-point:[0,5,10]
15:0	RW	0x0000	hw_sharp_fstSigma_offset The noise offset of denominator when calculating first-order derivative weight Fixed-point:[0,16,0]

ISP_SHARP_2900_TEXTURE2

Address: Operational Base(0x21D02900) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:12	RW	0x00	hw_sharp_noiseEst_alpha the alpha of noise estimation method Range: [0,32] Fixed-point:[0,1,5]
11:10	RO	0x0	reserved
9:8	RW	0x0	hw_sharp_texWgt_mode SHARP texture weight output mode 2'b00:fst_wgt * sec_wgt 2'b01:fst_wgt 2'b10:sec_wgt 2'b11: texture weight off Fixed-point:[0,2,0]
7:0	RO	0x00	reserved

ISP_SHARP_2900_TEXTURE3

Address: Operational Base(0x21D02900) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	hw_sharp_secSigma_scale The noise scale of denominator when calculating second-order derivative weight Fixed-point:[0,10,6]
15:0	RW	0x0000	hw_sharp_secNoise_scale The noise scale value when calculating the second-order derivative weight Fixed-point:[0,10,6]

ISP_SHARP_2900_TEXTURE4

Address: Operational Base(0x21D02900) + offset (0x0014)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
30:16	RW	0x0000	hw_sharp_secWgt_scale the scaling coefficient of second-order derivative weight Fixed-point:[0,5,10]
15:0	RW	0x0000	hw_sharp_secSigma_offset The noise offset of denominator when calculating second-order derivative weight Fixed-point:[0,16,0]

ISP_SHARP_2900_HPF_KERNEL0

Address: Operational Base(0x21D02900) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	hw_sharp_imgHpf_coeff0 5*5 high pass filter coefficient of center Notes: hw_sharp_imgHpf_coeff0+4*hw_sharp_imgHpf_coeff1+4*hw_sharp_imgHpf_coeff2+4*hw_sharp_imgHpf_coeff3+8*hw_sharp_imgHpf_coeff4+4*hw_sharp_imgHpf_coeff5 must be equal to 0
23:0	RO	0x000000	reserved

ISP_SHARP_2900_HPF_KERNEL1

Address: Operational Base(0x21D02900) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	hw_sharp_imgHpf_coeff4 5*5 high pass filter coefficient4
23:21	RO	0x0	reserved
20:16	RW	0x00	hw_sharp_imgHpf_coeff3 5*5 high pass filter coefficient2
15:14	RO	0x0	reserved
13:8	RW	0x00	hw_sharp_imgHpf_coeff2 5*5 high pass filter coefficient2
7:6	RO	0x0	reserved
5:0	RW	0x00	hw_sharp_imgHpf_coeff1 5*5 high pass filter coefficient1

ISP_SHARP_2900_TEXFLT_KERNEL

Address: Operational Base(0x21D02900) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	hw_sharp_texWgtFlt_coeff2 3*3 texture weight filter coefficient of corner
23:22	RO	0x0	reserved
21:16	RW	0x00	hw_sharp_texWgtFlt_coeff1 3*3 texture weight filter coefficient of up/down/left/right
15:14	RO	0x0	reserved
13:8	RW	0x00	hw_sharp_texWgtFlt_coeff0 3*3 texture weight filter coefficient of center Notes: hw_sharp_texWgtFlt_coeff0+4*hw_sharp_texWgtFlt_coeff1+4*hw_sharp_texWgtFlt_coeff2 must be equal to 64
7:5	RO	0x0	reserved
4:0	RW	0x00	hw_sharp_imgHpf_coeff5 5*5 high pass filter coefficient5

ISP_SHARP_2900_DETAIL0

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Address: Operational Base(0x21D02900) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	hw_sharp_fusionWgt_maxLimit The upper limit of detail fusion weight Fusion weight is equal to 0 when this bit set 0.
28	RW	0x0	hw_sharp_fusionWgt_minLimit The lower limit of detail fusion weight Fusion weight is equal to 1024 when this bit set 1.
27:26	RO	0x0	reserved
25:20	RW	0x00	hw_sharp_preBifilt_alpha The fusion alpha of input signal and 3x3 pre bilateral filter signal Range: [0,32] Fixed-point: [0,1,5]
19	RO	0x0	reserved
18:8	RW	0x000	hw_sharp_preBifilt_slope_fix The slope of the range weight curve Range: [0,1024] Fixed-point: [0,3,8]
7:6	RO	0x0	reserved
5:0	RW	0x00	hw_sharp_detailIn_alpha The fusion alpha of pre_y and hi_nr Range: [0,32] Fixed-point: [0,1,5]

ISP_SHARP_2900_LUMA_DX

Address: Operational Base(0x21D02900) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	hw_sharp_luma_dx6 Distance between point 6 and point 7. The actual distance is equal to 2^hw_sharp_luma_dx6
23:20	RW	0x0	hw_sharp_luma_dx5 Distance between point 5 and point 6. The actual distance is equal to 2^hw_sharp_luma_dx5
19:16	RW	0x0	hw_sharp_luma_dx4 Distance between point 4 and point 5. The actual distance is equal to 2^hw_sharp_luma_dx4
15:12	RW	0x0	hw_sharp_luma_dx3 Distance between point 3 and point 4. The actual distance is equal to 2^hw_sharp_luma_dx3
11:8	RW	0x0	hw_sharp_luma_dx2 Distance between point 2 and point 3. The actual distance is equal to 2^hw_sharp_luma_dx2
7:4	RW	0x0	hw_sharp_luma_dx1 Distance between point 1 and point 2. The actual distance is equal to 2^hw_sharp_luma_dx1
3:0	RW	0x0	hw_sharp_luma_dx0 Distance between point 0 and point 1. The actual distance is equal to 2^hw_sharp_luma_dx0 Notes: The total distance must be equal to 1024 Range: [1,9]

ISP_SHARP_2900_PBF_VSIGMA0

Address: Operational Base(0x21D02900) + offset (0x0030)

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Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	hw_sharp_preBifilt_vsigma_inv1 pre bilateral filter vsigma inverse1 Range: [0,16383]
15:14	RO	0x0	reserved
13:0	RW	0x0000	hw_sharp_preBifilt_vsigma_inv0 pre bilateral filter vsigma inverse0 Range: [0,16383]

ISP_SHARP_2900_PBF_VSIGMA1

Address: Operational Base(0x21D02900) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	hw_sharp_preBifilt_vsigma_inv3 pre bilateral filter vsigma inverse3 Range: [0,16383]
15:14	RO	0x0	reserved
13:0	RW	0x0000	hw_sharp_preBifilt_vsigma_inv2 pre bilateral filter vsigma inverse2 Range: [0,16383]

ISP_SHARP_2900_PBF_VSIGMA2

Address: Operational Base(0x21D02900) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	hw_sharp_preBifilt_vsigma_inv5 pre bilateral filter vsigma inverse5 Range: [0,16383]
15:14	RO	0x0	reserved
13:0	RW	0x0000	hw_sharp_preBifilt_vsigma_inv4 pre bilateral filter vsigma inverse4 Range: [0,16383]

ISP_SHARP_2900_PBF_VSIGMA3

Address: Operational Base(0x21D02900) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	hw_sharp_preBifilt_vsigma_inv7 pre bilateral filter vsigma inverse7 Range: [0,16383]
15:14	RO	0x0	reserved
13:0	RW	0x0000	hw_sharp_preBifilt_vsigma_inv6 pre bilateral filter vsigma inverse6 Range: [0,16383]

ISP_SHARP_2900_PBF_KERNEL

Address: Operational Base(0x21D02900) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x00	hw_sharp_preBifilt_coeff2 3*3 pre bilateral filter coefficient of corner
15:14	RO	0x0	reserved
13:8	RW	0x00	hw_sharp_preBifilt_coeff1 3*3 pre bilateral filter coefficient of up/down/left/right
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x00	hw_sharp_preBifilt_coeff0 3*3 pre bilateral filter coefficient of center Notes: hw_sharp_preBifilt_coeff0+4*hw_sharp_preBifilt_coeff1+4*hw_sharp_preBifilt_coeff2 must be equal to 64

ISP_SHARP_2900_DETAIL_KERNEL0

Address: Operational Base(0x21D02900) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	hw_sharp_hiDetailLpf_coeff3 5x5 hi_hf gaussian filter coefficient3
23:21	RO	0x0	reserved
20:16	RW	0x00	hw_sharp_hiDetailLpf_coeff2 5x5 hi_hf gaussian filter coefficient2
15:13	RO	0x0	reserved
12:8	RW	0x00	hw_sharp_hiDetailLpf_coeff1 5x5 hi_hf gaussian filter coefficient1
7	RO	0x0	reserved
6:0	RW	0x00	hw_sharp_hiDetailLpf_coeff0 5x5 hi_hf gaussian filter coefficient0 Notes: hw_sharp_hiDetailLpf_coeff0+4*hw_sharp_hiDetailLpf_coeff1+4*hw_sharp_hiDetailLpf_coeff2+4*hw_sharp_hiDetailLpf_coeff3+8*hw_sharp_hiDetailLpf_coeff4+4*hw_sharp_hiDetailLpf_coeff5 must be equal to 128

ISP_SHARP_2900_DETAIL_KERNEL1

Address: Operational Base(0x21D02900) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	hw_sharp_miDetailLpf_coeff1 5x5 mi_hf gaussian filter coefficient1
23	RO	0x0	reserved
22:16	RW	0x00	hw_sharp_miDetailLpf_coeff0 5x5 mi_hf gaussian filter coefficient0 Notes: hw_sharp_miDetailLpf_coeff0+4*hw_sharp_miDetailLpf_coeff1+4*hw_sharp_miDetailLpf_coeff2+4*hw_sharp_miDetailLpf_coeff3+8*hw_sharp_miDetailLpf_coeff4+4*hw_sharp_miDetailLpf_coeff5 must be equal to 128
15:12	RO	0x0	reserved
11:8	RW	0x0	hw_sharp_hiDetailLpf_coeff5 5x5 hi_hf gaussian filter coefficient5
7:4	RO	0x0	reserved
3:0	RW	0x0	hw_sharp_hiDetailLpf_coeff4 5x5 hi_hf gaussian filter coefficient4

ISP_SHARP_2900_DETAIL_KERNEL2

Address: Operational Base(0x21D02900) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	hw_sharp_miDetailLpf_coeff5 5x5 mi_hf gaussian filter coefficient5
23:20	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
19:16	RW	0x0	hw_sharp_miDetailLpf_coeff4 5x5 mi_hf gaussian filter coefficient4
15:12	RO	0x0	reserved
11:8	RW	0x0	hw_sharp_miDetailLpf_coeff3 5x5 mi_hf gaussian filter coefficient3
7:5	RO	0x0	reserved
4:0	RW	0x00	hw_sharp_miDetailLpf_coeff2 5x5 mi_hf gaussian filter coefficient2

ISP_SHARP_2900_GAIN

Address: Operational Base(0x21D02900) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	hw_sharp_localGain_scale Sharp local gain scale. Range: [0, 128] float range:[0, 1.0] Fixed-point: [0, 1, 7]
23:20	RO	0x0	reserved
19:16	RW	0x0	hw_sharp_gainMerge_alpha Sharp gain merge alpha. Range: [0, 8] float range:[0, 1.0] Fixed-point: [0, 1, 3]
15:10	RO	0x00	reserved
9:0	RW	0x000	hw_sharp_global_gain Sharp global gain Fixed-point: [0, 6, 4]

ISP_SHARP_2900_GAIN_ADJ0

Address: Operational Base(0x21D02900) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	hw_sharp_detailGain_minLimit the lower limit of detail gain weight The hw_sharp_detailGain_maxLimit must be bigger than hw_sharp_detailGain_minLimit. float range:[0, 1.99] Fixed-point:[0,1,7]
23:16	RW	0x00	hw_sharp_detailGain_maxLimit the upper limit of detail gain weight float range:[0, 1.99] Fixed-point:[0,1,7]
15:8	RW	0x00	hw_sharp_edgeGain_minLimit the lower limit of edge gain weight The hw_sharp_edgeGain_maxLimit must be bigger than hw_sharp_edgeGain_minLimit. float range:[0, 1.99] Fixed-point:[0,1,7]
7:0	RW	0x00	hw_sharp_edgeGain_maxLimit the upper limit of edge gain weight float range:[0, 1.99] Fixed-point:[0,1,7]

ISP_SHARP_2900_GAIN_ADJ1

Address: Operational Base(0x21D02900) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved
15:8	RW	0x00	hw_sharp_hitexGain_minLimit the lower limit of lossTexInHinr gain weight The hw_sharp_hitexGain_maxLimit must be bigger than hw_sharp_hitexGain_minLimit. float range:[0, 1.99] Fixed-point:[0,1,7]
7:0	RW	0x00	hw_sharp_hitexGain_maxLimit the upper limit of lossTexInHinr gain weight float range:[0, 1.99] Fixed-point:[0,1,7]

ISP_SHARP_2900_GAIN_ADJ2

Address: Operational Base(0x21D02900) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	hw_sharp_hitexGain_slope the slope of lossTexInHinr gain weight Fixed-point:[1, 4, 3]
15:8	RW	0x00	hw_sharp_detailGain_slope the slope of detail gain weight Fixed-point:[1, 4, 3]
7:0	RW	0x00	hw_sharp_edgeGain_slope the slope of edge gain weight Fixed-point:[1, 4, 3]

ISP_SHARP_2900_GAIN_ADJ3

Address: Operational Base(0x21D02900) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	hw_sharp_hitexGain_offset the gain offset of lossTexInHinr gain weight Fixed-point:[0, 6, 4]
19:10	RW	0x000	hw_sharp_detailGain_offset the gain offset of detail gain weight Fixed-point:[0, 6, 4]
9:0	RW	0x000	hw_sharp_edgeGain_offset the gain offset of edge gain weight Fixed-point:[0, 6, 4]

ISP_SHARP_2900_GAIN_ADJ4

Address: Operational Base(0x21D02900) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_sharp_detailGain_sigma the sigma of detail gain weight Fixed-point:[0, 1, 11]
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_sharp_edgeGain_sigma the sigma of edge gain weight Fixed-point:[0, 1, 11]

ISP_SHARP_2900_EDGE0

Address: Operational Base(0x21D02900) + offset (0x0068)

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Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_sharp_negEdgeWgt_scale The scaling coefficient for the estimated edge probability, as the x-value for the negative edge signal weight float range:[0, 1023] Fixed-point:[0, 10, 2]
15:12	RO	0x0	reserved
11:0	RW	0x000	hw_sharp_posEdgeWgt_scale The scaling coefficient for the estimated edge probability, as the x-value for the positive edge signal weight float range:[0, 1023] Fixed-point:[0, 10, 2]

ISP_SHARP_2900_EDGE1

Address: Operational Base(0x21D02900) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	hw_sharp_undershoot_alpha linear scaling ratio of the difference between edge undershoot signal and local extremum Range: [0, 32] Fixed-point:[0, 1, 5]
23:22	RO	0x0	reserved
21:16	RW	0x00	hw_sharp_overshoot_alpha linear scaling ratio of the difference between edge overshoot signal and local extremum Range: [0, 32] Fixed-point:[0, 1, 5]
15:14	RO	0x0	reserved
13:8	RW	0x00	hw_sharp_negEdge_strg negative edge global strength Fixed-point:[0, 4, 2]
7:6	RO	0x0	reserved
5:0	RW	0x00	hw_sharp_posEdge_strg positive edge global strength Fixed-point:[0, 4, 2]

ISP_SHARP_2900_EDGE_KERNEL0

Address: Operational Base(0x21D02900) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	hw_sharp_edgeBpf_coeff3 7x7 edge band pass filter coefficient3
23:22	RO	0x0	reserved
21:16	RW	0x00	hw_sharp_edgeBpf_coeff2 7x7 edge band pass filter coefficient2
15:14	RO	0x0	reserved
13:8	RW	0x00	hw_sharp_edgeBpf_coeff1 7x7 edge band pass filter coefficient1

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	hw_sharp_edgeBpf_coeff0 7x7 edge band pass filter coefficient0 Notes: hw_sharp_edgeBpf_coeff0+4*hw_sharp_edgeBpf_coeff1+4*hw_sharp_edgeBpf_coeff2+4*hw_sharp_edgeBpf_coeff3+8*hw_sharp_edgeBpf_coeff4+4*hw_sharp_edgeBpf_coeff5+4*hw_sharp_edgeBpf_coeff6+8*hw_sharp_edgeBpf_coeff7++8*hw_sharp_edgeBpf_coeff8 must be equal to 0

ISP_SHARP_2900_EDGE_KERNEL1

Address: Operational Base(0x21D02900) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	hw_sharp_edgeBpf_coeff7 7x7 edge band pass filter coefficient7
23:21	RO	0x0	reserved
20:16	RW	0x00	hw_sharp_edgeBpf_coeff6 7x7 edge band pass filter coefficient6
15:13	RO	0x0	reserved
12:8	RW	0x00	hw_sharp_edgeBpf_coeff5 7x7 edge band pass filter coefficien5
7:5	RO	0x0	reserved
4:0	RW	0x00	hw_sharp_edgeBpf_coeff4 7x7 edge band pass filter coefficient4

ISP_SHARP_2900_EDGE_KERNEL2

Address: Operational Base(0x21D02900) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:8	RW	0x00	hw_sharp_edgeBpf_coeff9 7x7 edge band pass filter coefficient9
7:5	RO	0x0	reserved
4:0	RW	0x00	hw_sharp_edgeBpf_coeff8 7x7 edge band pass filter coefficient8

ISP_SHARP_2900_EDGE_WGT_VAL0

Address: Operational Base(0x21D02900) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	hw_sharp_edgeWgt_val2 edge signal weight2 Fixed-point:[0, 10, 0]
19:10	RW	0x000	hw_sharp_edgeWgt_val1 edge signal weight1 Fixed-point:[0, 10, 0]
9:0	RW	0x000	hw_sharp_edgeWgt_val0 edge signal weight0 Fixed-point:[0, 10, 0]

ISP_SHARP_2900_EDGE_WGT_VAL1

Address: Operational Base(0x21D02900) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:20	RW	0x000	hw_sharp_edgeWgt_val5 edge signal weight5 Fixed-point:[0, 10, 0]
19:10	RW	0x000	hw_sharp_edgeWgt_val4 edge signal weight4 Fixed-point:[0, 10, 0]
9:0	RW	0x000	hw_sharp_edgeWgt_val3 edge signal weight3 Fixed-point:[0, 10, 0]

ISP_SHARP_2900_EDGE_WGT_VAL2

Address: Operational Base(0x21D02900) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	hw_sharp_edgeWgt_val8 edge signal weight8 Fixed-point:[0, 10, 0]
19:10	RW	0x000	hw_sharp_edgeWgt_val7 edge signal weight7 Fixed-point:[0, 10, 0]
9:0	RW	0x000	hw_sharp_edgeWgt_val6 edge signal weight6 Fixed-point:[0, 10, 0]

ISP_SHARP_2900_EDGE_WGT_VAL3

Address: Operational Base(0x21D02900) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	hw_sharp_edgeWgt_val11 edge signal weight11 Fixed-point:[0, 10, 0]
19:10	RW	0x000	hw_sharp_edgeWgt_val10 edge signal weight10 Fixed-point:[0, 10, 0]
9:0	RW	0x000	hw_sharp_edgeWgt_val9 edge signal weight9 Fixed-point:[0, 10, 0]

ISP_SHARP_2900_EDGE_WGT_VAL4

Address: Operational Base(0x21D02900) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	hw_sharp_edgeWgt_val14 edge signal weight14 Fixed-point:[0, 10, 0]
19:10	RW	0x000	hw_sharp_edgeWgt_val13 edge signal weight14 Fixed-point:[0, 10, 0]
9:0	RW	0x000	hw_sharp_edgeWgt_val12 edge signal weight12 Fixed-point:[0, 10, 0]

ISP_SHARP_2900_EDGE_WGT_VAL5

Address: Operational Base(0x21D02900) + offset (0x0090)

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Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:10	RW	0x000	hw_sharp_edgeWgt_val16 edge signal weight16 Fixed-point:[0, 10, 0]
9:0	RW	0x000	hw_sharp_edgeWgt_val15 edge signal weight15 Fixed-point:[0, 10, 0]

ISP_SHARP_2900_LUMA_ADJ_STRG0

Address: Operational Base(0x21D02900) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	hw_sharp_luma2strg_val3 the brightness weight3 mapped by lo_nr hw_sharp_luma2strg_val3 corresponds to endpoint hw_sharp_luma2Tab_idx3 Range: [0, 128] Fixed-point:[0, 1, 7]
23:16	RW	0x00	hw_sharp_luma2strg_val2 the brightness weight2 mapped by lo_nr hw_sharp_luma2strg_val2 corresponds to endpoint hw_sharp_luma2Tab_idx2 Range: [0, 128] Fixed-point:[0, 1, 7]
15:8	RW	0x00	hw_sharp_luma2strg_val1 the brightness weight1 mapped by lo_nr hw_sharp_luma2strg_val1 corresponds to endpoint hw_sharp_luma2Tab_idx1 Range: [0, 128] Fixed-point:[0, 1, 7]
7:0	RW	0x00	hw_sharp_luma2strg_val0 the brightness weight0 mapped by lo_nr hw_sharp_luma2strg_val0 corresponds to endpoint hw_sharp_luma2Tab_idx0 Range: [0, 128] Fixed-point:[0, 1, 7]

ISP_SHARP_2900_LUMA_ADJ_STRG1

Address: Operational Base(0x21D02900) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	hw_sharp_luma2strg_val7 the brightness weight7 mapped by lo_nr hw_sharp_luma2strg_val7 corresponds to endpoint hw_sharp_luma2Tab_idx7 Range: [0, 128] Fixed-point:[0, 1, 7]
23:16	RW	0x00	hw_sharp_luma2strg_val6 the brightness weight6 mapped by lo_nr hw_sharp_luma2strg_val6 corresponds to endpoint hw_sharp_luma2Tab_idx6 Range: [0, 128] Fixed-point:[0, 1, 7]

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	hw_sharp_luma2strg_val5 the brightness weight5 mapped by lo_nr hw_sharp_luma2strg_val5 corresponds to endpoint hw_sharp_luma2Tab_idx5 Range: [0, 128] Fixed-point:[0, 1, 7]
7:0	RW	0x00	hw_sharp_luma2strg_val4 the brightness weight4 mapped by lo_nr hw_sharp_luma2strg_val4 corresponds to endpoint hw_sharp_luma2Tab_idx4 Range: [0, 128] Fixed-point:[0, 1, 7]

ISP_SHARP_2900_CENTER

Address: Operational Base(0x21D02900) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	hw_sharp_center_y center ypos Fixed-point:[0,13,0]
15:13	RO	0x0	reserved
12:0	RW	0x0000	hw_sharp_center_x center xpos Fixed-point:[0,13,0]

ISP_SHARP_2900_OUT_LIMIT

Address: Operational Base(0x21D02900) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	hw_sharp_edge_minLimit the lower limit value of edge area The hw_sharp_edge_minLimit must be bigger than hw_sharp_flat_maxLimit. Range: [1, 1023] Fixed-point:[0, 10, 0]
15:10	RO	0x00	reserved
9:0	RW	0x000	hw_sharp_flat_maxLimit the upper limit value of flat area Range: [1, 1022] Fixed-point:[0, 10, 0]

ISP_SHARP_2900_TEX_X_INV_FIX0

Address: Operational Base(0x21D02900) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:0	RW	0x000000	hw_tex_x_inv_fix0 equal to (1<<22/hw_sharp_flat_maxLimit)

ISP_SHARP_2900_TEX_X_INV_FIX1

Address: Operational Base(0x21D02900) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:0	RW	0x000000	hw_tex_x_inv_fix1 equal to (1<<22/(hw_sharp_edge_minLimit - hw_sharp_flat_maxLimit))

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ISP_SHARP_2900_TEX_X_INV_FIX2

Address: Operational Base(0x21D02900) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:23	RO	0x000	reserved
22:0	RW	0x000000	hw_tex_x_inv_fix2 equal to (1<<22/(1024-hw_sharp_edge_minLimit))

ISP_SHARP_2900_LOCAL_STRG1

Address: Operational Base(0x21D02900) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	hw_sharp_tex2lossTexInHinrStrg_val1 The local weight of the lossTexInHinr layer generated based on texture weight, with an x-axis of [0, hw_sharp_flat_maxLimit, hw_sharp_edge_minLimit, 1024] hw_sharp_tex2lossTexInHinrStrg_val1 corresponds to endpoint hw_sharp_flat_maxLimit Range: [0, 1023] Fixed-point:[0, 1, 10]
19:10	RW	0x000	hw_sharp_tex2lossTexInHinrStrg_val0 The local weight of the lossTexInHinr layer generated based on texture weight, with an x-axis of [0, hw_sharp_flat_maxLimit, hw_sharp_edge_minLimit, 1024] hw_sharp_tex2lossTexInHinrStrg_val0 corresponds to endpoint 0 Range: [0, 1023] Fixed-point:[0, 1, 10]
9:0	RO	0x000	reserved

ISP_SHARP_2900_LOCAL_STRG2

Address: Operational Base(0x21D02900) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:10	RW	0x000	hw_sharp_tex2lossTexInHinrStrg_val3 The local weight of the lossTexInHinr layer generated based on texture weight, with an x-axis of [0, hw_sharp_flat_maxLimit, hw_sharp_edge_minLimit, 1024] hw_sharp_tex2lossTexInHinrStrg_val3 corresponds to endpoint 1024 Range: [0, 1023] Fixed-point:[0, 1, 10]
9:0	RW	0x000	hw_sharp_tex2lossTexInHinrStrg_val2 The local weight of the lossTexInHinr layer generated based on texture weight, with an x-axis of [0, hw_sharp_flat_maxLimit, hw_sharp_edge_minLimit, 1024] hw_sharp_tex2lossTexInHinrStrg_val2 corresponds to endpoint hw_sharp_edge_minLimit Range: [0, 1023] Fixed-point:[0, 1, 10]

ISP_SHARP_2900_DETAIL_SCALE_TAB0

Address: Operational Base(0x21D02900) + offset (0x00C0)

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	hw_sharp_contrast2posStrg_val3 the scale3 of detail positive signal based on local dynamic range hw_sharp_contrast2posStrg_val3 corresponds to endpoint contrast = 384 Fixed-point:[0, 1, 7]
23:16	RW	0x00	hw_sharp_contrast2posStrg_val2 the scale2 of detail positive signal based on local dynamic range hw_sharp_contrast2posStrg_val2 corresponds to endpoint contrast = 256 Fixed-point:[0, 1, 7]
15:8	RW	0x00	hw_sharp_contrast2posStrg_val1 the scale1 of detail positive signal based on local dynamic range hw_sharp_contrast2posStrg_val1 corresponds to endpoint contrast = 128 Fixed-point:[0, 1, 7]
7:0	RW	0x00	hw_sharp_contrast2posStrg_val0 the scale0 of detail positive signal based on local dynamic range hw_sharp_contrast2posStrg_val0 corresponds to endpoint contrast = 0 Fixed-point:[0, 1, 7]

ISP_SHARP_2900_DETAIL_SCALE_TAB1

Address: Operational Base(0x21D02900) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	hw_sharp_contrast2posStrg_val7 the scale7 of detail positive signal based on local dynamic range hw_sharp_contrast2posStrg_val7 corresponds to endpoint contrast = 896 Fixed-point:[0, 1, 7]
23:16	RW	0x00	hw_sharp_contrast2posStrg_val6 the scale6 of detail positive signal based on local dynamic range hw_sharp_contrast2posStrg_val6 corresponds to endpoint contrast = 768 Fixed-point:[0, 1, 7]
15:8	RW	0x00	hw_sharp_contrast2posStrg_val5 the scale5 of detail positive signal based on local dynamic range hw_sharp_contrast2posStrg_val5 corresponds to endpoint contrast = 640 Fixed-point:[0, 1, 7]
7:0	RW	0x00	hw_sharp_contrast2posStrg_val4 the scale4 of detail positive signal based on local dynamic range hw_sharp_contrast2posStrg_val4 corresponds to endpoint contrast = 512 Fixed-point:[0, 1, 7]

ISP_SHARP_2900_DETAIL_SCALE_TAB2

Address: Operational Base(0x21D02900) + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RW	0x00	hw_sharp_posDetail_strg positive detail global strength Fixed-point:[0, 4, 2]

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	hw_sharp_contrast2posStrg_val8 the scale8 of detail positive signal based on local dynamic range hw_sharp_contrast2posStrg_val8 corresponds to endpoint contrast = 1024 Fixed-point:[0, 1, 7]

ISP_SHARP_2900_DETAIL_SCALE_TAB3

Address: Operational Base(0x21D02900) + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	hw_sharp_contrast2negStrg_val3 the scale3 of detail negativesignal based on local dynamic range hw_sharp_contrast2negStrg_val3 corresponds to endpoint contrast = 384 Fixed-point:[0, 1, 7]
23:16	RW	0x00	hw_sharp_contrast2negStrg_val2 the scale2 of detail negativesignal based on local dynamic range hw_sharp_contrast2negStrg_val2 corresponds to endpoint contrast = 256 Fixed-point:[0, 1, 7]
15:8	RW	0x00	hw_sharp_contrast2negStrg_val1 the scale1 of detail negativesignal based on local dynamic range hw_sharp_contrast2negStrg_val1 corresponds to endpoint contrast = 128 Fixed-point:[0, 1, 7]
7:0	RW	0x00	hw_sharp_contrast2negStrg_val0 the scale0 of detail negativesignal based on local dynamic range hw_sharp_contrast2negStrg_val0 corresponds to endpoint contrast = 0 Fixed-point:[0, 1, 7]

ISP_SHARP_2900_DETAIL_SCALE_TAB4

Address: Operational Base(0x21D02900) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	hw_sharp_contrast2negStrg_val7 the scale7 of detail negativesignal based on local dynamic range hw_sharp_contrast2negStrg_val7 corresponds to endpoint contrast = 896 Fixed-point:[0, 1, 7]
23:16	RW	0x00	hw_sharp_contrast2negStrg_val6 the scale6 of detail negativesignal based on local dynamic range hw_sharp_contrast2negStrg_val6 corresponds to endpoint contrast = 768 Fixed-point:[0, 1, 7]
15:8	RW	0x00	hw_sharp_contrast2negStrg_val5 the scale5 of detail negativesignal based on local dynamic range hw_sharp_contrast2negStrg_val5 corresponds to endpoint contrast = 640 Fixed-point:[0, 1, 7]
7:0	RW	0x00	hw_sharp_contrast2negStrg_val4 the scale4 of detail negativesignal based on local dynamic range hw_sharp_contrast2negStrg_val4 corresponds to endpoint contrast = 512 Fixed-point:[0, 1, 7]

ISP_SHARP_2900_DETAIL_SCALE_TAB5

Address: Operational Base(0x21D02900) + offset (0x00D4)

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Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:8	RW	0x00	hw_sharp_negDetail_strg negative detail global strength Fixed-point:[0, 4, 2]
7:0	RW	0x00	hw_sharp_contrast2negStrg_val8 the scale8 of detail negativesignal based on local dynamic range hw_sharp_contrast2negStrg_val8 corresponds to endpoint contrast = 1024 Fixed-point:[0, 1, 7]

ISP_SHARP_2900_DETAIL_TEX_CLIP0

Address: Operational Base(0x21D02900) + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	hw_sharp_tex2detailPosClip_val2 the clip val2 of positive detail signals based on texture weight hw_sharp_tex2detailPosClip_val2 corresponds to endpoint texture weight = 256 Fixed-point:[0, 10, 0]
19:10	RW	0x000	hw_sharp_tex2detailPosClip_val1 the clip val1 of positive detail signals based on texture weight hw_sharp_tex2detailPosClip_val1 corresponds to endpoint texture weight = 128 Fixed-point:[0, 10, 0]
9:0	RW	0x000	hw_sharp_tex2detailPosClip_val0 the clip val0 of positive detail signals based on texture weight hw_sharp_tex2detailPosClip_val0 corresponds to endpoint texture weight = 0 Fixed-point:[0, 10, 0]

ISP_SHARP_2900_DETAIL_TEX_CLIP1

Address: Operational Base(0x21D02900) + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	hw_sharp_tex2detailPosClip_val5 the clip va5 of positive detail signals based on texture weight hw_sharp_tex2detailPosClip_val5 corresponds to endpoint texture weight = 640 Fixed-point:[0, 10, 0]
19:10	RW	0x000	hw_sharp_tex2detailPosClip_val4 the clip va4 of positive detail signals based on texture weight hw_sharp_tex2detailPosClip_val4 corresponds to endpoint texture weight = 512 Fixed-point:[0, 10, 0]
9:0	RW	0x000	hw_sharp_tex2detailPosClip_val3 the clip va3 of positive detail signals based on texture weight hw_sharp_tex2detailPosClip_val3 corresponds to endpoint texture weight = 384 Fixed-point:[0, 10, 0]

ISP_SHARP_2900_DETAIL_TEX_CLIP2

Address: Operational Base(0x21D02900) + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:20	RW	0x000	hw_sharp_tex2detailPosClip_val8 the clip va8 of positive detail signals based on texture weight hw_sharp_tex2detailPosClip_val8 corresponds to endpoint texture weight = 1024 Fixed-point:[0, 10, 0]
19:10	RW	0x000	hw_sharp_tex2detailPosClip_val7 the clip va7 of positive detail signals based on texture weight hw_sharp_tex2detailPosClip_val7 corresponds to endpoint texture weight = 896 Fixed-point:[0, 10, 0]
9:0	RW	0x000	hw_sharp_tex2detailPosClip_val6 the clip va6 of positive detail signals based on texture weight hw_sharp_tex2detailPosClip_val6 corresponds to endpoint texture weight = 768 Fixed-point:[0, 10, 0]

ISP_SHARP_2900_DETAIL_TEX_CLIP3

Address: Operational Base(0x21D02900) + offset (0x00E4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	hw_sharp_tex2detailNegClip_val2 the clip val2 of negative detail signals based on texture weight hw_sharp_tex2detailNegClip_val2 corresponds to endpoint texture weight = 256 Fixed-point:[0, 10, 0]
19:10	RW	0x000	hw_sharp_tex2detailNegClip_val1 the clip val1 of negative detail signals based on texture weight hw_sharp_tex2detailNegClip_val1 corresponds to endpoint texture weight = 128 Fixed-point:[0, 10, 0]
9:0	RW	0x000	hw_sharp_tex2detailNegClip_val0 the clip val0 of negative detail signals based on texture weight hw_sharp_tex2detailNegClip_val0 corresponds to endpoint texture weight = 0 Fixed-point:[0, 10, 0]

ISP_SHARP_2900_DETAIL_TEX_CLIP4

Address: Operational Base(0x21D02900) + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	hw_sharp_tex2detailNegClip_val5 the clip val5 of negative detail signals based on texture weight hw_sharp_tex2detailNegClip_val5 corresponds to endpoint texture weight = 640 Fixed-point:[0, 10, 0]
19:10	RW	0x000	hw_sharp_tex2detailNegClip_val4 the clip val4 of negative detail signals based on texture weight hw_sharp_tex2detailNegClip_val4 corresponds to endpoint texture weight = 512 Fixed-point:[0, 10, 0]
9:0	RW	0x000	hw_sharp_tex2detailNegClip_val3 the clip val3 of negative detail signals based on texture weight hw_sharp_tex2detailNegClip_val3 corresponds to endpoint texture weight = 384 Fixed-point:[0, 10, 0]

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ISP_SHARP_2900_DETAIL_TEX_CLIP5

Address: Operational Base(0x21D02900) + offset (0x00EC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	hw_sharp_tex2detailNegClip_val8 the clip val8 of negative detail signals based on texture weight hw_sharp_tex2detailNegClip_val8 corresponds to endpoint texture weight = 1024 Fixed-point:[0, 10, 0]
19:10	RW	0x000	hw_sharp_tex2detailNegClip_val7 the clip val7 of negative detail signals based on texture weight hw_sharp_tex2detailNegClip_val7 corresponds to endpoint texture weight = 896 Fixed-point:[0, 10, 0]
9:0	RW	0x000	hw_sharp_tex2detailNegClip_val6 the clip val6 of negative detail signals based on texture weight hw_sharp_tex2detailNegClip_val6 corresponds to endpoint texture weight = 768 Fixed-point:[0, 10, 0]

ISP_SHARP_2900_GRAIN_TEX_CLIP0

Address: Operational Base(0x21D02900) + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	hw_sharp_tex2GrainPosClip_val2 the clip val2 of positive grain signals based on texture weight hw_sharp_tex2GrainPosClip_val2 corresponds to endpoint texture weight = 256 Fixed-point:[0, 10, 0]
19:10	RW	0x000	hw_sharp_tex2GrainPosClip_val1 the clip val1 of positive grain signals based on texture weight hw_sharp_tex2GrainPosClip_val1 corresponds to endpoint texture weight = 128 Fixed-point:[0, 10, 0]
9:0	RW	0x000	hw_sharp_tex2GrainPosClip_val0 the clip val0 of positive grain signals based on texture weight hw_sharp_tex2GrainPosClip_val0 corresponds to endpoint texture weight = 0 Fixed-point:[0, 10, 0]

ISP_SHARP_2900_GRAIN_TEX_CLIP1

Address: Operational Base(0x21D02900) + offset (0x00F4)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	hw_sharp_tex2GrainPosClip_val5 the clip val5 of positive grain signals based on texture weight hw_sharp_tex2GrainPosClip_val5 corresponds to endpoint texture weight = 640 Fixed-point:[0, 10, 0]
19:10	RW	0x000	hw_sharp_tex2GrainPosClip_val4 the clip val4 of positive grain signals based on texture weight hw_sharp_tex2GrainPosClip_val4 corresponds to endpoint texture weight = 512 Fixed-point:[0, 10, 0]

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	hw_sharp_tex2GrainPosClip_val3 the clip val3 of positive grain signals based on texture weight hw_sharp_tex2GrainPosClip_val3 corresponds to endpoint texture weight = 384 Fixed-point:[0, 10, 0]

ISP_SHARP_2900_GRAIN_TEX_CLIP2

Address: Operational Base(0x21D02900) + offset (0x00F8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	hw_sharp_tex2GrainPosClip_val8 the clip val8 of positive grain signals based on texture weight hw_sharp_tex2GrainPosClip_val8 corresponds to endpoint texture weight = 1024 Fixed-point:[0, 10, 0]
19:10	RW	0x000	hw_sharp_tex2GrainPosClip_val7 the clip val7 of positive grain signals based on texture weight hw_sharp_tex2GrainPosClip_val7 corresponds to endpoint texture weight = 896 Fixed-point:[0, 10, 0]
9:0	RW	0x000	hw_sharp_tex2GrainPosClip_val6 the clip val6 of positive grain signals based on texture weight hw_sharp_tex2GrainPosClip_val6 corresponds to endpoint texture weight = 768 Fixed-point:[0, 10, 0]

ISP_SHARP_2900_GRAIN_TEX_CLIP3

Address: Operational Base(0x21D02900) + offset (0x00FC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	hw_sharp_tex2GrainNegClip_val2 the clip val2 of negative grain signals based on texture weight hw_sharp_tex2GrainNegClip_val2 corresponds to endpoint texture weight = 256 Fixed-point:[0, 10, 0]
19:10	RW	0x000	hw_sharp_tex2GrainNegClip_val1 the clip val1 of negative grain signals based on texture weight hw_sharp_tex2GrainNegClip_val1 corresponds to endpoint texture weight = 128 Fixed-point:[0, 10, 0]
9:0	RW	0x000	hw_sharp_tex2GrainNegClip_val0 the clip val0 of negative grain signals based on texture weight hw_sharp_tex2GrainNegClip_val0 corresponds to endpoint texture weight = 0 Fixed-point:[0, 10, 0]

ISP_SHARP_2900_GRAIN_TEX_CLIP4

Address: Operational Base(0x21D02900) + offset (0x0100)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	hw_sharp_tex2GrainNegClip_val5 the clip val5 of negative grain signals based on texture weight hw_sharp_tex2GrainNegClip_val5 corresponds to endpoint texture weight = 640 Fixed-point:[0, 10, 0]

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Bit	Attr	Reset Value	Description
19:10	RW	0x000	hw_sharp_tex2GrainNegClip_val4 the clip val4 of negative grain signals based on texture weight hw_sharp_tex2GrainNegClip_val4 corresponds to endpoint texture weight = 512 Fixed-point:[0, 10, 0]
9:0	RW	0x000	hw_sharp_tex2GrainNegClip_val3 the clip val3 of negative grain signals based on texture weight hw_sharp_tex2GrainNegClip_val3 corresponds to endpoint texture weight = 384 Fixed-point:[0, 10, 0]

ISP_SHARP_2900_GRAIN_TEX_CLIP5

Address: Operational Base(0x21D02900) + offset (0x0104)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	hw_sharp_tex2GrainNegClip_val8 the clip val8 of negative grain signals based on texture weight hw_sharp_tex2GrainNegClip_val8 corresponds to endpoint texture weight = 1024 Fixed-point:[0, 10, 0]
19:10	RW	0x000	hw_sharp_tex2GrainNegClip_val7 the clip val7 of negative grain signals based on texture weight hw_sharp_tex2GrainNegClip_val7 corresponds to endpoint texture weight = 896 Fixed-point:[0, 10, 0]
9:0	RW	0x000	hw_sharp_tex2GrainNegClip_val6 the clip val6 of negative grain signals based on texture weight hw_sharp_tex2GrainNegClip_val6 corresponds to endpoint texture weight = 768 Fixed-point:[0, 10, 0]

ISP_SHARP_2900_DETAIL_LUMA_CLIP0

Address: Operational Base(0x21D02900) + offset (0x0108)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	hw_sharp_luma2detailPosClip_val2 the clip val2 of positive detail signals based on lo_nr hw_sharp_luma2detailPosClip_val2 corresponds to endpoint hw_sharp_luma2Tab_idx2 Fixed-point:[0, 10, 0]
19:10	RW	0x000	hw_sharp_luma2detailPosClip_val1 the clip val1 of positive detail signals based on lo_nr hw_sharp_luma2detailPosClip_val1 corresponds to endpoint hw_sharp_luma2Tab_idx1 Fixed-point:[0, 10, 0]
9:0	RW	0x000	hw_sharp_luma2detailPosClip_val0 the clip val0 of positive detail signals based on lo_nr hw_sharp_luma2detailPosClip_val0 corresponds to endpoint hw_sharp_luma2Tab_idx0 Fixed-point:[0, 10, 0]

ISP_SHARP_2900_DETAIL_LUMA_CLIP1

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Address: Operational Base(0x21D02900) + offset (0x010C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	hw_sharp_luma2detailPosClip_val5 the clip val5 of positive detail signals based on lo_nr hw_sharp_luma2detailPosClip_val5 corresponds to endpoint hw_sharp_luma2Tab_idx5 Fixed-point:[0, 10, 0]
19:10	RW	0x000	hw_sharp_luma2detailPosClip_val4 the clip val4 of positive detail signals based on lo_nr hw_sharp_luma2detailPosClip_val4 corresponds to endpoint hw_sharp_luma2Tab_idx4 Fixed-point:[0, 10, 0]
9:0	RW	0x000	hw_sharp_luma2detailPosClip_val3 the clip val3 of positive detail signals based on lo_nr hw_sharp_luma2detailPosClip_va3 corresponds to endpoint hw_sharp_luma2Tab_idx3 Fixed-point:[0, 10, 0]

ISP_SHARP_2900_DETAIL_LUMA_CLIP2

Address: Operational Base(0x21D02900) + offset (0x0110)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:10	RW	0x000	hw_sharp_luma2detailPosClip_val7 the clip val7 of positive detail signals based on lo_nr hw_sharp_luma2detailPosClip_val7 corresponds to endpoint hw_sharp_luma2Tab_idx7 Fixed-point:[0, 10, 0]
9:0	RW	0x000	hw_sharp_luma2detailPosClip_val6 the clip val6 of positive detail signals based on lo_nr hw_sharp_luma2detailPosClip_val6 corresponds to endpoint hw_sharp_luma2Tab_idx6 Fixed-point:[0, 10, 0]

ISP_SHARP_2900_DETAIL_LUMA_CLIP3

Address: Operational Base(0x21D02900) + offset (0x0114)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	hw_sharp_luma2detailNegClip_val2 the clip val2 of negative detail signals based on lo_nr Fixed-point:[0, 10, 0]
19:10	RW	0x000	hw_sharp_luma2detailNegClip_val1 the clip val1 of negative detail signals based on lo_nr Fixed-point:[0, 10, 0]
9:0	RW	0x000	hw_sharp_luma2detailNegClip_val0 the clip val0 of negative detail signals based on lo_nr Fixed-point:[0, 10, 0]

ISP_SHARP_2900_DETAIL_LUMA_CLIP4

Address: Operational Base(0x21D02900) + offset (0x0118)

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Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	hw_sharp_luma2detailNegClip_val5 the clip val5 of negative detail signals based on lo_nr Fixed-point:[0, 10, 0]
19:10	RW	0x000	hw_sharp_luma2detailNegClip_val4 the clip val4 of negative detail signals based on lo_nr Fixed-point:[0, 10, 0]
9:0	RW	0x000	hw_sharp_luma2detailNegClip_val3 the clip val3 of negative detail signals based on lo_nr Fixed-point:[0, 10, 0]

ISP_SHARP_2900_DETAIL_LUMA_CLIP5

Address: Operational Base(0x21D02900) + offset (0x011C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:10	RW	0x000	hw_sharp_luma2detailNegClip_val7 the clip val7 of negative detail signals based on lo_nr Fixed-point:[0, 10, 0]
9:0	RW	0x000	hw_sharp_luma2detailNegClip_val6 the clip val6 of negative detail signals based on lo_nr Fixed-point:[0, 10, 0]

ISP_SHARP_2900_GRAIN_STRG

Address: Operational Base(0x21D02900) + offset (0x0120)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	hw_sharp_grain_strg grain global strength Fixed-point:[0, 4, 2]

ISP_SHARP_2900_HUE_ADJ_TAB0

Address: Operational Base(0x21D02900) + offset (0x0124)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	hw_sharp_hue2strg_val2 local weight based on hue hw_sharp_hue2strg_val1 corresponds to endpoint hue = 256 float range:[0, 1.999] Range:[0, 1023] Fixed-point:[0, 1, 9]
19:10	RW	0x000	hw_sharp_hue2strg_val1 local weight based on hue hw_sharp_hue2strg_val1 corresponds to endpoint hue = 128 float range:[0, 1.999] Range:[0, 1023] Fixed-point:[0, 1, 9]
9:0	RW	0x000	hw_sharp_hue2strg_val0 local weight based on hue hw_sharp_hue2strg_val0 corresponds to endpoint hue = 0 float range:[0, 1.999] Range:[0, 1023] Fixed-point:[0, 1, 9]

ISP_SHARP_2900_HUE_ADJ_TAB1

Address: Operational Base(0x21D02900) + offset (0x0128)

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Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	hw_sharp_hue2strg_val5 local weight based on hue hw_sharp_hue2strg_val1 corresponds to endpoint hue = 640 float range:[0, 1.999] Range:[0, 1023] Fixed-point:[0, 1, 9]
19:10	RW	0x000	hw_sharp_hue2strg_val4 local weight based on hue hw_sharp_hue2strg_val1 corresponds to endpoint hue = 512 float range:[0, 1.999] Range:[0, 1023] Fixed-point:[0, 1, 9]
9:0	RW	0x000	hw_sharp_hue2strg_val3 local weight based on hue hw_sharp_hue2strg_val1 corresponds to endpoint hue = 384 float range:[0, 1.999] Range:[0, 1023] Fixed-point:[0, 1, 9]

ISP_SHARP_2900_HUE_ADJ_TAB2

Address: Operational Base(0x21D02900) + offset (0x012C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	hw_sharp_hue2strg_val8 local weight based on hue hw_sharp_hue2strg_val1 corresponds to endpoint hue = 1024 float range:[0, 1.999] Range:[0, 1023] Fixed-point:[0, 1, 9]
19:10	RW	0x000	hw_sharp_hue2strg_val7 local weight based on hue hw_sharp_hue2strg_val1 corresponds to endpoint hue = 896 float range:[0, 1.999] Range:[0, 1023] Fixed-point:[0, 1, 9]
9:0	RW	0x000	hw_sharp_hue2strg_val6 local weight based on hue hw_sharp_hue2strg_val1 corresponds to endpoint hue = 768 float range:[0, 1.999] Range:[0, 1023] Fixed-point:[0, 1, 9]

ISP_SHARP_2900_DISATANCE_ADJ0

Address: Operational Base(0x21D02900) + offset (0x0130)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	hw_sharp_distance2strg_val3 Radial distance weight based on the distance from the center point Range: [0, 128] Fixed-point:[0, 1, 7]
23:16	RW	0x00	hw_sharp_distance2strg_val2 Radial distance weight based on the distance from the center point Range: [0, 128] Fixed-point:[0, 1, 7]

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	hw_sharp_distance2strg_val1 Radial distance weight based on the distance from the center point Range: [0, 128] Fixed-point:[0, 1, 7]
7:0	RW	0x00	hw_sharp_distance2strg_val0 Radial distance weight based on the distance from the center point Range: [0, 128] distance_power2_ratio = [0, 8, 24, 56, 88, 120, 184, 248, 312, 376, 440] Fixed-point:[0, 1, 7]

ISP_SHARP_2900_DISATANCE_ADJ1

Address: Operational Base(0x21D02900) + offset (0x0134)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	hw_sharp_distance2strg_val7 Radial distance weight based on the distance from the center point Range: [0, 128] Fixed-point:[0, 1, 7]
23:16	RW	0x00	hw_sharp_distance2strg_val6 Radial distance weight based on the distance from the center point Range: [0, 128] Fixed-point:[0, 1, 7]
15:8	RW	0x00	hw_sharp_distance2strg_val5 Radial distance weight based on the distance from the center point Range: [0, 128] Fixed-point:[0, 1, 7]
7:0	RW	0x00	hw_sharp_distance2strg_val4 Radial distance weight based on the distance from the center point Range: [0, 128] Fixed-point:[0, 1, 7]

ISP_SHARP_2900_DISATANCE_ADJ2

Address: Operational Base(0x21D02900) + offset (0x0138)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:16	RW	0x00	hw_sharp_distance2strg_val10 Radial distance weight based on the distance from the center point Range: [0, 128] Fixed-point:[0, 1, 7]
15:8	RW	0x00	hw_sharp_distance2strg_val9 Radial distance weight based on the distance from the center point Range: [0, 128] Fixed-point:[0, 1, 7]
7:0	RW	0x00	hw_sharp_distance2strg_val8 Radial distance weight based on the distance from the center point Range: [0, 128] Fixed-point:[0, 1, 7]

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ISP_SHARP_2900_TEX2DETAIL_STRG0

Address: Operational Base(0x21D02900) + offset (0x013C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	hw_sharp_tex2detailStrg_val2 hw_sharp_tex2detailStrg_val2 corresponds to endpoint 256 Range: [0, 1023] Fixed-point:[0, 1, 10]
19:10	RW	0x000	hw_sharp_tex2detailStrg_val1 hw_sharp_tex2detailStrg_val1 corresponds to endpoint 128 Range: [0, 1023] Fixed-point:[0, 1, 10]
9:0	RW	0x000	hw_sharp_tex2detailStrg_val0 hw_sharp_tex2detailStrg_val0 corresponds to endpoint 0 Range: [0, 1023] Fixed-point:[0, 1, 10]

ISP_SHARP_2900_TEX2DETAIL_STRG1

Address: Operational Base(0x21D02900) + offset (0x0140)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	hw_sharp_tex2detailStrg_val5 hw_sharp_tex2detailStrg_val5 corresponds to endpoint 640 Range: [0, 1023] Fixed-point:[0, 1, 10]
19:10	RW	0x000	hw_sharp_tex2detailStrg_val4 hw_sharp_tex2detailStrg_val4 corresponds to endpoint 512 Range: [0, 1023] Fixed-point:[0, 1, 10]
9:0	RW	0x000	hw_sharp_tex2detailStrg_val3 hw_sharp_tex2detailStrg_val3 corresponds to endpoint 384 Range: [0, 1023] Fixed-point:[0, 1, 10]

ISP_SHARP_2900_TEX2DETAIL_STRG2

Address: Operational Base(0x21D02900) + offset (0x0144)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	hw_sharp_tex2detailStrg_val8 hw_sharp_tex2detailStrg_val8 corresponds to endpoint 1024 Range: [0, 1023] Fixed-point:[0, 1, 10]
19:10	RW	0x000	hw_sharp_tex2detailStrg_val7 hw_sharp_tex2detailStrg_val7 corresponds to endpoint 896 Range: [0, 1023] Fixed-point:[0, 1, 10]
9:0	RW	0x000	hw_sharp_tex2detailStrg_val6 hw_sharp_tex2detailStrg_val6 corresponds to endpoint 768 Range: [0, 1023] Fixed-point:[0, 1, 10]

ISP_SHARP_2900_NOISE_SIGMA0

Address: Operational Base(0x21D02900) + offset (0x0148)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
25:16	RW	0x000	hw_sharp_hi_tex_threshold1 noise threshold for lossTexInHinr hw_sharp_hi_tex_threshold0 corresponds to endpoint lo_nr = 128 Fixed-point:[0, 10, 0]
15:10	RO	0x00	reserved
9:0	RW	0x000	hw_sharp_hi_tex_threshold0 noise threshold for lossTexInHinr hw_sharp_hi_tex_threshold0 corresponds to endpoint lo_nr = 0 Fixed-point:[0, 10, 0]

ISP_SHARP_2900_NOISE_SIGMA1

Address: Operational Base(0x21D02900) + offset (0x014C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	hw_sharp_hi_tex_threshold3 noise threshold for lossTexInHinr hw_sharp_hi_tex_threshold0 corresponds to endpoint lo_nr = 384 Fixed-point:[0, 10, 0]
15:10	RO	0x00	reserved
9:0	RW	0x000	hw_sharp_hi_tex_threshold2 noise threshold for lossTexInHinr hw_sharp_hi_tex_threshold0 corresponds to endpoint lo_nr = 256 Fixed-point:[0, 10, 0]

ISP_SHARP_2900_NOISE_SIGMA2

Address: Operational Base(0x21D02900) + offset (0x0150)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	hw_sharp_hi_tex_threshold5 noise threshold for lossTexInHinr hw_sharp_hi_tex_threshold0 corresponds to endpoint lo_nr = 640 Fixed-point:[0, 10, 0]
15:10	RO	0x00	reserved
9:0	RW	0x000	hw_sharp_hi_tex_threshold4 noise threshold for lossTexInHinr hw_sharp_hi_tex_threshold0 corresponds to endpoint lo_nr = 512 Fixed-point:[0, 10, 0]

ISP_SHARP_2900_NOISE_SIGMA3

Address: Operational Base(0x21D02900) + offset (0x0154)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	hw_sharp_hi_tex_threshold7 noise threshold for lossTexInHinr hw_sharp_hi_tex_threshold0 corresponds to endpoint lo_nr = 896 Fixed-point:[0, 10, 0]
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	hw_sharp_hi_tex_threshold6 noise threshold for lossTexInHinr hw_sharp_hi_tex_threshold0 corresponds to endpoint lo_nr = 768 Fixed-point:[0, 10, 0]

ISP_SHARP_2900_NOISE_SIGMA4

Address: Operational Base(0x21D02900) + offset (0x0158)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	hw_sharp_hi_tex_threshold8 noise threshold for lossTexInHinr hw_sharp_hi_tex_threshold0 corresponds to endpoint lo_nr = 1024 Fixed-point:[0, 10, 0]

ISP_SHARP_2900_TEX2MFDETAIL_STRG0

Address: Operational Base(0x21D02900) + offset (0x015C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	hw_sharp_tex2mfDetailStrg_val2 hw_sharp_tex2mfDetailStrg_val2 corresponds to endpoint 256 Range: [0, 1023] Fixed-point:[0, 1, 10]
19:10	RW	0x000	hw_sharp_tex2mfDetailStrg_val1 hw_sharp_tex2mfDetailStrg_val1 corresponds to endpoint 128 Range: [0, 1023] Fixed-point:[0, 1, 10]
9:0	RW	0x000	hw_sharp_tex2mfDetailStrg_val0 hw_sharp_tex2mfDetailStrg_val0 corresponds to endpoint 0 Range: [0, 1023] Fixed-point:[0, 1, 10]

ISP_SHARP_2900_TEX2MIDETAIL_STRG1

Address: Operational Base(0x21D02900) + offset (0x0160)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	hw_sharp_tex2mfDetailStrg_val5 hw_sharp_tex2mfDetailStrg_val5 corresponds to endpoint 640 Range: [0, 1023] Fixed-point:[0, 1, 10]
19:10	RW	0x000	hw_sharp_tex2mfDetailStrg_val4 hw_sharp_tex2mfDetailStrg_val4 corresponds to endpoint 512 Range: [0, 1023] Fixed-point:[0, 1, 10]
9:0	RW	0x000	hw_sharp_tex2mfDetailStrg_val3 hw_sharp_tex2mfDetailStrg_val3 corresponds to endpoint 384 Range: [0, 1023] Fixed-point:[0, 1, 10]

ISP_SHARP_2900_TEX2MIDETAIL_STRG2

Address: Operational Base(0x21D02900) + offset (0x0164)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:20	RW	0x000	hw_sharp_tex2mfDetailStrg_va8 hw_sharp_tex2mfDetailStrg_val8 corresponds to endpoint 1024 Range: [0, 1023] Fixed-point:[0, 1, 10]
19:10	RW	0x000	hw_sharp_tex2mfDetailStrg_val7 hw_sharp_tex2mfDetailStrg_val7 corresponds to endpoint 896 Range: [0, 1023] Fixed-point:[0, 1, 10]
9:0	RW	0x000	hw_sharp_tex2mfDetailStrg_val6 hw_sharp_tex2mfDetailStrg_val6 corresponds to endpoint 768 Range: [0, 1023] Fixed-point:[0, 1, 10]

ISP_SHARP_2900_LOSSTEXINHINR_STRG

Address: Operational Base(0x21D02900) + offset (0x016C)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5:0	RW	0x00	hw_sharp_lossTexInHinr_strg lossTexInHinr global strength Fixed-point:[0, 4, 2]

ISP_SHARP_2900_NOISE_CURVE0

Address: Operational Base(0x21D02900) + offset (0x0170)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	hw_sharp_noise_curve_ext1 Noise curve of external configuration hw_sharp_noise_curve_ext1 corresponds to endpoint luma = 64 Fixed-point:[0, 11, 0]
15:11	RO	0x00	reserved
10:0	RW	0x000	hw_sharp_noise_curve_ext0 Noise curve of external configuration hw_sharp_noise_curve_ext0 corresponds to endpoint luma = 0 Fixed-point:[0, 11, 0]

ISP_SHARP_2900_NOISE_CURVE1

Address: Operational Base(0x21D02900) + offset (0x0174)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	hw_sharp_noise_curve_ext3 Noise curve of external configuration hw_sharp_noise_curve_ext3 corresponds to endpoint luma = 192 Fixed-point:[0, 11, 0]
15:11	RO	0x00	reserved
10:0	RW	0x000	hw_sharp_noise_curve_ext2 Noise curve of external configuration hw_sharp_noise_curve_ext2 corresponds to endpoint luma = 128 Fixed-point:[0, 11, 0]

ISP_SHARP_2900_NOISE_CURVE2

Address: Operational Base(0x21D02900) + offset (0x0178)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
26:16	RW	0x000	hw_sharp_noise_curve_ext5 Noise curve of external configuration hw_sharp_noise_curve_ext5 corresponds to endpoint luma = 320 Fixed-point:[0, 11, 0]
15:11	RO	0x00	reserved
10:0	RW	0x000	hw_sharp_noise_curve_ext4 Noise curve of external configuration hw_sharp_noise_curve_ext4 corresponds to endpoint luma = 256 Fixed-point:[0, 11, 0]

ISP_SHARP_2900_NOISE_CURVE3

Address: Operational Base(0x21D02900) + offset (0x017C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	hw_sharp_noise_curve_ext7 Noise curve of external configuration hw_sharp_noise_curve_ext7 corresponds to endpoint luma = 448 Fixed-point:[0, 11, 0]
15:11	RO	0x00	reserved
10:0	RW	0x000	hw_sharp_noise_curve_ext6 Noise curve of external configuration hw_sharp_noise_curve_ext6 corresponds to endpoint luma = 384 Fixed-point:[0, 11, 0]

ISP_SHARP_2900_NOISE_CURVE4

Address: Operational Base(0x21D02900) + offset (0x0180)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	hw_sharp_noise_curve_ext9 Noise curve of external configuration hw_sharp_noise_curve_ext9 corresponds to endpoint luma = 576 Fixed-point:[0, 11, 0]
15:11	RO	0x00	reserved
10:0	RW	0x000	hw_sharp_noise_curve_ext8 Noise curve of external configuration hw_sharp_noise_curve_ext8 corresponds to endpoint luma = 512 Fixed-point:[0, 11, 0]

ISP_SHARP_2900_NOISE_CURVE5

Address: Operational Base(0x21D02900) + offset (0x0184)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	hw_sharp_noise_curve_ext11 Noise curve of external configuration hw_sharp_noise_curve_ext11 corresponds to endpoint luma = 704 Fixed-point:[0, 11, 0]
15:11	RO	0x00	reserved
10:0	RW	0x000	hw_sharp_noise_curve_ext10 Noise curve of external configuration hw_sharp_noise_curve_ext10 corresponds to endpoint luma = 640 Fixed-point:[0, 11, 0]

ISP_SHARP_2900_NOISE_CURVE6

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Address: Operational Base(0x21D02900) + offset (0x0188)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	hw_sharp_noise_curve_ext13 Noise curve of external configuration hw_sharp_noise_curve_ext13 corresponds to endpoint luma = 832 Fixed-point:[0, 11, 0]
15:11	RO	0x00	reserved
10:0	RW	0x000	hw_sharp_noise_curve_ext12 Noise curve of external configuration hw_sharp_noise_curve_ext12 corresponds to endpoint luma = 768 Fixed-point:[0, 11, 0]

ISP_SHARP_2900_NOISE_CURVE7

Address: Operational Base(0x21D02900) + offset (0x018C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	hw_sharp_noise_curve_ext15 Noise curve of external configuration hw_sharp_noise_curve_ext15 corresponds to endpoint luma = 960 Fixed-point:[0, 11, 0]
15:11	RO	0x00	reserved
10:0	RW	0x000	hw_sharp_noise_curve_ext14 Noise curve of external configuration hw_sharp_noise_curve_ext14 corresponds to endpoint luma = 896 Fixed-point:[0, 11, 0]

ISP_SHARP_2900_NOISE_CURVE8

Address: Operational Base(0x21D02900) + offset (0x0190)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:20	RW	0x00	hw_sharp_noiseClip_scale The scaling ratio of noise statistics in the previous frame, used as a texture threshold Fixed-point:[0, 4, 4]
19:12	RW	0x00	hw_sharp_noiseCountThred_ratio The lower limit of the count of pixel when noise estimation float range:[0, 0.249], fix bits = 10 Range: [0, 255]
11	RO	0x0	reserved
10:0	RW	0x000	hw_sharp_noise_curve_ext16 Noise curve of external configuration hw_sharp_noise_curve_ext16 corresponds to endpoint luma = 1024 Fixed-point:[0, 11, 0]

ISP_SHARP_2900_NOISE_CLIP

Address: Operational Base(0x21D02900) + offset (0x0194)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
26:16	RW	0x000	hw_sharp_noiseClip_maxLimit the upper limit of noise estimation threshold The hw_sharp_noiseClip_maxLimit must be bigger than hw_sharp_noiseClip_minLimit. Fixed-point:[0, 11, 0]
15:11	RO	0x00	reserved
10:0	RW	0x000	hw_sharp_noiseClip_minLimit the lower limit of noise estimation threshold Fixed-point:[0, 11, 0]

ISP_SHARP_2900_EDGEWGTFLT_KERNEL

Address: Operational Base(0x21D02900) + offset (0x0198)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x00	hw_sharp_edgeWgtFlt_coeff2 3x3 edge wgt gaussian filter coefficient2
15:14	RO	0x0	reserved
13:8	RW	0x00	hw_sharp_edgeWgtFlt_coeff1 3x3 edge wgt gaussian filter coefficient1
7:6	RO	0x0	reserved
5:0	RW	0x00	hw_sharp_edgeWgtFlt_coeff0 3x3 edge wgt gaussian filter coefficient0 Notes: hw_sharp_edgeWgtFlt_coeff0+4*hw_sharp_edgeWgtFlt_coeff1+4*hw_sharp_edgeWgtFlt_coeff2 must be equal to 64

ISP_SHARP_2900_EDGE_GLOBAL_CLIP

Address: Operational Base(0x21D02900) + offset (0x01A0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	hw_sharp_negEdge_clip the global clip val of negative edge signals Fixed-point:[0,10,0]
19:10	RW	0x000	hw_sharp_posEdge_clip the global clip val of positive edge signals Fixed-point:[0,10,0]
9:0	RW	0x000	hw_sharp_edgeGlbClip_thred edge global clip threshold Fixed-point:[0,10,0]

ISP_SHARP_2900_MIDETAIL

Address: Operational Base(0x21D02900) + offset (0x01A4)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x00	hw_sharp_negMfDetail_strg negaitive middle detail global strength Fixed-point:[0, 4, 2]
15:14	RO	0x0	reserved
13:8	RW	0x00	hw_sharp_posMfDetail_strg positive middle detail global strength Fixed-point:[0, 4, 2]
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x00	hw_sharp_mfDetailData_alpha the fusion alpha of pre_y and hi_nr Range: [0,32] Fixed-point:[0,1,5]

ISP_SHARP_2900_MIDETAIL_CLIP

Address: Operational Base(0x21D02900) + offset (0x01A8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:10	RW	0x000	hw_sharp_mfDetailNeg_clip the global clip val of negative mfDetail signals Fixed-point:[0,10,0]
9:0	RW	0x000	hw_sharp_mfDetailPos_clip the global clip val of positive mfDetail signals Fixed-point:[0,10,0]

ISP_SHARP_2900_SATURATION_STRG0

Address: Operational Base(0x21D02900) + offset (0x01AC)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	hw_sharp_saturation2strg_val3 local weight based on saturation hw_sharp_saturation2strg_val3 corresponds to endpoint saturation= 192 Fixed-point:[0, 1, 4]
23:21	RO	0x0	reserved
20:16	RW	0x00	hw_sharp_saturation2strg_val2 local weight based on saturation hw_sharp_saturation2strg_val2 corresponds to endpoint saturation= 128 Fixed-point:[0, 1, 4]
15:13	RO	0x0	reserved
12:8	RW	0x00	hw_sharp_saturation2strg_val1 local weight based on saturation hw_sharp_saturation2strg_val1 corresponds to endpoint saturation= 64 Fixed-point:[0, 1, 4]
7:5	RO	0x0	reserved
4:0	RW	0x00	hw_sharp_saturation2strg_val0 local weight based on saturation hw_sharp_saturation2strg_val0 corresponds to endpoint saturation= 0 Fixed-point:[0, 1, 4]

ISP_SHARP_2900_SATURATION_STRG1

Address: Operational Base(0x21D02900) + offset (0x01B0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	hw_sharp_saturation2strg_val7 local weight based on saturation hw_sharp_saturation2strg_val7 corresponds to endpoint saturation= 448 Fixed-point:[0, 1, 4]
23:21	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
20:16	RW	0x00	hw_sharp_saturation2strg_val6 local weight based on saturation hw_sharp_saturation2strg_val6 corresponds to endpoint saturation= 384 Fixed-point:[0, 1, 4]
15:13	RO	0x0	reserved
12:8	RW	0x00	hw_sharp_saturation2strg_val5 local weight based on saturation hw_sharp_saturation2strg_val5 corresponds to endpoint saturation= 320 Fixed-point:[0, 1, 4]
7:5	RO	0x0	reserved
4:0	RW	0x00	hw_sharp_saturation2strg_val4 local weight based on saturation hw_sharp_saturation2strg_val4 corresponds to endpoint saturation= 256 Fixed-point:[0, 1, 4]

ISP_SHARP_2900_SATURATION_STRG2

Address: Operational Base(0x21D02900) + offset (0x01B4)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:8	RW	0x000	hw_sharp_loSaturation_strg Adjust the global strg in areas with a saturation less than 512 float range:[0, 1.999] Range:[0, 1023] Fixed-point:[0, 1, 9]
7:5	RO	0x0	reserved
4:0	RW	0x00	hw_sharp_saturation2strg_val8 local weight based on saturation hw_sharp_saturation2strg_val8 corresponds to endpoint saturation= 512 Fixed-point:[0, 1, 4]

44.4.2.24 LDCH_B3DMC

ISP_LDCH_3B00_LDCH_ADR_STS

Address: Operational Base(0x21D03B00) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_ldch_en_shd LDCH enable signal shadow read is ldch_en_shd write is sys_itself_force_upd
30	RO	0x0	ldch_working LDCH working status
29	RO	0x0	ldch_map_data_err LDCH error interrupt signal
28:26	RO	0x0	reserved
25:24	RW	0x0	sys_itself_lut_mode LDCH update mode 2'b00: Open frame_st and force update load lut mode 2'b11: soft control force update load lut mode Suggest use frame_end lut mode
23:9	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
8	RW	0x0	sw_ldch_lut_mode 1'b0: LDCH use frm_st update lut 1'b1: LDCH use frm_end update lut
7	RW	0x0	sw_ldch_map13p3_en 1'b1: Every 16bit in LDCH table consist of 13bit integers and 3bit decimals. 1'b0: Every 16bit in LDCH table consist of 12bit integers and 4bit decimals. Note: Only valid when sw_ldch_force_map_en is 1.
6	RW	0x0	sw_ldch_force_map_en When value is 1, the number of bits used for integer part or decimal part is configured by software. Always set to 0 for 1106.
5	RO	0x0	reserved
4	RW	0x0	sw_bic_mode_en 1'b0: LDCH use bilinear mode. 1'b1: LDCH use bicubic mode.
3	RW	0x0	sw_sample_avr_en 1'b0: Use UV values of the pixel on the left when YUV444->YUV422. 1'b1: Use average of the left and right UV values when YUV444->YUV422.
2	RO	0x0	reserved
1	RW	0x0	sw_ldch_frm_end_dis 1'b0: Use last_frm_end to be frm_end 1'b1: Use in_frm_end to be frm_end
0	RW	0x1	sw_ldch_en_i LDCH enable signal

ISP_LDCH_3B00_LDCH_BIC_TABLE0

Address: Operational Base(0x21D03B00) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_ldch_bic_table0 LDCH bicubic mode table0

ISP_LDCH_3B00_LDCH_BIC_TABLE1

Address: Operational Base(0x21D03B00) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_ldch_bic_table1 LDCH bicubic mode table1

ISP_LDCH_3B00_LDCH_BIC_TABLE2

Address: Operational Base(0x21D03B00) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_ldch_bic_table2 LDCH bicubic mode table2

ISP_LDCH_3B00_LDCH_BIC_TABLE3

Address: Operational Base(0x21D03B00) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_ldch_bic_table3 LDCH bicubic mode table3

ISP_LDCH_3B00_LDCH_BIC_TABLE4

Address: Operational Base(0x21D03B00) + offset (0x0014)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_ldch_bic_table4 LDCH bicubic mode table4

ISP_LDCH_3B00_LDCH_BIC_TABLE5

Address: Operational Base(0x21D03B00) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_ldch_bic_table5 LDCH bicubic mode table5

ISP_LDCH_3B00_LDCH_BIC_TABLE6

Address: Operational Base(0x21D03B00) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_ldch_bic_table6 LDCH bicubic mode table6

ISP_LDCH_3B00_LDCH_BIC_TABLE7

Address: Operational Base(0x21D03B00) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_ldch_bic_table7 LDCH bicubic mode table7

ISP_LDCH_3B00_LDCH_BIC_TABLE8

Address: Operational Base(0x21D03B00) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_ldch_bic_table8 LDCH bicubic mode table8

ISP_LDCH_3B00_LDCH_OUT_HSIZE

Address: Operational Base(0x21D03B00) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14:0	RW	0x0000	sw_ldch_out_hsize if ldch output hsize not equal input size,then use this reg

ISP_LDCH_3B00_B3DMCV_CTRL

Address: Operational Base(0x21D03B00) + offset (0x0080)

Bit	Attr	Reset Value	Description
31	RO	0x0	hw_btnr_mcv_en_shd B3dmcv enable shadow
30	RW	0x0	b3dmcv_working B3dmcv working
29:27	RO	0x0	reserved
26	RW	0x0	sys_itself_force_upd B3dmc itself force update
25:24	RW	0x0	sys_itself_lut_mode B3dmcv update mode 2'b00: Open frame_st and force update load lut mode 2'b11: soft control force update load lut mode Suggest use frame_end lut mode
23:13	RO	0x000	reserved
12	RW	0x0	b3mcv_map_data_err B3dmcv map data error flag
11:9	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
8	RW	0x0	sw_b3dmcv_force_map_en When value is 1, the number of bits used for integer part or decimal part is configured by software
7	RW	0x0	sw_b3dmcv_map13p3_en 1'b1: Every 16bit in b3dmcv table consist of 13bit integers and 3bit decimals. 1'b0: Every 16bit in b3dmcv table consist of 12bit integers and 4bit decimals. Note: Only valid when sw_b3dmcv_force_map_en is 1.
6:1	RO	0x00	reserved
0	RW	0x0	hw_btnr_mcv_en B3dmcv enable

ISP_LDCH_3B00_B3DMCV_WR_ADDR

Address: Operational Base(0x21D03B00) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_b3dmcv_wr_base B3dmcv write base addr
3:0	RO	0x0	reserved

ISP_LDCH_3B00_B3DMCV_WR_STRIDE

Address: Operational Base(0x21D03B00) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_b3dmcv_wr_stride B3dmcv write stride
3:0	RO	0x0	reserved

ISP_LDCH_3B00_B3DMCV_FFFF_OFF

Address: Operational Base(0x21D03B00) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x000	sw_b3dmcv_last_ffff_offset The mcv map last fff position, if it is equal to 0 ,then the position is small than 26th line. If it is bigger than 26, write the accurate line number.

ISP_LDCH_3B00_B3DMCH_ADR_STS

Address: Operational Base(0x21D03B00) + offset (0x00E0)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_b3dmch_en_shd B3dmch enable shd(read only) sys_itself_force_upd(write only)
30	RW	0x0	b3dmch_working B3dmch working
29	RW	0x0	b3dmch_map_data_err B3dmch error interrupt signal
28:26	RO	0x0	reserved
25:24	RW	0x0	sys_itself_lut_mode B3dmch update mode 2'b00: Open frame_st and force update load lut mode 2'b11: soft control force update load lut mode Suggest use frame_end lut mode
23:9	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
8	RW	0x0	sw_b3dmch_lut_mode 1'b0: B3dmch use frm_st update lut 1'b1: B3dmch use frm_end update lut
7	RW	0x0	sw_b3dmch_map13p3_en 1'b1: Every 16bit in b3dmch table consist of 13bit integers and 3bit decimals. 1'b0: Every 16bit in b3dmch table consist of 12bit integers and 4bit decimals. Note: Only valid when sw_b3dmch_force_map_en is 1.
6	RW	0x0	sw_b3dmch_force_map_en When value is 1, the number of bits used for integer part or decimal part is configured by software
5:1	RO	0x00	reserved
0	RW	0x0	sw_b3dmch_en B3dmch enable

ISP_LDCH_3B00_B3DMC_EXTBOUND1

Address: Operational Base(0x21D03B00) + offset (0x00E8)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	hw_btnr_mcItp_mode B3dmc interpolation mode for mch, mcv.
15:0	RW	0x0000	hw_btnr_mcWarpExtBound_offset B3dmc pixel value out of image border for mch, mcv.

44.4.2.25 GAIN

ISP_GAIN_3F00_CTRL

Address: Operational Base(0x21D03F00) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	gain_wctrl_working 1'b0: GAIN module is idle. 1'b1: GAIN module is working.
30:28	RO	0x0	reserved
27	RW	0x0	sw_gain2ddr_force_ack1 The backdoor for force GAIN to DDR ack to 1.
26:25	RW	0x0	sw_gain2ddr_mode 2'b00, 2'b11: 4x8 mode 2'b01: 2x8 mode 2'b10: 1x8 mode
24	RW	0x0	sw_gain2ddr_wr_en Global gain to DDR enable bit
23:21	RO	0x0	reserved
20	RW	0x0	sw_yuvme_gain_bypass_en YUVME gain bypass enable 1'b0: Enble YUVME gain when YUVME module and GAIN module is enabled. 1'b1: YUVME gain bypass when YUVME module and GAIN module is enabled.
19:17	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
16	RW	0x0	sw_dhaz_gain_bypass_en DEHAZE gain bypass enable 1'b0: Enble DEHAZE gain when DEHAZE module and GAIN module is enabled. 1'b1: DEHAZE gain bypass when DEHAZE module and GAIN module is enabled.
15:13	RO	0x0	reserved
12	RW	0x0	sw_adrc_gain_bypass_en ADRC gain bypass enable 1'b0: Enble ADRC gain when ADRC module and GAIN module is enabled. 1'b1: ADRC gain bypass when ADRC module and GAIN module is enabled.
11:10	RO	0x0	reserved
9	RW	0x0	sw_force_lsc_indly Back door for LSC INDLY module always on.
8	RW	0x0	sw_lsc_gain_bypass_en LSC gain bypass enable 1'b0: Enble LSC gain when LSC module and GAIN module is enabled. 1'b1: LSC gain bypass when LSC module and GAIN module is enabled.
7	RO	0x0	reserved
6	W1C	0x0	soft_rst_inter GAIN module itself soft reset
5	RW	0x0	sw_gain_dmard_mode_en In dma read mode, set this bit to 1 will save some power.
4	RW	0x0	sw_b3dnr_gain_bypass_en BAY3D gain bypass enable 1'b0: Enble BAY3D gain when BAY3D module and GAIN module is enabled. 1'b1: BAY3D gain bypass when BAY3D module and GAIN module is enabled.
3	RW	0x0	sw_gain_mp_pipe_dis Back door for main path delay module
2	RW	0x0	sw_gain_gate_always_on Back door for gating
1	RW	0x0	sw_mge_gain_bypass_en HDRMGE gain bypass enable 1'b0: Enble HDRMGE gain when HDRMGE module and GAIN module is enabled. 1'b1: HDRMGE gain bypass when HDRMGE module and GAIN module is enabled.
0	RW	0x0	sw_gain_en GAIN enable bit

ISP_GAIN_3F00_GAIN_G0

Address: Operational Base(0x21D03F00) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00040	sw_gain0 HDR merge gain0, [0/64, 262144/64] when sw_mge_gain_en high. Or sw_gain_init (this signal is 12.9, here replace12.6 low 3bit assert to 0)

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ISP_GAIN_3F00_GAIN_G1_G2

Address: Operational Base(0x21D03F00) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0040	sw_gain2 HDR merge gain2, [0/64, 16383/64]
15:14	RO	0x0	reserved
13:0	RW	0x0040	sw_gain1 HDR merge gain1, [0/64, 16383/64]

ISP_GAIN_3F00_FIFO_STATUS

Address: Operational Base(0x21D03F00) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17	RW	0x0	ro_x2yuvme_fifo_err YUVME gain FIFO read or write error
16	RO	0x0	ro_shp_gain_in_fifo_err SHARP gain in FIFO read or write error
15	RO	0x0	ro_cnr_gain_in_fifo_err CNR gain in FIFO read or write error
14:12	RO	0x0	ro_ynrgain_fifo_err YNR gain FIFO read or write error
11	RO	0x0	ro_adrc2dhaz_fifo ADRC2DHAZE gain FIFO read or write error
10	RO	0x0	ro_lsc2adrc_fifo_err LSC2ADRC gain FIFO read or write error
9	RO	0x0	ro_bay2lsc_fifo_err BAY3D2LSC gain FIFO read or write error
8	RO	0x0	ro_mgegain_fifo_err HDRMGE gain FIFO read or write error
7:6	RO	0x0	reserved
5	RO	0x0	ro_gain_out_v_end GAIN out vertical end
4	RO	0x0	reserved
3	RO	0x0	ro_adrc2dhaz_fifo_full ADRC2DEHAZE gain FIFO full flag
2	RO	0x0	ro_lsc2adrc_fifo_full LSC2ADRC gain FIFO full flag
1	RO	0x0	ro_bay2lsc_fifo_full BAY2LSC gain FIFO full flag
0	RO	0x0	ro_mgegain_fifo_full HDRMGE gain FIFO full flag

44.4.2.26 BILINEAR_SCALE

BILINEAR_SCALE_1000_SCALE_CTRL

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	sw_scl_422to420_en Scale from yuv422 to yuv420 enable.
29:15	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
14	RW	0x0	sw_scl_in_clip_en Use for 8K 1'b0: Disable scale in clip 1'b1: Enable scale in clip
13	RW	0x0	sw_scl_clip_en Use for 8K 1'b0: Disable scale out clip 1'b1: Enable scale out clip
12:4	RO	0x000	reserved
3	RW	0x0	sw_scale_vc_en 1'b0: Bypass vertical chrominance scaling unit 1'b1: Enable vertical chrominance scaling unit
2	RW	0x0	sw_scale_vy_en 1'b0: Bypass vertical luminance scaling unit 1'b1: Enable vertical luminance scaling unit
1	RW	0x0	sw_scale_hc_en 1'b0: Bypass horizontal chrominance scaling unit 1'b1: Enable horizontal chrominance scaling unit
0	RW	0x0	sw_scale_hy_en 1'b0: Bypass horizontal luminance scaling unit 1'b1: Enable horizontal luminance scaling unit

BILINEAR_SCALE_1000_SCALE_UPDATE

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	reserved
5	RW	0x1	sys_cfg_gen_upd 1'b1: Automatic register update at frame end enabled 1'b0: Automatic register update at frame end disabled
4	WO	0x0	sys_cfg_force_upd 1'b0: Nothing happens 1'b1: Update shadow registers
3:0	RO	0x0	reserved

BILINEAR_SCALE_1000_SCALE_SRC_SIZE

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_scale_src_height Scale height of source (input)
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_scale_src_width Scale width of source (input)

BILINEAR_SCALE_1000_SCALE_DST_SIZE

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_scale_dst_height Scale height of destination (output)
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_scale_dst_width Scale width of destination (output)

BILINEAR_SCALE_1000_SCALE_HY_FAC

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Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00000	sw_scale_hy_fac This register is set to the horizontal luminance scaling factor. Fixed-point: [0, 6, 12] Bilinear: (src_width - 1) / (dst_width - 1)) = scale The value of the sw_scale_hy_fac register then has to be int(scale * 2^12).

BILINEAR_SCALE_1000_SCALE_HC_FAC

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00000	sw_scale_hc_fac This register is set to the horizontal luminance scaling factor. Fixed-point: [0, 6, 12] Bilinear: ((src_width / 2) - 1) / ((dst_width / 2) - 1)) = scale The value of the sw_scale_hc_fac register then has to be int(scale * 2^12).

BILINEAR_SCALE_1000_SCALE_VY_FAC

Address: **Operational Base** + offset (0x0018)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00000	sw_scale_vy_fac This register is set to the horizontal luminance scaling factor. Fixed-point: [0, 6, 12] Bilinear: (src_height - 1) / (dst_height - 1)) = scale The value of the sw_scale_vy_fac register then has to be int(scale * 2^12).

BILINEAR_SCALE_1000_SCALE_VC_FAC

Address: **Operational Base** + offset (0x001C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00000	sw_scale_vc_fac This register is set to the horizontal luminance scaling factor. Fixed-point: [0, 6, 12] Bilinear: If sw_scl_422to420_en = 0, (src_height - 1) / (dst_height - 1)) = scale Else (src_height - 1) / ((dst_height / 2) - 1)) = scale The value of the sw_scale_vc_fac register then has to be int(scale * 2^12).

BILINEAR_SCALE_1000_SCALE_HY_OFFS

Address: **Operational Base** + offset (0x0020)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x000	sw_scale_hy_offs This register is set to the horizontal luminance scaling coordinate offset (0~1) for bilinear. Fixed-point: [0, 0, 12]

BILINEAR_SCALE_1000_SCALE_HC_OFFS

Address: **Operational Base** + offset (0x0024)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	sw_scale_hc_offs This register is set to the horizontal chrominance scaling coordinate offset (0~1) for bilinear. Fixed-point: [0, 0, 12]

BILINEAR_SCALE_1000_SCALE_VY_OFFS

Address: **Operational Base** + offset (0x0028)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	sw_scale_vy_offs This register is set to the vertical luminance scaling coordinate offset (0~1) for bilinear. Fixed-point: [0, 0, 12]

BILINEAR_SCALE_1000_SCALE_VC_OFFS

Address: **Operational Base** + offset (0x002C)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	sw_scale_vc_offs This register is set to the vertical chrominance scaling coordinate offset (0~1) for bilinear. Fixed-point: [0, 0, 12]

BILINEAR_SCALE_1000_SCALE_HY_SIZE

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_scl_hy_size Scale out Y size, only works when sw_scl_clip_en equal to 1.

BILINEAR_SCALE_1000_SCALE_HC_SIZE

Address: **Operational Base** + offset (0x0044)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0000	sw_scl_hc_size Scale out UV size, only works when sw_scl_clip_en equal to 1.

BILINEAR_SCALE_1000_SCALE_HY_OFFS_MI

Address: **Operational Base** + offset (0x0048)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	sw_scl_hy_offs_mi The offset of first Y pixel in 128bit, which range from 0~15.

BILINEAR_SCALE_1000_SCALE_HC_OFFS_MI

Address: **Operational Base** + offset (0x004C)

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Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RW	0x0	sw_scl_hc_offs_mi The offset of first UV pixel in 128bit, which range from 0~15.

BILINEAR_SCALE_1000_SCALE_IN_CROP_OFFSET

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	sw_scl_in_hc_offs Scale in UV data cut some pixels if needed, only works when sw_scl_in_clip_en is effect. Read is shadow.
3:0	RW	0x0	sw_scl_in_hy_offs Scale in Y data cut some pixels if needed, only works when sw_scl_in_clip_en is effect. Read is shadow.

BILINEAR_SCALE_1000_SCALE_CTRL_SHD

Address: **Operational Base** + offset (0x0080)

Bit	Attr	Reset Value	Description
31:15	RO	0x00000	reserved
14	RO	0x0	sw_scl_in_clip_en_shd Use for 8K 1'b0: Disable scale in clip 1'b1: Enable scale in clip
13	RO	0x0	sw_scl_clip_en_shd Use for 8K 1'b0: Disable scale out clip 1'b1: Enable scale out clip
12:4	RO	0x000	reserved
3	RO	0x0	sw_scale_vc_en_shd 1'b0: Bypass vertical chrominance scaling unit 1'b1: Enable vertical chrominance scaling unit
2	RO	0x0	sw_scale_vy_en_shd 1'b0: Bypass vertical luminance scaling unit 1'b1: Enable vertical luminance scaling unit
1	RO	0x0	sw_scale_hc_en_shd 1'b0: Bypass horizontal chrominance scaling unit 1'b1: Enable horizontal chrominance scaling unit
0	RO	0x0	sw_scale_hy_en_shd 1'b0: Bypass horizontal luminance scaling unit 1'b1: Enable horizontal luminance scaling unit

BILINEAR_SCALE_1000_SCALE_SRC_SIZE_SHD

Address: **Operational Base** + offset (0x0088)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RO	0x0000	sw_scale_src_height_shd Scale height of source (input)
15:14	RO	0x0	reserved
13:0	RO	0x0000	sw_scale_src_width_shd Scale width of source (input)

BILINEAR_SCALE_1000_SCALE_DST_SIZE_SHD

Address: **Operational Base** + offset (0x008C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:16	RO	0x0000	sw_scale_dst_height_shd Scale height of destination(output)
15:14	RO	0x0	reserved
13:0	RO	0x0000	sw_scale_dst_width_shd Scale width of destination (output)

BILINEAR_SCALE_1000_SCALE_HY_FAC_SHD

Address: **Operational Base** + offset (0x0090)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	sw_scale_hy_fac_shd This register is set to the horizontal luminance scaling factor. Fixed-point: [0, 6, 12] Bilinear: (width_in - 1) / (width_out - 1)) = scale, The value of the sw_scale_hy_fac register then has to be int(scale * 2^12).

BILINEAR_SCALE_1000_SCALE_HC_FAC_SHD

Address: **Operational Base** + offset (0x0094)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	sw_scale_hc_fac_shd This register is set to the horizontal luminance scaling factor. Fixed-point: [0, 6, 12] Bilinear: ((width_in / 2) - 1) / ((width_out / 2) - 1)) = scale, The value of the sw_scale_hy_fac register then has to be int(scale * 2^12).

BILINEAR_SCALE_1000_SCALE_VY_FAC_SHD

Address: **Operational Base** + offset (0x0098)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	sw_scale_vy_fac_shd This register is set to the horizontal luminance scaling factor. Fixed-point: [0, 6, 12] Bilinear: (height_in - 1) / (height_out - 1)) = scale, The value of the sw_scale_hy_fac register then has to be int(scale * 2^12).

BILINEAR_SCALE_1000_SCALE_VC_FAC_SHD

Address: **Operational Base** + offset (0x009C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	sw_scale_vc_fac_shd This register is set to the horizontal luminance scaling factor. Fixed-point: [0, 6, 12] Bilinear: (height_in - 1) / (height_out - 1)) = scale, The value of the sw_scale_hy_fac register then has to be int(scale * 2^12).

BILINEAR_SCALE_1000_SCALE_HY_OFFS_SHD

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Address: **Operational Base** + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	sw_scale_hy_offs_shd This register is set to the horizontal luminance scaling coordinate offset (0~1) for bilinear. Fixed-point: [0, 0, 12]

BILINEAR_SCALE_1000_SCALE_HC_OFFS_SHD

Address: **Operational Base** + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	sw_scale_hc_offs_shd This register is set to the horizontal chrominance scaling coordinate offset (0~1) for bilinear. Fixed-point: [0, 0, 12]

BILINEAR_SCALE_1000_SCALE_VY_OFFS_SHD

Address: **Operational Base** + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	sw_scale_vy_offs_shd This register is set to the vertical luminance scaling coordinate offset (0~1) for bilinear. Fixed-point: [0, 0, 12]

BILINEAR_SCALE_1000_SCALE_VC_OFFS_SHD

Address: **Operational Base** + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RO	0x000	sw_scale_vc_offs_shd This register is set to the vertical chrominance scaling coordinate offset (0~1) for bilinear. Fixed-point: [0, 0, 12]

BILINEAR_SCALE_1000_SCALE_HY_SIZE_SHD

Address: **Operational Base** + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	sw_scl_hy_size_shd Scale out Y size shadow signal

BILINEAR_SCALE_1000_SCALE_HC_SIZE_SHD

Address: **Operational Base** + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	sw_scl_hc_size_shd Scale out UV size, only works when sw_scl_clip_en equal to 1.

BILINEAR_SCALE_1000_SCALE_HY_OFFS_MI_SHD

Address: **Operational Base** + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RO	0x0	sw_scl_hy_offs_mi_shd Shadow signal of sw_scl_hy_offs_mi

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BILINEAR_SCALE_1000_SCALE_HC_OFFS_MI_SHD

Address: **Operational Base** + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3:0	RO	0x0	sw_scl_hc_offs_mi_shd Shadow signal of sw_scl_hy_offs_mi

BILINEAR_SCALE_1000_SCALE_IN_CROP_OFFSET_SHD

Address: **Operational Base** + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RO	0x0	sw_scl_in_hc_offs_shd Scale in UV data cut some pixels if needed, only works when sw_scl_in_clip_en is effect. Read is shadow.
3:0	RO	0x0	sw_scl_in_hy_offs_shd Scale in Y data cut some pixels if needed, only works when sw_scl_in_clip_en is effect. Read is shadow.

44.4.2.27 DUAL_CROP

DUAL_CROP_0880_CTRL

Address: Operational Base(0x21D00880) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	in_upd_dis Input frame end update shadow registers disable 1'b0: update shadow with input frame end 1'b1: update shadow with output frame end Note: Since the input size is larger than the output size, the shadow registers should be updated with the input frame end.
30:29	RO	0x0	reserved
28	RO	0x0	regs_fbc_mode_shd regs_fbc_mode_shd Note: Shadow will only take effect when in_upd_dis is 0.
27:26	RO	0x0	regs_sp_mode_shd regs_sp_mode_shd Note: Shadow will only take effect when in_upd_dis is 0.
25:24	RO	0x0	regs_mp_mode_shd regs_mp_mode_shd Note: Shadow will only take effect when in_upd_dis is 0.
23:9	RO	0x0000	reserved
8	RW	0x0	regs_fbc_mode Fbc clipping enable signal
7	RO	0x0	reserved
6	RW	0x0	regs_gen_cfg_upd 1'b1: Generate frame synchronous configuration signal at the output of ISP for shadow registers of the following processing modules, write only
5	WO	0x0	regs_cfg_upd 1'b1: Immediately configure (update) shadow registers, write onlyd
4	WO	0x0	regs_gen_cfg_upd_fix 1'b1: Permanent configure (update) shadow registers on frame end

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	regs_sp_mode regs_sp_mode 2'b00: Bypass mode 2'b01: Yuv mode 2'b10: Rgb bayer mode 2'b11: Data mode
1:0	RW	0x0	regs_mp_mode regs_mp_mode 2'b00: Bypass mode 2'b01: Yuv mode 2'b10: Rgb bayer mode 2'b11: Data mode

DUAL_CROP_0880_M_H_OFFS

Address: Operational Base(0x21D00880) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0080	m_h_offs MP path h offset

DUAL_CROP_0880_M_V_OFFS

Address: Operational Base(0x21D00880) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0080	m_v_offs MP path v offset

DUAL_CROP_0880_M_H_SIZE

Address: Operational Base(0x21D00880) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0080	m_h_size MP path h size

DUAL_CROP_0880_M_V_SIZE

Address: Operational Base(0x21D00880) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0c00	m_v_size MP path v size

DUAL_CROP_0880_S_H_OFFS

Address: Operational Base(0x21D00880) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0080	s_h_offs SP path h offset

DUAL_CROP_0880_S_V_OFFS

Address: Operational Base(0x21D00880) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0080	s_v_offs SP path v offset

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DUAL_CROP_0880_S_H_SIZE

Address: Operational Base(0x21D00880) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0080	s_h_size SP path h size

DUAL_CROP_0880_S_V_SIZE

Address: Operational Base(0x21D00880) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0c00	s_v_size SP path v size

DUAL_CROP_0880_M_H_OFFS_SHD

Address: Operational Base(0x21D00880) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0080	m_h_offs_shd MP path h offset shadow signal

DUAL_CROP_0880_M_V_OFFS_SHD

Address: Operational Base(0x21D00880) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0080	m_v_offs_shd MP path v offset shadow signal

DUAL_CROP_0880_M_H_SIZE_SHD

Address: Operational Base(0x21D00880) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0080	m_h_size_shd MP path h size shadow signal

DUAL_CROP_0880_M_V_SIZE_SHD

Address: Operational Base(0x21D00880) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0000	m_v_size_shd MP path v size shadow signal

DUAL_CROP_0880_S_H_OFFS_SHD

Address: Operational Base(0x21D00880) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0080	s_h_offs_shd SP path h offset shadow signal

DUAL_CROP_0880_S_V_OFFS_SHD

Address: Operational Base(0x21D00880) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved

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Bit	Attr	Reset Value	Description
13:0	RO	0x0080	s_v_offs_shd SP path v offset shadow signal

DUAL_CROP_0880_S_H_SIZE_SHD

Address: Operational Base(0x21D00880) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0080	s_h_size_shd SP path h size shadow signal

DUAL_CROP_0880_S_V_SIZE_SHD

Address: Operational Base(0x21D00880) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RC	0x0080	s_v_size_shd SP path v size shadow signal

DUAL_CROP_0880_FBC_H_OFFS

Address: Operational Base(0x21D00880) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0080	fbc_h_offs FBC path h offset

DUAL_CROP_0880_FBC_V_OFFS

Address: Operational Base(0x21D00880) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0080	fbc_v_offs FBC path v offset

DUAL_CROP_0880_FBC_H_SIZE

Address: Operational Base(0x21D00880) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0080	fbc_h_size FBC path h size

DUAL_CROP_0880_FBC_V_SIZE

Address: Operational Base(0x21D00880) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0080	fbc_v_size FBC path v size

DUAL_CROP_0880_FBC_H_OFFS_SHD

Address: Operational Base(0x21D00880) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0080	fbc_h_offs_shd FBC path h offset shadow signal

DUAL_CROP_0880_FBC_V_OFF_SHD

Address: Operational Base(0x21D00880) + offset (0x0058)

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Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0080	fbc_v_offs_shd FBC path v offset shadow signal

DUAL_CROP_0880_FBC_H_SIZE_SHD

Address: Operational Base(0x21D00880) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0080	fbc_h_size_shd FBC path h size shadow signal

DUAL_CROP_0880_FBC_V_SIZE_SHD

Address: Operational Base(0x21D00880) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RO	0x0080	fbc_v_size_shd FBC path v size shadow signal

44.4.2.28 FLASH

ISP_FLASH_0660_CMD

Address: Operational Base(0x21D00660) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:3	RO	0x00000000	reserved
2	WO	0x0	preflash_on Preflash on 1'b0: No effect 1'b1: Flash delay counter is started at next trigger event No capture event is signaled to the sensor interface block.
1	WO	0x0	flash_on Flash on 1'b0: No effect 1'b1: Flash delay counter is started at next trigger event A capture event is signaled to the sensor interface block.
0	WO	0x0	prelight_on Prelight on 1'b0: Prelight is switched off at next trigger event 1'b1: Prelight is switched on at next trigger event --- ISP_FLASH_CMD --- Note: This is the command register for flash light and prelight activation. If the "rw" bits (e.g. "fl_cap_del") are re-programmed during operation, the following scheme shall be applied: i) Prelight is active (prelight_on = 1 has been set before): Every write access to this register shall use prelight_on = 1 (to prevent undesired switch off of the prelight). ii) Prelight is off: Every write access to this register shall use prelight_on = 0 (to prevent undesired switch on of the prelight).

ISP_FLASH_0660_CONFIG

Address: Operational Base(0x21D00660) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:4	RW	0x0	fl_cap_del Capture delay Frame number (0 to 15) to be captured after trigger event

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Bit	Attr	Reset Value	Description
3	RW	0x0	fl_trig_src Trigger source for flash and prelight 1'b0: Use vds_vsync for trigger event (with evaluation of vs_in_edge) 1'b1: Use fl_trig for trigger event (positive edge)
2	RW	0x0	fl_pol Polarity of flash related signals 1'b0: flash_trig, prelight_trig are high active 1'b1: flash_trig, prelight_trig are low active
1	RW	0x0	vs_in_edge VSYNC edge 1'b0: Use negative edge of "vds_vsync" if generating a trigger event 1'b1: Use positive edge of "vds_vsync" if generating a trigger event
0	RW	0x0	prelight_mode Prelight mode 1'b0: Prelight is switched off at begin of flash 1'b1: Prelight is switched off at end of flash

ISP_FLASH_0660_PREDIV

Address: Operational Base(0x21D00660) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x000	fl_pre_div Pre-divider for flush/preflash counter

ISP_FLASH_0660_DELAY

Address: Operational Base(0x21D00660) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00000	fl_delay Counter value for flash/preflash delay open_delay = (fl_delay + 1) * (fl_pre_div+1) / clk_isp fl_delay = (open_delay * clk_isp) / (fl_pre_div+1) - 1 --- ISP_FLASH_DELAY --- Note: Example: fl_delay = (10s * 100MHz) / (1023 + 1) C 1 = 976561

ISP_FLASH_0660_TIME

Address: Operational Base(0x21D00660) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RW	0x00000	fl_time Counter value for flash/preflash time open_time = (fl_time + 1) * (fl_pre_div+1) / clk_isp fl_time = (open_time * clk_isp) / (fl_pre_div+1) - 1 --- ISP_FLASH_TIME --- Note: Example: fl_time = (500ms * 100MHz) / (700 + 1) C 1 = 71530

ISP_FLASH_0660_MAXP

Address: Operational Base(0x21D00660) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	fl_maxp Maximum period value for flash or preflash max. flash/preflash period = 214 * (fl_maxp + 1) / clk_isp fl_maxp = (max_period * clk_isp) / 214 - 1 --- ISP_FLASH_MAXP --- Note: Example: fl_maxp = (10s * 100MHz) / (16384) C 1 = 61034

44.4.2.29 RAWAF

ISP_RAWAF_4D00_CTRL

Address: Operational Base(0x21D04D00) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_rawaf_meas_flag When rawaf measurement is over, this bit will pulled up by hardware itself, then software could read the result of rawaf. When read is over, it must been pulled down by software, and rawaf will work again at the beginning of next frame after pulled down.
30:29	RO	0x0	reserved
28	W1C	0x0	sys_rawaf_soft_rst_p Just a back door
27	RW	0x0	sw_rawaf_v2_acc_mode 1'b0: Sum all 1'b1: Sum max(tileline)
26	RW	0x0	sw_rawaf_v1_acc_mode 1'b0: Sum all 1'b1: Sum max(tileline)
25	RW	0x0	sw_rawaf_h2_acc_mode 1'b0: Sum all 1'b1: Sum max(tileline)
24	RW	0x0	sw_rawaf_h1_acc_mode 1'b0: Sum all 1'b1: Sum max(tileline)
23	RW	0x1	sw_rawaf_avg_ds_mode 1'b0: 8x8 down scale mode 1'b1: 16x16 down scale mode
22	RW	0x1	sw_rawaf_avg_ds_en RAWAF average down scale enable bit
21	RW	0x0	sw_rawaf_hiir_left_border_mode 1'b0: HIIR left border use above line right border out 1'b1: HIIR left border use cur line pixel
20	RW	0x0	sw_rawaf_bnr_be_sel RAWAF BNR BE select bit.
19	RW	0x0	sw_rawaf_from_ynr RAWAF input data come from YNR
18	RO	0x0	reserved
17:16	RW	0x1	sw_rawaf_v_dnscl_mode V direction downscale mode 2'b00: V direction downscale disable 2'b01: V direction each two lines drop one line 2'b10: V direction each four lines drop three line and H direction do 1/2 average downsample 2'b11: V direction down scale disable

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Bit	Attr	Reset Value	Description
15	RO	0x0	reserved
14	RW	0x0	sw_rawaf_vldg_sel V direction LDG input luma select. 1'b1: Data from gamma out 1'b0: Data from gauss out
13	RW	0x0	sw_rawaf_y_mode RAWAF cal data is Y (based input 5 RAW lines to 3 Y lines).
12	RO	0x0	reserved
11	RW	0x0	sw_rawaf_v2_fv_outmode 1'b0: Square mode 1'b1: Absolute mode
10	RW	0x0	sw_rawaf_v1_fv_outmode 1'b0: Square mode 1'b1: Absolute mode
9	RW	0x0	sw_rawaf_h2_fv_outmode 1'b0: Square mode 1'b1: Absolute mode
8	RW	0x0	sw_rawaf_h1_fv_outmode 1'b0: Square mode 1'b1: Absolute mode
7	RW	0x1	sw_rawaf_ldg_en LDG enable bit
6	RO	0x0	reserved
5	RW	0x1	sw_rawaf_viir_en Viir enable bit
4	RW	0x1	sw_rawaf_hiir_en Hiir enable bit
3	RO	0x0	reserved
2	RW	0x1	sw_gaus_en Gaus module enable bit
1	RW	0x1	sw_gamma_en Gamma module enable bit
0	RW	0x0	sw_rawaf_en AF measurement enable. Writing a 1 to this register starts a new measurement and resets the afm_fin (measurement finished) interrupt to 0.

ISP_RAWAF_4D00_OFFSET_WINA

Address: Operational Base(0x21D04D00) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0003	sw_a_h_l First pixel of window A (horizontal left row), value must be greater or equal 2.
15:13	RO	0x0	reserved
12:0	RW	0x0003	sw_a_v_t First line of window A (vertical top line), value must be greater or equal 1.

ISP_RAWAF_4D00_SIZE_WINA

Address: Operational Base(0x21D04D00) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28:16	RW	0x0000	sw_a_h_size Horizontal size of window A, value must be lower than (width of picture - 2 -- a_h_l). This value must be an integer multiple of 15.
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_a_v_size Vertical size of window A, value must be lower than (number of lines -2 -- a_v_t). This value must be an integer multiple of 15.

ISP_RAWAF_4D00_OFFSET_WINB

Address: Operational Base(0x21D04D00) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_b_h_l First pixel of window B (horizontal left row), value must be greater or equal 2
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_b_v_t First line of window B (vertical top line), value must be greater or equal 1

ISP_RAWAF_4D00_SIZE_WINB

Address: Operational Base(0x21D04D00) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_b_h_size Horizontal size of window A, value must be lower than (width of picture - 2 -- a_h_l)
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_b_v_size Vertical size of window A, value must be lower than (number of lines - 2 -- a_v_t)

ISP_RAWAF_4D00_INT_LINE

Address: Operational Base(0x21D04D00) + offset (0x0014)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_int_line4_en Int line4 is valid to produce an interrupt signal at the end of the line4 number is measured. 1'b0: AF line4 interrupt is disabled 1'b1: AF line4 interrupt is enabled
30	RW	0x0	sw_int_line3_en Int line3 is valid to produce an interrupt signal at the end of the line3 number is measured. 1'b0: AF line3 interrupt is disabled 1'b1: AF line3 interrupt is enabled
29	RW	0x0	sw_int_line2_en Int line2 is valid to produce an interrupt signal at the end of the line2 number is measured. 1'b0: AF line2 interrupt is disabled 1'b1: AF line2 interrupt is enabled

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Bit	Attr	Reset Value	Description
28	RW	0x0	sw_int_line1_en Int line1 is valid to produce an interrupt signal at the end of the line1 number is measured. 1'b0: AF line1 interrupt is disabled 1'b1: AF line1 interrupt is enabled
27	RW	0x0	sw_int_line0_en Int line0 is valid to produce an interrupt signal at the end of the line0 number is measured. 1'b0: AF line0 interrupt is disabled 1'b1: AF line0 interrupt is enabled
26:20	RO	0x00	reserved
19:16	RW	0xf	sw_int_line4 Fifth line number which need to produce int signal, range from 1 to 15, line4 need to be > line3, the interrupt will be produced at the at of ine_line4 - 1
15:12	RW	0xc	sw_int_line3 Fourth line number which need to produce int signal, range from 1 to 15, line3 need to be > line2, the interrupt will be produced at the at of ine_line3 - 1
11:8	RW	0x9	sw_int_line2 Third line number which need to produce int signal, range from 1 to 15, line2 need to be > line1, the interrupt will be produced at the at of ine_line2 - 1
7:4	RW	0x6	sw_int_line1 Second line number which need to produce int signal, range from 1 to 15, line1 need to be > line0, the interrupt will be produced at the at of ine_line1 - 1
3:0	RW	0x3	sw_int_line0 First line number which need to produce interrupt signal, range from 1 to 15, the interrupt will be produced at the at of ine_line0 - 1

ISP_RAWAF_4D00_CTRL1

Address: Operational Base(0x21D04D00) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:20	RW	0x0	sw_rawaf_tnrin_shift Variable shift for TNR input data. RAWAF_IN_TMP = (TNR_IN >>(sw_rawaf_tnrin_shift)). RAWAF_IN_REAL = RAWAF_IN_TMP >> 2. Note: in no HDR mode, valid 12bit data of TNR_IN is TNR_IN[11:0].
19	RO	0x0	reserved
18:16	RW	0x0	sw_rawaf_hldg_dilate_num 0 means not do HLDG dilate N means do (N+1) left direction dilate
15:14	RO	0x0	reserved
13	RW	0x0	sw_rawaf_aehgl_en RAWAF AE HIGHLIGHT enablt bit.
12	RW	0x0	sw_rawaf_bls_en RAWAF BLS enablt bit.
11:9	RO	0x0	reserved
8:0	RW	0x000	sw_rawaf_bls_offset Function: in_data - sw_rawaf_bls_offset Note: this signal is signed 1bit signed + 8bit interger

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ISP_RAWAF_4D00_HIGHLIT_CNT_WINB

Address: Operational Base(0x21D04D00) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RO	0x000000	ro_rawaf_highlit_cnt_winb High light count of window B

ISP_RAWAF_4D00_H1IIR_SUMB

Address: Operational Base(0x21D04D00) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawaf_h1iir_sumb Sharpness value of window B

ISP_RAWAF_4D00_H2IIR_SUMB

Address: Operational Base(0x21D04D00) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawaf_h2iir_sumb Sharpness value of window B

ISP_RAWAF_4D00_V1IIR_SUMB

Address: Operational Base(0x21D04D00) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawaf_v1iir_sumb Sharpness value of window B

ISP_RAWAF_4D00_V2IIR_SUMB

Address: Operational Base(0x21D04D00) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawaf_v2iir_sumb Sharpness value of window B

ISP_RAWAF_4D00_LUM_B

Address: Operational Base(0x21D04D00) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_afm_lum_b Luminance value of window B

ISP_RAWAF_4D00_GAMMA_Y0

Address: Operational Base(0x21D04D00) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x02d	sw_y1 y1 value of gamma table
15:10	RO	0x00	reserved
9:0	RW	0x000	sw_y0 y0 value of gamma table

ISP_RAWAF_4D00_GAMMA_Y1

Address: Operational Base(0x21D04D00) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x0b3	sw_y3 y3 value of gamma table
15:10	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x06c	sw_y2 y2 value of gamma table

ISP_RAWAF_4D00_GAMMA_Y2

Address: Operational Base(0x21D04D00) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x158	sw_y5 y5 value of gamma table
15:10	RO	0x00	reserved
9:0	RW	0x0f5	sw_y4 y4 value of gamma table

ISP_RAWAF_4D00_GAMMA_Y3

Address: Operational Base(0x21D04D00) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x1cb	sw_y7 y7 value of gamma table
15:10	RO	0x00	reserved
9:0	RW	0x199	sw_y6 y6 value of gamma table

ISP_RAWAF_4D00_GAMMA_Y4

Address: Operational Base(0x21D04D00) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x237	sw_y9 y9 value of gamma table
15:10	RO	0x00	reserved
9:0	RW	0x1f4	sw_y8 y8 value of gamma table

ISP_RAWAF_4D00_GAMMA_Y5

Address: Operational Base(0x21D04D00) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x2a4	sw_y11 y11 value of gamma table
15:10	RO	0x00	reserved
9:0	RW	0x26e	sw_y10 y10 value of gamma table

ISP_RAWAF_4D00_GAMMA_Y6

Address: Operational Base(0x21D04D00) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x341	sw_y13 y13 value of gamma table
15:10	RO	0x00	reserved
9:0	RW	0x2f7	sw_y12 y12 value of gamma table

ISP_RAWAF_4D00_GAMMA_Y7

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Address: Operational Base(0x21D04D00) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x3c2	sw_y15 y15 value of gamma table
15:10	RO	0x00	reserved
9:0	RW	0x380	sw_y14 y14 value of gamma table

ISP_RAWAF_4D00_GAMMA_Y8

Address: Operational Base(0x21D04D00) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x3ff	sw_y16 y16 value of gamma table

ISP_RAWAF_4D00_INT_STATE

Address: Operational Base(0x21D04D00) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16:13	RO	0x0	overflow_winb When sw_rawaf_meas_flag is pull down, this state can also be pull down
12	RO	0x0	overflow_h2_sum Overflow flag for H2 sum. When sw_rawaf_meas_flag is pull down, this state can also be pull down
11	RO	0x0	overflow_h1_sum Overflow flag for H1 sum. When sw_rawaf_meas_flag is pull down, this state can also be pull down
10	RO	0x0	overflow_v2_sum Overflow flag for V2 sum. When sw_rawaf_meas_flag is pull down, this state can also be pull down
9	RO	0x0	overflow_v1_sum Overflow flag for V1 sum. When sw_rawaf_meas_flag is pull down, this state can also be pull down
8	RO	0x0	overflow_afm_sum_b Overflow flag for AFM sum b. When sw_rawaf_meas_flag is pull down, this state can also be pull down
7:5	RO	0x0	reserved
4	RO	0x0	int_line4_state When int_line4_en is 1 and at the end of line4 number is measured, this bit will pulled up by hardware itself, then software could read the result of 15x15 rawaf sum. When read is over, it must been pulled down by software, and rawaf will work again at the beginning of next frame after pulled down. When sw_rawaf_meas_flag is pull down, this state can also be pull down
3	RO	0x0	int_line3_state When int_line3_en is 1 and at the end of line3 number is measured, this bit will pulled up by hardware itself, then software could read the result of 15x15 rawaf sum. When read is over, it must been pulled down by software, and rawaf will work again at the beginning of next frame after pulled down. When sw_rawaf_meas_flag is pull down, this state can also be pull down

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Bit	Attr	Reset Value	Description
2	RO	0x0	int_line2_state When int_line2_en is 1 and at the end of line2 number is measured, this bit will pulled up by hardware itself, then software could read the result of 15x15 rawaf sum. When read is over, it must been pulled down by software, and rawaf will work again at the beginning of next frame after pulled down. When sw_rawaf_meas_flag is pull down, this state can also be pull down
1	RO	0x0	int_line1_state When int_line1_en is 1 and at the end of line1 number is measured, this bit will pulled up by hardware itself, then software could read the result of 15x15 rawaf sum . When read is over, it must been pulled down by software, and rawaf will work again at the beginning of next frame after pulled down. When sw_rawaf_meas_flag is pull down, this state can also be pull down
0	WO	0x0	int_line0_state When int_line0_en is 1 and at the end of line0 number is measured, this bit will pulled up by hardware itself, then software could read the result of 15x15 rawaf sum. When read is over, it must been pulled down by software, and rawaf will work again at the beginning of next frame after pulled down. When sw_rawaf_meas_flag is pull down, this state can also be pull down

ISP_RAWAF_4D00_HIIR_THRESH

Address: Operational Base(0x21D04D00) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x020	sw_rawaf_v_fv_thresh This register defines a threshold which can be used for minimizing the influence of noise in the measurement result
15:12	RO	0x0	reserved
11:0	RW	0x020	sw_rawaf_h_fv_thresh This register defines a threshold which can be used for minimizing the influence of noise in the measurement result

ISP_RAWAF_4D00_H1_IIR1_COE01

Address: Operational Base(0x21D04D00) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x2bb	sw_rawaf_h1iir1_coe1 HIIR related coefficient ({1s,2i,9f})
15:12	RO	0x0	reserved
11:0	RW	0x200	sw_rawaf_h1iir1_coe0 HIIR related coefficient ({1s,2i,9f})

ISP_RAWAF_4D00_H1_IIR1_COE23

Address: Operational Base(0x21D04D00) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x03f	sw_rawaf_h1iir1_coe3 HIIR related coefficient ({1s,2i,9f})
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0xf19	sw_rawaf_h1iir1_coe2 HIIR related coefficient ({1s,2i,9f})

ISP_RAWAF_4D00_H1_IIR1_COE45

Address: Operational Base(0x21D04D00) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0xeb1	sw_rawaf_h1iir1_coe5 HIIR related coefficient ({1s,2i,9f})
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawaf_h1iir1_coe4 HIIR related coefficient ({1s,2i,9f})

ISP_RAWAF_4D00_H_CURVEL

Address: Operational Base(0x21D04D00) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0506	sw_rawaf_h_ldg_gslp0 LDG curve luma low slope({5i,8f})
15:8	RW	0x1c	sw_rawaf_h_ldg_gain0 LDG curve luma low minimum gain({8f})
7:0	RW	0x40	sw_rawaf_h_ldg_lumth0 LDG curve luma low threshold ({8f})

ISP_RAWAF_4D00_H1_IIR2_COE01

Address: Operational Base(0x21D04D00) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x1bf	sw_rawaf_h1iir2_coe1 HIIR related coefficient ({1s,2i,9f})
15:12	RO	0x0	reserved
11:0	RW	0x200	sw_rawaf_h1iir2_coe0 HIIR related coefficient ({1s,2i,9f})

ISP_RAWAF_4D00_H1_IIR2_COE23

Address: Operational Base(0x21D04D00) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0ac	sw_rawaf_h1iir2_coe3 HIIR related coefficient ({1s,2i,9f})
15:12	RO	0x0	reserved
11:0	RW	0xe7e	sw_rawaf_h1iir2_coe2 HIIR related coefficient ({1s,2i,9f})

ISP_RAWAF_4D00_H1_IIR2_COE45

Address: Operational Base(0x21D04D00) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0xfc1	sw_rawaf_h1iir2_coe5 HIIR related coefficient ({1s,2i,9f})
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawaf_h1iir2_coe4 HIIR related coefficient ({1s,2i,9f})

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ISP_RAWAF_4D00_H_CURVEH

Address: Operational Base(0x21D04D00) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0578	sw_rawaf_h_ldg_gslp1 LDG curve luma high slope({5i,8f})
15:8	RW	0x08	sw_rawaf_h_ldg_gain1 LDG curve luma high minimum gain({8f})
7:0	RW	0xb9	sw_rawaf_h_ldg_lumth1 LDG curve luma high threshold ({8f})

ISP_RAWAF_4D00_H2_IIR1_COE01

Address: Operational Base(0x21D04D00) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x272	sw_rawaf_h2iir1_coe1 HIIR related coefficient ({1s,2i,9f})
15:12	RO	0x0	reserved
11:0	RW	0x200	sw_rawaf_h2iir1_coe0 HIIR related coefficient ({1s,2i,9f})

ISP_RAWAF_4D00_H2_IIR1_COE23

Address: Operational Base(0x21D04D00) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x067	sw_rawaf_h2iir1_coe3 HIIR related coefficient ({1s,2i,9f})
15:12	RO	0x0	reserved
11:0	RW	0xecb	sw_rawaf_h2iir1_coe2 HIIR related coefficient ({1s,2i,9f})

ISP_RAWAF_4D00_H2_IIR1_COE45

Address: Operational Base(0x21D04D00) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0xf99	sw_rawaf_h2iir1_coe5 HIIR related coefficient ({1s,2i,9f})
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawaf_h2iir1_coe4 HIIR related coefficient ({1s,2i,9f})

ISP_RAWAF_4D00_V_CURVEL

Address: Operational Base(0x21D04D00) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0506	sw_rawaf_v_ldg_gslp0 LDG curve luma low slope({5i,8f})
15:8	RW	0x1c	sw_rawaf_v_ldg_gain0 LDG curve luma low minimum gain({8f})
7:0	RW	0x40	sw_rawaf_v_ldg_lumth0 LDG curve luma low threshold ({8f})

ISP_RAWAF_4D00_H2_IIR2_COE01

Address: Operational Base(0x21D04D00) + offset (0x0090)

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Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x1bf	sw_rawaf_h2iir2_coe1 HIIR related coefficient ({1s,2i,9f})
15:12	RO	0x0	reserved
11:0	RW	0x200	sw_rawaf_h2iir2_coe0 HIIR related coefficient ({1s,2i,9f})

ISP_RAWAF_4D00_H2_IIR2_COE23

Address: Operational Base(0x21D04D00) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0ac	sw_rawaf_h2iir2_coe3 HIIR related coefficient ({1s,2i,9f})
15:12	RO	0x0	reserved
11:0	RW	0xe9f	sw_rawaf_h2iir2_coe2 HIIR related coefficient ({1s,2i,9f})

ISP_RAWAF_4D00_H2_IIR2_COE45

Address: Operational Base(0x21D04D00) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0xf54	sw_rawaf_h2iir2_coe5 HIIR related coefficient ({1s,2i,9f})
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawaf_h2iir2_coe4 HIIR related coefficient ({1s,2i,9f})

ISP_RAWAF_4D00_V_CURVEH

Address: Operational Base(0x21D04D00) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0578	sw_rawaf_v_ldg_gslp1 LDG curve luma high slope({5i,8f})
15:8	RW	0x08	sw_rawaf_v_ldg_gain1 LDG curve luma high minimum gain({8f})
7:0	RW	0xb9	sw_rawaf_v_ldg_lumth1 LDG curve luma high threshold ({8f})

ISP_RAWAF_4D00_V_IIR_COE0

Address: Operational Base(0x21D04D00) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0ab	sw_rawaf_v2iir_coe0 VIIR related coefficient ({1s,2i,9f})
15:12	RO	0x0	reserved
11:0	RW	0x0ab	sw_rawaf_v1iir_coe0 VIIR related coefficient ({1s,2i,9f})

ISP_RAWAF_4D00_V_IIR_COE1

Address: Operational Base(0x21D04D00) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x033	sw_rawaf_v2iir_coe1 VIIR related coefficient ({1s,2i,9f})

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Bit	Attr	Reset Value	Description
15:12	RO	0x0	reserved
11:0	RW	0x033	sw_rawaf_v1iir_coe1 VIIR related coefficient ({1s,2i,9f})

ISP_RAWAF_4D00_V_IIR_COE2

Address: Operational Base(0x21D04D00) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0e7	sw_rawaf_v2iir_coe2 VIIR related coefficient ({1s,2i,9f})
15:12	RO	0x0	reserved
11:0	RW	0x0e7	sw_rawaf_v1iir_coe2 VIIR related coefficient ({1s,2i,9f})

ISP_RAWAF_4D00_CORING_H

Address: Operational Base(0x21D04D00) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x0e7	sw_rawaf_h_fv_slope CORING slope ({1i,8f})
15:10	RO	0x00	reserved
9:0	RW	0x0e7	sw_rawaf_h_fv_limit CORING limit ({10i})

ISP_RAWAF_4D00_V_FIR_COE0

Address: Operational Base(0x21D04D00) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x200	sw_rawaf_v2fir_coe0 VFIR related coefficient ({1s,2i,9f})
15:12	RO	0x0	reserved
11:0	RW	0x200	sw_rawaf_v1fir_coe0 VFIR related coefficient ({1s,2i,9f})

ISP_RAWAF_4D00_V_FIR_COE1

Address: Operational Base(0x21D04D00) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawaf_v2fir_coe1 VFIR related coefficient ({1s,2i,9f})
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawaf_v1fir_coe1 VFIR related coefficient ({1s,2i,9f})

ISP_RAWAF_4D00_V_FIR_COE2

Address: Operational Base(0x21D04D00) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0xe00	sw_rawaf_v2fir_coe2 VFIR related coefficient ({1s,2i,9f})
15:12	RO	0x0	reserved
11:0	RW	0xe00	sw_rawaf_v1fir_coe2 VFIR related coefficient ({1s,2i,9f})

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ISP_RAWAF_4D00_CORING_V

Address: Operational Base(0x21D04D00) + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x0e7	sw_rawaf_v_fv_slope CORING slope ({1i,8f})
15:10	RO	0x00	reserved
9:0	RW	0x0e7	sw_rawaf_v_fv_limit CORING limit ({10i})

ISP_RAWAF_4D00_GAUS_COE_03

Address: Operational Base(0x21D04D00) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:24	RW	0x10	sw_rawaf_gaus_coe3 GAUS related coefficient ({1i,7f})
23:16	RW	0x08	sw_rawaf_gaus_coe2 GAUS related coefficient({1i,7f})
15:8	RW	0x10	sw_rawaf_gaus_coe1 GAUS related coefficient ({1i,7f})
7:0	RW	0x08	sw_rawaf_gaus_coe0 GAUS related coefficient ({1i,7f})

ISP_RAWAF_4D00_GAUS_COE_47

Address: Operational Base(0x21D04D00) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:24	RW	0x10	sw_rawaf_gaus_coe7 GAUS related coefficient ({1i,7f})
23:16	RW	0x08	sw_rawaf_gaus_coe6 GAUS related coefficient ({1i,7f})
15:8	RW	0x10	sw_rawaf_gaus_coe5 GAUS related coefficient ({1i,7f})
7:0	RW	0x20	sw_rawaf_gaus_coe4 GAUS related coefficient ({1i,7f})

ISP_RAWAF_4D00_GAUS_COE_8

Address: Operational Base(0x21D04D00) + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x08	sw_rawaf_gaus_coe8 GAUS related coefficient ({1i,7f})

ISP_RAWAF_4D00_HVIIR_VAR_SHIFT

Address: Operational Base(0x21D04D00) + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	sw_rawaf_v2iir_shift_winb Variable shift for RAWAF v1iir channel
27:24	RW	0x0	sw_rawaf_v1iir_shift_winb Variable shift for RAWAF v1iir channel
23:20	RW	0x0	sw_rawaf_h2iir_shift_winb Variable shift for RAWAF h2iir channel
19:16	RW	0x0	sw_rawaf_h1iir_shift_winb Variable shift for RAWAF h1iir channel
15	RO	0x0	reserved
14:12	RW	0x0	sw_rawaf_v2iir_shift_wina Variable shift for RAWAF v1iir channel

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Bit	Attr	Reset Value	Description
11	RO	0x0	reserved
10:8	RW	0x0	sw_rawaf_v1iir_shift_wina Variable shift for RAWAF v1iir channel
7	RO	0x0	reserved
6:4	RW	0x0	sw_rawaf_h2iir_shift_wina Variable shift for RAWAF h2iir channel
3	RO	0x0	reserved
2:0	RW	0x0	sw_rawaf_h1iir_shift_wina Variable shift for RAWAF h1iir channel

ISP_RAWAF_4D00_HIGHLIT_THRESH

Address: Operational Base(0x21D04D00) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:10	RO	0x000000	reserved
9:0	RW	0x3cc	sw_rawaf_highlit_thresh If current data bigger than sw_rawaf_highlit_thresh, current data will be counted

ISP_RAWAF_4D00_THRES

Address: Operational Base(0x21D04D00) + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_ram_star_addr If ine_line0_en is 1, it need to be small than value of (ine_line0 - 1) * 15; Else if ine_line1_en is 1, it need to be small than value of (ine_line1 - 1) * 15, and so on
15:0	RO	0x0000	reserved

ISP_RAWAF_4D00_RAM_DATA

Address: Operational Base(0x21D04D00) + offset (0x00E0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	sum_data_wndx Total 15x15 windows, each window has 32*4bit. The 32*4bit data is align read_windx_data[127:0] = [32bitH2,32bitH1,32bitV2,32bitV1]

44.4.2.30 RAWAE

RAWAE_BIG_4400_4500_CTRL

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31	W1C	0x0	sw_aemeas_done This bit will be set to 1 by hardware when ae stats ready. The software can read ae stats and must clear this bit (write1 to clear) after operation. The hardware will run again when new flame arrived after this bit cleared.
30	RO	0x0	ro_working_r Module working signal
29:9	RO	0x000000	reserved
8	RW	0x0	sw_aemeas_debug_en The debug signal will toggle when this bit asset
7	RW	0x0	sw_rawae_big_wnd4_en 1'b0: Window close 1'b1: Window open

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Bit	Attr	Reset Value	Description
6	RW	0x0	sw_rawae_big_wnd3_en 1'b0: Window close 1'b1: Window open
5	RW	0x0	sw_rawae_big_wnd2_en 1'b0: Window close 1'b1: Window open
4	RW	0x0	sw_rawae_big_wnd1_en 1'b0: Window close 1'b1: Window open
3	RO	0x0	ro_rd_ram_en User need assert this bit to 1 before reading back RAM data and set to 0 after read operation
2:1	RW	0x0	sw_aemeas_wnd0_num 2'b0: 1x1 2'b1: 5x5 2'b2: 15x15 2'b3: 15x15
0	RW	0x0	sw_aemeas_en 1'b0: Disable this module 1'b1: Enable this module

RAWAE_BIG_4400_4500_WND0_BLK_SIZE

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_aemeas_v_size Vertical offset of first block in pixels. Note: The vertical size must be oven, and need leave 2lines at last.
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_aemeas_h_size Horizontal size in pixels of one block. Note: exp_h_size x window_num must be less (not equal) than the horizontal size of the picture

RAWAE_BIG_4400_4500_WND0_OFFSET

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_aemeas_v_offset Vertical offset of first block in pixels.
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_aemeas_h_offset Horizontal offset of first block in pixels.

RAWAE_BIG_4400_4500_RAM_CTRL

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31	RW	0x0	rd_ram_en Just for debug
30:24	RO	0x00	reserved
23:16	RO	0x00	ro_ram_cnt Ram cnt
15:8	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	sw_ram_offset Ram offset

RAWAE_BIG_4400_4500_WND1_SIZE

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_aemeas_v_size The down co-ordinates of this window Note: This signal is not this window's vertical size
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_aemeas_h_size The right co-ordinates of this window Note: This signal is not this window's horizontal size

RAWAE_BIG_4400_4500_WND1_OFFSET

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_aemeas_v_offset Vertical offset of first block in pixels.
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_aemeas_h_offset Horizontal offset of first block in pixels.

RAWAE_BIG_4400_4500_WND1_SUMR

Address: **Operational Base** + offset (0x0030)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RO	0x00000000	ro_rawae_big_wnd1_sumr Sum R channel data for this single separated window

RAWAE_BIG_4400_4500_WND1_SUMG

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawae_big_wnd1_sumg Sum G channel data for this single separated window

RAWAE_BIG_4400_4500_WND1_SUMB

Address: **Operational Base** + offset (0x0050)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RO	0x00000000	ro_rawae_big_wnd1_sumb Sum B channel data for this single separated window

RAWAE_BIG_4400_4500_RO_MEAN_BASE_ADDR

Address: **Operational Base** + offset (0x0080)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	ro_rawae_mean_channelr_xy Channel g mean luminance value of block 00~44 (x,y) xy means x and y coordinate
21:12	RO	0x000	ro_rawae_mean_channelb_xy Channel g mean luminance value of block 00~44 (x,y) xy means x and y coordinate

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Bit	Attr	Reset Value	Description
11:0	RO	0x000	ro_rawae_mean_channelg_xy Channel g mean luminance value of block 00~44 (x,y) xy means x and y coordinate

44.4.2.31 RAWAWB

ISP_RAWAWB_5000_CTRL

Address: Operational Base(0x21D05000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_rawawb_meas_done When rawawb measurement is over, this bit is pulled up by hardware itself, then software could read the result of rawawb. When read is over, it should been pulled down by software, and rawawb will work again at the beginning of next frame after pulled down
30	RO	0x0	ro_rawawb_working Rawawb working state read back 1'b1: Working 1'b0: Not working
29	RO	0x0	ro_rawawb2ddr_path_err RAWAWB2DDR path has error
28	RW	0x0	sw_rawawbin_low12bit_val For control the RAWAWB input data valid bit.
27	RW	0x0	sw_rawawb_2ddr_path_sel RAWAWB2DDR path select bit 1'b0: RAWAWB in (12'b0,rawawb_in[19:0]) 1'b1: RAWAWB dsout (R10 G12 B10)
26	RW	0x0	sw_rawawb_3dyuv_en1 1'b1: 3DYUV detect Enable for all light and big window 1'b0: 3DYUV detect disable for all light and big window
25	RW	0x0	sw_rawawb_xy_en1 1'b1: XY detect Enable for all light and big window 1'b0: XY detect disable for all light and big window
24	RW	0x0	sw_rawawb_uv_en1 1'b1: UV detect Enable for all light and big window 1'b0: UV detect disable for all light and big window
23	RW	0x0	sw_rawawb_2ddr_path_en RAWAWB2DDR path enable bit
22:20	RW	0x0	sw_rawawb_light_num Number of light sources, and range is from 0 to 7
19	RW	0x0	sw_rawlsc_bypass_en 1'b1: Rawlsc bypass Enable 1'b0: Rawlsc bypass disable
18	RW	0x0	sw_rawawb_wind_size Raw to RGB down sample window size 1'b0: 4x4 window 1'b1: 8x8 window If sw_rawawb_h_size > 2560, the window size would been 8x8 forced by hardware
17	RW	0x0	sw_rawawb_in_overexposure_check_en RAWAWB input data over exposure check enable bit
16	RW	0x0	sw_rawawb_in_rshift_to_12bit_en RAWAWB input data shift to 12bit enable bit

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Bit	Attr	Reset Value	Description
15:13	RW	0x0	sw_rawawb_3dyuv_ls_idx3 Light source selection for 3dyuv white point detected. There are four 3dyuv white detected logic to support maximum 4 lights white point detection at the same time. 3'd0: Light 0 for 3dyuv white point detected logic 3 .. 3'd6: Light 6 for 3dyuv white point detected logic 3 3'd7: Disable for 3dyuv white point detected logic 3
12:10	RW	0x0	sw_rawawb_3dyuv_ls_idx2 Light source selection for 3dyuv white point detected. There are four 3dyuv white detected logic to support maximum 4 lights white point detection at the same time. 3'd0: Light 0 for 3dyuv white point detected logic 2 .. 3'd6: Light 6 for 3dyuv white point detected logic 2 3'd7: Disable for 3dyuv white point detected logic 2
9:7	RW	0x0	sw_rawawb_3dyuv_ls_idx1 Light source selection for 3dyuv white point detected. There are four 3dyuv white detected logic to support maximum 4 lights white point detection at the same time 3'd0: Light 0 for 3dyuv white point detected logic 1 .. 3'd6: Light 6 for 3dyuv white point detected logic 1 3'd7: Disable for 3dyuv white point detected logic 1
6:4	RW	0x0	sw_rawawb_3dyuv_ls_idx0 Light source selection for 3dyuv white point detected. There are four 3dyuv white detected logic to support maximum 4 lights white point detection at the same time 3'd0: Light 0 for 3dyuv white point detected logic 0 .. 3'd6: Light 6 for 3dyuv white point detected logic 0 3'd7: Disable for 3dyuv white point detected logic 0
3	RW	0x0	sw_rawawb_3dyuv_en0 1'b1: 3DYUV detect Enable for all light and normal window 1'b0: 3DYUV detect disable for all light and normal window
2	RW	0x0	sw_rawawb_xy_en0 1'b1: XY detect Enable for all light and normal window 1'b0: XY detect disable for all light and normal window
1	RW	0x0	sw_rawawb_uv_en0 1'b1: UV detect Enable for all light and normal window 1'b0: UV detect disable for all light and normal window
0	RW	0x0	sw_rawawb_en 1'b1: Rawawb Enable 1'b0: Rawawb disable

ISP_RAWAWB_5000_BLK_CTRL

Address: Operational Base(0x21D05000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:16	RW	0xffff	sw_rawawb_in_overexposure_threshold Over exposure threshold (compare high 16bit with rawawb input 20bit data)
15:11	RO	0x00	reserved
10	RW	0x0	sw_rawawb_bnr_be_sel RAWAWB BNR data BE select bit.

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Bit	Attr	Reset Value	Description
9	RW	0x0	sw_rawawb_ovexp_2ddr_dis Over exposure bit to DDR bit disable bit
8	RW	0x0	sw_rawawb_blk_with_luma_wei_en Block luma weight Enable bit
7	RW	0x0	sw_rawawb_ds16x8_mode_en Raw to RGB down sample 16x8 mode enable bit(used for 8K size)
6:4	RW	0x0	sw_rawawb_blk_measure_illu_idx 3'b0: Select source light 3'b1: Select source light .. 3'b7: Select all lights
3	RW	0x0	sw_rawawb_blk_rtdw_measure_en The right and down corner of block measure Enable bit
2	RW	0x0	sw_rawawb_blk_measure_xytype 1'b0: Select normal window 1'b1: Select big window
1	RW	0x0	sw_rawawb_blk_measure_mode 1'b0: Measure all pixel 1'b1: Measure real one
0	RW	0x0	sw_rawawb_blk_measure_en Block measure Enable bit

ISP_RAWAWB_5000_WIN_OFFS

Address: Operational Base(0x21D05000) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_v_offs AWB vertical offset of crop measure window, and bit16 is written to 0 by hardware to align offset to 2
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_rawawb_h_offs AWB horizontal offset of crop measure window, and bit0 is written to 0 by hardware to align offset to 2

ISP_RAWAWB_5000_WIN_SIZE

Address: Operational Base(0x21D05000) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_v_size AWB vertical crop window size 8x8 down sample window: bit16 to bit18 are written to 0 by hardware to align size to 8 4x4 down sample window: bit16 to bit17 are written to 0 by hardware to align size to 4
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_rawawb_h_size AWB horizontal window size down sample window 8x8: bit0 to bit2 are written to 0 by hardware to align size to 8 down sample window 4x4: bit0 to bit1 are written to 0 by hardware to align size to 4

ISP_RAWAWB_5000_LIMIT_RG_MAX

Address: Operational Base(0x21D05000) + offset (0x0010)

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Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_g_max Max green value in white point detection
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_r_max Max red value in white point detection

ISP_RAWAWB_5000_LIMIT_BY_MAX

Address: Operational Base(0x21D05000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_y_max Max luminance value in white point detection
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_b_max Max blue value in white point detection

ISP_RAWAWB_5000_LIMIT_RG_MIN

Address: Operational Base(0x21D05000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_g_min Min green value in white point detection
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_r_min Min red value in white point detection

ISP_RAWAWB_5000_LIMIT_BY_MIN

Address: Operational Base(0x21D05000) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_y_min Min luminance value in white point detection
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_b_min Min blue value in white point detection

ISP_RAWAWB_5000_WEIGHT_CURVE_CTRL

Address: Operational Base(0x21D05000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:5	RO	0x0000000	reserved
4	RW	0x0	sw_rawawb_wp_hist_xytype Select normal or big window for YHIST 1'b0: Normal window 1'b1: Big window
3	RW	0x0	sw_rawawb_wp_blk_wei_en1 Block weight enable bit for big window
2	RW	0x0	sw_rawawb_wp_blk_wei_en0 Block weight enable bit for normal window
1	RW	0x0	sw_rawawb_wp_luma_wei_en1 Y weight curve enable for big window
0	RW	0x0	sw_rawawb_wp_luma_wei_en0 Y weight curve enable for normal window

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ISP_RAWAWB_5000_YWEIGHT_CURVE_XCOOR03

Address: Operational Base(0x21D05000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:24	RW	0x60	sw_rawawb_wp_luma_weicurve_y3 Y weight curve x coordinate
23:16	RW	0x40	sw_rawawb_wp_luma_weicurve_y2 Y weight curve x coordinate
15:8	RW	0x20	sw_rawawb_wp_luma_weicurve_y1 Y weight curve x coordinate
7:0	RW	0x00	sw_rawawb_wp_luma_weicurve_y0 Y weight curve x coordinate

ISP_RAWAWB_5000_YWEIGHT_CURVE_XCOOR47

Address: Operational Base(0x21D05000) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:24	RW	0xe0	sw_rawawb_wp_luma_weicurve_y8 Y weight curve x coordinate
23:16	RW	0xc0	sw_rawawb_wp_luma_weicurve_y7 Y weight curve x coordinate
15:8	RW	0xa0	sw_rawawb_wp_luma_weicurve_y6 Y weight curve x coordinate
7:0	RW	0x80	sw_rawawb_wp_luma_weicurve_y5 Y weight curve x coordinate

ISP_RAWAWB_5000_YWEIGHT_CURVE_XCOOR8

Address: Operational Base(0x21D05000) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0xff	sw_rawawb_wp_luma_weicurve_y8 Y weight curve x coordinate

ISP_RAWAWB_5000_YWEIGHT_CURVE_YCOOR03

Address: Operational Base(0x21D05000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x20	sw_rawawb_wp_luma_weicurve_w3 Y weight curve y coordinate
23:22	RO	0x0	reserved
21:16	RW	0x20	sw_rawawb_wp_luma_weicurve_w2 Y weight curve y coordinate
15:14	RO	0x0	reserved
13:8	RW	0x20	sw_rawawb_wp_luma_weicurve_w1 Y weight curve y coordinate
7:6	RO	0x0	reserved
5:0	RW	0x20	sw_rawawb_wp_luma_weicurve_w0 Y weight curve y coordinate

ISP_RAWAWB_5000_YWEIGHT_CURVE_YCOOR47

Address: Operational Base(0x21D05000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x20	sw_rawawb_wp_luma_weicurve_w7 Y weight curve y coordinate
23:22	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
21:16	RW	0x20	sw_rawawb_wp_luma_weicurve_w6 Y weight curve y coordinate
15:14	RO	0x0	reserved
13:8	RW	0x20	sw_rawawb_wp_luma_weicurve_w5 Y weight curve y coordinate
7:6	RO	0x0	reserved
5:0	RW	0x20	sw_rawawb_wp_luma_weicurve_w4 Y weight curve y coordinate

ISP_RAWAWB_5000_YWEIGHT_CURVE_YCOOR8

Address: Operational Base(0x21D05000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0100	sw_rawawb_pre_wbgain_inv_r For some sensor has already do awb-gain need do some pre-white-balance gain operation or use for rawawb gain
15:6	RO	0x000	reserved
5:0	RW	0x20	sw_rawawb_wp_luma_weicurve_w8 Y weight curve y coordinate

ISP_RAWAWB_5000_PRE_WBGAIN_INV

Address: Operational Base(0x21D05000) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0100	sw_rawawb_pre_wbgain_inv_b For some sensor has already do awb-gain need do some pre-white-balance gain operation or use for rawawb gain
15:13	RO	0x0	reserved
12:0	RW	0x0100	sw_rawawb_pre_wbgain_inv_g For some sensor has already do awb-gain need do some pre-white-balance gain operation or use for rawawb gain

ISP_RAWAWB_5000_UV_DETC_VERTEX0_0

Address: Operational Base(0x21D05000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_rawawb_vertex0_v_0 Vertex coordinate
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_rawawb_vertex0_u_0 Vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX1_0

Address: Operational Base(0x21D05000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_rawawb_vertex1_v_0 Vertex coordinate
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_rawawb_vertex1_u_0 Vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX2_0

Address: Operational Base(0x21D05000) + offset (0x0048)

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Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_rawawb_vertex2_v_0 Vertex coordinate
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_rawawb_vertex2_u_0 Vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX3_0

Address: Operational Base(0x21D05000) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_rawawb_vertex3_v_0 Vertex coordinate
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_rawawb_vertex3_u_0 Vertex coordinate

ISP_RAWAWB_5000_UV_DETC_ISLOPE01_0

Address: Operational Base(0x21D05000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_rawawb_islope01_0 Slope inversion

ISP_RAWAWB_5000_UV_DETC_ISLOPE12_0

Address: Operational Base(0x21D05000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_rawawb_islope12_0 Slope inversion

ISP_RAWAWB_5000_UV_DETC_ISLOPE23_0

Address: Operational Base(0x21D05000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_rawawb_islope23_0 Slope inversion

ISP_RAWAWB_5000_UV_DETC_ISLOPE30_0

Address: Operational Base(0x21D05000) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_rawawb_islope30_0 Slope inversion

ISP_RAWAWB_5000_UV_DETC_VERTEX0_1

Address: Operational Base(0x21D05000) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_rawawb_vertex0_v_1 Vertex coordinate
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_rawawb_vertex0_u_1 Vertex coordinate

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ISP_RAWAWB_5000_UV_DETC_VERTEX1_1

Address: Operational Base(0x21D05000) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_rawawb_vertex1_v_1 Vertex coordinate
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_rawawb_vertex1_u_1 Vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX2_1

Address: Operational Base(0x21D05000) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_rawawb_vertex2_v_1 Vertex coordinate
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_rawawb_vertex2_u_1 Vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX3_1

Address: Operational Base(0x21D05000) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_rawawb_vertex3_v_1 Vertex coordinate
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_rawawb_vertex3_u_1 Vertex coordinate

ISP_RAWAWB_5000_UV_DETC_ISLOPE01_1

Address: Operational Base(0x21D05000) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_rawawb_islope01_1 Slope inversion

ISP_RAWAWB_5000_UV_DETC_ISLOPE12_1

Address: Operational Base(0x21D05000) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_rawawb_islope12_1 Slope inversion

ISP_RAWAWB_5000_UV_DETC_ISLOPE23_1

Address: Operational Base(0x21D05000) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_rawawb_islope23_1 Slope inversion

ISP_RAWAWB_5000_UV_DETC_ISLOPE30_1

Address: Operational Base(0x21D05000) + offset (0x007C)

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Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_rawawb_islope30_1 Slope inversion

ISP_RAWAWB_5000_UV_DETC_VERTEX0_2

Address: Operational Base(0x21D05000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_rawawb_vertex0_v_2 Vertex coordinate
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_rawawb_vertex0_u_2 Vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX1_2

Address: Operational Base(0x21D05000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_rawawb_vertex1_v_2 Vertex coordinate
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_rawawb_vertex1_u_2 Vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX2_2

Address: Operational Base(0x21D05000) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_rawawb_vertex2_v_2 Vertex coordinate
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_rawawb_vertex2_u_2 Vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX3_2

Address: Operational Base(0x21D05000) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_rawawb_vertex3_v_2 Vertex coordinate
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_rawawb_vertex3_u_2 Vertex coordinate

ISP_RAWAWB_5000_UV_DETC_ISLOPE01_2

Address: Operational Base(0x21D05000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_rawawb_islope01_2 Slope inversion

ISP_RAWAWB_5000_UV_DETC_ISLOPE12_2

Address: Operational Base(0x21D05000) + offset (0x0094)

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Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_rawawb_islope12_2 Slope inversion

ISP_RAWAWB_5000_UV_DETC_ISLOPE23_2

Address: Operational Base(0x21D05000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_rawawb_islope23_2 Slope inversion

ISP_RAWAWB_5000_UV_DETC_ISLOPE30_2

Address: Operational Base(0x21D05000) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_rawawb_islope30_2 Slope inversion

ISP_RAWAWB_5000_UV_DETC_VERTEX0_3

Address: Operational Base(0x21D05000) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_rawawb_vertex0_v_3 Vertex coordinate
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_rawawb_vertex0_u_3 Vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX1_3

Address: Operational Base(0x21D05000) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_rawawb_vertex1_v_3 Vertex coordinate
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_rawawb_vertex1_u_3 Vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX2_3

Address: Operational Base(0x21D05000) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_rawawb_vertex2_v_3 Vertex coordinate
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_rawawb_vertex2_u_3 Vertex coordinate

ISP_RAWAWB_5000_UV_DETC_VERTEX3_3

Address: Operational Base(0x21D05000) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24:16	RW	0x000	sw_rawawb_vertex3_v_3 Vertex coordinate

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Bit	Attr	Reset Value	Description
15:9	RO	0x00	reserved
8:0	RW	0x000	sw_rawawb_vertex3_u_3 Vertex coordinate

ISP_RAWAWB_5000_UV_DETC_ISLOPE01_3

Address: Operational Base(0x21D05000) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_rawawb_islope01_3 Slope inversion

ISP_RAWAWB_5000_UV_DETC_ISLOPE12_3

Address: Operational Base(0x21D05000) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_rawawb_islope12_3 Slope inversion

ISP_RAWAWB_5000_UV_DETC_ISLOPE23_3

Address: Operational Base(0x21D05000) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_rawawb_islope23_3 Slope inversion

ISP_RAWAWB_5000_UV_DETC_ISLOPE30_3

Address: Operational Base(0x21D05000) + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	reserved
19:0	RW	0x00000	sw_rawawb_islope30_3 Slope inversion

ISP_RAWAWB_5000_CCM_COEFF0_R

Address: Operational Base(0x21D05000) + offset (0x01C0)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x7b7	sw_ccm_coeff1_r The n coefficient value of ccm matrix(S4.7).
15:12	RO	0x0	reserved
11:0	RW	0x065	sw_ccm_coeff0_r The n coefficient value of ccm matrix(S4.7).

ISP_RAWAWB_5000_CCM_COEFF1_R

Address: Operational Base(0x21D05000) + offset (0x01C4)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x7e4	sw_ccm_coeff2_r The n coefficient value of ccm matrix (S4.7).

ISP_RAWAWB_5000_CCM_COEFF0_G

Address: Operational Base(0x21D05000) + offset (0x01C8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:16	RW	0x058	sw_ccm_coeff1_g The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit fractional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff], so the value is expanded 128 times.
15:12	RO	0x0	reserved
11:0	RW	0x7d9	sw_ccm_coeff0_g The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit fractional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff], so the value is expanded 128 times.

ISP_RAWAWB_5000_CCM_COEFF1_G

Address: Operational Base(0x21D05000) + offset (0x01CC)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x7cf	sw_ccm_coeff2_g The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit fractional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff], so the value is expanded 128 times.

ISP_RAWAWB_5000_CCM_COEFF0_B

Address: Operational Base(0x21D05000) + offset (0x01D0)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x7b7	sw_ccm_coeff1_b The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit fractional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff], so the value is expanded 128 times.
15:12	RO	0x0	reserved
11:0	RW	0x002	sw_ccm_coeff0_b The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit fractional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff], so the value is expanded 128 times.

ISP_RAWAWB_5000_CCM_COEFF1_B

Address: Operational Base(0x21D05000) + offset (0x01D4)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x046	sw_ccm_coeff2_b The n coefficient value of ccm matrix. Values are 11-bit signed fixed-point numbers with 4-bit integer and 7-bit fractional. The range of the coefficient is from -8[0x400] to 7.992[0x3ff], so the value is expanded 128 times.

ISP_RAWAWB_5000_RGB2XY_WT01

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Address: Operational Base(0x21D05000) + offset (0x01FC)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	sw_rawawb_wt1 RGB2XY weight matrix, coefficient 1
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_rawawb_wt0 RGB2XY weight matrix, coefficient 0

ISP_RAWAWB_5000_RGB2XY_WT2

Address: Operational Base(0x21D05000) + offset (0x0200)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	sw_rawawb_wt2 RGB2XY weight matrix, coefficient 0

ISP_RAWAWB_5000_RGB2XY_MAT0_XY

Address: Operational Base(0x21D05000) + offset (0x0204)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0000	sw_rawawb_mat0_y RGB2XY, rotation matrix, first column XY
15	RO	0x0	reserved
14:0	RW	0x0000	sw_rawawb_mat0_x RGB2XY, rotation matrix, first column XY

ISP_RAWAWB_5000_RGB2XY_MAT1_XY

Address: Operational Base(0x21D05000) + offset (0x0208)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0000	sw_rawawb_mat1_y RGB2XY, rotation matrix, second column XY
15	RO	0x0	reserved
14:0	RW	0x0000	sw_rawawb_mat1_x RGB2XY, rotation matrix, second column XY

ISP_RAWAWB_5000_RGB2XY_MAT2_XY

Address: Operational Base(0x21D05000) + offset (0x020C)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0000	sw_rawawb_mat2_y RGB2XY, rotation matrix, third column XY
15	RO	0x0	reserved
14:0	RW	0x0000	sw_rawawb_mat2_x RGB2XY, rotation matrix, third column XY

ISP_RAWAWB_5000_XY_DETC_NOR_X_0

Address: Operational Base(0x21D05000) + offset (0x0210)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_nor_x1_0 XY detect, right x boundary of normal range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_nor_x0_0 XY detect, left x boundary of normal range

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ISP_RAWAWB_5000_XY_DETC_NOR_Y_0

Address: Operational Base(0x21D05000) + offset (0x0214)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_nor_y1_0 XY detect, down y boundary of normal range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_nor_y0_0 XY detect, up y boundary of normal range

ISP_RAWAWB_5000_XY_DETC_BIG_X_0

Address: Operational Base(0x21D05000) + offset (0x0218)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_big_x1_0 XY detect, right x boundary of big range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_big_x0_0 XY detect, left x boundary of big range

ISP_RAWAWB_5000_XY_DETC_BIG_Y_0

Address: Operational Base(0x21D05000) + offset (0x021C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_big_y1_0 XY detect, down y boundary of big range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_big_y0_0 XY detect, up y boundary of big range

ISP_RAWAWB_5000_XY_DETC_NOR_X_1

Address: Operational Base(0x21D05000) + offset (0x0228)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_nor_x1_1 XY detect, right x boundary of normal range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_nor_x0_1 XY detect, left x boundary of normal range

ISP_RAWAWB_5000_XY_DETC_NOR_Y_1

Address: Operational Base(0x21D05000) + offset (0x022C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_nor_y1_1 XY detect, down y boundary of normal range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_nor_y0_1 XY detect, up y boundary of normal range

ISP_RAWAWB_5000_XY_DETC_BIG_X_1

Address: Operational Base(0x21D05000) + offset (0x0230)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:16	RW	0x0000	sw_rawawb_big_x1_1 XY detect, right x boundary of big range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_big_x0_1 XY detect, left x boundary of big range

ISP_RAWAWB_5000_XY_DETC_BIG_Y_1

Address: Operational Base(0x21D05000) + offset (0x0234)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_big_y1_1 XY detect, down y boundary of big range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_big_y0_1 XY detect, up y boundary of big range

ISP_RAWAWB_5000_XY_DETC_NOR_X_2

Address: Operational Base(0x21D05000) + offset (0x0240)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_nor_x1_2 XY detect, right x boundary of normal range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_nor_x0_2 XY detect, left x boundary of normal range

ISP_RAWAWB_5000_XY_DETC_NOR_Y_2

Address: Operational Base(0x21D05000) + offset (0x0244)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_nor_y1_2 XY detect, down y boundary of normal range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_nor_y0_2 XY detect, up y boundary of normal range

ISP_RAWAWB_5000_XY_DETC_BIG_X_2

Address: Operational Base(0x21D05000) + offset (0x0248)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_big_x1_2 XY detect, right x boundary of big range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_big_x0_2 XY detect, left x boundary of big range

ISP_RAWAWB_5000_XY_DETC_BIG_Y_2

Address: Operational Base(0x21D05000) + offset (0x024C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_big_y1_2 XY detect, down y boundary of big range
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:0	RW	0x0000	sw_rawawb_big_y0_2 XY detect, up y boundary of big range

ISP_RAWAWB_5000_XY_DETC_NOR_X_3

Address: Operational Base(0x21D05000) + offset (0x0258)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_nor_x1_3 XY detect, right x boundary of normal range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_nor_x0_3 XY detect, left x boundary of normal range

ISP_RAWAWB_5000_XY_DETC_NOR_Y_3

Address: Operational Base(0x21D05000) + offset (0x025C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_nor_y1_3 XY detect, down y boundary of normal range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_nor_y0_3 XY detect, up y boundary of normal range

ISP_RAWAWB_5000_XY_DETC_BIG_X_3

Address: Operational Base(0x21D05000) + offset (0x0260)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_big_x1_3 XY detect, right x boundary of big range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_big_x0_3 XY detect, left x boundary of big range

ISP_RAWAWB_5000_XY_DETC_BIG_Y_3

Address: Operational Base(0x21D05000) + offset (0x0264)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_big_y1_3 XY detect, down y boundary of big range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_big_y0_3 XY detect, up y boundary of big range

ISP_RAWAWB_5000_MULTIWINDOW_EXC_CTRL

Address: Operational Base(0x21D05000) + offset (0x02B8)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_rawawb_multiwindow_en The multi-window measure enable 1'b1: Enable 1'b0: Disable
30:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27	RW	0x0	sw_rawawb_exc_wp_region6_domain The domain of exclude region 1'b1: XY range 1'b0: UV range
26	RO	0x0	reserved
25:24	RW	0x0	sw_rawawb_exc_wp_region6_excen The exclude enable of exclude region in both XY and UV range. Bit0 is for normal window and bit1 for big window
23	RW	0x0	sw_rawawb_exc_wp_region5_domain The domain of exclude region 1'b1: XY range 1'b0: UV range
22	RO	0x0	reserved
21:20	RW	0x0	sw_rawawb_exc_wp_region5_excen The exclude enable of exclude region in both XY and UV range. Bit0 is for normal window and bit1 for big window
19	RW	0x0	sw_rawawb_exc_wp_region4_domain The domain of exclude region 1'b1: XY range 1'b0: UV range
18	RO	0x0	reserved
17:16	RW	0x0	sw_rawawb_exc_wp_region4_excen The exclude enable of exclude region in both XY and UV range. Bit0 is for normal window and bit1 for big window
15	RW	0x0	sw_rawawb_exc_wp_region3_domain The domain of exclude region 1'b1: XY range 1'b0: UV range
14	RW	0x0	sw_rawawb_exc_wp_region3_measen The measurement enable of exclude region in XY or UV range 1'b1: Enable 1'b0: Disable
13:12	RW	0x0	sw_rawawb_exc_wp_region3_excen The exclude enable of exclude region in both XY and UV range. Bit0 is for normal window and bit1 for big window
11	RW	0x0	sw_rawawb_exc_wp_region2_domain The domain of exclude region 1'b1: XY range 1'b0: UV range
10	RW	0x0	sw_rawawb_exc_wp_region2_measen The measurement enable of exclude region in XY or UV range 1'b1: Enable 1'b0: Disable
9:8	RW	0x0	sw_rawawb_exc_wp_region2_excen The exclude enable of exclude region in both XY and UV range. Bit0 is for normal window and bit1 for big window
7	RW	0x0	sw_rawawb_exc_wp_region1_domain The domain of exclude region 1'b1: XY range 1'b0: UV range
6	RW	0x0	sw_rawawb_exc_wp_region1_measen The measurement enable of exclude region in XY or UV range 1'b1: Enable 1'b0: Disable

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Bit	Attr	Reset Value	Description
5:4	RW	0x0	sw_rawawb_exc_wp_region1_excen The exclude enable of exclude region in both XY and UV range. Bit0 is for normal window and bit1 for big window
3	RW	0x0	sw_rawawb_exc_wp_region0_domain The domain of exclude region 1'b1: XY range 1'b0: UV range
2	RW	0x0	sw_rawawb_exc_wp_region0_measen The measurement enable of exclude region in XY or UV range 1'b1: Enable 1'b0: Disable
1:0	RW	0x0	sw_rawawb_exc_wp_region0_excen The exclude enable of exclude region in both XY and UV range. Bit0 is for normal window and bit1 for big window

ISP_RAWAWB_5000_MULTIWINDOW0_OFFS

Address: Operational Base(0x21D05000) + offset (0x02BC)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_multiwindow0_v_offs The multi-window vertical offset
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_rawawb_multiwindow0_h_offs The multi-window horizontal offset

ISP_RAWAWB_5000_MULTIWINDOW0_SIZE

Address: Operational Base(0x21D05000) + offset (0x02C0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_multiwindow0_v_size The multi-window vertical size
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_rawawb_multiwindow0_h_size The multi-window horizontal size

ISP_RAWAWB_5000_MULTIWINDOW1_OFFS

Address: Operational Base(0x21D05000) + offset (0x02C4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_multiwindow1_v_offs The multi-window vertical offset
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_rawawb_multiwindow1_h_offs The multi-window horizontal offset

ISP_RAWAWB_5000_MULTIWINDOW1_SIZE

Address: Operational Base(0x21D05000) + offset (0x02C8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_multiwindow1_v_size The multi-window vertical size
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_rawawb_multiwindow1_h_size The multi-window horizontal size

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ISP_RAWAWB_5000_MULTIWINDOW2_OFFS

Address: Operational Base(0x21D05000) + offset (0x02CC)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_multiwindow2_v_offs The multi-window vertical offset
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_rawawb_multiwindow2_h_offs The multi-window horizontal offset

ISP_RAWAWB_5000_MULTIWINDOW2_SIZE

Address: Operational Base(0x21D05000) + offset (0x02D0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_multiwindow2_v_size The multi-window vertical size
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_rawawb_multiwindow2_h_size The multi-window horizontal size

ISP_RAWAWB_5000_MULTIWINDOW3_OFFS

Address: Operational Base(0x21D05000) + offset (0x02D4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_multiwindow3_v_offs The multi-window vertical offset
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_rawawb_multiwindow3_h_offs The multi-window horizontal offset

ISP_RAWAWB_5000_MULTIWINDOW3_SIZE

Address: Operational Base(0x21D05000) + offset (0x02D8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_rawawb_multiwindow3_v_size The multi-window vertical size
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_rawawb_multiwindow3_h_size The multi-window horizontal size

ISP_RAWAWB_5000_EXC_WP_REGION0_XU

Address: Operational Base(0x21D05000) + offset (0x02FC)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region0_xu1 The right boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region0_xu0 The left boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION0_YV

Address: Operational Base(0x21D05000) + offset (0x0300)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:16	RW	0x0000	sw_rawawb_exc_wp_region0_yv1 The bottom boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region0_yv0 The top boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION1_XU

Address: Operational Base(0x21D05000) + offset (0x0304)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region1_xu1 The right boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region1_xu0 The left boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION1_YV

Address: Operational Base(0x21D05000) + offset (0x0308)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region1_yv1 The bottom boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region1_yv0 The top boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION2_XU

Address: Operational Base(0x21D05000) + offset (0x030C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region1_xu1 The right boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region2_xu0 The left boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION2_YV

Address: Operational Base(0x21D05000) + offset (0x0310)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region2_yv1 The bottom boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region2_yv0 The top boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION3_XU

Address: Operational Base(0x21D05000) + offset (0x0314)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region3_xu1 The right boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:0	RW	0x0000	sw_rawawb_exc_wp_region3_xu0 The left boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION3_YV

Address: Operational Base(0x21D05000) + offset (0x0318)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region3_yv1 The bottom boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region3_yv0 The top boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION4_XU

Address: Operational Base(0x21D05000) + offset (0x031C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region4_xu1 The right boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region4_xu0 The left boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION4_YV

Address: Operational Base(0x21D05000) + offset (0x0320)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region4_yv1 The bottom boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region4_yv0 The top boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION5_XU

Address: Operational Base(0x21D05000) + offset (0x0324)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region5_xu1 The right boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region5_xu0 The left boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION5_YV

Address: Operational Base(0x21D05000) + offset (0x0328)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region5_yv1 The bottom boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region5_yv0 The top boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION6_XU

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Address: Operational Base(0x21D05000) + offset (0x032C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region6_xu1 The right boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region6_xu0 The left boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_REGION6_YV

Address: Operational Base(0x21D05000) + offset (0x0330)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_rawawb_exc_wp_region6_yv1 The bottom boundary of exclude region in XY or UV range
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_rawawb_exc_wp_region6_yv0 The top boundary of exclude region in XY or UV range

ISP_RAWAWB_5000_EXC_WP_WEIGHT0_3

Address: Operational Base(0x21D05000) + offset (0x0334)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x3f	sw_rawawb_exc_wp_region3_weight The white point weight of exclude region3
23:22	RO	0x0	reserved
21:16	RW	0x3f	sw_rawawb_exc_wp_region2_weight The white point weight of exclude region2
15:14	RO	0x0	reserved
13:8	RW	0x3f	sw_rawawb_exc_wp_region1_weight The white point weight of exclude region1
7:6	RO	0x0	reserved
5:0	RW	0x3f	sw_rawawb_exc_wp_region0_weight The white point weight of exclude region0

ISP_RAWAWB_5000_EXC_WP_WEIGHT4_6

Address: Operational Base(0x21D05000) + offset (0x0338)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21:16	RW	0x3f	sw_rawawb_exc_wp_region6_weight The white point weight of exclude region6
15:14	RO	0x0	reserved
13:8	RW	0x3f	sw_rawawb_exc_wp_region5_weight The white point weight of exclude region5
7:6	RO	0x0	reserved
5:0	RW	0x3f	sw_rawawb_exc_wp_region4_weight The white point weight of exclude region4

ISP_RAWAWB_5000_SUM_RGAIN_NOR_0

Address: Operational Base(0x21D05000) + offset (0x0340)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_rgain_nor_0 Read only: white point sum of R-gain

ISP_RAWAWB_5000_SUM_BGAIN_NOR_0

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Address: Operational Base(0x21D05000) + offset (0x0348)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_bgain_nor_0 Read only: white point sum of B-gain

ISP_RAWAWB_5000_WP_NUM_NOR_0

Address: Operational Base(0x21D05000) + offset (0x034C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_rawawb_wp_num_nor_0 Read only: white point number with weight

ISP_RAWAWB_5000_SUM_RGAIN_BIG_0

Address: Operational Base(0x21D05000) + offset (0x0350)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_rgain_big_0 Read only: white point sum of R-gain

ISP_RAWAWB_5000_SUM_BGAIN_BIG_0

Address: Operational Base(0x21D05000) + offset (0x0358)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_bgain_big_0 Read only: white point sum of B-gain

ISP_RAWAWB_5000_WP_NUM_BIG_0

Address: Operational Base(0x21D05000) + offset (0x035C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_rawawb_wp_num_big_0 Read only: white point number with weight

ISP_RAWAWB_5000_SUM_RGAIN_NOR_1

Address: Operational Base(0x21D05000) + offset (0x0370)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_rgain_nor_1 Read only: white point sum of R-gain

ISP_RAWAWB_5000_SUM_BGAIN_NOR_1

Address: Operational Base(0x21D05000) + offset (0x0378)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_bgain_nor_1 Read only: white point sum of B-gain

ISP_RAWAWB_5000_WP_NUM_NOR_1

Address: Operational Base(0x21D05000) + offset (0x037C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_rawawb_wp_num_nor_1 Read only: white point number with weight

ISP_RAWAWB_5000_SUM_RGAIN_BIG_1

Address: Operational Base(0x21D05000) + offset (0x0380)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_rgain_big_1 Read only: white point sum of R-gain

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ISP_RAWAWB_5000_SUM_BGAIN_BIG_1

Address: Operational Base(0x21D05000) + offset (0x0388)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_bgain_big_1 Read only: white point sum of B-gain

ISP_RAWAWB_5000_WP_NUM_BIG_1

Address: Operational Base(0x21D05000) + offset (0x038C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_rawawb_wp_num_big_1 Read only: white point number with weight

ISP_RAWAWB_5000_SUM_RGAIN_NOR_2

Address: Operational Base(0x21D05000) + offset (0x03A0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_rgain_nor_2 Read only: white point sum of R-gain

ISP_RAWAWB_5000_SUM_BGAIN_NOR_2

Address: Operational Base(0x21D05000) + offset (0x03A8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_bgain_nor_2 Read only: white point sum of B-gain

ISP_RAWAWB_5000_WP_NUM_NOR_2

Address: Operational Base(0x21D05000) + offset (0x03AC)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_rawawb_wp_num_nor_2 Read only: white point number with weight

ISP_RAWAWB_5000_SUM_RGAIN_BIG_2

Address: Operational Base(0x21D05000) + offset (0x03B0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_rgain_big_2 Read only: white point sum of R-gain

ISP_RAWAWB_5000_SUM_BGAIN_BIG_2

Address: Operational Base(0x21D05000) + offset (0x03B8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_bgain_big_2 Read only: white point sum of B-gain

ISP_RAWAWB_5000_WP_NUM_BIG_2

Address: Operational Base(0x21D05000) + offset (0x03BC)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_rawawb_wp_num_big_2 Read only: white point number with weight

ISP_RAWAWB_5000_SUM_RGAIN_NOR_3

Address: Operational Base(0x21D05000) + offset (0x03D0)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_rgain_nor_3 Read only: white point sum of R-gain

ISP_RAWAWB_5000_SUM_BGAIN_NOR_3

Address: Operational Base(0x21D05000) + offset (0x03D8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_bgain_nor_3 Read only: white point sum of B-gain

ISP_RAWAWB_5000_WP_NUM_NOR_3

Address: Operational Base(0x21D05000) + offset (0x03DC)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_rawawb_wp_num_nor_3 Read only: white point number with weight

ISP_RAWAWB_5000_SUM_BGAIN_BIG_3

Address: Operational Base(0x21D05000) + offset (0x03E0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_bgain_big_3 Read only: white point sum of B-gain

ISP_RAWAWB_5000_SUM_RGAIN_BIG_3

Address: Operational Base(0x21D05000) + offset (0x03E8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ro_rawawb_sum_rgain_big_3 Read only: white point sum of R-gain

ISP_RAWAWB_5000_WP_NUM_BIG_3

Address: Operational Base(0x21D05000) + offset (0x03EC)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_rawawb_wp_num_big_3 Read only: white point number with weight

ISP_RAWAWB_5000_SUM_R_EXC_0

Address: Operational Base(0x21D05000) + offset (0x05E0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RO	0x00000000	ro_sum_r_exc_0 The R-gain component summation in the exclude range

ISP_RAWAWB_5000_SUM_B_EXC_0

Address: Operational Base(0x21D05000) + offset (0x05E8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RO	0x00000000	ro_sum_b_exc_0 The B-gain component summation in the exclude range

ISP_RAWAWB_5000_WP_NM_EXC_0

Address: Operational Base(0x21D05000) + offset (0x05EC)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
17:0	RO	0x00000	ro_wp_nm_exc_0 The number of white point in the exclude region

ISP_RAWAWB_5000_SUM_R_EXC_1

Address: Operational Base(0x21D05000) + offset (0x05F0)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RO	0x00000000	ro_sum_r_exc_1 The R-gain component summation in the exclude range

ISP_RAWAWB_5000_SUM_B_EXC_1

Address: Operational Base(0x21D05000) + offset (0x05F8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RO	0x00000000	ro_sum_b_exc_1 The B-gain component summation in the exclude range

ISP_RAWAWB_5000_WP_NM_EXC_1

Address: Operational Base(0x21D05000) + offset (0x05FC)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	ro_wp_nm_exc_1 The number of white point in the exclude region

ISP_RAWAWB_5000_SUM_R_EXC_2

Address: Operational Base(0x21D05000) + offset (0x0600)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RO	0x00000000	ro_sum_r_exc_2 The R-gain component summation in the exclude range

ISP_RAWAWB_5000_SUM_B_EXC_2

Address: Operational Base(0x21D05000) + offset (0x0608)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RO	0x00000000	ro_sum_b_exc_2 The B-gain component summation in the exclude range

ISP_RAWAWB_5000_WP_NM_EXC_2

Address: Operational Base(0x21D05000) + offset (0x060C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	ro_wp_nm_exc_2 The number of white point in the exclude region

ISP_RAWAWB_5000_SUM_R_EXC_3

Address: Operational Base(0x21D05000) + offset (0x0610)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RO	0x00000000	ro_sum_r_exc_3 The R-gain component summation in the exclude range

ISP_RAWAWB_5000_SUM_B_EXC_3

Address: Operational Base(0x21D05000) + offset (0x0618)

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Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RO	0x00000000	ro_sum_b_exc_3 The B-gain component summation in the exclude range

ISP_RAWAWB_5000_WP_NM_EXC_3

Address: Operational Base(0x21D05000) + offset (0x061C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	ro_wp_nm_exc_3 The number of white point in the exclude region

ISP_RAWAWB_5000_Y_HIST01

Address: Operational Base(0x21D05000) + offset (0x0620)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_yhist_bin1 The bin of YHIST
15:0	RO	0x0000	ro_yhist_bin0 The bin of YHIST

ISP_RAWAWB_5000_Y_HIST23

Address: Operational Base(0x21D05000) + offset (0x0624)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_yhist_bin3 The bin of YHIST
15:0	RO	0x0000	ro_yhist_bin2 The bin of YHIST

ISP_RAWAWB_5000_Y_HIST45

Address: Operational Base(0x21D05000) + offset (0x0628)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_yhist_bin5 The bin of YHIST
15:0	RO	0x0000	ro_yhist_bin4 The bin of YHIST

ISP_RAWAWB_5000_Y_HIST67

Address: Operational Base(0x21D05000) + offset (0x062C)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ro_yhist_bin7 The bin of YHIST
15:0	RO	0x0000	ro_yhist_bin6 The bin of YHIST

ISP_RAWAWB_5000_WPNUM2_0

Address: Operational Base(0x21D05000) + offset (0x0630)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	ro_wp_num2_0 White pixel num when XY and UV all white pixel

ISP_RAWAWB_5000_WPNUM2_1

Address: Operational Base(0x21D05000) + offset (0x0634)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
17:0	RO	0x00000	ro_wp_num2_1 White pixel num when XY and UV all white pixel

ISP_RAWAWB_5000_WPNUM2_2

Address: Operational Base(0x21D05000) + offset (0x0638)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	ro_wp_num2_2 White pixel num when XY and UV all white pixel

ISP_RAWAWB_5000_WPNUM2_3

Address: Operational Base(0x21D05000) + offset (0x063C)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:0	RO	0x00000	ro_wp_num2_3 White pixel num when XY and UV all white pixel

ISP_RAWAWB_5000_WRAM_CTRL

Address: Operational Base(0x21D05000) + offset (0x0654)

Bit	Attr	Reset Value	Description
31	W1C	0x0	sys_rawawb_wram_clr_p Used for clear wram_wr_cnt
30:22	RO	0x000	reserved
21:16	RO	0x00	ro_rawawb_ram_cnt Configure ram count
15:0	RO	0x0000	reserved

ISP_RAWAWB_5000_WRAM_DATA_BASE

Address: Operational Base(0x21D05000) + offset (0x0660)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	WO	0x00	sw_rawawb_wp_blk_wei_w4 Sub-window weight from num0 to num224
23:18	WO	0x00	sw_rawawb_wp_blk_wei_w3 Sub-window weight from num0 to num224
17:12	WO	0x00	sw_rawawb_wp_blk_wei_w2 Sub-window weight from num0 to num224
11:6	WO	0x00	sw_rawawb_wp_blk_wei_w1 Sub-window weight from num0 to num224
5:0	WO	0x00	sw_rawawb_wp_blk_wei_w0 Sub-window weight from num0 to num224

44.4.2.32 RAWHIST

ISP_RAWHIST_BIG_4800_4900_CTRL

Address: **Operational Base** + offset (0x0000)

Bit	Attr	Reset Value	Description
31	W1C	0x0	sw_aehist_done This bit will be set to 1 by hardware when ae stats ready. The software can read ae stats and must clear this bit (write1 to clear) after operation. The hardware will run again when new flame arrived after this bit cleared.

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Bit	Attr	Reset Value	Description
30	RO	0x0	ro_aehist_working This module working signal
29:28	RW	0x2	sw_aehist_wnd_num 2'd0, 2'd1: 5x5 2'd2, 2'd3: 15x15
27	RO	0x0	reserved
26:24	RW	0x0	sw_aehist_data_sel 3'd0: Input_data[11:4] 3'd1: Input_data[10:3] 3'd2: Input_data[9:2] 3'd3: Input_data[8:1] 3'd4: Input_data[7:0] others: Input_data[7:0]
23:12	RW	0x000	sw_aehist_waterline For region statics
11	RO	0x0	reserved
10:8	RW	0x0	sw_aehist_mode Histogram mode, luminance is taken at ISP output before output formatter 3'd7, 3'd6: Must not be used 3'd5: Y (luminance) histogram 3'd4: B histogram 3'd3: G histogram 3'd2: R histogram 3'd1: Reserved 3'd0: Disable, no measurements Note: If RGB combined mode is used, then the 3 color components are sampled one after the other. The software has to assure that all 3 color components are inside the selected window.
7	RW	0x0	sw_aehist_debug_en The debug signal will toggle when this bit enable.
6:4	RO	0x0	reserved
3:1	RW	0x0	sw_aehist_stepsize Histogram previous divider, process every (step size) pixel, all other pixels are skipped
0	RW	0x0	sw_aehist_en Module enable bit

ISP_RAWHIST_BIG_4800_4900_SIZE

Address: **Operational Base** + offset (0x0004)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:16	RW	0x000	sw_aehist_v_size Vertical size in lines of one sub-window
15:11	RO	0x00	reserved
10:0	RW	0x000	sw_aehist_h_size Horizontal size in pixels of one sub-window

ISP_RAWHIST_BIG_4800_4900_OFFS

Address: **Operational Base** + offset (0x0008)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28:16	RW	0x0000	sw_aehist_v_offset Vertical offset of first window in pixels.
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_aehist_h_offset Horizontal offset of first window in pixels.

ISP_RAWHIST_BIG_4800_4900_HRAM_CTRL

Address: **Operational Base** + offset (0x000C)

Bit	Attr	Reset Value	Description
31	RW	0x0	rd_ram_en Just for debug
30:24	RO	0x00	reserved
23:16	RO	0x00	ro_ram_cnt RAM counter for write or read
15:8	RO	0x00	reserved
7:0	RW	0x00	sw_ram_offset RAM offset for write or read

ISP_RAWHIST_BIG_4800_4900_RAW2Y_CC

Address: **Operational Base** + offset (0x0010)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_rawae_off The coefficient of RAW2Y formula
23:16	RW	0x0d	sw_rawae_bcc RAW2Y blue channel coefficient
15:8	RW	0x20	sw_rawae_gcc RAW2Y green channel coefficient
7:0	RW	0x21	sw_rawae_rcc RAW2Y red channel coefficient

ISP_RAWHIST_BIG_4800_4900_WRAM_CTRL

Address: **Operational Base** + offset (0x0014)

Bit	Attr	Reset Value	Description
31	W1C	0x0	sys_rawhist_wram_clr_p Used for clear wram_wr_cnt
30:22	RO	0x000	reserved
21:16	RO	0x00	ro_ram_cnt RAM counter for write or read
15:6	RO	0x000	reserved
5:0	RW	0x00	sw_ram_offset RAM offset for write or read

ISP_RAWHIST_BIG_4800_4900_WEIGHT_BASE

Address: **Operational Base** + offset (0x0040)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x20	sw_aehist_weight_wnd4 Sub-window weight from num0 to num224
23:18	RW	0x20	sw_aehist_weight_wnd3 Sub-window weight from num0 to num224
17:12	RW	0x20	sw_aehist_weight_wnd2 Sub-window weight from num0 to num224
11:6	RW	0x20	sw_aehist_weight_wnd1 Sub-window weight from num0 to num224

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Bit	Attr	Reset Value	Description
5:0	RW	0x20	sw_aehist_weight_wnd0 Sub-window weight from num0 to num224

ISP_RAWHIST_BIG_4800_4900_RO_BASE_BIN

Address: **Operational Base** + offset (0x0080)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RO	0x0000000	ro_aehist_bin_x Measured bin count as 28-bit unsigned integer value with 5 fractional part

44.4.2.33 IE_CMSK

IMG_EFF_0200_IMG_EFF_CTRL

Address: Operational Base(0x21D00200) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	img_eff_en When black/white mode is enabled, UV component fix 8'h80. 1'b0: Disabled 1'b1: Enabled

IMG_EFF_0200_CMSK_CTRL0

Address: Operational Base(0x21D00200) + offset (0x0030)

Bit	Attr	Reset Value	Description
31	W1C	0x0	sys_cmsk_itself_force_upd Fouce update
30:15	RO	0x0000	reserved
14	RO	0x0	sw_msk_order_mode_shd Mosaic sample order shadow 1'b0: 0~7, 0~7 1'b1: 0~7, 7~0
13:12	RO	0x0	sw_cmsk_blksize_shd Mosaic block size 2'b00: 8x8 2'b01: 16x16 2'b10: 32x32 2'b11: 64x64
11	RO	0x0	sw_cmsk_en_bp_shd Cmsk module enable for bypass path shadow 1'b1: Enable 1'b0: Disable
10	RO	0x0	sw_cmsk_en_sp_shd Cmsk module enable for self path shadow 1'b1: Enable 1'b0: Disable
9	RO	0x0	sw_cmsk_en_mp_shd Cmsk module enable for main path shadow 1'b1: Enable 1'b0: Disable
8	RO	0x0	sw_cmks_en_shd Cmsk module enable shadow 1'b1: Enable 1'b0: Disable

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Bit	Attr	Reset Value	Description
7:6	RO	0x0	reserved
5:4	RO	0x0	sw_cmsk_blksize Mosaic block size 2'b00: 8x8 2'b01: 16x16 2'b10: 32x32 2'b11: 64x64
3	RW	0x0	sw_cmsk_en_bp Cmsk module enable for bp channel 1'b1: Enable 1'b0: Disable
2	RW	0x0	sw_cmsk_en_sp Cmsk module enable for self path 1'b1: Enable 1'b0: Disable
1	RW	0x0	sw_cmsk_en_mp Cmsk module enable for main path 1'b1: Enable 1'b0: Disable
0	RW	0x0	sw_cmsk_en Cmsk module enable 1'b1: Enable 1'b0: Disable

IMG_EFF_0200_CMSK_CTRL1

Address: Operational Base(0x21D00200) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RO	0x000	sw_cmsk_win_en_mp_shd Window 0~11 enable main path shadow
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_cmsk_win_en_mp Window 0~11 enable main path

IMG_EFF_0200_CMSK_CTRL2

Address: Operational Base(0x21D00200) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RO	0x000	sw_cmsk_win_en_sp_shd Window 0~11 enable self path shadow
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_cmsk_win_en_sp Window 0~11 enable self path

IMG_EFF_0200_CMSK_CTRL3

Address: Operational Base(0x21D00200) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RO	0x000	sw_cmsk_win_en_bp_shd Window 0~11 enable bypass path shadow
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_cmsk_win_en_bp Window 0~11 enable bypass path

IMG_EFF_0200_CMSK_CTRL4

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Address: Operational Base(0x21D00200) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RO	0x000	sw_cmsk_cov_mode_mp_shd Window 0~11 cover mode main path shadow 1'b1: Cover 1'b0: Mosaic
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_cmsk_cov_mode_mp Window 0~11 cover mode main path 1'b1: Cover 1'b0: Mosaic

IMG_EFF_0200_CMSK_CTRL5

Address: Operational Base(0x21D00200) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RO	0x000	sw_cmsk_cov_mode_sp_shd Window 0~11 cover mode self path shadow 1'b1: Cover 1'b0: Mosaic
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_cmsk_cov_mode_sp Window 0~11 cover mode self path 1'b1: Cover 1'b0: Mosaic

IMG_EFF_0200_CMSK_CTRL6

Address: Operational Base(0x21D00200) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RO	0x000	sw_cmsk_cov_mode_bp_shd Window 0~11 cover mode bypass path shadow 1'b1: Cover 1'b0: Mosaic
15:12	RO	0x0	reserved
11:0	RW	0x000	sw_cmsk_cov_mode_bp Window 0~11 cover mode bypass path 1'b1: Cover 1'b0: Mosaic

IMG_EFF_0200_CMSK_PIC_SIZE

Address: Operational Base(0x21D00200) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_pic_v_szie Picture v size
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_pic_h_size Picture horizontal size

IMG_EFF_0200_CMSK_YUV0

Address: Operational Base(0x21D00200) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
23:0	RW	0x000000	sw_cmsk_yuv0 Window 0 cover color, [7:0] y component, [15:8] u component, [23:16] v component

IMG_EFF_0200_CMSK_YUV1

Address: Operational Base(0x21D00200) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	sw_cmsk_yuv1 Window 1 cover color, [7:0] y component, [15:8] u component, [23:16] v component

IMG_EFF_0200_CMSK_YUV2

Address: Operational Base(0x21D00200) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	sw_cmsk_yuv2 Window 2 cover color, [7:0] y component, [15:8] u component, [23:16] v component

IMG_EFF_0200_CMSK_YUV3

Address: Operational Base(0x21D00200) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	sw_cmsk_yuv3 Window 3 cover color, [7:0] y component, [15:8] u component, [23:16] v component

IMG_EFF_0200_CMSK_YUV4

Address: Operational Base(0x21D00200) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	sw_cmsk_yuv4 Window 4 cover color, [7:0] y component, [15:8] u component, [23:16] v component

IMG_EFF_0200_CMSK_YUV5

Address: Operational Base(0x21D00200) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	sw_cmsk_yuv5 Window 5 cover color, [7:0] y component, [15:8] u component, [23:16] v component

IMG_EFF_0200_CMSK_YUV6

Address: Operational Base(0x21D00200) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	sw_cmsk_yuv6 Window 6 cover color, [7:0] y component, [15:8] u component, [23:16] v component

IMG_EFF_0200_CMSK_YUV7

Address: Operational Base(0x21D00200) + offset (0x006C)

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Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	sw_cmsk_yuv7 Window 7 cover color, [7:0] y component, [15:8] u component, [23:16] v component

IMG_EFF_0200_CMSK_YUV8

Address: Operational Base(0x21D00200) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	sw_cmsk_yuv8 Window 8 cover color, [7:0] y component, [15:8] u component, [23:16] v component

IMG_EFF_0200_CMSK_YUV9

Address: Operational Base(0x21D00200) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	sw_cmsk_yuv9 Window 9 cover color, [7:0] y component, [15:8] u component, [23:16] v component

IMG_EFF_0200_CMSK_YUV10

Address: Operational Base(0x21D00200) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	sw_cmsk_yuv10 Window 10 cover color, [7:0] y component, [15:8] u component, [23:16] v component

IMG_EFF_0200_CMSK_YUV11

Address: Operational Base(0x21D00200) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	reserved
23:0	RW	0x000000	sw_cmsk_yuv11 Window 11 cover color, [7:0] y component, [15:8] u component, [23:16] v component

IMG_EFF_0200_CMSK_OFFS0

Address: Operational Base(0x21D00200) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_cmsk_v_offs0 Window 0 vertical offset
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_cmsk_h_offs0 Window 0 horizontal offset

IMG_EFF_0200_CMSK_SIZE0

Address: Operational Base(0x21D00200) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_cmsk_v_size0 Window 0 vertical size
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x0000	sw_cmsk_h_size0 Window 0 horizontal size

IMG_EFF_0200_CMSK_OFFS1

Address: Operational Base(0x21D00200) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_cmsk_v_offs1 Window 1 vertical offset
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_cmsk_h_offs1 Window 1 horizontal offset

IMG_EFF_0200_CMSK_SIZE1

Address: Operational Base(0x21D00200) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_cmsk_v_size1 Window 1 vertical size
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_cmsk_h_size1 Window 1 horizontal size

IMG_EFF_0200_CMSK_OFFS2

Address: Operational Base(0x21D00200) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_cmsk_v_offs0 Window 0 vertical offset
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_cmsk_h_offs0 Window 0 horizontal offset

IMG_EFF_0200_CMSK_SIZE2

Address: Operational Base(0x21D00200) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_cmsk_v_size2 Window 2 vertical size
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_cmsk_h_size2 Window 2 horizontal size

IMG_EFF_0200_CMSK_OFFS3

Address: Operational Base(0x21D00200) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_cmsk_v_offs3 Window 3 vertical offset
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_cmsk_h_offs3 Window 3 horizontal offset

IMG_EFF_0200_CMSK_SIZE3

Address: Operational Base(0x21D00200) + offset (0x009C)

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Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_cmsk_v_size3 Window 3 vertical size
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_cmsk_h_size3 Window 3 horizontal size

IMG_EFF_0200_CMSK_OFFS4

Address: Operational Base(0x21D00200) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_cmsk_v_offs4 Window 4 vertical offset
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_cmsk_h_offs4 Window 4 horizontal offset

IMG_EFF_0200_CMSK_SIZE4

Address: Operational Base(0x21D00200) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_cmsk_v_size4 Window 4 vertical size
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_cmsk_h_size4 Window 4 horizontal size

IMG_EFF_0200_CMSK_OFFS5

Address: Operational Base(0x21D00200) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_cmsk_v_offs5 Window 5 vertical offset
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_cmsk_h_offs5 Window 5 horizontal offset

IMG_EFF_0200_CMSK_SIZE5

Address: Operational Base(0x21D00200) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_cmsk_v_size5 Window 5 vertical size
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_cmsk_h_size5 Window 5 horizontal size

IMG_EFF_0200_CMSK_OFFS6

Address: Operational Base(0x21D00200) + offset (0x00B0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_cmsk_v_offs6 Window 6 vertical offset
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x0000	sw_cmsk_h_offs6 Window 6 horizontal offset

IMG_EFF_0200_CMSK_SIZE6

Address: Operational Base(0x21D00200) + offset (0x00B4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_cmsk_v_size6 Window 6 vertical size
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_cmsk_h_size6 Window 6 horizontal size

IMG_EFF_0200_CMSK_OFFS7

Address: Operational Base(0x21D00200) + offset (0x00B8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_cmsk_v_offs7 Window 7 vertical offset
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_cmsk_h_offs7 Window 7 horizontal offset

IMG_EFF_0200_CMSK_SIZE7

Address: Operational Base(0x21D00200) + offset (0x00BC)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_cmsk_v_size7 Window 7 vertical size
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_cmsk_h_size7 Window 7 horizontal size

IMG_EFF_0200_CMSK_OFFS8

Address: Operational Base(0x21D00200) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_cmsk_v_offs8 Window 8 vertical offset
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_cmsk_h_offs8 Window 8 horizontal offset

IMG_EFF_0200_CMSK_SIZE8

Address: Operational Base(0x21D00200) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_cmsk_v_size8 Window 8 vertical size
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_cmsk_h_size8 Window 7 horizontal size

IMG_EFF_0200_CMSK_OFFS9

Address: Operational Base(0x21D00200) + offset (0x00C8)

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Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_cmsk_v_offs9 Window 9 vertical offset
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_cmsk_h_offs9 Window 9 horizontal offset

IMG_EFF_0200_CMSK_SIZE9

Address: Operational Base(0x21D00200) + offset (0x00CC)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_cmsk_v_size9 Window 9 vertical size
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_cmsk_h_size9 Window 9 horizontal size

IMG_EFF_0200_CMSK_OFFS10

Address: Operational Base(0x21D00200) + offset (0x00D0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_cmsk_v_offs10 Window 10 vertical offset
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_cmsk_h_offs10 Window 10 horizontal offset

IMG_EFF_0200_CMSK_SIZE10

Address: Operational Base(0x21D00200) + offset (0x00D4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_cmsk_v_size10 Window 10 vertical size
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_cmsk_h_size10 Window 10 horizontal size

IMG_EFF_0200_CMSK_OFFS11

Address: Operational Base(0x21D00200) + offset (0x00D8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_cmsk_v_offs11 Window 11 vertical offset
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_cmsk_h_offs11 Window 11 horizontal offset

IMG_EFF_0200_CMSK_SIZE11

Address: Operational Base(0x21D00200) + offset (0x00DC)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_cmsk_v_size11 Window 11 vertical size
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x0000	sw_cmsk_h_size11 Window 11 horizontal size

44.4.2.34 CPROC

CPROC_0800_CTRL

Address: Operational Base(0x21D00800) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:4	RO	0x0000000	reserved
3	RW	0x0	cproc_c_out_range Color processing chrominance pixel clipping range at output 0: CbCr_out clipping range 16..240 according to ITU-R BT.601 standard 1: full UV_out clipping range 0..255
2	RW	0x0	cproc_y_in_range Color processing luminance input range (offset processing) 0: Y_in range 64..940 according to ITU-R BT.601 standard; offset of 64 will be subtracted from Y_in 1: Y_in full range 0..1023; no offset will be subtracted from Y_in
1	RW	0x0	cproc_y_out_range Color processing luminance output clipping range 0: Y_out clipping range 16..235; offset of 16 is added to Y_out according to ITU-R BT.601 standard 1: Y_out clipping range 0..255; no offset is added to Y_out
0	RW	0x0	cproc_enable color processing enable 0: color processing is bypassed 2 * 10 Bit input data are truncated to 2 * 8Bit output data 1: color processing is active output data are rounded to 2 * 8Bit and clipping is active

CPROC_0800_CONTRAST

Address: Operational Base(0x21D00800) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x80	cproc_contrast contrast adjustment value 00H equals x 0.0 ... 80H equals x 1.0 ... FFH equals x 1.992

CPROC_0800_BRIGHTNESS

Address: Operational Base(0x21D00800) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	cproc_brightness brightness adjustment value 80H equals -128 ... 00H equals +0 ... 7FH equals +127

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CPROC_0800_SATURATION

Address: Operational Base(0x21D00800) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x80	cproc_saturation saturation adjustment value 00H equals x 0.0 ... 80H equals x 1.0 ... FFH equals x 1.992

CPROC_0800_HUE

Address: Operational Base(0x21D00800) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	reserved
7:0	RW	0x00	cproc_hue hue adjustment value 80H equals -90 deg ... 00H equals 0 deg ... 7FH equals +87.188 deg

44.4.2.35 MPFBC

ISP_MPFBC_18C0_CTRL

Address: Operational Base(0x21D018C0) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11	RW	0x1	sw_bp_yuv_mode_org Bypass path (BP) output YUV mode 1'b0: Crop BP path from YUV422 to YUV420 1'b1: No change BP path output format
10	RW	0x1	sw_sp_yuv_mode_org Self path (SP) output YUV mode 1'b0: Crop SP path from YUV422 to YUV420 1'b1: No change SP path output format
9	RW	0x1	sw_mp_yuv_mode_org Main path (MP) output YUV mode 1'b0: Crop MP path from YUV422 to YUV420 1'b1: No change MP path output format
8	RW	0x0	sw_seperate_yuv_cfg MI output YUV format configured seperately enable 1'b0: All MI path output YUV configuration reuse sw_mp_sp_yuv_mode. 1'b1: All MI path output YUV configuration seperately.
7:3	RO	0x00	reserved
2:1	RW	0x1	sw_mp_sp_yuv_mode MP/SP/BP YUV format 2'b00: YUV420 8bit 2'b01: YUV422 8bit Others: Reserved
0	RO	0x0	reserved

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44.4.2.36 3A_COMMON

COMMON3A_W3A_CTRL0

Address: Operational Base(0x21D04000) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	W1C	0x0	sys_itself_force_upd_3a 1'b1: itself update for w3a to update shadow register. The signal will be auto clear after cfg_wr for one cycle.
30	W1C	0x0	sys_itself_force_upd_3a_f 1'b1: itself update for w3a to update shadow register. The signal will be auto clear after cfg_wr for one cycle. For ISP-FE using when AIISP mode.
29:10	RO	0x00000	reserved
9	RW	0x0	sw_3a_rawlsc_sel 1'b0: RAWAWB select RAWLSC 1'b1: AIAWB select RAWLSC
8	RW	0x0	sw_b3dnrout_ilg_bypass_en B3DNR out ILG bypass enable bit.
7	RW	0x0	sw_w3a_fe_int_mode 1'b1: The each channel done can trigger pre3a_done interrupt. 1'b0: The w3a fe source alldone can trigger pre3a_done interrupt.
6	RW	0x0	sw_w3a_frm_hold_dis Backdoor for frame hold
5	RW	0x0	sw_w3a_clk_gating_dis 1'b1:The clock gating of w3a is disable. 1'b0:The clock gating of w3a is enable.
4	RW	0x0	sw_3a_auto_clr_en 1'b1: The w3a auto clear is enable 1'b0: The w3a auto clear is not enable, clear should be through software
3	RW	0x0	sw_w3a_pdaf2ddr_dis 1'b1: The w3a can not hold dpcc 1'b0: The w3a can hold dpcc
2	RW	0x0	sw_w3a_3a_hold_dis 1'b1: The 3a channel of w3a can not hold dpcc 1'b0: The 3a channel of w3a can hold dpcc
1	RW	0x0	sw_w3a_pdaf2ddr_en 1'b1: w3a write pdaf2ddr function is enable 1'b0: w3a write pdaf2ddr function is disable
0	RW	0x0	sw_w3a_en 1'b1: w3a slice mode is enable 1'b0: w3a frame mode(old version) is enable

COMMON3A_W3A_CTRL1

Address: Operational Base(0x21D04000) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:4	RW	0x0f0	sw_w3a_pdaf_vir_stride The value stands for virtual stride of pdaf data in ddr
3:0	RO	0x0	reserved

COMMON3A_W3A_INT_EN

Address: Operational Base(0x21D04000) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:17	RO	0x0000	reserved
16	RW	0x0	sw_w3a_err_int_en 1'b1: the overflow error interrupt is enable 1'b0: the overflow error interrupt is disable
15:8	RO	0x00	reserved
7	RW	0x0	sw_w3a_aiawb_done_int_en 1'b1: the aiawb done interrupt is enable 1'b0: the aiawb done interrupt is disable
6	RW	0x0	sw_w3a_pdaf_done_int_en 1'b1: the pdaf done interrupt is enable 1'b0: the pdaf done interrupt is disable
5	RW	0x0	sw_w3a_rawawb_done_int_en 1'b1: the rawawb done interrupt is enable 1'b0: the rawawb done interrupt is disable
4	RW	0x0	sw_w3a_rawaf_done_int_en 1'b1: the rawaf done interrupt is enable 1'b0: the rawaf done interrupt is disable
3:2	RO	0x0	reserved
1	RW	0x0	sw_w3a_rawae_ch0_done_int_en 1'b1: the rawae channel 0 done interrupt is enable 1'b0: the rawae channel 0 done interrupt is disable
0	RW	0x0	sw_w3a_rawae_big_done_int_en 1'b1: the rawae big done interrupt is enable 1'b0: the rawae big done interrupt is disable

COMMON3A_W3A_INT_STAT

Address: Operational Base(0x21D04000) + offset (0x0014)

Bit	Attr	Reset Value	Description
31	RW	0x0	ro_w3a_wcfifo_rd_err_int_stat The raw status of read wcfifo overflow interrupt.
30	RW	0x0	ro_w3a_wcfifo_wr_err_int_stat The raw status of write wcfifo overflow interrupt.
29:25	RO	0x00	reserved
24	RO	0x0	ro_w3a_pdaf_ovf_int_stat The raw status of pdaf overflow interrupt.
23	RO	0x0	ro_w3a_awb_ovf_int_stat The raw status of rawawb overflow interrupt.
22	RO	0x0	ro_w3a_af_aehgl_ovf_int_stat The raw status of rawaf aehgl overflow interrupt.
21	RO	0x0	ro_w3a_af_viir_ovf_int_stat The raw status of rawaf viir overflow interrupt.
20	RO	0x0	ro_w3a_af_hiir_ovf_int_stat The raw status of rawaf hiir overflow interrupt.
19:18	RO	0x0	reserved
17	RO	0x0	ro_w3a_ae_ch0_ovf_int_stat The raw status of rawae channel 0 overflow interrupt.
16	RO	0x0	ro_w3a_ae_big_ovf_int_stat The raw status of rawae big overflow interrupt.
15:8	RO	0x00	reserved
7	RO	0x0	ro_w3a_aiawb_done_int_stat The raw status of aiawb done interrupt.
6	RO	0x0	ro_w3a_pdaf_done_int_stat The raw status of pdaf done interrupt.
5	RO	0x0	ro_w3a_rawawb_done_int_stat The raw status of rawawb done interrupt.

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Bit	Attr	Reset Value	Description
4	RO	0x0	ro_w3a_rawaf_done_int_stat The raw status of rawaf done interrupt.
3:2	RO	0x0	reserved
1	RO	0x0	ro_w3a_rawae_ch0_done_int_stat The raw status of rawae channel 0 done interrupt.
0	RO	0x0	ro_w3a_rawae_big_done_int_stat The raw status of rawae big done interrupt.

COMMON3A_W3A_MASK_INT_STAT

Address: Operational Base(0x21D04000) + offset (0x0018)

Bit	Attr	Reset Value	Description
31	RW	0x0	ro_w3a_wcfifo_rd_err_msk_int_stat The mask status of read wcfifo overflow interrupt.
30	RW	0x0	ro_w3a_wcfifo_wr_err_msk_int_stat The mask status of write wcfifo overflow interrupt.
29:25	RO	0x00	reserved
24	RO	0x0	ro_w3a_pdaf_ovf_msk_int_stat The mask status of pdaf overflow interrupt.
23	RO	0x0	ro_w3a_awb_ovf_msk_int_stat The mask status of rawawb overflow interrupt.
22	RO	0x0	ro_w3a_af_aehgl_ovf_msk_int_stat The mask status of rawaf aehgl overflow interrupt.
21	RO	0x0	ro_w3a_af_viir_ovf_msk_int_stat The mask status of rawaf viir overflow interrupt.
20	RO	0x0	ro_w3a_af_hiir_ovf_msk_int_stat The mask status of rawaf hiir overflow interrupt.
19:18	RO	0x0	reserved
17	RO	0x0	ro_w3a_ae_ch0_ovf_int_stat The mask status of rawae channel 0 overflow interrupt.
16	RO	0x0	ro_w3a_ae_big_ovf_msk_int_stat The mask status of rawae big overflow interrupt.
15:8	RO	0x00	reserved
7	RO	0x0	ro_w3a_aiawb_done_msk_int_stat The mask status of aiawb done interrupt.
6	RO	0x0	ro_w3a_pdaf_done_msk_int_stat The mask status of pdaf done interrupt.
5	RO	0x0	ro_w3a_rawawb_done_msk_int_stat The mask status of rawawb done interrupt.
4	RO	0x0	ro_w3a_rawaf_done_msk_int_stat The mask status of rawaf done interrupt.
3:2	RO	0x0	reserved
1	RO	0x0	ro_w3a_rawae_ch0_done_msk_int_stat The mask status of rawae channel 0 done interrupt.
0	RO	0x0	ro_w3a_rawae_big_done_msk_int_stat The mask status of rawae big done interrupt.

COMMON3A_W3A_AEBIG_ADDR

Address: Operational Base(0x21D04000) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_w3a_ae_big_addr The value stands for memory address of rawae big data.(the data is 16 byte align, so low 4 bit auto fill 0)
3:0	RO	0x0	reserved

COMMON3A_W3A_AECH0_ADDR

Address: Operational Base(0x21D04000) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_w3a_ae_CH0_addr The value stands for memory address of rawae channel 0 data.(the data is 16 byte align, so low 4 bit auto fill 0)
3:0	RO	0x0	reserved

COMMON3A_W3A_AF_ADDR

Address: Operational Base(0x21D04000) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_w3a_af_addr The value stands for memory address of rawaf data.(the data is 16 byte align, so low 4 bit auto fill 0)
3:0	RO	0x0	reserved

COMMON3A_W3A_AWB_ADDR

Address: Operational Base(0x21D04000) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_w3a_awb_addr The value stands for memory address of rawawb data.
3:0	RO	0x0	reserved

COMMON3A_W3A_PDAF_ADDR

Address: Operational Base(0x21D04000) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_w3a_pdaf_addr The value stands for memory address of pdaf data.(the data is 16 byte align, so low 4 bit auto fill 0)
3:0	RO	0x0	reserved

COMMON3A_W3A_AEBIG_ADDR_SHD

Address: Operational Base(0x21D04000) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_w3a_aebig_addr_shd The shadow value of sw_w3a_aebig_addr.
3:0	RO	0x0	reserved

COMMON3A_W3A_AE0_ADDR_SHD

Address: Operational Base(0x21D04000) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_w3a_ae0_addr_shd The shadow value of sw_w3a_ae0_addr.
3:0	RO	0x0	reserved

COMMON3A_W3A_AF_ADDR_SHD

Address: Operational Base(0x21D04000) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_w3a_af_addr_shd The shadow value of sw_w3a_af_addr.
3:0	RO	0x0	reserved

COMMON3A_W3A_AWB_ADDR_SHD

Address: Operational Base(0x21D04000) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_w3a_awb_addr_shd The shadow value of sw_w3a_awb_addr.

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Bit	Attr	Reset Value	Description
3:0	RO	0x0	reserved

COMMON3A_W3A_PDAF_ADDR_SHD

Address: Operational Base(0x21D04000) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_w3a_pdaf_addr_shd The shadow value of sw_w3a_pdaf_addr.
3:0	RO	0x0	reserved

COMMON3A_VI3A_CTRL0

Address: Operational Base(0x21D04000) + offset (0x0080)

Bit	Attr	Reset Value	Description
31	W1C	0x0	sys_itself_force_upd_vi0 1'b1: itself update for vi3a to update shadow register, and for RAWAE0 start
30:29	RO	0x0	reserved
28	W1C	0x0	sys_vi3a_soft_rst_p 1'b1: for the module(which select input source is VICAP) soft reset using
27:8	RO	0x00000	reserved
7	RW	0x0	sw_vi3a_ckg_dis 1'b1: the gating of clock is disabled. 1'b0: the gating of clock is enabled.
6	RW	0x0	sw_vi3a_drop1pix_en 1'b1: vi3a drop 1 pixel is enable 1'b0: vi3a drop 1 pixel is not enable
5:4	RW	0x0	sw_vi3a_bayer_pat The value stands for the bayer pattern of vi3a input image.
3	RW	0x1	sw_vi3a_awbgain_en 1'b1: vi3a awbgain is enable 1'b0: vi3a awbgain is not enable
2	RW	0x1	sw_vi3a_bls_en 1'b1: vi3a bls is enable 1'b0: vi3a bls is not enable
1	RW	0x0	sw_vi3a_af_from_vicap 1'b1: af data is from vicap 1'b0: af data is from isp
0	RW	0x0	sw_vi3a_ae_from_vicap 1'b1: ae data is from vicap 1'b0: ae data is from isp

COMMON3A_VI3A_CTRL1

Address: Operational Base(0x21D04000) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	sw_vi3a_v_size The value stands for the v size of vi3a input image.
15	RO	0x0	reserved
14:0	RW	0x0000	sw_vi3a_h_size The value stands for the h size of vi3a input image.

COMMON3A_VI3A_INT_EN

Address: Operational Base(0x21D04000) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:19	RO	0x0000	reserved

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Bit	Attr	Reset Value	Description
18	RW	0x0	sw_vi3a_viaf_all_overflow_int_en 1'b1: the vi3a rawaf overflow interrupt is enable 1'b0: the vi3a rawaf overflow interrupt is disable
17	RW	0x0	sw_vi3a_err_int_en 1'b1: the w3a vi3a overflow interrupt is enable 1'b0: the w3a vi3a overflow interrupt is disable
16	RW	0x0	sw_vi3a_overflow_int_en 1'b1: the vi3a overflow interrupt is enable 1'b0: the vi3a overflow interrupt is disable
15:11	RO	0x00	reserved
10	RW	0x0	sw_vi3a_vihist0_finish_int_en 1'b1: the vi3a rawhist channel 0 finish interrupt is enable 1'b0: the vi3a rawhist channel 0 finish interrupt is disable
9	RW	0x0	sw_vi3a_viae0_finish_int_en 1'b1: the vi3a rawae channel 0 finish interrupt is enable 1'b0: the vi3a rawae channel 0 finish interrupt is disable
8	RW	0x0	sw_vi3a_viaf_finish_int_en 1'b1: the vi3a rawaf finish interrupt is enable 1'b0: the vi3a rawaf finish interrupt is disable
7:3	RO	0x00	reserved
2	RW	0x0	sw_vi3a_rawaf_done_int_en 1'b1: the vi3a rawaf done interrupt is enable 1'b0: the vi3a rawaf done interrupt is disable
1	RW	0x0	sw_vi3a_rawae_ch0_done_int_en 1'b1: the vi3a rawae channel 0 done interrupt is enable 1'b0: the vi3a rawae channel 0 done interrupt is disable
0	RW	0x0	sw_vi3a_ddr_done_int_en 1'b1: the vi3a ddr done interrupt is enable 1'b0: the vi3a ddr done interrupt is disable

COMMON3A_VI3A_INT_STAT

Address: Operational Base(0x21D04000) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RO	0x0	ro_vi3a_viaf_all_overflow_int_stat The raw status of vi3a rawaf overflow finish interrupt.
20	RO	0x0	ro_vi3a_af_aehgl_ovf_int_stat The raw status of vi3a rawaf aehgl overflow finish interrupt.
19	RO	0x0	ro_vi3a_af_viir_ovf_int_stat The raw status of vi3a rawaf viir overflow finish interrupt.
18	RO	0x0	ro_vi3a_af_hiir_ovf_int_stat The raw status of vi3a rawaf hiir overflow finish interrupt.
17	RO	0x0	ro_vi3a_ae_ch0_ovf_int_stat The raw status of vi3a rawae channel 0 overflow finish interrupt.
16	RO	0x0	ro_vi3a_overflow_int_stat The raw status of vi3a overflow finish interrupt.
15:11	RO	0x00	reserved
10	RO	0x0	ro_vi3a_vihist0_finish_int_stat The raw status of vi3a rawhist channel 0 finish interrupt.
9	RO	0x0	ro_vi3a_viae0_finish_int_stat The raw status of vi3a rawae channel 0 finish interrupt.
8	RO	0x0	ro_vi3a_viaf_finish_int_stat The raw status of vi3a rawaf finish interrupt.
7:3	RO	0x00	reserved

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Bit	Attr	Reset Value	Description
2	RO	0x0	ro_vi3a_rawaf_done_int_stat The raw status of vi3a rawaf done interrupt.
1	RO	0x0	ro_vi3a_rawae_ch0_done_int_stat The raw status of vi3a rawae channel 0 done interrupt.
0	RO	0x0	ro_vi3a_ddr_done_int_stat The raw status of vi3a ddr done interrupt.

COMMON3A_VI3A_MASK_INT_STAT

Address: Operational Base(0x21D04000) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:22	RO	0x000	reserved
21	RO	0x0	ro_vi3a_viaf_all_overflow_msk_int_stat The mask status of vi3a rawaf overflow finish interrupt.
20	RO	0x0	ro_vi3a_af_aehgl_ovf_msk_int_stat The mask status of vi3a rawaf aehgl overflow finish interrupt.
19	RO	0x0	ro_vi3a_af_viir_ovf_msk_int_stat The mask status of vi3a rawaf viir overflow finish interrupt.
18	RO	0x0	ro_vi3a_af_hiir_ovf_msk_int_stat The mask status of vi3a rawaf hiir overflow finish interrupt.
17	RO	0x0	ro_vi3a_ae_ch0_ovf_msk_int_stat The mask status of vi3a rawae channel 0 overflow finish interrupt.
16	RO	0x0	ro_vi3a_overflow_msk_int_stat The mask status of vi3a overflow finish interrupt.
15:11	RO	0x00	reserved
10	RO	0x0	ro_vi3a_vihist0_finish_msk_int_stat The mask status of vi3a rawhist channel 0 finish interrupt.
9	RO	0x0	ro_vi3a_viae0_finish_msk_int_stat The mask status of vi3a rawhist channel 0 finish interrupt.
8	RO	0x0	ro_vi3a_viaf_finish_msk_int_stat The mask status of vi3a rawaf finish interrupt.
7:3	RO	0x00	reserved
2	RO	0x0	ro_vi3a_rawaf_done_msk_int_stat The mask status of vi3a rawaf done interrupt.
1	RO	0x0	ro_vi3a_rawae_ch0_done_msk_int_stat The mask status of vi3a rawae channel 0 done interrupt.
0	RO	0x0	ro_vi3a_ddr_done_msk_int_stat The mask status of vi3a ddr done interrupt.

COMMON3A_VI3A_BLS_FIXED_0

Address: Operational Base(0x21D04000) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0002	sw_vi3a_bls_b_fixed The value stands for vi3a bls b fixed.
15:13	RO	0x0	reserved
12:0	RW	0x0001	sw_vi3a_bls_a_fixed The value stands for vi3a bls a fixed.

COMMON3A_VI3A_BLS_FIXED_1

Address: Operational Base(0x21D04000) + offset (0x00A4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0004	sw_vi3a_bls_d_fixed The value stands for vi3a bls d fixed.

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Bit	Attr	Reset Value	Description
15:13	RO	0x0	reserved
12:0	RW	0x0003	sw_vi3a_bls_c_fixed The value stands for vi3a bls c fixed.

COMMON3A_VI3A_GAIN_0

Address: Operational Base(0x21D04000) + offset (0x00A8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x102	sw_vi3a_gain_gr The value stands for vi3a gain gr.
15:12	RO	0x0	reserved
11:0	RW	0x101	sw_vi3a_gain_r The value stands for vi3a gain r.

COMMON3A_VI3A_GAIN_1

Address: Operational Base(0x21D04000) + offset (0x00AC)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x104	sw_vi3a_gain_gb The value stands for vi3a gain gb.
15:12	RO	0x0	reserved
11:0	RW	0x103	sw_vi3a_gain_b The value stands for vi3a gain b.

COMMON3A_W3A_FE_INT_EN

Address: Operational Base(0x21D04000) + offset (0x00C0)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	sw_w3a_fe_alldone_int_en 1'b1: the w3a fe source alldone interrupt is enable 1'b0: the w3a fe source alldone interrupt is disable

COMMON3A_W3A_FE_INT_STAT

Address: Operational Base(0x21D04000) + offset (0x00C4)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	ro_w3a_fe_alldone_int_stat The raw status of w3a fe source all done interrupt.

COMMON3A_W3A_FE_MASK_INT_STAT

Address: Operational Base(0x21D04000) + offset (0x00C8)

Bit	Attr	Reset Value	Description
31:1	RO	0x00000000	reserved
0	RW	0x0	ro_w3a_fe_alldone_msk_int_stat The mask status of w3a fe source all done interrupt.

COMMON3A_W3A_DBG0

Address: Operational Base(0x21D04000) + offset (0x00F0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ro_w3a_dbg0 The debug message of w3a.{23'd0,w3a_pdaf2ddr_hold,rd_current_state,wr_current_state}

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ISP_AI_1200_CTRL

Address: Operational Base(0x21D01200) + offset (0x0000)

Bit	Attr	Reset Value	Description
31:25	RO	0x00	reserved
24	RW	0x0	sw_aipre_its_force_upd Aipre itself update.NOTE: it is a level signal not a auto clr pulse.
23:18	RO	0x00	reserved
17	RW	0x0	sw_aipre_luma2gain_dis VPSL-luma2x2 back to gain cacl disable.
16	RW	0x0	sw_aipre_narmap_inv AIPRE narmap output 1'b0: normal output 1'b1: 256-narmap output
15	RW	0x0	sw_aipre_gain_mode AIPRE gain output mode 1'b0: output 4x2 1'b1: output 8x2
14	RW	0x0	sw_aipre_gain_bypass AIPRE gain bypass bit 1'b0: output nearmap 1'b1: output gain
13	RW	0x0	sw_aipre_nl_ddr_mode AIPRE nl data ddr mode. 1'b0: 8bit = iir-nl for NPU 1'b1: 16bit = 11bit-iir-nl<<5 fpr VPSL
12	RW	0x0	sw_aipre_yraw_sel AIPRE yraw date sel path 1'b0: yuv path 1'b1: raw-iir path
11	RW	0x0	sw_aipre_gain2ddr_en AIPRE-gain write into ddr enable.
10	RW	0x0	sw_aipre_gain_en AIPRE-gain enable.
9	RW	0x0	sw_aipre_iir2ddr_en AIPRE-iir/nl write into ddr enable.
8	RW	0x0	sw_aipre_iir_en AIPRE-iir/nl enable.
7	RO	0x0	reserved
6	RW	0x0	sw_npu_curve_en AI-ISP raw data curve(12bit to 12bit convertion) enable
5:4	RW	0x1	sw_aiisp_gain_mode AI-ISP gain data mode. 2'b00: Gain 32bit mode, [6'b0, wgt[5:0], w1[5:0], w0[5:0], gain[7:0]] 2'b01: Gain 16bit mode, [2'b0, w01[5:0], gain1[7:0], 2'b0, w00[5:0], gain0[7:0]] 2'b10: Gain 16bit mode, [2'b0, wgt3[5:0], 2'b0, wgt2[5:0], 2'b0, wgt1[5:0], 2'b0, wgt0[5:0]] 2'b11: Reserved Note: If sw_aiisp_gain_mode= 2'b10 (only wgt), sw_aiisp_path_en must be set 0.
3	RW	0x0	sw_aiisp_hdr_en AIISP hdr enable; 1'b1, aiisp gain-rd reuse ldch-rd path, aiisp support hdr.

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Bit	Attr	Reset Value	Description
2	RW	0x0	sw_aiisp_raw12_msb npu/aiisp mi-read raw12 msb in 16bit.
1	W1C	0x0	sys_aiisp_st AI-ISP data and gain read start
0	RW	0x0	sw_aiisp_path_en AI-ISP path enable

ISP_AI_1200_SIGMA_Y0

Address: Operational Base(0x21D01200) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x00d	sw_npu_sigma_y1 Curve-y1 value of sigma table. Note: No reset value
15:12	RO	0x0	reserved
11:0	RW	0x00b	sw_npu_sigma_y0 Curve-y0 value of sigma table. Note: No reset value

ISP_AI_1200_SIGMA_Y1

Address: Operational Base(0x21D01200) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x00d	sw_npu_sigma_y3 Curve-y3 value of sigma table. Note: No reset value
15:12	RO	0x0	reserved
11:0	RW	0x00b	sw_npu_sigma_y2 Curve-y2 value of sigma table. Note: No reset value

ISP_AI_1200_SIGMA_Y2

Address: Operational Base(0x21D01200) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x00d	sw_npu_sigma_y5 Curve-y5 value of sigma table. Note: No reset value
15:12	RO	0x0	reserved
11:0	RW	0x00b	sw_npu_sigma_y4 Curve-y4 value of sigma table. Note: No reset value

ISP_AI_1200_SIGMA_Y3

Address: Operational Base(0x21D01200) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x00d	sw_npu_sigma_y7 Curve-y7 value of sigma table. Note: No reset value
15:12	RO	0x0	reserved
11:0	RW	0x00b	sw_npu_sigma_y6 Curve-y6 value of sigma table. Note: No reset value

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ISP_AI_1200_SIGMA_Y4

Address: Operational Base(0x21D01200) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x00d	sw_npu_sigma_y9 Curve-y9 value of sigma table. Note: No reset value
15:12	RO	0x0	reserved
11:0	RW	0x00b	sw_npu_sigma_y8 Curve-y8 value of sigma table. Note: No reset value

ISP_AI_1200_SIGMA_Y5

Address: Operational Base(0x21D01200) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x00d	sw_npu_sigma_y11 Curve-y11 value of sigma table. Note: No reset value
15:12	RO	0x0	reserved
11:0	RW	0x00b	sw_npu_sigma_y10 Curve-y10 value of sigma table. Note: No reset value

ISP_AI_1200_SIGMA_Y6

Address: Operational Base(0x21D01200) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x00d	sw_npu_sigma_y13 Curve-y13 value of sigma table. Note: No reset value
15:12	RO	0x0	reserved
11:0	RW	0x00b	sw_npu_sigma_y12 Curve-y12 value of sigma table. Note: No reset value

ISP_AI_1200_SIGMA_Y7

Address: Operational Base(0x21D01200) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x00d	sw_npu_sigma_y15 Curve-y15 value of sigma table. Note: No reset value
15:12	RO	0x0	reserved
11:0	RW	0x00b	sw_npu_sigma_y14 Curve-y14 value of sigma table. Note: No reset value

ISP_AI_1200_SIGMA_Y8

Address: Operational Base(0x21D01200) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x00d	sw_npu_sigma_y17 Curve-y17 value of sigma table. Note: No reset value
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x00b	sw_npu_sigma_y16 Curve-y16 value of sigma table. Note: No reset value

ISP_AI_1200_SIGMA_Y9

Address: Operational Base(0x21D01200) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x00d	sw_npu_sigma_y19 Curve-y19 value of sigma table. Note: No reset value
15:12	RO	0x0	reserved
11:0	RW	0x00b	sw_npu_sigma_y18 Curve-y18 value of sigma table. Note: No reset value

ISP_AI_1200_SIGMA_Y10

Address: Operational Base(0x21D01200) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x00d	sw_npu_sigma_y21 Curve-y21 value of sigma table. Note: No reset value
15:12	RO	0x0	reserved
11:0	RW	0x00b	sw_npu_sigma_y20 Curve-y20 value of sigma table. Note: No reset value

ISP_AI_1200_SIGMA_Y11

Address: Operational Base(0x21D01200) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x00d	sw_npu_sigma_y23 Curve-y23 value of sigma table. Note: No reset value
15:12	RO	0x0	reserved
11:0	RW	0x00b	sw_npu_sigma_y22 Curve-y22 value of sigma table. Note: No reset value

ISP_AI_1200_SIGMA_Y12

Address: Operational Base(0x21D01200) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x00d	sw_npu_sigma_y25 Curve-y25 value of sigma table. Note: No reset value
15:12	RO	0x0	reserved
11:0	RW	0x00b	sw_npu_sigma_y24 Curve-y24 value of sigma table. Note: No reset value

ISP_AI_1200_SIGMA_Y13

Address: Operational Base(0x21D01200) + offset (0x0044)

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Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x00d	sw_npu_sigma_y27 Curve-y27 value of sigma table. Note: No reset value
15:12	RO	0x0	reserved
11:0	RW	0x00b	sw_npu_sigma_y26 Curve-y26 value of sigma table. Note: No reset value

ISP_AI_1200_SIGMA_Y14

Address: Operational Base(0x21D01200) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x00d	sw_npu_sigma_y29 Curve-y29 value of sigma table. Note: No reset value
15:12	RO	0x0	reserved
11:0	RW	0x00b	sw_npu_sigma_y28 Curve-y28 value of sigma table. Note: No reset value

ISP_AI_1200_SIGMA_Y15

Address: Operational Base(0x21D01200) + offset (0x004C)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x00d	sw_npu_sigma_y31 Curve-y31 value of sigma table. Note: No reset value
15:12	RO	0x0	reserved
11:0	RW	0x00b	sw_npu_sigma_y30 Curve-y30 value of sigma table. Note: No reset value

ISP_AI_1200_SIGMA_Y16

Address: Operational Base(0x21D01200) + offset (0x0050)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x00d	sw_npu_sigma_y32 Curve-y32 value of sigma table. Note: No reset value

ISP_AI_1200_AIPRE_NL_WR_BASE

Address: Operational Base(0x21D01200) + offset (0x0054)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_aipre_nl_wr_base Nlinear ddr write base addr.
3:0	RO	0x0	reserved

ISP_AI_1200_AIPRE_NL_WR_STRIDE

Address: Operational Base(0x21D01200) + offset (0x0058)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_aipre_nl_wr_stride Nlinear ddr write stride.
3:0	RO	0x0	reserved

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ISP_AI_1200_AIPRE_GAIN_WR_BASE

Address: Operational Base(0x21D01200) + offset (0x005C)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_aipre_gain_wr_base Gain ddr write base addr.
3:0	RO	0x0	reserved

ISP_AI_1200_AIPRE_GAIN_WR_STRIDE

Address: Operational Base(0x21D01200) + offset (0x0060)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_aipre_gain_wr_stride Gain ddr write stride.
3:0	RO	0x0	reserved

ISP_AI_1200_AIPRE_NL_PRE

Address: Operational Base(0x21D01200) + offset (0x0064)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:20	RW	0x000	sw_aipre_black_lvl AIPRE nlinear calculate black level, real value should mul 16(4bit).{13i}
19:16	RO	0x0	reserved
15:8	RW	0x00	sw_aipre_zp AIPRE nlinear out zp.{1s,7i}
7:0	RW	0x00	sw_aipre_scale AIPRE nlinear out scale.{8i}

ISP_AI_1200_AIPRE_GAIN_PARA

Address: Operational Base(0x21D01200) + offset (0x0068)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:12	RW	0x0000	sw_aipre_gain_ratio AIPRE gain alpha, narmap = ratio/gain_adjust.{15i}
11:4	RW	0x00	sw_aipre_global_gain AIPRE global gain.{8i}
3:0	RW	0x0	sw_aipre_gain_alpha AIPRE global gain alpha.range:[0,8],{4i}.

ISP_AI_1200_AIPRE_SIGMA_CURVE0

Address: Operational Base(0x21D01200) + offset (0x006C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	sw_aipre_sigma_y2 Curve-y2 value of nlinear sigma table.{10i}
19:10	RW	0x000	sw_aipre_sigma_y1 Curve-y1 value of nlinear sigma table.{10i}
9:0	RW	0x000	sw_aipre_sigma_y0 Curve-y0 value of nlinear sigma table.{10i}

ISP_AI_1200_AIPRE_SIGMA_CURVE1

Address: Operational Base(0x21D01200) + offset (0x0070)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	sw_aipre_sigma_y5 Curve-y5 value of nlinear sigma table.{10i}

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Bit	Attr	Reset Value	Description
19:10	RW	0x000	sw_aipre_sigma_y4 Curve-y4 value of nlinear sigma table.{10i}
9:0	RW	0x000	sw_aipre_sigma_y3 Curve-y3 value of nlinear sigma table.{10i}

ISP_AI_1200_AIPRE_SIGMA_CURVE2

Address: Operational Base(0x21D01200) + offset (0x0074)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	sw_aipre_sigma_y8 Curve-y8 value of nlinear sigma table.{10i}
19:10	RW	0x000	sw_aipre_sigma_y7 Curve-y7 value of nlinear sigma table.{10i}
9:0	RW	0x000	sw_aipre_sigma_y6 Curve-y6 value of nlinear sigma table.{10i}

ISP_AI_1200_AIPRE_SIGMA_CURVE3

Address: Operational Base(0x21D01200) + offset (0x0078)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	sw_aipre_sigma_y11 Curve-y11 value of nlinear sigma table.{10i}
19:10	RW	0x000	sw_aipre_sigma_y10 Curve-y10 value of nlinear sigma table.{10i}
9:0	RW	0x000	sw_aipre_sigma_y9 Curve-y9 value of nlinear sigma table.{10i}

ISP_AI_1200_AIPRE_SIGMA_CURVE4

Address: Operational Base(0x21D01200) + offset (0x007C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	sw_aipre_sigma_y14 Curve-y14 value of nlinear sigma table.{10i}
19:10	RW	0x000	sw_aipre_sigma_y13 Curve-y13 value of nlinear sigma table.{10i}
9:0	RW	0x000	sw_aipre_sigma_y12 Curve-y12 value of nlinear sigma table.{10i}

ISP_AI_1200_AIPRE_SIGMA_CURVE5

Address: Operational Base(0x21D01200) + offset (0x0080)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	sw_aipre_sigma_y17 Curve-y17 value of nlinear sigma table.{10i}
19:10	RW	0x000	sw_aipre_sigma_y16 Curve-y16 value of nlinear sigma table.{10i}
9:0	RW	0x000	sw_aipre_sigma_y15 Curve-y15 value of nlinear sigma table.{10i}

ISP_AI_1200_AIPRE_SIGMA_CURVE6

Address: Operational Base(0x21D01200) + offset (0x0084)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	sw_aipre_sigma_y20 Curve-y20 value of nlinear sigma table.{10i}

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Bit	Attr	Reset Value	Description
19:10	RW	0x000	sw_aipre_sigma_y19 Curve-y19 value of nlinear sigma table.{10i}
9:0	RW	0x000	sw_aipre_sigma_y18 Curve-y18 value of nlinear sigma table.{10i}

ISP_AI_1200_AIPRE_SIGMA_CURVE7

Address: Operational Base(0x21D01200) + offset (0x0088)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	sw_aipre_sigma_y23 Curve-y23 value of nlinear sigma table.{10i}
19:10	RW	0x000	sw_aipre_sigma_y22 Curve-y22 value of nlinear sigma table.{10i}
9:0	RW	0x000	sw_aipre_sigma_y21 Curve-y21 value of nlinear sigma table.{10i}

ISP_AI_1200_AIPRE_SIGMA_CURVE8

Address: Operational Base(0x21D01200) + offset (0x008C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	sw_aipre_sigma_y26 Curve-y26 value of nlinear sigma table.{10i}
19:10	RW	0x000	sw_aipre_sigma_y25 Curve-y25 value of nlinear sigma table.{10i}
9:0	RW	0x000	sw_aipre_sigma_y24 Curve-y24 value of nlinear sigma table.{10i}

ISP_AI_1200_AIPRE_SIGMA_CURVE9

Address: Operational Base(0x21D01200) + offset (0x0090)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	sw_aipre_sigma_y29 Curve-y29 value of nlinear sigma table.{10i}
19:10	RW	0x000	sw_aipre_sigma_y28 Curve-y28 value of nlinear sigma table.{10i}
9:0	RW	0x000	sw_aipre_sigma_y27 Curve-y27 value of nlinear sigma table.{10i}

ISP_AI_1200_AIPRE_SIGMA_CURVE10

Address: Operational Base(0x21D01200) + offset (0x0094)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	sw_aipre_sigma_y32 Curve-y32 value of nlinear sigma table.{10i}
19:10	RW	0x000	sw_aipre_sigma_y31 Curve-y31 value of nlinear sigma table.{10i}
9:0	RW	0x000	sw_aipre_sigma_y30 Curve-y30 value of nlinear sigma table.{10i}

ISP_AI_1200_AIPRE_NOISE0

Address: Operational Base(0x21D01200) + offset (0x0098)

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x000	sw_aipre_noise_luma_offset Offset of the luma noise.{10i}

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Bit	Attr	Reset Value	Description
15	RO	0x0	reserved
14:8	RW	0x00	sw_aipre_noise_mot_gain Gain of the noise motion.range:[-64,63],{1s,6i}.
7:0	RW	0x00	sw_aipre_noise_mot_offset Offset of the noise motion.{8i}

ISP_AI_1200_AIPRE_NOISE1

Address: Operational Base(0x21D01200) + offset (0x009C)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_aipre_noise_luma_static Static of luma noise.{8i}
23:22	RO	0x0	reserved
21:12	RW	0x000	sw_aipre_noise_luma_clip Clip of luma noise.{10i}
11	RO	0x0	reserved
10:0	RW	0x000	sw_aipre_noise_luma_gain Gain of the luma noise.range:[0,1024],{11i};

ISP_AI_1200_AIPRE_NOISE2

Address: Operational Base(0x21D01200) + offset (0x00A0)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	reserved
12:8	RW	0x00	sw_aipre_nar_manual_alpha Global alpha.range:[0,16],{5i}.
7:0	RW	0x00	sw_aipre_nar_manual Global narmap.{8i}

44.4.2.38 RGBIR

RGBIR_EN

Address: Operational Base(0x21D02E00) + offset (0x0000)

Bit	Attr	Reset Value	Description
31	RO	0x0	sw_rgbir_en_shd 1'b1: Rgbir enable. 1'b0: Rgbir disable. Note: Shadow register of sw_rgbir_en.
30	RO	0x0	ro_rgbir_working 1'b1: The Rgbir is working. 1'b0: The Rgbir is not working.
29	RW	0x0	sw_read_fifo_err 1'b1: The Rgbir reads empty FIFO . 1'b0: The Rgbir do not have read empty FIFO error.
28:1	RO	0x0000000	reserved
0	RW	0x0	sw_rgbir_en 1'b1: Rgbir enable. 1'b0: Rgbir disable.

RGBIR_THETA

Address: Operational Base(0x21D02E00) + offset (0x0004)

Bit	Attr	Reset Value	Description
31:12	RO	0x00000	reserved
11:0	RW	0x000	sw_rgbir_coe_theta The value ranges from 0 to 4095. Value stands for dark electricity offset.

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RGBIR_DELTA

Address: Operational Base(0x21D02E00) + offset (0x0008)

Bit	Attr	Reset Value	Description
31:14	RO	0x00000	reserved
13:0	RW	0x0004	sw_rgbir_coe_delta Value stands for directionality weights in the Red interpolation. Note: The value ranges from 1 to 16383. Value cannot be 0.

RGBIR_SCALE0

Address: Operational Base(0x21D02E00) + offset (0x000C)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x07b	sw_rgbir_scale_0 The value ranges from 1 to 256. Value stands for scale coefficient of channel 0.

RGBIR_SCALE1

Address: Operational Base(0x21D02E00) + offset (0x0010)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x073	sw_rgbir_scale_1 The value ranges from 1 to 256. Value stands for scale coefficient of channel 1.

RGBIR_SCALE2

Address: Operational Base(0x21D02E00) + offset (0x0014)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x072	sw_rgbir_scale_2 The value ranges from 1 to 256. Value stands for scale coefficient of channel 2.

RGBIR_SCALE3

Address: Operational Base(0x21D02E00) + offset (0x0018)

Bit	Attr	Reset Value	Description
31:9	RO	0x000000	reserved
8:0	RW	0x079	sw_rgbir_scale_3 The value ranges from 1 to 256. Value stands for scale coefficient of channel 3.

RGBIR_LUMA_POINT0

Address: Operational Base(0x21D02E00) + offset (0x001C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x330	sw_rgbir_luma_point_2 Value stands for the x position of the point 2 in the curve. Note: The value ranges from 0 to 1023. Value is 2 or 4 or 8 or 16 or 32 or 64 or 128 or 256 smaller than sw_rgbir_luma_point_3.
19:10	RW	0x328	sw_rgbir_luma_point_1 Value stands for the x position of the point 1 in the curve. Note: The value ranges from 0 to 1023. Value is 2 or 4 or 8 or 16 or 32 or 64 or 128 or 256 smaller than sw_rgbir_luma_point_2.

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Bit	Attr	Reset Value	Description
9:0	RW	0x320	sw_rgbir_luma_point_0 Value stands for the x position of the point 0 in the curve. Note: The value ranges from 0 to 1023. Value is 2 or 4 or 8 or 16 or 32 or 64 or 128 or 256 smaller than sw_rgbir_luma_point_1.

RGBIR_LUMA_POINT1

Address: Operational Base(0x21D02E00) + offset (0x0020)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x348	sw_rgbir_luma_point_5 Value stands for the x position of the point 5 in the curve. Note: The value ranges from 0 to 1023. Value is 2 or 4 or 8 or 16 or 32 or 64 or 128 or 256 smaller than sw_rgbir_luma_point_6.
19:10	RW	0x340	sw_rgbir_luma_point_4 Value stands for the x position of the point 4 in the curve. Note: The value ranges from 0 to 1023. Value is 2 or 4 or 8 or 16 or 32 or 64 or 128 or 256 smaller than sw_rgbir_luma_point_5.
9:0	RW	0x338	sw_rgbir_luma_point_3 Value stands for the x position of the point 3 in the curve. Note: The value ranges from 0 to 1023. Value is 2 or 4 or 8 or 16 or 32 or 64 or 128 or 256 smaller than sw_rgbir_luma_point_4.

RGBIR_LUMA_POINT2

Address: Operational Base(0x21D02E00) + offset (0x0024)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x390	sw_rgbir_luma_point_8 Value stands for the x position of the point 8 in the curve. Note: The value ranges from 0 to 1023. Value is 2 or 4 or 8 or 16 or 32 or 64 or 128 or 256 smaller than sw_rgbir_luma_point_9.
19:10	RW	0x370	sw_rgbir_luma_point_7 Value stands for the x position of the point 7 in the curve. Note: The value ranges from 0 to 1023. Value is 2 or 4 or 8 or 16 or 32 or 64 or 128 or 256 smaller than sw_rgbir_luma_point_8.
9:0	RW	0x350	sw_rgbir_luma_point_6 Value stands for the x position of the point 6 in the curve. Note: The value ranges from 0 to 1023. Value is 2 or 4 or 8 or 16 or 32 or 64 or 128 or 256 smaller than sw_rgbir_luma_point_7.

RGBIR_LUMA_POINT3

Address: Operational Base(0x21D02E00) + offset (0x0028)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x3d8	sw_rgbir_luma_point_11 Value stands for the x position of the point 11 in the curve. Note: The value ranges from 0 to 1023. Value is 2 or 4 or 8 or 16 or 32 or 64 or 128 or 256 smaller than sw_rgbir_luma_point_12.
19:10	RW	0x3d0	sw_rgbir_luma_point_10 Value stands for the x position of the point 10 in the curve. Note: The value ranges from 0 to 1023. Value is 2 or 4 or 8 or 16 or 32 or 64 or 128 or 256 smaller than sw_rgbir_luma_point_11.
9:0	RW	0x3b0	sw_rgbir_luma_point_9 Value stands for the x position of the point 9 in the curve. Note: The value ranges from 0 to 1023. Value is 2 or 4 or 8 or 16 or 32 or 64 or 128 or 256 smaller than sw_rgbir_luma_point_10.

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RGBIR_LUMA_POINT4

Address: Operational Base(0x21D02E00) + offset (0x002C)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x3f0	sw_rgbir_luma_point_14 Value stands for the x position of the point 14 in the curve. Note: The value ranges from 0 to 1023. Value is 2 or 4 or 8 or 16 or 32 or 64 or 128 or 256 smaller than sw_rgbir_luma_point_15.
19:10	RW	0x3e8	sw_rgbir_luma_point_13 Value stands for the x position of the point 13 in the curve. Note: The value ranges from 0 to 1023. Value is 2 or 4 or 8 or 16 or 32 or 64 or 128 or 256 smaller than sw_rgbir_luma_point_14.
9:0	RW	0x3e0	sw_rgbir_luma_point_12 Value stands for the x position of the point 12 in the curve. Note: The value ranges from 0 to 1023. Value is 2 or 4 or 8 or 16 or 32 or 64 or 128 or 256 smaller than sw_rgbir_luma_point_13.

RGBIR_LUMA_POINT5

Address: Operational Base(0x21D02E00) + offset (0x0030)

Bit	Attr	Reset Value	Description
31:21	RO	0x000	reserved
20:10	RW	0x400	sw_rgbir_luma_point_16 Value stands for the x position of the point 16 in the curve. Note: The value ranges from 0 to 1024. Value is 2 or 4 or 8 or 16 or 32 or 64 or 128 or 256 larger than sw_rgbir_luma_point_15.
9:0	RW	0x3f8	sw_rgbir_luma_point_15 Value stands for the x position of the point 15 in the curve. Note: The value ranges from 0 to 1023. Value is 2 or 4 or 8 or 16 or 32 or 64 or 128 or 256 smaller than sw_rgbir_luma_point_16.

RGBIR_SCALE_MAP0

Address: Operational Base(0x21D02E00) + offset (0x0034)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:18	RW	0x0f5	sw_rgbir_scale_map_2 Value stands for the y position of the point 2 in the curve. Note: The value ranges from 0 to 256. Value is larger than or equal to sw_rgbir_scale_map_3.
17:9	RW	0x0fd	sw_rgbir_scale_map_1 Value stands for the y position of the point 1 in the curve. Note: The value ranges from 0 to 256. Value is larger than or equal to sw_rgbir_scale_map_2.
8:0	RW	0x100	sw_rgbir_scale_map_0 Value stands for the y position of the point 0 in the curve. Note: The value ranges from 0 to 256. Value is larger than or equal to sw_rgbir_scale_map_1.

RGBIR_SCALE_MAP1

Address: Operational Base(0x21D02E00) + offset (0x0038)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:18	RW	0x0c3	sw_rgbir_scale_map_5 Value stands for the y position of the point 5 in the curve. Note: The value ranges from 0 to 256. Value is larger than or equal to sw_rgbir_scale_map_6.

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Bit	Attr	Reset Value	Description
17:9	RW	0x0d7	sw_rgbir_scale_map_4 Value stands for the y position of the point 4 in the curve. Note: The value ranges from 0 to 256. Value is larger than or equal to sw_rgbir_scale_map_5.
8:0	RW	0x0e8	sw_rgbir_scale_map_3 Value stands for the y position of the point 3 in the curve. Note: The value ranges from 0 to 256. Value is larger than or equal to sw_rgbir_scale_map_4.

RGBIR_SCALE_MAP2

Address: Operational Base(0x21D02E00) + offset (0x003C)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:18	RW	0x01f	sw_rgbir_scale_map_8 Value stands for the y position of the point 8 in the curve. Note: The value ranges from 0 to 256. Value is larger than or equal to sw_rgbir_scale_map_9.
17:9	RW	0x057	sw_rgbir_scale_map_7 Value stands for the y position of the point 7 in the curve. Note: The value ranges from 0 to 256. Value is larger than or equal to sw_rgbir_scale_map_8.
8:0	RW	0x0ad	sw_rgbir_scale_map_6 Value stands for the y position of the point 6 in the curve. Note: The value ranges from 0 to 256. Value is larger than or equal to sw_rgbir_scale_map_7.

RGBIR_SCALE_MAP3

Address: Operational Base(0x21D02E00) + offset (0x0040)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:18	RW	0x001	sw_rgbir_scale_map_11 Value stands for the y position of the point 11 in the curve. Note: The value ranges from 0 to 256. Value is larger than or equal to sw_rgbir_scale_map_12.
17:9	RW	0x001	sw_rgbir_scale_map_10 Value stands for the y position of the point 10 in the curve. Note: The value ranges from 0 to 256. Value is larger than or equal to sw_rgbir_scale_map_11.
8:0	RW	0x008	sw_rgbir_scale_map_9 Value stands for the y position of the point 9 in the curve. Note: The value ranges from 0 to 256. Value is larger than or equal to sw_rgbir_scale_map_10.

RGBIR_SCALE_MAP4

Address: Operational Base(0x21D02E00) + offset (0x0044)

Bit	Attr	Reset Value	Description
31:27	RO	0x00	reserved
26:18	RW	0x000	sw_rgbir_scale_map_14 Value stands for the y position of the point 14 in the curve. Note: The value ranges from 0 to 256. Value is larger than or equal tosw_rgbir_scale_map_15.
17:9	RW	0x000	sw_rgbir_scale_map_13 Value stands for the y position of the point 13 in the curve. Note: The value ranges from 0 to 256. Value is larger than or equal tosw_rgbir_scale_map_14.

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Bit	Attr	Reset Value	Description
8:0	RW	0x001	sw_rgbir_scale_map_12 Value stands for the y position of the point 12 in the curve. Note: The value ranges from 0 to 256. Value is larger than or equal to sw_rgbir_scale_map_13.

RGBIR_SCALE_MAP5

Address: Operational Base(0x21D02E00) + offset (0x0048)

Bit	Attr	Reset Value	Description
31:18	RO	0x0000	reserved
17:9	RW	0x000	sw_rgbir_scale_map_16 Value stands for the y position of the point 16 in the curve. Note: The value ranges from 0 to 256. Value is smaller than or equal to sw_rgbir_scale_map_15.
8:0	RW	0x000	sw_rgbir_scale_map_15 Value stands for the y position of the point 15 in the curve. Note: The value ranges from 0 to 256. Value is larger than or equal to sw_rgbir_scale_map_16.

44.5 Interface Description

Table 44-3 ISP Interface Description

Module Pin	Dir	Pad Name	IOMUX Setting
flash_trig	O	SPI1_MOSI_M1/SAI2_SDO_M0/PWM2_CH0_M0/FLASH_TRIG_OUT/GPIO3_B2	GPIO3B_IOMUX_SEL_0 [11:8] = 4'h6
prelight_trig	O	SPI1_MISO_M1/SAI2_SDI0_M0/PWM2_CH1_M0/PRELIGHT_TRIG_OUT/GPIO3_B3	GPIO3B_IOMUX_SEL_0 [15:12] = 4'h6

Notes: I=input, O=output, I/O=input/output, bidirectional

44.6 Application Notes

44.6.1 VICAP Interface

ISP support VICAP direct path into ISP process, including HDR/no-HDR on the fly mode. If this mode is no used, it is **strongly recommended** to configure sw_toisp0_en_ch0, sw_toisp0_en_ch1, sw_toisp0_en_ch2 (VICAP_BASE address offset 0x0780[0], [8], [16]) to 0.

44.6.1.1 normal mode (Single ID)

For this mode:
Configure sw_ibuf_op_mode = 0.
All DMATX are available, but all DMARX are unavailable.
For example: raw10, lanex4
CTRL0 = 0x0. (If sensor AR0239, CTRL0 = 0x4; If sensor IMX327, CTRL0 = 0x8)
CTRL1 = 0x3.
DATA_IDS_1 = 0x2b.

44.6.1.2 frame_x2_ddr mode (2IDs--HDR mode)

For this mode:
Configure sw_ibuf_op_mode = 8.
For example: raw10, lanex4
CTRL0 = 0x800.
CTRL1 = 0x3.
DATA_IDS_1 = 0x6b2b.
Configure ISP MI register for address and size:
RAW0_WR_BASE = “DMATX0 base address in DDR”.
RAW0_WR_SIZE = “pic_width * pic_height * 1.5”.

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44.6.1.3 line_x2_ddr_mode (2IDs--HDR mode)

For this mode:
Configure sw_ibuf_op_mode = 9.
For example: raw10, lanex4
CTRL0 = 0x900.
CTRL1 = 0x3.
DATA_IDS_1 = 0x6b2b.
Configure ISP_MI register for address and size:
RAW0_WR_BASE = "DMATX0 base address in DDR".
RAW0_WR_SIZE = "pic_width * pic_height * 1.5".

44.6.1.4 line_x2_noddr mode (2IDs--HDR mode)

For this mode:
Configure sw_ibuf_op_mode = 10.
For example: raw10, lanex4
CTRL0 = 0xa00.
CTRL1 = 0x3.
DATA_IDS_1 = 0x6b2b.

44.6.1.5 user mode

For this mode:
Configure sw_ibuf_op_mode = 3.
User defined mode. All DMATX and DMARX are available.

44.6.1.6 raw_rdback_framex1 mode

For this mode:
Configure sw_ibuf_op_mode = 4.
For example: raw10, lanex4 (all DMATX configurable, recommend DMATX2)
CTRL0 = 0x400.
CTRL1 = 0x3.
DATA_IDS_1 = 0x2b.
RAW2_WR_CTRL = 0x101.
Configure ISP_MI register for address and size:
MI_WR_CTRL2 = 0x1.
RAW2_WR_BASE = "DMATX2 base address in DDR".
RAW2_WR_SIZE = "pic_width * pic_height*1.5".
RAWS_RD_BASE = RAW2_WR_BASE.
Then, the time to start DMARXS is up to the user (maybe DMATX2 frame end):
Configure CTRL0 = 0x401.

44.6.1.7 raw_rdback_framex2 mode (HDR mode)

For this mode:
Configure sw_ibuf_op_mode = 5.
For example: raw10, lanex4 (all DMATX configurable, recommend DMATX2 and DMATX0)
CTRL0 = 0x500.
CTRL1 = 0x103.
DATA_IDS_1 = 0x6b2b.
RAW2_WR_CTRL = 0x101.
RAW0_WR_CTRL = 0x201.
Configure ISP_MI register for address and size:
MI_WR_CTRL2 = 0x3.
RAW2_WR_BASE = "DMATX2 base address in DDR".
RAW2_WR_SIZE = "pic_width * pic_height * 1.5".
RAW0_WR_BASE = "DMATX0 base address in DDR".
RAW0_WR_SIZE = "pic_width * pic_height * 1.5".
RAWS_RD_BASE = RAW2_WR_BASE.
RAW0_RD_BASE = RAW0_WR_BASE.
Then, the time to start DMARXS is up to the user (maybe both DMATX2 and DMATX20 frame end):
Configure CTRL0 = 0x501.

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44.6.1.8 VICAP semi-on-the-fly

VICAP divides a frame into two parts, with the left image to ISP on-the-fly (online) and the right image to DDR (offline). After the left image processing done, ISP read the right image from DDR, and finally the left and right images are joint together.
For VICAP,
1) MIPIx_IDx_CROP_START is configured to the begin of the offline image.
2) MIPIx_IDx_SET_SIZE is configured to the size of the offline image.
3) TOISP0_CHx_CROP_START is configured to the begin of the online image.
4) TOISP0_CHx_CROP_SIZE is configured to the size of the online image.

44.6.1.9 VICAP HDR wrap

When VICAP2ISP on-the-fly in HDR mode, the short-exposure frame is on-the-fly to ISP, and the long-exposure frame is to DDR, and will be read by ISP later, which means there is a full frame buffer in DDR in normal. For HDR wrap mode, the frame buffer size can less than one frame (for example, 1/2 or 1/4). There are two HDR wrap mode:
1) mode0, wrap clear, the address of next frame data start from the begin of frame buffer.
2) mode1, wrap continue, the address of next frame start at the end of last frame.

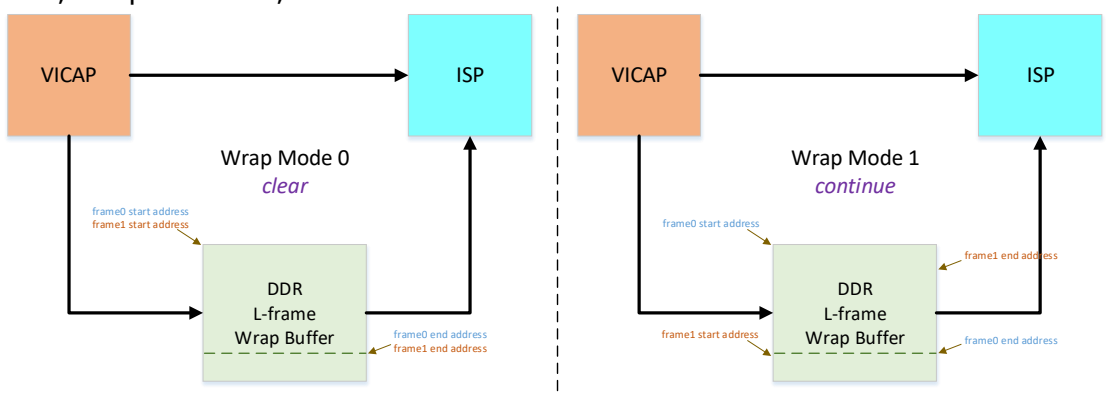

Figure 44-2 VICAP HDR Warp Mode

For VICAP HDR wrap mode, there are some additional configurations:
1) Configure VICAP wrap mode (VICAP address offset 0x0100), 2 means mode0, 3 means mode1.
2) Configure VICAP long-exposure frame write stride (VICAP address offset 0x0134[19:0]), be care of compact write or not.
3) Configure VICAP wrap line num (VICAP address offset 0x0134[30:20]).
4) Configure ISP wrap mode (address offset 0x18a0), 1 means mode1, otherwise mode0.
5) Configure ISP long-exposure frame read stride (address offset 0x1874), should the same as VICAP write stride.
6) Configure ISP wrap buffer size (address offset 0x187c) = stride * line_num.

44.6.2 MI

Three are 4 points to note:
1) The signal sw_mi_wr_init_offset_en (address offset 0x1400[21]) in MI_WR_CTRL register needs to be set to 1, otherwise, the address of MI will not be updated.
2) If output address need ping-pong, the signal sw_mp_wr_auto_upd (address offset 0x1400[13]) in MI_WR_CTRL register needs to be set to 1.
3) The signal sys_mi_cfg_upd (address offset 0x1404[4]) in MI_WR_INIT register needs to be set to 1 after all MI registers configuration complete when the 1st frame.
4) The respective force update (sys_dbrself_force_upd, sys_gainself_force_upd, sys_bay3dself_force_upd) is added to the register MI_WR_CTRL2 (address offset 0x1800), can be used to update the enable signal and shadow address.

44.6.3 HDRMGE

1) global register configuration:
   Enable and select mode, choose gain or Anti-gain, other configurations such as curves is recommended to use the default typical value.
2) Curve configuration:
   L curve: The first quarter is divided into 16 sections, other is equal to 1023.

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S curve: Middle 1/2 divided into 16 sections, other is equal to 1023.
E curve: Last 1/2 divided into 16 segments, other is equal to 0.

3) Software configuration:
sw_hdr_mode: 0: normal; 1: framex2.
sw_hdr_lightz = 0.1 * (short_gain / 16) ^ 3).
sw_hdr_gain2 = 1.
sw_hdr_gain1 = exposure_L / exposure_M; (Anti-gain1 is 1/gain1).
sw_hdr_gain0 = exposure_L / exposure_S; (Anti-gain0 is 1/gain0).
sw_hdr_lightzone = 0.1 * (short_gain / 16) ^ 3.
light_zone = img_short > sw_hdr_lightzone = 0.1 * (short_gain / 16) ^ 3.

44.6.4 BAY3D

1) The address offset of BAY3D module is 0x2b00~0x2dfc. There are spatial filtering of current frame and IIR frame and temporal motion compensation inside BAY3D module, and the effect can be modified by register configuration.
2) When BAY3D is enabled, sys_raw3d_fst_frame (address offset 0x0404[27]) must be configured to 1 in first frame, which will be auto cleared. The output of BAY3D in first frame is the result of spatial filtering of current frame.
3) Configured hw_btnr_tnrModule_bypass_en (address offset 0x2b00[1]) to 1 to enable BAY3D bypass mode, and pre frame still write data to DDR in this mode. There has some precision loss between input and output data in this mode because there has log operation and anti-log operation when hw_btnr_transf_bypass_en is 0.
4) BAY3D transforms the input 20bit data into 12bit data through a transform curve, and does data processing on 12bit to save hardware resources and bandwidth. To disable BAY3D, developer should configure hw_btnr_tnrModule_en to 0 and hw_btnr_transf_bypass_en to 1.
5) hw_btnr_outUsePre_mode is different mode of temporal reduction, see 错误!未找到引用源。 in detail.
6) The configuration of sigma curve of spatial and temporal filtering is determined by tuning, and the coordinate configuration should meet the constraint that the spacing between adjacent coordinate is 2^n.
7) The current spatial filtering coefficients are hw_btnr_curSpnrFilter_coeff0~ hw_btnr_curSpnrFilter_coeff5, which should meet the constraint that their weighted sum should be 256. The high frequency temporal filtering coefficients are hw_btnr_LpfHi_coeff0~hw_btnr_LpfHi_coeff8, which should meet the constraint that their weighted sum should be 1024. The low frequency temporal filtering coefficients are hw_btnr_LpfLo_coeff0~hw_btnr_LpfLo_coeff8, which should meet the constraint that their weighted sum should be 1024.
8) The use of sw_bay3d_iir_rw_fmt is shown as below, here w16 is pic_width aligned to 16pixel, and the same goes for w32 and w128.

sw_bay3d_iir_rw_fmt	data arrange	h_size for MI	virtual stride (unit in byte)	v_size for MI	wr_size	data width	comment
0	12bit pixdel data compacted mix 2 pk data with 8 pixel data in odd line	w16*7/4	0	h/2	(w16*7/8*h*2+15)/16*16	hdr/predgain/expd/nohdr	
1	12bit uncompat 16bit with {4bit pk data, 12bit pixel data}	w16	0	h	w16*h	nohdr only	linear input; predgain = 0; hw_btnr_transf_bypass_en = 1
2	16bit, one line pixel data, follow with half line pk data	w16+w16/8	((w16+w16/8)*2+15)/16*16	h	(vir_stirde*h+15)/16*16	hdr/predgain/expd/nohdr	data arrange for AIISP
3	16bit high precision mode one line pixel data, follow with half line pk data LDC write IIR data, MI_IIR write pk data	pk: w16/8 iir+pk: w32+w16/8	((w32+w128/8)*2+15)/16*16	h	rd: (vir_stride*h+15)/16*16	hdr/predgain/expd/nohdr	

9) BAY3D_IIR_WR_BASE (address offset 0x19a0) is the write address base of PRE (IIR) frame, and BAY3D_IIR_RD_BASE (address offset 0x19b0) is the read address base. The force update signal of BAY3D PRE write is sys_bay3d_iirself_force_upd (address offset 0x1800[22]) and the force update signal of BAY3D PRE read is sys_rxb3d_force_upd (address offset 0x1800[7]).
10) BAY3D_IIR_WR_SIZE (address offset 0x19a4) is the write size of bay3d MI PRE, which unit by byte and should by 16byte aligned. The calculation is BAY3D_IIR_WR_SIZE = (((MI_PRE_hsize * MI_PRE_vsize * 2Byte) + 15) >> 4) << 4), and the calculation of MI_PRE_xsize is show as below, here hsize16align = (((hsize + 15) >> 4) << 4),

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hsize32align = (((hsize + 31) >> 5) << 5), hsize128align = (((hsize + 127) >> 7) << 7), and the unit is pixel.

sw_bay3d_iir_rw_fmt	MI_PRE_xsize
0	MI_PRE_hsize = hsize16align * 2 * 3 / 4 + (hsize16align >> 2) (unit pixel) MI_PRE_vsize = vsize / 2 (unit pixel) STRIDE = 0 (unit byte)
1	MI_PRE_hsize = hsize16align (unit pixel) MI_PRE_vsize = vsize (unit pixel) STRIDE = 0 (unit byte)
2	MI_PRE_hsize = hsize16align + hsize16align / 8 (unit pixel) MI_PRE_vsize = vsize (unit pixel) STRIDE = (MI_PRE_hsize * 2 + 15) / 16 * 16 (unit byte)
3	MI_PRE_hsize = hsize32align + hsize128align / 8 (unit pixel) MI_PRE_vsize = vsize (unit pixel) STRIDE = (MI_PRE_hsize * 2 + 15) /16 * 16 (unit byte)

11) BAY3D_DS_WR_BASE (address offset 0x19e0) is the write address base of downscale data, and BAY3D_DS_RD_BASE (address offset 0x19f0) is the read address base. The force update signal of BAY3D DS write is sys_bay3d_dsself_force_upd (address offset 0x1800[24]) and the force update signal of BAY3D DS read is sys_rxb3d_force_upd (address offset 0x1800[7]).
12) BAY3D_DS_WR_SIZE (address offset 0x19e4) is the write size of bay3d MI DS, which unit by byte and should by 16byte aligned. The calculation is BAY3D_DS_WR_SIZE = (((ds_hsize * ds_vsize) + 15) >> 4) << 4), here ds_hsize = (hsize16align / 8 * 36 + 31) / 32 * 4, ds_vsize = (vsize + 7) / 8.
13) BAY3D_CUR_WR_BASE (address offset 0x19c0) is the write address base of weight data (WGT) of current frame, and BAY3D_CUR_RD_BASE (address offset 0x19d0) is the read address base. The force update signal of BAY3D WGT write is sys_bay3d_curself_force_upd (address offset 0x1800[23]) and the force update signal of BAY3D WGT read is sys_rxb3d_force_upd (address offset 0x1800[7]).
14) BAY3D_WGT_WR_SIZE (address offset 0x19c4) is the write size of bay3d MI WGT, which unit by byte and should by 16byte aligned. The calculation is BAY3D_CUR_WR_SIZE = ((wgt_hsize * wgt_vsize + 15) >> 4) << 4, here wgt_hsize = (((hsize + 31) / 32 + 1) / 2 * 2 + 3) / 4 * 4, wgt_vsize = (vsize + 31) / 32.
15) When sw_b3dldc_en (address offset 0x3b80[0]) is configured to 1, B3DLDC is enabled, and sw_bay3d_iir_rw_fmt should be configured to 3 at this time. B3DLDC_WR_BASE (address offset 0x3ba8) is the DDR wirte address base of B3DLDC, and B3DLDC_WR_STIRDE (address offset 0x3bac) is the write stride of B3DLDC, where stride = (MI_PRE_hsize*2 + 15)/16*16. B3DLDC will read LUT data from DDR in each frame, here address offset 0x1a00 is the read address base of B3DLDCH LUT, address offset 0x1a08 is the read hsize of B3DLDCH LUT, address offset 0x1a0c is the read vsize of B3DLDCH LUT, address offset 0x1a30 is the read address base of B3DLDCV LUT, address offset 0x1a38 is the read hsize of B3DLDCV LUT, address offset 0x1a3c is the read vsize of B3DLDCV LUT. Here, b3dldch_hsize = ceil((hsize16align / 16 + 1) / 2), b3dldch_vsize = vsize8align / 8 + 1, b3dldcv_hsize = ceil((hsize16align / 16 + 1) / 2), b3dldcv_vsize = vsize16align / 16 + 2. When B3DLDC is enabled, write address base need pingpong.
16) When sw_aipre_iir_en (address offset 0x1200[8]) and sw_aipre_gain_en (address offset 0x1200[10]) is configured to 1, AIPRE is enabled, and sw_bay3d_iir_rw_fmt should be configured to 2 at this time.
17) The MI configuration and enable configuration of BAY3D should be configured before the force update signal of MI configured to 1.

44.6.5 HDR-DRC

HDR-DRC global register configuration:
Enabling and select mode, lgscl and lgscl_inv, other configurations such as curves is recommended to use the default typical value.

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44.6.6 DEBAYER

The DEBAYER module has 3 important register configurations:

1) hw_dmT_en: When it is configured to 0 or hw_dmT_byapss is configured to 1, it corresponds to black and white mode, otherwise, RGB mode.
2) hw_dmT_gOutlsFlt_en: When it is configured to 0, G filter module will be bypassed.
3) hw_dmT_gInterpClip_en: Determine whether the horizontal and vertical interpolation result will clip according to the maximum value in the window when G interpolation.
4) The rest of the configuration is to adjust the algorithm effect. The following points need to be noted:
   - hw_dmT_loDrctFlt_coeff is a signed number, and it should meet constraints that coe1 + coe2 = 0, coe3 + coe4 = 0, 2 * coe1 + coe3 = ±8
   - hw_dmT_hiDrctFlt_coeff is a signed number, and it should meet constraints that 2 * coe1 + coe2 = 0, 2 * coe3 + coe4 = 0, 2 * coe2 + coe4 = ±8

coe1	0	coe2
coe3	0	coe4
coe1	0	coe2

loDrctFlt

coe1	coe2	coe1
coe3	coe4	coe3
coe1	coe2	coe1

hiDrctFlt

Figure 44-3 DEBAYER Filter Coefficient Arrangement

   - The step of hw_dmT_gInterpSharpStrg_maxLimit is 1/4, the step of hw_dmT_hiTexture_thred is 1/8, the step of hw_dmT_hiDrct_thred and hw_dmT_loDrct_thred is 1/32.
   - hw_dmT_gOutlsFlt_coeff0 + 4 * hw_dmT_gOutlsFlt_coeff1 + 4 * hw_dmT_gOutlsFlt_coeff2 = 128
   - (1 << hw_dmT_luma_val1) + (1 << hw_dmT_luma_val2) + (1 << hw_dmT_luma_val3) + (1 << hw_dmT_luma_val4) + (1 << hw_dmT_luma_val5) + (1 << hw_dmT_luma_val6) + (1 << hw_dmT_luma_val7) = 4096
   - hw_dmT_cnrLoGuideLpf_coeff0 +4 * hw_dmT_cnrLoGuideLpf_coeff1 + 4 * hw_dmT_cnrLoGuideLpf_coeff2 = 256
   - hw_dmT_cnrPreFlt_coeff0 + 4 * hw_dmT_cnrPreFlt_coeff1 + 4 * hw_dmT_cnrPreFlt_coeff2 = 256
   - hw_dmT_cnrAlphaLpf_coeff0 + 4 * hw_dmT_cnrAlphaLpf_coeff1 + 4 * hw_dmT_cnrAlphaLpf_coeff2 = 256
   - when the MSB of hw_dmT_cnrLoFltStrg_shift is 0, means right shift, while 1 means left shift, and the rest bit means bit number of shift.

44.6.7 CCM

1) Set sw_ccm_en_i to 1, open CCM module, otherwise, CCM module will be close, and data path will be bypassed.
2) Signals sw_ccm_coeff0_r~sw_ccm_coeff2_b are CCM 3x3 matrix parameters. These nine parameters are all 11bit signed numbers which have 7bit integer. The range is [-8,7.992].
3) Signals sw_ccm_offset_r, sw_ccm_offset_g, and sw_ccm_offset_b are offsets in calculation, which are 12bit signed integers.
4) Signals sw_ccm_coeff0_y~sw_ccm_coeff2_y are RGB2Y parameters, which are 11bit signed number with 7bit integer, range from -2 to 1.992.
5) The brightness interpolation curve in CCM mode supports symmetric and asymmetric modes:
   When sw_ccm_asym_adj_en is configured to 0, CCM module uses symmetric interpolation mode, sw_ccm_alp_y0~sw_ccm_alp_y16 are the 17 vertices of the 16 segments of alpha interpolation curve, and sw_ccm_bound_bit is the alpha power exponent configuration of inflexion of interpolation curve. The value of the inflection point is 2^sw_ccm_bound_bit, sw_ccm_bound_bit is ranged from 4 to 10.
   When sw_ccm_asym_adj_en is configured to 1, CCM module uses asymmetric interpolation mode, sw_ccm_alp_y0~sw_ccm_alp_y8 are the 9 vertices of the 8

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segments of the left alpha interpolation curve, sw_ccm_alp_y9~sw_ccm_alp_y17 are the 9 vertices of the 8 segments of the right alpha interpolation curve, and sw_ccm_right_bit is the alpha power exponent configuration of the right inflexion of interpolation curve. The value of the inflection point is 2^sw_ccm_right_bit, sw_ccm_right_bit is ranged from 3 to 11.

44.6.8 GAMMA_OUT

1) The GAMMA_OUT module is enabled when sw_gamma_out_en is configured to 1. This module is realized by interpolation.
2) When sw_gamma_out_equ is configured to 1, the segment length of x orientation is equal and the curve uses 32 segments to interpolate.
3) When sw_gamma_out_equ is asserted to 0, the segment length of x orientation is not equal and the curve uses 44 segments to interpolate.

44.6.9 HSV

1) Configure sw_hsv_en to 1 to enable HSV module.
2) There are 2 mode of HSV LUT, when sw_hsv_2dlut12_cfg_en is set to 1, HSV use 3 2DLUT, when set to 0, HSV use 2 1DLUT, 1 2DLUT.
3) When sw_hsv_2dlut12_cfg_en is set to 1, sw_1dlut0_en and sw_1dlut1_en should be set to 0. When sw_hsv_2dlut12_cfg_en is set to 0, sw_2dlut1_en and sw_2dlut2_en should be set to 1.
4) For LUT load by AHB when sw_hsv_2dlut12_cfg_en is set to 1, 2DLUT0 should be loaded first and then 2DLUT1, and then 2DLUT2. the LUT address offset of 2DLUT0 is 0x3e10, and 2DLUT1 is 0x3e14, 2DLUT2 is 0x3e18.
5) For LUT load by AHB when sw_hsv_2dlut12_cfg_en is set to 0, 2DLUT0 should be loaded first and then 1DLUT0, and then 2DLUT1. Configure address offset 0x3e10 to load 2DLUT0, then configured address offset 0x3e0c to load two 1DLUT.
6) For 1DLUT load by AHB, write two LUT value once time, like {1DLUT0[1], 1DLUT[0]}.
7) For LUT load by AHB, sw_hsv_fix_rw_conflict (address offset 0x3e00[8]) should be set to 1 before LUT load, and should be set to 0 after LUT load.

44.6.10 ENHANCE

1) Configure sw_enh_en to 1 to enable ENHANCE module.
2) When sw_enh_bypass is configured to 1, ENHANCE is bypassed.
3) When sw_enh_blf3_bypass is configured to 1, the 3*3 bilateral filtering in ENHANCE is disabled.
4) Configured sw_enh_het_aliquant to the result of pic_height % 3, which can be 0, 1, 2.
5) Configure sw_enh_scl_het to the result of (pic_height + 128) / 129, which means rounding.
6) The 128x129 down-sample result (enh_iir_mem) in ENHANCE can be read/write in address offset 0x3a80~0x3aa4, each register store 32bit data which joint by 4 down-sample data in 8bit. Configure address offset 0x3aa8 to read/write enh_iir_mem.
7) For enh_iir_mem read, configure sw_enh_iir_rd_row[6:0] and sys_enh_iir_rd_p, after ro_iir_rdata_val is 1 (0 means data no ready when read), sw_enh_iir0~sw_enh_iir9 will show the down-sample data of the specific row. Then configure next sw_enh_iir_rd_row and sys_enh_iir_rd_p.
8) For enh_iir_mem write, configure sys_enh_iir_wr_clear and sw_enh_iir_wr_row[5:0], then write register sw_enh_iir0~sw_enh_iir9 of the specific row. Then configure next sw_enh_iir_wr_row and sw_enh_iir0~sw_enh_iir9. Here sys_enh_iir_wr_clear can be configured 1time at first write. If data write interrupt in midway, sys_enh_iir_wr_clear shold be configured to restart data write.
9) The number of down-sample data depend on the image size. For example, when the input image size is 4096x3072, the number of down-sample data in horizon is ceil(4096 / 128) = 32, each data size is 8bit, which can be joint into 8 data in 32bit, from sw_enh_iir0~sw_enh_iir7. The number of down-sample data in vertical is ceil(3072 / 129) = 24, and so on.

44.6.11 YUVHIST

1) The configuration sw_hist_blk_wid and sw_hist_blk_het (address offset 0x3c08) is the width and height of HIST down-sample block, which must be even. The range is,

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sw_hist_blk_wid: [70, 684], where 684 = 4096 / 6, and sw_hist_blk_het: [64, 512], where 512 = 3072 / 6.

2) The configuration sw_hist_thumb_col and sw_hist_thumb_row (address offset 0x3c0c) is the number of HIST down-sample block of horizontal and vertical direction. The range is, sw_hist_thumb_col: [4:10], sw_hist_thumb_row: [4:8]. There are some constraints of these configurations:
   thumb_num = sw_hist_thumb_row * sw_hist_thumb_col
   bin_size = sw_dhaz_blk_wid * sw_dhaz_blk_het * 8
   There is constraint that bin_size < 2^21. If the bitwidth of bin_size is more than 18bit, thumb_num <= 40, otherwise, thumb_num <= 80.
3) When image height > 1620, sw_dhaz_thumb_row >= 6.
4) The down-sample block histogram result (hist_iir_mem) in HIST can be read/write in address offset 0x3c80~0x3c9c, each register store 32bit data which joint by 2 down-sample data in 10bit. Configure address offset 0x3ca0 to read/write hist_iir_mem.
5) For hist_iir_mem read, configure sw_hist_iir_rd_id[7:0] and sys_hist_iir_rd_p, after ro_iir_rdata_val is 1 (0 means data no ready when read), sw_hist_iir0~sw_hist_iir15 will show the down-sample data of the specific row. Then configure next sw_hist_iir_rd_id and sys_hist_iir_rd_p.
6) For hist_iir_mem write, configure sys_hist_iir_wr_clear and sw_hist_iir_wr_id[7:0], then write register sw_hist_iir0~sw_enh_iir15. Then configure next sw_hist_iir_wr_id and sw_hist_iir0~sw_hist_iir9. Here sys_hist_iir_wr_clear can be configured 1time at first write. If data write interrupt in midway, sys_hist_iir_wr_clear shold be configured to restart data write.

44.6.12 YNR

1) Configure hw_ynr_en (address offset 0x2700[0]) to 1 to enable YNR module.
2) The function of high frequency and low frequency noise reduction in YNR module is configured by hw_ynr_hiSpnr_bypass (address offset 0x2700[1]) and hw_ynr_miSpnr_bypass (address offset 0x2700[2]) respectively, which are no bypassed by default.
3) When hw_ynr_rnr_Hcneter[0] (address offset 0x2724) is configured to 1 by default, the center of RNR is the center of image. Otherwise, the center of RNR is depend on hw_ynr_rnr_Hcenter and hw_ynr_rnr_Vcenter (address offset 0x2724).
4) The configuration sw_ynr_rnr_max_r (address offset 0x2720) consists of 9bit integer and 5bit decimal, 1/R^2= M/(2^E), M and E should be calculated automatically by driver.
5) 4 * hw_ynr_hiSpnrFilt_coeff0 + 4 * hw_ynr_hiSpnrFilt_coeff1 + 4 * hw_ynr_hiSpnrFilt_coeff2 + 8 * hw_ynr_hiSpnrFilt_coeff3 <= 256.
6) hw_ynr_hiSpnrFilt1_coeff0 + 4 * hw_ynr_hiSpnrFilt1_coeff1 + 4 * hw_ynr_hiSpnrFilt1_coeff2 + 4 * hw_ynr_hiSpnrFilt1_coeff3 + 8 * hw_ynr_hiSpnrFilt1_coeff4 + 4 * hw_ynr_hiSpnrFilt1_coeff5 = 256.
7) hw_ynr_miSpnrFilt_coeff0 + 4 * hw_ynr_miSpnrFilt_coeff1 + 4 * hw_ynr_miSpnrFilt_coeff2 + 8 * hw_ynr_miSpnrFilt_coeff3 + 4 * hw_ynr_miSpnrFilt_coeff4= 128.
8) When hw_ynr_dsfilt_bypass is set to 1, down sample IIR filter is enabled.

44.6.13 CNR

1) Configure sw_cnr_en to 1 to enable CNR module.
2) YNR, CNR, SHARP, ENHANCE module must be enabled or disabled uniformly.
3) CNR module is not support YUV422 format in this version, so sw_cnr_yuv_422 is always configured to 0.
4) The remaining configurations can be configured according to the default values, or use reference configuration after tuning to achieve the best graphic quality.

44.6.14 SHARP

1) Configure sw_sharp_en to 1 to enable SHARP module, otherwise it is bypass mode.
2) The value of hw_sharp_luma_dx0~hw_sharp_luma_dx6 is 2^n, the sum of the seven coefficients should be 1024.
3) The signal hw_sharp_imgHpf_coeff0~hw_sharp_imgHpf_coeff5 are all signed value, and the sum of them should be 0.

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4) The signal hw_sharp_texWgtFlt_coeff0~ hw_sharp_texWgtFlt_coeff2 respectively represent the center point of the filtering coefficient, 4 points on the upper and lower left and right sides, and 4 points on the 45-degree angle. The sum of the nine coefficients should be guaranteed to be 64.
5) The signal hw_sharp_preBifilt_coeff0~ hw_sharp_preBifilt_coeff2 respectively represent the center point of the filtering coefficient, 4 points on the upper and lower left and right sides, and 4 points on the 45-degree angle. The sum of the nine coefficients should be guaranteed to be 64.
6) The sum of hw_sharp_imgHpf_coeff0~ hw_sharp_imgHpf_coeff5 and hw_sharp_miDetailLpf_coeff0~ hw_sharp_miDetailLpf_coeff5 are all unsigned value and the sum of them should be 128.
7) hw_sharp_edgeLpf_coeff0 + 4 * hw_sharp_edgeLpf_coeff1 + 4 * hw_sharp_edgeLpf_coeff2 + 4 * hw_sharp_edgeLpf_coeff3 + 8 * hw_sharp_edgeLpf_coeff4 + 4 * hw_sharp_edgeLpf_coeff5 + 4 * hw_sharp_edgeLpf_coeff6 + 8 * hw_sharp_edgeLpf_coeff7 + 4 * hw_sharp_edgeLpf_coeff8 = 128.
8) When hw_sharp_exgian_bypass is configured to 1 or hw_sharp_global_gain_alpha is configured to 8, the external gain is not be used by SHARP.
9) hw_sharp_noise_curve_ext0~hw_sharp_noise_curve_ext16 (address offset 0x2a70~0x2a90) is the noise curve, which is the frame statistic of sharp, and should be configured manually in first frame, then read these registers to get the adaptive noise curve of sharp in further frame.

44.6.15 GAIN

1) Configure sw_gain_en to 1 to enable global gain module.
2) GAIN module will configure the enable of corresponding gain from MERGE/LSC/ADRC/BAY3D module according to the enable of these modules adaptively.
3) If global gain module is disabled, exgain_bypass_en of YNR/CNR/SHARP module should be enabled.
4) The signal sw_gain0 is a reused configuration. When sw_mge_gain_en is configured to 1, sw_gain0 is composed of integer of 12 bits and decimal of 6 bits, which is used for the initial value of weight0 of gain of HDR-MGE module. When sw_mge_gain_en is configured to 0, the upper 12 bits of sw_gain0 is the integer part of sw_gain_init, and the lower 6 bits is the decimal part of sw_gain_init, which means sw_gain_init = {sw_gain0, 3'b0}.
5) The signal sw_gain1 and sw_gain2 is valid when sw_mge_gain_en is configured to 1.

44.6.16 RAWAF

1) If sw_rawaf_v1_fir_sel is 0, V1 channel will get old Sobel output, otherwise V1 channel will get new VIIR+VFIR output.
2) When sw_rawaf_viir_en is configured to 1, RAWAF module will open V1 channel. When sw_rawaf_hiir_en is configured to 1, RAWAF module will open H1 channel.
3) When sw_gamma_en is configured to 1, sw_rawaf_viir_en must be configured to 1 too.
4) When sw_rawaf_ae_mode is configured to 1, RAWAF module will enable 5x5 luminance mean statistics, which is reused in RAWAE_BIG module.

44.6.17 RAWAE

1) RAWAE module needs configure as follows:
   - Configure window size, window offset, and so on.
   - Configure sw_aemeas_start to 1 to enable RAWAE module.
   - Waiting for interruption of RAWAE module.
   - Read back the statistics data when the interruption is available.
   - Configure sw_aemeas_start to 1 to clear this signal and restart RAWAE module.
   - Waiting for the interruption of next frame.
2) It is a large amount of readback data. When the statistics data of the 1st frame is ready but not completely readback during vblank of 1st frame until the middle of the 2nd frame, if the enable of statistics is configured at this time, RAWAE module will get statistics data at the 3rd frame, and generate interruption after the statistics data of the 3rd frame is ready. When the statistics data of the 1st frame is ready and completely readback during vblank of 1st frame, if the enable of statistics is configured

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at this time, RAWAE module will get statistics data at the 2nd frame.

Here have some constraints for AE:

3) The sub-window size and offset must even. For non-independent sub-windows, it is required that the data of last two lines of a frame cannot be used in statistics. Each sub-window size is at least 16x4, and each sub window cannot exceed the right boundary and lower boundary of the input image after configuration.
4) The statistics of RAWAE_BIG module is stored at DDR, so it is necessary to use a for loop to read RAWAE_BIG_RO_MEAN_BASE_ADDR repeatedly. RAWAE_BIG module supports RAM address offset to get the statistics in a certain address by configuring sw_ram_offset.
5) One window in RAWAE_BIG module should be configured by using coordinate directly instead of window size, whose enable is configured in sw_rawae_big_wnd1. The statistics of this window is stored without division operation, so it needs to divide by window size manually. The maximum window size is 2kx1k. If statistics overflow, all the bits of statistics will be 0xf.
6) RAWAE_BIG module supports 1x1, 5x5, 15x15 window size.

44.6.18 RAWAWB

1) Data Pre-Process
   RAWAWB input data is 12bit raw format and the input picture could crop by the crop module. The cropped picture should align at the down sample window size, 4 or 8 configurable, and the hardware would guarantee this by force. The RGB data down sampled from RAW data and Y data converted from RGB data will do some limitation (the limitation is configurable) and then output to detection module.
2) White Point Detection
   There are three region white point detection method, XY region, UV region and YUV region. These three methods will do and logic to catching the white point. The enable of three detection method is configurable.
3) Block Measurement
   The down sampled picture would divide into 5x5 blocks and then accumulate each block input data. The input data could be down sampled data, XY white point data or UV white point data and it is configured by sw_rawawb_blk_measure_mode.
4) Data Read Back
   All measurement information could read back to software by AHB bus. When the measurement is over the hardware will pull up the sw_rawawb_meas_done signal. And then the software could read back all the information. The software should pull the signal down by setting this signal to 1 when read is over. The next frame measurement is valid only if the sw_rawawb_meas_done is 0 before the next frame start.

44.6.19 RAWHIST

RAWHIST_BIG module needs to read the fix address RO_BASE_BIN 256 times when read back

1) RAWHIST module needs configure as follows:
   - Configure window size, window offset, and so on.
   - Configure sw_aehist_en to 1.
   - Waiting for interruption of RAWHIST module.
   - Read back the statistics data when the interruption is available.
   - Configure sw_aehist_done to 1 to clear this signal and restart RAWAE module.
   - Waiting for the interruption of next frame.

Here have some constraints for HIST:

2) The sub-window size and offset must even.
3) When user sets the weights of RAWHIST_BIG, sw_config_wram_en needs to be configured to 1 ahead.
4) The coefficient sw_rawae_gcc needs half because there are two G (Gr, Gb) in the RAW2Y formula.

44.6.20 IRQ

There are three important interrupt registers in ISP, one is ISP_MIS (address offset 0x05c4), one is ISP3A_MIS (address offset 0x05d8), the other is MI_MIS (address offset 0x1500).

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The following chart shows the interrupt sequence between several interrupts:

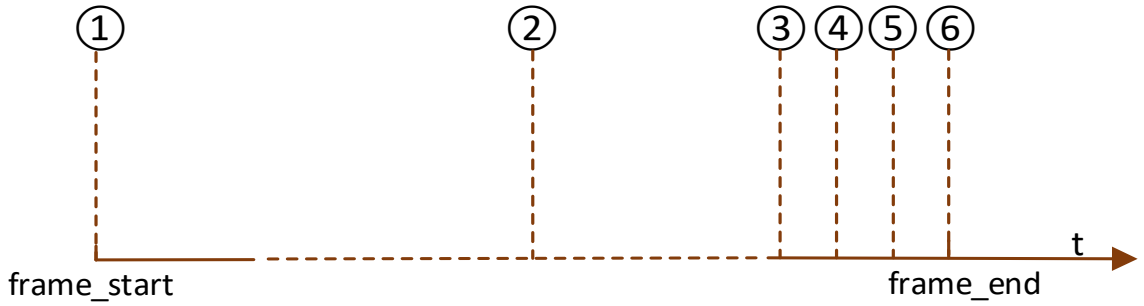

Figure 44-4 Interrupt Sequence

The meanings of the above numerical symbols are as follows:

Table 44-4 Meaning of IRQ

No.	Interrupt name	Register name	Meaning
1	MIS_V_START	ISP_MIS	start edge of v_sync, pull up time is the same as first pixel valid is ISP
2	MIS_RAWXX_DONE	ISP3A_MIS	3A module done signal
3	MIS_FRAME_IN	ISP_MIS	INFORM module frame end signal
4	MIS_HDR_DONE	ISP_MIS	HDR module frame end signal
5	MIS_FRAME_OUT	ISP_MIS	ISP module frame end signal
6	mp_frame_end	MI_MIS	MI module frame end signal

MIS_RAWXX_DONE of above table indicates different 3A interrupts, which interrupt time are determined by the size of the window in different 3A module.

44.6.21 SHD_REG

All MI shadow registers are list in following table (The shadow registers in other function module not listed here, refer to 44.4.2 in detail).

Table 44-5 Shadow Register List

Signal	In which module	Registers addr	Bit	Meaning
sw_csi_raw0_wr_en_shd	MIPI	0x1C40	31	Raw0_wr enable shadow, hold when enable. Update when mp frame end. The channel that write csi data to DDR. 1'b1: Enable the channel 1'b0: Disable the channel
sw_csi_raw1_wr_en_shd	MIPI	0x1C50	31	Raw1_wr enable shadow, hold when enable. Update when mp frame end. The channel that write csi data to DDR. 1'b1: Enable the channel 1'b0: Disable the channel
sw_csi_raw2_wr_en_shd	MIPI	0x1C60	31	Raw2_wr enable shadow, hold when enable. Update when mp frame end.

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				The channel that write csi data to DDR. 1'b1: Enable the channel 1'b0: Disable the channel
sw_csi_raw3_wr_en_shd	MIPI	0x1C70	31	Raw3_wr enable shadow, hold when enable. Update when mp frame end. The channel that write csi data to DDR. 1'b1: Enable the channel 1'b0: Disable the channel
path_enable_in	MI	0x1474	3:0	path_enable shadow register for module MI_IN (former raw_enable_in, jpeg_enable_in, sp_enable_in, mp_enable_in)
path_enable_out	MI	0x1474	19:16	path_enable shadow register for module MI_OUT (former raw_enable_out, jpeg_enable_out, sp_enable_out, mp_enable_out)
sw_mp_wr_y_base_shd	MI	0x1478	31:4	Base address of main picture Y component ring buffer, JPEG ring buffer or raw data ring buffer. --- MI_MP_WR_Y_BASE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
sw_mp_wr_y_size_shd	MI	0x147C	28:4	Size of main picture Y component ring buffer, JPEG ring buffer or raw data ring buffer. --- MI_MP_WR_Y_SIZE_SHD --- Note: This register protects from non-aligned access.
sw_mp_wr_y_offs_cnt_shd	MI	0x1480	28:4	Current offset counter of main picture Y component, JPEG or raw data ring buffer for address generation. Note: Soft reset will reset the contents to reset value. --- MI_MP_WR_Y_OFFS_CNT_SHD --- Note: This register protects from non-aligned access.

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sw_mp_wr_y_irq_offs_shd	MI	0x1484	28:4	Reaching this offset value by the current offset counter for addressing main picture Y component, JPEG or raw data leads to generation of fill level interrupt fill_mp_y. --- MI_MP_WR_Y_IRQ_OFFS_SHD --- Note: This register protects from non-aligned access.
sw_mp_wr_cb_base_shd	MI	0x1488	31:4	Base address of main picture Cb component ring buffer. --- MI_MP_WR_CB_BASE_SHD --- Note: This register protects from non-aligned access.
sw_mp_wr_cb_size_shd	MI	0x148C	27:4	Size of main picture Cb component ring buffer. --- MI_MP_WR_CB_SIZE_SHD --- Note: This register protects from non-aligned access.
sw_mp_wr_cb_offs_cnt_shd	MI	0x1490	27:4	Current offset counter of main picture Cb component ring buffer for address generation. Note: Soft reset will reset the contents to reset value. --- MI_MP_WR_CB_OFFS_CNT_SHD --- Note: This register protects from non-aligned access.
sw_mp_wr_cr_base_shd	MI	0x1494	31:4	Base address of main picture Cr component ring buffer. --- MI_MP_CR_BASE_AD_SHD --- Note: This register protects from non-aligned access.
sw_mp_wr_cr_size_shd	MI	0x1498	27:4	Size of main picture Cr component ring buffer. --- MI_MP_WR_CR_SIZE_SHD --- Note: This register protects from non-aligned access.
sw_mp_wr_cr_offs_cnt_shd	MI	0x149C	27:4	Current offset counter of main picture Cr component ring buffer for address generation. Note: Soft reset will reset the contents

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				to reset value. --- MI_MP_WR_CR_OFFS_CNT_SHD --- Note: This register protects from non-aligned access.
sw_sp_wr_y_base_shd	MI	0x14A0	31:4	Base address of self picture Y component ring buffer. --- MI_SP_WR_Y_BASE_SHD --- Note: This register protects from non-aligned access.
sw_sp_wr_y_size_shd	MI	0x14A4	28:4	Size of self picture Y component ring buffer. --- MI_SP_WR_Y_SIZE_SHD --- Note: This register protects from non-aligned access.
sw_sp_wr_y_offs_cnt_shd	MI	0x14A8	28:4	Current offset counter of self picture Y component ring buffer for address generation. Note: Soft reset will reset the contents to reset value. --- MI_SP_WR_Y_OFFS_CNT_SHD --- Note: This register protects from non-aligned access.
sw_sp_wr_cb_base_shd	MI	0x14B0	31:4	Base address of self picture Cb component ring buffer. --- MI_SP_WR_CB_BASE_AD_SHD --- Note: This register protects from non-aligned access.
sw_sp_wr_cb_size_shd	MI	0x14B4	27:4	Size of self picture Cb component ring buffer. --- MI_SP_WR_CB_SIZE_SHD --- Note: This register protects from non-aligned access.
sw_sp_wr_cb_offs_cnt_shd	MI	0x14B8	27:4	Current offset counter of self picture Cb component ring buffer for address generation. Note: Soft reset will reset the contents to reset value. --- MI_SP_WR_CB_OFFS_CNT_SHD --- Note: This register protects from non-

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				aligned access.
sw_sp_wr_cr_base_shd	MI	0x14BC	31:4	Base address of self picture Cr component ring buffer. --- MI_SP_WR_CR_BASE_SHD --- Note: This register protects from non-aligned access.
sw_sp_wr_cr_size_shd	MI	0x14C0	27:4	Size of self picture Cr component ring buffer. --- MI_SP_WR_CR_SIZE_SHD --- Note: This register protects from non-aligned access.
sw_sp_wr_cr_offs_cnt_shd	MI	0x14C4	27:4	Current offset counter of self picture Cr component ring buffer for address generation. Note: Soft reset will reset the contents to reset value. --- MI_SP_WR_CR_OFFS_CNT_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
sw_mp_wr_y_irq_offs2_shd	MI	0x15E4	28:4	Reaching this offset value by the current offset counter for addressing main picture Y component, JPEG or raw data leads to generation of fill level interrupt fill_mp_y. --- MI_MP_WR_Y_IRQ_OFFS_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
sw_bp_wr_y_base_shd	MI	0x1634	31:4	Base address of bypass picture Y component ring buffer. --- MI_BP_WR_Y_BASE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
sw_bp_wr_y_size_shd	MI	0x1638	28:4	Size of bypass picture Y component ring buffer.

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				--- MI_BP_WR_Y_SIZE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
sw_bp_wr_y_offs_cnt_shd	MI	0x163c	28:4	Current offset counter of bypass picture Y component ring buffer for address generation Note: Soft reset will reset the contents to reset value. --- MI_BP_WR_Y_OFFS_CNT_SHD --- Note: This register protects from non-aligned access.
sw_bp_wr_cb_base_shd	MI	0x1640	31:4	Base address of bypass picture Cb component ring buffer. --- MI_BP_WR_CB_BASE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
sw_bp_wr_cb_size_shd	MI	0x1644	27:4	Size of bypass picture Cb component ring buffer. --- MI_BP_WR_CB_SIZE_SHD --- Note: This register protects from non-aligned access. Refer to MI_MP_WR_Y_BASE register description for details.
sw_bp_wr_cb_offs_cnt_shd	MI	0x1648	27:4	Current offset counter of bypass picture Cb component ring buffer for address generation Note: Soft reset will reset the contents to reset value. --- MI_BP_WR_CB_OFFS_CNT_SHD --- Note: This register protects from non-aligned access.
sw_raw0_wr_base_shd	MI	0x182C	31:4	Base address of raw0 tx data ring buffer. --- RAW0_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to RAW0_WR_BASE register description

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				for details.
sw_raw1_wr_base_shd	MI	0x183C	31:4	Base address of raw1 tx data ring buffer. --- RAW0_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to RAW0_WR_BASE register description for details.
sw_raw2_wr_base_shd	MI	0x184C	31:4	Base address of raw2 tx data ring buffer. --- RAW0_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to RAW0_WR_BASE register description for details.
sw_raw3_wr_base_shd	MI	0x185C	31:4	Base address of raw3 tx data ring buffer. --- RAW0_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to RAW0_WR_BASE register description for details.
sw_raw0_rd_base_shd	MI	0x1878	31:4	Base shadow address of raw0 rx data ring buffer
sw_raw1_rd_base_shd	MI	0x1888	31:4	Base shadow address of raw1 rx data ring buffer
sw_raws_rd_base_shd	MI	0x1898	31:4	Base shadow address of raws rx data ring buffer
dbr_wr_base_shd	MI	0x196C	31:4	Base address of mimux write data ring buffer. --- DBR_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to DBR_WR_BASE register description for details.
dbr_rd_base_shd	MI	0x1978	31:4	Base shadow address of mimux read data ring buffer
gain_wr_base_shd	MI	0x1990	31:4	Base address of gain write data ring buffer. --- GAIN_WR_BASE_SHD --- Note: This register protects from non-

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				aligned access. Refer to GAIN_WR_BASE register description for details.
bay3d_wr_iir_base_shd	MI	0x19ac	31:4	Base address shadow register for bayer 3dnr iir write data ring buffer
bay3d_iir_rd_base_shd	MI	0x19b8	31:4	Base shadow address of bayer 3dnr iir read data ring buffer.
bay3d_cur_wr_base_shd	MI	0x19cc	31:4	Base address of bayer 3dnr current write data ring buffer. --- BAY3D_CUR_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to BAY3D_CUR_WR_BASE register description for details.
bay3d_cur_rd_base_shd	MI	0x19d8	31:4	Base shadow address of bayer 3dnr current read data ring buffer.
bay3d_ds_wr_base_shd	MI	0x19ec	31:4	Base address of bayer 3dnr iir write data ring buffer. --- BAY3D_IIR_WR_BASE_SHD --- Note: This register protects from non-aligned access. Refer to BAY3D_IIR_WR_BASE register description for details.
bay3d_ds_rd_base_shd	MI	0x19f8	31:4	Base shadow address of bayer 3dnr down scale read data ring buffer.
scale_hy_enable_shd	SELF_RESIZE	0x0C30, 0x1030	0	1'b0: Bypass horizontal luminance scaling unit 1'b1: Enable horizontal luminance scaling unit
scale_hc_enable_shd	SELF_RESIZE	0x0C30, 0x1030	1	1'b0: Bypass horizontal chrominance scaling unit 1'b1: Enable horizontal chrominance scaling unit
scale_vy_enable_shd	SELF_RESIZE	0x0C30, 0x1030	2	1'b0: Bypass vertical luminance scaling unit 1'b1: Enable vertical luminance scaling unit
scale_vc_enable_shd	SELF_RESIZE	0x0C30, 0x1030	3	1'b0: Bypass vertical chrominance scaling unit 1'b1: Enable vertical chrominance

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				scaling unit
scale_hy_up_shd	SELF_RESIZE	0x0C30, 0x1030	4	1'b1: Horizontal luminance up-scaling selected 1'b0: Horizontal luminance down-scaling selected
scale_hc_up_shd	SELF_RESIZE	0x0C30, 0x1030	5	1'b1: Horizontal chrominance up-scaling selected 1'b0: Horizontal chrominance down-scaling selected
scale_vy_up_shd	SELF_RESIZE	0x0C30, 0x1030	6	1'b1: Vertical luminance up-scaling selected 1'b0: Vertical luminance down-scaling selected
scale_vc_up_shd	SELF_RESIZE	0x0C30, 0x1030	7	1'b1: Vertical chrominance up-scaling selected 1'b0: Vertical chrominance down-scaling selected
scale_hy_shd	SELF_RESIZE	0x0C34, 0x1034	15:0	This register is set to the horizontal luminance downscale factor or to the reciprocal of the horizontal luminance upscale factor.
scale_hcb_shd	SELF_RESIZE	0x0C38, 0x1038	15:0	This register is set to the horizontal Cb downscale factor or to the reciprocal of the horizontal Cb upscale factor.
scale_hcr_shd	SELF_RESIZE	0x0C3C, 0x103C	15:0	This register is set to the horizontal r downscale factor or to the reciprocal of the horizontal r upscale factor.
scale_vy_shd	SELF_RESIZE	0x0C40, 0x1040	15:0	This register is set to the vertical luminance downscale factor or to the reciprocal of the vertical luminance upscale factor.
scale_vc_shd	SELF_RESIZE	0x0C44, 0x1044	15:0	This register is set to the vertical chrominance downscale factor or to the reciprocal of the vertical chrominance upscale factor.
phase_hy_shd	SELF_RESIZE	0x0C48, 0x1048	15:0	This register is set to the horizontal luminance phase offset
phase_hc_shd	SELF_RESIZE	0x0C4C, 0x104C	15:0	This register is set to the horizontal chrominance phase offset.

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phase_vy_shd	SELF_RESIZE	0x0C50, 0x1050	15:0	This register is set to the vertical luminance phase offset.
phase_vc_shd	SELF_RESIZE	0x0C54, 0x1054	15:0	This register is set to the vertical chrominance phase offset.
isp_enable_shd	ISP_CTRL	0x5A8	0	ISP enable shadow register shows, if ISP currently outputs data (1) or not (0)
isp_inform_enable_shd	ISP_CTRL	0x5A8	1	Input formatter enable shadow register
isp_out_h_offs_shd	ISP_CTRL	0x5AC	13:0	Current vertical pic offset in lines
isp_out_v_offs_shd	ISP_CTRL	0x5B0	13:0	Current vertical pic offset in lines
isp_out_h_size_shd	ISP_CTRL	0x5B4	14:0	Current horizontal pic size in pixel
isp_out_v_size_shd	ISP_CTRL	0x5B8	13:0	Vertical pic size in lines
sw_sws_en_shd	SWS	0x1C	30	sw_sws_en_shd

How to update the shadow register:

- You can choose to update through force_upd and frame end update.
- The forced update is generally used before the start of a frame. The configuration mode is to enable ISP control, which is the 9th bit of address offset 0x0400.
- If you need to enable the end of frame update, you need to pull up the 8th bit of address offset 0x0400, otherwise it will not be updated by default.
- 10th bit of address offset 0x0400 can update shadow registers only one time while frame end is coming.

44.6.22 Multi-Sensor

Multi-sensor mainly uses the frame buffers to cache the data of the previous frame to solve the problem of previous frame data caching. Frame buffer is read/write by AHB in each frame of each sensor.

44.6.23 LDCH

LDCH module supports minimum resolution of 256x256 because of the constraint of LUT. When bicubic mode, LDCH will read 16bit table data from DDR, where the upper 12bit is integer part, which is used to strobe 4 pixels for calculation, and the lower 4bit is decimal part, which is used to strobe 4 coefficients of bicubic table for calculation. If the resolution is bigger than 4080, the 16bit table data is comprised of 13bit integer and 3bit decimal, at this time module will right shift the 3bit decimal to get a 4bit decimal for calculation when strobing bicubic table. This process is show below:

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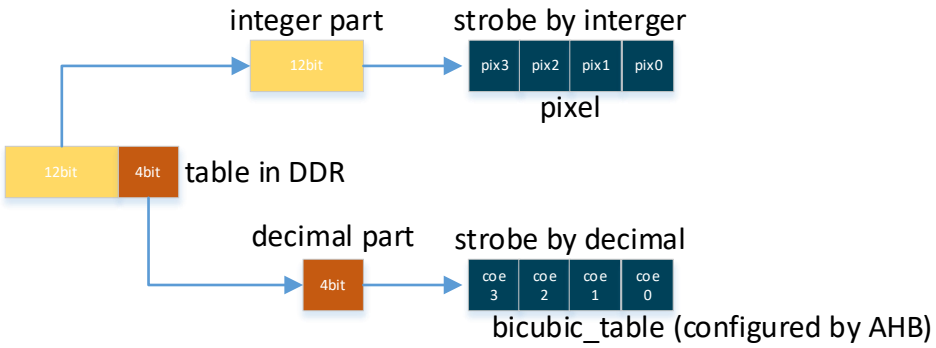

Figure 44-5 LDCH Process

44.6.24 AXI Register Readback

When sys_axi_conf_rd_st (address offset 0x1a40[0]) is enabled, AXI will readback register configuration from DDR to configure ISP, MI and CSI2RX. AXI register readback and AHB register configuration can work at the same time, and the latter has higher priority.
AXI register configuration is composed of head (address offset + mode + counter) + data, which is shown as below:

	[31:18]	[17:16]	[15:0]
head	addr[15:2]	mode	counter
data	data(32bit)		

Figure 44-6 AXI Register Configuration

mode 2'b00 is increased mode, mode 2'b11 is fixed mode, counter is the number of register configuration, which must be consistent with data number. When data is 32'hffffffff, AXI Register Readback is finished. Here is an example of AXI register readback:

	[31:18]	[17:16]	[15:0]		
head	0x3c00>>2	00	5		
data	data_0			0x3c00	mode=2'd00, address increment
	data_1			0x3c04	
	data_2			0x3c08	
	data_3			0x3c0c	
	data_4			0x3c10	
head	0x2600>>2	11	6		
data	data_0			0x2600	mode=2'd11, address fixed
	data_1			0x2600	
	data_2			0x2600	
	data_3			0x2600	
	data_4			0x2600	
	data_5			0x2600	
	32'hffff_ffff			结束	

Figure 44-7 An Example of AXI Register Readback

The step of AXI register readback:
1) Calculate the word number of configuration, configure sw_axi_conf_wsize (address offset 0x1a48) and sw_axi_conf_vsize (address offset 0x1a4c). The word number of configuration is sw_axi_conf_wsize * sw_axi_conf_vsize (this product results must be greater than or equal to 64). When sw_axi_conf_wsize is no more than 8192, sw_axi_conf_vsize is 1, otherwise when sw_axi_conf_wsize is no more than 8192 * 2, sw_axi_conf_vsize is 2, and so on.
2) Configure sw_axi_conf_rd_base (address offset 0x1a44), where has loaded the AXI register configuration.
3) Configure sys_axi_conf_rd_st (address offset 0x1a40[0]) to 1 to start AXI register readback. There are two modes of AXI register readback. When sys_axi_conf_rd_st_mode (address offset 0x1a40[1]) is configured to 1, AXI register readback start by configuring sys_axi_conf_rd_st to 1 in each frame. When sys_axi_conf_rd_st_mode is 0, AXI register

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readback start by sys_axi_conf_rd_st in first frame, then will start by frame end signal automatically, and on this condition axi_conf_rd_status (address offset 0x1a40[31]) must be cleared by configuring axi_conf_rd_clear (address offset 0x1a40[4]) to 1 during current frame.

4) Constraint: The MMU registers need to be configured by AHB.

44.6.25 Slice Start

ISP support slice start in this version. Configure sw_isp_irq_line0 (address offset 0x0564[13:0]) to the line number you want to suspend, then configure sw_isp_slice_en (address offset 0x06a4[1]) to 1 to enable slice start function. The signal isp_slice_done (address offset 0x06a4[31]) will be 1 when ISP output line number equal to sw_isp_irq_line0, then configure sys_isp_slice_st (address offset 0x06a4[0]) to 1 to continue ISP process. When slice start is enabled, the range of sw_isp_irq_line0 is 0 < sw_isp_irq_line0 < sw_csi_col.

44.6.26 CAC

1) Configure sw_cac_en (address offset 0x2600[0]) to 1 to enable CAC module.
2) CAC module use bypass mode when sw_cac_bypass (address offset 0x2600[1]) is configured to 1.
3) CAC cannot support PSF configuration in this version.

44.6.27 EXPANDER

- When use sensor with data compression, HDRMGE module is disabled, expander module should be enabled.
- When use sensor without data compression, HDRMGE module is disabled, expander module should be bypass.
- When use sensor without data compression, HDRMGE module is enabled, expander module must be bypass.
- Register sw_expd_mode, 1'b0 means 12bit to 20bit, 1'b1 means 16bit to 20bit.
- Register sw_expd_x0~sw_expd_x31 configure the abscissa, and sw_expd_y0~ sw_expd_y31 configure the ordinate.
- Register sw_expd_k0~sw_expd_k31 configure the gradient, whose bit width is expanded to meet accuracy requirements of certain curve, sw_expd_k0 = floor(2 ^ sw_expd_k_shift * (sw_expd_y1- sw_expd_y0) / (sw_expd_x1-sw_expd_x0)), and so on.
- Conifigure the maximum input value in sw_expd_imax, and the maximum output value in sw_expd_omax.
- EXPAND function is conflict with GAMMA_IN, HDRMGE, PREDGAIN, RGBIR, AI-ISP.

44.6.28 GIC

1) Configure sw_gic_en to 1 to enable GIC module.
2) If process mode is to reduce single black or white pixel, configure sw_gic_pro_mode to 0. Otherwise, configure to 1 to reduce lattice effect.
3) When sw_gic_manualnoisethred_en is configured to 0, the noise threshold curve is auto calculated by module. Otherwise, the noise threshold curve need to be configured manually.
4) When the noise threshold curve is auto calculated by module, the external gain is be used, or configure sw_gic_gain_bypass_en to 1 to bypass the external gain.
5) The noise curve needs to be configured manually when the first frame of GIC or sw_gic_manualnoisecurve_en is configured to 0. Otherwise, configured sw_gic_manualnoisecurve_en to 1 to use noise curve from SHARP module.

44.6.29 RGBIR

RGBIR module should be enabled just in noHDR mode. When RGBIR is enabled, the image height must be aligned to 4pixel.

44.6.30 AI-ISP

1) AI-ISP function is conflict with HDRMGE, PREDGAIN function.
2) AI-ISP write the ISP intermediate RAW data and gain data to DDR, which will be processed by AINR and then readback to ISP.
3) Support a certain line write done IRQ and slice control.
4) Support RAW data 32 segment interpolation
5) Support RAW data DDR read/write in specific line interrupt and slice controll.

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6) The data path of AI-ISP is shown as below:

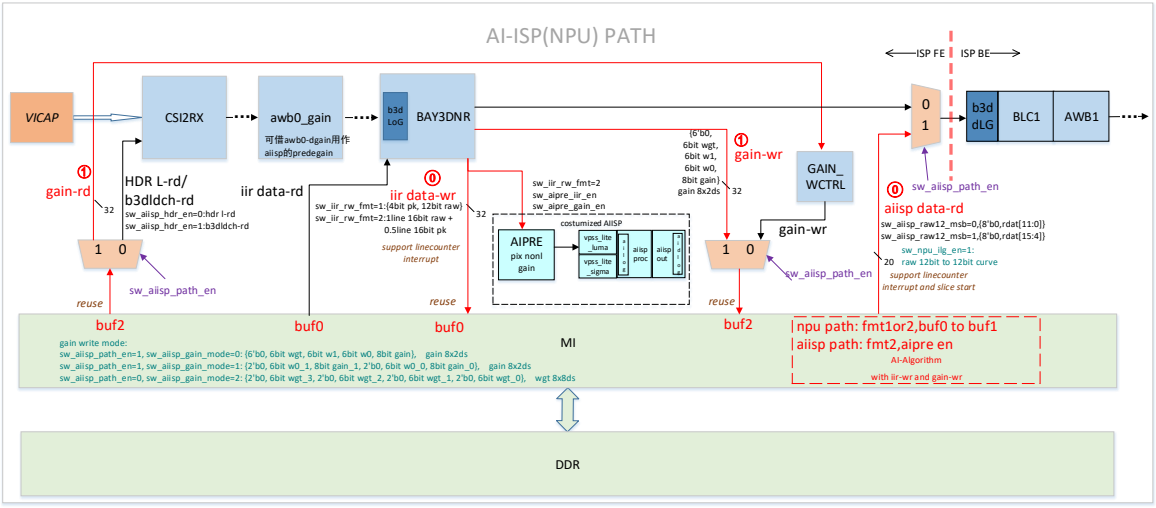

Figure 44-8 AI-ISP Path

44.6.31 AIPRE

1) set sw_bay3d_iir_rw_fmt to 2.
2) set sw_aipre_yraw_sel, 1 for RAW path out, 0 for YUV path out. when sw_aipre_yraw_sel is 1, set sw_aipre_iir_en to 1, otherwise, set to 0.
3) When sw_aipre_iir_en is 1, set sw_aipre_iir2ddr_en to 1 to enable data output to DDR. At this time, sw_aipre_nl_ddr_mode can be set to 0 for DDR output to NN, and 1 for DDR output to VPSL offline.
4) When ISP gain module is enable, set sw_aipre_gain_en to 1 and sw_aipre_gain2ddr_en to 1 to output gain data to DDR to AIISP.

44.6.32 W3A

The step of W3A configuration is

1) configure sw_w3a_en, sw_3a_auto_clr_en
2) configure W3A DDR base address and IRQ setting
3) start ISP
4) configure W3A DDR base address of next frame
5) wait for W3A all done IRQ
6) read 3A statistical data from DDR, then repeat 3)

44.6.33 Low power mode

ISP can disable some function of module to reduce power consumption with effect decrease in some low power required application scenarios. The module support low power mode includes BAY3D, ADRC, YNR, CNR, ENHANCE. Disable some function inside these modules manually to reduce power, and use Y400/YUV420 output and disable SP output can also reduce power.

44.6.34 SHD register update

3A/W3A, AIPRE, B3DLDC, AIAWB should use itself_force_upd inside module to update their register, can not use ISP force_upd in common. Their itself_force_upd can see 44.4.2 in detail.

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Chapter 45 NPU

45.1 Overview

RKNN is the process unit which is dedicated to neural network and General operation. It is designed to accelerate the neural network arithmetic in field of AI (artificial intelligence) such as machine vision and natural language processing. It can also be used for general purpose computing. The variety of applications for AI is expanding, and currently provides functionality in a variety of areas, including face tracking as well as gesture and body tracking, image classification, video surveillance, automatic speech recognition (ASR) and advanced driver assistance systems (ADAS).
RKNN supports the following features:

- AHB interface used for configuration only support single
- NSP Slave Bus Interface used for internal buffer access
- AXI interface used to fetch data from memory
- Support integer 4, integer 8, integer 16, float 16, Bfloat 16 and tf32 operation
- 1024 integer 8 MAC operations per cycle
- 512 integer 16 MAC operations per cycle
- 512 float 16 MAC operations per cycle
- 512 bfloat 16 MAC operations per cycle
- 256 tf32 MAC operation per cycle
- 2048 integer 4 MAC operation per cycle
- 512KB internal buffer
- Inference Engine: TensorFlow, Caffe, Tflite, Pytorch, Onnx NN, Android NN, etc.

45.2 Block Diagram

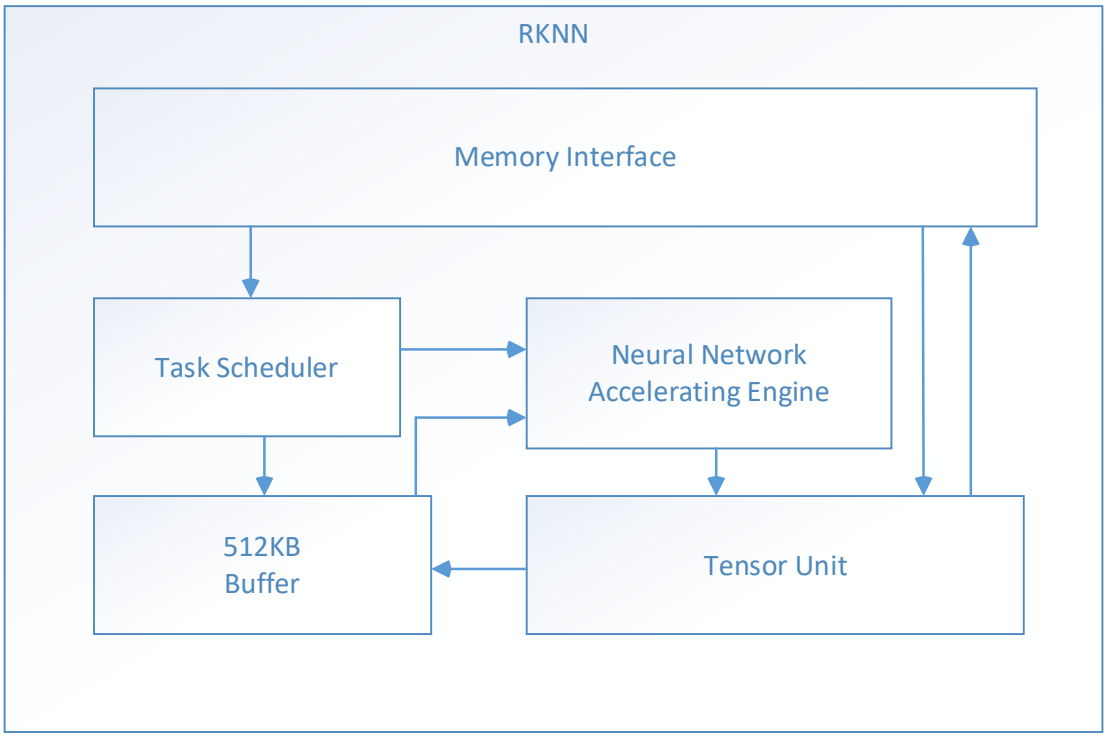

Fig. 45-1 RKNN Architecture

45.3 Function Description

45.3.1 Memory Interface

The AXI master interface is used to fetch data from memory that is attached to the SoC AXI interconnect. The AHB slave interface is used to access the registers for configuration, debug and test.

45.3.2 Neural Network Accelerating Engine

As the unit name, this engine is the main process unit for Neural Network arithmetic. This

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unit include convolution pre-process controller, internal buffer, mac array, accumulator. It provides parallel convolution MAC for recognition functions and int4, int8, int16, fp16, bfloat16 and tf16 are supported.

45.3.3 Tensor Unit

Tensor Unit include dot and planar process function. Dot unit mainly process the single data calculate, such as leaky_relu, relu, relux, sigmoid, tanh…etc. It also provides function: softmax, transpose, data format conversion, …etc.

Planar unit mainly provide planar function followed by output data from Data Processing Unit, such as average pooling, max pooling, min pooling… are supported.

45.3.4 Task Scheduler

Task scheduler focus on register configuration from external system memory through AXI interface, and process flow control inside RKNN.

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