

# **IT66121 Programming Guide**

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# Term

<b>Bank</b>	IT66121 internal registers are accessed by I <sup>2</sup> C interface with PCSCL/PCSDA pins. They are separated into two bank, with I <sup>2</sup> C Subaddress 0xF[0] to separate. Registers in bank 0 can be accessed when register 0x0F[0] = '0', otherwise the registers in bank 1 can be accessed by update the value of register 0x0F[0] = '1'. The registers with subaddress 0x00~0x2F are common accessed whatever the bank register 0x0F[0] is '0' or '1', then the bank can be switched anytime.
<b>HDMI</b>	High Definition Multimedia Interface
<b>HPD</b>	Hot Plug Detect – the voltage value read back from the HDMI HPD pin
<b>RegXX</b>	Means the register with subaddress XX in bank 0. eg: Reg04 means the register with subaddress 0x04, RegE0 means the register with the subaddress 0xE0, while the reg0F[0] = '0'.
<b>Reg1XX</b>	Means the register with subaddress XX in bank 1. eg: Reg133 means the register with the subaddress 0x33, while reg0F[0] = '1'.
<b>Tx</b>	HDMI Transmitter
<b>Rx</b>	HDMI Receiver
<b>HDMI Packet</b>	The packets carried in HDMI data island period
<b>Infoframe</b>	The HDMI packet with the infoframe format defined CEA861B/CEA861D/CEA861E
<b>AVMute</b>	The control bit status defined in the <i>General Control Packet</i> of HDMI. When AVMute set is '1', HDMI Rx should mute the video and audio output, otherwise if the AVMute clear is '1', the video and audio should be present.

## Chap 1 Introduce

IT66121 uses I<sup>2</sup>C bus to program its internal registers. The I<sup>2</sup>C slave address is defined as 0x98 when PCADR pin is pulled low, otherwise it is 0x9A. IT66121 series has three packages: IT66121FN, IT66121G, and IT66120FN. The relate pin assignment need to map the corresponding data sheet for each package.

There are two banks of registers in IT66121. The bank switching depends on the content of reg0F (in term reg0F means the register accessed by I<sup>2</sup>C sub-address is 0x0F), 0 means the given subaddress of I<sup>2</sup>C refers to the register set of bank 0; and 1 means the given subaddress of I<sup>2</sup>C refers to the register set of bank 1.

In following term, reg0yy or regyy means the register set of bank 0 with subaddress 0xyy, which yy is from 0x00 to 0xFF; and reg1zz means the register set of bank 1 with subaddress 0xzz and reg0F='1'.

## Programming of IT66121

The programming of IT66121 is separated into following parts:

- [Initial.](#)
- [DDC Command Programming](#)
- [Interrupt Handling.](#)
- [Program video mode.](#)
- [Program audio mode.](#)
- [Activate HDCP](#)
- [Infoframe Programming](#)

And provide [software sample interface](#).

## Chap 2 Initial

To initial IT66121, the following steps should be implement.

1. Chip identifying
2. Reset internal circuit.
3. Enable clock ring.
4. Set default DVI mode and turn off all packet.
5. Set default interrupt mask for event handling.

### Chip Identifying

Before programming IT66121 chip, system needs to identify if the chip is IT66121.

Reg	Register Name	Bit	Definition	Default Value
00	Vender ID	7:0		0x54
01	Vender ID	7:0		0x49
02	Device ID	7:0		0x12
03	Revision ID	7:4		0x0
	Device ID	3:0		0x6

As the table, if I<sup>2</sup>C slave on address 0x98/0x9A responses the sub-address 0x00 ~ 0x03 with the value as the table above, the device is IT66121.

### Enable IT66121 Power Register

0F		7	Reserved	
	RegGateRCLK	6	1: power down RCLK(for I2C)	0
	RegGateIACLK	5	1: power down IACLK (for audio fifo)	0
	RegGateTxCLK	4	1: power down Txclk (for CSC)	0
	RegGateCRCLK	3	1: power down CRCLK (for CEC)	1
		2	Reserved	
RegBankSel	1:0	00: Bank 0, reg00h~ regffh 01: Bank 1, reg130h ~ reg1ffh	0	

Before enable IT66121, the reg0F[6] has to set as '0' for enabling register programming. When reg0F[6] is set as '1', only the I2C read request can be responded but no writing access is available on the chip.

For reg0F[5:3] corresponding to the power control of different parts as described above.

### Initial Power On Sequence

```

Reg0F[6] ← '0'
Reg05[0] ← '0'
Reg61[5] ← '0' // power on the DRV
Reg62[6][2] ← '0' '0' // power on XPLL
Reg64[6] ← '0' // power on IPLL
Reg61[4] ← '0' // enable DRV
Reg62[3] ← '1'
Reg64[2] ← '1'
    
```

### Reset internal circuit.

Reg04 is the software reset control register of IT66121. To reset all circuit of IT66121, reg04[5] = '1'

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then reset to zero, all circuit will be zero.

To enable functions for using, the bits of reg04 should be cleared to zero for enabling. In initial state, reg04 should be 0x1D to wait for function enable.

## **Set default DVI mode and turn off all packet.**

IT66121 usually set to DVI mode under initial state. RegC0 is set to zero for DVI mode, and RegC1~RegD0 are all set to zero for disabling all HDMI packets; reg158 is set to zero for output RGB444 mode under DVI mode.

## **Set default interrupt mask for event handling.**

IT66121 interrupt mask are defined in reg09~reg0B. The bits in these registers are for each interrupt status responding switch, '0' for enabling the responding on status registers, and '1' for disabling the responding of status registers bit.

After initial, the system can be prepare to output with programming video and audio mode.



## Chap 3 Power Setting

This chapter describes how to set IT66121 power setting for standby mode or resume mode.

### Power Down Sequence

```
Reg0F[6] ← '0' ; // Enable global clock to set registers.  
Reg61[4] ← '1' ; // reset AFE  
Reg62[3] ← '0' ;  
Reg64[2] ← '0' ;  
delay about 100 μs
```

```
Reg61[5] ← '1' ; // power down AFE  
Reg62[6][2] ← '1' '1'  
Reg64[6] ← '1'  
Reg05[0] ← '1' // power down PCLK
```

```
Reg0F[6:3] ← '1111' // power all clocks.
```

After above setting, the IT66121 enter to power down status and only accept I<sup>2</sup>C access to resume power.

*\*reference – the Power Down Table in the reference code*

```
// { offset, modify bit mask, modify bit value }  
_CODE RegSetEntry HDMITX_PwrDown_Table[] = {  
    // Enable GRCLK  
    {0x0F, 0x40, 0x00},  
    // PLL Reset  
    {0x61, 0x10, 0x10}, // DRV_RST  
    {0x62, 0x08, 0x00}, // XP_RESETB  
    {0x64, 0x04, 0x00}, // IP_RESETB  
    {0x01, 0x00, 0x00}, // idle(100);  
  
    // PLL PwrDn  
    {0x61, 0x20, 0x20}, // PwrDn DRV  
    {0x62, 0x44, 0x44}, // PwrDn XPLL  
    {0x64, 0x40, 0x40}, // PwrDn IPLL  
  
    // HDMITX PwrDn  
    {0x05, 0x01, 0x01}, // PwrDn PCLK  
    {0x0F, 0x78, 0x78}, // PwrDn GRCLK  
    {0x00, 0x00, 0x00} // End of Table.  
};
```

### Power Resume Sequence

```
Reg0F[6:3] ← '0111' // Enable GCLOCK Only  
Reg05[0] ← '0' // Enable PCLK  
Reg61[5] ← '0'  
Reg62[6][2] ← '0' '0'  
Reg64[6] ← '0'  
Reg61[4] ← '0'  
Reg62[3] ← '1'  
Reg64[2] ← '1'  
Reg0F[5:4] ← '00' // Enable Audio FIFO clock and CSC clock , CEC clock need to enable while using.
```

After above setting, the power state is resumed.

*\*Reference Power On Setting table in the reference code*

```
_CODE RegSetEntry HDMITX_PwrOn_Table[] = {  
    {0x0F, 0x78, 0x38}, // PwrOn GRCLK
```

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```
{0x05, 0x01, 0x00}, // PwrOn PCLK

// PLL PwrOn
{0x61, 0x20, 0x00}, // PwrOn DRV
{0x62, 0x44, 0x00}, // PwrOn XPLL
{0x64, 0x40, 0x00}, // PwrOn IPLL

// PLL Reset OFF
{0x61, 0x10, 0x00}, // DRV_RST
{0x62, 0x08, 0x08}, // XP_RESETB
{0x64, 0x04, 0x04}, // IP_RESETB
{0x0F, 0x78, 0x08}, // PwrOn IACLK
{0x00, 0x00, 0x00} // End of Table.
};
```

## Chap 4 Handling Interrupt

IT66121 activates interrupt pin while events defined in interrupt mask registers occurred. The interrupt activating polarity is programmed in reg05[7]. To check interrupt status is also to read back the register value reg0E[7], where '1' identifying interrupt activated and '0' for otherwise.

Off	Register Name	bit	Description	Default Value
05	REG_INTPol	7	0: INT active low 1: INT active high	0
	REG_INTIOMode	6	1: Open-Drain mode 0: Push-Pull Mode	1
	REGPDTxCLK	0	1: TxCLK power down 0: TxCLK active	0

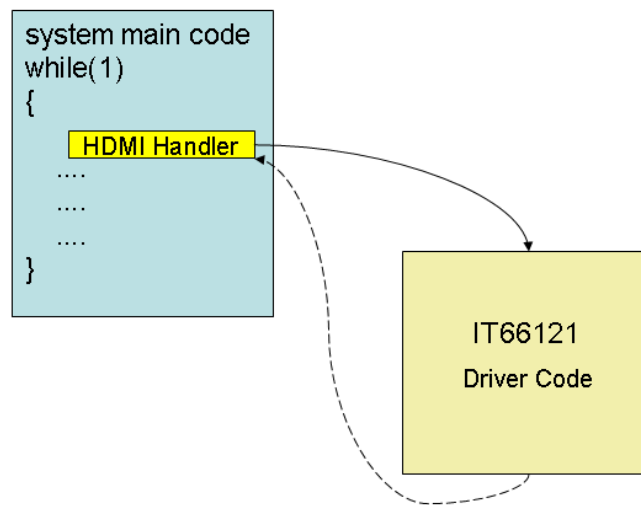


Fig SW Handler

When system process detected if an interrupt activated by the INT pin or reg0E[7] of IT66121, the driver should report what event occurred. To define the events of activating interrupt, the bits of events should be cleared to zero in reg09, reg0B, reg0A. For example, to monitor the hot-plug event changing event, reg09[0] should be set to zero, then while hot-plug change event occurring it trigger the interrupt signal and set reg06[0] as '1'.

To clear the interrupt and interrupt status recorded in reg06, reg07, and reg08, the corresponding bits in reg0C, reg0D, and reg0E[1] should set to '1' then set reg0E[0] with '1' to clear interrupt and status. For example, after processed the hot-plug change event, the status flag and interrupt have to be cleared, then next event can be detected and processed.

The definition of these registers is shown as following table:

Off	Register Name	bit	Description	Default Value
Interrupt Status				
06	RInt_AudioOvFlwStus	7	R, Reset by REGAudReset	
	Reserved	6		
	RDDC_Stus_NoACK	5	R	
	Rint_DDCFIErr	4	R, Reset by RDDC_Req=0x9 REG_MastersSel='1'	
	Reserved	3		
	RInt_DDCBusHang	2	R, Reset by RDDC_Req=0xF REG_MastersSel='1'	
	RInt_RxSENStus	1	R, Reset by REG_RxSENCIr	

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	RInt_HPDCStus	0	R, Reset by REG_HPDClr	
07	RInt_Pkt3DStus	7	R, Reset by REG_3DClr	
	RInt_PktISRC1Stus	6	R, Reset by REG_ISRC1Clr	
	RInt_PktACPStus	5	R, Reset by REG_PktACPClr	
	RInt_PktNullStus	4	R, Reset by REG_PktNullClr	
	RInt_PktGenStus	3	R, Reset by REG_PktGenCr	
	RInt_KSVListChkStus	2	R, Reset by REG_KSVListChkClr	
	RInt_AuthDoneStus	1	R, Reset by REG_AuthenDoneClr	
	RInt_AuthFailStus	0	R, Reset by REG_AuthFailClr	
08	Reserved	7		
	RInt_AudCTSStus	6	R, Reset by Reg_AudCTSClr	
	RInt_VSyncStus	5	R, Reset by REG_VsyncClr	
	RInt_VidStableStus	4	R, Reset by REG_VidStaleClr	
	RInt_PktMpgStus	3	R, Reset by REG_PktMpgClr	
	RInt_PktSPDStus	2	R, Reset by REG_PktSPDClr	
	RInt_PktAudStus	1	R, Reset By REG_PktAudClr	
	RInt_PktAVIStus	0	R, Reset by REG_PktAVIClr	
<b>Interrupt Mask Registers</b>				
09	REG_AudioOvFlwMask	7	1: disable this interrupt.	1
	Reserved	6	0: Enable this interrupt	1
	REG_DDCNoACKMask	5		1
	REG_DDCFIFOErrMask	4		1
	Reserved	3		1
	REG_DDCBusHangMask	2		1
	REG_RxSEnMask	1		1
	REG_HPDMask	0		1
0A	REG_PktAVIMask	7		1
	REG_PktISRCMask	6		1
	REG_PktACPMask	5		1
	REG_PktNullMask	4		1
	REG_PktGenMask	3		1
	REG_KSVListChkMask	2		1
	REG_AuthDoneMask	1		1
	REG_AuthFailMask	0		1
0B	REG_Pkt3DMask	6		1
	REG_AudCTSMask	5		1
	REG_VsyncMask	4		1
	REG_VidStableMask	3		1
	REG_PktMpgMask	2		1
	REG_PktSPDMask	1		1
	REG_PktAudMask	0		1
<b>Interrupt Clear</b>				
0C	REG_PktACPClr	7	1: Clear the interrupt	0
	REG_PktNullClr	6		0
	REG_PktGenClr	5		0
	REG_KSVListChkClr	4		0
	REG_AuthDoneClr	3		0
	REG_AuthFailClr	2		0
	REG_RxSEnClr	1		0
	REG_HPDClr	0		0
0D	REG_VsyncClr	7	1: Clear the interrupt	0
	REG_VidStableClr	6		0
	REG_PktMpgClr	5		0
	REG_PktSPDClr	4		0
	REG_PktAudClr	3		0
	REG_PktAVIClr	2		0
	REG_Pkt3DClr	1		0
	REG_PktISRC1Clr	0		0
<b>System Status</b>				
0E	RInt_FSMON	7	R. 1: Interrupt is active.	
	RHPDetect	6	R Hot Plug Detect: 1: plug on. 0: plug off	
	RxSEnDetect	5	R	
	TxVidStable	4	R. Video input status: 1: stable video input. 0: unstable video input.	
	RegCTSIntStep[1:0]	3:2	R/W	11

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Reg_AudCTSClr	1	Clear AduCTS interrupt	0
Reg_IntActDone_	0	1: Make interrupt clear active. 0: Disable interrupt clear action	0

We usually check the following interrupt events:

1. To detect if the HDMI sink connect and active.

The hot-plug status responds on reg06[0], it is activated for plug status change, high to low or low to high of the HPD pin of IT66121. When this event occurs, system need to handle the sink detecting or turning the output off depends on the HPD status (reg0E[6]).

To enable the event handling, system should set reg09[0] = '0'.

To clear this status, reg0C[0] should be '1' while reg0E[0] written with '1'.

The receiver sense status responds on reg06[1], it is activated for TMDS differential terminate change, ON to OFF or OFF to ON. When this event occurs, system need to handle the sink detecting or turning the output off depends on the HPD status (reg0E[5]).

To enable the event handling, system should set reg09[1] = '0'.

To clear this status, reg0C[1] should be '1' while reg0E[0] written with '1'.

2. When video enable, to detect the input video stable for setting output analog front end.

The video input stable status change event responds on reg08[4], it is activates for input stable changing from stable to unstable or unstable to stable, under reg04[3] = '1'. If this event occurs means there has been unstable input and need to fire AFE while input stable again (reg0E[4] = '1').

To enable the event handling, reg0B[3] = '0'.

To clear this status, reg0D[6] should be '1' while reg0E[0] written with '1'.

3. DDC status events.

When IT66121 issue a request on DDC bus, the bus hang will activate the reg06[2] = '1'. This interrupt status can only clear by Abort DDC command.

When the DDC fetch FIFO has error, the reg06[4] will be activated and only can be clear by DDC FIFO clear command.

4. HDCP status events.

When activate the authentication, there are three related events: authenticate done, authenticate fail, and wait for KSV FIFO.

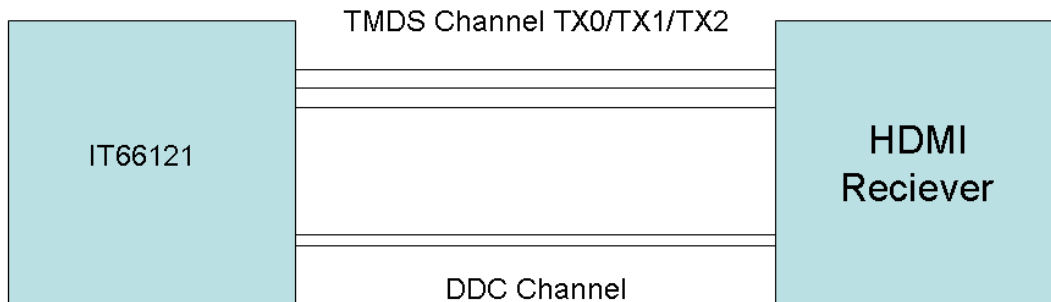
Authentication done event responded in reg07[1] is activated when HDCP authentication integration verification  $R_i = R_i'$ , for each  $i$  include zero when sink is a receiver or does not include zero when sink is repeater. This event is enabled by reg0A[1] = '0', and cleared by setting reg0C[3] = '1' when reg0E[0] is written by '1'. System usually enable this after the authentication start and disable this after first authentication done.

Authentication fail event responded in reg07[0] is activated whenever HDCP authentication fail, include the initial authentication checking fail or any integrating check fail. Whenever this event occurs, the HDCP authentication should be restart. This event is enabled by reg0A[0] = '0', and cleared by setting reg0C[2] when writing reg0E[0] with '1'.

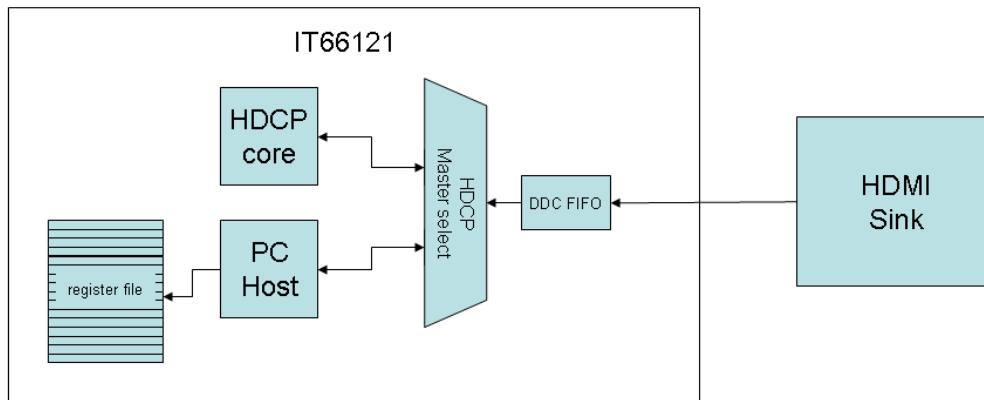
KSVListCheck event responded in reg07[2] is activated when the sink is an HDCP repeater and the first stage of  $R_0 = R_0'$  is checked, then IT66121 should collect the KSVList, confirm them are correct wht  $V = V'$  after SHA-1 encoding. When system receive this event, it should begin to check the BCaps of HDCP sink and do the following action. The detail will be describe in the chapter about HDCP authentication. This event is enabled by reg0A[2] = '0', and cleared by setting reg0C[4] with '1' when writing reg0E[0] = '1'.

## Chap 5 DDC Command Programming

HDMI transmitter communicates with HDMI sink to exchange data for HDCP authentication and to fetch VESA EDID via DDC bus.



IT66121 has internal DDC master circuits for fetching sink EDID data and exchanging HDCP data. Instead of software implement by firmware, IT66121 provide DDC command to fetch data via DDC. Driver can use these commands to get EDID and HDCP B status registers via DDC.



As described in above figure, there are two DDC masters in IT66121. One is PC-host to fetch data by software controlling, and the other is HDCP core which automatically fetching data via DDC bus.

Reg	Register Name	bit	Definition	Default Value
10	Reg_MasterSel	0	Switch HDCP controller or PC host to command the DDC port 0: HDCP 1: PC	0
11	RDDC_Header[7:0]	7:0	PC DDC request slave address: 0x74 when access Rx HDCP 0xA0 when access Rx EDID	
12	RDDC_ReqOffSet[7:0]	7:0	Register address	
13	RDDC_ReqByte[7:0]	7:0	Register R/W byte number	
14	RDDC_Segment[7:0]	7:0	EDID segment	
15	DDC_SDA	7	R. DDC SDA pin status	
	DDC_SCL	6	R. DDC SCL pin status	
	ROM_SDA	5	R. ROM SDA pin status	
	ROM_SCL	4	R. ROM SCL pin status	

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	RDDC_Req[3:0]	3:0	PC DDC request command 0x0 : Sequential Burst Read 0x3: EDID read 0x9: DDC FIFO clear 0xA: GenerateSCL clock pulse 0xF: Abort DDC command.	
16	RDDC_Status[7:0]	7 6 5 4 3 2 1 0	Read Only. RDDC_Stus_Done '0' : DDC is not complete '1' : DDC transfer is complete RDDC_Active RDDC_Stus_NoACK '1' : DDC has something error RDDC_Stus_WaitBus '1' : DDC has something error RDDC_Stus_ArbiLose '1' : DDC has something error RDDC_FIFOFull RDDC_FIFOEmpty TxFIFO status VRValid	
17	RDDC_ReadFIFO	7:0	R. Read DDC FIFO content. There are 32 DDC FIFO, which can read back from the byte. See Fig. 1	

To select DDC master, software needs to set the reg10[0]. If software wish to fetch data from DDC bus, reg10[0] should be set as '1'. reg10[0] should be set as zero that will be described in HDCP chapter.

There are numerous commands defined in IT66121 PC-host master, to read EDID data and HDCP sink registers. These commands are described following:

## Command – DDC Burst Read (0x0)

Software can use this command to read data via DDC bus. To issue the burst read command, the following registers should be programmed:

- Reg11 – I<sup>2</sup>C address. Write 0x74 for reading B registers of HDCP, and write 0xA0 to read EDID data. However, to read data of EDID usually use EDID read command (0x03).
- Reg12 – the subaddress of I<sup>2</sup>C access on DDC bus. For example, the following table is for reading the registers of HDCP sink while reg11=0x74

sub address	Meaning
0x00	BKSV
0x08	Ri'
0x0A	Pj'
0x20~0x30	V:H0 ~ V:H4
0x40	BCaps
0x41/0x42	BStatus

By the way, if the data fetched via DDC with HDCP address, IT66121 will automatically put them into the corresponding registers for HDCP between reg3B ~ reg45 instead of the DDC FIFO. For other data, the read back value are kept in DDC FIFO read back from reg17.

- Reg13 – the count to read from DDC bus.
- Reg15 – Only bit [3:0] can be write of this registers, and should be 0x00 for burst read.

After the reg15 fired, the data are ready when reg16[7] = '1' or DDC fail by reg16[5:3] contains any bit as '1'. After the DDC done, software can read the data from corresponding registers (for HDCP) or DDC FIFO.

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## Get BKSV

Reg10 = 0x01

Reg11 = 0x74

Reg12 = 0x00

Reg13 = 0x05

Reg15 = 0x00

The five bytes of BKSV are ready in reg3B ~ reg3F when reg16[7] = '1'; fail for otherwise.

reg	name	bit	description	default, value
3B	BKSV [7:0]	7:0	Read only.	
3C	BKSV [15:8]	7:0	Read only.	
3D	BKSV [23:16]	7:0	Read only.	
3E	BKSV [31:24]	7:0	Read only.	
3F	BKSV [39:32]	7:0	Read only.	

## Get BCaps

Reg10 = 0x01

Reg11 = 0x74

Reg12 = 0x40

Reg13 = 0x01

Reg15 = 0x00

BCaps is ready in reg43 when reg16[7] = '1'; fail for otherwise.

reg	name	bit	description	default, value
43	Bcaps[7:0]	7	HDMI_Reserved	1
		6	HDCP Repeater capability.	
		5	KSV FIFO ready.	
		4	FAST. 1: the device supports 400KHz transfers.	
		3	reserved. must be zero.	
		2	reserved. must be zero.	
		1	1: HDCP 1.1 Features. support HDCP Enhanced encryption status signaling (EESS), Advance Cipher, and Enhanced Link Verification options.	
		0	1: Fast reauthenticagtion. When set to 1, the receiver is capable of receiving (unencrypted) video signal during the session re-authentication. All HDMI-capable receivers shall be capable of performing the fast re-authentication even if this bit is not set. This bit does not change while the HDCP receiver is active.	



# IT66121 PROGRAMMING GUIDE

## Get BStatus

Reg10 = 0x01  
 Reg11 = 0x74  
 Reg12 = 0x41  
 Reg13 = 0x02  
 Reg15 = 0x00

The Bstatus is ready in reg44/reg45 when reg16[7] = '1'; fail for otherwise.

reg	name	bit	description	default, value
45	Bstatus[15:8]	7	reserved 0.	
		6	reserved 0.	
		5	Reserved for future possible HDMI used.	
		4	HDMI_Mode 1: HDMI mode. 0: DVI mode.	
		3	MAX_CASCADE_EXCEEDED Topology error indicator. 1: more than seven levels of video repeater have been cascaded together.	
		2:0	Three-bit repeater cascade depth.	
44	Bstatus[7:0]	7	1: more than 127 downstream devices or KSV fifo.	
		6:0	Total number of attached downstream devices.	

## Get KSV FIFO List

Reg10 = 0x01  
 Reg11 = 0x74  
 Reg12 = 0x43  
 Reg13 = count of attached down stream device × 5. Maximum is 30, minimum is 5, zero value is not acceptable.  
 Reg15 = 0x00

The KSV List is ready in reg17 which DDC FIFO when reg16[7] = '1'; fail for otherwise.

## Get V'

Reg10 = 0x01  
 Reg11 = 0x74  
 Reg12 = 0x20  
 Reg13 = 0x14  
 Reg15 = 0x00

The 20 bytes of V' are ready in reg3B ~ reg3F when reg16[7] = '1'; fail for otherwise.

Reg	Name	Bit	Description	Default Value
50	SHASel[2:0]	2:0	See SHA_Rd_ByteX registers below	
51	SHA_Rd_Byte1[7:0]	7:0	V0h[7:0] when SHASel="000" V1h[7:0] when SHASel="001" V2h[7:0] when SHASel="010" V3h[7:0] when SHASel="011" V4h[7:0] when SHASel="100" Mi[7:0] when SHASel="101"	
52	SHA_Rd_Byte2[7:0]	7:0	V0h[15:8] when SHASel="000" V1h[15:8] when SHASel="001" V2h[15:8] when SHASel="010" V3h[15:8] when SHASel="011" V4h[15:8] when SHASel="100" Mi[15:8] when SHASel="101"	

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53	SHA_Rd_Byte3[7:0]		V0h[23:16] when SHASel="000" V1h[23:16] when SHASel="001" V2h[23:16] when SHASel="010" V3h[23:16] when SHASel="011" V4h[23:16] when SHASel="100" Mi[23:16] when SHASel="101"	
54	SHA_Rd_Byte4[7:0]	7:0	V0h[31:24] when SHASel="000" V1h[31:24] when SHASel="001" V2h[31:24] when SHASel="010" V3h[31:24] when SHASel="011" V4h[31:24] when SHASel="100" Mi[31:24] when SHASel="101"	
55	Aksv_Rd_Byte5[7:0]	7:0	Mi[39:32] when SHASel="000" Mi[47:40] when SHASel="001" Mi[55:48] when SHASel="010" Mi[63:56] when SHASel="011"	

In HDCP spec, V' is in V0[31:0], V1[31:0], V2[31:0], V3[31:0], and V4[31:0]. When getting V' via DDC is done, the V' can be get by the following steps:

```

Set Reg50 = 0x00 ; then
V0[7:0] = reg51 ; V0[15:8] = reg52 ; V0[23:16] = reg53 ; V0[31:24] = reg54 , and
Set Reg50 = 0x01 ; then
V1[7:0] = reg51 ; V1[15:8] = reg52 ; V1[23:16] = reg53 ; V1[31:24] = reg54 , and
Set Reg50 = 0x02 ; then
V2[7:0] = reg51 ; V2[15:8] = reg52 ; V2[23:16] = reg53 ; V2[31:24] = reg54 , and
Set Reg50 = 0x03 ; then
V3[7:0] = reg51 ; V3[15:8] = reg52 ; V3[23:16] = reg53 ; V3[31:24] = reg54 , and
Set Reg50 = 0x04 ; then
V4[7:0] = reg51 ; V4[15:8] = reg52 ; V4[23:16] = reg53 ; V4[31:24] = reg54 .

```

## Command – EDID Read (0x3)

To get the EDID data, DDC master should write segment with I<sup>2</sup>C address 0x60 then ask the bytes with I<sup>2</sup>C address 0xA0. (That is the major difference to burst read.) The programming of EDID read should set the following registers:

- Reg11 – Should set 0xA0 for EDID fetching.
- Reg12 – Set the starting offset of EDID block on current segment.
- Reg13 – Set the number of byte to read back. The data will be put in DDC FIFO, therefore, cannot exceed the size (32) of FIFO.
- Reg14 – The segment of EDID block to read.
- Reg15 – DDC command should be 0x03.

After reg15 written 0x03, the command is fired and successfully when reg16[7] = '1' or fail by reg16[5:3] contains any bit '1'. When EDID read done, EDID can be read from DDC FIFO.

*Note: By hardware implementation, the I<sup>2</sup>C access sequence on PCSCCL/PCSDA should be*

*<start>-<0x98/0x9A>-<0x17>-<Restart>-<0x99/0x9B>-<read data>-<stop>*

*If the sequence is the following sequence, the FIFO read will be fail.*

*<start>-<0x98/0x9A>-<0x17>-<stop>-<start>-<0x99/0x9B>-<read data>-<stop>*

## Command – DDC FIFO Clear (0x9)

To avoid the remaining data confusing the data fetching from DDC, before data read (burst or EDID), we suggest to clear DDC FIFO at first. To clear DDC FIFO should write reg0F with 0x09, and while reg16[7] = '1', the action is done. Otherwise, the

## **Command – Abort DDC Bus (0xF)**

Sometime the DDC bus will hang by slave incorrect action, IT66121 provide the abort DDC command to resume DDC bus. Writing reg10 with 0xF abort the DDC bus (with sending numerous '1'-'0' pair to bus). If DDC bus aborting is done, reg16[7] will be '1', otherwise reg16[5:3] will contain any bit as '1'.

For processing HDCP fail, DDC bus aborting and DDC FIFO clearing are also necessary, before process them, HDCP should be turned off (by reg04[0] = '1') and DDC master should switch from HDCP core to PC-host with writing '1' to reg10.

## Chap 6 Program Video Mode

To enable the video of IT66121, the input signal type and output TMDS should be programmed.

The following sequence is to set the video mode:

1. Set regC1[0] = '1' for AVMUTE the output.
2. Programming Input Signal Type
3. Set color space converting by the input color space and output color space.
4. Set AFE by the input video pixel clock.
5. Set HDMI package or DVI mode.
6. Set HDCP if necessary.
7. Set Audio if necessary.
8. Clear the AVMUTE by regC1[0] = '0' and regC6 = 0x03.

### Programming Input Signal

For setting the input signal type, reg70[4:2] should be indicated. If input signal do not include DE (data enable) or use sync-embedded mode, the Pattern Sync/DE Generation Registers (reg90~regA3) need to be programmed by timing standard.

Following registers are for input signal and color mode setting:

Video register and input signal controlling registers

Reg	Register Name	bit	Definition	Default Value
04	RegSoftRefRst	5	Software RCLK reset.	0
	RegSoftARst	4	Software Audio clock base signal reset.	1
	REGSoftVRst	3	Software Video clock base signal reset.	1
	REGAudReset	2	Audio FIFO reset.	1
	REGHDCP_rst	0	HDCP reset.	0
<b>Input Data Format Registers</b>				
70	Reg_InColMod[1:0]	7:6	00: RGB mode 01: YUV422 mode 10: YUV444 mode	00
	Reg_2x656Clk	4	1: CCIR656 mode( YUV422, 8/12 bit mode) 0: non- CCIR656 mode	0
	Reg_SyncEmb	3	1: Sync Embedded mode 0: Sync Sep mode	0
	Reg_InDDR	2	1: Input DDR 0: Input SDR	0
72	Reg_EnDither	7	Enable dither function	0
	Reg_EnUdFilt	6	Enable Cr/CB up/down sampling function	0
	Reg_DNFreeGo	5	Dither Noise Pattern	0
	Reg_CSCSel[1:0]	1:0	00: No color space conversion. 10: RGB to YUV 11: YUV to RGB	00
90	Reg_PGHTotal[3:0]	7:4	PG Horizontal Total; See also Reg 0x91	00
	RegGenSync	3	Generate HSync VSync	0
	RegVSPol	2	Generated Vertical Sync Polarity	0
	RegHSPol	1	Generated Horizontal Sync Polarity	0
	Reg_GenDE	0	DE generation Enable	0

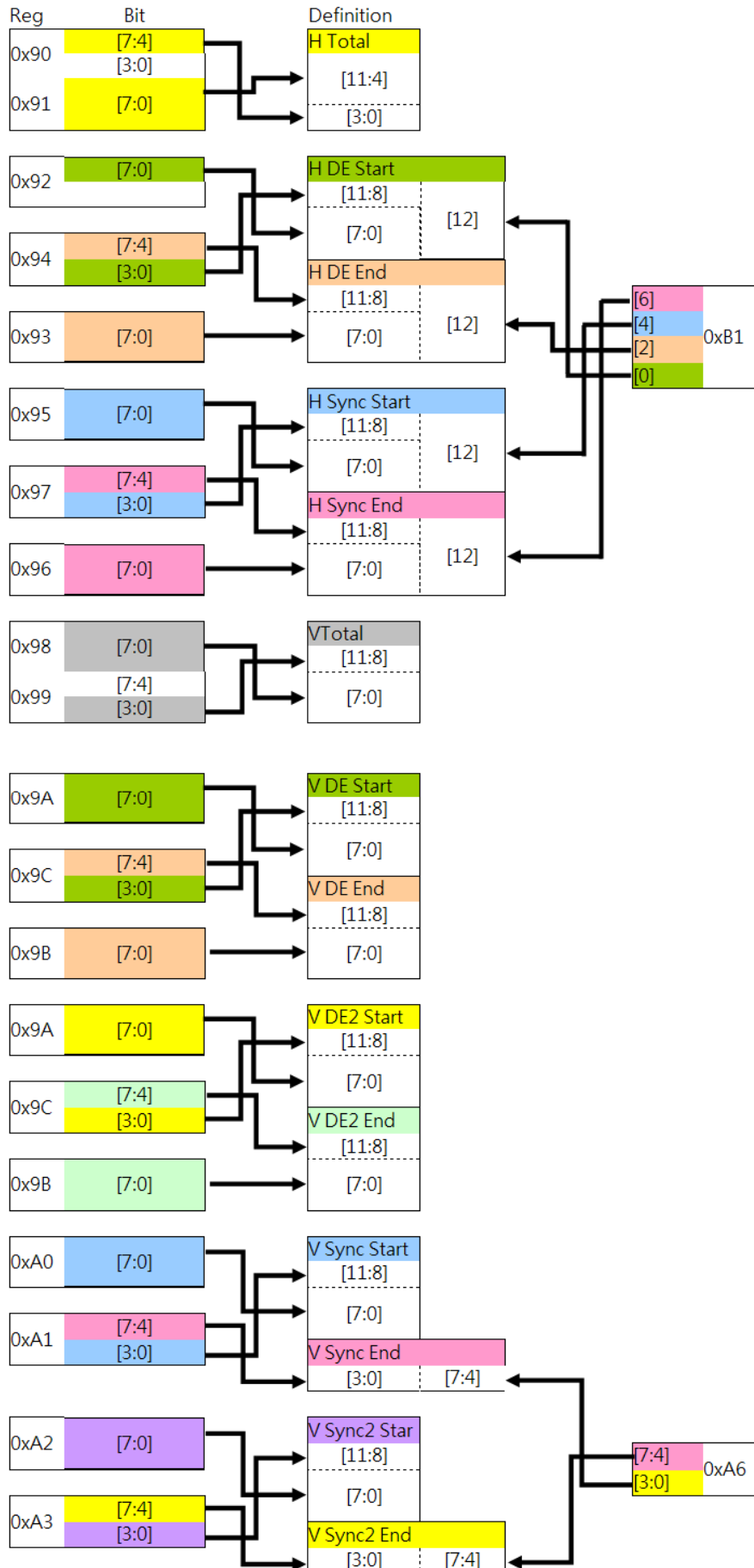
Pattern Generation /Sync/ DE Generation Registers

Reg	Register Name	bit	Definition	Default Value
<b>Pattern Sync/DE Generation Registers</b>				

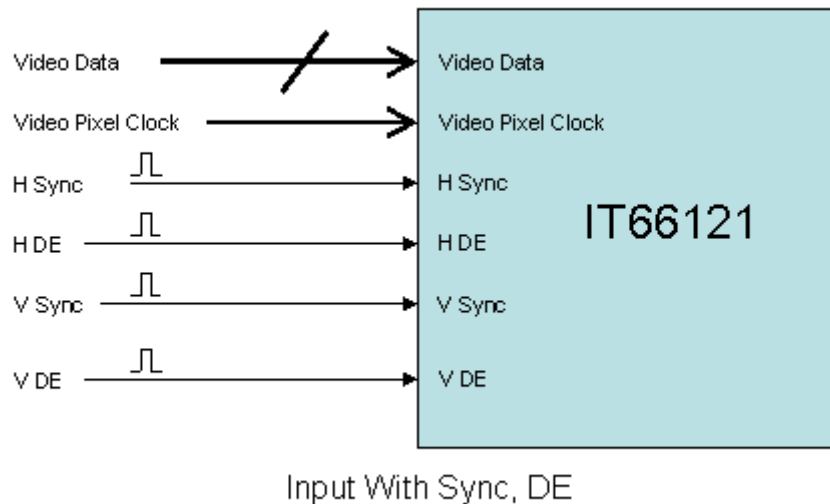
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90	Reg_PGHTotal[3:0]	7:4	PG Horizontal Total; See also Reg 0x91	00
	RegGenSync	3	Generate HSync VSync	0
	RegVSPol	2	Generated Vertical Sync Polarity	0
	RegHSPol	1	Generated Horizontal Sync Polarity	0
	Reg_GenDE	0	DE generation Enable	0
91	Reg_PGHTotal[11:4]	7:0	PG Horizontal Total	
92	Reg_PGHDES[7:0]	7:0	PG Horizontal Display Start; Low Byte.	H DE
93	Reg_PGHDEE[7:0]	7:0	PG Horizontal Display End; Low Byte.	
94	Reg_PGHDEE[11:8]	7:4	PG Horizontal Display End ; High Byte.	
	Reg_PGHDES[11:8]	3:0	PG Horizontal Display Start ; High Byte.	
95	Reg_PGHRS[7:0]	7:0	PG Horizontal Sync Start; Low Byte.	H Sync
96	Reg_PGHRE[7:0]	7:0	PG Horizontal Sync End; Low Byte.	
97	Reg_PGHRE[11:8]	7:4	PG Horizontal Sync End ; High Byte.	
	Reg_PGHRS[11:8]	3:0	PG Horizontal Sync Start ; High Byte.	
98	Reg_PGVTotal[7:0]	7:0	PG Vertical Total; Low Byte.	V Total
99	Reg_PGVTotal[10:8]	2:0	PG Vertical Total; High Byte.	
9A	Reg_PGVDES[7:0]	7:0	PG Vertical Display Start; Low Byte.	V DE
9B	Reg_PGVDEE[7:0]	7:0	PG Vertical Display End; Low Byte.	
9C	Reg_PGVDEE[10:8]	6:4	PG Vertical Display End; High Byte.	
	Reg_PGVDES[10:8]	2:0	PG Vertical Display Start; High Byte.	
9D	Reg_PGVDES2nd[7:0]	7:0	PG 2 <sup>nd</sup> Field Vertical Display Start; Low Byte.	V DE2
9E	Reg_PGVDEE2nd[7:0]	7:0	PG 2 <sup>nd</sup> Field Vertical Display End; Low Byte.	
9F	Reg_PGVDEE2nd[10:8]	6:4	PG 2 <sup>nd</sup> Field Vertical Display Start; High Byte.	
	Reg_PGVDES2nd[10:8]	2:0	PG 2 <sup>nd</sup> Field Vertical Display End; High Byte.	
A0	Reg_PGVRS[7:0]	7:0	PG Vertical Sync Start; Low Byte.	V Sync
A1	Reg_PGVRE[3:0]	7:4	PG Vertical Sync End	
	Reg_PGVRS[10:8]	2:0	PG Vertical Sync Start; High Byte.	
A2	Reg_PGVRS2nd[7:0]	7:0	PG 2 <sup>nd</sup> Field Vertical Sync Start; Low Byte.	V Sync2
A3	Reg_PGVRE2nd[3:0]	7:4	PG 2 <sup>nd</sup> Field Vertical Sync End	
	Reg_PGVRS2nd[10:8]	2:0	PG 2 <sup>nd</sup> Field Vertical Sync Start; High Byte.	
A6	Reg_PGVRE2nd[7:4]	7:4	PG 2 <sup>nd</sup> Field Vertical Sync End	[7:4]
	Reg_PGVRSnd[7:4]	3:0	PG Field Vertical Sync End	
B1	Reg_PGHRE[12]	6	PG Horizontal Sync End ; High Byte.	[12]
	Reg_PGHRS[12]	4	PG Horizontal Sync Start ; High Byte.	
	Reg_PGHDEE[12]	2	PG Horizontal Display End ; High Byte.	
	Reg_PGHDES[12]	0	PG Horizontal Display Start ; High Byte.	

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## Setting with Input Sync and DE



If video source provides horizontal/vertical sync and data enable (DE), IT66121 converts the input data directly to TMDS signals. When HDMI receiver received that, it converts the TMDS input to the original timing.

Therefore, if the input timing is not a standard timing of CEA861/B or VESA standard, CAT HDMI transmitter cannot convert them to a standard timing.

For this setting, Reg70[7:6] use the given setting of source output.

Reg70[4] = '0'

Reg70[3] = '0'

Reg90[3] = '0'

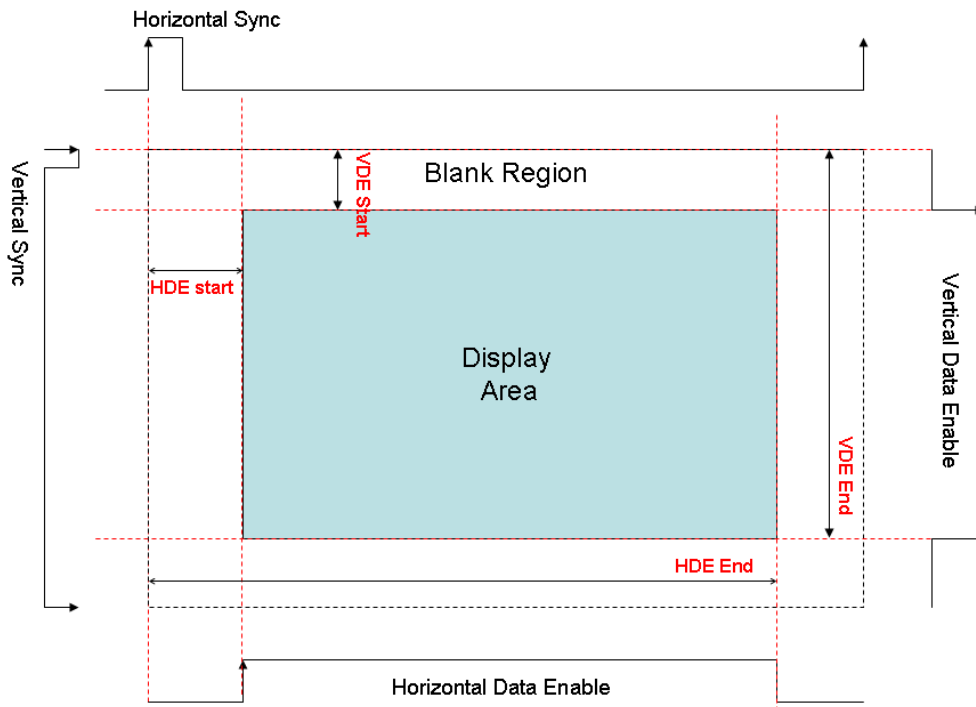
Reg90[0] = '0'

Reg70[2] refers to the input setting. If the input data are triggered by dual edge mode, set this bit as '1'; otherwise set as '0'.

## Setting Sync Embedded and DE Generating

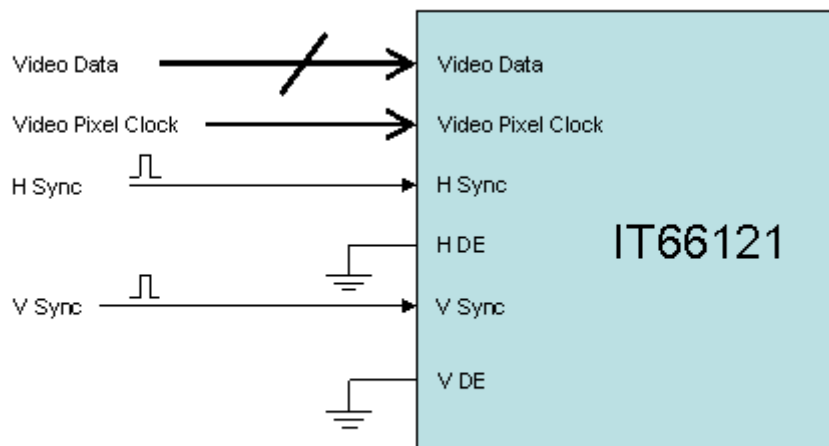
If the input signal do not include DE even though the sync is embedded, the output signal have to be programmed. If the timing generating registers are not programmed, the input video stable will not detected (reg0E[4]) and the output timing will be wrong.

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Video Timing Generating Parameter

## Generate DE with given horizontal sync and vertical sync



Input With Sync, No DE, DE should be generated by Sync Start Edge

Reg90[0] = '1' for DE Generating setting.

Reg90[3] = '0' for no sync gen.

PGHTotal[11:0] = don't care;

PGHDES[11:0] = HDE Start - 2 ;



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---

$PGHDEE[11:0] = HDE\ End - 2 = HActive + PGHDES ;$

$PGVTotal[11:0] = \text{don't care.}$

$PGVDES[10:0] = VDE\ Start - 1 ;$

$PGVDEE[10:0] = PGVDES + VActive = VDE\ End - 1 ;$

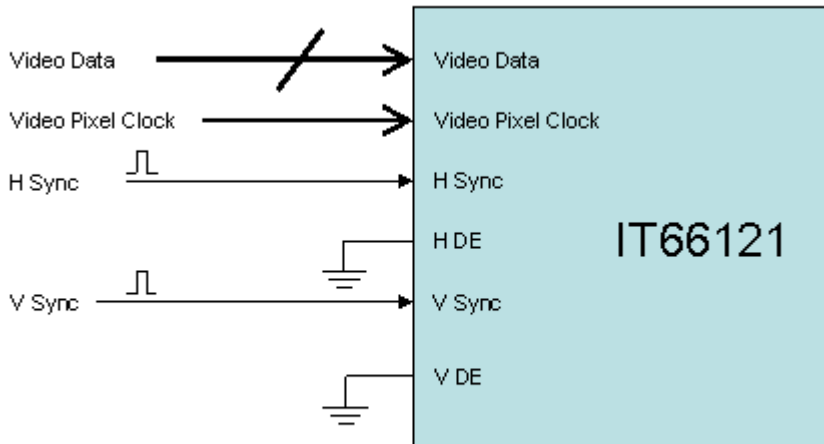
$PGVDES2[10:0] = VDE\ Start\ of\ field\ 2\ (from\ sync\ 1) - 1 ;$  (check the timing table)

If DE and Sync are both given, input is 24bit or 16bit,  $reg70=0xX0$ ,  $reg90[3][0] = '0' '0'$ , Timing Generation Registers are don't care.

If Sync are provided and DE is muxed in Data (CCIR656/CCIR601),  $reg70[3] = '1'$ ,  $reg90[3]$

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## Generate DE and Horizontal sync/Vertical sync with given sync



Input With Sync, No DE, DE should be generated by Sync Start Edge, And Sync should be regenerate to fit standard

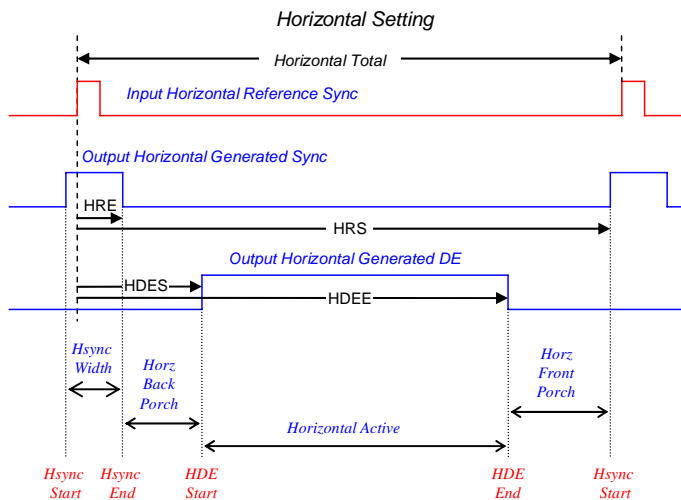
*(The timing parameter should be referred to CEA861/B or VESA detail timing sepc.)*

If under progressive mode,

$$PGHTotal = 0xFFF.$$

If under interlaced mode,

$$PGHTotal = HTotal/2 - 2.$$



This value is for the vertical starting setting of 2<sup>nd</sup> field.

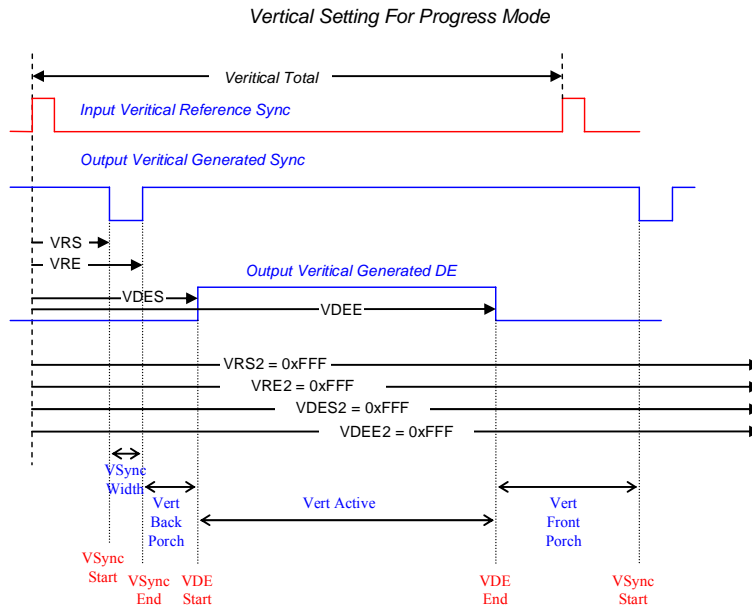
PGHRS = By Customer define (*Adjusting active video horizontal position*)

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PGHRE = PGHRS+HSYNC width

PGHDES = PGHRE +Horizontal Back Proch

PGHDEE = PGHDE Start+ Horizontal Clocks of Active video



*PGVTotal is not use*

PGVDES= PGVRS+ VSYNC width+ V Front Proch1

PGVDEE= PGVDES+ Active Vertical Line per field

PGVRS= By Customer define(*Adjust active video vertical Position*)

PGVRE=(PGVRS+ VSYNC width) % 16

If the mode is progress mode

PGVDES2=0xFFF

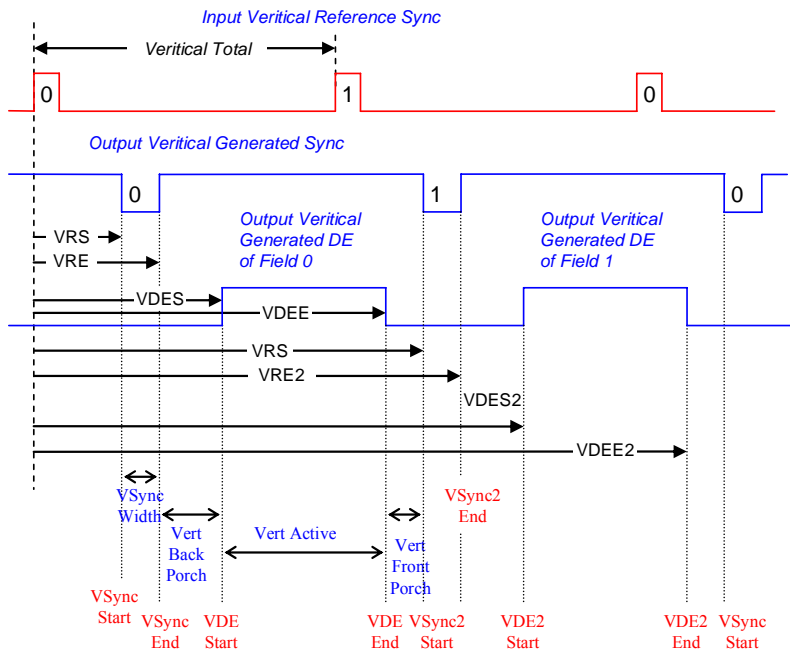
PGVDEE2=0xFFF

PGVRS2=0xFFF

PGVRE2=0xFFF

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## Vertical Setting For Interlaced Mode



If the mode is interlaced mode:

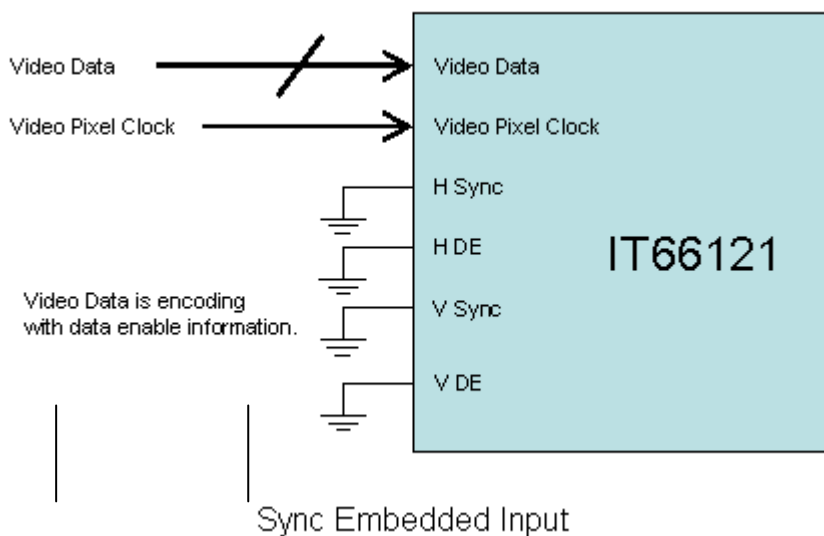
$PGVDES2 = PGVDEE + \text{field2 Vertical Blanking Lines}$

$PGVDEE2 = PGVDES2 + \text{Active Vertical Line per field}$

$PGVRS2 = PGVDES2 + V \text{ Front Proch2}$

$PGVRE2 = (PGVRS2 + VSYNC \text{ width}) \% 16$

## Sync Embedded for 16 bit Input



Timing need to generate horizontal sync start and horizontal sync end from horizontal DE embedded in

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input, and vertical sync start and end are generated by vertical DE too.

Reg70[3] = '1'

Reg90[3][0] = '0' '0'

$PGHTotal = HTotal/2 + FrontPorch - 2$  ;

$PGHRS = DEEnd\ to\ HSyncStart - 2 = FrontPorch - 2$

$PGHRE = DEEnd\ to\ HSyncStart - 2 = FrontPorch - 2$

$PGVRS = \text{scan line from VDE end to VSync Start} = VFrontPorch$

$PGVRE = \text{scan line from VDE end to VSync End} = VFrontPorch + VSync\ Width$

*For PGVRE is only 4 bit available, we just define the bit [10:4] use as the same value of PGVRS*

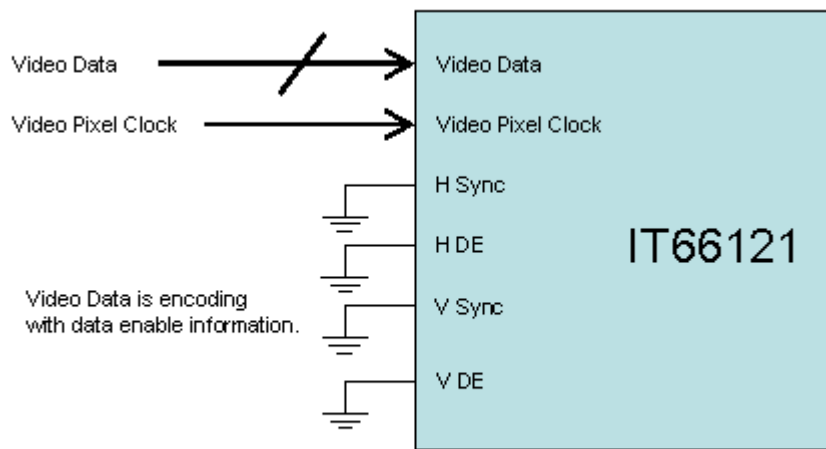
$PGVRS2 = \text{scan line from VDE end to VSync2 Start} = VFrontPorch + VTotal$

$PGVRE2 = \text{scan line from VDE end to VSync2 End} = VFrontPorch + VSyncEnd + VTotal$

*For PGVRE2 is only 4 bit available, we just define the bit [10:4] use as the same value of PGVRS2*

For VRS2 will check the field change for odd field, if the field is later than VSync2, VSync2 will be ignore. Then the VSync should be pushed later to avoid this issue but will produce timing not meet standard.

## Sync Embedded Mode With 8 bit (CCIR656) YCbCr422 Input



Sync Embedded Input

With CCIR656 input, video timing need to generate horizontal sync start and horizontal sync end from horizontal DE embedded in input, and vertical sync start and end are generated by vertical DE too. Because of the half bus using, the horizontal clock use twice count of the parameter to the sync embedded input with 16 bit, and the maximum input video clock can be up to 81MHz only because of the maximum DAC input of IT66121 is 162MHz.

Reg70[3] = '1'

Reg90[3][0] = '0' '0'

$PGHTotal = HTotal/2 + FrontPorch - 2$  ;

$PGHRS = 2*(DEEnd\ to\ HSyncStart - 2) + 1 = 2*(FrontPorch - 2) + 1$

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---

$PGHRE = 2 * (DEEnd\ to\ HSyncStart - 2) + 1 = 2 * (FrontPorch - 2) + 1$

$PGVRS = \text{scan line from VDE end to VSync Start} = VFrontPorch$

$PGVRE = \text{scan line from VDE end to VSync End} = VFrontPorch + VSync\ Width$

*For PGVRE is only 4 bit available, we just define the bit [10:4] use as the same value of PGVRS*

$PGVRS2 = \text{scan line from VDE end to VSync2 Start} = VFrontPorch + VTotal$

$PGVRE2 = \text{scan line from VDE end to VSync2 End} = VFrontPorch + VSyncEnd + VTotal$

*For PGVRE2 is only 4 bit available, we just define the bit [10:4] use as the same value of PGVRS2*

For VRS2 will check the field change for odd field, if the field is later than VSync2, VSync2 will be ignore. Then the VSync should be pushed later to avoid this issue but will produce timing not meet standard.

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The setting for necessary registers are listed below:

## Setting Color

Color Setting Registers are as following described:

Reg	Name	bit	Description	Default
70	Reg_InColMod[1:0]	7:6	00: RGB mode 01: YUV422 mode 10: YUV444 mode	00
	Reg_PCLKDiv2	5	0: IO clock = TxCLK 1: IO clk=1/2 *TxCLK	0
	Reg_2x656Clk	4	1: CCIR656 mode( YUV422, 8/12 bit mode) 0: non- CCIR656 mode	0
	Reg_SyncEmb	3	1: Sync Embedded mode 0: Sync Sep mode	0
	Reg_InDDR	2	1: Input DDR 0: Input SDR	0
72	Reg_EnDither	7	Enable dither function	0
	Reg_EnUdFilt	6	Enable Cr/CB up/down sampling function	0
	Reg_DNFreeGo	5	Dither Noise Pattern	0
	Reg_CSCSel[1:0]	1:0	00 : No color space conversion. 10: RGB to YUV 11: YUV to RGB	00
<b>Color Space Conversion</b>				
73	Reg_YoffSet	7:0	Y blank level	0x10
74	Reg_CoffSet[7:0]	7:0	C blank level	0x80
75	Reg_RGBOffSet[7:0]	7:0	R/G/B blank level	0x00
76	Reg_Matrix11V[7:0]	7:0	Color space conversion Matrix	
77	Reg_Matrix11V[13:8]	4:0		
78	Reg_Matrix12V[7:0]	7:0	Color space conversion Matrix	
79	Reg_Matrix12V[13:8]	5:0		
7A	Reg_Matrix13V[7:0]	7:0	Color space conversion Matrix	
7B	Reg_Matrix13V[13:8]	5:0		
7C	Reg_Matrix21V[7:0]	7:0	Color space conversion Matrix	
7D	Reg_Matrix21V[13:8]	5:0		
7E	Reg_Matrix22V[7:0]	7:0	Color space conversion Matrix	
7F	Reg_Matrix22V[13:8]	5:0		
80	Reg_Matrix23V[7:0]	7:0	Color space conversion Matrix	
81	Reg_Matrix23V[13:8]	5:0		
82	Reg_Matrix31V[7:0]	7:0	Color space conversion Matrix	
83	Reg_Matrix31V[13:8]	5:0		
84	Reg_Matrix32V[7:0]	7:0	Color space conversion Matrix	
85	Reg_Matrix32V[13:8]	5:0		
86	Reg_Matrix33V[7:0]	7:0	Color space conversion Matrix	
87	Reg_Matrix33V[13:8]	5:0		
<b>Output Color Mode in AVI Infoframe</b>				
158	REGPktAVIInfoV[1:0]	6:5	Output Color Mode '00' – RGB444 mode '01' – YCbCr422 mode '10' – YCbCr444 mode	
	REGPktAVIInfoA	4		
	REGPktAVIInfoB[1:0]	3:2		
	REGPktAVIInfoS[1:0]	1:0		

To program color setting of IT66121, software should set

1. Program the input color mode (depends on the input signal type).
2. Program the output color mode setting , in AVI Infoframe Y field (reg158[6:5]), even though the output is under DVI mode (have to set as RGB444 mode).
3. Program the color converting matrix.

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Color space converting table

		RGB to YUV				YUV to RGB			
		RGB to YUV 601		RGB to YUV 709		YUV to RGB 601		YUV to RGB 709	
	reg	16~ 235	0 ~ 255	16~ 235	0 ~ 255	16~ 235	0 ~ 255	16~ 235	0 ~ 255
Reg_CSCSel[1:0]	72[1:0]	10	10	10	10	11	11	11	11
Reg_YoffSet[7:0]	73	0x00	0x10	0x00	0x10	0x00	0x04	0x00	0x04
Reg_CoffSet[7:0]	74	0x80	0x80	0x80	0x80	0x00	0x00	0x00	0x00
Reg_RGBOffset[7:0]	75	0x10	0x10	0x10	0x10	0x00	0xA7	0x00	0xA7
Reg_Matrix11V[13:0]	76	0xB2	0x09	0xB8	0xE4	0x00	0x4F	0x00	0x4F
	77	0x04	0x04	0x05	0x04	0x08	0x09	0x08	0x09
Reg_Matrix12V[13:0]	78	0x65	0x0E	0xB4	0x77	0x6B	0x81	0x55	0xBA
	79	0x02	0x02	0x01	0x01	0x3A	0x39	0x3C	0x3B
Reg_Matrix13V[13:0]	7A	0xE9	0xC9	0x94	0x7F	0x50	0xDD	0x88	0x4B
	7B	0x00	0x00	0x00	0x00	0x3D	0x3C	0x3E	0x3E
Reg_Matrix21V[13:0]	7C	0x93	0x0F	0x4A	0xD0	0x00	0x4F	0x00	0x4F
	7D	0x3C	0x3D	0x3C	0x3C	0x08	0x09	0x08	0x09
Reg_Matrix22V[13:0]	7E	0x18	0x84	0x17	0x83	0xF5	0xC4	0x51	0x57
	7F	0x04	0x03	0x04	0x03	0x0A	0x0C	0x0C	0x0E
Reg_Matrix23V[13:0]	80	0x55	0x6D	0x9F	0xAD	0x02	0x01	0x00	0x02
	81	0x3F	0x3F	0x3F	0x3F	0x00	0x00	0x00	0x00
Reg_Matrix31V[13:0]	82	0x49	0xAB	0xD9	0x4B	0x00	0x4F	0x00	0x4F
	83	0x3D	0x3D	0x3C	0x3D	0x08	0x09	0x08	0x09
Reg_Matrix32V[13:0]	84	0x9F	0xD1	0x10	0x32	0xFD	0xFD	0x00	0xFE
	85	0x3E	0x3E	0x3F	0x3F	0x3F	0x3F	0x00	0x3F
Reg_Matrix33V[13:0]	86	0x18	0x84	0x17	0x84	0xDA	0x1F	0x84	0xE8
	87	0x04	0x03	0x04	0x03	0x0D	0x10	0x0E	0x10

Following then above table, depends on the input and output color relationship, program the value into the reg72~reg87 for converting the color table, the color mode is OK.



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## Analog Front End

IT66121 output signal setting is on reg61~reg65. The setting depends on the output TMDS clock frequency. The setting are as following table.

Reg	Register Name	bit	Definition	Default Value
61		7:6		0
	REG_DRV_PWD	5	Reset signal for HDMI_TX_DRV. '1' all flip-flops in the transmitter are reset while all other analog parts are powered off.	0
	REG_DRV_RST	4	Reset signal for HDMI_TX_DRV. '1': all flip-flops in the transmitter, including those in the BIST pattern generator, are reset.	1
		3		
	REG_DRV_PDRXDET	2	0: Normal operation 1: Power down monitor sense (RX detection) circuits	0
	REG_DRV_TERMON	1	Reserved, this bit must be 0 for normal operation. 0: transmitter termination resistors are disabled 1: transmitter termination resistors are enabled	0
		0		0
62	REG_XP_GAINBIT	7	Video frequency band selection For video clock frequency < 80Mhz, set to '0', otherwise set to '1'.	1
	REG_XP_PWDPLL	6	Power down signal for TMDSTXPLL018C When '0', normal operation When '1', TMDSTXPLL018C is powerdowned	0
	REG_XP_ENI	5	When '1', the charge pump current of TMDSTIPLL018 is increased.	0
	REG_XP_ERO	4	Adjust filter parameters of TMDSTXPLL018C When '0', base filter resistance value(>80Mhz) When '1', increased filter resistance value(<80Mhz) ** If XP_GAINBIT_LV = '0', XP_ERO_LV should be set to '1'	0
	REG_XP_RESETB	3	Low-active reset signal for TMDSTXPLL018C When '0', TMDSTXPLL018C is reset. When '1', normal operation	1
	REG_XP_PWDI	2	Decides whether the output bias currents provided by TMDSTXPLL018C to other analog blocks are power-downed (turned off) or not. When '0', output bias currents are not turned off even if XP_PWDPLL_LV is asserted. When '1', output bias currents are unconditionally turned off, which at the same time renders the VCO inoperable (CAUTION!!)	0
	REG_XP_DEI	1	When '1', charge pump current of TMDSTXPLL018C is decreased.	0
	REG_XP_BYPASS	0	Selecting the reference clock for TMDSTXPLL018C. When '1', input clock from logic core PCLKIN_LV will be selected — i.e. un-filtered mode. When '0', a filtered clock generated by TMDSIPLL018 (internal node name PCLKIV) will be selected — i.e. filtered mode. <b>For CAT6611, this bit should be zero.</b> <b>For CAT6612, this bit should be '1'.</b>	0
63	<del>REG_RTERM_SEL</del>	7		<del>0</del>
	REG_IP_BYPASS	6	Only used in testing mode 1: bypass PCLKIN to PCLK, IP_VCLK, CLK_SYS. All other PLL function normally.	0
	REG_DRV_ISW	5:3	Output current level setting <011: lower swing 011: default swing >011: higher swing	011
	REG_DRV_ISWK	2:0		000
64	REG_IP_GAINBIT	7	Video frequency band selection For video clock frequency < 80Mhz, set to '0', otherwise set to '1'.	1
	REG_IP_PWDPLL	6	Powerdown signal for TMDSIPLL018 When '0', normal operation When '1', TMDSIPLL018 is powerdowned	0

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	REG_IP_CKSEL	5:4	When IP_GAINBIT = 0 (<80MHz) 00: PCLK (IP_VCLK) = 0.5*VCO 01: PCLK (IP_VCLK) = 1*VCO 10: PCLK (IP_VCLK) = 2*VCO 11: PCLK (IP_VCLK) = 4*VCO When IP_GAINBIT = 1 (>80MHz) 00: PCLK (IP_VCLK) = 0.5*VCO 01: PCLK (IP_VCLK) = 1*VCO 10: PCLK (IP_VCLK) = 2*VCO 11: PCLK (IP_VCLK) = 2*VCO	01
	REG_IP_ER0	3	Adjust filter parameters of TMDSIPLL018 When '0', base filter resistance value(>80Mhz) When '1', increased filter resistance value(<80Mhz) ** If IP_GAINBIT_LV = '0', IP_ER0_LV should be set to '1'	0
	REG_IP_RESETB	2	Low-active reset signal for TMDSIPLL018 When '0', TMDSIPLL018 is reset. When '1', normal operation	1
	REG_IP_ENC	1	1: Larger filter parallel capacitance 0: Normal condition	0
	REG_IP_EC1	0	Adjust filter parameters of TMDSIPLL18VA0 0: when PCLKIN>80MHz 1: when PCLKIN<80MHz	0
65				
	REG_RING_SLOW	1	Set RING_SLOW_LV=1 to speed up the frequency of RING_CK_LV	0
	REG_RING_FAST	0	Set RING_FAST_LV = '1' to slow down the frequency of RING_CK_LV	0
66	REG_AFE_ENTEST	6	1: Enable testing mode for both PLLs.(WP) 0: Normal operation	0
	REG_AFE_ENBIST	5	1: Enable AFE BIST function, used for test only.(WP) 0: Normal operation	0
67	REGAFELFSRVal	7	BIST shifter flip-flops initial value (WP)	0
	REGDisAFELFSR	6	1: BIST shifter disable (WP) 67 0: BIST shifter enable.	0
68	REG_XP_EC1	4	0: when output TMDS clock frequency >80MHz 1: when output TMDS clock frequency <80MHz	0

Sample code :

```
switch(level)//SetupAFE
{
    case PCLK_HIGH:// (>80Mhz)
        HDMITX_set(0x62, 0x90, 0x80);//[7]、[4]
        HDMITX_set(0x64, 0x89, 0x80);//[7]、[3]、[1]
        HDMITX_set(0x68, 0x10, 0x80);//[4]
        break ;
    default:
        HDMITX_set(0x62, 0x90, 0x10); //[7]、[4]
        HDMITX_set(0x64, 0x89, 0x09); //[7]、[3]、[1]
        HDMITX_set(0x68, 0x10, 0x10); //[4]
        break ;
}
```

HDMITX\_WriteI2C\_Byte(0x61,0);//FireAFE

## DVI HDMI Mode

IT66121 HDMI mode setting is in regC0, all HDMI packet and audio can only run under HDMI mode (regC0 = '1').

If set regC0 = '0', it is DVI mode.

Reg	Register Name	bit	Definition	Default Value
C0	REGHDMIMode	0	Set TX Mode '0': DVI mode '1': HDMI mode	0

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## Mute

When regC1[0] = '1', IT66121 send blank screen, with (black screen under regC1[1] = '0' or blue screen under regC1[1] = '1').

Under HDMI mode (regC0[0] = '1'), AVMute should set in general control package (GCP), the general control package have to be programmed. If regC6[1:0] = '11', the general control package will be enabled and sent repeating. The AVMute and color depth function contained in GCP will send with the setting of regC6.

Reg	Register Name	bit	Definition	Default Value
C1	REGAVMute	0	Set AVMute '0': not AVMute '1': AVMute	1
	REGBlueScrMute	1	Set Blue screen output when AVMute='1'	0
C6	REGPktGenCtrlRpt	1	Repeat General Control packet '0': send once '1': one for each field	0
	REGPktGenCtrlEn	0	Enable General Control packet '0': disable '1': enable	0

## Video Pixel Repetition

AVI Packet				
reg	Name	bit	Definition	Default Value
15C	REGPktAVIInfoPR[3:0]	3:0	0000 – 1X (no repetition) 0001 – 2X (one repetition) 0011 – 4X otherwise – no define	0x0

In HDMI and CEA861/D, there is pixel repetition defined in AVI Infoframe databyte[5][3:0]. IT66121 implement hardware repetition in AVI Infoframe databyte[5]. If the source video signal is the original timing (for example, 480i with 720x480i@60Hz with 13.5MHz), to write Infoframe is OK.

## Invert Video Data Latch Edge

The quality of video need the data latch edge setting depends on the PCB layout. The video data latch edge setting is in reg59[3].

reg	Name	bit	Definition	Default Value
59	REGManualPLLPR	7:6	VCLK frequency depends on REGManualPLLPR when REGDisLockPR='1' 00: 1x 01: 2x 11: 4x	0
	REGENTxCnt	5	Enable TxCLK to count REFCLK '1': enable '0': disable	0
	REGDisLockPR	4	'1' – Pixel repetition refer to the setting in reg59[7:6]. '0' – Pixel repetition refer to th setting oin reg15C[1:0]	0
	REGVidLatEdge	3	Video Data Latch Edge	0
	REGAudDiv	1:0	Audio down-sampling selection "00" : no down-sampling "01" : divided by 2 "10" : no defined "11" : divided by 4	0x0

## Sequence

For all the video timing setting, all necessary setting include the AVMUTE should be set before the assignment of reg61← 0x00, then all the setting could be applied.

## Chap 7 Program Audio Mode

When HDMI video mode is ready and the TMDS clock is higher than 27MHz, the audio of IT66121 can be enabled.

To enable audio, regE0[3:0] should be set to zero at first, then enable audio reference clock (reg04[4] = '0') and audio FIFO (reg04[2] = '0'). Then program the audio clock recovery, audio format register (except audio channel enable), audio channel status, then enable audio channel enable while input clock stable (if SPDIF).

### IEC60958 Programming

This section describes the general setting of IT66121 audio. The sequence to program the audio should following the steps:

1. Disable audio channel with regE0[3:0] = '0000'.
2. Enable audio reference clock and audio FIFO with reg04[4][2] = '0' '0'
3. Depends on the audio sample clock and TMDS clock, [program the N/CTS](#).
4. Program audio format in regE0[7:4], and regE1~regE5.
5. Program audio channel status if not refer the S/PDIF channel status (when regE3[4] = '0').
6. If the audio sample frequency provided by system is not reliable, count the correct audio frequency with auto generated CTS and the formula between N and CTS, and set the N and channel status by detected value while reg5F[5] = '1'.
7. If input is from I2S, regE0[3:0] = 'xxx1' depends on audio source number.
8. If input is from SPDIF, regE0[3:0] = '0001' when reg5F[5] = '1'.

IT66121 only provide two channel audio.

### Audio Clock Recovery (N/CTS)

IT66121 provides the auto generating clock time stamp (CTS) mechanism with regC5[0] = '0'.

Reg	Register Name	bit	Definition	Default Value
C5	REGPktAudNCTSSel	1	Audio CTS selection '0': hardware auto count '1': user defined	0
	REGSinglePkt	0	Single Packet mode '0': burst packet mode '1': signal packet mode	0

#### CTS/N registers

N/CTS Packet				
reg	Name	bit	Definition	Default Value
130	REGPktAudCTS[7:0]	7:0		
131	REGPktAudCTS[15:8]	7:0		
132	REGPktAudCTS[19:16]	3:0		
133	REGPktAudN[7:0]	7:0		0x80
134	REGPktAudN[15:8]	7:0		0x18
135	REGPktAudN[19:16]	3:0		0x0
1A0	REGPktAudCTSCnt[7:0]	7:0	Read Only	
1A1	REGPktAudCTSCnt[15:8]	7:0	Read Only	
1A2	REGPktAudCTSCnt[19:16]	3:0	Read Only	

Usually, the CTS do not need to program, when software provide 20bit N value, IT66121 automatically generates the CTS depends the formula:

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$$(CTS_{average}) = (TMDS\_Clock \times N) / (128 \times Fs)$$

Where  $F_s$  is the input audio sample frequency, and  $TMDS\_Clock$  is the clock of TMDS including the pixel repetition and deep color ratio. For example, in 1440×480i@24bit mode, the TMDS clock is  $13.5MHz \times 2 = 27MHz$ ; and for 1080p60@36bit mode, the TMDS clock is  $148.5MHz \times 36/24 = 222.75MHz$ .

If the audio sample frequency is undetermined, software can provide a default N value (such as 0x1880), while the audio clock is locked, the follow the readback CTS and TMDS clock to count the actually  $F_s$ , then set the N with suggested value as following rule:

$$128 \times Fs / 1500Hz \leq N \leq 128 \times Fs / 300Hz,$$

therefore, a recommended optimal value of N comes by

$$N = 128 \times Fs / 1000Hz$$

Recommended N and CTS are as following table:

TMDS Clock(MHz)	32KHz	
	N	CTS
25.2/1.001	4576	28125
25.2	4096	25200
27	4096	27000
27×1.001	4096	27027
54	4096	54000
54×1.001	4096	54054
74.25/1.001	11648	210937-210938
74.25	4096	74250
148.5/1.001	11648	421850
148.5	4096	148500
Other	4096	Measure

Recommended N and CTS for 44.1KHz and Multiples

TMDS Clock(MHz)	44.1KHz		88.2KHz		176.4KHz	
	N	CTS	N	CTS	N	CTS
25.2/1.001	7007	31250	14014	31250	28028	31250
25.2	6272	28000	12544	28000	25088	28000
27	6272	30000	12544	30000	25088	30000
27×1.001	6272	30030	12544	30030	25088	30030
54	6272	60000	12544	60000	25088	60000
54×1.001	6272	60060	12544	60060	25088	60060
74.25/1.001	17836	234375	35672	234375	71344	234375
74.25	6272	82500	12544	82500	25088	82500
148.5/1.001	8918	234375	17836	234375	35672	234375
148.5	6272	165000	12544	165000	25088	165000
Other	6272	Measured	12544	Measured	25088	Measured

Recommended N and CTS for 48KHz and Multiples

TMDS Clock(MHz)	48KHz		96KHz		192KHz	
	N	CTS	N	CTS	N	CTS
25.2/1.001	6864	28125	13728	28125	27456	28125
25.2	6144	25200	12288	25200	24576	25200
27	6144	27000	12288	27000	24576	27000
27×1.001	6144	27027	12288	27027	24576	27027
54	6144	54000	12288	54000	24576	54000
54×1.001	6144	54054	12288	54054	24576	54054
74.25/1.001	11648	140625	23296	140625	23296	140625
74.25	6144	74250	12288	74250	24576	74250
148.5/1.001	5824	140625	11648	140625	23296	140625
148.5	6144	148500	12288	148500	24576	148500

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Other	6144 Measured	12288 Measured	24576 Measured
-------	---------------	----------------	----------------

CTS will be automatically generated by `regC5[1] = '0'`. Therefore, the N value on the table above should be assigned only. However, sometime the CTS should be assigned manually. Write the CTS register, and write `regC5` with the sequence:

`regF8 = 0xC3`

`regF8 = 0xA5` // the password register is enabled and write protection is disabled.

`regC5[1] = '1'`

`regF8 = 0xFF` // enabling the write protection of `regC5`.

## Audio Format

IT66121 programs linear pulse code modulation (LPCM) audio in registers `regE0~regE5`.

Audio format register definition

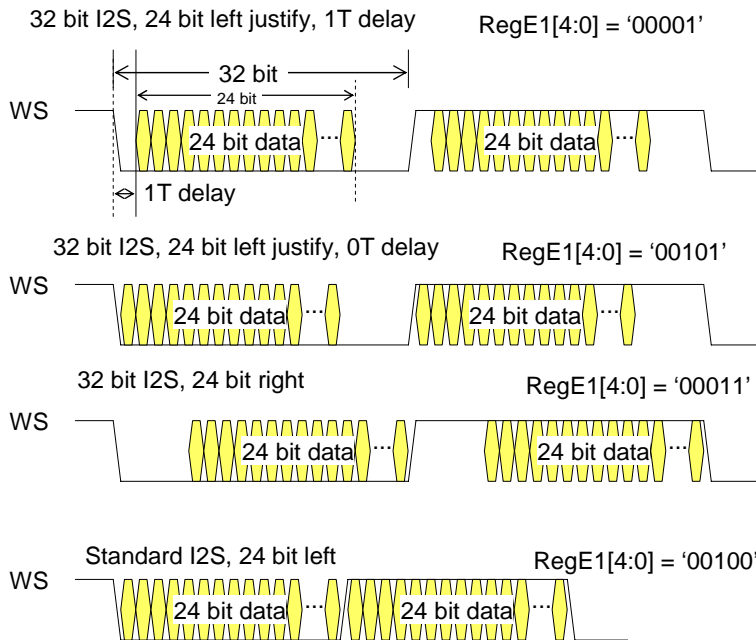
Reg	Register Name	bit	Definition	Default Value
E0	REGAudSWL[1:0]	7:6	00: 16 bits 01: 18 bits 10: 20 bits 11: 24 bits	11
	REGSPDIFTC	5		0
	REGAudSel	4	0: I2S 1: SPDIF	0
	REGAudioEn[3:0]	3:0	Enable Audio Source [0] for audio source 0 [1] for audio source 1 [2] for audio source 2 [3] for audio source 3 '0': disable '1': enable	0
E1	REGAudFullPkt	6	Enable audio full packet mode '0': not full packet mode '1': full packet mode	1
	REGAudLatEdge	5	0: use rising edge to sample WS and I2S 1: use falling edge to sample WS and I2S	0
	REGAudFmt[4:0]	[4:0]	REGAudFmt[0] 0: Standard I2S 1: 32-bit I2S REGAudFmt[1] 0: Left-justified 1: Right-justified REGAudFmt[2] 0: Data delay 1T correspond to WS 1: No data delay correspond to WS REGAudFmt[3] 0: WS='0' is left channel 1: WS='0' is right channel REGAudFmt[4] 0: MSB shift first 1: LSB shift first	0x01
E2	REGFifo3Sel[1:0]	7:6	Audio FIFO 3 source selection "00": from audio source 0 "01": from audio source 1 "10": from audio source 2 "11": from audio source 3	11
	REGFifo2Sel[1:0]	5:4	Audio FIFO 2 source selection "00": from audio source 0 "01": from audio source 1 "10": from audio source 2 "11": from audio source 3	10

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	REGFifo1Sel[1:0]	3:2	Audio FIFO 1 source selection "00": from audio source 0 "01": from audio source 1 "10": from audio source 2 "11": from audio source 3	01
	REGFifo0Sel[1:0]	1:0	Audio FIFO 0 source selection "00": from audio source 0 "01": from audio source 1 "10": from audio source 2 "11": from audio source 3	00
E3	REGAudMulCh	7	Read only. Depends on REGPktAudEn	
	REGPktZeroCTS	6	Enable zero CTS value '0': disable '1': enable	0
	REGChStSel	4	Channel status selection '0': from user defined '1': from SPDIF interface	0
	REGS3RLChg	3	Audio source 3 R/L swap '1': swap R/L channel '0': not swap R/L channel	0
	REGS2RLChg	2	Audio source 2 R/L swap '1': swap R/L channel '0': not swap R/L channel	0
	REGS1RLChg	1	Audio source 1 R/L swap '1': swap R/L channel '0': not swap R/L channel	0
	REGS0RLChg	0	Audio source 0 R/L swap '1': swap R/L channel '0': not swap R/L channel	0
E4	REGAudSPxFlat[3:0]	[7:4]	User defined audio flat bit [0] for source 0 [1] for source 1 [2] for source 2 [3] for source 3	0x0
	REGAudErr2Flat	[3]	Auto audio error to flat setting '0': disable '1': enable	1
	REGAudS3Valid	[2]	Validity bit for source 3 '0': reliable '1': not reliable	0
	REGAudS2Valid	[1]	Validity bit for source 2 '0': reliable '1': not reliable	0
	REGAudS1Valid	[0]	Validity bit for source 1 '0': reliable '1': not reliable	0

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Audio format set on I2S sampling, as the following figure:



IT66121 supports audio with up to four sources (eight channels), and sample word length with maximum 24bits (16/18/20/24 bits). There are two input types of audio source interface, I2S or S/PDIF. If audio come from the I2S,  $\text{regE0}[4]$  should set as zero and  $\text{regE0}[3:0]$  should set with corresponding sources. The word length of audio sample should set in  $\text{regE0}[7:4]$ . If the source interface is S/PDIF,  $\text{regE0}[4]$  should be '1' and  $\text{regE0}[3:0] = '0001'$ . Under S/PDIF interface, audio channel enable should be enabled after audio clock locked by  $\text{reg5F}[5] = '1'$ . If using I2S interface, don't care the bit but only enable the audio channel.

Reg	Register Name	bit	Definition	Default Value
5F	IP_LOCK	7	R.	
	XP_LOCK	6	R.	
	OSFreqLock	5	R.	
	TxCLKCnt[11:8]	3:0	R. Ring OSC counter read back.	

For LPCM audio,  $\text{regE1} = 0x01$  while audio source is only one and  $\text{regE1} = 0x41$  when audio source number is larger or equal to two.

$\text{RegE2}$  defined the mapping between input audio sources and output HDMI audio sample sources. As described in the table, usually set as  $0xE4$ .

$\text{RegE3}[3:0]$  defines the channel swapping, for each audio source, the corresponding bit defined if the right and left channel swapping.

$\text{RegE3}[4]$  is only using under S/PDIF interface. If the input audio source is not in LPCM format, our audio channel status cannot set the related information but can refer the original holding channel status in the digital interface. If  $\text{regE3}[4] = '1'$ , the channel status in  $\text{reg191} \sim \text{reg198}$  will be ignored and refer to the original channel status of S/PDIF input.

$\text{RegE4}[7:4]$  defined the flat bit of audio. While corresponding bit is set to '1', the audio source will become flat (as mute).

$\text{RegE5}$  and  $\text{regE6}$  should be zero.



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## Audio Channel Status

We support IEC60958 channel status in reg191~reg198. As following table, the corresponding bit is defined in IEC60958-3 spec. Filled the registers with correct audio source number, sample frequency, audio sample word length, and the other information.

Audio Channel Status				
Reg	Name	bit	Definition	Default Value
191	REGAudChStD[2:0]	6:4	IEC60958-3 p9 bit[5:3] Additional format information depends on linear PCM audio mode: 5 4 3 ----- 000: 2 audio channels without pre-emphasis. 001: 2 audio channels with 50 μs/15 μs pre-emphasis. 010: reserved 011: reserved All other combination are reserved and shall not be used until further defined.	
	REGAudChStC	3	refer to IEC60958-3 p9 bit[2] 0: Software for which copyright is asserted. 1: Software for which no copyright is asserted.	
	REGAudNLPCM	2	refer to IEC60958-3 p9 bit[1] 1: None-PCM setting. 0: for I2S setting.	0
	REGAudMono	0	Monochrome bit 1: if there is only one audio source	0
192	REGAudChStCat	7:0	Audio category code groups. Refer to <i>IEC60958-3 5.3.2</i> channel status byte 2 (bit 15-8)	
193	REGAudChStSrc	3:0	refer to <i>IEC60958-3 p11 bit 16-19</i> Source number, 0~15, 0 means don't take number into account.	
194	REGAudChStCH	3:0	refer to <i>IEC60958-3 p11 bit 23-20</i> single and dual channel operating modes are defined in <i>IEC60958-1</i> Channel number of source 0 L-channel	
198	REGAudChStCA	7:4	refer to <i>IEC60958 p12 bit 29~28</i> Clock accuracy 00 Level II 01 Level I 10 Level III 11 Interface frame rate not matched to sampling frequency.	
	REGAudChStFs	3:0	Sample frequency indicated in <i>IEC60958-3 p11 bit 24~27</i> . Sample frequency of software indicated 27..24 ----- 0000 44.1 KHz 1000 88.2 KHz 1100 176.4 KHz  0110 24 Khz 0010 48Khz 1010 96Khz 1110 192KHz  0011 32KHz 0000 sampling frequency not indicated.	0x0

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199	REGAudChStOfs	7:4	Sample frequency indicated in <i>IEC60958-3 p11 bit 24~27</i> . Original Sampling Frequency 27..24 ----- 1111 44.1 KHz 0111 88.2 KHz 0011 176.4 KHz  1001 24 KHz 1101 48KHz 0101 96KHz 0001 192KHz 1100 32KHz 0000 sampling frequency not indicated.	
	REGAudChStWL	3:0	Audio sample word length 1101 21 bits 1011 24 bit 1001 23 bit 0101 22 bit 0011 20 bit 0001 Word length not indicated 1100 17 bit 1010 20 bit 1000 19 bit 0100 18 bit 0010 16 bit 0000 Word length not indicated	

If the input audio from SPDIF is not an LPCM format, reg191[2] should be set to '1', whenever the channel status is from SPDIF internal (regE3[4] = '1') or not.

## Chap 8 Activate HDCP

IT66121 supports high-bandwidth digital content protection (HDCP) with Tx format.

### Initial HDCP of IT66121

For enabling the HDCP function of IT66121, please program the registers by the following sequence:

regF8 <- 0xC3

regF8 <- 0xA5

reg20[7] <- '1'

reg37[0] <- '0'

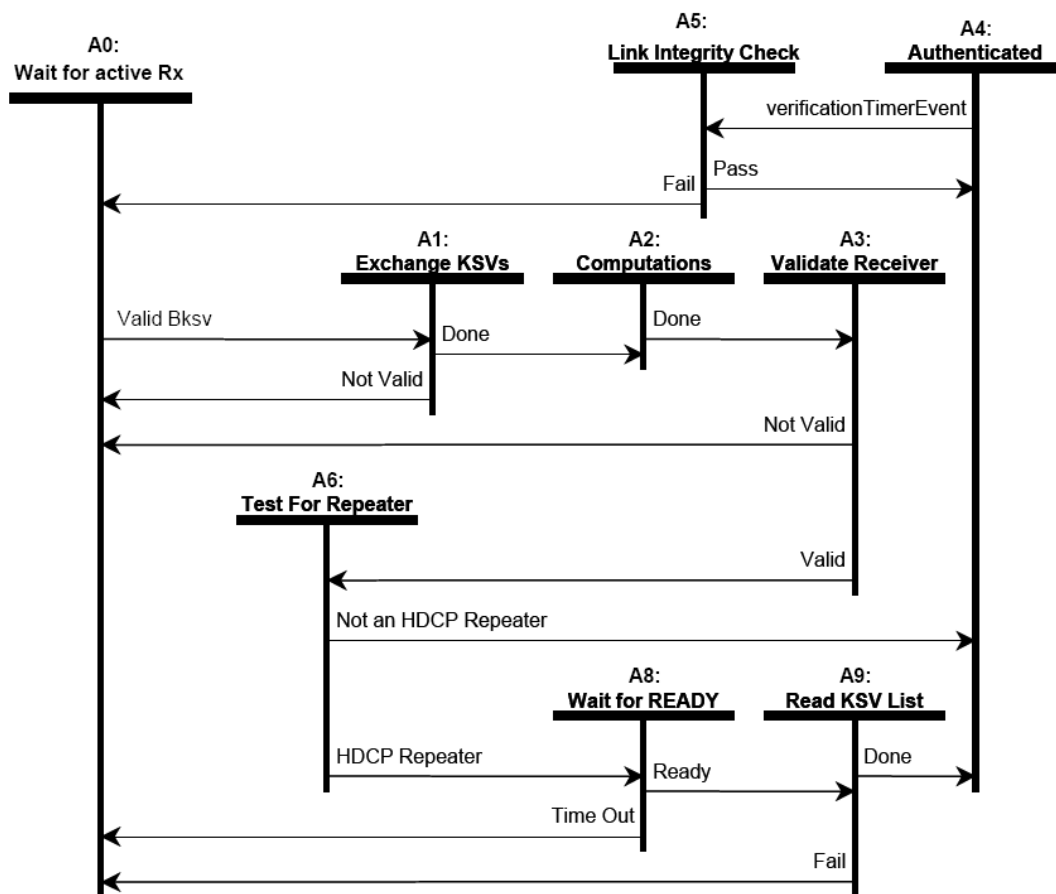
reg20[7] <- '0'

regF8 <- 0xFF

If register reset (reg04[5]) was programmed, it need to set again.

### HDCP State Transition

The state transition diagram is as the following figure:



**HDCP Transmitter Authentication Protocol State Diagram**

The transition from A0 to A4 and A9 to A4 are done by hardware functions, and repeater KSV List

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checking is implement by software. They are described in following.

## HDCP Progress

Following registers are for HDCP programming.

Reg	Register Name	Bit	Definition	Default Value
1F	Reg_AnGen	0	Write this bit '1' to enable Cipher Hardware generating a random number. Write '0' to stop the Cipher Hardware. The generated Random number can be read back from register 30~37	0
20	REGAEnable1p1Feature	1	Enable HDMI Tx HDCP1.1 Feature	0
	REGCPDesired	0	'1' to enable HDCP	0
21	Rauthen_Fire	7:0	Write '1' to stare HDCP authentication process	X
22	REGList_Fail	1	Write this bit when process KSVList Check interrupt Routine. 1: HDCP Authentication FSM will return to wait and try state.	0
	REGList_Done	0	Write this bit when process KSVList Check interrupt routine. Write this '1' after PC check KSV FIFO list.	0
28~2F	An	63:0	Random number used at HDCP Authentication.	
30~37	VgenAn	63:0	Read only These 8 bytes are generated random number. To generate random number, see Reg1F[0]	
3B	BKSV [7:0]	7:0	Read only.	
3C	BKSV [15:8]	7:0	Read only.	
3D	BKSV [23:16]	7:0	Read only.	
3E	BKSV [31:24]	7:0	Read only.	
3F	BKSV [39:32]	7:0	Read only.	
40	BRI[7:0]	7:0	Read only.	
41	BRI[15:8]	7:0	Read only.	
42	BPj[7:0]	7:0	Read only.	
43	Bcaps[7:0]	7	HDMI_Reserved	
		6	HDCP Repeater capability.	
		5	KSV FIFO ready.	
		4	FAST. 1: the device supports 400KHz transfers.	
		3	reserved. must be zero.	
		2	reserved. must be zero.	
		1	1: HDCP 1.1 Features. support HDCP Enhanced encryption status signaling (EESS), Advance Cipher, and Enhanced Link Verification options.	
		0	1: Fast reauthentication. When set to 1, the receiver is capable of receiving (unencrypted) video signal during the session re-authentication. All HDMI-capable receivers shall be capable of performing the fast re-authentication even if this bit is not set. This bit does not change while the HDCP receiver is active.	
45	Bstatus[15:8]	7	reserved 0.	
		6	reserved 0.	
		5	Reserved for future possible HDMI used.	
		4	HDMI_Mode 1: HDMI mode. 0: DVI mode.	
		3	MAX_CASCADE_EXCEEDED Topology error indicator. 1: more than seven levels of video repeater have been cascaded together.	
		2:0	Three-bit repeater cascade depth.	
44	Bstatus[7:0]	7	1: more than 127 downstream devices or KSV fifo.	
		6:0	Total number of attached downstream string devices.	
46	Rauthenticated	7	R	
	RautheFailStatus	6:0	Fail Status for debug	

To start HDCP authentication, the action for the following steps are as described.

## A0 – Wait for active Rx

For starting the HDCP authentication, software must judge

1. Sink is a HDCP sink device
2. Sink have valid BKSv
3. (For HDMI requirement) Sink is HDMI device

Switch [DDC master to PC-Host](#), then [get BCaps](#) and [BStatus](#). If the BCaps exists and valid, then [get BKSv](#), check if BKSv contains 20 bits as '1' and the other 20 bits as '0', and check it is not revoked by source SRM (*check the HDCP specification, chap 3.*). If BStatus[12] = '1', the HDCP sink is in HDMI mode.

If the BKSv checking is valid and is a HDMI sink, then start HDCP authentication by the following steps:

1. Enable HDCP circuit by reg04[0] = '0'.
2. Generate a pseudo random number An by reg1F = 0x01 for a period time, then stop the cipher to fix the number.  
Read the eight bytes random number from reg30~reg37, then write them to reg28~reg2F.
3. Set reg20[1] = '1' if sink support HDCP 1.1 feature while BCaps[1] = '1'; and set reg20[0] = '1' to enable the HDCP.
4. Set reg22 = 0x00.
5. Set interrupt mask reg0A[2:0] = '000' to listen authentication done, authentication fail, and authentication wait for repeater KSV list checking. Set reg0C[4:2] = '111' and reg0E[0] = '1' to clear all HDCP interrupt status before HDCP authentication start.
6. To start hardware authentication, the DDC master should be changed to HDCP core. Set reg10 = 0x00.
7. Write any value (we usually write 0xFF) to reg21 to fire HDCP authentication, IT66121 will do A1~A3 automatically until it issues a interrupt with status responded in any bit of reg07[2:0] with value '1'.

Whenever int07[1] = '1' after HDCP authentication fired, the authentication is fail. If sink is a pure receiver, reset HDCP with reg04[0] = '1' and reg20 = '00', then restart the authentication; if sink is a repeater, set reg22 = 0x3, then set reg04[0] = '1', reg20 = '00' and reg22 = 0x00.

If sink is a receiver, after hardware exchange the KSV and computed the information successfully, reg47[7] will be '1' and int07[0] = '1' with interrupt.

If sink is a repeater, int07[2] will be '1' after the information exchanging and computation done successfully. Then the status will be.

Handling the state transition for A0 to A6 should be interrupt handler.

## A1 – Exchange KSVs

The KSV exchanging is done by hardware automatically.

If any interrupt occurs with int07[1] = '1', switch state to A0 and reset HDCP circuit.

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## A2 – Computations

The computations are done by hardware automatically.

If any interrupt occurs with int07[1] = '1', switch state to A0 and reset HDCP circuit.

## A3 – Validate Receiver

The validate receiver is done before authenticate start, thus it can be ignored.

If any interrupt occurs with int07[1] = '1', switch state to A0 and reset HDCP circuit.

## A6 – Test for Repeater

Off	Register Name	bit	Description	Default Value
<b>Interrupt Status</b>				
07	RInt_PktISRC2Stus	7	R, Reset by REG_ISRC2Clr	
	RInt_PktISRC1Stus	6	R, Reset by REG_ISRC1Clr	
	RInt_PktACPStus	5	R, Reset by REG_PktACPClr	
	RInt_PktNullStus	4	R, Reset by REG_PktNullClr	
	RInt_PktGenStus	3	R, Reset by REG_PktGenCr	
	RInt_KSVListChkStus	2	R, Reset by REG_KSVListChkClr	
	RInt_AuthDoneStus	1	R, Reset by REG_AuthenDoneClr	
	RInt_AuthFailStus	0	R, Reset by REG_AuthFailClr	

*Table Interrupt for Authentication*

Switch state to A6 if interrupt received with int07[0] = '1' or int07[2] = '1'. If sink is receiver only, the interrupt report authentication done successfully and direct switch state to A4; if sink is repeater, the interrupt with int07[2] = '1' will be received and need to wait for KSV list ready by polling BCaps. Switch the state to A8 and switch DDC master to PC-Host with reg10=0x01.

## A8 – Wait for Ready

On the state, software should keep polling BCaps with KSV FIFO Ready bit (BCaps[5] = '1'). If the time is out of 5 seconds after A6 without KSV FIFO ready, the authentication should be fail and turned to A0. Before fail it, reg22 should be 0x03 to turn off the state machine inner chip.

If BCaps[5] = '1', it means the KSV FIFO is ready. For some sink implementation, we suggest to wait 500 milliseconds after KSV FIFO ready, then switch state to A9.

## A9 – Read KSV List

While the KSV FIFO ready responded in BCaps[5] = '1', software should get KSV FIFO list via DDC command. The downstream count (not include the repeater itself) should be between 1 to 6.

To [get KSV FIFO list](#) with count = downstream × 5.

After get KSV FIFO list, do SHA-1 encoding with KSV List, BStatus, and M0 in 8 bit value which computed by HDCP hardware cipher. It will get a 20-byte V from the SHA-1 encoding.

Reg	Name	Bit	Description	Default Value
50	SHASel[2:0]	2:0	See SHA_Rd_ByteX registers below	
51	SHA_Rd_Byte1[7:0]	7:0	V0h[7:0] when SHASel="000" V1h[7:0] when SHASel="001" V2h[7:0] when SHASel="010" V3h[7:0] when SHASel="011" V4h[7:0] when SHASel="100" Mi[7:0] when SHASel="101"	
52	SHA_Rd_Byte2[7:0]	7:0	V0h[15:8] when SHASel="000" V1h[15:8] when SHASel="001" V2h[15:8] when SHASel="010" V3h[15:8] when SHASel="011" V4h[15:8] when SHASel="100" Mi[15:8] when SHASel="101"	

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53	SHA_Rd_Byte3[7:0]		V0h[23:16] when SHASel="000" V1h[23:16] when SHASel="001" V2h[23:16] when SHASel="010" V3h[23:16] when SHASel="011" V4h[23:16] when SHASel="100" Mi[23:16] when SHASel="101"	
54	SHA_Rd_Byte4[7:0]	7:0	V0h[31:24] when SHASel="000" V1h[31:24] when SHASel="001" V2h[31:24] when SHASel="010" V3h[31:24] when SHASel="011" V4h[31:24] when SHASel="100" Mi[31:24] when SHASel="101"	
55	Aksv_Rd_Byte5[7:0]	7:0	Mi[39:32] when SHASel="000" Mi[47:40] when SHASel="001" Mi[55:48] when SHASel="010" Mi[63:56] when SHASel="011"	

The 64bit M0 value is get from

```
reg50 = 0x05 ; M0[7:0] = reg51 ;  
reg50 = 0x05 ; M0[15:8] = reg52 ;  
reg50 = 0x05 ; M0[23:16] = reg53 ;  
reg50 = 0x05 ; M0[31:24] = reg54 ;  
reg50 = 0x00 ; M0[39:32] = reg55 ;  
reg50 = 0x00 ; M0[47:40] = reg55 ;  
reg50 = 0x00 ; M0[55:48] = reg55 ;  
reg50 = 0x00 ; M0[63:56] = reg55 ;
```

Then get the V' from sink, if the V' is equal to V in all bytes, the authentication is done.

If anything error occurs, set reg22 = 0x3 to cancel the state machine for repeater checking, then reset HDCP circuit with reg04[0] = '1', and switch the state to A0 for authentication fail.

If all items are successful, set reg10 = 0x00 for switching DDC master to HDCP core, and set reg22 with 0x01 for continuing the authentication, and switch state to A4 for successfully authenticated.

## A4 – Authenticated

In this state, HDCP is authenticated and the output data should be encrypted. We suggested to set reg0A[1] = '1' to turn off the interrupt for authenticated done, by ignoring the handling for each authenticated successfully by Ri==Ri' check of A5.

## A5 – Link Integrity Check

For each 128 frame HDCP source should collect next Ri to do link integrity check. IT66121 does it automatically after HDCP authentication fired, and will issue a authentication done interrupt if reg0A[1] is '0' when link integrity check successfully, and received a fail interrupt in reg07[0] if reg0A[0] = '0'. Whenever received this interrupt, HDCP source state should switch back to A0.

## Reset HDCP

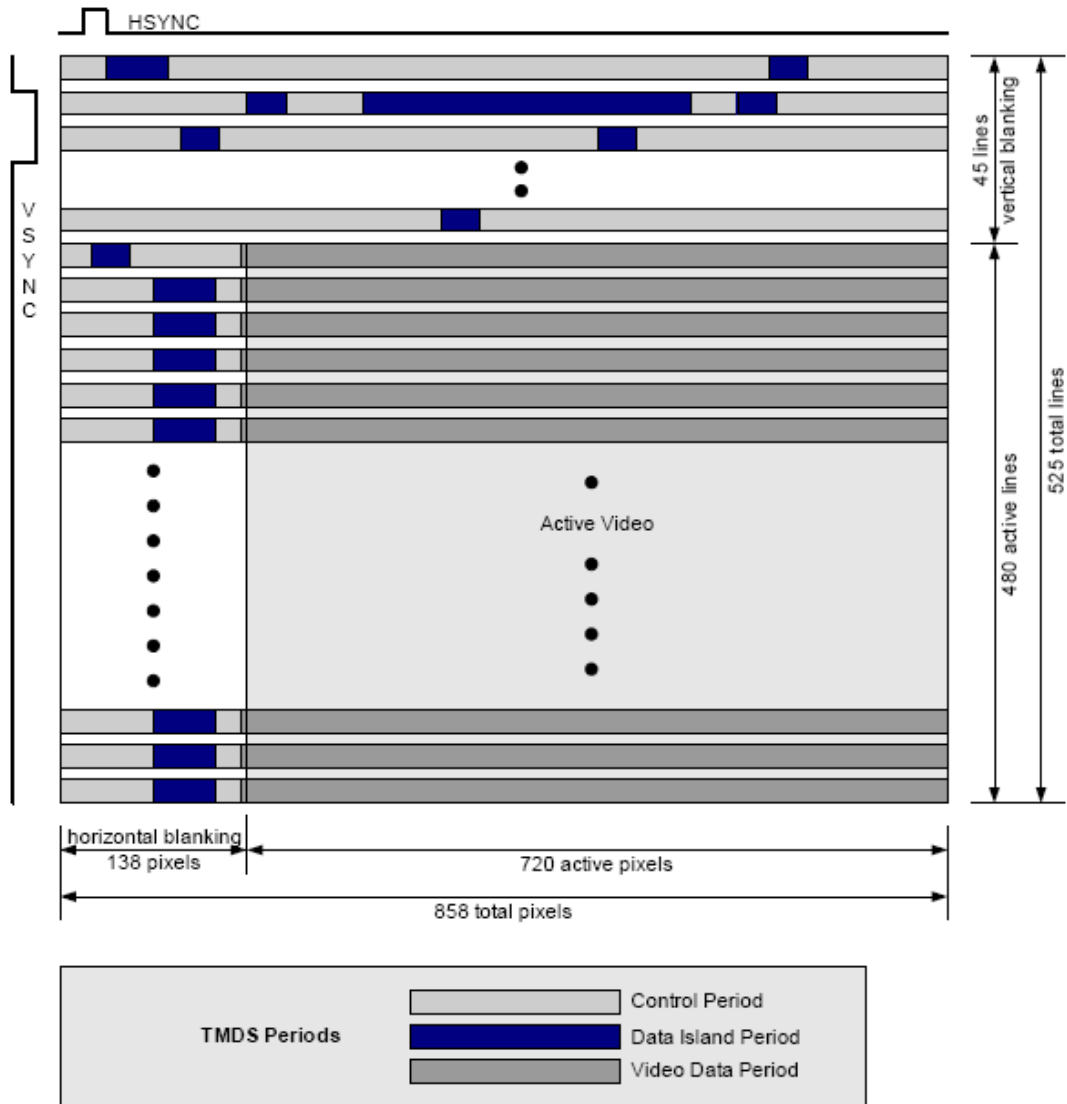
To reset HDCP, reg04[0] = '1', reg20 = '0'. If state is in A6~A9, reg22 should write 3 at first, then write to zero.

## Encryption

IT66121 enabled output encryption while HDCP done, and blanked while HDCP fail when HDCP is enabled and reg20[0] = '1'. If reg20[0] = '0', HDCP cannot start.

## Chap 9 HDMI Infoframe/Package

Unlike DVI mode, the TMDS link contains audio sample packets (programmed with IT66121 audio registers) and auxiliary data in data island period. The auxiliary data describe the video type, color information, audio auxiliary information, mute and other informations. As following figure (refer to HDMI specification 1.3 section 5.1.2)



*Informative Example: TMDS periods in 720x480p video frame*

Before enabling the HDMI package on IT66121, the mode should be switched to HDMI mode with `regC0[0] = '1'`.

Reg	Register Name	bit	Definition	Default Value
C0	REGHDMIMode	0	Set TX Mode '0': DVI mode '1': HDMI mode	0

The programming of HDMI auxiliary information is described in following sections.



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## HDMI Packet and CEA861/D Infoframe

An HDMI packet includes a 24-bit packet header, and a 28 bytes length packet body. A packet header includes an 8-bit Packet Type and 16 bits of packet-specific data.

The packet header format is as following table:

Byte / Bits#	7	6	5	4	3	2	1	0
HB0	Packet Type							
HB1	Packet-specific data							
HB2	Packet-specific data							

A sink shall be able to receive, with no adverse effects, any packet defined in the HDMI 1.0 spec including any InfoFrame packet with an InfoFrame Type defined in CEA861/D.

The packet type of HDMI spec defined as the following table:

Packet Type Value	Packet Type	
0x00	NULL Packet	
0x01	Audio Clock Regeneration (N/CTS)	
0x02	Audio Sample (Include LPCM and IEC 61937 compressed format)	
0x03	General Control	
0x04	ACP Packet	
0x05	ISRC1 Packet	
0x06	ISRC2 Packet	
0x0A	Gamut Metadata Packet	
0x80+ Infoframe Type	0x81	Vendor Specific Infoframe
	0x82	AVI Infoframe
	0x83	Source Product Descriptor (SPD) InfoFrame
	0x84	Audio InfoFrame
	0x85	MPEG Source InfoFrame

The relate information of each packet specification are defined in CEA861/D specification for infoframe and in HDMI 1.3 specification with the other packet. The enabling registers of HDMI packets are in RegC1~RegD0, and see the following section description.

## General Control Package

General control packet defined in HDMI 1.1 spec section 5.3.6 controls the output color depth, Pixel Packing Phase, and AVMute set/clear. IT66121 automatically handle the pixel packing phase, and send the color depth and AVMute status set in regC1 as following table described.

Reg	Register Name	bit	Definition	Default Value
C1	REGBlueScrMute	1	Set Blue screen output when AVMute='1'	0
	REGAVMute	0	Set AVMute '0': not AVMute '1': AVMute	1
C6	REGPktGenCtrlRpt	1	Repeat General Control packet '0': send once '1': one for each field	0
	REGPktGenCtrlEn	0	Enable General Control packet '0' : disable '1': enable	0

To send regC6[0] = '1' will enable GCP once if regC6[1] = '0', and sends frequently while regC6[1] = '1'.

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## Infoframe

The infoframe defined in CEA861/D which implemented in HDMI are as following

Byte / Bit #	7	6	5	4	3	2	1	0
HB0	1	Info Frame ID in CEA861/D						
HB1	Infoframe Version							
HB2	0	0	0	Infoframe Length				
PB0	Checksum							
PB1	Data byte 1 defined in CEA861/D nframe							
PB2	Data byte 2 defined in CEA861/D Infoframe							
PB3 .. PB26	-							
PB27	Data byte 27 defined in CEA861/D Infoframe							

The checksum of infoframe is the two's complement of byte summary HB0~HB2 and PB1~PB27.

$$PB0 = 0 - \left( \sum_{i=0}^2 HBi + \sum_{i=1}^{27} PBi \right)$$

IT66121 provides determined registers for AVI Infoframe, audio infoframe, and Mpeg source infoframe identically, and general purpose registers in reg138~reg156 controlling with regC9.

## AVI Infoframe

IT66121 provides AVI infoframe with version 2 in reg158~reg165.

Reg	Register Name	bit	Definition	Default Value
CD	REGPktAVIInfoRpt	1	Repeat AVI InfoFrame packet '0': send once '1': one for each field	0
	REGPktAVIInfoEn	0	Enable AVI InfoFrame packet '0': disable '1': enable	0

AVI Infoframe controlling registers is regCD with enabling bit in regCD[0], and repeating bit for each field while regCD[1] = '1'.

The infoframe data byte defined in following byte, which checksum in PB0 is defined in reg15D, and only 13 bytes valid in AVI infoframe.

AVI Packet					
Reg	Register Name	bit	Definition	Default Value	PB Value
158	REGPktAVIInfoV[1:0]	6:5	Output HDMI Color Space 00 – RGB444 mode 01 – YCbCr422 mode 10 – YCbCr444 mode		1
	REGPktAVIInfoA	4			
	REGPktAVIInfoB[1:0]	3:2			
	REGPktAVIInfoS[1:0]	1:0			
159	REGPktAVIInfoC[1:0]	7:6			2
	REGPktAVIInfoM[1:0]	5:4			
	REGPktAVIInfoR[3:0]	3:0			
15A	REGPktAVIInfoITC	7			3
	REGPktAVIInfoEC[2:0]	6:4			
	REGPktAVIInfoQ[1:0]	3:2			
	REGPktAVIInfoSC[1:0]	1:0			
15B	REGPktAVIInfoVIC[6:0]	6:0			4
15C	Reserved	7:4		0000	5
	REGPktAVIInfoPR[3:2]	3:2		0	
	REGPktAVIInfoPR[1:0]	1:0	Set the pixel repetition if reg59[4] = '0' 00 – no repetition 01 – 2X repetition	0x0	

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			11 – 4X repetition otherwise – undefined	
15D	REGPktAVIInfoSUM[7:0]	7:0	The checksum of infoframe	0
15E	REGPktAVIInfo06PB[7:0]	7:0		6
15F	REGPktAVIInfo07PB[7:0]	7:0		7
160	REGPktAVIInfo08PB[7:0]	7:0		8
161	REGPktAVIInfo09PB[7:0]	7:0		9
162	REGPktAVIInfo10PB[7:0]	7:0		10
163	REGPktAVIInfo11PB[7:0]	7:0		11
164	REGPktAVIInfo12PB[7:0]	7:0		12
165	REGPktAVIInfo13PB[7:0]	7:0		13

The checksum in reg15D = 0 - (sum of (reg158~reg15C) + sum of (reg15E~reg165) + 0x82 + 2 + 0x0D).

## Audio Infoframe

Audio infoframe defined in CEA861/D can be enabled by regCE[0] and send repeating with regCE[1] = '1'.

Reg	Register Name	bit	Definition	Default Value
CE	REGPktAudInfoRpt	1	Repeat Audio InfoFrame packet '0': send once '1': one for each field	0
	REGPktAudInfoEn	0	Enable Audio InfoFrame packet '0': disable '1': enable	0

IT66121 provides audio infoframe with version 1 only in reg168, reg169, reg16B, and reg16C, and the other six byte defined in CEA861/D are assumed as zero. Checksum byte is defined in reg16D.

Audio InfoFrame Packet					
Reg	Register Name	bit	Definition	Default Value	PB
168	REGPktAudInfoCC[2:0]	2:0	Channel Number 000 Refer to Stream Header 001 2 channel 010 3 channel 011 4 channel 100 5 channel 101 6 channel 110 7 channel 111 8 channel		1
169	REGPktAudInfoSF[2:0]	4:2	Sampling Frequency 000 Refer to stream header 001 32KHz 010 44.1KHz(CD) 011 48KHz 100 88.2KHz 101 96KHz 110 176.4KHz 111 192KHz		2
16B	REGPktAudInfoCA[7:0]	7:0	refer to the CEA861/D definition.	0x0	4
16C	REGPktAudInfoDM	7	DM_INH Down-mix Inhibit Flag '0' Permitted or no information about any assertion of this '1' Prohibited		5
	REGPktAudInfoLSV[3:0]	6:3	Level shift values of db		
16D	REGPktAudInfoSUM[7:0]	7:0			0

reg16D = 0 – (reg168+reg169+reg16B+reg16C+0x84+0x01+0x0A).

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## MPEG InfoFrame

Mpeg source infoframe is enabled in regD0[0] and send repeating on each field when regD0[1] = '1'.

Reg	Register Name	bit	Definition	Default Value
D0	REGPktMpgInfoRpt	1	Repeat MPEG InfoFrame packet '0': send once '1': one for each field	0
	REGPktMpgInfoEn	0	Enable MPEG InfoFrame packet '0': disable '1': enable	0

The data byte definition is in the following table, note the reg18A is not pure mpeg definition:

Reg	Name	bit	Definition	PB sequence
18A	REGPktMpgInfoFR	0	DB5[4]	5
	REGPktMpgInfoMF[1:0]	2:1	DB5[1:0]	
18B	REGPktMpgInfo01PB[7:0]	7:0	MB#0 (Mpeg Bit Rate Hz )	1
18C	REGPktMpgInfo02PB[7:0]	7:0	MB#1	2
18D	REGPktMpgInfo03PB[7:0]	7:0	MB#2	3
18E	REGPktMpgInfo04PB[7:0]	7:0	MB#3	4
18F	REGPktMpgInfoSUM[7:0]	7:0	checksum	0

The checksum in reg18F = 0 – (reg18B+reg18C+reg18D+reg18E) - (reg18A[0] \* 16) - (reg18A[2:1])

## Vendor Specific Registers

D2	REGPkt3DInfoRpt	1	Repeat 3D InfoFrame packet '0': send once '1': one for each field	0
	REGPkt3DInfoEn	0	Enable 3D InfoFrame packet '0': disable '1': enable	0
<b>Vendor Specific InfoFrame Packet</b>				
180	REGPkt3DInfo04PB[7:0]	7:0		XX
181	REGPkt3DInfo05PB[7:0]	7:0		XX
182	REGPkt3DInfo06PB[7:0]	7:0		XX
183	REGPkt3DInfoSUM[7:0]	7:0	checksum = 0 – (0x81+1+len(5 or 6)+0x03+0x0C+reg180+reg181) If 3D format > 7, len = 6, otherwise = 5.	XX

IT66121 provide 3D package registers in reg180, 181 and 182, which checksum in the register 183 and enable bit in regD2.

## SPD/ ISRC1/ISRC2/General Purpose

The registers named “NULL Packet” in IT66121 are for general purpose, which is enabled by regC9[0] and sent each field once when regC9[1] = '1'.

Reg	Register Name	bit	Definition	Default Value
C9	REGPktNullRpt	1	Repeat Null packet '0': send once '1': one for each field	0
	REGPktNullEn	0	Enable Null packet '0': disable '1': enable (mutual exclusive with ACP/ISRC1/ISRC2 packet)	0

The layout in reg138~reg156 is fully compatible to the HDMI packet format. There are three bytes of header and 28 bytes of packet body. For those types sharing these registers should enable exclusive. For software implement, to disable the packet with regC9[0], then write the content, then enable it again to implement multiple package types using these registers.

Reg	Name	Bit	Definition	
138	REGPktNull0Hdr[7:0]	7:0	HDMI Packet HB0	
139	REGPktNull1Hdr[7:0]	7:0	HDMI Packet HB1	

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13A	REGPktNull2Hdr[7:0]	7:0	HDMI Packet HB2	
13B	REGPktNull00PB[7:0]	7:0	HDMI Packet PB0	
13C	REGPktNull01PB[7:0]	7:0	HDMI Packet PB1	
~	~		~	
155	REGPktNull26PB[7:0]		HDMI Packet PB26	
156	REGPktNull27PB[7:0]	7:0	HDMI Packet PB27	

## ACP register

ACP packet can be programmed with regCA[0] = '1' and sending frequently with regCA[1] = '1'.

Reg	Register Name	bit	Definition	Default Value
CA	REGPktACPRpt	1	Repeat ACP packet '0': send once '1': one for each field	0
	REGPktACPEn	0	Enable ACP packet '0': disable '1': enable	0

Above registers are enable the ACP packet and the detail registers are enabled in the following registers.

ACP InfoFrame Packet				
16E	REGPktACP01HB[7:0]	7:0	Bit2:0→ REGPktACPTYPE[2:0] Content protection type 000: Generic Audio 001: IEC60958-Identified Audio 010: DVD-Audio 011: Super Audio CD 1XX Reserved	XX
16F	REGPktACP00PB[7:0]	7:0	ACP Packet Byte00	XX
170	REGPktACP01PB[7:0]	7:0	ACP Packet Byte01	XX
171	REGPktACP02PB[7:0]	7:0	ACP Packet Byte02	XX
172	REGPktACP03PB[7:0]	7:0	ACP Packet Byte03	XX
173	REGPktACP04PB[7:0]	7:0	ACP Packet Byte04	XX
174	REGPktACP05PB[7:0]	7:0	ACP Packet Byte05	XX
175	REGPktACP06PB[7:0]	7:0	ACP Packet Byte06	XX
176	REGPktACP07PB[7:0]	7:0	ACP Packet Byte07	XX
177	REGPktACP08PB[7:0]	7:0	ACP Packet Byte08	XX
178	REGPktACP09PB[7:0]	7:0	ACP Packet Byte09	XX
179	REGPktACP10PB[7:0]	7:0	ACP Packet Byte10	XX
17A	REGPktACP11PB[7:0]	7:0	ACP Packet Byte11	XX
17B	REGPktACP12PB[7:0]	7:0	ACP Packet Byte12	XX
17C	REGPktACP13PB[7:0]	7:0	ACP Packet Byte13	XX
17D	REGPktACP14PB[7:0]	7:0	ACP Packet Byte14	XX
17E	REGPktACP15PB[7:0]	7:0	ACP Packet Byte15	XX
17F	REGPktACP16PB[7:0]	7:0	ACP Packet Byte 16	XX